NOTE TO USERS

Quality Factor Enhanced Coupled Inductor Structures and their RF Applications

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Abstract

The beauty of wireless connection through radio frequency (RF), for both communications and data transmission, has been motivating research work in this field ever since Guglielmo Marconi successfully sent the first radio signal cross the Atlantic in 1901. Nowadays, increasing demand for bandwidth has pushed new standards in the wireless domain constantly towards higher operating frequencies and higher level of integration. All those standards put strong emphasis on low power, low voltage, low cost, and high performance.

Although, traditionally, silicon based bipolar technologies (BJT) dominated radio frequency integrated circuit (RFIC) designs and fabrication, due to their superior RF performance (e.g. high transconductance, low noise, etc.), recent technology progress in submicron complementary metal oxide semiconductor (CMOS) has made it one of the most comparative alternatives for the giga Hertz range RFIC designs. Beyond this progress in performance, the CMOS technology also attracts designers for its capability of integrating analog RF front-ends and digital base-band signal processing circuitry on one die. This will directly lower the cost of the product. More and more RF designs have been realized using modern CMOS technologies, and this trend is continuing.

This thesis is concerned with one of the key passive components in RFIC design, namely on-chip inductors. Complete design equations, EM simulation and data processing procedures have been established and demonstrated for 0.18um and 0.13um CMOS technologies. Following these procedures, several inductors have been designed and fabricated. A low noise amplifier (LNA) working at 6 GHz has been implemented using the TSMC

0.18 standard CMOS technology, and the prototype chip was successfully tested.

As an attempt to build higher performance on-chip inductors, a new quality factor enhanced coupled inductor structure is proposed and discussed. Through intertwining and coupling two inductors, and making use of the positive mutual inductance built up between them, a 56% increase in quality factor has been achieved. Detailed design guidelines and methodologies are presented. Measurement and simulation results of the fabricated prototypes demonstrated the accuracy and effectiveness of the work proposed.

VCO and LNA designs using the coupled structures are presented. Simulation results also demonstrate the performance improvement resulting from using coupled structures, compared to using optimized standard inductors.

Résumé

Les connections sans fils utilisant les radiofréquences (RF) pour les transmissions de données et pour les systèmes de télécommunications ont poussé les chercheurs à faire un travail colossal dans ce domaine depuis que Gugliemo Marconi a transmis avec succès le premier signal radio par-dessus l'Atlantique en 1901. De nos jours, la demande croissante de bande passante pour les systèmes de télécommunications et pour les transmissions de données a encouragé l'implantation de nouveaux standards pour les communications sans fils, dans le but de permettre des transmissions à des fréquences plus élevées et d'améliorer le niveau d'intégration des circuits. Tous ces standards imposent la conception de circuits RF avec des performances supérieures opérant à de basses consommations d'énergie et à de bas voltages, tout en optimisant le prix de fabrication.

Traditionnellement, les circuits RF ont été intégrés dans les technologies bipolaires (BJT) car elle offrent des performances RF supérieures aux autres technologies disponibles (une meilleure transconductance, un bas niveau de bruits, etc.). Cependant, les progrès récents dans la technologie submicronique de métal-oxyde-semiconducteur complémentaire (CMOS) ont fait d'elle la meilleure alternative pour l'intégration de circuits RF opérant à plusieurs Gigahertz. De plus, les designers de circuits RF apprécient énormément la technologie CMOS, car elle offre, avec une facilité remarquable, l'intégration des systèmes analogues frontaux des receveurs RF et des processeurs des signaux digitaux de la bande de base, et ce sur la même puce. Ceci a pour effet de diminuer le prix de fabrication des receveurs/transmetteurs RF. Grâce à tous ces avantages, de plus en plus de designers optent pour la technologie CMOS.

Cette thèse étudie en détails un des éléments passifs les plus importants dans les circuits RF : les inducteurs sur puce. Leurs paramètres dans différentes technologies, des équations de design et des procédures de simulation EM et ont été établis dans les technologies CMOS 0.18μm et 0.13μm. Plusieurs inducteurs ont été créés et simulés. Ils ont aussi été utilisés pour concevoir, dans la technologie standard CMOS 0.18μm offerte par TSMC, un amplificateur à bas bruits (LNA) opérant à 6GHz. Une puce prototype a été fabriquée et testée au laboratoire avec succès.

Une tentative de construire des inducteurs sur puce avec de meilleures performances a été étudiée. Dans le but d'améliorer le facteur de qualité, un inducteur avec une structure

couplée est proposé. En couplant deux inducteurs et en utilisant les inductances mutuelles établies entre eux, 56% d'amélioration dans le facteur de qualité a été obtenu.

Des suggestions de design et différentes méthodologies sont présentées. Des résultats expérimentaux et de simulations des prototypes fabriqués prouvent la précision et l'efficacité des méthodes d'amélioration du facteur de qualité proposées.

Un oscillateur hyperfréquences commandé en tension (VCO) et un LNA qui utilisent cette structure de couplage des inducteurs ont été conçus. Les résultats de simulation démontrent l'efficacité des méthodes suggérées.

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Many people shared my graduate education as supervisor, friends, and colleagues.

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CHAPTER 1

Introduction

The rising demand for low-cost radio frequency integrated circuits (RFIC) has generated tremendous interest in on-chip passive components. Compared to resistors and capacitors, which currently have several integrated options, with most implementations being easy to model and implement, considerable effort has gone into the design and modeling of on-chip inductors, of which the most practical options are bond wires and planar spiral geometries. Although bond wires permit a high quality factor to be achieved, with typical values in the 20-50 range [1], their inductance values are constrained and can be sensitive to production fluctuations. On the other hand, planar spiral inductors have limited quality factors. However, the inductance of the structure can be well defined over a broad range of process variations. Thus, planar spiral inductors have become essential elements of communication circuit blocks, such as voltage controlled oscillators, low noise amplifiers, mixers and intermediate frequency filters [2] [3].

Among all possible geometry designs, square spirals are very popular because of the ease of their modeling and layout. However, other polygonal spirals have also come to use in circuit designs recently. Polygons with more than four sides are now used to improve the design performance. Among these designs, hexagonal and octagonal inductors are used most widely. To facilitate the use of such components, significant work has been made to model spiral inductors [4][5]. The most accurate and reliable solution for on-chip spiral structures would be based on Maxwell's equations. Through the use of a three dimensional finite element simulator such as MagNet, very accurate numerical solutions may be

obtained [6]. Usually, 3-D simulators are computationally intensive and require long processing times. This method is for design verification by prudent designers using their own tools. However, with the progressing computation power nowadays, numerical computation based solutions are taking less and less time. At the same time, more and more dedicated EM simulation software and design tools are being developed and used, such as ADS Momentum, Ansoft HFSS, and Sonnet, etc. RF designers now give more and more attentions to EM simulations at the design stage, instead of using it as a post verification tool. Together with the increase of the computational capability, progress in the modeling and analysis technologies also help designers to get accurate results in shorter time. The Greenhouse method [7], which offers sufficient accuracy and moderate speed, is one of the common technologies used. However, designers using the Greenhouse method may also find it cumbersome to the initial design stages, due to its inability to provide final inductor design parameters directly from specifications. Research work involving this technology are reported in [4][8].

1.1 Motivations and State-of-the-Art Inductor Design Technologies

With all the progress in all design aspects, designers can now build specified inductors quickly and accurately. However, there is one thing that never changed since on-chip inductors have been introduced into RF designs, that is the low quality factors of the structures. Compared to traditional off-chip or discrete component inductors, which can have very high quality factors, such as the silver coated copper coils, the highest quality factor for on-chip monolithic inductors that has been reported and used in common silicon based RF circuit designs in the 2 to 6GHz range, is in the range of Q=15 to 20. Table 1.1 lists some of the published inductors realized by traditional planar spiral technologies. Quality factors are also function of the operating frequency of the circuit, the inductance, and even how the inductors are used, e.g. differentially driven, single ended, etc. As one of the most important design factors that intensively affect the performance of the RF designs, such as

Table 1.1: Planar spiral inductors for RF circuits

References	L [nH]	Q*	Q_{Max} @ Freq [GHz]	F_{self_res}**[GHz]
J.Lin[9]	6.0	15	15 @ 2.5	8.0
A.M.Niknejad[10]	3.0	4.5	6.7 @ 4.9	-
	9.0	3.5	3.5 @ 2.5	-
J.A.Power[11]	3.0	8.5	9.5 @ 5	12.0
K. Schimpf[12]	6.5	8.0	12 @ 3.1	8.0
C.P.Yue[13]	-	4.5	5.0 @ 1.5	6.5
S.F.Zhou[14]	16.2	3.0	3.3 @ 1.6	4.6

* Quality factor measured at 2GHz.
** Self resonance frequency

the gain/power ratio of low noise amplifiers (LNAs), and the phase noise of voltage controlled oscillators (VCOs), high quality factor inductors have been the center of research for a long time. Many researchers are exploring different methods to build high performance on-chip inductors. Some designers focused on structure geometries which do not request extra processing stages. These approaches include using multi-metal layers to increase the effective thickness of the spiral [15], connecting multi-metal layer spirals in series to reduce the area of the inductors [16][17], and fabricating inductors on high resistivity substrates [9]. Other designers are using methods which utilize features in modern processing technologies, which include using thick oxide or floating inductors to isolate

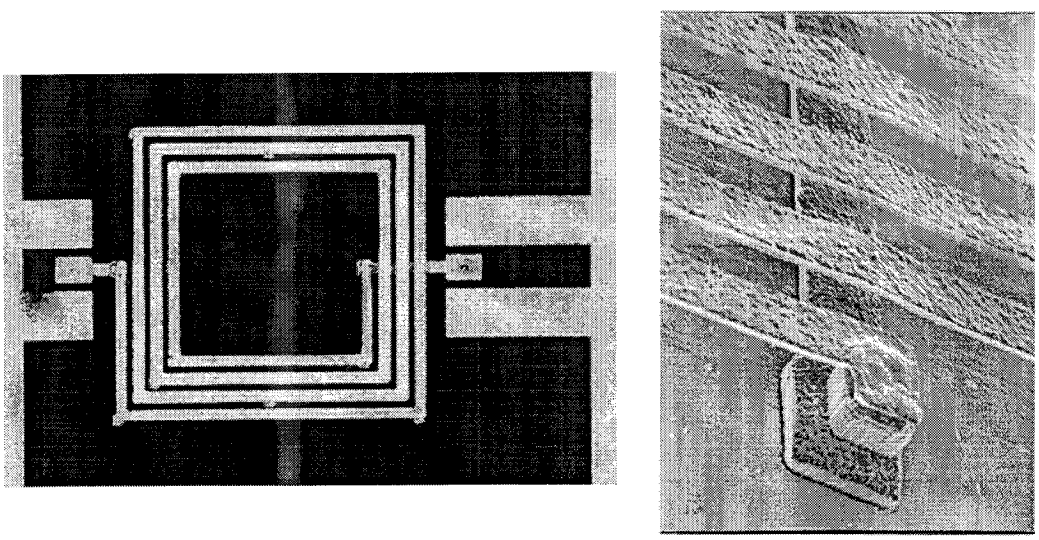


Fig. 1.1: Suspended spiral air core inductor which has been designed to have the inductance value of 9 nH, with quality factor of Q=3.5 at 2.5GHz

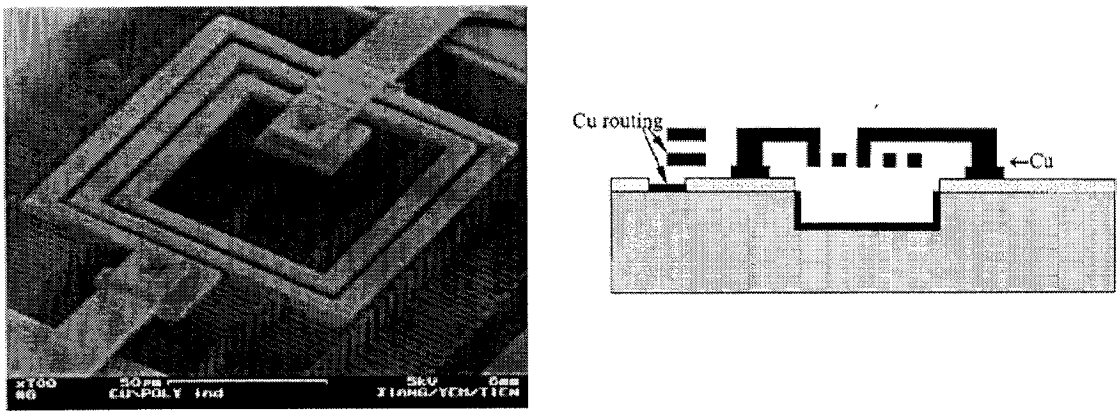


Fig. 1.2: The substrate under the inductor structure has been removed. The quality factor is up to Q=36 at 5.2GHz, with an inductance value equal to 2.3 nH has been achieved.

the structure from the lossy substrate (Fig. 1.1 [18]), and removing the substrate underneath (Fig. 1.2 [19]).

Recent developments in Micro-Electro Mechanical Systems (MEMS) suggest that hybrid technologies, where micromachined passive devices and integrated electronics reside on a single chip, will be another approach to realize high performance RF circuits and will be widely accepted in the future, e.g. [20]. Commercial products such as pressure sensors in air-bag systems are readily available. Inductors realized in this technology could have very high quality factors, compared to monolithic spirals in silicon based ICs. High quality fac-

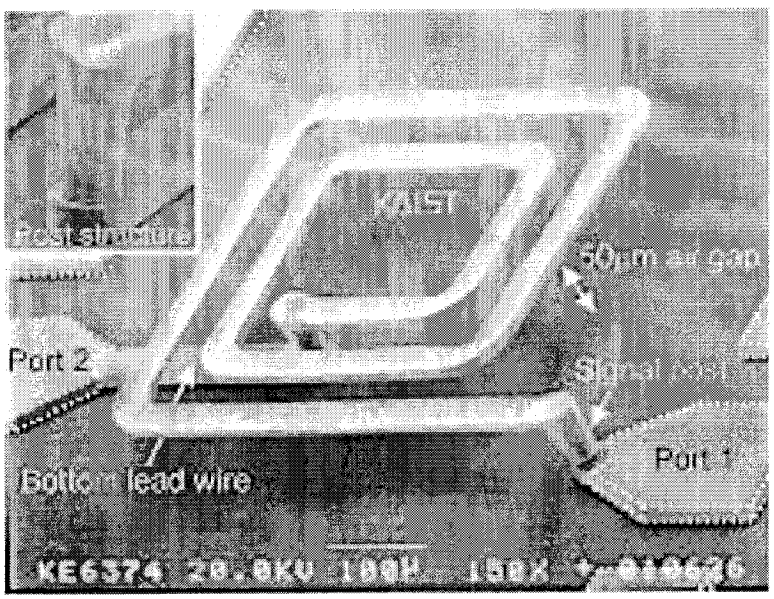


Fig. 1.3: SEM microphotograph of the suspended MEMS spiral inductor fabricated on standard silicon by using a new CMOS-compatible surface micromachining technology [25]. The white dotted line illustrates the open-pad.

tors ranging from 30 to 80 at 2 GHz have been obtained using this technology [21]-[24]. Fig. 1.3 [25] shows one inductor design built in a MEMS technology, with inductance value equal to 1.38 nH and quality factor up to 70 at 6GHz. With those benefits, designers should still be aware of some of the difficulties of MEMS technologies in mind. MEMS components are often sensitive to the change and influence of the outer environment, such as temperature and vibrations. Moreover, MEMS are not compatible with main stream silicon based IC design procedures and technologies. Finally, MEMS components are also facing difficulties in modeling and characterization. Nevertheless, MEMS is a prospective technology in high performance RF circuit design, and more mature and reliable structures and design guidelines are expected to be coming into sight in the near future.

Compared to those "hard" approaches discussed above, which focus on achieving high quality factors for the inductors using new technologies, "soft" solutions emphasizing obtaining higher performance through proper and innovative usage of the inductors are also very active. In [26], Danesh and Long proposed and proved that a differentially driven inductor will have higher quality factor compared to a single ended one. Based on this idea, the center tapped transformer structure has been widely used, and became an attractive and popular approach in LNA and differential VCO designs. However, its single ended nature (center tap) may restrict its applicability in more generic circuit designs. Some other publications reported a specially designed signal driving approach in using inductors which could boost the quality factor up to 1000 [29], but the signal driving mechanism of this technology also limits its applicability only to very few applications.

1.2 Work in this Thesis and Outline

1.2.1 Work in this Thesis

One thing that designers already know and are always trying to make use of for inductor designs is the mutual inductance. When putting two parallel conductive segments close to each other, and depending on the phase of the currents, mutual inductance can be built up between these two conductors. The effective inductance value of each of the two conduc-

tive segments will be its self-inductance plus the mutual inductance. Maximum positive mutual inductance will be obtained when in-phase currents flow in the conductors. A multi looped inductor structure is one of the examples utilizing mutual inductance in its construction. As positive mutual inductance is added, the same inductance value could be realized using a smaller structure, shorter conductive segments, and, for on-chip inductors, less chip area. All these factors will help to lower the energy loss and increase the quality factor.

The main focus of this thesis is to use standard CMOS technology to implement high quality factor inductors for RF circuit designs, based on an extension of this idea. A coupled inductor structure will be proposed in this thesis in which, compared to a single inductor, mutual inductance will be built up and shared by "sub-inductors" in a coupled structure. Positive mutual inductance will be maximized through proper design and layout of the structure, to ensure in phase signal currents are obtained. Higher quality factors will be achieved by adding the positive mutual inductance to the effective self-inductance while keeping the losses low.

1.2.2 Related Publication and Presentations

Part of the research work done for this thesis is compiled and published in the paper [27]:

H. Zhang, T. K. K. Tsang, and M. N. El-Gamal, "Simple and Accurate Modeling of Q-Enhanced Transformer-Coupled Monolithic Inductors for Silicon RF IC's and their Applications", Workshop on Wireless Circuits and Systems (WoWCAS), Vancouver May 2004.

Presentation of the research work of this thesis has also been given in Micronet Annual Workshop 2004, April 2004, in Ottawa [28].

1.2.3 Thesis Outlines

Chapter 2 begins with an overview of the IC fabrication and metallization technology. Bases of on-chip inductor design and analysis equations are then discussed in detail.

Guidelines which would be useful for designers starting their inductor designs are then listed. Being the bridge connecting geometry design and circuit simulations, π-models are widely used and accepted in RF designs and are worth some discussion. As the main simulation tool used for on-chip design and verification, the ADS EM simulator Momentum is thoroughly presented in the later half of chapter 2. Details including substrate modeling, metallization modeling, simulation setup and data extraction are discussed. One successful CMOS LNA working at 6GHz which uses inductors designed following the design procedures discussed in this chapter is presented at the end.

In chapter 3, the concept of coupled inductor structures is proposed. A systematic design strategy is then presented and discussed. Wheeler's formula which serves as an important calculation equation at the initial stage of the design is addressed. Based on the EM simulation procedure discussed in chapter 2, coupled inductor structures could be simulated and verified as a four port network in Momentum, using the same substrate and metallization models. To quantify the design using design specifications such as effective inductance, self-inductance, coupling coefficient, mutual inductance and quality factors, a data processing and extraction procedure is proposed. This procedure will transform four port S-parameters from EM simulations into a differentially driven effective inductance and quality factor for each of the inductors in the coupled structure. With a four-port Vector Network Analyzer (VNA), this procedure could also serve to characterize fabricated prototypes. Coupled structures fabricated using a standard CMOS p13 technology and its measurement results are presented as the conclusion of this chapter.

In chapter 4, application examples using the coupled structures are presented with simulation results. Guidelines for differential RF VCO and LNA are addressed. Two VCO designs working at 2.4GHz and 6GHz are designed. Simulation results show distinctive progress in terms of phase noise over the same designs using standard inductors. For the 6GHz differential LNA design, coupled inductor structures are used as input gate matching inductors which, in most cases, are realized using off chip components for their high quality factors. Benefits of using coupled structures are demonstrated by comparing the noise performance to that of the same LNA designed using optimized standard inductors for gate matching. Also, simulation results show that, although high quality matching will

not increase the intrinsic forward gain of the LNA, it will increase the amplifier's total gain by minimizing the signal loss in the matching network.

Finally, in chapter 5, the thesis concludes with a summary of the work done and the results obtained.

CHAPTER 2

On-Chip Inductor Design

In this chapter, on-chip inductor design will be discussed. Being the starting point, metallization and standard CMOS processing technology will be described first. Basic theories for on-chip inductor designs and calculations will then be discussed. This includes microstrip line self-inductance, mutual inductance, self-resonance effect, losses, quality factor and modeling, etc. With the progressing computer numerical calculation capabilities and modeling technologies, faster and accurate EM simulations become even more practical then ever, and are now being accepted and used by more and more designers. This chapter will give detailed design procedures of using the ADS Momentum simulator for on-chip inductor designs. The chapter will conclude with a successful LNA design using optimized on-chip inductors.

2.1 CMOS IC Technology and Metallization

The first step in realizing a microcircuit is to produce a defect-free, single-crystalline, lightly doped wafer. To realize such a wafer, one starts by creating highly purified single-crystalline silicon using *Czochralski method* [30]. In this method, pure poly crystalline silicon is first melted and allowed to cool. As it cools, a single-crystalline ingot is slowly pulled and turned from the molten silicon. The pull rate and speed of rotation determine the diameter of the crystalline rod. Normally, heavily doped silicon is added to the melt

before the single-crystalline ingot is pulled. The reason this heavily doped silicon is added is because the doped silicon diffuses through the molten silicon and will finally result in a lightly doped silicon ingot. To obtain a P^- substrate, boron impurities are added [31][32].

Then, the ingot is cut into wafers using a large diamond saw. A typical wafer thickness is about 1 mm. After the ingot is cut into wafers, Al_2O_3 is used to polish the wafer surface. Chemical etching is also used to remove mechanically damaged material. Finally, an NaOH solution with SiO_2 particles is used for a fine-polish. At this moment, wafers are ready to be patterned into monolithic circuits.

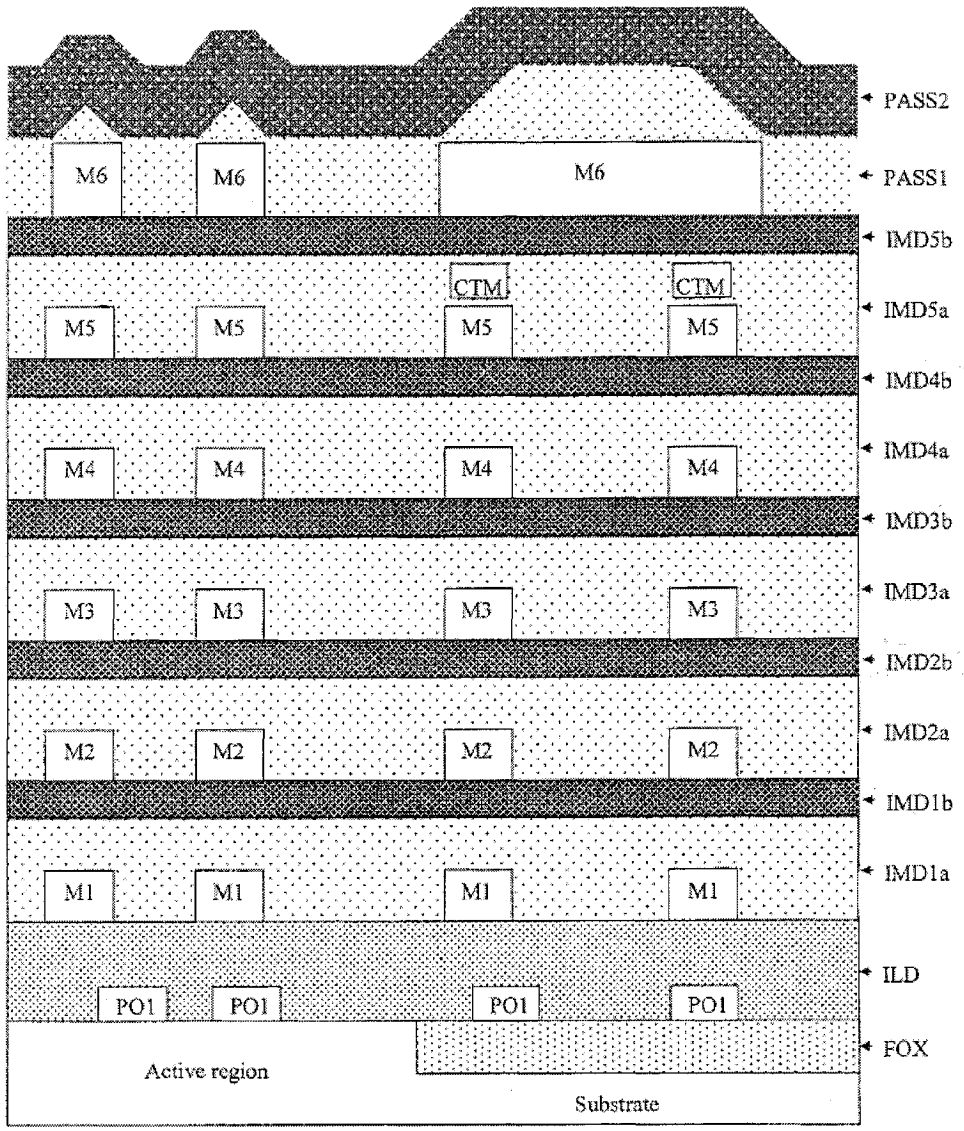


Fig. 2.1: Metallization structure of TSMC CMOS p18 technology.

Active regions and transistors are then fabricated on the wafer through diffusion and implantation. Photolithography is used in this procedure to select portions of the silicon wafer to be processed. Then, the complete wafer is covered in protective Chemical Vapor Deposition (CVD) SiO_2 and annealed. Annealing entails heating the wafer in inert gas (such as Nitrogen) for some period of time (15 to 30 minutes) at temperatures up to 1000 $°C$. The purpose of this is to heal the lattice damage sustained during all the ion implantations, broaden the concentration profiles of the implanted dopants, and increase the density of the deposited SiO_2 layer. Finally, contact holes are opened through the protective SiO_2 glass layer. Interconnect metal is then deposited to generate electrical connections.

Historically, aluminum (Al) was used for the interconnect. However, recently, other metals that have less tendency to diffuse into silicon during electrical operation of the microcircuit are used. Metal connection is deposited using evaporation techniques in a vacuum. The heat required for evaporation is normally produced by using electron-bean bombarding or, possibly, ion bombarding in a sputtering system. After the metal is deposited on the entire wafer, it is patterned using proper mask and then etched. Next, an additional layer of CVD SiO_2 is deposited and additional contact holes are formed and then, the upper layer of metal is deposited and etched. In a modern CMOS technology, this process will be repeated several times (6 layers of metal in CMOS p18 and 8 layers of metal layers in the CMOS p13 technology). After the last level of metal is finished, a final passivation, or overglass, is deposited for protection. The final microcircuit processing step is to etch openings to the pads used for wire bonding.

For the metallization interconnects, the bottom metal is usually Tungsten, which is highly resistive. However, it will not diffuse into silicon. Other metals such as Aluminum, or, Copper will diffuse into silicon and cause junctions. The leakage of the junctions will seriously impair the performance of transistors. A contact layer is used to connect this Tungsten layer to the active circuitry in the silicon. Higher levels of metal can be connected to adjacent layers using conductive plugs through via openings as described in above. Metal can be made in almost any shape desired by the designer. Vias are typically limited to a

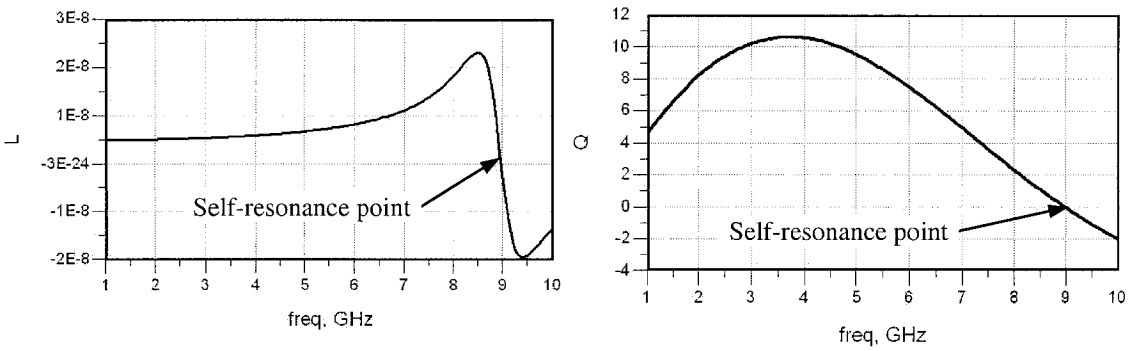
standard square size. However, it is possible to use arrays of vias to reduce the contact resistance. Higher metal layers are often made of Aluminum or, Copper, which have less resistivity than Tungsten. The top layer of metal will often be made much thicker than the lower levels to provide a low resistance routing option. However, the lithography for this layer may be much coarser than that of the underline layers. Thus, the top layer can accommodate lower density of routing lines [33].

Fig. 2.1 shows the metallization structure of the CMOS p18 technology [34]. Being the main stream of the standard CMOS technology nowadays, CMOS p18 is used widely in both digital and analog designs. Discussion in this chapter will be mainly based on this technology.

2.2 Bases of On-Chip Inductor Designs

2.2.1 Spiral Inductors

From the point of view of RF circuits, the lack of good inductors is one of the most conspicuous shortcoming of standard IC processes. Active circuits can synthesize the equivalent of an inductor. However, they always have higher noise, distortion, and power consumption than "real" passive inductors made with turns of wires. Presently, the widely used on-chip inductors are planar spiral inductors. This kind of inductors are easy to layout and their values and quality factors could be controlled by their geometry parameters such as inner outer diameters, spacing, strip width and number of turns, etc. As for the shape of the inductors, usually, circular ones will have higher quality factors while squares are easy to layout and calculate. Where a circular structure is not allowed, octagonal spirals are often used as a compromise between higher quality factors and restrictions of design rules. A spiral is always implemented in the topmost available metal because of its low resistivity and low parasitic capacitances to the substrate. Sometimes two or three levels of metal are used together through via connections to reduce the resistance to an even lower level, depending on the working frequency and applications [1].



(a) (b)

Fig. 2.2: Simulated inductance of an inductor spiral when frequency approaches the self-resonance point.

The inductance of a spiral is a complicated function of the geometry parameters. So far, there is no closed form equation which could be generally applied to all spiral designs and give accurate results. Though, there are many crude estimations or empirical formulas. Accurate computations always require the use of numerical calculation based on EM field solvers. This also applies to quality factor calculations of spiral inductors. Simple inductor structures, such as rectangular, could be calculated using Greenhouse's method. However, for other complicated inductor structures, presently, EM simulation is the only way to get an accurate inductance and quality factor.

2.2.2 Self-Resonance

At low frequencies, the inductance of an integrated inductor is relatively constant. However, with the increase of the operating frequency, parasitic capacitance elements start to become significant. And finally, at one frequency point, the admittance of the parasitic elements will cancel that of the inductor and the inductor will act as a purely resistive load to the circuit. This phenomenon is call inductor self-resonates. The inductance is nearly constant at frequencies much lower than the self-resonance frequency. Simulation and measurement results show that approaching self-resonance, the inductance will rise and then abruptly fall to zero Fig. 2.2 (a). Also, at this point, the quality factor of the inductor drops to zero, as shown in Fig. 2.2 (b). Beyond the self-resonant frequency, the parasitic capacitances will dominate and the inductor will act as a capacitor.

From the description above, spiral on-chip inductors have limited bandwidth over which

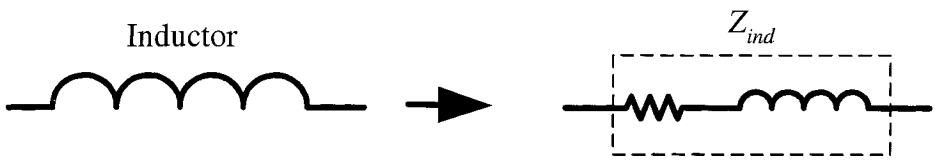


Fig. 2.3: Inductor impedance equivalent circuit.

they could be used. For reliable operation, it is necessary to stay well below the self-resonance frequency. Since parasitic capacitances increase in proportion to the size of the inductor, the self-resonance frequency decreases as the size of the inductor increases. Thus, especially at high operating frequencies, the size of the on-chip inductors that can be built effectively is practically limited.

2.2.3 The Quality Factor of an Inductor

The quality factor, or Q, of a passive circuit element, including inductors, can be defined as:

$$Q = 2\pi \cdot \frac{E_{Stored}}{E_{Dissipated}}, \tag{2.1}$$

where E_{Stored} is the energy stored in the passive component while $E_{Dissipated}$ is the energy loss in one cycle. Another equation that has been widely used for inductor quality factor characterization is:

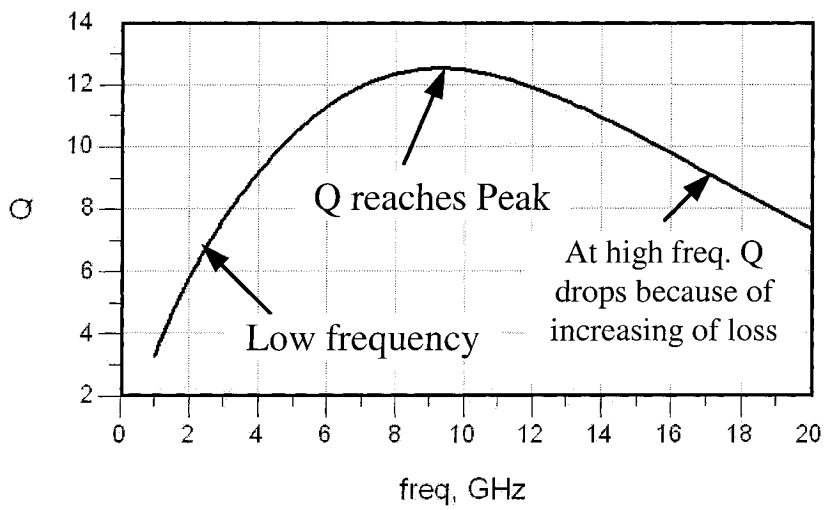


Fig. 2.4: Typical quality factor for on-chip inductors.

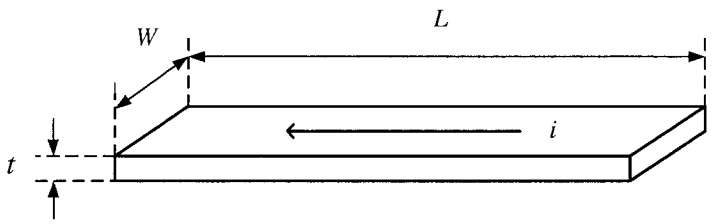


Fig. 2.5: Rectangular conductor with current flowing in the direction of *L*.

$$Q = \frac{Im(Z_{ind})}{Re(Z_{ind})}, \tag{2.2}$$

where Z_{ind} is the impedance of the inductor shown in Fig. 2.3. A good way to think about this is that Q is a measure of the ratio of the desired quantity (inductance reactance) to the undesired quantity (resistance). Obviously, a higher Q device is more ideal.

The quality factor of an on-chip inductor is affected by many things. As shown in Fig. 2.4, at low frequency, the quality factor tends to increase with frequency, because the losses are relatively constant (mostly due to the metal resistance of the spiral as will be discussed later in this chapter), while the imaginary part of the impedance is increasing linearly with frequency. However, as the frequency increases, currents start to flow in the substrate through capacitive and magnetic coupling. This loss of energy into the substrate causes an increase in the effective resistance. In addition, the skin effect starts to raise the resistance of the metal strips at higher frequency. Thus, most integrated inductors have quality factors that rise at low frequency then reach a peak, beyond which the losses make the effective resistance rise faster than the imaginary part of the impedance, and the quality factor starts to fall off. Design optimization always consists of ensuring that the inductor has a Q that peaks at around the frequency of interest.

2.2.4 Losses in On-chip Inductors

2.2.4.1 Sheet Resistance and Skin Effect

All conductive materials can be characterized by their resistivity ρ, or by their conductivity σ. These two quantities are related by:

Table 2.1: Skin depth of various metals at different frequencies

	ρ [μΩ · cm]	500 MHz	1 GHz	2 GHz	5 GHz	10 GHz
Gold	2.44	3.5	2.5	1.8	1.1	0.79
Tungsten	5.49	5.3	3.7	2.6	1.7	1.2
Aluminum	2.62	3.6	2.6	1.8	1.2	0.82
Copper	1.72	3.0	2.1	1.5	0.93	0.66
Silver	1.62	2.9	2.0	1.4	0.91	0.64
Nickel	6.90	5.9	4.2	3.0	1.9	1.3

* All depths are in micron meter

$$\rho = \frac{1}{\sigma}. \tag{2.3}$$

Resistivity is expressed as Ω-meters. Knowing the geometry of a metal and its resistivity is enough to estimate the resistance between any two points on the metal. As shown in Fig. 2.5, the resistance along the direction of L is expressed as:

$$R = \frac{\rho L}{Wt}. \tag{2.4}$$

All on-chip spiral inductors will have the DC resistance determined by (2.4), with L being the total length of the strip winding.

At high frequency, another effect comes into play. EM waves suffer attenuation as they enter a conductor. As the frequency approaches the GHz range, the distance that the waves can penetrate becomes comparable to the size of the metal line. The result is that the current becomes concentrated around the outside of the conductor, with lower current flowing in the center. The depth at which the magnitude of the EM wave decreases to 36.8% of its intensity at the surface is called the skin depth of the metal. Skin depth is given by:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}, \tag{2.5}$$

where f is the frequency and u is the permeability of the metal. Table 2.1 shows the skin depth of some commonly used metals in IC fabrication over the frequency band of interest. Because of this skin effect, it is easy to see that making lines much thicker will only

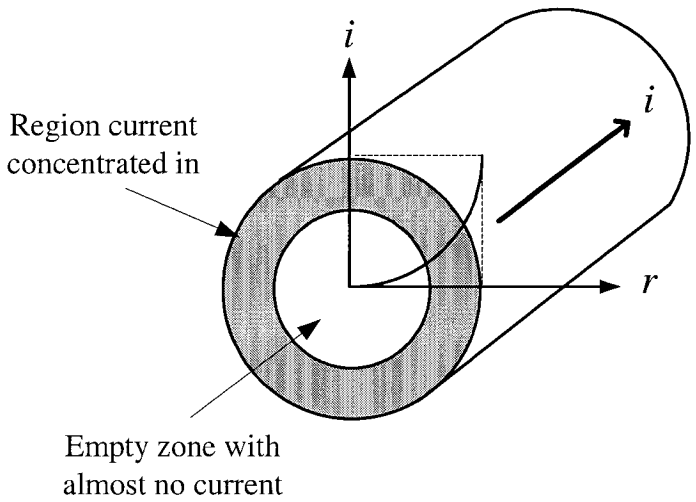


Fig. 2.6: Skin effect and "dead zone"

yield little advantage. The center of the conductor will form an "empty zone" where low current will flow, as shown in Fig. 2.6.

The importance of skin effect could be demonstrated using the following example: Assume a rectangular aluminum line with a width of 20 um, thickness of 3 um, and length of 100 um. At DC, the resistance of this line is 50 mΩ, while at 5 GHz the effective resistance becomes 98.2 mΩ. There is almost a 100% increase in resistivity!

2.2.4.2 Parasitic Capacitance

Metal lines, in addition to having resistances, as discussed in section 2.2.4.1, also have capacitances. Since the metal in an IC technology is embedded in an insulator over a conductive substrate, the metal trace and the substrate form a parallel-plate capacitor. The parasitic capacitance of a metal line can be approximated by:

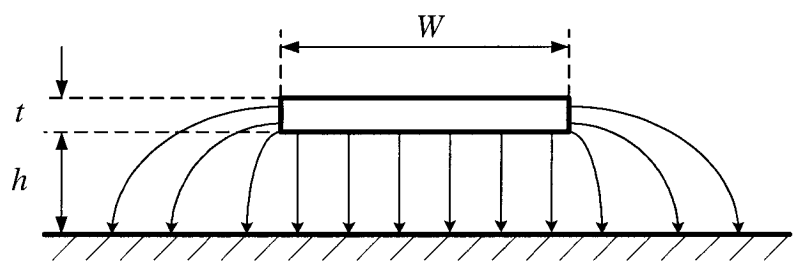


Fig. 2.7: Electric field lines showing the effect of fringing capacitance

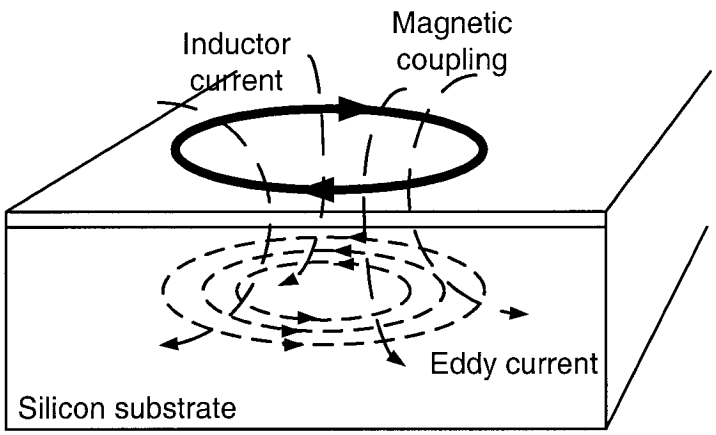


Fig. 2.8: Magnetic coupled Eddy current

$$C = \frac{\varepsilon_0 \varepsilon_r A}{h}, \tag{2.6}$$

where A is the area of the trace and h is the distance to the substrate.

Since metal lines in ICs can often be quite narrow, the fringing capacitance can be important, and the electric fields cannot be approximated as being perpendicular to the conductor near the edges, as shown in Fig. 2.7. For a strip line, the capacitance per unit length, taking into account the fringing portion, can be determined from the following equation [35]:

$$C = \varepsilon_0 \varepsilon_r \left[\frac{W}{h} + 0.77 + 1.06 \cdot \left(\frac{W}{h} \right)^{1/4} + 1.06 \cdot \left(\frac{Wt}{h} \right)^{1/(2)} \right]. \tag{2.7}$$

The final capacitance has units of F/m. In the square brackets, the first term accounts for the bottom-plate capacitance, while the other three terms account for fringing capacitances. As seen from Fig. 2.7, wider lines, or lines with high *W/t* ratio, will be less affected by fringing capacitances. This substrate coupling capacitor will couple the signal from the inductor winding into the conductive substrate, thus increasing the energy loss and decreasing the quality factor. It will also be part of the parasitics which will resonate with the inductor at a certain frequency. The larger the capacitor, the lower the self-resonance frequency.

There are also capacitances between lines, both vertically and horizontally. A rough esti-

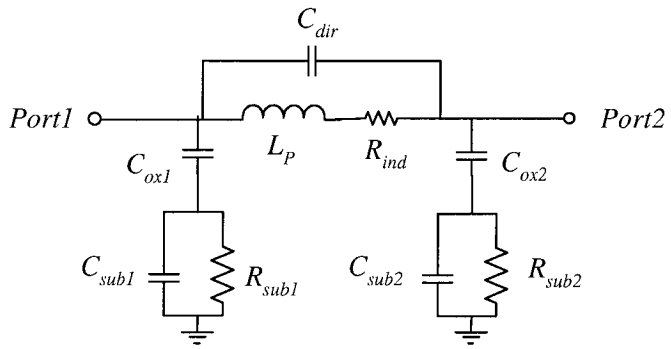


Fig. 2.9: Widely accepted π-model for on-chip inductor modeling

mate of the capacitance could be obtained by using the parallel-plate capacitance formula, though this may underestimate the value. These capacitors can lead to crosstalk between parallel lines, or between lines that cross over. Increasing the line spacing could reduce the crosstalk effect. Lowering this capacitor will obviously increase the self-resonance frequency.

2.2.4.3 Substrate Losses

When current is flowing in the spiral above the substrate, the magnetic flux it induces will penetrate into the conductive substrate below and excite in it closed loop currents, as shown in Fig. 2.8. This induced current is called the Eddy current. It has two effects: First, it introduces energy loss to the inductor. Magnetic energy which is supposed to be stored in the inductor coil is now transformed into current flowing in the substrate, and the energy is dissipated because of the resistivity of the Si material. In addition to contributing to the losses, the Eddy current also flows in a direction opposite to that of the current in the main inductor, generating negative magnetic flux into the inductor coil, and partially decreasing the inductance of the structure. This effect also causes temperature dependent inductance variation, because as the temperature increases, the substrate resistivity also increases, resulting in decreasing the Eddy current. As a consequence, the inductance tends to increase somewhat with temperature. This temperature coefficient may be as high as 200ppm/C° [1], and should be considered at the design stages.

Some refinements have been applied to reduce the Eddy current effect. Properly designed Patterned Ground Shields (PGS) will prevent the short-circuiting of the magnetic flux. It

also lowers the capacitive coupling to the lossy substrate [36]. The shielding is always made of lower level metal layers or, sometimes, using the poly layer underneath the inductor coil. Another effect of PGS is that the shielding greatly reduces coupling of the noise from the substrate [37]. However, the price paid is the lowered self-resonant frequency caused by the increased capacitance. Another approach that has been tried by some designers consists of removing the substrate material under the inductor spiral [19]. This would eliminate the Eddy current. But, this technology often requests extra fabrication procedures and increases the cost.

2.3 Analytical Models of an Inductor

When describing on-chip inductors, it is useful to build an equivalent model of the structure for both analysis and simulation. Fig. 2.9 shows a relatively complete model for on-chip spiral inductors, which includes the parasitic effects discussed above. In the model, R_s models the series resistance of the metal traces of the inductor. The value of R_s will increase at higher frequencies due to the skin effect. C_{oxide} models the capacitance from the trace to substrate. This is essentially a parallel-plate capacitor formed between the inductor metal and the substrate. C_{sub} and R_{sub} model the losses due to the magnetic and capacitive coupling to the lossy substrate. Both C_{sub} and R_{sub} are proportional to the area of the metal trace of the inductor, and their exact values depend on the properties of the substrate in question. C_{dir} models the direct forward coupling capacitance induced by the metal cross-unders. All component values can be calculated using analytical and empirical equations. Much more accurate results could be obtained through EM simulations and data fitting. This will be discussed later in this chapter.

An estimation for the series resistance at a specified frequency may be obtained from the following equation:

$$R_s \approx \frac{l}{W \cdot \sigma \cdot \delta(1 - e^{-t/\delta})}, \tag{2.8}$$

where σ is the conductivity of the material, l is the total length of the winding, W and t are the width and thickness of the metal trace, and the skin depth δ is given by (2.5).

As for the direct forward coupling capacitor C_{dir}, the following equation could be used:

$$C_{dir} = n \cdot W^2 \cdot \frac{\varepsilon_{OX}}{t_{OX}} \quad , \tag{2.9}$$

where t_{ox} is the thickness of the oxide between the cross-unders and the main spiral.

The capacitance between the spiral and the substrate is C_{ox}, and is here calculated using the parallel plate formula with fringing effect, where the length l is the total length of the spiral:

$$C_{OX} = \varepsilon_0 \varepsilon_r \left[\frac{W}{h} + 0.77 + 1.06 \cdot \left(\frac{W}{h} \right)^{1/4} + 1.06 \cdot \left(\frac{Wt}{h} \right)^{1/(2)} \right] \cdot l \tag{2.10}$$

The substrate loss is modeled with R_{sub}, which accounts for the following two distinct mechanisms: i) the loss associated with current flowing into the substrate through C_{ox} and ii) the losses due to the flow of the image current (Eddy current) induced in the substrate by the current flowing in the spiral above. Its value is given by:

$$R_{sub} \approx \frac{2}{W \cdot l \cdot G_0} \quad , \tag{2.11}$$

where G_0 is a fitting parameter that has the dimensions of conductance per area. It is constant for a given substrate material and distance between the spiral and the substrate. A typical value of G_0 is about $10^{-7} \mathrm{S}/u\mathrm{m}^2$.

The capacitor C_{sub} reflects the capacitance of the substrate, as well as other reactive effects. It is given by:

$$C_{sub} = \frac{W \cdot l \cdot C_0}{2} \quad , \tag{2.12}$$

where C_0 is also a fitting parameter that is constant for a given substrate and distance between the spiral and the substrate. A typical range for C_0 is between 10^{-3} and 10^{-2} fF/

$u\text{m}^2$ [1].

From the discussion above, it is very clear that on-chip inductors design is a geometrically oriented procedure. Also, all component values in the model circuit could only be obtained after the layout parameters have been defined. For on-chip inductors design, following the guidelines listed below will greatly speed up the design procedure:

1. At low frequency (under 2 GHz), keep the line spacing as tight as possible, while at higher frequencies, larger line spacing is needed to lower the coupling between adjacent traces.

2. Increasing the metal width will decrease the number of turns in a given area as well as lessen the inductance per unit length, thus reducing the inductance. A wider strip line will also decrease the series resistance of the lines at low frequency. However, large inductance area means bigger capacitance, which means more coupling to the substrate, and lower self-resonance. As W goes up, the inductance decreases and the frequency of the peak quality factor is lower. Usually, in the CMOS p18 technology, for 1 to 5 nH inductor in the 2 to 6 GHz range, the line width would be expected to range from 10 to 25 um.

3. As for the inductor area, a bigger area means that more current would be coupled to the substrate. This will definitely lower the higher frequency performance. Also, a bigger area means longer strip lines, with the same line width. So, as the area goes up, the inductance goes up and the frequency of the peak quality factor will be lower.

4. The last design parameter for the layout is the number of turns. It is usually best to pick fewer rather than more turns, for less parasitic effects. However, balance should be reached between less turns and bigger inductor dimensions for the specified inductance value, because more self-inductance will be needed to compensate for the loss of the mutual inductance caused by lessening of the turns. Also, inner turns add less to the inductance but more to the resistance, so it is always desirable to keep the inductor hollow. By changing the area and line width, the peak frequency of a the quality factor for a specified inductance could be fine-tuned.

2.4 ADS EM Momentum Simulation

2.4.1 Introduction to Momentum

Momentum is part of the HP Advanced Design System (ADS) design software. It gives the designer the simulation tools that would be needed to evaluate and design modern communication systems. Momentum is an electromagnetic simulator that can compute the S-parameters for general planar circuits, including microstrips, slot-lines, coplanar waveguides, and other topologies. Vias and airbrigdes connect topologies between different layers, so designers can simulate multilayer RF/microwave printed circuit boards, hybrids, multi-chip models, and integrated circuits. Momentum offers a complete tool set to predict the performance of high-frequency circuit boards, antennas, and ICs. Key features of Momentum includes:

1. An electromagnetic simulator based on the Method of Moments;
2. Adaptive frequency sampling for fast, accurate, simulation results;
3. Optimization tools that alter geometric dimensions of a design to achieve performance specifications;
4. Comprehensive data display tools for viewing results;
5. Equation and expression capabilities for performing calculations on simulated data;
6. Full integration in the ADS circuit simulation environment allowing EM/Circuit co-simulation.

For more information on Momentum, readers could refer to other dedicated documentations [38]. In this section, a detailed procedure on using Momentum to simulate on-chip inductors will be given. This procedure includes substrate modeling, simulation setup, S-parameter processing, inductance and quality factor extraction, and finally data fitting to get accurate π-models that can be used in circuit simulation.

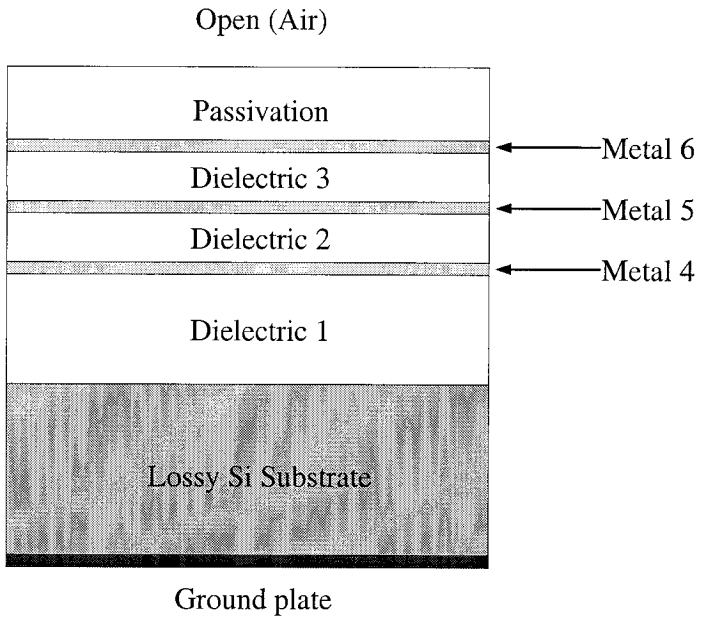


Fig. 2.10: Simplified CMOS p18 substrate model

2.4.2 Substrate and Metallization Modeling

The first step in conducting accurate EM simulations using Momentum requires careful modeling of the substrate structure. Modeling of the substrate is achieved by creating discrete elements that take into account the substrate properties. The modeling procedure is initiated by entering the substrate details shown in Fig. 2.1 into Momentum, to build the stack substrate model. Three substrate elements are defined here. They are: i) lossless, or

Table 2.2: Electrical parameters for substrate layers

	Thickness [μm]	Permittivity (Real part)	Conductivity [S/m]
Free space	Open boundary	1	0
Passivation 2	0.7	7.9	0
Passivation 1	1	4.2	0
IMD 5	1.33	3.9	0
IMD 4	1.33	3.9	0
IMD 321	3.99	3.9	0
ILD_FOX	1.05	3.9	0
Substrate	760	11.7	10
Ground	Close boundary	0	0

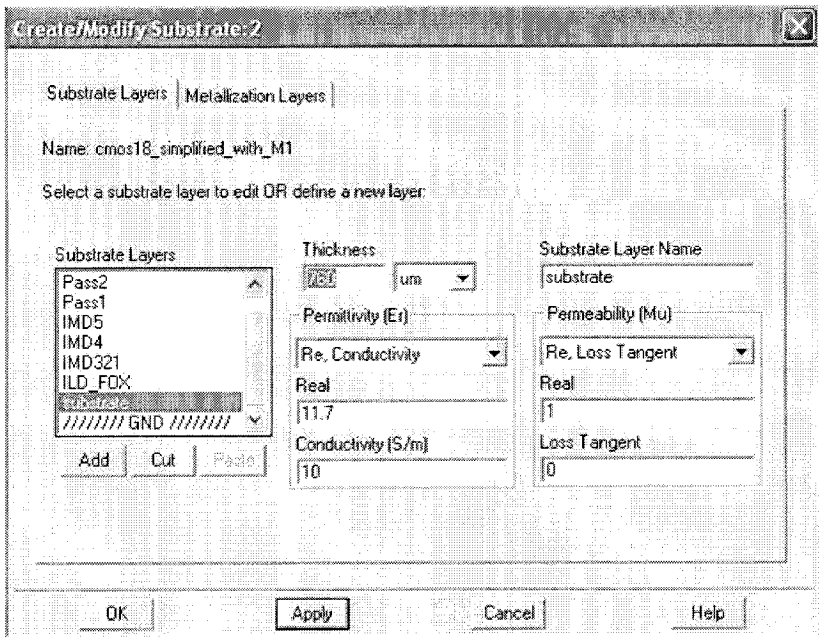


Fig. 2.11: Substrate model input window in Momentum.

dielectric layers such as SiO_2 and passivation protective layers. Relative permittivity and thickness are required to model these layers; ii) the lossy layer, which is the lighter doped silicon substrate upon which the circuit is fabricated. Parameters used to characterize this layer are conductivity and the real part of the permittivity; and iii) conductive metal layers which are used to build all interconnects between transistors and on-chip passive components such as inductors and capacitors. The conductivity and thickness of the metal will be used in modeling. Elements i) and ii) will be viewed as substrate models in Momentum while iii) will be treated as a metallization model.

It is clear that to completely model the CMOS p18 substrate, designers need to model sixteen substrate layers (one lossy silicon layer, fifteen lossless SiO_2 layers) and six metallization layers (metal 1 to metal 6). In addition to the tedious work of building this complicated model, its complexity will also greatly increase the simulation time, because the simulator will mesh and calculate each of the substrate layers whether or not there is a metallization interconnection. To decrease the simulation time without sacrificing the accuracy consists of combining the layers that have the same permittivity into one which has a height equal to the sum of the thicknesses of those layers. In most inductor designs, metal 6 and metal 5 are mostly used, while sometimes metal 4 is needed to build the

underpass or outleads. Thus, all the dielectric layers under metal 4 could be combined into one layer, and metal layers 1, 2, and 3 could also be neglected. By doing so, only 5 substrate layers will be considered in the modeling. They are one Si lossy substrate, and four dielectric layers separating the remaining metal layers. Metal 6 to metal 4 will be modeled as metallization layers. The simplified substrate model is given in Fig. 2.10.

Table 2.2 shows an example of the electrical parameters needed by Momentum to build the substrate model. Fig. 2.11 shows the substrate model input window in Momentum. Some changes have been made to the substrate layers in Fig. 2.10, which include splitting the passivation layer into two parts to reflect the permittivity difference between them and, adding one more dielectric layer, ILD_FOX, for possible use of metal 1 as PGS.

For the substrate characteristics definition, the permittivity, loss tangent, and conductivity could be used. The relationship between these three values is discussed below. The complex relative permittivity could be expressed as:

$$\varepsilon = \varepsilon_r + j\varepsilon' = \varepsilon_r\left(1 + j\frac{\varepsilon'}{\varepsilon_r}\right), \tag{2.13}$$

where ε_r is the relative dielectric constant which is a real number, and

$$\frac{\varepsilon'}{\varepsilon_r} \tag{2.14}$$

is defined as loss tangent. While another definition of loss tangent uses the following equation:

$$\tan\Delta = \frac{2 \cdot \sigma}{\varepsilon_r \cdot f}, \tag{2.15}$$

Table 2.3: Parameters of metallization

	Metal 6	Metal 5 & 4
Thickness [μm]	0.99	0.53
Conductivity [S/m]	2.8e7	2.42e7
Ohm/Sq [Ω/sp]	0.036	0.078

where σ is the conductivity and f is the frequency. Comparing (2.14) and (2.15), the following relations could be obtained:

$$\tan\Delta = \frac{2 \cdot \sigma}{\varepsilon_r \cdot f} = \frac{\varepsilon'}{\varepsilon_r} , \tag{2.16}$$

and

$$\varepsilon' = \frac{2 \cdot \sigma}{f} . \tag{2.17}$$

So, knowing two of the permittivity, loss tangent, and conductivity parameters, plus the frequency, the electrical characteristics could be defined using (2.13) to (2.17). The conductivity σ and the real part of the permittivity ε_r are chosen in this case for their frequency independency.

Clearly, for dielectric material, the loss tangent will be zero because $\sigma = 0$, which means that there is no energy loss in those layers.

The parameters needed to model the metallization are conductivity and thickness. Some calculations are required to obtain the conductivity from the Ohm/sq value given in the technical file. The Ohm/sq value of metal 6 from the technical file is:

$$R_{sq} = \frac{\rho}{h} = \frac{1}{\sigma \cdot h} = 0.036[\Omega/\text{sq}] , \tag{2.18}$$

where h is the thickness of metal 6, which equals 0.99 [um] according to the technology file. The conductivity could be calculated using the following equation:

$$\sigma_6 = \frac{1}{0.036 \cdot h} = \frac{1}{0.036 \cdot 0.99[u\text{m}]} = 2.8e7[\text{S/m}] . \tag{2.19}$$

Metal 5 and metal 4 have different thicknesses and Ohm/Sq values, which are 0.53 um and 0.078 Ohm/sq, respectively. Using (2.19), the conductivities of metal 5 and metal 4 are calculated as:

$$\sigma_{5,4} = \frac{1}{0.078 \cdot h} = \frac{1}{0.078 \cdot 0.53[u\text{m}]} = 2.42e7[\text{S/m}] . \tag{2.20}$$

Fig. 2.13 shows the metallization model input window in Momentum.

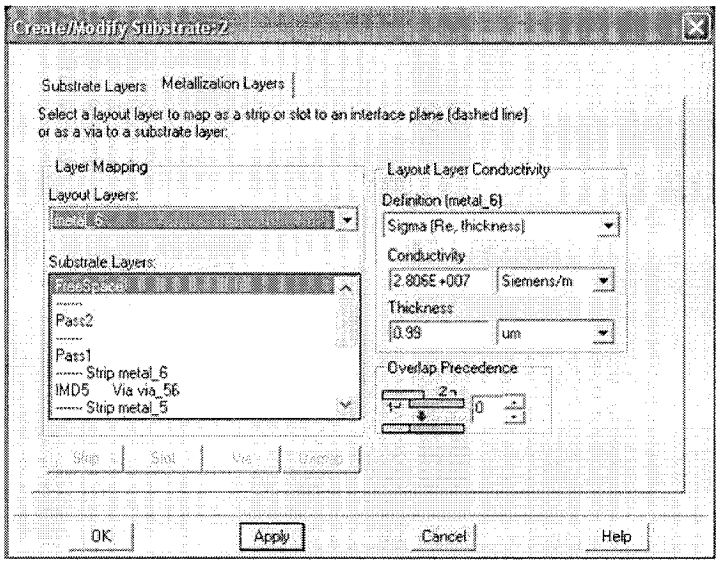
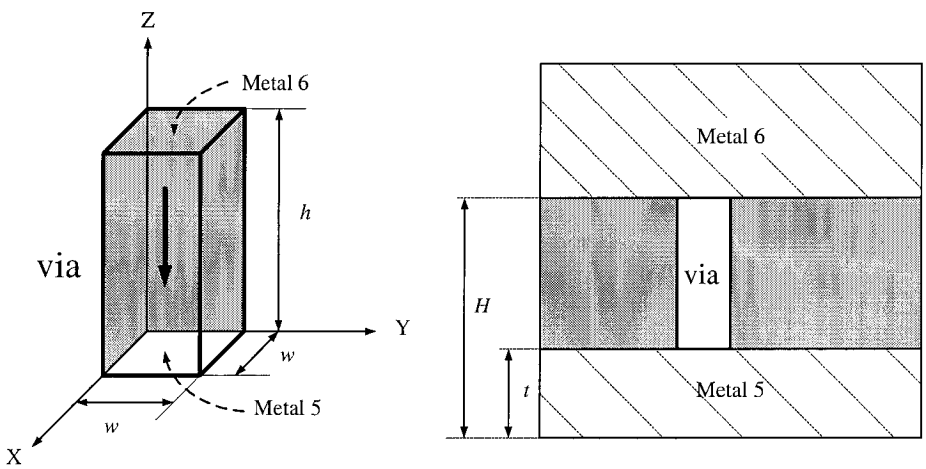


Fig. 2.13: Metallization model input window in Momentum.

To emulate the resistivity of vias, the conductivity of the via layer should be calculated. According to ASITIC's technical file, the resistance for one via is 6.4Ω [40]. This resistance is in the Z direction as shown in Fig. 2.12 (a). Equations (2.3) and (2.4) could be used to calculate the conductivity of the via layer, as follows:

$$6.4[\Omega] = \frac{h}{\sigma \cdot w \cdot w}, \tag{2.21}$$

where h and w are the height and width of the via respectively, and h is the distance between metal 6 and metal 5 minus the thickness of metal 5, as shown in Fig. 2.12 (b):



(a) **(b)**

Fig. 2.12: (a) Dimension of the via between metal 5 and metal 6; (b) Thickness of the via in a real circuit.

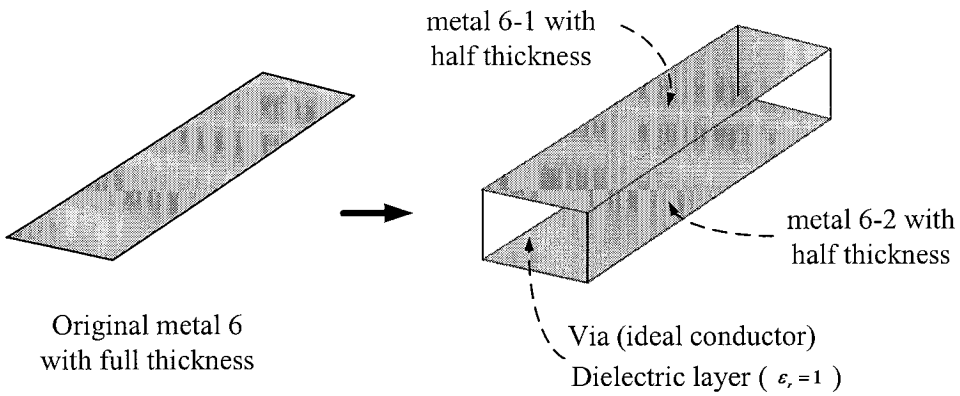


Fig. 2.14: Thick metal layer model

$$h = H - t = 1.33[um] - 0.53[um] = 0.8[um] . \tag{2.22}$$

The width of the via also comes from the technical file, which is 0.26 [um]. Then, the conductivity of the via layer is given by:

$$\sigma_{\text{via}} = \frac{h}{6.4[\Omega] \cdot w \cdot w} = \frac{0.8[um]}{6.4[\Omega] \cdot 0.26[um] \cdot 0.26[um]} = 2.4e6[\text{S/m}] . \tag{2.23}$$

Compared to normal metal layers which are defined by their conductivity and thickness, a via layer will be defined only by the conductivity value with the real part equal to σ_{via}, and the imaginary part equal to zero.

2.4.3 Thick Metal Modeling

As for a 2.5D EM simulator, Momentum will not normally consider the thickness of the stripline in simulation. However, the thickness is an important modeling parameter, because the simulator will need it to calculate the resistance of the stripline. Ignoring the thickness is acceptable if the height of the stripline is much less compared to the width. However, the thickness of the top metal in a modern CMOS technology, which designers usually use nowadays to build inductors, is significant. To consider this thickness and get even more accurate simulation results, a modification to the metallization model of metal 6 is required [41]. The method is to divide metal 6 into 3 metal layers: metal 6-1 and metal 6-2 and a via-6 in between. Metal 6-1 and metal 6-2 will have the same conductivity as the original metal 6, while only half of the thickness. Via-6 will be defined as an ideal conductor to connect these two metal layers. One more dielectric layer with $\varepsilon_r = 1$, will

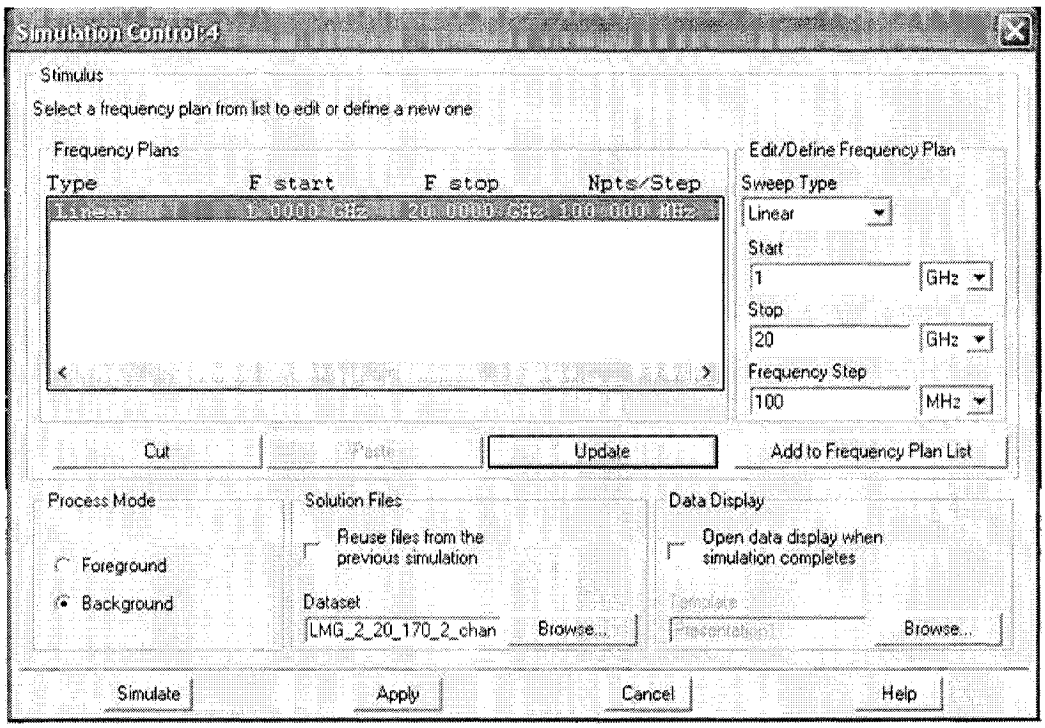


Fig. 2.15: S-parameter simulation setup

also be defined to accommodate the via-6 layer. The final thick metal layer model structure is shown in Fig. 2.14.

One consideration is that the thick metal model will increase the simulation time because of the addition of extra layers. Designers may have to balance between accuracy and simulation time if necessary.

2.4.4 Simulation

Two port network S-parameter simulation is used to simulate the inductor structure. The frequency range is 1 to 20 GHz. The frequency sweep type is chosen to be adaptive, to save simulation time. Later verification simulations can use linear sweep to cover small frequency steps in the frequency range of interest (Fig. 2.15). Before starting the simulation, two more things should be considered: i) mesh setup and ii) port setup.

Meshing is the procedure of dividing the planar design structure into grid-like patterns of triangles and rectangles. The pattern of cells is based on the geometry of the design and, optionally, user-defined parameters, so each circuit will have a unique mesh calculated for

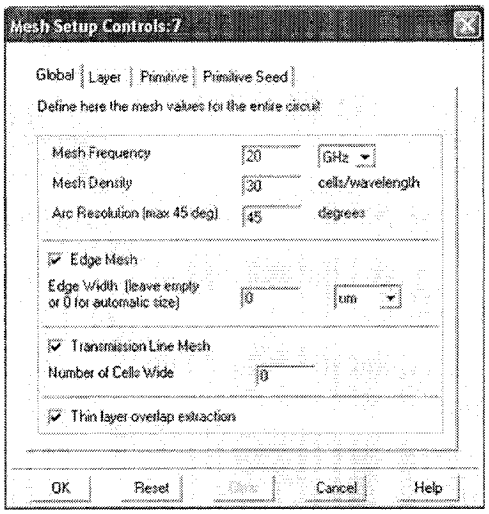


Fig. 2.16: Mesh setup for inductor simulations

it. Each triangle or rectangle in the mesh becomes a cell. The mesh is then applied to the structure in order to compute the current within each cell and identify any coupling effects during simulation. From these calculations, S-parameters are then computed for the structure. The mesh frequency is the frequency at which the mesh pattern is calculated. It will be setup to be the highest frequency of simulation. For mesh density, higher density per wave length will give higher simulation accuracy, and will take longer simulation time. In inductors design, 30 cells/wavelength is a reasonable compromise. For all the other parameters, default settings will be good enough for the simulation, as shown in Fig. 2.16.

There are several types of ports which could be used for simulation in Momentum. In most cases, a single port is used for each end of the inductor. Fig. 2.17(a) shows the single port setup for a two port structure. When a thick metal model is used, some modifications are

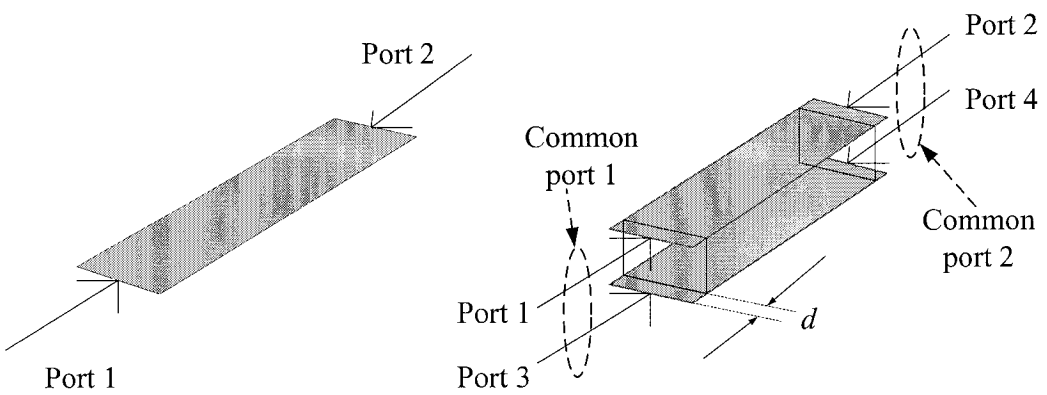


Fig. 2.17: (a) Single port for two port network simulations; (b) Common ports for thick metal models

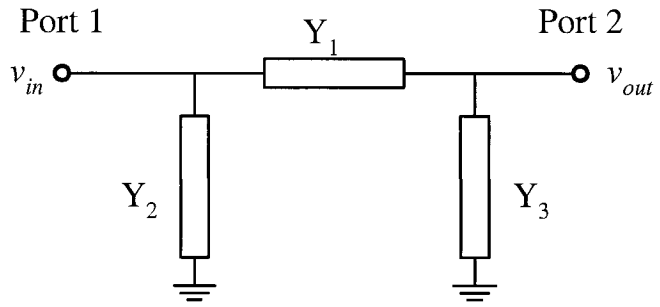


Fig. 2.18: Widely used π model of the inductor, expressed using three admittances

needed because two metal layers are used for signal transmission, e.g. metal 6-1 and metal 6-2, as shown in Fig. 2.14. To accommodate this change, for each of the two ends of the inductor, two ports are used, as shown in Fig. 2.17 (b): port 1 and port 3 for one end and port 2 and port 4 for the other end. Then, port 1 and port 3 (same for port 2 and port 4) could be combined into one equivalent common port by assigning them to be a common port pair (Fig. 2.17 (b)). The final setup would still be a two port network with 2 equivalent common ports, similar to the single port setup shown in Fig. 2.17 (a). Note that small extensions *d* have been made to the metal layers in Fig. 2.17 (b). This will avoid putting ports at the edge of a via layer, which can generate an error.

For more detailed procedures to setup the port properties, interested readers could refer to the related ADS documentation [38].

2.4.5 Data Processing and L & Q Extraction

EM simulations and measurements will give S-parameters as results, thus effective and accurate data post-processing is needed to extract the inductance and quality factor from those S-parameters. This section will discuss the L & Q extraction procedures from the S-parameters and, as examples, differentially driven and single ended setups are presented.

Both the inductance and quality factor could be calculated using the three components of the π-model shown in Fig. 2.18. Replacing Y_1, Y_2 and Y_3 in Fig. 2.18 with the corresponding inductor, capacitor and resistors will lead to the inductor wide-band π-model discussed in Fig. 2.9. To calculate Y_1, Y_2 and Y_3, S-parameters should firstly be transform to Y-parameters using the equations listed below.

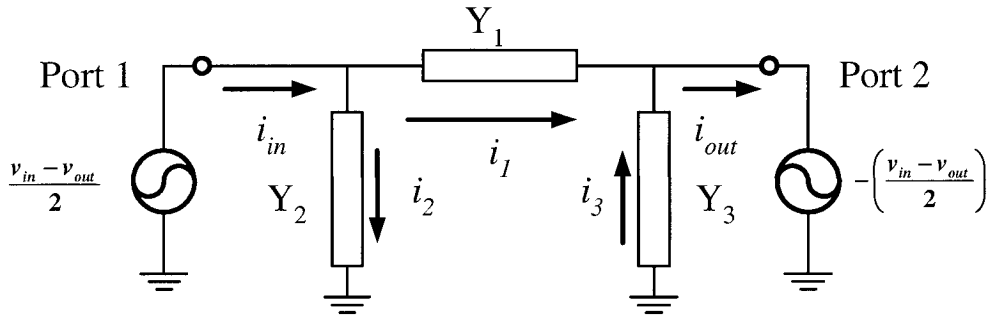


Fig. 2.19: Inductor under a differential driving voltage

$$Y_{11} = Y_0 \cdot \frac{(1-S_{11})\cdot(1+S_{22})+S_{12}\cdot S_{21}}{\Delta} \tag{2.24}$$

$$Y_{12} = Y_0 \cdot \frac{-2\cdot S_{12}}{\Delta} \tag{2.25}$$

$$Y_{21} = Y_0 \cdot \frac{-2\cdot S_{21}}{\Delta} \tag{2.26}$$

$$Y_{22} = Y_0 \cdot \frac{(1+S_{11})\cdot(1-S_{22})+S_{12}\cdot S_{21}}{\Delta}, \tag{2.27}$$

where Y_0 is the reference admittance and Δ is defined as:

$$\Delta = (1+S_{11})\cdot(1+S_{22})-(S_{12}\cdot S_{21}). \tag{2.28}$$

Then, from the Y-parameters, Y_1, Y_2 and Y_3 in Fig. 2.18 could be obtained using:

$$Y_1 = -Y_{12}[or]-Y_{21} \tag{2.29}$$

$$Y_2 = Y_{11}+Y_{12} \tag{2.30}$$

$$Y_3 = Y_{22}+Y_{21}. \tag{2.31}$$

For symmetric inductor designs, Y_2 equals Y_3.

Then, to calculate the inductance and quality factor, we suppose the inductor is excited by v_{in} at one end, and v_{out} at the other end, as shown in Fig. 2.19. By changing the forms of the excitation voltages, v_{in} and v_{out} could be expressed as:

$$v_{in} = \frac{v_{in}+v_{out}}{2}+\frac{v_{in}-v_{out}}{2} \tag{2.32}$$

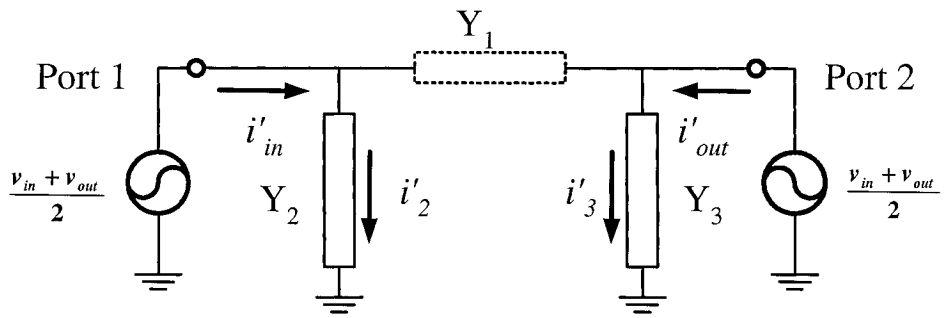


Fig. 2.20: Inductor under common mode driven

$$v_{out} = \frac{v_{in} + v_{out}}{2} - \frac{v_{in} - v_{out}}{2} . \tag{2.33}$$

The first terms of the right side of (2.32) and (2.33) could be viewed as common mode excitation voltages with:

$$v_{comm} = \frac{v_{in} + v_{out}}{2} . \tag{2.34}$$

While, the second terms are the differential voltages applied to the inductor, with:

$$v_{diff} = \pm\frac{v_{in} - v_{out}}{2} . \tag{2.35}$$

According to the circuit excitation superposition theory, these common mode and differential voltages could be treated separately for analysis. By viewing the excitation as the combination of common mode and differential mode, more insight into the excitation voltage dependent quality factor mechanism of the inductor could be revealed.

First, only the differential part is considered, as shown in Fig. 2.19. The signal current i_1 is flowing through Y_1, while i_2 and i_3 are the signal currents flowing into/from substrate, causing energy losses. Under the fully differential excitation, i_2 equals i_3. Thus, using simple circuit analysis methods, the following relations are obtained:

$$i_{in} = i_1 + i_2 = i_1 + i_3 = i_{out} . \tag{2.36}$$

An equivalent signal current flows into port 1 and comes out from port 2. The equivalent impedance of the model circuit under a differentially driving signal is then given by:

$$Y_{ind} = Y_1 + \frac{Y_2 \cdot Y_3}{Y_2 + Y_3}, \tag{2.37}$$

and finally,

$$Z_{ind} = \frac{1}{Y_{ind}}. \tag{2.38}$$

Now, consider the situation under which the inductor is driven by a common mode voltage, as shown in Fig. 2.20. Clearly, under common mode excitation, there will be no signal current in Y_1, because the same voltages are applied to port 1 and port 2. The following relations are obviously derived:

$$i_{in}' = i_2' \tag{2.39}$$

$$i_{out}' = i_3'. \tag{2.40}$$

Since the signal currents at port 1 and port 2 are different in direction, there is no equivalent impedance between port 1 and port 2 that could be obtained in this case. A common mode excited signal current will not go through Y_1, thus it will not contribute to the inductive energy storage. It will only contribute to the losses.

The total loss of the inductor will be the sum of the losses generated by both the differential and common mode portions of the excitation voltage, while the inductance value would be extracted using only the differential excitation related term, which is Z_{ind}. The inductance and quality factor could be expressed using the following equations:

$$L = \frac{Im(Z_{ind})}{2\pi f} \tag{2.41}$$

$$Q = 2\pi \cdot \frac{E_{stored}}{E_{diff} + E_{comm}}, \tag{2.42}$$

where Z_{ind} is calculated from (2.38), E_{diff} is the energy dissipation by the differential portion of the signal voltage, and E_{comm} implies common mode portion energy loss. Note that only the differential excitation contributes to E_{stored}, which is the energy stored in the inductor structure.

While Z_{ind} could be expressed explicitly, which will give a specific inductance value using (2.41), it would be difficult to calculate the quality factor from (2.42), because both of the energy stored and energy dissipated are excitation related. However, under some special conditions, (2.42) could be simplified to give specific quality factor values:

i) Assume the following relation is true:

$$v_{in} = -v_{out} . \tag{2.43}$$

In this fully differentially driven application, common mode excitation is zero according to (2.34). E_{comm} in (2.42) will also be zero. Thus, both inductance and quality factor could be calculated using only differential excitation related terms. In this case, (2.42) can be simplified to the following expression:

$$Q = \frac{Im(Z_{ind})}{Re(Z_{ind})} . \tag{2.44}$$

Because there is no common mode energy loss under this situation, (2.44) gives the highest quality factor that the inductor structure could reach.

ii) At another extreme, assume

$$v_{in} = v_{out} . \tag{2.45}$$

This is the fully common mode driving application. Both E_{diff} and E_{stored} are zero because there is no differential driving portions in the excitation. The quality factor is zero accordingly. However, this is not likely to happen in real designs.

iii) In the third situation, where either v_{in} or v_{out} is grounded, the inductor is viewed as a single ended structure. The input impedance Z_{in} looking into the un-grounded port could be calculated from the one port S-parameters, either through simulation or measurement. Then, replacing Z_{ind} in (2.41) and (2.44) with Z_{in} would give the inductance and the quality factor. Because of the common mode losses, the quality factor will effectively be lower.

For a specific technology, a fabricated inductor will have a relatively constant inductance

value, because this value is only set by the geometry of the structure. However, for the quality factor, it will not only depend on the loss characteristics of the structure, but will also depend on how the inductor is used in the circuit. Thus, the effective qualify factors may vary a lot.

2.4.6 Model Parameters Fitting

Even though component values in the inductor π-model could be calculated using the equations discussed in section 2.3, much more accurate model parameters considering more practical aspects such as the asymmetry of the structure, the vias resistances, and the fringing effects between adjacent windings, could be obtained through "parameter fitting". Through this procedure, the S-parameters response obtained from EM simulation or prototype measurement could be fitted to the components of the wide band π-model, which would then have the exact same S-parameters response. For designers using Cadence Spectre or Hspice, this step is mandatory because they both are time domain based simulators. Though some simulation tools could use S-parameters directly, they may give convergence problems during the time domain based simulations such as transient, because of the limitation of their integrated frequency-to-time domain transform functions. A π-model is always the most decent equivalent circuit in terms of accuracy and simplicity.

2.5 Design Prototypes and Applications

Based on the discussion above, several inductor structures have been designed and simulated using ADS Momentum. All designs targeted the application in a folded cascode LNA design operating at 5.8 GHz and fabricated in a CMOS p18 technology. Simulation and measurement results for the LNA match very well. This demonstrated that our implementation of the design methods and modeling approach discussed earlier is accurate and reliable. For more details about the folded cascode LNA design, readers could refer to [39].

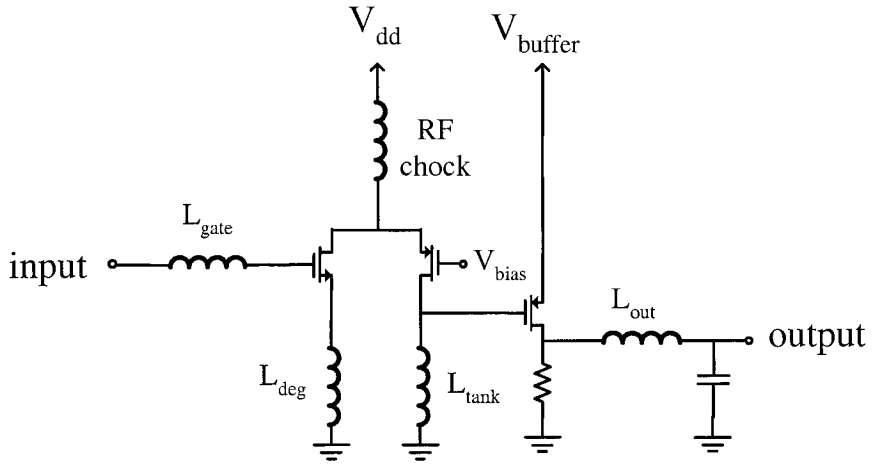


Fig. 2.21: Folded cascode LNA topology

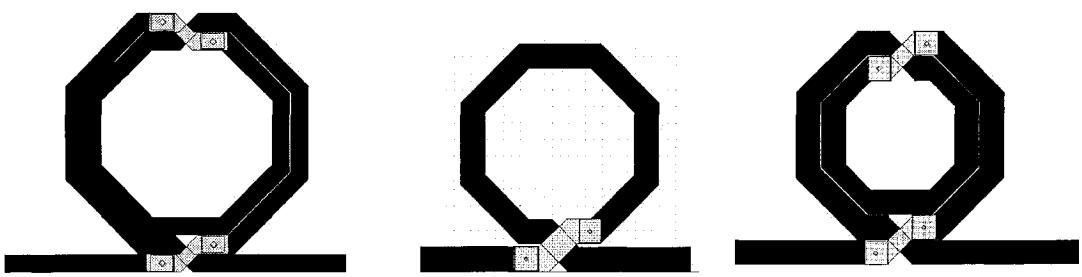
2.5.1 Inductors Designs

The folded cascode LNA topology is shown in Fig. 2.21. For monolithic integrated circuits, all inductors are preferably implemented on-chip. A total of 4 inductors are used: the input gate matching inductor L_{gate}, the source degeneration inductor L_{deg}, the tank inductor L_{tank},and the output matching inductor L_{out}. Fig. 2.22 shows the inductors' layout.

Table 2.4: Design parameters for the inductors

	Q*	L [nH]	d_{in} [um]	d_{out} [um]	Metal	W [um]
L_{gate}	12.2	2.6	193	275	6	20
L_{deg}	10	0.47	90	120	6	15
L_{tank} & L_{out}	11.4	1.24	88	170	6	20

* Q value results from differential extraction at 6 GHz in simulation



L_{gate} L_{deg} L_{tank} & L_{output}

Fig. 2.22: Layout of the inductors used in the LNA design.

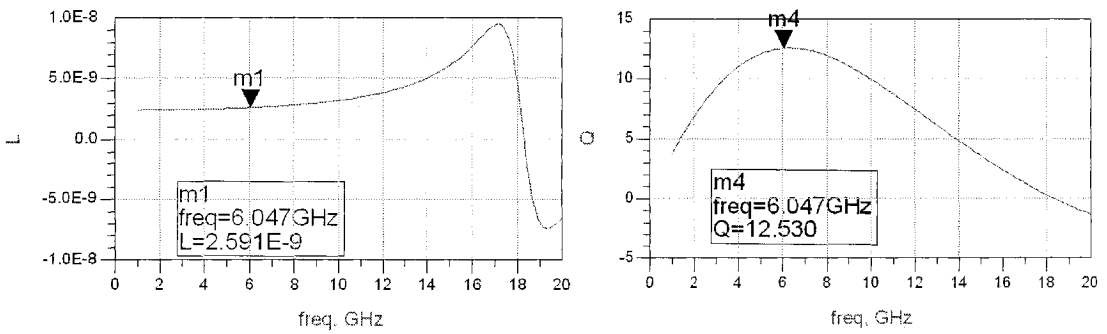


Fig. 2.23: Simulation results for L and Q of gate matching inductor, L_{gate}

Table 2.4 summarizes the design parameters. Please note that, according to this LNA design, the tank inductor and the output matching inductor had the same value, so only one inductor was designed. However, this is not always the case. All inductors were simulated as two port networks and extracted as differentially driven inductors using the equations discussed in section 2.4.5. Fig. 2.23 shows the simulation results for L_{gate} as an example. When used in the LNA design, the effective quality factor is lower, due to the presence of the common mode excitation in this non-differential application.

The π-model of the inductors used in Cadence Spectre simulations for the LNA are obtained using data fitting. Fig. 2.24 shows the S-parameters of the tank inductor from

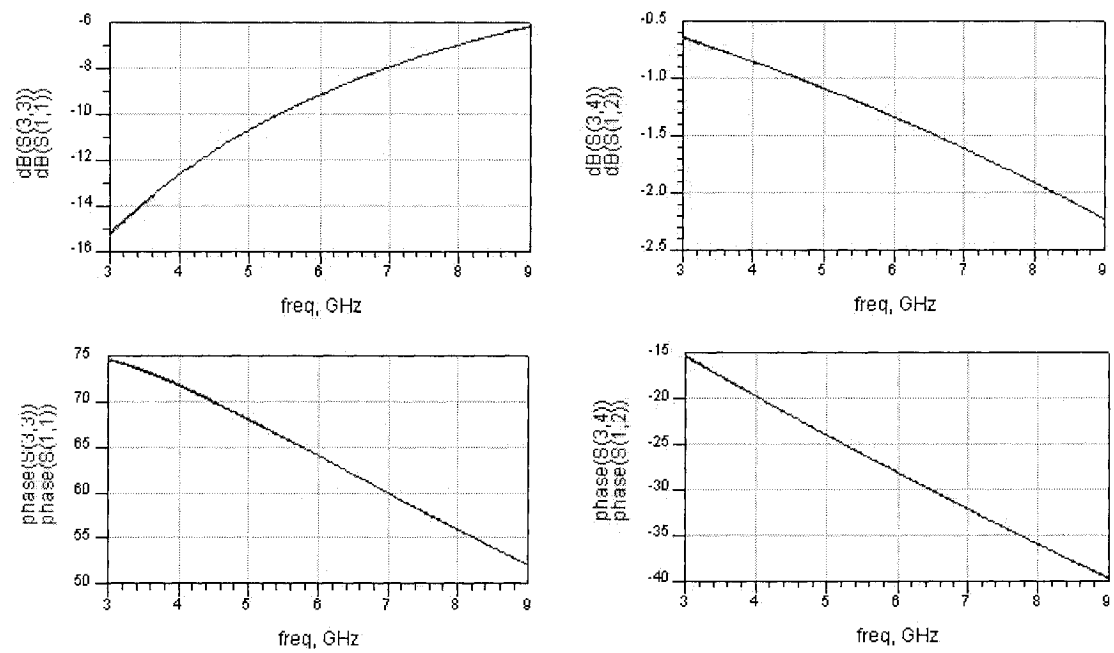


Fig. 2.24: Result of data fitting for the π model of the tank inductor.

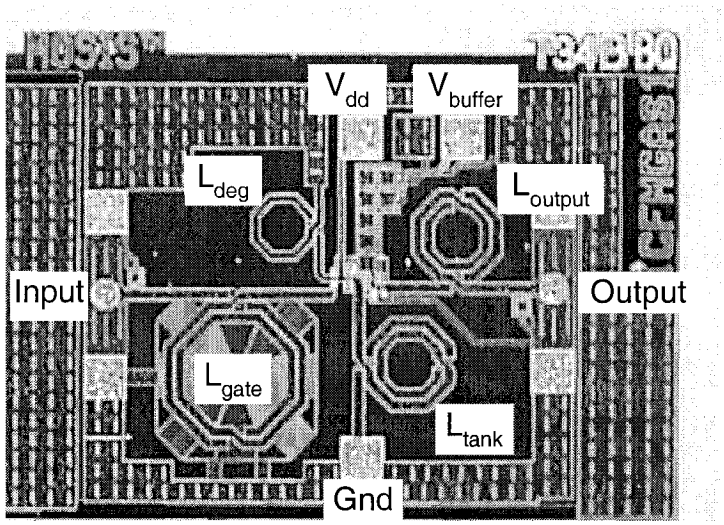


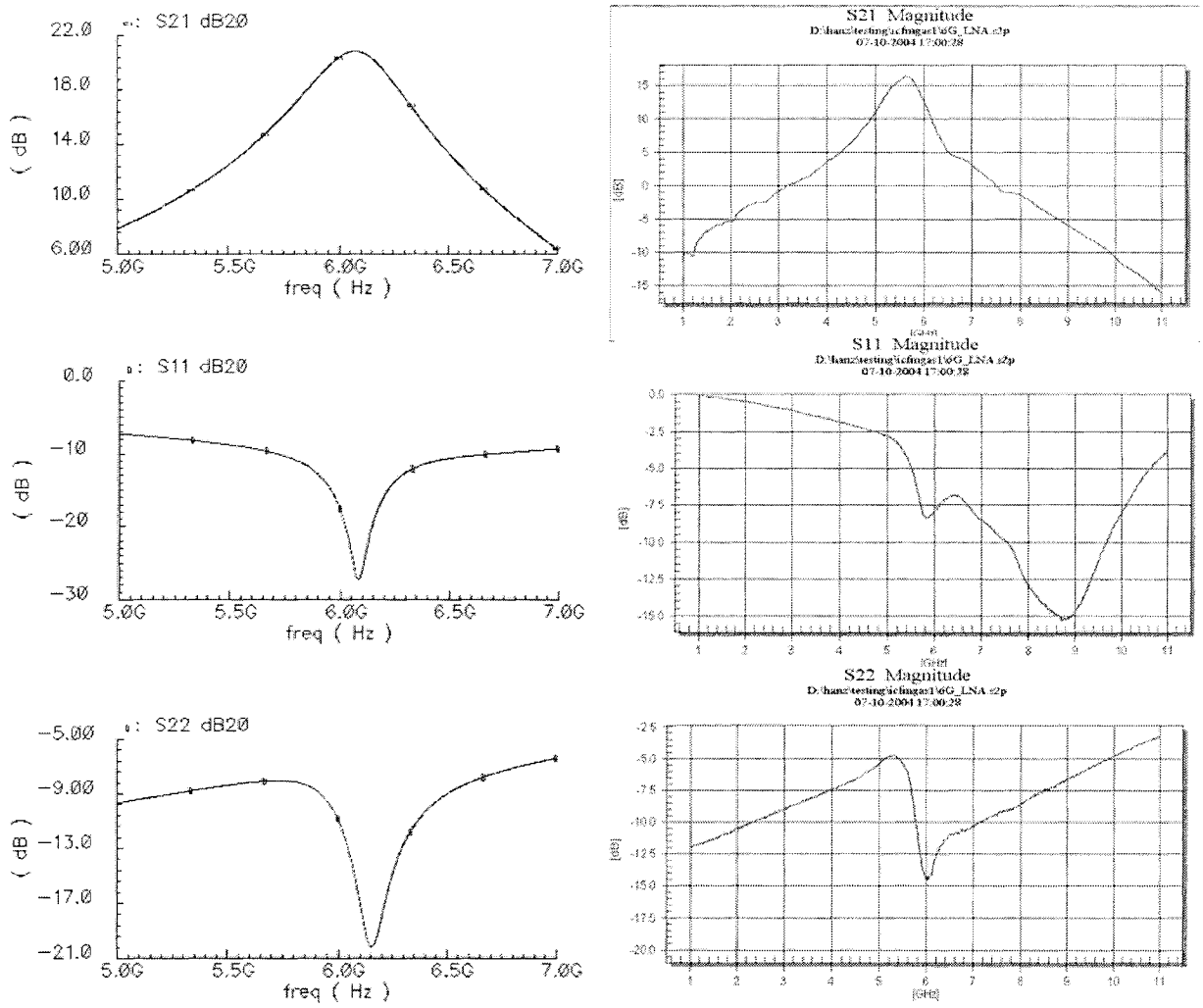
Fig. 2.25: Chip photograph of the 5.8 GHz LNA fabricated in a CMOS p18 technology [27]

both EM simulation and the equivalent π-model. Comparison shows good matching in the 3 to 9 GHz range. Both the magnitude and phase curves overlap each other completely. The thick metal model was used. Usually, using a thick metal model structure will decrease the quality factor by around 1 to 1.5, while maintaining the same inductance value.

2.5.2 LNA Simulation and Measurement

Fig. 2.25 shows the micro-photograph of the 5.8 GHz LNA fabricated using a standard TSMC CMOS p18 technology. The LNA was designed for a 1 V DC power supply, and more than 15 dB gain at 6 GHz.

Both input and output matching have been realized using on-chip inductors. Poly PGS has been used under the input matching inductor to help lower the substrate loss and shield the inductor from substrate coupled noise. All inductors are put far apart from each other, and keeping reasonable distance to active circuitry and other traces such as the Vdd lines. The input transistor, the cascode transistor, and the output buffer transistor are put close to each other to minimize inter-stage parasitics. Grounded multi substrate guard rings and deep N-wells are used to isolate each of the transistors. The layout of the components has been arranged to give the simplest signal flow which, in Fig. 2.25, is from left to right. RF input and output ports are placed on opposite sides of the chip to improve isolation. DC pads are



(a) (b

Fig. 2.26: (a) Simulated S-parameters for S21, S11 and S22; (b) On-chip measurement results

implemented using all metal layers, while RF input and output pads only use top most metal layer to minimize parasitic effects. A grounded metal 1 layer is inserted between the RF pads and the substrate to minimize possible substrate coupled noise. RF chokes are realized using the DC probes used for on-chip probing measurements. Two more DC probes were needed for the buffer power supply and ground. For RF measurement, two Cascade 40 GHz GSG probes were used. Probes and system calibration was made using LRM calibration procedures, with a standard calibration substrate and Cascade Wincal 3.1 computer aided measurement automation software. A 20 GHz Agilent 8720ES vector network analyzer was also used in the measurement.

S-parameters from Cadence Spectre simulations and prototype on-chip measurements are

shown in Fig. 2.26. It is clear that the simulation correctly predicted the performance of the LNA. The gain of the prototype is 3 dB lower than simulation, while they have almost the same peaks - 5.8 GHz for measurement and 6 GHz for the simulation. The drop of the gain may come from the incomplete modeling of the RF chokes, which is a DC needle modeled as a 4 nH inductor in simulation. Leakage of the RF signal through the Vdd pad and DC needle will drop the gain of the circuit. The deviation of the peak frequency may be due to the missing or inaccurate modeling of the parasitic capacitances of the layout extraction. Diva was used for this procedure. For more accurate extractions, Mentor Calibre may be a better choice. Inaccuracies in the MOS transistor models at RF frequency range may also contribute to the simulation errors. Differences in S11 is the result of the capacitive effects of the poly silicon PGS, which was not considered in simulation. Adding poly silicon PGS under the input matching inductor L_{gate} will increase the parasitics and change the original matching arrangement. Accurate modeling and consideration of the PGS capacitive effects are needed to eliminate these errors. Simulations and measurements of the output matching correspond well. The difference in magnitude comes from the incorrect modeling of the parasitic effects in the layout extraction.

One of the common limitations in all RF designs is that the performance of the circuits are heavily dependent on the quality factors of the on-chip inductors, which are usually low in CMOS technologies. In the next chapter, a quality factor enhanced coupled inductor structure is going to be discussed. Discussions already presented in this chapter, including EM simulation, data processing and extraction, data fitting, and design guidelines will serve as basis for the analysis of the proposed structure in chapter 3.

CHAPTER 3

High Quality-Factor Coupled Inductors Design

Based on the discussions in previous chapters, four-port coupled inductor structures featuring high quality factors and small chip area, are proposed. The modified Wheeler's equation is used to generate simple and fast analytical models, and also to initialize the geometry parameters such as the inner and outer diameters, number of turns, etc. Momentum is used for optimization and verification. An extraction procedure used to calculate the inductance and quality factor of the four-port differential driven coupled inductors is developed and used for post-simulation and measurement data processing. Simulation and measurement results of the fabricated prototypes are presented at the end.

3.1 Mutual Inductance and Coupled Structures

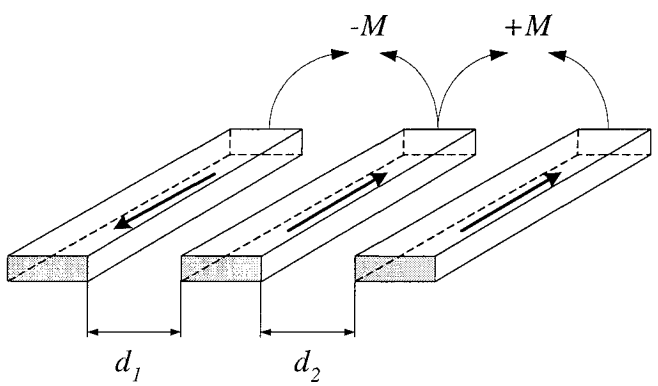


Fig. 3.1: Depending on the direction of the current, mutual inductance could be positive or, negative

As discussed in chapter 2, in ordinary inductors, mutual inductance exists between metal strips in which the signal current flows either in the same direction (positive mutual inductance $+M$) or, in the opposite direction (negative mutual inductance $-M$), as shown in Fig. 3.1. This mutual inductance contributes to the final effective self-inductance of the inductor structure.

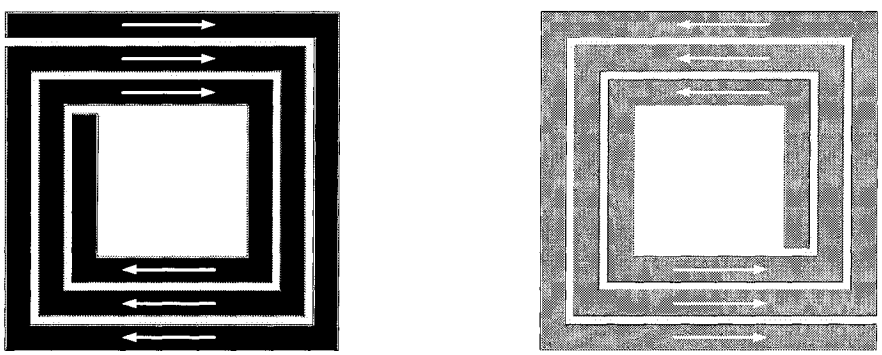
Mutual inductance could also exist between different inductors. Suppose there are two identical inductors L_1 and L_2 and each of them has the same self-inductance L_{self} and quality factor Q_{self} (Fig. 3.2). The loss of each of the inductors is modeled by an equivalent resistor R_s. The relation is given by

$$Q_{self(1,2)} = \frac{2\pi f \cdot L_{self(1,2)}}{R_{S(1,2)}} . \tag{3.1}$$

To make use of the mutual inductance, L_1 and L_2 could be intertwined in a way so that signal currents in L_1 and L_2 are in the same direction, as shown in Fig. 3.3 (a). Positive mutual inductance will be built up between L_1 and L_2 and will be added to the original self-inductance L_{self}. L_{eff} will be used to define this new effective inductance of each of the intertwined inductors in this coupled structure:

$$L_{eff(1,2)} = L_{self(1,2)} + M . \tag{3.2}$$

Here, M is the mutual inductance resulting from the coupling of L_1 and L_2. From (3.2), the effective inductance L_{eff} will be larger than the original designed value L_{self} due to the addition of the extra positive mutual inductance M. This implies that a simpler and smaller



L_1 L_2

Fig. 3.2: Identical inductor pair used in differential designs.

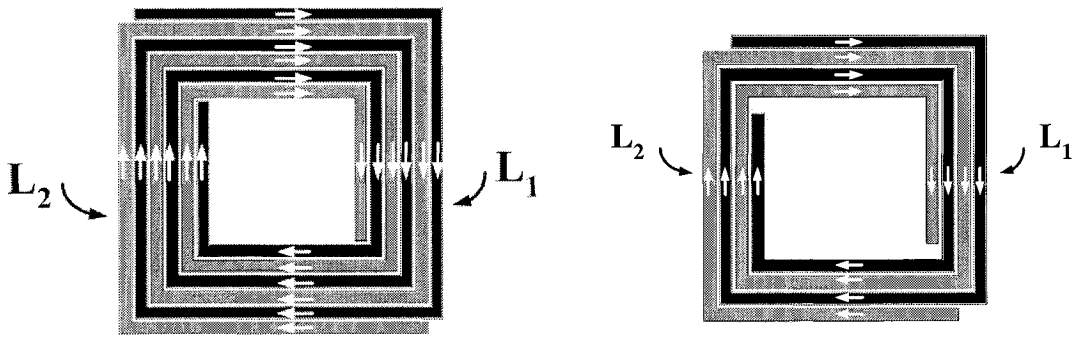


Fig. 3.3: (a) To make use of the mutual inductance, L_1 and L_2 are intertwined to each other. Currents are in the same direction. (b) Simplified structure which has an effective inductance equal to L_{self}.

structures could be used to generate the original value L_{self} using a coupled structure (Fig. 3.3 (a)). In on-chip inductor designs, simpler and smaller structures always mean shorter strip lines and less chip area. Both of these are directly related to the decreasing of loss, and thus increasing of the quality factor. Based on this idea, a redesigned and simplified structure is shown in Fig. 3.3 (b), in which each of the intertwined inductors will have the same originally designed inductance value, which is L_{self}

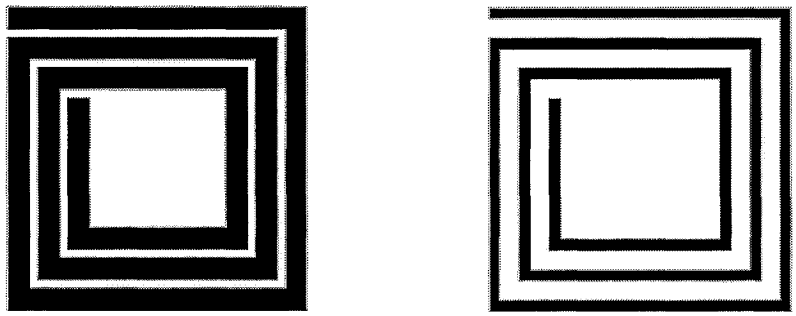
$$L_{self} = L_{eff}' = L_{self}' + M' , \tag{3.3}$$

where L_{eff}' is the new effective inductance consisting of the new self-inductance L_{self}' and the new mutual inductance M', resulting from the coupling of the two inductors. The loss of each of the coupled inductors in Fig. 3.3 (b) will be expressed as R_S'. With the same available inductance, smaller loss has been achieved by using less windings and chip area. The quality factor could now be calculated and compared between the structures in Fig. 3.2 and Fig. 3.3 (b) (for the same available inductance). The following relation could be derived:

$$Q_{eff}' = \frac{2\pi f L_{eff}'}{R_s'} = \frac{2\pi f L_{self}}{R_s'} \tag{3.4}$$

$$Q_{self} = \frac{2\pi f L_{self}}{R_s} . \tag{3.5}$$

Here, Q_{eff}' is the effective quality factor of each of the new intertwined inductors in Fig. 3.3 (b). With



(a) (b)

Fig. 3.4: (a) Original inductor; (b) Spacing has been increased to make the coupling possible

$$R_S > R_S' \,. \tag{3.6}$$

Thus coupled structures will have higher quality factors than their standard counterparts

$$Q_{eff}' > Q_{self} \,. \tag{3.7}$$

One thing needs some explanation here: when a designer intertwines or couples L_1 and L_2, the original inductor structures will be changed to make the intertwining possible. For example by increasing the spacing to make L_1 and L_2 fit each other, as shown in Fig. 3.4. Also, in Fig. 3.3, the simplified coupled structure (b) was generated just by using one less loop compared to (a). It should be noted that here (b) is just used for demonstrating the idea and benefits of coupling. In a real design, coupled structures still need optimization based on EM simulations to get the highest quality factor at around the specified frequency. Also, to use the mutual inductance to increase the quality factor, all signal currents flowing in the coupled inductors need to be coming from the same signal processing stage of the circuit in order to eliminate possible undesired feedback effects. Besides the higher quality factor, coupled structures bring some other benefits such as better component matching compared to separated inductors, because of the common center and interdigitated layout nature, especially for circuits that require higher inductor matching.

3.2 Design Procedure and Circuit Model

3.2.1 Modified Wheeler's Formula

Considerable effort has gone into the design and modeling of inductors. For a given shape, an inductor is completely specified by the number of turns, the turn width, the turns spacing, and any one of the outer diameter, the inner diameter, the average diameter, or the fill ratio. Usually, the thickness of the inductor has only a very small effect on the value of the inductance, and will therefore be ignored in the calculation. Wheeler presented several formulas, which were originally intended to calculate the inductances of discrete inductors, in 1928 [42]. Later, in 1999, S. Mohan et al. [43] found that, after a simple modification to the original formulation, a modified Wheeler's formula could also be used to calculate planar spiral integrated inductors. For the inductors in Fig. 3.5, the self-inductance could be calculated using the modified Wheeler's formula as follows

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho}, \tag{3.8}$$

where L is the total self-inductance, n is the number of turns and

$$d_{avg} = \frac{(d_{out} + d_{in})}{2} \tag{3.9}$$

defined as the average diameter, and

$$\rho = \frac{(d_{out} - d_{in})}{(d_{out} + d_{in})} \tag{3.10}$$

is the fill ratio which represents how hollow the inductor is. For a small value, it represents a hollow inductor (d_{out}=d_{in}), and for a large value it stands for a full inductor (d_{out}>>d_{in}). Two inductors with the same average diameter, but different fill ratios, will have different inductance values. The full one has a smaller inductance because its inner turns are closer to the center of the spiral, and so contribute less positive mutual inductance and more negative mutual inductance. Another reason is that a full inductor will have shorter and wider

Table 3.1: Coefficients for the modified Wheeler's Formula

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

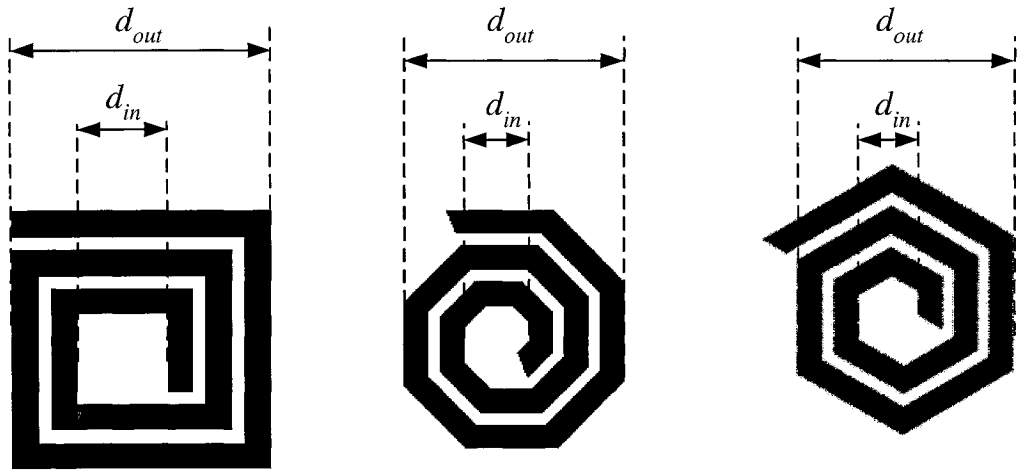


Fig. 3.5: Modified Wheeler's formula parameter definitions for square, octagonal, and hexagonal inductors

striplines, i.e. less self-inductance, compared to a hollow one. Coefficients K_1 and K_2 are layout geometry dependent and are listed in Table 3.1.

The accuracy of the modified Wheeler's formula has been verified using both a field solver and measurement results from real fabricated inductors, with the definition of absolute error *err* as follows

, (3.11)

where $\hat{L}$ is the calculated inductor value using the modified Wheeler's formula, and L is the inductance value from the field solver or measurement. Results show that, compared to field solver simulation, around 80% of the calculated values have *err* less than 4% with the maximum *err* being 12%. While for measurements, 80% of the inductors have *err* less than 8%, with the maximum *err* equal to 20% [43].

Another widely used equation to calculate the inductance of planar inductors is the Greenhouse equation [7]. The inductance is expressed as the sum of the self-inductance of each of the striplines constructing the inductor and the mutual inductances between any 2 segments [35]:

$$L = \sum_{i=1}^{4n} L_{self}(i) + \sum_{i=1}^{4n} \sum_{j=i+1}^{4n-1} M(i,j) \tag{3.12}$$

where n is the number of turns, and L_{self} is the self-inductance of a stripline, which could be calculated using the Greenhouse equation

$$L_{self} = 2 \cdot 10^{-7} \cdot l \cdot \left[ln\left(\frac{2l}{W+T}\right) + 0.50049 + \frac{W+T}{3l} \right], \tag{3.13}$$

where T is the thickness of the inductor metal layer, and W and l represent the width and length respectively. For the mutual inductance, the following equation is used

$$M = \pm 2 \times 10^{-7} l \left\{ ln\left[\left[\left(\frac{l}{GMD}\right) + \left[1 + \left(\frac{l}{GMD}\right)^2\right]^{0.5}\right]\right] - \left[1 + \left(\frac{l}{GMD}\right)^2\right]^{0.5} + \left(\frac{GMD}{l}\right) \right\}, \tag{3.14}$$

where GMD is the geometric mean distance expressed by:

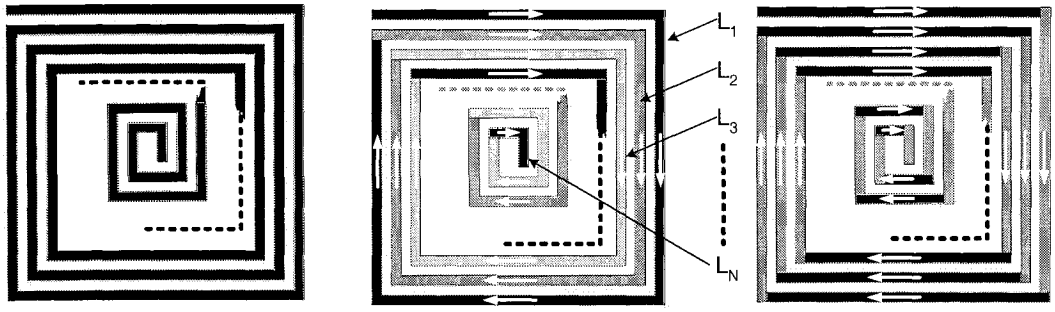
$$GMD = e^{ln(G' - \beta)} \tag{3.15}$$

and

$$\beta = \frac{1}{12}\left(\frac{G'}{W}\right)^2 + \frac{1}{60}\left(\frac{G'}{W}\right)^4 + \frac{1}{168}\left(\frac{G'}{W}\right)^6 + \frac{1}{360}\left(\frac{G'}{W}\right)^8 + \frac{1}{660}\left(\frac{G'}{W}\right)^{10} + \ldots, \tag{3.16}$$

where G' is defined as the center to center spacing between the two striplines under consideration. Depending on the direction of the current in the parallel strips, M could be positive or negative.

Comparing the two methods, it is clear that the modified Wheeler's approach is much easier to use for both square and non-square inductor designs. The inductance will only be decided by the inner, outer diameters, and the number of turns. This is the most crucial feature which could be used in coupled structures designs, as will be shown later in this chapter. One thing should be noted is that both the modified Wheeler's formula and the Greenhouse equation can not give the quality factor of the inductor. This is easy to understand for on-chip planar inductors, since the quality factor is also a function of the working frequency and substrate characteristics, which could not be realistically included in one equation. A EM simulation remains the fast and accurate approach to get and optimize the quality factor.



(a) (b) (c)

Fig. 3.6: (a) Normal standard inductor. (b) View as *N* inductor sections put in serial. (c) Extreme situation where every stripline is treated as one inductor

3.2.2 Design Procedure

To make use of coupled inductor structures, designers need accurate and easy to use design procedures. Before starting the discussion, some changes could be made to (3.12) to expand it to a more generic form. As shown in Fig. 3.6, the inductor in Fig. 3.6 (a) could be viewed as an *N* section inductors (L_1, L_2, L_3,...., L_N) in series, as shown in Fig. 3.6 (b). The total inductance could be calculated by adding all the self-inductances and mutual inductances of the inductor sections in Fig. 3.6 (b), and be expressed as [27]:

$$L = \sum_{i=1}^{N} L_i + \sum_{i=1}^{N} \sum_{j=1, i \neq j}^{N} M_{i,j} \quad , \tag{3.17}$$

where N is the number of serial inductor sections, and $M_{i,j}$ is the mutual inductance which occurs between the ith and jth inductor sections, with the currents flowing along the arrows. In the extreme situation, when every single stripline is treated as an inductor, as shown in Fig. 3.6 (c), equation (3.17) becomes the same as (3.12). When there are only two inductor sections, equation (3.17) could be simplified as follows

$$L = L_1 + L_2 + M_{1,2} + M_{2,1} \cdot \tag{3.18}$$

Given that the inner, the outer diameters, and the number of turns of the structure, and the direction of the signal current flow are the same (which means L, the total self-inductance of the inductor in Fig. 3.6 (a) will be kept the same), equation (3.18) will not depend on how the two inductor sections are assigned.

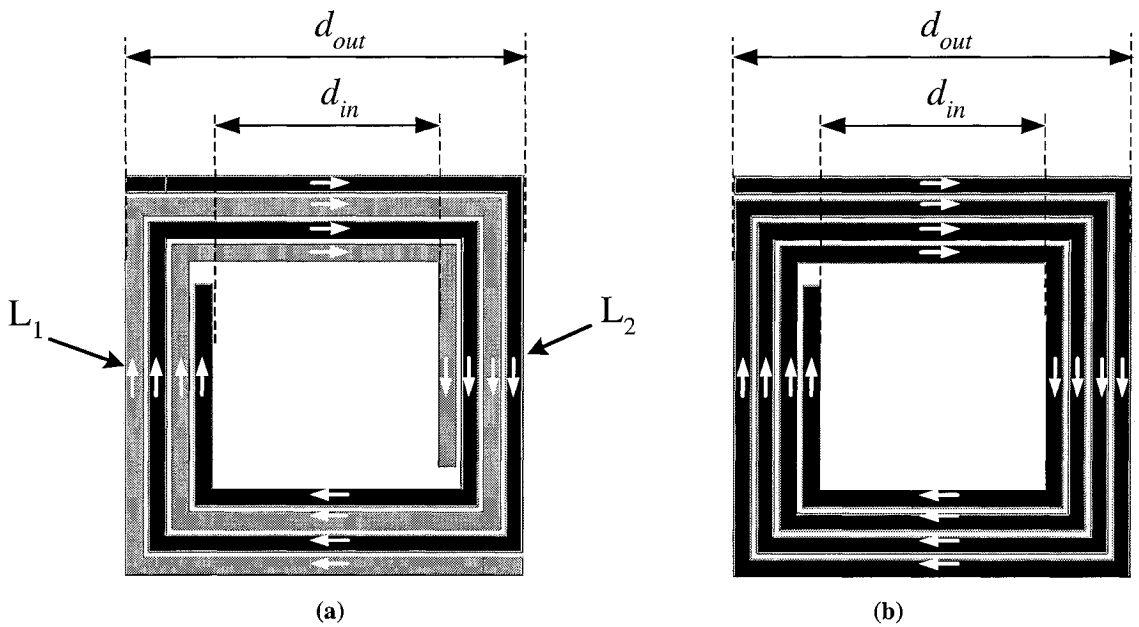


Fig. 3.7: (a) Single looped standard inductor. (b) coupled structure composed of two square inductors, with the same equivalent inner and outer diameters.

Now, suppose there is one coupled structure composed of two identical square inductors, as shown in Fig. 3.7 (a), with the geometry parameter values and current directions as given on the graph. These two inductors could be viewed as two sections in a single loop standard inductor, with the same inner and outer diameters and number of turns as shown in Fig. 3.7 (b). Fig. 3.8 shows how to re-arrange the strip corner connections to combine

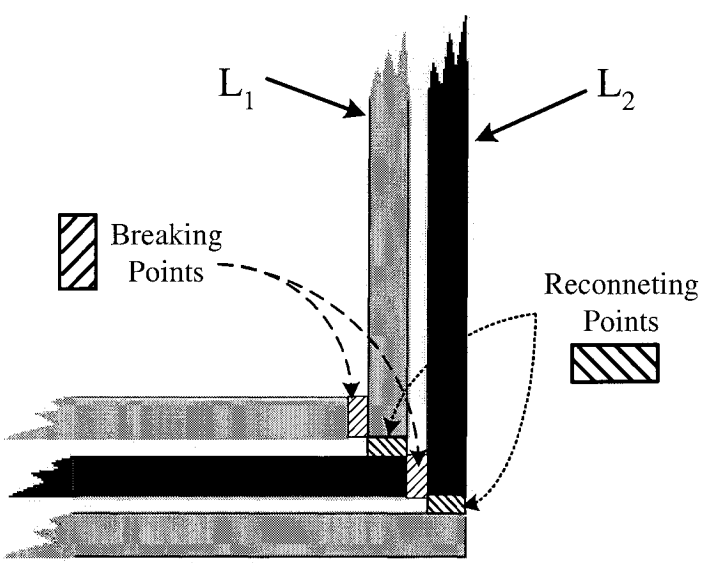


Fig. 3.8: Rearranging the corners to combine L_1 and L_2 into one single looped standard inductor.

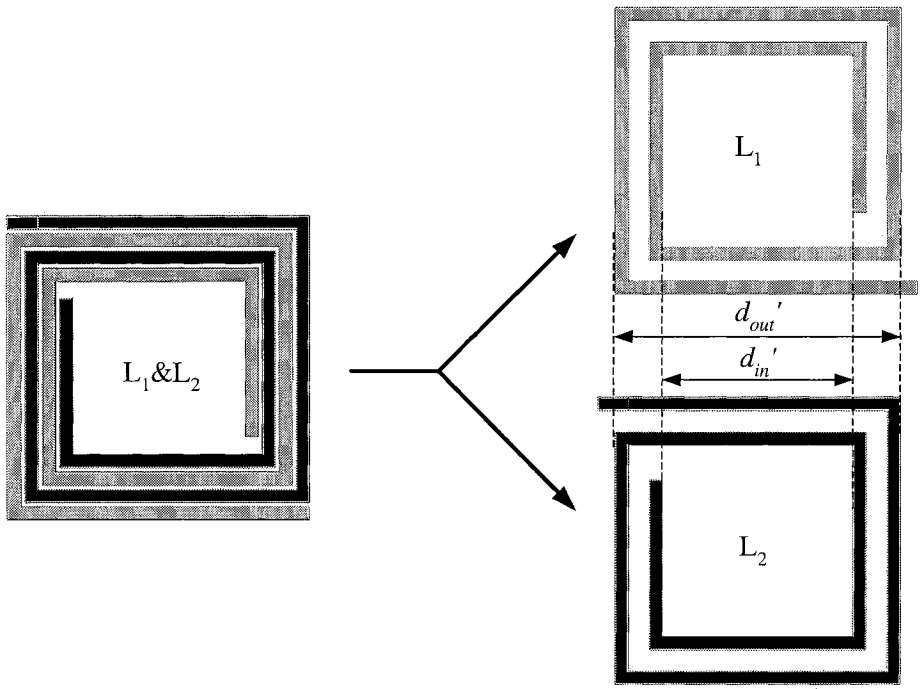


Fig. 3.9: The modified Wheeler's formula could also be used for each of the two coupled inductors L_1 and L_2 for self-inductance calculation.

Fig. 3.7 (a) into Fig. 3.7 (b).

The self-inductance of the inductor in Fig. 3.7 (b) could be calculated using the modified Wheeler's formula in (3.8). According to (3.18), this inductance L also equals the sum of the self-inductance of each of the two coupled inductors in Fig. 3.7 (a) and the mutual inductances between them. Clearly seen from Fig. 3.9, the modified Wheeler's formula could also be applied to each of the two coupled inductors L_1 and L_2 as if they were stand alone single loop inductors with different numbers of turns. Substituting the values of L, L_1, and L_2 into (3.18) and using proper transformation, the mutual inductance would be

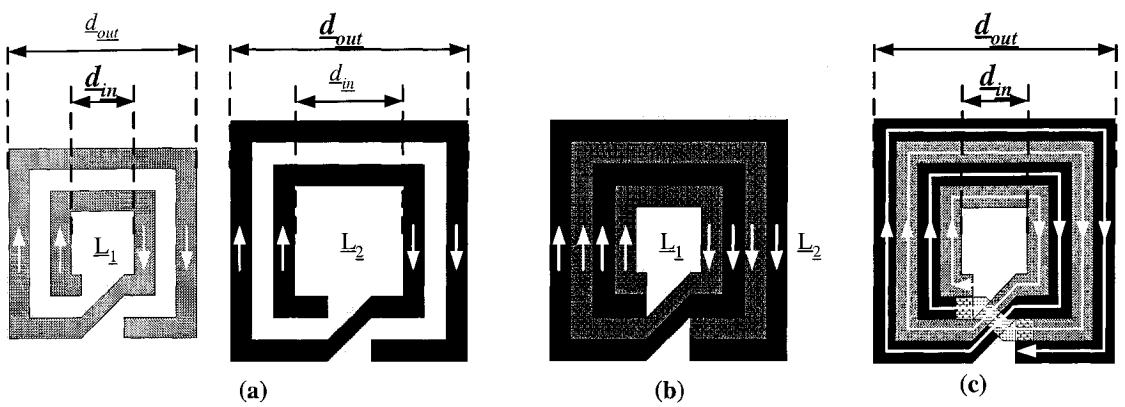


Fig. 3.10: (a) Two inductor sections; (b) Coupled structure; (c) Two sections connected into one inductor so that the current flows in the same direction as in (b).

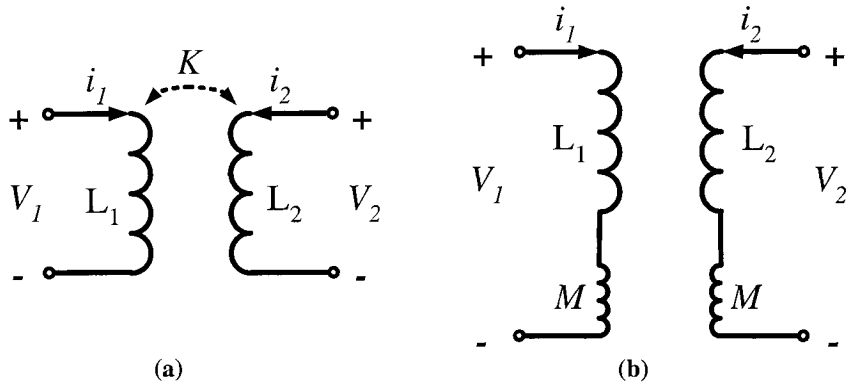


Fig. 3.11: (a) Transformer with coupling coefficient K; (b) Mutual inductance is added to each side of the transformer.

expressed as

$$M = \frac{L - L_1 - L_2}{2} . \tag{3.19}$$

Here, the following relation between the mutual inductances has been used

$$M_{1,2} = M_{2,1} . \tag{3.20}$$

The coupling coefficient K could thus be calculated using

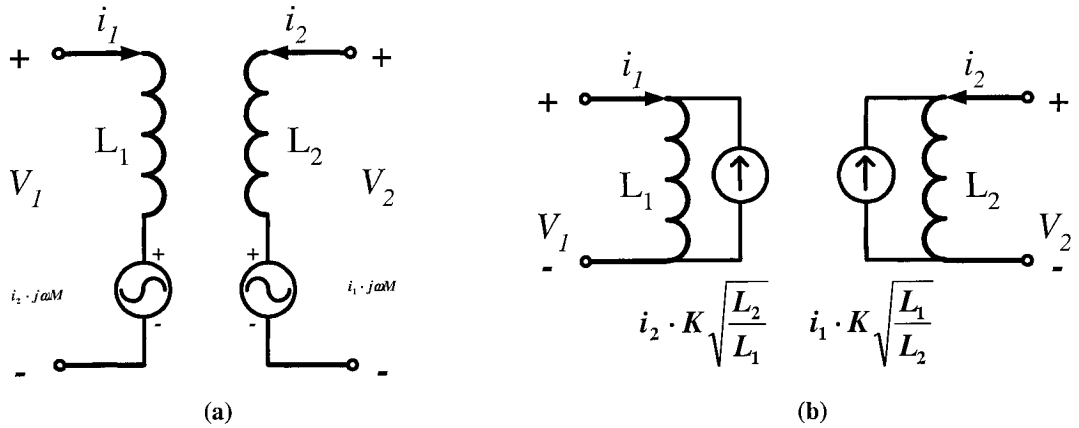
$$K = \frac{M}{\sqrt{L_1 \cdot L_2}} . \tag{3.21}$$

Table 3.2: Parameters used in the modified Wheeler's formula

	d_{in} (um)	d_{out}(um)	n
L	75.5	274.5	4
L_1	75.5	224.5	2
L_2	125.5	274.5	2

Table 3.3: Calculation and EM simulation results

	Calculation	EM Simulation
L (nH)	3.21	3.29
L_1 (nH)	0.745	0.75
L_2 (nH)	1.16	1.19
M (nH)	0.653	0.675
K	0.7010	0.7145



(a) (b)

Fig. 3.12: (a) Use CCVS to model the mutual inductance with complex gain; (b) CCCS model of mutual inductance

3.2.3 A Simulation Example

One specific coupled structure has been calculated and simulated to verified the idea proposed above. Two inductor sections, Fig. 3.10 (a), are coupled together as shown in Fig. 3.10 (b). In Fig. 3.10 (c), these two inductors are connected properly so that they form a standard inductor with current flowing in the same direction as in Fig. 3.10 (b). Simulation and calculation results for the design are summarized in Table 3.2 and Table 3.3. Clearly, very good agreement is observed.

3.2.4 The Circuit Model

Transistor lever simulations need equivalent circuit models which could be used in modern main stream tools such as Cadence Spectre and Hspice. Transformer model could be used to accurately model the coupled inductor structures.

Fig. 3.11 (a) shows a coupled inductor structure with a coupling coefficient K. Mutual inductance M will be built up and added to the self-inductance of each of the inductors, as shown in Fig. 3.12 (b). Considering the effect of mutual inductance, the v-i relation of each inductor could be expressed as

$$\begin{cases} v_1 = i_1 \cdot j\omega L_1 + i_2 \cdot j\omega M \\ v_2 = i_2 \cdot j\omega L_2 + i_1 \cdot j\omega M \end{cases} \quad (3.22)$$

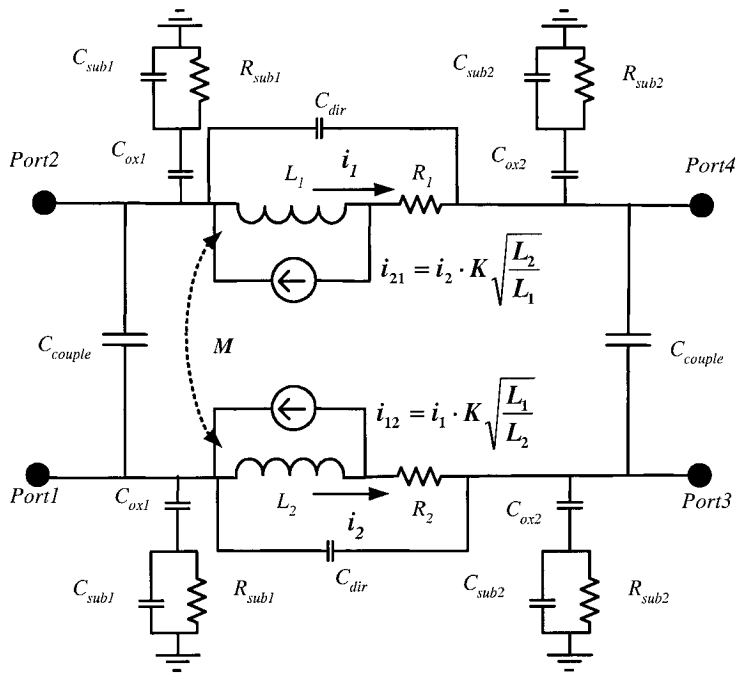


Fig. 3.13: Wide band π -model based coupled structure equivalent circuit.

The mutual inductance describes the voltage which is generated by the current in the other inductor loop in a coupled structure. Based on (3.22), this current-voltage relationship could be modeled as a current controlled voltage source (CCVS), with a transimpedance equal to *jwM*. However, designers may find this model hard to use for its complex trans-impedance gain. To simplify this relation, (3.21) could be used to transform (3.22) into

$$\begin{cases} v_1 = j\omega L_1\left(i_1 + i_2 \cdot K\sqrt{\dfrac{L_2}{L_1}}\right) \\ v_2 = j\omega L_2\left(i_2 + i_1 \cdot K\sqrt{\dfrac{L_1}{L_2}}\right) \end{cases} \tag{3.23}$$

Equation (3.23) transforms the mutual inductance into a current controlled current source (CCCS), with current gain equal to $K\sqrt{\frac{L_i}{L_j}}$, where i and j equal 1 or 2. This current gain will be only decided by the coupling coefficient K and the inductor values L_1 and L_2. All parameters needed for the CCCS gain could be calculated using the modified Wheeler's formula according to Fig. 3.10 and (3.21), as discussed in section 3.2.2.

Table 3.4: Model components summary for the circuit in Fig. 3.13

Model components name	Value
L_i $(i=1,2)$	Self-inductance
M_{12} & M_{21}	Mutual inductance
R_i	Resistive loss of the loop including skin effect.
C_{ox}	Dielectric capacitor to substrate
C_{sub} & R_{sub}	Capacitive and loss effect in substrate
C_{dir}	Direct coupling between two ends of the inductor itself
C_{couple}	Capacitive coupling between two coupled inductors

After calculating and modeling the self-inductance and mutual inductance of the coupled structure, the rest of the work will be to consider the parasitic effects of the structure. As discussed in chapter 2, π-model based inductor equivalent circuit could be used to model each of the coupled inductors in the structure. One more effect needs to be considered and modeled, which is the direct capacitive coupling between the two inductors which results from putting two inductors side by side. This coupling is modeled using two capacitors (C_{couple}) connected between each of the two ends of the coupled inductors in the model. The complete equivalent circuit is shown in Fig. 3.13. Table 3.4 summarizes all the component used in the model. All the parasitic capacitors and resistors could be calculated using well established inductor design equations as discussed in chapter 2.

3.3 4-Port Network Representation of the Coupled Structure

3.3.1 4-port S-parameters for the Coupled Structure

From a general point of view, a coupled structure is a 4-port network, as shown in Fig. 3.14. Using incident and reflective traveling waves as in Fig. 3.14, the following S-parameter equations could be obtained:

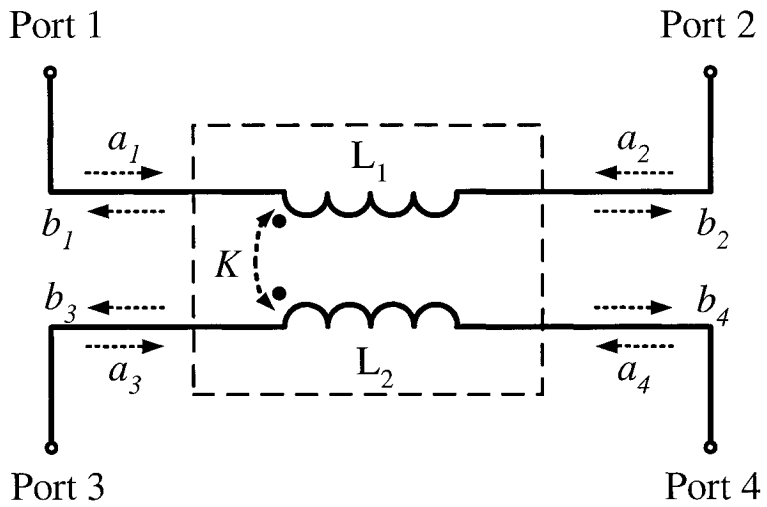


Fig. 3.14: View of a coupled structure as a 4-port network

$$\begin{cases} b_1 = a_1 \cdot S_{11} + a_2 \cdot S_{12} + a_3 \cdot S_{13} + a_4 \cdot S_{14} \\ b_2 = a_1 \cdot S_{21} + a_2 \cdot S_{22} + a_3 \cdot S_{23} + a_4 \cdot S_{24} \\ b_3 = a_1 \cdot S_{31} + a_2 \cdot S_{32} + a_3 \cdot S_{33} + a_4 \cdot S_{34} \\ b_4 = a_1 \cdot S_{41} + a_2 \cdot S_{42} + a_3 \cdot S_{43} + a_4 \cdot S_{44} \end{cases}, \tag{3.24}$$

where a_i is an incident traveling wave and b_i is a reflective traveling wave at the ith port, where $i=1,2,3,4$. Meanwhile, L_1 and L_2 could also be viewed as 2-port networks with the following S-parameter equations:

$$L_1 \rightarrow \begin{cases} b_1' = a_1 \cdot S_{11} + a_2 \cdot S_{12} \\ b_2' = a_1 \cdot S_{21} + a_2 \cdot S_{22} \end{cases} \tag{3.25}$$

$$L_2 \rightarrow \begin{cases} b_3' = a_3 \cdot S_{33} + a_4 \cdot S_{34} \\ b_4' = a_3 \cdot S_{43} + a_4 \cdot S_{44} \end{cases}, \tag{3.26}$$

where b_i' represents the outgoing traveling wave from each port of the inductor which was only generated by that inductor's own inputs. For L_1, the inputs are a_1 and a_2, while for L_2, the inputs are a_3 and a_4. Substituting (3.25) and (3.26) into (3.24), following equation is obtained:

$$\begin{cases} b_1 = b_1' + a_3 \cdot S_{13} + a_4 \cdot S_{14} \\ b_2 = b_2' + a_3 \cdot S_{23} + a_4 \cdot S_{24} \\ b_3 = a_1 \cdot S_{31} + a_2 \cdot S_{32} + b_3' \\ b_4 = a_1 \cdot S_{41} + a_2 \cdot S_{42} + b_4' \end{cases} \quad (3.27)$$

Clearly seen from (3.27), the mutual inductance, or the coupling effect between the inductors, has been described by S_{13}, S_{14}, S_{23}, S_{24}, S_{31}, S_{32}, S_{41}, and S_{42}. This will be discussed in detail later.

Although in real simulations and measurements it is easy to get the S-parameters characterizing a 4-port network, designers still face the problem of transforming the S-parameters into meaningful design specifications such as the self-inductance, the mutual inductance, and the quality factor, which are needed to quantify the design. This section will discuss a data processing technique which could be used to transform 4-port coupled inductor structures into an equivalent differentially driven 2-port network. The differential effective inductances and quality factors of the inductors in the coupled structure could then be extracted from this 2-port network. Here, "differentially driven" means that both of the inductors in the coupled structure are differentially excited. This will give the highest quality factor of the structure, as mentioned in chapter 2 and in [26]. While in a real application, depending on how the coupled structure is used, the quality factor may be less than the value extracted here. However, coupled inductors could be well characterized using this value when compared to differentially driven standard non-coupled inductors with the same value and used in the same application.

3.3.2 Differential S-Parameters: S_{11} and S_{22} of The Coupled Inductors

Consider inductor L_1 of the coupled structure, shown in Fig. 3.15 (a), as a two port net-

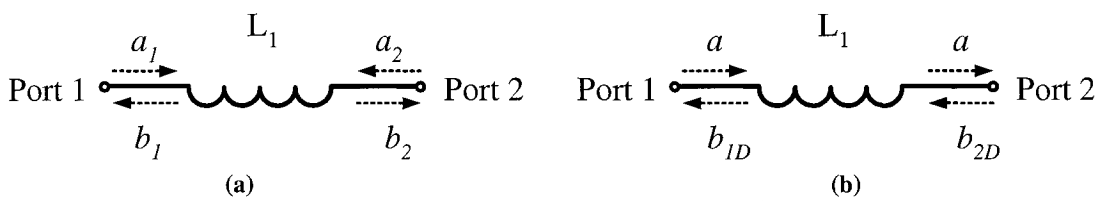


Fig. 3.15: (a) L_1 in a coupled structure as a 2-port inductor; (b) Differentially driven L_1.

work. Fig. 3.15 (b) shows the situation when L_1 is differentially driven. Arrows show the actual direction of the incident and reflective waves. The following relation could be derived from Fig. 3.15 (b),

$$a_1 = -a_2 = a \tag{3.28}$$

and

$$\begin{cases} b_1 = b_{1D} \\ b_2 = -b_{2D} \end{cases}. \tag{3.29}$$

Differential incident and reflective waves could be defined as:

$$\begin{cases} a_{1diff} = 2a = a_1 - a_2 \\ b_{1diff} = b_1 - b_2 = b_{1D} + b_{2D} \end{cases}. \tag{3.30}$$

By defining these differential incident and reflective waves, the inductor's two ports could be combined into one equivalent differentially driven port, thus the differential S-parameters could be defined. Substituting (3.30) into (3.25), using the necessary transformations, the following relation between the differential input and output is derived:

$$b_1 - b_2 = S_{11}a - S_{12}a - S_{21}a + S_{22}a = \frac{S_{11} - S_{12} - S_{21} + S_{22}}{2} \cdot 2a \,. \tag{3.31}$$

Substituting (3.30) into (3.31), the following differential incident and reflective relation is obtained:

$$b_{1diff} = S_{11diff} \cdot a_{1diff}, \tag{3.32}$$

where

$$S_{11diff} = \frac{S_{11} - S_{12} - S_{21} + S_{22}}{2} \,. \tag{3.33}$$

Thus, a 2-port differentially driven inductor could be viewed as a 1-port network, with its port described using differential incident and reflective waves, and a differential S11. The same transformation could also be applied to (3.26), which leads to:

$$S_{22diff} = \frac{S_{33} - S_{34} - S_{43} + S_{44}}{2} \quad (3.34)$$

3.3.3 Differential S-Parameters: S_{21} and S_{21}

Let us rearrange Fig. 3.14 into Fig. 3.16. Suppose inputs a_1 and a_2 are applied to Port 1_{Diff}. Because of the mutual inductance coupling, there will be an output coming out from Port 2_{Diff}, shown as b_3 and b_4.

The forward transmission from Port 1 to Port 3 is:

$$b_{31} = a_1 \cdot S_{31} , \quad (3.35)$$

where b_{31} is the output wave from Port 3 generated due to the input signal in Port 1. The same applies from Port 2 to Port 3

$$b_{32} = a_2 \cdot S_{32} . \quad (3.36)$$

Under the differential input situation, combining (3.28), (3.35), and (3.36), b_3 could be express as

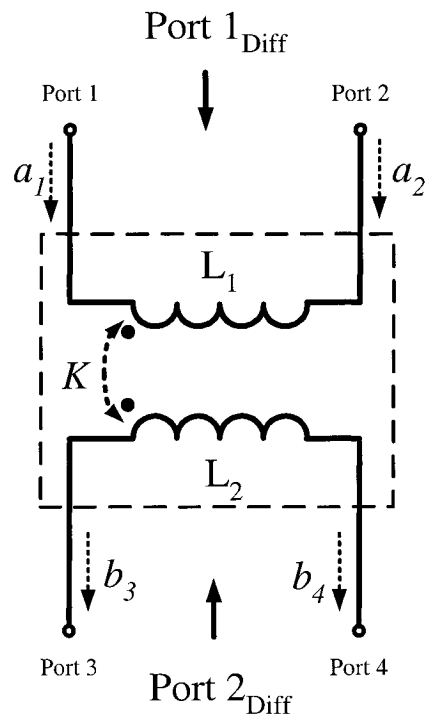


Fig. 3.16: Differentially driven coupled inductor.

$$b_3 = a(S_{31} - S_{32}) , \tag{3.37}$$

where a is the differential input. The same approach could be used to derive b_4 which is generated from the differential input a:

$$b_4 = a(S_{41} - S_{42}) . \tag{3.38}$$

The differential output from Port 2_{Diff} could then be calculated as:

$$b_{21diff} = b_3 - b_4 = a \cdot (S_{31} - S_{31} + S_{31} - S_{31}) = 2a \cdot \frac{(S_{31} - S_{32} + S_{42} - S_{41})}{2} , \tag{3.39}$$

where the subscript $_{21}$ means that this output comes from the differential input of Port 1_{Diff}. Clearly from (3.39), the differential S21 could be expressed as:

$$S_{21diff} = \frac{S_{31} - S_{32} + S_{42} - S_{41}}{2} . \tag{3.40}$$

The same applies to the differential S12 which could be derived as:

$$S_{12diff} = \frac{S_{13} - S_{23} + S_{24} - S_{14}}{2} . \tag{3.41}$$

One thing should be noted is that all the differential S-parameters obtained from the discussion above will not only apply to coupled inductors. Assume a 4-port network with all the S-parameters defined in (3.24), if the network is driven differentially, as shown in Fig. 3.17, this 4-port network could be simplified into a differentially driven 2-port network, and the corresponding differential S-parameters would be

$$\begin{cases} S_{11diff} = \dfrac{S_{11} - S_{12} - S_{21} + S_{22}}{2} \\ S_{22diff} = \dfrac{S_{33} - S_{34} - S_{43} + S_{44}}{2} \\ S_{21diff} = \dfrac{S_{31} - S_{32} + S_{42} - S_{41}}{2} \\ S_{12diff} = \dfrac{S_{13} - S_{23} + S_{24} - S_{14}}{2} \end{cases} . \tag{3.42}$$

This is a summary of equations (3.33), (3.34), (3.40), and (3.41).

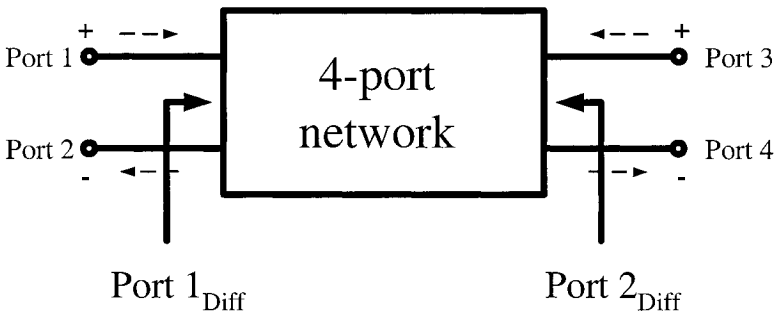


Fig. 3.17: A 4-port network under differential excitation

3.3.4 Self- and Mutual Inductance Extraction

A 2-port network could also be characterized using the Z-parameters:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} . \tag{3.43}$$

When (3.43) is used to describe a coupled structure, and comparing (3.43) to (3.22), in which the *v-i* relation is expressed using the self-inductance and mutual inductance, the relation below is obtained:

$$\begin{cases} Z_{11} = jwL_1 \\ Z_{22} = jwL_2 \\ Z_{12} = Z_{21} = jwM \end{cases} . \tag{3.44}$$

Thus, the following equations could be used to extract the self-inductance and mutual inductance

$$L_1 = \frac{Img(Z_{11})}{jw} \tag{3.45}$$

$$L_2 = \frac{Img(Z_{22})}{jw} \tag{3.46}$$

$$M = \frac{Img(Z_{12})}{jw} = \frac{Img(Z_{21})}{jw} . \tag{3.47}$$

This procedure could also be used in extracting the parameters for differentially driven coupled inductors. A standard S-to-Z transformation will be used to transform the differ-

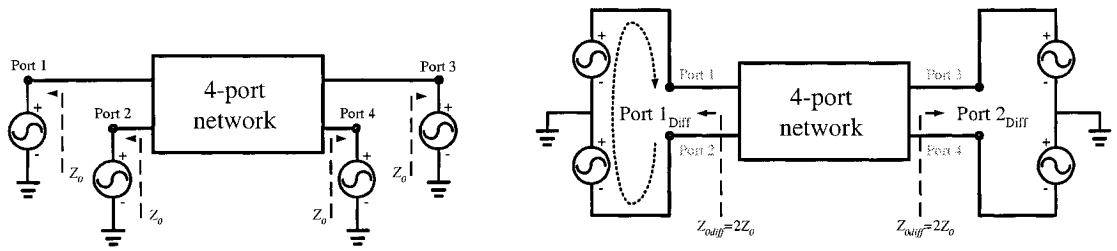


Fig. 3.18: (a) In simulation or measurement, all ports are matched to Z_0=50 Ohm; (b) A differential drive will double the impedance because the signal will go through 2 sources.

ential S-parameters in (3.42) into differential Z-parameters

$$Z_{11diff} = Z_{0diff} \cdot \frac{(1 + S_{11diff}) \cdot (1 - S_{22diff}) + S_{12diff} \cdot S_{21diff}}{\Delta} \tag{3.48}$$

$$Z_{12diff} = Z_{0diff} \cdot \frac{2 \cdot S_{12diff}}{\Delta} \tag{3.49}$$

$$Z_{21diff} = Z_{0diff} \cdot \frac{2 \cdot S_{21diff}}{\Delta} \tag{3.50}$$

$$Z_{22diff} = Z_{0diff} \cdot \frac{(1 - S_{11diff}) \cdot (1 + S_{22diff}) + S_{12diff} \cdot S_{21diff}}{\Delta}, \tag{3.51}$$

where

$$\Delta = (1 - S_{11diff}) \cdot (1 - S_{22diff}) - S_{12diff} \cdot S_{21diff} \tag{3.52}$$

and Z_{0diff} is the differential reference impedance defined as

$$Z_{0diff} = 2 \cdot Z_0 = 100\Omega, \tag{3.53}$$

because in simulation and measurement all the ports of the 4-port network are connected to 50 Ohm impedances, i.e. Z_0 (Fig. 3.18 (a)). When a differential drive is applied, the input port will face two 50 Ohm impedances in series (Fig. 3.18 (b)). Thus, the characteristics impedance needs to be doubled, and is given by Z_{0diff} in (3.53).

Substituting the differential Z-parameters of (3.45) into (3.47), the differential effective self-inductance and mutual inductance could then be calculated as:

$$\begin{cases} L_{1diff} = \dfrac{Img(Z_{11diff})}{jw} \\ L_{2diff} = \dfrac{Img(Z_{22diff})}{jw} \end{cases} \tag{3.54}$$

$$M_{diff} = \frac{Img(Z_{12diff})}{jw} = \frac{Img(Z_{21diff})}{jw} . \tag{3.55}$$

The differential quality factors could then be calculated using the imaginary parts over the real parts of the Z-parameters:

$$\begin{cases} Q_{1diff} = \dfrac{Img(Z_{11diff})}{Re(Z_{11diff})} \\ Q_{2diff} = \dfrac{Img(Z_{22diff})}{Re(Z_{22diff})} \end{cases} . \tag{3.56}$$

The total effective inductance of each of the coupled inductors will equal the self-inductance plus mutual inductance:

$$\begin{cases} L_{1eff} = L_{1diff} + M_{diff} \\ L_{2eff} = L_{2diff} + M_{diff} \end{cases} . \tag{3.57}$$

Then, the effective quality factor of each of the coupled inductors could be calculated through the effective imaginary part over the real part of the impedance of each inductor

$$\begin{cases} Q_{1eff} = \dfrac{Img(Z_{11diff}) + Img(Z_{12diff})}{Re(Z_{11diff})} \\ Q_{2eff} = \dfrac{Img(Z_{22diff}) + Img(Z_{12diff})}{Re(Z_{22diff})} \end{cases} . \tag{3.58}$$

Finally, the coupling coefficient is obtained as

$$K = \frac{M_{diff}}{\sqrt{L_{1diff} \cdot L_{2diff}}} . \tag{3.59}$$

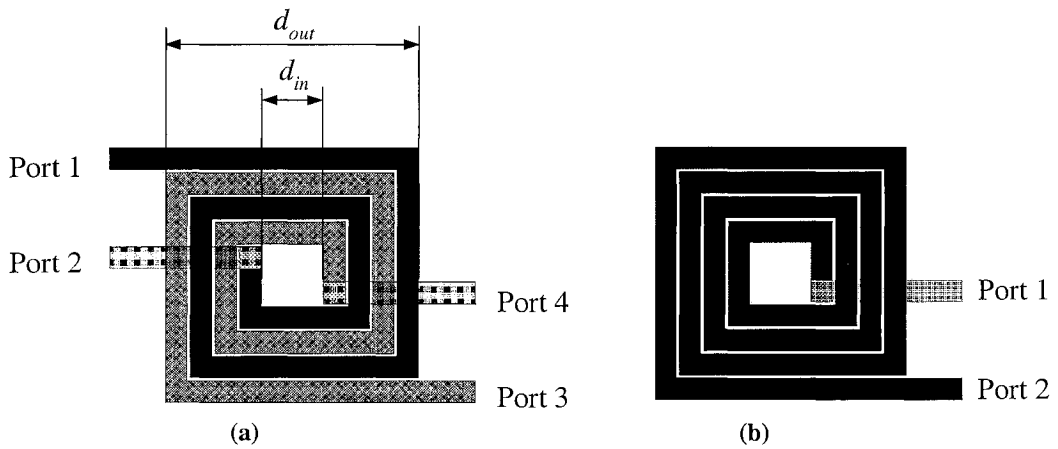


Fig. 3.19: (a) Fabricated coupled inductor layout; (b) Equivalent single loop standard inductor.

3.4 Prototypes and Measurements

Several prototypes have been designed, fabricated, and tested using a standard CMOS p13 technology.

Fig. 3.19 shows one layout of the coupled inductors designed using the ADS Momentum simulator. Two intertwined indictors, port 1 to port 2 and port 3 to port 4, are shown in Fig. 3.19 (a). Fig. 3.19 (b) shows the single equivalent inductor resulting from the combination of the two inductors in Fig. 3.19 (a). Table 3.5 summarizes the geometry dimensions of the design. Using the modified Wheeler's formula, the total effective self-inductance of Fig. 3.19 (b) is found to be

$$\rho = \frac{(232.53 - 57.3)}{(232.53 + 57.3)} = 0.605 \tag{3.60}$$

$$d_{avg} = \frac{(232.53 + 57.3)}{2} = 144.915 \tag{3.61}$$

Table 3.5: Geometry sizing of the structure in Fig. 3.19

	d_{in}[um]	d_{out}[um]	n
Equivalent Single inductor	57.3	232.53	4
Intertwined inductor	79.84	210	2

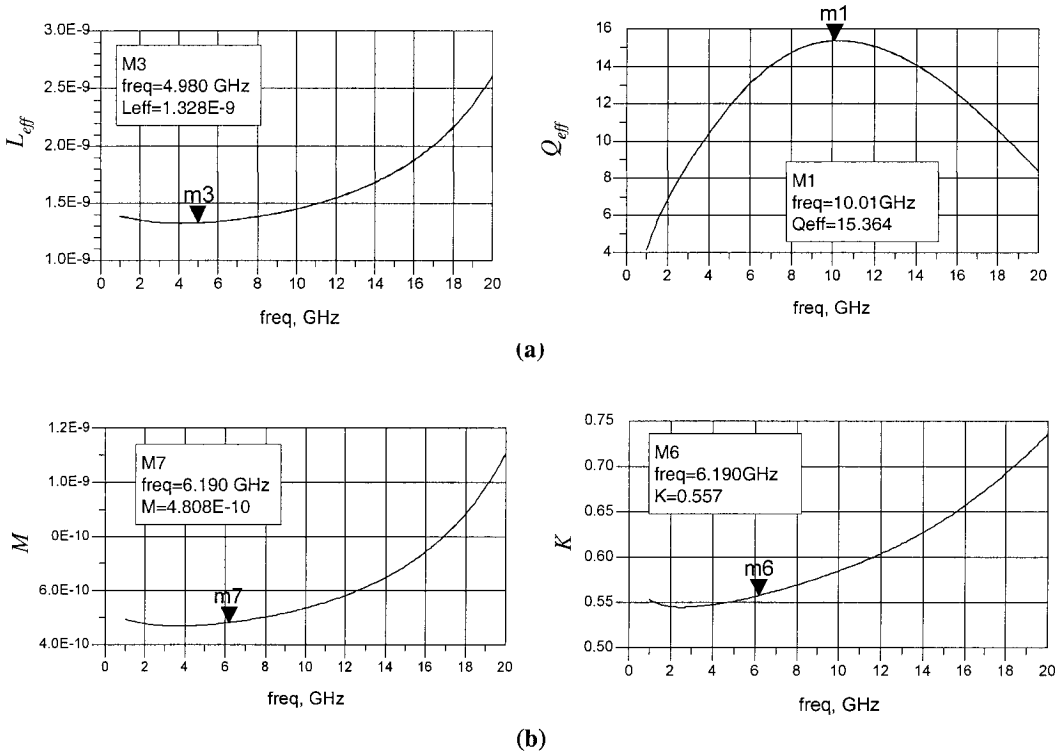


Fig. 3.20: (a) The total effective differential inductance and quality factor; (b) The extracted mutual inductance *M* and coupling coefficient *K*.

$$L_{single}' = K_1\mu_0\frac{4^2 \cdot 114.915[um]}{1+K_2 0.605} = 2.56[nH] \quad . \tag{3.62}$$

For each one of the coupled inductors, the self-inductance is:

$$\rho = \frac{(210-79.84)}{(210+79.84)} = 0.449 \tag{3.63}$$

$$d_{avg} = \frac{(210+79.84)}{2} = 144.92 \tag{3.64}$$

$$L_{1,2}' = K_1\mu_0\frac{2^2 \cdot 114.92[um]}{1+K_2 0.449} = 0.77[nH] \quad . \tag{3.65}$$

One thing needs to be considered in the layout is that in both Fig. 3.19 (a) and (b) a strip-line made by metal layer 7 has been used to lead the inductor's inner end outside. Equation (3.13) could be used to calculate the inductance that this output leading strip may contribute, which gives

$$L_{out-leading} = 2 \cdot 10^{-7} \cdot 118.8[um] \cdot \left[ln\left(\frac{2 \cdot (118.8)}{20+0.8}\right) + 0.50049 + \frac{20+0.8}{3 \cdot (118.8)}\right] = 0.071[nH] \quad . \tag{3.66}$$

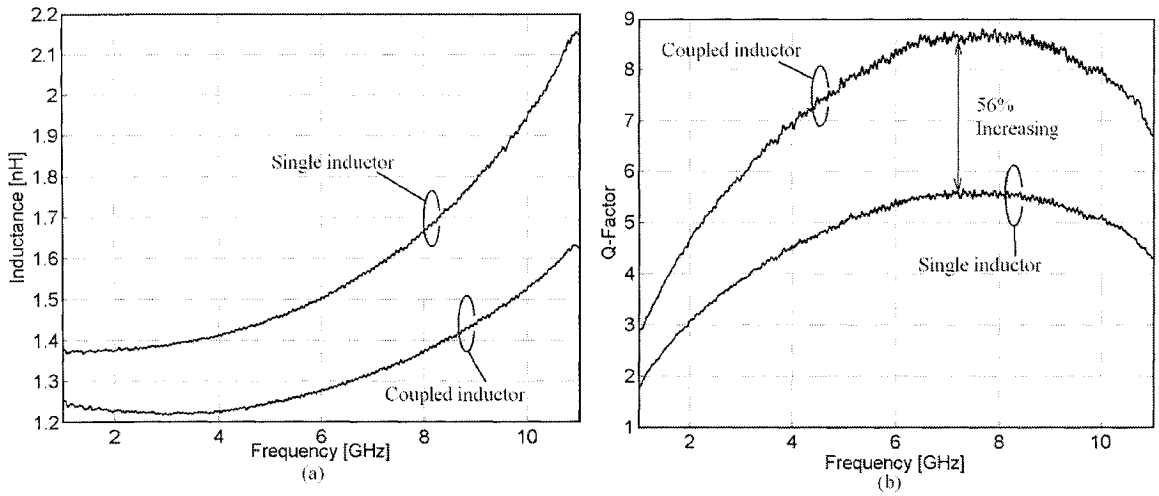


Fig. 3.21: Comparison between measurement results of a coupled inductor structure and the corresponding single looped standard inductor.

This inductance will be added to the values obtained in (3.62) and (3.65). Thus, the total effective inductance value for the equivalent single looped inductor, and each of the coupled inductors are:

$$L_{single} = L_{single}' + L_{out-leading} = 2.56 + 0.071 = 2.631[nH] \quad (3.67)$$

$$L_{1,2} = L_{1,2}' + L_{out-leading} = 0.77 + 0.071 = 0.841[nH] \quad . \quad (3.68)$$

Then, using (3.19) and (3.21), the mutual inductance M, coupling coefficient K, and total effective inductance could be calculated as follows

$$M = \frac{L_{single} - (2 \cdot L_{1,2})}{2} = 0.475[nH] \quad (3.69)$$

$$K = \frac{M}{L_{1,2}} = 0.564 \quad (3.70)$$

$$L_{eff} = L_{1,2} + M = 0.841 + 0.475 = 1.316[nH] \quad . \quad (3.71)$$

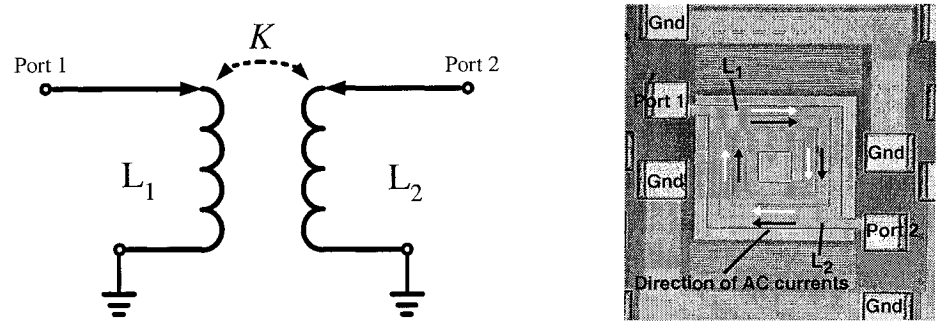
ADS Momentum simulation results for Fig. 3.19 (a) are given in Fig. 3.20. Part (a) of Fig. 3.20 shows the total effective inductance L_{eff} including the mutual inductance, and the quality factor Q_{eff}. The extracted mutual inductance M and coupling coefficient K are shown in Fig. 3.20 (b). Clearly, the hand calculation results correspond very well to the simulation results within the inductor's normal operating frequency range (Table 3.6). Frequency dependent effects are not considered by hand calculations because of complexity.

Table 3.6: Summary for Fig. 3.20 and equations (3.69)-(3.71)

	Simulation	Calculation
Effective inductance (L_{eff}) [nH]	1.328	1.316
Effective quality factor (Q_{eff})	15.364	-
Mutual inductance (M) [nH]	0.48	0.475
Coupling coefficient (K)	0.557	0.564

The quality factor is also left for computer simulation and extraction. Because of the continuous progress in modeling techniques and numerical computation capabilities, faster and more accurate EM simulations are more and more common and used by designers while, at the same time, hand calculations focus more on theoretical analysis and setting reasonable starting points for EM simulations and optimizations.

The prototype in Fig. 3.19 (a) has been fabricated with the two ports port 2 and port 4 grounded, so that our two port VNA could be used for measurement, as shown in Fig. 3.22. A corresponding standard single loop square inductor, which has the same peak quality factor frequency and inductance has also been fabricated on the same die for comparison. Measurement results are given in Fig. 3.21. With nearly the same inductance value, which is about 1.3nH, the quality factor of the coupled structure is 56% higher than that of the single looped standard inductor, because of the addition of the positive mutual inductance. The inductance of the single looped standard inductor is a little bit higher than the designed value. This may be due to process variations. The quality factor is lower in measurement because of the single ended arrangement in the prototype. Some other reasons that may cause the low quality factor is the incomplete calibration procedure that was



(a) (b)

Fig. 3.22: (a) Single ended coupled structure. A two port single ended design facilitates the measurement by two port VNA, (b) chip photograph

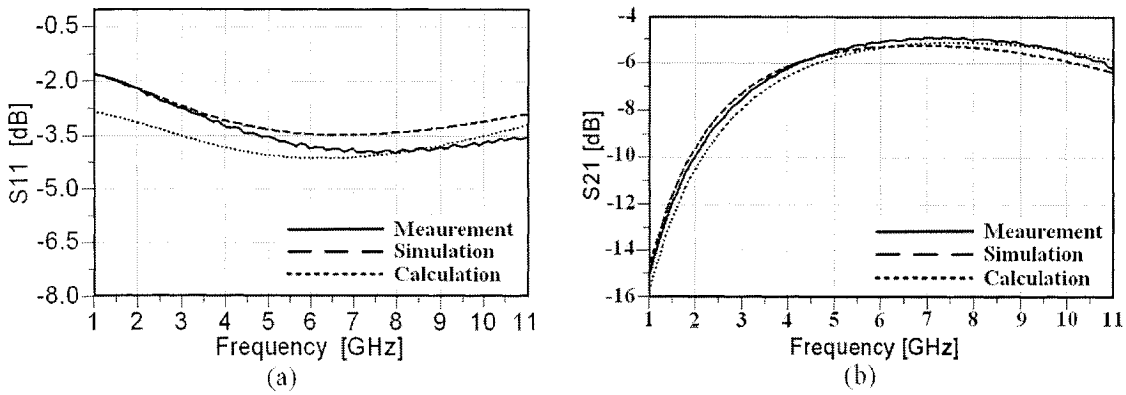


Fig. 3.23: S11 and S21 from measurement and simulation.

used: only open dummy deembedding structures were fabricated, while short deembedding structures used to remove the contact serial resistance between the probes and the pads were not included on the die to save chip area. According to simulation, and based on the dimensions of the inductor coil, this contact resistance may lower the quality factor by around 1 to 1.5. Fig. 3.23 shows S11 and S21 from simulation and measurement results of the structure in Fig. 3.19. EM simulations match the measurement results very well.

Another coupled structure has been measured. Its geometry dimensions are listed in Table 3.7. Fig. 3.24 shows the results from simulation, hand analysis, and measurement. The effective inductance before and after the addition of the mutual inductance (L_{self} and L_{eff}) are shown in Fig. 3.24 (a), and all results match well. Because hand analysis didn't consider the frequency dependent effects, it assumed that the inductance maintains the

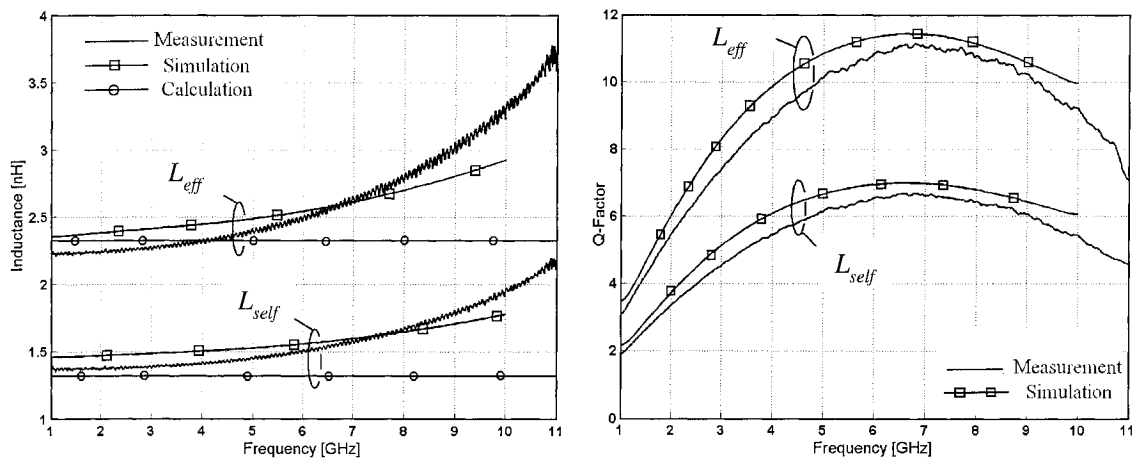


Fig. 3.24: (a) Extracted effective inductance and self-inductance of each of the coupled inductors; mutual inductance equals L_{eff}-L_{self}. (b) Quality factors of L_{eff} and L_{self}

Table 3.7: Geometry sizing of the structure

	d_{out} [um]	d_{out} [um]	n
Equivalent Single inductor	222.54	127.3	4
Intertwined inductor	210	139.84	2

same value in all frequency ranges. Fig. 3.24 (b) shows the simulation and measurement results for the quality factors of L_{self} and L_{eff}. The small difference between the curves may result from the error introduced from calibration as discussed above. Both the inductance and quality factor are calculated using the equations discussed in section 3.3.4. From Fig. 3.24 (a), the mutual inductance could be calculated to be around

$$M = L_{eff} - L_{self} \approx 2.44 - 1.5 = 0.94[nH] \quad , \tag{3.72}$$

and the coupling coefficient K is:

$$K = \frac{M}{\sqrt{L_1 \cdot L_2}} \approx \frac{0.94}{1.5} = 0.623 \quad . \tag{3.73}$$

As clearly seen from the simulation and measurement results, the addition of the positive mutual inductance to the self-inductance of an inductor is a simple and effective way of increasing the quality factor. The higher the coupling coefficient K, the higher the proportion of the mutual inductance M will be in the final effective inductance, thus the higher the increasing of the quality factor. To maximize the quality factor increase, a higher K is always desirable. The quality factor will be doubled under the ideal situation when K equals one. However, a higher K is always accompanied by a higher parasitic capacitance between the coupled inductors. This direct coupling of capacitors will lower the inductive performance of the coupled inductors and finally turn the whole structure into a capacitor. Design structures bearing higher K while keeping this capacitance low is the goal future the research. Another benefit of this technology is its potential of providing two identical inductors in a small chip area. This will help to lower the cost, increase the components matching, and decrease the substrate related noise coupling.

CHAPTER 4

Applications: LNA and VCO Designs

In this chapter, applications of the coupled inductor structures discussed in chapter 3 will be given. Differential VCO and LNA designs are used to demonstrate the enhanced quality factor of the inductors in coupled structures, and its effect on improving the circuit performance. Two VCOs are implemented using the same circuit topology, with one using coupled inductors as a resonant tank and the other using optimized standard inductors. While working at the same frequency and power consumption, the coupled inductor tank will result in up to 8.7 dB decrease in the phase noise of a 2.4 GHz VCO, and 5.26 dB for a 6 GHz VCO. For the differential LNA design, a coupled inductor structure is used for on-chip gate matching, which, in most cases, are realized using off-chip components because of their high quality factor requirements. Distinctive improvement in the NFmin and NF of the LNA are observed, compared to on-chip matching which uses standard planar inductors.

4.1 Differential VCO Design

In modern RF circuit transceivers, voltage controlled oscillators (VCO) have been extensively used in both the transmit and receive paths. In fact, in most systems, one input of every mixer is driven by a periodic signal at a specified frequency. Thus, a VCO is one of the most crucial building blocks for RF communications systems.

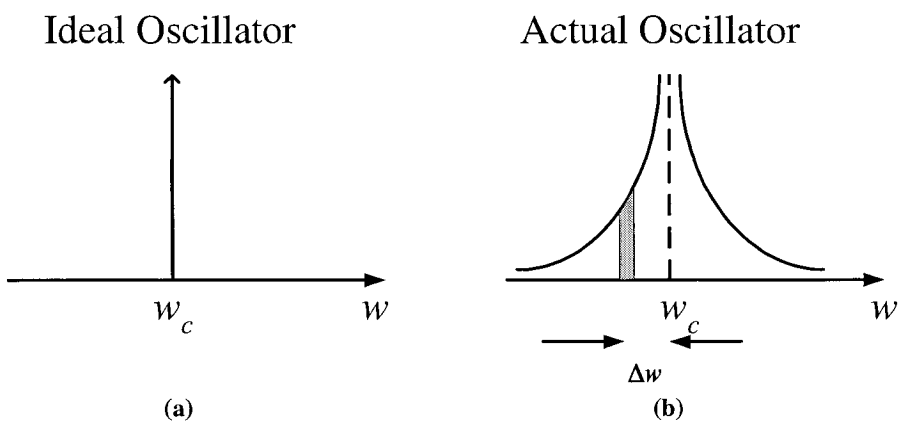


Fig. 4.1: Output spectrum of a) ideal and b) actual oscillator

4.1.1 Phase Noise

As other analog circuits, VCOs are also susceptible to noise. Noise injected into an oscillator by its constituent devices, or by external mechanisms, will affect both the frequency and the amplitude of the VCO output signal. In most cases, mixers will be connected to the output of the VCO. Disturbance in the amplitude is often negligible or unimportant. So, random deviations of the frequency is always a focus of consideration. Frequency changing can be viewed as random variations in the period, or deviations of the zero crossing points from the ideal position along the time domain axis. The definition of the phase noise is shown below [36]:

$$x(t) = A\cos[w_c t + \phi_n(t)] \ , \tag{4.1}$$

where A is the magnitude of the sinusoidal signal, w_c is the center oscillation frequency, $\phi_n(t)$ is a small random excess phase representing variations in the period. Because this noise has been expressed in terms of phase, $\phi_n(t)$ is called the phase noise. In RF applications, phase noise is usually characterized in the frequency domain. For an ideal sinusoidal oscillator operating at w_c, the spectrum assumes the shape of an impulse, as shown in Fig. 4.1(a). However, for an actual oscillator, because of the phase noise, the spectrum exhibits a skirt like region around the center frequency, as shown in Fig. 4.1(b). Quantification of the phase noise is done by calculating the noise power in a unit bandwidth at an offset Δw with respect to the center frequency w_c, then divide the result by the carrier sig-

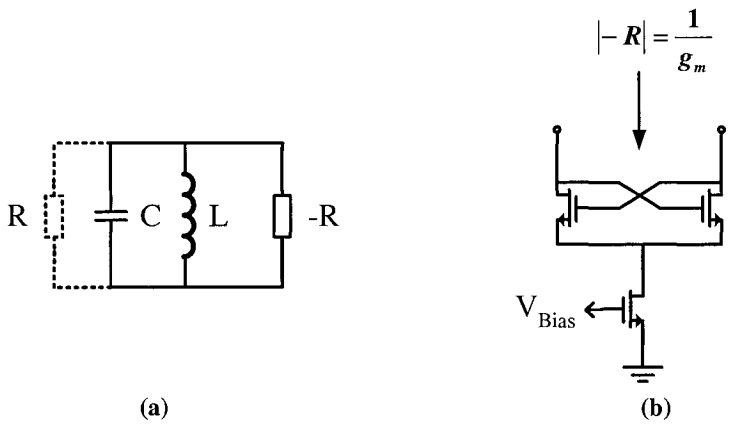


Fig. 4.2: (a) Negative resistance resonant LC tank; (b) Coupled transistor pair.

nal power. The unit of phase noise is dBc/Hz. Here, dBc means "expressed in dB with respect to carrier" [36][44].

In RF communications systems, the difference between two adjacent channels could be as small as tens of kilohertz, with the center carrier frequency ranging from 900MHz to 5GHz. Thus, to prevent corruption between two close channels, the output of the local oscillation is requested to be very sharp. This means it should have extremely low phase noise. Building very low phase noise VCOs is an ongoing active research topic in RF integrated circuits designs.

4.1.2 Negative Resistance *LC* Tank VCO

Fig. 4.2(a) shows the concept of the popular negative resistance LC oscillator. In real circuit design, a negative resistance is usually realized using a coupled transistor pair, as shown in Fig. 4.2(b). The negative resistance this pair could provide is:

$$|-R| = \frac{1}{g_m} , \tag{4.2}$$

where g_m is the transconductance of each of the transistors. By optimizing the bias current and the transistors sizing, this negative resistance will be able to compensate for the losses in the LC tank, modeled by R in Fig. 4.2(a), and ensure sustained oscillation. Usually, to guarantee the start up of oscillation, the negative g_m used will be larger than the minimum required value. After the circuit starts, the nonlinearity in the circuit will limit the effective

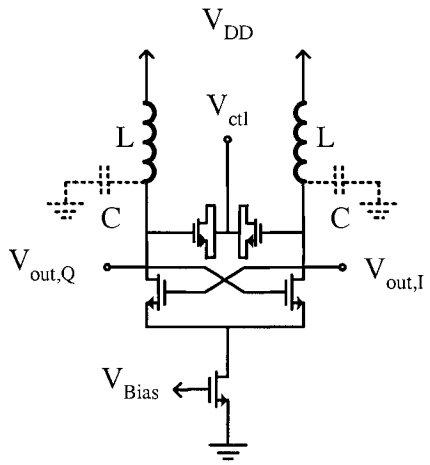


Fig. 4.3: Current biased differential LC oscillator

gain of the circuit. As a balance between the start up requirements and power consumption, the initial g_m is usually made 2 to 3 times bigger than the tank losses. The complete differential VCO using the coupled transistor pair is shown in Fig. 4.3. The phase noise of the circuit in Fig. 4.3 has been thoroughly studied and reported based on Leeson's equation [45]:

$$L(w_m) \propto \frac{1}{V_0^2} \cdot \frac{kT}{C} \cdot \frac{w_0}{Q} \cdot \frac{1}{w_m^2} . \tag{4.3}$$

This equation was first postulated by Leeson to reveal the thermally induced phase noise in any oscillators and has been modified into the following form in [46]:

$$L(w_m) = \frac{4FkTR}{V_0^2}\left(\frac{w_0}{2Qw_m}\right)^2 , \tag{4.4}$$

where in both equations, V_0 is the output oscillation amplitude, w_0 is the center frequency, w_m is the offset frequency where the phase noise is calculated, or being measured, Q is the quality factor of the tank, and R is the tank resistance. In (4.4), F is the noise factor which has been introduced and expanded to account for the phase noise contributed by the coupled pair and bias current source and it is given by

$$F = 1 + \frac{4\gamma IR}{\pi V_0} + \gamma\frac{4}{9} g_{mbias} R , \tag{4.5}$$

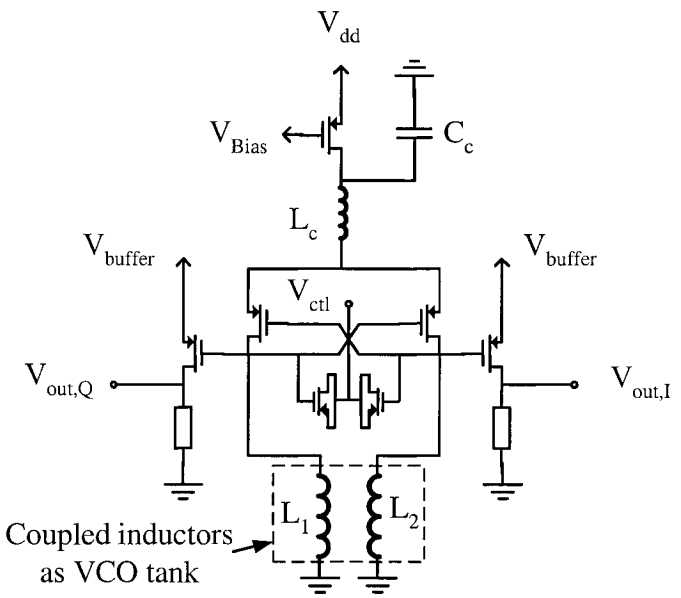


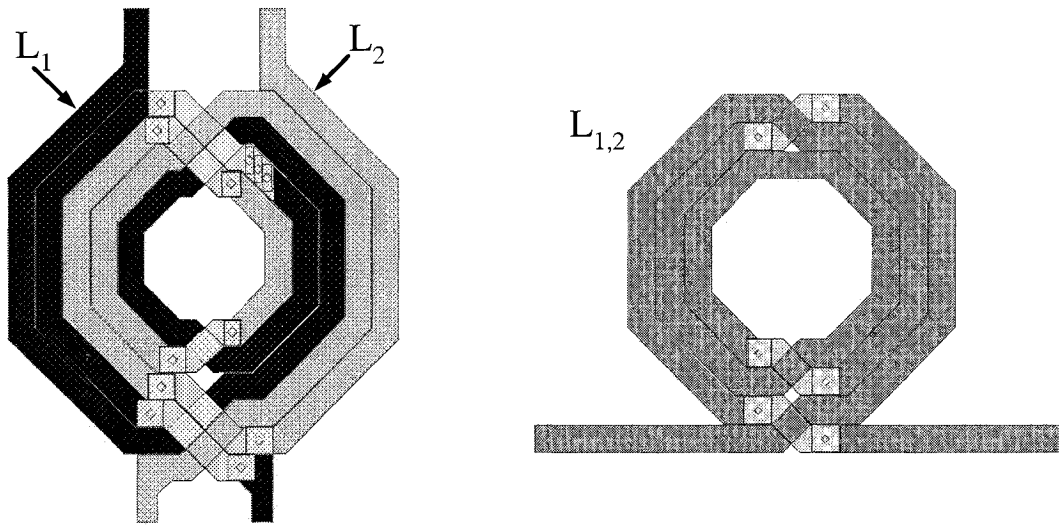
Fig. 4.4: All PMOS transistors low voltage VCO structure

where, g_{mbias} is the transconductance of the current source transistor, and Υ is a constant. Three noise contributions are included in (4.5), which are i) the noise that comes from the tank resistance, ii) the differential coupled pair transistors noise, and iii) the bias current source noise.

With the trend for low voltage and high frequency circuit designs, which results in smaller output swings V_0 and higher w_0, it would be more and more difficult to maintain low phase noise, according to (4.4). While the current source contributed noise could be eliminated mostly by using a filtering approach [46], increasing the quality factor of the tank, or actually the Q of the inductor, would be the most straight forward and practical way to build low phase noise, low voltage, high frequency VCOs.

4.1.3 Prototype VCO Designs

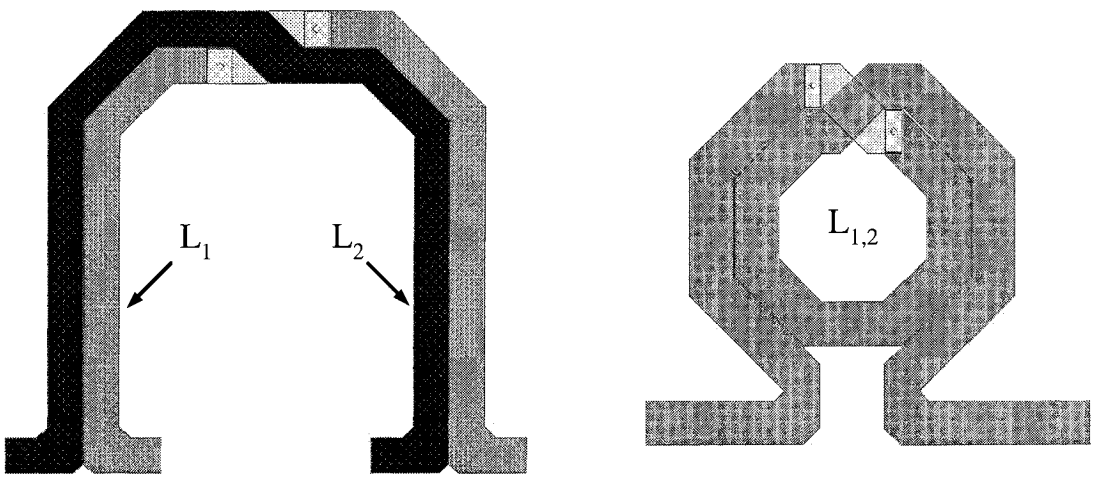
The VCOs discussed in this chapter have been designed using a 1V power supply, working at 2.4GHz and 6GHz [28]. At each frequency, 2 prototypes are implemented: one using optimized stand alone inductors, while the other using a coupled inductors structure. Fig. 4.4 shows the VCO circuit. To minimize the flicker noise up conversion induced phase noise, an all-PMOS transistors topology is chosen. Two common source buffers are



(a) (b)

Fig. 4.5: (a) A coupled inductor tank for 2.4GHz; (b) The corresponding optimized standard inductor for 2.4GHz.

added to isolate the tank from the following stages. The coupled transistor pair was designed to provide enough negative resistance, while keeping moderate bias current and transistor sizing. C_c provides a low impedance path to ground for the noise of the current source. L_c and the source parasitic capacitances of the coupled transistors form a filter that resonates at twice the oscillating frequency of the VCO. This filter will provide a high impedance at $2w_c$ to prevent the differential pair transistors operating in the triode mode from loading the resonator, and thus suppress the phase noise [46]. One point should be noted is that, because PMOS transistors usually have a smaller g_m, larger transistor sizes



(a) (b)

Fig. 4.6: (a) A coupled inductor tank for 6GHz; (b) The corresponding optimized standard inductor for 6GHz.

Table 4.1: Summary of the design parameters and component values

	2.4GHz Standard	2.4GHz Coupled	6GHz Standard	6GHz Coupled
L* [nH]	3.56	3.45	0.82	0.815
Q*	8.65	12.4	10.2	15.5

* All inductances and quality factors come from differential excitation simulations.

are always needed to get the equivalent negative resistance. Bigger transistors will contribute large drain node parasitic capacitances, which will decrease the tuning range of the VCO.

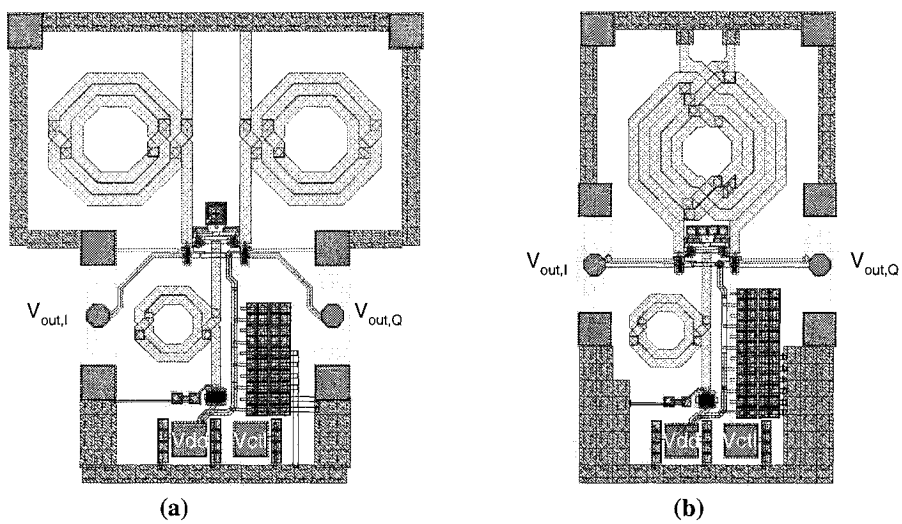
Fig. 4.5 shows the layout of the tank inductor for the 2.4GHz VCO. The 6GHz inductors are shown in Fig. 4.6. The choice of the inductors values is based on the following equation [47]:

$$\frac{\langle v_n^2 \rangle}{V_{tank}^2} \propto \begin{cases} (L \cdot g_L^2)/I_{bias}^2 \\ L \end{cases} \tag{4.6}$$

where V_{tank} is the tank amplitude, and v_n is the noise voltage cross the tank defined as

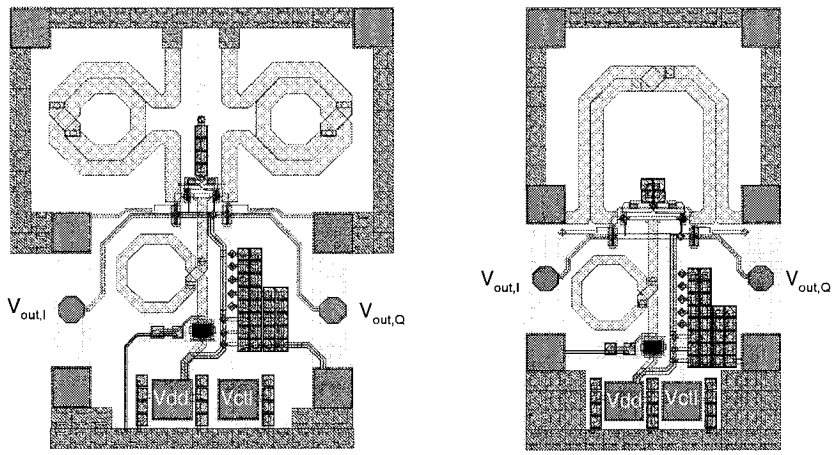
$$\langle v_n^2 \rangle = \frac{kT}{C} = kTw_c^2 L\,, \tag{4.7}$$

and g_L is the equivalent parallel conductance of the inductor representing the losses. Under



(a) (b)

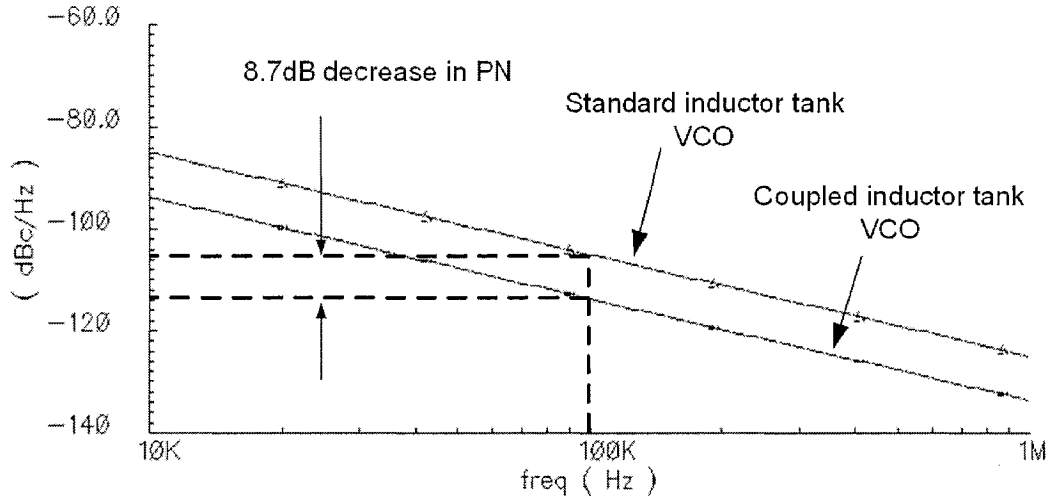
Fig. 4.7: (a) The 2.4GHz VCO with optimized standard tank inductors; (b) Same VCO with coupled structures.



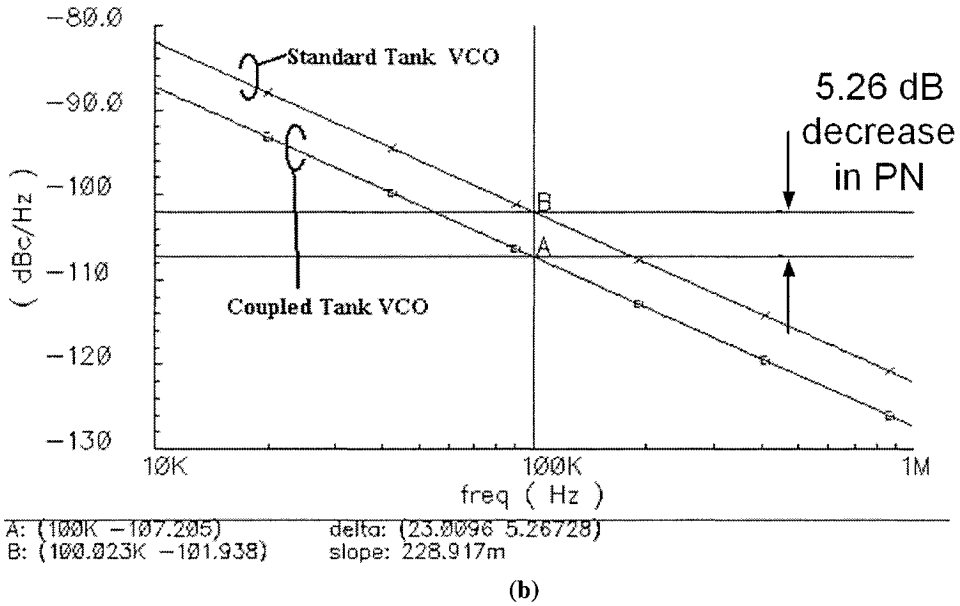
(a) (b)

Fig. 4.8: (a) The 6GHz VCO with optimized standard tank inductors; (b) Same VCO with coupled structures.

the condition that start up and the minimum output swing are satisfied, small inductor values are chosen to minimize the noise and avoid the VCO entering the voltage limited mode, which is more likely to happen in low voltage VCO designs. Table 4.1 summarizes the design parameters of the tank inductors. As expected, coupled structures have higher quality factors than the standard tank inductors. The VCO layout is shown in Fig. 4.7 for the 2.4GHz design, and in Fig. 4.8 for the 6GHz design. At the layout stage, effort has been made to keep the design geometry as symmetric as possible. Coupled transistors are placed close to the tank inductors to minimize parasitic capacitances and inductances. Because the tuning voltage range available is from 0 to 1V, the varactors are realized using inversion PMOS transistors, which will give a maximum tuning range, compared to other varactor forms, such as accumulation NMOS, etc. [48][49]. As large as possible de-coupling capacitors are placed between the control voltage lines and ground. This helps to filter out the noise on the control voltage. Both the standard inductors and coupled structures are simulated in Momentum using the CMOS p18 technology files. Data fitting is applied to transform the S-parameters into lumped component circuit models as discussed in chapter 2 and 3. Cadence Spectre is then used to simulate the phase noise of the VCO designs. Fig. 4.9 shows the phase noise results, and the data is summarized in Table 4.2. For the same power consumption and circuit topology, the VCOs using coupled inductor structures as tanks have up to 8.7dB decrease in phase noise at a 100kHz offset for the 2.4GHz design, and 5.6dB for the 6GHz one. From Table 4.2, it is also clear that coupled tank



(a)



(b)

Fig. 4.9: (a) Spectre simulation for the 2.4GHz VCO; (b) Spectre phase noise simulation for the 6GHz VCO

VCOs take less chip area compared to VCOs using standard tank inductors. it should be noted that the tuning range decreases for the 2.4GHz design when using the coupled structure. This could be explained as follows: using two intertwined inductors will increase the fringing capacitances between them. When used at the VCO tank, this fringing capacitance will be added to C_{fix}. Increasing C_{fix} will directly lead to the decrease of the tuning range. While for the 6GHz VCO design, because the coupled structure is much simpler, the increase of C_{fix} caused by fringing capacitances will not be so pronounced. So, the tun-

Table 4.2: Summary of the simulation results for the 2.4 GHz and 6 GHz 1V coupled and standard inductors VCO's.

	2.4GHz CMOS VCO		6GHz CMOS VCO	
Tank Inductor Implementation	standard	**coupled**	standard	**coupled**
Phase Noise @ 10KHz (dBc/Hz)	-84.9	**-93.6**	-81.9	**-87.2**
Phase Noise @ 100KHz (dBc/Hz)	-104.9	**-113.6**	-101.9	**-107.2**
Phase Noise @ 10MHz (dBc/Hz)	-124.9	**-133.6**	-121.9	**-127.2**
Tuning Range (V_{tune} = 0 to 1V)	12%	**10%**	9%	**9%**
Chip Area (mm^2)	0.65	**0.37**	0.46	**0.25**
Power Consumption (mW)	7.4	**7.3**	5.2	**5.3**
Figure of Merit (dBc/Hz)	-183.8	**-192.5**	-190.3	**-195.5**

ing range of the 6GHz VCO is not affected much. Designers should take this coupling induced C_{fix} increase into account at early stages of their design.

4.2 A Differential LNA Design

In this section, a much more generic and relevant application of the coupled structures is proposed, as shown in Fig. 4.10 [28]. In this design, a coupled inductor is used as an on-chip gate matching inductor for a differential LNA. Compared to the usage as a coupled tank in a VCO, which could be viewed as a single ended three-port network, gate matching inductor is a "quasi-differential" four-port application. Here quasi-differential means that each of the inductors in the coupled structure is not really ifferentially excited, but the

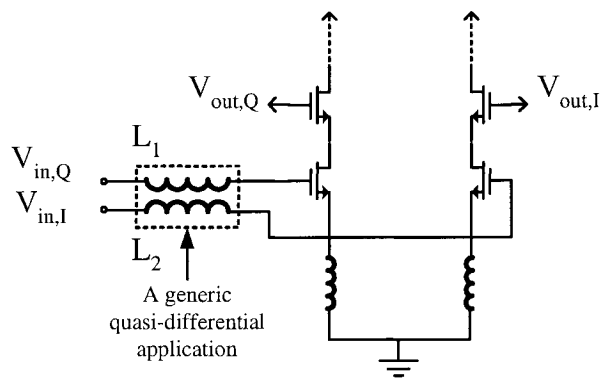


Fig. 4.10: A coupled inductor structure used as on-chip gate matching inductors for LNA designs

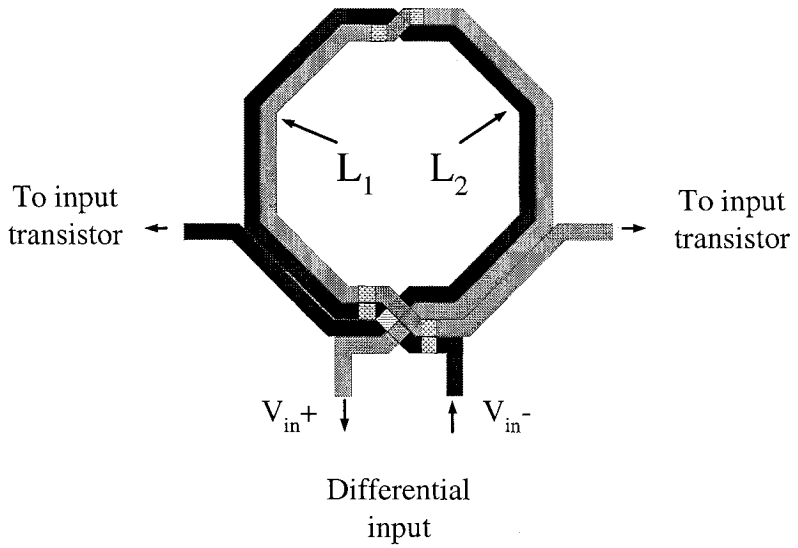


Fig. 4.11: Coupled inductor structure optimized for the 6GHz LNA.

entire structure is. Being the first lossy stage in the RF receiving path, the quality factor of the gate matching inductor has strong influence on the noise figure of the entire receiver. Usually, those matching inductors are realized using off-chip high quality factor components [50]. However, realizing on-chip gate matching inductors will always be an attractive alternative for RF designers who aim at building fully integrated monolithic RF front-ends.

Based on the successful LNA discussed in chapter 2, a differential LNA has been designed and simulated. In this LNA, all inductors in the original design are kept as standard inductors, except those used for gate matching, which are replaced with an optimized coupled inductor structure that offers the same inductance value, and thus the same matching for the input RF signal.

Fig. 4.11 shows the coupled structure used in the differential LNA design. Table 4.3. lists the parameters and extracted inductance and quality factors of the structure. All inductors and coupled structures are simulated using Momentum. Data fitting procedure are also

Table 4.3: Parameters of the coupled gate matching inductor

	L [nH]	Q	d_{in} [um]	d_{out} [um]
Coupled structure	2.54	16	301	383
Standard inductor	2.6	12.2	193	275

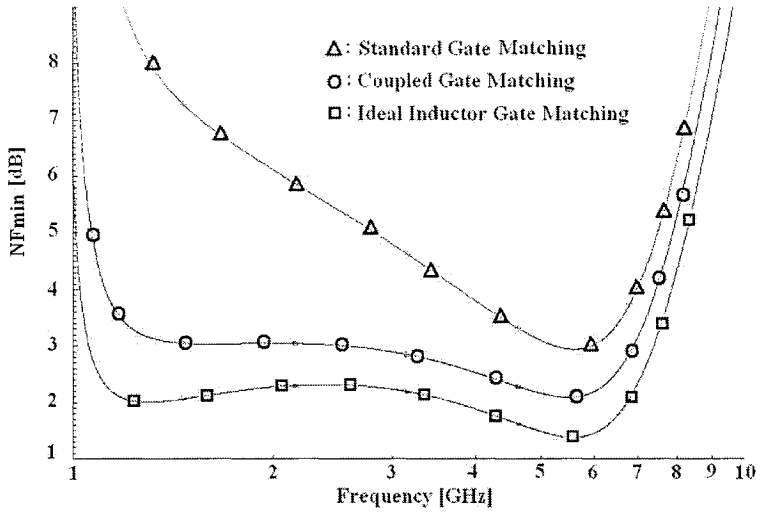


Fig. 4.12: NFmin of the differential LNA using ideal inductors, coupled structures, and standard inductors for gate matching.

used to transform the S-parameters into lumped equivalent circuit as discussed in chapter 2 and chapter 3. Cadence Spectre is used for the differential LNA simulation. Simulation results are shown in Fig. 4.12, Fig. 4.13 and Fig. 4.14.

In Fig. 4.12, improvement in the LNA's minimum noise figure (NFmin) is demonstrated. A 1 dB decrease of the NFmin at 6GHz was achieved by using the high quality factor coupled inductor structure shown in Fig. 4.11. An additional benefit of using coupled structures is that a wider NFmin range is obtained compared to the NFmin responses when using standard gate matching. Accompanying the decrease of the NFmin, the overall noise

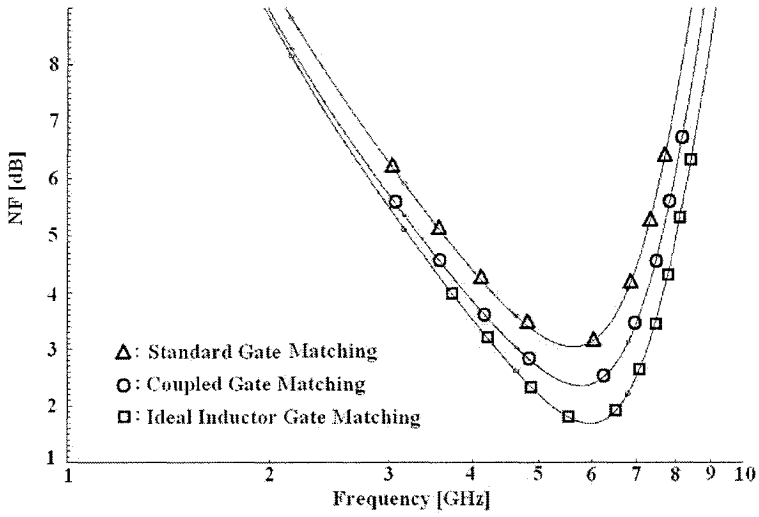


Fig. 4.13: Noise figure of the differential LNA using ideal inductors, coupled structures and standard inductors for gate matching.

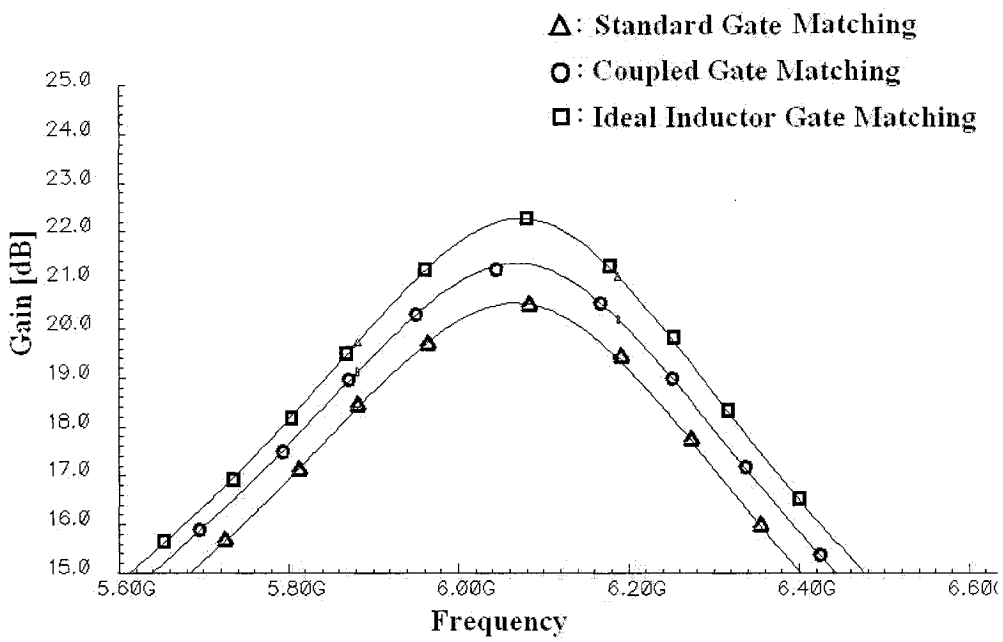


Fig. 4.14: Gain of the differential LNA using ideal inductors, coupled structures and standard inductors for gate matching.

figure (NF) of the LNA is also decreased. At 6GHz, the NF of the LNA drops from 3.1 dB to 2.2 dB (Fig. 4.13). As expected, ideal gate matching inductors would give the lowest NF of 1.7 dB. Finally, Fig. 4.14 shows a 1 dB increase of the forward gain when using coupled inductor structures. This could be explained by the fact that higher quality factor of the matching inductor lowers the energy loss in the input matching network. One thing should be noted is that the matching network will not influence the intrinsic forward gain of the LNA, which is set by the circuit topology, transistor sizing, and the bias current.

CHAPTER 5

Conclusion

The growing demand for modern wireless communications systems, and the continuous progress of the manufacturing technologies have pushed RFIC designs towards monolithic solutions with low voltage, low power, low noise, and ever higher frequency of operation. All these design specifications are demanding higher and higher performance from the on-chip passive components, especially the inductors. The emerging dominance of CMOS circuits in the 2 to 6GHz RF applications pushes this to its limits. Designers are attracted by the CMOS's potential of offering single chip solutions by integrating the analog RF front-ends together with the baseband digital circuitry. Being one of the most crucial passive RF components, which determine the performance of key RF building blocks, high quality, low cost silicon based on-chip inductors, along with effective and accurate design methodologies, have always been an important research focus of RF circuit designers.

This thesis was concerned with the design of quality factor enhanced on-chip inductor structures. In chapter 1, an overview of the technology and the choices for inductor designs was presented. The motivation, challenges, and need for on-chip inductors operating in the 2 to 6 GHz frequency band were addressed.

In chapter 2, modern silicon IC fabrication and metallization technologies were first addressed. Then, basic theory and important formulas for analyzing and modeling on-chip inductors, along with some major design guidelines were introduced. Complete and detailed procedures of using the ADS Momentum EM simulator for inductors design were

then discussed throughout this chapter. One successful design of a CMOS LNA working at 6GHz was also presented.

In chapter 3, coupled inductor structures which make use of positive mutual inductance between intertwined on-chip spirals were proposed. Detailed calculation and simulation procedures were presented. Data processing procedures to extract the equivalent differential inductance and quality factors of each of the inductors in the coupled structure were outlined. Through this method, the S-parameters of the structure could be mapped into a π-model based lumped equivalent circuit, which could be used in time domain based simulators such as Hspice and Spectre. Prototype measurement results match well calculations and simulations.

Applications of the coupled structures proposed in chapter 3 were presented in chapter 4. Differential VCO and LNA designs are discussed, and simulation results were reported. As expected, for the same circuit topology and power consumption, coupled structures improve the circuits performance in terms of phase noise for the VCO, and in terms of noise figure and gain for the LNAs. Also, in the differential LNA designs, gate matching demonstrated the potential generic use of a 4-port coupled inductor network. Moreover, smaller chip area was achieved using the coupled structures.

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