ABSTRACT

The present industrial practice of ac to dc conversion uses diode or thyristor bridges which are harmonic polluters and poor power factor sources. This thesis exploits PWM techniques to develop a new generation of rectifiers with near sinusoidal current waveforms, unity and even leading power factor and bilateral power transfer capability through bidirectional current flow in the dc link.

The Boost Type PWM Voltage Regulated Rectifier was originally conceived as being Direct Current Controlled. The work of this thesis advances the control methodology by using Indirect Current Control and the standard Sinusoidal PWM technique. Two high quality current transducers are avoided and the harmonics become more predictable for elimination purposes.

The thesis addresses the problem of upscaling the power ratings of the rectifiers by connecting rectifier modules in series and in parallel. Different topologies are proposed and analyzed.

The research was carried out by building two 2-kW size laboratory models which were subjected to demanding tests. Experimentally justified mathematical models and computer simulations have been developed and have been successfully used in predicting stability boundaries.

RÉSUMÉ

Il est pratique courante dans l'industrie d'utiliser des ponts de diodes ou de thyristors pour la conversion du courant alternatif en courant continu. Ces méthodes ont le désavantage de créer beaucoup d'harmoniques et d'offrir un facteur de puissance médiocre.

Cette these exploite les techniques d'impulsion de largeur variable pour développer une nouvelle génération de pont de redresseur. Ces ponts ont l'avantage de drainer un courant quasi-sinusoidal et d'offrir un facteur de puissance unitaire et même capacitif. Ils offrent un transfert de puissance bidirectionnel puisque le courant continu est libre de circuler dans les deux directions.

Un redresseur de type élevateur de tension, régularise par impulsion de largeur variable a été conçu pour être contrôlé par le courant continu. Cette these fait un pas en avant en utilisant le contrôle de courant indirect et la méthode standard d'impulsion de largeur variable. Ceci permet d'éviter l'utilisation de deux capteurs de courant de haute qualité. De plus, le contenu en harmonique est prévisible, ce qui aidera a leur élimination.

Cette these s' attaque au problème de l'augmentation de la capacité des redresseurs en connectant plusieurs modules en série et en parallèle. Différentes topologies sont proposées et analysées.

Ces recherches sont basées sur la construction de prototypes de 2-kW qui ont été l'object des tests. Des modèles mathématiques et simulation par ordinateur ont été developpés et vérifiés expérimentalement. Ceux-ci ont par la suite été utilisés avec succès pour prédire les limites de stabilité des prototypes.

CLAIM TO ORIGINALITY

To the best of the author's knowledge, the following contributions are original:

1. The static compensator [Section 3.5.2] of Indirect Current Control yields sluggish transient response and poor stability region by comparison with Direct Current Control.

2. The dynamic compensator [Section 3.5.3] reinstates the lost stability region so that Indirect Current Control is both statically and dynamically equivalent to Direct Current Control.

3. The concept of series and parallel connections at the modular level so as to side-step the difficulties of voltage and current sharing at the semiconductor switch level [Chapters IV and V].

4. The invention of Type C configuration [Sections 4.4 and 5.4] which is one of the most economical configurations in terms of components count.

5. Proof that when the Master is stable, the Slaves of series Types C, D and E configurations are also stable [Sections 4.4.1, 4.5.1 and 4.6.2].

ACKNOWLEDGEMENTS

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Appendix B: Practical Implementation.

NOMENCLATURE

BD	Base Drive
BDL	Base Drive Logic
C	Dc link Filter capacitor
e	Error signal
e_a, e_b, e_c	Instantaneous phase-to-neutral supply voltages
e_T	Triangular carrier signal
ø	Power factor angle
f_s	Supply frequency
GTO	Gate-Turn-Off thyristor
h	Hysteresis band
I	Rms input rectifier current
i_1	Output rectifier dc current
i_2	Load dc current
i_a, i_b, i_c	Instantaneous rectifier input currents
i_d, i_q	Instantaneous input currents in the d-q frame
K_D	Derivative control gain
K_I	Integral control gain
Kp	Proportional control gain
L	Input rectifier inductance per phase
L_b	Representative value of L for dynamic compensation
L_c	Representative value of L for static compensation
M	Middle point of the dc link
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

N	Neutral connection
P	Proportional control
P_1	Output dc power
P_2	Load dc power
P_{in}	Input ac power
PI	Proportional-Integral control
PWM	Pulse Width Modulation
R	Input rectifier resistance per phase
Rc	Representative value of R in the control blocks
SCR	Silicon Controlled Rectifier
SPWM	Sinusoidal Pulse Width Modulation
Vc	Dc link and filter capacitor voltage
v_c	Instantaneous dc link voltage
V	Rms phase to neutral supply voltage
V_{mod}	Rms fundamental phase to neutral voltage at the ac rectifier terminals
w_s	Angular supply frequency
w_t	Triangular carrier angular frequency
Z	Rectifier input impedance

CHAPTER I

INTRODUCTION

Since the invention of the Mercury Arc Rectifier at the beginning of this century [1], power rectifiers have played an important role in the development of power conversion. The introduction of the control grid in 1926 made it possible to control the dc voltage by varying the instant of firing of the valve [2]. Further development led to the first High Voltage DC transmission lines in about 1940 [3]. Around 1960, with the advent of power semiconductors and the invention of the Silicon Controlled Rectifier (SCR) [4], the era of the mercury arc devices quickly came to an end. Accompanying the power valve development, many rectifier topologies were proposed [5,6], the most popular and widely used being the Graetz Bridge Rectifier [7]. Basically, it is a line commutated converter, Power reversal is achieved by voltage reversal at the dc link.

Despite its popularity, the Graetz Bridge Rectifier has proven to be the largest harmonic polluter in the utility system [8,9,10]. Furthermore, since it adjusts power demands by delaying the power angle, the power factor is very poor at lower loads [11]. These problems are presently solved by high cost power filters and VAR compensators [12]. In addition, many direct current power loads need current reversal in the dc link instead of the voltage reversal offered by the Graetz

Bridge. Some examples of this requirement are the dc lines for electric traction (with standards set at 750, 1500 and 3000 Vdc) as well as many kinds of machine drives (choppers and voltage source inverters) [13]. Presently, this problem is solved by using dual converters or a diode rectifier along with a line-commutated thyristor inverter, which roughly double the capital cost.

Some authors have anticipated considerable improvements in the power converter area by taking advantage of the force commutated technique, using Mosfets, Power Darlingtons or Gate turn-off Thyristors (GTO's) [14,15,16]. These new converters, implemented with gate turn-off semiconductors, are replacing the traditional power conversion topologies which make use of line commutation. Most of this research has been focused on the inverter mode (dc to ac conversion) for variable speed drives [17,18,19] or for Uninterruptible Power Supplies (UPS) [75,76,77]. The research has led to significant improvements, such as the elimination of low order harmonics by using different kinds of Pulse Width Modulation (PWM) techniques to control the gates of the power switches [20,21,22,23], or the use of resonant circuits to obtain "zero" switching losses [78,79,80].

The success in inverter applications has initiated the consideration of the same techniques for rectification purposes. In recent years, the PWM techniques have begun to be applied to the rectifier side, using force commutated devices

[24,25,26]. However, these rectifiers lack the current reversal capability. Few papers have been written about PWM rectifiers with dc current reversal, despite the fact that the technical tools already exist. The first attempts can be found in [27]. Brown Boveri has also been working on the topic, without disclosing any details [28]. The company is running an experimental train which should reach a top speed of 350 km/h by 1991, using rectifiers of this type [29]. McGill University [30,31,32,33] and some German researchers [34,35] have been working on this problem using the Boost type modulators [36].

McGill University has focused its work on the use of Controlled Current PWM converters with hysteresis band control [37,38,39] and unidirectional dc voltage. When a dc voltage feedback loop is implemented in such a modulator, it can operate as a stand-alone voltage regulated dc power supply with dc current reversal capability and a fast transient response [40,41]. The input ac current is directly controlled (Direct Current Control) by forcing it to follow a sinusoidal template with a small tolerance band (hysteresis). The amplitude of this template is controlled by the error signal generated between the dc link voltage and the desired reference voltage. Because the phase-shift of the sinusoidal template is adjustable, the rectifier can operate at unity or even leading power factor for all load conditions [42].

The Controlled Current PWM Rectifier has innumerable applications in mating the standard frequency of the power utility to the variable frequencies, required in inverter/ac motor drives or to chopper/dc motor drives. In the high power range, one sees it in having a role in High Voltage Direct Current (HVDC) applications. Its ability to operate at a regulated dc link voltage suggests that multi-terminal HVDC connections can easily be realized. Presently, the Graetz Bridge Type of HVDC stations is not a perfect match in multi-terminal connections.

Unfortunately, some of these useful applications are limited by the power ratings of the semiconductor switches. Despite the continuing increase in the ratings of the high power semiconductor switches, the gate-turn-off devices, with the exception of the GTO's, fall short in comparison with thyristors [43,44].

This thesis focuses on developing methods of increasing the overall power of the rectifier system, by connecting modules of converter units in series and in parallel, [45,46,47,48], while keeping the overall system simple, reliable and harmonic-free.

The designation "Boost Type" in the thesis title follows the terminology used by workers in Switch-Mode Power Supplies. In the Boost Type Rectifier, the power from the ac side is first converted to magnetic energy in inductances during the turning ON of the valves. When the valves are turned OFF, the

Ldi/dt voltages of the inductances cause the anti-parallel diodes on the opposite side of the rectifier branches to conduct, thus admitting the stored magnetic energy to the dc side. The research on the Boost Type Rectifier began with the Controlled Current PWM Converters with Hysteresis Band Control and was the subject of the author's M. Eng. thesis. In retrospect, this mode of control is considered here as Direct Current Control. Because it has excellent characteristics, its performance has become a standard to which that of Indirect Current Control is compared. For this reason, Direct Current Control forms the subject matter in Chapter II as it shows the thought process which led to the successful implementation of Indirect Current Control.

The research on Indirect Current Control is motivated by the following considerations: i) How can the expensive high quality broad bandwidth current measuring devices [53,54] in hysteresis band control be eliminated? and ii) How can its harmonic frequencies be made more predictable as in Sinusoidal Pulse Width Modulation (SPWM)?. As it turns out, the inner current control feedback loop can be mimicked mathematically and implemented by hardware representing the transfer function blocks [55].

The first attempt, based on static compensation, fulfilled all the expectations of steady-state behaviour. However, it has a sluggish transient response and a very limited stability region compared to Direct Current Control.

These difficulties led to intensive research in mathematical modelling and stability analysis. The outcome is a dynamic compensator by which the Indirect Current Controller can be made equivalent to the Direct Current Control in all respects. In addition, the dynamic compensator can secure a larger margin of stability than was thought to be possible until now.

By connecting multiple units in series and in parallel and by suitably shifting the triangular carriers of each module, the effect of high frequency switching is achieved. This has the implication that the relatively slow GTO's and even the force commutated thyristors can be used in PWM converters. The method also reduces switching losses.

All the ideas in the thesis have been proven experimentally. The experimental work was performed on a 2 kW size, 30 kHz, bipolar transistor PWM converter. The experimental research went hand-in-hand with mathematical modelling, digital simulation and analysis.

The main body of the Thesis has been divided into four Chapters:

CHAPTER II begins by describing the operation of the PWM rectifiers using Current Hysteresis Controllers which is followed by analyzing mathematically the method of Direct Current Control. Because a complete analysis has already been developed in [31,56], only a brief explanation and some important results are repeated here. The stability limits, the

influence of the parameters in the behaviour of the system, along with some simulations and experiments are included as well.

CHAPTER III describes the Indirect Current Control. It consists of applying the switched voltages of Sinusoidal PWM (SPWM) strategy to achieve a constant power factor output with near sinusoidal current waveforms, without the inner current feedback loop of the Direct Current Control. An experimentally verified mathematical model is developed. The mathematical model is used in stability analysis, which follows the Nyquist approach and the state-space approach, The stability analysis reveals the inadequacy of the static compensator and the concept of pole cancellation leads the way to a dynamic compensator. The expanded stability boundaries of the dynamic compensator have been verified experimentally. With confidence in the correctness of the mathematical model, predictions are made of the sensitivity of performance characteristics to parameter variations, the transient response and the stability limits. In addition to experimental data, the predicted results are supported by digital simulations based on two programs: the Mathematical and the Valve-by-Valve Simulations (see Appendix A). The Mathematical Simulations are based on the numerical integration of the system of differential equations modelling the rectifier, assuming that only the Fundamental Fourier Harmonic Component is important. The

Valve-by-Valve Simulations use a special eight-state algorithm and consider the entire Harmonic Spectrum.

CHAPTER IV develops the ideas concerning the series connected PWM rectifiers. Three different topologies for Direct Current Control and two for Indirect Current Control are analyzed:

A. Direct Current Control

i) Independent Local Control

ii) Common Current Reference Control

iii) Common Switching Control

B. Indirect Current Control

i) Indirect Common Switching Control

ii) Shifted Triangular Carrier Control

Conditions of stability, power, current, voltage sharing as well as the parameter variation sensitivity are analyzed. Each topology is discussed independently and the results are compared to each other. To support the mathematical analysis, digital computer simulations and experiments are included. The possibility of implementing Series Back-to-Back Systems has also been considered in this Chapter.

CHAPTER V considers the case of parallel connected PWM rectifiers. The same topologies as Chapter IV are analyzed. This Chapter follows the same format as chapter IV.

CHAPTER VI summarizes the work developed in the previous chapters and discusses the results obtained in each one of them. Future lines of research are also proposed.

Digital simulations and experiments have played an important part in supporting this work. **APPENDIX A** lists the computational algorithms developed to simulate the behaviour of the different topologies for Direct and Indirect Current Control.

Considerable time was spent implementing the hardware for the many configurations. **APPENDIX B** is devoted to recording the detailed circuit diagram of the vital parts of the rectifiers.

CHAPTER-II

DIRECT CURRENT CONTROL

2.1 Introduction.

The subject of **Direct Current Control** has formed the topic of the author's Master Engineering Thesis under the title **"A DC Voltage Regulated Controlled Current PWM Rectifier"**. A brief overview is given in one chapter of the Ph.D Thesis for two reasons:

i) to introduce the structure of the Boost Type PWM Rectifier (Section 2.2) and to summarize the findings concerning Current Hysteresis Control (Section 2.3), mathematic modelling (Section 2.4) and stability analysis (Section 2.5). This brief repetition is essential to understand the thought process which leads to the **Indirect Current Control** in Chapter III and subsequently to its use in series and parallel connections in Chapters IV and V respectively. The background also allows one to make comparison as to the relative effectiveness of Indirect Current Control.

ii) the second reason is that further research has been pursued on the subject of Direct Current Control since

the M. Eng. Thesis and this chapter serves as the repository for documenting some additional research results. This consists of Proportional-Integral Control in Section 2.6 and Valve-by-Valve Digital Simulation in Section 2.7. The Valve-by-Valve simulation programs have been developed as tools in the verification of the mathematical models and experimental results.

The reader is invited to omit Sections 2.2 and 2.3 if the subject material is already familiar. Section 2.2 is a brief review of force commutation and PWM principles. Section 2.3 describes the Current Hysteresis Control which is known here as Direct Current Control to contrast it with the Indirect Current Control of Chapter III. Sections 2.4 and 2.5 present the mathematical model and the stability analysis of the voltage regulated system under Proportional feedback. The Proportional-Integral feedback is described in Section 2.6.

Finally, the Sections 2.7 and 2.8 show the results based on valve-by-valve computer simulations and experimental oscillograms. The experiments were performed with two 2-kW, current hysteresis controlled rectifiers. The software developed for the computer simulations and practical implementation of the rectifiers are described in Appendix A and Appendix B respectively.

2.2 Force Commutation and PWM Principles.

Low harmonic pollution and high input power factor are two of the most desirable requirements in a good rectifier. Most of the thyristor bridge rectifiers, such as the Graetz Bridge [7] mentioned in Chapter I, use the Line Commutation principle. It is employed in circuits excited by ac sources in which the current necessarily falls to zero at some point of the cycle. Negative forward voltage will then extinguish the semiconductor. The problem with line commutation is that neither the power factor nor the harmonics can be controlled.

The above inconveniences can be removed by using Force Commutation, which permits the choice of the "right switch-off time" of a device, without waiting until the current falls to zero [13,57].

Force commutation allows a device to be switched ON and OFF many times in one cycle of the supply frequency. This is the principle of operation used in the Pulse Width Modulation (PWM) techniques. With PWM, the fundamental and the harmonic components, as well as the power factor, can be controlled through the proper choice of the switching pattern [31,58]. Figure 2.1 a) shows a simplified circuit of a PWM rectifier, in which the semiconductors have been replaced with ideal switches. Figure 2.1 b) shows a transistorized version of the Boost principle which has been implemented for the experimental work.

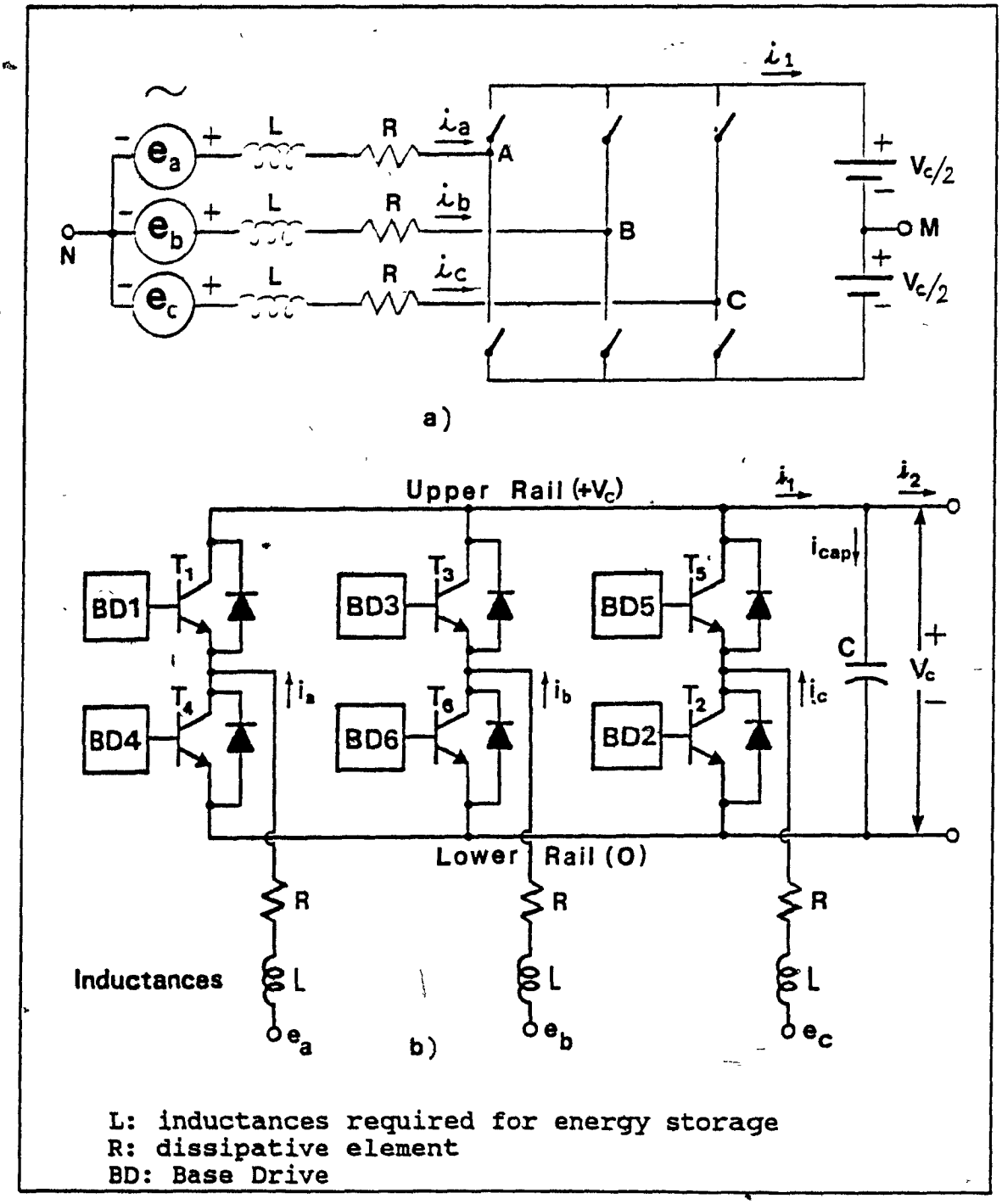


Fig.2.1 Simplified Circuit of a PWM Rectifier
a) Idealized version
b) Transistorized version (Boost Type)

By making the ON-OFF action of the switches (the gates of the semiconductors) follow a particular timing pattern, the input current of the rectifier can be controlled, as shown in Figure 2.2. It can be observed that the modulation pattern of the voltage $V_{(A-M)}$, gives complete control of the input current: magnitude, angle (0^{o} to 360^{o}) and harmonic content. For example, Figure 2.2 a) shows the rectifier operation at unity power factor. Figure 2.2 b) on the other hand, shows the inverter operation, again at unity power factor. Figure 2.2 c) shows the rectifier operation at leading power factor and Figure 2.2 d) shows the operation of the rectifier near 90^{o} lagging. Note that in Figures 2.2 c) and d) the current ripples are coarse because a lower switching frequency is being used.

The principles of operation of the **Direct Current Control**, enable the amplitude of the input currents to be controlled, while keeping the power angle at any desired constant value. This is achieved by measuring the instantaneous phase currents and forcing them to follow a current reference template, by activating the gates of the semiconductors.

Many different switching strategies can be applied to obtain direct control of the current. The so called "Current Hysteresis Control" [37,38,59] is the most popular. A circuit implementation of this switching strategy is shown in Figure

2.3. This method has been used here and will be discussed in some detail.

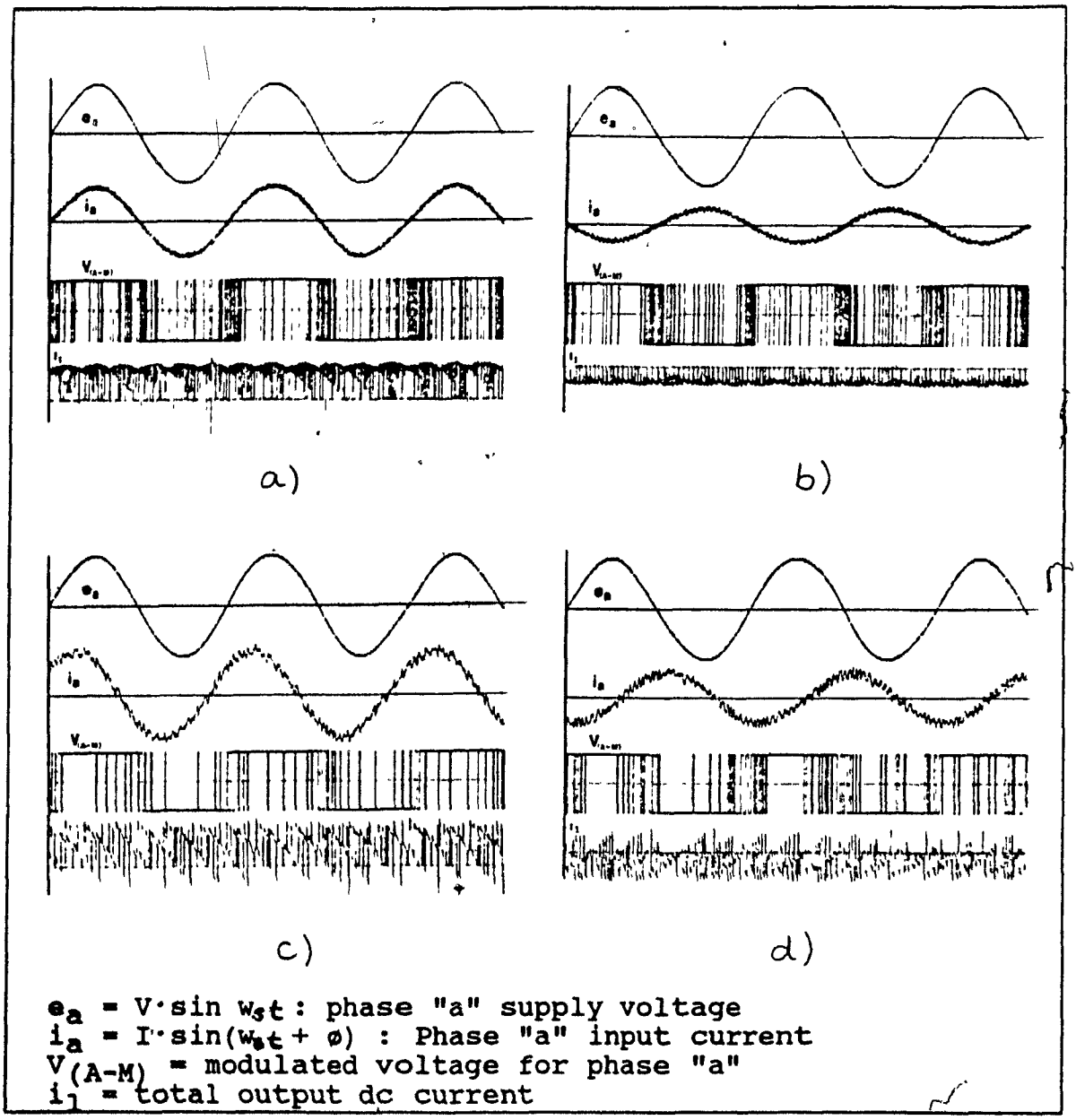


Fig.2.2 Current and voltage waveforms in a PWM rectifier.
a) rectifier operation at unity power factor
b) inverter operation at unity power factor
c) rectifier operation at leading power factor
d) operation near ninety degrees lagging

2.3 Current Hysteresis Control.

The goal of the PWM techniques is to achieve sinusoidal input current in the rectifier, which is controllable in amplitude and in phase. Harmonics should be in the high frequency range where they are cheaper to filter. This can be achieved by defining the desired magnitude and phase angle of the sinusoidal input current waveform. A current template of such a kind can be generated from the input voltage. For example, the filtered output from the secondary of a voltage transformer may be used. Magnitude and phase can then be introduced through electronic methods. For example, amplitude control can be implemented through a multiplier and phase control through a phase shifter. The input current is measured and compared with this current template. By using negative feedback switching of the power devices in the rectifier, the current is forced to follow the desired current template. Using this technique, the input can be made to form any desired current waveshape.

Unfortunately, the current cannot exactly follow the current reference template, because the switching frequency cannot be infinite [39]. An allowable departure from this template is necessary. Current control is thus achieved by defining a "Hysteresis Band", with an upper and lower current reference bound between which the input current is allowed to vary, as shown in Figure 2.4. If a phase current remains within this band then no switching action is required. If the

phase current exceeds the upper current reference bound, then that phase is connected to the positive terminal of the dc load. The opposite action is required when the current exceeds the lower bound.

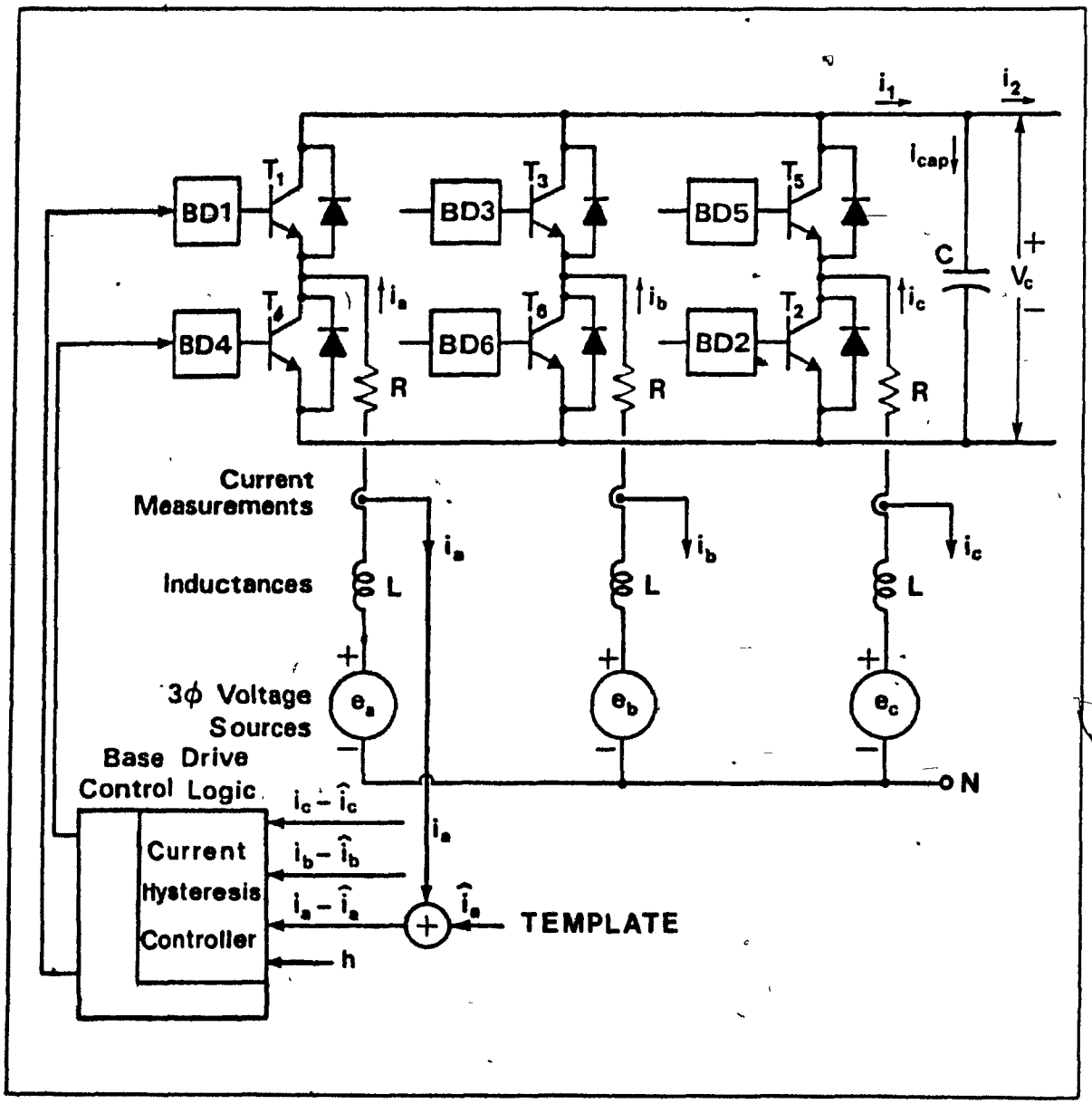


Fig.2.3 Current Hysteresis Control Circuit.

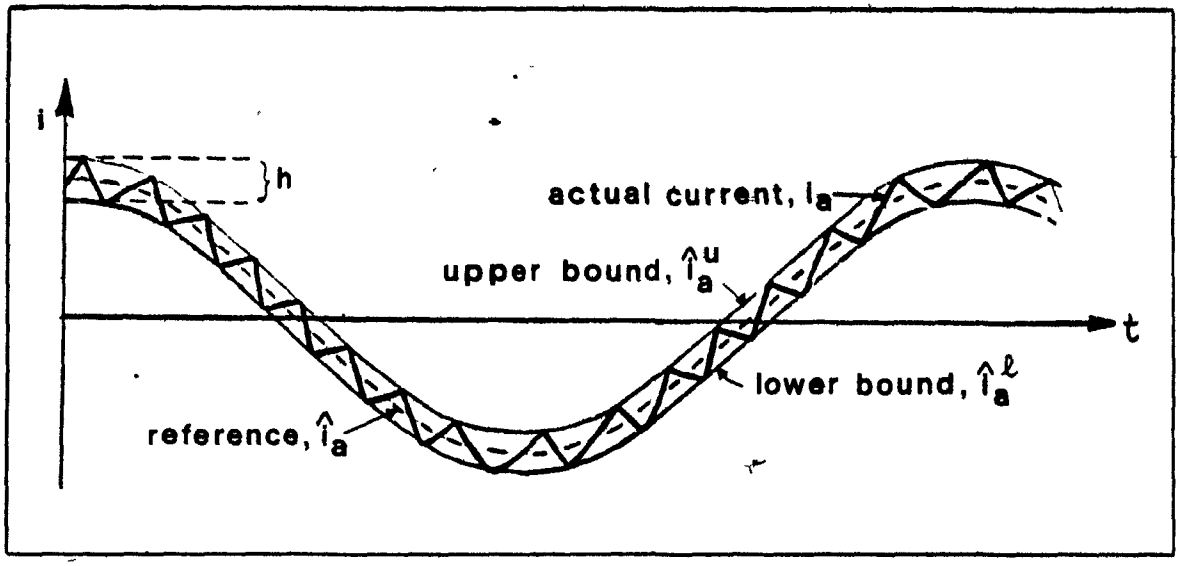


Fig.2.4 Operation of the Current Hysteresis Controller.

2.3.1 Regulation of the dc Voltage.

To make the PWM rectifier work properly, the dc link voltage must be maintained high enough to keep the diodes of the bridge (see Figure 2.3) reverse biased. Otherwise they will conduct and proper control of the bridge will not be possible. A dc battery could be connected as shown in Figure 2.1 a). However, a more cost-efficient solution is to use the voltage across a charged capacitor in the dc link.

The dc link voltage across the capacitor can be regulated using a feedback control loop as shown in Figure 2.5. The feedback voltage control loop allows the rectifier to have a self supporting dc voltage capability. The dc capacitor C is initially given a voltage Vc, which is high enough so that the previously mentioned free-wheeling diodes (across the power transistors of the converter T_1, T_2,...T_6) are reverse

biased. The voltage Vc is measured and compared to a reference voltage V_{REF}. An error signal is obtained, and is used to command the magnitude Im of the three phase currents of the rectifier.

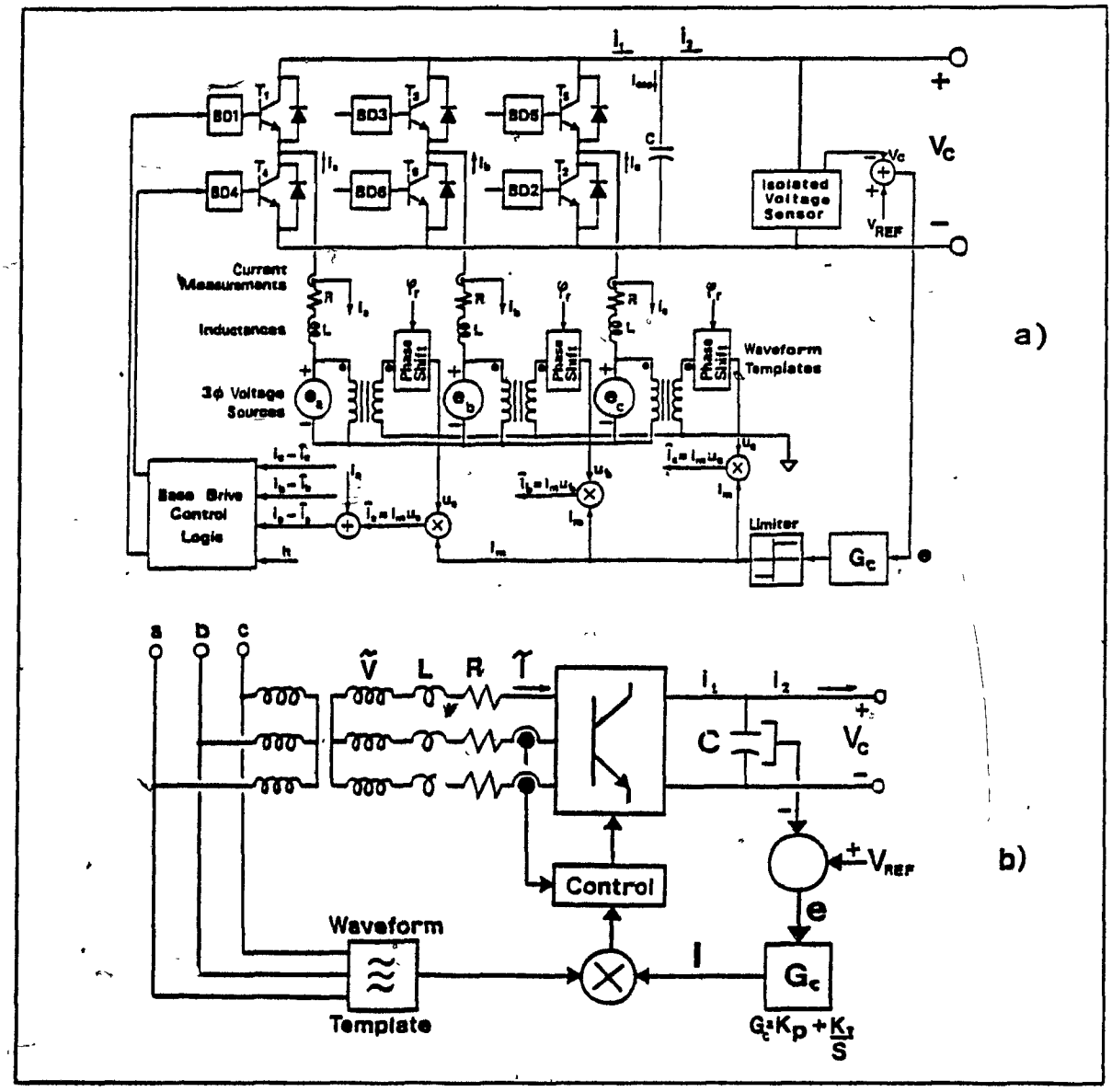


Fig.2.5 Voltage Regulated Rectifier.
a) detailed circuit
b) simplified circuit with input transformer

As shown in Figure 2.5, the current command Im (Im=I· 2) is multiplied with the sinusoidal waveform templates (taken from phase shifted voltages of voltage transformers) to produce the current reference template. Since the template waveshape and power angle are predetermined and the dc link voltage error controls the ac current, the negative feedback loop determines the amount of ac power to be rectified until the dc voltage error is reduced. The dc link capacitor voltage will drop as long as its charge is depleted by the dc current consumed by the load. This dc voltage error can be only reduced once the power rectified from the ac side is sufficient to feed the dc load power and replenish the depleted charge across the capacitor. As is well known, in proportional feedback there is always a voltage error with respect to the voltage reference.

The voltage-regulated current-controlled PWM rectifier described up to here has some intrinsic properties and operational constraints. These characteristics will be analyzed with the help of mathematical tools.

2.4 Mathematical Model.

When the hysteresis band "h" becomes small enough, the switching ripples can be neglected and a "harmonic-free" mathematical model can be developed [30]. This approximation is valid even with hysteresis bands as large as 25% of the total current.

The total, instantaneous rectifier input power, in accordance with Figure 2.5, can be expressed as:

$$p_{in}(t) = e_a(t)\cdot i_a(t) + e_b(t)\cdot i_b(t) + e_c(t)\cdot i_c(t)$$
$$- R\cdot\{i_a(t)^2 + i_b(t)^2 + i_c(t)^2\}$$
$$- \frac{1}{2} L \frac{d}{dt}\{i_a(t)^2 + i_b(t)^2 + i_c(t)^2\} \qquad (2.1)$$

where the supply phase voltages are

$$e_a(t) = V\cdot\sqrt{2}\cdot\sin w_s t$$
$$e_b(t) = V\cdot\sqrt{2}\cdot\sin(w_s t - 120^o)$$
$$e_c(t) = V\cdot\sqrt{2}\cdot\sin(w_s t - 240^o) \qquad (2.2)$$

and the phase currents are

$$i_a(t) = I(t)\cdot\sqrt{2}\cdot\sin(w_s t + \phi)$$
$$i_b(t) = I(t)\cdot\sqrt{2}\cdot\sin(w_s t + \phi - 120^o)$$
$$i_c(t) = I(t)\cdot\sqrt{2}\cdot\sin(w_s t + \phi - 240^o) \qquad (2.3)$$

By substituting eqs.(2.2) and (2.3) into (2.1):

$$p_{in}(t) = 3\cdot\{V\cdot I(t)\cdot\cos\phi - R\cdot I(t)^2 - \frac{1}{2} L \frac{d}{dt} I(t)^2\} \qquad (2.4)$$

The total output power (before the dc capacitor) is:

$$p_1(t) = i_1(t) \cdot v_c(t) \qquad (2.5)$$

where $i_1(t)$ is the local average dc current and $v_c(t)$ is the dc link voltage.

If the terms $R \cdot I(t)^2$ from eq.(2.4) are assumed to include the rectifier losses, then:

$$p_{in}(t) = p_1(t) \qquad (2.6)$$

or

$$3 \cdot (V \cdot I(t) \cdot \cos \phi - R \cdot I(t)^2 - \frac{1}{2} L \cdot \frac{d}{dt} I(t)^2) = v_c(t) \cdot i_1(t) \qquad (2.7)$$

Equation (2.7) is the **"Power Balance Equation"** of the Direct Current Control Rectifier and represents the main mathematical tool of the system.

2.5 Stability analysis.

As eq.(2.7), is nonlinear, the problem of stability can be analyzed by assuming small perturbation around a specific operating point. From eqs.(2.5) and (2.7):

$$3 \cdot (V \cdot I(t) \cdot \cos \phi - R \cdot I(t)^2 - \frac{1}{2} L \cdot \frac{d}{dt} I(t)^2) = p_1(t) \qquad (2.8)$$

Assuming that V, cos ø, R and L are all constants and applying small perturbations to I(t) and $p_1(t)$, one has:

$$I(t) = Io + \Delta I \qquad (2.9)$$

$$p_1(t) = P_1 + \Delta p_1 \qquad (2.10)$$

Substituting (2.9) and (2.10) into eq.(2.8):

$$3\cdot(V\cdot(Io+\Delta I)\cdot\cos\phi - R\cdot(Io+\Delta I)^2 - \frac{1}{2}L\frac{d}{dt}(Io+\Delta I)^2 =$$

$$= P_1 + \Delta p_1 \qquad (2.11)$$

Subtracting eq.(2.8) with $I(t)=Io$ and $p_1(t)=P_1$ from eq.(2.11), and neglecting second order terms:

$$3\cdot V\cdot\cos\phi\cdot\Delta I - 6\cdot R\cdot Io\cdot\Delta I - 3\cdot L\cdot Io.\frac{d\Delta I}{dt} = \Delta p_1 \qquad (2.12)$$

Equation (2.12) is a linearization of eq.(2.8) around the point (Io,P_1). Taking the Laplace Transform of eq.(2.12):

$$\Delta I(S)\cdot(3\cdot V\cdot\cos\phi - 6\cdot R\cdot Io - 3\cdot L\cdot Io\cdot S) = \Delta P_1(S) \qquad (2.13)$$

and writing

$$G_1(S) = \frac{\Delta P_1(S)}{\Delta I(S)} = 3\cdot(V\cdot\cos\phi - 2\cdot R\cdot Io - L\cdot Io\cdot S) \qquad (2.14)$$

Equation (2.14) represents the **transfer function** of the rectifier around the operating point.

The instantaneous dc load power, $p_2(t)$, is related with the output power $p_1(t)$ through the equation:

$$C\cdot v_c\cdot\frac{dv_c}{dt} = p_1(t) - p_2(t) \qquad (2.15)$$

where

$$p_2(t) = v_c\cdot i_2 \qquad (2.16)$$

i_2 and v_c are the dc load current and voltage respectively. Equation (2.15) is also nonlinear and so small perturbation linearization is also required. With Laplace Transform on the linearized equation:

$$Vc \cdot C \cdot S \cdot \Delta Vc(S) = \Delta P_1(S) - \Delta P_2(s) \qquad (2.17)$$

Vc is the capacitor voltage at the same operating point as eq.(2.14). ΔP_2 represents a small change in the load power of the system. The transfer function of the dc capacitor is then:

$$G_2(S) = \frac{\Delta Vc(S)}{\Delta P_1(S) - \Delta P_2(S)} = \frac{1}{Vc \cdot C \cdot S} \qquad (2.18)$$

Equations (2.14) and (2.18) yield the representation of the open loop rectifier transfer function around the operating point and is shown in Figure 2.6.

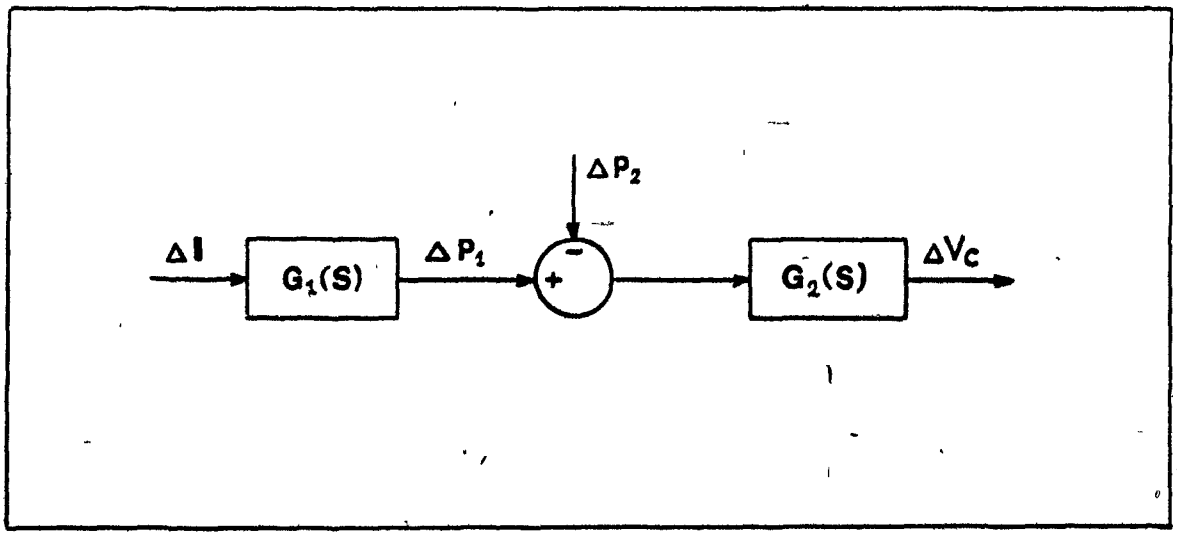


Fig.2.6 Open Loop Rectifier Transfer Function Around the Operating Point.

2.5.1 Proportional Control.

Upon introducing the voltage feedback and proportional control with gain Kp, the system can be represented as shown in Figure 2.7.

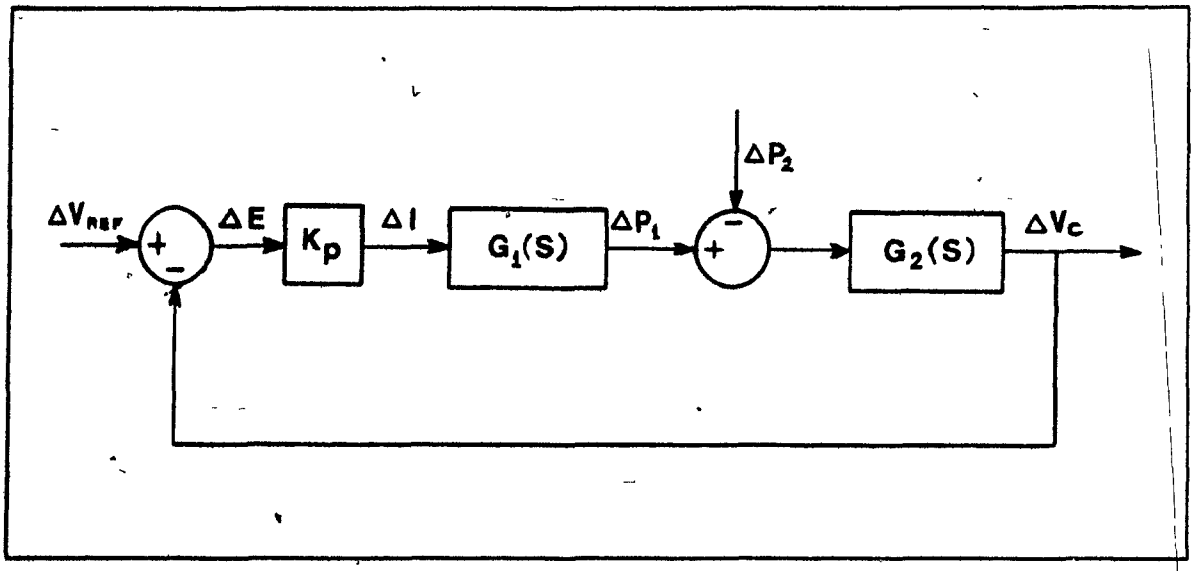


Fig.2.7 Closed-Loop Rectifier System.

Stability criterion can now be applied for the closed-loop system of Figure 2.7:

$$Kp \cdot G_1(S) \cdot G_2(S) + 1 = 0 \qquad (2.19)$$

which finally yields:

$$S = -3 \cdot Kp \cdot \frac{(V \cdot \cos \phi - 2 \cdot R \cdot Io)}{C \cdot Vc - 3 \cdot Kp \cdot L \cdot Io} \qquad (2.20)$$

From eq.(2.20) two conditions of stability are encountered:

$$Io < \frac{V \cdot \cos \phi}{2 \cdot R} \qquad (2.21)$$

and

$$Io < \frac{C \cdot Vc}{3 \cdot Kp \cdot L} \qquad (2.22)$$

Relation (2.21) is normally satisfied because cos ø is chosen close to unity and R is very small. Relation (2.22), on the other hand, establishes an important relation between the dc capacitor, its voltage, the proportional gain and the input inductance of the rectifier. Relation (2.22) predicts that Kp cannot be too big. Otherwise C has to be excessively large.

2.6 Proportional-Integral Control.

Because Kp cannot be too big, the rectifier regulation can become poor due to the steady-state error introduced. The addition of an integral gain K_I can solve the problem.

The transfer function of a PI control can be represented by:

$$G_C(S) = Kp + \frac{K_I}{S} \qquad (2.23)$$

where Kp and K_I are the proportional and integral gains respectively. Replacing Kp for $G_C(S)$ into eq.(2.19):

$$G_C(S)\cdot G_1(S)\cdot G_2(S) + 1 = 0 \qquad (2.24)$$

and replacing eqs.(2.14), (2.18) and (2.23) into (2.24), a second degree algebraic equation is obtained:

$$A\cdot S^2 + B\cdot S + Co = 0 \qquad (2.25)$$

where

$$A = C\cdot Vc - 3\cdot Kp\cdot L \qquad (2.26)$$

$$B = 3\cdot(Kp\cdot V\cdot\cos\ø - 2\cdot Kp\cdot R\cdot Io - K_I\cdot L\cdot Io) \qquad (2.27)$$

$$Co = 3\cdot K_I\cdot(V\cdot\cos\ø - 2\cdot R\cdot Io) \qquad (2.28)$$

The solution of eq.(2.25) yields

$$S = -\frac{B}{2A} \pm \sqrt{\left(\frac{B}{2A}\right)^2 - \frac{C}{A}} \qquad (2.29)$$

To have a stable system, two conditions have to be satisfied:

$$\frac{C}{A} > 0 \qquad (2.30)$$

$$\frac{B}{2A} > 0 \qquad (2.31)$$

From rel.(2.30) one gets

$$Io < \frac{C \cdot Vc}{3 \cdot Kp \cdot L} \qquad (2.32)$$

$$Io < \frac{V \cdot \cos \phi}{2 \cdot R} \qquad (2.33)$$

and from rel.(2.31)

$$Io < \frac{C \cdot Vc}{3 \cdot Kp \cdot L} \qquad (2.34)$$

$$Io < \frac{Kp \cdot V \cdot \cos \phi}{2 \cdot R \cdot Kp + L \cdot K_I} \qquad (2.35)$$

Relations (2.32) and (2.34) are exactly the same as (2.22), and rel.(2.33) is also the same as (2.21). However, rel.(2.35) establish a new stability limit for the system with PI control, which is more restrictive than the limit given by rel.(2.33). It can be seen that rel.(2.35) becomes the same as rel.(2.33) when K_I=0 (only Proportional Control). Fortunately,

the new restriction set by rel.(2.35) has a good stability margin. By choosing the right value of K_I, it is possible to get a good transient response in addition to having zero steady-state error.

2.7 Valve-by-Valve Digital Simulations.

The behaviour of the experimental rectifiers is most faithfully represented by the Valve-by-Valve Digital Simulation Program. This simulation program is based on treating the rectifier bridge as a piece-wise circuit problem. The ON-OFF states of each of the power switches of the bridge give rise to eight possible circuit topologies, which are discussed in Appendix A. The instants of switching of the semiconductors are monitored by keeping track of the intersections of the actual input current with the upper and lower bound of the hysteresis band and so a time sequence of eight circuit topologies is generated. The differential equations arising from the Kirchhoff Voltage and Current Laws for the topologies are solved numerically and they are joined together by the requirements that the flux linkages of inductances and electric charges across capacitors must be continuous.

The Valve-by-Valve Simulation Program is very simple and powerful. It is flexible enough to simulate almost every situation and circuit configuration. Once the simulation program is checked against experimental results at the 2-kW

power levels of the laboratory rectifiers, the program can be used to predict the behaviour of large rectifiers in the 100 kW or MW range.

2.7.1 Examples of Valve-by-Valve Simulations.

Figure 2.8 shows a power reversal simulation for a medium power rectifier. Figure 2.9 shows a power reversal for a Rectifier/Inverter link system. Abnormal conditions, such as the loss of one phase, can also be simulated using the Valve-by-Valve program as is shown in Figure 2.10, where phase "a" has been opened. These simulations have also verified the stability limits given by rels.(2.21), (2.22) and (2.35).

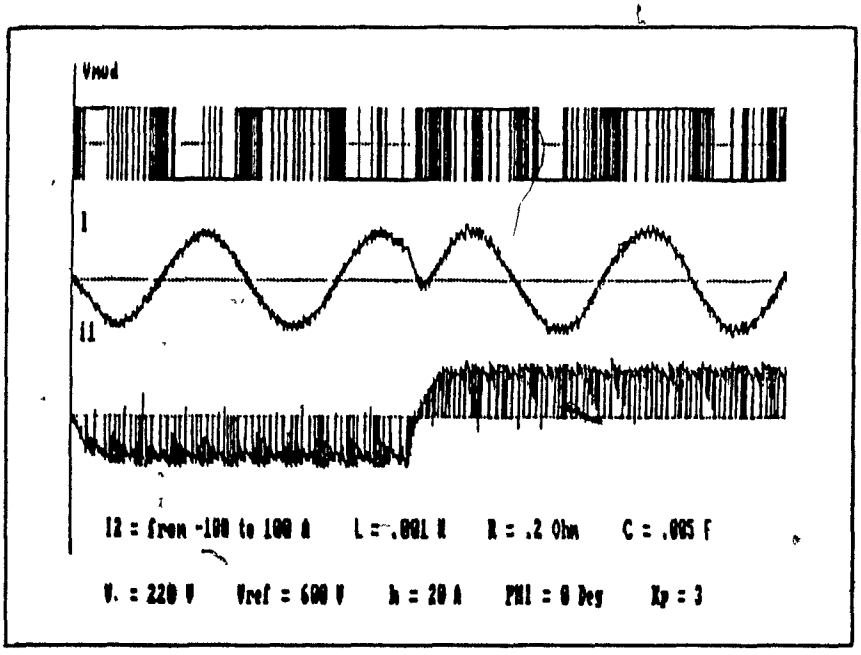


Fig.2.8 Valve-by-Valve Simulation for a Medium Power Rectifier During Power Reversal.
a) modulated rectifier voltage v_{mod}
b) input current, I
c) output dc current before C, i_1

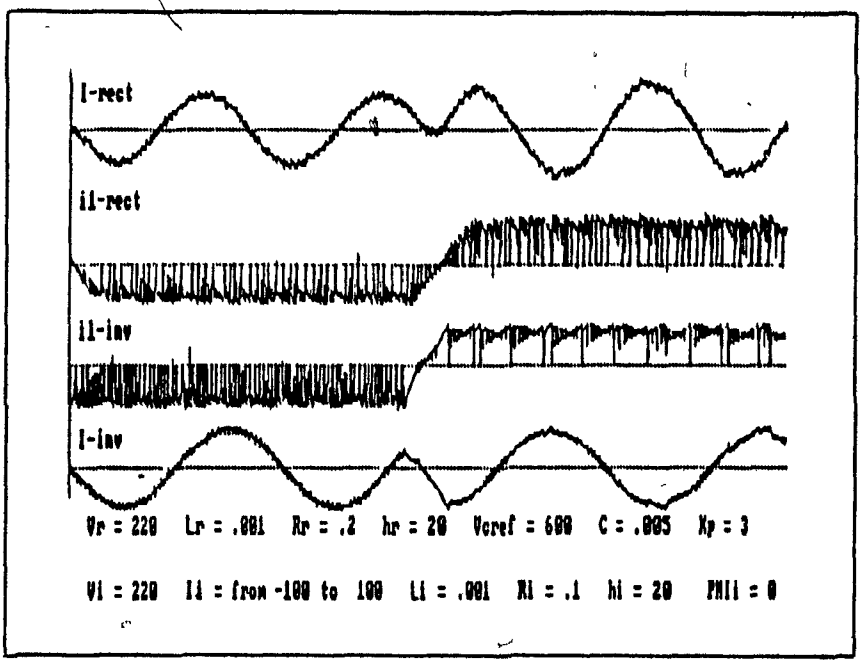


Fig.2.9 Valve-by-Valve Simulation for a Rectifier/Inverter Link During Power Reversal.

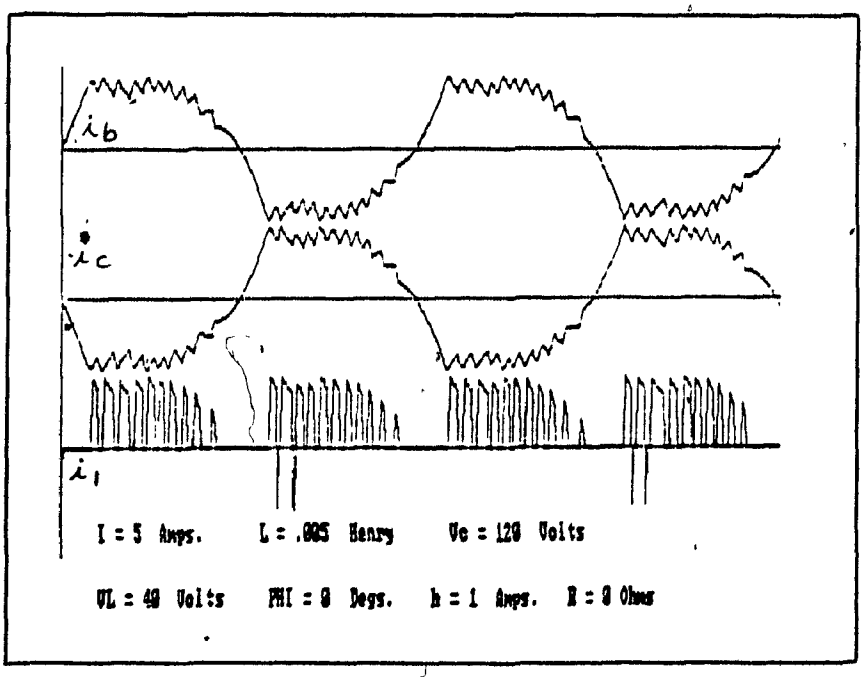


Fig.2.10 Valve-by-Valve Simulation During Lost of One Phase.

2.8 Experimental Results.

Extensive experimental tests have been performed on the Current Hysteresis Controlled Rectifier. Most of this work can be found in the author's M. Eng. Thesis [31]. Only two important results are shown here.

Figure 2.11 shows an oscillogram of the rectifier operating near the stability limit given by relation (2.21). The input current "I" begins to distort dangerously and spikes appear in the dc link voltage. If the power demand is increased, the system collapses.

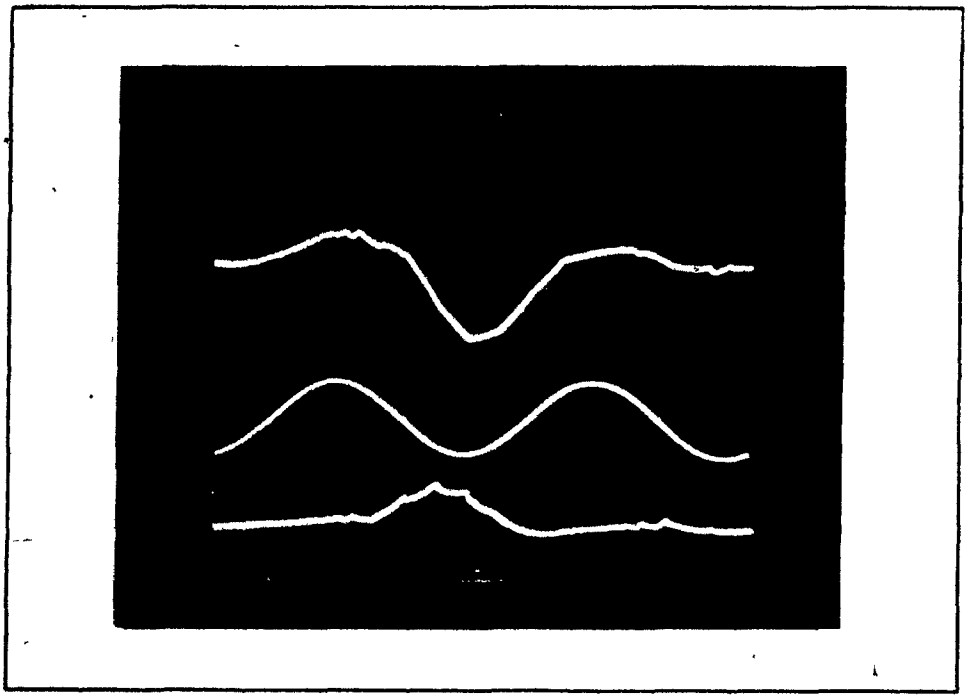


Fig.2.11 Rectifier Operation Near the Stability Limit.
a) input current (5A/div)
b) input supply voltage (40 V)
c) dc voltage error (5V/div)

Figure 2.12 shows a reversal of power response from rectifier to inverter operation. The load dc current is forced to change from +6 to -6 A dc almost instantaneously. The power angle has been adjusted to operate at unity power factor and remains as such even after the inversion. It can be seen that the ac current during rectification is higher than during inversion. This is due to the ohmic losses (they are always positive).

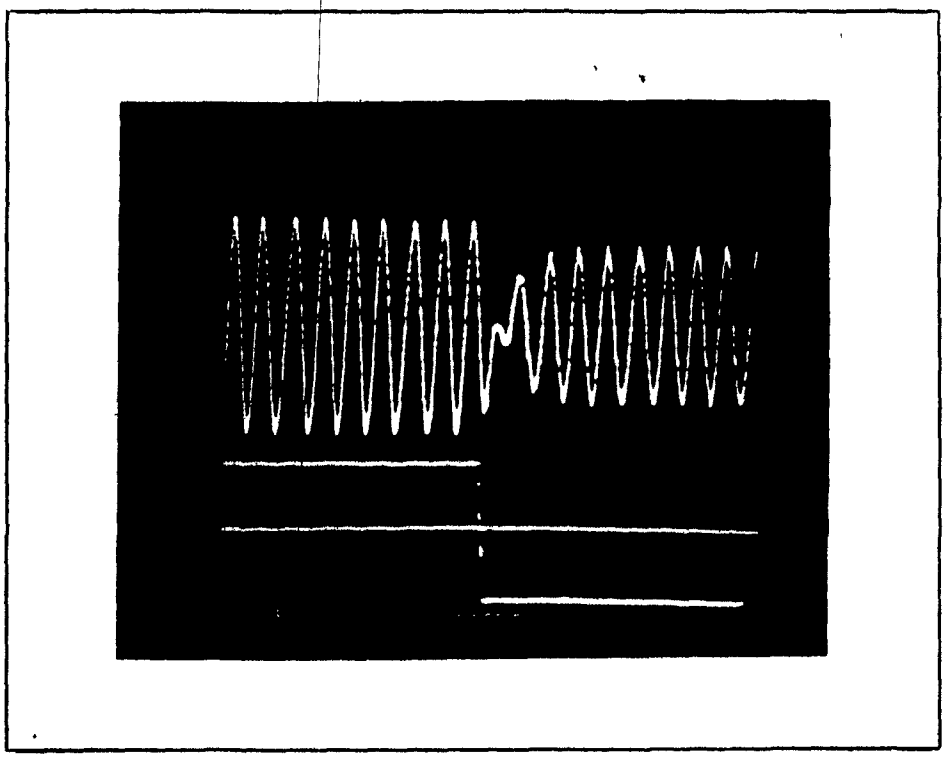


Fig.2.12 Oscillogram of Reversal of Power.
a) input current (+7 to -5 A ac)
b) load current (+6 to -6 A dc)

The parameters for this experiment were: C = 12 mF, wL = 2.5 Ohms, R = 1 Ohm, V_{REF} = 120 V dc, V = 45 V ac and Kp = 3 A/V.

2.9 Summary.

A brief description of the Direct Current Control Method has been presented. Because the purpose of this chapter has only been to introduce the concepts and operation of the Direct Current Controlled rectifiers, the ideas have not been developed in detail. More information can be found in ref.[31]. The additional knowledge beyond those described in the M. Eng. Thesis [31] has been: i) the use of Proportional-Integral Control in Section 2.6, and ii) the development of the Valve-by-Valve simulations in Section 2.7.

The next chapter will describe the method of Indirect Current Control, in which the rectifier is controlled without the necessity of measuring the input currents.

CHAPTER III

INDIRECT CURRENT CONTROL

3.1 Introduction.

In the previous chapter, the method of Direct Current Control, using Current Hysteresis Controllers, was analyzed. Mathematical analysis, digital simulations and experiments have revealed the behaviour of that system.

The present chapter develops the ideas concerning to the method of Indirect Current Control. This method introduces a simplification with respect to the previous system: the elimination of the high quality broad bandwidth current measuring transducers. The rest of the system is very similar to the former: a dc voltage feedback loop is also required to keep the rectifier under control. However, because input currents are not being measured, dedicated hardware that takes into account the rectifier parameters is introduced into the feedback. This basic difference brings a new degree of freedom to the system: the appearance of dc components in the input currents during transients. As a consequence, the system can have a very limited stable region of operation if adequate compensations are not implemented. This problem in the Direct Control method is automatically eliminated through the inner hysteresis current control, which enforces current waveform and phase angle compliancies.

The reasons mentioned above have made it necessary, to develop a different set of mathematical tools and to use power invariant transformations.

This chapter explains the fundamentals of the Indirect Current Control and then analyzes the well known Sinusoidal Pulse Width Modulation (SPWM) method, which has been implemented in experimental work. Subsequently, the dc voltage regulation is described and then the mathematical model is developed. The next step analyzes the stability of the system, particularly its operation at unity power factor. The chapter follows with a brief discussion about parameter sensitivity and comparison with the Direct Current Control method. Finally, the mathematical analyses are verified with computer simulations and experimental results.

This chapter does not discuss hardware details as they are explained in Appendix B.

3.2 Indirect Current Control: the Fundamentals.

The problem of how to control the input rectifier current without measuring it is solved by knowing the impedance between the source and the rectifier terminals. A periodical 60 Hz modulation of the rectifier power switches produces a fundamental voltage $\tilde{V}_{mod}$, which interacts with the supply voltage $\tilde{V}$, through the impedance R+jX, producing a very well defined phase current $\tilde{I}$, as shown in Figure 3.1.

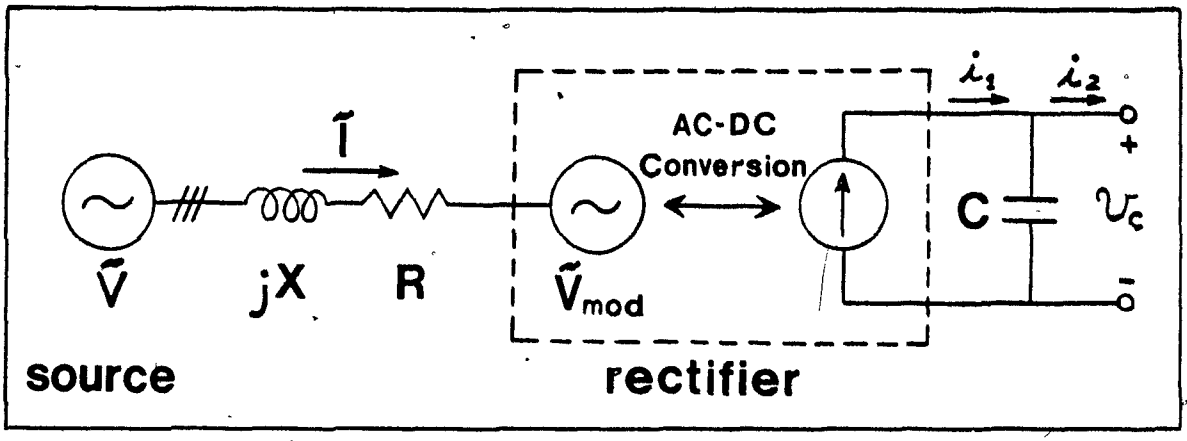


Fig.3.1 Indirect Current Control Principle.

As the source voltage $\tilde{V}$ can be known (and also R and L), the current can be controlled by changing the modulating signal which generates the fundamental $\tilde{V}_{mod}$. Constant power factor operation may be obtained by the precise control of this fundamental, as shown in Figure 3.2.

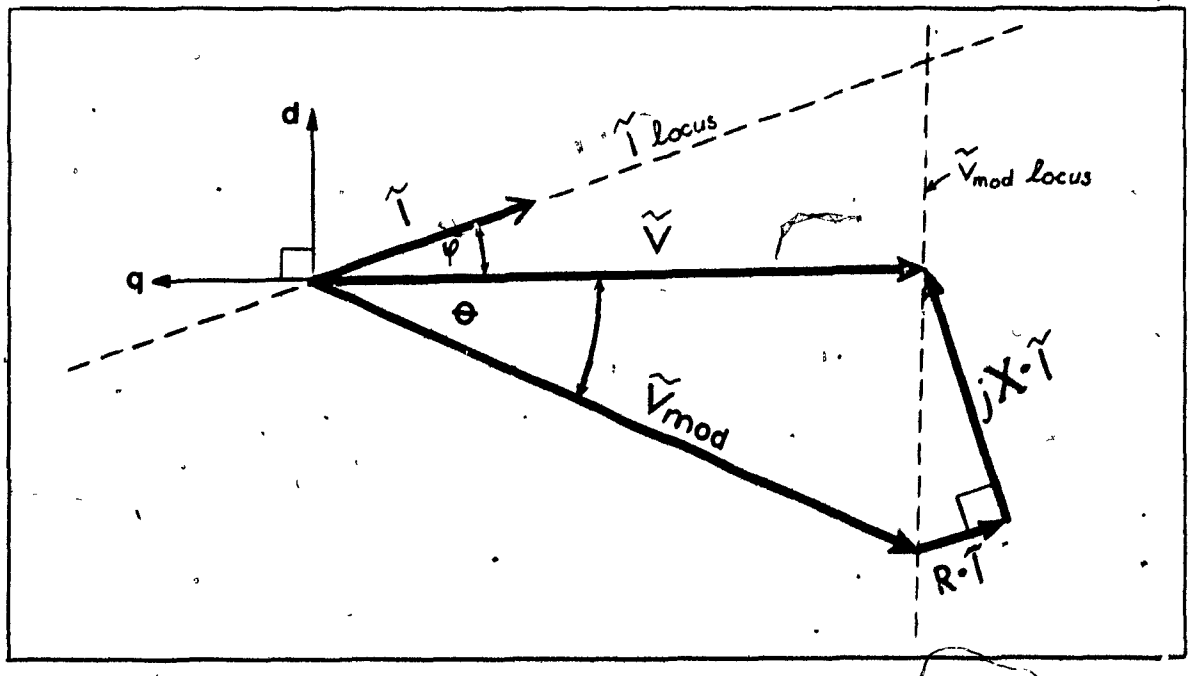


Fig.3.2 Constant Power Factor Operation Principle.

From Figure 3.2, the trigonometrical equations describing the rectifier maintained at a constant power angle ø are easily found:

$$V_{mod} \cdot \cos\theta = V + (X \cdot \sin\phi + R \cdot \cos\phi) \cdot I \qquad (3.1)$$

$$V_{mod} \cdot \sin\theta = (X \cdot \cos\phi + R \cdot \sin\phi) \cdot I \qquad (3.2)$$

Eqs.(3.1) and (3.2) represent the in-phase and the in-quadrature terms of V_{mod} respectively. V_{mod} and θ are the magnitude and the phase angle of V_{mod} respectively.

3.3 Sinusoidal PWM rectifier.

The problem of controlling the current has been translated to a problem of controlling the fundamental voltage V_{mod}. There are many different switching strategies which can generate the desired fundamental V_{mod}.

It is not the purpose of this Thesis to discuss the best modulation method, because this matter has been thoroughly analyzed in many references [20,21,22,23,67]. The Sinusoidal Pulse Width Modulation (SPWM) has been selected here for three reasons: i) it is relatively simple to implement, ii) it can generate good sinusoidal currents and iii) it is a very well known method, allowing us to avoid explanations beyond the purpose of this work.

The conventional technique of generating three-phase SPWM waveforms in a converter uses a triangular carrier wave and a three-phase sinusoidal modulating wave.

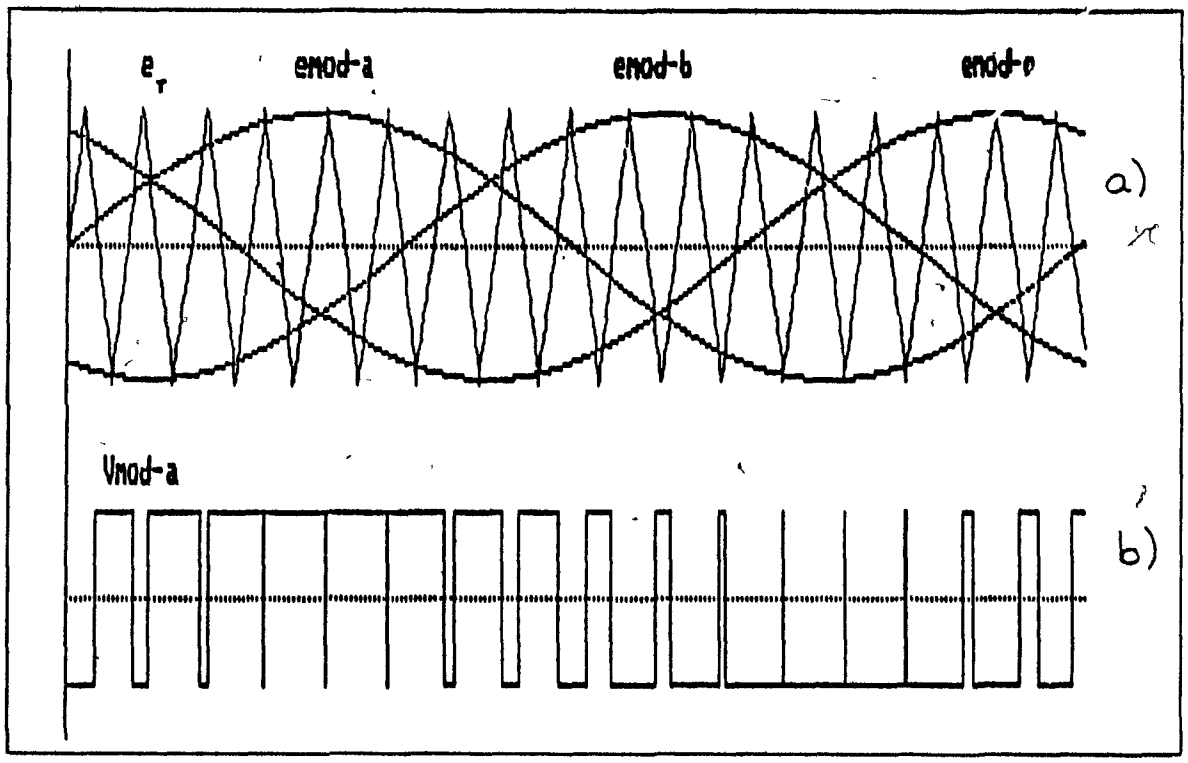


Fig.3.3 Operation Principle of SPWM.
a) modulating signals and triangular carrier
b) modulated voltage for phase "a"

As it is shown in Figure 3.3 a), the carrier signal e_T has an amplitude E_T and angular frequency w_T. The sinewaves e_{moda}, e_{modb} and e_{modc} are called the modulating signals. They are balanced three-phase voltages which have the amplitude E_{mod} and the source angular frequency w_S. Figure 3.3 b) shows the modulated voltage of phase "a", V_{moda}, which has a fixed amplitude $\pm$ Vc/2 determined by the dc voltage. The switching times are determined by the intersections of e_{moda} and e_T. Since the ratio of the two frequencies w_T/w_S is generally incommensurable, the SPWM wave becomes a non-periodic function. The harmonic analysis of such a wave can be made by

using the double Fourier series [68]. The resultant modulated signal for phase "a", shown in Figs.3.3 b) and 3.4 a), v_{moda}, can be expressed by the Double Fourier Series in complex form as:

$$v_{moda} = \sum_{m} \sum_{n} K_{mn} \cdot \exp[j(m \cdot w_T t + n \cdot w_S t)] \qquad (3.3)$$

where K_{mn} is the complex Fourier coefficient.

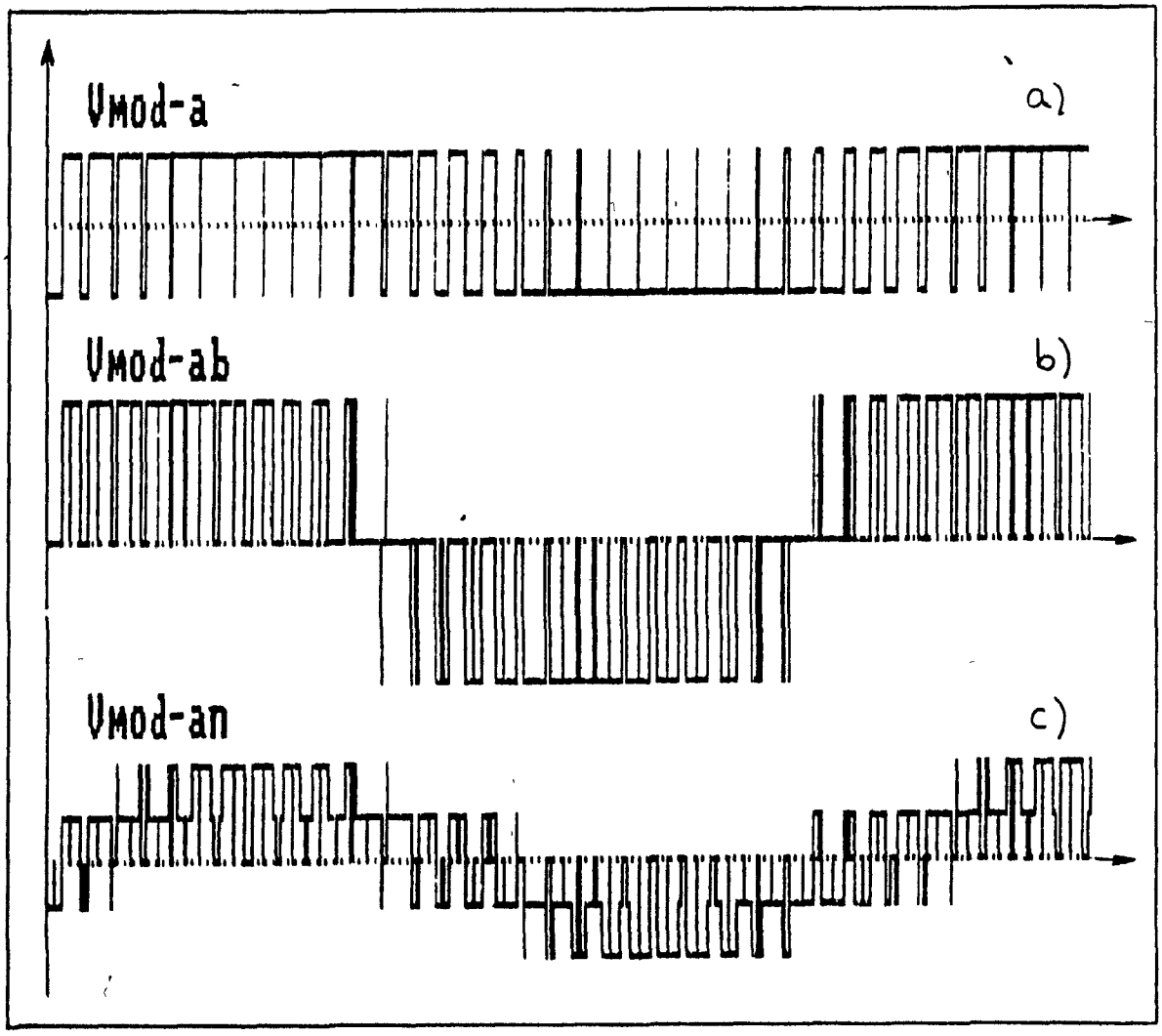


Fig.3.4 Switching Waveforms in SPWM for the phase "a".
a) modulated voltage, v_{moda}
b) phase-to-phase rectifier voltage, v_{moda-b}
c) phase-to-neutral rectifier voltage, v_{moda-n}

Further development of eq.(3.3) gives the SPWM phase-to-phase voltage, v_{moda-b}, as [69]:

$$v_{moda-b} = \frac{\sqrt{3}\cdot Vc\cdot E_{mod}}{2\cdot E_T}\cdot\sin(w_s t + 30^o) + Vc\cdot\sum_m\sum_n(\text{Bessel Functions}) \qquad (3.4)$$

where Vc is the dc link voltage. The first term is the phase-to-phase fundamental voltage. The second term contains the unwanted frequency components. The desired fundamental V_{mod} of Figure 3.1 belongs to the phase-to-neutral voltage of Figure 3.4 c). It can be obtained from the fundamental of v_{moda-b} in eq.(3.4):

$$\text{Fund}[v_{moda-n}(t)] = \frac{0.5\cdot Vc}{E_T}\cdot E_{mod}\cdot\sin w_s t \qquad (3.5)$$

As Vc and E_T can be considered constants, the magnitude of V_{mod} is proportional to the amplitude of the modulating signal, E_{mod}, and they are in phase. This result is very important because the control of V_{mod} becomes straightforward and its implementation simple. The phase-to-neutral voltage, $v_{moda-n}(t)$ is shown in Figure 3.4 c).

As shown in Figure 3.5, the "Sinusoidal PWM Control Block" handles the function of generating the ON-OFF logic commands to the base drives of the Rectifier Bridge based on the inputs e_{moda}, e_{modb} and e_{modc}. The details in Appendix B show the production of the triangular carrier e_T and the detection of its intersections with the three modulating waveforms.

3.3.1 Regulation of the dc Voltage.

The same ideas developed in Section 2.2.1 are valid here, except that the error signal will now control V_{mod} instead of the magnitude of the input current I. The link between V_{mod} and I is obtained from eqs.(3.1) and (3.2). These equations show that hardware containing these expressions has to be built into the feedback loop to transform the error signal in the desired fundamental V_{mod}. Figure 3.5 shows the block diagram for the implementation of the voltage-regulated SPWM rectifier. Note that the parameters L and R have been called Lc and Rc in the control block. This is because, in general, one cannot be sure of the exact values of L and R, and also because the system becomes more general for analytical purposes.

With the help of Figures 3.2 and 3.5, the mechanism of the voltage control can be understood. When the dc voltage is perturbed by the load, the error signal changes the magnitude of the current command I which, through eqs.(3.1) and (3.2), modifies V_{mod} in magnitude and angle, making it follow a locus of constant power factor. As the selection of cos ø is arbitrary through the control blocks of Figure 3.5, unity or even leading power factor can be selected, for all load conditions.

It can be noted that in Figure 3.5 the in-phase and the in-quadrature references are formed from the filtered outputs of voltage transformers whose primaries are connected to the

source voltages. The current command I, which is still taken from the error $e=V_{REF}-v_c$ through the transfer function Gc, is combined with V, Xc, Rc, sin ø and cos ø through electronic adders, multipliers and proportioners to implement eqs.(3.1) and (3.2).

Only the a-phase implementation is shown. The b and c-phases are identical except that the in-phase and the in-quadrature references are generated with -120_o and -240_o phase shifts.

3.4 Mathematical Model.

To develop the mathematical tools, the harmonics will be neglected. They do not affect the results when they are small enough, as is the case for most of the practical PWM systems.

The mathematical expression for the instantaneous input power is the same as eq.(2.1):

$$p_{in}(t) = e_a(t)\cdot i_a(t) + e_b(t)\cdot i_b(t) + e_c(t)\cdot i_c(t)$$
$$- R\cdot(i_a(t)^2 + i_b(t)^2 + i_c(t)^2$$
$$- \frac{1}{2} L \frac{d}{dt}(i_a(t)^2 + i_b(t)^2 + i_c(t)^2) \qquad (3.6)$$

where $e_a(t)$, $e_b(t)$ and $e_c(t)$ are the same as eqs.(2.2). However, $i_a(t)$, $i_b(t)$ and $i_c(t)$ cannot be represented by eqs.(2.3), because the currents are not measured directly and hence they might have dc components during transients.

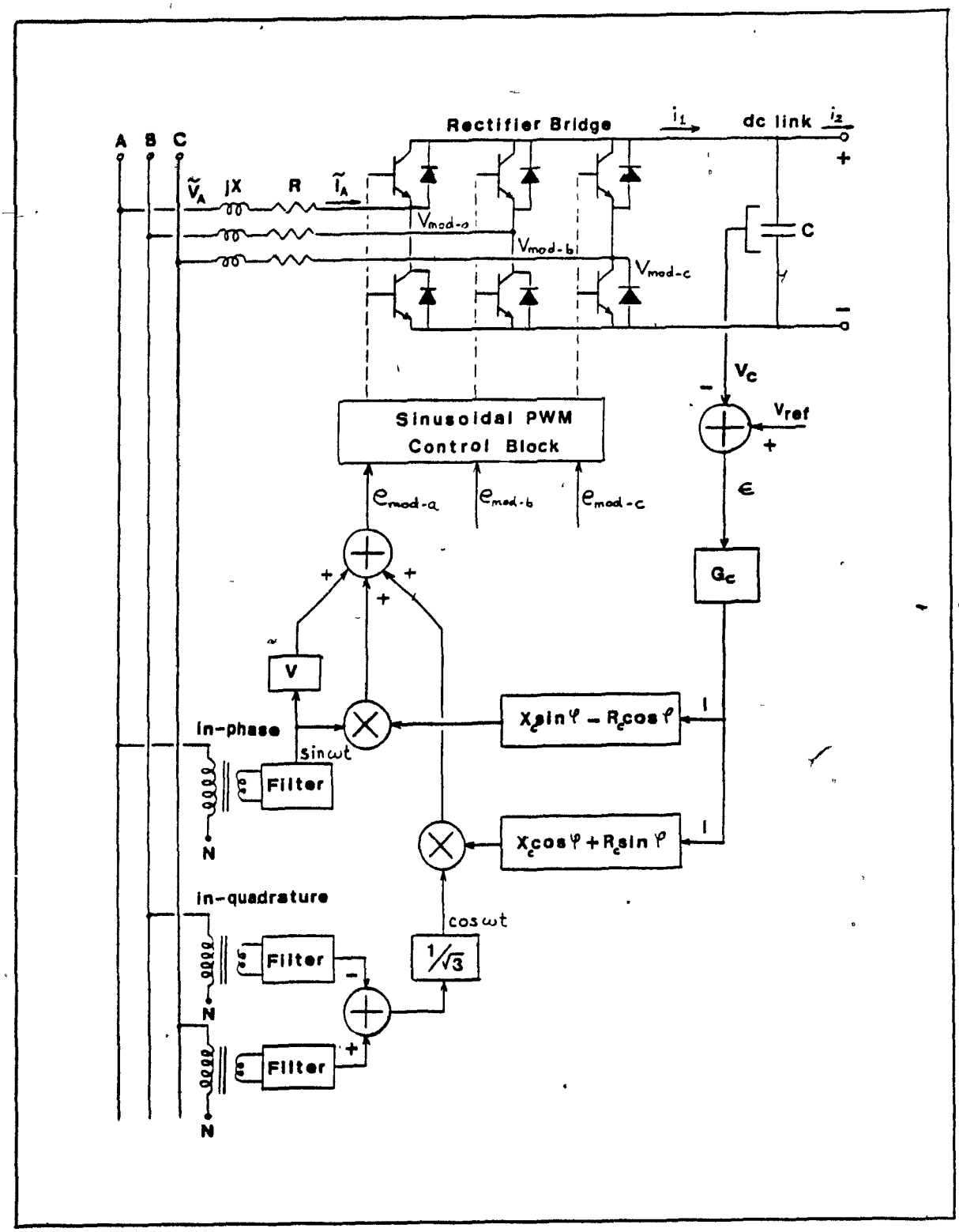


Fig.3.5 Block Diagram of the SPWM Voltage-Regulated Rectifier.

3.4.1 Unity Power Factor Operation.

For simplicity, the analysis will be based on a unity power factor controller. For a supply phase voltage:

$$e_a(t) = \sqrt{2} \cdot V \cdot \sin w_s t \qquad (3.7)$$

From eqs.(3.1) and (3.2), for the case cos ø = 1, it is required that in the control blocks:

$$V_{moda} \cdot \cos \theta = V - Rc \cdot I \qquad (3.8)$$

$$V_{moda} \cdot \sin \theta = Xc \cdot I \qquad (3.9)$$

The time function $v_{moda}(t)$ then becomes:

$$v_{moda}(t) = \sqrt{2} \cdot ((V - Rc \cdot I) \cdot \sin w_s t - Xc \cdot I \cdot \cos w_s t) \qquad (3.10)$$

Eq.(3.10) represents the voltage V_{mod} generated through the action of the control blocks of Figure 3.5. The voltage difference $e_a(t)-v_{moda}(t)$, will produce a rectifier current i_a which is a solution to the differential equation:

$$L \cdot \frac{d}{dt} i_a + R \cdot i_a = e_a(t) - v_{moda}(t) \qquad (3.11)$$

For a constant value of I, in eq.(3.10), the solution of eq.(3.11) is:

$$i_a(t) = \sqrt{2} \cdot Io \cdot \sin w_s t + A \cdot \exp(-t/T) \qquad (3.12)$$

where A is the constant of integration with T=L/R and Io=I when Rc=R and Xc=X. In general, I is not constant but a function of time I(t) determined from the variations of the error signal.

A set of equivalent eqs.(3.7) to (3.12) for the b-phase and the c-phase can be written with time delay angles of 120° and 240° respectively.

As v_{moda}, v_{modb} and v_{modc} can be evaluated through a set of equations represented by eq.(3.10), a more tractable power equation can be used, this time right at the ac terminals of the rectifier:

$$p_{in}(t) = v_{moda}(t)\cdot i_a(t) + v_{modb}(t)\cdot i_b(t) + v_{modc}(t)\cdot i_c(t) \qquad (3.13)$$

If i_1 is the local average of the output current of the rectifier, the dc power output is:

$$p_1(t) = i_1(t)\cdot v_c(t) \qquad (3.14)$$

Assuming negligible losses in the rectifier

$$p_1(t) = p_{in}(t) \qquad (3.15)$$

The output current i_1 is related to the load current i_2, through the dc link capacitor C.

$$C.\frac{dv_c}{dt} = i_1 - i_2 \qquad (3.16)$$

Multiplying (3.16) by v_c, and using eqs.(3.14) and (3.15)

$$v_c \cdot C \cdot \frac{dv_c}{dt} = p_{in}(t) - P_2 \qquad (3.17)$$

where P_2 is the dc load power. Substituting eq.(3.13) into eq.(3.17)

$$C \cdot v_c \cdot \frac{dv_c}{dt} = v_{moda} \cdot i_a + v_{modb} \cdot i_b + v_{modc} \cdot i_c - P_2 \qquad (3.18)$$

There are four ordinary differential equations describing the dynamics of the Indirect Current Controlled Rectifier. Three of these consist of the a, b, and c phases of eq.(3.11). The fourth differential equation is eq.(3.18).

In the case where the 3-phase power supply is without neutral return (as is assumed in this study), the algebraic equation

$$i_a + i_b + i_c = 0 \qquad (3.19)$$

allows the system equations to be reduced from 4th order to 3rd order.

3.5 Stability Analysis.

As eq.(3.18) is nonlinear, the standard technique used is to perturb about the equilibrium point $\underline{X}o$, i. e. apply $\underline{X}=\underline{X}o+\Delta\underline{X}$ to obtain:

$$\frac{d\,\Delta\underline{X}}{dt} = [A] \cdot \Delta\underline{X} \qquad (3.20)$$

If [A] is a constant matrix, then the system is stable if none of its eigenvalues appear on the right-hand-side of the S-plane. The immediate difficulty is that since the phase voltages

$$\underline{e}_{abc} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} = \sqrt{2}\cdot V\cdot \begin{bmatrix} \sin w_s t \\ \sin(w_s t + 120^o) \\ \sin(w_s t + 240^o) \end{bmatrix} \tag{3.21}$$

are time dependent, the equilibrium operating point $\underline{X}o$ is also time dependent and so is [A] in eq.(3.20).

This problem is overcome by using the Park-Blondel power invariant transformation [70,71]:

$$\underline{v}_{odq} = [B]\cdot\underline{v}_{abc} \tag{3.22}$$

$$\underline{i}_{odq} = [B]\cdot\underline{i}_{abc} \tag{3.23}$$

where

$$[B] = \sqrt{\frac{2}{3}} \begin{bmatrix} \sqrt{2}/2 & \sqrt{2}/2 & \sqrt{2}/2 \\ \cos w_s t & \cos(w_s t - 120^o) & \cos(w_s t - 240^o) \\ -\sin w_s t & -\sin(w_s t - 120^o) & -\sin(w_s t - 240^o) \end{bmatrix} \tag{3.24}$$

Applying this transformation to the a, b, and c phases of eq.(3.11) and assuming no neutral connection so that the zero-sequence does not exist, one obtains:

$$L\frac{di_d}{dt} + R\cdot i_d - w_s\cdot L\cdot i_q = \sqrt{3}\cdot Xc\cdot I \tag{3.25}$$

$$L\frac{di_q}{dt} + R\cdot i_q + w_s\cdot L\cdot i_d = -\sqrt{3}\cdot Rc\cdot I \tag{3.26}$$

On the other hand, eq.(3.18) becomes:

$$C\cdot v_c\cdot\frac{dv_c}{dt} = -\sqrt{3}\cdot((V - Rc\cdot I)\cdot i_q + Xc\cdot I\cdot i_d) - P_2 \tag{3.27}$$

3.5.1 Equilibrium Operating Point.

From eqs.(3.25) and (3.26) the steady state solutions are:

$$I_d = \sqrt{3}\cdot Io\cdot\frac{(R\cdot Xc - X\cdot Rc)}{R^2 + X^2} \qquad (3.28)$$

$$I_q = -\sqrt{3}\cdot Io\cdot\frac{(R\cdot Rc + X\cdot Xc)}{R^2 + X^2} \qquad (3.29)$$

Io represents the steady-state current command, generated by the error signal in the control block. The real rectifier steady-state current I_{ss}, is given by:

$$I_{ss} = \frac{1}{\sqrt{3}}\cdot\sqrt{I_d^2 + I_q^2} \qquad (3.30)$$

Replacing eqs.(3.28) and (3.29) into eq.(3.30)

$$I_{ss} = Io\cdot\sqrt{\frac{Rc^2 + Xc^2}{R^2 + X^2}} \qquad (3.31)$$

The current command and the real current become equal (I_{ss}=Io) when R=Rc and X=Xc. The input power factor may not be unitary if this condition is not satisfied. In general:

$$\cos\phi = \frac{R\cdot Rc + X\cdot Xc}{\{(R^2+X^2)\cdot(Rc^2+Xc^2)\}^{\frac{1}{2}}} \qquad (3.32)$$

The current rectifier I_{ss} is obtained from the Steady-State Power Balance:

$$P_2 = 3\cdot(V\cdot I_{ss}\cdot\cos\phi - R\cdot I_{ss}^2) \qquad (3.33)$$

3.5.2 Boundaries of Stability.

Let us assume simple proportional control to get the boundaries of stability and let us also assume that R=Rc and X=Xc. With proportional control gain of constant Kp, the current command will be:

$$I = Kp \cdot (V_{REF} - v_c) \tag{3.34}$$

Defining the vector of perturbations as

$$\Delta X = \begin{pmatrix} \Delta v_c \\ \Delta i_d \\ \Delta i_q \end{pmatrix} = \begin{pmatrix} v_c - Vc \\ i_d - I_d \\ i_q - I_q \end{pmatrix} \tag{3.35}$$

knowing from eq.(3.34) that

$$\Delta I = - Kp \cdot \Delta Vc \tag{3.36}$$

and applying small perturbation linearization on eqs.(3.25) to (3.27), one obtains:

$$L \frac{d}{dt}\Delta i_d + R \cdot \Delta i_d - X \cdot \Delta i_q = - \sqrt{3} \cdot X \cdot Kp \cdot \Delta v_c \tag{3.37}$$

$$L \frac{d}{dt}\Delta i_q + R \cdot \Delta i_q + X \cdot \Delta i_d = \sqrt{3} \cdot R \cdot Kp \cdot \Delta v_c \tag{3.38}$$

$$Vc \cdot C \cdot \frac{d}{dt}\Delta v_c = - \sqrt{3} \cdot Io \cdot X \cdot \Delta i_d - \sqrt{3} \cdot (V - R \cdot Io) \cdot \Delta i_q + 3 \cdot Kp \cdot Io \cdot R \cdot \Delta v_c \tag{3.39}$$

The characteristic [A]-matrix of eq.(3.20) is then obtained

$$[A] = \begin{bmatrix} \frac{3 \cdot Kp \cdot Io \cdot R}{C \cdot Vc} & \frac{-\sqrt{3} \cdot Io \cdot X}{C \cdot Vc} & \frac{-\sqrt{3} \cdot (V - R \cdot Io)}{C \cdot Vc} \\ \frac{-\sqrt{3} \cdot Kp \cdot X}{L} & \frac{-R}{L} & w_S \\ \frac{\sqrt{3} \cdot Kp \cdot R}{L} & -w_S & \frac{-R}{L} \end{bmatrix} \qquad (3.40)$$

The eigenvalues of the [A]-matrix are evaluated numerically by the IMSL subroutine [72]. Figure 3.6 shows the stability boundaries obtained for a rectifier with Kp=3 A/V, Vc=120 Vdc, V=40 Vac and L=.005 H. The Direct Current Control has superior stability characteristics as shown in Figure 3.6.

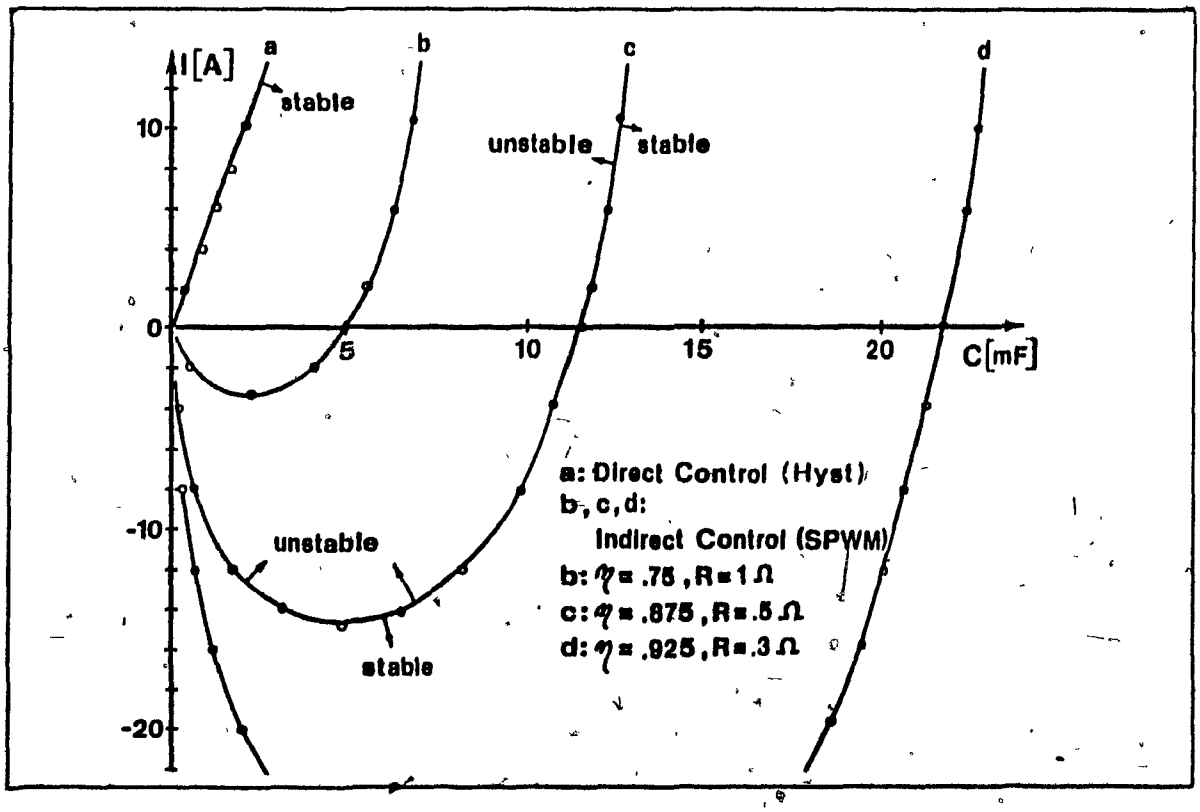


Fig.3.6 Stability Boundaries of Direct and Indirect Control with R as a Parameter. Input Current vs DC Link Capacitor.

It can be seen that the stability region decreases as the ac phase resistance R is reduced. There is good reason to believe that this is related to the increased time constant T=L/R in the circuit. The Direct Control, on the other hand, has a stability region which is independent of R.

3.5.2.1 Verification of Stability Theory.

The stability boundaries predicted from eigenvalue analysis are shown in Figure 3.6. These predictions have been verified using the Valve-by-Valve Simulations which will be described in section 3.6 and analyzed in Appendix A. The circled points of Figure 3.6 are the points at the margin of stability based on the Valve-by-Valve simulations.

3.5.3 Dynamic Compensation.

The poor stability region for small values of R, as shown in Figure 3.6, is a serious issue, unless a solution, other than connecting big dc capacitors, is found. As the problem seems to be caused by the dc component of the input current, one should be able to reanalyze the problem starting from the desired solution of eq.(3.11):

$$L \frac{d}{dt} i_a + R \cdot i_a = e_a(t) - v_{moda}(t) \qquad (3.41)$$

The desired solution is

$$i_a(t) = I(t) \cdot 2 \cdot \sin(w_s t + \phi) \qquad (3.42)$$

In contrast to eq.(3.12), there should be no dc offset term in this solution. Replacing eq.(3.42) into (3.41), one gets the desired time function $v_{moda}(t)$:

$$v_{moda}(t) = \sqrt{2}\cdot(V + X\cdot I\cdot\sin\phi - (R\cdot I + L\cdot\frac{dI}{dt})\cdot\cos\phi)\cdot\sin w_s t -$$

$$-\sqrt{2}\cdot(X\cdot I\cdot\cos\phi + (R\cdot I + L\cdot\frac{dI}{dt})\cdot\sin\phi)\cdot\cos w_s t \qquad (3.43)$$

and for unity power factor:

$$v_{moda}(t) = \sqrt{2}\cdot((V - R\cdot I - L\cdot\frac{dI}{dt})\cdot\sin w_s t - X\cdot I\cdot\cos w_s t) \qquad (3.44)$$

Comparing eq.(3.44) term for term with eq.(3.10), it is clear that they cannot be identical even with Rc=R and Xc=X, because there is a missing L·dI/dt term which was not considered in the first equation. Let us then analyze a system with L·dI/dt in the control block as shown in Figure 3.7.

To allow for generalization, the representative inductance of this new block will be called L_b. The time function $v_{moda}(t)$ then generated by the control block will be:

(3.45)

$$v_{moda}(t) = \sqrt{2}\cdot((V - Rc\cdot I - L_b\cdot\frac{dI}{dt})\cdot\sin w_s t - Xc\cdot I\cdot\cos w_s t)$$

Using eq.(3.45) instead of eq.(3.10) for the a, b, and c phases to obtain the d-q frame equations, one gets:

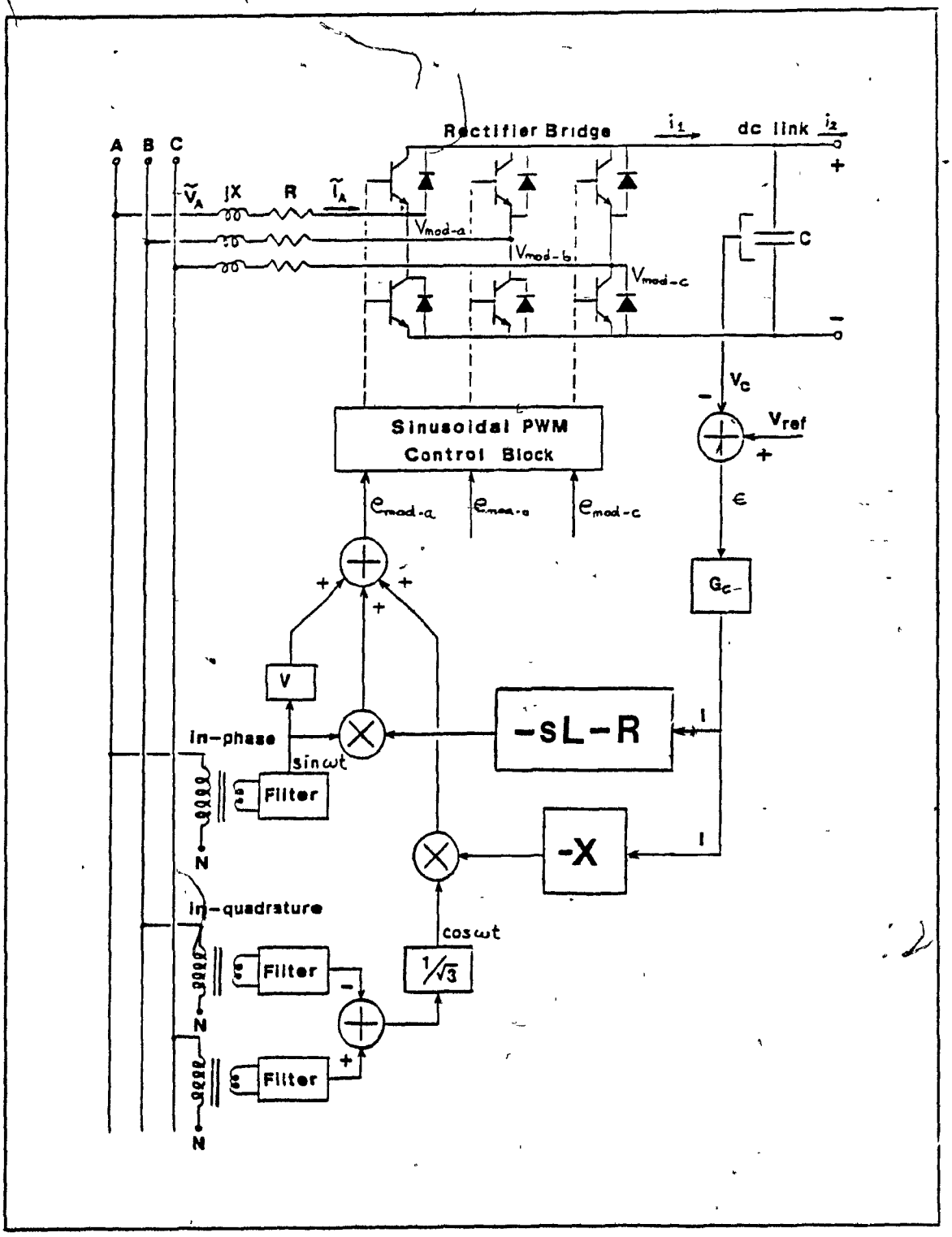


Fig.3.7 Dynamic Compensation with L·dI/dt Block. Cos ø = 1

$$L \cdot \frac{di_d}{dt} + R \cdot i_d - w \cdot L \cdot i_q = \sqrt{3} \cdot Xc \cdot I \qquad (3.46)$$

$$L \cdot \frac{di_q}{dt} + R \cdot i_q + w \cdot L \cdot i_d = -\sqrt{3} \cdot (Rc \cdot I + L_b \cdot \frac{dI}{dt}) \qquad (3.47)$$

$$C \cdot v_c \cdot \frac{dv_c}{dt} = -\sqrt{3} \cdot (V - Rc \cdot I - L_b \cdot \frac{dI}{dt}) \cdot i_q + Xc \cdot I \cdot i_d - P_2 \qquad (3.48)$$

This new set of equations gives the same equilibrium operating points for I_d, I_q and cos ø as eqs.(3.28), (3.29) and (3.32), as should be expected.

Applying small perturbation linearization on eqs.(3.46) to (3.48), and subsequently taking the Laplace Transform:

$$L \cdot S \cdot \Delta i_d(S) = -R \cdot \Delta i_d(S) + X \cdot \Delta i_q(S) + \sqrt{3} \cdot Xc \cdot \Delta I(S) \qquad (3.49)$$

$$L \cdot S \cdot \Delta i_q(S) = -R \cdot \Delta i_q(S) - X \cdot \Delta i_d(S) - \sqrt{3} \cdot (Rc + L_b \cdot S) \cdot \Delta I(S) \qquad (3.50)$$

$$Vc \cdot C \cdot S \cdot \Delta Vc(s) = \sqrt{3} \cdot (Rc \cdot I_q - Xc \cdot I_d + L_b \cdot I_q \cdot S) \cdot \Delta I(S) - $$

$$- \sqrt{3} \cdot Xc \cdot Io \cdot \Delta i_d(S) - \sqrt{3} \cdot (V - Rc \cdot Io) \Delta i_q(S) \qquad (3.51)$$

From eqs.(3.49) to (3.51), the open loop transfer function of the system, $G_s(S)$, is found

$$G_s(S) = \frac{\Delta Vc(S)}{\Delta I(S)} = Ko \cdot \frac{a_3 \cdot S^3 + a_2 \cdot S^2 + a_1 \cdot S + a_0}{S \cdot (S^2 + 2 \cdot S \cdot d + d^2 + w_s^2)} \qquad (3.52)$$

where

$$Ko = \frac{\sqrt{3}}{Vc \cdot C} \tag{3.53}$$

$$a_3 = L_b \cdot I_q \tag{3.54}$$

$$a_2 = (Rc + 2 \cdot \frac{L_b}{L} \cdot R) \cdot I_q - Xc \cdot I_d + (V - Rc \cdot Io) \cdot \sqrt{3} \cdot \frac{L_b}{L} \tag{3.55}$$

$$a_1 = 2 \cdot \frac{R}{L} \cdot (Rc \cdot I_q - Xc \cdot I_d) + L_b \cdot I_q \cdot \frac{(R^2+X^2)}{L^2} -$$

$$- \frac{\sqrt{3} \cdot Xc}{L} \cdot (Xc - L_b \cdot w_s) \cdot Io + \sqrt{3} \cdot \frac{(V - R \cdot Io)}{L} \cdot (Rc + \frac{L_b}{L} \cdot R) \tag{3.56}$$

$$a_0 = \sqrt{3} \cdot V \cdot \frac{(R \cdot Rc + X \cdot Xc)}{L^2} -$$

$$- \frac{2 \cdot \sqrt{3} \cdot Io}{L^2} \cdot ((R \cdot Rc + X \cdot Xc) \cdot Rc + (R \cdot Xc - X \cdot Rc) \cdot Xc) \tag{3.57}$$

and

$$d = \frac{R}{L} \tag{3.58}$$

Let us analyze the case where Rc=R, Xc=X and L_b=L. In such a situation eqs.(3.28) and (3.29) become

$$I_d = 0 \tag{3.59}$$

$$I_q = -\sqrt{3} \cdot Io \tag{3.60}$$

Replacing the values of I_d and I_q into the coefficients a_3 to a_0 results in

$$a_3 = -\sqrt{3} \cdot Io \cdot L \tag{3.61}$$

$$a_2 = \sqrt{3} \cdot (V - 4 \cdot R \cdot Io) \tag{3.62}$$

$$a_1 = \sqrt{3} \cdot (2 \cdot V \cdot R - 5 \cdot R^2 \cdot Io - X^2 \cdot Io)/L \tag{3.63}$$

$$a_0 = \sqrt{3} \cdot (V - 2 \cdot R \cdot Io)(R^2 + X^2)/L^2 \tag{3.64}$$

Replacing these new coefficients into $G_s(S)$ of eq.(3.52), and manipulating some algebra yields:

$$G_s(S) = \frac{\Delta Vc(S)}{\Delta I(S)} = \frac{3.(V - 2\,R\,Io - L\,Io\,S)}{C \cdot Vc \cdot S} \qquad (3.65)$$

This new transfer function is exactly the same as of the Direct Control Method, $G_1(S) \cdot G_2(S)$, obtained in Chapter II. The addition of the $L \cdot dI/dt$ block, makes the Indirect Current Control Method dynamically equivalent to the Direct method. This means that the stability boundariy is now the same straight line shown in Figure 3.6 a) for each system. Note that this equivalence makes it unnecessary to repeat the analysis already done in Chapter II, concerning P and PI control.

It has been shown that it is possible to make the Indirect Current Control as stable as the Direct method. The question now is to see whether or not the stability region of the Indirect Current Control can be improved even more by changing the value of L_b in the control block. Let us go back to the general transfer function represented by eq.(3.52) and analyze it using the Nyquist Criterion. Through the Nyquist plot it will be possible to see how the changes in L_b can affect the stability region.

3.5.4 Nyquist Criterion.

Adding the controller to the system, which in general is of the form:

$$G_C(S) = S \cdot K_D + Kp + \frac{K_I}{S} \tag{3.66}$$

where

K_D : Derivative control gain

Kp : Proportional control gain

K_I : Integral control gain

yields

$$G(S) = G_s(S) \cdot G_C(S) =$$

$$= Ko \cdot \frac{A_5 \cdot S^5 + A_4 \cdot S^4 + A_3 \cdot S^3 + A_2 \cdot S^2 + A_1 \cdot S + A_0}{S^2 \cdot (S^2 + 2 \cdot S \cdot d + d^2 + w_s^2)} \tag{3.67}$$

where

$$A_5 = a_3 \cdot K_D \tag{3.68}$$

$$A_4 = a_3 \cdot Kp + a_2 \cdot K_D \tag{3.69}$$

$$A_3 = a_3 \cdot K_I + a_2 \cdot Kp + a_1 \cdot K_D \tag{3.70}$$

$$A_2 = a_2 \cdot K_I + a_1 \cdot Kp + a_0 \cdot K_D \tag{3.71}$$

$$A_1 = a_1 \cdot K_I + a_0 \cdot Kp \tag{3.72}$$

$$A_0 = a_0 \cdot K_I \tag{3.73}$$

Making S=jw to plot the Nyquist diagrams, eq.(3.67) becomes:

(3.74)

$$G(jw) = Ko \cdot \frac{A_4 \cdot w^4 - A_2 \cdot w^2 + A_0 + j \cdot (A_5 w^5 - A_3 \cdot w^3 + A_1 \cdot w)}{w^2 \cdot (\beta^2 - 2 \cdot jw \cdot d)}$$

where $\beta^2 = w^2 - w_s^2 - d^2$ (3.75)

The real and imaginary part of G(jw) are obtained from eq.(3.74)

$$Re[G(jw)] = Ko.\frac{R(w)\cdot\beta 2 - 2\cdot I(w)\cdot w\cdot d}{w^2\cdot(\beta^4 + 4\cdot w^2\cdot d^2)} \qquad (3.76)$$

$$Im[G(jw)] = Ko.\frac{2\cdot R(w)\cdot w\cdot d + I(w)\cdot\beta^2}{w^2\cdot(\beta^4 + 4\cdot w^2\cdot d^2)} \qquad (3.77)$$

where

$$R(w) = A_4\cdot w^4 - A_2\cdot w^2 + A_0 \qquad (3.78)$$

$$I(w) = A_5\cdot w^5 - A_3\cdot w^3 + A_1\cdot w \qquad (3.79)$$

With a small computer program, eqs.(3.76) and (3.77) can be solved graphically for different values of L_b, as shown in figures 3.8 to 3.11.

The simulations assume a rectifier with the following values: V=220 Vac, Vc=660 Vdc, Kp=3 A/V, K_I=K_D=0, R=Rc=.1 Ohm, L=Lc=.001 H and C=2000 uF. The Figure 3.8 a) shows a rectifier without the L·dI/dt block (L_b=0). It begins to be stable with currents more negative than -340 A ac, and hence, can only work in the inverter region. Such a system has no practical application. To make this rectifier able to operate with a stable region close to +100 A ac, a 14000 uF capacitor would be required, as shown in the Nyquist plot of Figure 3.8 b).

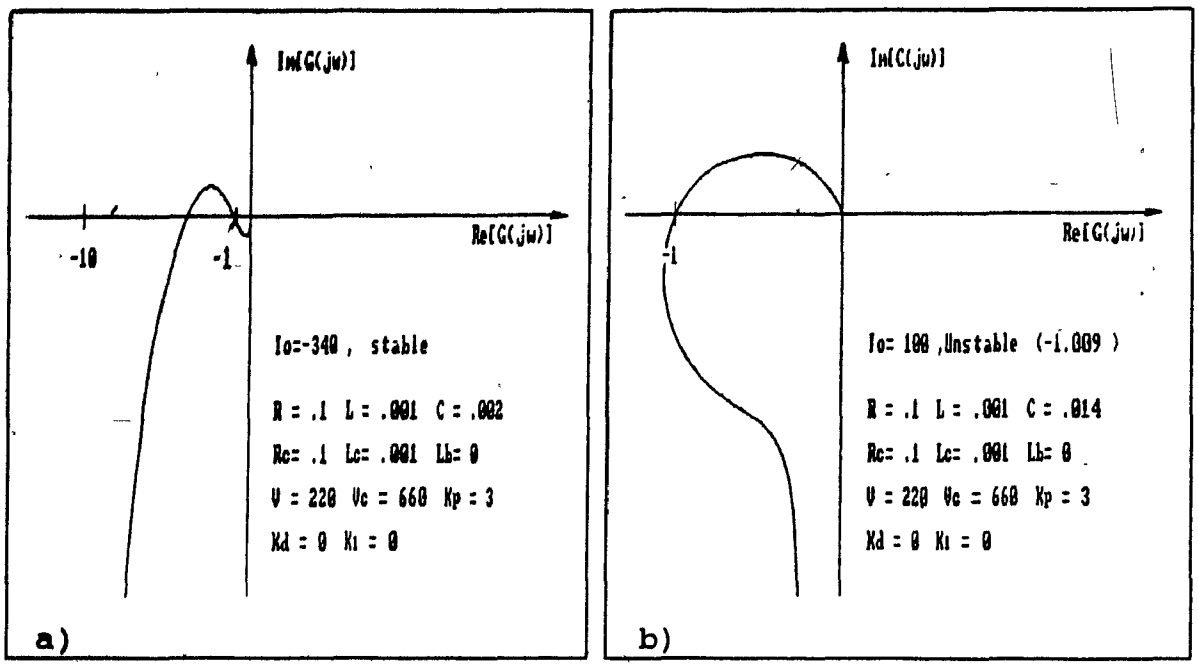


Fig. 3.8 Nyquist Plot without L·dI/dt Block (L_b=0).
a) C=2000 uF: stable when I<-340 A.
b) C=14000 uF: stable for I<100 A.

The Figure 3.9 shows the improvement reached when the L·dI/dt block is connected to the system. With the same 2000 uF capacitor of Figure 3.8 a), the rectifier can operate with more than 145 A ac. In this case, L_b is equal to L and the system is equivalent to the Direct Current Control.

When L_b is increased, taking values bigger than L, the stability region begins to deteriorate. A different situation is observed when L_b is reduced. At some point in this case, when L_b is around 50% of L, the rectifier remains stable with as much as 290 A ac as shown in Figure 3.10. This is twice the current that the Direct Control can carry with the same dc capacitor.

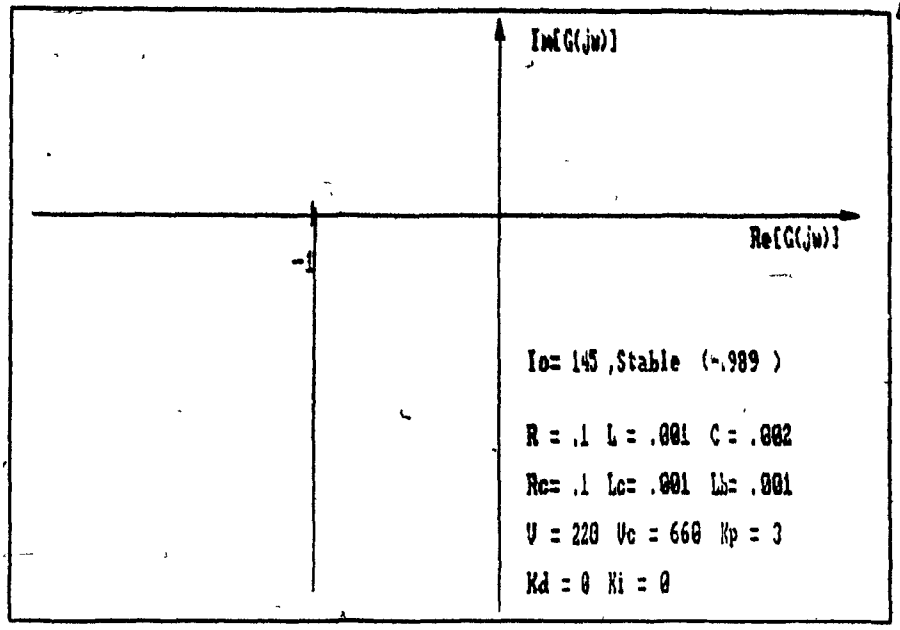


Fig.3.9 Nyquist Plot for L_b=L: the Indirect Control Becomes Equivalent to the Direct Control.

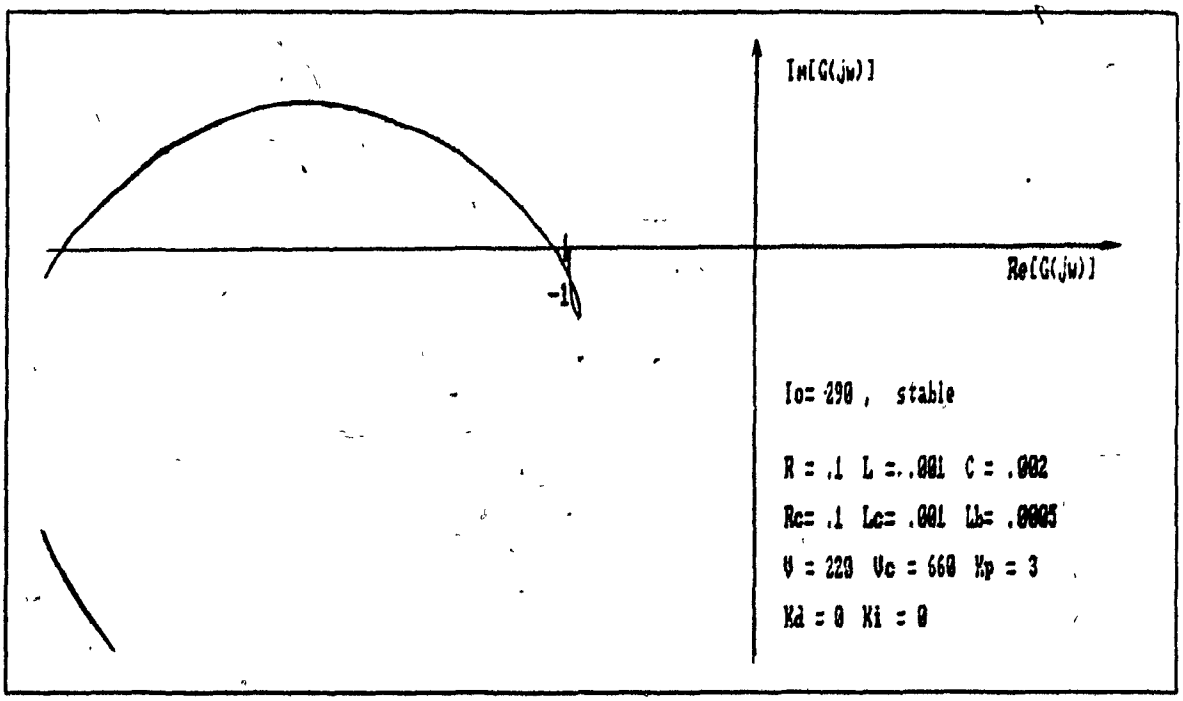


Fig. 3.10 Nyquist Diagram for L_b=0.5·L: the Stability Region Is Twice as Good.

Smaller rectifiers show the same behaviour, as shown in Figure 3.11. The converter, with 4000 uF dc capacitor, can carry up to 12 A, but only when L_b is around 80% of L. Otherwise, it is unstable.

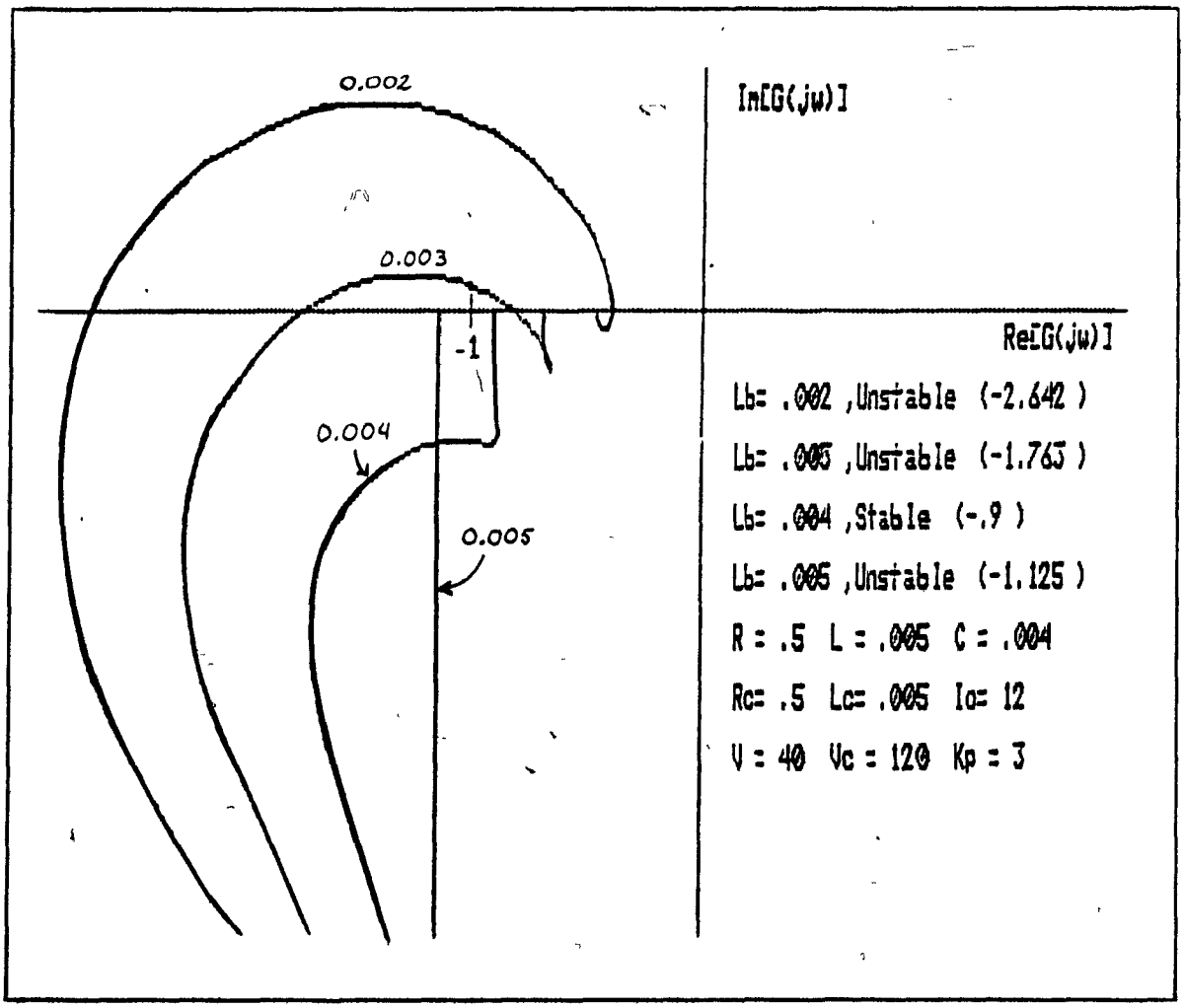


Fig.3.11 Nyquist plots for a small rectifier, showing stability when L_b=0.8·L.

A better idea of what is going on with the stability boundaries of Figure 3.6 when L_b changes is shown in Figure 3.12, where R=0.5 has been chosen arbitrarily. These curves

clearly show that improvements can be reached with $L_b<L$, by paying careful attention to the size of the capacitor and the rating current of the rectifier.

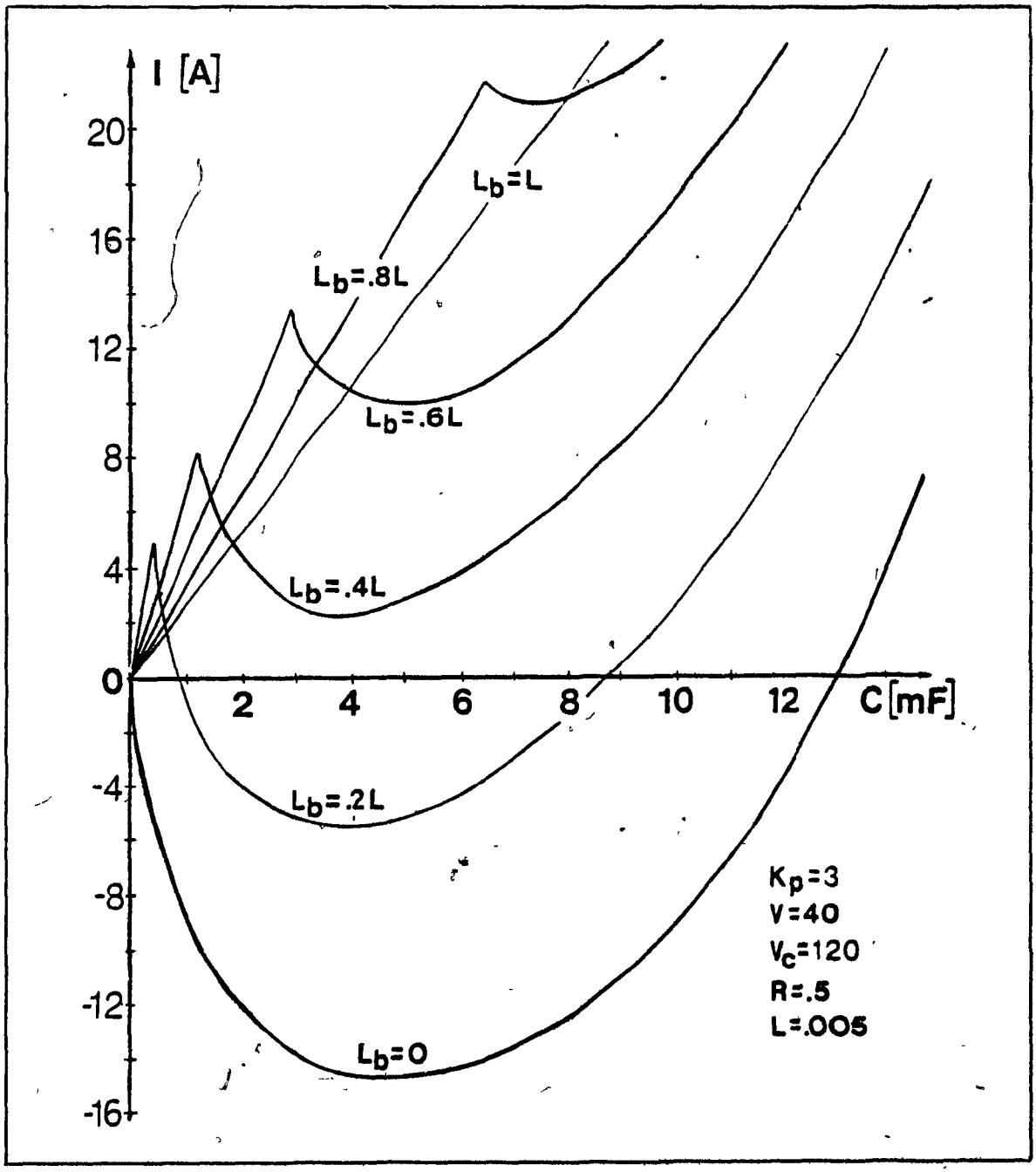


Fig.3.12 Stability Boundaries with L_b as a Parameter. Input Current vs DC Link Capacitor.

With the results shown in Figures 3.8 to 3.12, it appears that the Indirect Current Control can be made more stable than the direct one. Experiments with L_b different from L have not been performed and for this reason no conclusive proof about this has been obtained. Further investigation and research on it will have to be done. Nonetheless, experiments show that L_b=L produces an effective equivalence between the two methods.

3.6 Parameter Sensitivity.

In the Direct Current Control, analyzed in Chapter II, the input current is insensitive to the variations of L and R, because it is measured directly and the hysteresis current control ensures that the power factor remains unaltered.

For the Indirect Control, the situation is different. L and R variations do have effect on the input currents, because Lc and Rc in the control block are kept constant. The question is to see whether or not these variations can produce significant changes in the current.

One important property of the converter is that under steady state conditions, the Power Balance Equation, eq.(3.33)

$$P_2 = 3\cdot(V\cdot I_{ss}\cdot\cos\phi - R\cdot I_{ss}^2) \qquad (3.80)$$

must be satisfied. This important fact points out that the system avoids big variations in the current. As V and P_2 can be assumed constants, "I" can change only through cos ø variations as R is usually small.

In a simple form, for a converter designed for unity power factor operation, variations in the ϕ angle can be expected when the real values R and X are not exactly the same as the control block values Rc and Xc. In such a case, according to eqs.(3.28) and (3.29), the angle ϕ will be

$$\phi = tg^{-1} \frac{R \cdot Xc - X \cdot Rc}{R \cdot Rc + X \cdot Xc} \qquad (3.81)$$

which is equal to 0^o when R=Rc and X=Xc. In the particular case R=Rc=0, ϕ is also equal to 0^o and the current will be constant no matter the size of X or the value of Xc assigned in the control block.

Let now assume that X changes and R=Rc>0. This means that $X=\lambda \cdot Xc$. Keeping R=Rc eq.(3.81) becomes

$$\phi = tg^{-1} \frac{(1-\lambda) \cdot \frac{Xc}{Rc}}{1 + \lambda \cdot \frac{Xc^2}{Rc^2}} \qquad (3.82)$$

Eq.(3.82) shows that the ϕ variations will depend on the ratio Xc/Rc. The bigger this ratio is, the smaller the variation of the angle ϕ. Note that $|(1-\lambda)|$ is likely to be less than 0.1 since variations of Xc from X is due to component tolerance deviation.

Let us develop an example in which the reactance decreases. The system initially has the following values in per unit: V=1 [pu], $P_2/3$=1 [pu], R=0.05 [pu] and X=0.25 [pu]. Rc and Xc had previously been adjusted at Rc=R and Xc=X. The

system was then operating at unity power factor and the current is obtained from eq.(3.80)

$$I_{sso} = \frac{1 - \sqrt{1 - 0.2}}{0.1} = 1.056 \text{ [pu]}$$

Let us now assume that X decreases by 50%. The angle ø will be

$$\phi = tg^{-1} \frac{R \cdot Xc - X \cdot Rc}{R \cdot Rc + X \cdot Xc} = tg^{-1}(0.185) = 10.49^{\circ}$$

and

$$\cos \phi = 0.983$$

From eq.(3.80) the new current will be

$$I_{ss} = \frac{0.983 - \sqrt{(0.983)^2 - 0.2}}{0.1} = 1.073 \text{ [pu]}$$

Comparing the magnitudes I_{ss}/I_{sso} it can be concluded that a 50% decrease in the value of the reactance X results in an increase of the current magnitude of only 1.6%. Similar results have been obtained for an increase in the reactance or variations in the input resistance R.

The R and X variations in a real system can be assumed to be a lot smaller than 50%, in fact of the order of 5 or 10%. Hence, the variations in the current magnitude cannot be expected to be bigger than 1%. On the other hand the angle variations should not be greater than 5 degrees. In accordance with these results and from a practical point of view, it can be concluded than the Indirect Current Control is insensitive to the parameter deviation.

3.7 Simulations and Experimental Results.

Experimental work has been pursued together with digital simulation studies. The very close agreement of experiment and theory prove the mathematical models of Section 3.4 to be correct.

Mathematical and Valve-by-Valve simulations have been realized. The Mathematical Simulations consist of numerically integrating eqs.(3.25) to (3.27). These equations neglect the ripple harmonics and only embody the fundamental Fourier component. The Valve-by-Valve Digital Simulation Program is based on treating the rectifier bridge as a piece-wise circuit problem. The ON-OFF states of each of the six power switches give rise to eight possible circuit topologies, which are discussed in Appendix A. The instants of switching of the transistors are monitored by keeping track of the intersections of the triangular carrier and the modulating signal of each phase. Thus a time sequence of eight circuit topologies is generated. The differential equations arising from the Kirchhoff Voltage and Current Laws for the topologies are solved numerically and are joined together by the requirements that the flux linkages of inductances and electric charges across capacitors must be continuous.

3.7.1 Unity power factor.

Figure 3.13 shows the operation of the rectifier under steady-state at unity power factor. It can be seen that the

input current of the rectifier "I" is in phase with the supply voltage V. The delay angle θ of the modulating signal V_{mod}, with respect to V is also visible. For the valve-by-valve simulation of Figure 3.13, the same triangular carrier frequency has been considered. The frequency of the carrier is 1600 Hz. The dc load current i_2 is 6 A and the dc voltage was adjusted to 120 V. The ac supply voltage V=40 V. The values of X and R are 2.5 and 1 Ohm respectively.

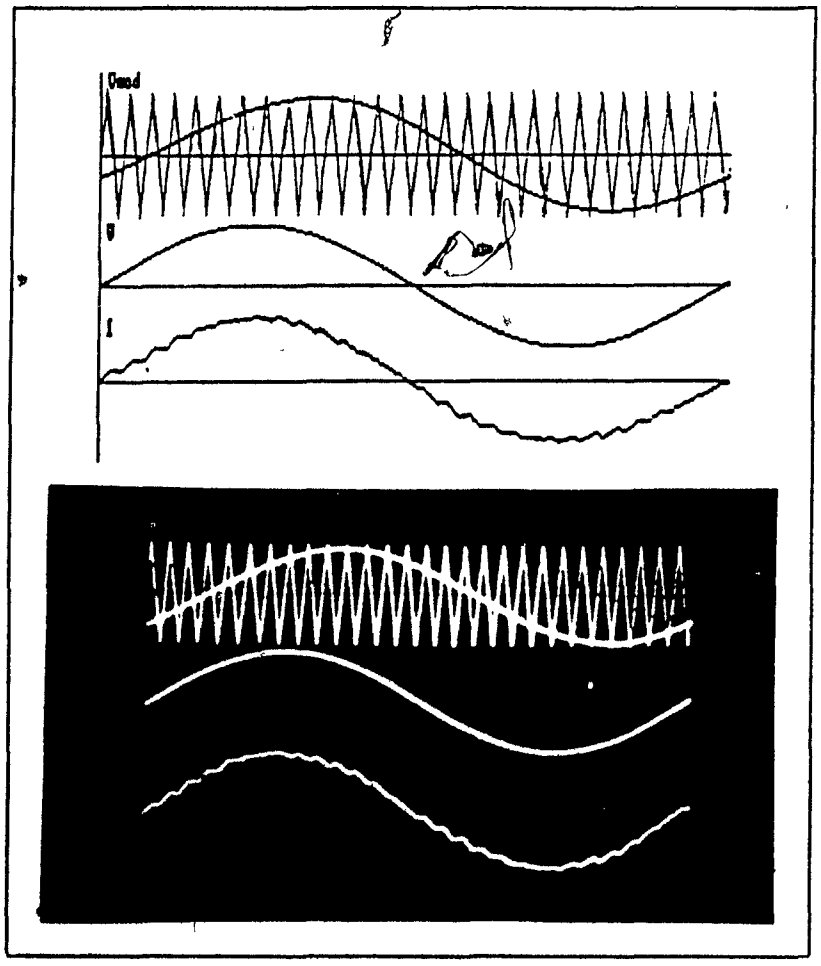


Fig.3.13 Steady-State at Unity Power Factor Operation. Valve-by-Valve and Experimental Oscillograms.
a) modulating signal and triangular carrier.
b) supply voltage V.
c) rectifier input current I.

The system behaves very well under transient conditions. Figure 3.14 shows the experimental oscillogram of the rectifier response when the filtered dc current i_2, changes instantaneously from 0 to 7 A dc. It can be seen that the magnitude and phase of the modulating signal V_{mod} changes to satisfy the unity power factor requirement. The parameters are the same as in Figure 3.13.

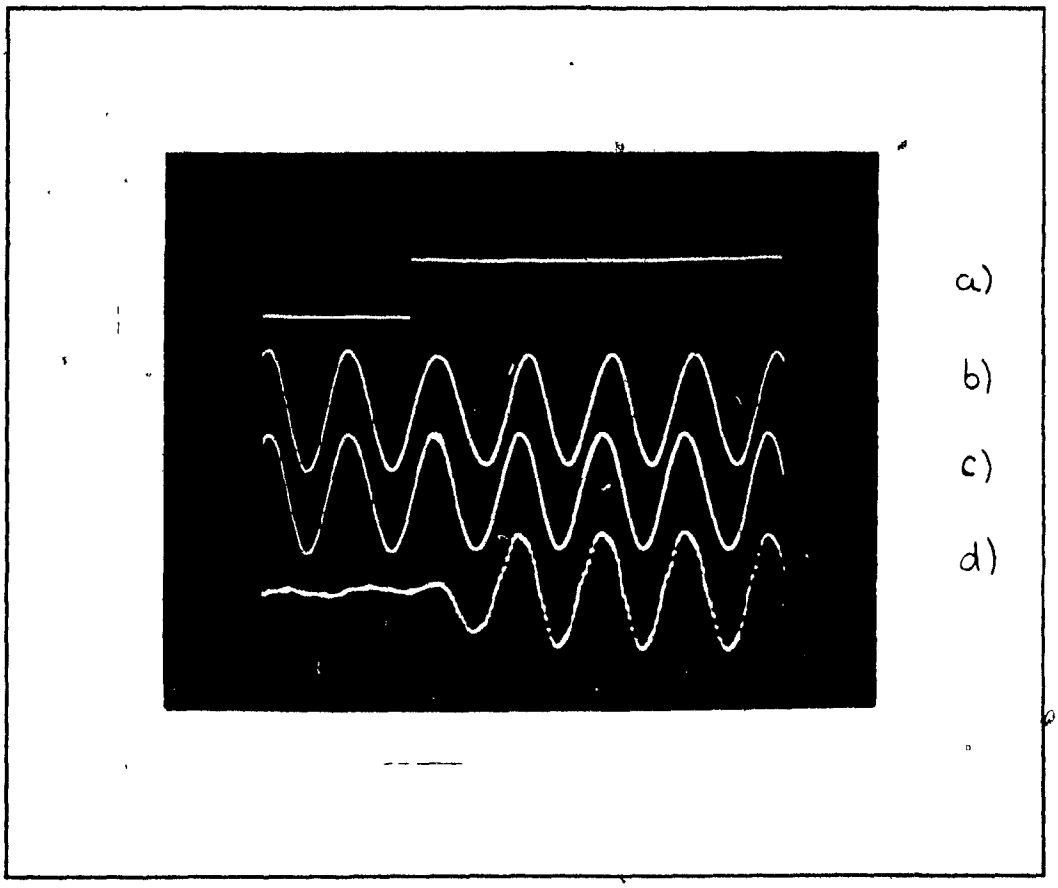


Fig.3.14 Step Response. Experimental Oscillogram.
a) output dc current i_2, from 0 to 7 A dc
b) modulating signal V_{mod}
c) supply voltage V
d) Input current I

A more critical transient situation is the reversal of power from either, rectifier to inverter or inverter to rectifier operation. The simulation of Figure 3.15 and the experimental oscillogram of Figure 3.16 show the results obtained when power is reversed from inverter to rectifier. Here the filtered dc current i_2 is forced to change from -7 to +5 A dc. In these oscillograms, the change in magnitude and phase of the modulating signal V_{mod} is much clearer.

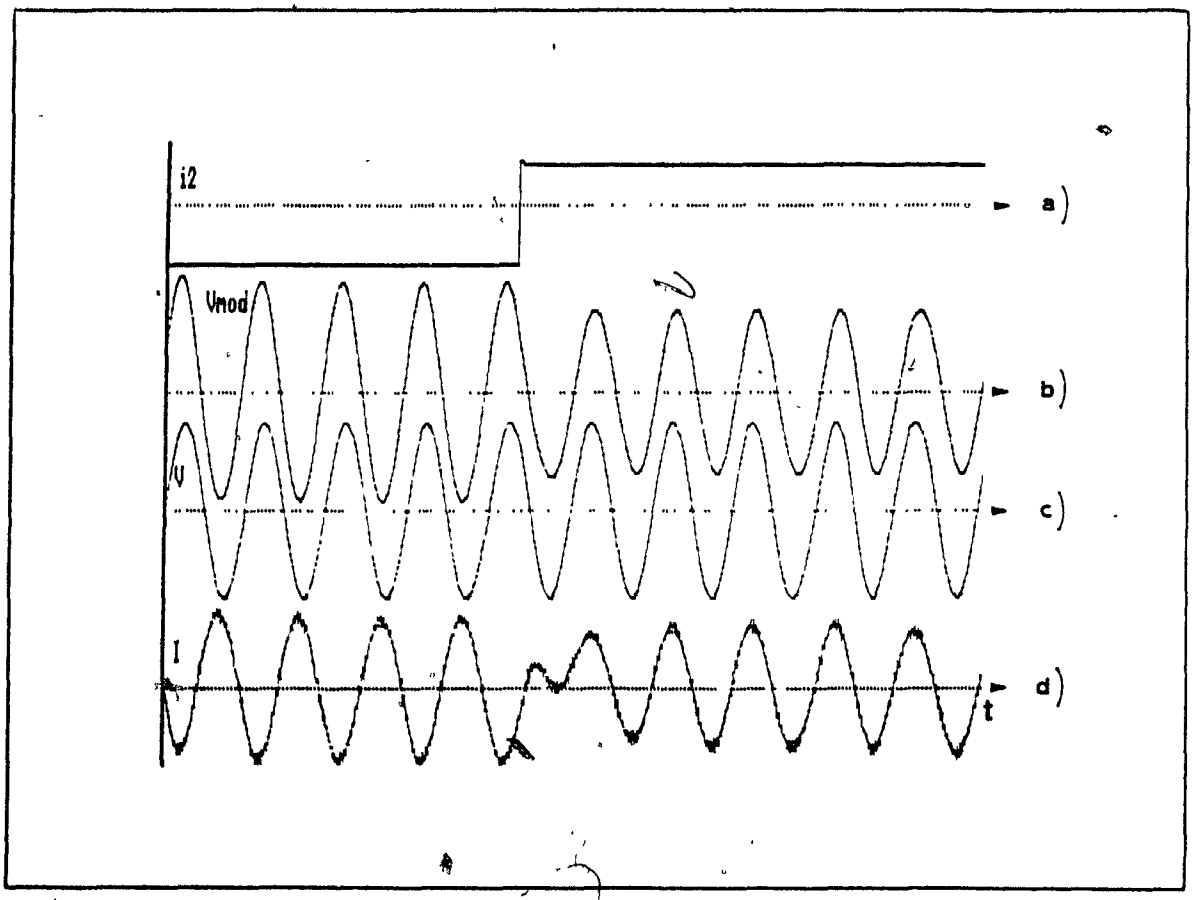


Fig.3.15 Reversal of Power, Valve-by-Valve Simulation.
a) load current i_2, from -7 to 5 A dc
b) modulating signal V_{mod}
c) supply voltage V
d) input current I

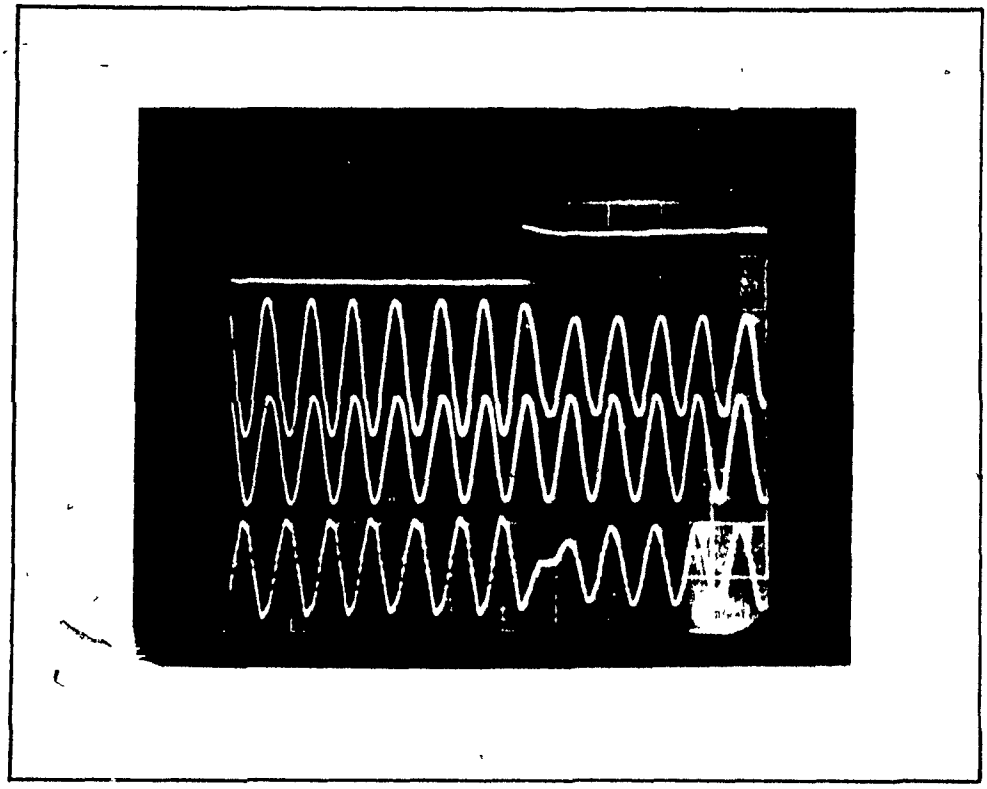


Fig.3.16 Experimental Oscillogram of Figure 3.15.
a) load current i_2, from -7 to 5 A dc
b) modulating signal V_{mod}
c) supply voltage V
d) input current I

3.7.2 Stability.

The problem of stability has been analyzed considering the system with and without compensation. As was mentioned previously, only the cases of L_b=0 and L_b=L have been implemented in the laboratory model. The experiments were performed with Vc=120 V, V=40 V, Kp=3, K_I=0, R=1 ohm and X=2.5 ohms. The value of the dc capacitor C, is indicated for each case. The experiments were also realized with PI control.

The following pages show the results obtained for a step response without LdI/dt (L_b=0) and with LdI/dt (L_b=L).

Figure 3.17 is a valve-by-valve simulation without L·dI/dt block. Figure 3.18 is the experimental result for the same conditions shown in Figure 3.17, with C=12000 uF.

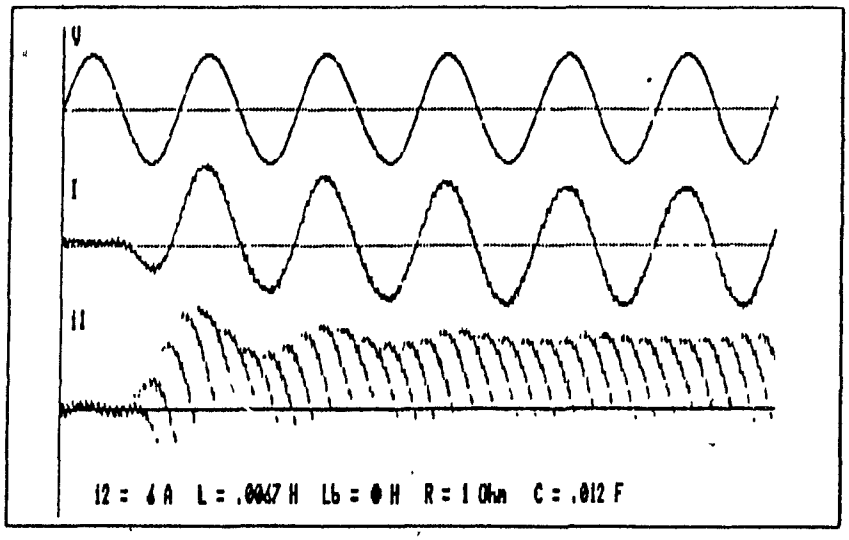


Fig.3.17 Valve-by-Valve Simulation for a Step Response. No L·dI/dt. Current i_2 from 0 to 6 A dc.

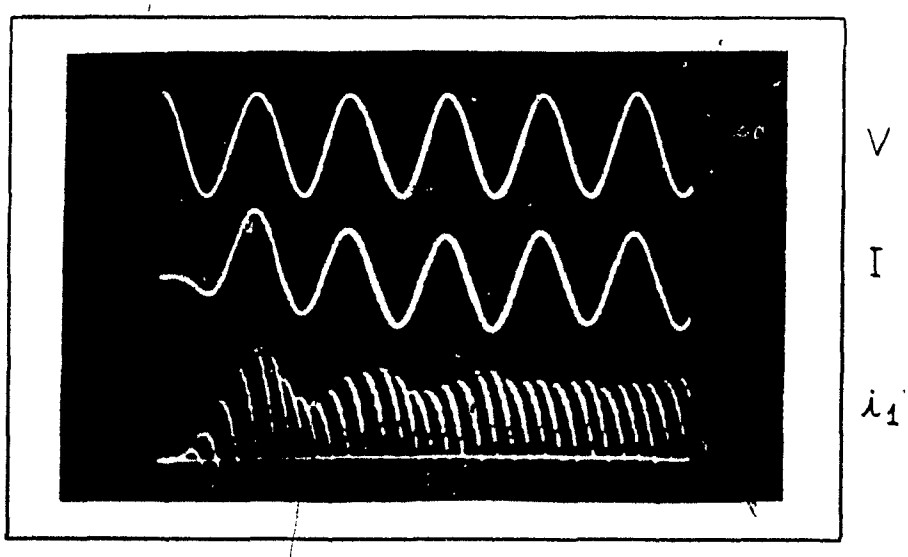


Fig.3.18 Experimental Oscillogram for the same conditions.

The improvement obtained when the LdI/dt block is used can be seen in Figures 3.19 and 3.20. The first shows the simulation and the second the experiment, using C=12000 uF.

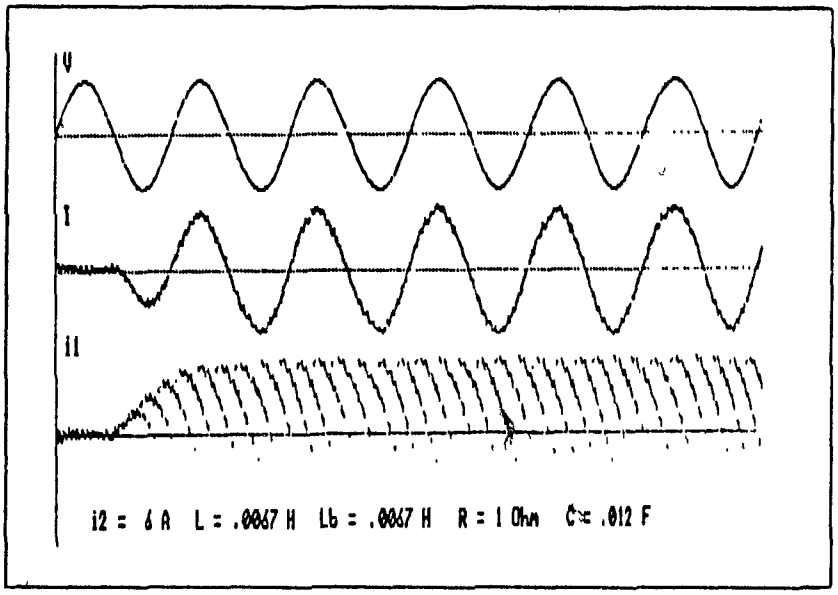


Fig.3.19 Simulation for a Step Response with L·dI/dt.
Current i_2 from 0 to 6 A dc.

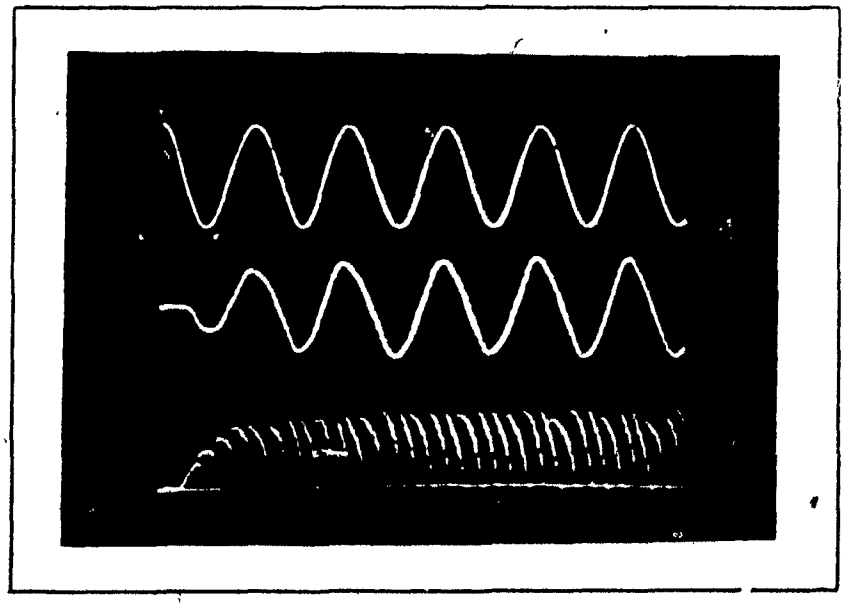


Fig.3.20 Experimental Oscillogram for the Same Conditions.

In the compensated oscillograms of Figures 3.19 and 3.20 (L_b=L), it can be seen that both the dc component in the input current and the ac component in the output current shown in Figures 3.17 and 3.18 have disappeared.

As the control of the rectifier is in V_{mod}, it is interesting to see how it behaves during the transients in both cases, L_b=0 and L_b=L. Figure 3.21 shows that V_{mod} changes slowly during the transient when L_b=0, and is unable to avoid the appearance of the unwanted components during the step

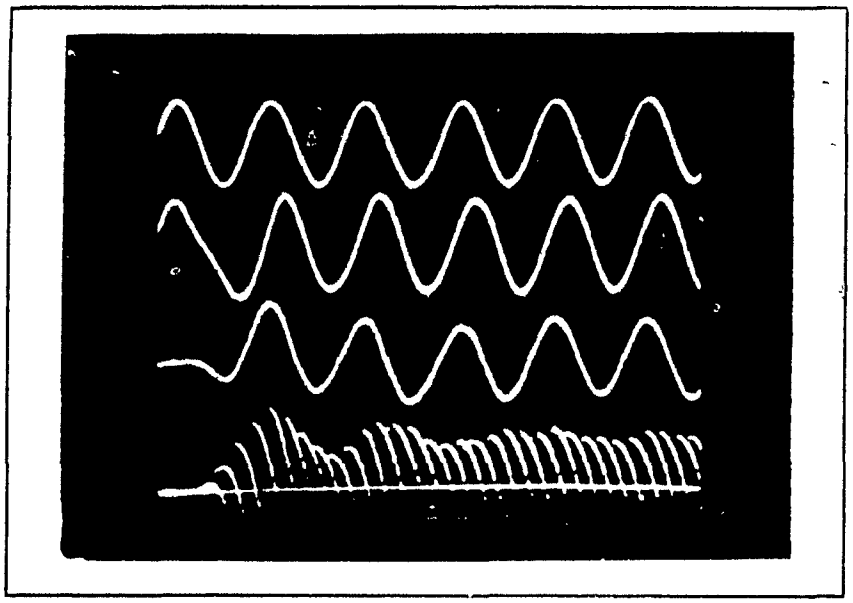


Fig.3.21 V_{mod} Behaviour during the Transient Without LdI/dt.
a) supply voltage V
b) modulating signal V_{mod}
c) input current I
d) output current i_1

In contrast, when L_b=L, the derivative action of the LdI/dt block produces a fast change on V_{mod}, eliminating the undesirable components. This is shown in Figure 3.22.

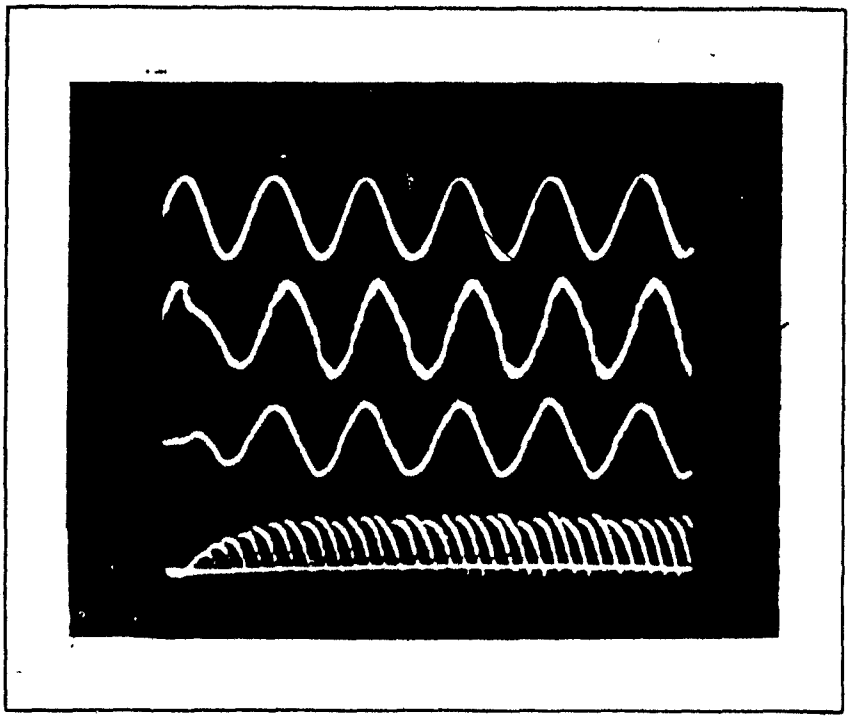


Fig.3.22 V_{mod} Behaviour during the Transient with L·dI/dt.
a) supply voltage V
b) modulating signal V_{mod}
c) input current I
d) output dc current i_1

Mathematical simulations, derived from the theoretical analysis of the indirect control, show the same behaviour as can be seen in Figure 3.23.

A more critical experiment, the reversal of power, is shown in Figures 3.24 and 3.25 with L_b=0 and L_b=L respectively. The parameters are all the same as in Figures 3.19 and 3.20. The dc current i_2 changes from -5 to +5 A dc. Mathematical simulations for these two figures are shown in Figure 3.26.

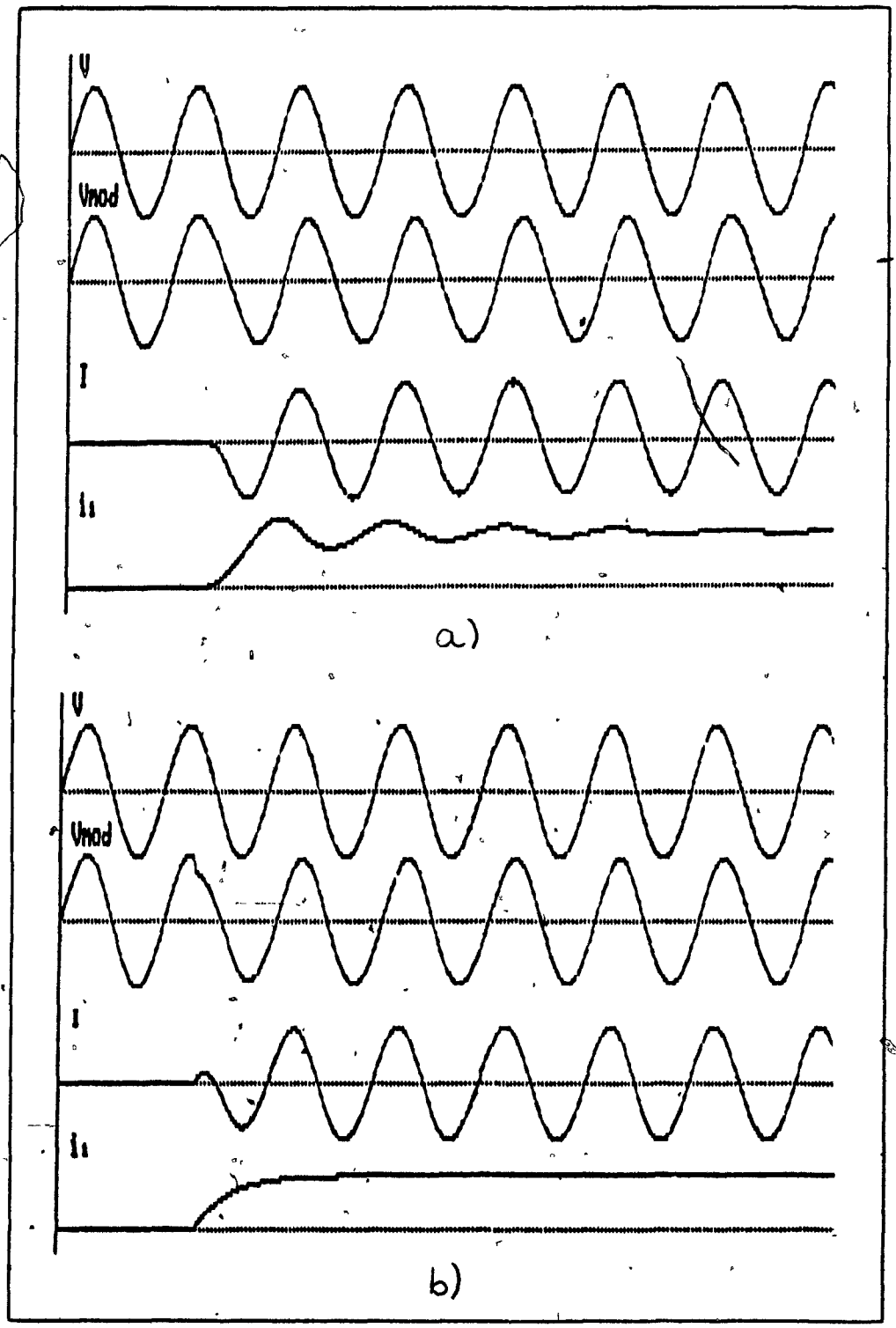


Fig.3.23 Mathematical Simulation of Figures 3.21 and 3.22.
a) no LdI/dt block
b) LdI/dt block

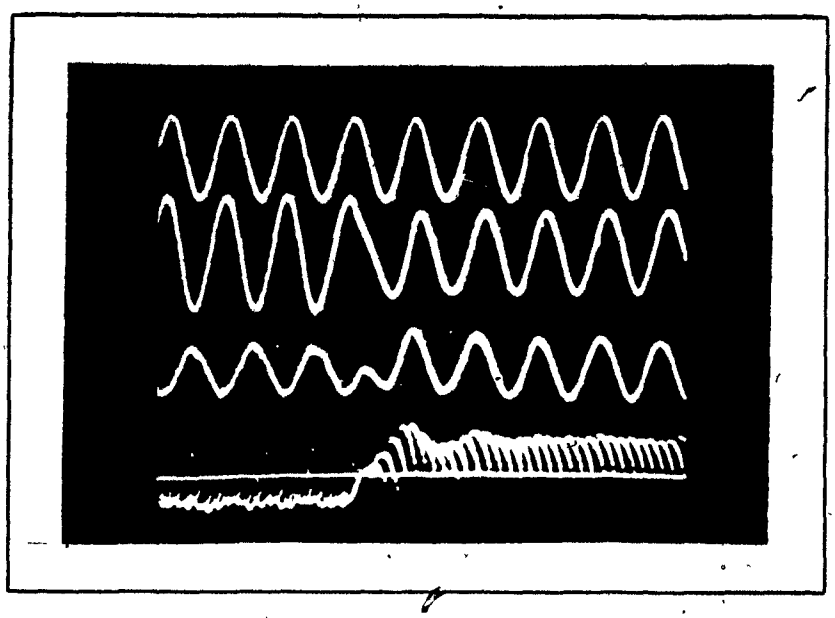


Fig.3.24 Reversal of Power without LdI/dt Block.
a) supply voltage V
b) modulating signal V_{mod}
c) input current I
d) output current i_1

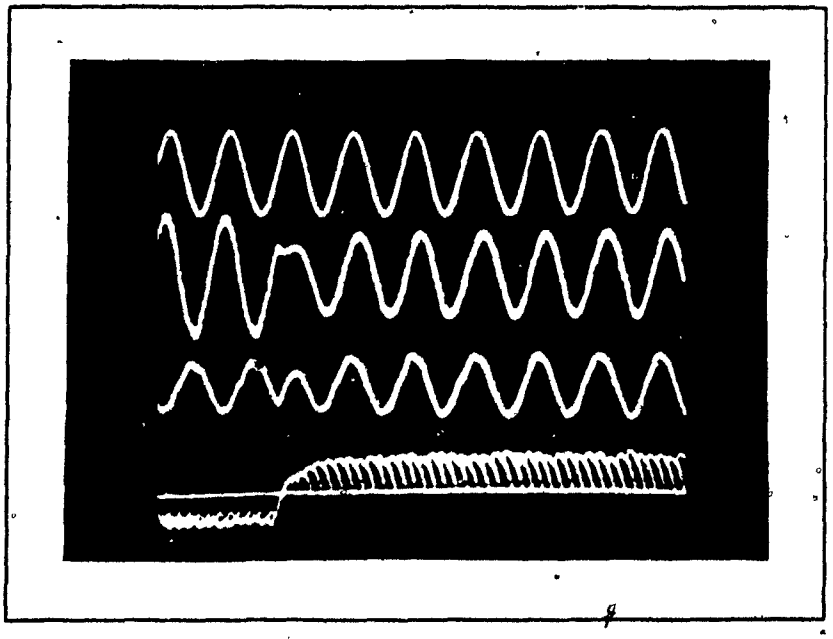


Fig.3.25 Reversal of Power with LdI/dt Block.
a) supply voltage V
b) modulating signal V_{mod}
c) input current I
d) output current i_1

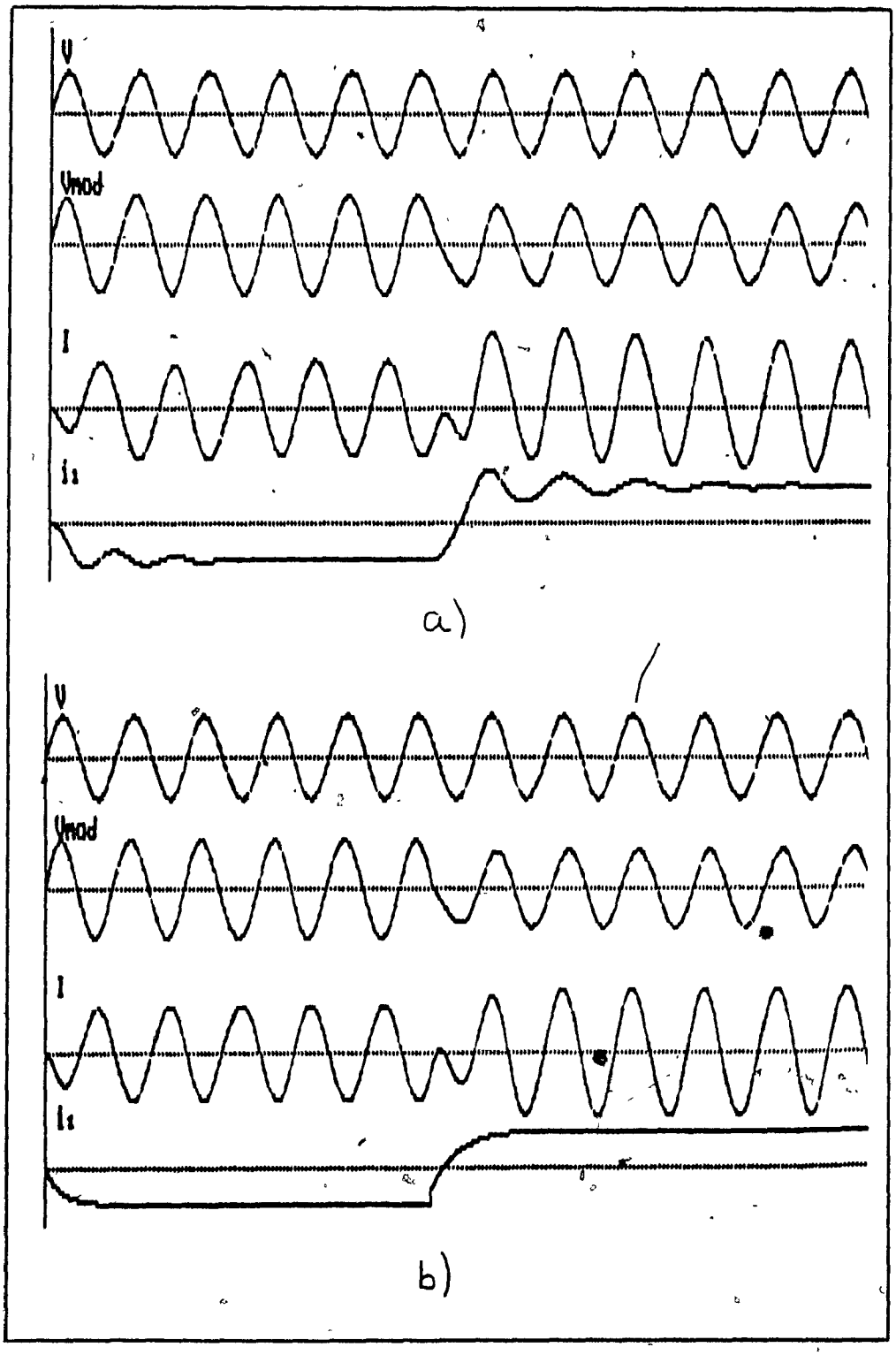


Fig.3.26 Mathematical Simulation of Figures 3.24 and 3.25.
a) no LdI/dt block
b) LdI/dt block

The next oscillograms of Figures 3.27 and 3.28 show that the stability limit of the rectifier is greater when the LdI/dt block is used, supporting the theory and the simulations. The two cases (L_b=0 and L_b=L) are compared under the same load conditions (i_2=5 A dc, I=7 A ac and C=6000 uF). The LdI/dt block in Figure 3.28 keeps the system strongly stable while in Figure 3.27, the removal of this block (L_b=0) has made the system dangerously unstable. The input current has a low frequency oscillatory component which does not exist in the compensated rectifier.

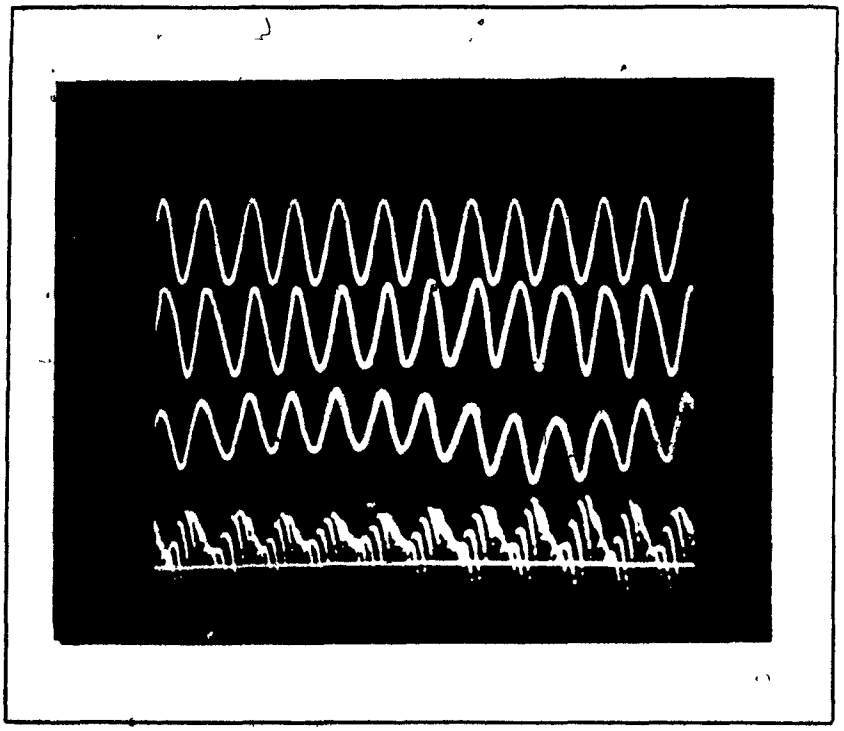


Fig.3.27 Stability without LdI/dt block.
a) supply voltage V
b) modulating signal V_{mod}
c) input current I
d) output current i_1

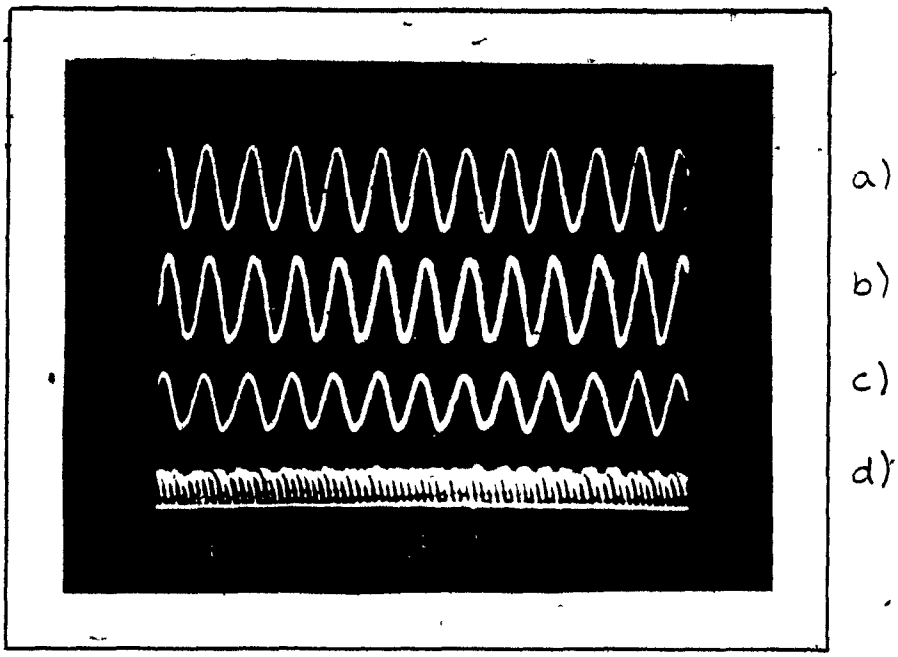


Fig.3.28 Stability with LdI/dt Block. -
a) V; b) V_{mod}; c) I; d) i_1

Figure 3.29 shows a simulation of Figure 3.27.

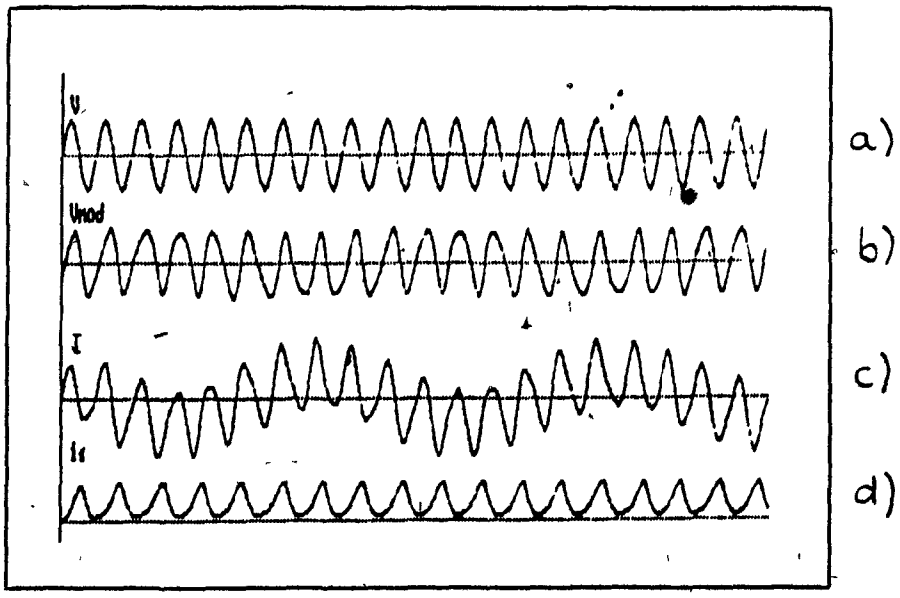


Fig.3.29 Mathematical Simulation of Figure 3.27.
a) V; b) V_{mod}; c) I; d) i_1

3.7.2.1 Proportional-Integral Control.

Figures 3.30 and 3.31 show a comparison between P and PI control. These Figures show: a) the dc voltage drop; b) the modulating signal V_{mod}; c) the input rms current I and d) the output dc current i_1 (before the dc capacitor). The main improvement in the PI control is the fact that the dc voltage returns to its reference value V_{REF} (null error) after a number of cycles of the supply source. This allows the reduction of the proportional gain Kp and consequently, the reduction of the dc capacitor. The bigger the value of the integral gain K_I, the faster the system returns to its zero error condition. However, there is a transient overcurrent which becomes undesirable if the integral gain K_I is too big. For the particular system implemented in the experiments, integral gains greater than 100 are not recommended because the system can become unstable. Figure 3.31 shows the case where K_I=50. It can be seen that with this value, the dc voltage returns to its reference value V_{REF} after a couple of cycles of the supply. The integral gain permits the reduction of the dc capacitor size two or three times with respect to the system with only proportional control.

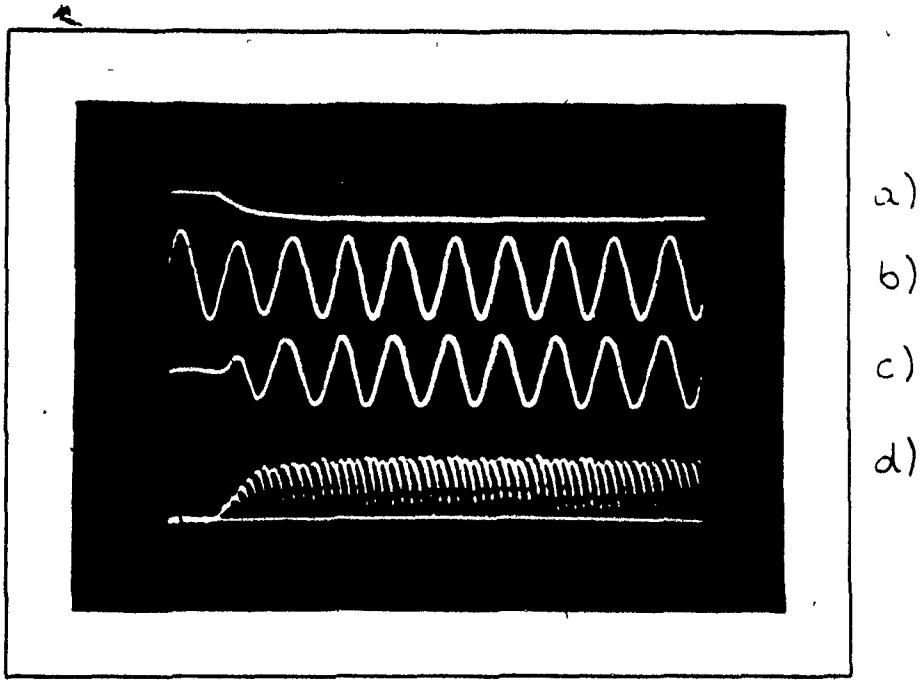


Fig.3.30 Compensated System with P Control. Kp=1
a) v_c; b) v_{mod}; c) I; d) i_1

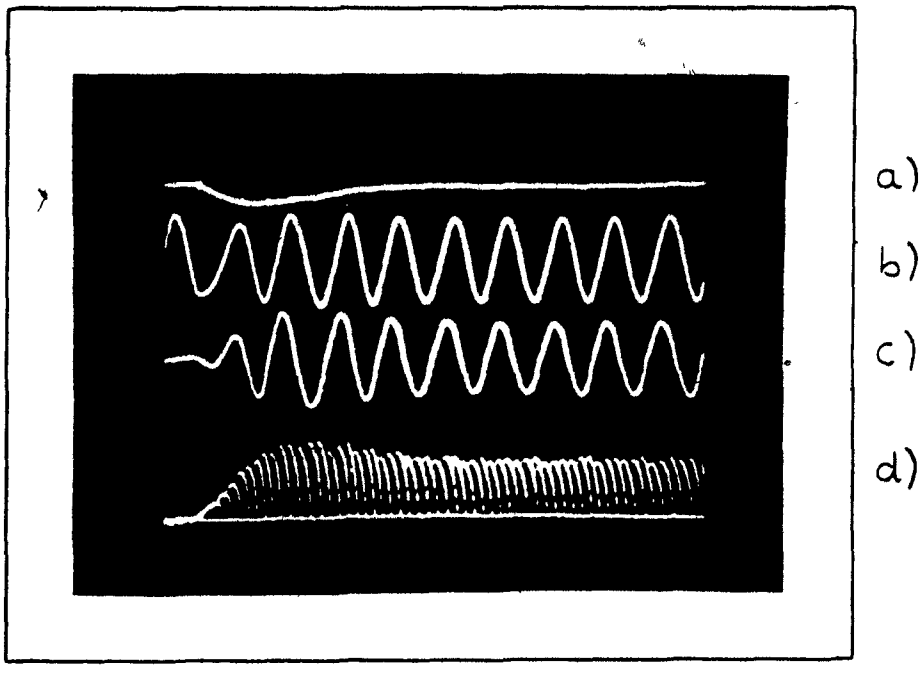


Fig.3.31 Compensated System with PI Control. Kp=1, K_I=50.
a) v_c; b) v_{mod}; c) I; d) i_1

3.8 Summary.

The principles, mathematical analyses, computer simulations and experiments for SPWM rectifiers using the Indirect Current Control Method have been presented.

It was shown that with the proper compensations, Indirect Control is as good as the direct method. The theory also supports the idea that Indirect Control can be made even better. Although the time restriction in research has not allowed experimental evidence to be obtained to support this claim, there is little doubt in its possibility. This is because the theory on which the claim is based, is strongly supported by experimental results.

The next chapter analyzes the connection of the PWM rectifiers in series. Different topologies are proposed using both the Direct and the Indirect Current Control Methods. Mathematical tools to find the stability for these topologies are developed. Computer simulations and experiments support the mathematical analyses.

CHAPTER IV

SERIES CONNECTED RECTIFIERS

4.1 Introduction.

The analyses of high quality, Boost type PWM rectifiers, with almost sinusoidal input currents, unity power factor operation and instantaneous power reversal capability have been presented in the previous chapters. Chapter II analyzed the Direct Current Control Method, in which the input current of the rectifier is measured and forced to follow a current reference template to satisfy the dc load requirements. Chapter III examined the Indirect Current Control Method, which simplifies the previous system by eliminating the current sensors. This is possible by estimating the input current needed to satisfy the dc load requirements, through previous knowledge of the parameters of the rectifier.

The present chapter intends to develop and describe some new concepts about series-connected rectifiers, which use the Direct and the Indirect Current Control Methods. The series connection, and later on the parallel connection in Chapter V, are the necessary steps in reaching high levels of power rectification, because the power ratings of the PWM rectifiers are limited by the low voltage and low current ceilings of commercially available power electronic switches (bipolar transistors, GTO's, power FET's).

Three different series topologies for Direct Control and two for the Indirect Control are discussed. In terms of hardware, they are organized from the most complex to the simplest.

A. Direct Current Control.

i) Type A: Independent Local Control

ii) Type B: Common Current Reference Control

iii) Type C: Common Switching Control

B. Indirect Current Control

i) Type D: Indirect Common Switching Control

ii) Type E: Shifted Triangular Carrier Control

Conditions of stability, input current and output voltage sharing and parameter sensitivity for each topology are analyzed. The mathematical analysis, based on the assumption that the fundamental harmonic predominates over the higher harmonics are verified by valve-by-valve simulations and experiments, using two series-connected PWM rectifiers.

4.2 Type A: Independent Local Control.

The Independent Local Control is a consequence of the self-supporting dc voltage capability of the voltage controlled PWM rectifiers discussed in the previous chapters. In this configuration, each modular unit is autonomous in that it has its current and its voltage control feedback loop.

Each rectifier requires at least two current sensors and an outer voltage regulator feedback loop which needs one voltage sensor. See Figure 4.1.

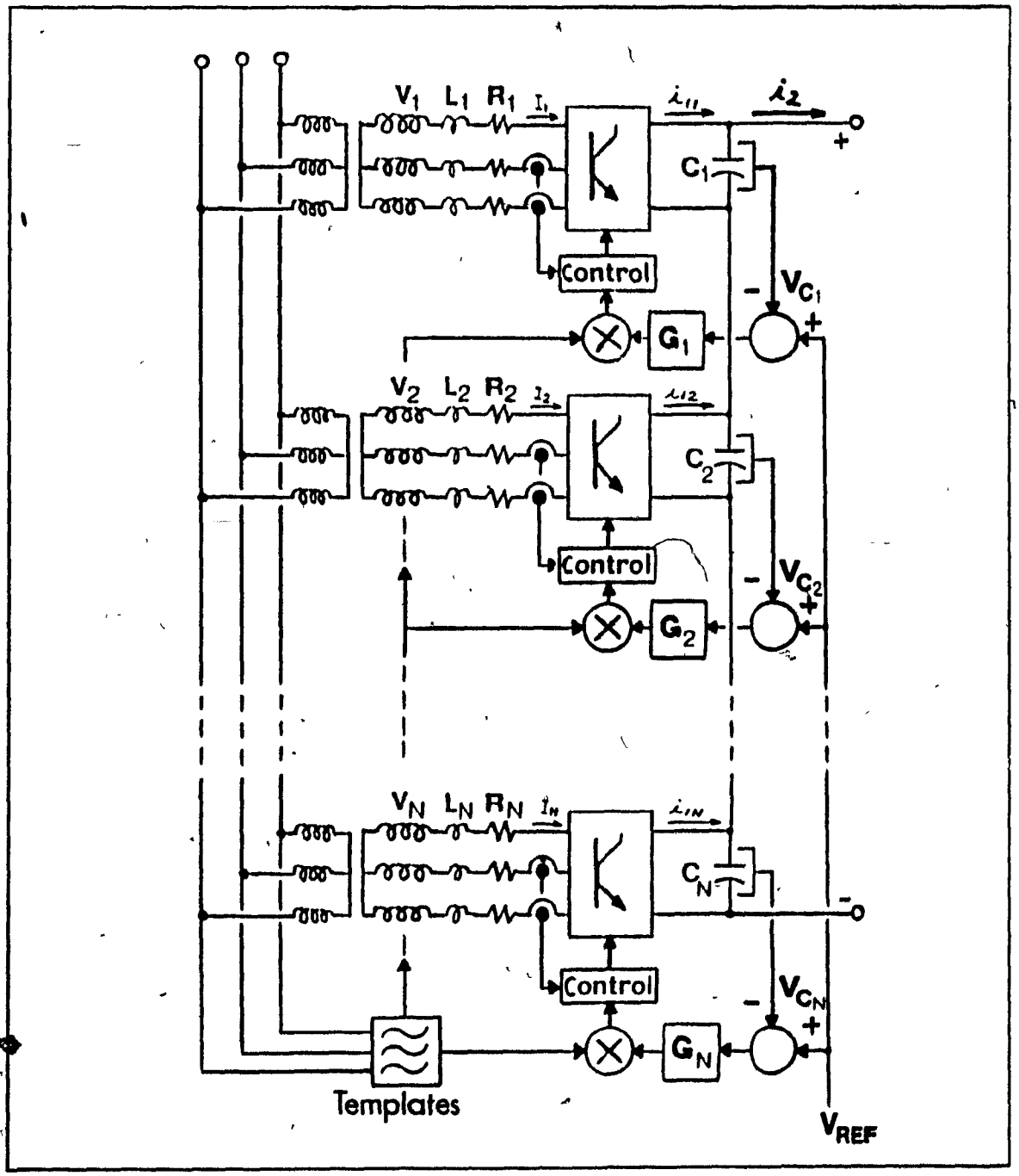


Fig.4.1 Type A: Independent Local Control Topology.

As shown in Figure 4.1, the series connected topology with Independent Local Control consists of connecting the autonomous modular units discussed in Chapter II in series. The floating transformer secondaries allow the dc link voltages to be added to form the output v_{out}.

$$v_{out} = \sum_n v_{cn} \tag{4.1}$$

The output current i_{2n} is common through each unit:

$$i_{2n} = i_2 \qquad (n=1,2...N) \tag{4.2}$$

and the output dc power is

$$P_{out} = i_2 \cdot \sum_n v_{cn} \tag{4.3}$$

4.2.1 Mathematical Model.

In this Chapter, it is assumed that the dc voltage regulator loop is a proportional controller. The control law of the rms ac phase current is:

$$I_n = K_n \cdot (V_{REF} - v_{cn}) \qquad (n=1,2...N) \tag{4.4}$$

where

K_n = proportional gain

V_{REF} = reference dc voltage

v_{cn} = dc link voltage

Based on the Power Balance Equation and assuming unity power factor operation, the dc link output power is:

$$i_{1n} \cdot v_{cn} = 3 \cdot (V_n I_n - R_n I_n^2 - \frac{1}{2} \cdot \frac{d}{dt} L_n I_n^2) \quad (n=1,2...N) \qquad (4.5)$$

where

V_n = rms phase voltage

i_{1n} = local average dc link current output

R_n = per phase resistance

L_n = per phase inductance

Kirchhoff's Current Law applied to the node of the dc link capacitance yields:

$$C_n \cdot \frac{dv_{cn}}{dt} = i_{1n} - i_2 \quad (n=1,2...N) \qquad (4.6)$$

The dynamic equation of each module is obtained by combining eqs.(4.4), (4.5) and (4.6), and yielding:

$$\frac{dv_{cn}}{dt} = \frac{3V_nK_n(V_{REF} - v_{cn}) - 3R_nK_n^2(V_{REF} - v_{cn})^2 - i_{2e}v_{cn}}{C_nv_{cn} - 3K_n^2L_n(V_{REF} - v_{cn})} \quad (n=1,2...N) \qquad (4.7)$$

4.2.2 Stability Analysis.

Applying the standard technique of small perturbation linearization of eq.(4.7) about the equilibrium point and assuming that $\Delta i_2=0$, one obtains:

$$\frac{d\Delta v_{cn}}{dt} = -\frac{1}{T_n} \cdot \Delta v_{cn} \quad (n=1,2...N) \qquad (4.8)$$

where

$$T_n = \frac{C_nv_{cn} - 3K_nL_nI_{ne}}{3K_n(V_n - 2R_nI_{ne}) + i_{2e}} \qquad (4.9)$$

Vc_n and i_{2e} are the equilibrium operating values of v_{cn} and i_2 and

$$I_{ne} = K_n \cdot (V_{REF} - Vc_n) \qquad (4.10)$$

To ensure stability, the time constant T_n must be positive which requires both the numerator and the denominator in eq.(4.9) to be positive. The positive numerator sets the limit of stable operation to:

$$I_{ne} < \frac{C_n \cdot Vc_n}{3 \cdot K_n \cdot L_n} \qquad (n=1,2...N) \qquad (4.11)$$

The positive denominator requires that:

$$I_{ne} < (V_n + \frac{i_{2e}}{3K_n})/2R_n \qquad (n=1,2...N) \qquad (4.12)$$

To keep the overall series system stable, each rectifier must satisfy rels.(4.11) and (4.12). Otherwise, the system voltage collapses.

4.2.3 Voltage and Current Sharing.

K_n is always chosen to be as large as possible and then, under steady-state conditions, the error magnitude becomes negligible. Because V_{REF} is common to all the rectifiers, one gets

$$Vc_n \simeq V_{REF} \qquad (n=1,2...N) \qquad (4.13)$$

Therefore, the voltage sharing is close to being balanced. This result is almost independent of the values of the

parameters R_n, L_n, and V_n. As the output current i_2 is the same for all the modules, the modular dc power

$$P_n = Vc_n \cdot i_2 \simeq V_{REF} \cdot i_2 \qquad (4.14)$$

is also almost the same for all the converters and hence

$$P_{out} \simeq N \cdot P_n \qquad (4.15)$$

The input currents may not be equal as they depend on the input voltages V_n and the resistances R_n. In particular, the current sharing between the modules n=j and n=k can be obtained from the steady-state Power Balance Equation

$$3 \cdot V_j \cdot I_j - 3 \cdot R_j \cdot I_j^2 = 3 \cdot V_k \cdot I_k - 3 \cdot R_k \cdot I_k^2 = P_n \qquad (4.16)$$

Where P_n, according to eq.(4.14), is the same for all the rectifiers. The Figure 4.2 shows the current sharing between the converters number j and k, when $V_j > V_k$. The cases $R_j = R_k = 0$ and $R_j = R_k > 0$ are displayed. It can be seen that the bigger is V_n, the smaller is the input current, because the system is trying to keep the input power constant. On the other hand, bigger resistances produce higher input currents.

As an example, let us assume that three rectifiers are connected in series using the Independent Local Control strategy, and with the following parameters in [pu]:

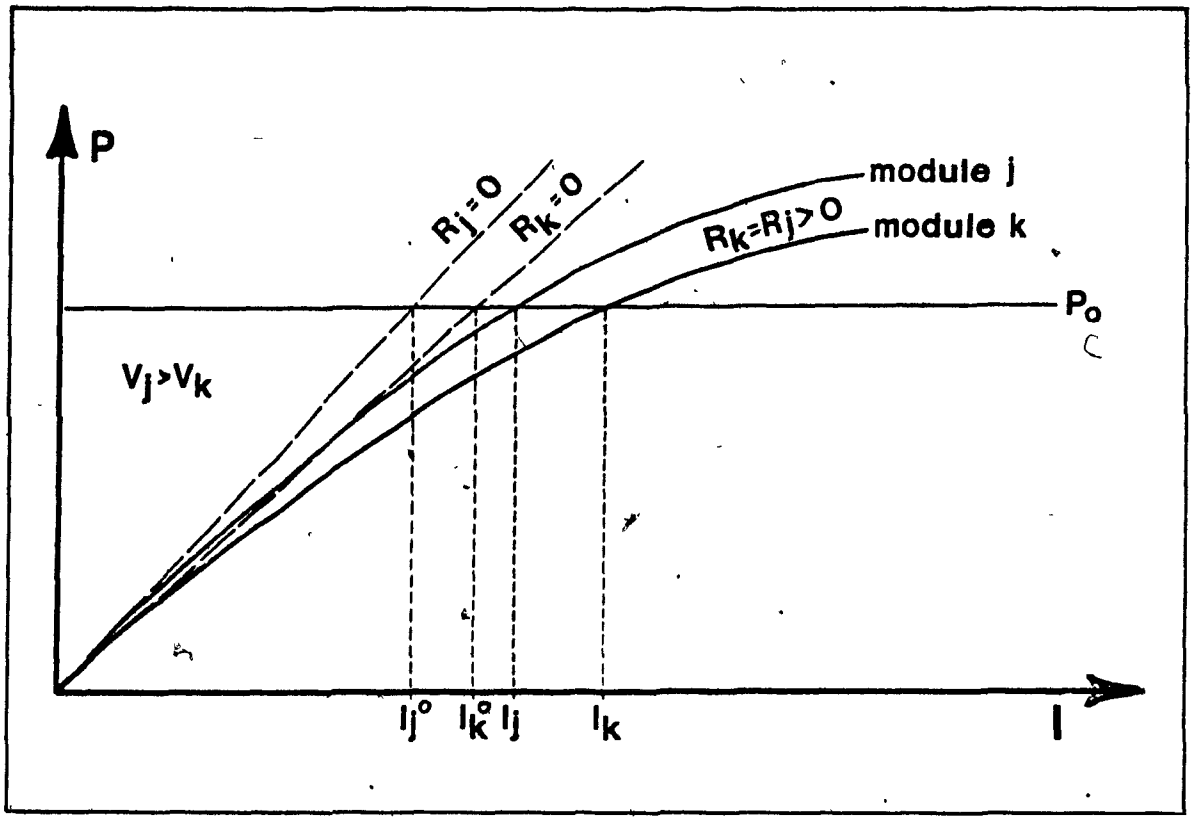


Fig.4.2 Input Current Sharing

$V_1 = V_2 = 1.0$ [pu]

$V_3 = 0.9$ [pu]

$R_1 = R_3 = 0.05$ [pu]

$R_2 = 0.1$ [pu]

$P_n/3 = 1.0$ [pu]

From eq.(4.16)

$$I_n = \frac{V_n - \sqrt{V_n^2 - 4/3 \cdot R_n \cdot P_n}}{2 \cdot R_n} \qquad (n=1,2...N) \qquad (4.17)$$

and from eq.(4.17) one gets:

$$I_1 = 1.06 \quad [pu]$$

$$I_2 = 1.13 \quad [pu] \quad (R_2=2R_1)$$

$$I_3 = 1.19 \quad [pu] \quad (V_3=0.9V_1)$$

These results show that current sharing is very sensitive to the input voltage, which means that the voltages from the input transformers must be balanced. The variations in resistance, on the other hand, show negligible change in the input currents. It should be noted that R_2 was increased twice and V_3 was only decreased 10 %.

4.3 Type B: Common Current Reference Control.

The Common Current Reference Control topology introduces the first simplification in the series system, by eliminating N-1 voltage sensors. The voltage is controlled in just one rectifier called "Master", as shown in Figure 4.3. The rest of the rectifiers, called "Slaves", are controlled by the same current reference generated in the Master rectifier. As a consequence, the input currents of all the rectifiers are identical

$$I_n = I_N = I \qquad (n=1,2...N) \qquad (4.18)$$

Because only one current reference must be produced, the voltage control blocks are also reduced from N to only one.

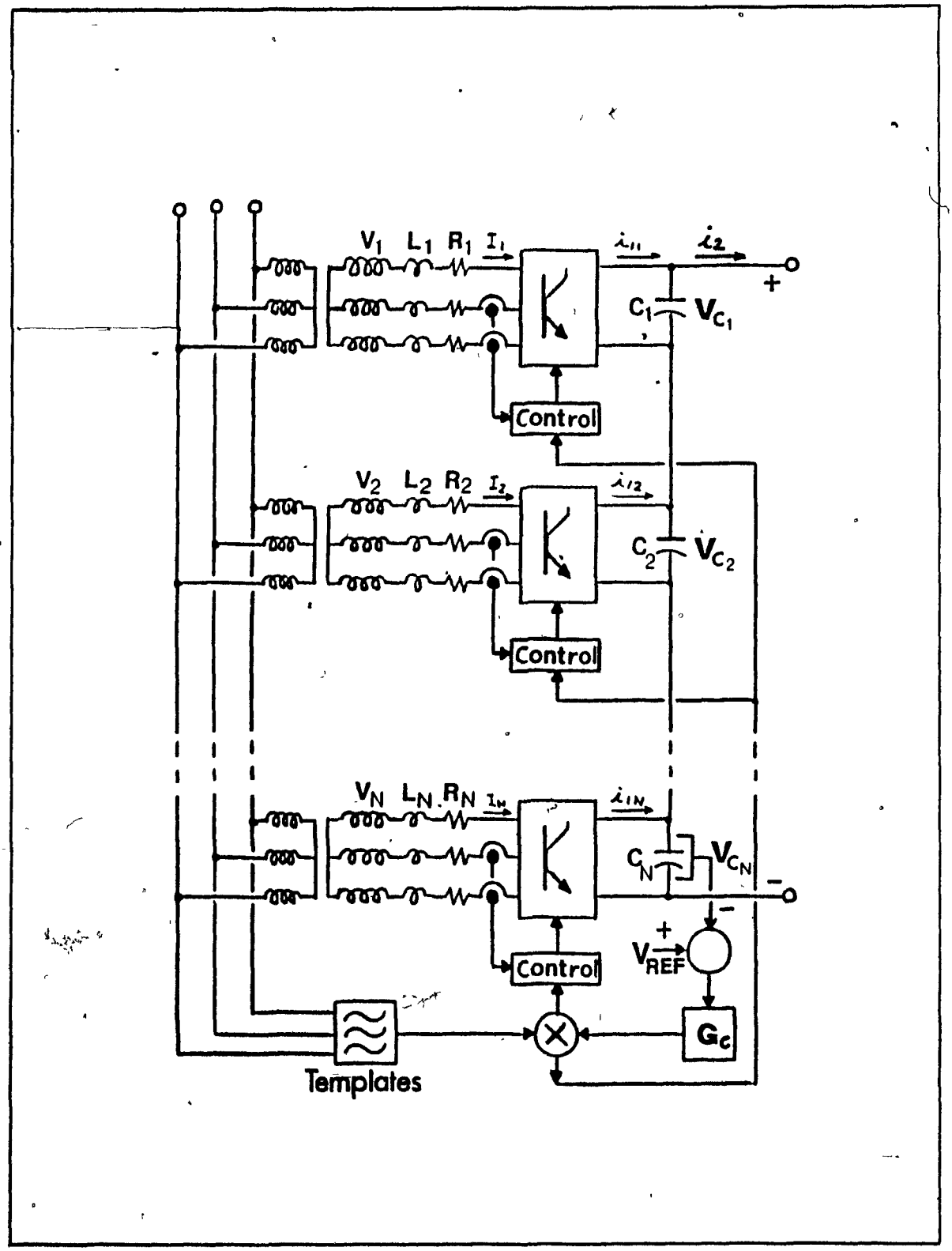


Fig.4.3 Type B: Common Current Reference Control Topology.

4.3.1 Stability Analysis.

The first stability condition for the Common Current Reference topology is that the Master Rectifier (converter number N) must satisfy rels.(4.11) and (4.12)

$$I < \frac{C_N \cdot V_{CN}}{3 \cdot Kp \cdot L_N} \tag{4.19}$$

$$I < (V_N + \frac{i_2}{3Kp})/2R_N \tag{4.20}$$

Because the Slaves do not have voltage reference and use the same current reference, the Power Balance Equation for the jth Slave is:

$$3 \cdot (V_j \cdot I - R_j \cdot I^2 - \frac{1}{2} L \frac{d}{dt} I^2) = v_{cj} \cdot i_2 + C_j \cdot v_{cj} \cdot \frac{dv_{cj}}{dt} \tag{4.21}$$

Let us assume that the Master satisfies rels.(4.19) and (4.20) and let us also assume that it is under steady-state. As the supply voltage V_j, the resistance R_j and the inductance L_j are considered constants, eq.(4.21) can be reduced to

$$v_{cj} \cdot i_2 + C_j \cdot v_{cj} \cdot \frac{dv_{cj}}{dt} = P_j = \text{constant} \tag{4.22}$$

This simple, non linear, first order differential equation can be written as:

$$\frac{dv_{cj}}{dt} = \frac{P_j}{C_j \cdot v_{cj}} - \frac{i_2}{C_j} \tag{4.23}$$

and solved through the phase plane as shown in Figure 4.4.

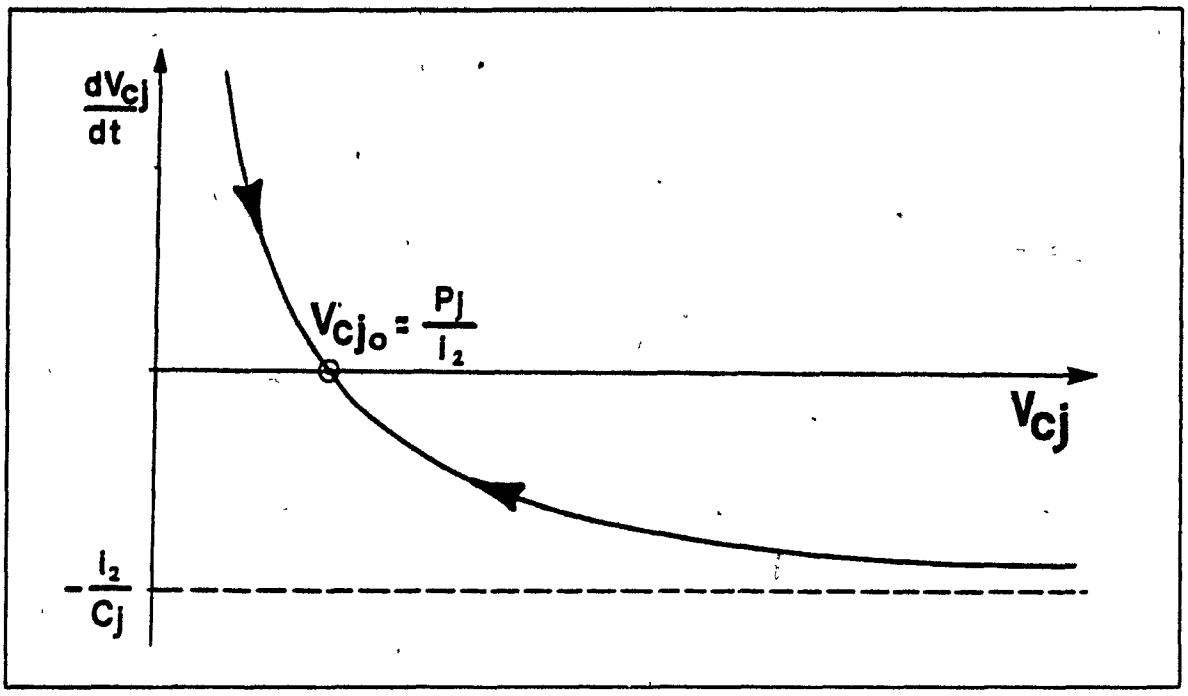


Fig.4.4 Phase Plane Portrait of Eq.(4.23)

From the phase portrait of Figure 4.4, it can be seen that the equilibrium point Vc_{jo} is stable and independent of the size of the dc capacitor. Therefore, the jth Slave is stable, even with very small dc capacitors. This means that Type B connection overcome the problem of stability given by rel.(4.19) for all the Slaves. As a consequence, besides the already mentioned saving in components, the Type B topology allows one to reduce the size of the dc capacitors, which are normally expensive.

However, an important drawback of the Type B is that it is unstable in the inverter quadrant and hence, it can only operate in the rectifier mode. This can be seen by making i_2 and P_j negative in eq.(4.22) from which a phase plane portrait

with an unstable equilibrium point is obtained. As a result, this system does not have power reversal capability.

4.3.2 Voltage and Current Sharing.

Unlike the Type A topology discussed in 4.2, the Type B strategy keeps the input currents identical, no matter what the values of the parameters are, because the Slaves use the same current reference as the Master. This fact has already been pointed out by eq.(4.18).

However, the dc voltages may not be identical. They are defined by the equilibrium points Vc_{jo} shown in Figure 4.4.

$$Vc_{jo} = \frac{P_j}{i_2} \tag{4.24}$$

As P_j represents the steady-state power of the jth Slave,

$$P_j = 3 \cdot V_j \cdot I - 3 \cdot R_j \cdot I^2 \tag{4.25}$$

Neglecting the resistance as a first approximation one gets

$$\frac{Vc_j}{Vc_N} = \frac{P_j}{P_N} = \frac{V_j}{V_N} \tag{4.26}$$

Thus, the dc voltage sharing directly depends on the balancing of the voltage transformers from the supply. The Type B topology can be made to operate in a perfectly balanced condition by the proper adjustment of the input transformers. This result has a dual relationship with the one obtained for the Type A configuration, in which perfectly balanced transformers were required to keep the input currents balanced.

4.4 Type C: Common Switching Control.

The Type C or Common Switching Control topology allows a second simplification in the series system, by eliminating all the current sensors from the Slaves, as shown in Figure 4.5.

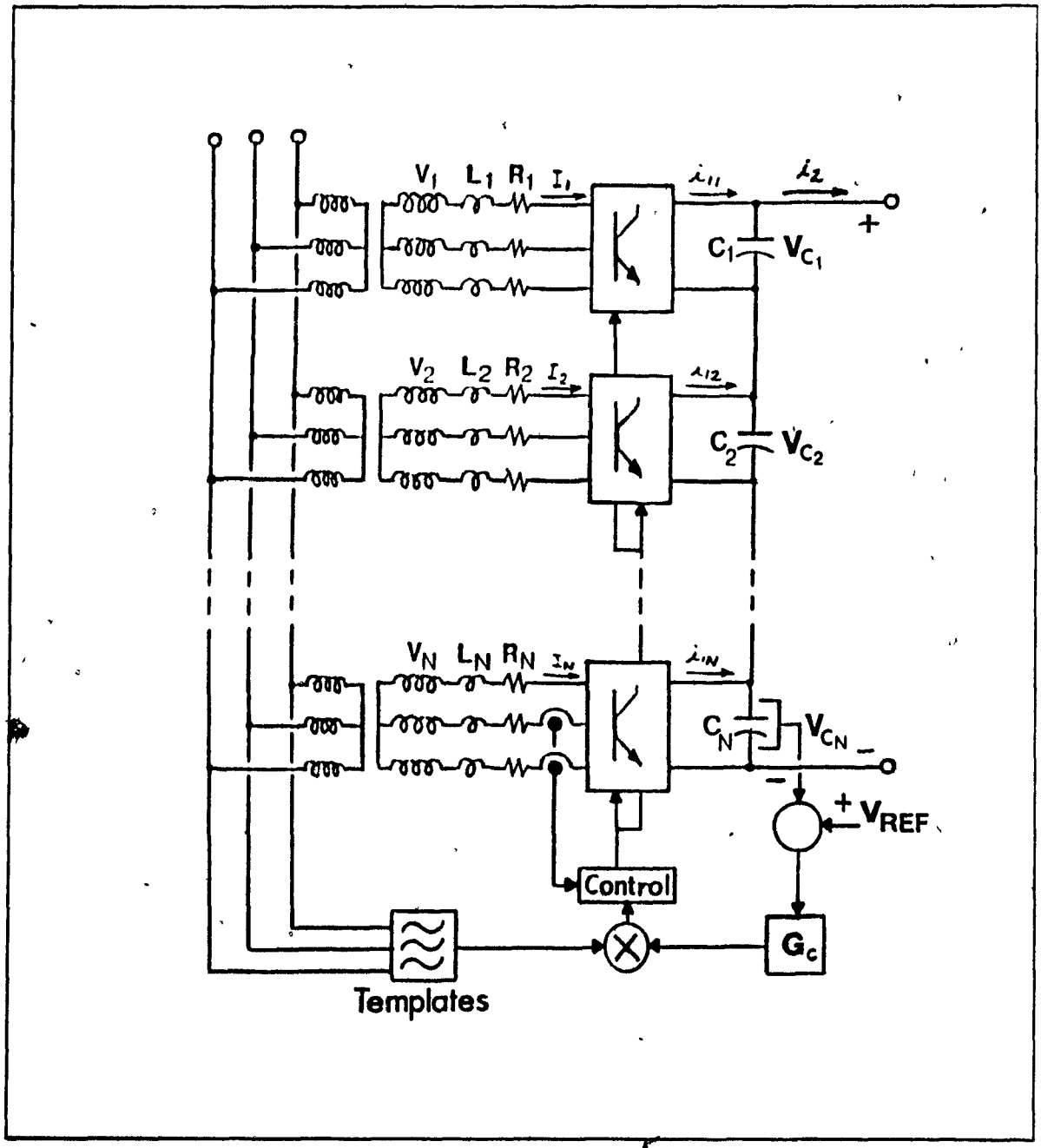


Fig.4.5 Type C: Common Switching Control Topology.

Only the Master rectifier keeps all the sensors, feedbacks and control blocks. The Slave units are in open loop. They receive logic commands from the Master so that the power electronic switches in the bridge turn ON and OFF in unison with the corresponding switches of the Master. Thus, the voltage at one phase of each of the modules will have identical patterns such as shown in the simulated oscillogram of Figure 4.6.

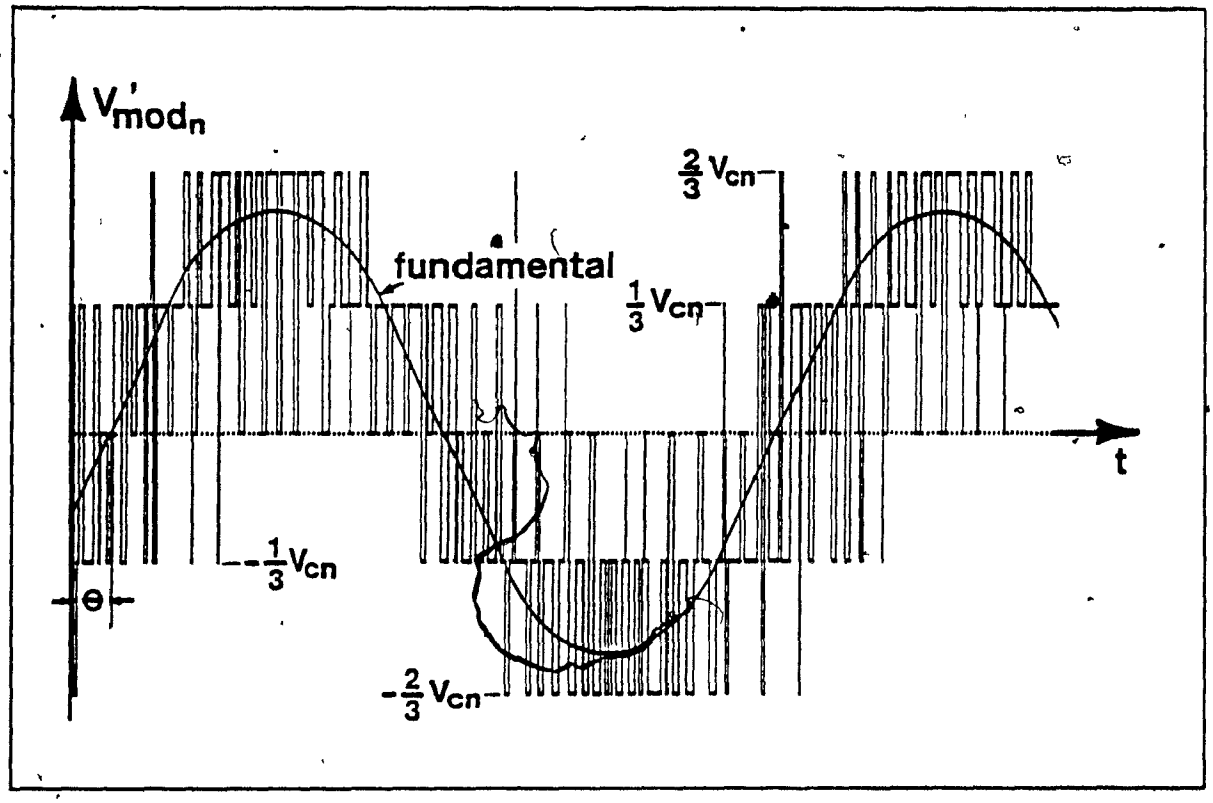


Fig.4.6 Simulated Waveform of the Phase Voltage of One Rectifier Terminal and its Fundamental.

In a Fourier analysis, the fundamental component of the voltage can be represented by a phasor $\hat{V}_{mod_n}$ (n=1,2...N). The magnitude of the phasors are related to the Master (converter number N) by the relationship

$$|\tilde{V}_{modn}| = \frac{V_{cn}}{V_{cN}} \cdot |\tilde{V}_{modN}| \qquad (4.27)$$

and they have the same phase angle as the Master

$$\theta_n = \theta_N = \theta \qquad (n = 1,2...N) \qquad (4.28)$$

In the Master unit, it is the phase current magnitude I_N which is being controlled by the hysteresis current feedback. The voltage phasor diagram of the fundamental harmonic as depicted in Figure 4.7 a) shows how $\tilde{V}_{modN}$ is related to $\tilde{V}_N, \tilde{I}_N$ and the impedance $\tilde{Z}_N = R_N + jX_N$.

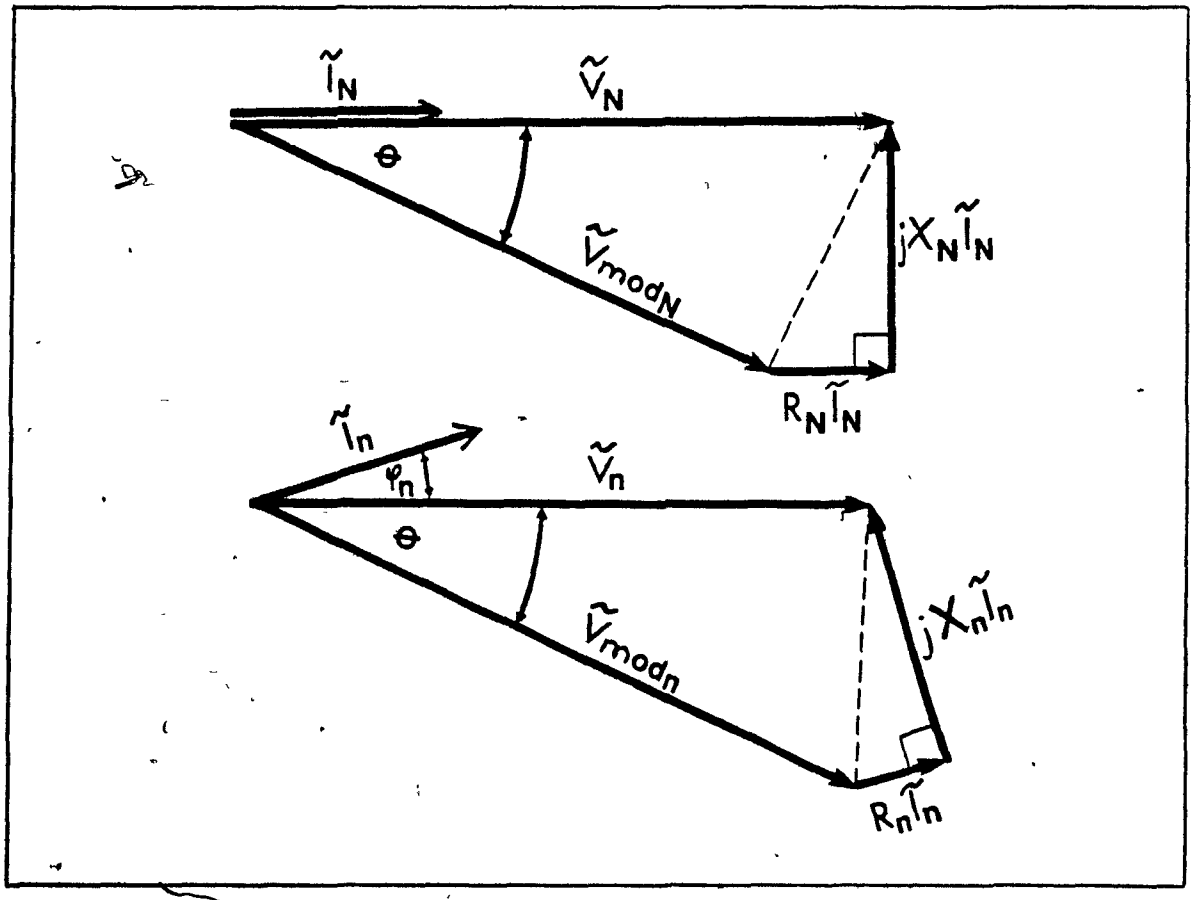


Fig.4.7 Phasor Diagram Relating Fundamental Harmonic Component a) Master, unity power factor operation; b) Slave

The control of the Slave Units is through $\tilde{V}_{modn}$ which is related to $\tilde{V}_{modN}$ through eqs.(4.27) and (4.28).

One sees from the voltage phasor diagram of Fig.4.7 b) that the Slave current $\tilde{I}_n$, which can change in magnitude and angle, is determined by $\tilde{I}_n \cdot \tilde{Z}_n$ which is the closing side of the triangle formed by $\tilde{V}_n$ and $\tilde{V}_{modn}$. $\tilde{V}_n$ is assumed to be constant and $\tilde{V}_{modn}$ can only vary in amplitude through eq.(4.27).

4.4.1 Stability Analysis.

Unlike the previous topologies, in which the power angle ϕ remains unaltered, the Type C configuration does modify the angle ϕ of the Slaves and then it becomes a variable in the mathematical analysis. To overcome the problem of having differential equations with trigonometrical functions, the d-q frame, using the power invariant transformation described in Section 3.4 of Chapter III is used. This mathematical analysis will also be valid for the Types D and E topologies, which will be discussed later.

4.4.1.1 Master Rectifier.

To ensure the stability of the Master rectifier, once again the relations (4.19) and (4.20) must be respected. As the Master is assumed to operate at unity power factor

$$I_N < \frac{C_N \cdot Vc_N}{3 \cdot Kp \cdot L_N} \qquad (4.29)$$

$$I_N < (V_N + \frac{i_2}{3Kp})/2R_N \qquad (4.30)$$

In controlling the time dependent magnitude of the input current I_N, the voltage $v_{modN}(t)$ at the Master Rectifier terminals for phase "a" is

$$v_{modN}(t) = \sqrt{2}\cdot\left(\left(V_N - L_N\cdot\frac{dI_N}{dt} - R_N\cdot I_N\right)\cdot\sin w_s t - X_N\cdot I_N\cdot\cos w_s t\right) \tag{4.31}$$

Transforming the a-b-c frame into a d-q frame it yields

$$v_{modNd} = -\sqrt{3}\cdot X_N\cdot I_N \tag{4.32}$$

$$v_{modNq} = -\sqrt{3}\cdot\left(V_N - R_N\cdot I_N - L_N\cdot\frac{dI_N}{dt}\right) \tag{4.33}$$

4.4.1.2 Slaves.

Because of the relations (4.27), (4.28), (4.32) and (4.33), the modulating voltage v_{modn} in the d-q frame for the Slaves (n=1,2..,N-1) is

$$\begin{bmatrix} v_{modnd} \\ v_{modnq} \end{bmatrix} = -\sqrt{3}\cdot\frac{v_{cn}}{v_{cN}}\begin{bmatrix} X_N\cdot I_N \\ V_N - R_N\cdot I_N - L_N\cdot\frac{dI_N}{dt} \end{bmatrix} \tag{4.34}$$

The transformed dynamic equation in the d-q frame for the Slaves is

$$\begin{bmatrix} L_n & 0 \\ 0 & L_n \end{bmatrix}\cdot\frac{d}{dt}\begin{bmatrix} i_{dn} \\ i_{qn} \end{bmatrix} + \begin{bmatrix} R_n & -X_n \\ X_n & R_n \end{bmatrix}\cdot\begin{bmatrix} i_{dn} \\ i_{qn} \end{bmatrix} = \begin{bmatrix} V_{nd} \\ V_{nq} \end{bmatrix} - \begin{bmatrix} v_{modnd} \\ v_{modnq} \end{bmatrix} \tag{4.35}$$

The angle of each supply voltage V_n (n=1,2...N) is the same and is the reference in the d-q frame. As a result, the vector $\underline{V}_n$ is

$$\underline{V}_n = \begin{bmatrix} V_{nd} \\ V_{nq} \end{bmatrix} = \begin{bmatrix} 0 \\ -\sqrt{3}\cdot V_n \end{bmatrix} \qquad (4.36)$$

Replacing eqs.(4.34) and (4.36) into eq.(4.35) it yields

$$\frac{d}{dt}\begin{bmatrix} i_{dn} \\ i_{qn} \end{bmatrix} = \frac{\sqrt{3}}{L_n}\begin{bmatrix} \frac{v_{cn}}{v_{cN}}\cdot X_N \cdot I_N \\ \frac{v_{cn}}{v_{cN}}(V_N - R_N I_N - L_N \frac{dI_N}{dt}) - V_n \end{bmatrix} - \begin{bmatrix} \frac{R_n}{L_n} & -w_s \\ w_s & \frac{R_n}{L_n} \end{bmatrix} \cdot \begin{bmatrix} i_{dn} \\ i_{qn} \end{bmatrix} \qquad (4.37)$$

There are three unknown values in the two-dimension differential equation, eq.(4.37): i_{dn}, i_{qn} and v_{cn}. A third relation is required. The Power Balance Equation for the Slaves, in the d-q frame, overcome the problem

$$v_{cn}\cdot i_{1n} = v_{modnd}\cdot i_{dn} + v_{modnq}\cdot i_{qn} \qquad (n=1,2..,N-1) \qquad (4.38)$$

where

$$i_{1n} = C_n\cdot\frac{dv_{cn}}{dt} + i_2 \qquad (n=1,2..,N-1) \qquad (4.39)$$

Replacing eq.(4.34) and (4.39) into (4.38), results

$$C_n\cdot\frac{dv_{cn}}{dt} = \frac{-\sqrt{3}}{v_{cN}}\{X_N I_N i_{dn} + (V_N - R_N I_N - L_N\frac{dI_N}{dt})i_{qn}\} - i_2 \qquad (4.40)$$

Because of eq.(4.4), the term dI_N/dt in eqs.(4.37) and (4.40) can be replaced by:

$$\frac{dI_N}{dt} = -Kp.\frac{dv_{cn}}{dt} \qquad (4.41)$$

The standard small perturbation linearization on eqs.(4.7) for the Master and (4.37) and (4.40) for the Slaves, about their equilibrium operating states, yields the following linear state equation for the N-1 Slaves and the Master

$$\frac{d}{dt}\begin{bmatrix} X_1 \\ X_2 \\ \cdot \\ \cdot \\ \cdot \\ X_{N-1} \\ X_N \end{bmatrix} = \begin{bmatrix} A_{11} & 0 & \cdots & 0 & A_{1N} \\ 0 & A_{22} & \cdots & 0 & A_{2N} \\ \cdot & \cdot & & \cdot & \cdot \\ \cdot & \cdot & & \cdot & \cdot \\ \cdot & \cdot & & \cdot & \cdot \\ 0 & 0 & \cdots & A_{N-1,N-1} & A_{N-1,N} \\ 0 & 0 & \cdots & 0 & A_{NN} \end{bmatrix} \cdot \begin{bmatrix} X_1 \\ X_2 \\ \cdot \\ \cdot \\ \cdot \\ X_{N-1} \\ X_N \end{bmatrix} \qquad (4.42)$$

The Master is characterized by the 1-tuple vector $X_N=\Delta v_{cN}$ and A_{NN} is a 1x1 matrix in the last line of eq.(4.42), based on perturbations of eq.(4.7):

$$A_{NN} = -\frac{3Kp(V_N - 2R_N I_N) + i_2}{C_N V c_N - 3Kp L_N I_N} \qquad (4.43)$$

The dynamics of each of the N-1 Slaves is described by equations involving the 3-tuple vector $X_n^T=[\Delta v_{cn}, \Delta i_{dn}, \Delta i_{qn}]$ and the 3x3 matrix:

$$[A_{nn}] = \begin{bmatrix} 0 & -p_n L_n & -q_n L_n \\ p_n C_n & r_n & s_n \\ q_n C_n & -s_n & r_n \end{bmatrix} \qquad (n=1,2..,N-1) \qquad (4.44)$$

where

$$p_n = \frac{\sqrt{3} \cdot X_N \cdot I_N}{Vc_N C_n L_n} \tag{4.45}$$

$$q_n = \frac{\sqrt{3}(V_N - R_N I_N)}{Vc_N C_n L_n} \tag{4.46}$$

$$r_n = -\frac{R_n}{L_n} \tag{4.47}$$

$$s_n = w_s \tag{4.48}$$

Each Slave is coupled to the Δv_{cN} of the Master through

$$[A_{nN}]^T = [e_n, f_n, g_n] \qquad (n=1,2..,N-1) \tag{4.49}$$

where

$$e_n = \frac{\sqrt{3}Kp}{Vc_N C_n} \cdot (X_N I_{dn} - R_N I_{qn} + L_N I_{qn} \cdot A_{NN} - \frac{i_2}{3Kp}) \tag{4.50}$$

$$f_n = \frac{X_n I_{qn} - R_n I_{dn} - \sqrt{3} X_N Vc_N Kp}{L_n Vc_N} \tag{4.51}$$

$$g_n = \frac{\sqrt{3}KpVc_n}{Vc_N L_n} \cdot (R_N - L_N \cdot A_{NN} - \frac{\sqrt{3}V_n \pm X_n I_{dn} \pm R_n I_{qn}}{3KpVc_N}) \tag{4.52}$$

I_{dn}, I_{qn} and Vc_n are the steady-state solutions of eqs.(4.37) and (4.40).

As Δv_{cN} of the Master can be regarded as a forcing function in the equation

$$\dot{X}_n = [A_{nn}] \cdot X_n + [A_{nN}] \cdot \Delta v_{cN} \tag{4.53}$$

the stability of each Slave is determined by the eigenvalues of the matrix $[A_{nn}]$. As the objective is to prove global

stability, the characteristic equation is obtained in the 3rd order polynomial form:

$$\text{determinant}\,(S[I] - [A_{nn}]) = a_{0n}S^3 + a_{1n}S^2 + a_{2n}S + a_{3n} = 0 \qquad (n=1,2..,N-1) \qquad (4.54)$$

where

$$a_{0n} = 1 \qquad (4.55)$$

$$a_{1n} = 2R_n/L_n \qquad (4.56)$$

$$a_{2n} = \frac{R_n^2 + X_n^2}{L_n^2} + \frac{3[(X_N I_N)^2+(V_N-R_N I_N)^2]}{L_n C_n V_{C_N}^2} \qquad (4.57)$$

$$a_{3n} = \frac{3[(X_N I_N)^2+(V_N-R_N I_N)^2]}{L_n C_n V_{C_N}^2} \cdot \frac{R_n}{L_n} \qquad (4.58)$$

The stability of the Slaves can be found by Routh's Criterion. Routh's Criterion assures stability when $a_{jn}>0$ for $j=0,1,2,3$ and $(a_{1n}\cdot a_{2n}-a_{0n}\cdot a_{3n})>0$. From eqs.(4.55) to (4.58) it is clear that $a_{jn}>0$ is satisfied when $R_n>0$. The second condition, $(a_{1n}\cdot a_{2n}-a_{0n}\cdot a_{3n})>0$,

$$\left(\frac{2(R_n^2+X_n^2)}{L_n^2} + \frac{3[(X_N I_N)^2+(V_N-R_N I_N)^2]}{L_n C_n V_{C_n}^2}\right)\cdot\frac{R_n}{L_n} > 0 \qquad (4.59)$$

is satisfied again if $R_n>0$.

In conclusion, the Slaves are always stable, because the ideal condition $R_n=0$ for 100% efficiency, is never reached. The direction of the power does not come into the stability conditions and hence, the Slaves are stable for both, rectifier and inverter operation. Therefore, the overall

system is stable when the Master does not violate the relations (4.29) and (4.30) and the Type C configuration, like Type A, has power reversal capability.

Let us try to explain the stability of the Slaves through the phasor diagram of Figure 4.8. When the Master is under steady-state, the θ angle is constant and hence, any perturbation in the Slave voltage v_{cn} only affects the amplitude of V_{modn}, making the input current to move following the "ac locus", shown in Figure 4.8, to satisfy the phasor diagram. But, because of the power balance between the ac and the dc side of the rectifier, the load current i_2 tries to force the input current I_n to follow the "dc locus", also shown in Figure 4.8.

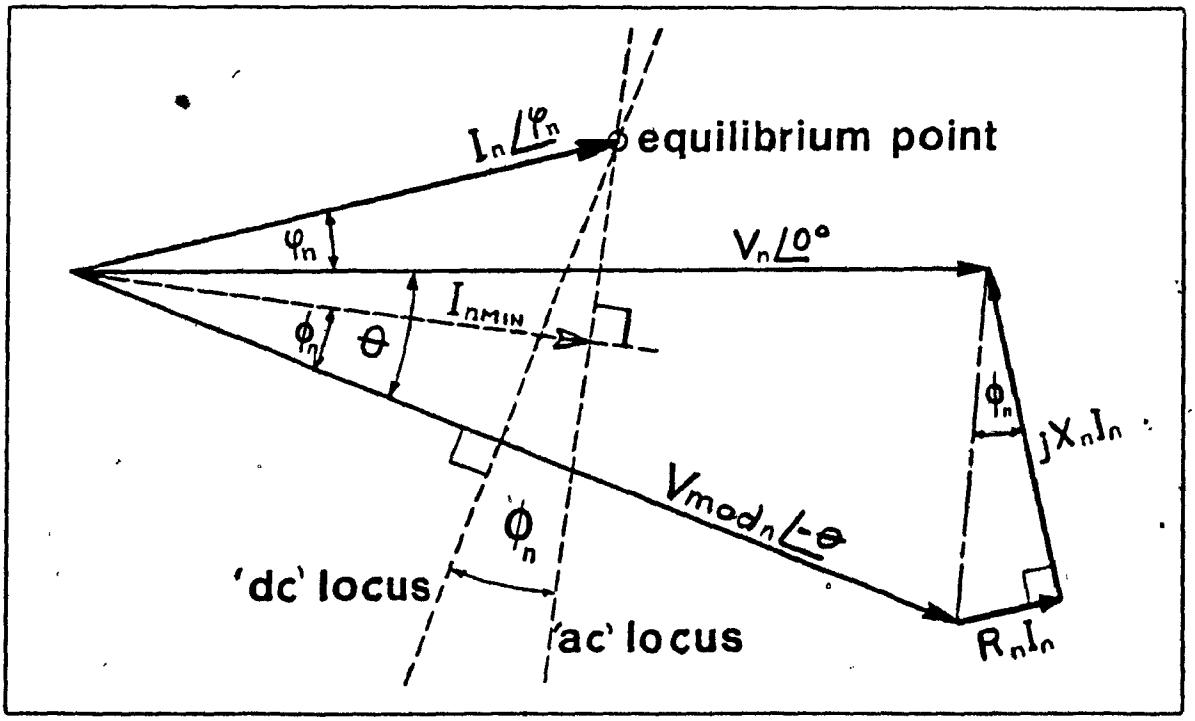


Fig.4.8 Slave Phasor Diagram and its Equilibrium point

The intersection of these two locii represents a stable equilibrium point, because when v_{cn} increases (decreases), less (more) power comes from the ac side, discharging (charging) the capacitor C_n and making the Slave to return to the equilibrium point. Similar reasoning can be used for the inverter mode, in which a stable equilibrium point is also reached.

It can be seen from Figure 4.8 that the equilibrium point is stable and only possible when $R_n>0$. When $R_n=0$, the two locii are parallel and hence cannot meet. On the other hand, a hypothetical Rn<0 would produce an unstable equilibrium point.

4.4.2 Voltage and Current Sharing.

The voltage (Vc_n) and current (I_n) sharing for the Type C configuration is found from the steady-state solutions of eqs.(4.37) and (4.40). Eq.(4.37) gives the in-phase and the in-quadrature terms of I_n. The steady-state solution of eq.(4.37) is:

$$\begin{bmatrix} I_{dn} \\ I_{qn} \end{bmatrix} = \frac{\sqrt{3}}{R_n^2+X_n^2} \begin{bmatrix} \frac{Vc_n}{Vc_N}\cdot\{I_N X_N R_n+(V_N-R_N I_N)X_n\}-V_n X_n \\ \frac{Vc_n}{Vc_N}\cdot\{-I_N X_N X_n+(V_N-R_N I_N)R_n\}-V_n R_n \end{bmatrix} \qquad (4.60)$$

and the steady-state solution for eq.(4.40) is

$$i_{2e}Vc_n = -\sqrt{3}\{I_N X_N I_{dn} + (V_N-R_N I_N) I_{qn}\} \qquad (4.61)$$

where, from the Master steady-state Power Balance Equation:

$$i_{2e} Vc_N = 3(V_N - R_N I_N) I_N \tag{4.62}$$

Eqs.(4.60) to (4.62) permit one to express the values of I_{dn}, I_{qn} and Vc_n, in terms of the Master current I_N, the Master voltage Vc_N, and the constants R_N, R_n, X_N, X_n, V_N and V_n.

Substituting eq.(4.62) into (4.61) and then this result into eq.(4.60) yields:

$$Vc_n = \hat{Vc}_N \cdot \frac{(V_n X_n - X_N I_N + (V_N - R_N I_N)(R_n V_n - I_N(R_n^2 + X_n^2)))}{R_n \cdot Denom} \tag{4.63}$$

$$I_{dn} = \sqrt{3} \cdot I_N \cdot \frac{(V_N - R_N I_N) \cdot (V_n X_N - V_N X_n + I_N(R_N X_n - R_n X_N))}{R_n \cdot Denom} \tag{4.64}$$

$$I_{qn} = -\sqrt{3} \cdot I_N \cdot \frac{(R_n(V_N - R_N I_N)^2 + X_N I_N(V_n X_N - V_N X_n \pm R_N I_N X_n))}{R_n \cdot Denom} \tag{4.65}$$

where

$$Denom = (V_N - R_N I_N)^2 + (I_N X_N)^2 \tag{4.66}$$

The magnitude and phase of the input Slave current, I_n, is found through eqs.(4.64) and (4.65):

$$I_n = |I_n| \angle \phi_n \tag{4.67}$$

where

$$|I_n| = \frac{1}{\sqrt{3}} \sqrt{I_{dn}^2 + I_{qn}^2} \tag{4.68}$$

and

$$\phi_n = tg^{-1}(-I_{dn}/I_{qn}) \tag{4.69}$$

From eqs.(4.63) to (4.69), it can be found that voltages and currents are perfectly balanced when the parameters of the Slaves are identical to the corresponding parameters of the Master ($R_n=R_N$, $X_n=X_N$ and $V_n=V_N$). Based on these equations, Figures 4.9 and 4.10 show graphically the effect of the parameter variations on I_n and Vc_n with respect to the Master steady-state conditions, as a function of X_n and V_n respectively. The Master operates at its rated power and X_N=0.25 [pu].

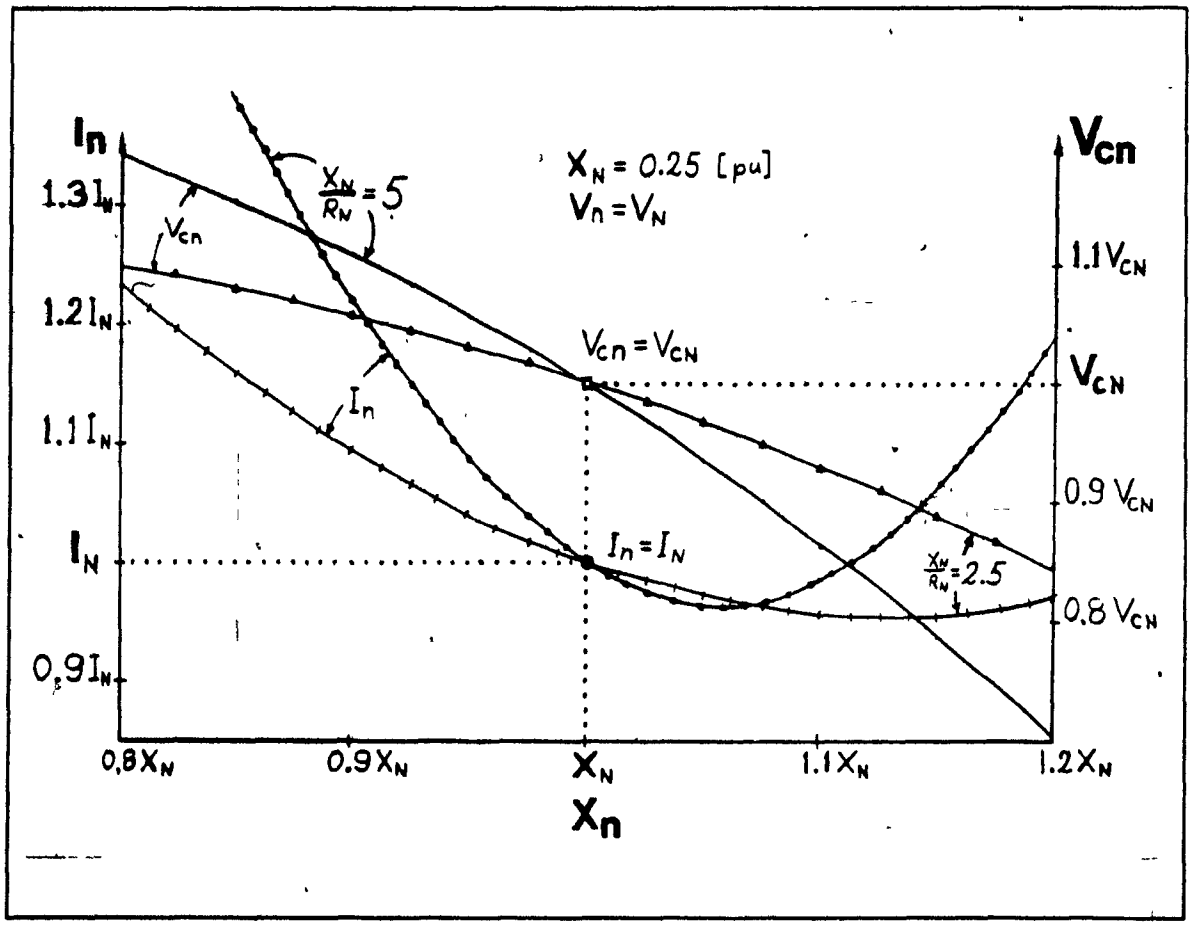


Fig.4.9 Parameter Sensitivity of Type C Connection to X_n Variations

It can be seen from Figure 4.9 that the Slave current I_n is very sensitive to X_n variations. The Slave output voltage Vc_n, is also affected by X_n variations. Note that in both cases, the X_N/R_N ratio has an important influence in the parameters variation. The bigger is this ratio, the more sensitive becomes the system. It is clear that the system should keep all the reactances with deviations not bigger than 5 % with respect to the Master reactance.

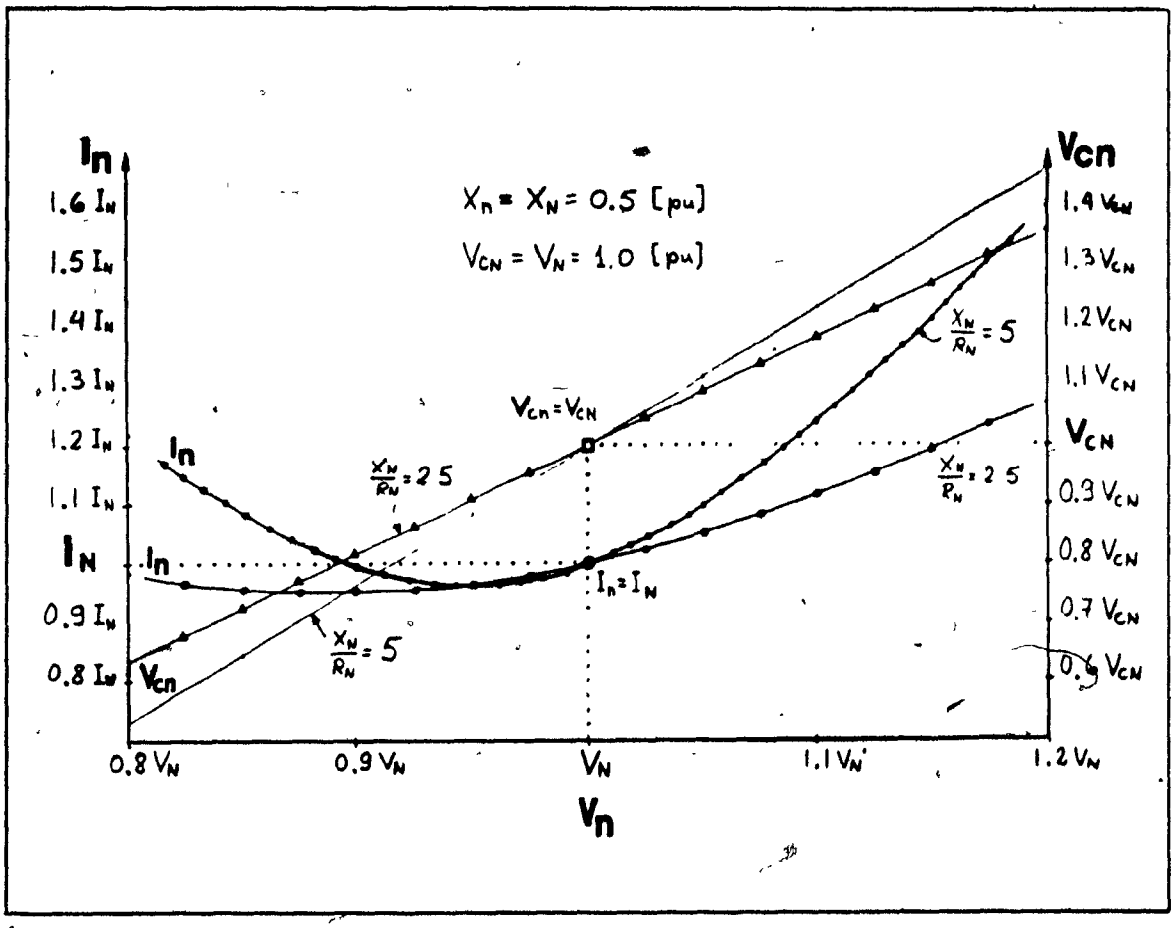


Fig.4.10 Parameter Sensitivity of Type C Connection to V_n Variations

The values of R=0.05 [pu] (X_N/R_N=5) and R=0.1 [pu] (X_N/R_N=2.5) represent modular efficiencies of about 95 and 90 percent respectively. The figure shows the I_n and Vc_n variations for X_N/R_N=5 and X_N/R_N=2.5. These ratios and the value X_N=0.25 [pu] are very representative of real systems.

The Figure 4.10 shows similar behaviour in the Slave input current and output voltage when its supply voltage V_n changes with respect to V_N. The voltage Vc_n increases almost linearly when V_n increases. Once again, bigger X_N/R_N ratios produce high current and voltage sensitivity to parameters variation. The supply voltage V_n should be kept as close to the Master supply voltage V_N as possible.

With these results it is easy to realize that it is very important to keep the Slave reactance X_n and the supply voltage V_n of this configuration as close to the Master values as possible. Any variation in these parameters exceeding 5 % cannot be tolerated.

The resistance R_n has been proven to produce a negligible effect on I_n and Vc_n. For this reason, it is not shown graphically.

The capacitors C_n play neither a role in the sharing of the power nor in the stability of the system. Hence, they can be made small in the Slaves. However, the Master has to have a sufficiently large capacitance to satisfy rel.(4.29).

4.5 Type D: Indirect Common Switching Control.

The Type D or Indirect Common Switching Control is based on the same operation principle as Type C. The difference is that the Indirect Current Control Method, discussed in Chapter III replaces the Direct Method of control used in the Type C configuration. This allows a third simplification in the series system: the elimination of the last two current sensors from the Master. In the Type D configuration, the overall feedback system is controlled by only measuring the Master dc voltage.

Figure 4.11 shows the diagrammatic representation of the Master rectifier which uses the Indirect Current Control Method discussed in Section 3.2 of Chapter III: The Sinusoidal PWM or SPWM strategy.

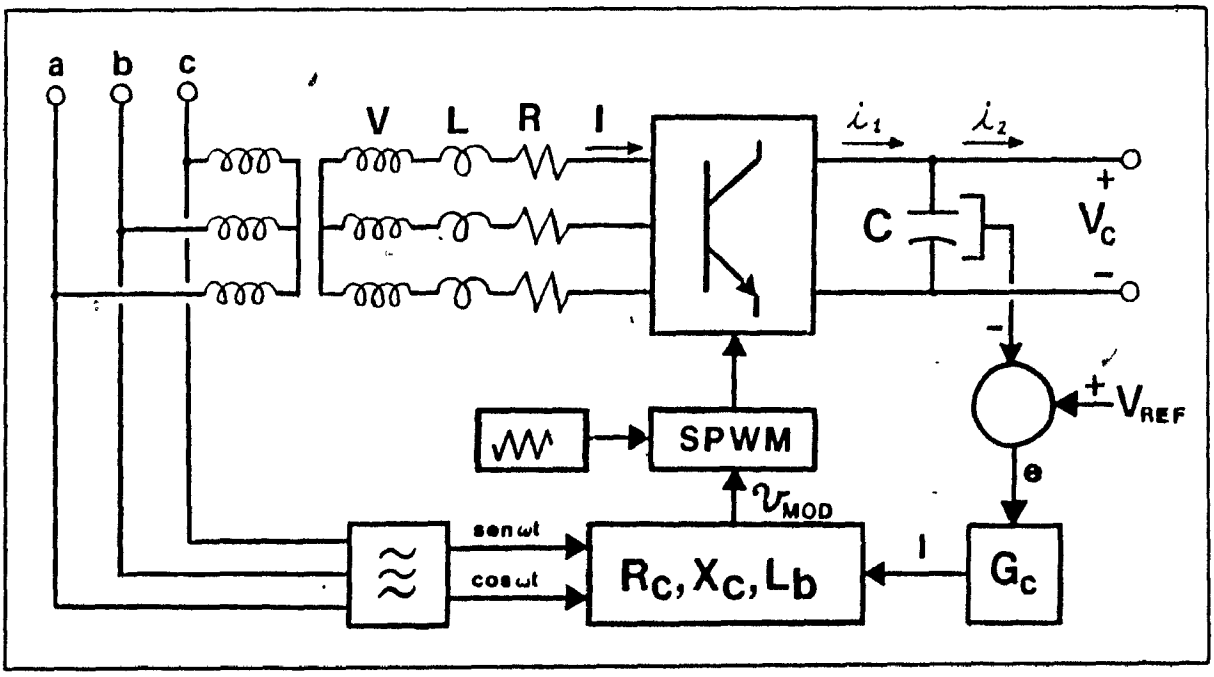


Fig.4.11 Diagrammatic Representation of the Indirect Current Control Method, Using SPWM Strategy

The SPWM strategy generates the voltage V_{mod} through the intersections of a triangular carrier and the three-phase modulating signals produced in the hardware.

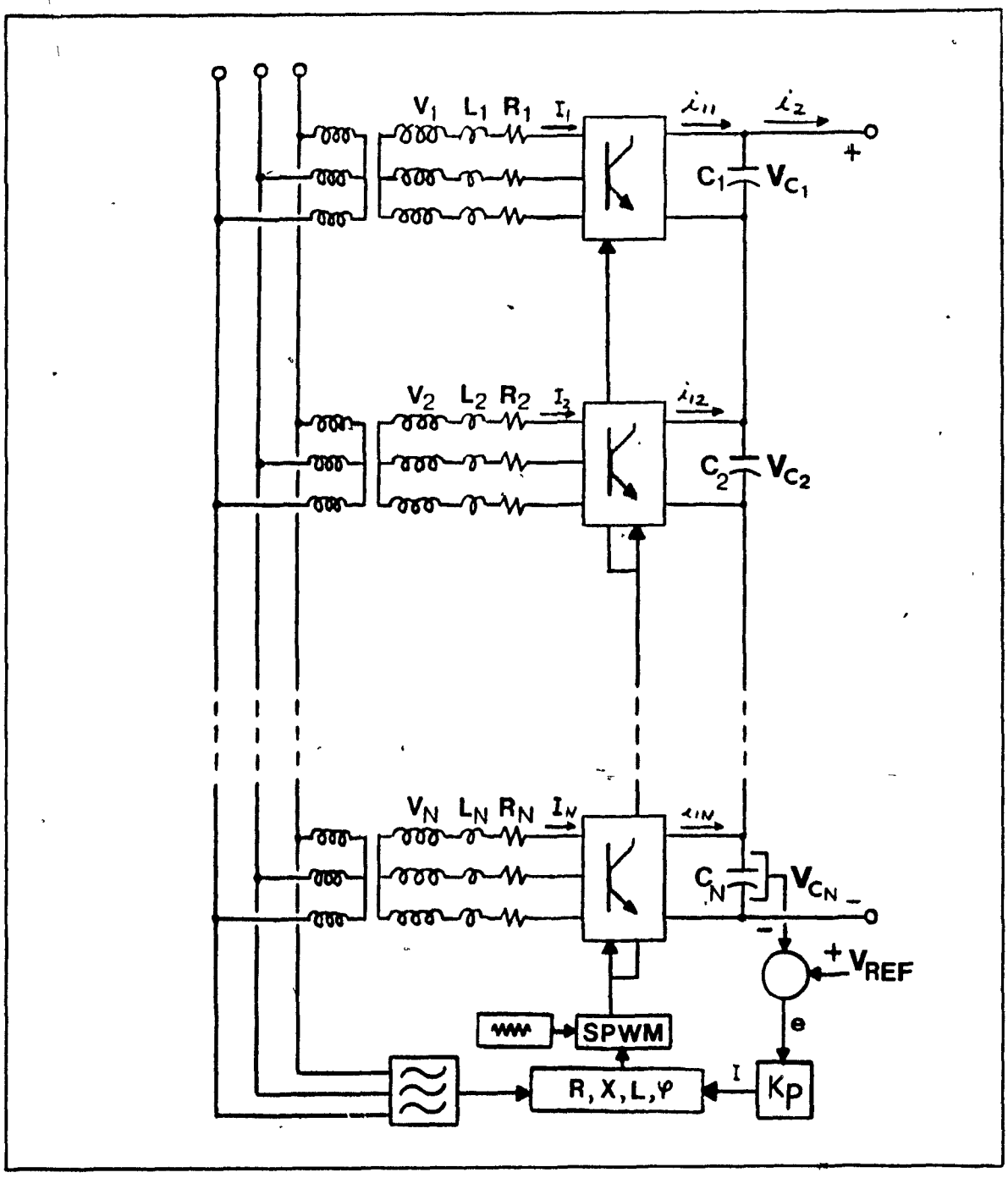


Fig.4.12 Type D: Indirect Common Switching Control Topology

The Master, represented in Figure 4.11, is connected to the Slaves driven by the Common Switching principle shown in Figure 4.12. The word "Indirect" has been added to the definition of Type D to differentiate it from the Direct Current Method (hysteresis) used in the Type C configuration.

4.5.1 Stability Analysis.

As this system uses the same principle of operation as Type C, the stability analysis developed for the former in Section 4.4.1 is also valid here and will not be repeated. The Slaves are stable for $R_n>0$. The Master has conditional stability. Thus, the overall system stability depends on the Master. The stable conditions for the overall system (assuming $L_b=L_N$ in the Master rectifier) are:

$$R_n > 0 \qquad (n=1,2..,N-1) \tag{4.70}$$

$$I_N < \frac{C_N \cdot V_{C_N}}{3kp \cdot L_N} \tag{4.71}$$

$$I_N < (V_N + \frac{i_2}{3Kp})/2R_N \tag{4.72}$$

4.5.2 Voltage and Current Sharing.

As the mathematical analysis of the Type D is the same as of the Type C configuration, the voltage and current sharing can be based on eqs.(4.63) to (4.69) and Figures 4.9 and 4.10. Therefore, it is not required to repeat it.

4.6 Type E: Shifted Triangular Carrier Control.

The Type E or Shifted Triangular Carrier Control configuration does not introduce any reduction in the hardware. On the contrary, a slight increase in the number of hardware components is required. However, the system performance is greatly improved in terms of operational costs. The Type E configuration is able to produce excellent current waveforms with low switching frequency and hence high overall efficiency with respect to the other configurations.

The idea is based on generating independent triangular carriers for each Slave, with the purpose of eliminating some unwanted harmonics. The Type E configuration is shown in Figure 4.13.

4.6.1 Harmonic Elimination.

It is shown here that by using the same modulating signal as the Master but with the slight modification that each Slave has its own triangular carrier which is suitably phase-shifted, significant numbers of unwanted harmonics are eliminated.

When w_T and w_S (see Chapter III) are the angular frequencies of the triangular carrier and the modulating sinusoidal signal respectively, the double Fourier Series method of analysis [68], expresses the jk^{th} harmonic voltage component of SPWM as:

$$v_{jk}(t) = V_{jk}\cdot\sin(jw_Tt + kw_St + \phi_{jk}) \qquad (4.73)$$

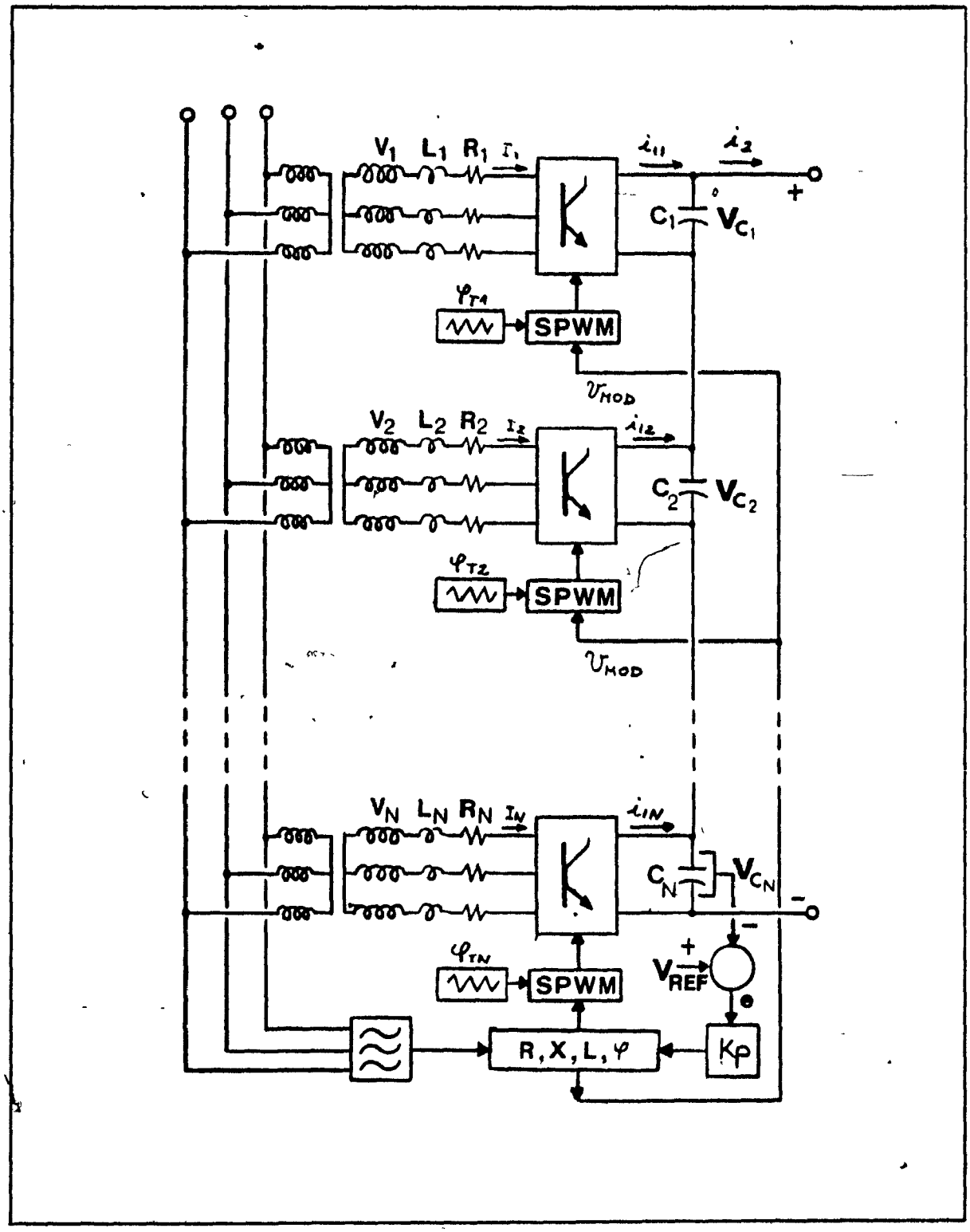


Fig.4.13 Type E: Triangular Carrier Shifted Topology.

Eq.(4.73) is in the polar form, where V_{jk} (Bessel Function) is the magnitude and ϕ_{jk} is the phase angle.

From ref.[68] which gives the derivation, $x=w_T t$ and $y=w_s t$ should be treated as orthogonal variables, although the time t appears to be common. Thus, when the carrier phase is shifted by an angle δ, the Fourier Series component becomes:

$$v_{jk}^{\delta}(t) = V_{jk}\cdot\sin[j(w_T t+\delta) + kw_s t + \phi_{jk})] \qquad (4.74)$$

When there are N identical rectifier units whose triangular carriers are each phase shifted by

$$\delta_n = \frac{2\pi n}{N} \qquad (n=1,2..,N) \qquad (4.75)$$

then the composite Fourier Series component of the N rectifiers is:

$$S_{jk} = V_{jk}\cdot\sum_n \sin(jw_T t + kw_s t + \phi_{jk} + j\frac{2\pi n}{N}) \qquad (4.76)$$

From the trigonometric identity,

$$\sum_n \sin(\xi + j\frac{2\pi n}{N}) = \begin{cases} 0 & \text{for } j \neq NL \quad (L=1,2,3...) \\ N\cdot\sin\xi & \text{for } j = NL \quad (L=1,2,3...) \end{cases} \qquad (4.77)$$

When the ξ term in eq.(4.77) is defined as

$$\xi = jw_T t + kw_s t + \phi_{jk} \qquad (4.78)$$

it can be concluded that all Fourier Series harmonics are eliminated, except those associated with j=NL and k in

$$v_{NL,k} = V_{NL,k}\cdot\sin(NL\omega_T t + k\omega_s t + \phi_{NL,k}) \qquad (4.79)$$

$$(L=1,2..)\ (k=\pm1,\pm2,..)$$

4.6.2 Stability Analysis.

The stability analysis developed in Section 4.4.1 is based on fundamental power and neglects harmonic power. As a result, it can be applied for the Type E when the switching frequency of this topology is high enough. Type E reduces overall harmonics but those of individual modules can be large if we lower the switching frequency. We have not analyzed the effect of harmonics in the stability of Type E configuration.

4.7 Subtopologies.

Types A to E topologies, which have already been discussed, can behave differently by making slight changes in their electrical structure. Only one is mentioned here: Type E1, which is a modification of the Shifted Triangular Carrier configuration.

The Type E1 or Total Voltage Control topology can be considered as a subtopology of the Type E configuration, because they only differ in the dc voltage sensing procedure. The total dc voltage, instead of just the Master voltage, is measured. The drawback of this procedure is that a high voltage sensor is required. However, the advantages of such a topology are:

i) Master and Slaves disappear; all the converters have the same hierarchy.

ii) Reliability increases, because it does not depend on the reliability of the Master.

iii) In the Type E, a failure in one Slave reduces the output voltage to (N-1)/N. The Type E1 maintains the voltage by increasing the modular voltages automatically.

iv) The modulating signal V_{mod} is less distorted than the one from the Type E, because it comes from the total dc voltage, whose harmonics have been reduced by the shifted triangular carrier.

No attempt has been made to analyze Type E1 mathematically. However, simulations have shown that it is stable under both inverter and rectifier operation.

Besides the possibility of implementing subtopologies, there is also the alternative of combining topologies in order to overcome stability problems. Type BA configuration for example, (B under rectifier mode and A under inverter) avoids the instability problems of Type B under inversion and Type A under rectification for the Slaves.

4.8. High Voltage Back-to-Back Systems.

The stability characteristics of Types C, D and E permit the implementation of High Voltage Back-to-Back systems like the one using Type C shown in Figure 4.14.

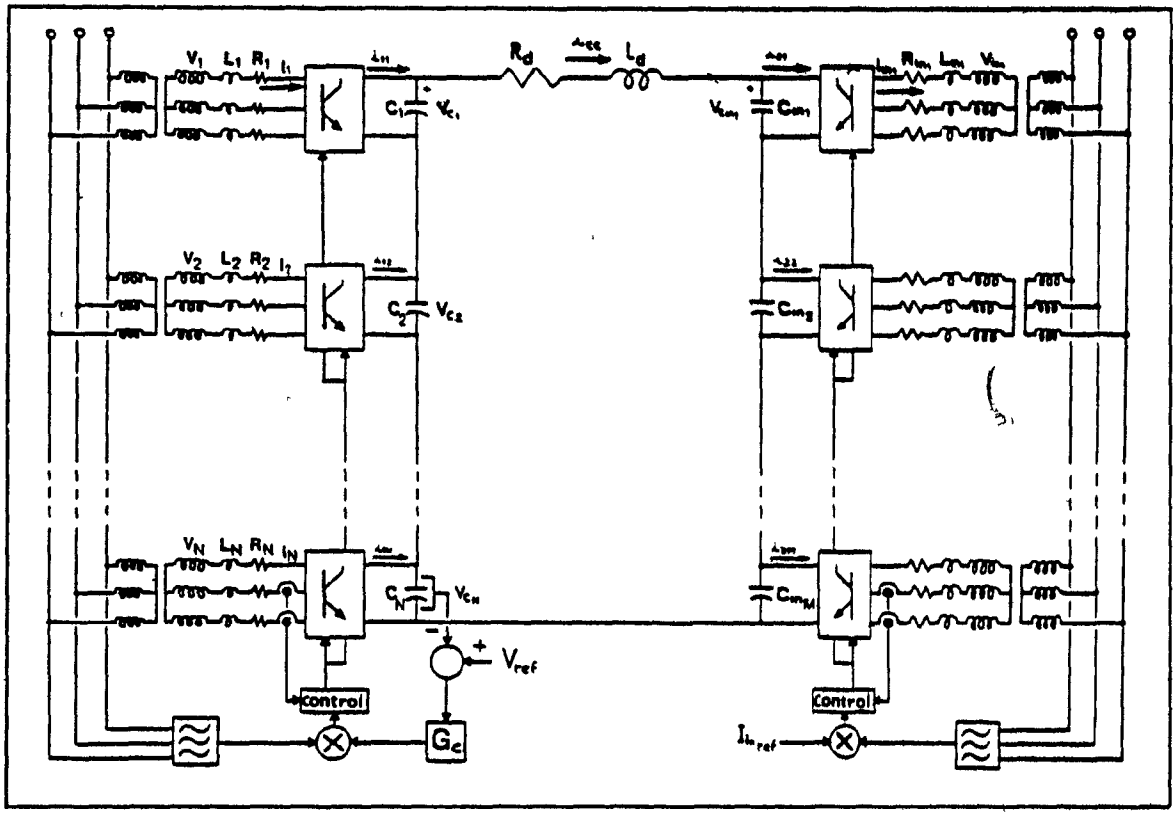


Fig.4.14 Back-to-Back System.

The Back-to-Back system allows either the interconnection of asynchronized power systems or with different frequency of operation. The multiterminal configuration with a common dc bus is also realizable: one terminal controls the dc voltage and the others control the power flow at constant power factor.

In the two-terminal system of Figure 4.14, the dc voltage is controlled by the left-hand terminal. The right-hand terminal controls the power flow by changing the magnitude of the sinusoidal current template 'Iin_{ref}' shown in the Figure 4.14.

4.9 Digital Simulations and Experimental Results.

The mathematical analyses that have been developed in this chapter have shown excellent agreement with the digital simulations and the experimental work.

As it was already explained in section 3.6, the Valve-by-Valve Digital Simulation Program is based on treating each rectifier bridge as a piece-wise circuit problem, in which the ON-OFF states of each of the six power switches of each rectifier give rise to the eight possible circuit states discussed in the Appendix A.

In addition to Valve-by-Valve Simulation, Mathematical Simulation has also been used and has proven to be a reliable tool as well. The Mathematical Simulation solves numerically the system of differential equations expressed in the d-q frame of Section 4.4.1 by the digital computer. The very close agreement between the Mathematical Simulation and the Valve-by-Valve Simulation is another good justification of the correctness of the mathematical models and the assumption that high harmonic power quantities can be neglected. To avoid redundancy, only the results from Valve-by-Valve Simulations are shown here.

The experimental work was realized with the following ratings: supply voltage V_n=40 V; reference dc voltage V_{REF}=120 V; proportional controller gain Kp=3 A/V; reactance per phase X_n=2.5 Ohms and resistance per phase R_n≅1 Ohm. Higher ratings were obtained with the Valve-by-Valve Digital Simulations.

4.9.1 Type A: Independent Local Control.

In the Type A configuration, there is no Master rectifier and hence, all the converters have the same hierarchy. Each modular unit is autonomous and so every one has to satisfy rels.(4.11) and (4.12). The simulation in Figure 4.15 shows what happens when two rectifiers connected in series Type A feed a dc load whose current demand i_2 changes from 0 to -100 and then to +100 A. In this example, the first rectifier does not have enough dc capacitance to keep the module stable and it collapses when the dc current becomes positive. The rectifier has violated rel.(4.11). It can be noted that the system works well in the inverter mode because rel.(4.11) is applicable for rectifier operation only.

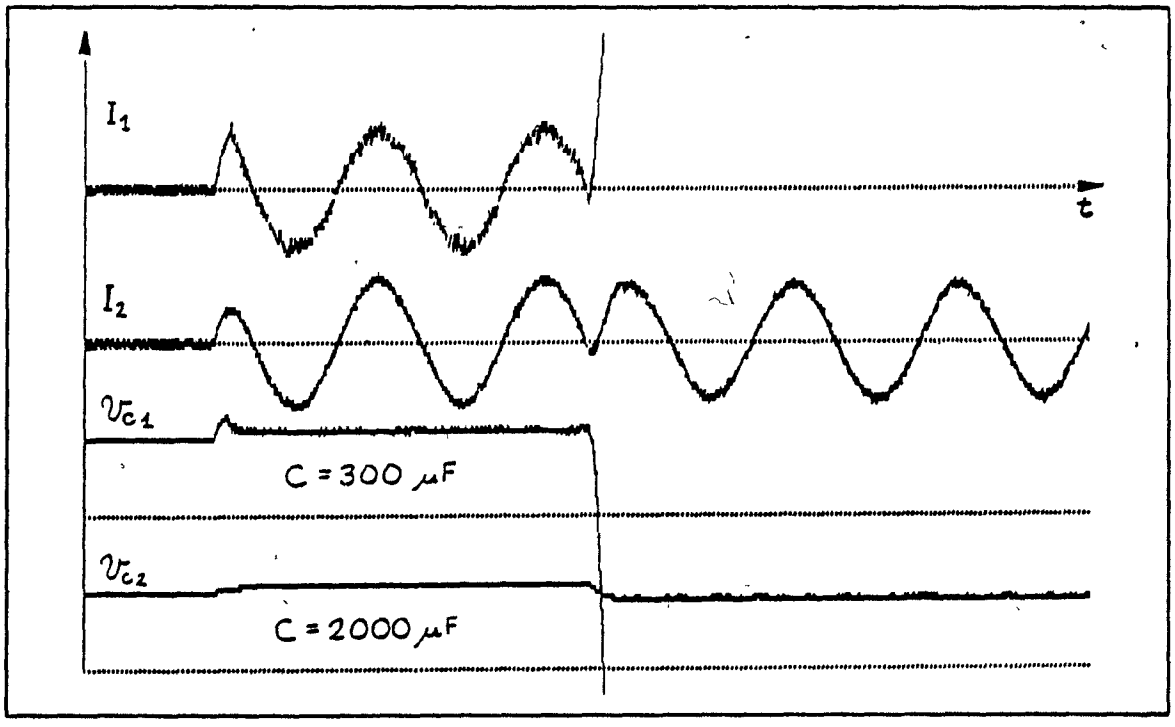


Fig.4.15 Type A Simulation: rectifier 1 collapses because its dc capacitor is too small.

The ratings and parameters of this simulation are: V_n=220 V ac; V_{REF}=660 V dc; Kp=2 A/V; X_n=0.4 Ohm and R_n=0.1 Ohm. The dc capacitors are C_1=300 uF and C_2=2000 uF.

Experiments with Type A configuration were not performed.

4.9.2 Type B: Common Current Reference.

In the Type B configuration, the Slaves are independent of relation (4.11) and so they can use small dc capacitors. Figure 4.16 shows a simulation with the same parameters as Figure 4.15, for three series connected Type B rectifiers. The dc capacitors in this oscillogram are: C_1=100 uF, C_2=200 uF and C_3(Master)=2000 uF. It can be seen that the slaves remain stable even with these small dc capacitors as was predicted by the mathematical analysis. As this system is unstable under inverter mode, the simulation only shows the step response of the rectifier operation from i_2=0 to +100 A dc.

An experimental oscillogram for the Type B is shown in Figure 4.17. The perturbation is a change in the load current i_2 from 0 to 7 A dc. The dc voltages and the input currents are displayed. It can be noted that the Slave is stable and that its dc voltage follows the Master dc voltage variations. The dc capacitors are C_1=C_2=12000 uF. The dc voltage drop is V_{REF}-Vc=3 V. The input currents I_1 and I_2 (Master Rectifier) are nine amperes each. Because the theory predicts that the inverter mode is unstable, experiments under inverter mode were not performed.

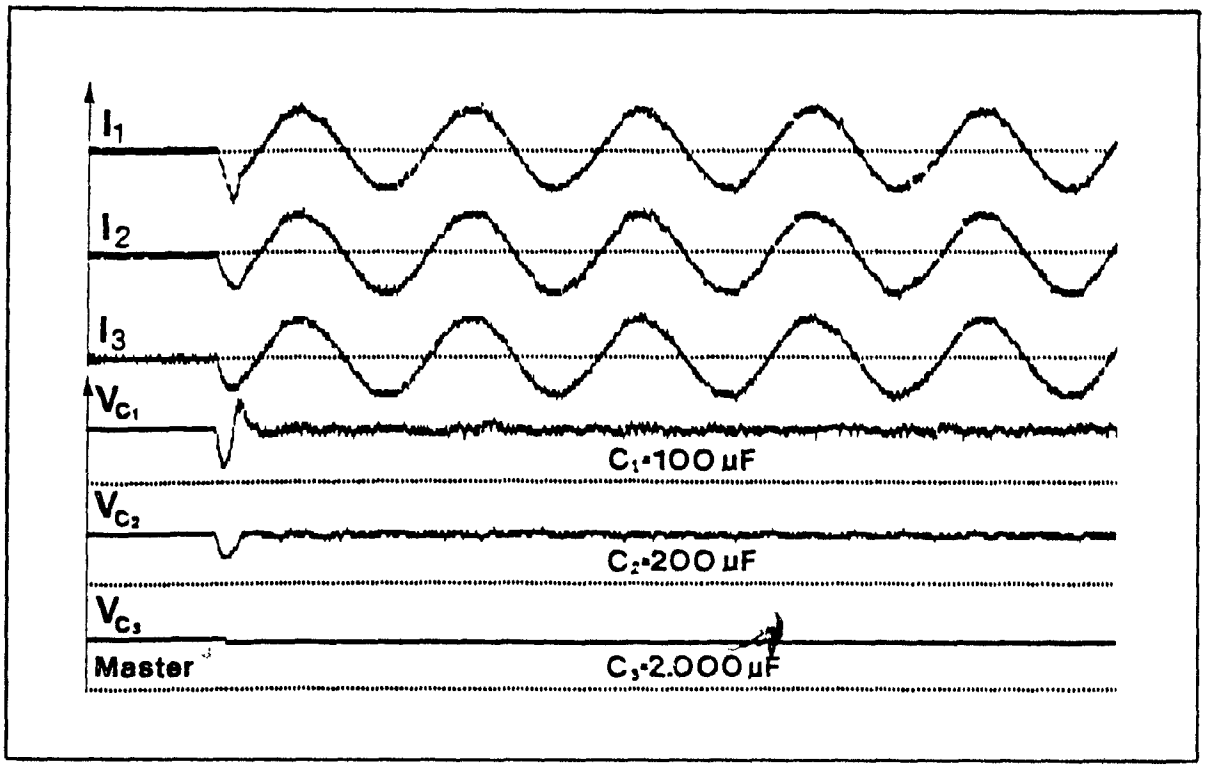


Fig.4.16 Type B Simulation. Slaves stability does not depend on the size of the dc capacitor.

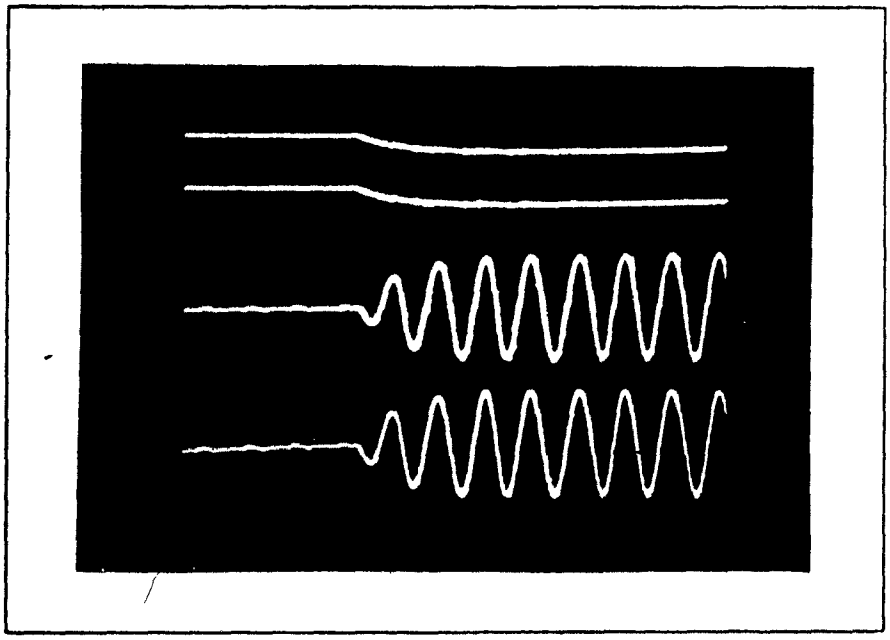


Fig.4.17 Type B: Experimental Oscillogram for a Step Response
a) Slave voltage v_{c1}; b) Master voltage v_{c2};
d) Slave Current I_1; d) Master current I_2.

The analysis developed for the Type B configuration showed that this topology is unstable under inversion. Figure 4.18 clearly demonstrates this fact. The Master, as well as the Slaves use the same dc capacitor C=1000 uF, but despite the increase in the Slaves dc capacitors with respect to Figure 4.16, they do not sustain the dc voltage. The Slave voltages begin to increase asymptotically following a constant slope $m=i_2/C$.

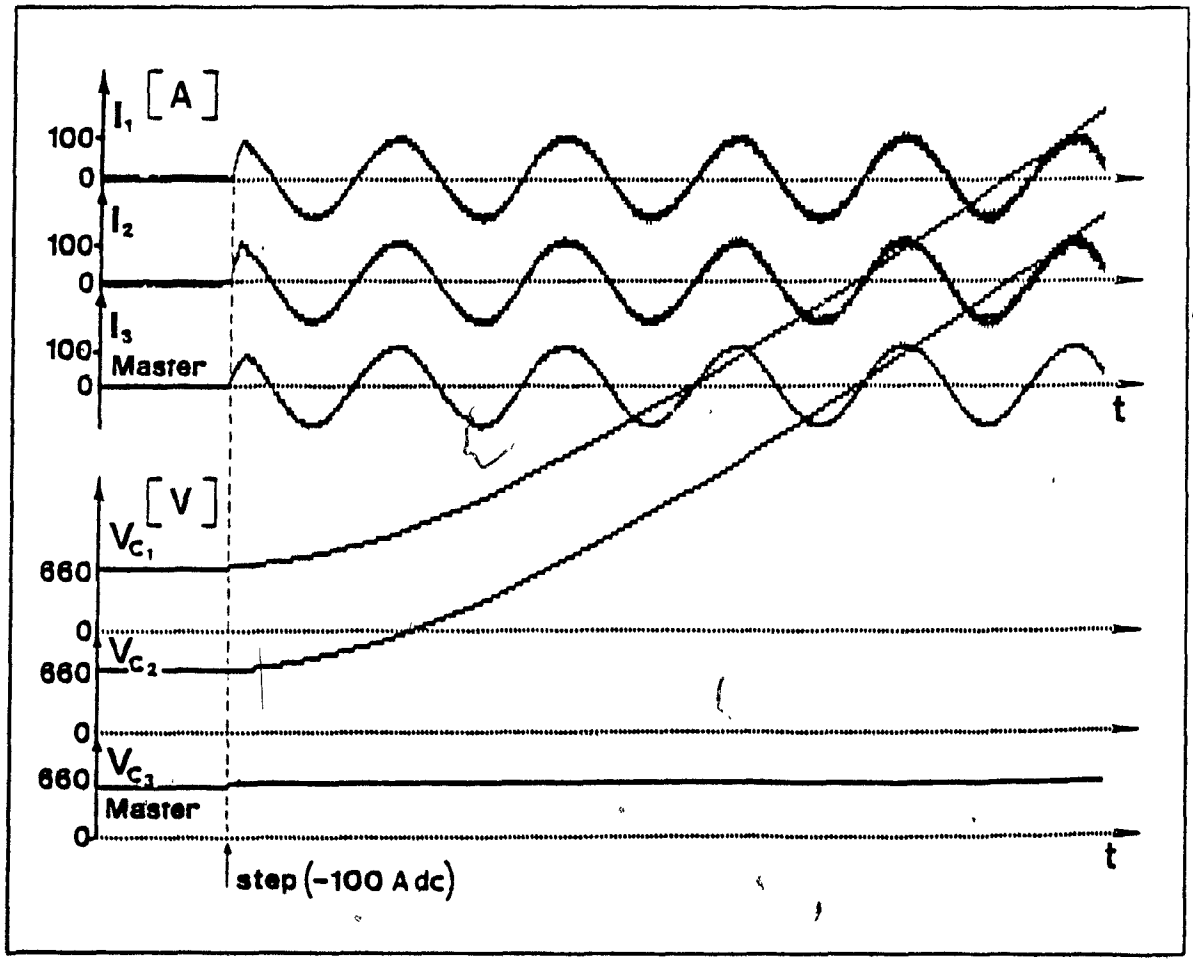


Fig.4.18 Type B Inverter Simulation. The Slaves do not sustain the dc voltage and the system collapses.

4.9.3 Type C: Common Switching Control.

As it was shown in the analysis of Type C, this configuration is stable in both rectifier and inverter operation. Figure 4.19 shows a simulated oscillogram under the same conditions as Figure 4.15: C_1=300 uF and C_2(Master)=2000 uF. It can be seen that an oscillating transient perturbs the behaviour of the Slave and then, more capacitance is required to reduce this problem. In Figure 4.20, the Slave capacitor C_1 has been increased to 500 uF and the oscillations become less severe.

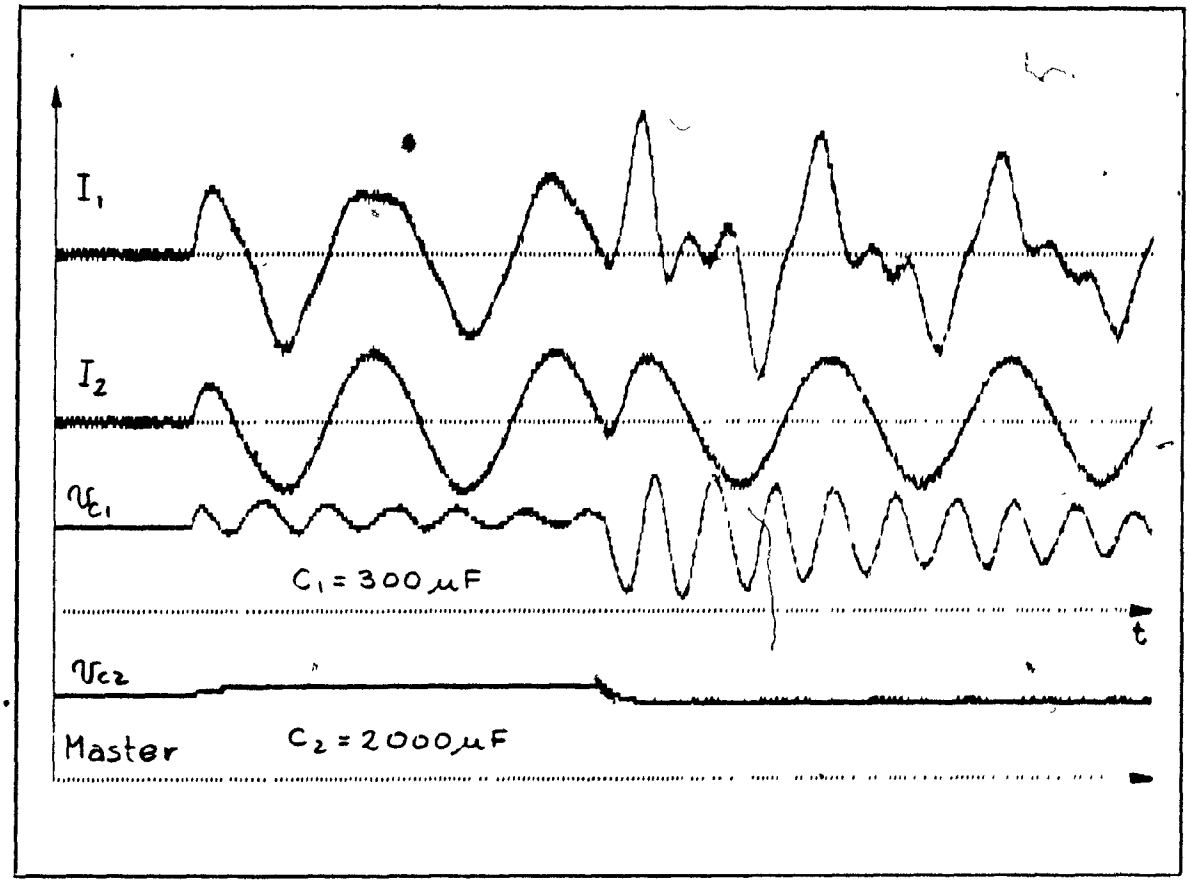


Fig.4.19 Type C Simulation. Transient Response from a Change in the Load Current i_2 from 0 to -100 to +100 A dc.

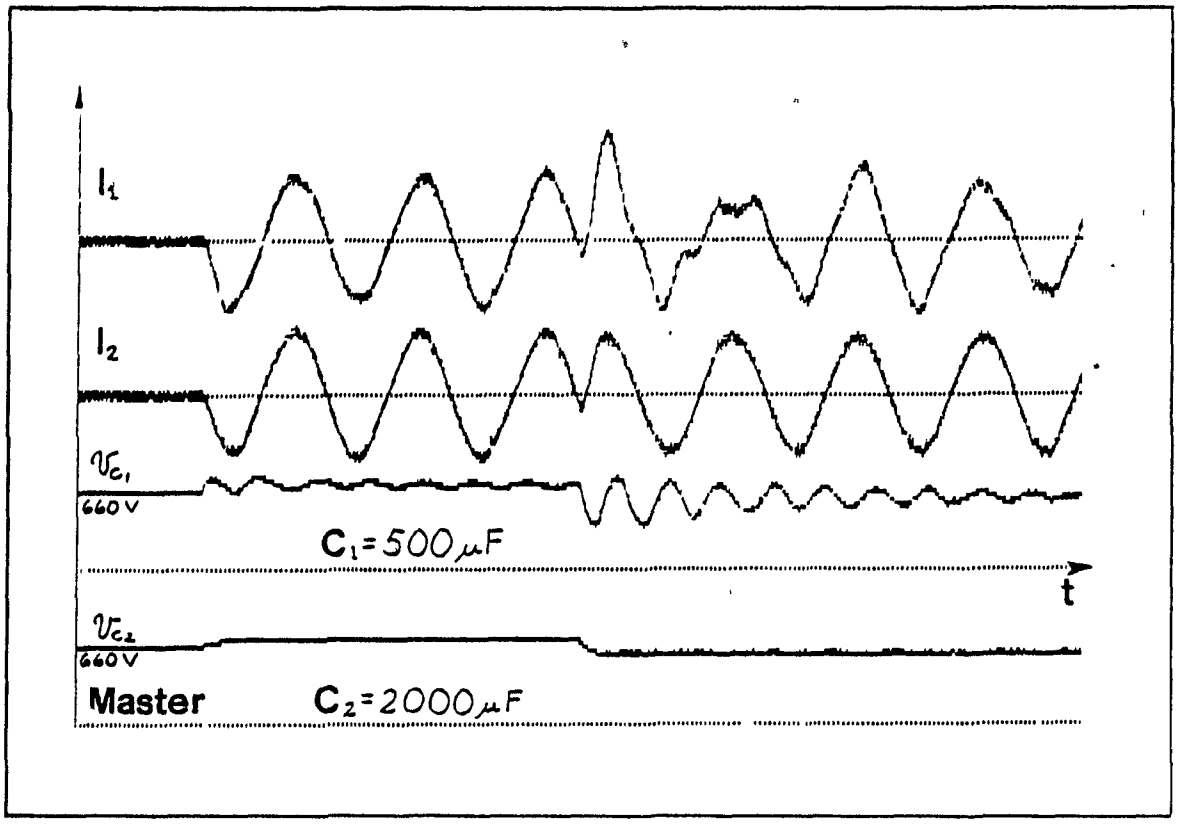


Fig.4.20 Type C Simulation. The Slave dc capacitor has been increased from 300 uF to 500 uF to reduce the oscillations.

To avoid the transient problem of Figures 4.19 and 4.20, the Slaves should use the same capacitor as the Master but this increases the cost. Because the PI control permits one to reduce the proportional gain, it offers a good solution to the capacitor size. Figure 4.21 shows a simulated oscillogram of a Type C configuration with PI control. The proportional gain has been reduced from Kp=2 to Kp=0.6, allowing (accordingly to relation 4.29) the same proportional reduction in the Master capacitor from 2000 uF to 600 uF. Using the same capacitor value in the Slave, the unwanted oscillations of Figures 4.19 and 4.20 disappear. The integral gain is K_I=300.

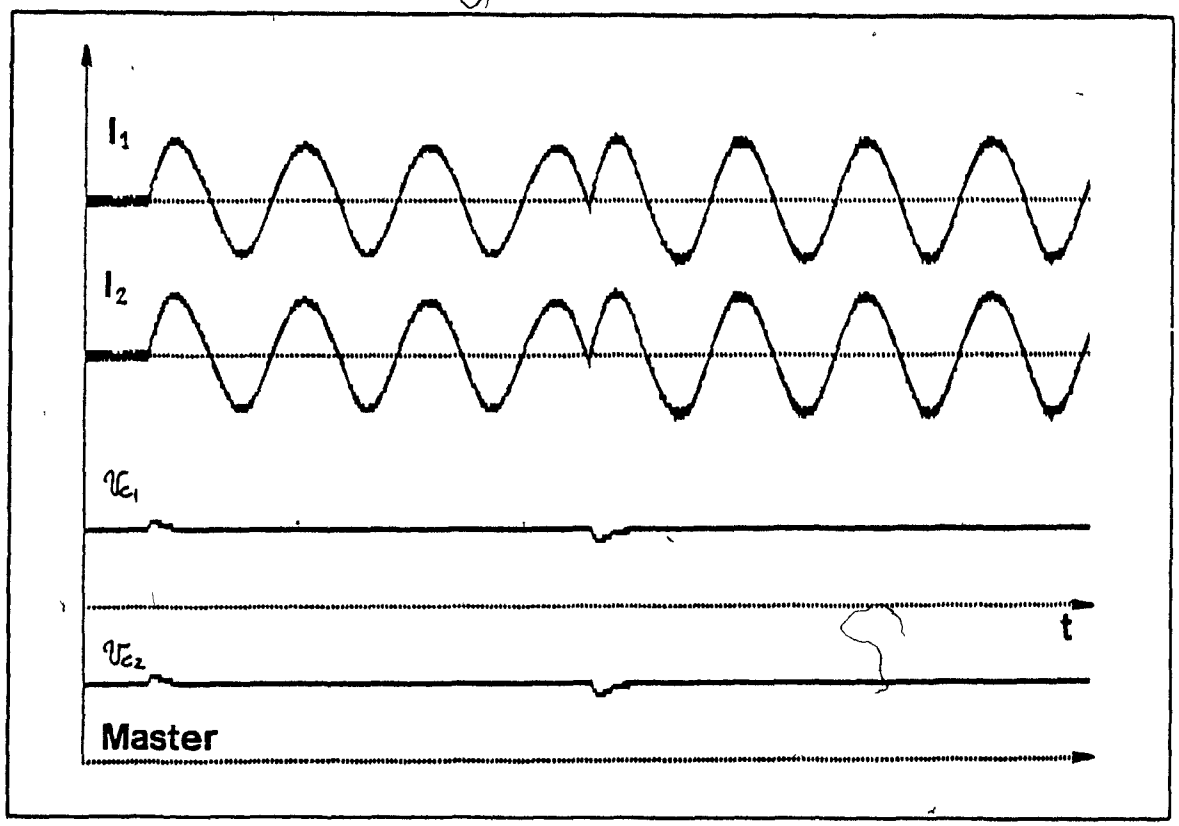


Fig.4.21 Type C Simulation with PI Control. C_1=C_2=600 uF.

A large number of experiments were performed using the Type C configuration. Figure 4.22 shows the Common Switching Control strategy driving each converter with the same pattern. The Slave and Master currents are almost identical. As a consequence, the total input current will have proportionally the same waveform, this being the drawback of this configuration.

The experiment in Figure 4.23 demonstrates that the Type C configuration has power reversal capability. The load current changes from -5 to +5 A dc and the dc capacitors are C_1=C_2=6000 uF.

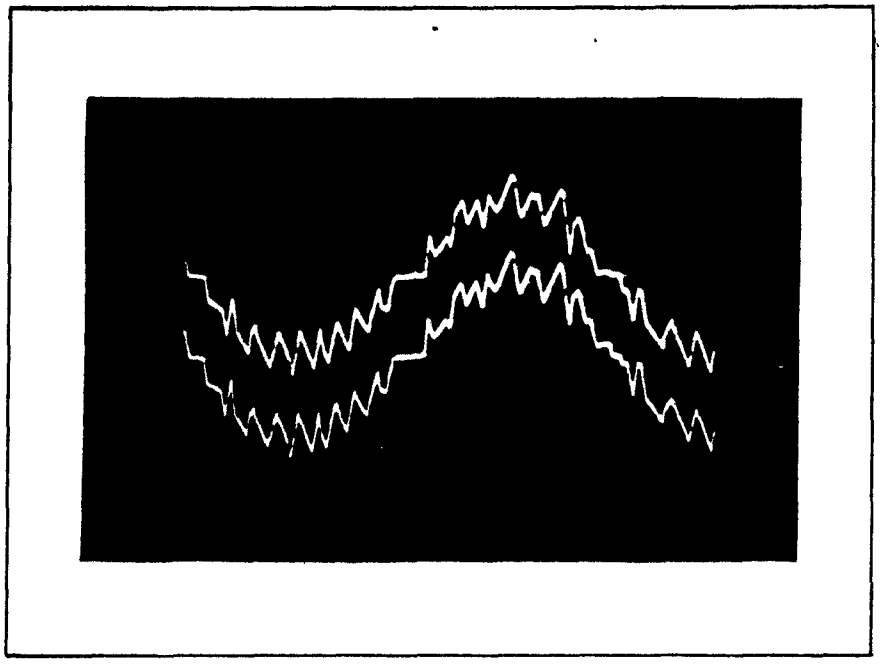


Fig.4.22 The Common Switching Control Strategy Gives Exactly the Same Pattern to Each Rectifier Current.
a) Slave current; b) Master current.

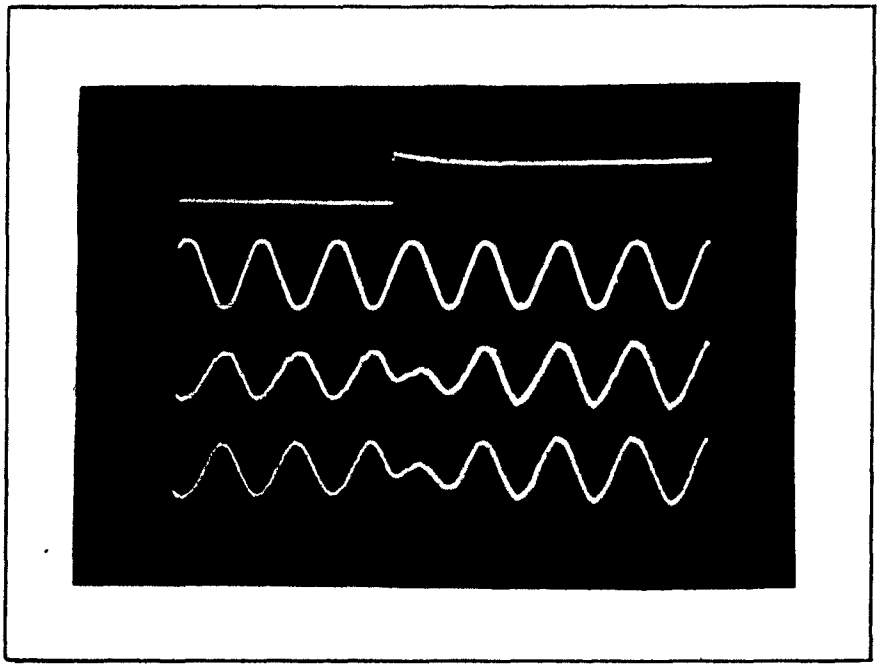


Fig.4.23 Experimental Verification of the Type C Power Reversal Capability.
a) load current i_2; b) supply Master voltage V_2
c) Slave current I_1; d) Master current I_2

The valve-by-valve simulations of Figures 4.19 and 4.20 showed that Master and Slaves behave differently during transients when $C_n \neq C_N$. The experimental oscillogram of Figure 4.24 shows this fact when C_1=950 uF and C_2=6000 uF. Oscillations are not visible because they are damped for the big resistive element R_1=1 Ohm of the rectifier. This oscillogram shows a step response when i_2 goes from 0 to +7 A dc.

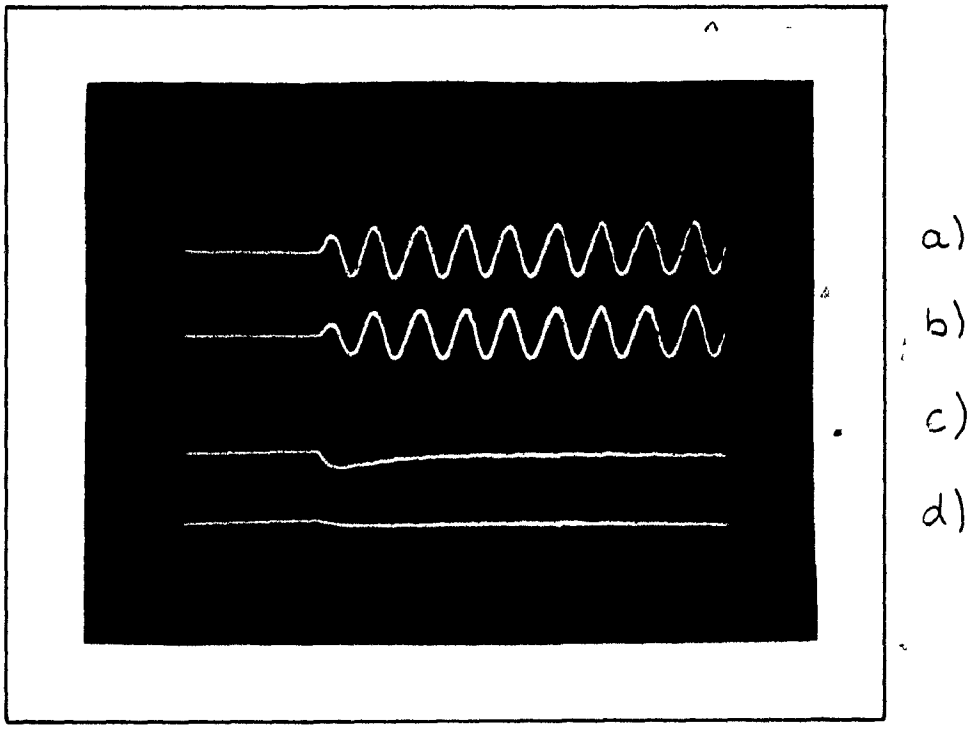


Fig.4.24 Transient Behaviour of Type C when $C_1 \neq C_2$.
a) Slave current I_1
b) Master current I_2
c) Slave dc voltage v_{c1}
d) Master dc voltage v_{c2}

The mathematical analysis also showed that the stability of the Slaves does not depend on the size of the dc capacitor. Figure 4.25 shows the input currents and output dc voltages of an experimental oscillogram, where the Slave capacitor is only C_1=250 uF and C_2(Master)=6000 uF. It can be seen that the ripple in the Slave voltage has become quite big and it begins to distort its input current, but the system remains stable.

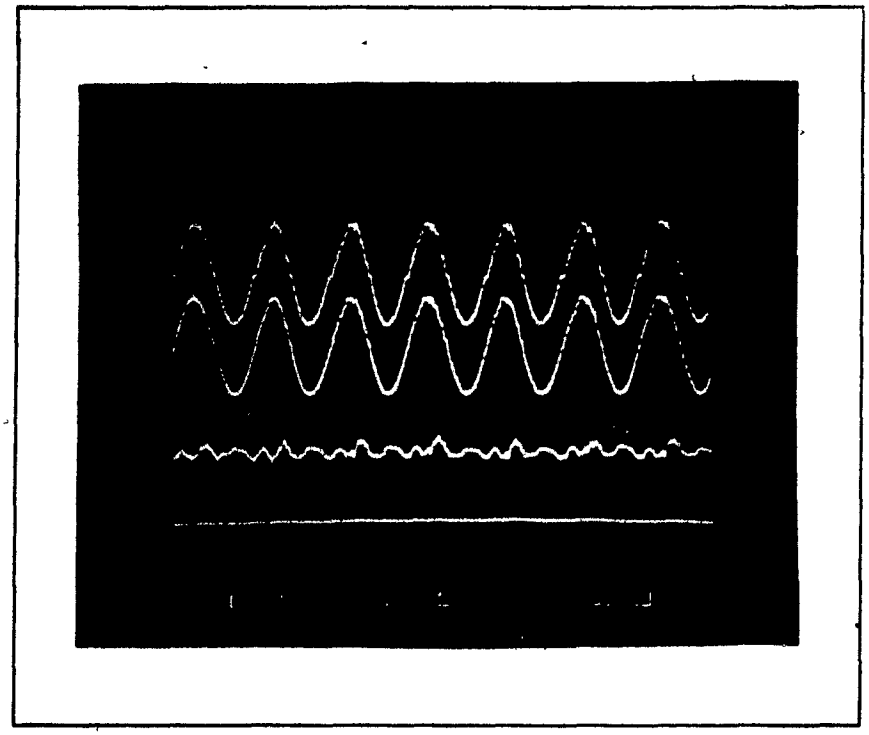


Fig.4.25 Experimental Proof of Slave Stability with Small dc Capacitor.
a) Slave current I_1
b) Master current I_2
c) Slave dc voltage v_{c1}
d) Master dc voltage v_{c2}

4.9.3.1 Pulsating Loads.

Until now all the simulations and experiments have been performed with harmonic-free dc current loads. Practical applications in Power Electronics sometimes require equipment which is able to feed pulsating loads, like a dc Chopper. Figure 4.26 shows a simulation of four series Type C connected rectifiers, with a total dc voltage Vc=1500 V, feeding a Chopper-driven electrical locomotive. The Chopper frequency is f_C=840 Hz and the current starts increasing from 0 to 1200 A dc.

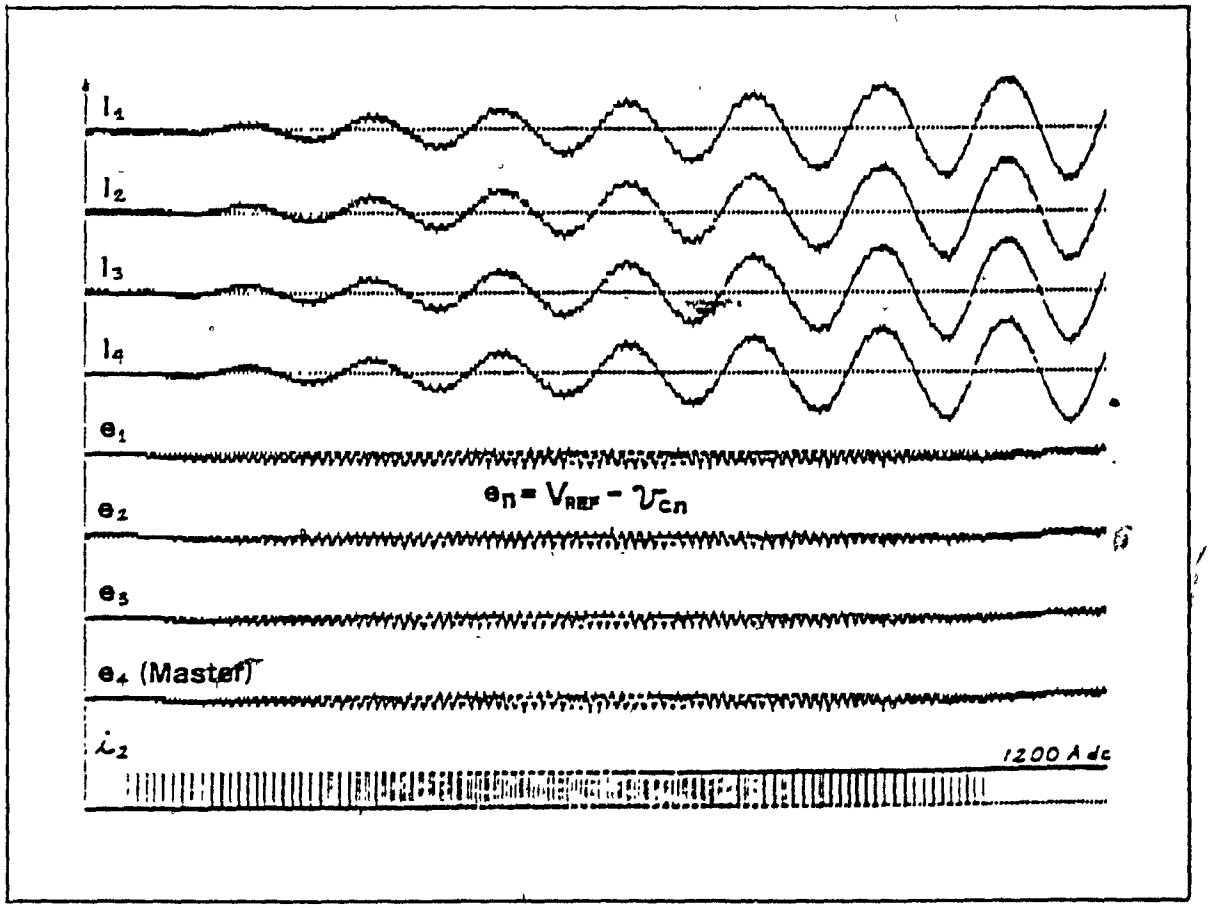


Fig.4.26 Four Type C Rectifiers Feeding a Pulsating Load.

The ratings and parameters of this simulation are: V_n=130 V ac, I_n=1300 A ac, V_{REF}=375 V dc, R_n=0.01 Ohm, X_n=0.05 Ohm, C_n=10000 uF, Kp=3 and K_I=1000. The size of the hysteresis band is h=80 A which gives a maximum switching frequency of of 7.5 kHz. With state-of-the-art power semiconductors, such a rectifier is realizable.,

4.9.4 Type D: Indirect Common Switching Control.

Figure 4.27 shows a step response for a Type D rectifier, with two non-compensated (L_b=0) Indirect Current Controlled rectifiers. The forcing function i_2 changes from 0 to -6 A dc. Because L_b=0, the dc capacitor has to be big to keep the system stable: C_n=18000 uF.

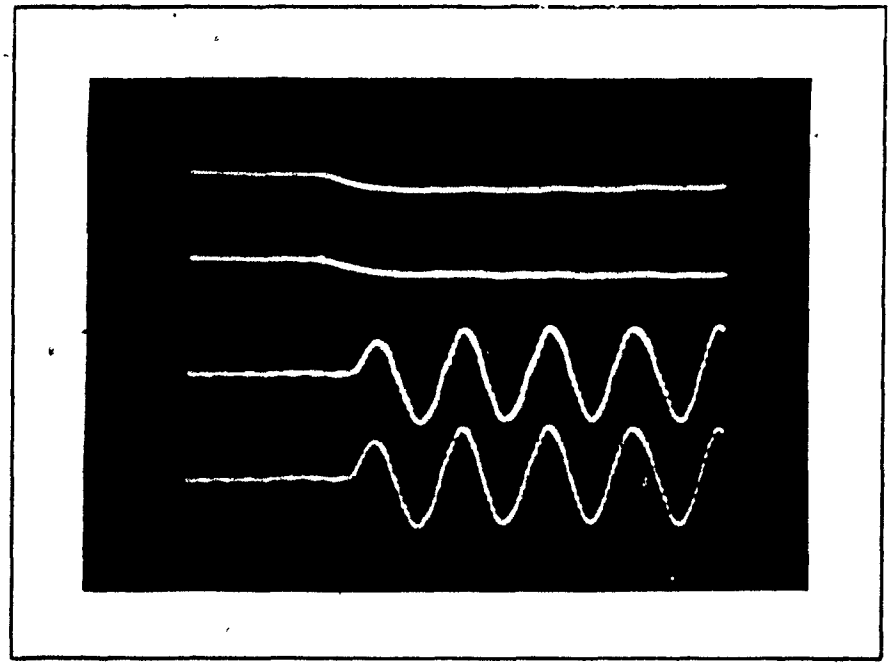


Fig.4.27 Type D Configuration. Transient Response.
a) Slave voltage v_{c1}; b) Master voltage v_{c2}
d) Slave current I_1; d) Master current I_2

4.9.5 Type E: Shifted Triangular Carrier Control.

The Shifted Triangular Carrier topology offers the additional advantage of harmonic elimination, as compared to the other topologies. Figure 4.28 shows an experimental oscillogram of this feature. The two converters are under steady-state and the input current of each rectifier is $I_1=I_2=7$ A dc. The figure shows that the resulting total current is cleaner than its components.

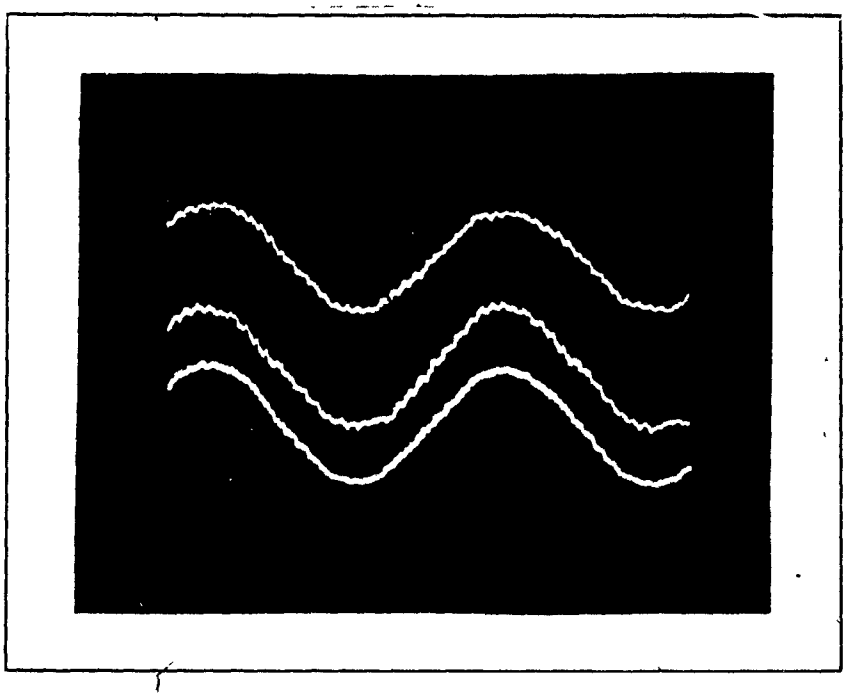


Fig.4.28 Type E Configuration. Experimental Proof of the Harmonic Elimination.
a) Slave current I_1
b) Master current I_2
c) total current I_1+I_2

The more the converters are used, the cleaner the total current is. Figure 4.29 shows a simulation with seven converters in series. The total current is virtually sinusoidal.

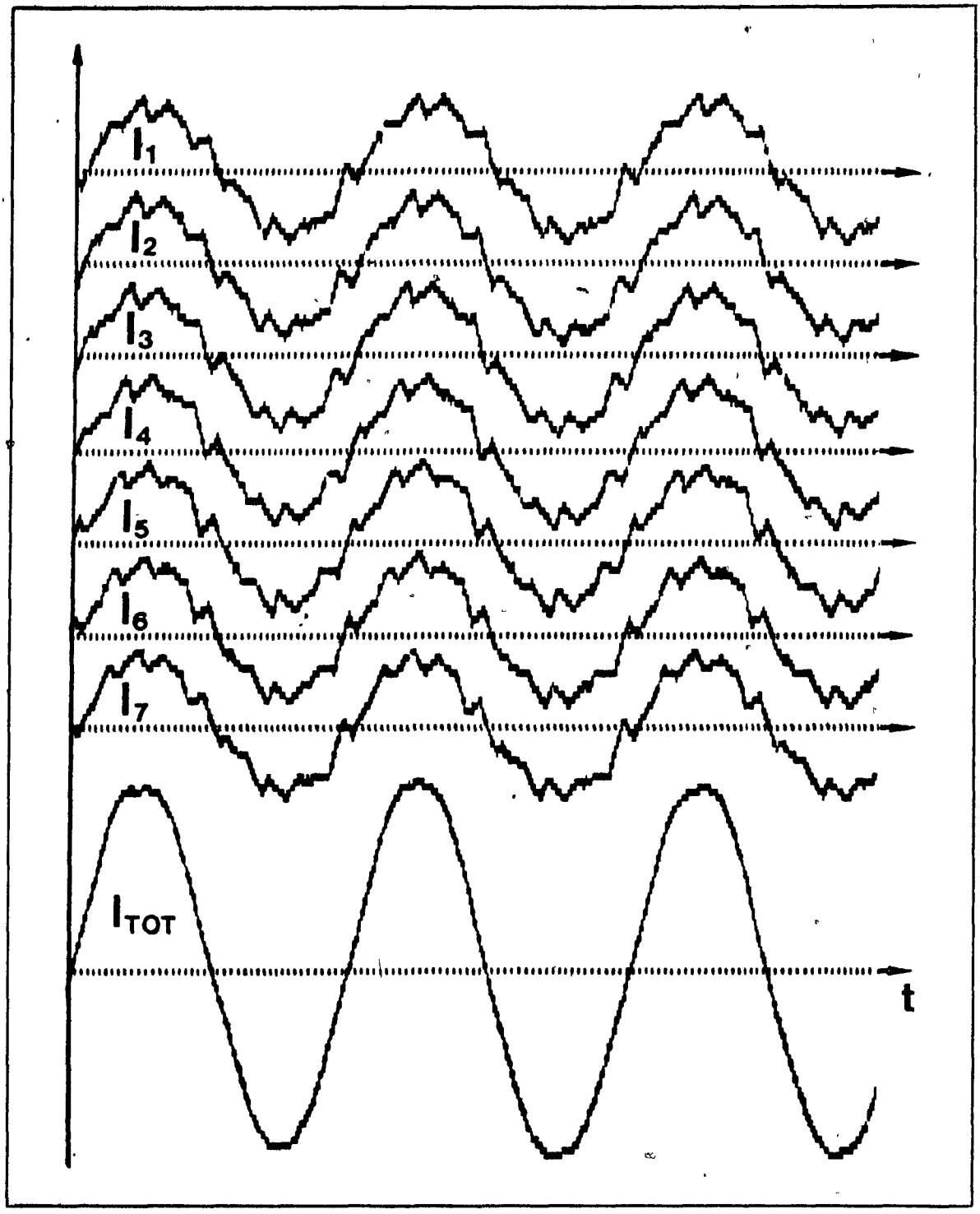


Fig.4.29 Current Waveforms from Digital Simulation of 7 SPWM Rectifiers whose Triangular Carriers are Phase-Shifted by $\delta=2\pi/7$. The Carrier Frequency is 600 Hz.

The simulation of Figure 4.30 shows two different aspects: the transient response under a negative current step from 0 to -8 A dc and the quality of the total current for a carrier frequency as low as 300 Hz. The system only has 5 converters in series. Only the first Slave and the total current are displayed in this oscillogram. The ratings of this simulated system are the same as that of the experimental device.

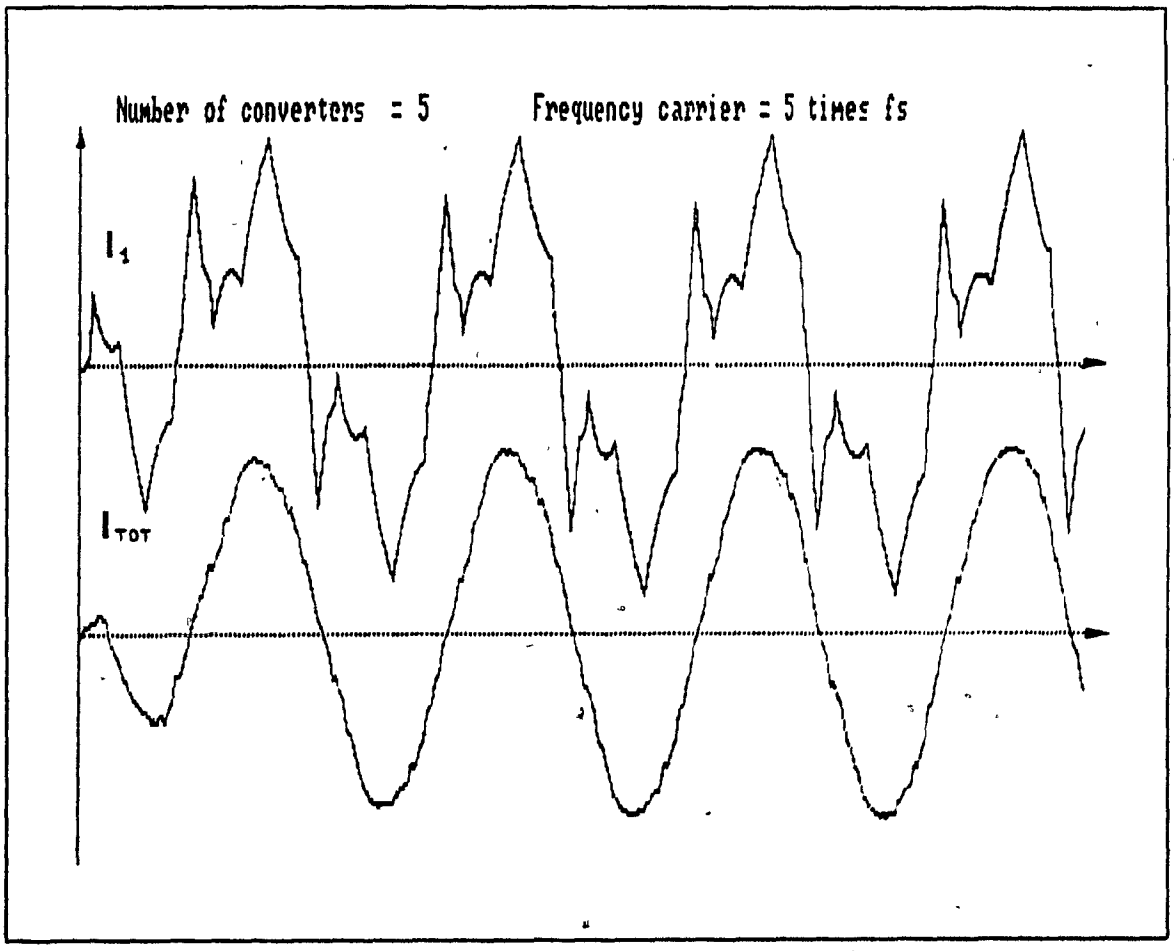


Fig.4.30 Type E Oscillogram with Five Converters in Series and Low Switching Frequency. Carrier Frequency f_T=300 Hz.

4.9.6 Back-to-Back Systems.

Figure 4.31 shows the simulation of a two terminal Back-to-Back system like the one shown in Figure 4.14. Each terminal has two series connected Type C rectifiers. The power rating of the system is 260 kVA and it operates at unity power factor in the both terminals. The system is subject to a very severe situation: a step in the reference current of the right-hand terminal from 0 to 1000 A and then from 1000 to -1000 A ac.

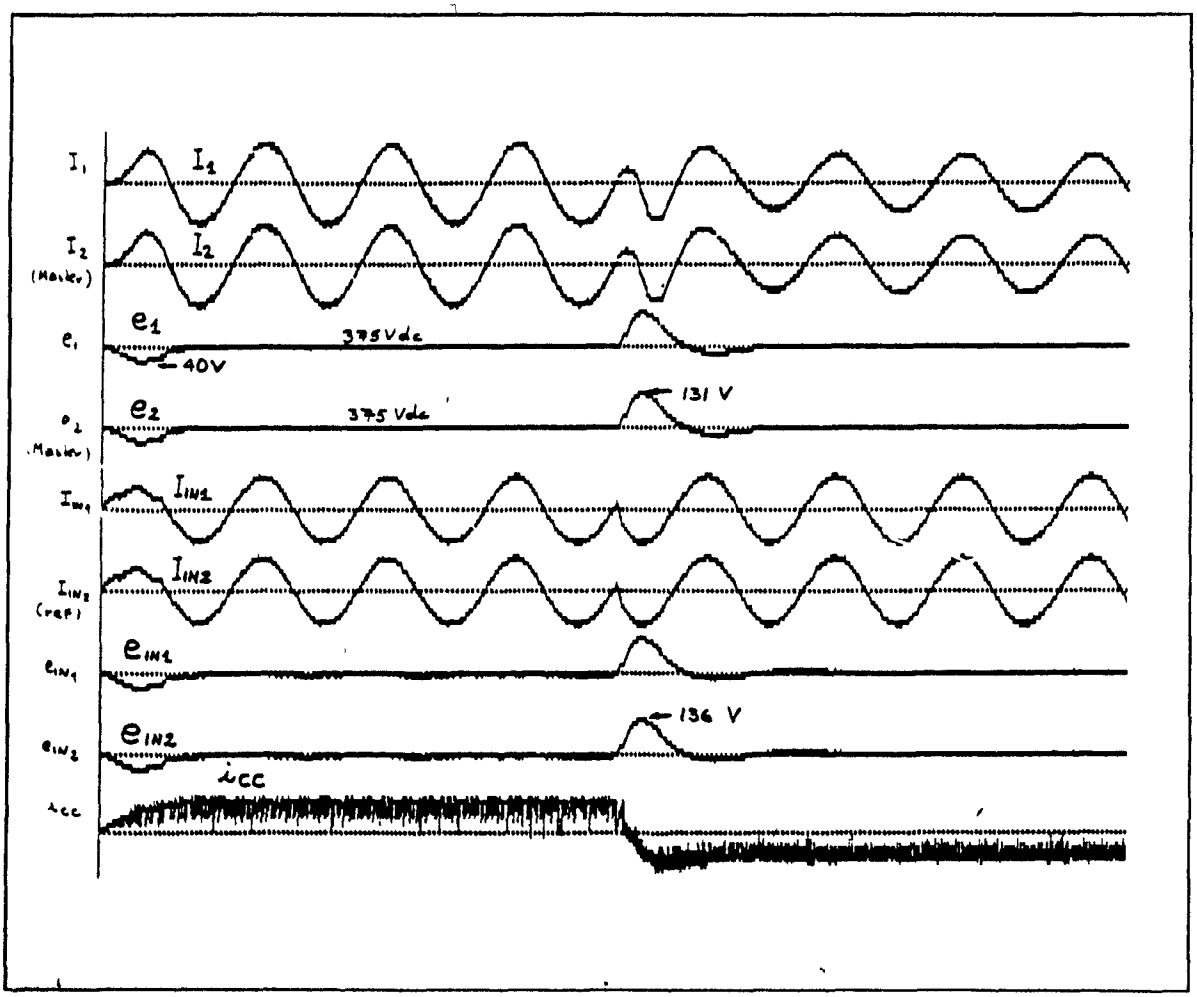


Fig.4.31 Back-to-Back System Simulation.

The oscillogram shows: the input currents of the voltage regulator terminal, I_1 and I_2; the error in their dc voltages, e_1 and e_2; the output currents of the other terminal, I_{IN1} and I_{IN2}; their dc voltage errors, e_{IN1} and e_{IN2}; and the dc link current i_{CC}.

It can be seen that the system has to withstand overvoltages in the dc link of up to 30%, but it overcomes the severe transient.

Other parameters for this simulation are: $C_n=C_{INn}=15$ mF, $V_n=V_{INn}=130$ volts ac, $V_{REF}=375$ volts dc, $R_n=R_{INn}=0.01$ ohms, $L_n=L_{INn}=0.15$ mH, Kp=8 and $K_I=4000$.

4.10 Summary.

Different topologies for series connected PWM rectifiers have been analyzed. Mathematical analyses and computer simulations have been verified with experimental results.

One of the most important findings in this chapter, the quite simple Type C configuration, combined with the Indirect Current Control Method, has made it possible to conceive the optimal Type E configuration, which only needs one voltage sensor to control the overall system and possesses the property of harmonic elimination. This last feature allows one to use very low switching frequency, thus reducing the switching losses and increasing the efficiency of the complete rectifier.

Other fields of study opened up by this research, like improved subtopologies, combined topologies, topologies with

different control strategies and high power back-to-back systems are suggestions for further and detailed investigation.

The next chapter, Chapter V, analyzes the power rectifiers connected in parallel. Similar development carried out in this chapter is followed in the next one.

CHAPTER V

PARALLEL CONNECTED RECTIFIERS

5.1 Introduction.

In Chapter II, the principles of operation and analyses of the Direct Current Control Method were described. Chapter III developed the Indirect Current Control Method. Finally, Chapter IV analyzed different topologies for series-connected PWM rectifiers, using the two current control methods discussed in Chapters II and III.

This chapter presents the analytical and experimental work on parallel-connected PWM rectifiers, using both the Direct and Indirect Current Control Methods. The parallel connection becomes necessary when the required rated current of the converters is beyond the ratings of commercially available power electronic switches. The parallel-connected modules also represent an alternative to the use of individual components connected in parallel in a simple rectifier.

Because of the limited time set to the completion of the Thesis, the analyses, as well as the experiments, are not as detailed as in the previous chapter. Some topologies are briefly mentioned but are not discussed in detail. There is a scope for further investigation by future researchers.

The same number of topologies as in the previous chapter are introduced: three for Direct Current Control and two for Indirect Current Control.

A. Direct Current Control.

i) Type A: Independent Local Control

ii) Type B: Common Current Reference Control

iii) Type C: Common Switching Control

B. Indirect Current Control.

i) Type D: Indirect Common Switching Control

ii) Type E: Shifted Triangular Carrier Control.

As in the previous chapter, conditions of stability, current and voltage sharing, and the parameter sensitivity are analyzed for each topology. The mathematical analyses are verified experimentally, by using two parallel-connected PWM rectifiers.

Unlike the series-connected rectifiers, the parallel connection has a common dc bus for all the converters and so requires only one voltage sensor for all the topologies. A common input transformer may also be used in parallel topologies but in most of the cases this does not offer important advantages. A single transformer reduces the reliability of the system and requires 3N-1 current sensors instead of 2N. The chapter assumes the parallel connection with independent transformers.

5.2 Type A: Independent Local Control.

In this configuration, each modular unit is autonomous in that each one has its inner hysteresis current control

feedback loop requiring at least two current sensors. Figure 5.1 shows the topology for the parallel-connected Type A rectifiers.

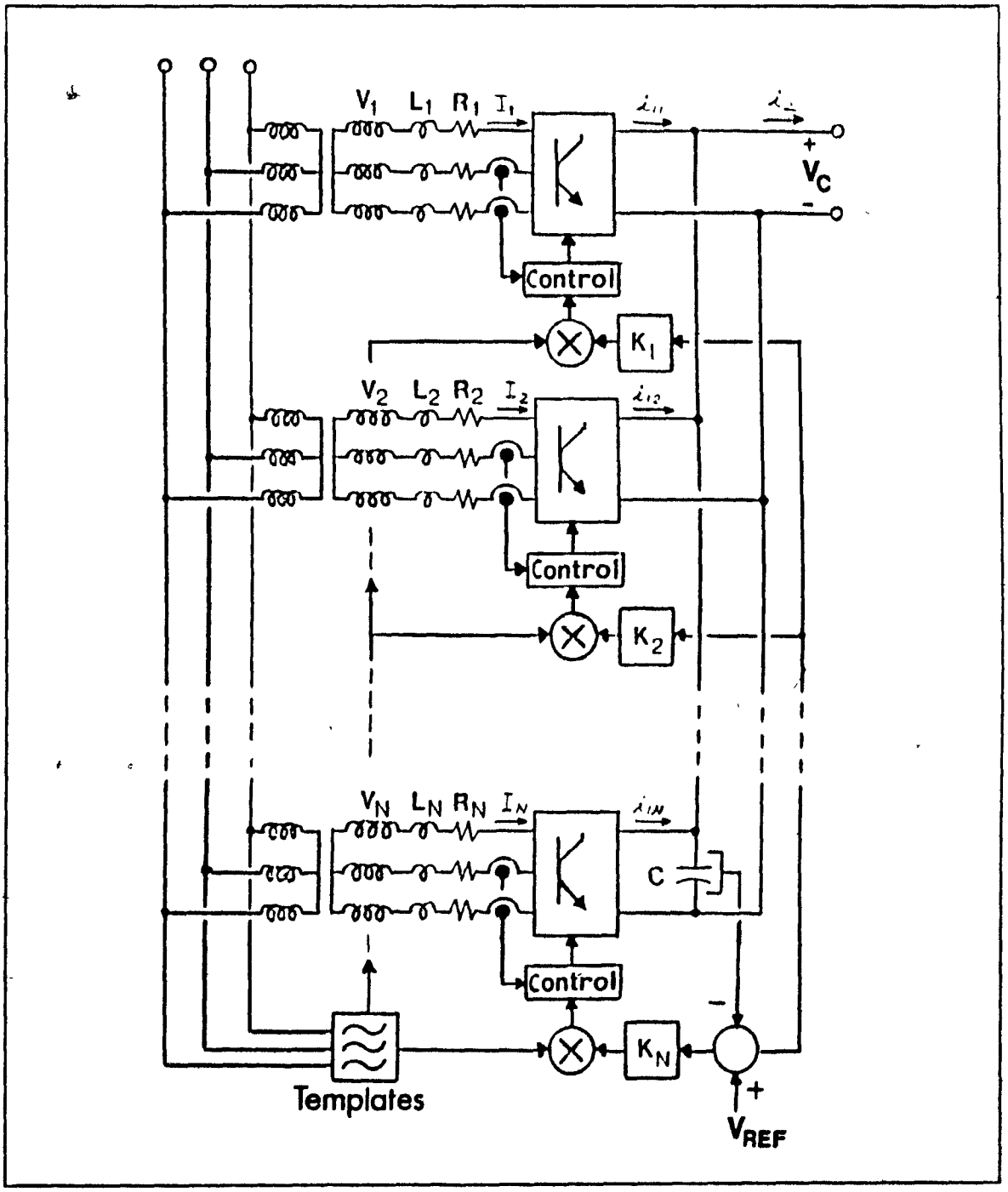


Fig.5.1 Type A: Independent Local Control Topology.

5.2.1 Mathematical Model and Stability Analysis.

In the parallel configuration the dc link output voltage v_{cn} is common so that:

$$v_{cn} = v_c \qquad (n=1,2..,N) \qquad (5.1)$$

Because of eq.(5.1), the dynamic Power Balance Equation is:

$$v_c \cdot C \cdot \frac{dv_c}{dt} + P_2 = 3 \cdot \sum_n (V_n I_n - R_n I_n^2 - \frac{1}{2} \cdot \frac{d}{dt} L_n I_n^2) \qquad (5.2)$$

where P_2 is the total dc power load. Assuming that the voltage regulator is a proportional controller whose transfer gain is K_n, the control law of the rms ac phase current is:

$$I_n = K_n \cdot (V_{REF} - v_c) \qquad (n=1,2..,N) \qquad (5.3)$$

where V_{REF} is the reference voltage. Substituting eq.(5.3) into (5.2) and applying small signal linearization about the equilibrium voltage Vc, the system linearized dynamic equation is obtained:

$$\frac{d\Delta v_c}{dt} = -\frac{1}{T_e} \Delta v_c \qquad (5.4)$$

where the time constant T_e is:

$$T_e = \frac{C \cdot Vc - 3(V_{REF}-Vc) \cdot \sum_n L_n K_n^2}{3 \cdot \{\sum_n V_n K_n - 2(V_{REF}-Vc) \cdot \sum_n R_n K_n^2\}} \qquad (5.5)$$

For stable operation, T_e has to be positive which requires both the expressions in the numerator and the denominator to be positive.

5.2.2 Input and Output Current Sharing.

The sharing of the input ac currents can be obtained from eq.(5.3). In particular, for the modules n=j and n=k:

$$\frac{I_j}{I_k} = \frac{K_j}{K_k} \tag{5.6}$$

Thus, the input ac current sharing depends on the proportional gains. Making K_n=Kp (n=1,2..,N), the input currents become perfectly balanced.

The sharing of the output currents i_{1n} in the dc link, can be obtained from the steady-state Power Balance Equation

$$i_{1n} \cdot Vc = 3 \cdot (V_n I_n - R_n I_n^2) \qquad (n=1,2..,N) \tag{5.7}$$

Equation (5.7) gives the sharing of the output dc currents between the converters number j and k as:

$$\frac{i_{1j}}{i_{1k}} = \frac{V_j I_j - R_j I_j^2}{V_k I_k - R_k I_k^2} \tag{5.8}$$

Neglecting the value of the resistances and replacing eq.(5.6) into (5.8) yields:

$$\frac{i_{1j}}{i_{1k}} = \frac{V_j K_j}{V_k K_k} \tag{5.9}$$

Thus, the balanced condition in the both input and output currents requires that V_j=V_k and K_j=K_k for all j, k into n. As X_n does not appear in the equations, the parallel Type A configuration is insensitive to X_n variations.

5.3 Type B: Common Current Reference Control.

It can be concluded from eq.(5.6) that when K_n=Kp in the Type A configuration, the current reference becomes the same for all the converters. In such a case, the proportional gain can be reduced to one. This allows the elimination of (N-1) controllers and multipliers from the system. The configuration becomes the Type B or Common Current Reference Control with the following characteristic

$$I_n = I \qquad (n=1,2..,N) \tag{5.10}$$

The Type B configuration is shown in Figure 5.2.

5.3.1 Stability Analysis.

For K_n=Kp, n=1,2..,N, eq.(5.5) becomes

$$T_e = \frac{C \cdot Vc - 3 \cdot Kp^2 (V_{REF}-Vc) \cdot \Sigma_n L_n}{3N \cdot Kp \cdot [\Sigma_n V_n - 2Kp(V_{REF}-Vc) \cdot \Sigma_n R_n} \tag{5.11}$$

with

$$I = Kp(V_{REF} - Vc) \tag{5.12}$$

One gets the first stability condition from the numerator of eq.(5.11) with T_e>0:

$$I < \frac{C \cdot Vc}{3 \cdot Kp \cdot \Sigma_n L_n} \tag{5.13}$$

When L_n=L (n=1,2..,N), it yields:

$$I < \frac{C \cdot Vc}{3N \cdot Kp \cdot L} \tag{5.14}$$

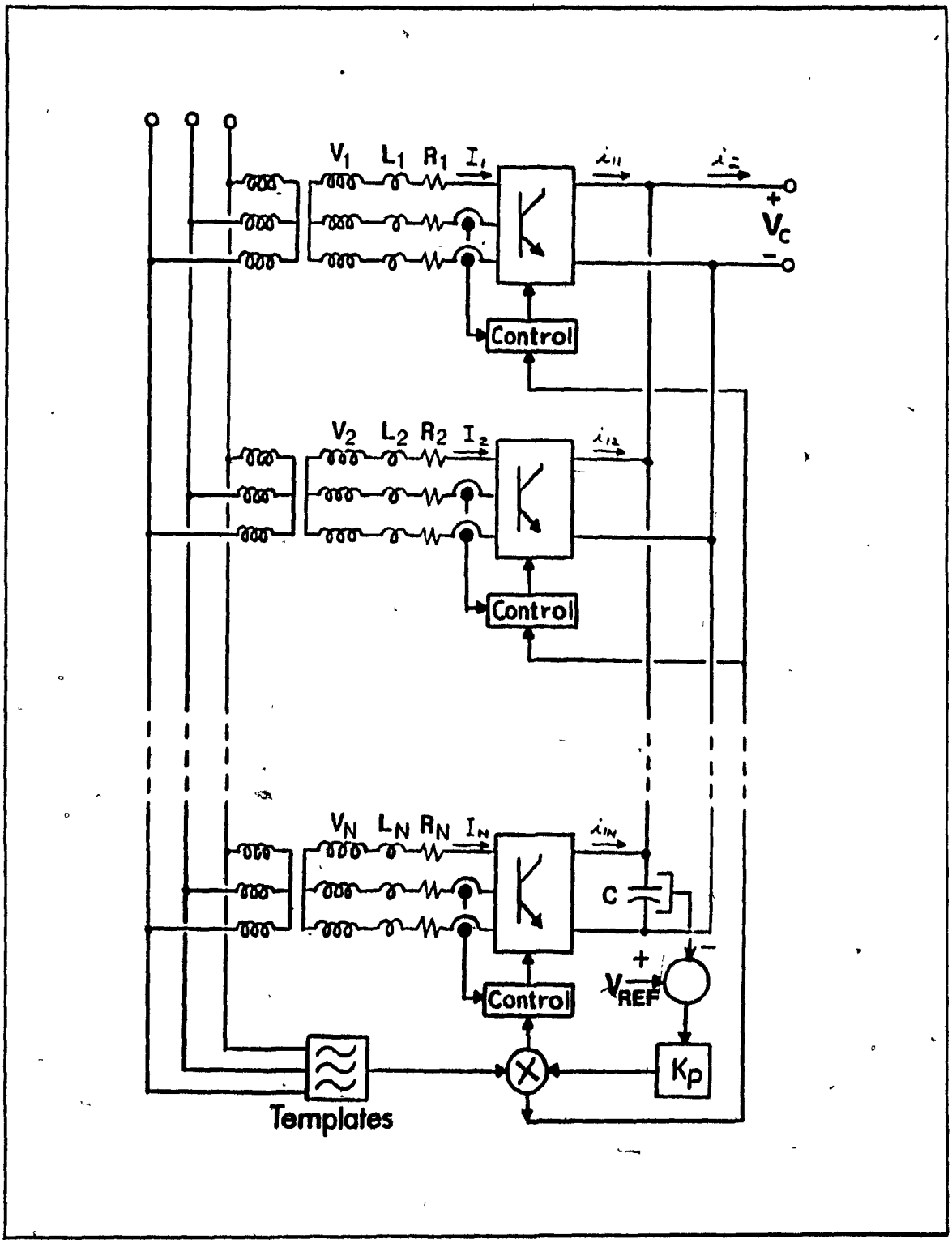


Fig.5.2 Type B: Common Current Reference Control.

This condition must be satisfied for every one of the N rectifiers.

The second condition for stability is obtained from the denominator of T_e

$$\Sigma_n V_n > 2I \Sigma_n R_n \tag{5.15}$$

or

$$I < \frac{\Sigma_n V_n}{2 \cdot \Sigma_n R_n} \tag{5.16}$$

5.3.2 Input and Output Current Sharing.

Because Type B configuration uses a common current reference, the input ac currents are identical by definition. The sharing of the output currents on the dc side can be obtained from eq.(5.8), with the condition $I_j=I_k=I$ for all j, k into n.

$$\frac{i_{1j}}{i_{1k}} = \frac{V_j - R_j I}{V_k - R_k I} \tag{5.17}$$

Assuming $R_j = R_k = 0$ it yields

$$\frac{i_{1j}}{i_{1k}} = \frac{V_j}{V_k} \tag{5.18}$$

Thus, the dc current sharing depends directly on the balancing of the voltage transformers from the supply. If a common transformer is used, the Type B configuration is always balanced and independent of X_n variations.

5.4 Type C: Common Switching Control.

In the Type C configuration, shown in Figure 5.3, the input current is measured only in the converter number N, called Master. The rest, called Slaves (n=1,2..,N-1), receive their logic commands from the Master so that their power electronic switches turn ON and OFF in unison with the corresponding switches of the Master.

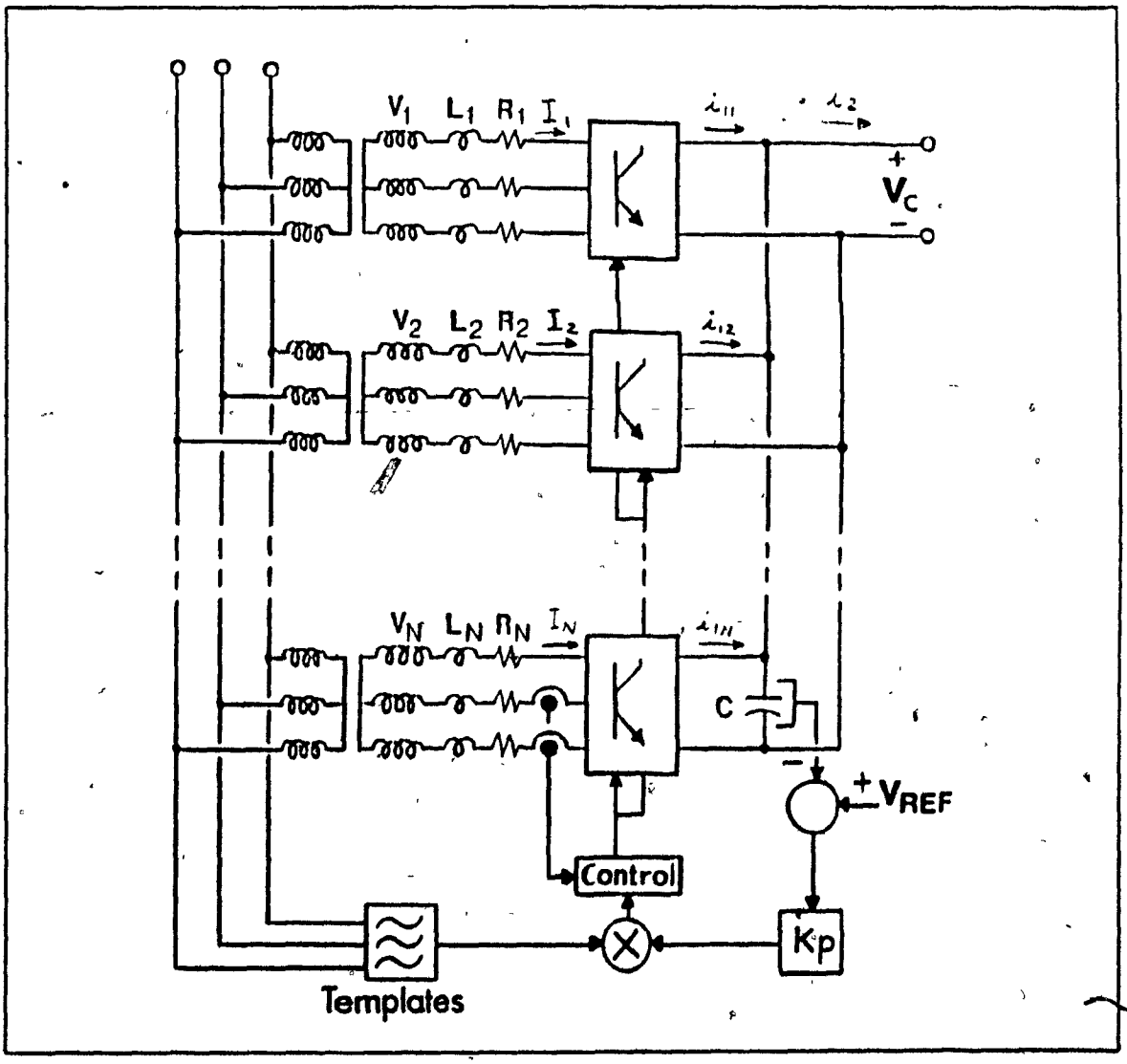


Fig.5.3 Type C: Common Switching Control.

Thus, like the Type C series connection, the voltage at one phase of each of the modules will have identical patterns, as shown in Figure 5.4.

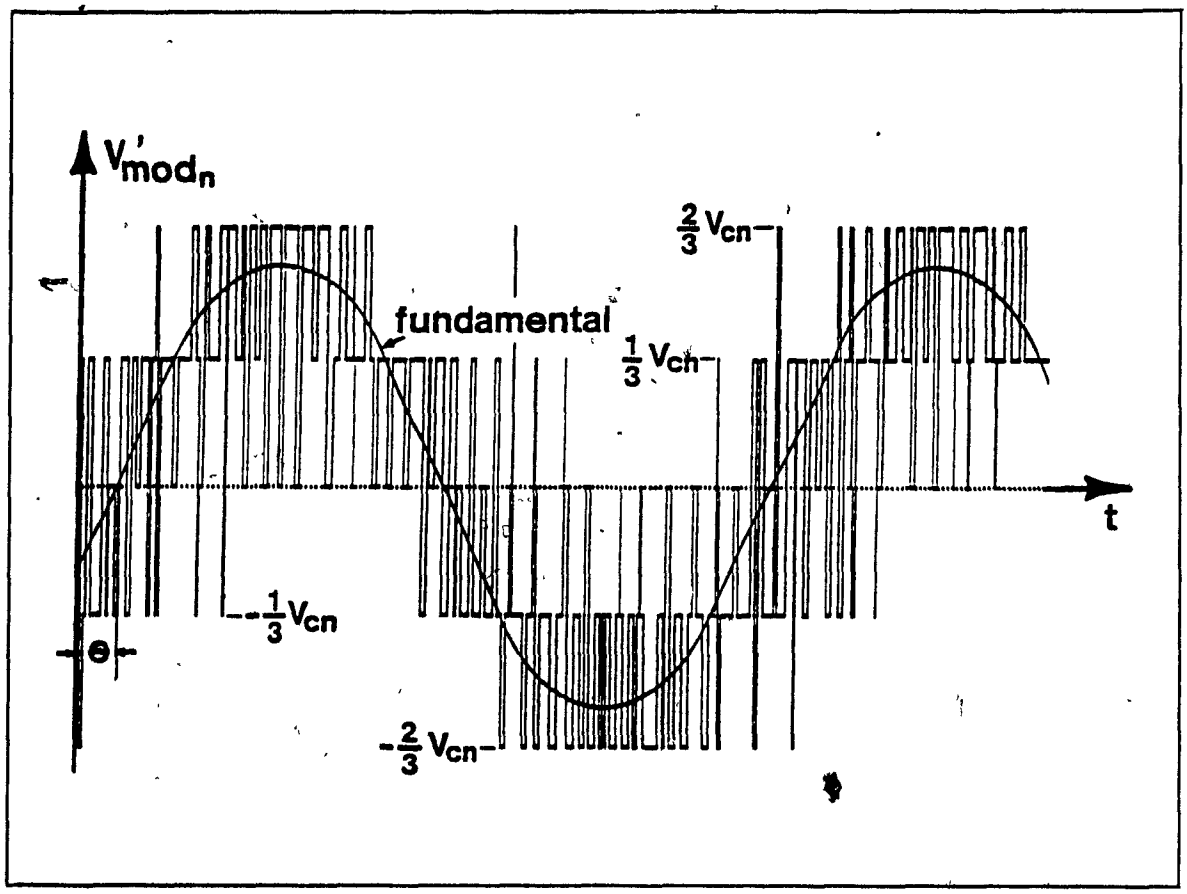


Fig.5.4 Simulated Waveform of the Phase Voltage of One Rectifier and its Fundamental Fourier Component for Type C.

Because the dc link voltage v_c is common for all the rectifiers, the resultant fundamental Fourier component from Figure 5.4, $\tilde{V}_{modn}$, will be identical in amplitude and angle for all converters.

$$\tilde{V}_{modn} = \tilde{V}_{modN} = \tilde{V}_{mod} \qquad (5.19)$$

5.4.1 - Mathematical Analysis and Stability.

The mathematical analysis for the Type C configuration, is based on the fact that all the rectifiers are controlled with the same common voltage V_{mod}, as was described by eq.(5.19). In consequence, in general the Slave currents will not have the same power angle ϕ as the Master, under unbalanced conditions. To avoid the trigonometrical functions in the differential equations, the use of the d-q frame for the analyses is recommended.

In controlling the time dependent magnitude of its input current I_N, the voltage $v_{mod}(t)$ generated at the Master Rectifier terminals for phase "a" is

$$v_{mod}(t) = \sqrt{2}\cdot\left(\left(V_N - L_N\cdot\frac{dI_N}{dt} - R_N\cdot I_N\right)\cdot\sin w_s t - X_N\cdot I_N\cdot\cos w_s t\right) \tag{5.20}$$

where the Master is assumed to operate at unity power factor. Transforming the a-b-c frame into a d-q frame yields

$$V_{modd} = -\sqrt{3}\cdot X_N\cdot I_N \tag{5.21}$$

$$V_{modq} = -\sqrt{3}\cdot\left(V_N - R_N\cdot I_N - L_N\cdot\frac{dI_N}{dt}\right) \tag{5.22}$$

The dynamic equation in the d-q frame describing the Slaves is

$$\begin{bmatrix} L_n & 0 \\ 0 & L_n \end{bmatrix}\cdot\frac{d}{dt}\begin{bmatrix} i_{dn} \\ i_{qn} \end{bmatrix} + \begin{bmatrix} R_n & -X_n \\ X_n & R_n \end{bmatrix}\cdot\begin{bmatrix} i_{dn} \\ i_{qn} \end{bmatrix} = \begin{bmatrix} V_{nd} \\ V_{nq} \end{bmatrix} - \begin{bmatrix} V_{modnd} \\ V_{modnq} \end{bmatrix} \tag{5.23}$$

where

$$\begin{bmatrix} V_{nd} \\ V_{nq} \end{bmatrix} = \begin{bmatrix} 0 \\ -\sqrt{3}\cdot V_n \end{bmatrix} \tag{5.24}$$

Replacing eqs.(5.21), (5.22) and (5.24) into (5.23), one has

$$\frac{d}{dt}\begin{bmatrix} i_{dn} \\ i_{qn} \end{bmatrix} = \frac{\sqrt{3}}{L_n}\begin{bmatrix} X_N\cdot I_N \\ V_N - R_N I_N - L_N\frac{dI_N}{dt} - V_n \end{bmatrix} - \begin{bmatrix} \frac{R_n}{L_n} & -w_s \\ w_s & \frac{R_n}{L_n} \end{bmatrix}\cdot\begin{bmatrix} i_{dn} \\ i_{qn} \end{bmatrix} \tag{5.25}$$

On the other hand, the dynamic power balance equation gives:

i) for the Master

$$v_c\cdot i_{1N} = 3\cdot(V_N I_N - R_N I_N^2 - L_N I_N\frac{dI_N}{dt}) \tag{5.26}$$

ii) for the jth Slave

$$v_c\cdot i_{1j} = v_{modd}\cdot i_{dj} + v_{modq}\cdot i_{qj} \tag{5.27}$$

Replacing eqs.(5.21) and (5.22) into (5.27), it yields for the jth Slave

$$v_c\cdot i_{1j} = -\sqrt{3}\cdot X_N I_N i_{dj} - \sqrt{3}\cdot(V_N - R_N I_N - L_N\frac{dI_N}{dt})\, i_{qj} \tag{5.28}$$

The overall system is formed by the Master and the N-1 Slaves. As a result, the dynamic power balance equation for the complete configuration is given by

$$v_c \cdot \sum_n i_{1n} = -\sqrt{3} \cdot (X_N I_N \cdot \sum_n i_{dn} + (V_N - R_N I_N - L_N \frac{dI_N}{dt}) \cdot \sum_n i_{qn}) +$$

$$+ 3 \cdot (V_N - R_N I_N - L_N \frac{dI_N}{dt}) \cdot I_N \qquad (5.29)$$

From Figure 5.3, the following expression is obtained

$$\sum_n i_{1n} = C \frac{dv_C}{dt} + i_2 \qquad (5.30)$$

Introducing eq.(5.29) into (5.30) and assuming $i_2 \cdot v_C = P_2$ yields

$$C \cdot v_C \frac{dv_C}{dt} = (V_N - R_N I_N - L_N \frac{dI_N}{dt})(3I_N - \sum_n i_{qn}) - \sqrt{3} X_N I_N \cdot \sum_n i_{dn} - P_2 \qquad (5.31)$$

The Slave currents (i_{dn}, i_{qn}) are solved by eq.(5.25). The input Master current I_N, is related to v_C through the proportional feedback Kp and the reference dc link voltage V_{REF}.

$$I_N = Kp \cdot (V_{REF} - v_C) \qquad (5.32)$$

With eqs.(5.25), (5.31) and (5.32), the system is completely defined. However, its analytical solution is long and tedious. Nevertheless, some conclusions can be obtained by replacing the derivative of eq.(5.32), dI_N/dt, into (5.31), yielding:

$$\frac{dv_C}{dt} = \frac{(V_N - R_N I_N) \cdot (3I_N - \sqrt{3} \cdot \Sigma_n i_{qn}) - \sqrt{3} X_N I_N \cdot \Sigma_n i_{dn} - P_2}{C \cdot v_C - L_N Kp \cdot (3I_N - \sqrt{3} \cdot \sum_n i_{qn})} \qquad (5.33)$$

It can be pointed out from eq.(5.33) that the denominator cannot be zero, otherwise this equation is undefined. Thus, one can find a limit of stability of the system making the denominator of (5.33) equal to zero

$$C \cdot v_c - L_N \cdot Kp \cdot (3I_N - \sqrt{3} \cdot \sum_n i_{qn}) = 0 \qquad (5.34)$$

from which

$$I_N = \frac{C \cdot v_C + \sqrt{3} \cdot \Sigma_n i_{qn}}{3 \cdot L_N \cdot Kp} \qquad (5.35)$$

A particular but important case is when the system is perfectly balanced. In such a case, $R_n=R_N$, $X_n=X_N$ and $V_n=V_N$ (n=1,2..,N-1). Because v_{mod} is a common driver, the input currents become identical and so

$$i_d(t) = 0 \qquad (5.36)$$

$$i_q(t) = -\sqrt{3} I_N(t) \qquad (5.37)$$

Replacing eq.(5.37) into (5.34) results

$$C \cdot v_c - 3N \cdot L_N Kp \cdot I_N = 0 \qquad (5.38)$$

from which one gets the limit of stability as

$$I_N = \frac{C \cdot v_C}{3N \cdot L_N Kp} \qquad (5.39)$$

This is exactly the same stability limit as the one obtained in eq.(5.14) for the Type B configuration, under balanced conditions.

5.4.2 Input and Output Current Sharing.

The input currents of the Slaves can be obtained from the steady-state solutions of eq.(5.25):

$$I_{dn} = \frac{\sqrt{3}\cdot\left[(V_N-V_n)X_n - (R_NX_n-R_nX_N)I_N\right]}{R_n^2 + X_n^2} \qquad (5.40)$$

$$I_{qn} = \frac{\sqrt{3}\cdot\left[(V_N-V_n)R_n - (R_nR_N+X_nX_N)I_N\right]}{R_n^2 + X_n^2} \qquad (5.41)$$

and the Slave output current i_{1n} from the steady-state solution of eq.(5.28)

$$i_{1n} = \frac{-\sqrt{3}\cdot X_N I_N I_{dn} - \sqrt{3}\cdot(V_N-R_NI_N)I_{qn}}{Vc} \qquad (5.42)$$

where Vc is obtained from eq.(5.32) under steady-state condition

$$Vc = V_{REF} - \frac{I_N}{Kp} \qquad (5.43)$$

From eqs.(5.40) to (5.42), it can be found that input and output currents are perfectly balanced when the parameters of the Slaves are identical to the corresponding parameters of the Master. Based on these equations, the Figures 5.5 and 5.6 graphically show the effect of the parameter variations on I_n and i_{1n} with respect to the Master steady-state conditions, as a function of X_n and V_n respectively. The Master operates at its rated power and X_N=0.25 [pu].

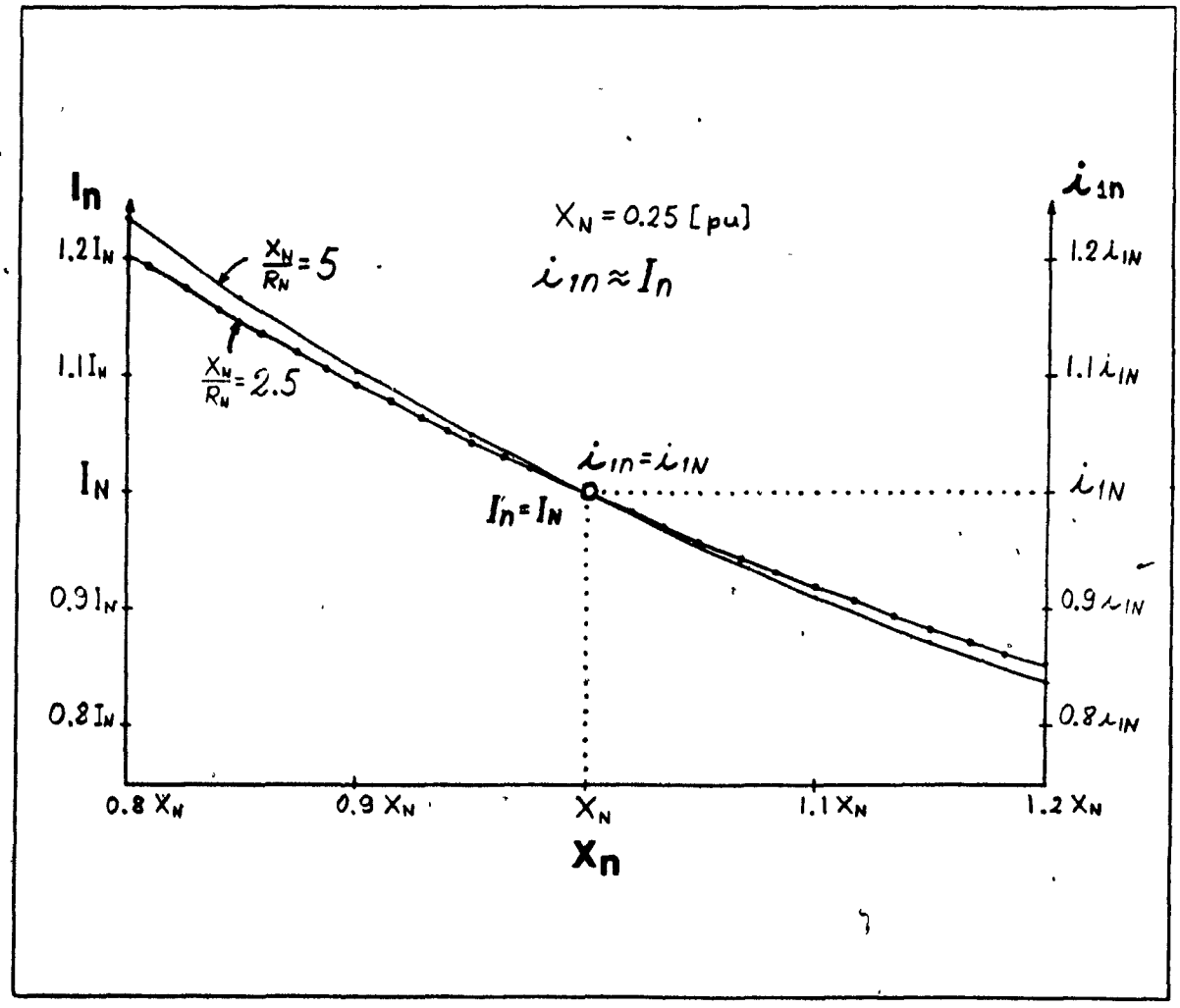


Fig.5.5 Parameter Sensitivity of Type C Connection to AC Line Reactance X_n Variations

It can be seen from Figure 5.5 that the Slave current I_n changes almost linearly and inversely with X_n. A 20% increase in X_n implies about a 20% decrease in I_n and viceversa. The output current i_{1n} follows almost exactly the same curve in the graphs (i_{1n}-I_n). Therefore, these plots are also valid for i_{1n}. It can be noted that the X_N/R_N ratio does not play an important role in the deviations of I_n and i_{1n}. In the graphs, the cases for X_N/R_N=2.5 and X_N/R_N=5 are displayed.

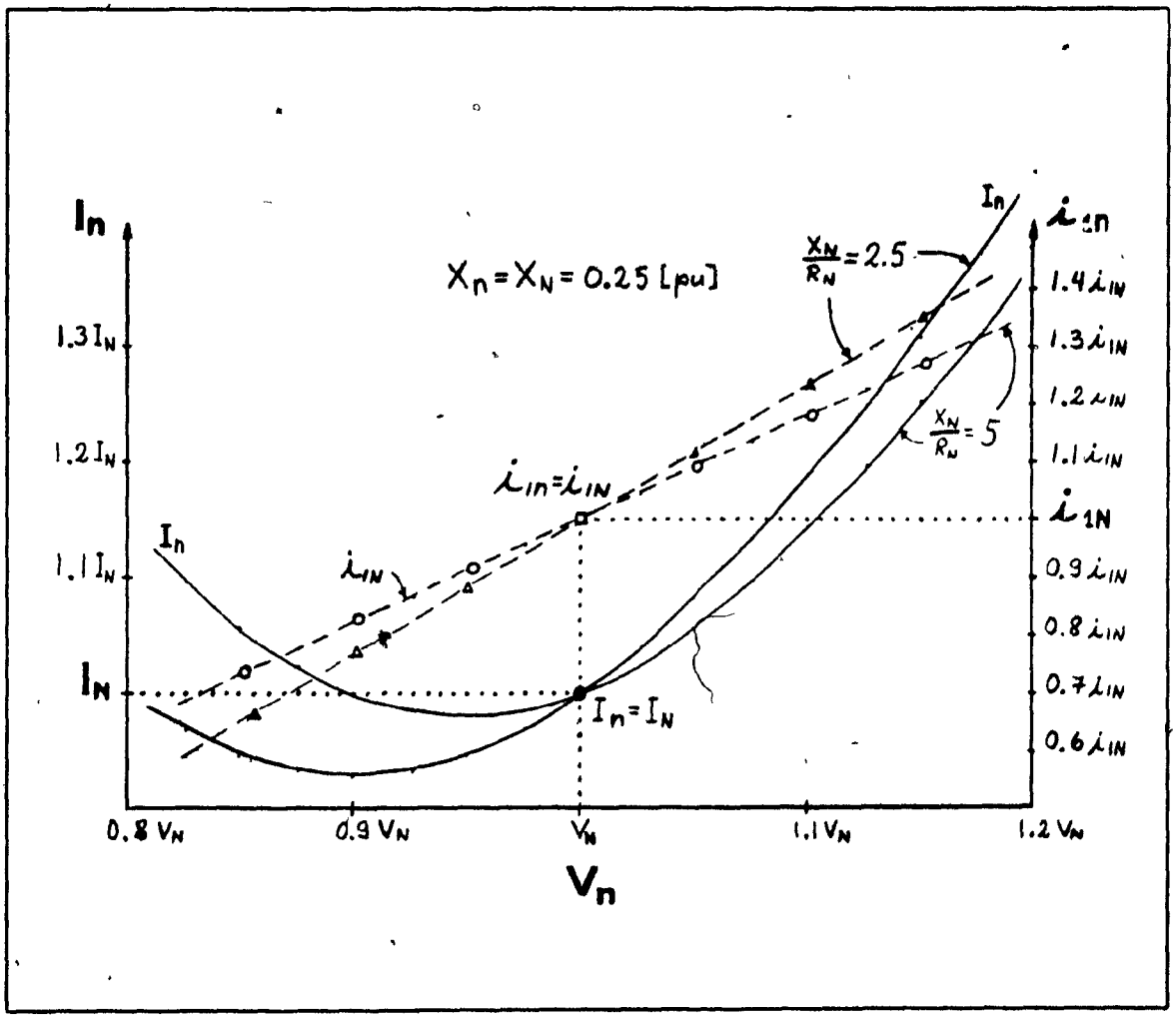


Fig.5.6 Parameter Sensitivity of Type C connection to AC Source Voltage V_n Variations.

Figure 5.6 shows the behaviour of the input and output Slave currents under V_n variations. It can be seen that the Slave currents are very sensitive to V_n variations and hence, input voltage transformers must be very well balanced. Variations in V_n beyond 10% are undesirable because they can produce more than 20% variations in the currents. Furthermore, unbalances in the input transformers increase the sensitivity of the currents to X_N and R_N variations, as can be seen from eqs.(5.40) to (5.42). All these reasons makes it recommendable to use a common input transformer for parallel Type C configuration instead of independent units. As a result, the number of current sensors will increase from two to three units.

The resistance R_n has been shown to produce very small changes on the currents. For this reason, it is not shown graphically.

5.5 Type D: Indirect Common Switching Control.

The Type D or Indirect Common Switching Control is based on the same operation principle as Type C. The difference is that here, the Indirect Current Control Method discussed in Chapter III replaces the Direct Method of control used in the Type C configuration. This allows a third simplification in the parallel system: the elimination of all current sensors. In the Type D configuration, the overall feedback system is controlled by just sensing the dc voltage.

The method of control used here has been discussed in Chapter III and is based on the application of the well known Sinusoidal Pulse Width Modulation technique (SPWM).

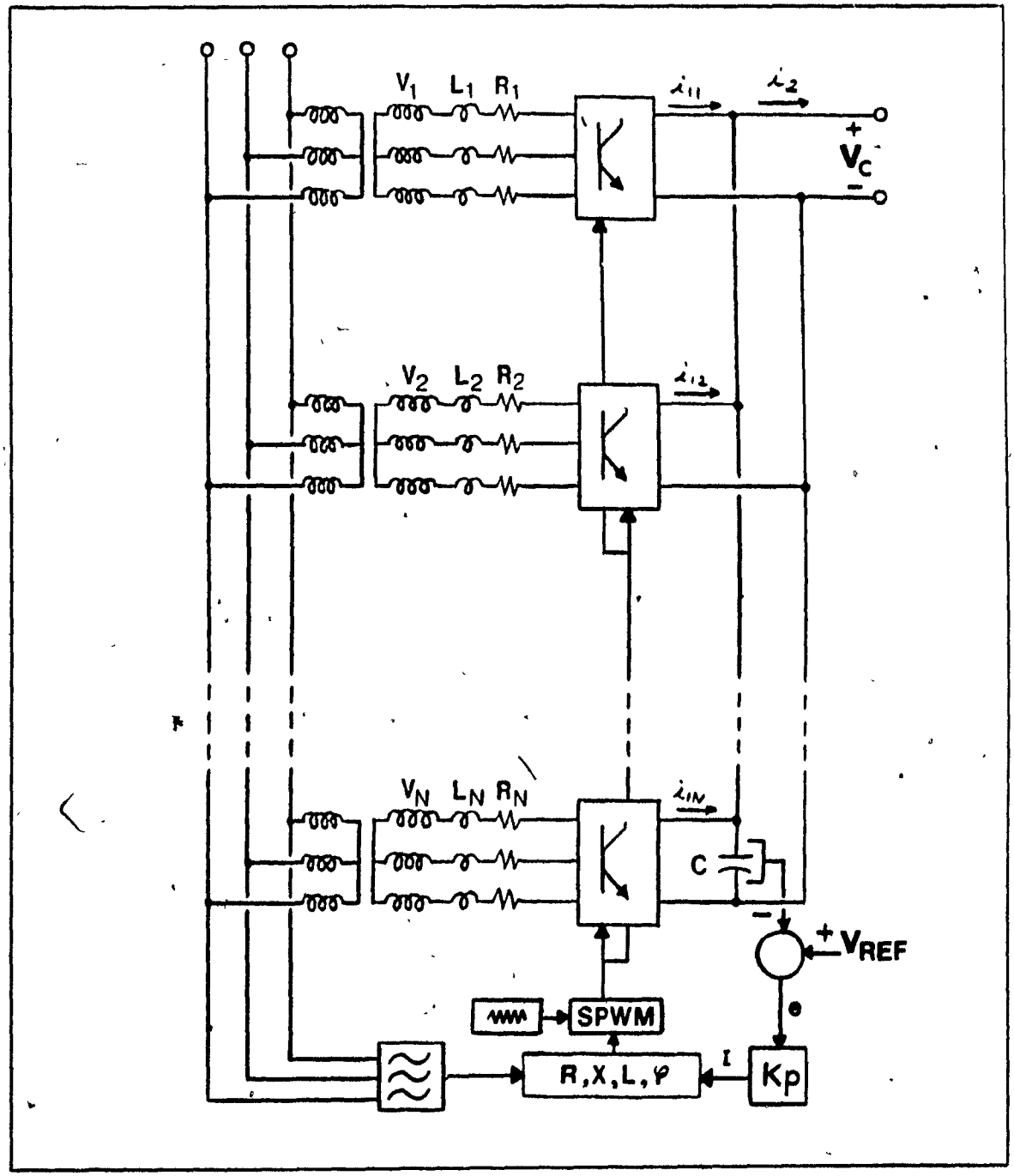


Fig.5.7 Type D: Indirect Common Switching Control Topology

5.5.1 Stability and Parameter Sensitivity.

Figure 5.7 shows the circuit configuration of the Type D topology. Its stability and parameter sensitivity are based on the same equations developed for the Type C configuration and hence will not be repeated again.

5.6 Type E: Shifted Triangular Carrier Control.

The Type E or Shifted Triangular Carrier Control configuration does not introduce any reduction in the hardware. On the contrary, a slight increase in hardware components is required. However, the system performance is greatly improved in terms of operational costs. The Type E configuration is able to produce excellent current waveforms with low switching frequency and hence high overall efficiency with respect to the other configurations. In Type E configuration, as well as in Type D, there is no Master Rectifier. All the converters have the same hierarchy.

5.6.1 Harmonic elimination.

The harmonic elimination process is based on the idea of using the same modulating signal for all the converters, with the slight modification that each one has its own triangular carrier suitably phase-shifted. In this form, a significant number of unwanted harmonics are eliminated. The mathematical analysis of harmonic elimination has already been developed in Section 4.6.1 and so will not be repeated again.

The Type E or Shifted Triangular Carrier topology is shown in Figure 5.8.

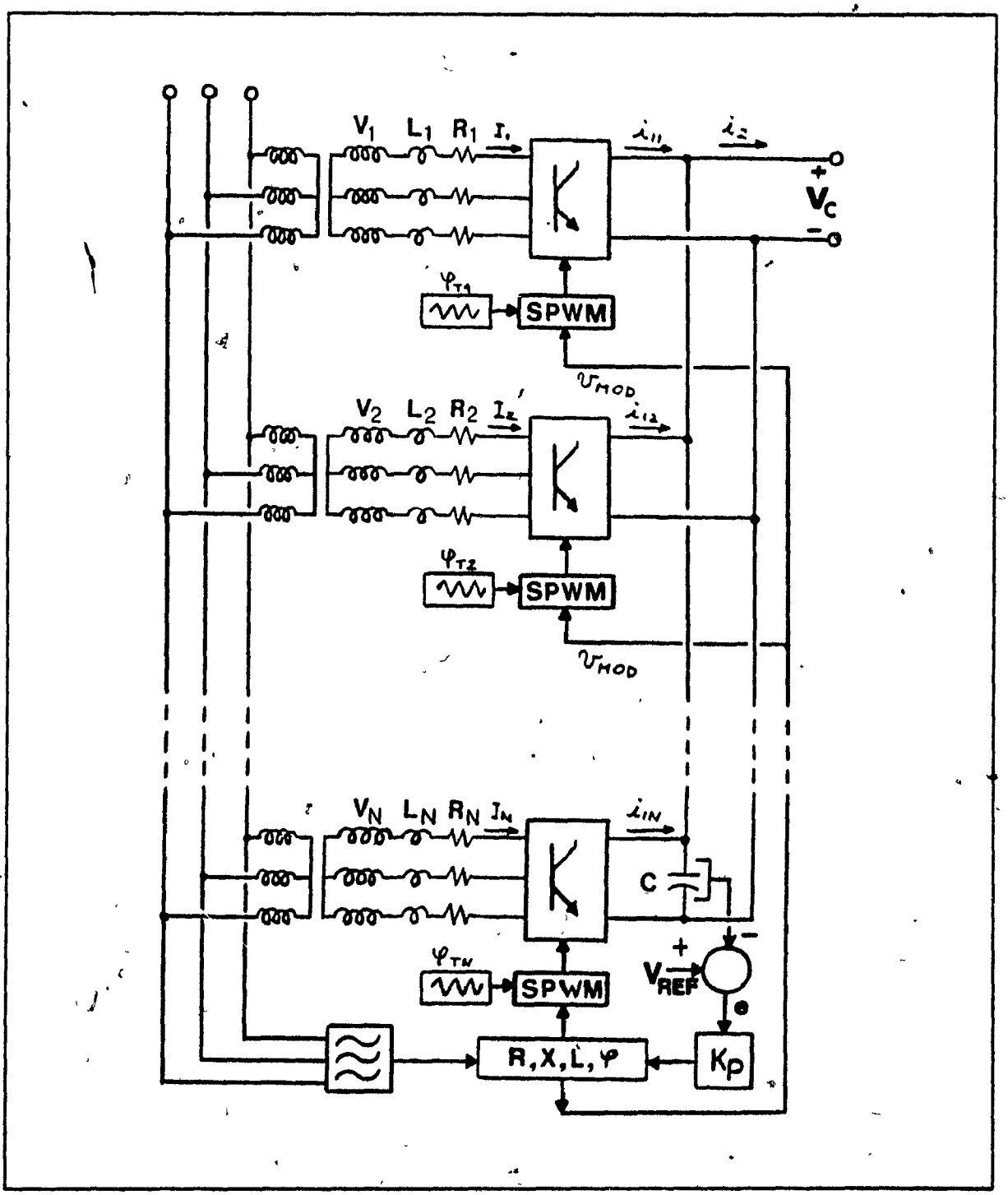


Fig.5.8 Type E: Triangular Carrier Shifted Topology.

5.7 Subtopologies.

Types A to E topologies, which have already been discussed, can be made to have different properties by making slight changes in their electrical structure. For example, in Type C topology, it is possible to measure the total current at the primary of the input transformers instead of measuring the partial current at the secondary of the Master transformer. This change can have some advantages like the elimination of the Master unit and the reduction of the current sensors from three to two when a common transformer is used. Subtopologies have not been analyzed in this work.

5.8 Experimental Results.

The mathematical analyses that have been developed in this chapter closely agree with experimental work. Valve-by-valve digital simulations were also obtained to support the analyses. The agreements have also been excellent but they are not shown here.

The experimental work was realized with two 2-kW parallel connected rectifiers, each with the following ratings: supply voltage V_n=40 V; reference dc voltage V_{REF}=120 V; proportional controller gain Kp=3 A/V; reactance per phase X_n=2.5 Ohms and resistance per phase R_n=1 Ohm. Higher ratings were obtained with the valve-by-valve digital simulations.

The Figure 5.9 shows the step response of the parallel Type B topology. The load current i_2 changes from 0 to 15 Adc. It can be seen that the input currents react identically with the perturbation. The oscillogram also allows one to see the close in-phase relationship of the currents with respect to one of the supply voltages. The upper beam of the oscillogram shows the forcing function i_2.

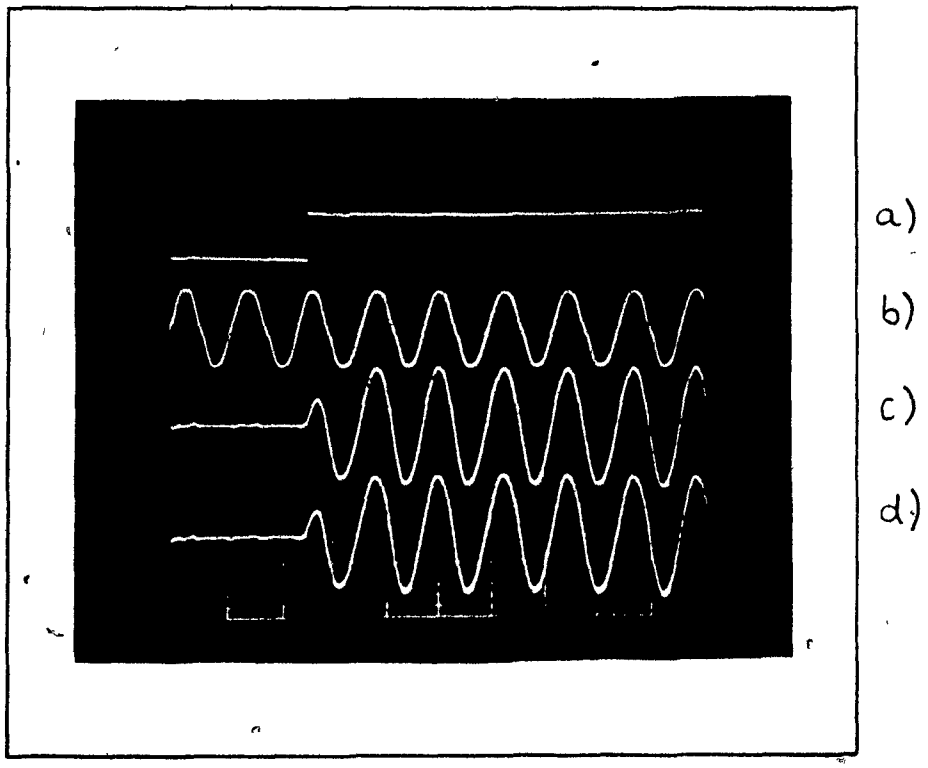


Fig.5.9 Type B: Step Response.
a) load dc current i_2
b) input supply voltage V_1
c) input current I_1
d) input current I_2

Figures 5.10 to 5.12 show the Type B configuration under unbalanced reactances. Figure 5.10 shows the step response, where X_1=2.5 Ohms and X_2=5 Ohms. It can be seen that the currents remain unaltered. Only small distortions appear. The insensitivity to X_n variations was predicted in the analytical work developed for Type B connection in Section 5.3.2. Power reversal and a detail of the input currents for this configuration are shown in Figures 5.11 and 5.12 respectively.

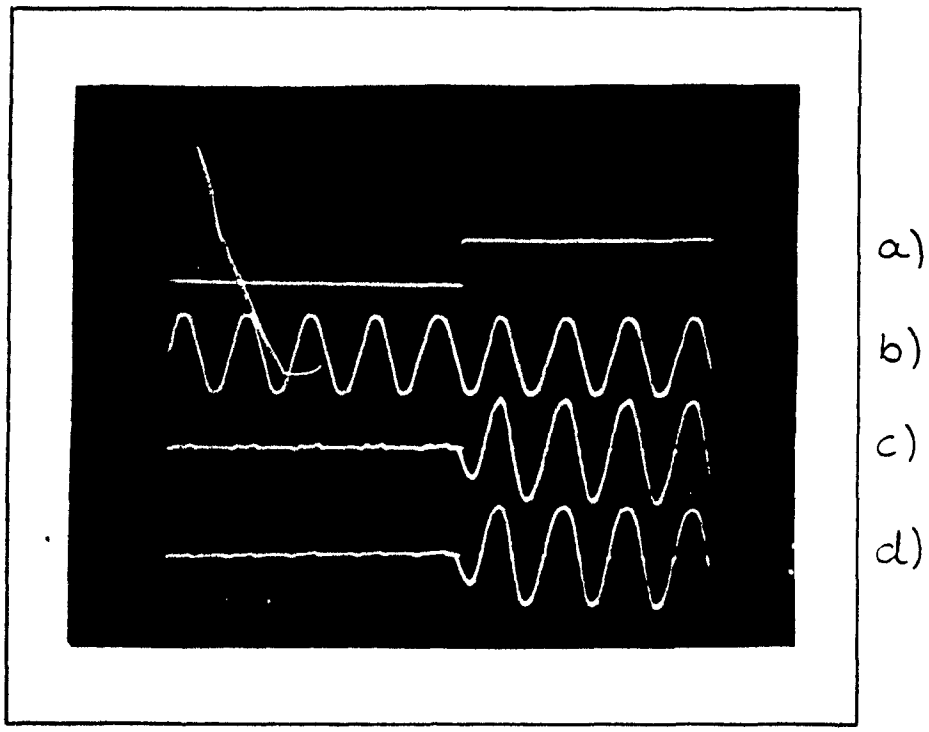


Fig.5.10 Type B: Step Response with Unbalanced Reactances.
a) load dc current i_2
b) input supply voltage V_1
c) input current I_1 with X_1=2.5 Ohms
d) input current I_2 with X_2=5 Ohms

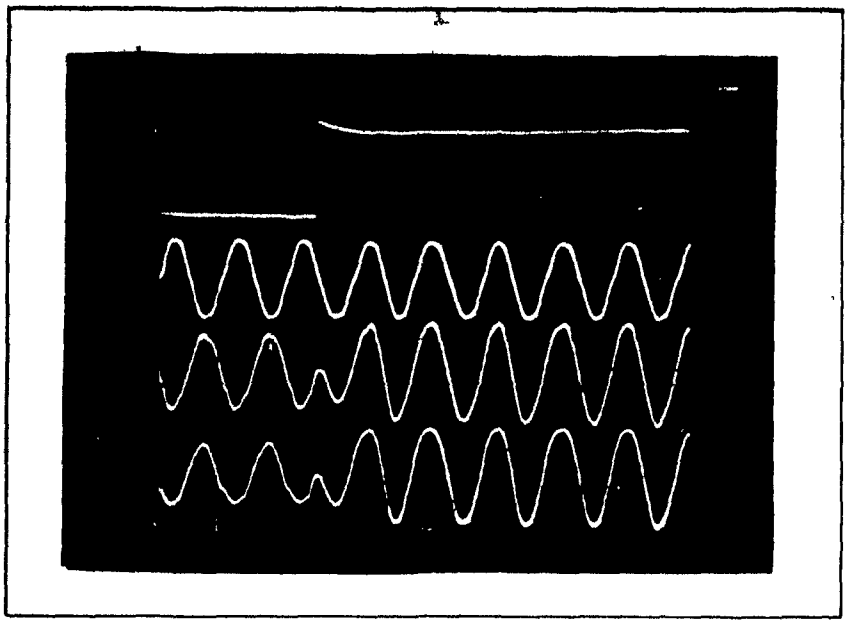


Fig.5.11 Type B: Reversal of Power with Unbalanced Reactances.
a) load dc current i_2
b) input supply voltage V_1
c) input current I_1 with X_1=2.5 Ohms
d) input current i_2 with X_2=5 Ohms

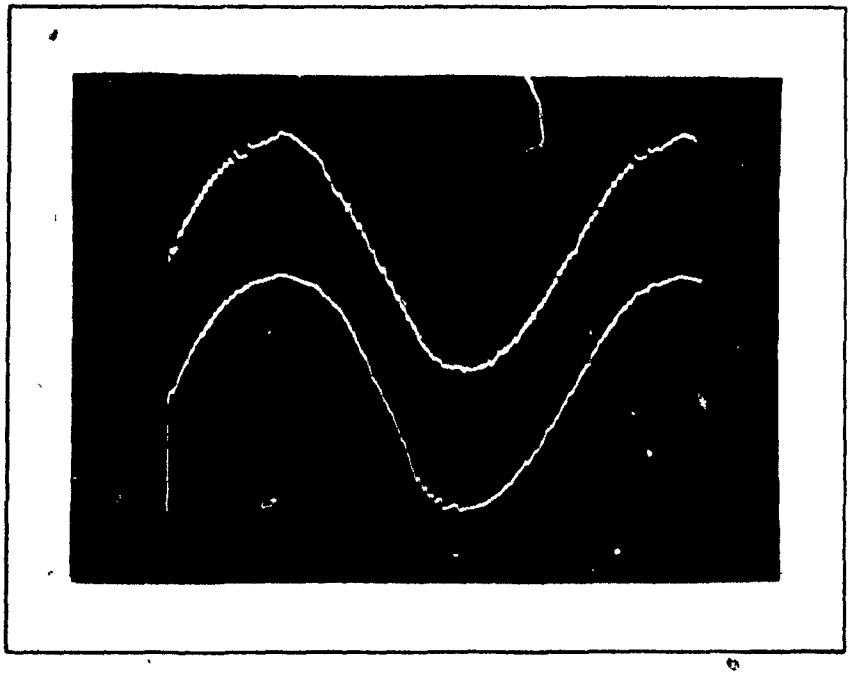


Fig.5.12 A Detail of the Input Currents I_1 and I_2 for Type B Configuration with X_1=2.5 Ohms and X_2=5 Ohms.

Figures 5.13 and 5.14 show the step response and power reversal response for the Type C configuration respectively. In Figure 5.13, the dc current i_2 changes from 0 to +15 Adc and in Figure 5.14 from -10 to 10 Adc.

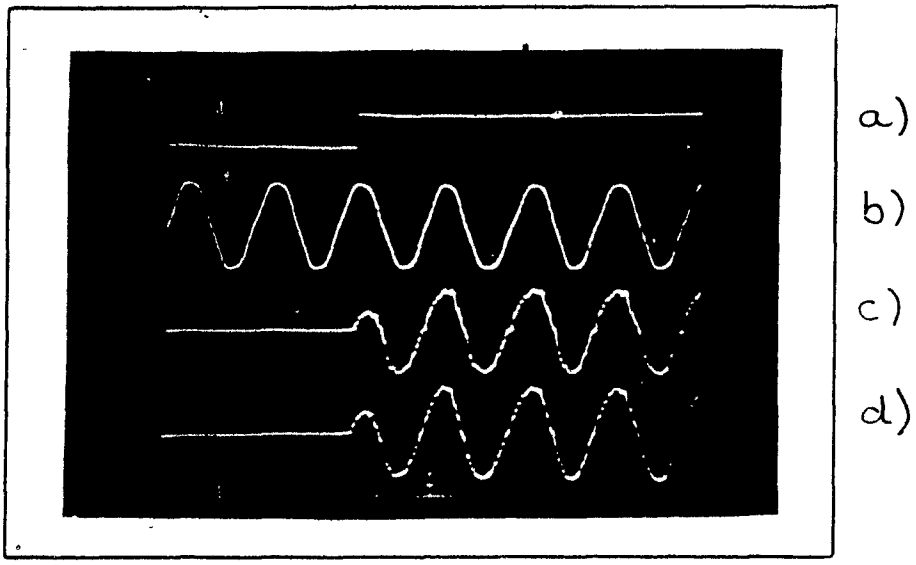


Fig.5.13 Step Response for Type C Configuration.
a) load dc current i_2; b) supply voltage V_1
c) input current I_1; d) input current i_2

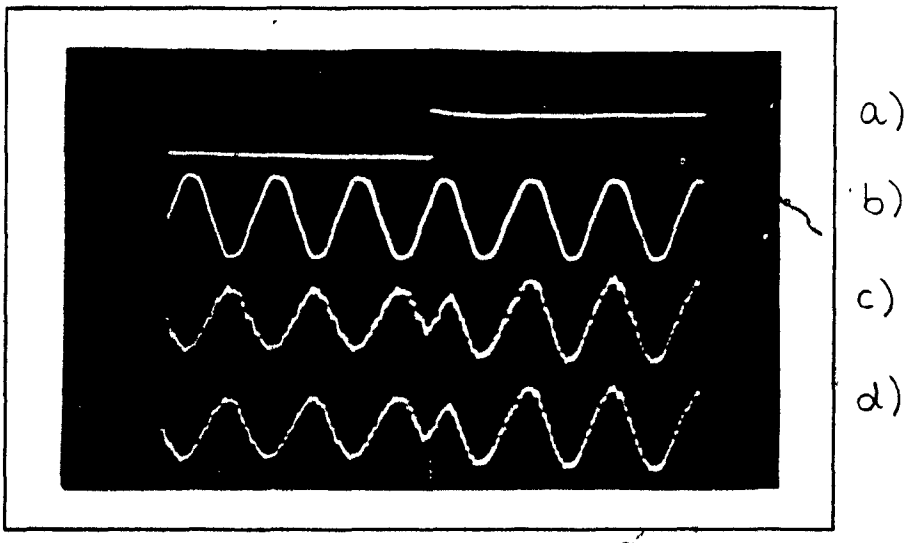


Fig.5.14 Type C Configuration: Reversal of Power.
a) load dc current i_2; b) supply voltage V_1
c) input current I_1; d) input current i_2

Figure 5.15 shows the step response for a Type D configuration. The output dc current also changes from 0 to 15 Adc.

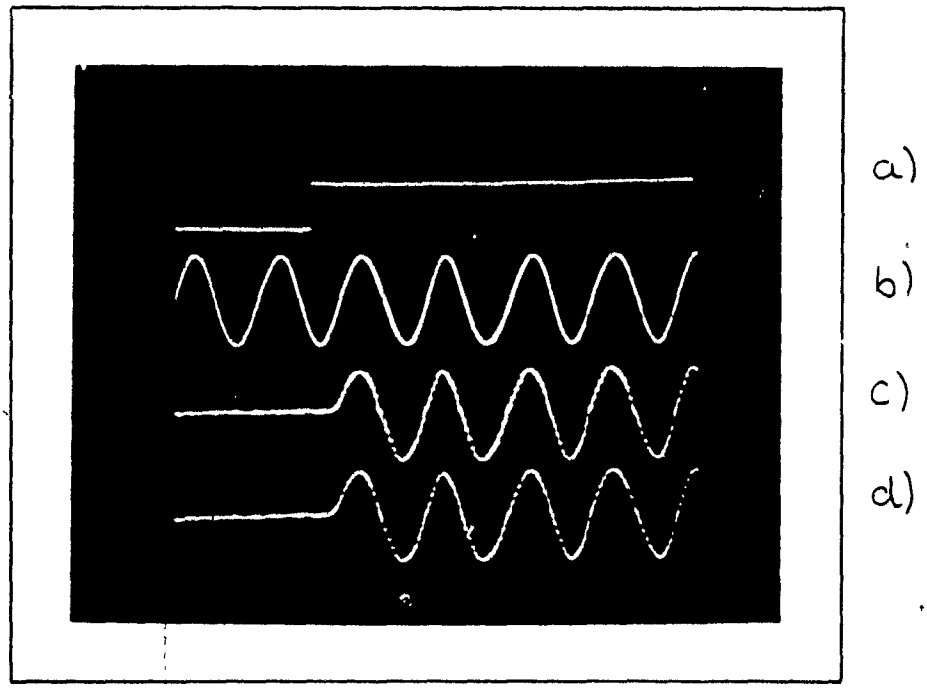


Fig.5.15 Step Response for Type D Configuration.
a) load current i_2
b) supply voltage V_1
c) input current I_1
d) input current I_2

Finally, Figure 5.16 shows a detail of the input currents of the Type E configuration, in which it can be observed that the ripple of the total current is smaller than that of the currents of each one of the single units.

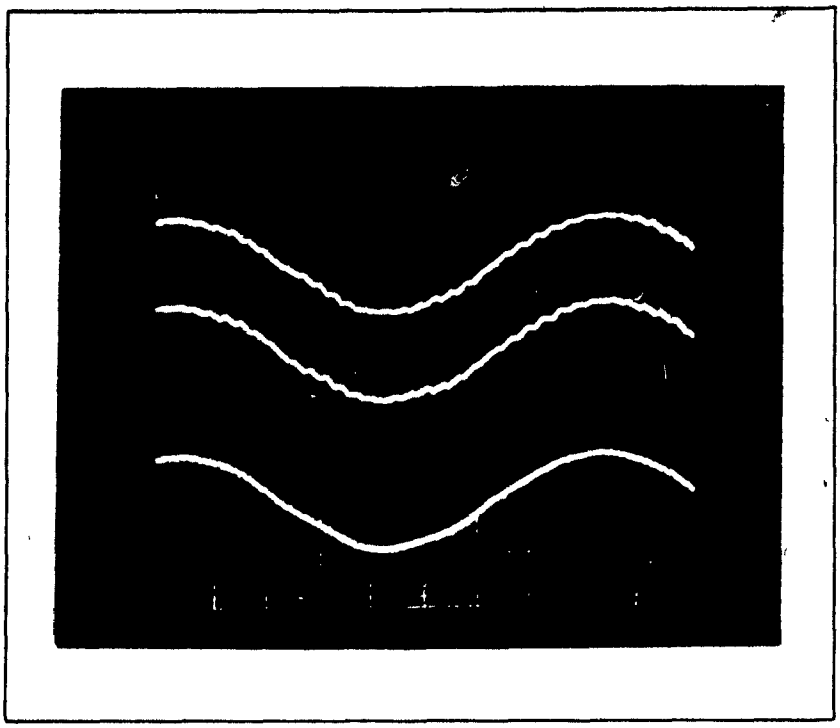


Fig.5.16 Type E Configuration: Harmonics are Eliminated by Using the Shifted Triangular Carrier.

5.9 Summary.

This chapter has presented the results of a brief investigation of parallel connected rectifiers using different control strategies. Although this chapter is not as complete as the previous one, it presents the relevant mathematical tools for stability and sensitivity analyses for all the five topologies that have been analyzed.

The experimental work showed that all the topologies are stable in both, rectifier and inverter mode.

The next chapter will summarize all the work pursued in this thesis and will discuss possible future work related with this research.

CHAPTER VI

CONCLUSION

6.1 A Summary of the Work.

The main topic of this Thesis has been to study the utilization of Boost type PWM rectifiers in the field of high power applications. Research in this field has been focused on finding ways to produce high quality rectifiers, capable of generating almost sinusoidal current waveforms at unity power factor with power reversal capability. To obtain these features, two different methods of control, based on keeping the dc voltage regulated, have been analyzed: the **Direct Current Control Method** and the **Indirect Current Control Method**, discussed in Chapters II and III respectively. A complete analytical study has been carried out for each one of these two methods and digital simulations along with experimental work have verified the results.

The use of rectifiers in high power applications is limited by the voltage and current ceilings of power electronic switches available on the market. One solution to this problem is to connect many modular rectifier units in series and/or in parallel. Chapter IV studied different topologies and arrangements using series connected Boost type rectifiers. Chapter V analyzed the parallel configurations.

Complete mathematical analyses have been developed for all series and parallel connections. The stability, parameter sensitivity and power sharing capability of the converters have been analyzed. Digital valve-by-valve simulations and experiments have made it possible to verify the mathematical equations.

Of the different topologies that have been analyzed in this work, one is particularly stable and economical. This is the series Type E configuration discussed in Section 4.6, which uses a combination of features that makes this topology very promising: a) it is controlled by measuring only one converter voltage; b) it is very stable and c) it permits the elimination of low order harmonics.

Possible high power applications for series and/or parallel connected rectifiers have also been mentioned in this work. Among them are rectifiers for electric traction applications discussed in Section 4.9.3.1 and Back-to-Back systems in Section 4.9.6.

6.2 Conclusion.

Investigation of this thesis allow the following conclusions to be made:

1) The Boost Type PWM Rectifier has a very promising future in industrial applications. Its commercial importance will be appreciated when stringent harmonic standards

will be enforced to reduce harmonic pollution in the utility network.

2) In the near future, since the Boost Type PWM Rectifier is more expensive than the Thyristor Graetz Bridge, it will find a market niche in applications where its fast dc current reversal capability is a valuable asset.

3) The Volt-Ampere capability of the Boost Type PWM Rectifier can be increased by connecting modular units in series and in parallel. It should be mentioned that this approach is different from connecting switch devices (GTO's, Power Transistors, Power MOSFET's) in series and in parallel. In Power MOSFET's, for example, there is no difficulty in connecting multiple units in parallel, but their connection in series has proved to be problematic. The multiple modular connection has proven to be a method of overcoming such difficulties. The study of multiple modular unit connections paves the road to applications in High Voltage Direct Current (HVDC).

4) The Boost Type PWM Rectifier was originally conceived in the context of Hysteresis Current Control. The study of this thesis has brought it one step further into the mainstream of PWM techniques, in this particular case SPWM. There are two advantages in this improvement: i) the savings in cost from doing without the need of high quality current transducers and ii) simpler filter

design due to the predictability of the characteristic harmonics.

5) When the principles of SPWM are combined with the operation of multiple modular units in series and/or in parallel, a further advantage appears: one can use the phase delays between the individual modular units to cancel the characteristic harmonics. This has the implication that the switching rates of each modular unit need not be very high. The effect of fast switching can be achieved by staggering the switching times of many modular units. This means that fairly slow devices such as GTO's or even forced commutated thyristors can be used to attain high quality current waveforms. Furthermore, the switching losses can be reduced. This characteristic cannot be accomplished by using multiple electronic switches in the branches of a single rectifier, because they must all be switched simultaneously.

6) By configuring the control of the Boost Type PWM Rectifier as that of a DC Voltage Regulator, one has a fast response, stand alone, operating system. The power demand is automatically matched by any voltage deviation from the preset DC Voltage Reference. For comparison purposes, a proportional feedback control is used as a standard. Thus SPWM (Indirect Current Control) can be implemented in such a way as to have better stability

region than the Hysteresis Current Control (Direct Current) implementation. At the back of one's mind, one is aware that a proportional-integral control can achieve better control characteristics.

7) Although unstable conditions exist, the stable operating regions are extensive so that, from a practical viewpoint, stability is not a serious concern.

8) As the Boost Type PWM Rectifiers have such remarkable characteristics as:

   i) near sinusoidal current waveforms

   ii) controllable power factor (unity, leading or lagging)

   iii) fast, simple controls

   iv) unidirectional regulated dc voltage

   v) power reversal by reversal of dc link current

and have operated in rectifier/inverter and rectifier/chopper links in variable speed drives involving induction motors, synchronous motors and dc motors in 3 years of testing, there is good reason to believe that it will play an important role in the world of power electronics.

6.3 Suggestions for Future Work.

Very high power applications would require a combination of series and parallel configurations in a single rectifier station. Future study to analyze the compatibility of

combining different types of topologies to find the optimal in terms of economy, stability and reliability is the way for future research.

Other methods of modulation instead of Current Hysteresis Control or SPWM are another posibility of research. There are to many switching strategies that can be investigated which could improve the rectifier performance.

The digitalization of all the hardware configuration for practical systems seems to be mandatory. High accuracy, easy adjustment, drift elimination, noise reduction and microprocessor control are some of the obvious advantages of a digital system.

Finally, the possibility of using some of the configurations analyzed in this Thesis for High Voltage Direct Current Transmission (HVDC) is proposed for future analysis. One foreseen problem is the line inductance of the dc link. Simulations in the Back-to-Back system with high dc link inductance have shown that resonance problems between this inductance and the dc link capacitors may appear during transients. This and other possible problems have to be analyzed to determine the feasibility of implementing HVDC systems with Boost type PWM rectifiers connected in series and in parallel.

APPENDIX A

APPENDIX A

COMPUTER SIMULATIONS

A.1 Valve-by-valve Digital Simulation.

The Valve-by-Valve Digital Simulation Program is based on treating the rectifier bridge as a piece-wise linear circuit problem. The ON-OFF states of each of the six power switches give rise to eight possible circuit topologies, which will be discussed here. The instants of switchings of the power devices, depend on the method of control. Some application examples are given here.

Each one of the 8 possible circuit topologies, give rise to a different set of differential equations, which can be solved numerically using one of the many methods of integration available in literature. The polygonal method [74] was used in the simulation work because of its simplicity. Some simulations were also realized with the very well known 4th order Runge-Kutta method.

A.1.1 The Algorithm.

The Figure A.1 shows a rectifier circuit configuration with the essential components: the 3-phase power supply, inductances and resistances per phase, a dc link voltage source and six ideal switches which model the power semiconductor devices.

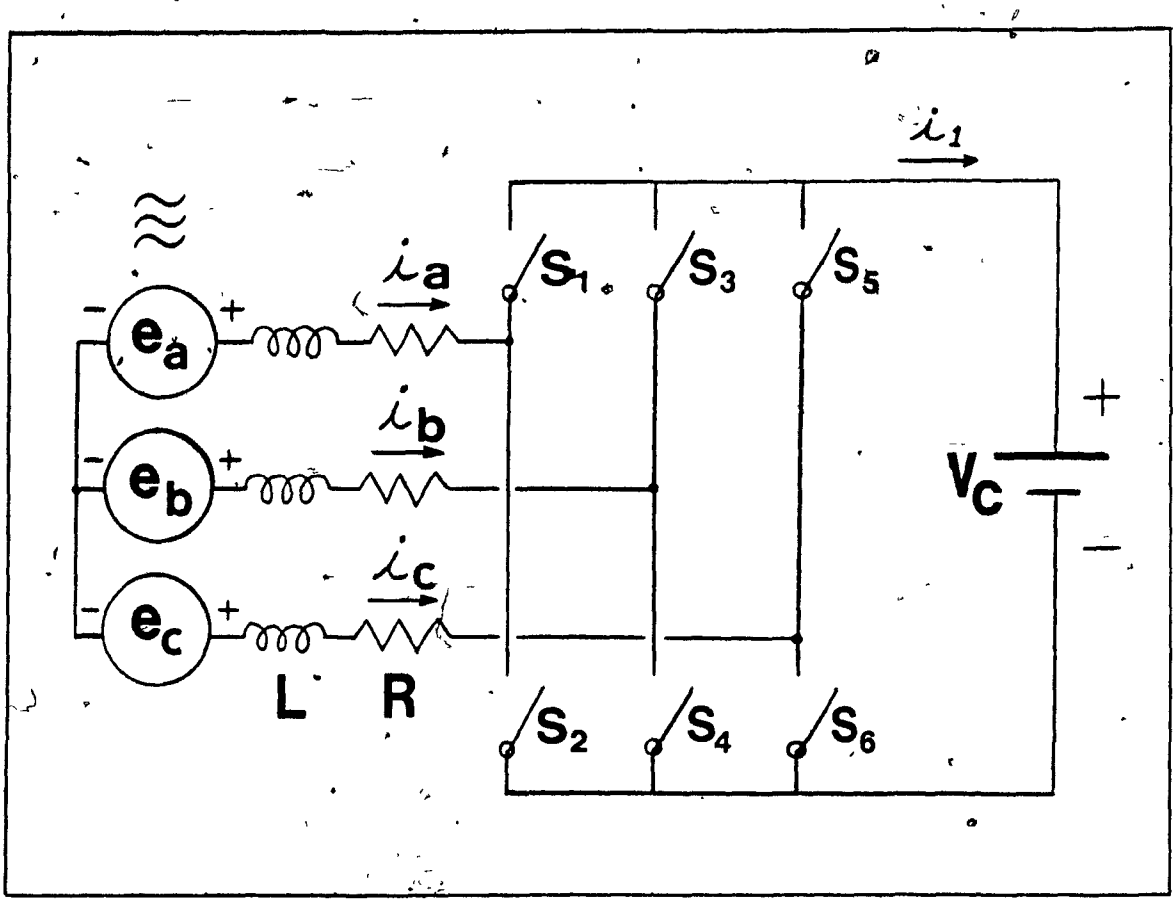


Fig.A.1 Rectifier Circuit Configuration.

The ON-OFF operation of the switches of Figure A.1 ($S_1, S_2, \ldots S_6$) is restricted for one constraint: the two switches of one phase (i.e. S_1, S_2) can neither be ON (closed) nor OFF (open) simultaneously. Their simultaneous ON operation means a dc shortcircuit and their simultaneous OFF operation results in an overvoltage in either of the two switches. This restriction allows the existence of only 8 possible ON-OFF switching combinations or states, which are shown in Table A.1.

TABLE A.1 Rectifier Switching States.

STATE	1	2	3	4	5	6	7	8
Phase a	+	+	+	+	-	-	-	-
Phase b	+	+	-	-	+	+	-	-
Phase c	+	-	+	-	+	-	+	-

The "+" sign indicates that the corresponding upper switch (S_1, S_3 or S_5) is ON (phase connected to the positive rail of the dc supply) and vice versa.

Each one of the 8 states has its proper set of differential and algebraical equations. For example, Figure A.2 shows the resultant circuit topology when the rectifier is in the state number 6 of Table A.1.

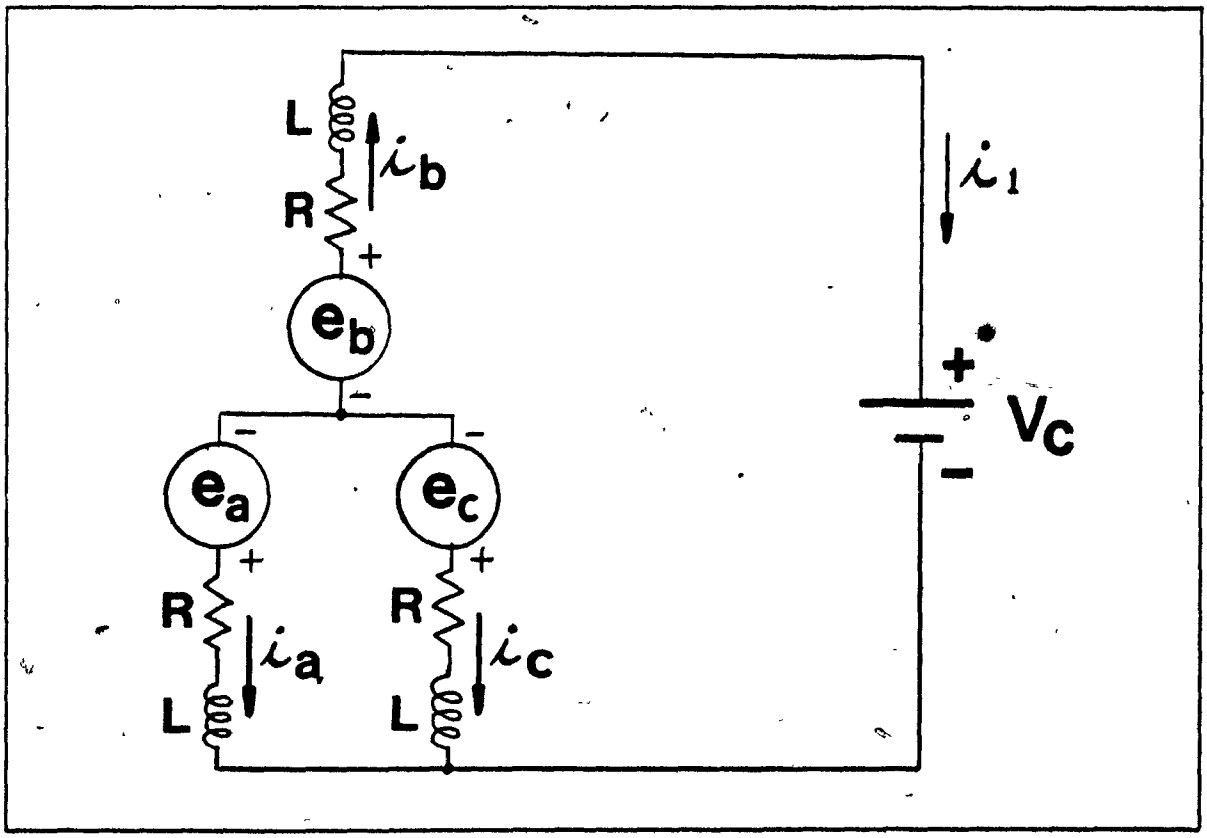


Fig.A.2 Rectifier Circuit in the 6th State.

The set of equations which describe the 6th state operation is:

$$\frac{di_a}{dt} = \frac{e_a}{L} - \frac{R i_a}{L} + \frac{1}{3}\cdot\frac{Vc}{L} \qquad (A.1)$$

$$\frac{di_b}{dt} = \frac{e_b}{L} - \frac{R i_b}{L} - \frac{2}{3}\cdot\frac{Vc}{L} \qquad (A.2)$$

$$i_c = - i_a - i_b \qquad (A.3)$$

$$i_1 = i_b \qquad (A.4)$$

This set of equations is solved numerically, with the initial conditions of the system given by the previous state.

The equations given for the 6th state can be generalized for all the 8 states as follows:

$$\frac{di_a}{dt} = \frac{e_a}{L} - \frac{R i_a}{L} - \frac{1}{3}\cdot\frac{Vc\cdot\{Ka - 0.5(Kb+Kc)\}}{L} \qquad (A.5)$$

$$\frac{di_b}{dt} = \frac{e_b}{L} - \frac{R i_b}{L} - \frac{1}{3}\cdot\frac{Vc\cdot\{Kb - 0.5(Ka+Kc)\}}{L} \qquad (A.6)$$

$$i_c = - i_a - i_b \qquad (A.7)$$

$$i_1 = 0.5\cdot(Ka\cdot i_a + Kb\cdot i_b + Kc\cdot i_c) \qquad (A.8)$$

where the corresponding switching functions Ka, Kb or Kc are equal to +1 when the phase is connected to the positive rail of the dc link and equal to -1 otherwise. For the 6th state the switching functions are Ka=Kc=-1 and Kb=1.

Each time that a switching action occurs, one of the switching functions reverses its sign and change the state equations given by eqs. (A.5) to (A.8). The switching action depends on the control strategy being used in the rectifier.

For example, in the case of current control with hysteresis band, the switching times are generated by intersections points defined by the interaction of the actual input current with the upper and lower sides of the hysteresis band. In the case of SPWM, the intersection points are defined when a sinusoidal reference is compared with a high frequency carrier, like a triangular or sawtooth wave.

A.1.2 The DC Voltage Feedback.

The dc voltage feedback is added to the rectifier system by replacing the dc supply with a dc capacitor. The dc capacitor voltage is measured and compared with a reference, from where an error signal is obtained. This error signal is used to command the input currents of the rectifier in either the Direct Control Method or the Indirect Control Method. The resultant set of algebraical and differential equations (already developed in Chapters II and III) is introduced in the software program and is combined with the switching algorithm given by eqs.(A.5) to (A.8). The Figure A.3 shows a simplified flowchart for the computer program. The question block about intersection points in Figure A.3 contains the information about the method of control that is being used: SPWM, Hysteresis or any other.

A.1.3 Program Examples.

Figure A.4 shows a program example for the SPWM control, and Figure A.5 for the series Type E topology.

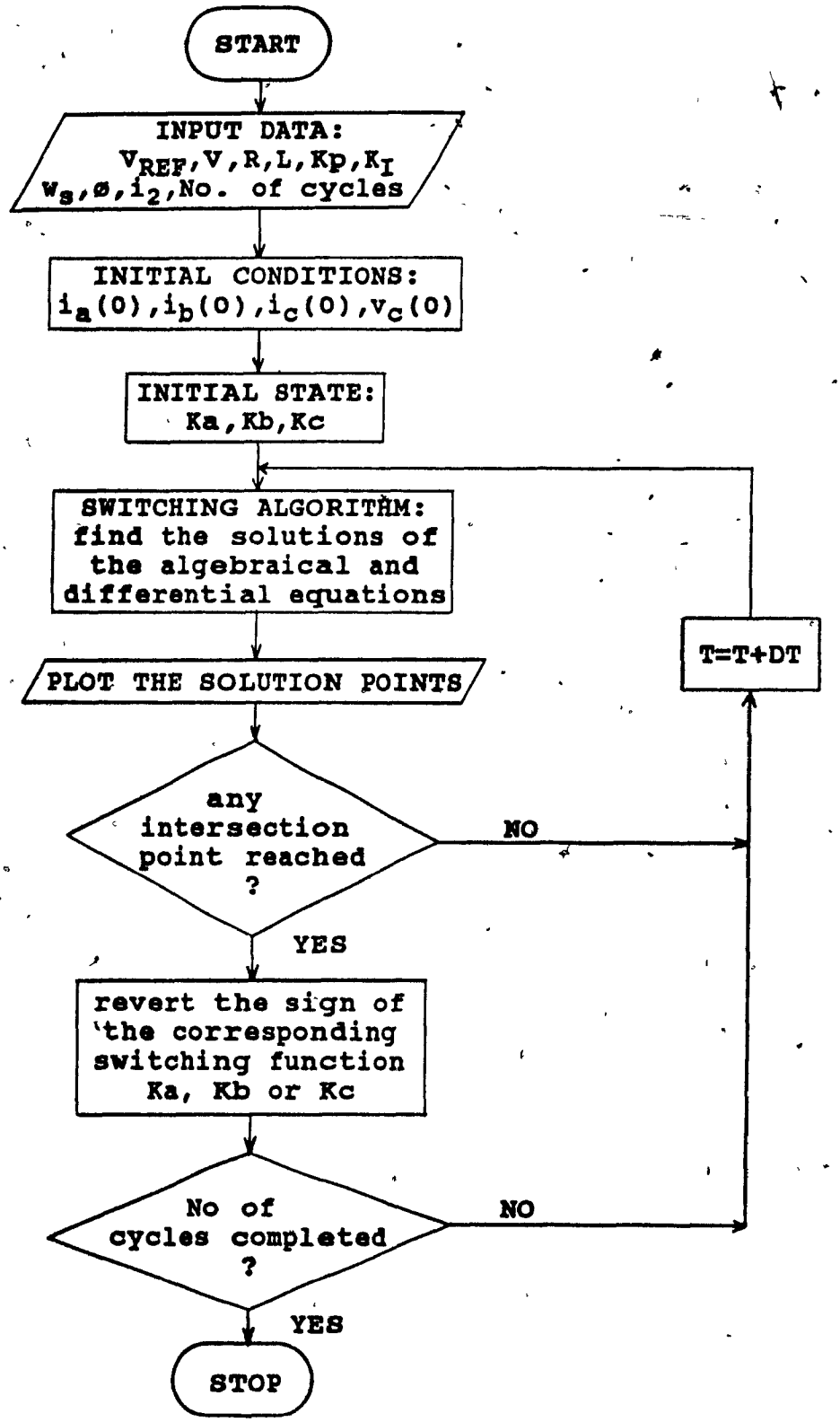


Fig.A.3 Rectifier Program Flowchart.

```
REM SPWMDIDT
REM SPWM rectifier with L*di/dt control block and triangular synchronized
READ PHIDEG,W,DT,VR,KP,KI,ICC,ICCF,MO
DATA 0,377,2e-5,110,2,0,0,3,0
SCREEN 2
PI=3.1415926535
 READ VLC,RC,LC,LB
 DATA 40,1, 0067, 0067
    VMC=SQR(2)*VLC
    LIM=VR/2
    XC=W*LC
    DTI=1/DT
    PERS=20*W
    PERT=PI/PERS
    MM=2*LIM/PERT
 READ VL,R,L,C
 DATA 30,1,.0067,.012
 RL=R/L
 VM=VL*1.41421356
 VDC=VR
 L3=3*L
 CI=1/C
 VML=VM/L
 VL13=VDC/L3
 TRIANG=LIM*SIN(2*PI)
 VL23=2*VL13
 FOR K=0 TO 220:PSET(3*K,60):PSET(3*K,130):NEXT K
 KA=1:KB=-1:KC=-1
   CYCLES=12
 ABI=ABS(ICCF)
 IF ABI=0 THEN ABI=1
 X5=7/ABI
 XV=35/VM
 PHI=.0174532925*PHIDEG
 Z0=38124!/CYCLES
 LINE (0,0)-(0,200)
 PSET(0,90)
 T=0
110  IA=IA+(VML*SIN(W*T)-RL*IA-VL13*(KA-.5*(KB+KC)))*DT
     IB=IB+(VML*SIN(W*T-2.0944)-RL*IB-VL13*(KB-.5*(KA+KC)))*DT
     IC=-IA-IB
       IDC=.5*(KA*IA+KB*IB+KC*IC)
     REF=SIN(PERS*T+2*PI)
   IF (REF-REF1)>0 THEN M=MM ELSE M=-MM
   IF REF1*REF<0 THEN TRIANG=0
   TRIANG=TRIANG+M*DT
   REF1=REF
        IF VTA>TRIANG THEN KA=1 ELSE KA=-1
        IF VTB>TRIANG THEN KB=1 ELSE KB=-1
        IF VTC>TRIANG THEN KC=1 ELSE KC=-1
     ITGB=-IA*X5+60
  LINE(TGP,ITGBP)-(TG,ITGB)
     ITGBP=ITGB
     DV=(IDC-ICC)*DT*CI
     VDC=VDC+DV
     VL13=VDC/L3
  IF TG>0 AND J=0 THEN J=J+1:ICC=ICCF
   IF TG>320 AND X=0 THEN X=X+1:ICC=-ICCF
     ITGA=-IDC*X5+130
     ITGC=-VR*XV+130
     LINE(TGP,ITGAP)-(TG,ITGA)
      LINE(TGP,ITGCP)-(TG,ITGC)
     ITGAP=ITGA
     ITGCP=ITGC
     TGP=TG
     TG=T*Z0
     IM=IM+1.41421356*(KI*(VR-VDC)*DT-KP*DV)
     VTA=(VMC-RC*IM-LB*(IM-IP)*DTI)*SIN(W*T)-XC*IM*COS(W*T)
     VTB=(VMC-RC*IM-LB*(IM-IP)*DTI)*SIN(W*T-2.0944)-XC*IM*COS(W*T-2.0944)
     VTC=-VTA-VTB
     IP=IM
     T=T+DT
        IF TG<640 THEN GOTO 110
150 GOTO 150
```

Fig.A.4 Program Example for SPWM Control.

```
  REM SSPWMTR2
  REM Series connection PWM rectifiers with triangular carriers shifted
  READ PHIDEG,W,DT,VR,KP,KI,ICC,N,ICCF,MM
  DATA 0,377,2e-5,120,2,0,0,7,-8,0
  DIM TRIANG(N),M(N),IA(N),IB(N),IC(N),KA(N),KB(N),IDC(N),REF(N)
  DIM DV(N),VM(N),VDC(N),VL13(N),VL23(N),L3(N),CI(N),VML(N),RL(N)
  DIM VL(N),R(N),L(N),C(N),ITGA(N),ITGB(N),ITGAP(N),ITGBP(N),REF1(N)
  SCREEN 2
  N80=120/N
  PI=3.1415926535
  LIM=VR/2
   READ VLC,RC,LC,LB
  DATA 40,1, 0067, 0087
      VMC=SQR(2)*VLC
      XC=W*LC
      DTI=1/DT
      PERS=10*W
      PERT=PI/PERS
      MM=2*LIM/PERT
   FOR I=1 TO N
   READ VL(I),R(I),L(I),C(I)
   DATA 40,1, 0067, 012
   DATA 40,1, 0067, 012
   DATA 40,1, 0067,.012
   DATA 40,1,.0067, 012
   DATA 40,1,.0067, 012
   DATA 40,1, 0067,.012
   DATA 40,1, 0067,.012
   RL(I)=R(I)/L(I)
   VM(I)=VL(I)*1 41421356
   VDC(I)=VR
   L3(I)=3*L(I)
   CI(I)=1/C(I)
   VML(I)=VM(I)/L(I)
   VL13(I)=VDC(I)/L3(I)
   TRIANG(I)=LIM*SIN(2*PI*I/N)
   VL23(I)=2*VL13(I)
   FOR K=0 TO 220 PSET(3*K,N80*I) PSET(3*K,165):NEXT K
   KA(I)=1:KB(I)=-1 KC(I)=-1
     NEXT I
     CYCLES=5
   ABI=ABS(ICCF)
   IF ABI=0 THEN ABI=1
   X5=70/N/ABI
   X6=2.8*X5/N
   PHI=.017453292E*PHIDEG
   ZO=38124!/CYCLES
   LINE (0,0)-(0,200)
   PSET(0,90)
   T=0
110    FOR I=1 TO N
    IA(I)=IA(I)+(VML(I)*SIN(W*T)-RL(I)*IA(I)-VL13(I)*(KA(I)- 5*(KB(I)+KC(I))))*
DT
    IB(I)=IB(I)+(VML(I)*SIN(W*T-2.0944)-RL(I)*IB(I)-VL13(I)*(KB(I)-.5*(KA(I)+KC
(I)))*DT
    IC(I)=-IA(I)-IB(I)
     IDC(I)=.5*(KA(I)*IA(I)+KB(I)*IB(I)+KC(I)*IC(I))
  REF(I)=SIN(PERS*T+2*PI*I/N)
  IF (REF(I)-REF1(I))>0 THEN M(I)=MM ELSE M(I)=-MM
  IF REF1(I)*REF(I)<0 THEN TRIANG(I)=0
  TRIANG(I)=TRIANG(I)+M(I)*DT
  REF1(I)=REF(I)
      IF VTA>TRIANG(I) THEN KA(I)=1 ELSE KA(I)=-1
      IF VTB>TRIANG(I) THEN KB(I)=1 ELSE KB(I)=-1
      IF VTC>TRIANG(I) THEN KC(I)=1 ELSE KC(I)=-1
   ITGB(I)=-IA(I)*X5+N80*I
 LINE(TGP,ITGBP(I))-(TG,ITGB(I))
   ITGBP(I)=ITGB(I)
   DV(I)=(IDC(I)-ICC)*DT*CI(I)
   VDC(I)=VDC(I)+DV(I)
   VL13(I)=VDC(I)/L3(I)
   IREB=IREB+IA(I)
 IF TG>10 AND J=0 THEN J=J+1 ICC=ICCF
  IF TG>320 AND X=0 THEN X=X+1:ICC=-ICCF
  NEXT I
   ITGA=-IREB*X6+165
   LINE(TGP,ITGAP)-(TG,ITGA)
   ITGAP=ITGA
   IREB=0
  TGP=TG
  TG=T*ZO
  IM=IM+1 4142135b*(KI*(VR-VDC(N))*DT-KP*DV(N))
  VTA=(VMC-RC*IM-LB*(IM-IP)*DTI)*SIN(W*T)-XC*IM*COS(W*T)
  VTB=(VMC-RC*IM-LB*(IM-IP)*DTI)*SIN(W*T-2.0944)-XC*IM*COS(W*T-2 0944)
  VTC=-VTA-VTB
  IP=IM
  T T+DT
     IF TG<640 THEN GOTO 110
150 GOTO 150
```

Fig.A.5 Valve-by-Valve Simulation for Series Type E.

A.2 Mathematical Simulations.

The mathematical simulations consist of numerical integration of the state equations of each particular system and configuration described in this Thesis. These equations neglect the ripple harmonics and only embody the fundamental Fourier component. For example, the Direct Current Control Method, using a simple proportional control is described by the set of equations:

$$i_a(t) = I(t) \cdot \sqrt{2} \cdot \sin(wt+\phi) \qquad (A.9)$$

where $i_a(t)$ is the input current of the rectifier (phase a), ϕ is the desired power factor angle of operation and I(t) is obtained from the dc voltage regulated, feedback control loop:

$$I(t) = Kp^* (V_{REF} - v_c) \qquad (A.10)$$

The link between the input rms current I(t) and the output dc current i_1 is obtained from the Power Balance Equation:

$$v_c \cdot i_1 = 3 \cdot V \cdot I(t) - 3 \cdot R \cdot I(t)^2 - \frac{3L}{2}\frac{d}{dt} I(t)^2 \qquad (A.11)$$

and the link between the output dc current i_1 and the load dc current i_2, from the dc capacitor equation:

$$\frac{dv_c}{dt} = \frac{i_1 - i_2}{C} \qquad (A.12)$$

Figure A.6 shows a program example of the mathematical simulation for the Direct Current Control Method and Figure A.7 shows the mathematical simulation developed for the series Type C configuration.

A.3 Other Simulation Programs.

Figure A.8 shows the program used to get the Nyquist plots of Chapter III. Many other simulations were developed but they will not be displayed here.

```
' STEP
' Direct Current Control  Step reversal of power
  CYCLES=20
    READ I2,VL,VR,L,C,KP,R
    DATA 10,40,120, 005, 012,3, 5
 IABS=ABS(I2)
    AMPLITUDE=1
    SCREEN 2
       IF IABS<1 THEN IABS=1
 LOCATE 23,15 PRINT "I2 =",I2;"A       L = ";L;"H       R =";R;"Ohm "
   X5=30/(1 8*IABS)*AMPLITUDE
    LOCATE 25,15 PRINT "Vref =";VR;"V     C =";C;"F       VL =";VL
    LOCATE 2,2 PRINT "I"
    READ W,DT2,I1,I,PHIDEG
     LINE(0,0)-(0,180)
    DATA 377.1e-5,0,0,0
      FOR K=0 TO 220 PSET(3*K,60):PSET(3*K,120):NEXT K
  DT=DT2*CYCLES
     PHI=3 1415926E*PHIDEG/180
     VA0=3*VL*COS(PHI)
     Z0=38124'/CYCLES
     VDC=VR
     L3=3*L
     R3=3*R
     SQ=SQR(2)
     KPL=3*KP*L
     CI=1/C
    DTI=1/DT
    T=0
500 ITA=IM*SIN(W*T+PHI)
    TG=T*Z0
    ITGA=-ITA*X5+60
       LINE(TGP,ITGAP)-(TG,ITGA)
    ITGB=-I1*X5+120
       LINE(TGP,ITGBP)-(TG,ITGB)
    TGP=TG
    ITGAP=ITGA
    ITGBP=ITGB
                T=T+DT
     IP=I
        IF TG>650 THEN GOTO 2000
     VDC=(I1-I2)*DT*CI+VDC
     I KP*(VR-VDC)
        I1=1*(VA0-R3*I-L3*(I-IP)*DTI)/VDC
     IM=SQ*I
     IF TG>284 AND N=0 THEN N=N+1 I2=-I2
     GOTO 500
2000 GOTO 2000
```

Fig.A.6 Mathematical Simulation of the Direct Current Control

```
'MATHSERC
' Mathematical simulation for Series Case C
    SCREEN 2
    CYCLES=25
  READ W1,RN,LN,LB,CN,KP,KI,VREF
  DATA 40,1.1,.0066, 0, 006,2,0,120
  READ vJ,RJ,LJ,CJ
  DATA 40,1.1,.0066,1e-3
'Initial conditions
    VCN=VREF:VCJ=VREF
    I1N=0:I1J=0
    IN=0:IJ=0
  READ W,DT2,I2,I2F,PHIDEG
  DATA 377,1E-5,0,6,0
    IABS=ABS(I2F)
    AMPLITUDE=1
    X5=15/(1.8*IABS)*AMPLITUDE
    XV=20/VREF
    LINE(0,0)-(0,199)
   FOR M=0 TO 220:PSET(3*K,71):PSET(3*K,105):PSET(3*K,163):PSET(3*K,199):NEXT K
    DT=DT2*CYCLES
    L3=3*LN:R3=3*RN
    XN=W*LN:XJ=W*LJ
    PHI=3.1415926*PHIDEG/180
    V3=3*VN*COS(PHI)
    Z0=38124/CYCLES
    SQ2=SQR(2):SQ3=SQR(3)
    CNI=1/CN:CJI=1/CJ
    LNI=1/LN:LJI=1/LJ
    DTI=1/DT
  T=0
50  IAN=INM*SIN(W*T+PHI)
    IAJ=IJM*SIN(W*T+PHIJ)
    TG=T*Z0
       ITGA=-IAJ*X5+71
       ITGB=-IAN*X5+105
       ITGC=-VCJ*XV+163
       ITGD=-VCN*XV+199
  LINE(TGP,ITGAP)-(TG,ITGA)
  LINE(TGP,ITGBP)-(TG,ITGB)
  LINE(TGP,ITGCP)-(TG,ITGC)
  LINE(TGP,ITGDP)-(TG,ITGD)
       ITGAP=ITGA
       ITGBP=ITGB
       ITGCP=ITGC
       ITGDP=ITGD
       TGP=TG
    DVCN=(I1N-I2)*DT*CNI
    VCN=VCN+DVCN
    IP=IN
    IN=IN+KI*(VREF-VCN)*DT-KP*DVCN
  I1J=-SQ3*(IN*XN*IDJ+(VN-RN*IN-LB*(IN-IP)*DTI)*IQJ)/VCN
    DVCJ=(I1J-I2)*DT*CJI
    VCJ=VCJ+DVCJ
  I1N=1N*(V3 R3*IN 4.3*(IN IP)*DTI)/VCN
IDJ IDJ+(SQ3*VCJ*XN*IN*LJI/VCN RJ*LJI*IDJ+W*IQJ)*DT
IQJ=IQJ+CQ3*VCJ*LJI*((VN RN*IN)*DT LB*(IN IP))/VCN (SQ3*Z)*LJI*W*IDJ*LB*LJI*IQJ
)*DT
   IF IQJ<>0 THEN PHIJ=ATN(-IDJ/IQJ)
    IJ=-SQR(IDJ*IDJ+IQJ*IQJ)*SGN(IQJ)/SQ3
      INM=SQ2*IN
      IJM=SQ2*IJ
    T=T+DT
     IF TG>80 THEN CJ=CJ- 01*CJ+CJI-1/CJ
    IF VCJ>3*VCJ THEN GOTO 80
  IF TG>75 AND N=0 THEN N=N+1 I2=I2F
  IF TG>320 AND M=0 THEN M=M+1:I2=-I2F
  IF TG<640 THEN GOTO 50
80   LOCATE 1,3:PRINT " Ij =",INT(IJ*100)/100;"  In =";INT(IN*100)/100;"  In*SQ3
 = , INT(IN*SQ3*100)/100,"  Vcj =",INT(VCJ*100)/100;"  Vcn ",INT(VCN*100)/100
  LOCATE 3,3:PRINT   Idj  ",INT(IDJ*100)/100;"  Iqj  ",INT(IQJ*100)/100,"  PHI
 - ;INT(PHIJ*18000/3 1415926)/100;"  Vref =";VREF;"  Kp =",KP;"  KI =",KI
  LOCATE 5,3:PRINT " Vn =",VN;" Vj =";VJ;" Rn =";RN;" Rj =",RJ;" Ln =";LN," LJ
 ",LJ;" I2 =",I2
  LOCATE 18,25 PRINT " Cj = ,CJ*1000000," uF "
  LOCATE 22,25:PRINT " Cn =",CN*1000000;" uF"
100 GOTO 100
```

Fig.A.7 Mathematical Simulation for Series Type C

```
  'NYQGEN
'Nyquist plot for SPWM system
SCREEN 2
READ KD,KP,KI,RC,LC,LB
DATA 0,3,0,.5,.005,.002
S$="Stable"
U$="Unstable"
READ R,L,C,V,VC
DATA .5, 005, .004,40,120
WS=377
X=WS*L
XC=WS*LC
IO=12
N=0
' ZI,ZR are scale factors for graphics. ZR may be 15 or 150
ZR=150
ZI=70
D=R/L
KO=SQR(3)/(VC*C)
  FOR K=0 TO 220 PSET(3*K,60):NEXT K
  LINE(370,0)-(370,199)
  LINE(220,56)-(220,64)
  LOCATE 7,27:IF ZR=150 THEN PRINT "-1" ELSE PRINT " -10"
  LOCATE 1,50:PRINT "Im[G(jw)]"
  LOCATE 9,72 PRINT "Re[G(jw)]"
5  ID=SQR(3)*IO*(R*XC-X*RC)/(R*R+X*X)
   IQ=-SQR(3)*IO*(R*RC+X*XC)/(R*R+X*X)
     A3=LB*IQ
     A2=(RC+2*LB*R/L)*IQ-XC*ID+SQR(3)*(V-RC*IO)*LB/L
     A1=2*R*(RC*IQ-XC*ID)/L+LB*IQ*(R*R+X*X)/(L*L)-SQR(3)*XC*(XC-WS*LB)*IO/L+SQR(
3)*(V-R*IO)*(RC*L+LB*R)/(L*L)
     A0=SQR(3)/(L*L)*(V*(R*RC+X*XC)-2*IO*(RC*(R*RC+X*XC)+XC*(R*XC-X*RC)))
                  AA5=A3*KD
            AA4=A3*KP+A2*KD
       AA3=A3*KI+A2*KP+A1*KD
       AA2=A2*KI+A1*KP+A0*KD
       AA1=A1*KI+A0*KP
       AA0=A0*KI
  W=-1E6
  W2=W*W-WS*WS-D*D
   RW=AA4*W*W*W*W-AA2*W*W-AA0
   IW=AA5*W*W*W*W*W-AA3*W*W*W+AA1*W
    DENO=W*W*(W2*W2+4*D*D*W*W)
    REJW=KO*(RW*W2-2*IW*W*D)/DENO
    IMJW=KO*(2*RW*W*D+IW*W2)/DENO
  REALP=REJW*ZR+370
  IMAGP=-IMJW*ZI+60
 W=10000
10  W2=W*W-WS*WS-D*D
    RW=AA4*W*W*W*W-AA2*W*W+AA0
    IW=AA5*W*W*W*W*W AA3*W*W*W+AA1*W
    POL1=SGN(IMJW)
    DENO=W*W*(W2*W2+4*D*D*W*W)
    REJW=KO*(RW*W2-2*IW*W*D)/DENO
    IMJW=KO*(2*RW*W*D+IW*W2)/DENO
    REAL=REJW*ZR+370
    IMAG=-IMJW*ZI+60
     LINE(REALP,IMAGP)-(REAL,IMAG)
    REALP=REAL
    IMAGP=IMAG
   'PRINT " Re[G(jw)] =",REJW,"Im[G(jw)] =",IMJW,"w = ",W
    W=W- 01*W
    POL2=SGN(IMJW)
    IF POL1+POL2=0 THEN CRIT=REJW
    IF IMAG<299 AND REAL>-5000 THEN GOTO 10
    IF CRIT<-1 THEN R$=U$ ELSE R$=S$
    LOCATE 11+2*N,50:PRINT"Lb=";LB;",",R$;"  (";INT(CRIT*1000)/1000;")"
    CRIT=0
    N=N+1
   IF N=1 THEN LB=LB+ 001 GOTO 5
    IF N=2 THEN LB=LB+ 001 GOTO 5
    IF N=3 THEN LB=LB+ 001 GOTO 5
    LOCATE 19,50 PRINT "R =",R;" L =";L;" C =",C
    LOCATE 21,50 PRINT "Ro=",RC;" Lc=";LC;" Io=";IO
    LOCATE 23,50 PRINT "V =";V;" Vc =";VC;" Kp =";KP
'   LOCATE 23,50 PRINT "Kd =",KD;" Ki =";KI
'   PRINT " w =",W,"Re[G(0)] =";-KP*(B*(WS*WS+D*D)-2*D*C)/((WS*WS+D*D)^2)
200 GOTO 200
```

Fig.A.8 Nyquist Plot Computer Program.

APPENDIX B

APPENDIX B

PRACTICAL IMPLEMENTATION.

B.1 Introduction

The experimental work has been the most relevant and time consuming part of this research. For this reason, it is important to show and briefly describe the implementation of the hardware which made it possible to verify the theory and the digital simulations.

The Figure B.1 shows a photograph of the complete arrangement of two three-phase Boost Type PWM Rectifier Units, implemented for the experimental work. The hardware for each Rectifier Unit is divided in two groups: the Power Unit and the Control Unit. The Power unit is common to all the topologies and methods of control. The Control Unit changes with the control strategy and/or the configuration to be used. Each Power Unit has three Power Modules: one for each phase of the mains. The control unit has components that are common to the three phases and others that are in triplicate.

B.2 The Power Units.

The Power Unit of each rectifier has 3 Power Modules. For the implementation of each Power Module, printed circuit board technology was adopted. Emphasis was directed towards modularity and interchangeability of circuit boards.

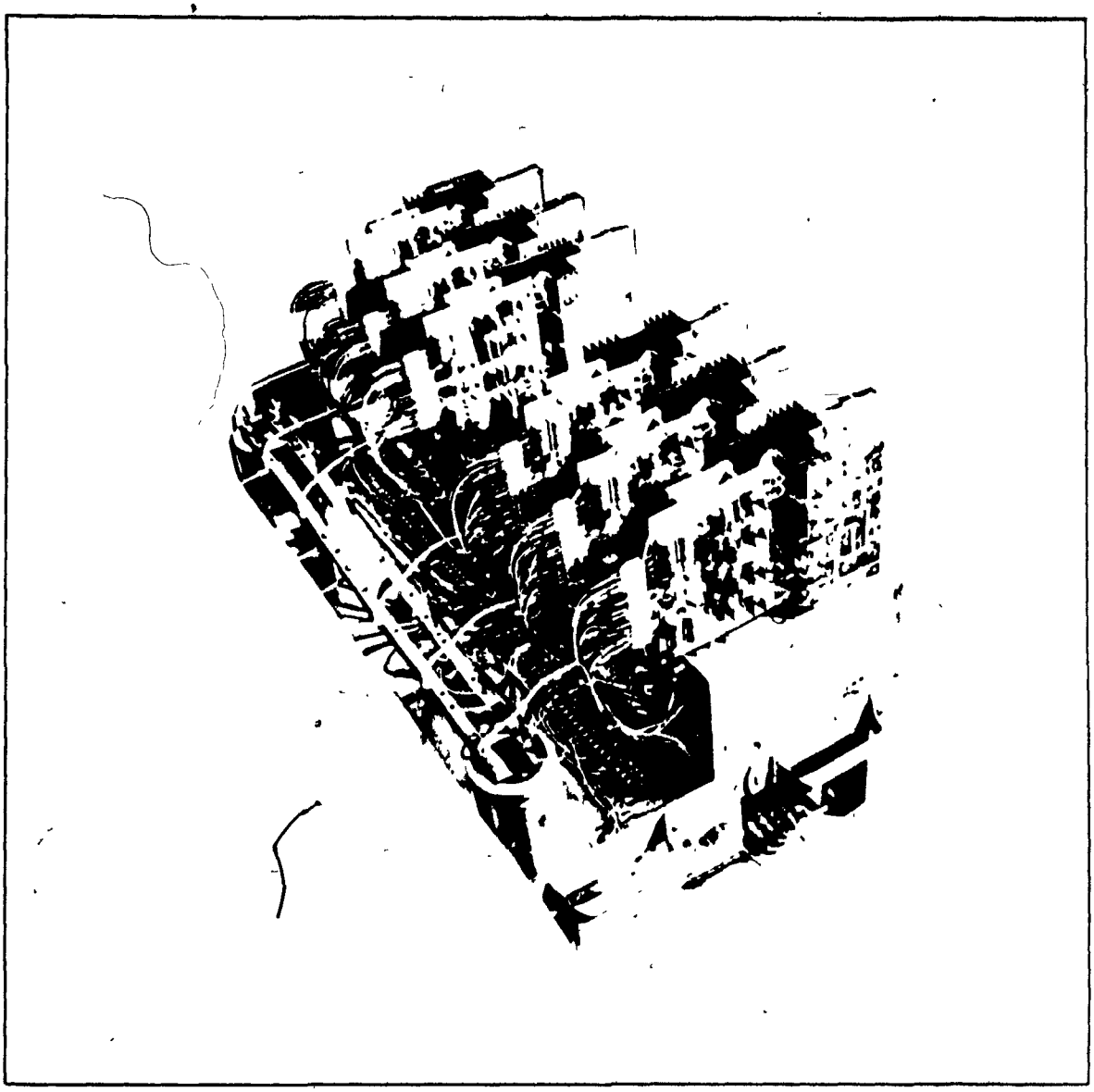
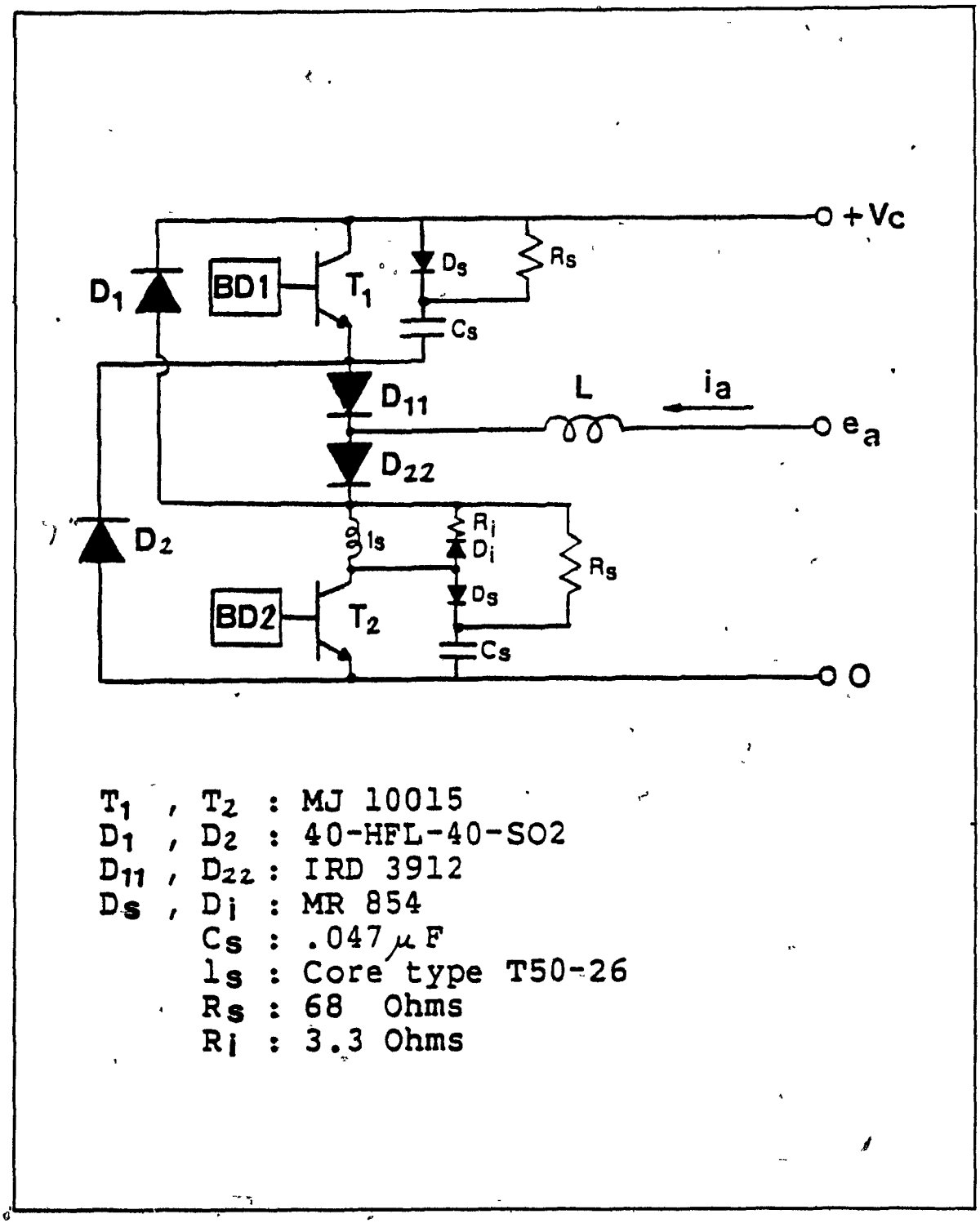


Fig.B.1 Two-Converter Arrangement for Experimental Work.

Each Power Module is formed by two Power Darlingtons, the snubber circuits and two Base Drives. Figures B.2 and B.3 show the snubber protection circuit and one of the Base Drives respectively. Figure B.4 shows a photograph of one of the Power Modules.



T_1 , T_2 : MJ 10015
D_1 , D_2 : 40-HFL-40-SO2
D_{11} , D_{22} : IRD 3912
D_s , D_i : MR 854
C_s : .047 μF
l_s : Core type T50-26
R_s : 68 Ohms
R_i : 3.3 Ohms

Fig.B.2 Snubber Protection Circuit for Phase "a".

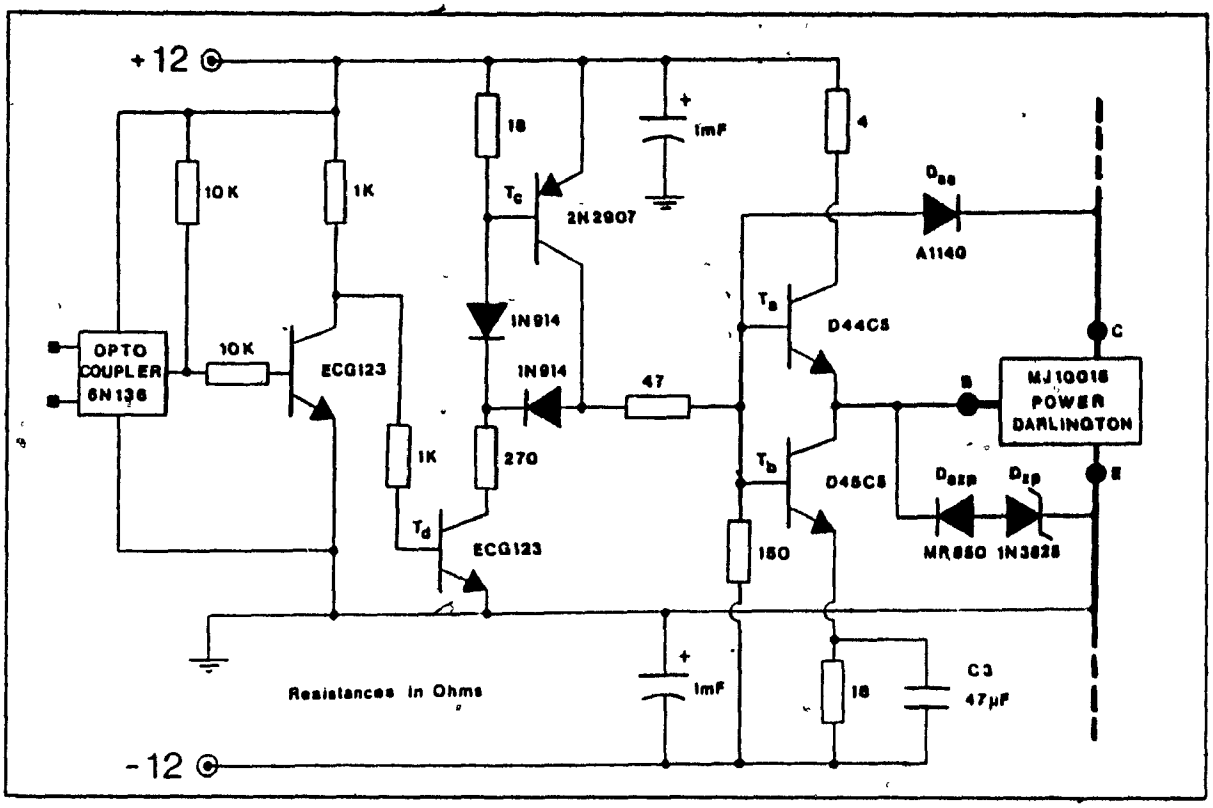


Fig.B.3 Base Drive (BD) Unit.

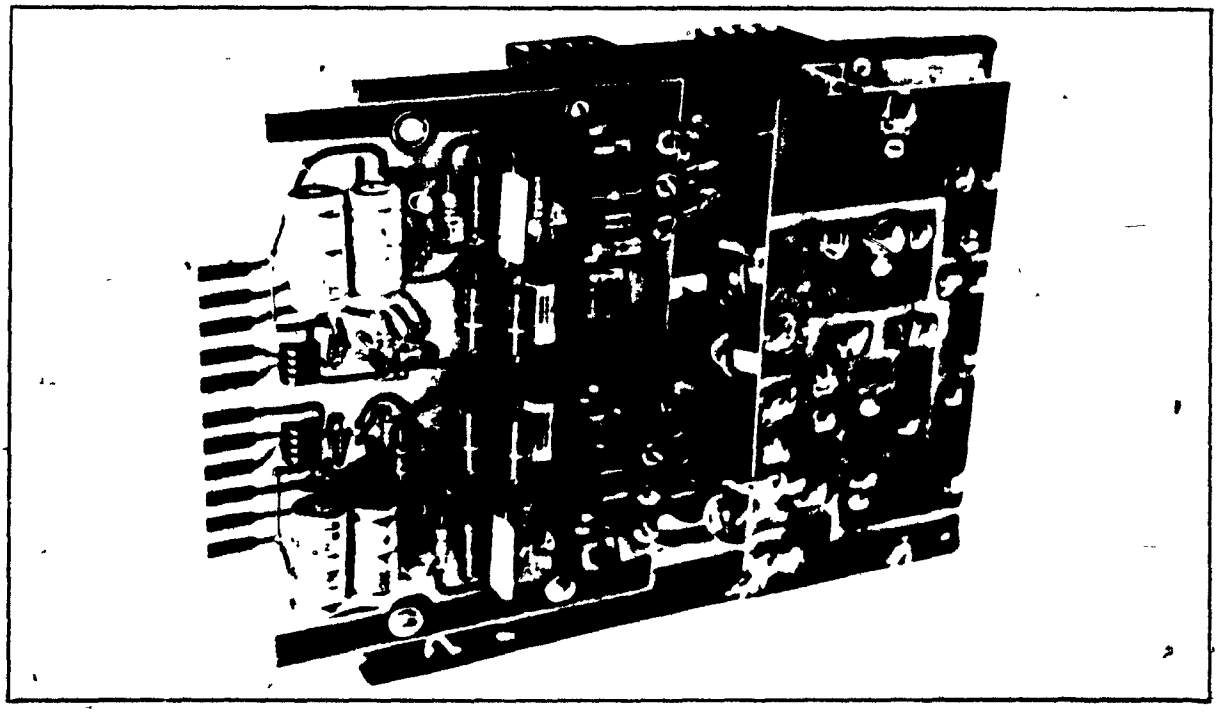


Fig.B.4 Power Module.

B.3 The Control Units.

There is a part common to all Control Units: the dc voltage feedback, which generates the amplitude of the input current command "I" for both, the Direct and the Indirect Current Control Methods. Figure B.5 shows this common part of the Control Units, with PI control.

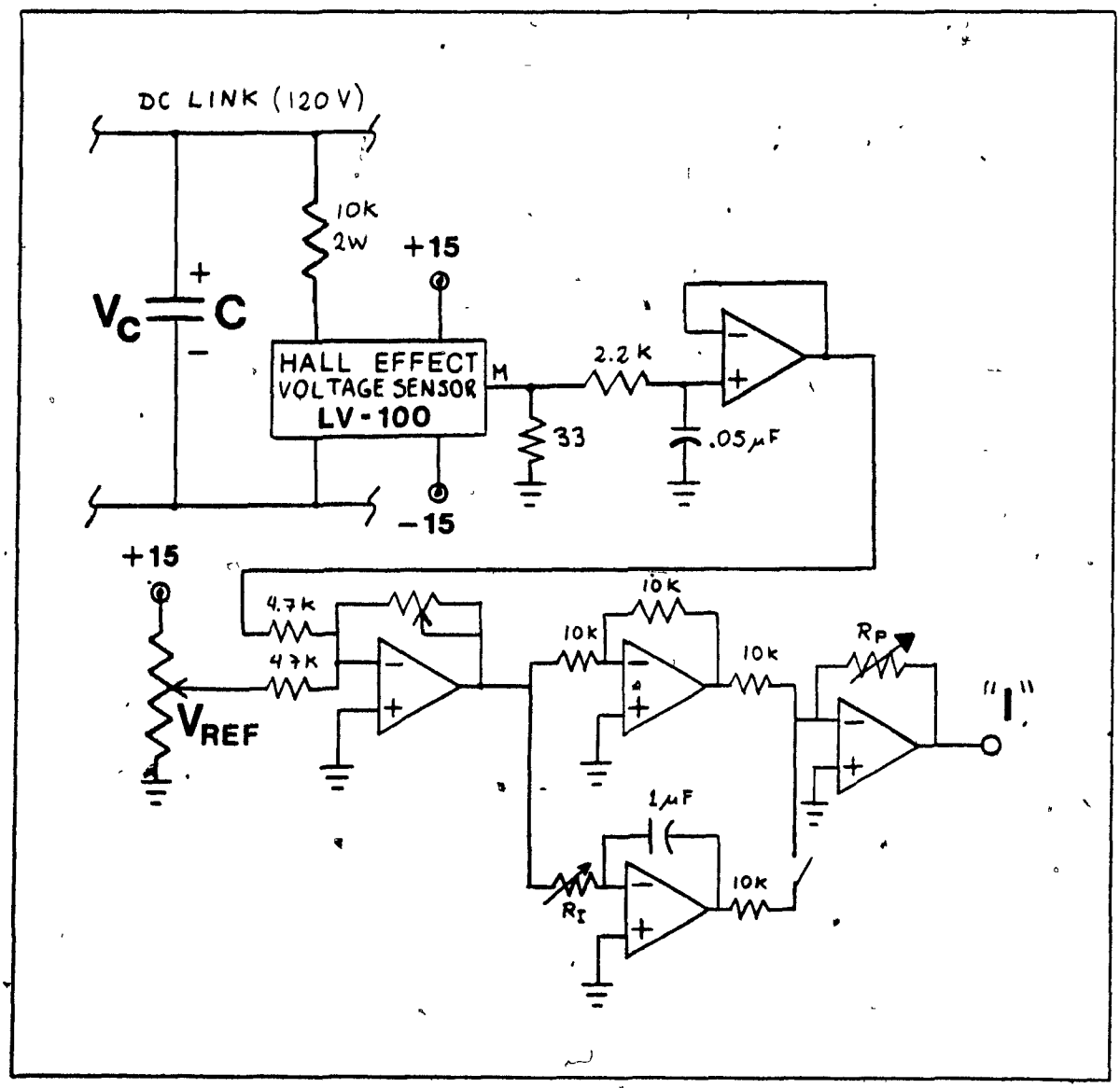


Fig.B.5 Generation of the Current Command "I" Through the DC Voltage Feedback.

The rest of the hardware is different for each type of control method and will be described separately.

B.3.1 Current Hysteresis Control.

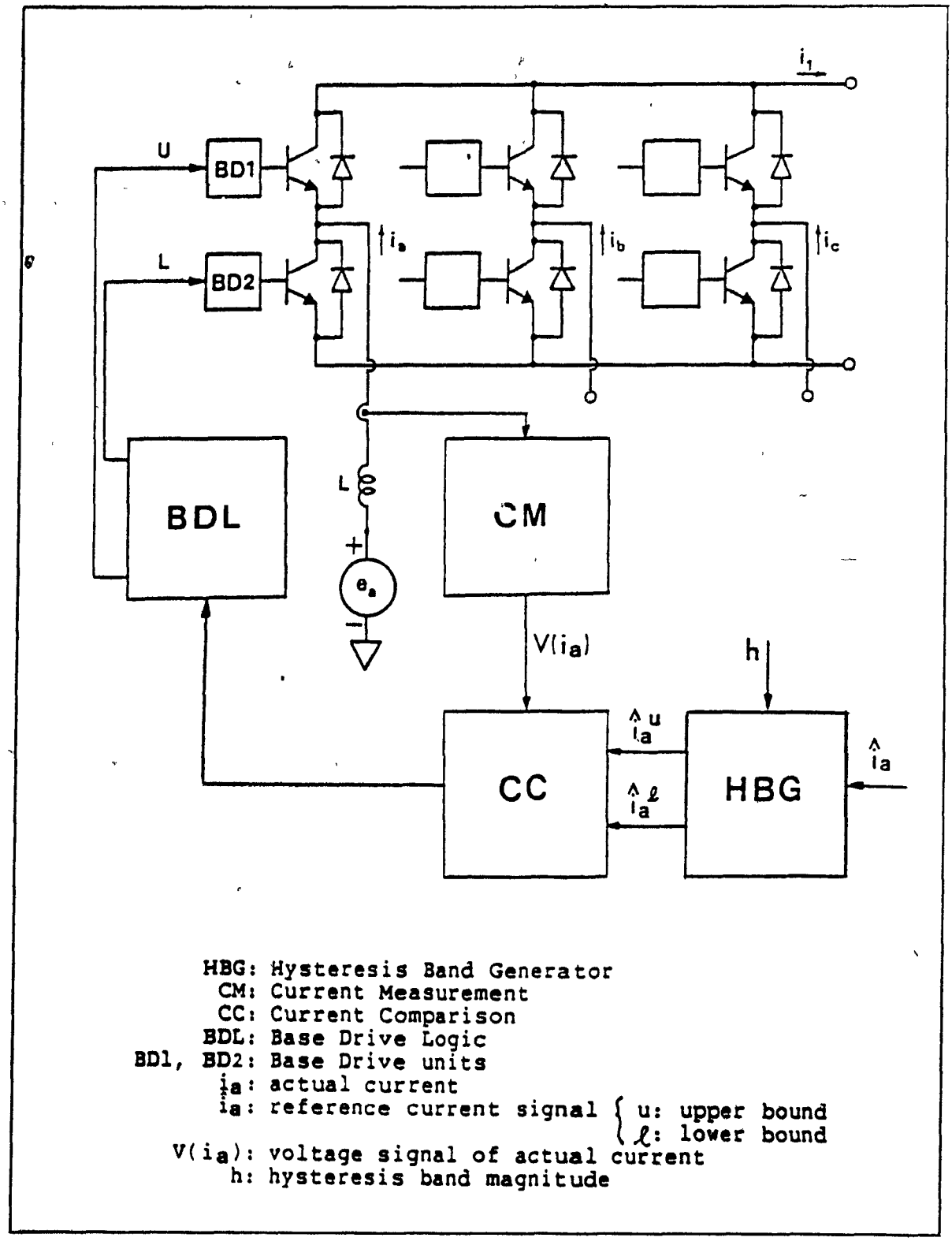
The Current Hysteresis Control was the method used to implement the Direct Control. The block diagram implementation of the current hysteresis control for one phase is shown in Figure B.6. Each block will be explained separately.

B.3.1.1 Hysteresis Band Generator (HBG).

This circuit produces the upper and lower reference bounds with hysteresis bandwidth "h" and offset adjustments. Figure B.7 shows the circuit for one phase. The rms value of the reference current signal $\hat{I}_a$, shown in this Figure and in Figure B.6, is precisely the current command "I" generated in the dc voltage feedback, which has been multiplied by sin $w_s t$ ($\hat{I}_a = I \cdot \sin w_s t$). The sinusoidal waveform template "sin $w_s t$" has been taken from the supply voltage.

B.3.1.2 Current Measurement (CM).

The current measurement block uses a commertially available Hall Effect Current Transducer [53,54]. Its frequency response goes from dc to 100 kHz. The circuit is shown in Figure B.8.



HBG: Hysteresis Band Generator
CM: Current Measurement
CC: Current Comparison
BDL: Base Drive Logic
BD1, BD2: Base Drive units
i_a: actual current
$\hat{i}_a$: reference current signal { u: upper bound; ℓ: lower bound }
V(i_a): voltage signal of actual current
h: hysteresis band magnitude

Fig.B.6 Current Hysteresis Control for One Phase.

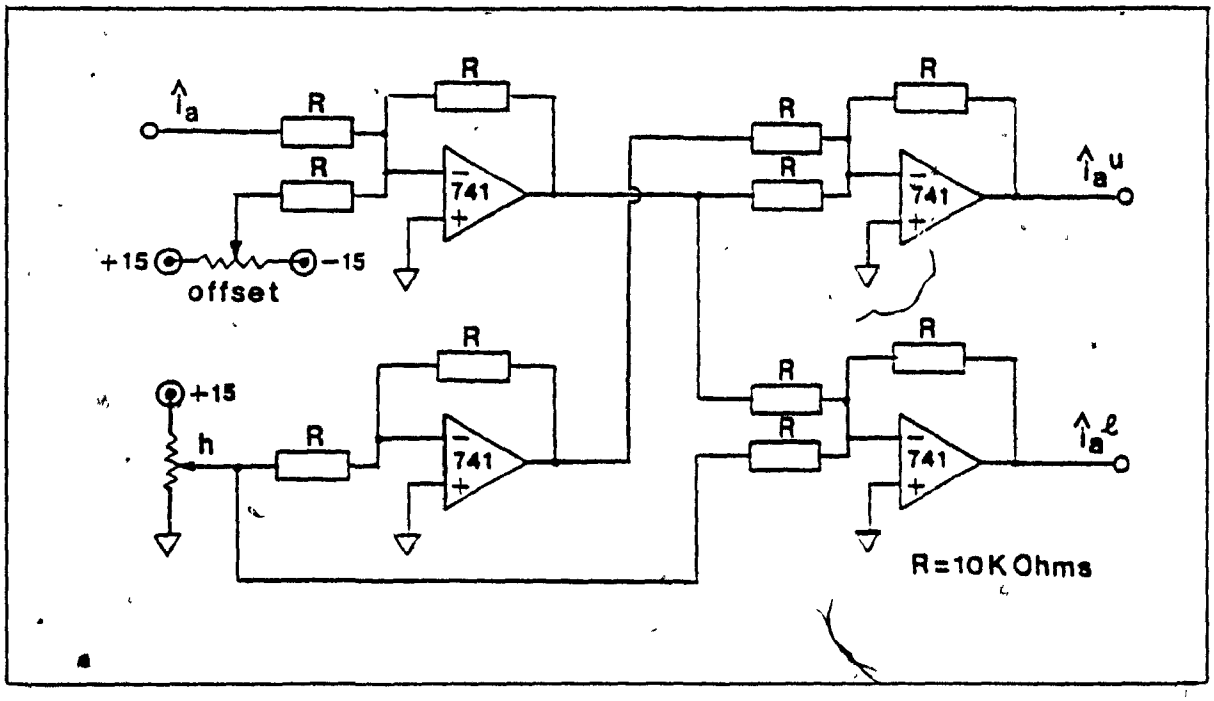


Fig.B.7 Hysteresis Band Generator (HBG).

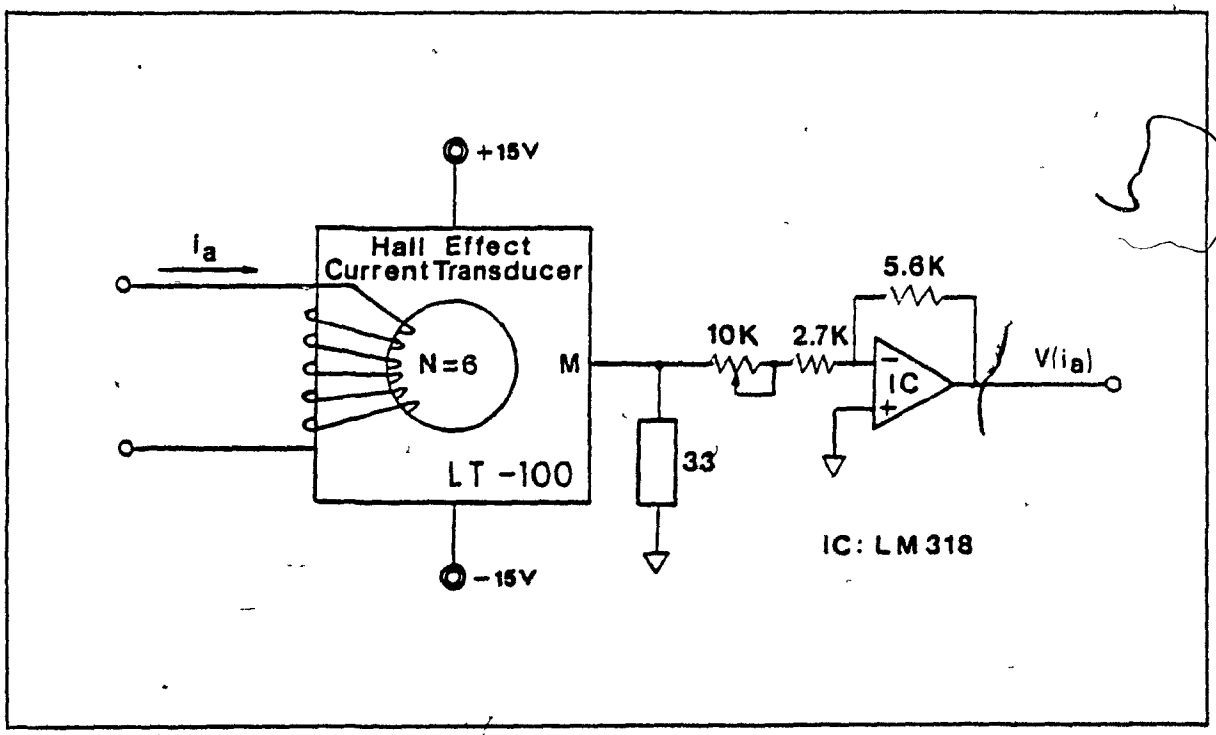


Fig.B.8 Current Measurement (CM) Circuit.

B.3.1.3 Current Comparison (CC).

The circuit of the Current Comparison is given in Figure B.9. The input signals are: the upper and the lower bound reference currents coming from the HBG circuit (Figure B.7) and the actual current signal $v(i_a)$ coming from the CM circuit (Figure B.8). Its output contains the modulated signals which go to the Base Drive Logic (BDL) circuit.

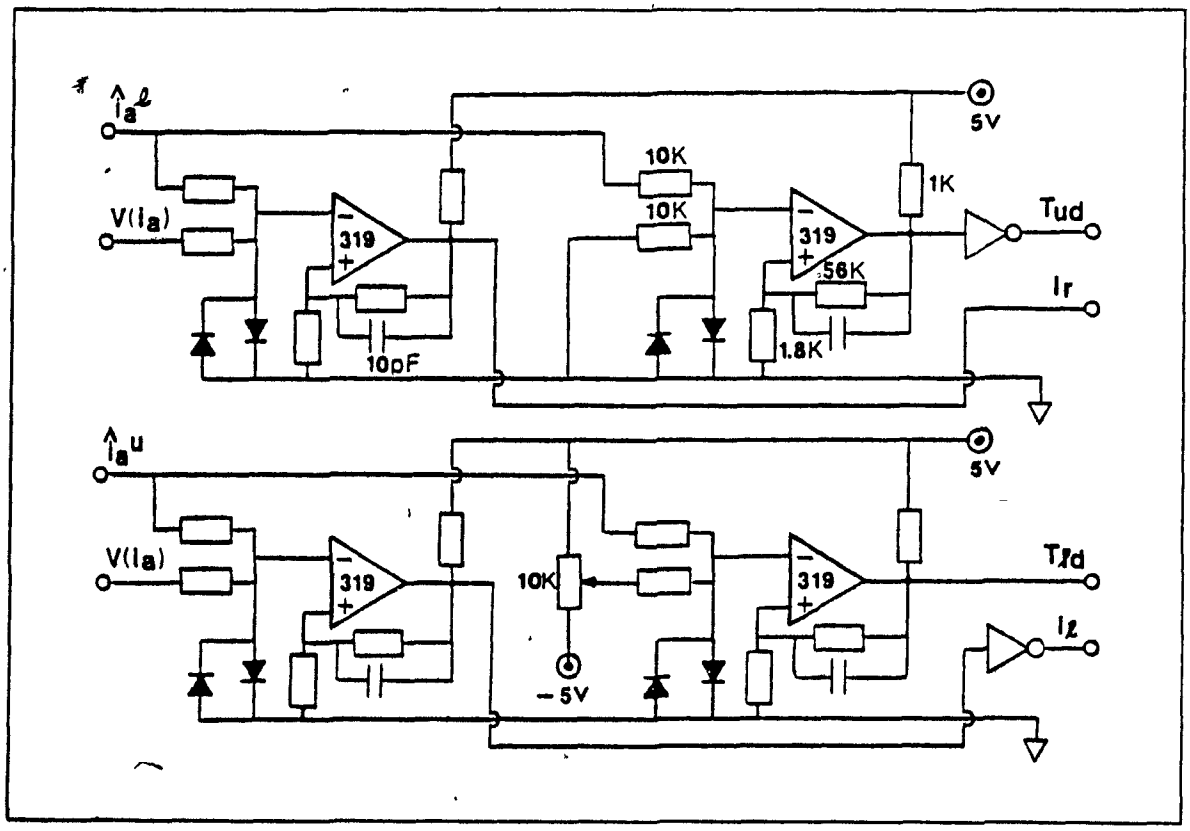


Fig.B.9 Current Comparison (CC) Circuit.

The output signals I_r and I_l in Figure B.9 are the normal signals to the Base Drive Logic to raise and lower the phase level current.

However, these signals are inhibited at the gate unless enabling signals are sent by two supplementary output signals, Tud and Tld. The purpose of the enabling signals is two-fold:

a) to reduce switching and consequently losses of the Base Drive circuit.

b) to avoid the danger of shoot-through due to simultaneous firing of the upper and the lower transistor.

B.3.1.4 Base Drive Logic (BDL).

This circuit ensures again that the upper and lower transistors cannot be ON at the same time, and that the delay between the turning OFF of one transistor to the turning ON of the other transistor is controlled by the clock period. This circuit is shown in Figure B.10.

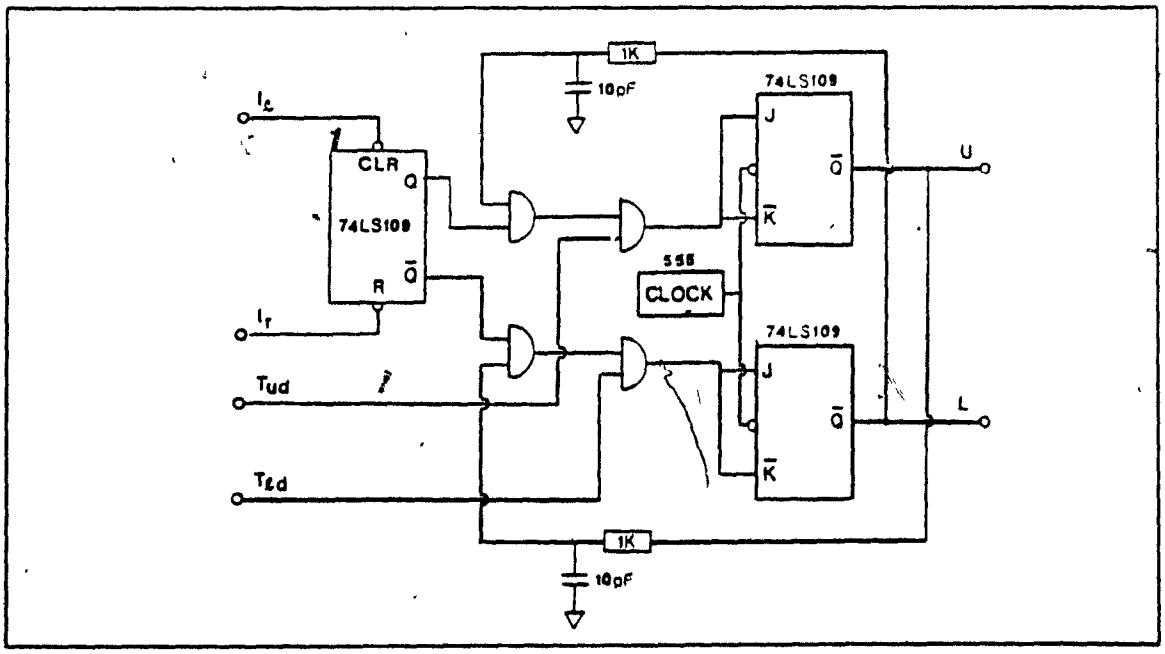


Fig.B.10 Base Drive Logic (BDL) Circuit.

B.3.2 Sinusoidal PWM (SPWM) Control.

The SPWM control was the method used for the Indirect Current Control Method. The block diagram is shown in Figure B.11.

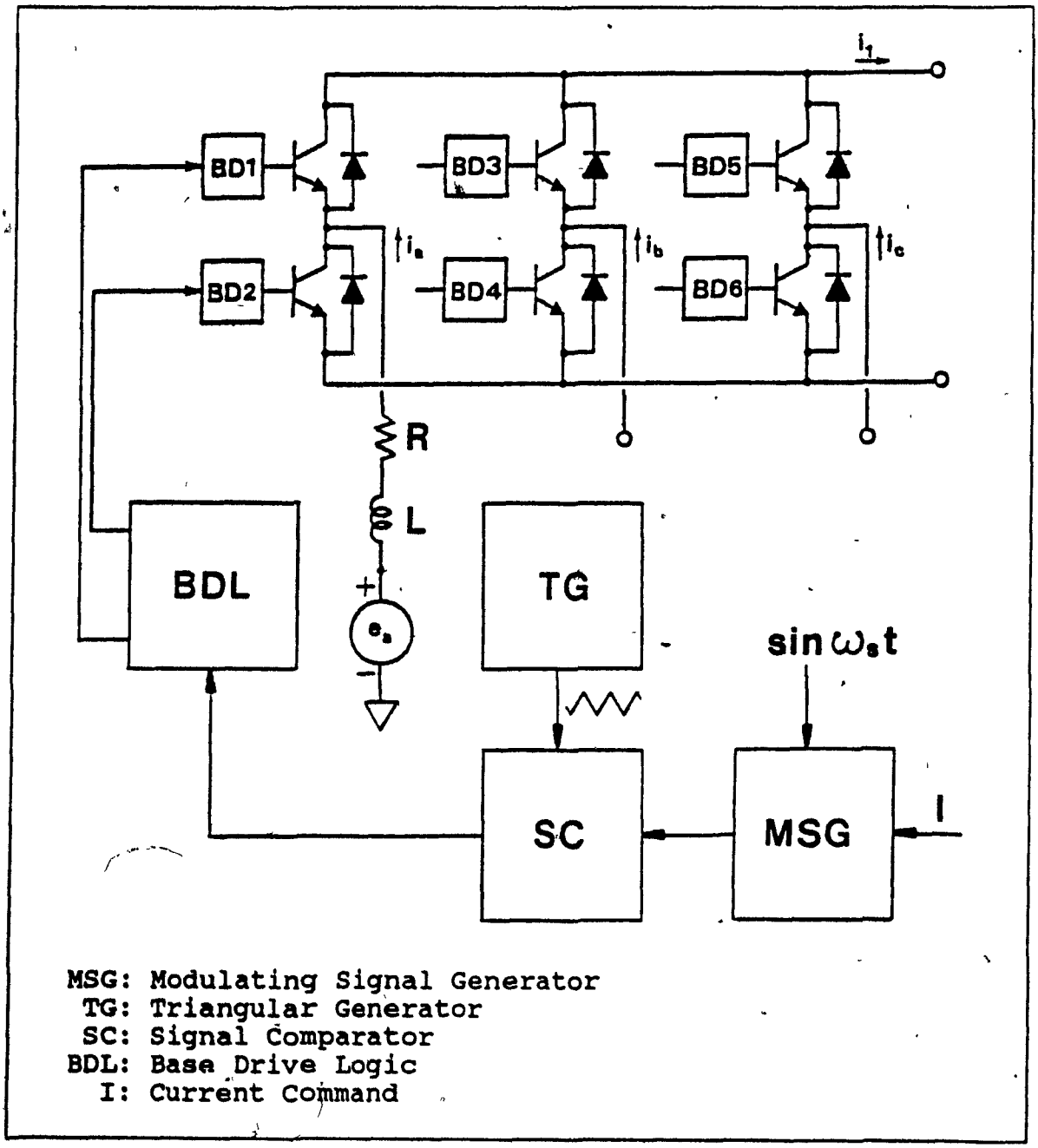


Fig.B.11 SPWM Control for One Phase.

B.3.2.1 Modulating Signal Generator (MSG).

The Modulating Signal Generator is the most important block in the SPWM control. Its input signals are the current command "I" and the sinusoidal references $\sin w_s t$, $\sin(w_s t - 120^o)$ and $\sin(w_s t - 240^o)$ from the voltage supply. The outputs are the modulating signals for each one of the three phases: v_{moda}, v_{modb} and v_{modc}. For instance, the phase "a" of this circuit obeys the relation given by eq.(3.10). The Figure B.12 shows the implementation of the MSG circuit. This circuit has been designed to match the values of the parameters of the experimental rectifier: X=2.5 ohms and R=1 ohm.

B.3.2.2 Triangular Generator (TG).

The Triangular Generator circuit produces the triangular carrier whose function is to define the switching intervals in the modulating signal. The Figure B.13 shows this circuit.

B.3.2.3 Signal Comparator (SG).

The Signal Comparator produces the SPWM modulated signals which go to the BDL (Base Drive Logic) circuit. Its inputs are the triangular carrier e_T and the modulating signals v_{moda}, v_{modb} and v_{modc}. The circuit is quite similar to the CC circuit of Figure B.9 and it is not shown here.

The Base Drive Logic (BDL) circuit of the SPWM control is the same as of Figure B.10.

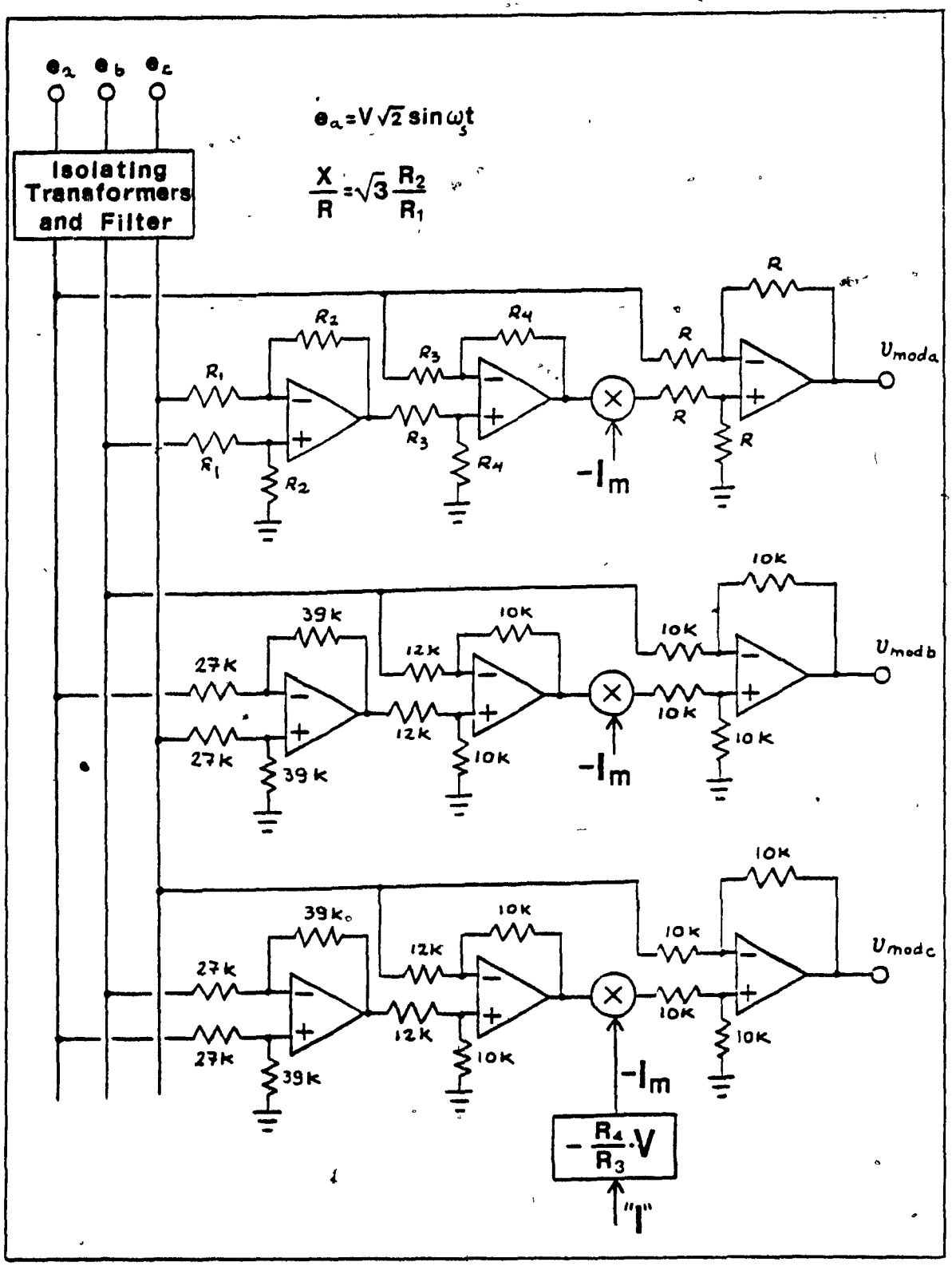


Fig.B.12 Modulating Signal Generator (MSG).

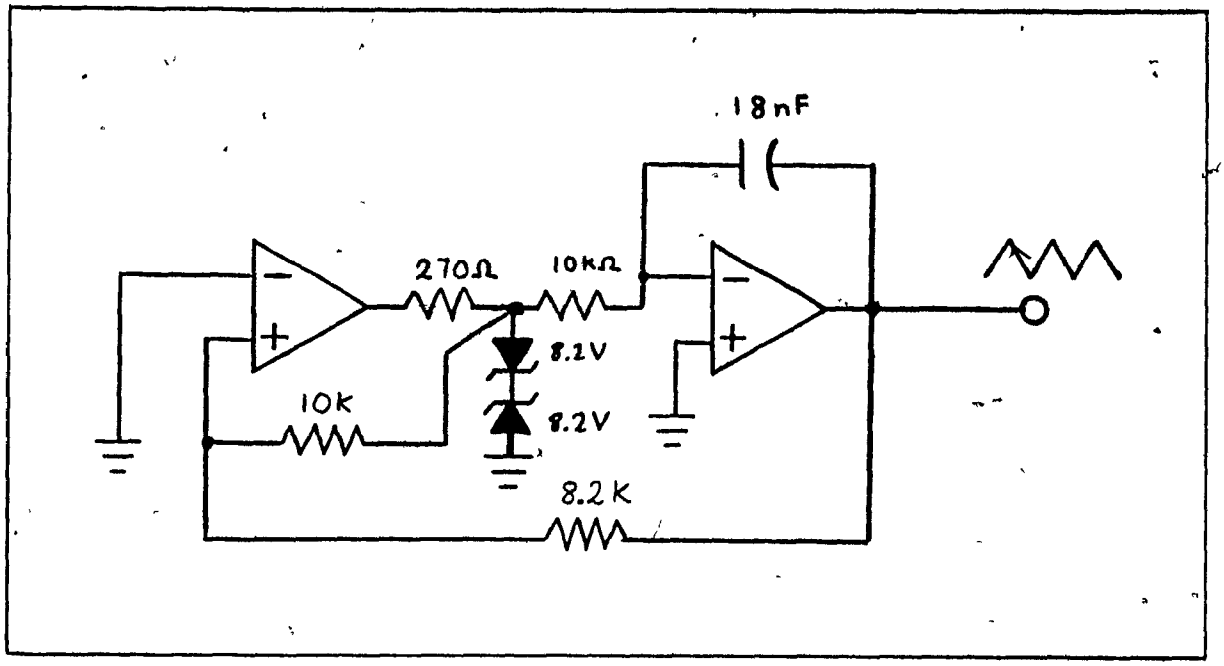


Fig.B.13 Triangular Generator (TG) Circuit.

B.3.2.4 Dynamic Compensator.

The dynamic compensator circuit generates the LdI/dt block and is shown in Figure B.14.

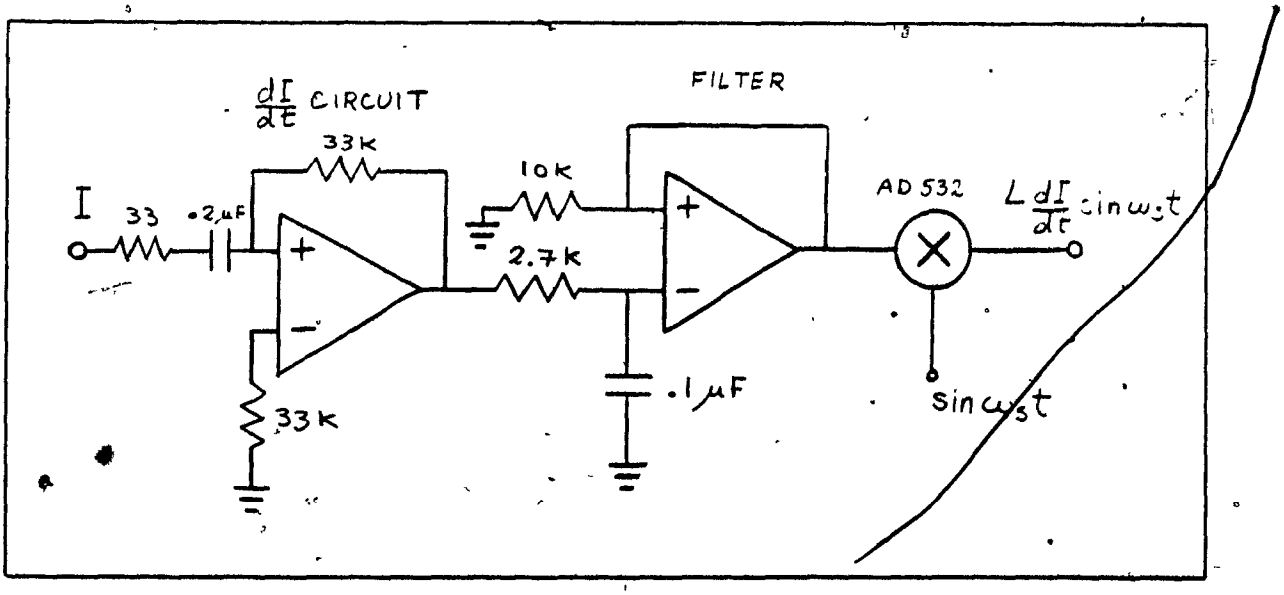


Fig.B.14 Dynamic Compensator Circuit.

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