A Novel Electrical-Optical Interconnect

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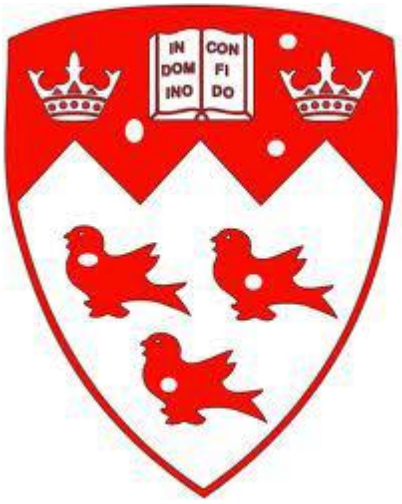

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2016

A thesis submitted to McGill University in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

Abstract

The need for high bandwidth is rapidly increasing mainly due to the adoption of data-hungry services such as online streaming of high-definition videos, online gaming, and cloud services. Further, end-users want to access data from anywhere and as fast as possible. This has created a momentum in telecommunication industry to push for higher bandwidth and low latency communication links. So far, this goal has been achieved by expanding data centers infrastructure and increasing the number of components as well as developing high bandwidth optoelectronic circuitry. The advances in downsizing integrated circuits (ICs) is supporting the latter, resulting in the implementation of faster and smaller central processing units (CPUs). In other words, the number of bits generated within a given footprint area of an IC chip is continuously increasing. To keep up with this trend, interconnect links between electronic chips (e.g., between memory and CPU) and boards (e.g., between a motherboard and an external graphics card) need to carry a larger amount of data while ensuring a low loss interconnect with low latency. In such context, the interconnect has become the bottleneck of the overall system performance. Indeed, its technology has not evolved in performance as quickly as the IC technology. To address this bottleneck, optical interconnects for chip-to-chip data communication are extensively investigated due to their advantages regarding their large transmission bandwidth capacity at low loss, low latency, and low crosstalk. This thesis proposes a novel electrical-optical interconnect structure for chip-to-chip communication which is capable of transmitting optical and electrical signals, simultaneously. The demonstration of such structure is significant as it utilizes existing metal waveguides in electronics and merges two layers of communications (i.e., electrical and optical) onto the same structure towards increased aggregated bandwidth. The hybrid link discussed here has the potential to be implemented as an interposer between chips on a board that are bonded via micro-bumps. The proposed structure consists of a few millimeters long finite-ground coplanar waveguide (FGCPW) supporting radio frequency (RF) signals. Thin ground stripes are designed to support long-range surface plasmon polaritons (LRSPP) at optical frequencies. The use of LRSPPs on thin gold stripes is the key to the structure as it provides the interface enabling transmitting RF and optical signals, simultaneously. In this thesis, I provide details of the design methodology using analytical formulation as well as commercial electromagnetic solvers. Then, I explain the customized fabrication process of the proposed structure where gold and copper stripes are embedded in a

Cytop polymer. Next, I thoroughly discuss characterization and validation methods. Finally, I present the measurement results of high-speed system-level performance of the structure. The performance of the proposed hybrid link achieves an error-free (bit-error-rate < 10^{-9}) transmission of a 12 Gbps microwave signal with 0.65 dB/mm loss as well as of 40 Gbps optical signal with 1.8 dB/mm loss. Additionally, I demonstrate error-free transmission of a 49 Gbps single channel and 40 Gbps wavelength division multiplexed (WDM) optical signals over a 3.6 mm long LRSPP waveguides. The demonstrated hybrid link provides a new paradigm for inter-chip connectivity with further potential to be implemented for chip-to-chip communication. This innovative link approach reduces the number of interconnection layers (i.e., less complexity) with increased bandwidth density.

Résumé

Les besoins pour de larges bandes passantes grandissent rapidement en raison des services qui consomment beaucoup de données tels que la diffusion en continu de vidéos à haute définition, les jeux en ligne and les services infonuagiques. De plus, les consommateurs veulent avoir accès à leurs données partout et rapidement. Cela a créé un élan dans l'industrie des télécommunications pour prôner des bandes passantes plus larges et des liens de communications à faible temps de latence. Jusqu'à maintenant, cet objectif a été atteint par l'expansion des infrastructures des centres de données, l'augmentation du nombre de composantes ainsi que le développement de circuits optoélectroniques à larges bandes passantes. Les avancées dans la réduction de la taille des circuits intégrés ont aidé se qui a permis l'implémentation d'unités centrales plus rapides et plus petites. En d'autres mots, le nombre de bits générés par une aire de circuits intégrés donnée augmente constamment. Pour suivre la tendance, les liens d'interconnexion entre les circuits électroniques (ex : entre la mémoire et l'unité centrale) et les cartes (ex : entre une carte mère et une carte graphique externe) doivent acheminer une grande quantité de données tout en minimisant les pertes et la latence. Dans ce contexte, les liens d'interconnexion sont devenus le goulot d'étranglement de toute la performance du système. En effet, cette technologie n'a pas évolué en performance aussi rapidement que la technologie des circuits intégrés. Pour y remédier, les liens d'interconnexion pour la communication de données entre puces sont grandement examinés en raison de leur capacité de transmission à large bande passante avec un minimum de perte, de latence et de diaphonie. Dans cette thèse, une nouvelle structure d'interconnexion électrique-optique pour la communication entre puces qui peut transmettre des signaux optiques et électriques simultanément est proposée. La démonstration d'une telle structure est pertinente puisqu'elle utilise des guides d'ondes électroniques en métal déjà existants and regroupe deux niveaux de communications (électrique et optique) sur la même structure pour augmenter la bande passante commune. Le lien hybride présenté dans cette thèse pourrait être réalisé comme liaison entre les puces d'une carte qui sont liées par micro-billes. La structure est un guide d'onde coplanaire avec conduite à la terre limité de quelques millimètres de long qui fonctionne aussi pour les signaux en radiofréquences. De minces bandes mises à la terre sont conçues comme support pour des plasmon polaritons de surface à longue portée (LRSPP) à des fréquences optiques. L'utilisation de LRSPPs sur de minces bandes d'or est l'élément important de la structure puisque ces derniers créent

l'interface qui permet la transmission de radiofréquences et de signaux optiques simultanément. Dans cette thèse, je fournis les détails de la méthode de conception en utilisant des formules analytiques ainsi que des solveurs électromagnétiques commerciaux. J'explique ensuite le processus de fabrication de la structure proposée où les bandes d'or and de cuivre sont incorporés dans un polymère Cytop suivi d'une discussion minutieuse sur les méthodes de caractérisation et de validation. Finalement, je présente les résultats sur la performance à haute vitesse de la structure au niveau du système. La performance du lien hybride proposé effectue une transmission sans erreur (taux d'erreurs binaires < 10^{-9}) d'un signal micro-onde de 12 Gbps avec une perte de 0.65 dB/mm ainsi qu'un signal optique de 40 Gbps avec une perte de 1.8 dB/mm. De plus, je démontre une transmission sans erreur d'un canal unique à 49 Gbps et un signal optique en multiplexage en répartition par longueur d'onde de 40 Gbps dans un guide d'onde LRSPP de 3.6 mm de long. La démonstration de ce nouveau lien hybride permet un nouveau paradigme pour les connexions sur puces avec le potentiel d'être réalisé pour des communications entre puces. Cette approche innovatrice réduit le nombre de niveaux d'interconnexion (moins complexe) en augmentant la densité de la bande passante.

Acknowledgments

First and foremost, I would like to express my genuine appreciation to Prof. Odile Liboiron-Ladouceur for her tireless supports and encouragement throughout the course of my Ph.D. research. I am thankful of her for trusting me and accepting me in her research group. During my years at McGill, I was able to perform research in the area that I was very enthusiastic about. I had access to the very well-equipped labs at the photonic systems group (PSG) at McGill University, and I had the opportunity to acquire theoretical and experimental knowledge in the field of optics, and I am very thankful of Prof. Liboiron-Ladouceur for this experience.

Secondly, I wish to express my gratitude to Prof. Pierre Berini for accepting to collaborate in this project and for his support and guidance during my Ph.D. It was an honor for me to have Prof. Berini as my collaborator and be able to work with him.

I would like to acknowledge Prof. R. Niall Tait, Ewa Lisicka-Skrzek, Sa'ad M. Hassan, Norman R. Fong, Martin Dussault, and Carleton University Microfabrication staff: Rob Vandusen and Angela McCormick for their help and support for the fabrication of my design.

I am grateful to all the professors in the PSG for building a world-class research laboratory infrastructure and creating a professional and friendly work environment. I am thankful to all the staff at PSG: Ms. Maru Basanez, Ms. Carrie Serban, Chris Rolston, and Brent Snow for their administrative and technological support. As well, I would like to thank Dr. Phil Roche for his help in troubleshooting experimental setups.

Last but not least, many thanks to my friends and colleagues at PSG: Monir Moayedi, Mehrdad MirShafiei, Ali Salehiomran, Farhad Shokraneh, Md Shafiqul Hai, Chris Williams, Rubana Pariti, Vernon Elmo Paul, Yule Xiong, David Patel, and Venkat Veerasubramania, who worked alongside me in the labs. I would like to acknowledge Sandrine Filion Côté for her constant encouragements and help with the French translation of the abstract.

To my beloved mother and late father

To my dearest brothers

To my beloved wife, my life partner

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List of Acronyms

ADS	Advanced Design System
AFM	Atomic Force Microscopy
ASE	Amplified Spontaneous Emission
ASIC	Application Specific Integrated Circuit
BER	Bit-Error-Rate
CMOS	Complementary Metal–Oxide–Semiconductor
CPW	Co-Planar Waveguides
DLSPPW	Dielectric-Loaded SPP Waveguides
DPSK	Differential Phase Shift Keying
DSP	Digital Signal Processing
DWG	Dielectric Waveguides
EDFA	Erbium-Doped Fiber Amplifier
EM	Electromagnetic
EO	Electrical-to-Optical
EPB	Energy Per Bit
FEM	Finite Element Method
FGCPW	Finite Ground Co-Planar Waveguide
GSG	Ground-Signal-Ground
HMDS	Hexamethyldisilazane
HR silicon	High Resistivity Silicon
IC	Integrated Circuits
IL	Insertion Loss
IPA	Isopropyl Alcohol
ISP	Internet Service Provider
ITU	International Telecommunication Union
LCD	Liquid Crystal Display
LD	Laser diode
LR-DLSPPWs	Long-Range DLSPPWs

LRSPPs	Long-Range SPP
LRSPPWs	Long-Range SPP Waveguides
LSI	Large-Scale Integration
MFD	Mode Field Diameter
MoL	Method of Line
MSL	Microstrip Lines
MZM	Mach–Zehnder Modulator
NA	Numerical Aperture
NRZ	Non-Return-to-Zero
OE	Optical-to-Electrical
OOK	On-Off-Keying
OSA	Optical Spectrum Analyzer
PCB	Printed Circuit Boards
PD	Photo Detector
PEC	Perfect Electrical Conductor
PMGI	Polymethylglutarimide
PM-SMF	Polarization-Maintaining Single Mode Fiber
PPG	Pulse Pattern Generator
PRBS	Pseudorandom Binary Sequence
RF	Radio Frequency
SOI	Silicon on Insulator
TE	Transverse Electric
TEM	Transverse Electric and Magnetic
TM	Transverse Magnetic
VCSEL	Vertical-cavity-surface-emitting-laser
WDM	Wavelength Division Multiplexing

1. Introduction

This chapter explains the motivation for this thesis research, and provides a literature review of different interconnect technologies and discusses the electrical and optical interconnects. Finally, an introduction of plasmonics as the interface between electronics devices and photonics components are presented.

1.1. Motivation

The popularity of mobile devices such as smartphones and tablets, running data-intensive applications, online high-definition video streaming, online gaming, cloud services, and high-speed wireless networks (4G/LTE) are a few of the driving forces for internet service providers (ISPs) to demand higher bandwidth. There are two solutions to this issue. One solution is to increase the bandwidth by adding more equipment in data centers. Alternatively, the telecommunications networking equipment suppliers must increase the bandwidth in their existing form factors (i.e., higher bandwidth density). The latter is more attractive to the industry compared to the former, mainly due to its lower cost per bit. However, this approach requires tackling some challenges such as designing high bandwidth optical-to-electrical and electrical-to-optical (OE/EO) converters (e.g., modulators and receivers), advanced modulation formats, complex

digital signal processing (DSP) algorithms, high-speed application-specific integrated circuits (ASICs), and high bandwidth interconnects. The focus of this thesis is to investigate the high bandwidth interconnects.

In recent years, by the advance of CMOS technology where high-speed ICs with multi- and many-core architectures are built, the discussion on using optical interconnects for off-chip and board-to-board communication has gained much interest. The concept of "partition length," above which information transports more efficiently by photons rather than electrons, assesses the feasibility of optical interconnects compared to their electrical counterpart. In [1] it was discussed that for channel width of below 1 μm the partition length for high frequencies (> 40 GHz) is in range of several millimetres.

In this context, researchers have extensively investigated multiple technologies such as multi-core optical fibers, polymer waveguides, silicon waveguides, and plasmonic-based waveguides. Each of these technologies inherits some advantages and disadvantages, which I will discuss in more details in this chapter

In this thesis, I propose, design, fabricate and characterize a new structure for chip-to-chip communication where metal interconnects embedded in a polymer are deployed to transmit both microwave and optical signals simultaneously. The envisioned application for the hybrid link discussed in this thesis is in architectures where an electrical interface between chips is implemented using ball-grid arrays (BGAs) or micro bumps. The goal of this structure is to provide efficient and low energy consumption chip-to-chip interconnects by sending high data rate via optical section, and switching to low data rate electrical signal when the required bandwidth demand is not at its full capacity. Measurement results of the hybrid link are promising and show comparable performance with recent works, and justify future analysis to further improve the performance of the structure and achieve practical chip-to-chip implementation.

1.2. Thesis outline

Chapter 2 explains the principles of plasmonics and reviews different demonstrations of optical signal transmission through plasmonic waveguides. Since the proposed electrical-optical interconnect comprises of a plasmonic waveguide, chapter 2 provides the background information on the plasmonic waveguides and the design of plasmonic interconnects.

Chapter 3 explains the design and modeling of an LRSPP waveguide made of thin gold stripes embedded in Cytop. The fabricated device is characterized and the transmission of multiple OOK (4×49 Gbps) and differential phase shift keying (DPSK) (4×10 Gbps) modulated data is experimentally demonstrated. The signal transmission is further verified by performing bit-error-rate (BER) measurements.

Chapter 4 proposes a novel metal waveguide structure, which simultaneously transmits optical and microwave signals. The design and optimization of optical and electrical waveguides are explained. Moreover, the fabrication steps for implementation of the designed structure are described. And finally, the measurement results of the fabricated devices are presented.

In chapter 5, circuit model analysis is performed to provide more insight into the RF performance of the proposed structure in chapter 4.

Chapter 6 gives a conclusion of the thesis and provides a list of the possible future works.

Finally, chapter 7 gives a list of the references of this thesis.

1.3. Literature review

1.3.1. Introduction

Interconnects are the physical connections enabling the intra-chip (within a chip), inter-chip (chip-to-chip), and board-to-board data transfers. As the increasing bandwidth demand is pushing computing modules to work at higher speeds, the interconnection between different computing modules has become the bottleneck limiting the performance of the system. Consequently, interconnects with high bandwidth density and energy efficiency are of great interest.

Interconnects are evaluated based on multiple factors including delay, noise, bandwidth density, power dissipation, and cost. The bandwidth density or the bisectional bandwidth is the data transmission bandwidth per unit width and is expressed in the unit of Gbps/mm or Gbps/µm. This section gives a brief review of different types of interconnects and discusses the drawbacks and advantages of different approaches.

Conventionally, the chip-to-chip and board-to-board connections only included electrical interconnects. However, as it will be discussed in the next sections, the conventional copper-based electrical interconnects can no longer satisfy the essential requirements of the interconnection. Hence, researchers have explored other types of electrical links. Moreover, optical and plasmonic interconnects have been proposed as the alternative solutions. The next sections give a brief review of electrical and optical interconnects.

1.3.2. Electrical interconnect

On-chip electrical interconnects consist of copper wires surrounded by a low-k dielectric. The effective time constant (RC) of a conventional electrical interconnect, where R and C are the total resistance and capacitance of the line, determines its delay time. Downsizing the minimum feature size of integrated circuits (ICs) has enabled the transistors to work at higher speed and therefore perform more computations per second [2,3]. As the interconnect dimensions are scaled down, the metal wire cross section reduces which consequently increases the wire resistivity. However, the capacitance per unit length of the metallic wire is not significantly affected. By scaling down the metallic wire interconnection, its effective time constant (RC) increases. Hence, while transistors

delay decreases with scaling, the delay of interconnects increases [4], and the delay due to the communication between the parts of the chip becomes comparable to the computation delay itself. This is called the "interconnect bottleneck" which refers to IC performance constraint due to connections between components instead of their internal speed.

There are different types of electrical interconnects including transmission lines (e.g., coplanar waveguides and microstrip lines), dielectric waveguides (DWGs), and wireless (i.e., air is the dielectric medium). They all have the advantage of compatibility with silicon processes. However, each scheme suffers from different restrictions on transmission loss, electromagnetic interferences (EMI), etc. [5]. This section provides some examples of different types of electrical interconnects.

Fig. 1.1(a) shows a motherboard based electrical interconnect [6]. The metallic transmission line interconnects suffer from high conduction loss at high operating frequencies. A complementary metal–oxide–semiconductor (CMOS) microstrip line (MSL) at 100 GHz has 1 dB/mm loss which increases with the operating frequency [5]. By using differential transmission lines in the printed circuit boards (PCB), the data transmission speed increases at the expense of doubling the number of signal lines [7]. The typical pitch of a high-density differential stripline is 600 μm and assuming 10 Gbps data transmission per channel, the maximum bandwidth density of 16 Gbps/mm can be achieved [6, 7]. Higher bandwidth channels are limited by dispersion and need more equalization taps and hence produce more power dissipation [6]. In [7] three patterns of the cross-sectional shape of differential transmission lines are studied to reduce the cross-talk noise and consequently improve the wiring density of the transmission line. Using square shape cross section instead of conventional wide rectangle cross section for the conductor, the wiring density of the differential transmission line improves by up to 12.5 % (from 600 μm to 525 μm).

An alternative approach is to use low-loss ribbon cables instead of FR4 boards as depicted in Fig. 1.1(b) [6]. In [8], four different flex circuit constructions have been studied which consist of microstrip lines embedded in a polyimide substrate. The measurement results show that the raw bandwidth on low-loss flex ribbons is three times larger than FR-4 boards. The measurement results also show that the attenuation constant at the frequency of 20 GHz for microstrip transmission line on FR4 is 1 dB/cm while in the case of differential microstrip line implemented in the flex circuit; it is 0.3 dB/cm [8].

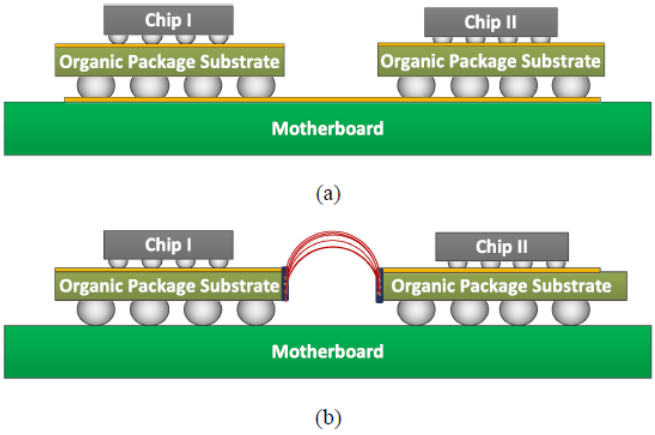


Fig. 1.1. a) Electrical interconnects on motherboard, b) flexible electrical interconnects [6].

In 2012, Park et al. proposed a wireless link operating at 260 GHz which can be especially useful for routing between chips when a physical interconnection is not feasible [9]. At the given frequency, the dimensions of the on-chip antenna for chip-to-chip communications can be comparable to the device dimensions and does not incur a large area penalty. However, the wireless interconnects suffer from large path loss and channel interferences.

In [5] by Yu et al. in 2016, a sub-THz dielectric interconnect channel is proposed and implemented as depicted in Fig. 1.2. The dielectric waveguide structure is made of high resistivity (HR) silicon because of its low loss of 0.1 dB/m at 200 GHz. Two configurations of dielectric interconnect are proposed and implemented [5]. In the first structure, the signal is excited through a coplanar waveguide (CPW) and tapered to an MSL. The signal from MSL then feeds a patch antenna. The waves radiated by the patch antenna couple to the HR silicon DWG propagating at the sub-THz wavelength. At the other end of DWG, waves are collected by another patch antenna. The bending loss at the DWG deteriorates the performance of the proposed sub-THz interconnect channel. Moreover, the limited bandwidth of the patch antenna limits the transmission bandwidth of the fabricated interconnect. The second configuration uses a near-field excitation scheme. In this approach, a tapered DWG and a tapered MSL are overlapped with each other. Hence the quasi-TEM mode of MSL is transitioned to the first order mode of the dielectric interconnect channel. The measured minimum insertion loss (IL) for the interconnect with far-field transitions is 8.4 dB with a 3-dB bandwidth of 12.6 GHz, while the near-field configuration has 4.0 dB IL with 3-dB bandwidth of 59 GHz [5].

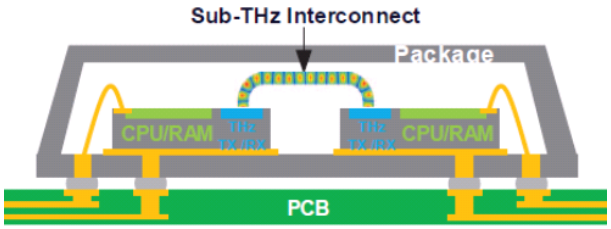


Fig. 1.2. Sub-THz interconnect using the advantages of both optical and electrical interconnects [5] © [2016] IEEE.

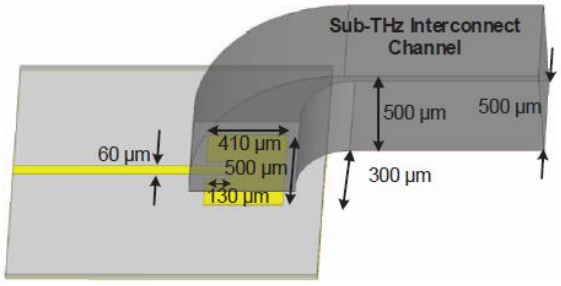


Fig. 1.3. Far field transition of MSL-to-DWG [5] © [2016] IEEE.

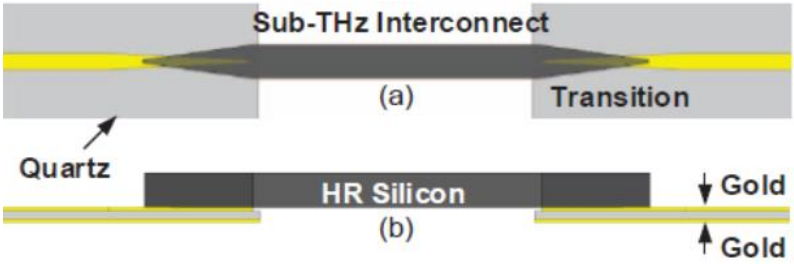


Fig. 1.4. a) Top view of sub-THz interconnect using near-field transition, b) side view of the dielectric channel [5] © [2016] IEEE.

1.3.3. Optical interconnects

1. Introduction

Due to the inherent low loss, high bandwidth, low latency, and low mutual interference of optical waveguides, researchers have investigated optical interconnects for the implementation of low loss

and high-speed interconnections and substituting conventional electrical interconnects. Additionally, optical links have the ability to send multiple wavelengths in a single waveguide using wavelength division multiplexing (WDM) which further increases the data transmission bandwidth. However, the implementation of optical interconnects requires the electrical-to-optical and optical-to-electrical conversion which increases the total energy consumption per bit of transmitted data (Energy per bit (EPB)). Silicon photonics is a promising optical interconnect solution due to the advantage of using the industrial resources in the electronics industry and compatibility with CMOS process. Fig. 1.5 depicts the diagram of an optical link system which consists of four primary optical elements: laser, an optical modulator, waveguide, and an optical detector. In addition to the required EPB of an optical interconnect, the integration of a laser with the CMOS process is another challenge.

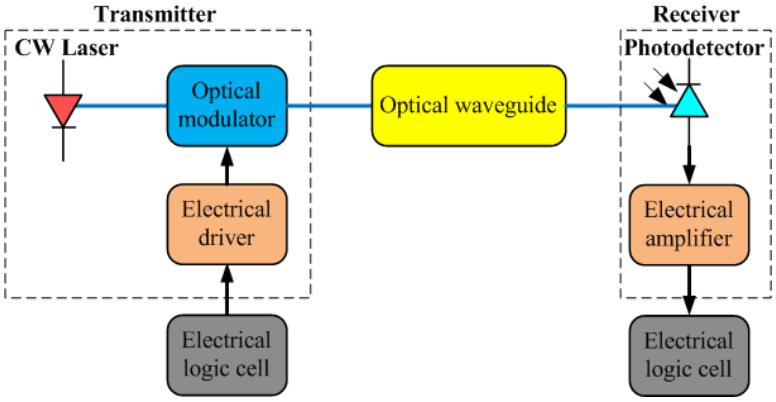


Fig. 1.5. An optical interconnect system.

2. Photonic and electronic circuit integration techniques

The implementation of an optical interconnection system as depicted in Fig. 1.5, requires multiple functions such as light generation, modulation, and detection. These functionalities can only be performed using different materials, which must be combined using either monolithic or hybrid integration. In monolithic integration, different functionalities are all fabricated on the same wafer substrate. While in the case of hybrid integration, different devices are fabricated on separate substrates and then mechanically integrated to make the final system.

Due to its compactness and compatibility with large scale integration (LSIs) chips, Silicon Photonics is believed to be the most suitable technology for the integration of electronic and photonic circuits [10]. Fig. 1.6 depicts three types of silicon photonic and electronics integration. In front-end integration, the electronic and photonic circuits are integrated near the surface of a silicon substrate, while in back-end integration the photonic circuit is integrated on the wiring layer. In the case of flip-chip bonding, electronics, and photonic chips are fabricated separately and then stacked by the flip-chip bonding technique [10]. The front-end and back-end techniques are monolithic integration method, and the flip-chip techniques is a hybrid integration method.

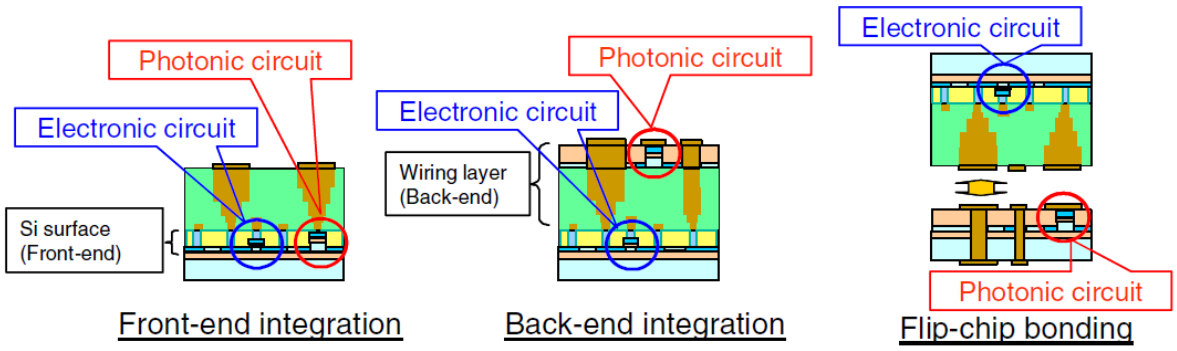


Fig. 1.6. Schematic cross sections of integration between photonics and electronics [10].

Monolithic integration provides higher speed and lower cost than hybrid integration. However, it requires very strict CMOS compatibilities for the design, fabrication, and test processes. On the other hand, hybrid integration provides the opportunity to integrate the most suitable technology for photonics and electronics circuits and is the most practical choice for implementation of optical interconnects by photonic and electronic integration [10].

In [11] by Doany et al., a highly integrated module-to-module board-level optical interconnect is demonstrated (see Fig. 1.7). The electrical signal in converted to an optical signal using a silicon-based chip. The optical signal is then transmitted to the polymer waveguides at the motherboard using an optical lens array. The polymer waveguides on the PCB have a 62.5 µm pitch. There are 24 transmitter, receiver, and waveguide channels on the board each operating at 15 Gbps which provide a bandwidth density of 240 Gbps/mm [11].

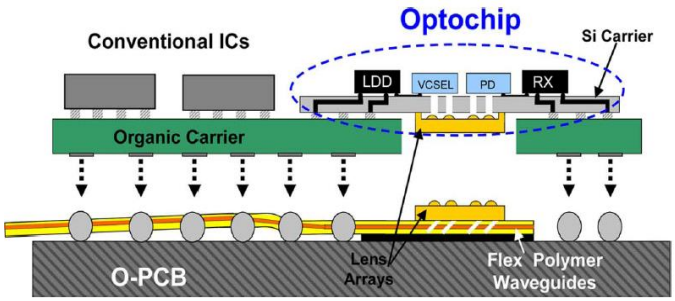


Fig. 1.7. Schematic of the Terabus architecture with polymer waveguide at board level [11] © [2012] IEEE.

In [12] by Urino et al., a high density optical interconnect using silicon photonics is implemented using a combination of monolithic and hybrid integration techniques. The optical modulators, waveguides, and photodetector (PD) are monolithically integrated on a single silicon substrate (depicted in Fig. 1.8). LSI bare chips and a laser diode (LD) are hybridly integrated on the silicon substrate using flip-chip bonding. The optical interconnection replaces the conventional electronic wires on a printed circuit board (PCB), and the silicon substrate is called the "Silicon interposer" [12]. In this case, since the entire optical link (i.e., array of optical sources, interconnects, and receivers) is implemented, it is more beneficial to describe the data transmission per unit area of the chip which is equal to 3.5 $\mathrm{Tbps/cm^2}$. Fig. 1.9 shows another implementation of optical interconnection using a silicon interposer [10]. The results show that the silicon interposer is capable of 2.1 Tbps bandwidth of optical interconnection [10].

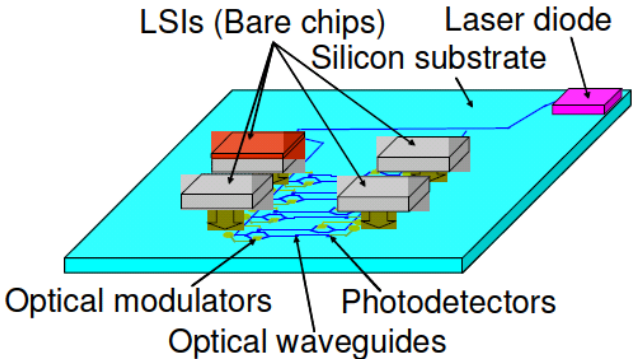


Fig. 1.8. A photonics-electronics convergence platform for inter-chip interconnects using silicon interposer [12].

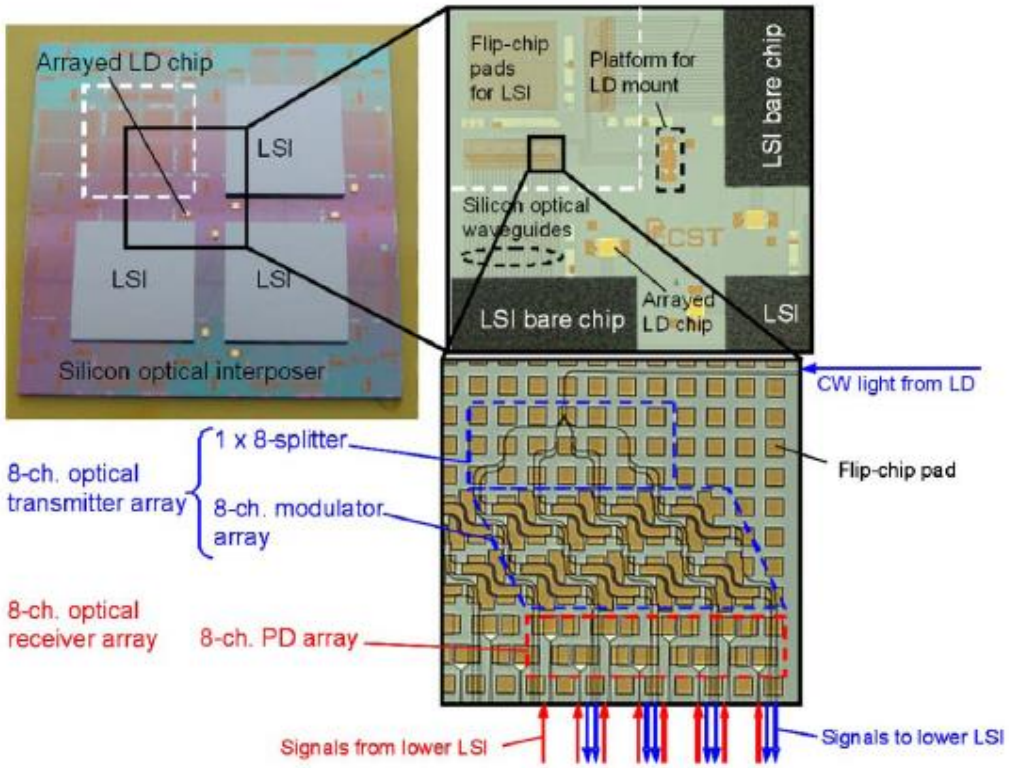


Fig. 1.9. Silicon interposer as the photonics–electronics convergence system for inter-chip interconnects [10].

Table 1.1 summarizes the data transmission density of the three different interconnect solutions discussed. The first type belongs to a single layer differential stripline realized on the motherboard for implementation of chip-to-chip electrical interconnect [6 and 7]. The second type correspond to the implementation of optical interconnects using polymer waveguides [11], and the last type achieves high data transmission density of optical interconnect implementation using a silicon interposer. All of the compared technologies consist of single layer interconnect boards.

In [13] by Michaels and Yablonovitch, a multilayer optical communication fabric similar to modern electrical circuit boards is proposed. The structure consists of a passive optical circuit board, a silicon photonic optical interposer, and an electrical chip as depicted in Fig. 1.10(a). Unlike the configurations introduced in [6] and [12], the optical signal is transmitted through the passive optical board and not the silicon interposer. Each electrical chip is flip-chip bonded to a silicon photonic optical interposer which handles electrical-to-optical (E/O) and optical-to-electrical (O/E) conversion for high-bandwidth optical signals. Light couples vertically between

the optical interposer and the passive optical circuit board using inverse designed grating couplers. While the light propagating in the optical circuit board evanescently couples between layers as shown in Fig. 1.10(b) [13].

Table 1.1 Comparison of different interconnect solutions

Ref	Affiliation (year)	Technology	Data transmission density
[6 and 7]	Kuwahara et al. (2015)	Single layer differential stripline on motherboard	16 Gbps/mm
[11]	Doany et al. (2012)	Optical interconnects with polymer waveguide at board level	240 Gbps/mm
[12]	Urino et al. (2011)	Chip-to-chip interconnection using a silicon interposer	3.5 Tbps/cm^2
This work	Banan et al.(2016)	Electrical-optical chip-to-chip interconnection using metal stripes	1 Tbps/mm

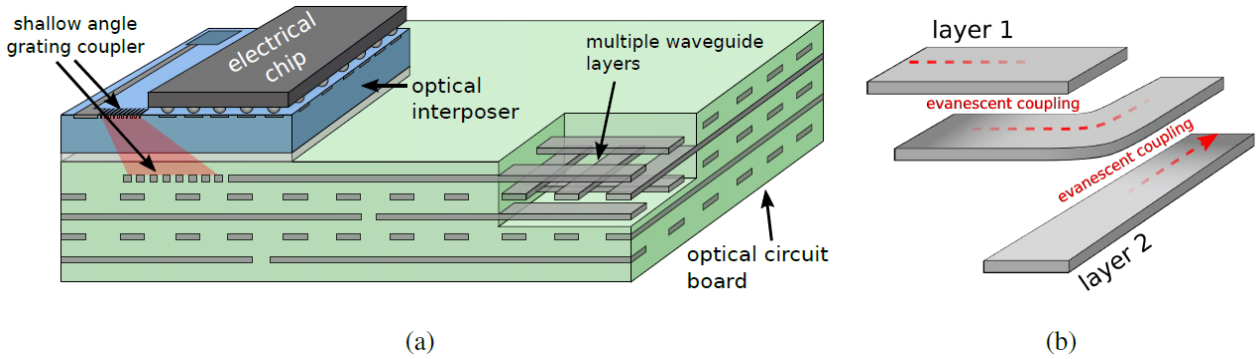


Fig. 1.10. a) Diagram of multilayer optical circuit board including multiple layers of Si_3N_4 waveguides, an optical interposer, and an electrical chip, b) diagram of evanescent interlayer coupling: a waveguide in an intermediate runs parallel to layer 1, coupling light evanescently, and then bends such that it runs parallel to layer 2 [13]. © [2016] IEEE.

1.3.4. Conclusion

This chapter discussed the concepts of electrical and optical interconnects. First, different types of electrical interconnects were introduced, and the limitations of each approach were explained. Then, pros and cons of optical interconnect as well as their implementation challenges were discussed. Moreover, using different examples of optical interconnect implementations, the evolution of optical interconnect was explained. The next chapter discusses plasmonics as another technology to consider for implementation of high bandwidth and low loss interconnects.

2. Background

2.1. Introduction

As described in the previous chapter, the ever-increasing demand for fast data transmission and processing has driven a continuous progress towards smaller, faster, and more efficient electronic chips. This trend has created a bottleneck for chip-to-chip interconnects. Optical interconnects, with their large data carrying capacity may offer new solutions for resolving the power dissipation and signal delay issues of electronics [14]. However, the size of photonic devices is limited by the diffraction law to about half a wavelength of light which is at least one or two orders of magnitude larger than their electronic counterparts. Therefore, there is a size mismatch between nano-electronics and dielectric photonic components, making the integration of these technologies challenging. On the other hand, plasmonic structures adopt different shapes and sizes from nano-particles to stripe and slab waveguides. This feature enables the routing and manipulation of light at different technology feature sizes. Fig. 2.1 shows the operating speeds and critical dimensions of different chip-scale device technologies. As illustrated, electronics cover feature sizes from nanometers to several meters, but their operating speed can only go up to few tens of gigahertz. The signal delay as well as bandwidth limit the reach of electrical waveguides (e.g., coaxial cables). The former is related to the signal propagation speed which is limited by the permittivity of the dielectric material used in the waveguide. The latter is limited by conductor loss in which propagation loss increases by increasing frequency or length. Therefore, photonics seems to be an appealing technology for applications requiring high operating speeds or long distances (up to several thousand kilometers) reach. Optical waveguides inherently offer lower loss and signal delay mainly due to the different waveguide material and propagation mechanism. However, as mentioned before, optical waveguide feature size hits a limit due to the diffraction law. Plasmonics

can break this limit, and provide access to electromagnetic wave confinement at nanometer scales with the same operating speed as photonics. Though, due to the interaction of EM waves with lossy metal, the propagation length of the plasmonic structures ranges from few microns to several centimeters depending on the geometry and material properties.

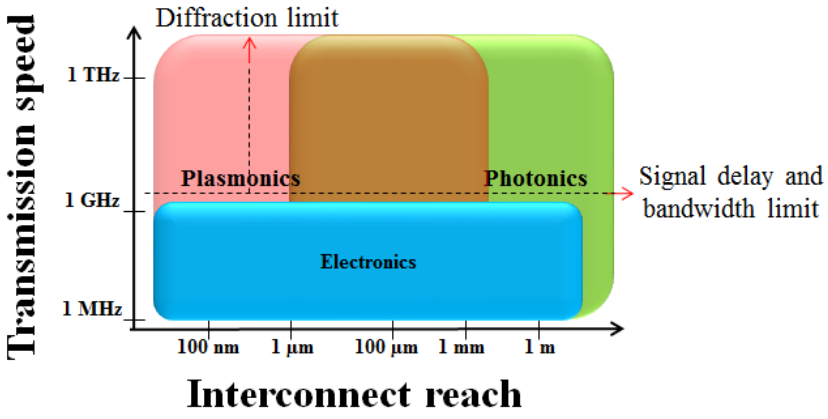


Fig. 2.1. Operating speeds and critical dimensions of various chip-scale device technologies.

In this chapter, first, fundamentals of plasmonics and its excitation methods are briefly reviewed. Then, the metal slab/stripe waveguides are discussed in more details. This thesis mainly focuses on this structure, since it provides propagation lengths of up to several millimeters and even centimeters, which is desired for the target application of chip-to-chip communication. Finally, this chapter presents a review of few previous works on this topic.

2.1.1. Surface plasmon polaritons (SPPs)

It is mathematically proven that the interface between two semi-infinite materials with positive and negative dielectric constants guides transverse magnetic (TM) surface waves. Since the dielectric constant of many metals is negative near optical wavelengths, the metal-dielectric interface at optical wavelengths can also propagate TM surface waves. These waves are electromagnetic excitation of surface plasmons (surface plasma oscillations comprised of conduction electrons in the metal) which are called surface plasmon polaritons (SPPs). The metallic interconnects that support SPPs are called plasmonic waveguides [15 and 16]. Fig. 2.2 shows the SPP propagating in the z-axis along the interface of a semi-infinite metal and a semi-

infinite dielectric. The SPP field is mostly confined to the metal-dielectric interface with exponential decay into both media at the interface. Due to high confinement to the metal surface, SPP is very sensitive to surface irregularities and therefore has been used for surface analysis applications [17].

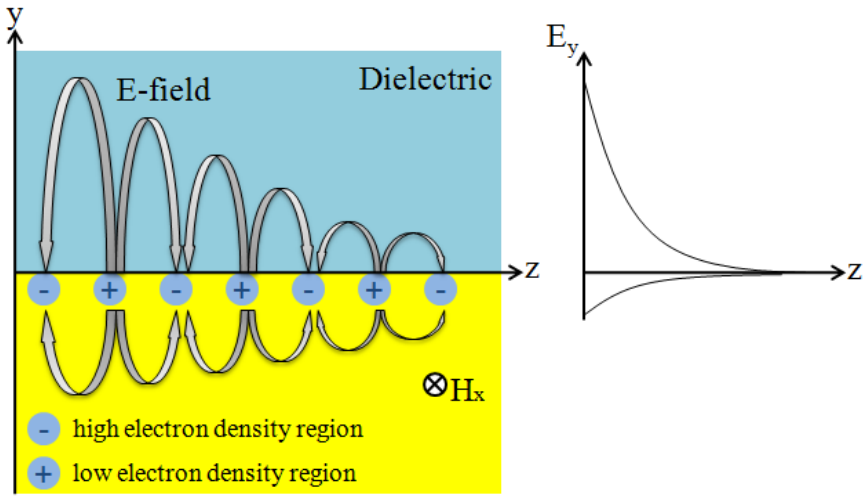


Fig. 2.2. SPP propagation along a metal-dielectric interface.

The dispersion relation of the SPP mode propagating at the metal-dielectric interface with relative dielectric permittivity of ε_d and ε_m is

$$\beta = k_0 \sqrt{\frac{\varepsilon_m \varepsilon_d}{\varepsilon_m + \varepsilon_d}} \tag{1}$$

In this equation, β (radians/meter) is the propagation constant in z direction, and k_0 (radians/meter) is the free space wave number. In the optical wavelength range, the dielectric permittivity of a loss-less metal can be defined using the Drude model

$$\varepsilon_m = 1 - \frac{\omega_p^2}{\omega^2} \tag{2}$$

where ω_p is the plasma angular frequency and ω is the optical angular frequency of light. Using equations (1) and (2), the dispersion can be plotted as demonstrated in Fig. 2.3. The light line shown in the figure divides dispersion diagram into non-guiding (left) and guiding regions (right). The SPPs dispersion relation completely resides to the right of the light line which means the SPP mode has a greater momentum than a free photon at the same frequency. A crossing between dispersion curve and light line only occurs in the limit of ω = 0, β = 0. For small angular

frequencies, the dispersion diagram follows the light line, however, as the angular frequency reaches $\omega_{sp} = \frac{\omega_p}{\sqrt{1+\varepsilon_d}}$, β approaches infinity (in other words, it becomes asymptotic with $\omega = \omega_{sp}$ line). The angular frequency of ω_{sp} is called surface plasmon polariton resonance, near which the wave slows down and the area of its field on the two sides of the interface becomes infinitesimal.

In reality, metals are lossy with complex dielectric permittivity ($\varepsilon_m = \varepsilon'_m + j\varepsilon''_m$), hence, the propagation constant of SPP also includes an imaginary part. In this case, the propagation distance δ_{SP} is the distance over which the power of SPP wave drops to 1/e of its initial magnitude and is given by

$$\delta_{SP} = \frac{c}{\omega}\left(\frac{\varepsilon_d+\varepsilon''_m}{\varepsilon_d\varepsilon'_m}\right)^{3/2}\frac{(\varepsilon'_m)^2}{\varepsilon''_m} \tag{3}$$

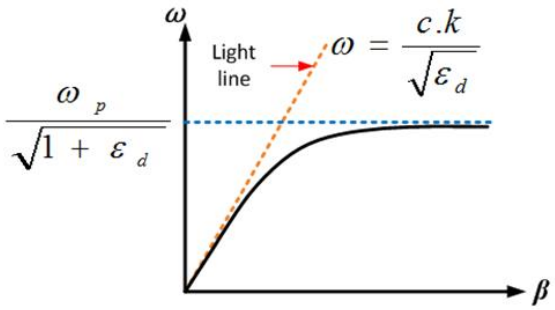


Fig. 2.3. Dispersion diagram of the metal-dielectric interface using a Drude model with no loss [18].

2.1.2. SPPs excitation

SPPs cannot be excited by direct illumination of light, as energy and momentum conservation (i.e., $\omega_{incident} = \omega_{spp}$ and $k_{incident} = k_{spp}$) cannot be fulfilled at the same time. Instead, in order to excite SPPs, a momentum transfer has to be established. Techniques to achieve this will be discussed in this section. It is possible to excite SPPs by means of a high energy electron beam hitting the metal surface. The electrons which hit the metal surface get scattered to different directions and provided that they have the correct momentum they excite the SPP modes.

The most common methods to excite SPPs are by the prism or grating coupling in which the mismatch between wave numbers of SPPs and light is compensated. Fig. 2.4 shows coupling light to SPPs using a prism. By placing the prism at a few hundred nanometer distance off the metal

surface, light enters the prism such that total internal reflection happens at the prism-air interface. The evanescent field at this interface then excites SPPs at the metal surface [18].

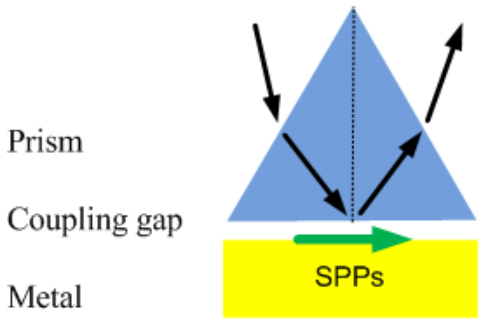


Fig. 2.4. Schematics of different schemes to excite SPP.

2.1.3. Long-range surface plasmon polaritons (LRSPPs)

Using a thin metal film embedded in a dielectric material, the attenuation of SPPs is reduced, mainly due to the small overlap of EM field with the lossy metal, resulting in longer propagation distances. Thus, this mode is called long-range SPPs (LRSPPs). The LRSPP modes of thin metal films are less confined than the single-interface SPP mode. This section discusses the LRSPPs properties of thin metal films of infinite and finite width.

1. Metal slab with infinite width

The configuration consists of the metal film with a thickness of *t* embedded between two semi-infinite dielectrics, and infinite width which is called a metal slab (Fig. 2.5). In the case of symmetric metal slab, two bound single-interface SPPs propagate at the two metal–dielectric interfaces. By reducing the thickness of the metal slab, due to field tunneling through the metal, the two SPP modes couple together and form bound TM-polarized symmetrical and asymmetrical supermodes that exhibit dispersion with metal thickness. As the mode propagates in z direction (perpendicular to the plane), the transverse electric field component E_y of the first two modes of the structure, have symmetric and asymmetric distribution (relative to y axis) and are demonstrated as s_b and a_b, (the symmetric bound and asymmetric bound mode) where s_b mode is the LRSPP mode [19].

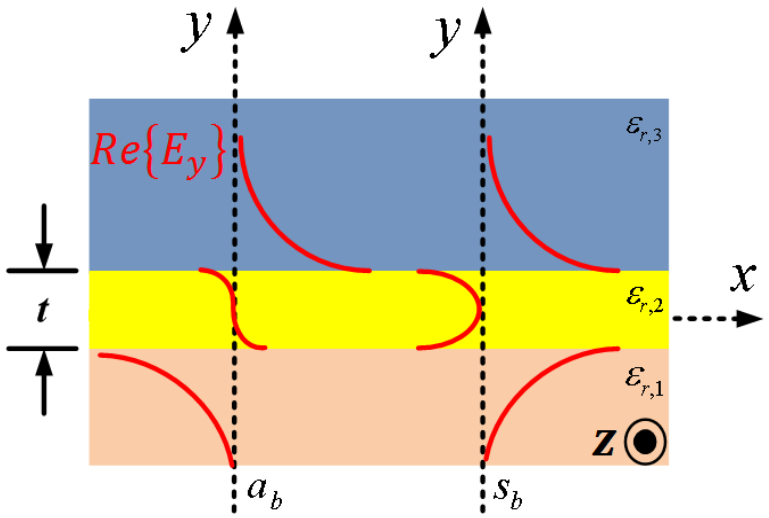


Fig. 2.5. Metal slab with a thickness of *t* bounded by semi-infinite dielectrics, supporting two bound SPP modes, s_b and a_b.

The H_x component of the modes has the same symmetry as E_y field, but the longitudinal electric field E_z has the opposite symmetry. As the thickness of metal slab decreases, the attenuation and effective index of the s_b mode and the mode confinement are also reduced. However, the a_b mode attenuation increases by reducing the thickness of metal slab. Fig. 2.6 shows the normalized propagation and attenuation constant of s_b and a_b modes of an asymmetric sliver (Ag) metal slab at the wavelength of $\lambda_0 = 632.8\,nm$ with a relative dielectric permittivity of $\varepsilon_{r2} = (0.0657 - j4)^2$ for the metal and a relative dielectric permittivities of $\varepsilon_{r1} = 1.5^2$ and $\varepsilon_{r3} = 1.55^2$ of the surrounding dielectrics [19].

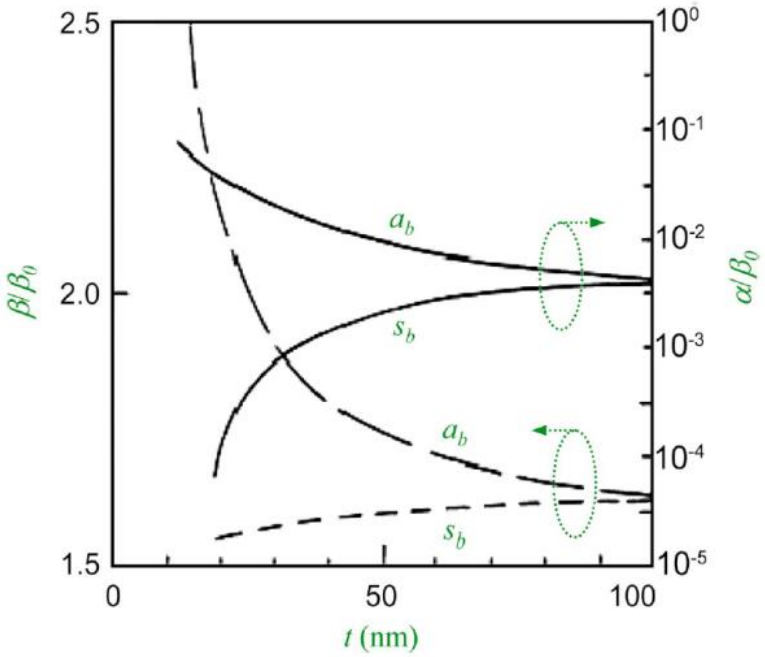


Fig. 2.6. Normalized phase and attenuation constant of s_b and a_b modes of an asymmetric Ag metal slab at $\lambda_0 = 632.8\,nm$ with $\varepsilon_{r2} = (0.0657 - j4)^2$, $\varepsilon_{r1} = 1.5^2$, and $\varepsilon_{r3} = 1.55^2$ [19].

2. Metal stripe

A metal slab with finite width creates the metal stripe structure. The finite width of metal stripe waveguide provides lateral confinement of the LRSPP mode. Consequently, the LRSPP mode of the metal stripe has lower attenuation than the LRSPP mode of the slab waveguide (as discussed in 1). Contrary to the metal slab configuration, the field distribution of metal stripe cannot be analytically derived from Maxwell's equations and must be calculated using numerical methods. Fig. 2.7 shows the cross section of a metal stripe waveguide in which the metal stripe with dielectric permittivity of ε_{r2} is bound by dielectrics with permittivity of ε_{r1} and ε_{r3}.

The modes of a metal stripe plasmonic waveguide were first calculated using Method of Line (MoL) by Berini [19]. The metal stripe has four fundamental modes which are defined by the distribution of E_y component as aa_b^0, as_b^0, sa_b^0, and ss_b^0. In this definition, a and s stand for asymmetric and symmetric mode. The first letter in each of aa_b^0, as_b^0, sa_b^0, and ss_b^0 definitions refer to the symmetry or asymmetry of the mode in the horizontal direction (x), while the second letter defines the symmetry or asymmetry of the mode in the vertical direction (y). In the case of thin symmetric metal stripe, the ss_b^0 mode is the fundamental LRSPP mode. Fig. 2.8 shows the

contour and 3D plots of the real part of Poynting vector (Re $\{S_z\}$) of ss_b^0 mode for Ag stripe with relative dielectric permittivity of $\varepsilon_{r2} = -19 - j0.53$ and width of $w = 1$ μm, surrounded by dielectrics of relative permittivity of $\varepsilon_{r1} = \varepsilon_{r3} = 4$ at four different waveguide thicknesses and wavelength of $\lambda_0 = 633\ nm$ [19].

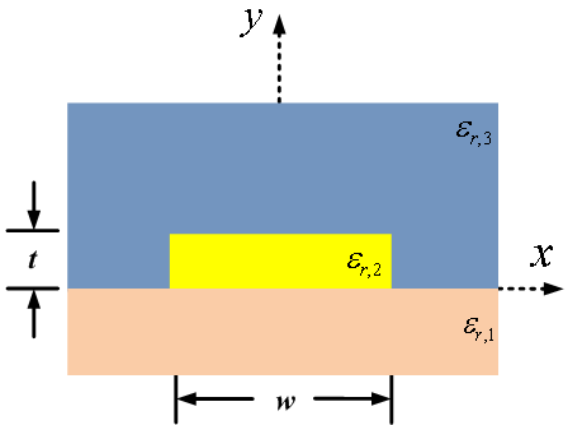


Fig. 2.7. Cross section of the metal stripe waveguide with a thickness of *t*, and width of *w* bounded by semi-infinite dielectrics.

The finite-width embedded metal structure provides 2D mode confinement in the transverse plane and therefore can be exploited to implement passive optical components [16]. As the thickness of embedded metal decreases, the attenuation of SPP mode also decreases which leads to increased propagation length. Using long-range SPP waveguides (LRSPPWs), the propagation losses due to the metal absorption is reduced by minimizing the longitudinal component of the electric field in the metal [16].

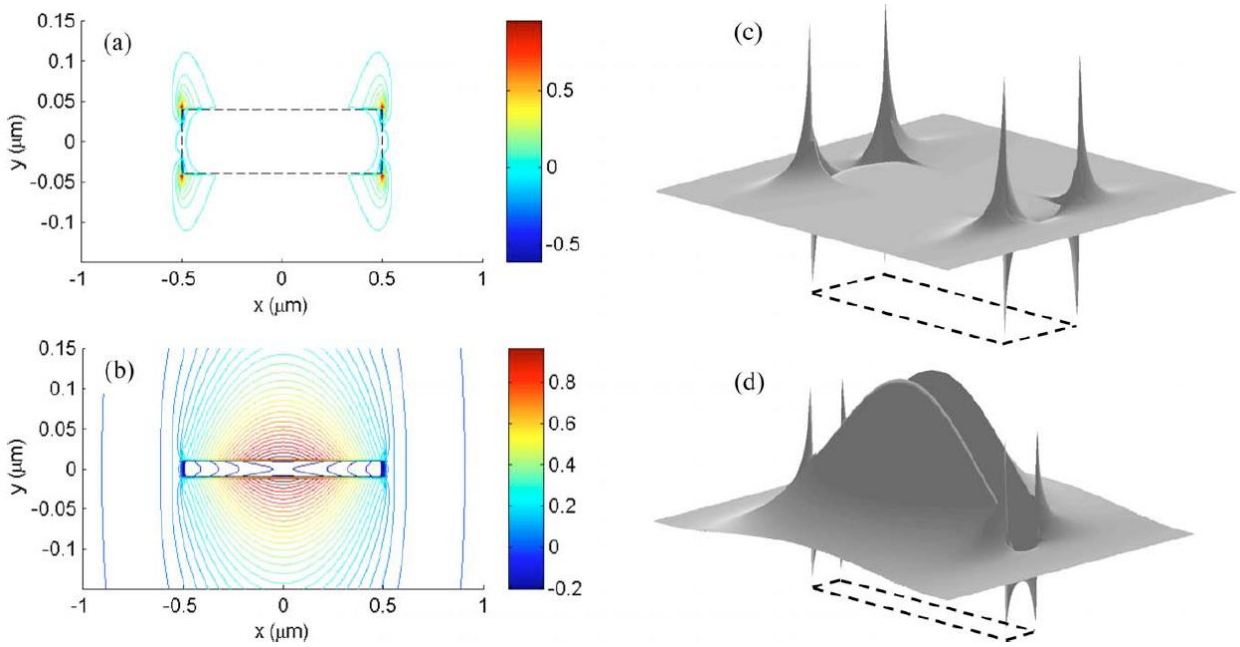


Fig. 2.8. Contour and 3D plots of $\mathrm{Re}\{S_z\}$ of ss_b^0 mode for w=1 μm (a) t=80 nm, (b) t=20 nm, (c) t=100 nm, (d) t=40 nm [19].

For sufficiently thin metal films, the mode field diameter of LRSPP becomes large enough to enable the excitation of LRSPPs to TM-polarized Gaussian-like beams in an edge coupling arrangement [19]. Fig. 2.9 shows a longitudinal cross-sectional view of edge coupling between fiber and the structure. Edge coupling can be achieved with a polarization-maintaining single mode fiber (PM-SMF) or tapered SMF as well as the polarization aligned mode of a SMF.

Burke et al. first proposed the edge coupling of LRSPPs [20]. Then Charbonneau et al. experimentally demonstrated the edge coupling to thin gold stripes embedded in silica glass [21]. Moreover, Nikolajsen et al. demonstrated LRSPP excitation with coupling loss of 0.5 dB, and 6–8 dB/cm propagation loss at telecom wavelengths along 10-nm-thin gold stripes embedded in polymer [22]. Fortunately, LRSPP edge-coupling to SM-fiber is achievable with more than 90% efficiency [19].

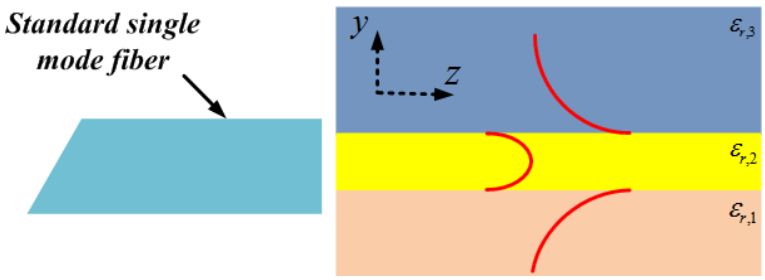


Fig. 2.9. Longitudinal cross-sectional view of edge coupling between the fiber and the structure input.

2.2. Plasmonic interconnects

Plasmonic provides a platform for the realization of low-cost and power efficient optical interconnect [23]. The metallic dielectric interface of SPP waveguides provides an efficient interface between electrical and optical signals, which can merge broadband optical links with intelligent electronic processing [23].

Polymer-based LRSPP devices are of great interest for implementation of plasmonic waveguide optical interconnects due to low absorption loss of polymer materials and their large thermo-optic coefficient (e.g., switching applications) [23]. In [24] by Ju et al., the LRSPP waveguide consists of a gold stripe of 14 nm thickness, 2.5 µm width, and 4 cm length embedded in a UV curable polymer. The LRSPP waveguide has 3 dB/cm propagation loss. The optical chip was diced, and the facets were pigtailed and polished with V-grooved single mode fibers. The authors experimentally demonstrated the transmission of 10 Gbps optical signal through a pigtailed 4-cm Au stripe LRSPP waveguide. In the 10 Gbps data transmission experiment, the device has 1.7 dB power penalty at 10^{-9} BER and 2.2 dB power penalty at 10^{-12} BER.

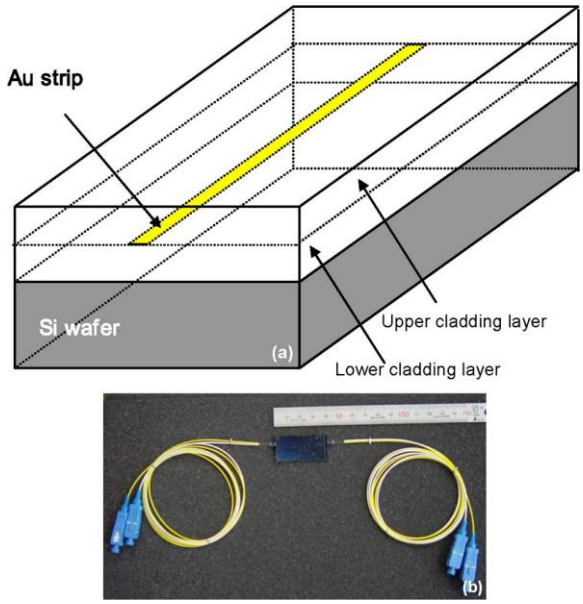


Fig. 2.10. (a) Schematic diagram of an Au stripe waveguide based on LRSPP and (b) the pigtailed LRSPP waveguide [24].

In [25] by Ju et al., a 4 cm LRSPP waveguide consisting of gold metal stripe embedded in a low loss polymer is fabricated, and the authors experimentally demonstrated 40 Gbps optical signal transmission through the device. In [26] by Ju et al., a flexible optical interconnect based on LRSPP waveguides is demonstrated. The interconnect length is 7 cm with 2.5 Gbps data rate. The LRSPP waveguide consists of an 8 nm thick silver stripe embedded in a free-standing multilayer polymer film composed of a 10 μm thick inner cladding (refractive index = 1.432), and a pair of 20 μm thick outer claddings (refractive index = 1.422). At a wavelength of 1310 nm, the insertion loss of the fabricated LRSPP waveguide does not dramatically change by bending the waveguide to a radius of 2 mm or twisting it to 90º. After transmission of a digital signal through the fabricated waveguide, an eye pattern of 2.5 Gbps is measured. The authors demonstrate the transmission of the high definition (HD) image captured by a mobile phone camera into the liquid crystal display (LCD) using LRSPP optical interconnect [26].

Fig. 2.11. The flexible plasmonic waveguide connecting transmitter and receiver ICs [26].

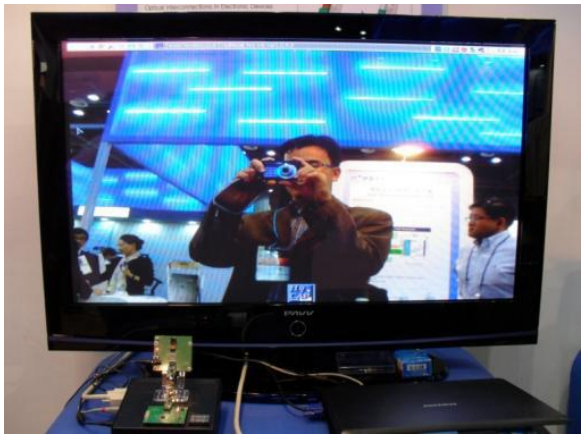


Fig. 2.12. The mobile phone camera records HD digital image then the image data is transmitted to the LCD using the LRSPP interconnect [26].

In [27] by Kim et al., an on-board chip-to-chip optical interconnect using LRSPP waveguide is implemented. As illustrated in Fig. 2.13, the structure consists of driver IC and a vertical-cavity-surface-emitting-laser (VCSEL) array chip as the optical transmitter module, a photodiode array chip as the receiver module, and a polymer-based LRSPP waveguide. Data transmission of four channels of 2.5 Gbps is accomplished at a wavelength of 1.3 μm. As the width of the metal stripe is reduced the propagation loss reduces, however, this comes at the cost of increased mode field diameter and consequently higher coupling loss between LRSPP and VCSEL modes.

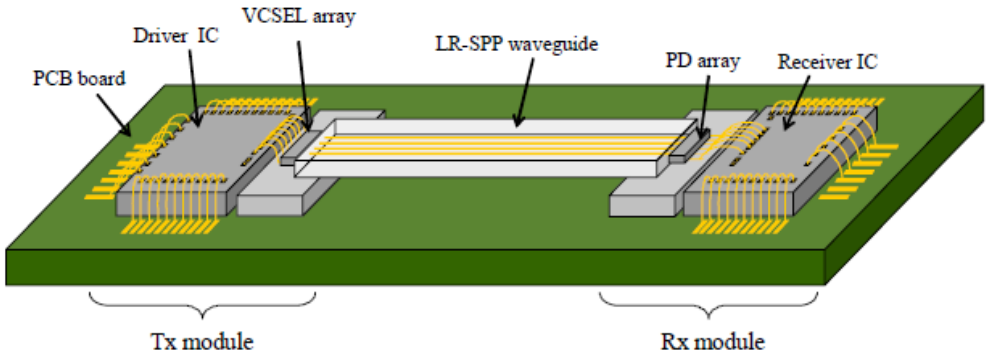


Fig. 2.13. On-board chip-to-chip optical interconnect using polymer based Au LRSPP waveguide [27].

In [28] by Kalavrouziotis et al., the transmission of twelve WDM-enabled channels of 40 Gbps Non-Return-to-Zero (NRZ) modulated data through a 60 µm long straight dielectric-loaded SPP waveguides (DLSPPW) is demonstrated. DLSPPWs consist of a dielectric stripe deposited on top of a metallic film which demonstrates sub-wavelength confinement of SPPs with the typical propagation distance of 50 µm at 1550 nm wavelength [29]. The propagation length of DLSPPW can be significantly improved to mm-long SPP guiding using the long-range DLSPPWs (LR-DLSPPWs). In [29], the authors experimentally demonstrate the transmission of 10 Gbps on-off keying (OOK) modulated signal through the LR-DLSPPWs. Fig. 2.14 illustrates the cross-section of the fabricated waveguide which has a length of 300 µm.

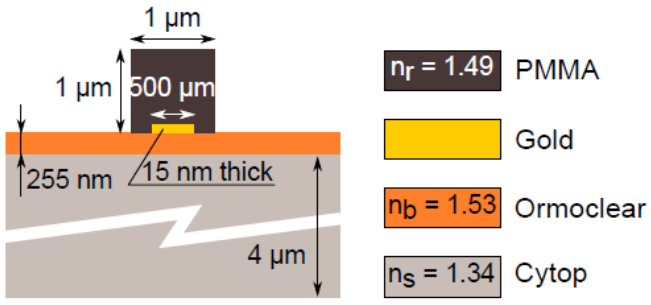
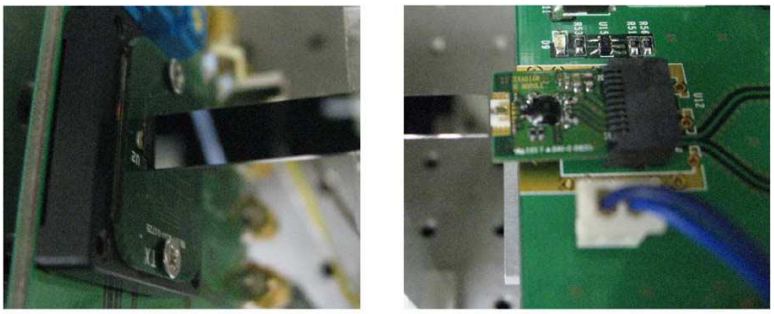


Fig. 2.14. The layout of the LR-DLSPP waveguide structure [29].

To reduce the propagation loss of gold-based LRSPP waveguides at 1.3 µm wavelength, one can reduce the thickness of the metal layer. However, this comes at the cost of mode field diameter (MFD) increase and larger coupling loss to the SPP waveguide. In [23] due to the lower absorption

of silver, the authors investigated silver-based LRSPP waveguides and compared the results with those of gold-based LRSPP waveguides. A 2.5 Gbps chip-to-chip optical signal transmission through a 10-cm-long silver stripe optical waveguide was successfully demonstrated. The lowest measured propagation loss was 0.8 dB/cm corresponding to LRSPP waveguide with a 14 nm thickness and 1.5 μm width of the metal stripe at the wavelength of 1.3 μm.



(a) (b)

Fig. 2.15. Assembled chip-to-chip optical interconnection system installed with 10-cm-long silver stripe waveguide, (a) Coupling between TM-VCSEL and silver stripe optical waveguide, (b) coupling between silver stripe optical waveguide and photodetector (PD) [23]. © [2009] IEEE.

Table 2.1 summarizes different demonstrations of modulated data transmission through plasmonic waveguides. The transmission length, loss, and transmitted data rate of different demonstrations are given in the table.

Table 2.1 Different demonstrations of modulated data transmission through a plasmonic waveguide.

Ref	Technology	Loss (dB/cm)	Transmission length	Wavelength (nm)	Data rate
Ju et al. (2007) [24]	A gold stripe of 14 nm thickness and 2.5 µm width embedded in ZPU polymer	3	4 cm	1550	10 Gbps
Ju et al. (2007) [25]	A gold stripe of 2.5 µm width and 14 nm thickness embedded in ZPU polymer	2	4 cm	1550	40 Gbps
Ju et al. (2012) [26]	An Ag stripe of 8 nm thickness and 5 µm width embedded in ZPU polymer	1	7 cm	1310	2.5 Gbps
Kim et al. (2008) [27]	14.5 nm-thick, 3 µm width Au stripe embedded in ZPU polymer	6	2.5 cm	1300	10 Gbps (4x2.5 Gbps)
Kalavrouziotis et al. (2012) [28]	DLSPPW, gold film with 65 nm thickness and 3 µm width and a PMMA stripe with 500x600nm^2 cross section	1000	60 µm	1542 - 1560	480 Gbps (12x40 Gbps)
Kharitonov et al. (2014) [29]	Gold stripes of 15 nm thickness covered with PMMA polymer	-	300 µm	1550	10 Gbps
This work	Gold stripe of 35 nm thickness and 5 µm width embedded in Cytop	35 (simulated)	3.6 mm	1550	196 Gbps (4x49 Gbps)
	Gold stripe of 25 nm thickness and 30 µm width embedded in Cytop	18	4.6 mm	1550	40 Gbps

2.3. Conclusion

In this chapter, first basics of surface plasmon polaritons physics were explained. Then, it was discussed that SPPs could only be excited if they are exposed to either electrons or photons with the right momentum. This chapter explained long-range SPPs properties on thin metal films where low propagation loss and edge coupling compatibility make this structure a viable solution for chip-to-chip interconnects. The low attenuation comes at the expense of large mode distribution, so careful design consideration is required for implementation (e.g., mode size mismatch with optical source). Finally, a few previous works where LRSPPs are implemented as optical interconnect were discussed.

3. Plasmonic stripe waveguide

3.1. Introduction

This chapter explains the design procedure of an LRSPP waveguide made of embedded thin gold stripes in Cytop amorphous fluoropolymer. The fabricated device is characterized and its system-level performance for transmitting multiple OOK (4×49 Gbps) and differential phase shift keying (DPSK) (4×10 Gbps) modulated channels is investigated. The signal transmission was verified through bit-error-rate (BER) measurements. The author of this thesis has published the discussions presented in this chapter in the following paper:

- B. Banan, M. S. Hai, E. Lisicka-Skrzek, P. Berini, and O. Liboiron-Ladouceur, "Multi-channel transmission through a gold stripe plasmonic waveguide embedded in Cytop," IEEE Photon. J. 5(3), 2201811 (2013).

3.2. Design of the LRSPP waveguide

This section discusses the design and simulation results of LRSPP waveguide comprised of embedded thin gold stripes in Cytop amorphous fluoropolymer. The main characteristics of Cytop for interconnect applications are its transparency at optical frequencies, low refractive index, low dispersion coefficient, and good lamination properties [30]. The schematic of the plasmonic stripe waveguide is shown in Fig. 3.1. The relative permittivity (ε_1) of the gold stripe is assumed to be -131.95+12.65i (refractive index, n = 0.55+11.5i) at a wavelength of 1.55 μm (ε_1 is an adjusted value based on optical loss measurement on thin gold strips) [31]. While the refractive index of Cytop is 1.3335 at 1.55 μm [30]. The Cytop layer is thick enough to accommodate LRSPP modes and neglect the effect of silicon layer on LRSPP mode.

Plasmonic stripe waveguide

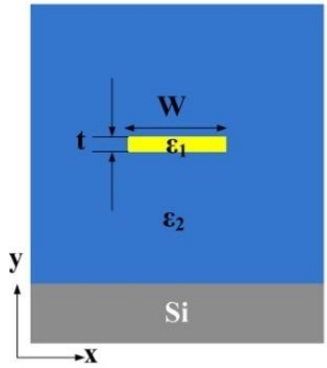


Fig. 3.1. Schematic of the plasmonic stripe waveguide cross section © [2013] IEEE.

Lumerical MODE Solutions software is used to simulate the structure and obtain attenuation and mode field diameter (MFD). The software meshes the cross section of the waveguide using finite-difference algorithm and then solves Maxwell's equations by sparse matrix technique to calculate effective index and mode profile. In the simulation, thickness *t* is varied from 10 to 35 nm, and width *w* is varied from 2 to 8 µm in 1.5 µm increments. It must be mentioned that the LRSPP mode does not have cut-off thickness, and it remains guided at t → 0, since it evolves into the TEM mode supported by the background dielectric. On the other hand, the higher order modes cannot propagate as t → 0, because their mode fields do not evolve into a TEM mode. Fig. 3.2 illustrates the simulation results obtained for attenuation of different gold widths and thicknesses. As seen, attenuation decreases with decreasing thickness and width, as expected [16]. The lowest simulated attenuation obtained for a 10 nm thick gold film corresponds to 0.01902 dB/m, which is achieved when the width is designed to be 2 µm. Fig. 3.3 shows the near-field image of the dominant electric field ($Re\{E_y\}$) distribution of a 5 µm wide and 35 nm thick gold stripe. These dimensions were used for the fabricated devices. In Fig. 3.4, calculated MFD along the lateral and vertical slices of the LRSPP mode is shown. The MFD in this case is defined as the full-width electric field (($Re\{E_y\}$)) spot size at 1/e points. In general, both lateral and vertical MFDs become larger with decreasing gold thickness and width. The exception is the lateral MFD for 10 and 20 nm-thick gold stripes with a width in the range of 8 down to 5 µm, and this is attributed to the fact that the lateral MFD is always larger than the width of the metal stripe [32]. As seen from simulation result, there is a clear trade off between attenuation (see Fig. 3.2) and MFD (see Fig. 3.4). These results are in good agreement with previously reported works [25], and [33–35].

Plasmonic stripe waveguide

The low refractive index of Cytop (n = 1.3335 at 1.55 μm) leads to lower LRSPP propagation loss compared with higher index materials such as ZPU450, at the expense of lower confinement. For instance, theoretically, a gold stripe of 20 nm thickness and 5 μm width embedded in ZPU450 is expected to have approximately 6.5 dB/cm attenuation, and an MFD of approximately 8 μm laterally and 7 μm vertically [33]. On the other hand, the same gold stripe fabricated in Cytop is expected to have approximately 3.6 dB/cm attenuation with lateral MFD of 8.2 μm and vertical MFD of 10.2 μm.

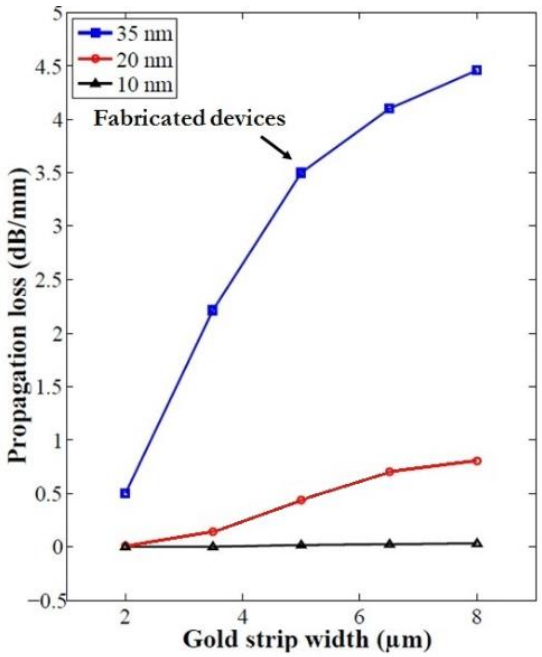


Fig. 3.2. Simulated propagation loss as a function of gold stripe width *w* and thickness *t*. © [2013] IEEE.

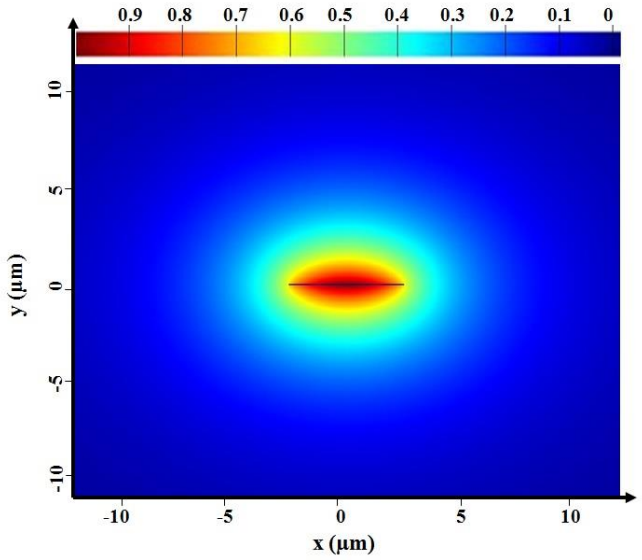


Fig. 3.3. The near-field image of the electric field ($\mathrm{Re}\{E_y\}$)distribution of the 5-µm-wide and 35 nm-thick gold stripe. (These dimensions were used for the fabricated devices.) © [2013] IEEE.

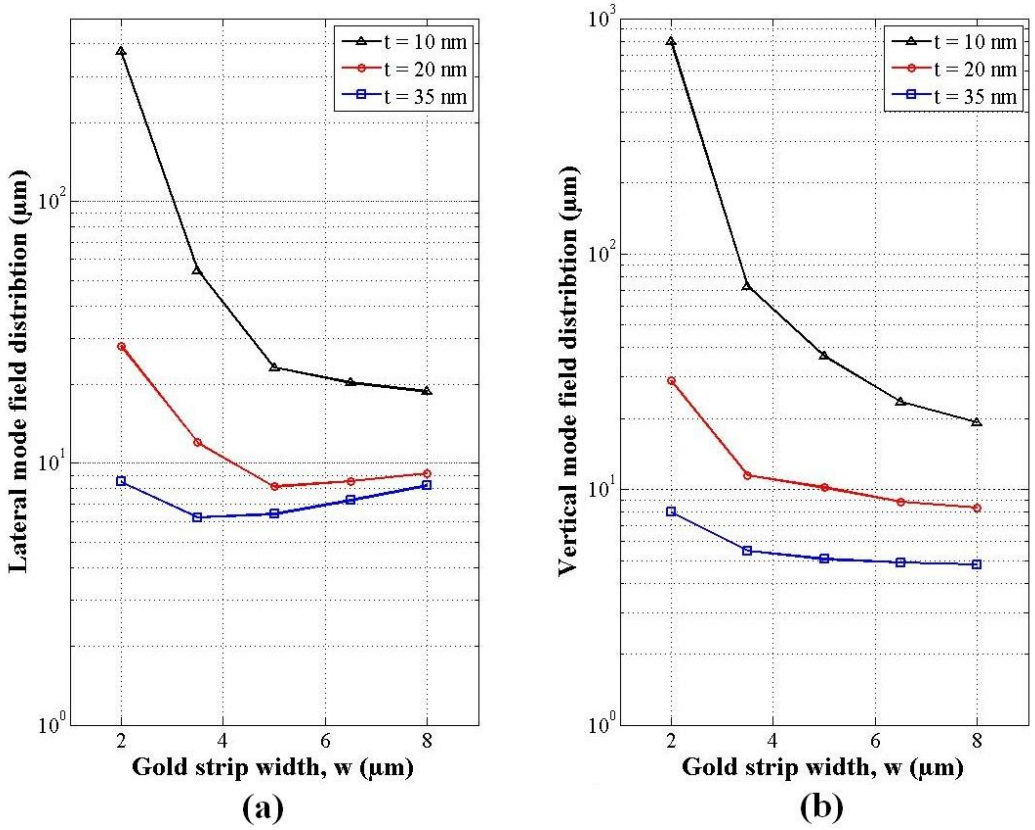


Fig. 3.4. Simulated (a) lateral and (b) vertical MFD as a function of gold stripe width (*w*) and thickness (*t*). © [2013] IEEE.

3.3. Fabrication of the LRSPP waveguide

The structure used in the experimental demonstration was fabricated as follow: first, a 7 μm thick layer of the Cytop polymer is coated on a silicon wafer using multiple spin coating and solvent evaporation to form the lower cladding. The wafer is then patterned using bilayer reentrant photolithography. A 35 nm-thick layer of gold (Au) is then deposited using E-beam evaporation followed by wet solvent stripping to reveal the metal structures. Thickness of the gold layer is verified through atomic force microscopy (AFM). The structures are then covered by an additional 7 μm thick layer of Cytop to form the upper cladding. Gold stripe dimensions were chosen to provide a reasonable trade-off between attenuation and mode confinement. Also, based on computations, with chosen dimensions, the coupling loss between the LRSPP waveguide and a standard single-mode fiber (SMF-28, MFD of 10.4 μm and numerical aperture (NA) of 0.14) is sufficiently low (0.52 dB/facet). Moreover, there are some fabrication challenges, which need to be considered while determining the gold stripe thickness (discussed in detail in chapter 4). Finally, the wafer is diced into several dies, and the length of the LRSPP waveguides is set to 3.6 mm (fabrication details for this structure can be found in [36]).

3.4. Measurement

3.4.1. Single NRZ-OOK Channel at 40 and 49 Gbps

Error! Reference source not found.(a) shows the schematic of the experimental setup for insertion loss and mode profile measurements. The input power at 1.55 μm (10 dBm) is provided by a laser source with its fiber coupled output passing through a polarization controller. The polarized output signal (9.5 dBm) is sent through a Mach–Zehnder modulator (MZM), which has a 3-dB electrical bandwidth of 33 GHz. The electrical amplifier of the MZM has a 3-dB bandwidth of 40 GHz. The DC bias of the MZM is set at 1.8 V (approximately $V_\pi/2$) to produce an OOK signal with maximum eye opening. A 50 Gbps 4:1 MUX clocked by a signal generator drives the modulator at 40 and 49 Gbps with a $2^{31}-1$ pseudo-random binary sequence (PRBS) non-return-to-zero (NRZ) electrical data using a pulse pattern generator (PPG). Then, the signal is amplified to an optical power level of 10 dBm using an erbium-doped fiber amplifier (EDFA). The modulated optical signal passes through a polarization controller exciting LRSPPs with TM

polarized light. **Error! Reference source not found.**(b) shows one of the fabricated waveguides with the electrical DC pads attached to it, which are designed to investigate the thermo-optic effect of the LRSPP mode (not used in this section). The output signal is edge coupled to the chip through a standard single-mode fiber with alignment control accomplished using a 6-axis nano-positioner stage. Then, the output power from the structure is collected using a 20× microscope objective and collimated. The beam passes through a variable aperture (500 µm to 18 mm) and then is divided by a 50/50 non-polarizing cubic beam splitter to simultaneously direct the light to IR-camera and free space power meter.

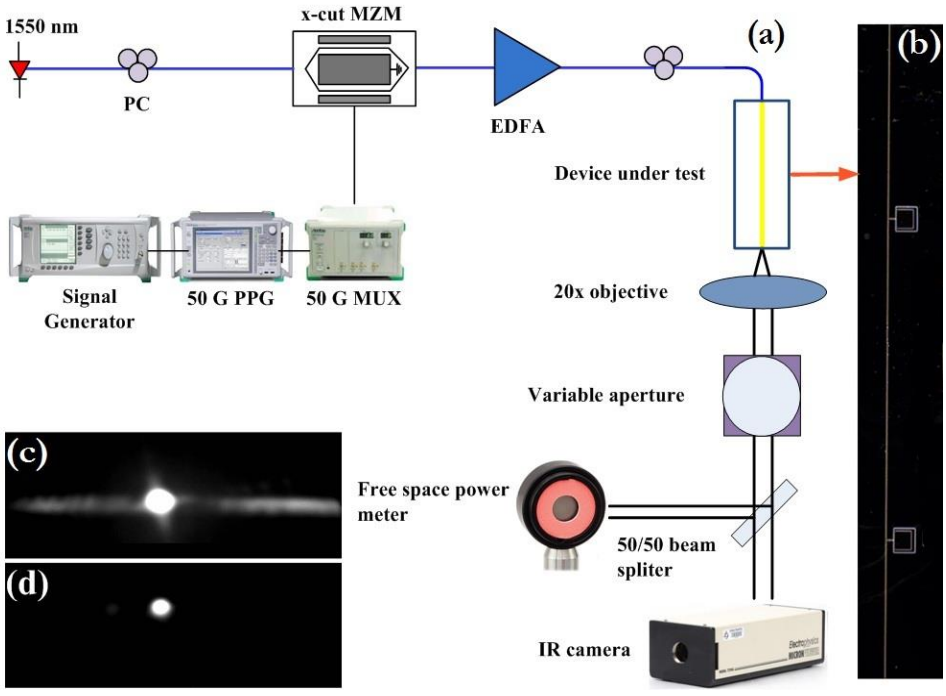


Fig. 3.5. (a) Schematic of the setup to measure the insertion loss and capture the mode profile. (b) Fabricated devices, (c) Far-field captured LRSPP and scattered light from the cladding layer (open aperture), (d) Far-field captured LRSPP (partially closed aperture and attenuated). © [2013] IEEE.

Error! Reference source not found.(c) illustrates the far-field captured LRSPP when the aperture is open (aperture diameter of 18 mm). The background light is primarily attributed to the random polarization of amplified spontaneous emission (ASE) noise emerging from the EDFA and leaking of the uncoupled light through the polymer. **Error! Reference source not found.**(d) shows the far-field captured LRSPP when the aperture is partially closed in order to block the background light and also attenuated by approximately 50% using a free-space attenuator. The

average measured insertion loss from seven different straight waveguides with 3.6 mm in length is 13.2 dB, which is in good agreement with the simulation result. Simulation predicted 3.45-dB/mm attenuation, which corresponds to 12.42 dB propagation loss for the length of 3.6 mm. In addition, the expected coupling loss between the fabricated LRSPP waveguide and SMF-28 is 0.52 dB/facet. Therefore, considering the insertion loss measurement setup (see **Error! Reference source not found.**(a)), the expected total loss was 12.94 dB, which is close to the measured values. The experimental setup for the eye diagram and BER measurements is illustrated in Fig. 3.6. The input to the chip is similar to the previous setup. At the output, the power is collected using a standard single-mode fiber, and alignment control is accomplished by a 3-axis nano-positioner stage. Then, the signal is amplified using a second EDFA and passes through a tunable filter (0.85 nm) to remove out-of-band ASE noise. The output is connected to a variable optical attenuator (VOA), and then, a 10/90 coupler is used to send the signal to an optical spectrum analyzer (OSA) and a PD (3-dB bandwidth of 47 GHz), respectively. The signal is analyzed using a digital communication analyzer with 30 GHz of RF bandwidth and a 50 Gbps 1:4 DEMUX connected to a 50-Gbps capable error detector. Fig. 3.7 shows the measured BER for a single channel with respect to the received power at the PD for the back-to-back and transmitted signals. In the case of back-to-back measurements, the device is replaced by an attenuator set to the corresponding plasmonic waveguide total loss (approximately 14 dB). The inset shows the eye diagrams for the back-to-back (top) and transmitted signals (bottom) at 40 and 49 Gbps, respectively. As seen from the measurements, the LRSPP waveguide effectively transmits optical data with negligible power penalties at 40 and 49 Gbps, and error-free performance (BER < 10^{-9}) has been achieved. The power penalty between the two data rates is 0.86 dB at BER of 10^{-9}. The noise floor for 49 Gbps transmission is caused by the bandwidth limitation of the optoelectronic components used in the experimental setup, which primarily originates from the MZM's optimum point of operation being at 40 Gbps.

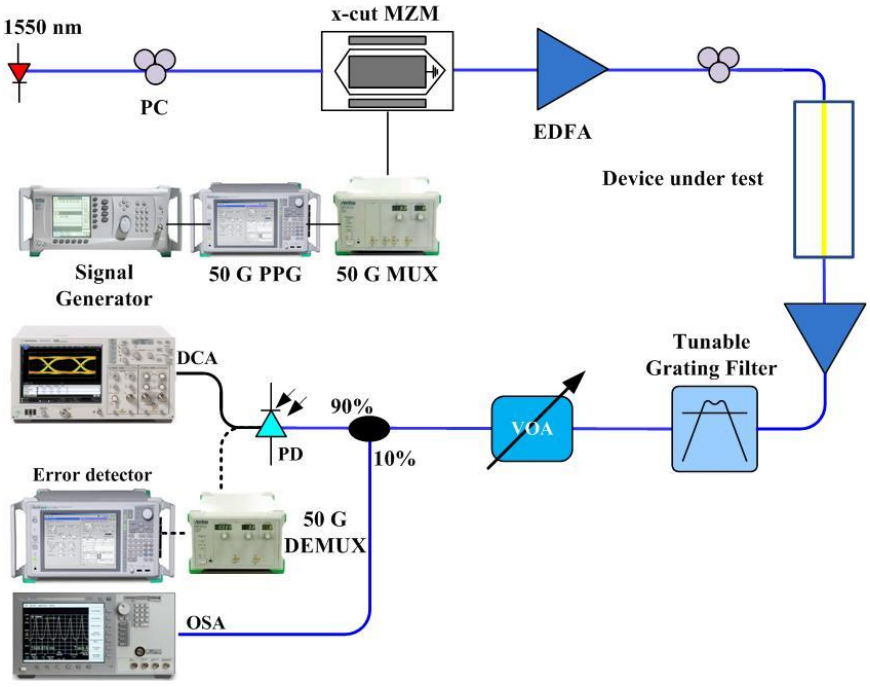


Fig. 3.6. Schematic of the setup for a single channel at 1550 nm to measure the BER. © [2013] IEEE.

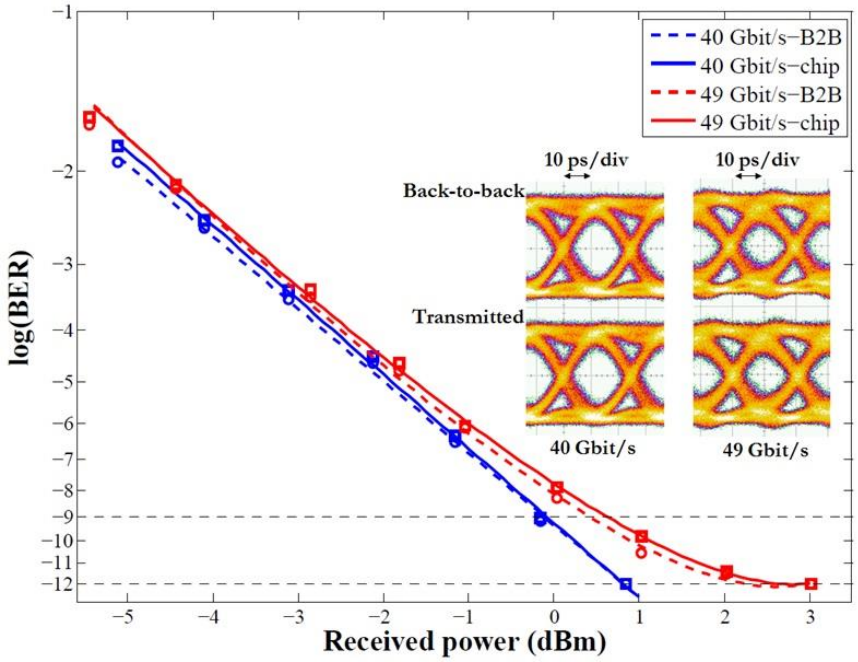


Fig. 3.7. Measured BER versus the received power for a single channel at 40 and 49 Gbps. (The inset shows the eye diagrams). © [2013] IEEE.

3.4.2. Multiple NRZ-OOK Channel at 49 Gbps

Fig. 3.8 shows the schematic of the experimental setup for four channels with OOK modulation transmission. Four 10-dBm distributed feedback laser sources are each fiber coupled to polarization controllers and are emitting at 1536.12, 1536.93, 1537.71, and 1538.59 nm. The four channels are separated by approximately 0.79 nm matching the 100-GHz international telecommunication union (ITU) grid. The polarized output signal (9.5 dBm) from each channel is sent to a 4×1 coupler (resulting in ~7 dB loss) and then passes through the modulator. A 50 Gbps 4:1 MUX clocked by a signal generator drives the modulator at 49 Gbps with a $2^{31} - 1$ PRBS electrical data using a PPG. Then, the signal is amplified to a power level of 7.5 dBm per channel using an EDFA. Finally, the modulated optical signals pass through a polarization controller to obtain LRSPPs from TM polarized light.

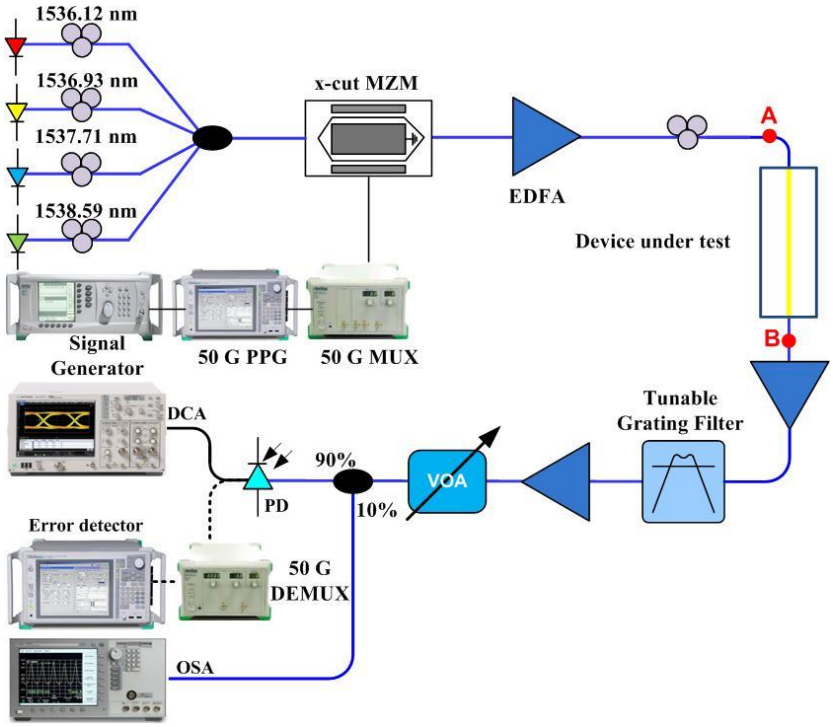


Fig. 3.8. Schematic of the setup for four channels OOK signals transmission to measure the BER.

Fig. 3.9 shows the optical spectrum of the four channels at the input and output of the chip (with 0.06-nm resolution) corresponding to points A and B in Fig. 3.8, respectively. The input

signal is edge coupled to the fabricated chip through a 10-μm single-mode fiber using a 6-axis nano-positioner stage. At the output, the power is collected using a 10-μm single-mode fiber aligned with a 3-axis nano-positioner stage. Then, the signal is amplified to 7 dBm per channel using a second EDFA and then passes through a tunable filter (0.4 nm) to select the channel under test and remove out-of-band ASE noise. The signal is again amplified with an EDFA, and the output is connected to a VOA, and a 10/90 coupler is used to simultaneously send the signal to an OSA and a photodetector. Fig. 3.10(a) shows the measured BER versus the received power at the photodetector for the back-to-back and transmitted signals. In the case of back-to-back measurements, the device is replaced by an attenuator set to the corresponding plasmonic waveguide total loss (approximately 15 dB). The 1-dB increase in total loss compared with the single-channel transmission is due to the wavelength dependency of the LRSSP propagation loss. Error-free performance is achieved only for two channels, and a noise floor appears, which is due to the additional ASE noise associated with the third EDFA. This leads to an OSNR limitation of the experimental setup. Fig. 3.10(b) shows the eye diagrams for the back-to-back (top) and transmitted signals (bottom) at 49 Gbps. As observed, the eye diagrams are noisier compared with that of the single-channel transmission. However, both the back-to-back and transmitted eye diagrams exhibit the same level of noise. Thus, the power penalty is relatively low. At a BER of 10^{-7}, where the noise floor is minimum, the power penalty is negligible, except for the channel at 1536.93 nm where it is less than 1 dB.

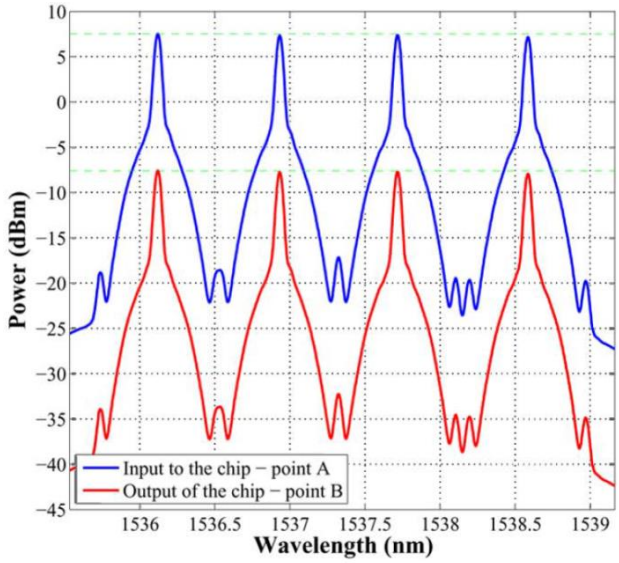


Fig. 3.9. Input (blue) and output (red) signals of the chip with OOK modulation at 49 Gbps corresponding respectively to points A and B in Fig. 3.8. © [2013] IEEE.

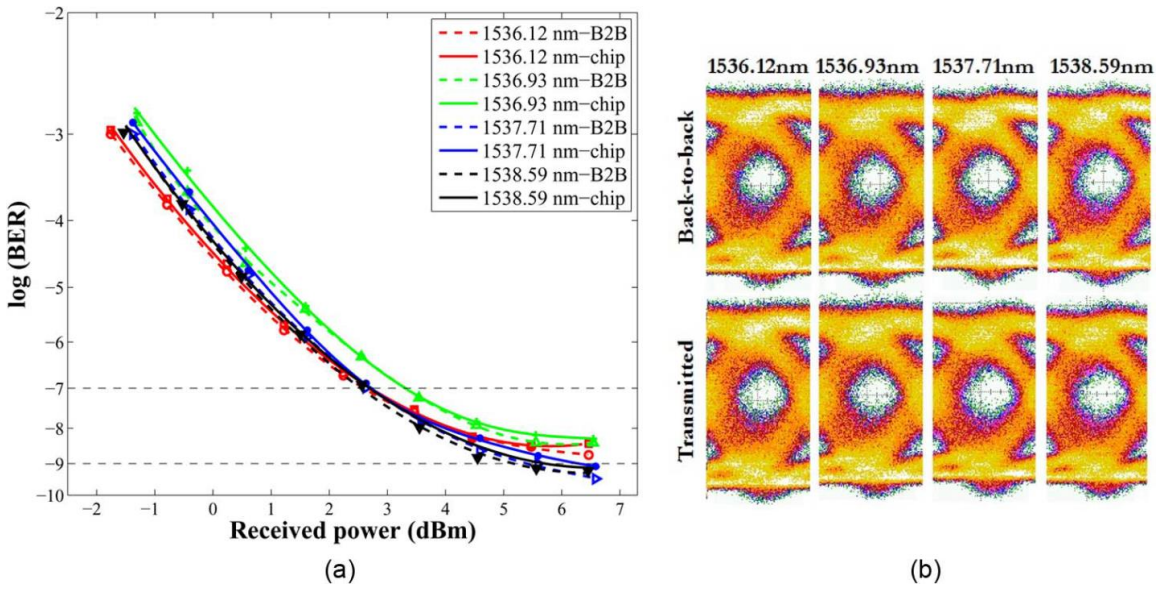


Fig. 3.10. (a) Measured BER and (b) eye diagrams for the back-to-back and transmitted signals for four channels with OOK modulation at 49 Gbps. © [2013] IEEE.

3.4.3. Multiple NRZ-DPSK Channel at 10 Gbps

Fig. 3.11 shows the schematic of the experimental setup for four channels with the DPSK modulated signal transmission. The setup is similar to the OOK transmission setup described in the previous section, except at the input where the MZM has a 3-dB electrical bandwidth of 12 GHz (The maximum input data rate of the electrical amplifier of the MZM is 12.5 Gbps). The DC bias of the MZM is set at 2.5 V (approximately V_π) to generate the DPSK modulated signal with maximum eye opening. A 50-Gbps 4:1 MUX clocked by a signal generator drives the modulator at 10 Gbps with a $2^{31}-1$ PRBS electrical data using a PPG. Additionally, at the receiver end, a 10 Gbps DPSK delay line demodulator is added, which converts the phase variation of the DPSK modulated signal to intensity variation. Another EDFA is added after the demodulator to compensate for the insertion loss of the demodulator.

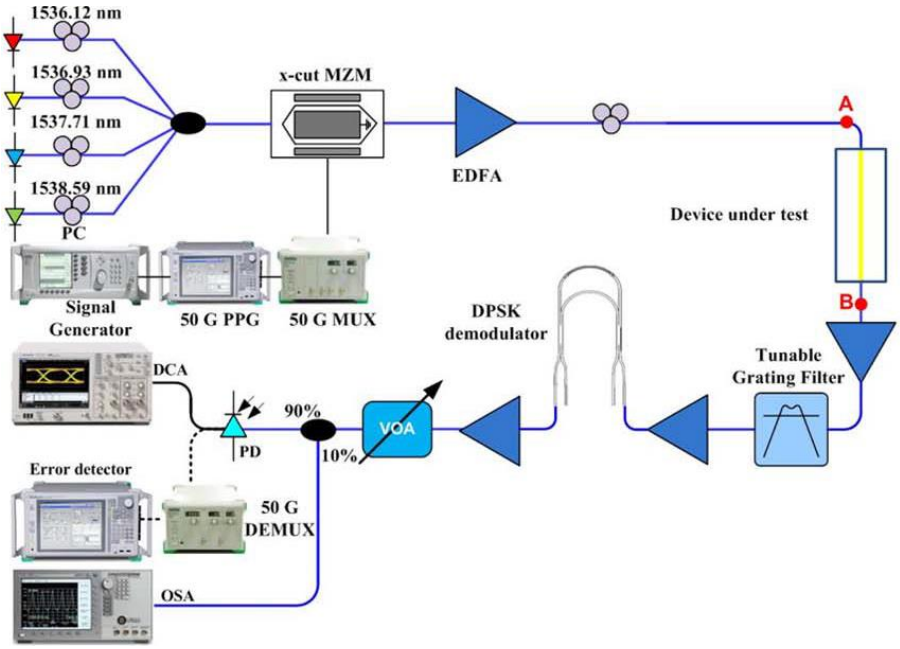


Fig. 3.11. Schematic of the setup for four channels DPSK signals transmission to measure the BER. © [2013] IEEE.

Fig. 3.12 shows the optical spectrum of the four channels at the input and output of the chip, corresponding to points A and B in Fig. 3.11, respectively.

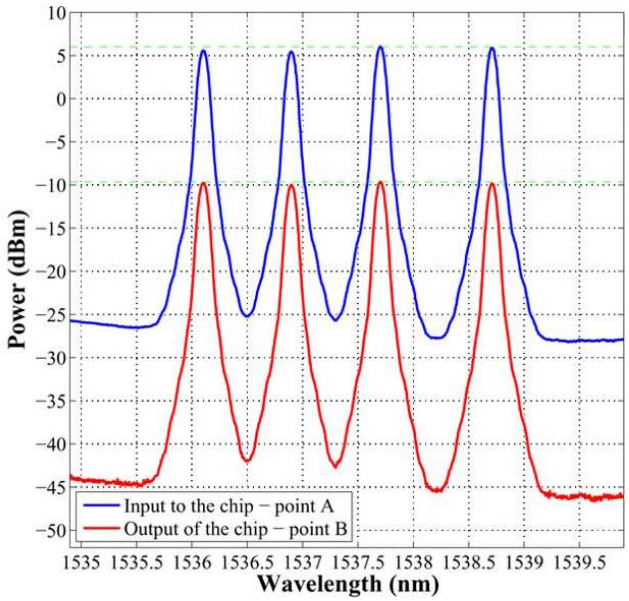


Fig. 3.12. Input (blue) and output (red) signals of the chip with DPSK modulation at 10 Gbps corresponding to points A and B in Fig. 3.11, respectively. © [2013] IEEE.

Fig. 3.13 shows the measured BER versus the received power at the photodetector for the back-to-back and transmitted DPSK signals. From Fig. 3.13, it is seen that error-free operation (BER < 10^{-9}) is achieved for all channels with negligible power penalty for two channels and less than 1 dB for the other two channels. Furthermore, roughly a 1-dB wavelength dependency is observed, and this can be attributed to the frequency response of the delay line demodulator. The insets show the received open eye diagrams produced from single-ended DPSK demodulation for transmitted signals through the chip for all channels at BER of 10^{-12}. For received eye diagrams, the constructive output port of the DPSK demodulator is shown for the two channels. The DPSK eye diagrams show the presence of noise in the system, which is attributed to the ASE noise emerging from four EDFAs in the experimental setup. Furthermore, our measurements showed no sign of phase shift due to possible nonlinear effects in the waveguide.

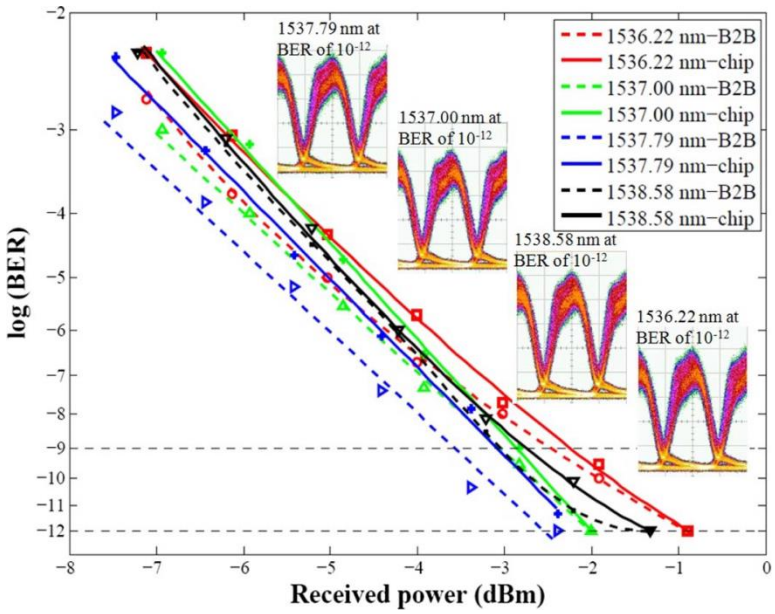


Fig. 3.13. Measured BER for four channels with DPSK modulation at 10 Gbps. The insets show eye diagrams of the transmitted signal for all channels at BER of 10^{-12} © [2013] IEEE.

3.5. Transmission distortion analysis

By comparing the transmission with the back-to-back measurements, it is concluded that the LRSPP waveguide introduces negligible dispersion. Which is in good agreement with expectations as Cytop has very low material dispersion at 1.55 µm [37], and waveguides are short with low

confinement (i.e., the fields do not overlap strongly with the dispersive metal). Fig. 3.14 shows the calculated dispersion parameter of the LRSPP mode as a function of wavelength.

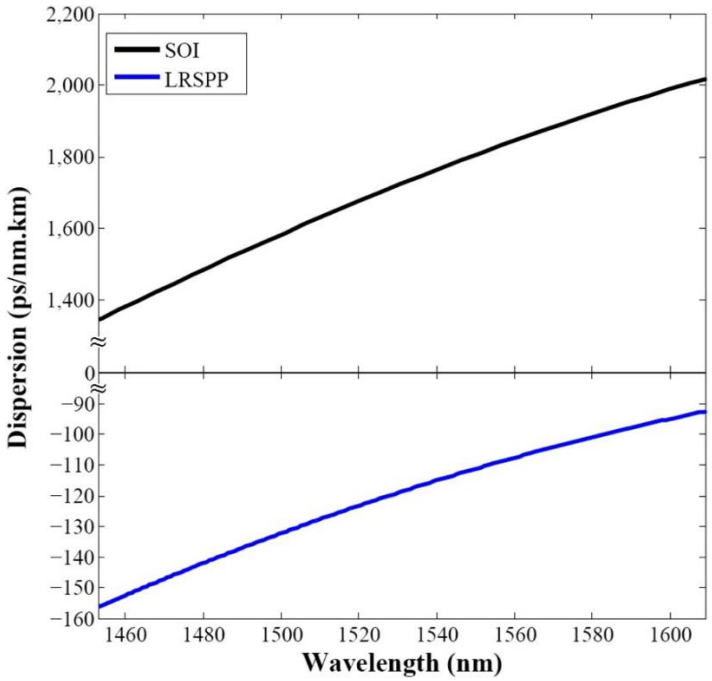


Fig. 3.14. Calculated dispersion for silicon on insulator (SOI) waveguide with 525-nm width and 226-nm thickness and embedded gold stripe with 5-μm width and 35-nm thickness in Cytop polymer© [2013] IEEE.

The waveguide exhibits about D = -111 ps/(nm.km) at 1.55 μm. The calculated dispersion is low compared with silicon-on-insulator (SOI) waveguides, which are proposed for on-chip photonic interconnections. For silicon waveguides of 525-nm width and 226-nm thickness, the dispersion parameter D ≅ 1800 ps/(nm.km) (see Fig. 3.14) and ~4400 ps/(nm.km) (experimental [38]). The dispersion length can be estimated for a half-pulse width at the 1/e power points, T_0 = 5 ps (for a 50-Gbps data rate), using the following equation [16], i.e.,

$$L_D = \frac{2\pi c_0 T_0^2}{\lambda^2 D} \quad (1)$$

where c_0 is the speed of light, λ is the wavelength, and D is the dispersion parameter. It is found that the theoretical dispersion length of our LRSPP waveguide is around 177 m at 50 Gbps, which is 16 times longer than that of the mentioned SOI waveguide (approximately 11 m). Therefore, considering its length (3.6 mm), dispersion is negligible, and the structure is considered

bandwidth unlimited. In this chapter, the bandwidth limitation is attributed to the optoelectronics used in the experimental setup.

The nonlinearity that may distort the signal originates from the nonlinear electron oscillation at the metal-dielectric interface caused by the incident photons, leading to second- and third-order nonlinear processes [39], [40]. Furthermore, in the case of LRSPP excitation, a misalignment between the incident wave and the propagating plasmonic mode leads to a reduction in coupling efficiency. These impairments were negligible in our demonstration. Considering these factors, one may draw a conclusion that the LRSPP waveguide is capable of transmitting much higher bit-rates (50 Gbps and more) per channel, as well as larger aggregated bandwidth.

3.6. Conclusion

In this chapter, the objective was to investigate the system-level performance of an LRSPP waveguide and assess its feasibility for implementation as an optical link for a short-reach WDM system. The fabricated 3.6 mm long gold stripes (thickness of 35 nm and width of 5 μm) showed an average insertion loss of 13.2 dB at 1.55 μm (measurements) with lateral MFD of 6.5 μm and vertical MFD of 5 μm. The propagation loss of 35 nm thick gold stripe can be reduced by a factor of 7 with decreasing its width down to 2 μm, and yet maintain reasonable optical mode confinement. The BER measurements and eye diagrams confirmed the effective transmission of multichannel high data rate signals with either OOK or DPSK modulation format through LRSPP waveguides embedded in Cytop. The results demonstrated that plasmonic stripe waveguides are capable of transmitting NRZ-OOK data signals at 4×49 Gbps, as well as NRZ-DPSK data signals at 4×10 Gbps. Potentially higher data rates are achievable as the dispersion length of the fabricated waveguides is estimated at 177 m for 50 Gbps data. Results suggest no degradation due to the possible dispersion, nonlinearities, and wave vector mismatch. The demonstrated aggregate bandwidth are compared with few previous works in Table 2.1.

4. Simultaneous optical and microwave data transmission

4.1. Introduction

This chapter presents a novel metal waveguide structure which can simultaneously support LRSPPs at optical frequencies and microwave signals. The design and optimization procedure of optical and electrical waveguides are explained. Then, fabrication steps for implementation of the designed structure are discussed. And finally, measurement results of the fabricated devices are presented. The author of this thesis has published the discussions presented in this chapter in the following two papers:

- B. Banan, M. S. Hai, P. Berini, and O. Liboiron-Ladouceur, "Simultaneous high-capacity optical and microwave data transmission over metal waveguides," Opt. Express 23, 14135-14147 (2015).
- B. Banan, R. Niall Tait, O. Liboiron-Ladouceur, and P. Berini, "Fabrication of metal stripe waveguides for optical and microwave data transmission," J. Vac. Sci. Technol. B 33(6) 061208 (2015).

4.2. Proposed structure

Fig. 4.1(a) and (b) show the schematic of the designed structure to propagate both optical and electrical signals over a distance of several millimeters. The proposed configuration is a coplanar waveguide (CPW) which consists of two thin ground stripes (labeled G) along with a thick signal stripe (labeled S) in the center. The LRSPPs modes propagate over the two thin ground stripes

while the electrical microwave signal propagates over the full CPW structure. At both ends of the structure three gold stripes with two 100×100 μm^2 electrical pads are implemented. In order to provide low propagation loss for the optical and microwave signal transmission, the dimensions of proposed configuration must be optimized.

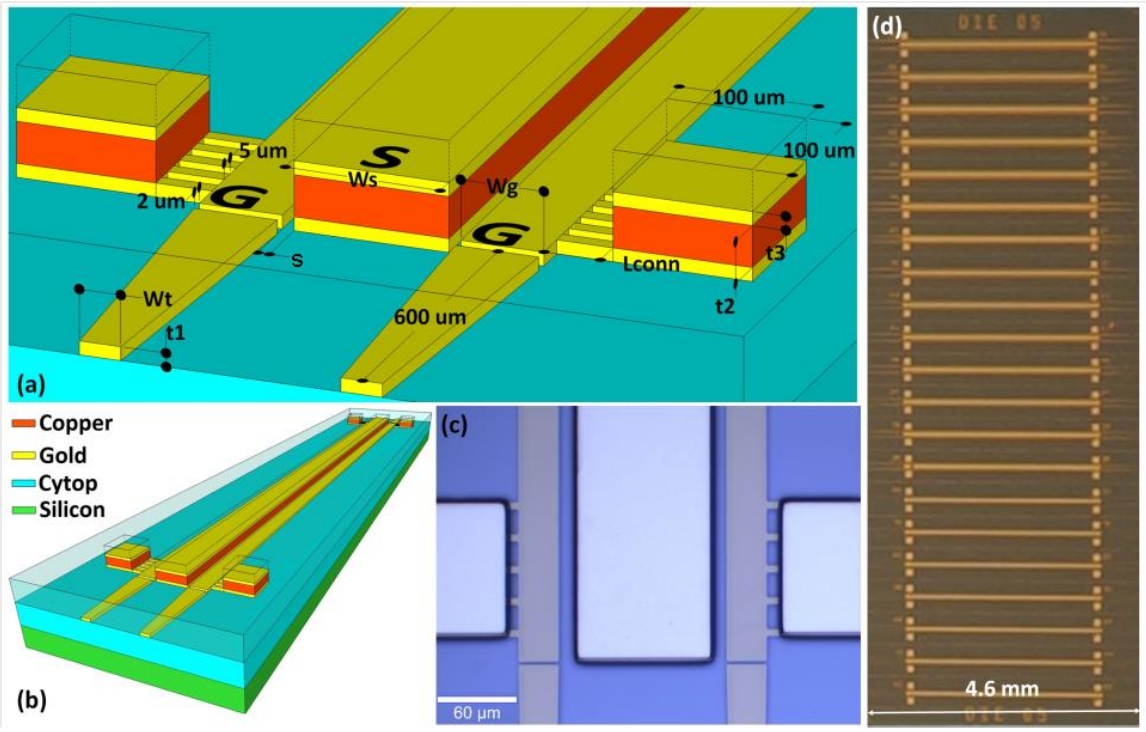


Fig. 4.1. (a) and (b): Schematic of the structure of interest, and (c) 20× magnification microscope image of one of the fabricated structures at one end. The pad area is 100×100 μm^2 with a 100 µm wide signal stripe (W_s), and two 30 µm wide ground stripes (W_g) separated by 2 µm gap from optical tapers. (d) Image of a 4.6 mm long fabricated die which includes 21 different microwave-optical transmission lines with straight optical reference waveguides in between.

4.2.1. LRSPP waveguide design and optimization

LRSPPs mode propagation over the structure is modeled with the same approach (i.e., similar software, and parameters) explained in chapter 3. To investigate the optimum structure dimensions, the thickness t_1 is varied from 20 to 35 nm, and the width W_g is varied from 2 to 30 µm in 1 µm increments. The dielectric is again Cytop, and the claddings are assumed thick enough (100 µm) to accommodate LRSPP modes.

Fig. 4.2(a) shows the computed attenuation for different widths and thicknesses. As expected, attenuation decreases with decreasing thickness and width [16]. The lowest simulated propagation loss, obtained for a 20 nm thick gold film, corresponds to 0.02 dB/mm which happens for the width of 2 μm. Fig. 4.2(b) and (c), respectively, shows the vertical and lateral mode field diameters of the LRSPP mode. The mode field diameter, in this case, is defined as the full-width electric field (E_y) spot size at the 1/e point. As shown in Fig. 4.2(b), the vertical mode field diameter becomes larger with reducing gold thickness and width, eventually reaching the field diameter of the background slab mode supported by the thick Cytop cladding in the absence of the metal stripe. The inset shows a near-field image of the electric field ($Re\{E_y\}$) distribution of the 5 μm wide and 35 nm thick gold stripe. The lateral mode field diameter (Fig. 4.2(c)), however, behaves differently. It initially gets smaller with reducing stripe width from 30 μm, but then increases with further reduction of the stripe width. This behaviour is attributed to the fact that the lateral mode field diameter is always larger than the width of the metal stripe [32]. For sufficiently wide metal, the lateral mode field diameter becomes as wide as the width of the stripe. This results in a linear-like trend for the lateral mode field diameter versus width. However, for a narrower metal stripe, the lateral field distribution becomes comparable to the field of the background slab mode (similar to the vertical mode field behaviour), resulting in an increase of the lateral field diameter.

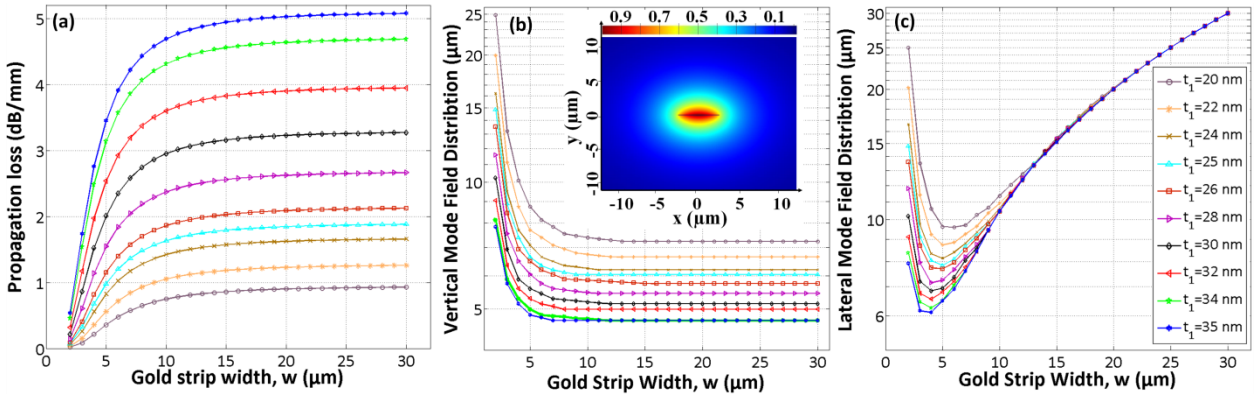


Fig. 4.2. Computed (a) propagation loss, (b) vertical and (c) lateral mode field diameter as a function of gold ground stripe width (W_g) and thickness (t_1) for a single gold stripe waveguide in a homogenous medium, The inset in (b) shows a near-field image of the electric field ($\mathrm{Re}\{E_y\}$) distribution of the 5 μm wide and 35 nm thick gold stripe.

Simultaneous optical and microwave data transmission

In the proposed structure, overlap of the optical modes propagating in the ground stripes with the middle signal stripe leads to increased optical loss which needs to be investigated. In Fig. 4.3, the optical loss of a thin stripe of two different widths (W_g = 5 and 30 μm) is computed for various thicknesses (t_1 = 20, 25, and 30 nm). The effect of the 50 μm wide (W_s), 500 nm thick (t_2) middle signal stripe is studied for various separation distances (s). In these computations, the cladding of 15 μm of Cytop and a thick silicon substrate are considered.

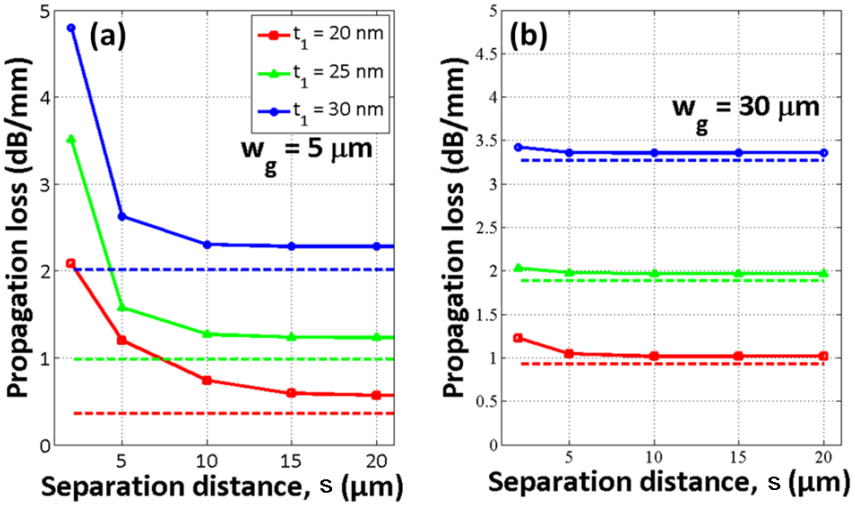


Fig. 4.3. Computed propagation loss versus separation distance (s) and thickness (t_1), for ground stripes (a) 5 μm and (b) 30 μm wide (W_g). The signal stripe width (W_s) and thickness (t_2 are 50 μm and 500 nm, respectively. Cytop thickness is assumed to be 15 μm on a thick silicon substrate. Dashed lines show propagation loss when Cytop thickness is 100 μm.

As illustrated in Fig. 4.3, in the presence of signal stripe, the smaller the separation distance (s < 10 μm), the higher the attenuation. Also, comparing Fig. 4.3(a) and (b) shows that the loss increase at smaller gap sizes is more significant for 5 μm wide ground stripes (W_g) compared to 30 μm stripes which is attributed to high mode overlap with signal stripe. The dashed lines show attenuation of their respective stripe embedded in a thick homogenous Cytop cladding (100 μm) in presence of signal stripe. The difference between dashed and solid lines shows the effect of 15 μm thick Cytop and silicon substrate on optical loss.

According to this computation, at smaller separation distances (*s*), the lower the width and thickness of the metal ground stripes (W_g, t_1), the higher the effect of the signal stripe on the

propagation loss. The result suggests that in case of separation distances lower than 10 µm, wide ground stripes (optical waveguides) are preferable in order to avoid additional optical loss.

4.3. Microwave performance optimization

4.3.1. Characteristic impedance calculation based on conformal mapping

For the investigation of the electrical microwave propagation, this section considers an analytical solution to finite-ground coplanar waveguides (FGCPW) based on the conformal mapping. Fig. 4.4. depicts the schematic cross section of the structure. The structure consists of three metal stripes of thicknesses t_1 and t_2, widths W_g and W_s, respectively. A distance s separates the metal stripes. Metals with permittivities of ε_1 for the ground and ε_2 for the signal stripes surrounded by a finite homogenous dielectric of thickness t_3 and permittivity $\varepsilon_3$sitting on a dielectric of thickness t_4 with permittivity ε_4.

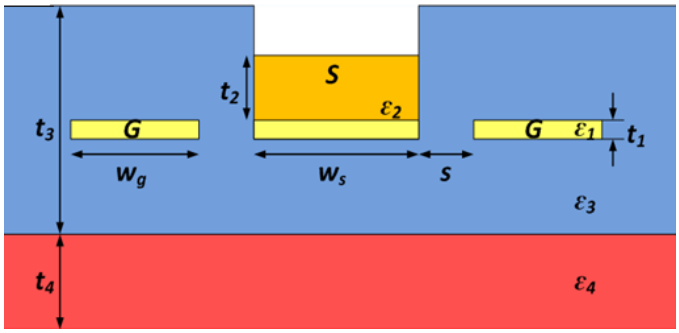


Fig. 4.4 Schematic cross-section of the proposed structure excluding the ground pads with connections as well as optical tapers.

Assuming that the propagation mode in the FGCPW is quasi-static (i.e., a pure TEM mode: the field lines exist within a homogeneous medium), a conformal mapping technique is employed to characterize the FGCPW and derive the analytical expressions of the line capacitance per unit length [41, 42]. Indeed, conformal mapping transforms the geometry of the CPW into a parallel plate capacitor whose capacitance is a linear function of dielectric constant. In this analysis, the

metal structure is considered to be a perfect electrical conductor (PEC, $\varepsilon_1 = \varepsilon_2 = \infty$) embedded in Cytop polymer with a dielectric constant of $\varepsilon_3 = 2$ which is spin coated on a silicon wafer with a dielectric constant of $\varepsilon_4 = 11.7$. Once the total line capacitance of the FGCPW is obtained, the characteristic impedance Z_c can also be determined by

$$Z_c = \frac{1}{C_{tot}\, v_p} \tag{1}$$

where, v_p is the phase velocity given by $v_p = \frac{c}{\sqrt{\varepsilon_{eff}}}$. Here, c is the speed of light, and ε_{eff} is the effective dielectric constant which is given by

$$\varepsilon_{eff} = \frac{C_{tot}\,(\varepsilon_r)}{C_{tot}\,(\varepsilon_r=1)} \tag{2}$$

where, ε_r denotes the relative dielectric constant of the medium between the parallel plates of the capacitor.

Considering that the dielectric-air boundaries (magnetic walls) are along the electric field lines, C_{tot} can be expressed as the sum of all partial capacitances without affecting the field [41, 42, and 43]. Therefore,

$$C_{tot} = C_0 + C_1 + C_2 + C_3 \tag{3}$$

where C_0 represents the air capacitance in the absence of any dielectric, and C_1 is the capacitance of the top cladding (Cytop polymer [30]) with the thickness of $h_1 = t_3/2$ and the equivalent dielectric constant of $(\varepsilon_3 - 1)$ which is the difference between the cladding and the air relative dielectric constants. Similarly, C_2 expresses the capacitance of the bottom cladding layer (Cytop polymer) that is beneath the signal and ground traces with the thickness of $h_2 = t_3/2$ and the equivalent dielectric constant of $(\varepsilon_3 - \varepsilon_4)$. Finally, C_3 denotes the capacitance of the bottom substrate (silicon) layer with the thickness of $h_3 = t_4$ and the equivalent dielectric constant of $(\varepsilon_4 - 1)$ [41 and 42].

The conformal mapping tailors the separation into two parallel plates using complete elliptical integral of the first kind, $K(k)$ [41]. In this sense, the partial capacities can be given by

$$C_0 = 4\varepsilon_0 \frac{K(k'_0)}{K(k_0)} \tag{4}$$

$$C_1 = 2\varepsilon_0(\varepsilon_3 - 1)\frac{K(k'_1)}{K(k_1)} \tag{5}$$

$$C_2 = 2\varepsilon_0(\varepsilon_3 - \varepsilon_4)\frac{K(k'_2)}{K(k_2)} \tag{6}$$

$$C_3 = 2\varepsilon_0(\varepsilon_4 - 1)\frac{K(k'_3)}{K(k_3)} \tag{7}$$

where,

$$k_0 = \frac{x_3}{x_2}\sqrt{\frac{x_2^2 - x_1^2}{x_3^2 - x_1^2}}, \quad k'_0 = \sqrt{1 - k_0^2} \tag{8}$$

$$x_1 = \frac{W_s}{2}, \qquad x_2 = x_1 + s, \; x_3 = x_2 + W_g$$

Furthermore, for the rest of the complete elliptical integrals of the first kind, the modulus k_i can be obtained by

$$k_i = \frac{\sinh\left(\frac{\pi x_3}{2h_i}\right)}{sinh\left(\frac{\pi x_2}{2h_i}\right)}\sqrt{\frac{sinh^2\left(\frac{\pi x_2}{2h_i}\right) - sinh^2\left(\frac{\pi x_1}{2h_i}\right)}{sinh^2\left(\frac{\pi x_3}{2h_i}\right) - sinh^2\left(\frac{\pi x_1}{2h_i}\right)}} \tag{9}$$

$$k'_i = \sqrt{1 - k_i^2} \;\; , \;\; i = 1, 2, and\ 3$$

Thus, C_{tot} can finally be expressed as

$$C_{tot} = 4\varepsilon_0\frac{K(k'_0)}{K(k_0)} + 2\varepsilon_0(\varepsilon_3 - 1)\frac{K(k'_1)}{K(k_1)} + 2\varepsilon_0(\varepsilon_3 - \varepsilon_4)\frac{K(k'_2)}{K(k_2)} + 2\varepsilon_0(\varepsilon_4 - 1)\frac{K(k'_3)}{K(k_3)} \tag{10}$$

Once the transmission line capacitance per unit length (C_{tot}) is determined, the effective dielectric constant (ε_{eff}), can also be obtained using the following expression

$$\varepsilon_{eff} = 1 + Q_1(\varepsilon_3 - 1) + Q_2(\varepsilon_3 - \varepsilon_4) \tag{11}$$

where, $Q_1$and Q_2 can be obtained by

$$Q_1 = \frac{1}{2}\frac{K(k_0)}{K(k'_0)}\left(\frac{K(k'_3)}{K(k_3)} + \frac{K(k'_1)}{K(k_1)}\right) \tag{12}$$

$$Q_2 = \frac{1}{2}\frac{K(k_0)}{K(k'_0)}\frac{K(k'_2)}{K(k_2)}$$

Finally, the characteristic impedance of the FGCPW can be determined by

$$Z_C = \frac{30\pi}{\sqrt{\varepsilon_{eff}}}\frac{K(k_0)}{K(k'_0)} \tag{13}$$

Based on the above analysis, the impact of the separation distance, signal and ground traces width on the FGCPW line characteristic impedance, Z_C, is investigated. As illustrated, Fig. 4.5(a)

shows that an increase in the signal stripe width W_s decreases the characteristic impedance. Additionally, decreasing the separation distance reduces the characteristic impedance. Furthermore, in Fig. 4.5(b), at 40 GHz frequency for a fixed gap size of 15 µm, increasing the ground stripes width decreases the impedance. This decrease is more significant for lower frequencies (not shown here).

To characterize the proposed waveguide structure with data transmission using high-speed test and measurement equipment, a transmission line impedance of 50 Ω is set as a design requirement. In such context, as shown in Fig. 4.5(b), the optimal signal stripe dimension for a 50 Ω FGCPW line is W_s = 50 µm. Additionally, according to Fig. 4.5(a), the requirement of 50 Ω transmission line for the signal stripe width of 50 µm is met if the optimal values for the two other parameters W_g and s would be 30 µm and 15 µm, respectively. Thus, these dimensions are considered for the fabrication of the structure, and the calculation results are compared with measured values in chapter 5 in which they are in good agreements

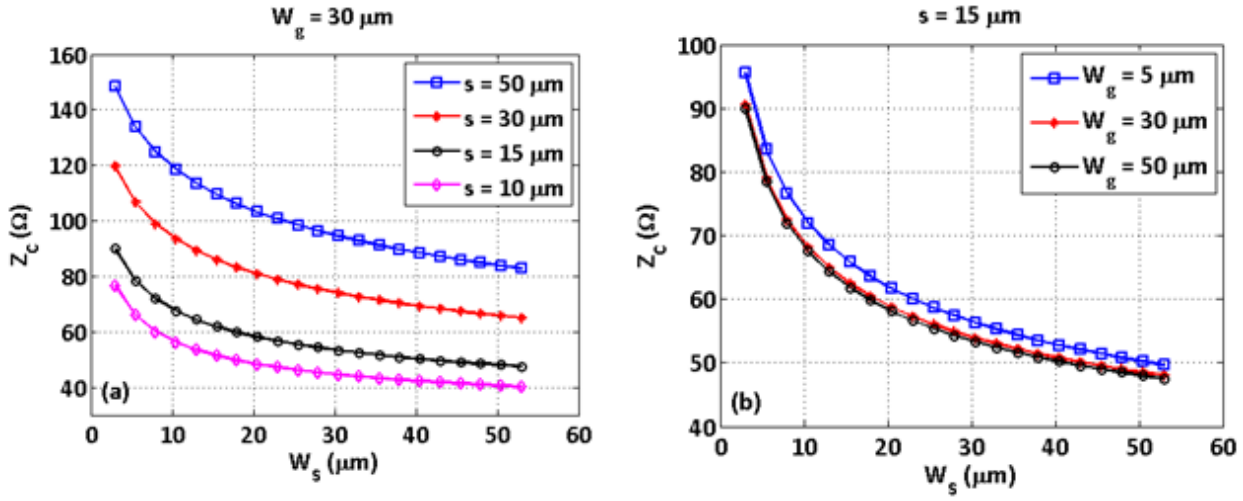


Fig. 4.5. Calculated characteristic impedance of the FGCPW at 40 GHz as a function of signal stripe width (W_s) for (b) s = 15 µm and different ground stripe widths, and (a) W_g = 30 µm and different gap sizes.

The analytical formulation described in this section provided a good estimation of the impedance of the structure. In the next section, a full 3D EM solver is used in order to provide more insight on the microwave performance of the structure.

4.3.2. Microwave performance analysis using HFSS software

In the calculation presented in the previous section, metals were considered as a PEC. However, in reality metals do not possess infinite conductivity and permittivity. In this section, the simulation was carried out using ANSYS HFSS software to more accurately assess the microwave performance of the structure using actual physical parameters of metals. A 3D full-wave frequency domain electromagnetic field solver based on the finite element method (FEM) simulates the electrical behavior of the structure. In computations, first, the optimum dimensions of the structures cross section are found, for which the characteristic impedance (Z_c) is close to 50 Ω. Then, the S-parameters of the structure is extracted by de-embedding the cross-section for different lengths and termination with 50 Ω load representing the measurement equipment ports. In these computations, the electrical properties of bulk copper, gold, and silicon are used from the software library. For the Cytop claddings, the relative dielectric constant used is 2 with a dielectric loss tangent of 0.0003 [30]. Fig. 4.6 gives results for the characteristic impedance of the structure as a function of frequency for different geometries.

As shown in Fig. 4.6, the characteristic impedance decreases with increasing frequency. Importantly for microwave transmission, the characteristic impedance decreases and approaches 50 Ω by decreasing the separation distance (s) from 15 to 5 μm and by increasing the ground stripe width (W_g) from 5 to 30 μm. Moreover, comparing Fig. 4.6(a)–(c) to Fig. 4.6(d)–(f) shows that the wider the signal stripe-width the lower the impedance becomes. Furthermore, the S-parameters were computed as shown in Fig. 4.7 for different parameters. The structures have a 50 μm wide signal stripe and 30 μm wide ground stripes. As illustrated, the wider the gap between the stripes, the higher the electrical transmission (lower loss). Also, it can be seen that the performance of the structure in terms of loss and bandwidth decreases by increasing the length. Based on the computational results, the available fabrication capabilities, and the available measurement equipment, structures were designed to enable simultaneous optical and electrical transmission. In the fabricated structures, the middle stripe (electrical signal line) consists of a 1 μm thick copper (t_2) film sandwiched between a 25 nm thick gold (t_1) layer at the bottom and a 10 nm gold (t_3) layer on top. The top gold layer serves as a protective layer to passivate the copper in order to prevent surface oxidization and degradation of copper conductivity. In the signal stripe, mainly

copper is used instead of gold to reduce fabrication costs. The side stripes (electrical ground lines) are thin gold films (25 nm thick) supporting LRSPP modes at optical frequencies.

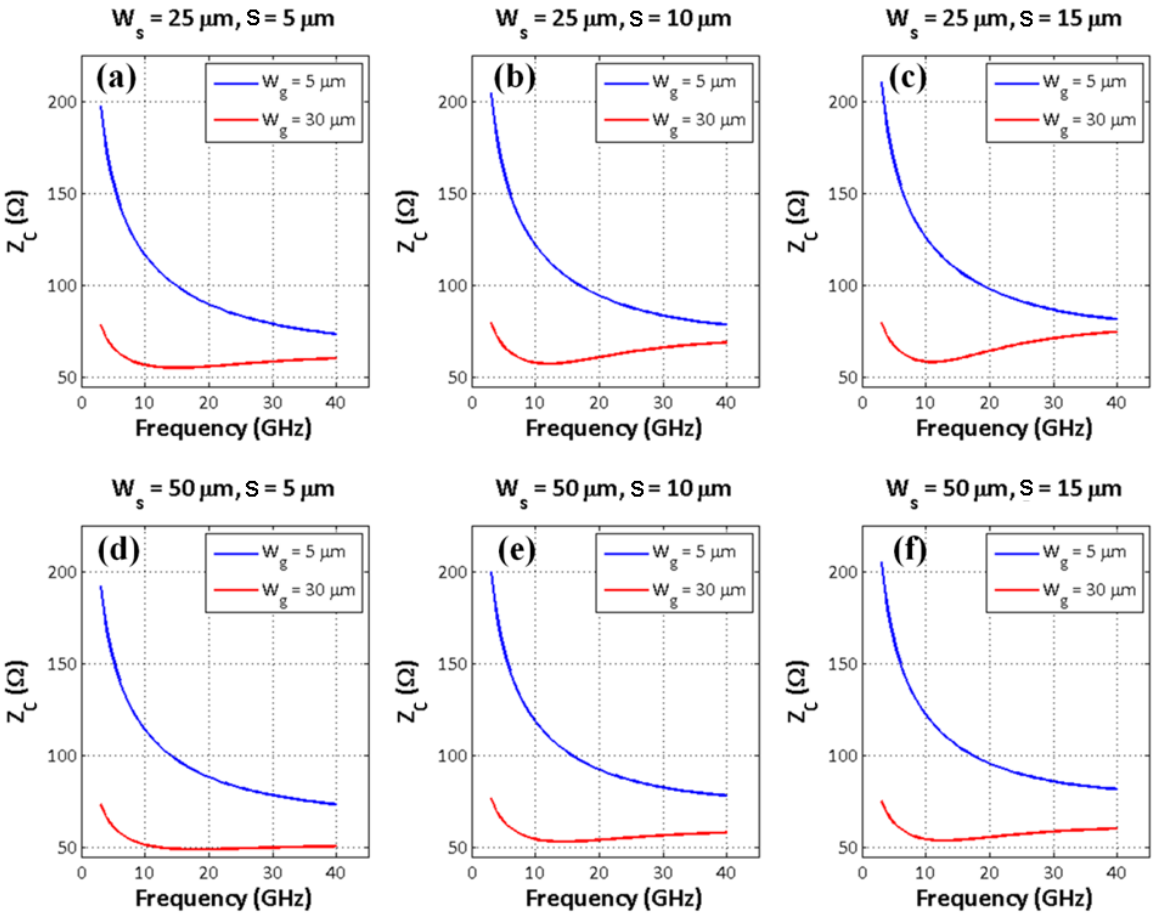


Fig. 4.6. (a)-(f) Computed electrical characteristic impedance Z_c of the proposed structure as a function of frequency for different ground (W_g) and signal (W_s) stripe widths, and separation (s).

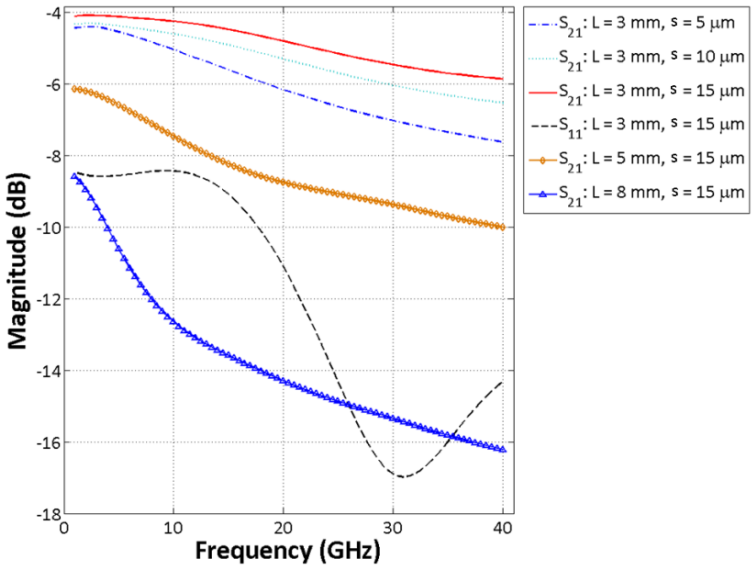


Fig. 4.7. Computed electrical response of structures comprised of a 50µm wide signal stripe and 30 µm wide ground stripes for different separation sizes (*s*) and lengths.

The microwave mode is excited from the top via RF electrical probes configured as ground-signal-ground (GSG) with a pitch of 150 µm. The LRSPP mode is excited via an end-coupled optical single-mode optical fiber. To maximize the coupling efficiency between the structure and the standard single mode fiber, on-chip linear tapers are designed from 8 µm (W_t) to the width of the ground stripes over a length of 600 µm (see Fig. 4.1(a) and Fig. 4.8). Also, 200 µm long straight segments (not shown in Fig. 4.1) are added to the end of the taper input to compensate for possible dicing inaccuracies. A small gap of 2 µm is inserted between the taper and the ground stripe waveguides for electrical isolation. The total optical path is approximately 1.6 mm longer than that of the electrical transmission line because of the tapers and gaps. The width of the middle stripe waveguide (W_s) is set to 50 µm, and the side stripe waveguides have width (W_g) of 30 µm. The separation distance (*s*) is 15 µm. The electrical contact pads are 100 µm by 100 µm in the area. The connections between the electrical pads to the electrical ground lines consist of five thin gold (25 nm thick) stripes that are 5 µm wide and of length (L_{conn}) of 10 µm.

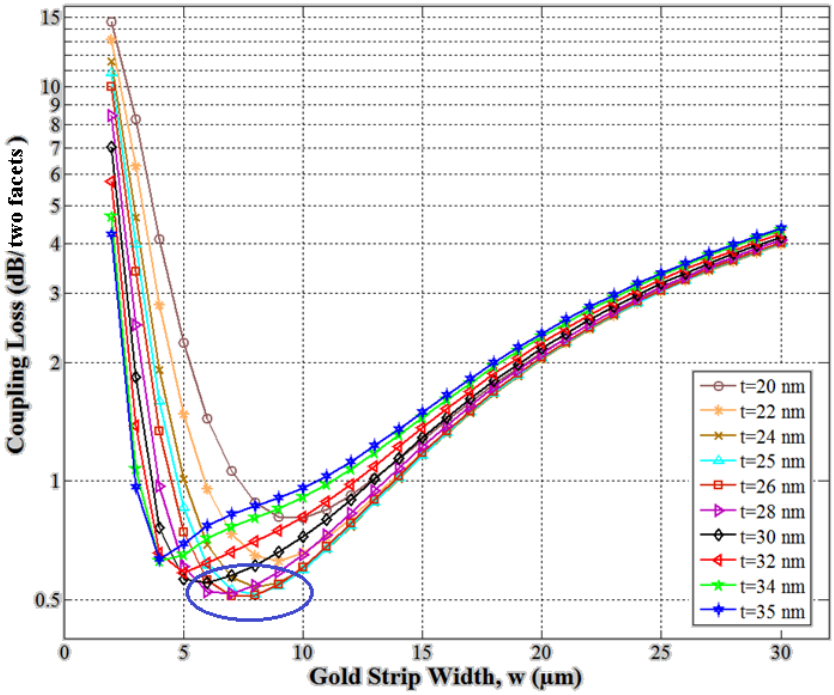


Fig. 4.8. Computed coupling loss per two facets as a function of gold ground stripe width (W_g) and thickness (t_1) for a single gold stripe waveguide in a homogenous medium.

4.4. Fabrication process for the FGCPW

4.4.1. Bottom cladding and first metal layer deposition

Fig. 4.9 shows the schematic of the fabrication process flow. Silicon wafer preparation, bottom cladding spin coating, and first metal layer patterning were performed similarly to the fabrication steps described in [36, 44] with some minor modifications. These steps are summarized as follows: five 4" silicon wafers were cleaned by dipping them in 10% hydrofluoric (HF) acid for 1 minute to remove all native oxide. Then, wafers were subjected to O_2 plasma using the Plasma Preen II-862 for 10 minutes (in 5-minute intervals) in order to remove any organic compound from the surface (Fig. 4.9(a)). Afterwards, the thick (roughly 9 μm) bottom Cytop cladding was spin coated in five steps. First, diluted M-grade Cytop was spun (~0.4 μm) in order to increase the adhesion, then three layers of S-grade were spun (~2.3 μm each). This was followed by spinning a diluted S-grade layer again (~0.8 μm) for planarization purposes. It should be mentioned that after

spinning each layer, a soft bake was performed at 50°C for 30 minutes to partially evaporate the solvent. After spinning all layers, a final hard bake was carried out at 220 °C (from 50 °C with ramp of 150 °C/hr) for more than 12 hours (Fig. 4.9(b)).

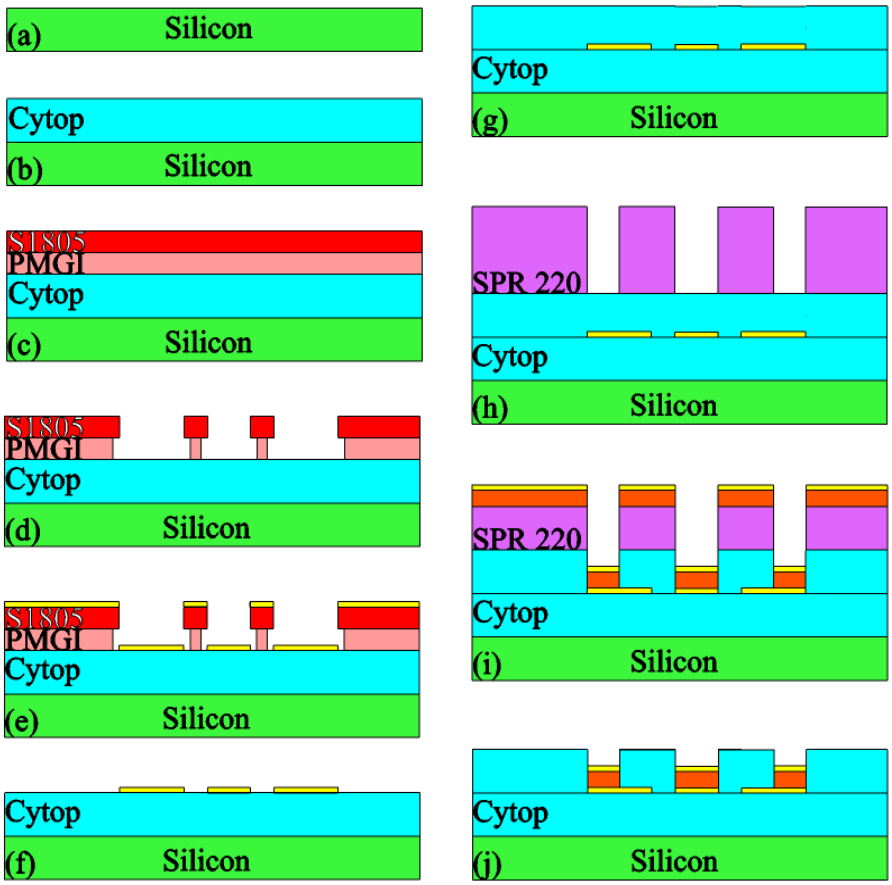


Fig. 4.9. Schematic of the fabrication process flow. (a) Cleaning of a silicon wafer (10% HF and O_2 plasma), (b) sequential spin coating of Cytop bottom cladding, (c) surface preparation followed by PMGI and S1805 spin coating, (d) UV patterning and developing, (e) gold deposition via thermal evaporation, (f) lift-off, cleaning, and dehydration, (g) Cytop top cladding spin coating with slow thermal treatment, (h) surface preparation, SPR 220 spin coating, patterning, and developing, (i) etching followed by copper and gold deposition, and (j) lift-off and cleaning.

Then, the first metal layer (25 nm gold) is patterned via a bi-layer photolithography technique using Polymethylglutarimide (PMGI) and S1805 photoresists. Before spinning the PMGI, the Cytop was subjected to O_2 plasma using a reactive ion etcher (RIE, March Jupiter II) for 30 seconds (so-called ashing) and coated with hexamethyldisilazane (HMDS) to improve the Cytop-PMGI adhesion. After the surface preparation, 105 nm of PMGI was spin coated and baked at 180 °C for

3 minutes, followed by 500 nm of S1805 spin coated and baked at 115 °C (Fig. 4.9(c)). Then, the first metal layer was patterned using an MA6 Karl SUSS mask aligner (the exposure time depends on the ultraviolet (UV) lamp intensity). Afterward, patterns were developed using an MF321 solution (Fig. 4.9(d)). The 25-nm thick gold layer was thermally deposited using a Balzers BA510 at a pressure of 2.6×10^{-7} Torr with a 0.9 Å/s deposition rate (Fig. 4.9(e)). The lift-off was performed in two baths of Microposit™ remover 1165 at 80 °C for 10 minutes followed by 10 seconds of agitation in an ultrasonic bath. Then, the wafers were placed in isopropyl alcohol (IPA) for another 10 minutes, followed by 10 minutes in a de-ionized water bath, and then dehydration at 95 °C for 15 minutes (Fig. 4.9(f)).

4.4.2. Top cladding and signal stripe formation

1. Top cladding formation

Cytop remains susceptible to its solvent when a layer of Cytop is spin coated on a hard-baked Cytop. The solvent diffuses into the latter [36]. This must be managed when forming the top cladding because the thermal treatment also evaporates the solvent diffused into the bottom cladding, which can stress the thin metal layers deposited thereon. If the amount of diffused solvent is considerable and the thermal process is not slow enough, this results in a deformation of the patterned metal layers [44]. If the metal layer consists of large-area features, it makes the structure even more vulnerable. So, careful thermal processing is required.

To reduce metal deformation, the amount of solvent diffusing into the bottom cladding should be reduced. Which is done by spinning the top cladding into five layers (~1.4 µm thick each). Then, each layer is soft-baked at 50 °C for 30 minutes and hard-baked at 90 °C for at least 12 hours (Fig. 4.9(g)). The hard bake should be performed at a temperature below the Cytop glass transition temperature (107°C) to avoid any waveguide deformation due to reflow of the bottom cladding. Fig. 4.10 shows the effect of different thermal processing on the device. Images are taken under polarized light to enhance the contrast in deformed regions.

As Fig. 4.10(a) illustrates, if the Cytop is hard-baked at 90 °C without a thermal ramp, bulging of the metal layer is observed due to rapid evaporation of the diffused solvent. This defect is most noticeable around the edges of the features and results in shadowed regions in the optical microscope images. To minimize the metal deformation, the thermal ramp should be as slow as

possible. Fig. 4.10(b) shows a hard-baked structure when the thermal ramp was set to 10 °C/hr. As shown, the deformation is significantly reduced, but there is still some rounding near edges and corners due to solvent evaporation. For a reduced thermal ramp of 5 °C/hr, there is no observable deformation as shown in Fig. 4.10(c).

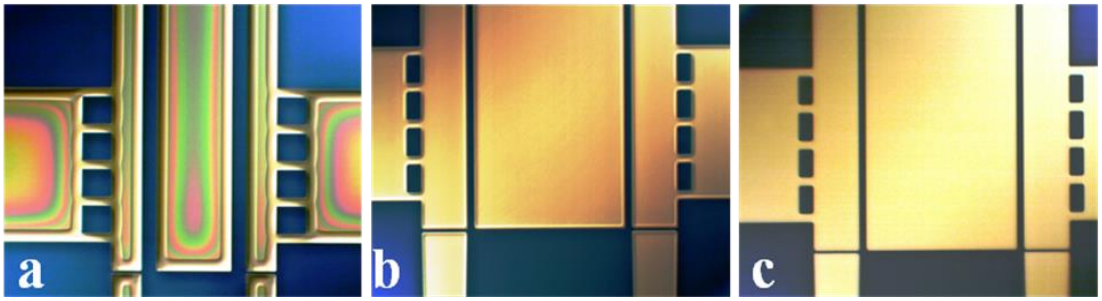


Fig. 4.10. The effect of top cladding thermal processing on the first metal layer of the device (50× magnification) where Cytop is hard-baked at 90 °C: (a) without a thermal ramp, (b) with a 10 °C/hr thermal ramp, and (c) with a 5 °C/hr thermal ramp.

2. Second metal layer deposition

After top cladding formation, the second and third metal layers of the signal stripe and contact pads must be patterned. In this step, a thick layer of SPR 220 (10 µm) was spun as the photoresist. To improve the adhesion between the resist and the top cladding, the wafers were exposed to O_2 plasma for 5 seconds and then covered with HMDS. After SPR 220 spin coating and thermal curing (30 s at 35 °C and 90 s at 115 °C), the wafers were exposed and developed in MF-24A solution (Fig. 4.9(h)). Then, the patterns were etched using a March Jupiter II RIE at 200 W for about 10 minutes. Inspections with a profilometer were performed to ensure that the first metal layer was clear. Then, wafers were placed into a Balzers BA510 to deposit 1 µm of copper at a pressure of 2.7×10-7 Torr with a 5 Å/s deposition rate, followed by 10 nm of gold at a 1 Å/s rate (Fig. 4.9(i)). Afterward, lift-off was performed in Acetone (of what remained of the etch mask - also used as the lift-off mask), and the wafers were cleaned in IPA and DI water baths (Fig. 4.9(j)). Finally, the wafers were sent out for dicing.

4.4.3. Microscopy and AFM

Fig. 4.11(a)-(c) show microscope images of a fabricated structure under 20× and 40× optical magnifications. As illustrated, the fabricated device does not have any observable imperfections. Fig. 4.11(d) gives a cross-sectional image of a device, confirming the acceptable quality of the end facets along with the thickness of the Cytop cladding layers (~14.5 µm).

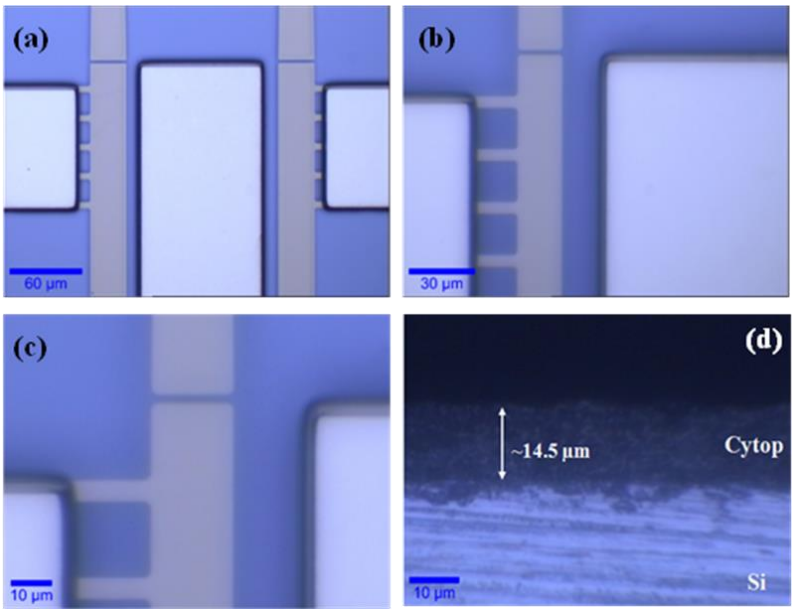


Fig. 4.11. (a) 20×, (b) 40×, and (c) 40× with digital zoom-in microscope images of a fabricated structure near one end of a device comprising two optical tapers, two pads 100×100 µm^2 in area, a 50 µm wide signal stripe, and 30 µm wide ground stripes separated by 2 µm long gaps from the optical tapers. (d) Microscope image of a device cross-section with 40× magnification and digital zoom-in.

Fig. 4.12(a) shows AFM measurements of the etch profile from top cladding down to passivation gold layer. As illustrated, the etch depth is approximately 6 µm which is in line with expectation considering five layers of ~1.4 µm thick top cladding and 1 µm of copper. Also, the measured roughness of the signal line (Fig. 4.12(b)) is 7.34 nm rms (5.34 nm average) which are acceptable considering the deposition rate of the copper and the over-etching required to expose the first metal layer.

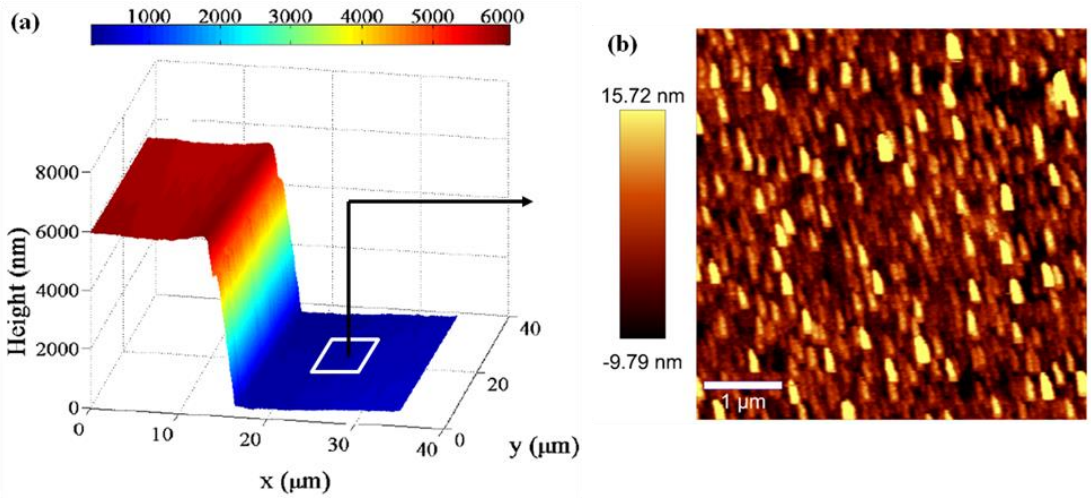


Fig. 4.12. AFM measurement of a final structure indicating (a) the etch profile and (b) surface roughness of a 5×5 μm^2 area of a signal line.

4.5. Measurements

4.5.1. Optical insertion loss measurement

Optical transmission measurements were obtained at a wavelength of 1550 nm, although longer wavelengths (up to 1675 nm) compatible with communication bands can propagate with lower propagation losses. Fig. 4.13(b) depicts the measured optical insertion loss at 1550 nm for two different waveguide widths (8 μm straight as a reference and 30 μm with two tapers) at three different lengths. According to our computations (Fig. 4.8), a gold metal stripe of 8 μm width and 25 nm thickness has the highest coupling efficiency to a standard single mode fiber (94%). Hence, an 8 μm wide straight waveguide was used as a reference sample. The inset shows the far-field LRSPP mode measured using an infrared camera. The background light is attributed primarily to uncoupled input light leaking through the polymer cladding surrounding the metallic waveguide. The slope of the curve is the attenuation and the intercept with the vertical axis is the input coupling loss. Thus, the measured attenuation for the 8 μm long straight waveguide is 1.71 dB/mm with a coupling loss of 2.42 dB/facet. Computations predict an attenuation of 1.48 dB/mm and 0.25 dB of coupling loss per facet. Also, the measured attenuation for a 30 μm wide stripe waveguide is 1.88 dB/mm with a coupling loss of 3.9 dB/facet, compared to computations of approximately 2 dB/mm of attenuation (see Fig. 4.3(b), t_1 of 25 nm and s of 15 μm), and a coupling loss of

0.25 dB/facet. Therefore, for 30 µm wide stripes the expected total insertion loss for a length of 4.6 mm (3 mm waveguide with 1.6 mm tapers) is 9.25 dB. The difference between the measured values (12.6 dB, Fig. 4.13(b), first red data point) and modeling is attributed to the reason listed below, as well as fabrication and measurement errors. In the modeling, only the metal absorption based on the bulk properties of gold is considered as the sole source of loss. However, metal and edge roughness, as well as radiation losses in the tapers may contribute to the total insertion loss. The difference between predicted coupling loss and measured values is due to reflections from fiber/air and air/chip interfaces, and also to the non-ideal optical facets. Also, it must be mentioned that the effect of the contact pads were not considered in the optical modeling; based on the computations shown in Fig. 4.3(b), when a 30 µm wide and 25 nm thick LRSPP waveguide is at a 10 µm distance from a thick metal structure (signal stripe or contact pads), the excess loss on the LRSPP is negligible (~ 0.1 dB). Additionally, comparison between measured coupling losses in straight waveguides and tapered waveguides suggests that the designed tapers at the input and output are not perfectly adiabatic. Also, in the measurement setup, background radiation from uncoupled input light to the LRSPP cannot be completely eliminated.

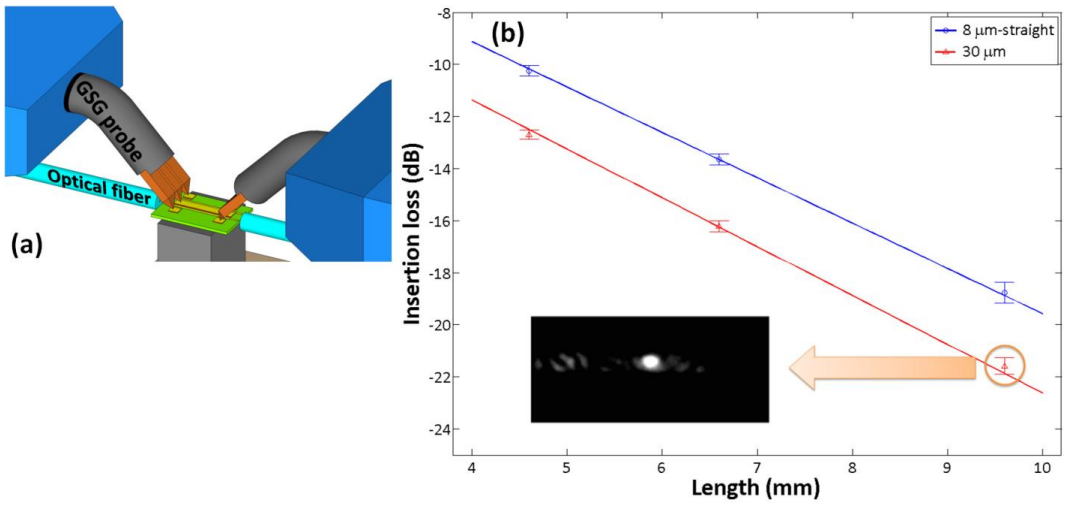


Fig. 4.13. (a) Illustration of the experimental set-up for the simultaneous excitation of LRSPP and microwave modes. (b) Measured insertion loss versus waveguide length for 8 and 30 µm wide, 25 nm thick gold stripe waveguides. The inset shows a far-field image of the LRSPP mode output.

4.5.2. Electrical S-parameters measurement

A 40 GHz vector network analyzer (VNA) was used to excite the fabricated CPW by providing an electrical input power of 10 dBm then the VNA captured the quasi-TEM mode propagating along the fabricated CPW. The waveguide was excited using electrical probes with a GSG configuration. The characterized waveguide was 3 mm long, comprised of a 50 µm wide signal stripe with 30 µm wide ground stripes and a separation of 15 µm. The overall width of the structure matches the 150 µm pitch of the ground-signal-ground (GSG) probes. Fig. 4.14(a) shows electrical transmission and reflection (S_{21} and S_{11}) of the structure. The drop in transmission at frequencies below 10 GHz is thoroughly discussed in the next chapter. Accounting for the drop at low frequency, the 3-dB bandwidth of the structure is beyond 40 GHz. Also, the reflection response (S_{11}) exhibits a similar trend and is in general agreement with modelling (Fig. 4.7). In Fig. 4.14(b), the measured electrical transmission (S_{21}) for waveguides of different lengths is given. The 3-dB bandwidth logically decreases to approximately 28 and 20 GHz as the length of the structure increases to 5 and 8 mm, respectively.

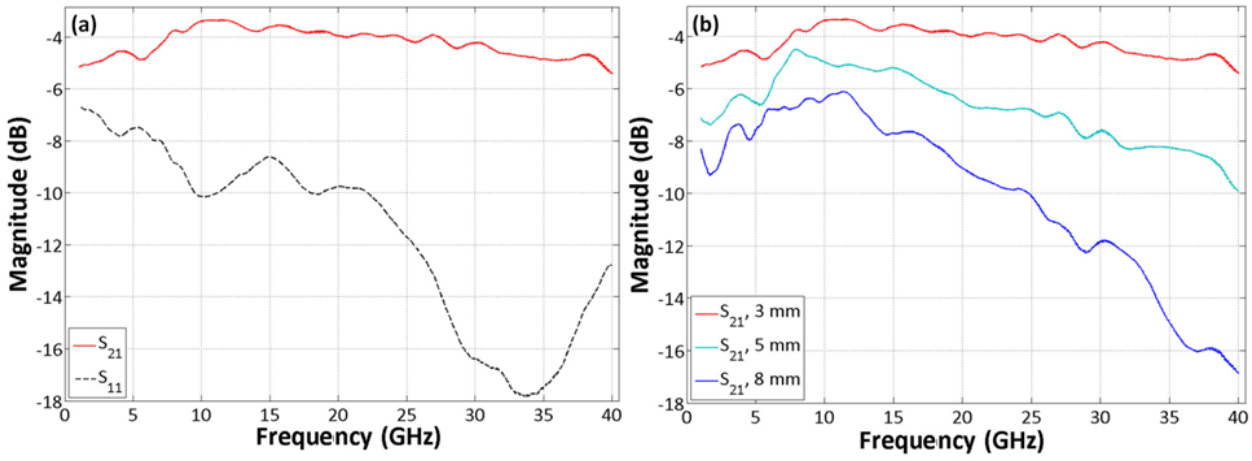


Fig. 4.14. (a) S-parameter magnitude for a 3 mm long waveguide, and (b) S_{21} for different lengths.

4.5.3. Optical and electrical modulated data transmission

Simultaneous optical and electrical digital signal transmit through the proposed structure without interference between the two signals for 3 mm length. Fig. 4.15 shows BER measurements of 40 Gbps optical and 12 Gbps electrical for simultaneous and independent propagation. The experimental setup limits the transmission bit rate. As observed, the electrical signal does not interfere with the optical signal, as confirmed by measuring the BER of the optical signal in the presence and absence of the electrical signal (simultaneous and independent transmissions); the simultaneous and independent transmissions overlap perfectly. The inset shows the transmitted optical eye at 40 Gbps when the electrical data is present at 12 Gbps. Also, 12 Gbps electrical data transmits with low BER ($< 10^{-9}$) in the presence of 40 Gbps optical signals and that no interference between the two co-propagating signals is noted. The inset shows the electrical eye in the presence of optical data. The solid lines in Fig. 4.15 are exponential fit curves to measured values. The sensitivity of the BER tester in the experimental setup is 10 mV_{pp} (roughly -36 dBm).

These results confirm the possibility of transmitting optical and microwave signals simultaneously on the same structure. Based on the measured RF bandwidth for a 3 mm long structure (Fig. 4.14(a)), it is fair to assume that transmission of a 50 Gbps electrical data rate is possible. In the case of the optical channels, the speed of the optoelectronics at each end of the link limits the bit rate. Assuming also a data rate of 50 Gbps per optical channel, the aggregate bandwidth would be 150 Gbps because there are two optical (LRSPP) channels (one on each ground stripe, 100 Gbps) and one microwave channel over the CPW (50 Gbps). Now, considering that the lateral footprint of the tested structure, excluding the contact pads and any area required to fit the optical and electrical components, is 140 μm, yields a bandwidth density of approximately 1 Gbps/μm. This density compares favorably to recent advances in electronic transmission line designs [45, 46] where full-swing RC lines produce a bandwidth density of the same order (1 Gbps/μm).

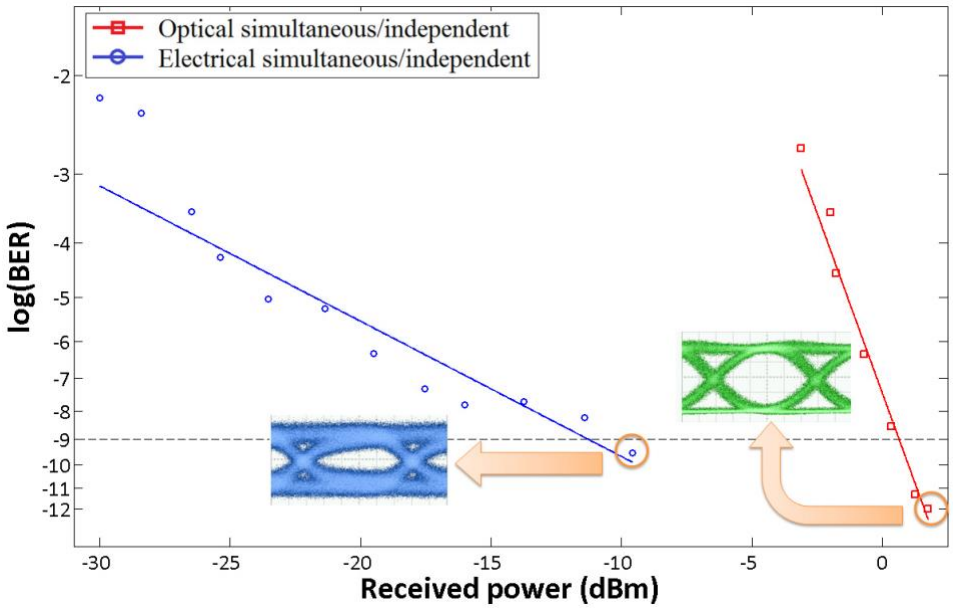


Fig. 4.15. BER measurements of simultaneous and independent 40 Gbps optical and 12 Gbps electrical signals. The insets show captured eye diagrams. The solid lines are exponential fit curves to measured values.

In the fabricated structure, the width of the signal stripe was chosen to minimize the reflection of a line terminated with 50 Ω load (experimental setup). However, this limitation results in a large width of the signal stripe (50 µm), thus a wide footprint and a lower bandwidth density. Computations show by relaxing this restriction; a narrow signal stripe can be used. Fig. 4.16 shows results for an identical 3 mm long line as the tested structure except with 1 µm wide signal stripe and gap size (*s*) of 4 µm. As illustrated, significant reflection and poor transmission occur for the proposed structure terminated with 50 Ω loads (Fig. 4.16(b)), as opposed to the case when ports are terminated with 90 Ω loads as shown in Fig. 4.16(c).

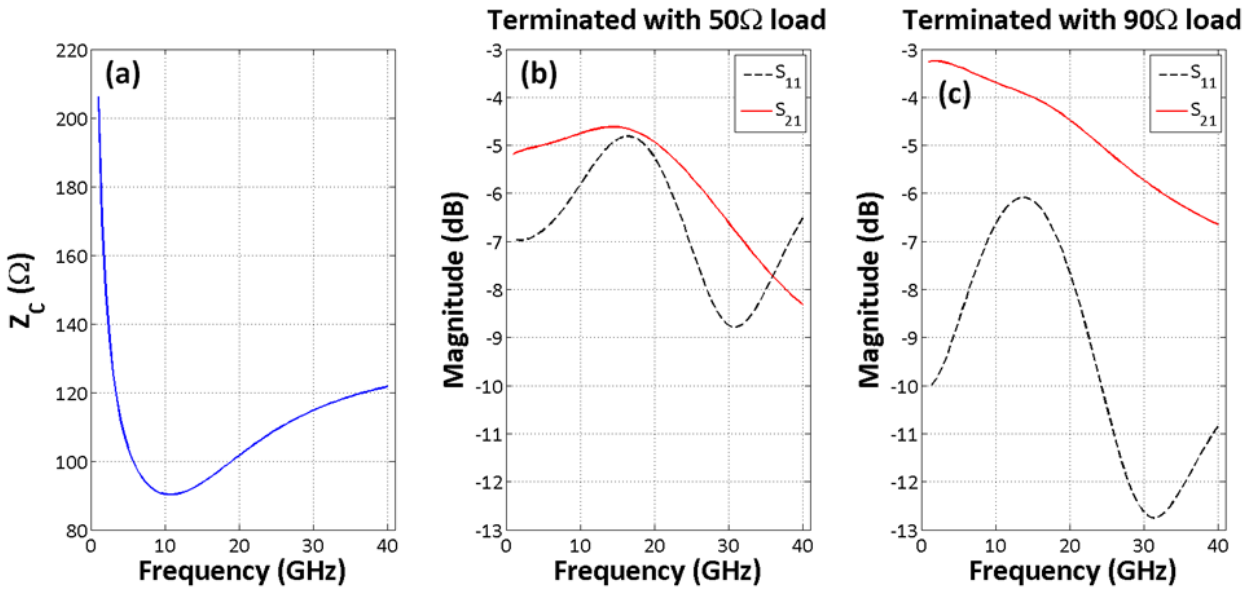


Fig. 4.16 Computed (a) characteristic impedance and S-parameters when terminated with a (b) 50Ω load, and (c) 90Ω load for a structure comprised of a 1 µm wide signal stripe (W_s), a 30 µm wide ground stripe (W_g), and a gap of 4 µm (s).

Electrical interconnects become difficult to design as data rates begin to exceed about 10 Gbps, due to frequency dependent losses, crosstalk, and frequency resonance effects [47]. The proposed structure in this work is capable of transmitting electrical signals up to data rates for which more complex design, signaling and equalization approaches are not required. By co-propagating optical and electrical signals, the aggregate bandwidth further increases. Moreover, the bandwidth density of the proposed solution can be improved significantly in two ways. Firstly, based on computations, the lateral size of the structure can be reduced to a few tens of microns if the requirement for impedance matching is relaxed (see Fig. 4.16), which can be the case for the monolithic integration of the structure with ancillary electronics. Secondly, the optical bandwidth can be increased by increasing the speed of the optoelectronics (channel data rate) and, in principle, by wavelength division multiplexing (WDM).

4.6. Conclusion

In this chapter, a novel metallic waveguide structure is proposed for the simultaneous transmission of optical and microwave data signals. This capability was confirmed by the simultaneous error-free transmission (BER$< 10^{-9}$) of optical and electrical data at 40 Gbps and 12 Gbps, respectively,

over a 3 mm long structure without any observable interference. The measured channel losses for the optical and electrical signals are approximately 12.6 dB (at 1550 nm) and 3.4 dB (at 12 GHz), respectively. The overall bandwidth density of the tested structure is approximately 1 Gbps/μm which is already comparable to existing state-of-the-art electronic interconnects. Additionally, the estimated bandwidth density requirement of ASIC chips in 2022 is 0.7 Gbps/μm, assuming 95 μm pitch in a flip-chip ball-grid-array (BGA) packaging technology [3]. The structure is capable of far greater bandwidth densities via optimization of its design, and by increasing the speed of the optoelectronics or adding optical carriers in a wavelength multiplexing scheme. The structure is, therefore, capable of addressing the bandwidth density challenge in present and future chip-to-chip communications, leading to increased module bandwidth for high-performance computing platforms among other applications.

5. Electrical performance analysis of the proposed FGCPW

5.1. Introduction

In chapter 4, an electrical-optical interconnect was proposed. The simulation results of the optical waveguide were provided. Moreover, the microwave waveguide performance was investigated using a numerical analysis based on conventional CPW's analytical formulations and full-wave simulation using ANSYS HFSS. In this chapter, two conventional circuit model analysis are performed based on measurement results of several different structures discussed in chapter 4. The aim of this chapter is to provide more insight into the RF behavior of the structure, and more specifically investigate the effect of contact pads. Additionally, the discussion presented in this chapter provides a better tool to model this structure for future designs compared to full 3D EM solvers, since due to the large aspect ratio of the proposed structure (i.e., nanometer thickness and several millimeters of length), the computer hardware requirement is beyond personal computers. The results presented in this chapter is accepted for publication in International Journal of Microwave and Wireless Technologies.

5.2. Structure

Fig. 5.1(a) depicts the schematic cross-section of the structure. The structure consists of three metal stripes of thicknesses t_1 and t_2, widths W_g and W_s, separated by distance *s*, and permittivities of ε_1 and ε_2, surrounded by a finite homogenous dielectric of thickness t_3 and permittivity ε_3 sitting on a dielectric of thickness t_4 and permittivity ε_4. This structure forms an embedded finite-ground

coplanar waveguide (FGCPW) capable of supporting quasi transverse electromagnetic (TEM) waves at microwave frequencies [48]. Each ground stripe is designed to be thin enough (~few tens of nanometer) to support long range surface plasmon polaritons (LRSPPs) at optical frequencies [19]. The microwave mode is excited and captured via GSG radio frequency (RF) probes from the top. In order to provide contact between the probes and the FGCPW transmission line, two ground pads with the same thickness as the signal stripe ($t_1 + t_2$) are designed (Fig. 5.1(b)). The two ground pads are connected to the corresponding ground stripes via five parallel connections of 5 µm width and t_1 thickness. The length of these connections is adjusted such that the overall trace pitch is compatible to that of available GSG RF probes. The LRSPP modes are excited and captured through edge-coupling technique via single mode fibers. In order to increase the optical coupling efficiency between the fibers and the ground stripes, optical tapers are designed. A 2 µm gap between optical tapers and ground stripes is inserted to provide electrical isolation of the ground stripes.

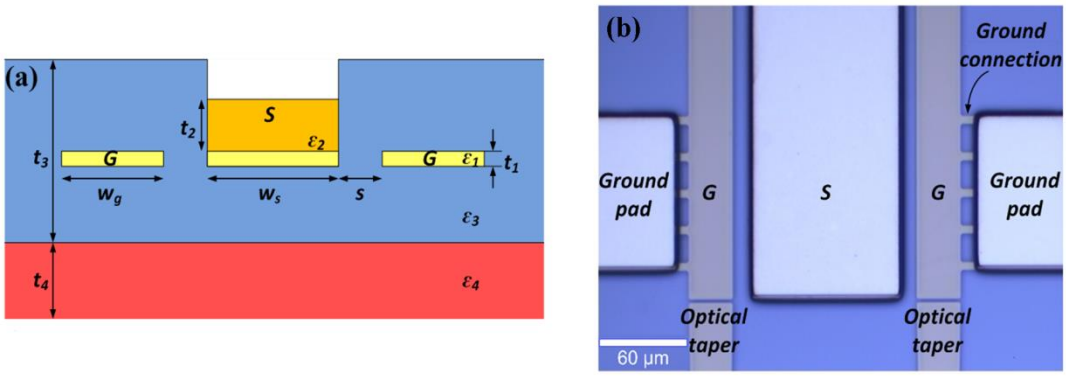


Fig. 5.1. (a) Schematic cross section of the proposed structure excluding the ground pads with connections as well as optical tapers. (b) Microscope image of a fabricated structure at one end of the transmission line.

5.3. Characterization of the FGCPW waveguide

Fig. 5.2 illustrates the schematic of the electrical S-parameter measurement setup for the characterization of fabricated waveguide structure using a 40 GHz vector network analyzer (VNA). An electrical input power of -10 dBm from the VNA is used to excite and capture the quasi-TEM mode of the proposed FGCPW. The waveguide is excited using an electrical GSG probe at its input. The transmitted signal is collected with a GSG probe at the output of the

waveguide structure. Both probes are controlled with 3-axis micro-positioners. The setup was calibrated prior characterization (*i.e.*, SOLT: short, open, 50 Ω load, and through) using a calibration substrate (Manufacturer: Cascade Microtech, 101-190B) to normalize the impact of the 40 GHz RF probes and electrical cables.

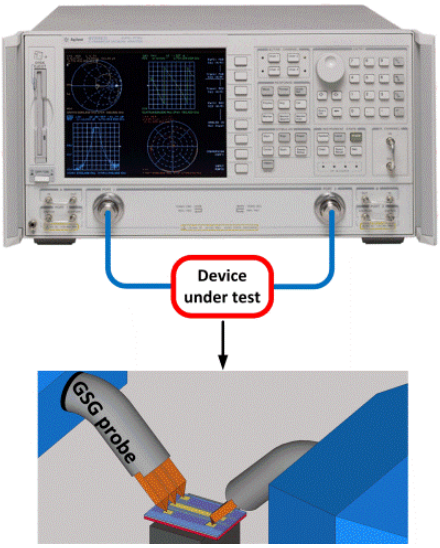


Fig. 5.2. Schematic of the experimental setup for the S-parameter measurements.

Fig. 5.3 presents the S-parameters results for various 3 mm long waveguides with a 50 µm wide signal stripe (W_s) and three different ground stripe widths (W_g of 5, 20, and 30 µm) and seven different separation distances (s of 2, 5, 8, 10, 12, 15, and 18 µm). As shown in Fig. 5.3(a)-(c), all structures show an amplitude drop at low frequencies up to approximately 1 GHz frequency. Then the transmission improves up to approximately 12 GHz. The transmission then decreases as frequency increases. The transmission drop at low frequencies is largely due to reflection in the structure. This will be discussed in section 5.4.2. The measurement shows that the wider the ground stripes (W_g) and separation distance (s), the lower the transmission loss. The results confirmed that a wider ground stripe leads to lower reflections due to improved impedance match (see Fig. 4.5 and Fig. 4.6), whereas, a larger separation distance leads to higher reflections.

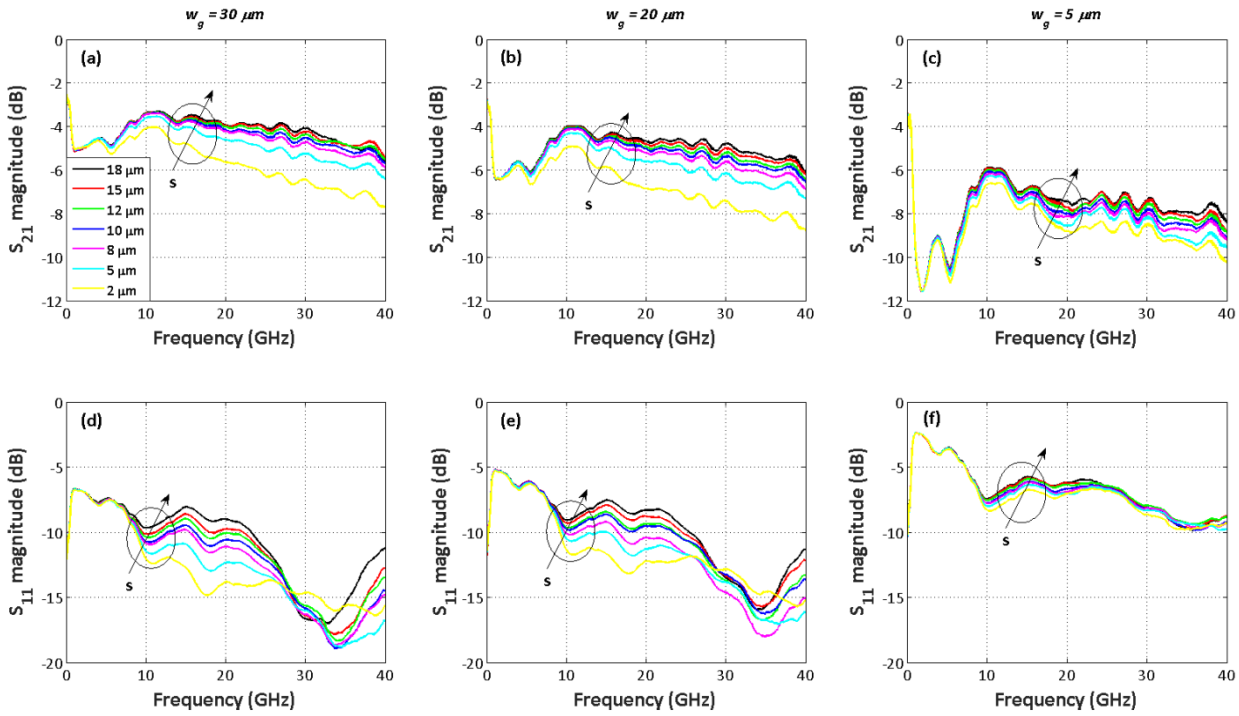


Fig. 5.3. Measured transmission (S_{21}) and reflection (S_{11}) parameters of the 3 mm long waveguides with W_s = 50 μm for different W_g and *s*.

5.4. Circuit models and transmission parameters extraction

Transmission line models are necessary to predict interconnect properties such as impedance, and propagation constant. There are two approaches to model a transmission line: distributed and lumped. The former is applied when the line's length is considered to be larger than the signal wavelength, and the latter is used otherwise. However, when the line's length becomes comparable to the wavelength of the signal (e.g., frequency from DC to few tens of GHz), careful consideration of these two models are required. This section provides analysis based on both models and discuss the accuracy of either approach.

5.4.1. Conventional distributed circuit model

Solutions to the well-known Telegraph's equations govern the interconnects where a pair of linear differential equations describes the voltage and current on an electrical transmission line as a

function of time and length. To simplify solving these equations, a two port network S-parameters model is introduced in which line voltage and current are described in terms of propagation constant (γ) and characteristic impedance (Z_C) as a function of frequency. Then, frequency dependency of the distributed transmission line parameters (i.e., R: resistance, L: inductance, C: capacitance, and G: conductance) are extracted. When the RLCG parameters are determined, the transmission line small signal frequency response can then be extracted [49]. Fig. 5.4 shows an infinitesimal section of the conventional distributed model for a transmission line with per unit length R, L, C, and G. In this section, all line parameters are considered to be a function of frequency.

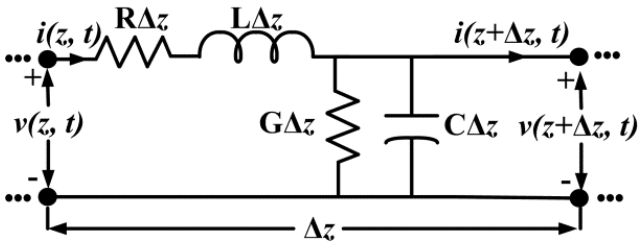


Fig. 5.4. The distributed element model applied to the FGCPW.

The solutions for a 50 Ω terminated (Z_0) line are formulated below [49],

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_C \sinh(\gamma l) \\ \frac{\sinh(\gamma l)}{Z_C} & \cosh(\gamma l) \end{bmatrix} \tag{1}$$

where,

$$\mathrm{A} = \frac{1+\mathrm{S}_{11}-\mathrm{S}_{22}-\Delta\mathrm{S}}{2\mathrm{S}_{21}} \tag{2}$$

$$\mathrm{B} = \frac{(1+\mathrm{S}_{11}+\mathrm{S}_{22}+\Delta\mathrm{S})\mathrm{Z}_0}{2\mathrm{S}_{21}}$$

$$\mathrm{C} = \frac{(1-\mathrm{S}_{11}-\mathrm{S}_{22}+\Delta\mathrm{S})}{2\mathrm{S}_{21}\mathrm{Z}_0}$$

$$\mathrm{D} = \frac{(1-\mathrm{S}_{11}+\mathrm{S}_{22}-\Delta\mathrm{S})}{2\mathrm{S}_{21}}$$

$$\Delta\mathrm{S} = \mathrm{S}_{11}\mathrm{S}_{22}-\mathrm{S}_{21}\mathrm{S}_{12}$$

whereby γ and Z_C can be determined and used for extracting the RLCG parameters from the standard transmission line equations [50],

$$\boldsymbol{\gamma} = \frac{1}{L}\cosh^{-1}(D), \qquad \boldsymbol{Z_C} = \frac{\sinh(\gamma L)}{C}$$
$$\boldsymbol{R}(\omega) = Re\{\gamma Z_C\}, \qquad \boldsymbol{L}(\omega) = \frac{Im\{\gamma Z_C\}}{\omega} \tag{3}$$
$$\boldsymbol{C}(\omega) = \frac{Im\left\{{}^{\gamma}/_{Z_C}\right\}}{\omega}, \qquad \boldsymbol{G}(\omega) = Re\left\{{}^{\gamma}/_{Z_C}\right\}$$

Fig. 5.5 shows the extracted parameters based on this model. The transmission line's extracted propagation constant is described by attenuation (Fig. 5.5(a)) and phase (Fig. 5.5(b)). As expected from the S_{21} measurements in the previous section, the attenuation increases with frequency, but benefits from an increased separation distance *s*. The phase linearly increases with frequency after approximately 7 GHz. At lower frequencies, the propagation phase fluctuates around zero, where small negative values suggest propagation in negative direction. This is mainly due to the high reflection at low frequencies (Fig. 5.3(d)-(f)). The characteristic impedance (Fig. 5.5(c)) decreases from large values at DC frequencies to 100 Ω at 1 GHz, and then it fluctuates between approximately 17 Ω and 100 Ω up to 40 GHz. At 40 GHz frequency the impedance is approximately 50 Ω which was the intended design (see Fig. 4.5 and Fig. 4.6). The phase of the characteristic impedance (Imag$\{Z_C\}$, not shown here) is mostly negative from DC to 40 GHz with the exception of a range 9.6 GHz to 15.5 GHz with relatively small positive values. These phase values show that the line's impedance is mainly capacitive over the range of tested frequencies.

The interconnect series resistance in Fig. 5.5(d) shows a weak increase up to approximately 16 GHz (depending on the separation distance), and then a sharp increase followed by a smoother decrease. The inductance (Fig. 5.5(e)) is relatively constant over the tested frequency range (~few hundred pico-Henry per millimeter), but there is a sharp decrease from DC to 1 GHz and negative values up to approximately 7 GHz. Fig. 5.5(f) shows that transmission line capacitance is varying from approximately 0.03 fF/mm to 0.25 fF/mm for the frequency range from DC to 40 GHz. The reduction in capacitance over certain frequency range indicates a transition from slow mode propagation to quasi-TEM mode propagation. Finally, Fig. 5.5(g) shows the extracted conductance which represents the dielectric loss.

The extracted parameters with negative values are not physically real. This is the case for the resistance *R* and inductance *L* below 7 GHz, and for the conductance *G* above 20 GHz. They

satisfy Telegraph's equation for propagation in the negative direction. This is due to the fact that the conventional transmission line model does not consider the effect of the contact pads. As such, a more accurate model is discussed in the following section where parasitic effects of the pads are modeled and extracted from measurement results of devices with different lengths.

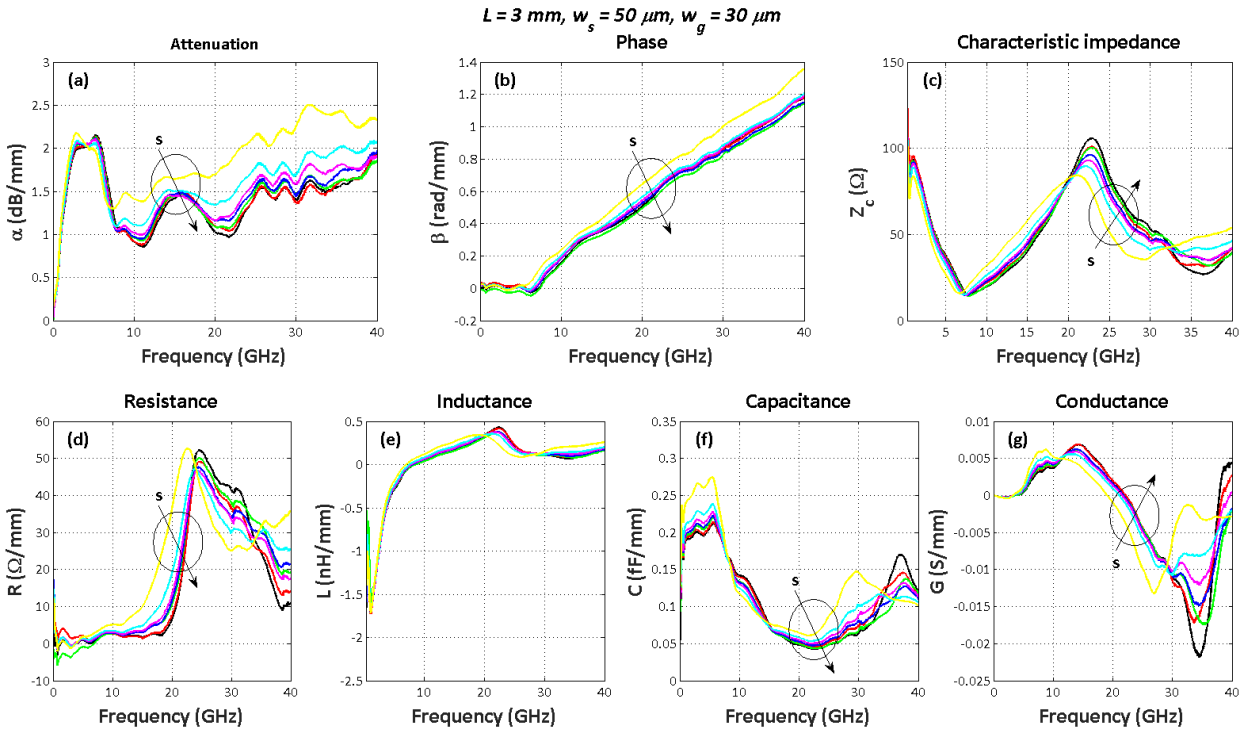


Fig. 5.5. Extracted distributed parameters as a function of frequency for a 3 mm long waveguide structure with W_s = 50 µm, W_g = 30 µm, and seven different separation distances *s* (direction of arrow refers to an increase in separation). (a) Attenuation, (b) propagation constant, (c) characteristic impedance, (d) resistance, (e) inductance, (f) capacitance, and (g) conductance.

5.4.2. Lumped circuit model

In this part, the optimal equivalent circuit model of the fabricated FGCPW is introduced and lumped circuit parameters are obtained using the Advanced Design System (ADS) commercial software. In this model, the two electrical pads at both ends and their connections are considered (Fig. 5.1(b)). These structures pose additional parasitic RLC elements onto the FGCPW transmission line which degrade the forward transmission (S_{21}), particularly at low frequencies

(i.e., below 10 GHz). This is mainly due to the sheet resistance, inductance and capacitance of the pads and their connections. Fig. 5.6 shows the circuit model which takes into account the pads at the input (TX) and at the output (RX) of the waveguide structure.

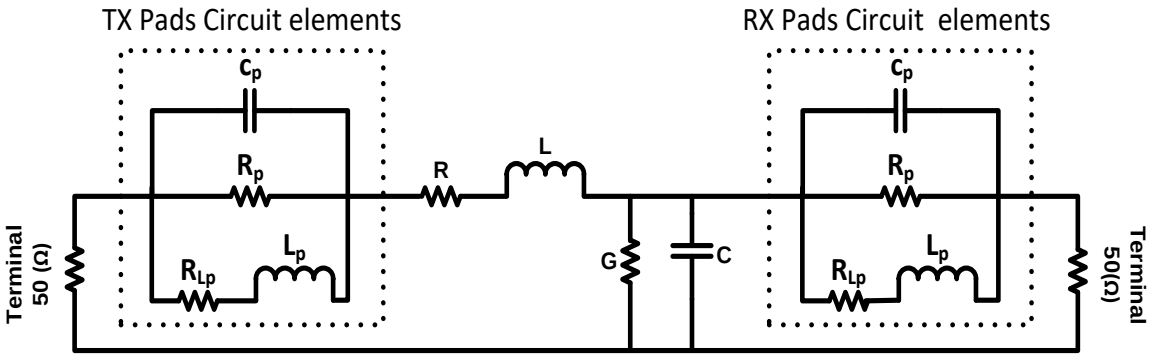


Fig. 5.6. Equivalent lumped circuit of the FGCPW transmission line in which the effects of the pads and their connections are considered.

To extract the optimized values of the lumped elements in the circuit model shown in Fig. 5.6, the measured S_{21} data are imported to the Agilent ADS software and the difference between the forward transmissions of the circuit model and the measured S_{21} is minimized. This process is done by applying the "Random" and "Gradient" optimization methods in the OPTIM engine of ADS software.

Table 5.1 summarizes the results for different waveguide lengths with a signal width of 50 µm (W_s), ground stripes of 30 µm (W_g) width, and a 15 µm gap (s). As expected, increasing the length results in an increase in the transmission line's resistance *R* and inductance *L*. It also reveals that the line's conductance *G* (or dielectric loss) is negligible. Additionally, the lumped capacitance of the proposed FGCPW is approximately two orders of magnitude less than conventional CPW structures on silicon substrate. It should be underlined that the small divergence in the parameters of the pads and their connections for different lengths is mainly associated with the optimization process of the ADS to find the minimum difference between the forward transmission of the circuit model and the measured S_{21}.

Table 5.1 Extracted lumped parameters from measured S-parameters based on lumped circuit model.

Electrical performance analysis of the proposed FGCPW

	Line parameters				Tx and Rx pads and connections parameters			
L (mm)	**R (Ω)**	**L (pH)**	**G (pS)**	**C (fF)**	**R_p(Ω)**	**R_{Lp} (mΩ)**	**L_p (nH)**	**C_p (pF)**
3	32.82	2.78	87.31	110.8	23.57	0.6983	6.109	1.263
5	42.20	3.46	65.69	213.4	44.07	1.0544	8.200	1.142
8	50.30	595.2	84.07	285.6	60.23	5.4571	10.67	0.834
13	65.60	1461.5	113.00	291.9	60.01	2.42	5.680	2.128

Fig. 5.7 shows the measured S_{21} transmission (solid line) for the four device lengths investigated in Table 5.1. Overlaid are the calculated transmission response obtained from the extracted circuit element values based on both the conventional model from the Telegraph's equation (black dash line) where the pads effect is not considered, and the customized accurate circuit model (red dash-dotted line) which includes the pads parasitic circuit elements. The circuit model results for four different lengths are plotted in two figures for proper scaling of the magnitude. As can be inferred from the figure, the conventional and custom circuit models for different lengths provide approximately the same results for frequencies above 10 GHz, while they differ at lower frequencies due to the effect of the parasitic elements originating from the pads and their connections, in which they act as a parallel lossy LC oscillator (i.e., parallel RLC circuit). This can be confirmed by calculating the equivalent impedance (Z_{in}) of the lumped circuit model as a function of frequency, in which the parallel RLC components cause high impedance mismatch at the input at low frequencies (below 10 GHz) resulting in high reflections. Therefore, the impact of the pads is significant and must be taken into account to optimize the structure across the entire frequency range.

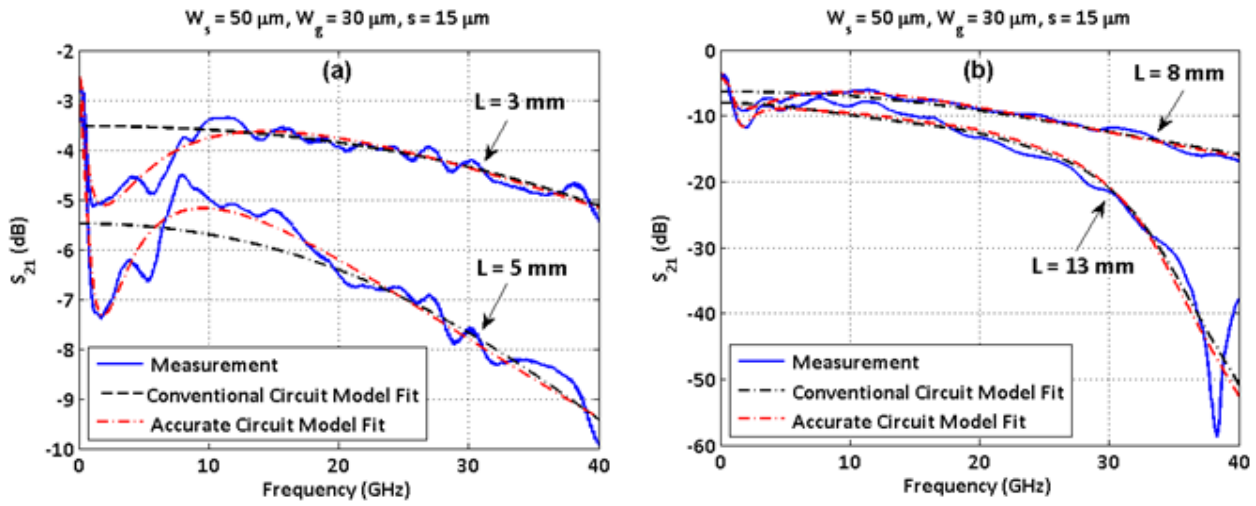


Fig. 5.7. The measured S_{21} parameter (solid line) along with the modeled transmission responses (with and without considering the parasitic elements) for the conventional circuit model (dashed line) and the accurate circuit models (dash-dot) for 3, 5, 8, and 13 mm long waveguides with 50 µm signal stripe width, 30 µm ground stripe widths, and 15 µm separation distance.

Fig. 5.8, shows that the 13-mm long transmission line exhibits a resonance at 38 GHz frequency which suggests the formation of a standing wave within the waveguide structure. Indeed, an impedance mismatch between the transmission line and the load will lead to reflections. If the incident signal is a continuous AC waveform, these reflections will mix with more of the oncoming incident waveform and produce stationary waveforms (i.e., standing waves) [51]. Measurements shown in Fig. 5.8 show that the resonance becomes weaker with smaller separation distances.

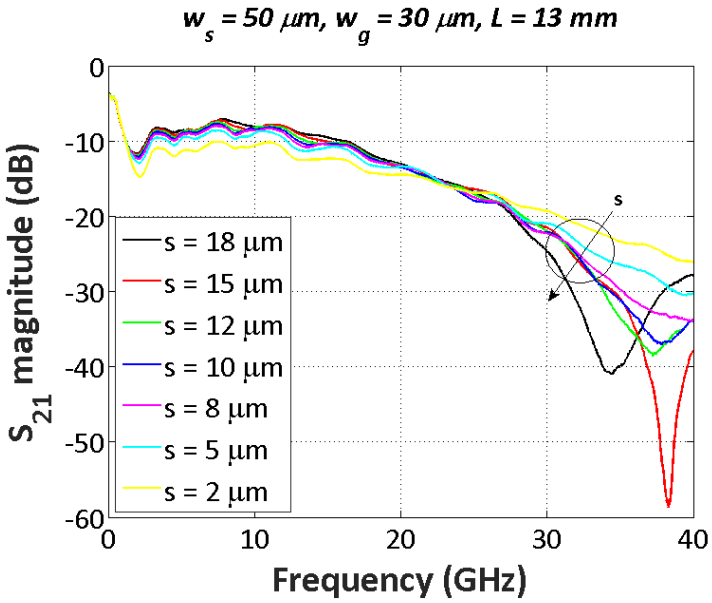


Fig. 5.8. Measured transmission of 13 mm long lines with W_s of 50 µm and W_g 30 µm for different separation distances.

5.5. Conclusion

This chapter presented the microwave performance of the discussed FGCPW waveguide. The hybrid waveguide is capable of supporting microwave and optical signals, simultaneously. A numerical method was discussed to optimize the geometrical parameters of the transmission line to match a given characteristic impedance. Using a conventional circuit model, the frequency dependent parameters were extracted from experimental measurements of fabricated waveguides with different dimensions. A more accurate circuit model enabled to take into account the impact of the parasitic elements from the ground pads at lower frequencies. Thus, to improve the performance of the structure, the pad effects should be minimized by reducing pad area (i.e., less capacitance) and length of the connection (i.e., less resistance and inductance).

6. Conclusion and future works

6.1. Conclusion

Long-range surface plasmon polariton (LRSPP) waveguides possess unique characteristics and potentially few advantages over popular silicon waveguides, which make them attractive for implementation as chip-to-chip interconnects. Despite, higher propagation losses and lower mode field confinement, LRSPP waveguides provide low coupling loss upon interfacing edge/surface emitting laser sources. Additionally, unlike silicon waveguides that require silicon-on-insulator (SOI) substrates, LRSPP waveguides can be fabricated on any substrate (e.g., flexible polymers). In this thesis, I first demonstrated that LRSPP waveguides are capable of transmitting NRZ-OOK data signals at 4x49 Gbps, as well as NRZ-DPSK data signals at 4x10 Gbps. The 3.6-mm-long gold stripe with a thickness of 35 nm and a width of 5 μm in Cytop supports an LRSPP mode with 13.2 dB of insertion loss at 1.55 μm.

Next, I proposed a novel structure comprised of three co-planar stripes which are capable of simultaneous transmission of optical and microwave signals. I experimentally demonstrated this capability by the simultaneous error-free transmission (BER < 10^{-9}) of optical and electrical data at 40 Gbit/s and 12 Gbit/s, respectively, over a 3 mm long structure without any observable interference. The measured channel losses for the optical and electrical signals are approximately 12.6 dB (at 1550 nm) and 3.4 dB (at 12 GHz), respectively.

Finally, I focused on RF behavior of the structure and provided circuit model analysis. This study showed that at low frequencies (< 10 GHz) the electrical pads and their connections act as RF chokes resulting in performance degradation.

The deployment of the hybrid link in short-reach interconnects is viable provided that higher bandwidth density and at least comparable power efficiency is achievable (including

optoelectronics) compared to electrical counterparts. In this thesis, I have demonstrated promising system-level performance and bandwidth density of the proposed hybrid link. These results suggest that the structure has the potential of being implemented as short-reach optical interconnects. However, further investigations such as power budget analysis are essential to completely assess the feasibility of this structure.

6.2. Future works

The proposed hybrid structure in this thesis is best fitted in architectures (e.g., concept structure proposed in [52]) where electrical interconnects are implemented using micro bumps (~20 µm, see Fig. 6.1 [53]). Thus, depending on the available fabrication technology, the ground pads as well as the signal connection (or pad) can be designed such that they are compatible with micro bumps for the electrical interface. Also, ideally the laser source and photodetector must be edge coupled to the waveguide. For laser source, edge emitting semiconductor lasers, and directly modulated such as quantum dot structures are a good fit.

Additionally, bandwidth and reach of the discussed transmission line are comparable to recent works [54, 55]. The bandwidth density of the proposed waveguide structures is 1 Gbps/µm [see reference 56] compared to 1.16 Gbps/µm in [54] and 1.5 Gbps/µm in [55]. In the former case, signal and ground traces width are 0.54 µm separated by 0.64 µm, supporting 2 Gbps data rate over 10 mm length. The bandwidth density of the hybrid structure in this work is limited mainly because the line's impedance was designed to be 50 Ω for characterization purpose. By relaxing this limitation to larger impedance (e.g., 100 Ω), the lateral dimension can be reduced to 31 µm by designing signal width of 1 µm (W_s), ground width of 5 µm (W_g), and separation distance of 10 µm (s) to achieve bandwidth density of roughly 5 Gbps/µm (see Fig. 4.5 and Fig. 4.6).

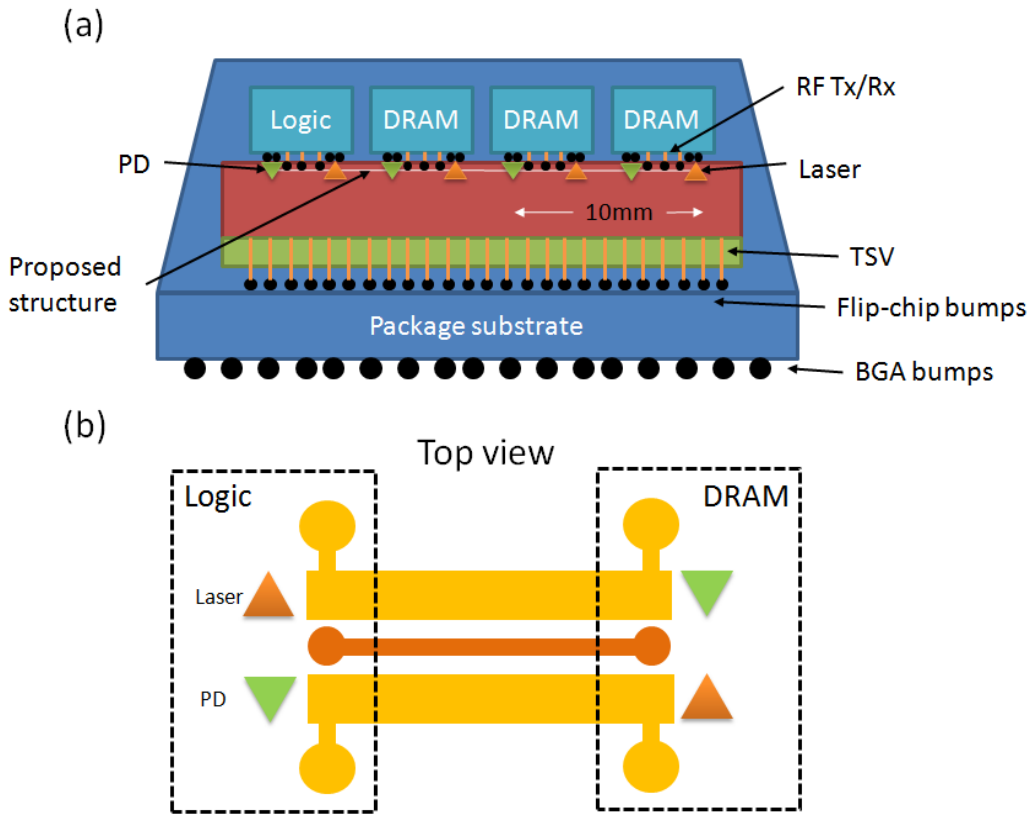


Fig. 6.1. The potential application of the proposed structure.

The proposed structure has inherently unlimited bandwidth density because it supports optical signal. Optical bandwidth limitations originate from E/O and O/E converters bandwidth. The goal of this structure is to provide efficient and low energy consumption chip-to-chip interconnects by allocating high data rate channels to the optical section and sending lower data rates (e.g., control signals) over electrical section. Assuming CMOS electrical transmitter and receiver with impedances in the range of 1000 Ω, the signal trace width can be as small as 0.5 µm and ground traces width can be designed to be as small 5 µm. The separation distance between signal and ground traces should be such that the optical mode on the signal stripe does not overlap with the signal stripe. For the aforementioned ground width a 10 µm separation distance must be considered for 20 nm thick stripe. Structures with thicker lines (35 nm) can have 7 µm separation distances. In conclusion, the geometry of the proposed structure can be optimized for a given characteristic of electrical transmitter and receiver.

6.3. Contributions

This section outlines the contributions of the author of this thesis (B. Banan) in chronological order.

6.3.1. Main contributions

1. Journals

[J1] **B. Banan**, F. Shokraneh, P. Berini, and O. Liboiron-Ladouceur, "Electrical performance analysis of a CPW capable of transmitting microwave and optical signals," *Int. J. Microw. Wirel. T.*, (in press).

B. Banan performed the design, fabrication, and characterization as well as the distributed circuit model analysis. F. Shokraneh contributed to the conformal mapping analysis and lumped circuit modeling. B. Banan and F. Shokraneh wrote the paper. P. Berini and O. Liboiron-Ladouceur helped with editing the paper and its structure.

[J2] **B. Banan**, R. Niall Tait, O. Liboiron-Ladouceur, and P. Berini, "Fabrication of metal stripe waveguides for optical and microwave data transmission," *J. Vac. Sci. Technol. B* vol. 33, pp. 061208, Nov. 2015.

B. Banan developed the fabrication process at Carleton University Microfabrication Facility (CUMFF) under the supervision of R. Niall Tait, and P. Berini. B. Banan wrote the paper and the co-authors helped with editing the paper and its structure.

[J3] **B. Banan**, M. S. Hai, P. Berini, and O. Liboiron-Ladouceur, "Simultaneous high-capacity optical and microwave data transmission over metal waveguides," *Opt. Express* vol. 23, pp. 14135-14147, Jun. 2015.

B. Banan and O. Liboiron-Ladouceur proposed the idea. B. Banan performed the design, simulation, fabrication, and characterization of the structure. P. Berini and O. Liboiron-Ladouceur provided feedback and suggestions during all steps. M. S. Hai helped with high-speed measurements. B. Banan wrote the paper and P. Berini, and O. Liboiron-Ladouceur helped with editing the paper and its structure.

[J4] **B. Banan**, M. S. Hai, E. Lisicka-Skrzek, P. Berini, and O. Liboiron-Ladouceur, "Multi-channel transmission through a gold stripe plasmonic waveguide embedded in Cytop," *IEEE Photon. J.* vol. 5, pp. 2201811, June. 2013.

B. Banan performed the characterization of devices provided by P. Berini's group (designed by E. Lisicka-Skrzek and fabricated by C. Chiu). P. Berini and O. Liboiron-Ladouceur provided feedback and suggestions during all steps. M. S. Hai helped with high-speed measurements. B. Banan wrote the paper and P. Berini, and O. Liboiron-Ladouceur helped with editing the paper and its structure.

2. Conferences

[C1] **B. Banan**, M. Mirshafiei, P. Berini, O. Liboiron-Ladouceur, "Microwave and optical transmission on metal stripe plasmonic waveguides," *International Conference on Surface Plasmon Photonics SPP6*, May 2013.

B. Banan performed the simulations. M. Mirshafiei, P. Berini, and O. Liboiron-Ladouceur provided feedback and suggestions during all steps. B. Banan wrote the paper and P. Berini, and O. Liboiron-Ladouceur helped with editing the paper and its structure.

[C2] **B. Banan**, M. Hai, E. Lisicka-Skrzek, P. Berini, and O. Liboiron-Ladouceur, "49 Gbps optical transmission through long-range plasmon polariton waveguide," *IEEE Photonics Conference*, paper TuI3, Oct. 2012.

B. Banan performed characterization of devices provided by P. Berini and E. Lisicka-Skrzek. P. Berini and O. Liboiron-Ladouceur provided feedback and suggestions during all steps. M. S. Hai helped with high-speed measurements. B. Banan wrote the paper and P. Berini, and O. Liboiron-Ladouceur helped with editing the paper and its structure.

[C3] **B. Banan**, A. Salehiomran, and O. Liboiron-Ladouceur, "Investigation of a flexible on-chip interconnection using a plasmonic stripe," *IEEE Photonics Conference*, MB4, Arlington, Oct. 2011.

B. Banan performed the simulations. A. Salehiomran and O. Liboiron-Ladouceur provided feedback and suggestions during all steps. B. Banan wrote the paper and A. Salehiomran, and O. Liboiron-Ladouceur helped with editing the paper and its structure.

6.3.2. Other contributions

In this listed publications on the topic of inter-chip data transmission exploiting optical mode-division multiplexing, B. Banan contributed in building the experimental setup and performing high-speed measurements.

[J1]. C. Williams, **B. Banan**, G. Cowan, O. Liboiron-Ladouceur, "A source-synchronous architecture using mode-division multiplexing for on-chip silicon photonic interconnects," IEEE Journal on Selected Topics in Quantum Electronics, 22(6), pp. 1-9, Apr. 2016.
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