HETEROJUNCTIONS ON MONOCRYSTALLINE SILICON

by

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Abstract

Transparent low resistivity CdS films have been evaporated on p-Si and n-p Si monocrystalline substrates to form heterojunction solar cells. Electrical and optical properties are investigated by I-V, C-V and quantum efficiency measurements. By comparing to conventional n-p Si cells, it is found that CdS/n-p Si configuration has the advantage of homojunction cells with a high V_{oc}, and the advantage of heterojunction cells with a high I_{sc}. The high V_{oc} is due to the electrical property domination of the homojunction of this configuration and the high I_{sc} is due to more electron-hole pairs excited by high energy photons at or near the homojunction of this configuration.

Effects of interface states on heterojunctions is also studied. Frequency dispersion on capacitance is observed on CdS/p-Si cells. The dispersion is due to the lattice mismatch between CdS and Si which introduces high densities of interface state. The densities of interface state and the relaxation time constant are calculated. The cause of dispersion can be determined by doing capacitance measurements at low temperature so that trap level effect is eliminated. No significant dispersion is observed on CdS/n-p Si cells. It further confirms the electrical property domination of the homojunction of the CdS/n-p Si cells.

RÉSUMÉ

Des films transparents et de basse resistivité de CdS ont été évaporés sur des substrats Si monocrystallin dopés n ou p pour ainsi former des cellules solaires à hétérojonction Des mesures I-V, C-V et d'éfficacité quantique ont été entreprises afin de déterminer les propriétés électriques et optiques Par rapport aux cellules solaires conventionnelles de Si p et n, la configuration CdS/n-pSi a, d'une part, l'avantage des cellules à homojonction, c'est-à-dire un grand V_{oc}, et d'autre part, un grand I_{sc}, ceci représente l'avantage des cellules à hétérojonction. La grandes valeur de V_{oc} est due au fait que les propriétés électriques de l'homojonction dominent dans cette configuration alors qu'une grande valeurs de I_{sc} est due à un nombre plus grand de paires électron-trou excités par les photons de haute énergie dans la région de l'homojonction

Les effets dus aux états d'interface sur l'hétérojonction ont aussi été étudiés Une dispersion de fréquence sur la capacitance a été observée pour les celleules CdS/p-Si Cette dispersion est due au "mismatch" des paramètres de mailles du CdS/p-Si, ce qui induit une assez grande densité d'États à l'interface La densité d'État à l'interface ainsi que le temps de relaxation ont été calculés Les phénomènes causant la dispersion peuvent être déterminés en faisant des mesures de capacitance à basse température afin d'éliminer les effets dûs aux étapes de piégeage Aucune dispersion significative n'a été observeé pour les cellules CdS/n-pSi, confirmant ainsi que les propriétés électriques de l'homojonction des cellules CdS/n-pSi sont dominantes.

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Chapter 1

Introduction

Energy resources on earth are limited but the energy demand is increasing rapidly. Novel and reliable energy resources are being sought urgently One promising candidate is solar energy using direct conversion of photovoltaic cells

Nowadays, some small units like calculators or complicated units like satellites are using monocrystalline homojunction silicon cells as power sources. Cells with an efficiency towards 20% have been reported [1.1] However, compared to heterojunctions, homojunctions usually collect less current because of surface recombination On the other hand, heterojunctions yield low open circuit voltage and often have large densities of interface state due to lattice mismatch of the two materials A homojunction-heterojunction configuration is then studied in this work to see if this configuration has the advantages or disadvantages from each type of junction or it has some other interesting characteristics

The semiconductor CdS is a well known window material and its preparation technologies are very well developed [1.2, 1.3]. Monocrystalline silicon solar cells technologies are also well developed As a result, these materials are chosen to form a heterojunction-homojunction cell, i e CdS on n-p Si cell The cell performance and band diagram are compared to the simple homojunction and heterojunction In order to have a better idea of the CdS/n junction of this structure, isolated CdS/n-Si devices are made

and studied as well Moreover, interface state effect on the cells is also studied

CdS/Si heterojunction has been investigated since 1967 [1 4, 1 5] Because of the improvement of the CdS films, cell with 11 3 % efficiency has been obtained [1 6, 1 7, 1 8]. The performance of the cells reported in this work may not be as good as those reported previously However, the goal is to characterize the Si homojunctions, CdS/Si heterojunctions and CdS/Si hetero-homojunctions and compare their performance

The arrangement of the thesis is as follows Some solar cell theories are given in Chapter 2. Fabrication processes of the n-p Si substrates and CdS evaporation processes are first given in chapter 3 P-n junction theories and all measuring methods to characterize junctions and CdS films are then described in chapter 4 Procedures for band diagram construction for homojunctions, heterojunctions and n-n junctions are presented in chapter 5. All experimental results are analyzed and reported in chapter 6 Finally, main conclusions of the thesis are given in chapter 7

Chapter 2

Solar Cell Theory

A solar cell is a photovoltaic device designed to convert sunlight into electrical power and to deliver this power into a suitable load in an efficient manner Solar behaviour can conveniently be examined through three main parameters (Fig. 2 1)· the open circuit voltage V_{oc}, which is the voltage output when the load impedence is much greater than the device impedence, the short current I_{sc}, which is the current output when the load impedence is much smaller than the device impedence; and the "fill factor" (F.F.), the ratio of the maximum power output to the product of V_{oc} and I_{sc} (the voltage and current for maximum output are known as V_m and I_m, respectively). These three parameters determine the efficiency and the circuit conditions to be used with the cell or an array of such cells.

The open circuit voltage of a p-n junction solar cell is directly related to the band gap of the semiconductor through the energy barrier height at the junction, it is often written as a function of the short circuit photocurrent, the dark current I_o of the junction, and the junction ideality factor n:

$$V_{oc}=n\left(\frac{kT}{q}\right)\ln\left(\frac{I_{sc}}{I_o}+1\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.1)$$

n is an empirical factor which describes the disagreement between ideal I-V p-n junction characteristic and experimental one. For a "perfect" junction, n is equal to 1 and

V_{oc} attains its highest value, while for larger values of n, I_o is larger in such a way that V_{oc} is reduced. The logarithmic nature of the relation (equation (2.1)) causes V_{oc} to effectively saturate as a function of light intensity. The dark current I_o is mainly determined by the band gap of the material and the temperature, I_o decreases and V_{oc} consequently increases with increasing band gap or decreasing temperature.

$$I_o \propto e^{\frac{-E_g}{kT}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2.2)$$

where E_g is the energy band gap of the semiconductor, k is the Boltzmann constant and T is the absolute temperature.

The short circuit current I_{sc} is determined by the spectrum of the light source and the spectral response (electron-hole pairs collected per incident photon) of the cell The spectral response in turn depends on the optical absorption coefficient α, the junction depth x_j, the width of the depletion region W, the lifetimes and mobilities on both sides of the junction, the presence or absence of electric fields on both sides of the junction The band gap dependence enters through the absorption coefficient, wider band gap materials absorb less sunlight and have smaller short circuit currents than narrow band gap materials

The fill factor (F.F.) is determined by the magnitude of the open circuit voltage, the value of n, and the series and shunt resistances R_s and R_{sh} (the internal resistances in series and in parallel with the p-n junction). The higher the V_{oc} and R_{sh}, and the lower the n and R_s, the larger the F F will be

In Fig 2.2, when photons are incident with energy greater than the bandgap,

absorption of the photons can take place and electrons can be raised in energy from the valence band to the conduction band, breaking electron-hole pairs. If the excess minority carriers (holes on the n-side and electrons on the p-side of the junction) are able to diffuse to the edges of the space charge region before they recombine, they are "swept" across the junction due to the electrical field in the depletion region, giving rise to a photocurrent In a short circuit condition, the photocurrent is called short circuit current I_{sc}. If a load is connected to the p-n junction, photovoltage is created In an open circuit condition, charges built-up take place at both side of the junction leading to open circuit voltage V_{oc} The polarity of the output voltage is the same as the forward bias direction of the device, but the photocurrent is opposite in direction to the forward bias current through the device in the dark.

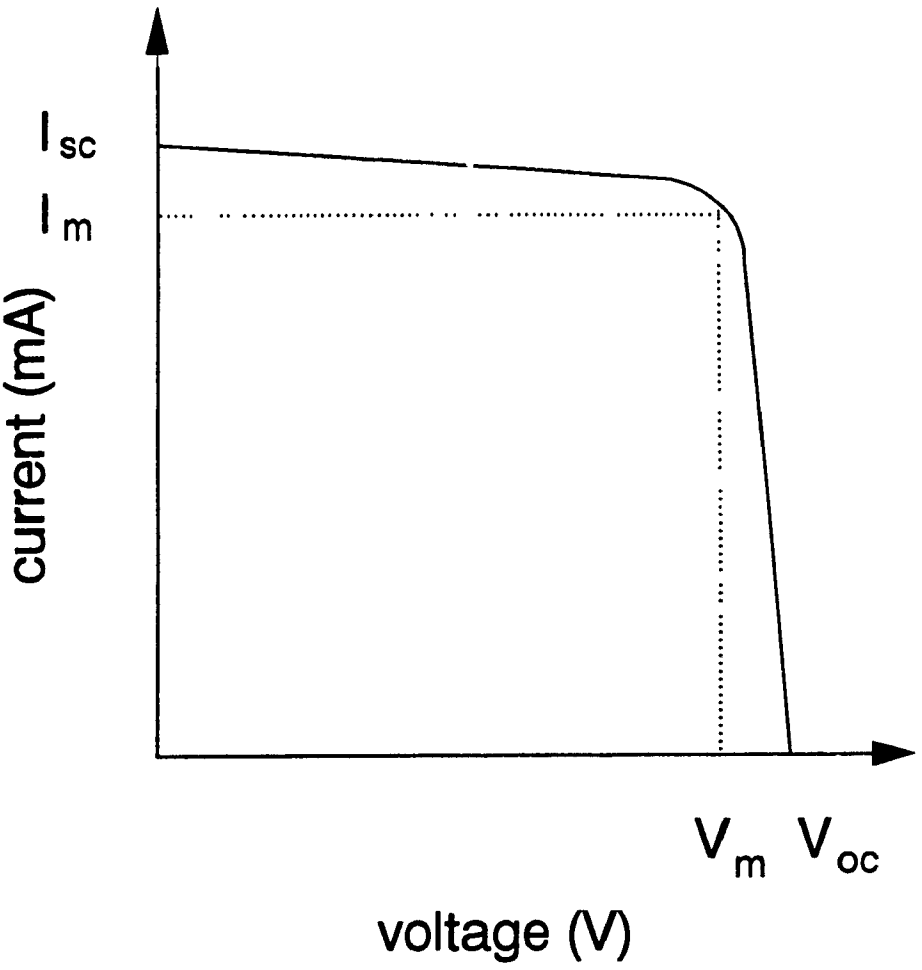


Fig. 2.1 Voltage and current output from an illuminated solar cell.

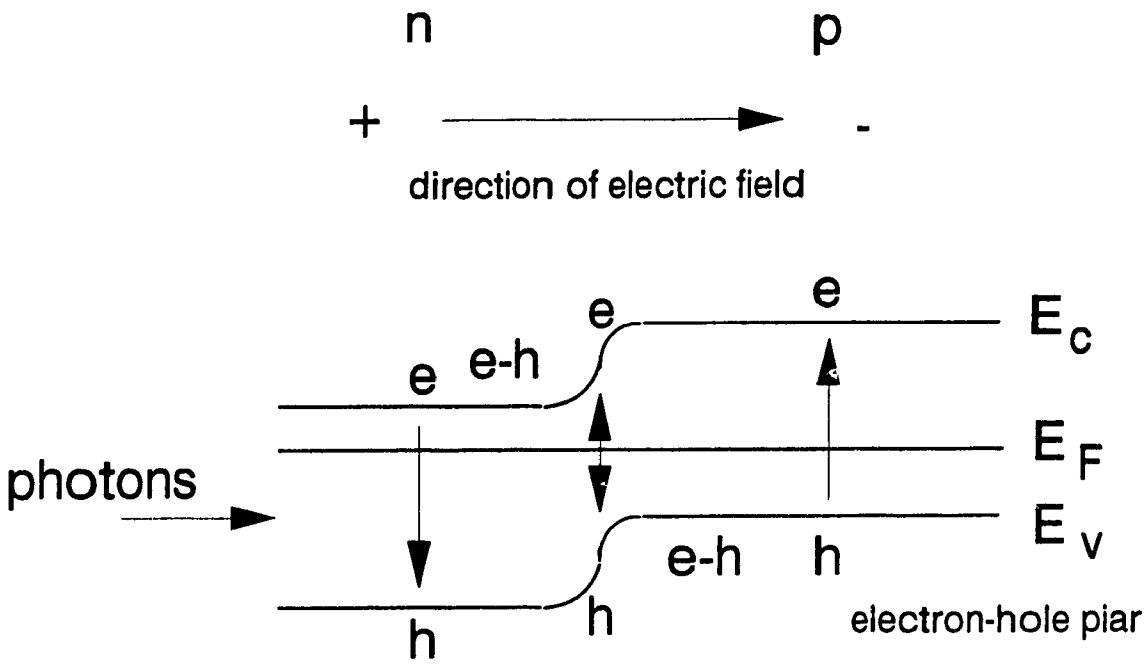


Fig. 2.2(a) Carriers generated by the incident photons.

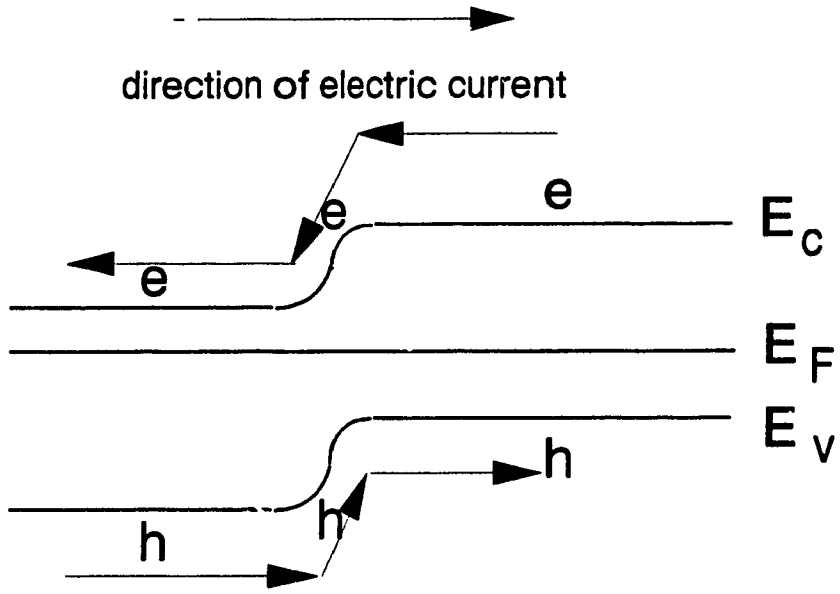


Fig. 2.2(b) Direction of electrical current and this is the short circuit condition with current equal to I_{sc}.

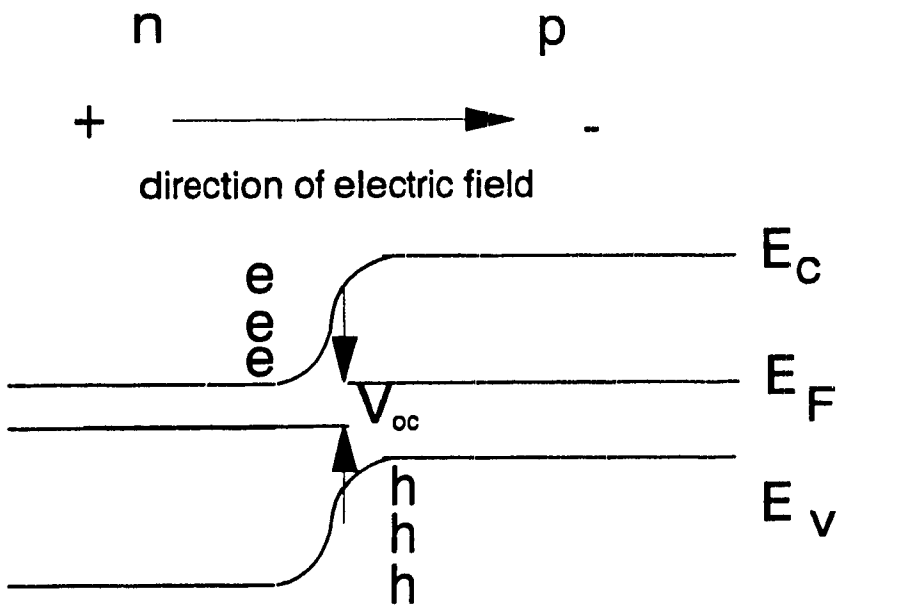


Fig. 2.2(c) V_{oc} generated at open circuit condition.

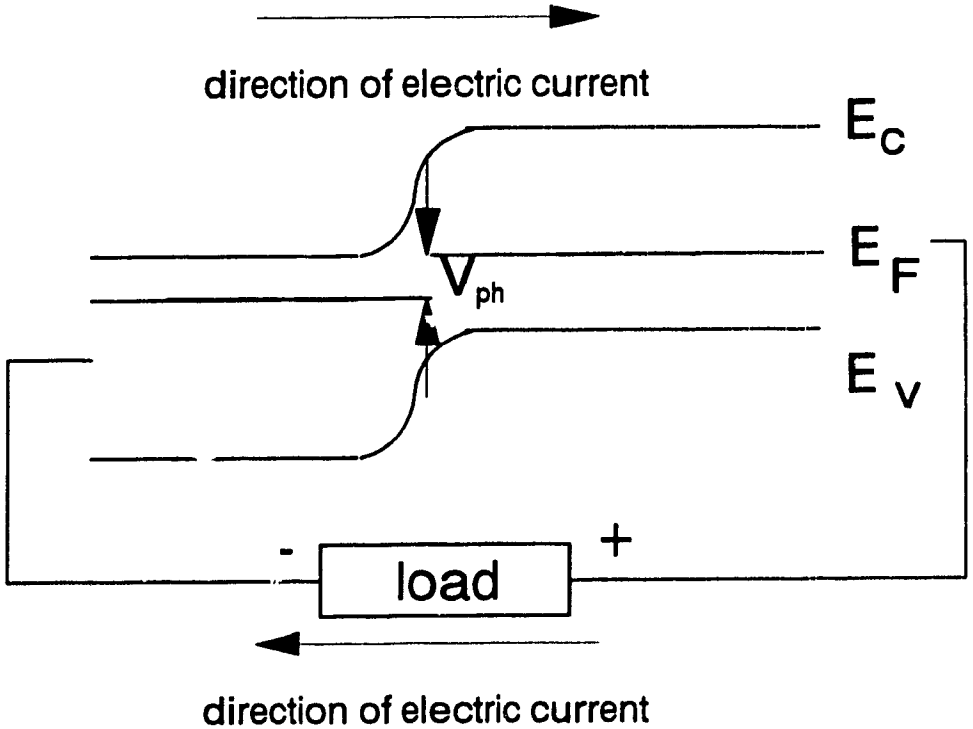


Fig. 2.2(d) Photovoltage V_{ph} generated when a load is connected to the solar cell.

Chapter 3

Experimental Procedures

In this chapter, experimental procedures for the fabrication of Si homojunctions, CdS/Si heterojunctions and CdS/Si hetero-homojunctions are described

3.1 Homojunction Solar Cell Fabrication (n-p Si)

The basic structure of a silicon solar cell is a p-type silicon wafer into which n-type dopant is diffused. The pertinent details of the n and p-type wafer are listed in appendix I The reader who is interested in the details of each step in fabricating the cells can refer to the appendices(I-IV)

The general procedure of making the cells is given as follows:

[1] A piece of p-type wafer is selected and hot point probe is used to confirm the wafer conduction type

[2] The resistivity of the wafer is then determined by using a four point probe resistivity test instrument.

[3] The wafer is put through the cleaning process, i.e., the degreasing, etching, and decontamination stages [see Appendix I]

[4] After the wafer is cleaned, a p+ layer is diffused into the back side of the wafer to obtain an ohmic contact between the wafer and the evaporated aluminum at the

back

The p+ layer can also avoid the type conversion at the back during n+ diffusion on the front. In order to avoid the p+ dopant contamination on the front side of the wafer, a layer of silicon dioxide is grown before the p diffusion. The reader who is interested in the details of wet oxidation process can refer to the appendix V

[5] After the wet oxidation process, a layer of SiO_2 is grown on the wafer. The back side of the wafer is then etched using buffered HF to remove the oxide Then two drops of p+ dopant(borosilicafilm from Emulsitone Co) are applied on the back side of the wafer. The wafer is spun at 3000 rpm for 15 seconds Then the wafer is put on a quartz boat and pushed into the center of the furnace slowly using a quartz rod. The diffusion temperature and time are 1100°C and 15 to 30 minutes, respectively

[6] After the p+ diffusion, the wafer is etched using the buffered HF to remove the excess dopant on the back side and the silicon dioxide formed on the front side

[7] The wafer is doped with n-type dopant (phosphorosilicafilm from Emulsitone Co). This is done by placing the wafer with the shiny surface facing up on a spinner, applying one or two drops of phosphorosilicafilm on the centre of the wafer and spinning immediately at 3000 rpm for 15 seconds Then the wafer is baked in a preheated oven at 150°C for 20 minutes.

[8] This is followed by diffusing the n-type dopant into the p-type wafer. The wafer is put in the center of the furnace similar to the p+ diffusion and diffused for the required time and temperature.

[9] After diffusion, the wafer is etched in the buffered HF solution to remove the

excess dopant on the surface of the wafer and the silicon dioxide layer which is formed during the diffusion process

[10] A layer of aluminum film (thickness about 1 um) is evaporated at the back side of the wafer. The wafer is then treated at 500 ^{o}C in nitrogen gas for 15 minutes The evaporated aluminum forms an ohmic contact to the p+ layer of the back of the wafer.

[11] In order to achieve low series resistance, an eight finger aluminum mask is used to make the front contact of a 1 cm^2 cell. The area of the fingers is 0.19 cm^2 and the active area of the cell is equal to 0 81 cm^2. A top view of the cells is in Fig. 3.1. Aluminum forms an ohmic contact to n+ type Si semiconductor and no heat treatment is necessary.

3.2 n+/n Silicon Wafer Preparation

Since heavily doped n-typed wafer is not available, CdS is evaporated on the wafer in which an n^+ layer is diffused The pertinent details of the n-type wafer is in Appendix I. Both CdS/n+ Si and CdS/n Si structures are studied.

The diffusion steps for the n^+-n substrates are similar to that of the n-p Si cell fabrication. The only differences are the type of the substrate and without p^+ back diffusion, since Wood's metal forms low resistance ohmic contact to n-type Si semiconductor. Wet oxidation is also not necessary.

3.3 Determination of Junction Depth

Since the junction is shallow (0.05 um - 0 2 um), angle lapping and staining of junction used in determination of the junction depth of a deep diffused silicon cell is practically impossible. The only way to determine the junction depth is by theoretical approximation.

The diffusivity, D, is given by [3.1]:

$$D=D_o\exp\left(-\frac{E_n}{kT}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.1)$$

where D_o (3.85 cm^2/sec) is the diffusivity of phosphorus in silicon at zero temperature and E_n (3.66 eV) is the activation energy of phosphorus in silicon. The Gaussian approximation [3.2] is employed to calculate the approximate junction depths.

3.4 CdS Evaporation

To fabricate a heterojunction solar cell (CdS/p-Si or CdS/n-p Si), CdS evaporation is done prior to front aluminum evaporation. The CdS evaporation is carried out in an Edwards model E306A vacuum evaporator. Cadmium sulphide powder with 2 % (by weight) indium sulphide is used for the evaporation. The background pressure of the system at the start of the evaporation is in the order of 10^{-6} Torr. Powder of CdS is loaded in a tantalum boat which has a quartz-wool at the opening to prevent spattering, i.e. the direct ejection of small particles of CdS from the source. The samples are

mounted on an Al substrate holder and heated to about 180°C before the evaporation. Since the sublimation temperature of indium is higher than that of cadmium sulphide, a shutter covers the samples while the boat is heating up. As the temperature is higher than about 700°C, the shutter is open. If the samples are not covered by the shutter when the boat heats up, a thin layer of high resistivity cadmium sulphide is deposited on the samples prior to the In-doped low resistivity one The heating process of the CdS evaporation is in appendix VI. After the evaporation, the substrate holder is cooled by circulating water through the water feedthrough. The thickness of the CdS layer is about 1 to 3 um. The resistivity is in the order of 10^{-3} to 10^{-4} ohm-cm and the impurity concentration is about 10^{19} cm^{-3}. A schematic diagram of the apparatus in the vacuum system is shown in Fig. 3.2.

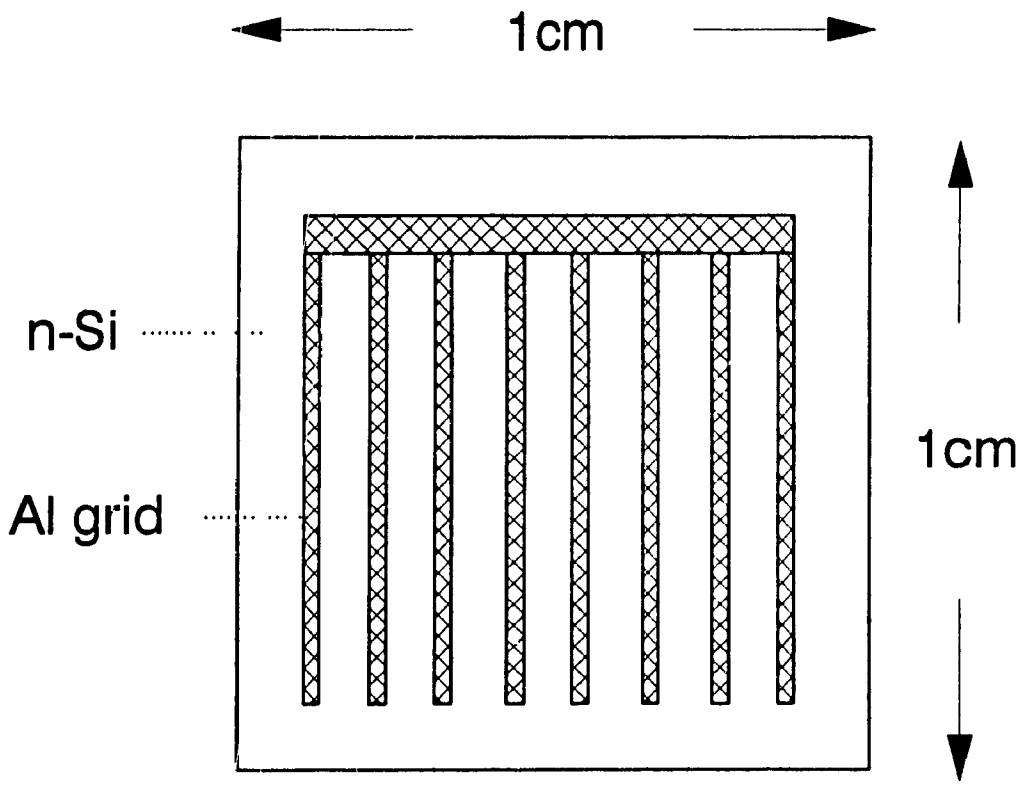


Fig. 3.1 The top view of a solar cell, the shaded aluminium grid has an area of 0.19cm^2.

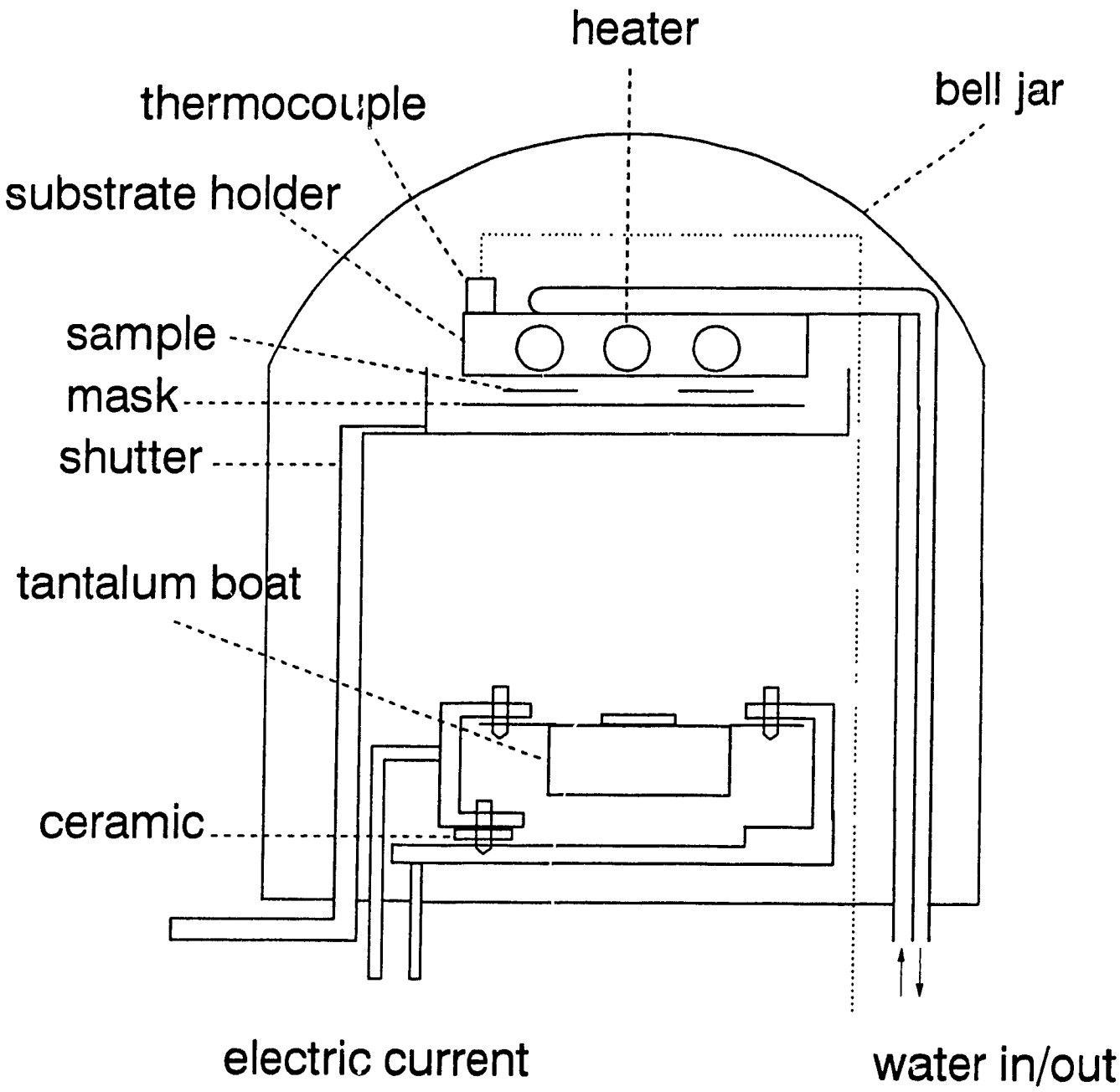


Fig. 3.2 The vacuum chamber setup for CdS evaporation.

Chapter 4

Device Characterization

4 1 Current-Voltage Measurements

The current-voltage characteristics (I-V) of the cells are measured by using an HP model 4145A semiconductor parameter analyzer The open circuit voltage (V_{oc}), short circuit current (I_{sc}), fill factor, ideality factor, series resistance, efficiency and the voltage shift between dark and illuminated conditions can be obtained A calibrated tungsten lamp is used to simulate AM1 illumination conditions

The V_{oc} and I_{sc} are directly obtained from the I-V characteristic. The fill factor (F.F.) is calculated from the equation,

$$F.F. = \frac{V_m I_m}{V_{oc} I_{sc}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.1)$$

where V_m and I_m are the voltage and current which yield the maximum power The ideality factor, n, which can tell the forward current mechanisms is obtained by fitting the measured I-V values to the equation,

$$I = I_o \left[\exp\left(\frac{qV}{nkT}\right) - 1\right] - I_{ph} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.2)$$

where I_{ph} is the photocurrent and I_o is the saturation current. q is charge of an electron, k is the Boltzmann's constant (8.62×10^{-5} eV/°K), T is absolute temperature and V is the

voltage across the device. The parameters I_o and n are determined by fitting the experimental ln(I) versus V dark characteristic (I_{ph}=0) by the straight line,

$$\ln(I) - \ln(I_o) = \frac{qV}{nkT} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.3)$$

The slope of the line and the intercept at V = 0 yield the values of n and I_o, respectively

The ln(I) vs V curve of a junction is shown in Fig. 4.1. The ideality factor tells the quality of the junction For "perfect" junction, n is equal to 1 at any forward bias. However, this is not the case in real p-n junction. For small forward bias, the generation recombination current in the space charge region is dominant and the ideality factor is equal to 2. For intermediate forward bias, the low level injection current takes over and the ideality factor is equal to 1 For larger forward bias, the high level injection current causes an increase in recombination and generation mechanisms that changes the ideality factor to 2 The ln(I) vs V curve bends downward as the forward voltage increase further because of the series resistance effect

Built-in potential, V_{bi}, is the potential across the depletion region of the device at thermal equilibrium The voltage shift, which is illustrated in Fig. 4.2., at I=0 between dark and illuminated conditions shows if there are high density of interface states at the junction When the cell is illuminated, the interface states will charge up at the junction As a result, the electric field near the junction and the band bending are changed. As long as the cell is being illuminated, the interface state is still charged and the band bending is different from that in dark condition. Therefore, the V_{bi} of dark condition is

different from that of illuminated condition. The shift can be as large as 0.2 V. For homojunctions, the voltage shift usually is less than 0.1 V.

The shift of V_{bi} can be positive or negative and it depends on the type of interface states, i.e. acceptor or donor like interface states. In Fig. 4 3, there are acceptor like interface states at p side of a n-p junction. As they charge up negatively under illumination, the electric field increases near the junction and this causes the V_{bi} to increase On the other hand, if the interface states are donor like such as the ones shown in Fig. 4.4, they charge up positively under illumination and the electric field will decrease near the junction In this case, the V_{bi} is smaller than that in a dark condition

4.2 Capacitance Measurements

4.2.1 Setup

Junction characteristics are obtained by measuring the complex impedence at frequencies in the range from 50 Hz to 2 MHz and at dc bias voltage from -0.8 V to 0 2 V. The dc bias voltage is monitored by an HP model 3478A multimeter The sample is mounted in a cryostat which can be cooled down to liquid nitrogen temperature or warmed up to 500 K. The required temperature range for the measurements of Si devices is from 200 K to 400 K. The capacitance of the cells is measured using an HP model 4192A impedence analyzer which is controlled by an IBM-PC computer. All the data is stored in a diskette. A schematic diagram of the apparatus is shown in Fig. 4 5.

4.2.2 C-V Measurements

The capacitance vs voltage (C-V) measurements at high frequency (100 kHz) give the V_{bi}, substrate impurity concentration and depletion width. These are important parameters to construct experimental band diagrams. Details of the band diagram are described in chapter 5.

4.2.3 C-F Measurements

The capacitance vs frequency (C-F) measurements at different bias voltages can obtain information on interface states and/or trap levels near the junctions. This method is used by many researchers and proven to give reasonable results [4.1, 4.2].

4.2.4 C-F Characteristics of Homojunctions

The interface state densities in homojunction cells are expected to be low ($<10^9$ $eV^{-1}cm^{-2}$), therefore the capacitance values are ideally unchanged throughout the frequency (f) range (see section 4.2.5 for explanation). However, a slight drop on capacitance is usually seen at high frequency (~1 MHz). This change is not due to the interface states, but is due to series resistance, R_s, according to the following equation [4.3],

$$C_m = \frac{C}{(R_s G+1)^2 + (wR_s C)^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.4)$$

where C_m is the measured value, C is the actual diode capacitance, G is the actual diode shunt conductance, R_s is the series resistance and w is the angular frequency.

4.2.5 C-F Characteristics of Heterojunctions

A model of a heterojunction (CdS/p-Si) with the presence of interface states is given in Fig. 4.3. When a bias voltage is applied to a heterojunction, the occupancy of the interface states will follow the variation of the bias voltage across the depletion region. The small alternating signal will then cause changes in the interface states density at the Fermi level if it can respond to the frequency of the applied signal. The measured capacitance usually decreases as the frequency is increased. This can be interpreted as the failure of interface states to respond to the higher frequency. The capacitance can therefore be expressed as the sum of the depletion region capacitance and the contribution of the interface states according to the following equation [4.1, 4.2, 4.4]

$$C = C_d + \frac{C_{is}}{[1+(w\tau)^2]} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.5)$$

where C_d, the capacitance at high frequencies, is the capacitance of the depletion region, C_{is} is the contribution to the capacitance due to interface states. At low frequencies, the measured capacitance is equal the sum of C_d and C_{is}. τ is the characteristic time of the relaxation process associated with interface states and w is the angular frequency ($2\pi f$).

In a typical measurement, the capacitance per unit area vs frequency curve is like Fig. 4.6. C_d is obtained at high frequency and C_{is} is equal to the capacitance at low frequency minus C_d. The density of interface states N_{is} can be related to C_{is} per cm^2 by the following equation [4.1, 4.2, 4.4],

$$N_{is}(V) = \frac{C_{is}(V)}{q} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.6)$$

where q is the coulomb charge of one electron and C_{is} and N_{is} are dependent on bias voltages

If either interface states or trap levels affect the capacitance vs frequency measurements, the mid-section of the curve is approximately a straight line. If more than one frequency dispersion factor exists, multiple values for τ are expected and more than one straight line section can be drawn.

To find τ [4.5], on each straight line section, two different points are chosen, (C_i,f_i) and (C_j,f_j). Then a second line is sketched from $[(C_i-C_d),(2\pi f_i)^2(C_i-C_d)]$ and $[(C_j-C_d),(2\pi f_j)^2(C_j-C_d)]$ to fit the points Finally, the square root of the slope of the second line is τ. A detailed calculation of an example is in appendix VII.

The time constants of interface states are relatively smaller than that of trap levels [4.5]. In presence of interface states with a high density, the deionization of the level that interacts with the Fermi level will take place involving a great quantity of other levels and will perhaps take place by tunnelling (illustrated in Fig. 4.7(a)) through the energy levels created by the interfacial states rather than by the usual thermal band to band emission (illustrated in Fig. 4.7(b)), thus justifying the lack of temperature dependence of the

relaxation time constant and capacitance values. From these two facts, the nature of the mechanism causing the frequency dispersion of capacitance can be known

Finally, the frequency dispersion of capacitance is less significant as the junction is reverse biased. The probable interpretation is that with a wider depletion layer, the edge of the space charge regions in both side of the semiconductors are further away from the interface states so that the influence to capacitance measurements is diminished [4 6].

4.3 Quantum Efficiency

Quantum efficiency or photo-response is the actual number of carriers collected per incident photon at each wavelength The photo-response of the cells is calculated by the ratio of the numbers of input photons to the cells and generated charge carriers from the cells. A Beckman model 2400 Monochromater with a halogen light source are used A silicon detector is used to monitor numbers of input photons. The spectrum concerned is from 0.5 um to 1.1 um. The quantum efficiency (Q.E.) can be calculated using the following equation,

$$Q.E. = \frac{J_{cell}}{q} / \frac{J_{detector}}{R*h\upsilon} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.7)$$

where J_{cell} and $J_{detector}$ are the current generated form the cell and the detector per unit area (A/cm^2), respectively R is the responsivity (A/W) and hυ is the energy per photon at each frequency. The experimental setup is shown in Fig 4 8(a)

The currents generated from the cells are measured directly by the HP model

4145A semiconductor analyzer since it is capable of measuring currents in the order of 10^{-9} A. The voltage bias effect on the cells from the resistor during measurements can then be avoided

In addition, by looking at the variation of photoresponse, one can tell if it is a one-sided junction, n-p junction or back to back n-type junction, etc. Detailed explanation is given in section 5.4.

4.4 Characterization of Cadmium Sulphide Thin Films

The CdS film is deposited on a piece of glass and the sheet resistance of the film is found by using four point probe method The resistivity of the CdS films used for heterojunction cells is about 10^{-3} to 10^{-4} ohm-cm. Moveover, the optical transmission of the film as a function of wavelength is measured and shown in Fig. 4.7. A typical transmission rate of a CdS film is shown in Fig 4.9. The same optical arrangement for quantum efficiency measurements is used in Fig 4.8(b). The light reaching the silicon detector through a plain glass is compared to that through a glass with CdS film.

The film thickness is estimated using interference of light in the thin film [4.7]. When visible light with a wavelength from 0.4 um to 0.8 um is incident on the surface of a film, interaction of two or more rays causes the intensity of the light to increase or to decrease in a specific direction [4.8].

As shown in Fig 4.10, when an incident light reaches the top surface of the thin film, it will be partially reflected and partially refracted. When the refracted light reaches

the bottom surface, it is partially reflected to the top surface and is refracted again. For a transparent material, the intensity of the reflected light usually is much lower than the refracted light. Therefore, it is sufficient to consider only the interference of the first two reflected rays.

The difference in the optical path Δl of the interacting light beams is:

$$\Delta l = (OC+OC_1)\, n-OF=\frac{2t*n}{cosB}-2t*tanB*sinA \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.8)$$

Here n is the refractive index of the film, and n=sinA/sinB,

$$\Delta l=\frac{2t}{cosB}\frac{sinA}{sinB}-2t*tanB*sinA \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.9)$$

$$\Delta l=2t*n*cosB=2t\sqrt{n^2-\sin^2 A} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.10)$$

Since the phase of the light reflected from the top surface will change by π,

$$\Delta l_{ef}=1-\frac{\lambda}{2} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.11)$$

when $\Delta l_{ef}=2K\lambda/2$ or $\Delta l=(2K+1)\lambda/2$, the maximum interference will occur

By knowing K, λ, A and n, the thickness t can be obtained

$$t=\frac{K\lambda}{2\sqrt{n^2-\sin^2 A}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.12)$$

where K is number of rings, λ is the wavelength of the incident light (red light = 0.7 um), n is the refractive index of the film and A is the incident angle of light which is equal to zero. During the measurements, the samples are placed under white light or a microscope illuminator and the number of interference rings is counted. Usually, red interference

rings are chosen for the calculation because they can be clearly seen under white light The wavelength of red light is about 0.7 um and the refractive index of CdS is about 1.2. Therefore, from equation (4.12), each ring corresponds to about 0.3 um. In addition, the mobility of the carriers and impurity concentration of the film are obtained by Hall Effect measurements.

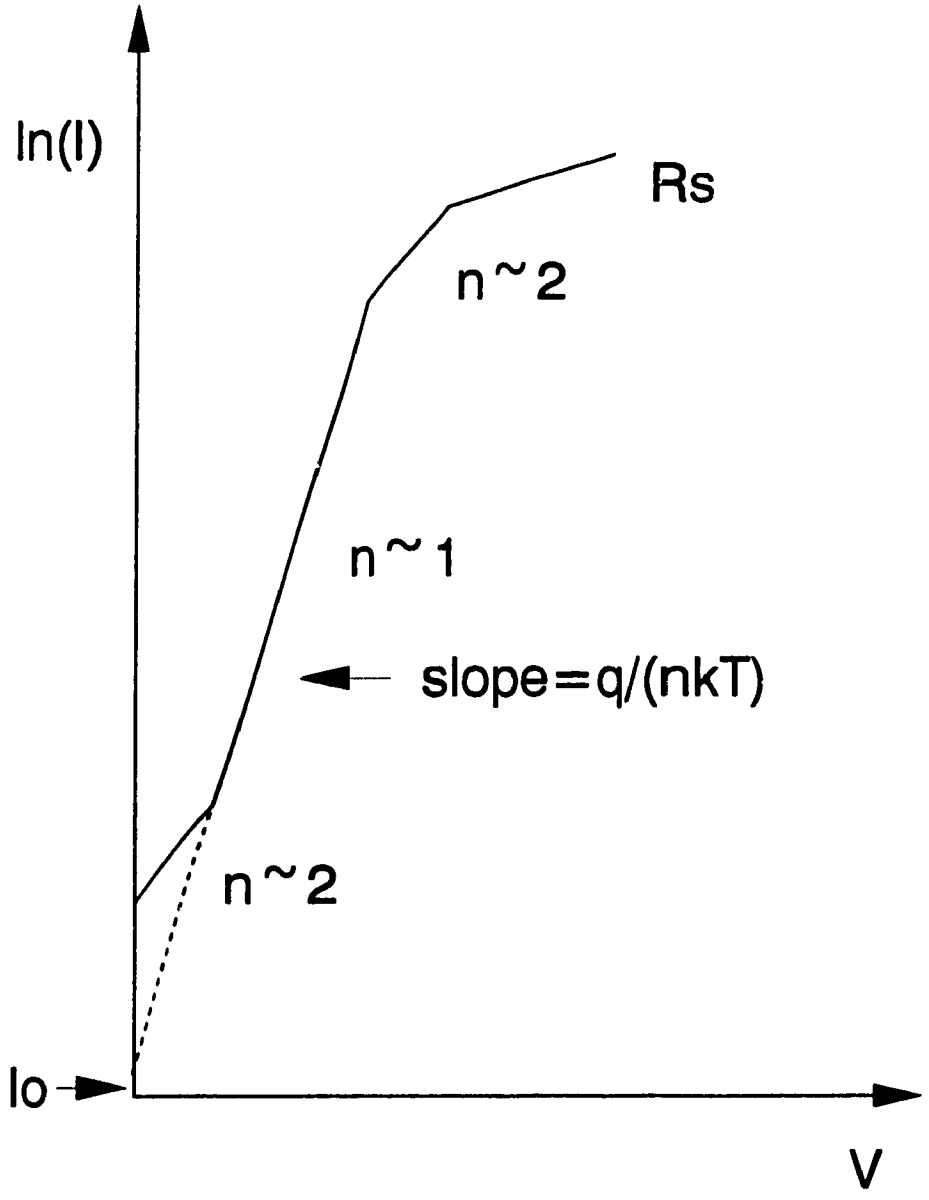


Fig. 4.1 Forward bais deviations from the ideal of a PN junction.

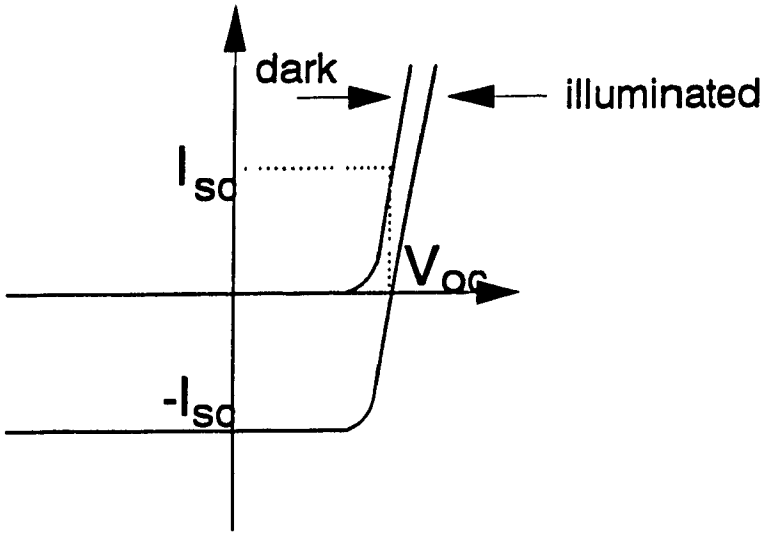


Fig. 4.2(a) I-V Characteristics of ideal p-n junction solar cell without voltage shift.

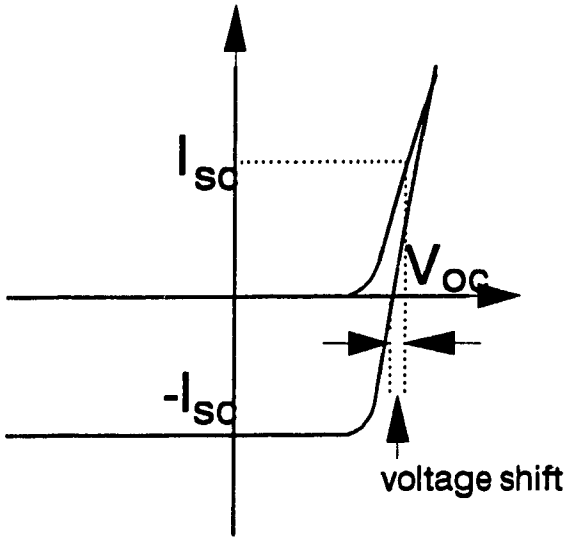


Fig. 4.2(b) I-V Characteristics of actual p-n junction solar cell with voltage shift.

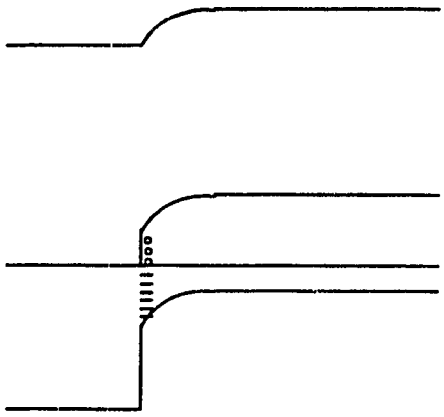


Fig. 4.3(a)

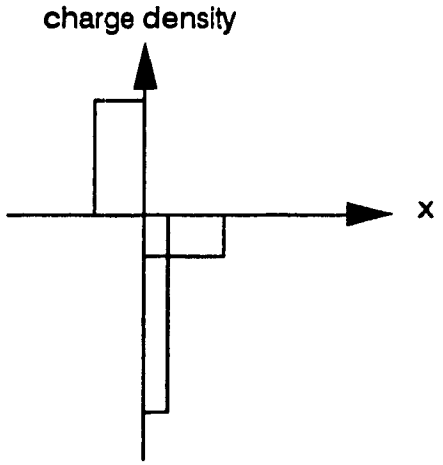


Fig. 4.3(b)

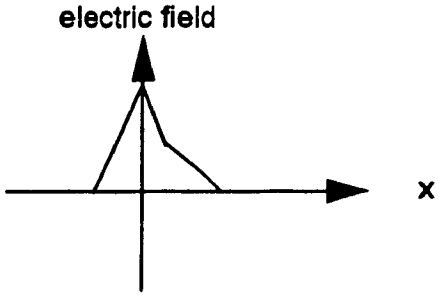


Fig. 4.3(c)

Fig. 4.3 The band diagram (a), charge distribution (b) and electric field distribution (c) of a junction with acceptor like interface states.

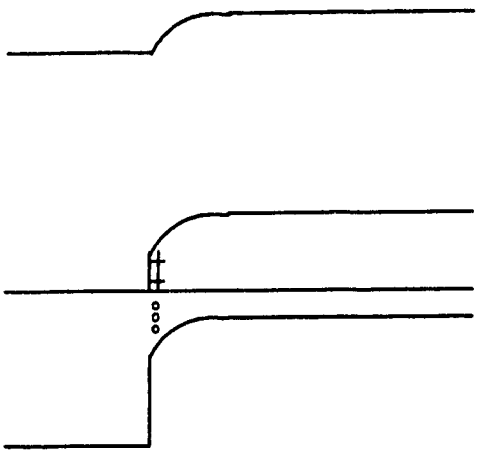


Fig. 4.4(a)

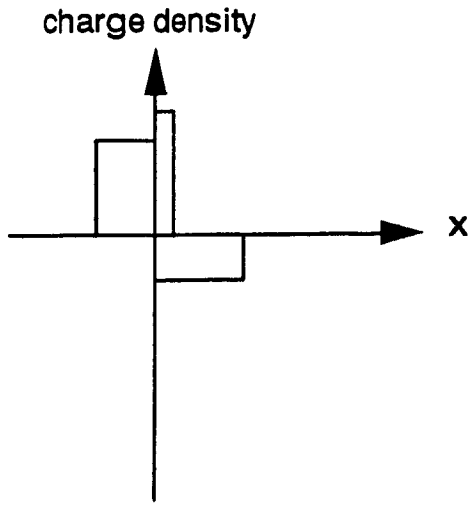


Fig. 4.4(b)

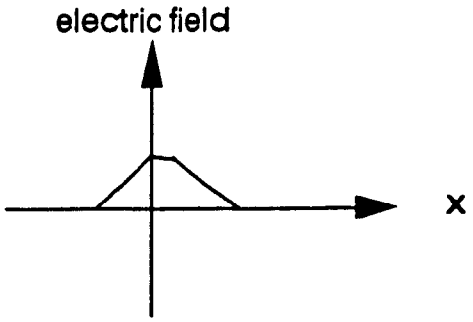


Fig. 4.4(c)

Fig. 4.4 The band diagram (a), charge distribution (b) and electric field distribution (c) of a junction with donor like interface states.

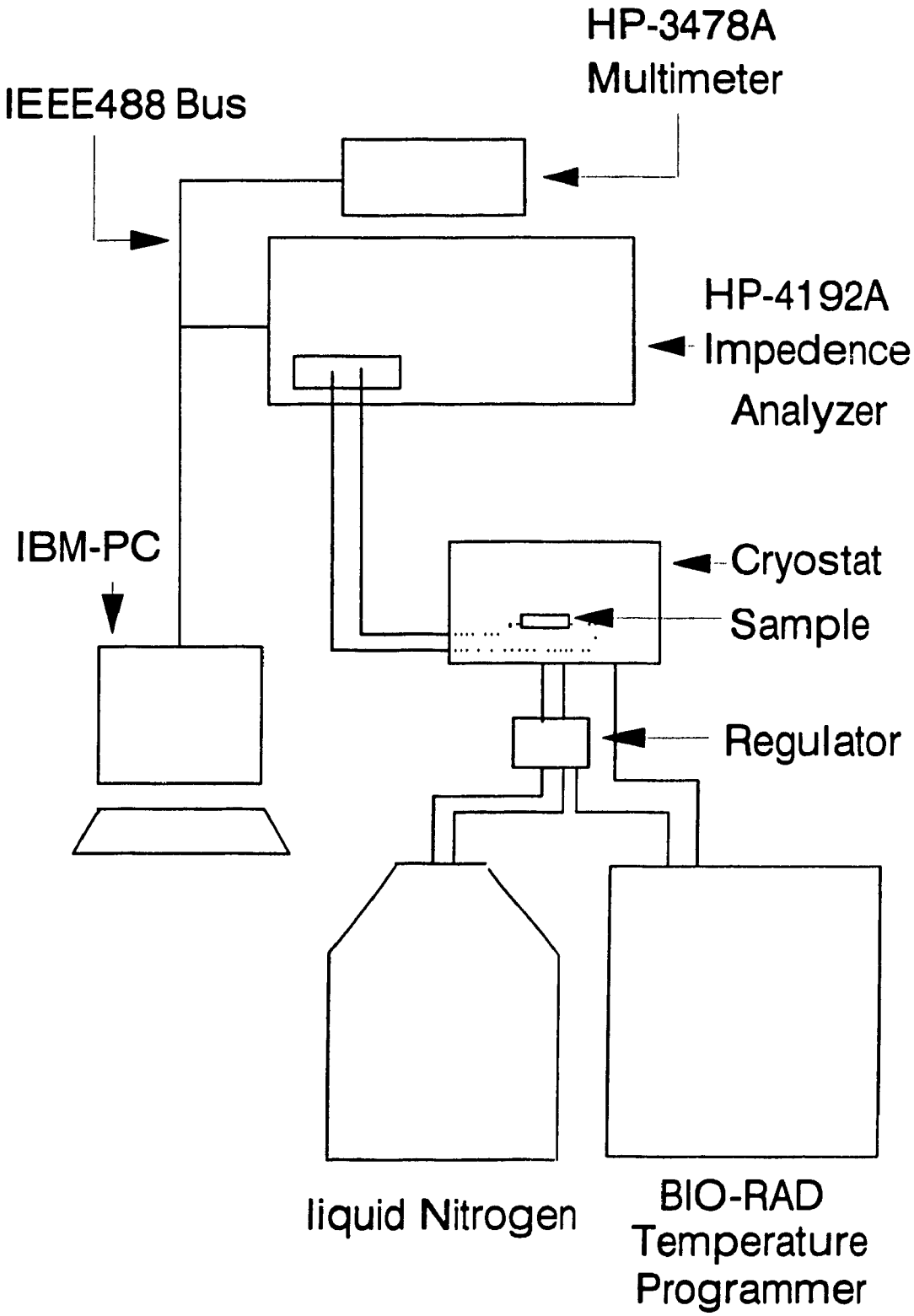


Fig. 4.5 Capacitance measurement setup.

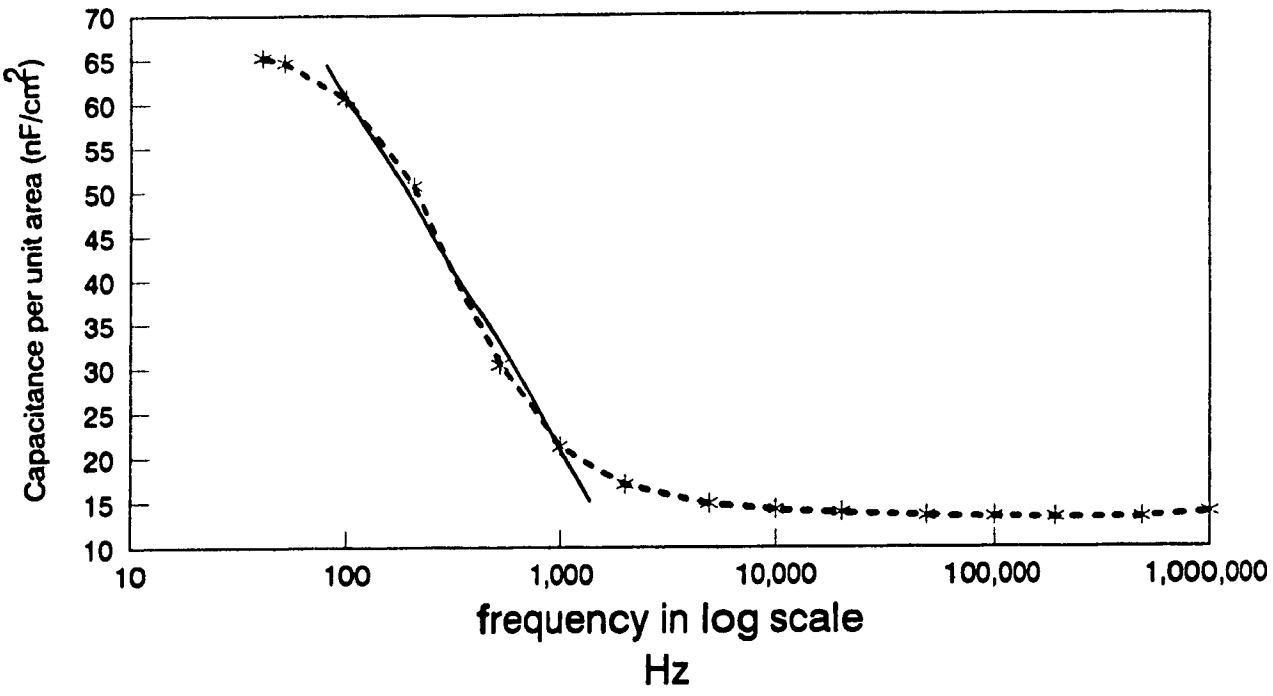


Fig. 4.6 Capacitance per unit area vs frequency of a typical CdS/p Si heterojunction cell.

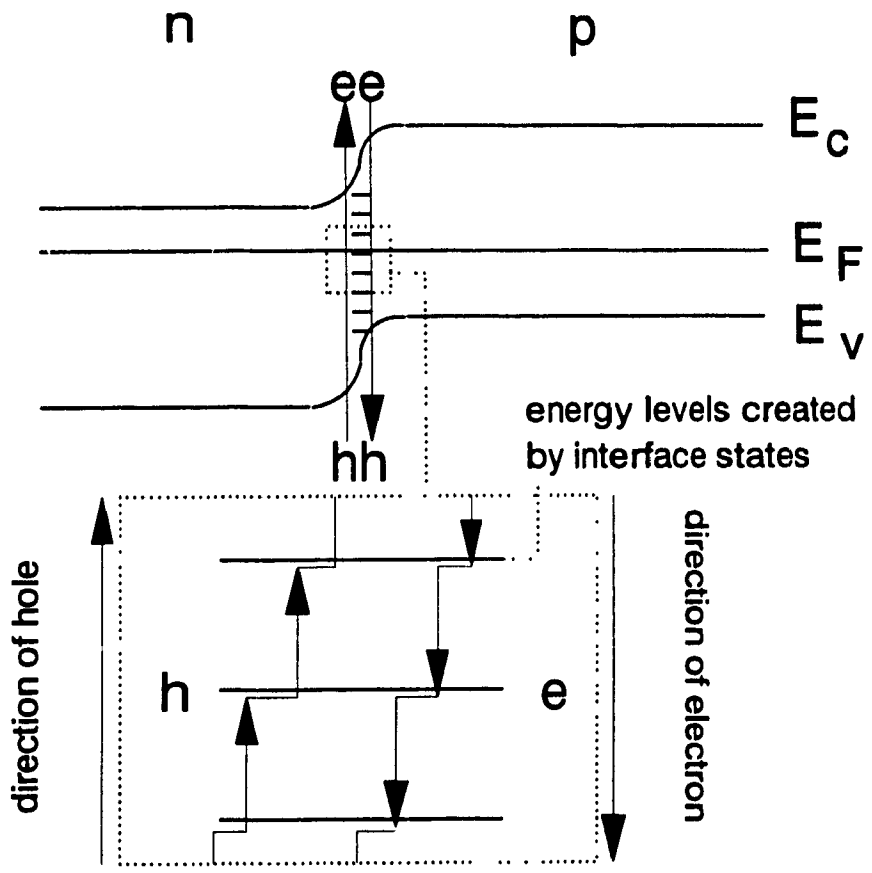


Fig. 4.7(a) Electron-hole pair recombination through energy levels created by interface states.

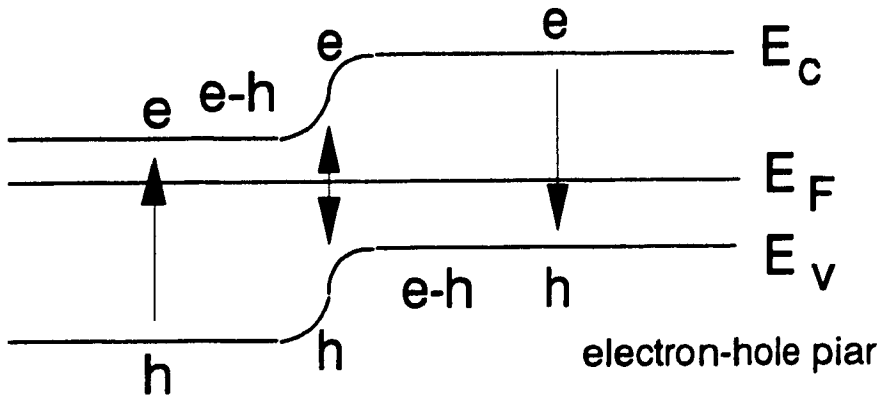


Fig. 4.7(b) Electron-hole pair recombination through band to band emission.

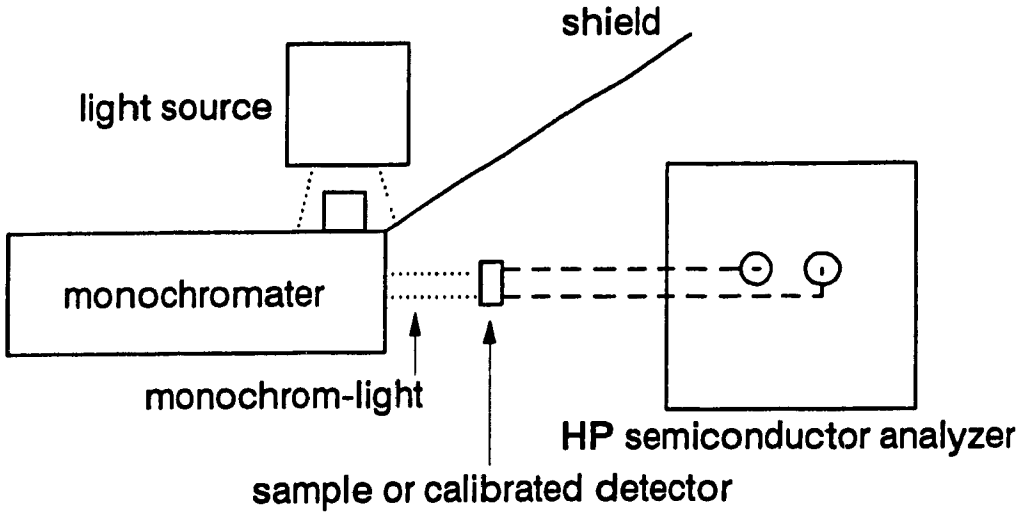


Fig. 4.8(a) Experimental arrangement for quantum efficiency measurement.

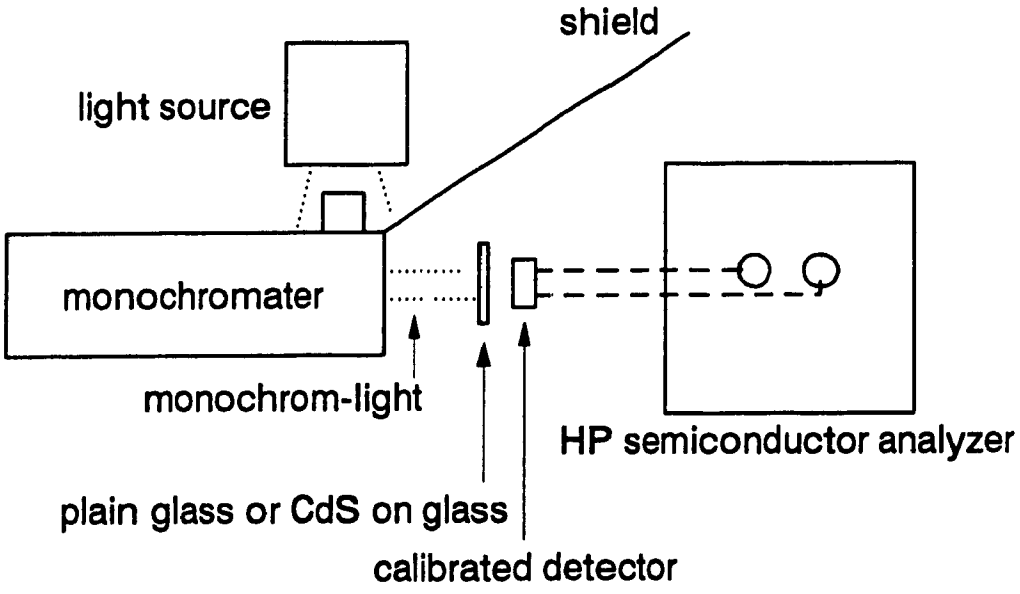


Fig. 4.8(b) Experimental arrangement for optical transmission measurement.

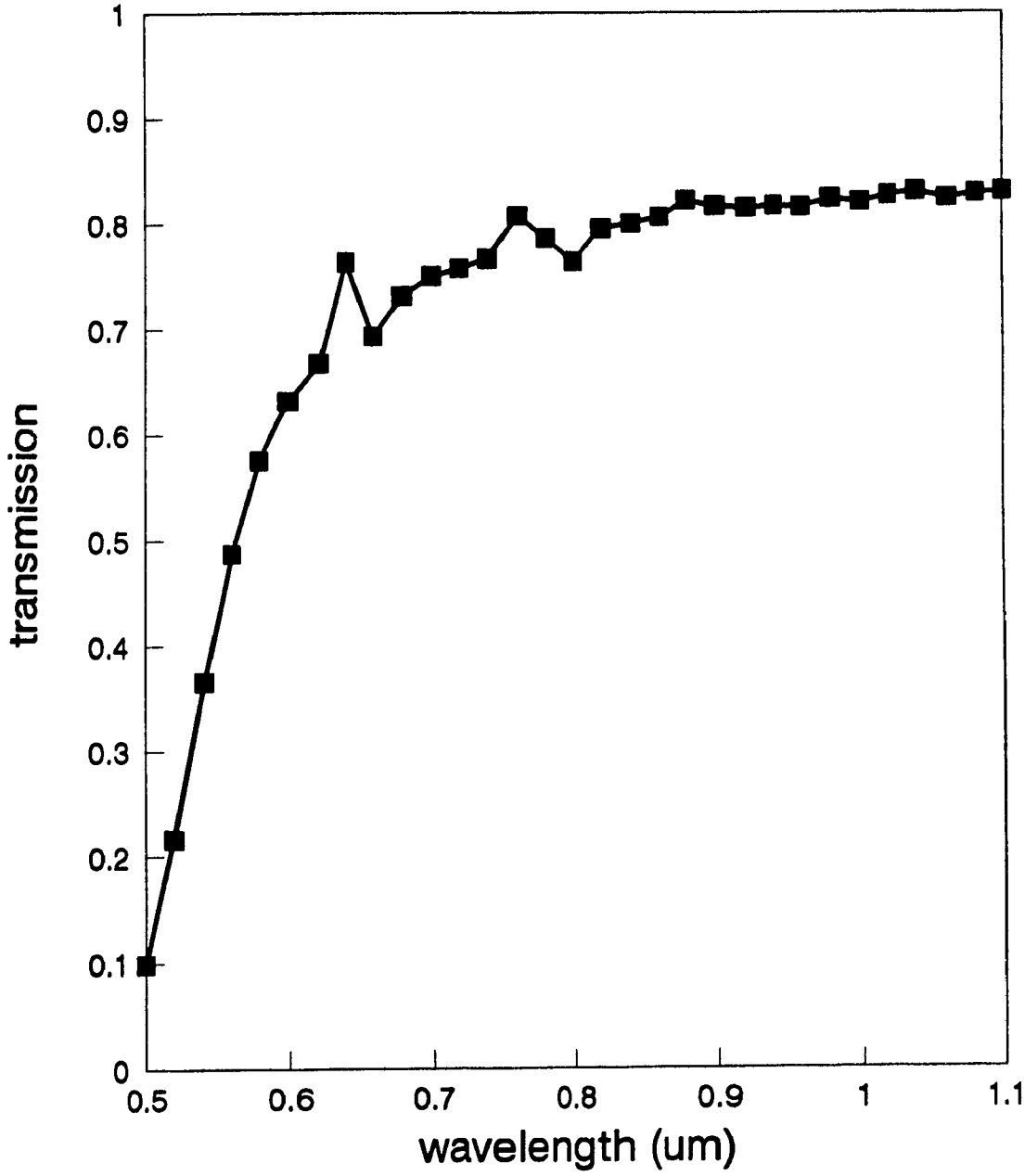


Fig. 4.9 Results of optical transmission of a CdS film used for heterojunction cells.

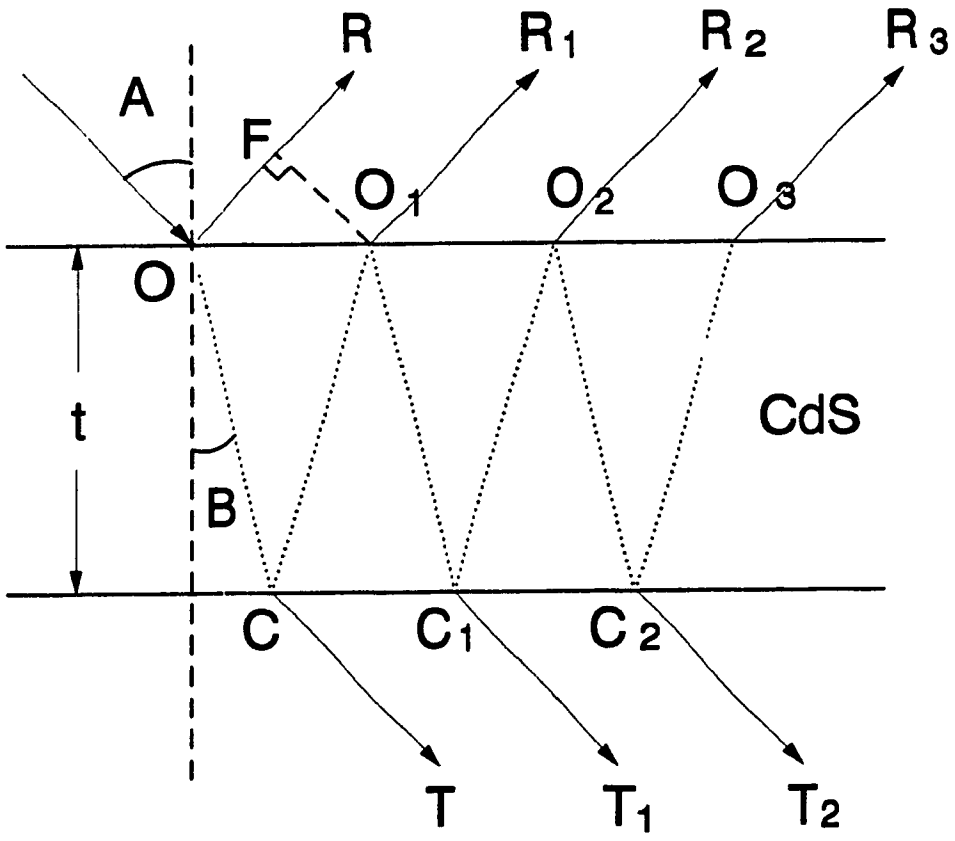


Fig. 4.10 Interference of light in the CdS thin film.

Chapter 5

Band Diagrams

Band diagrams of n-p Si, CdS/p Si , CdS/n Si, and CdS/n-p Si cells are constructed in this chapter and the diagrams will be compared to the experimental results

5.1 Parameters Needed to Construct a Band Diagram

The ratio of the depletion widths at two sides of the junction is inversely proportional to the ratio of the its doping concentrations, i.e.,

$$\frac{x_{n\text{-}Si,CdS}}{x_{p\text{-}Si}} \propto \frac{N_{p\text{-}Si}}{N_{n\text{-}Si,CdS}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.1)$$

where x is the depletion width and N is the doping concentration. In this work, the n-p homojunctions are assumed to be one-sided junction since the heavily doped diffused layers (10^{19} cm^{-3}) are shallow. The CdS on Si cells are also one-sided junction since the doping concentration of CdS (10^{19} cm^{-3}) is much greater than that of Si (10^{15} cm^{-3}) If the depletion region is predominantly on one side (i.e. on Si side), the relationship between junction capacitance and applied voltage is,

$$\frac{1}{C^2} = \frac{2}{qA^2\epsilon N}\frac{V_{bi}-V-kT}{q} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.2)$$

where V is the applied voltage, V_{bi} is the built-in potential of the device, A is the junction

area, ε is the permittivity of the Si and N is the net density of donors or acceptors in the Si. By plotting ($1/C^2$) vs V and extrapolating the straight line portion to its intercept with the abscissa, one obtains an apparent V_{bi},

$$V = V_{bi} - \frac{kT}{q} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.3)$$

Since kT/q is equal to 0.025 eV which is small at room temperature, it is safe to say that,

$$V \approx V_{bi} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.4)$$

In addition, the density of the dopants can be obtained from the slope, i.e.,

$$N = -\left(\frac{2}{qA^2\epsilon}\right)\left(\frac{d}{dV}\frac{1}{C^2}\right)^{-1} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.5)$$

For the case of heterojunction cells, the plot usually consisted of two regions, one from slight reverse to forward bias (shallow region, near the depletion region), and the other from slight reverse to large reverse bias (deep region). The reason for this is that the bias voltage affected the charging of the interface states which altered the junction barrier This phenomenon will not occur in a homojunction solar cell which has less interface states ($<10^9$ $eV^{-1}cm^{-2}$). As a result, extrapolating the large reverse bias region will deduce the V_{bi} with less interface state charging effect. On the other hand, the slight reverse to forward region will deduce the doping concentration near the junction with interface state charging effect In order to construct an ideal band diagram, the large reverse region is considered. Afterwards, the band diagram with interface states will be considered.

Again, it has been mentioned at the end of the **C-F measurements** section (section

4.2.5) that as the bias voltage becomes more forward, the effect of interface states on capacitance value is larger Therefore, the slope at large reverse bias is chosen in order to obtain the bulk impurity concentration.

5.2 Band Diagrams of Homojunctions

For the case of n-p Si cell, since there is a shallow n+ layer, which is about 0 05 to 0.2 um, on top of the p wafer, the n-p Si cell can be considered as a one-sided junction, i e. the V_{bi} and the depletion width, x_j, are in the p side The x_j can be deduced from the value of capacitance at zero bias.

$$x_j = \frac{K\epsilon_o}{C(0V)} * area \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5.6)$$

here ϵ_0 is the permittivity of free space ($8\ 85 \times 10^{-14}$ Fcm^{-1}), K is the dielectric constant of Si (11.8) and C(0V) is the capacitance at zero bias.

The diffusion is approximated by Gaussian distribution [3.2] and the profile is shown in Fig. 5.1. If the diffused layer is shallow and the dopant concentration is much greater than that of the back ground concentration, it is safe to assume that the junction is abrupt and the concentration of the diffused layer is equal to the dopant concentration

For the concentration larger than about 10^{18} cm^{-3}, a degenerate semiconductor is expected and the Fermi level can be approximately located at the conduction band edge. For a substrate with the concentration of the n+ layer less than 10^{18} cm^{-3}, the location of the Fermi level is found by the equation,

$$n=n_i\exp\left(\frac{E_F-E_i}{kT}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.7)$$

where n_i is the intrinsic carrier concentration of Si (~10^{10} cm^{-3} at room temperature), n is the carrier concentration of the semiconductor, E_F and E_i are the Fermi level and mid-level of band gap, respectively. kT is the thermal energy (~0 025 eV at room temperature).

The theoretical V_{bi} and depletion width, x_j, for the homojunction can be computed by the equations,

$$V_{bi}=\frac{kT}{q}\ln\left(\frac{N_D N_A}{n_i^2}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.8)$$

$$x_j=\left(\frac{2K\epsilon_o V_{bi}}{q}\frac{N_D}{N_A(N_A+N_D)}\right)^{1/2} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.9)$$

where N_D and N_A are the total numbers of donor and acceptor (atoms/cm^3), respectively.

5.3 Band Diagrams of Heterojunctions

Anderson model [5.1] is employed for heterojunction band diagram construction. A sample energy-band diagram of n-p heterojunction at equilibrium is shown in Fig 5.2(a) with θ and ϕ equal to electron affinities and work functions, respectively. Since there are band discontinuities in heterojunctions, more equations are involved than homojunction. For CdS/p Si cells, C-V measurements on the cells obtain most of the parameters, such as E_F, V_{bi}, N_A and x_j. Hall Effect measurements can yield impurity

concentration of CdS. Since CdS side is degenerated, it is assumed that the Fermi level is at the conduction band edge. A CdS/p-Si heterojunction band diagram model based on Anderson model is shown in Fig. 5.2(b), it is obvious that,

$$\Delta E_C = Eg_{Si} - qV_{bi} - (E_{F_{Si}} - E_{V_{Si}}) \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.10)$$

or simply,

$$\Delta E_c = \chi_{CdS} - \chi_{Si} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.11)$$

where

$$(E_{F_{Si}} - E_{V_{Si}}) = kT * \ln\frac{N_V}{N} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.12)$$

where N_v is the effective density of valence band states and is equal to $2.5\times10^{19}(m_p/m_o)^{3/2}(T/300)^{3/2}$ cm^{-3} [5 2] and N is doping concentration m_p/m_o is the ratio of the effective mass of hole to the rest mass of electron By the Anderson model, ΔE_c is also simply $\Delta\chi$.

The difference between the work functions is the total V_{bi} which is equal to V_1+V_2. V_1 and V_2 are the contact potentials at the n and p sides, respectively The distribution of this voltage on each side of the semiconductor is inversely proportional to its concentration, i.e

$$\frac{V_1}{V_2} = \frac{N_{A2}\epsilon_2}{N_{D1}\epsilon_1} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.13)$$

where ε_1 and N_{D1} are the dielectric constant and impurity concentration of semiconductor 1. ε_2 and N_{A2} are the ones of semiconductor 2.

The measured V_{bi} can be compared to the theoretical value. The measured x_j can be compared to the theoretical value from the equation,

$$x_{Si}=\sqrt{\frac{2N_{D_{CdS}}\epsilon_{Si}\epsilon_{CdS}V_{bi}}{qN_{A_{Si}}(\epsilon_{CdS}N_{D_{CdS}}+\epsilon_{Si}N_{A_{Si}})}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5.14)$$

where ε_{Si} and ε_{CdS} are the dielectric constants of Si and CdS, respectively. N_{ASi} and N_{DCdS} are the impurity concentrations at the Si and CdS sides

Since the doping concentration of CdS is 4 decades larger than that of Si, by equations (5 13) and (5 14), it is obvious that the amount of band bending V and depletion width are negligible at the heavily doped side (CdS) compared to the Si side. Therefore, an isotype junction is assumed.

The theoretical band diagrams of n-p Si and CdS/p-Si are in Fig. 5.3(a) and 5.3(b), respectively

5.4 Band Diagrams of n+/n Junctions

For CdS/n Si cells, a rough idea of how the E_C and E_V bend at two sides has to be known prior to C-V measurements in order to understand the $1/C^2$ vs V curve and extract data from it. By using the specifications of the impurity concentration of the n wafer and calculating that of the CdS film using Hall effect measurements, the approximate ratio of the depletion widths at two sides can be obtained,

$$\frac{x_{CdS}}{x_{Si}} \approx \frac{N_{Si}}{N_{CdS}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5.15)$$

If $x_{CdS}/x_{Si}<<1$, this n+/n junction can be approximate as a Schottky junction and V_{bi}, experimental N_A, x_{Si} can be obtained from C-V measurements If the ratio is within the order of 0.1 to 10, the band bending at the CdS side is comparable to that of n-Si side Two possible cases are shown in Fig. 5 4 For the case in Fig. 5 4(a), the C-V curve is similar to that of n-p homojunctions or CdS/p-Si heterojunctions and the measurement will give V_{bi} and depletion width. However, for the case in Fig. 5 4(b), the C-V curve consists of two straight line sections (Fig 5 5) with opposite slope and the extrapolation of the lines to their intercepts with the abscissa will give the two V_{bi} at the CdS and n-Si sides. x_{CdS} and x_{Si} can be obtained from the intercepts of the lines at C=0 and then use equation (5.6).

Moreover, photoresponse results also show how the band bendings are If $x_{CdS}/x_{Si}<<1$ or $x_{CdS}/x_{Si}\sim1$ with the band diagram as shown in Fig. 5 4(a), the polarity of the photocurrent will not change because the electric field at the depletion is unidirectional. On the other hand, if the band bending is like Fig. 5.4(b), the polarity will switch somewhere near the photon energy equal to the energy gap of semiconductor which is facing the incident light. When the photon energy is larger than that of the illuminated semiconductor energy gap, electron-hole pairs are excited and the carriers are swept by the electric field at the illuminated side, on the other hand, if the photon energy is less than that of the illuminated semiconductor energy side, the photons are transparent to this semiconductor and no carriers are generated at this side The electric field at this side

plays no role When the photons reach the smaller energy gap semiconductor side, electron-hole pairs are excited and carriers are generated. These carriers are swept by the electric field at this side and since the polarity of the electric field at this side is opposite to that of the illuminated side (opposite band bending), the carriers are swept in an opposite direction Therefore, the polarity of the current is switched. The is illustrated in Fig 5 6

If the electron affinities, χ, of Si and CdS are taken as 4 eV and 4.5 eV [5.3], the only way to cause the conduction band of CdS to bend up in Fig. 5 4(b) is the Fermi level of Si located at least 0 5 eV below the conduction band edge. However, the substrate impurity concentration is roughly 10^{15} cm^{-3} and the Fermi level is about 0.2 eV below the conduction band Some reports show the result of having the band diagram of Fig. 5.4(b) with Fermi level of Si less than 0.5 eV from the conduction band edge [5.4]. The only reason to explain this phenomenon is χ for both semiconductors are different at the junction The operational definition of the electron affinity is that it is the amount of work needed to remove an electron from the bottom of the conduction band of a solid, just inside the solid, to a point outside the solid beyond the range of the image force This makes electron affinity data vulnerable to surface polarization effects and interface states, etc. In the presence of high density of interface states, χ can be very different from the reported values [5.5].

5.5 Band Diagrams of CdS/n-p Si Junctions

Since there are two band bendings in this structure, some predictions of the band diagrams are made here and these diagrams will be verified in next chapter The band diagram of CdS/n-p Si is predicted by combining the n-p Si and the CdS/n+ Si junctions With the n-layer highly doped, the band diagrams may look like Fig 5 7 Fig 5 7(a) is constructed followed the Anderson model, Fig 5 7(b) is possible if χ's are different from reported values. On the other hand, with n-layer lightly doped, the band diagram may look like Fig. 5.8(a) without interface state effect and this prediction is based on the Anderson model Fig 5.8(b) is a prediction with interface state effects and probably is the best band diagram for this CdS/n-p Si cell since no "spike" on the band diagram

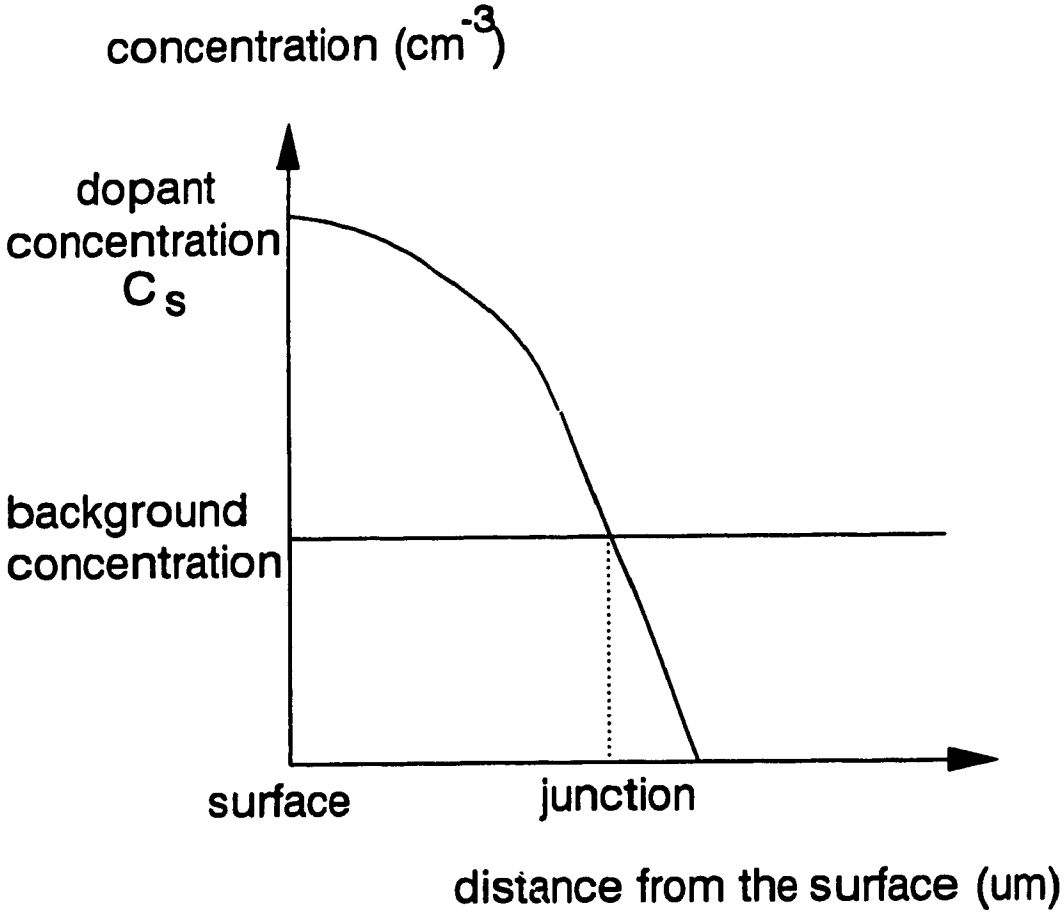


Fig. 5.1 The diffusion profile approximated by Gaussian distribution.

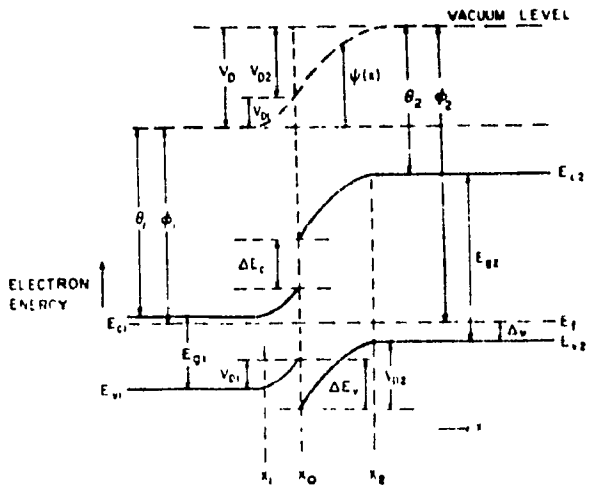


FIG. 2 Energy-band diagram of n-p heterojunction at equilibrium.

Fig. 5.2(a) Energy band diagram of n-p heterojunction at equilibrium.

(R.L.Anderson, Solid-State Electronics Pergamon Press, 5, P.342 Fig. 1, 1962)

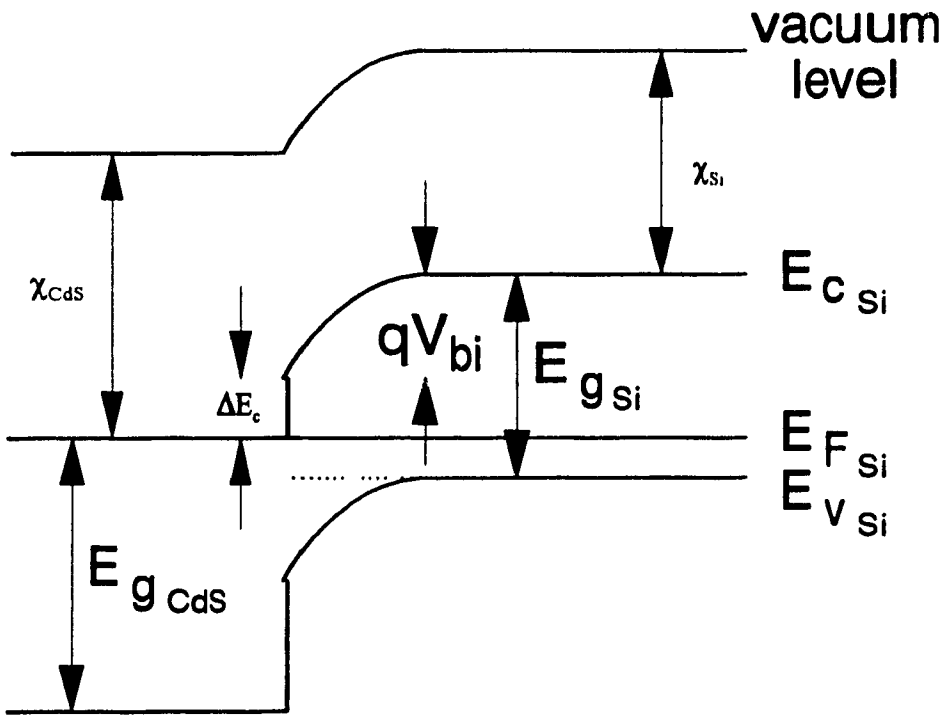


Fig. 5.2(b) Energy band diagram of CdS/p-Si heterojunction.

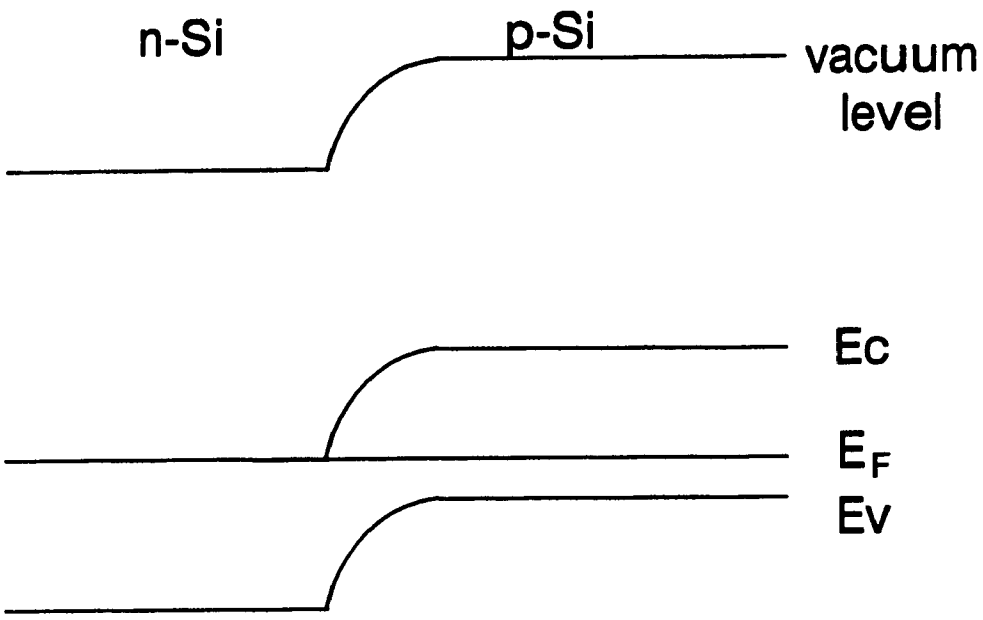


Fig. 5.3(a) The band diagram of n/p Si cell.

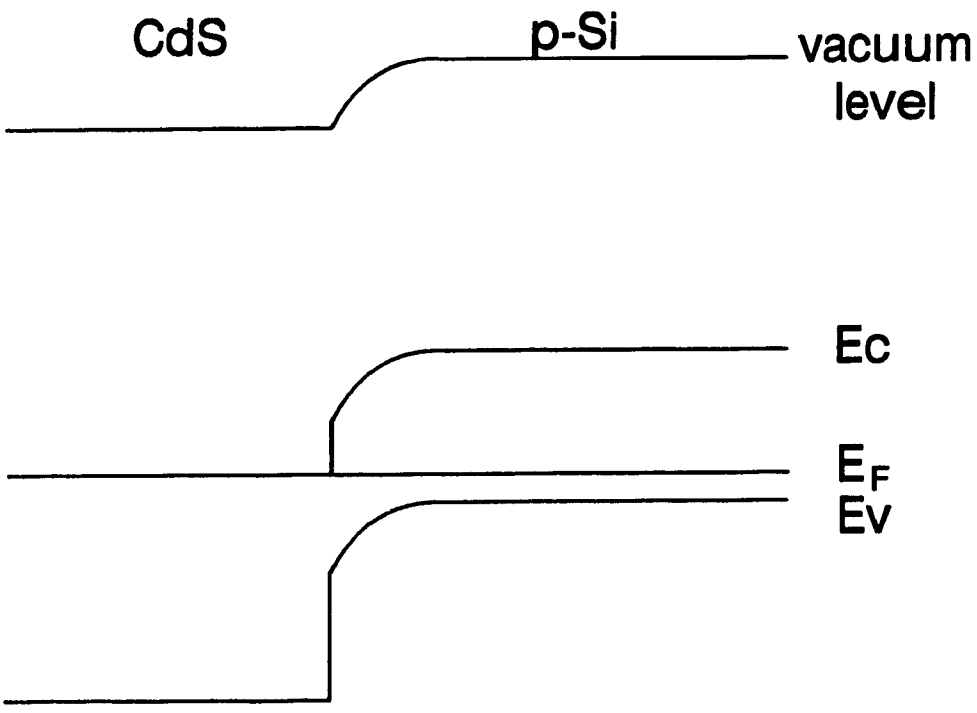


Fig. 5.3(b) The band diagram of CdS/p Si cell.

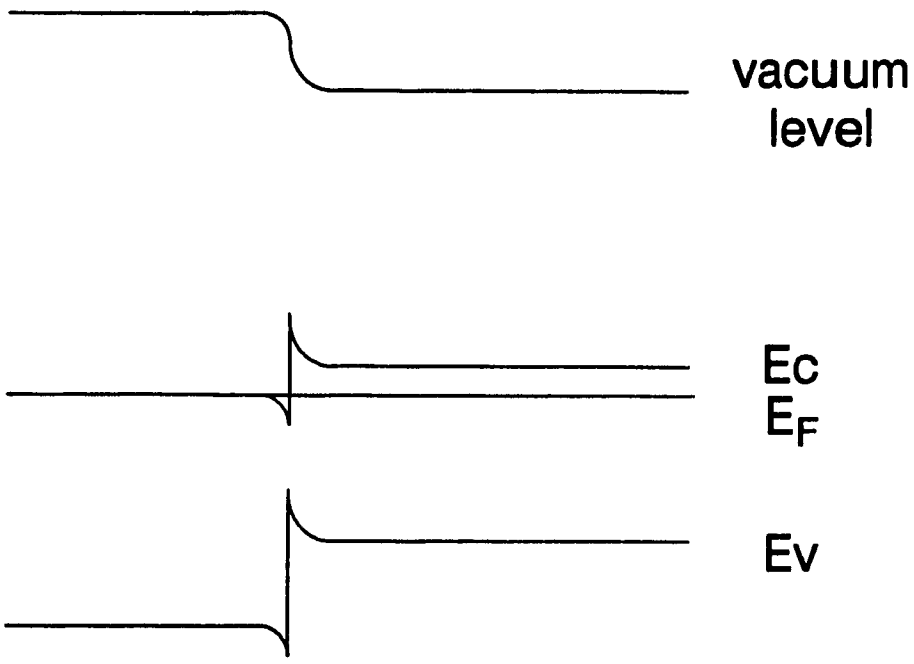


Fig. 5.4(a) Ideal n+/n band diagram (CdS/n Si).

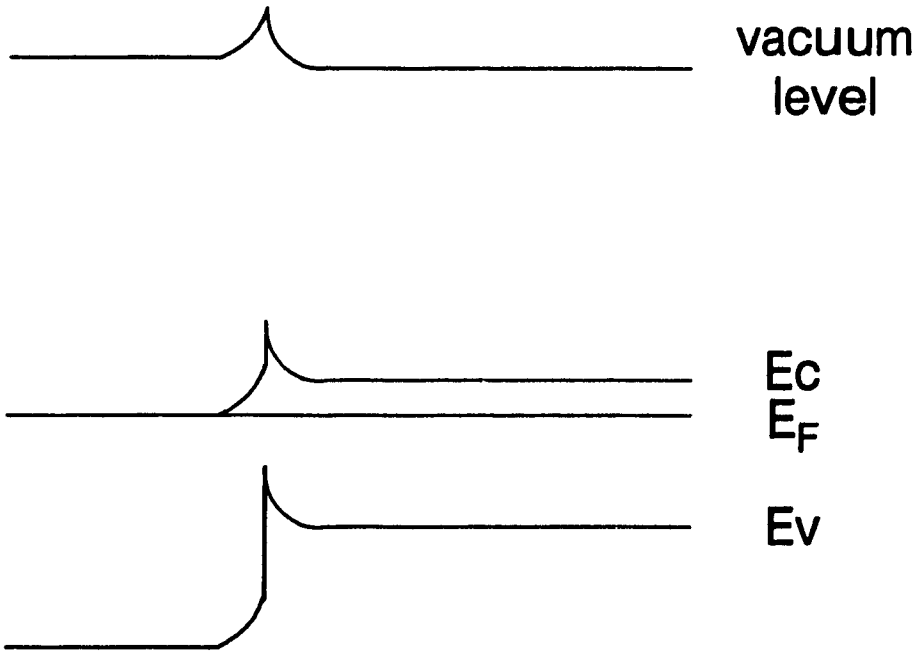


Fig. 5.4(b) Band diagram of an n+/n junction with interface state effect.

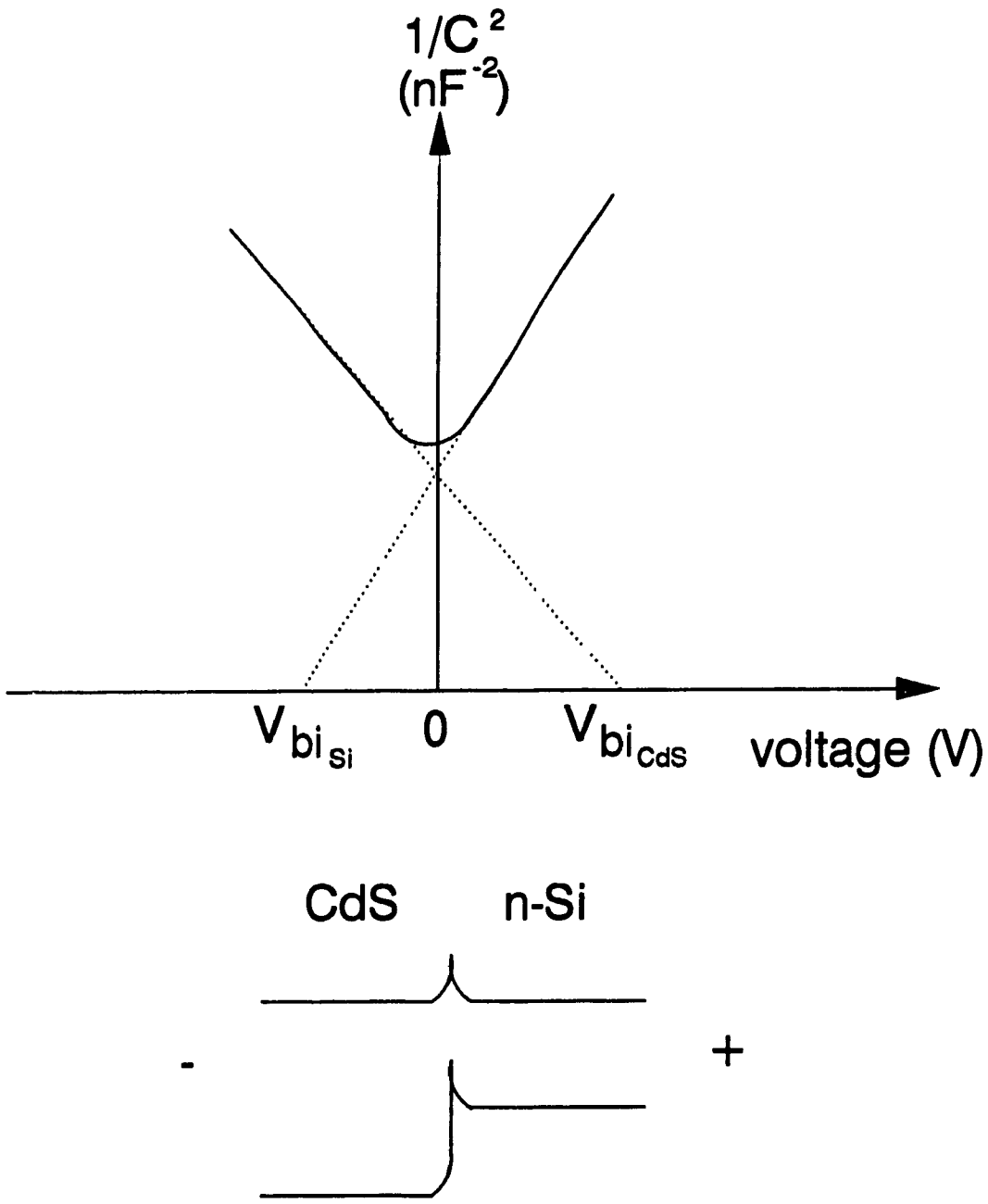


Fig. 5.5 A $1/C^2$ vs V measurement of an n-n heterojunction with n-Si as positive side and CdS as negative side.

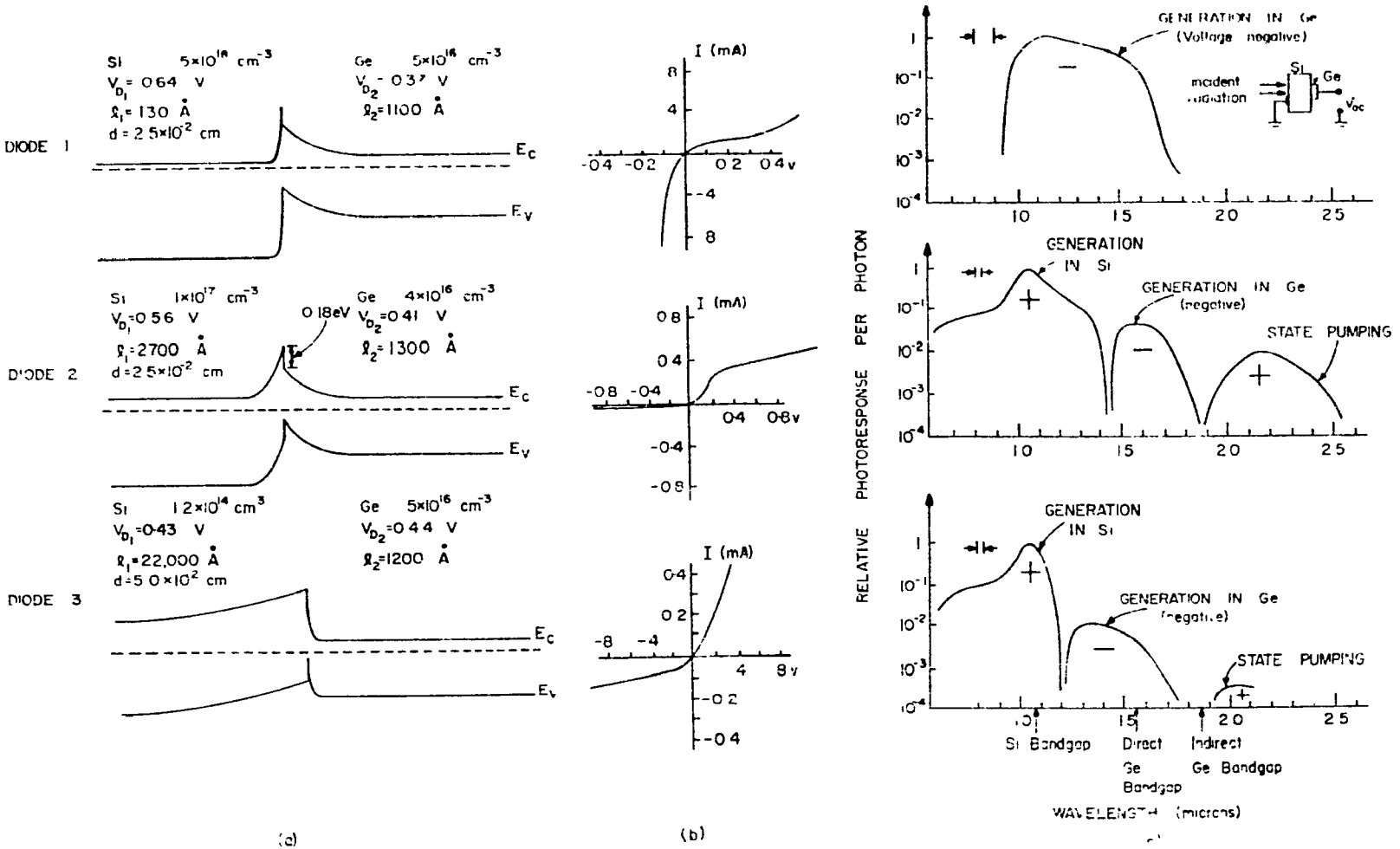


FIG. 1. Characteristics of *n* Ge–*n* Si Diodes (3 doping types) at room temperature; (*a*) Equilibrium band diagrams, (*b*) I-V characteristics, (*c*) Relative photoresponse per incident photon.

Fig. 5.6

(J.P.Donnelly & A.G.Milnes, Solid-State Electronics Pergamon Press, 9, P.175 Fig. 1, 1966)

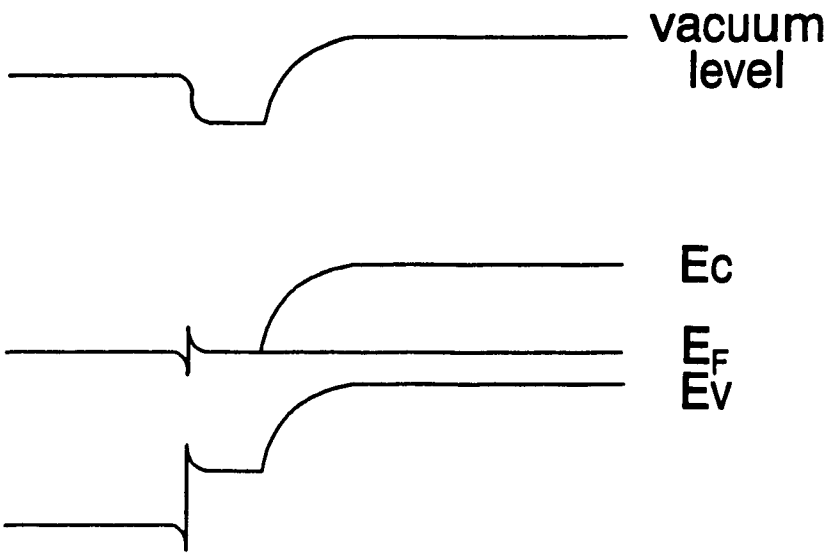


Fig. 5.7(a) Band diagram without interface states at the CdS/n junction.

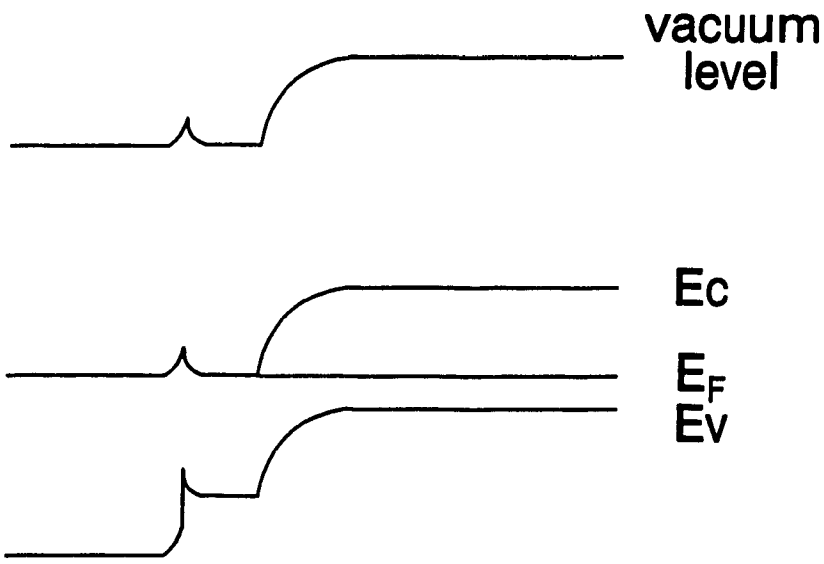


Fig. 5.7(b) Band diagram with interface at the CdS/n junction.

note : The middle n layers are heavily doped in both figures.

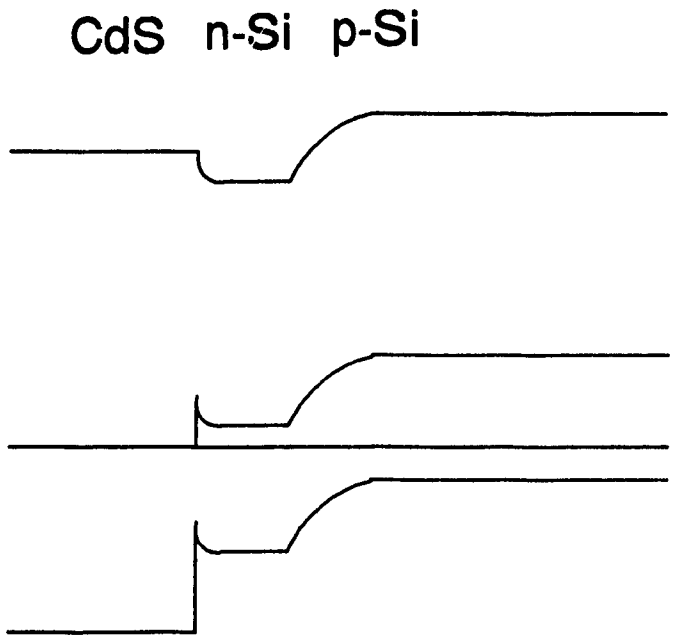


Fig. 5.8(a) Possible band diagram of a CdS/n-p Si cell.

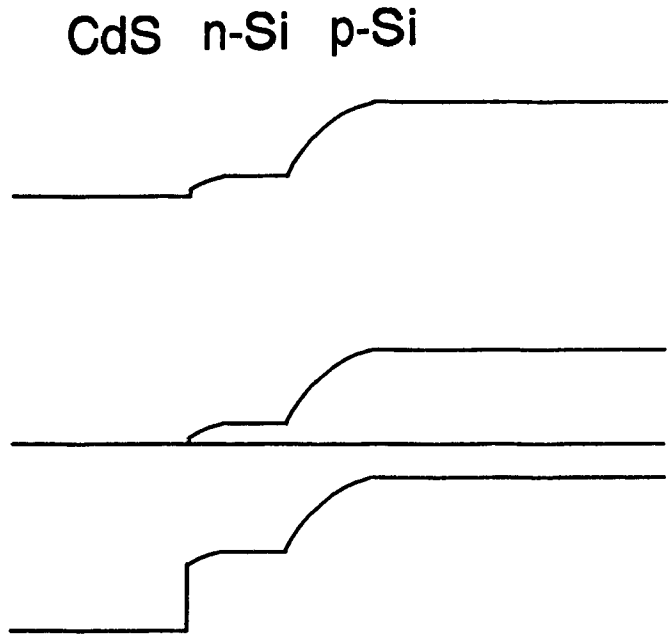


Fig. 5.8(b) Possible band diagram of a CdS/n-p Si cell.

note : The middle n layers are lightly doped in both figures.

Chapter 6

Results and Discussion

6.1 Introduction

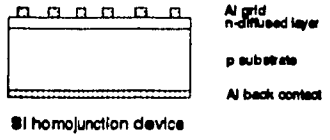
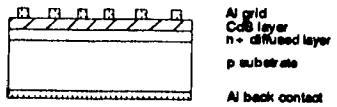
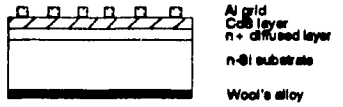
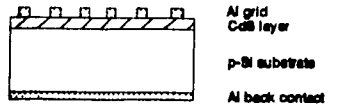
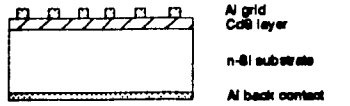
First of all, n-p Si cells are studied and the band diagrams are given. Then, CdS/n-Si cells and CdS/p-Si cells are analyzed, and the results are compared to that of CdS/n-p Si cells. Effects of interfacial state are considered at the final section

The performance of different cells are compared using a simulated AM1 light source. However, the spectrum and intensity of this light source are different from the real AM1 condition. Therefore, the following results of cells performance can be used to compare among themselves only and this is not necessary the real performance under AM1.

6.2 Fabrication Conditions of Cells

Fourteen samples of n-p Si, CdS/n-Si, CdS/n-p Si and CdS/p-Si cells are examined and the fabrication conditions are listed in **Table 6.1**:

Table 6.1 Fabrication conditions of Si substrates for CdS/Si cell fabrication

Sample No.	Diffusion Condition
p-type 162 p-type 168  SI homojunction device	10 minutes at 850°C $N_s=1x10^{19}cm^{-3}$ 10 minutes at 900°C $N_s=5x10^{17}cm^{-3}$
p-type 163[a] 164[b], 165[c] p-type 169[a] 170[b], 171[c]  CdS/SI hetero-homojunction device	10 minutes at 850°C $N_s=1x10^{19}cm^{-3}$ 10 minutes at 900°C $N_s=5x10^{17}cm^{-3}$
n-type 173 n-type 175  CdS/n+ SI junction device	10 minutes at 850°C $N_s=1x10^{19}cm^{-3}$ 10 minutes at 900°C $N_s=5x10^{17}cm^{-3}$
p-type 178[a] 166[b], 167[c]  CdS/p-SI heterojunction device	no diffusion
n-type 180  CdS/n-SI heterojunction device	no diffusion

note:

(i) properties of the p-type and n-type wafers are listed in appendix I.

(ii) the superscripts a, b and c are corresponding to three different CdS evaporations on

the samples.

a : N_D=4.7x10^{18} cm^{-3}, thickness=1.8 um, ρ=2.2x10^{-2} ohm-cm

b : N_D=8.6x10^{18} cm^{-3}, thickness=2.4 um, ρ=3.4x10^{-3} ohm-cm

c : N_D=9.5x10^{18} cm^{-3}, thickness=2.4 um, ρ=6.8x10^{-3} ohm-cm

(iii) a picture of CdS fiim of b evaporation is taken by scanning electron microscope (S.E M.) and is shown in Fig. 6.1.

(iV) the junction depth of sample 162 is 0.010 um, 168 is 0.018 um.

6 3.1 Band Diagrams of n-p Si Junctions

From the C-V measurements (Fig. 6.2), the V_{bi}, impurity concentrations and depletion widths of sample 162 and 168 by using equations (5.3)-(5.6) are listed in the following table:

Table 6.2 Experimental parameters of n-p Si cells.

sample no.	V_{bi} (V)	substrate impurity concentration(cm^{-3})	depletion width(um)
162	0.75	3.8x10^{15}	0.52
168	0 62	4.2x10^{15}	0.42

By using equations (5.8), (5.9) and (5.13), the theoretical values are (N_A=1x10^{15} cm^{-3} is used):

Table 6.3 Theoretical parameters of n-p Si cells

sample no.	V_{bi} (V)	depletion width (um)
162	0.72	0.5
168	0.65	0 45

The locations of the Fermi level of samples 162 and 168 are obtained by using equation (5.7) and are indicated in the band diagrams of 162 and 168 in Fig 6.3 Data in Table 6.2 is used. If the energy band gap of Si is assumed to be 1 1 eV, the values of $V_{bi} + (E_F\text{-}E_v)_{p\text{-}Si} + (E_c\text{-}E_F)_{n\text{-}Si}$ of the experimental data are less than 0.06 eV away from 1.1 eV. As a result, the experimental data is used to construct the band diagrams and these are the n-p band diagrams for n-p side of CdS/n-p samples.

The diffused junction depths are calculated by using equation (3.1) and the values are less than 0.015 um, so the junction depth contribution to the depletion width in either the experimental or theoretical results can be neglected

6.3.2 Performance Analysis of n-p Cells

The I-V characteristics and quantum efficiencies are shown in Fig. 6.4, which consists dark and illuminated I-V, and in Fig. 6.5, respectively. Parameters of the n-p cells are listed in the following table with η representing the efficiencies at AM1.

Table 6.4 Performance of the n-p Si cells.

Sample No.	V_{oc} (V)	J_{sc} (mA/cm^2)	F F	V_{shift} (V)	R_S (Ω)	n	η (%)
162	0.47	10 52	0 55	0.045	4	2.7	3.4
168	0 48	12.62	0.56	0.05	4	2.5	4.2

The performance of a Radio Shack commercial silicon solar cell is in the following **Table 6.5**:

Table 6.5
The performance of a commercial cell.

V_{oc} (V)	I_{sc} (mA)	η (%)
0.53	37	13.6

The V_{oc} values of both cells are satisfactory since the wafer is thick (~500 um) so that the V_{oc} cannot be improved by back surface field which is generated by a diffused p+ layer at the back of the p-Si wafer. Fig. 6.6 shows an energy band diagram of a back surface field device If W_p is comparable to or less than the diffusion length (minority carrier diffusion length of p-Si is about 100 um) of carriers in region 1, then some of the electrons that would have been lost at the back surface cross the p-n junction boundary instead, enhancing the short circuit current. Since the loss of electrons at the back side

is reduced, the dark current I_o is lowered. By equation (2.1), V_{oc} is improved.

The currents are considerably small compared to the best Si cells because of the relatively large series resistance and insufficiency of fine fingers on the front side The effects of R_S on the performance of cells are shown in Fig 6 7 [6 1] Ideal solar cell series resistances are below 1 Ω/cm^2 The main effects of series resistance to the performance of solar cells are that R_S decreases the photocurrent generated by the cells and lowers the fill factors The high series resistances of the two cells can be reduced by modifying the front grid contacts, i.e more fine lines The ideal width of the each finger is about 50 um to 100 um and the distance between fingers is about 100 um More current can also be collected at this configuration However, simple metal evaporation cannot give this fine line contact For this purpose, photolithography is needed However, it cannot be used on CdS-Si cells since the CdS layers will be affected during photoresist process and etching For experimental purpose, in order to compare the performance of the cells with and without CdS layers, the evaporated eight finger front grid contacts are used. In addition, a "dead" layer, which is a thin region adjacent to the front surface with very short lifetime resulting of the diffusion process, extends over a fraction of the diffused top region may form and cause the recombination of electron hole pairs or carriers loss near the surfaces If recombination mechanism is dominant, n is greater than 1 (~2, see section 4.1) This is also the reason for large values of ideality factors. The voltage shifts are small in both cells and it is expected from homojunction cells since densities of interfacial states are low.

6.4 Band Diagrams of CdS/n-Si Junctions

For the case of n-n junctions, the I-V characteristics have to be considered first before going to C-V measurements because the injected currents may reach 1 or 2 mA in a few millivolt forward or reverse bias When one tries to bias the cell to -0 5 V for C-V measurements a huge current may be created. The reasons why high currents are avoided are because it reduces the cells shunt resistance and the values of capacitance measurements are not accurate In addition, such high current may damage the cells

The samples 173, 175 and 180 are fabricated in a form CdS/n Si and their dark and illuminated I-V curves are in Fig 6.8. Since sample 173 and 180 have large current at reverse bias, there is no point to carry out C-V measurement on these two samples The C-V characteristics is obtained only for the sample 175. The properties of the cells are listed in **Table 6.1** The similarity of the three cells is that they all have a highly doped CdS layer and the only difference is the impurity concentrations on the substrate surfaces

Table 6.5
Substrate surface impurity concentrations
of the CdS/n Si cells

Sample No	Substrate surface doping concentration (cm^{-3})
173	$1x10^{19}$
175	$5x10^{17}$
180	$1x10^{15}$

By looking at Fig. 6.8, the CdS/n-Si junctions are not like Fig. 5 4(a) but Fig. 5.4(b) in **Chapter 5** and this is similar to the result of Si-Ge [6 2] in Fig 5 6. An I-V characteristic of a simple back to back diode is plotted in Fig. 6.9 and it is similar to any of the I-V in Fig 6 8 However, they are not the same. Fig 6 8 is I-V of samples of heterojunctions and because of the different electron affinities of the materials and doping concentrations, the I-V characteristics behave differently from a simple back to back diode. Moreover, heterojunctions may give photovoltage and current [5 4, 6 2] These cells configurations are similar to n-Ge - n-Si cells [6.2] Moreover, the C-V measurements of sample 175 in Fig 6 10 further confirm the shape of the bending However, no impurity concentration or built-in potential information can be extracted from the curve since only a short curve is acquired

Equation (5.18) can be used to approximate the depletion widths of three n-n junction samples, since the sample 173 is heavily doped on both sides and the depletion widths are expected to be very narrow The samples 175 and 180 can be approximated as metal-semiconductor contacts

Table 6.6
Approximate depletion widths
of the three n-n samples

Sample No.	173	175	180
CdS side (um)	0.006	0 002	0 0001
Si side (um)	0 005	0.03	0 48

note

(i) ϵ_{Si} and ϵ_{CdS} are taken as 11 8 and 8 5, respectively

(ii) χ_{Si} and χ_{CdS} are taken as 4 eV and 4.5 eV, respectively.

(iii) V_{bi}'s are taken as $\Delta\chi$ minus (E_C-E_F) on the Si side.

(iv) V_{bi} of sample 175 is 0 34 V, sample 180 is 0 18 V and sample 173 is 0.5 V shared by both sides

By using the above data, the band diagrams of the three n-n samples are constructed and shown on Fig 6 11 The depletion width on both sides of sample 173 is so small and can be neglected When the depletion width is small, carriers can tunnel through the barrier For samples 175 and 180, as the samples are biased to forward, Schottky junction behaviour effect is observed The samples are like a Schottky junction with Si as n side Therefore, when positive voltage is applied with respect to Si side, rectifying effect is observed The sample 180 also shows rectifying behaviour but it turns on at a lower voltage This is because the barrier height on the Si side is smaller than that of sample 175 The high leakage current is due to the small depletion width caused by reverse bias and tunnelling takes place

The band diagrams in Fig 6 11 are confirmed by the three sets of I-V curves of the samples 173, 175 and 178, the C-V curve of the sample 175 and the model of n-Ge - n-Si [6 2] shown in Fig 5 6 No photoresponse is obtained from the three samples The possible reason is that the space charge regions are too narrow and this causes inadequacy of carriers collection For the sample 173, there is no considerable space charge region to collect electron hole pairs For the samples 175 and 180, slight photoresponses are

observed only at reverse bias, i.e. further bend down the conduction band edge of Si sides and it causes the electric field to increase

Since diffused substrates is used to simulate heavily doped n-type wafer, another barrier between the diffused layer and the original $1x10^{15}$ cm^{-3} substrate is formed However, the effect of this barrier does not show on the I-V measurements. The sample 173 clearly is a back-to-back n junction with comparable impurity concentration on both sides, the second barrier of the sample 175 is only 0 16 eV so that its effect is negligible

6.5.1 Band Diagrams of CdS/p-Si Junctions

The procedure to construct CdS/p-Si band diagrams is similar to that of n-p Si From C-V measurements shown in Fig. 6 12, the experimental data for samples 166, 167 and 178 are listed in the following table

Table 6.7
Experimental parameters of CdS/p-Si cells.

Sample No.	V_{bi} (V)	Substrate impurity concentration(cm^{-3})	depletion width(um)
166	0.45	$3\ 9x10^{15}$	0 4
167	0.5	$4.4x10^{15}$	0 4
178	0.6	$5.1x10^{15}$	0 41

However, by using equations (5.10) to (5.14), the theoretical V_{bi} values, which is obtained by knowing ΔE_c and the location of E_F on the Si side, and depletion widths are different from the experimental values,

Table 6.8
Theoretical parameters of CdS/p Si cells.

sample no	V_{bi} (V)	depletion width (um)
166	0.31	0.32
167	0 32	0.31
178	0 33	0.29

note . ΔE_c (or $\Delta\chi$, assuming Anderson model) is 0 5 eV, energy gap of Si is assumed to 1.1 eV, E_F-E_v on the Si side of the sample 166 is 0.29 eV, 167 is 0.28 eV, 178 is 0.27 eV.

The experimental V_{oc} are larger than expected. The only reason is that $\Delta\chi$ (or ΔE_c) is different from the reported data [5.3] due to interface states at the junction. The explanation is in section 5.4. Based on the experimental data, $\Delta\chi$ of the three CdS/p Si cells are listed in the following table :

Table 6.9
Experimental $\Delta\chi$ of the CdS/p-Si cells.

sample no	V_{bi} (V)	E_F-E_V (eV)	$\Delta\chi$ (eV)
166	0.45	0.29	0.36
167	0.5	0.28	0 32
178	0.6	0.27	0.23

The band diagrams are based on the experimental data are shown in Fig. 6 13.

6.5.2 Performance Analysis of CdS/p Si Cells

The I-V characteristics and quantum efficiencies for samples 166, 167 and 178 are shown in Fig. 6.14 and Fig. 6.15, respectively. The performances of the CdS/p-Si cells are listed in the following table :

Table 6.10
Performance of the CdS/p-Si cells.

Sample No	V_{oc} (V)	J_{sc} (mA/cm^2)	F F	V_{shift} (V)	R_S (Ω)	n	η (%)
166	0 39	15 8	0 44	0 03	4	4	3 4
167	0 34	16 7	0 54	0 08	6	2	3 8
178	0.32	15 7	0 64	0 03	4	1 3	4 7

note The area of the sample 178 is 0 6 cm^2 rather than 1 cm^2 for samples 166 and 167, the photocurrent generated is less

The V_{oc} of the three samples are reasonable for heterojunction cells because it is smaller than that of homojunction The reason is that V_{bi} of a heterojunction is smaller than that of a homojunction and V_{bi} is proportional to V_{oc} The higher currents compared to n-p homojunctions are due to that high energy photons can be absorbed within or very near the depletion region of the cells, leading to good high photo-response Moreover, since the window layer (CdS) is a wide energy gap material, photons with energy lower than the band gap of CdS (2 4 eV) is transparent to this layer, causing less electron-hole pairs excited in this layer, so that less carriers are generated near the surface and therefore electron-hole pair recombination loss due to surface recombination is reduced The lifetime of carriers in a heavily doped semiconductor (CdS here) is smaller and higher rate

electron-hole pair recombination is expected On the other hand, since extra photons in the energy range between 2 4 eV and 1 1 eV (band gap of Si) reach the space charge region, high photocurrents are expected The voltage shifts are considerably small It implies that the densities of interface states may be relatively low to cause a noticeable shift This will be analyzed in section 6 7 Comparing to Fig 6.5, the quantum efficiencies of CdS/p-Si in Fig 6.15 show a sharp-rise near the CdS band gap energy The band gap of CdS is 2.4 eV,

$$\lambda = \frac{1.24}{E_g} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (6.1)$$

λ, the wavelength corresponding to 2.4 eV, is called the cut off wavelength of CdS, i.e photons with wavelengths longer than this value are transparent to CdS In this case, λ is equal to 520 nm. Only the photons with wavelength longer than 520 nm can reach the space charge region on the Si side and excite electron-hole pairs. The photons with wavelength shorter than 520 nm are absorbed and lost in the CdS side The photoresponses are also relatively high compared to that of n-p cells

The series resistances of these CdS/p-Si cells are not expected to be as high as that of homojunctions since the low resistivity CdS film gives a better contact to the cells between aluminum and silicon compared to aluminum direct on top of silicon in the case of homojunctions. As a result, the series resistances of the homojunction and heterojunction cells are from the back contact.

6.6.1 Band Diagrams of CdS/n-p Si Junctions

The C-V characteristics in Fig. 6.16 of the four CdS/n-p Si cells are similar to that of n-p cells. If one assumes they are n-p homojunctions, they have the following characteristics,

Table 6.11
Experimental parameters of CdS/n-p Si cells.

Sample No.	V_{bi}(V)	substrate impurity concentration(cm^{-3})	depletion width(um)
164	0 7	$4.7x10^{15}$	0.44
170	0 7	$4.7x10^{15}$	0.46
165	0.7	$4.3x10^{15}$	0.47
171	0 7	$3.3x10^{15}$	0.53

Because of the similarity of the C-V characteristics of n-p and CdS/n-p Si cells, it suggests that the n-p Si junction of the CdS/n-p Si cells will dominate the electrical properties The only differences are a slightly higher substrate impurity concentrations and a slightly smaller V_{bi} for the CdS/n-p Si cells. As a result, the CdS layer acts as an electrode and affects only the optical properties.

The experimental data extracted from C-V measurements agrees with the

theoretical values. The theoretical values are given in **Table 6.12**.

Table 6.12
Theoretical parameters of CdS/n-p Si cells.

Sample No.	V_{bi}(V)	Depletion Width(um)
164	0.73	0.45
170	0.65	0.42
165	0.73	0 47
171	0.65	0 51

From the I-V characteristics in Fig 6 17, a simple n-p junction is expected. This fact further confirms that the CdS layer and the junction formed between the layer and the n+ diffused region do not exhibit any significant effect on top of the n-p homojunction. As a result, band diagrams of the CdS/n-p Si cells are simply the CdS/n-Si linked to the n-p Si cells diagrams The n-p junction of the CdS/n-p cells parameters are from the homojunction measurements and the final band diagrams are shown in Fig. 6 18 note : samples 163 and 169 have similar result.

6 6.2 Performance Analysis of CdS/n-p Si Cells

The I-V characteristics and quantum efficiencies for the cells are shown in Fig.

6.17 and Fig. 6.19, respectively. The performances of the cells are listed in the following table

Table 6.13
Performance of CdS/n-p Si cells.

Sample No	V_{oc} (V)	J_{sc} (mA/cm^2)	F F.	V_{shift} (V)	R_S (Ω)	n	η (%)
164	0 51	16.3	0 57	0.05	5	2.2	5.8
170	0.51	15.1	0.69	0.03	3	2.2	6.5
165	0.51	15.7	0.72	0.02	4	1.8	7.1
171	0.50	15	0 65	0.02	5	3.3	5.7

There are two advantages from this cell configuration. First, it provides large V_{oc} like a homojunction cell, second, it provides large J_{sc} like a heterojunction cell, i.e. it provides the same amount of current as a CdS/p-Si cell. The large V_{oc} comes from the n-p homojunction which dominates the electrical properties. The large J_{sc} comes from the fact that high energy photons are allowed to go through the CdS layer and excite electrons and holes at or near the space charge region of the homojunction so that more carriers can be collected This is shown in the quantum efficiencies in Fig. 6.19. Compared to the homojunction, high energy photons excite less electron-hole pairs on the surface so that surface recombination or "dead" layer effect is reduced in the CdS/n-p configuration. By

combining the advantages of the homojunction and heterojunction, the CdS/n-p configuration gives higher efficiencies.

6.7 Series Resistance of All Samples

As mentioned at the end of section 6.5.2, the series resistance is from the back contact. By improving the quality of the back contact, series resistance can be lowered and higher photocurrent and better fill factor are expected On the other hand, by improving the front Al grid, more current can be collected.

6.8 Effect of Interface States

No frequency dispersion on capacitance is observed in homojunctions. The C-F results of samples 162 and 168 are shown in Fig. 6.20. On the other hand, CdS/p Si heterojunction cells have significant dispersion on C-F measurements and it is expected because of the high densities of interface states caused by lattice mismatch of CdS and (100)Si. The C-F curves of samples 166 and 167 are shown in Fig 6 21 The densities of interface state and time constants for different bias voltages are calculated as in appendix VII and the results are listed in the following tables

Table 6.14
Density of interface state and time constant
of the CdS/p Si heterojunction (sample 166).

Bias Voltage (V)	τ from line section. in Fig. 5 18(a) (sec)	Interfacial state density ($eV^{-1}cm^{-2}$)
0 1	a to b : $1.6x10^{-5}$	$6.5x10^{10}$
0	c to d : $1.2x10^{-5}$	$6.9x10^{10}$
-0 2	e to f : $3.1x10^{-5}$	$5.3x10^{10}$

Table 6.15
Density of interface state and time constant
of the CdS/p Si heterojunction (sample 167).

Bias Voltage (V)	τ from line section . in Fig. 5 18(b) (sec)	Interfacial State Density ($eV^{-1}cm^{-2}$)
0 1	a to b : $2.1x10^{-4}$	$3.6x10^{10}$
0	c to d · $4.9x10^{-5}$	$2.7x10^{10}$

Both samples show interface state effects as evident from C-F measurements. The interface state density of the sample 167 is slightly lower than that of the sample 166

so that sample 167 has a higher photocurrent and smaller n factor. However, the interface state densities of both samples are relatively small (usually 10^{11} to 10^{12} $eV^{-1}cm^{-2}$ for heterojunctions with large lattice mismatch) so that voltage shifts between dark and illuminated conditions are not significant The time constants of the sample 167 at 0 1 V and 0 V bias voltages are larger than that of sample 166. No conclusion can be made on the exact origin of the frequency dispersions at this moment However, the effect of trap levels is more sensitive to temperature, i e it can be inhibited at low temperature At a low temperature of 200 K, C-F measurements are made on samples 166 and 167 and the results are shown in Fig. 6 22. The data deduced from the measurements are listed in the following two tables.

Table 6.16
Density of interface state and time constant
of the CdS/p Si heterojunction (sample 166)
at 200 K

Bias Voltage (V)	τ from line section. in Fig. 5.19(a) (sec)	Interfacial State Density ($eV^{-1}cm^{-2}$)
0.1	a to b : $1.1x10^{-4}$	$8.0x10^{10}$
0	c to d : $9.5x10^{-5}$	$5.9x10^{10}$

Table 6.17
Density of interface state and time constant
of the CdS/p Si heterojunction (sample 167)
at 200 K.

Bias Voltage (V)	τ from line section.. in Fig. 5.19(b) (sec)	Interfacial State Density ($eV^{-1}cm^{-2}$)
0.1	a to b : $3.3x10^{-5}$	$1.4x10^{10}$
0	c to d : $1.5x10^{-5}$	$8.1x10^{9}$

The capacitance values are relatively lowered at low temperatures because of the widening of depletion region caused by freezed out of carriers. However, if the frequency dispersion on capacitance is dominant by interface states, the shape of the C-F curve and the dispersion only change very little [4.6]. Sample 166 has same frequency dispersions at 0 V and 0.1 V bias at room temperature and 200 K. Since the C-F curves are different at different temperatures, both trap level and interface state mechanisms are present. By assuming the inhabitation of trap level at low temperature, only interface state caused dispersion is shown in the C-F curve The time constants show an increase with the decrease in temperature [4.6]. Sample 167 also shows very slight dispersion at 200 K and it suggests that the dispersion is dominated by trap level. By carrying out C-V measurement on sample 166 at low frequency (1000 Hz), the real band diagram information can be extracted from the curve in Fig. 6.23.

Table 6.18
Experimental parameters of sample 166
at 1000 Hz.

Sample	V_{bi}(V)	E_F-E_v(eV)	$\Delta\chi$(eV)
166	0.38	0.28	0 44

All four CdS/n-p Si cells show very small frequency dispersions in Fig 6.24 and Fig. 6.25 either at room temperature or 200 K because of the electrical properties domination of the n-p homojunction over the CdS/n heterojunction As a result, interface state has no effect on this cell configuration.

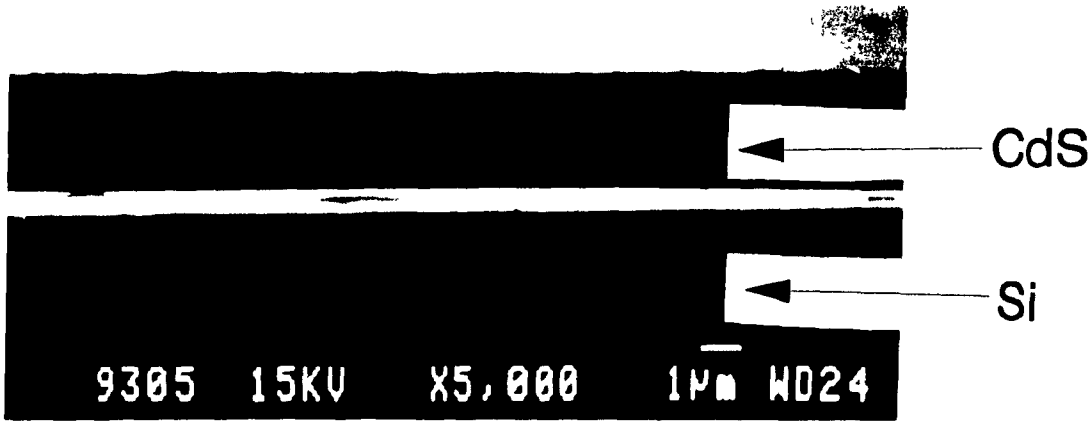


Fig. 6.1 A SEM photograph showing a CdS film on SI substrate.

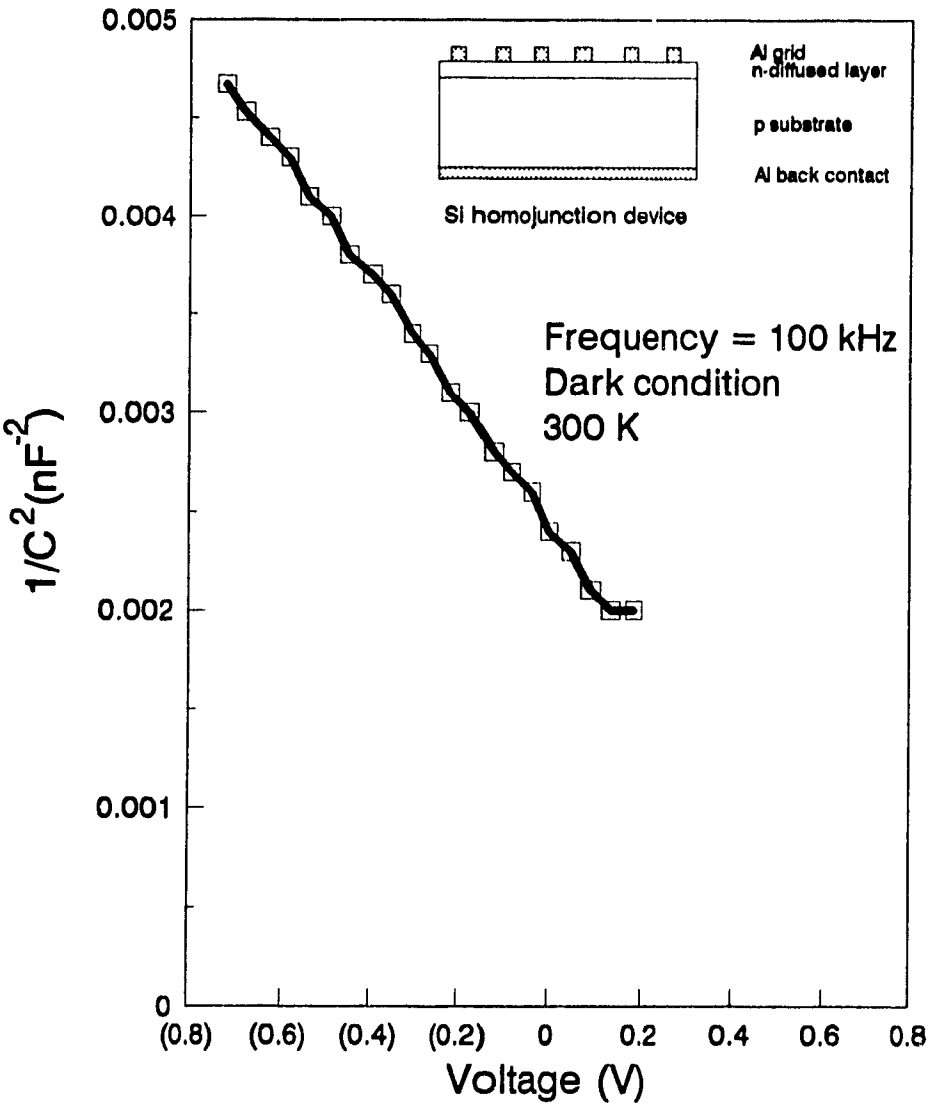


Fig. 6.2 C-V characteristics of sample 162.
(n/p homojunction cell)

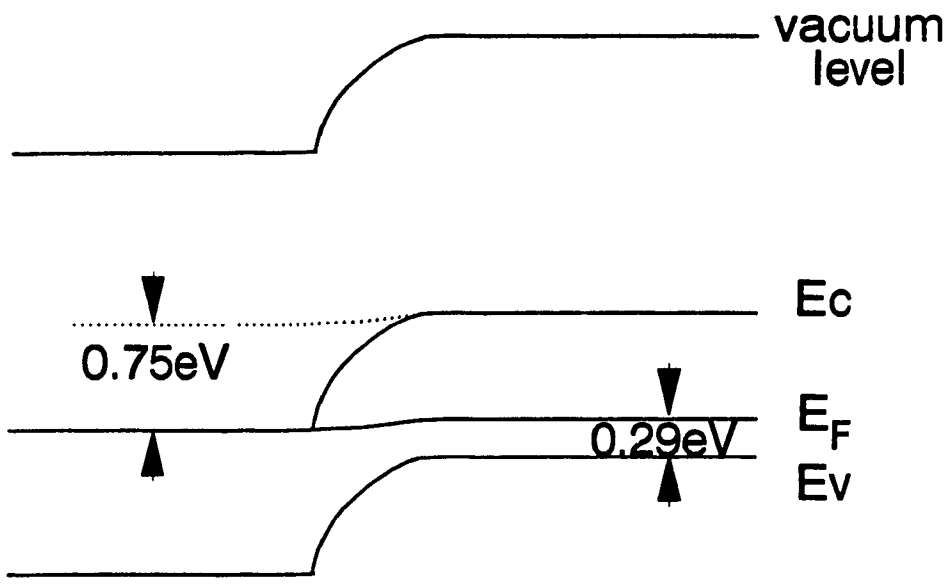


Fig. 6.3(a) Band diagram of the n/p Si cell.
(#162)

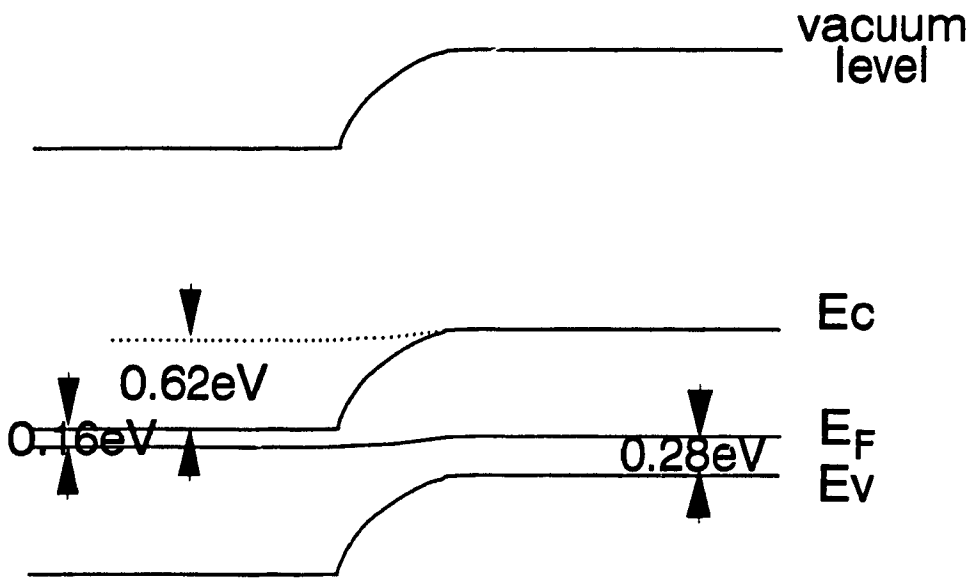


Fig. 6.3(b) Band daigram of the n/p Si cell.
(#168)

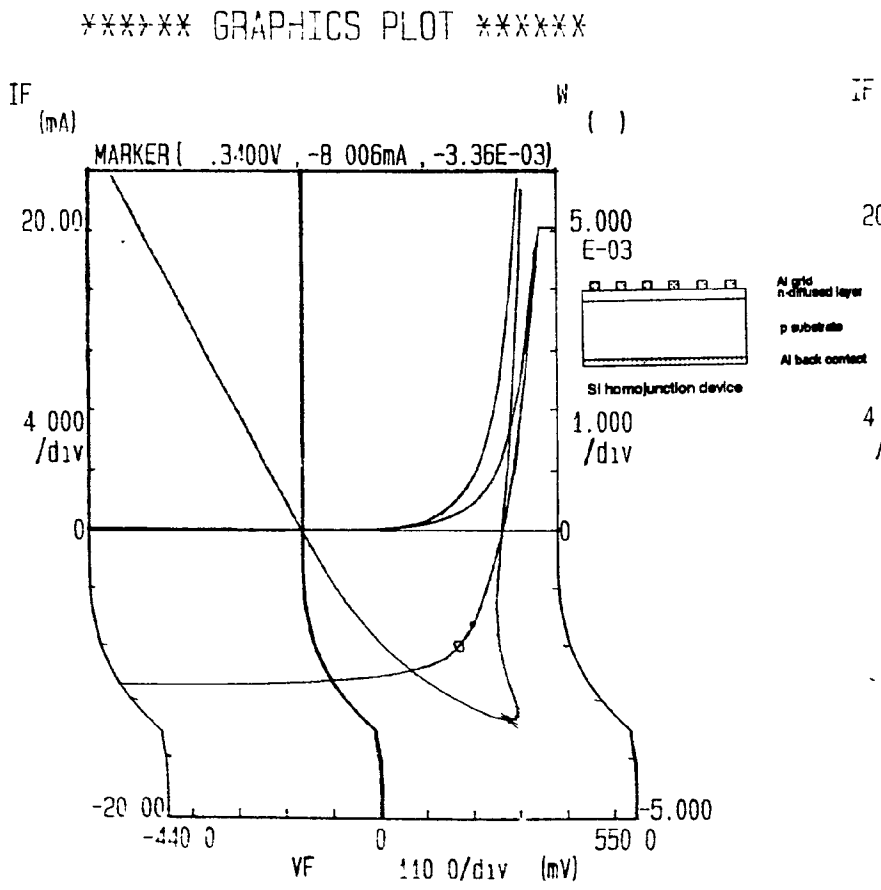


Fig. 6.4(a) I-V characteristics of sample 162.

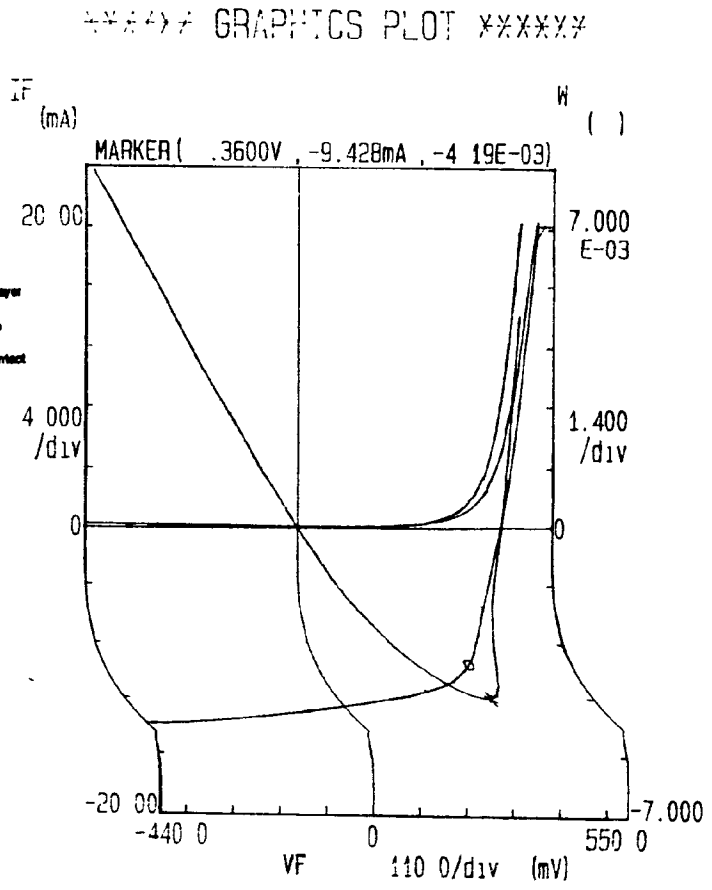


Fig. 6.4(b) I-V characteristics of sample 168.

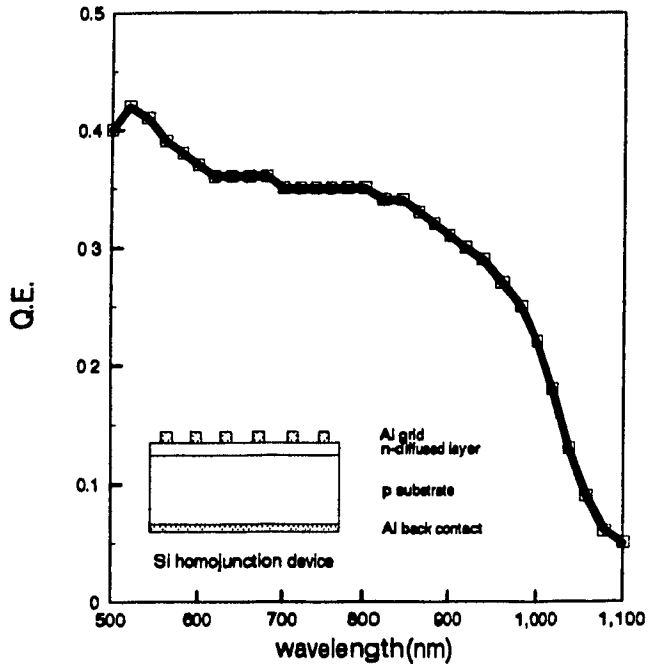


Fig. 6.5(a) Quantum efficiency of sample 162.

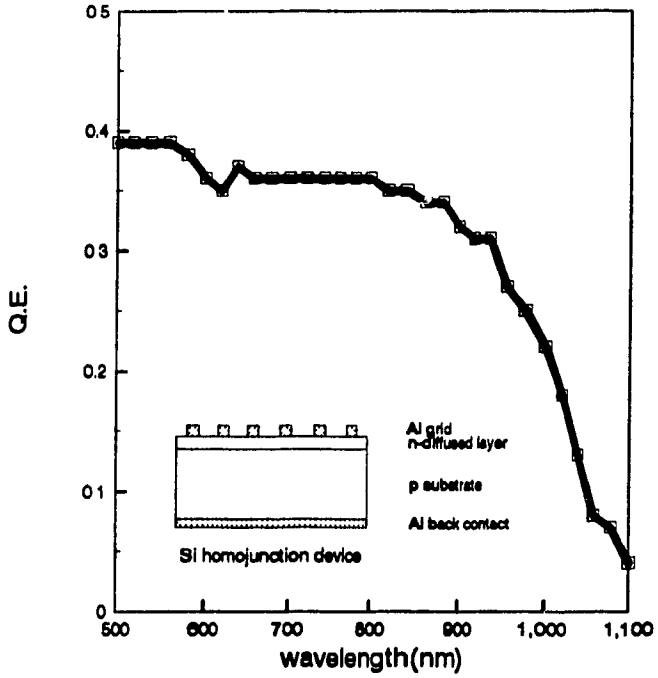


Fig. 6.5(b) Quantum efficiency of sample 168.

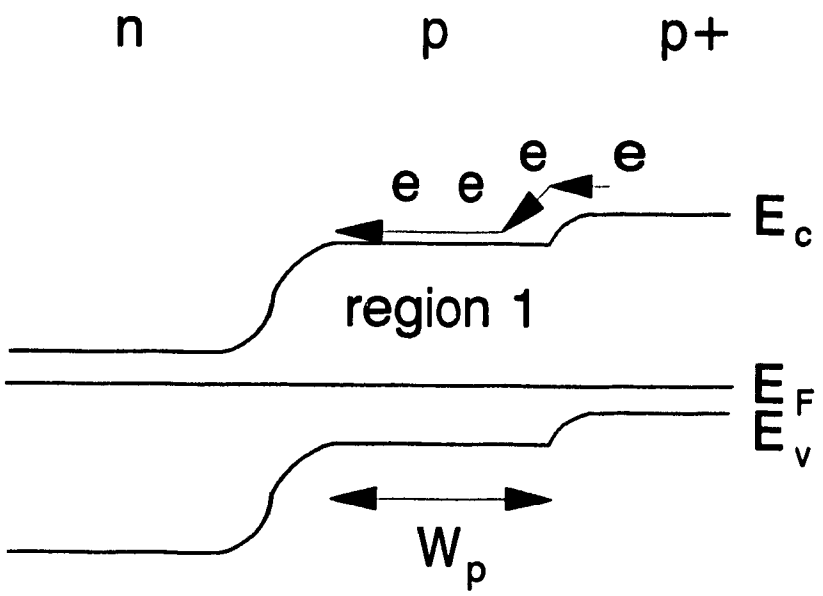


Fig. 6.6 Energy band diagram of a back surface field device.

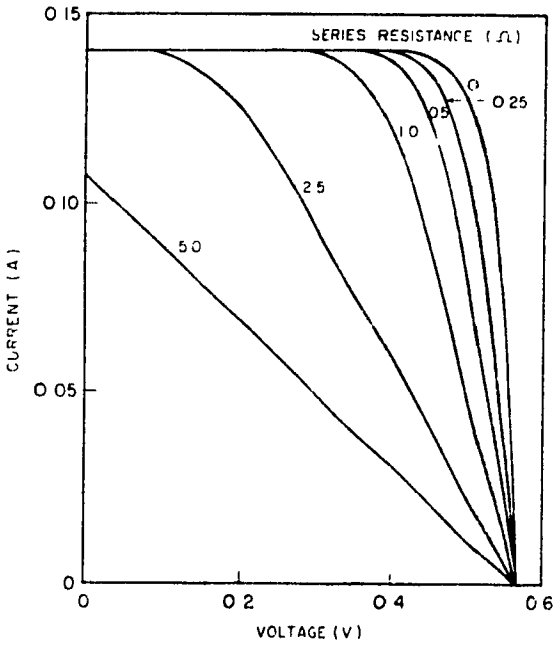


Figure 2.10 Effect of series resistance on the I–V curve shape

Fig. 6.7 The effects of series resistance on the performance of cells.

(F.Lasnier & T G.Ang, Photovoltaic Engineering Handbook, Adam Hilger, Bristol and New York, P.77 Fig. 2.10 (1990).

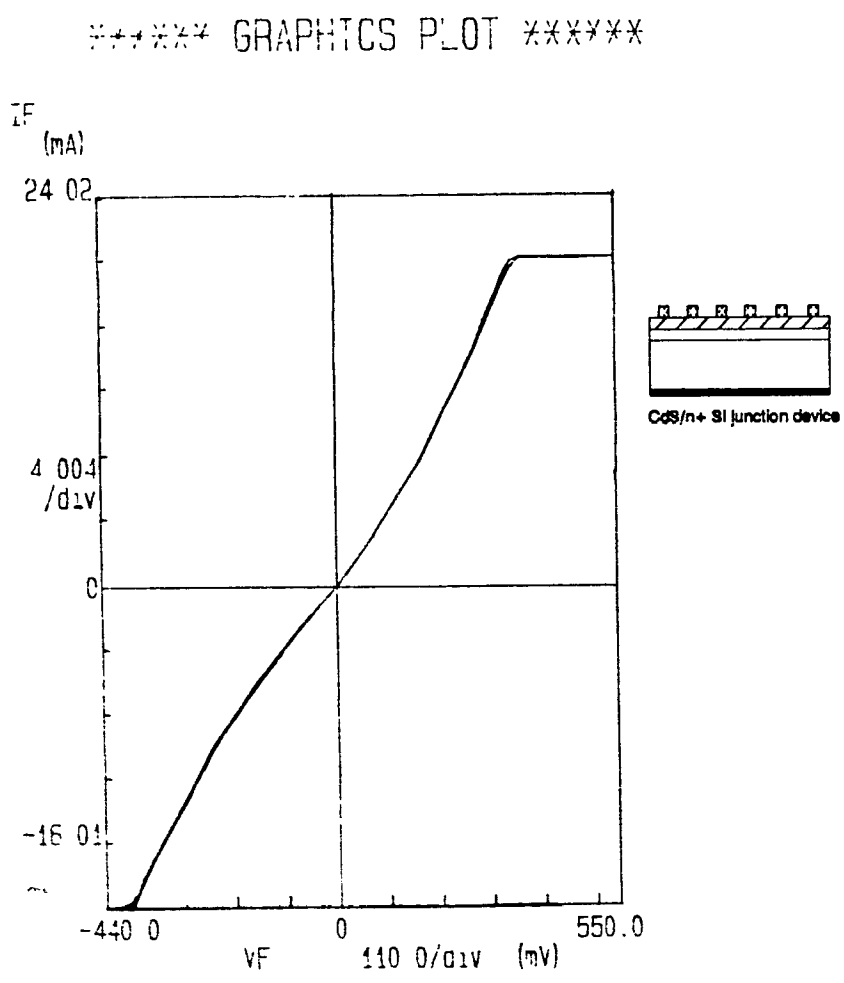


Fig. 6.8(a) I-V characteristics of sample 173.

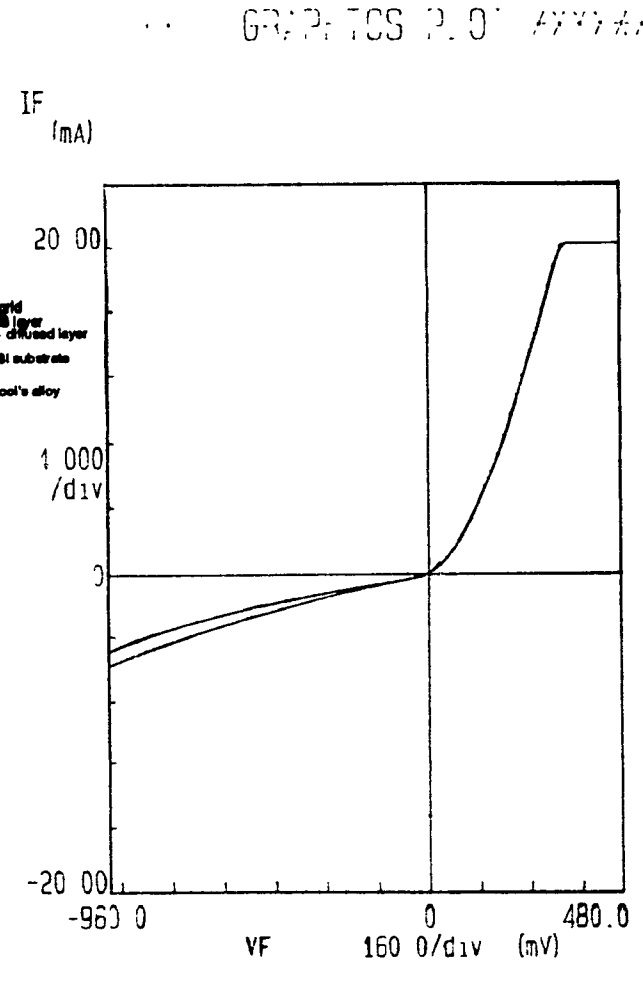


Fig. 6.8(b) I-V characteristics of sample 175.

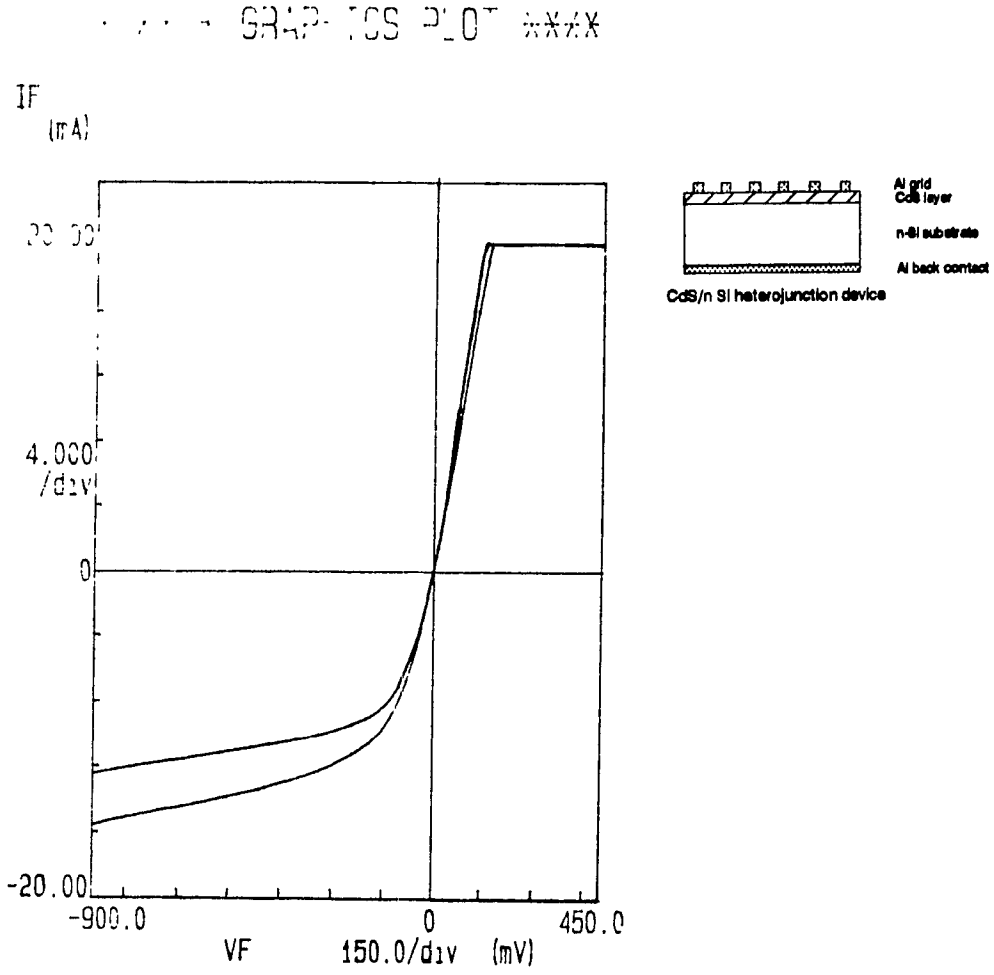


Fig. 6.8(c) I-V characteristics of sample 180.

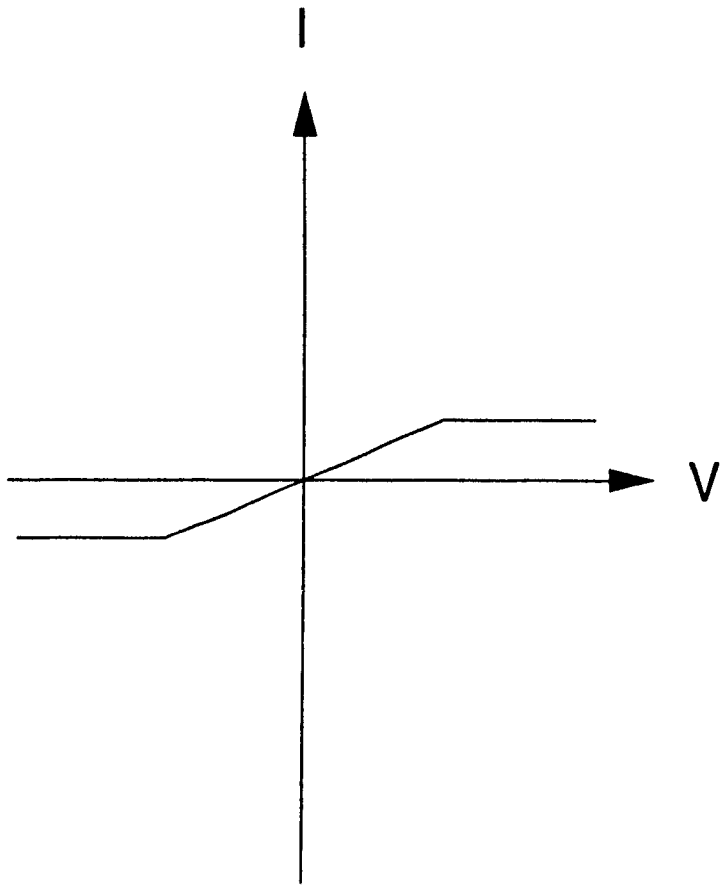


Fig. 6.9 I-V characteristic of a back-to-back diode.

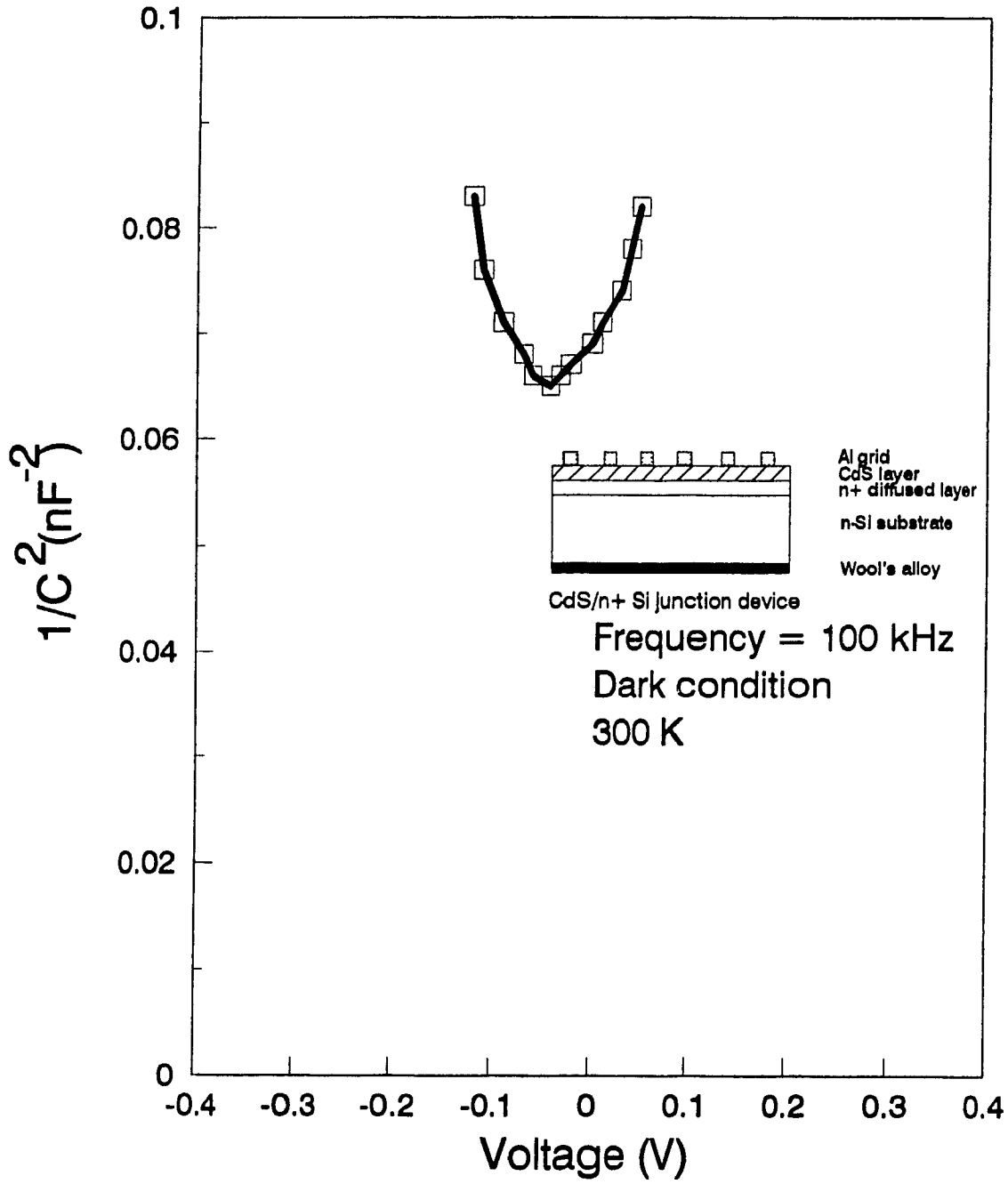


Fig. 6.10 C-V characteristics of sample 175.

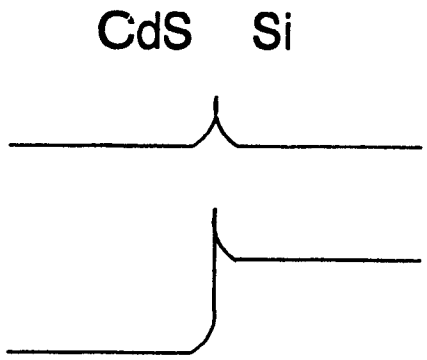


Fig. 6.11 (a) Band diagram of sample 173.

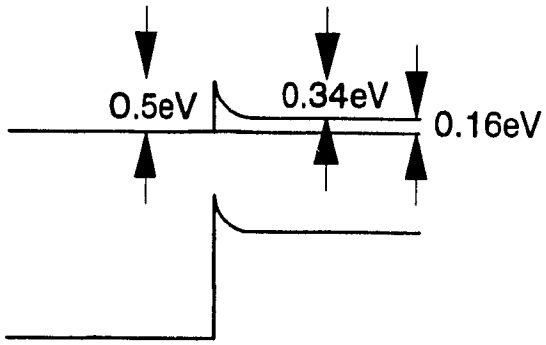


Fig. 6.11 (b) Band diagram of sample 175.

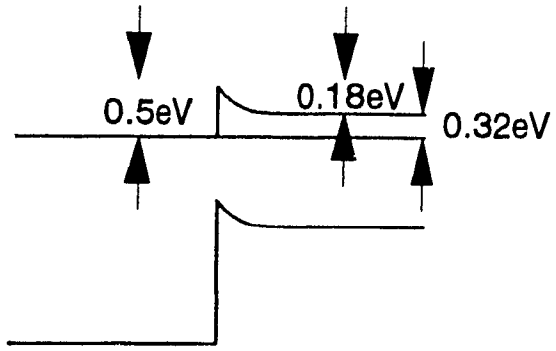


Fig. 6.11 (c) Band diagram of sample 180.

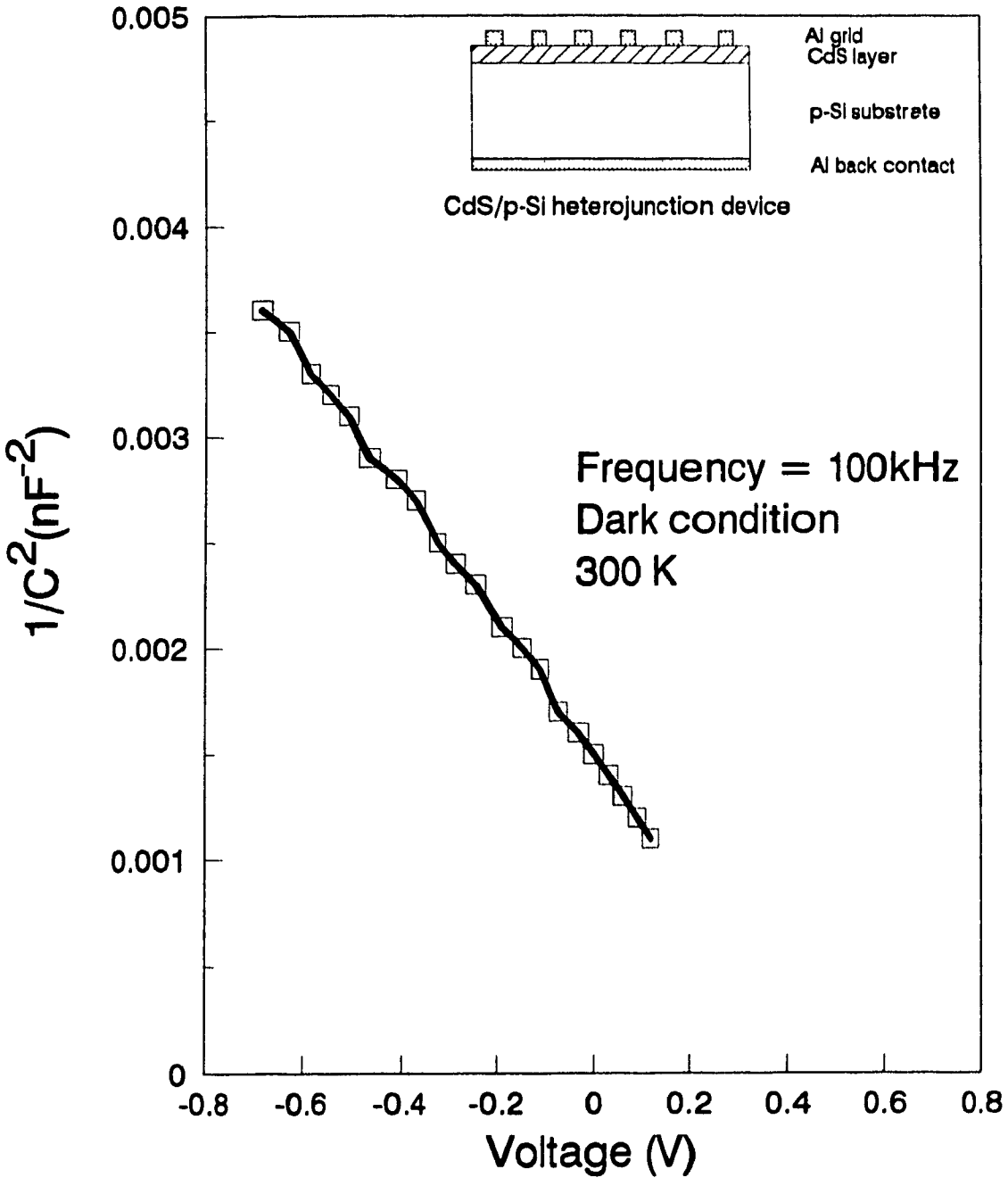


Fig. 6.12 C-V characteristics of sample 166.

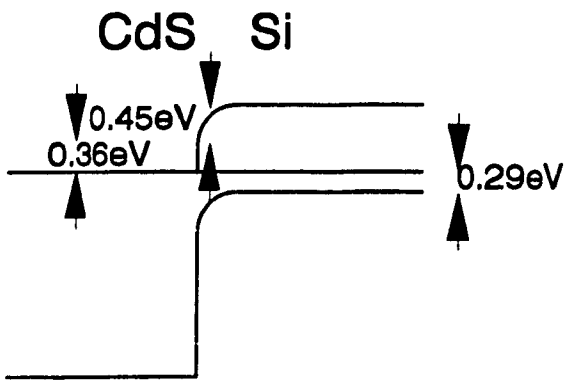


Fig. 6.13(a) Band diagram of sample 166.

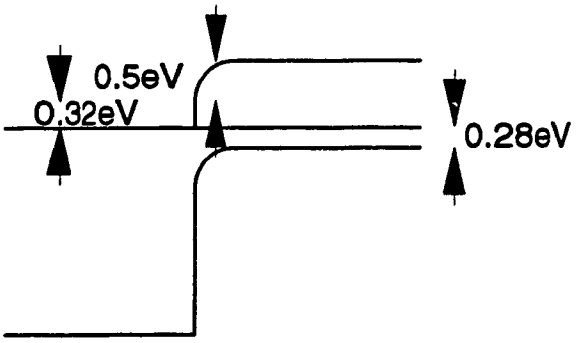


Fig. 6.13(b) Band diagram of sample 167.

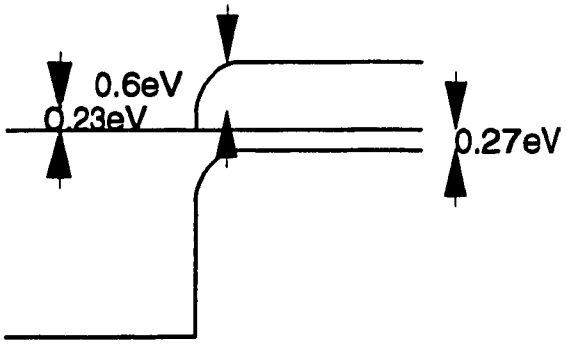


Fig. 6.13(c) Band diagram of sample 178.

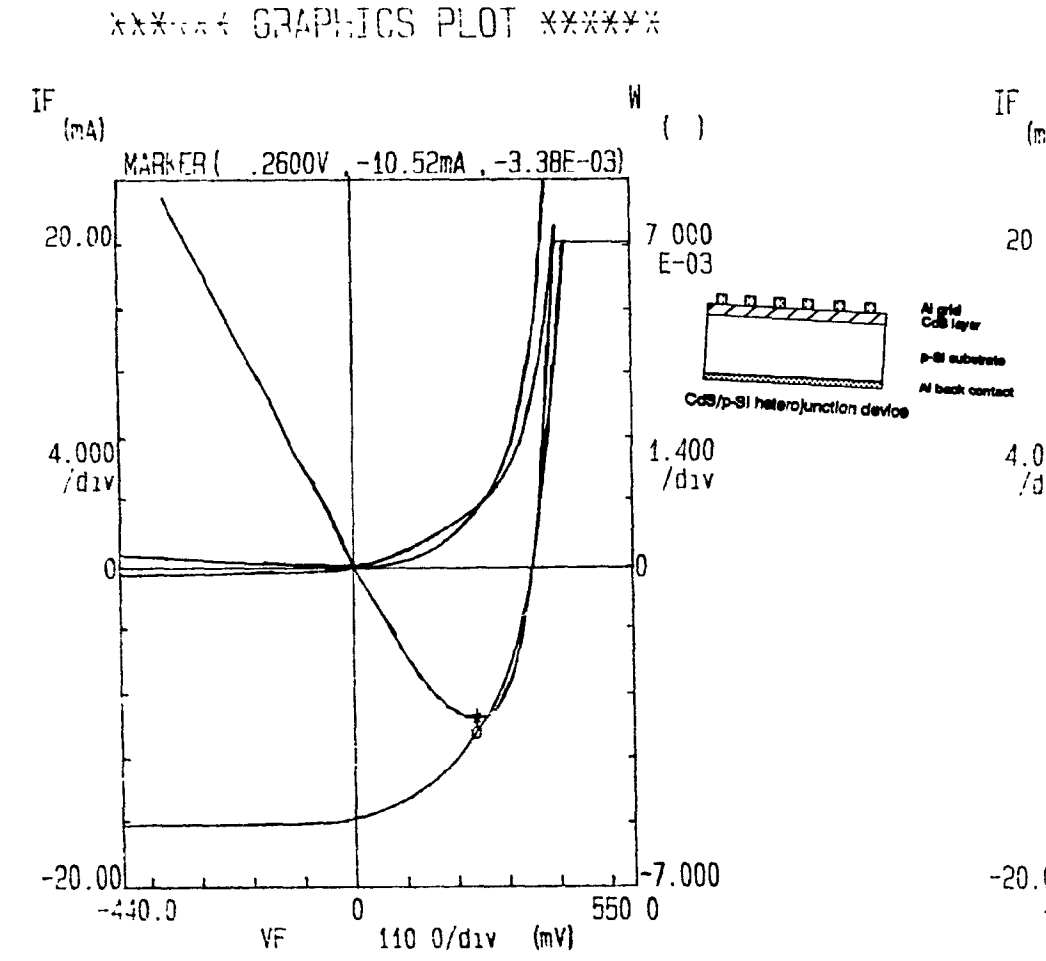


Fig. 6.14(a) I-V characteristics of sample 166.

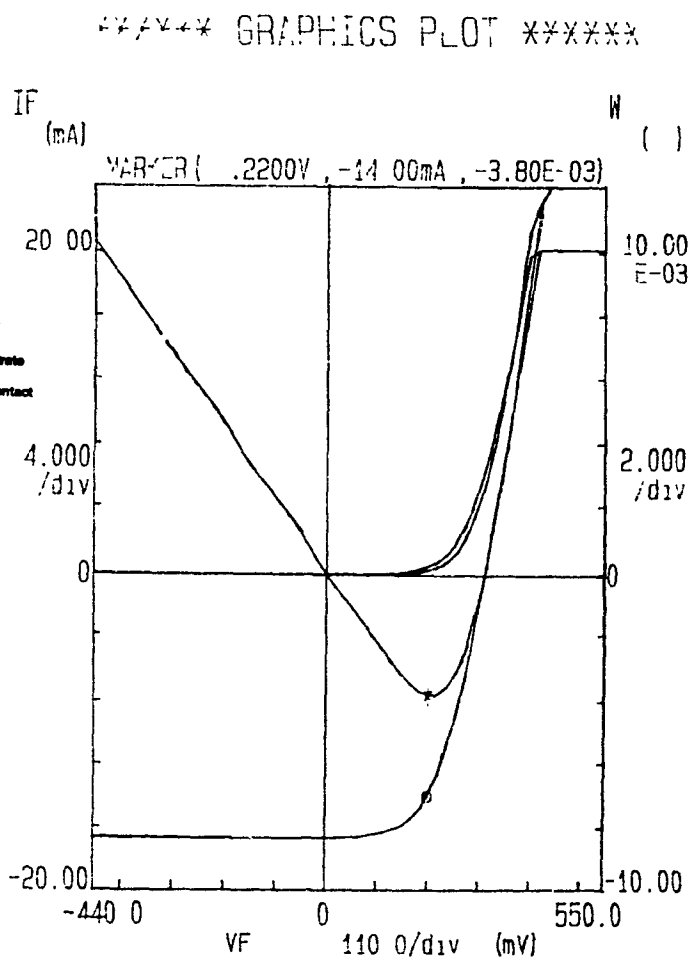


Fig. 6.14(b) I-V characteristics of sample 167.

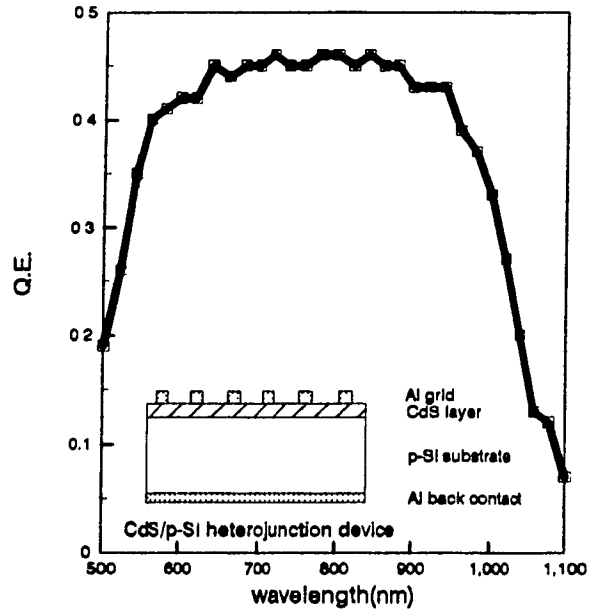


Fig. 6.15(a) Quantum efficiency of sample 167.

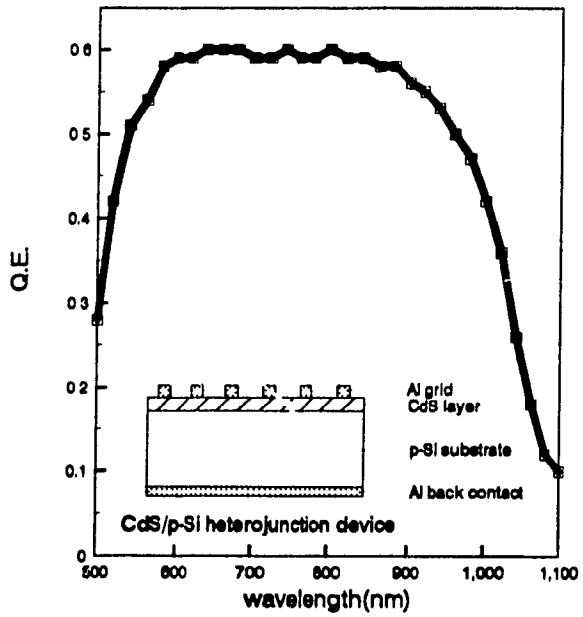


Fig. 6.15(b) Quantum efficiency of sample 178.

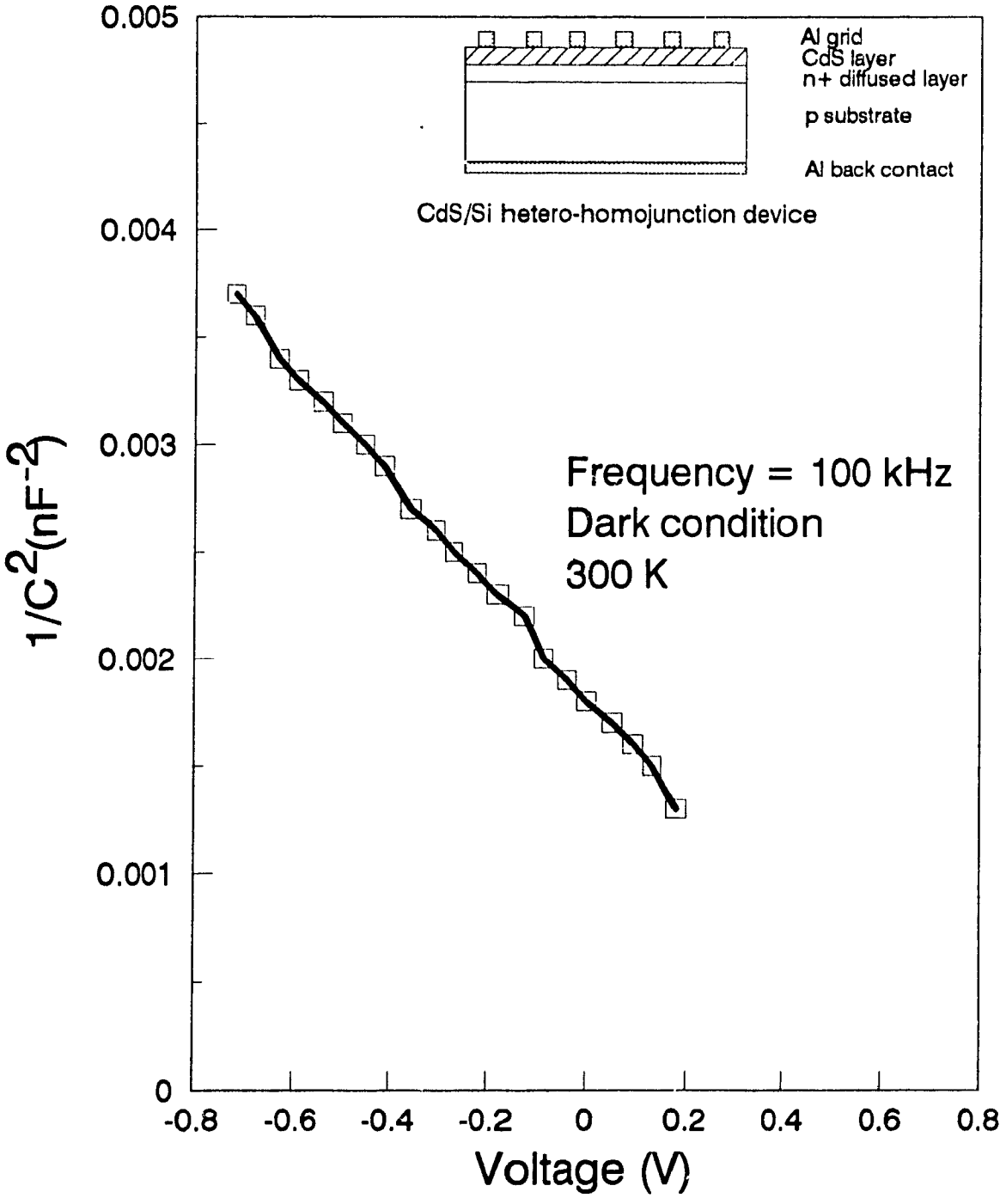
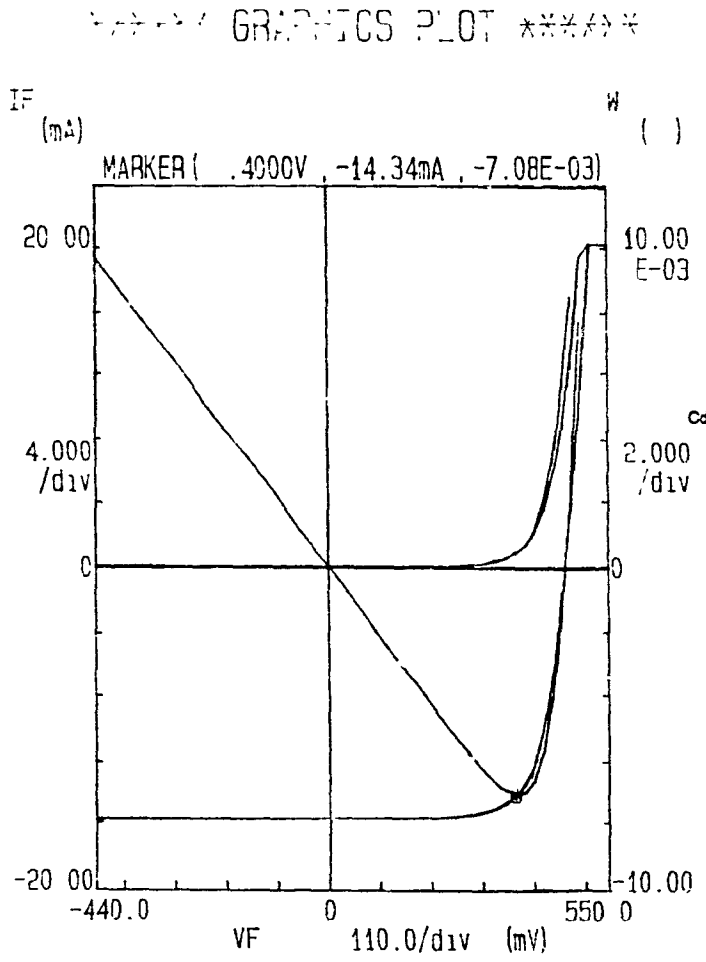
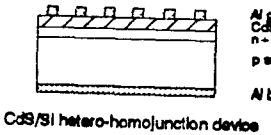


Fig. 6.16 C-V characteristics of sample 164.





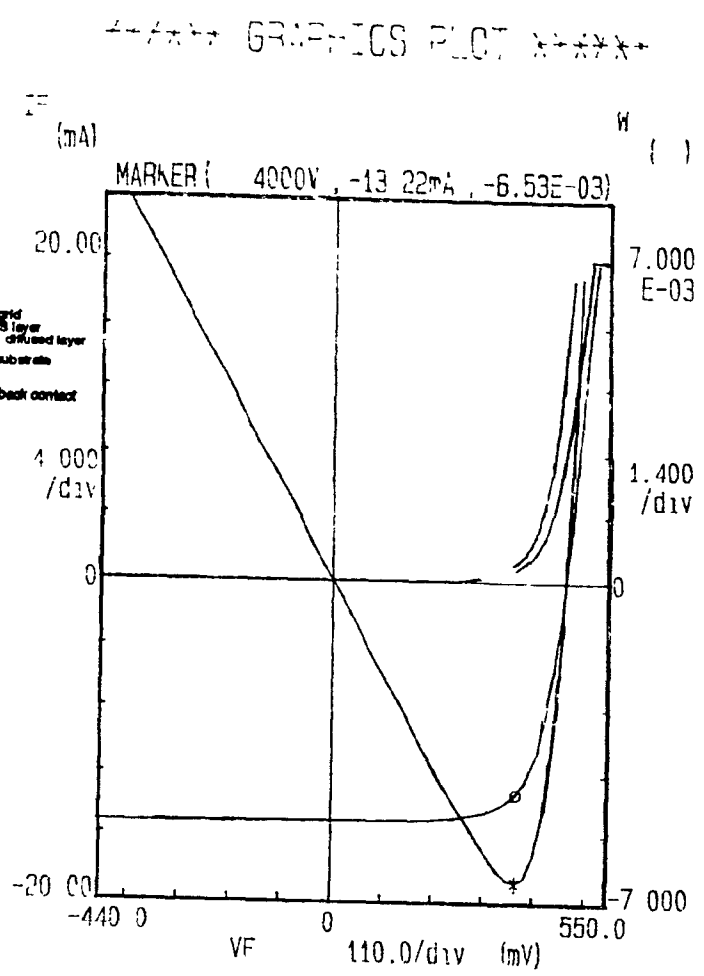


Fig. 6.17(a) I-V characteristics of sample 165.

Fig. 6.17(b) I-V characteristics of sample 170.

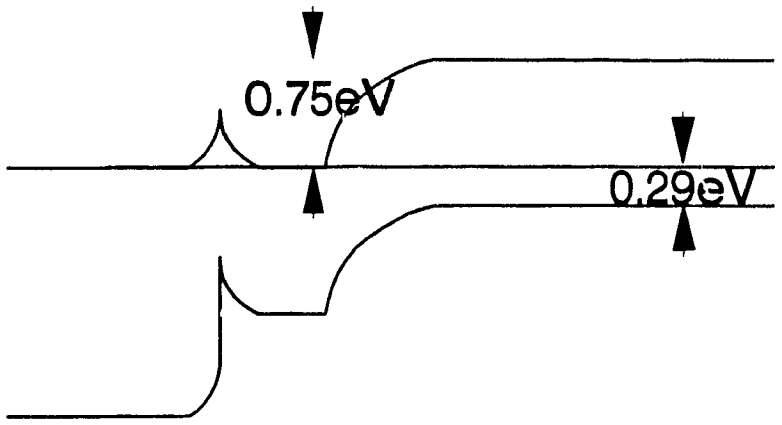


Fig. 6.18(a) Band diagram of sample 164.

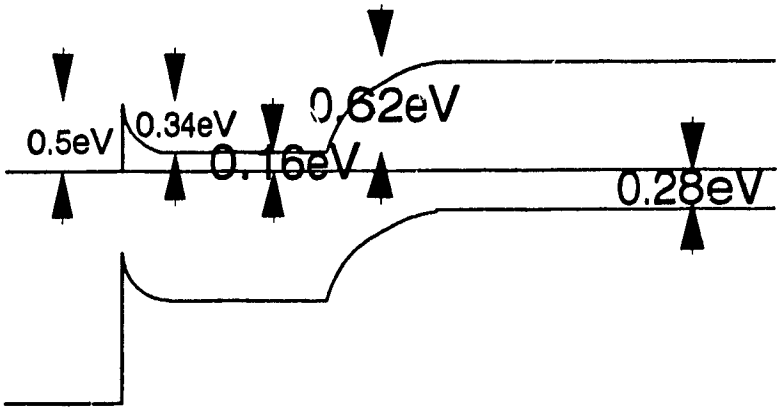


Fig. 6.18(b) Band diagram of sample 170.

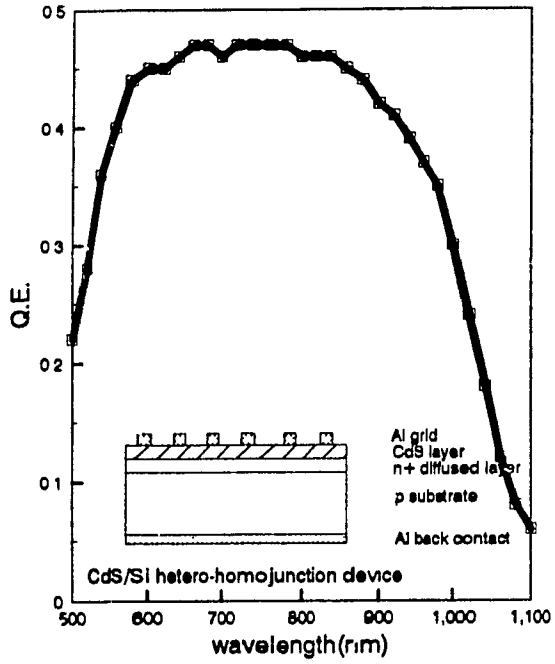


Fig. 6.19(a) Quantum efficiency of sample 164.

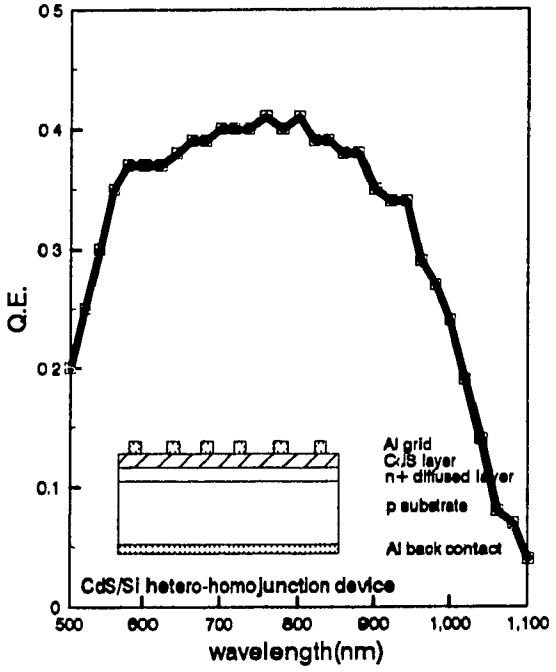


Fig. 6.19(b) Quantum efficiency of sample 170.

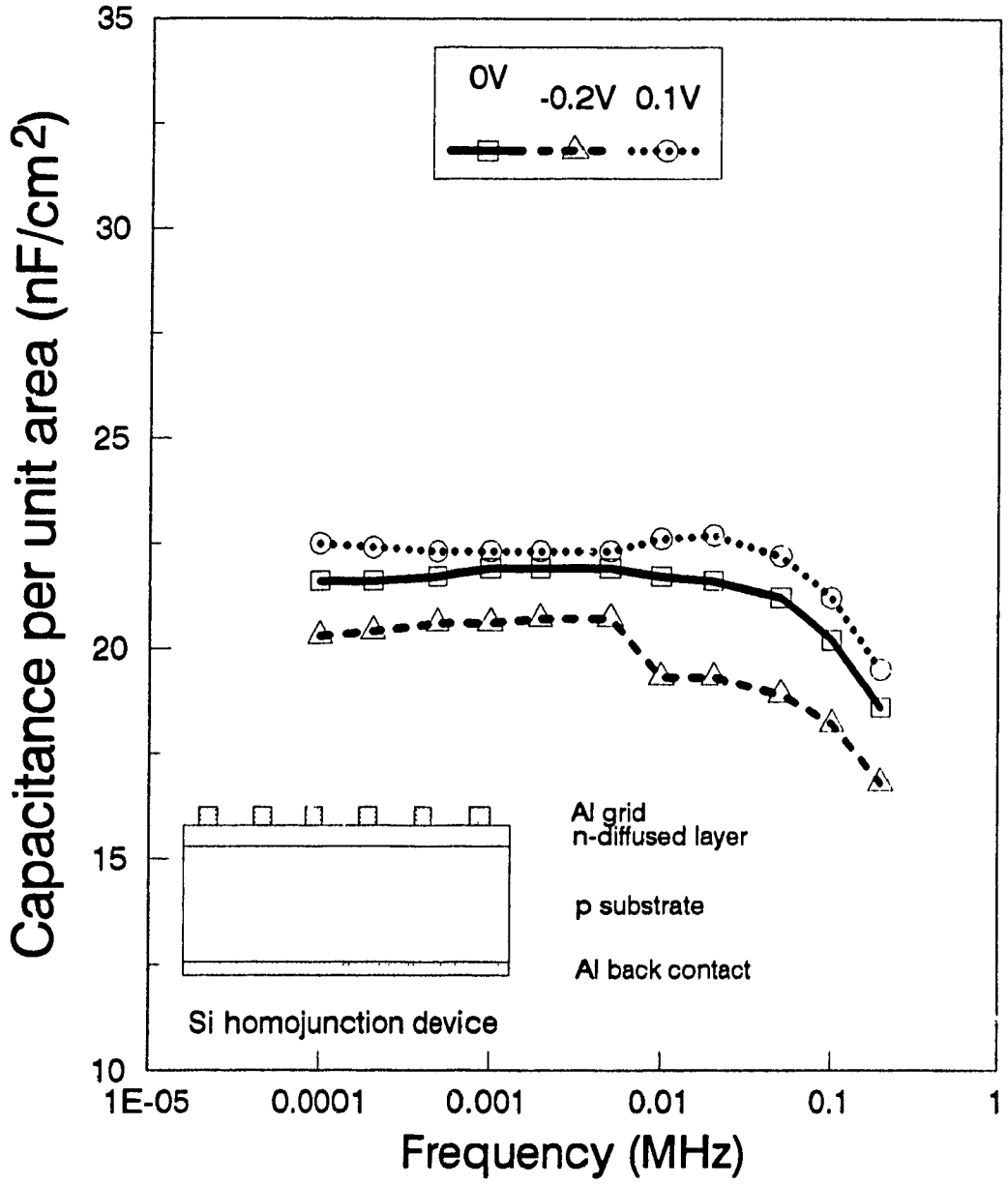


Fig. 6.20(a) Results of C-F measurements of sample 162 at 300 K.

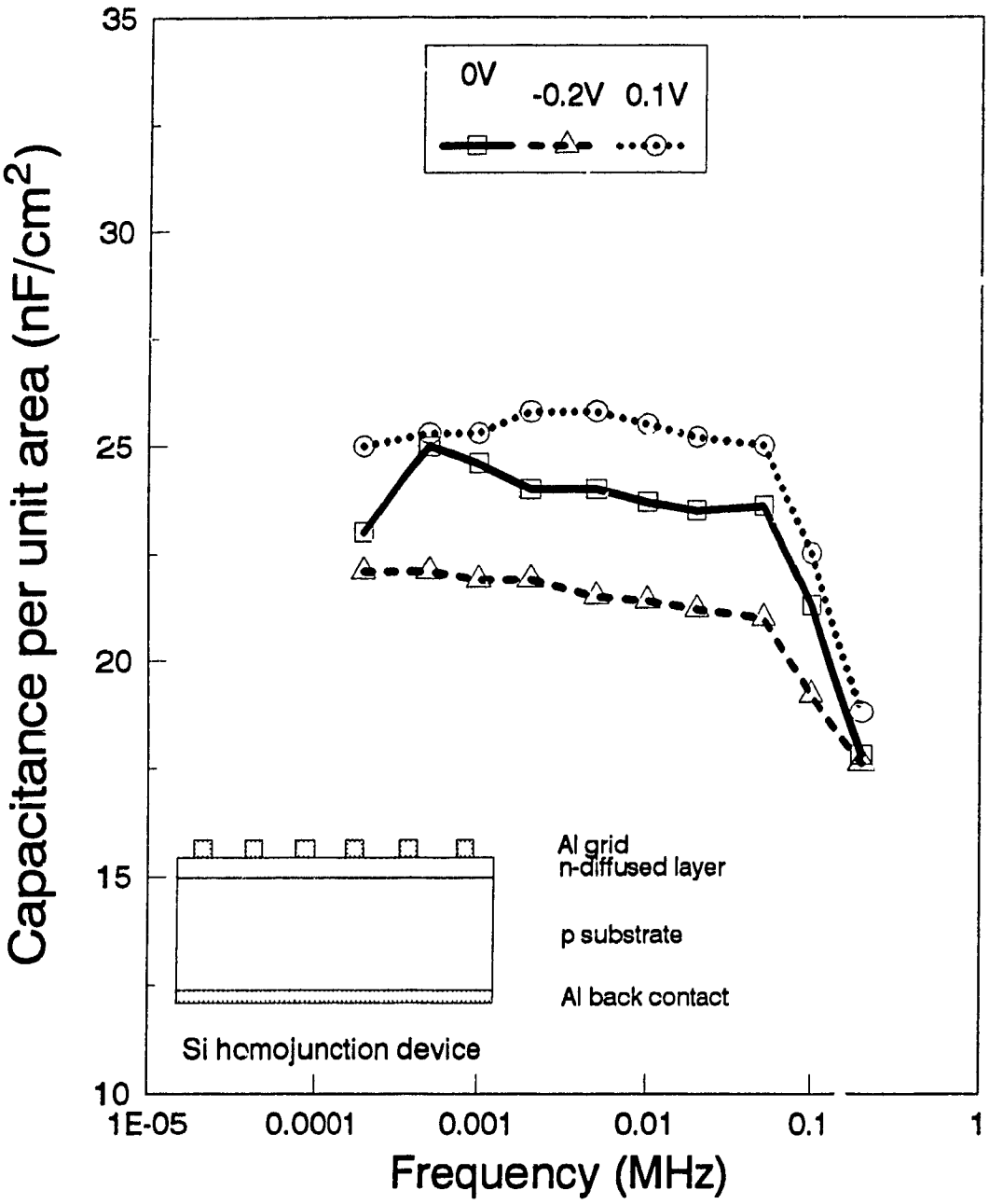


Fig. 6.20(b) Results of C-F measurements of sample 168 at 300 K.

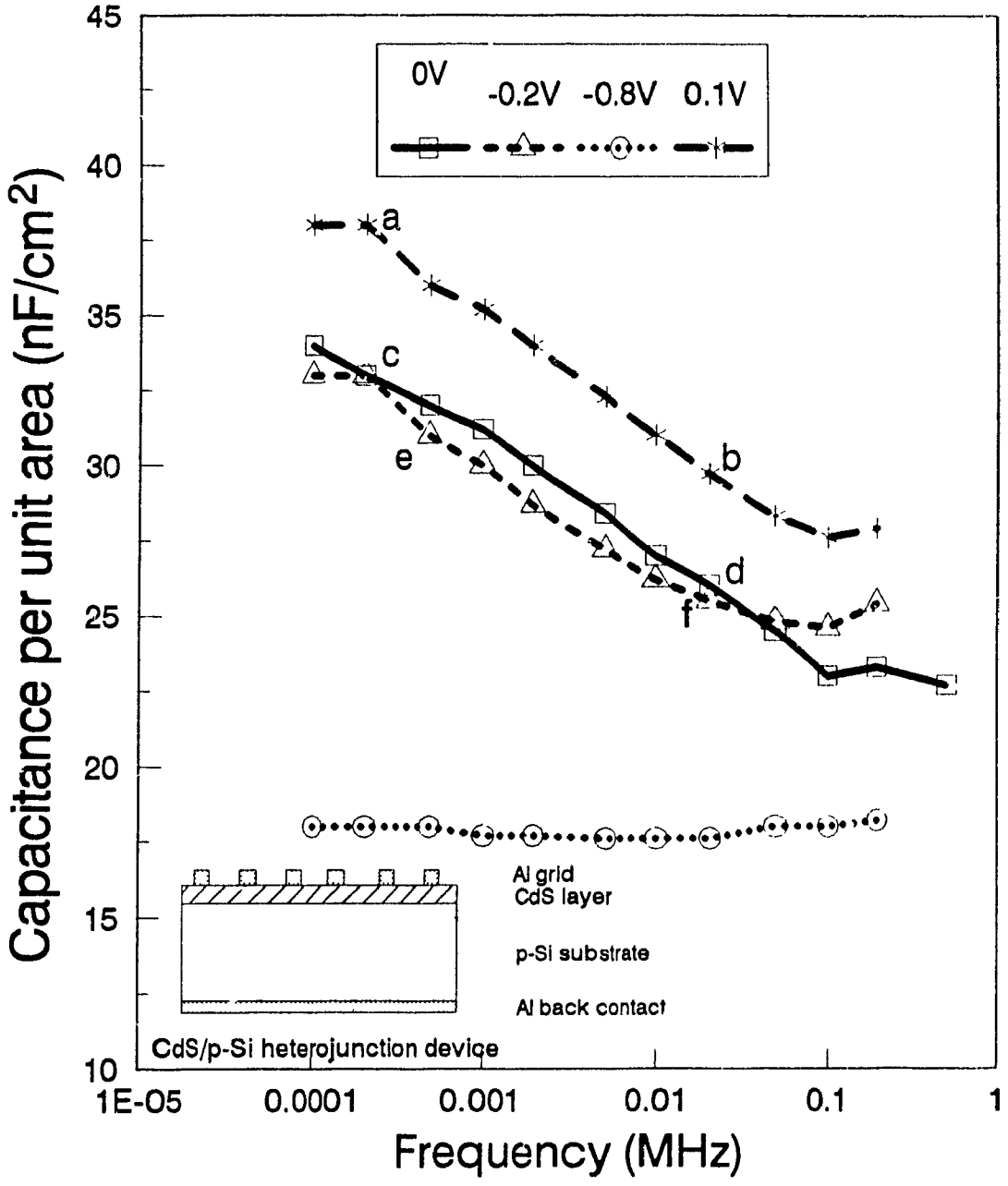


Fig. 6.21(a) Results of C-F measurements of sample 166 at 300 K.

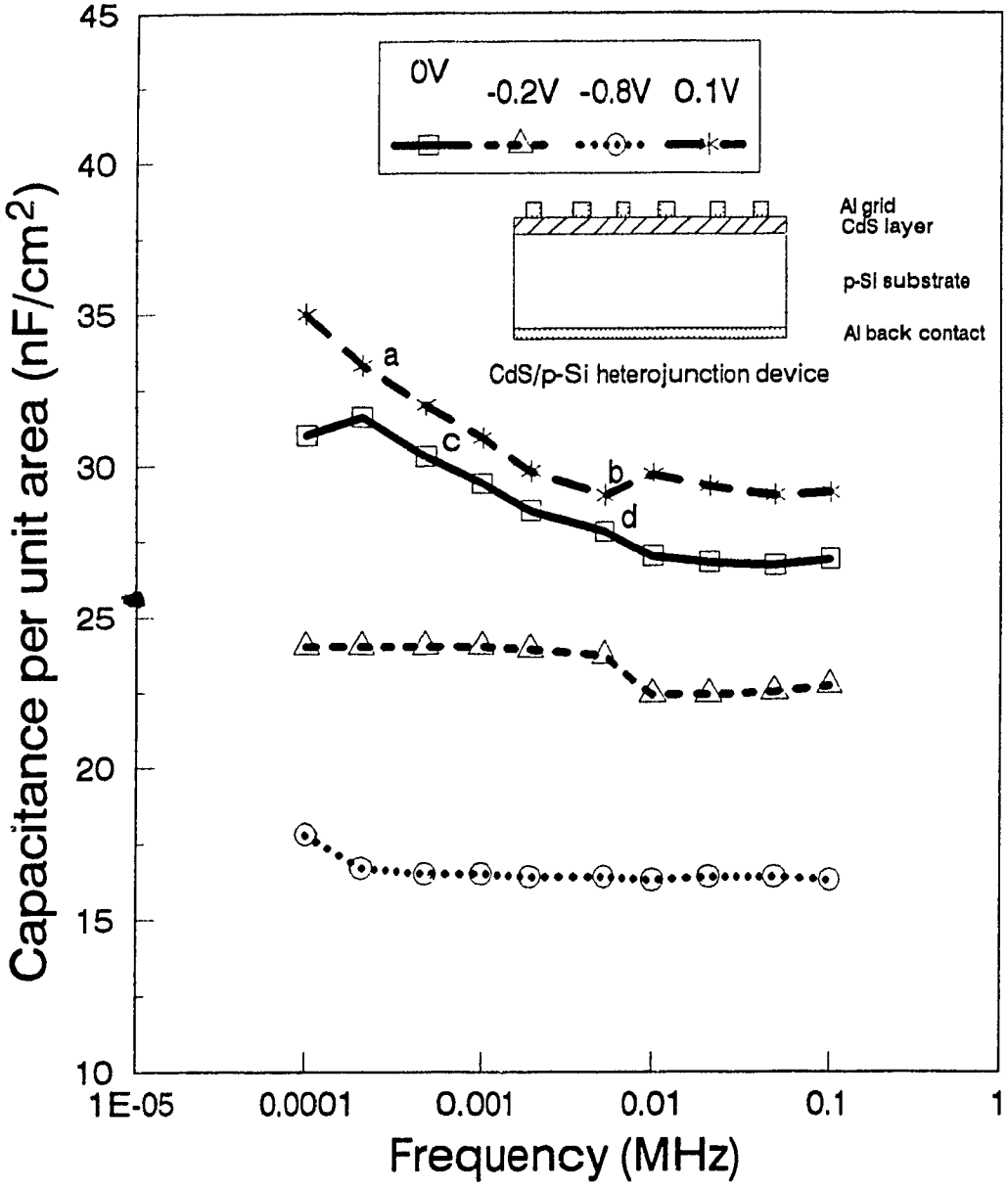


Fig. 6.21 (b) Results of C-F measurements of sample 167 at 300 K.

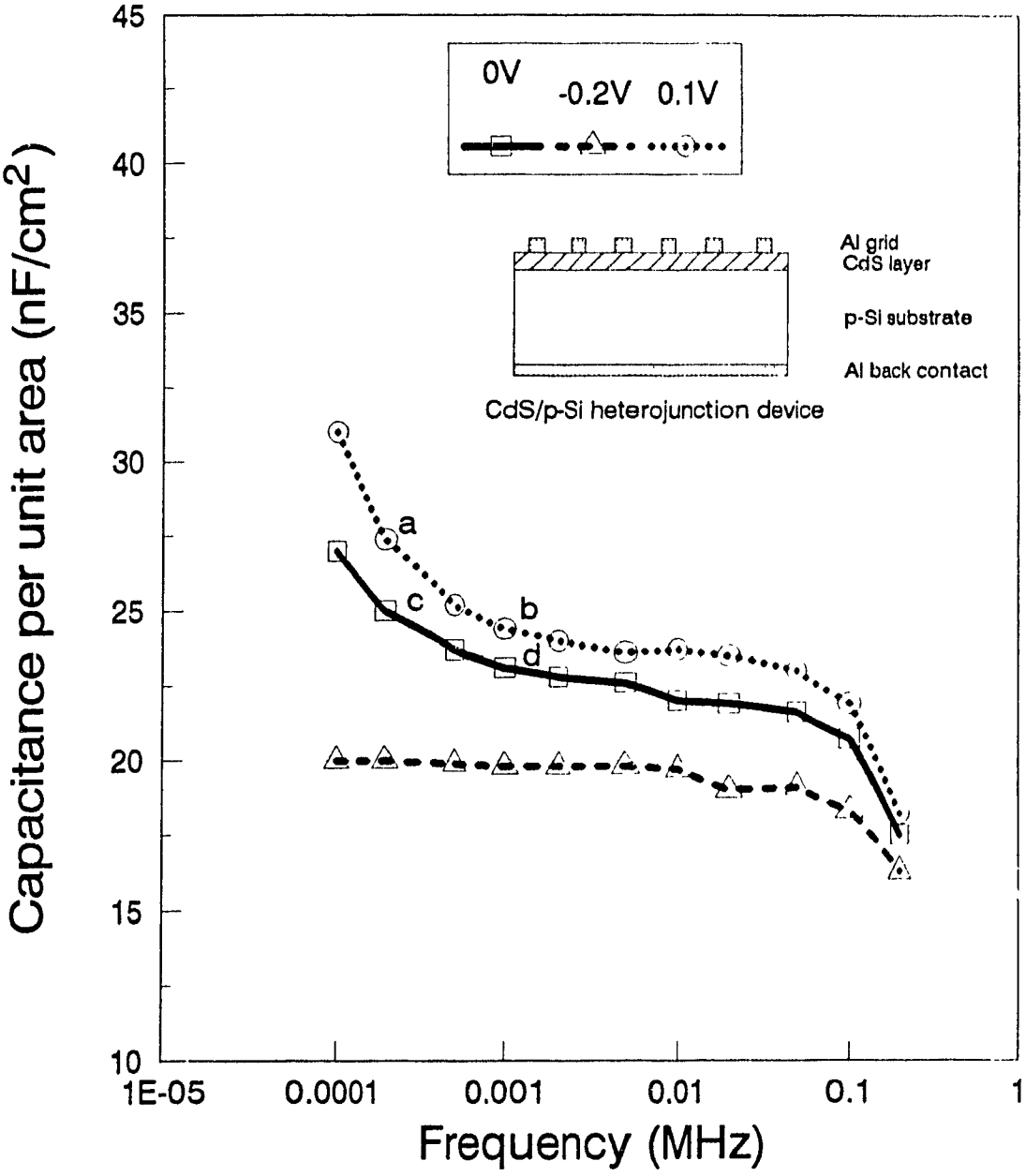


Fig. 6.22(a) Results of C-F measurements of sample 166 at 200 K.

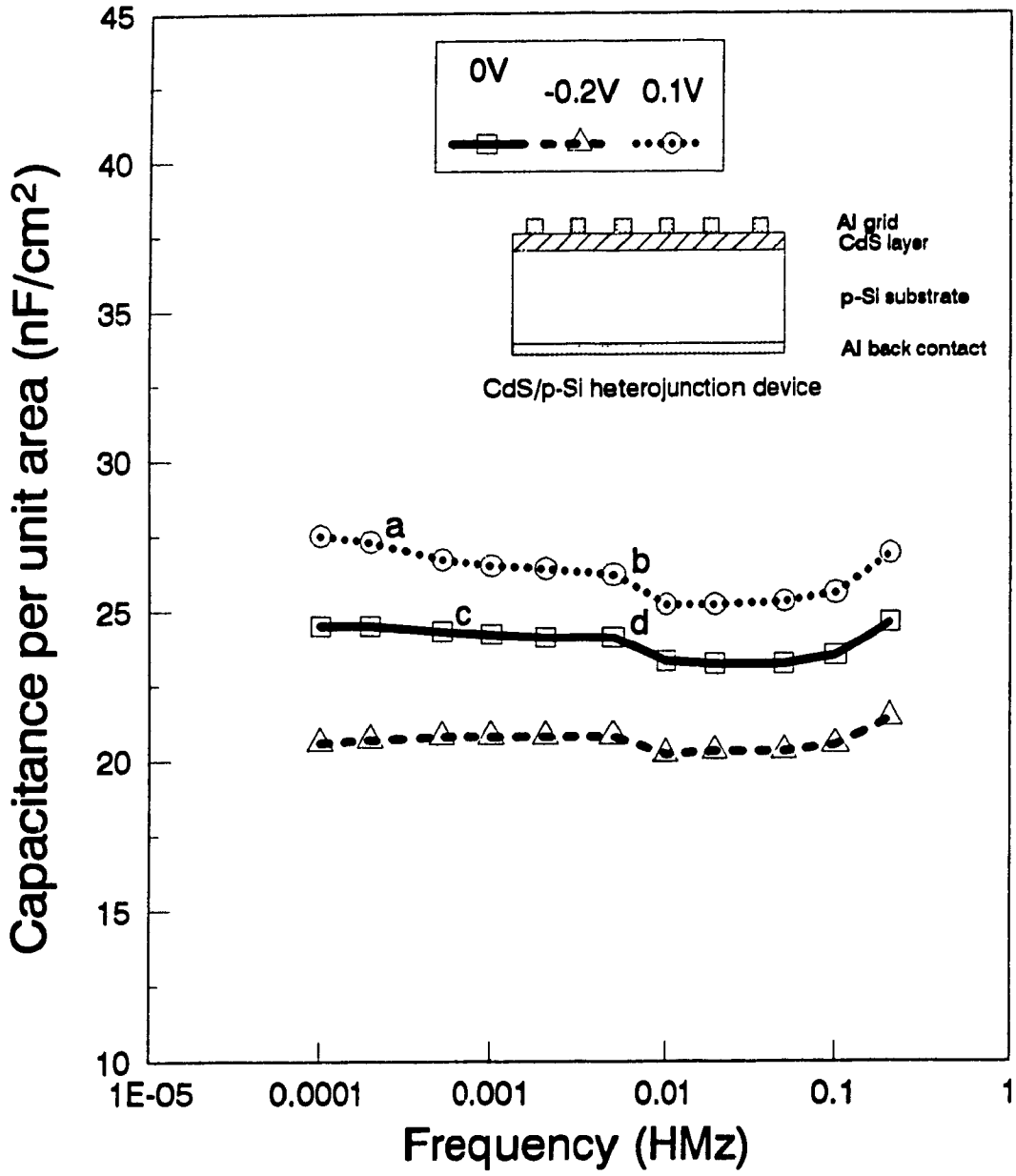


Fig. 6.22(b) Results of C-F measurements of sample 167 at 200 K.

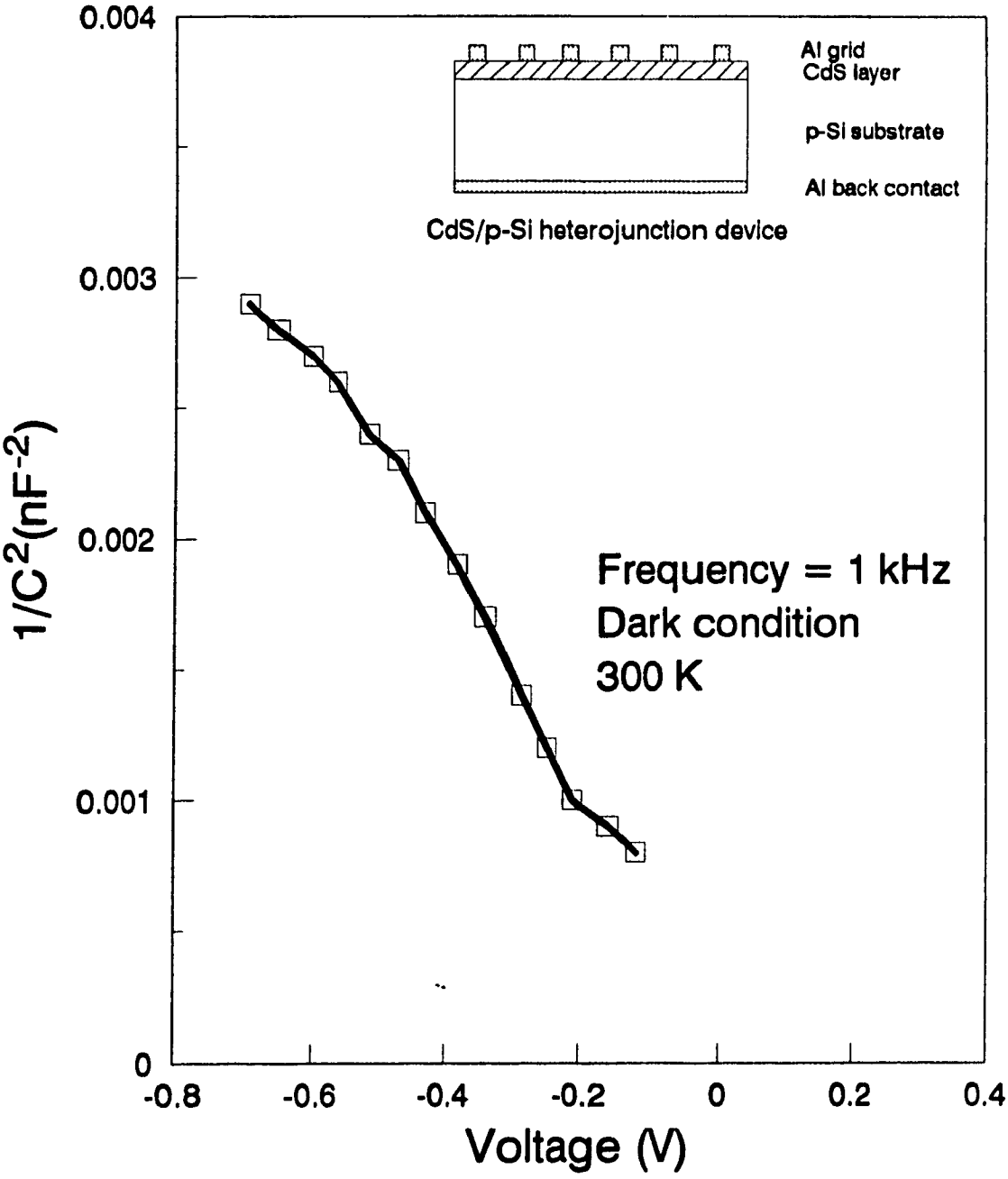


Fig. 6.23 C-V characteristics of sample 166.

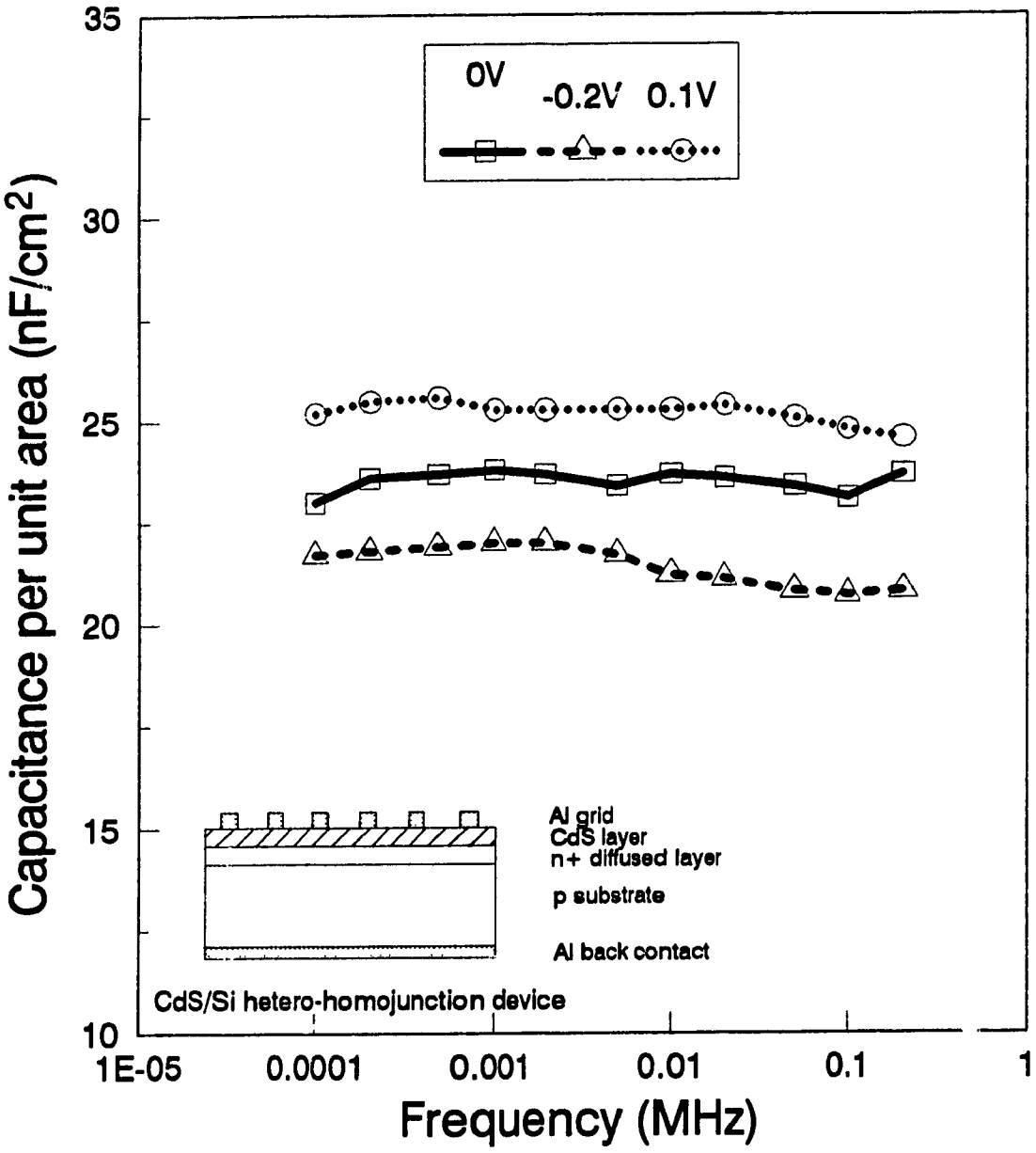


Fig. 6.24 Results of C-F measurements of sample 164 at 300 K.

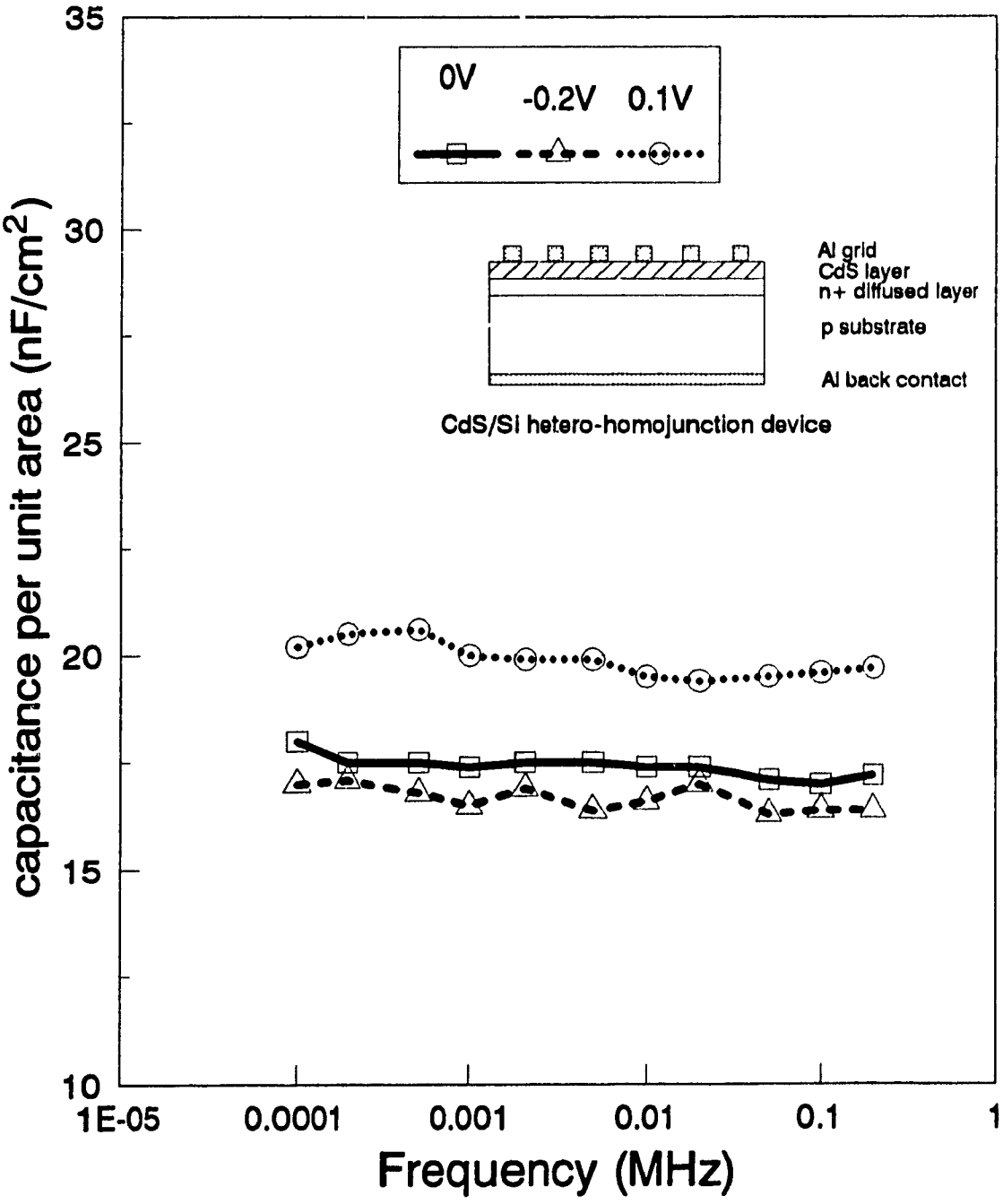


Fig. 6.25 Results of C-F measurements of sample 164 at 200 K.

Chapter 7

Conclusions

Different kinds of heterojunctions formed by CdS and monocrystalline silicon are studied and some important conclusions are summarized below.

(1) Single crystal Si homojunction cells provide larger V_{oc} than that of CdS/p-Si heterojunction cells, however, heterojunctions provide larger I_{sc} than that of homojunctions because of the wide band gap window material CdS.

(2) By adding an n-diffused layer between the CdS and the p-Si substrate, the advantages of homojunctions and heterojunctions are combined, i.e. The CdS/n-p Si configuration generates high I_{sc} and V_{oc}.

(3) In order to study CdS/n-p Si band diagrams, CdS/n-Si junctions are studied. CdS (N_D=1x10^{19} cm^{-3}) on n-Si (N_D=1x10^{19} cm^{-3}) forms a back to back n junction which bends up Using n-Si with a lower doping (N_D=5x10^{17} and 1x10^{15} cm^{-3}), a Schottky junction behaviour is ooserved.

(4) No photocurrent at 0 V bias voltage on the three CdS/n-Si devices. Small photocurrents are obtained at reverse bias which suggests that the electric fields of the three n-n junctions are too weak to collect photogenerated carriers.

(5) The C-V and I-V characteristics of CdS/n-p Si cells are similar to that of homojunctions. It suggests that the homojunction of the CdS/n-p Si cell dominates all of the electrical properties. The CdS layer acts as an electrode and only affects optical

properties of the cell.

(6) Effects of interface states on heterojunctions are studied using the C-F method CdS/p-Si cells show significant frequency dispersion on capacitance because of the lattice mismatch between CdS and Si (The crystal structure of CdS is wurtzite and that of Si is diamond. (0001)CdS on (111)Si has a 7 % lattice mismatch (0001)CdS and (100)Si do not match at all) CdS/n-p Si cells show very slight dispersion and again it confirms the electrical property domination of the homojunction of the structure. The time constants and densities of interface state are calculated

(7) By assuming the inhabitation of the trap level mechanism at low temperatures, if the C-F curves at low and room temperatures show the same dispersion, i e. same values of C_{is} and line sections, the cause of the frequency dispersion is interface states only. However, if the two curves have same C_{is} but different line sections, the dispersion is caused by interface states and trap levels. Finally, if C_{is} is smaller at low temperature, the dispersion is caused by trap level only The causes of the dispersions of the two heterojunctions examined in this work are different Trap levels and interface states cause the dispersion on sample 166 while only trap levels cause the dispersion on sample 167

(8) The densities of interface state are relatively low, therefore the voltage shifts between dark and illumination conditions are small It suggests the changes of band bending between the two conditions are less severe

(9) The nature of the interface states are acceptor-like since the capacitances are larger at low frequencies. It suggests that the apparent depletion width on the p-side becomes narrower because the space charge region contains more negative charges when

the acceptor-like interface states charge up.

Again, the light source used to test the cells performance has different spectrum and intensity from that of real AM1 condition. The performance of the cells reported in this work is not necessary the performance under AM1. However, performance comparison among different cell configurations can be done.

By adding a thin n-diffused layer between the window material and the p substrate, the advantages of the homojunction and heterojunction are combined. The larger V_{oc} is caused by the V_{bi} at the homojunction. The larger I_{sc} is obtained because high energy photons can pass through the wide band gap window material and reach the depletion region of the homojunction. The photons are collected more efficiently and the "dead" layer or surface recombination effect is less severe because less photons are absorbed at the surface Moreover, the interface state effect on CdS/p-Si heterojunctions does not affect the performance of the CdS/n-p Si cell.

The addition of the thin n-diffused layer between the window material and the p-substrate is proven to be helpful in increasing the performance of the cells. Moreover, cells with a better performance can be made by using this cell configuration. For example, a sputtered low resistivity ZnO layer can be added on top of the CdS layer or directly on an n/p Si in order to allow photons with even greater energy reach the n-p depletion region.

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Appendix I

Pertinent details of the p-type wafer

DOPANT : BORON

RESISTIVITY : 1.5-5 ohm-cm

THICKNESS . 20 mil

ORIENTATION : (100)

DIAMETER : 4 inches

MANUFACTURER : Monsanto

Pertinent details of the n-type wafer

DOPANT : PHOSPHORUS

RESISTIVITY : 1-10 ohm-cm

ORIENTATION : (111)

DIAMETER : 2 inches

MANUFACTURER : Pensilco

Cleaning Steps

1. Degreasing step

(a) Boil in trichloroethylene (TCE) for about 8 minutes, setting 6 on the hot plate.

(b) Immerse in acetone for about 15 minutes. Rinse with deionised-distilled water (D.I. water)

2. Etching step

Etch for about 5 minutes in buffered HF solution which is (49% HF solution) : (40g NH_4F + 60ml H_2O) = 1 : 7. To stop etching, dilute the HF solution with D.I. water. Rinse with D.I. water.

3. Decontamination step

(a) Boil in a solution of H_2O : H_2O_2 : NH_4OH mixed in the ratio 35ml : 10ml : 5ml at high temperature setting of the hot plate for about 8 minutes. Rinse with D.I. water.

(b) Boil in a solution of H_2O : H_2O_2 : HCl mixed in the ratio 35ml : 10ml : 5ml at high temperature of the hot plate for 8 minutes. Rinse with D.I. water, then dry the wafer by using the spinner which is set at 5000 rpm for 20 seconds.

Appendix II

Doping

1. Place the clean wafer on the spinner.

2. Set the speed of the spinner at 3000 rpm for 15 seconds

3. Switch on the vacuum pump, this will hold the wafer on the spinner while it is spinning.

4. Drop one or two drops of n-type dopant (phosphorosilicafilm) to the shiny surface of the wafer from a pipette. Note : for p+ doping, p-type dopant (borosilicafilm) is used instead.

5. Bake the wafer in a preheated oven at 150°C for 15 minutes.

Appendix III

Diffusion

1. Set the temperature of the furnace at 850°C.

2. Set the gas flow : N_2 at 2 litres/minute

O_2 at 1 litre/minute.

3. Place the wafer in a quartz boat and push the boat with a quartz rod into the center of the furnace at a rate of 25mm every minute.

4. Leave the boat in the furnace for the required time.

5 After diffusion, remove the boat slowly in the same way as it is inserted into the furnace.

Appendix IV

Aluminum evaporation

The major steps of evaporating the aluminum metal are as follow:

1. Clean the bell jar, the chamber base, the mask holder and the microglass with absolute ethyl alcohol

2 Choose proper form of mask pattern (e.g. grid pattern) and place the mask on the mask holder

3. With the tungsten wire held by the filament holder, place 9 pieces of bent aluminum wire.

4. With proper form of masking plate, place the diffused wafer on top of the mask and cover it with a piece of microglass

5 Place the bell jar in position

6. Vacuum the bell jar

7. Apply the current to melt the metal.

8 Wait for 15 minutes before exposing the wafer to air.

Appendix V

Wet oxidation

1. Clean the wafer as in appendix I

2. Set the temperature to 1100°C.

3. Set the gas flow : O_2 at 1 litre/minute

4. The oxygen flows through a cylinder which contains D I. water. The cylinder is immersed in a large beaker which contains tap water The beaker is heated by a hot plate

5 Put the wafer in the quartz boat and push it slowly at 25mm/minute until it reaches the center of the furnace.

6. Leave the wafer in the furnace for 2 hours. The thickness of the oxide will be about 0.3um.

7. Pull it out at the speed as push it in

Note: the setup is shown in Fig (A1)

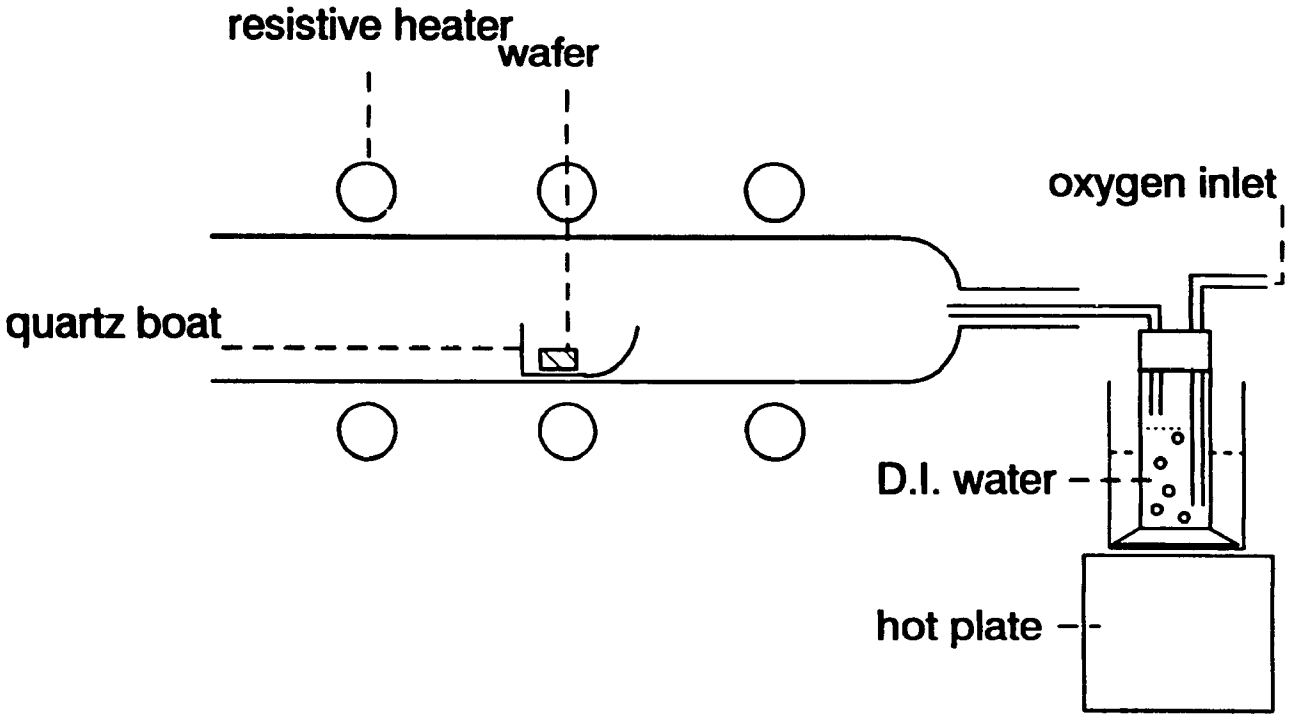

Fig.(A1) The arrangement for wet oxidation.

Appendix VI

CdS evaporation procedures

1. Set up the vacuum as in Fig. 3.2 of chapter 3. Pump it down to 10^{-6} Torr

2. Switch on the substrate heater which is controlled by a temperature controller Wait until the temperature reaches 180°C.

3 The evaporation steps are as follow.

(i) Shutter close

current dial at 70

3 minutes

(ii) Shutter open

current dial at 70

5 minutes

(iii)Shutter open

current dial at 95

10 minutes

As the bowl heating up, tap water is running through the end of the bowl holder (location H in Fig.(1) in Chapter 1) to cool it down. The deterioration of the O-ring is avoided.

4. After the evaporation steps, the substrate holder is cooled by tap water.

5. Wait until the holder reaches room temperature. Take out the samples.

Appendix VII

The following is a demonstration of how to calculate the time constant and density of interface states of a typical heterojunction device.

From the diagram, the capacitance per unit area at high frequency, C_d, is 13 5nF and the one at low frequency, $C_d + C_{is}$, is 65nF. Therefore, the approximate interfacial state density, N, is,

$$N=\frac{C_{is}}{q}=\frac{65nFcm^{-2}-13.5nFcm^{-2}}{1.6x10^{-19}C}=3.2x10^{11}eV^{-1}cm^{-2}$$

A straight line is drawn between two points on the curve and the values are (100 Hz, 60.6 $nFcm^{-2}$) and (1000 Hz, 21.3 $nFcm^{-2}$). Since C_d is 13.5 $nFcm^{-2}$, by using the equations, the new values of the two points are,

$$60.6-13.5=47.1nFcm^{-2}$$

$$(2\pi*100Hz)^2*47.1nFcm^{-2}=18594334.69nFcm^{-2}s^{-2}$$

$$21.3-13.5=7.8nFcm^{-2}$$

$$(2\pi*1000Hz)^2*7.8nFcm^{-2}=307931657.3nFcm^{-2}s^{-2}$$

The slope of this line is,

$$\frac{47.1-7.8}{307931657.3-18594334.69}s^2=1.36x10^{-7}s^2$$

The time constant, τ, is equal to the square root of $1.36x10^{-7}s^2$ which is **0.369ms**.