DESIGN OF CIRCUIT BREAKERS FOR LARGE AREA CMOS VLSI CIRCUITS

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Abstract

Large-area ICs require adequate defect-tolerance to achieve a reasonable yield. One concern is that the power distribution network is shared by a number of modules, and any single short between the supply (V_{dd}) and ground can disable all these modules. The object of this thesis is to evaluate the feasibility of incorporating circuit breakers in large area ICs, which provide protection against such defects by disconnecting the defective modules from the array. A critical analysis and comparison of MOS transistors and parasitic bipolar transistors as circuit breakers are carried out. It is shown that MOS transistors offer a better and a more practical solution than their bipolar counterparts. Several rules applicable to a MOS circuit breaker in a bulk CMOS process are defined and discussed. These rules, if strictly adhered to, are predicted to result in a design which is defect-tolerant, latch-up free and optimal in size. The design of a large MOS transistor, based on the Manhattan style of "waffle-iron" design is described. Results of two test chips provide the experimental validation of this design. The peak instantaneous current through the modules has to be known in order to realize a circuit breaker of optimal size. A preliminary analysis of a possible technique to estimate the magnitude of this worst case peak current for a CMOS combinational block is carried out. Finally a short discussion on the defect sensitivity of the power switch is presented.

Résumé

Dans les circuits intégrés de grande surface, l'obtention d'un bon rendement de fabrication requiert l'introduction d'une tolérance aux défauts adéquate. En effet, le réseau étant partagé par de nombreux modules, il suffit d'un court-circuit entre la source d'alimentation (V_{dd}) et la masse pour les affecter tous. Cette thèse évalue la faisabilité d'introduire des disjoncteurs dans des circuits intégrés de grande surface, dans le but de les protéger contre les court-circuits entre la source d'alimentation et la masse résultant d'un défaut de fabrication. Une analyse critique et une comparaison entre des disjoncteurs utilisant comme interrupteurs des transistors MOS et des transistors bipolaires parasites est effectuée. Il est démontré que les solutions utilisant des transistors MOS sont pratiques pour l'implántation de disjoncteurs, malgré l'économie potentielle de surface due à la transconductance supérieure des transistors bipolaires parasites. Plusieurs règles de conception, applicable à n'importe quel disjoncteur dans un procédé "bulk CMOS" sont discutées. Ces règles, lorsque strictement respectées, résultent en un design de disjoncteur libre de défauts et de "latchup", et de taille optimale. La méthodologie de design d'un transistor MOS basée sur un design "moule à gaufres" de style Manhattan est présentée. Les résultats des tests de deux circuits intégrés experimentaux valident expérimentalement la méthode de design. La conception d'un disjoncteur de taille optimale nécessite la connaissance du courant instantanné de pointe du module alimenté. L'analyse préliminaire d'une technique pouvant estimer l'amplitude du courant de pointe le plus élevé pouvant survenir dans un bloc de logique combinatoire est présentée. Elle est suivie, en dernier, par une discussion de la sensibilité du disjoncteur aux défauts.

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Chapter 1 Introduction

A single defect in an integrated circuit(IC) chip can cause a short circuit between the supply line V_{dd} and the ground line, thereby disabling the IC. If the chip area is small compared to the starting wafer, the associated yield may be acceptable However, as the size of the chip starts to approach that of the wafer, the yield will rapidly tend to zero unless these fatal V_{dd}-to-ground shorts are tolerated

To achieve an acceptable yield, for large area ICs, the important requirements are redundancy, testability and reconfigurability collectively referred to as fault-tolerance. The issue of fault-tolerance for large area VLSI and wafer scale integration (WSI) processing arrays have been the subject of research for quite some time [1]-[12]. Various schemes that introduce fault-tolerance in the ICs, to enhance yield and performance have been proposed in these publications.

Fault-tolerant strategies can be designed to deal with two distinct types of failures; namely production defects and operational faults. In the current technology, a relatively large number of defects categorized as production defects are expected while manufacturing a silicon wafer. These production defects are usually screened at the testing phase. Operational faults occur during normal circuit operation due to reasons such as electromigration, oxide breakdown etc. These type of faults are unpredictable and can lead to a complete system failure. Consequently, a fault-tolerant strategy that enables a system to continue processing even in the presence of operational faults is essential to achieve an acceptable yield, especially in large area ICs.

Large area circuits usually incorporate various functional modules which are interconnected in the form of an array. This type of a design facilitates error detection and allows the use of redundant modules which can replace faulty ones during testing or while the system is in operation. Typically, fault-tolerant strategies, employing such spatial redundancy are carried out in two steps. 1)Testing of the array to detect and locate faulty modules and 2) system reconfiguration to disconnect and replace each faulty module by a good one, and reroute the circuit so that a new array may be formed. This new array can also be a reduced size array leading to a gracefully degraded design.

Reconfiguration to replace the faulty module is of two main types ; hard and soft reconfiguration. Hard reconfiguration is permanent and is suitable only to avoid the use of circuitry with production faults. An example is laser linking to add connection links or laser cutting to delete connection links [13]-[17]. Soft reconfiguration, on the other hand is achieved by using some control circuitry to automatically reconfigure the array around the faults. This type of reconfiguration is flexible and can be used to handle both production and operational faults [18].

One soft reconfiguration strategy is to use independent power wires for every module. This seems reasonable for modules where the current consumed approaches the maximum current that can flow reliably through a bonding wire. However, for smaller modules, this would result in a large area overhead and any packaging cost advantage of WSI will be offset by additional off-wafer wiring [19]. A robust soft reconfiguration strategy was not available until Agarwal et al. [18] proposed an automatic circuit breaker as a feasible soft reconfiguration scheme. The idea is to provide a ground or V_{dd} circuit breaker within each module which can be used to isolate the module from the subnetwork ground or V_{dd}, thereby preventing of the other modules connected to this subnetwork from being disabled. These breakers can also be used to minimize power consumption by disconnecting otherwise good modules which remain unused after reconfiguration. Figure 1.1 shows the initial proposal [18], which assumed a bulk CMOS p-well process. The circuit breaker consists of a MOS transistor exhibiting very low on-resistance and

very high off-resistance and suitable control circuitry. During normal operation, the power transistor operates in the linear region and is sufficiently large to guarantee a low voltage drop across it, thus providing the module with an adequate virtual ground Excessive current flow through the module due to a V_{dd} -Ground short results in a voltage drop across the transistor large enough to trigger the latch, which in turn shuts off the power transistor. The mechanism which is automatic at "power up" can also be activated later with an enable input (SIN in Figure 1.1), to disconnect good but unused modules. Since the mechanism is automatic, even a module with a solid short does not prevent testing.

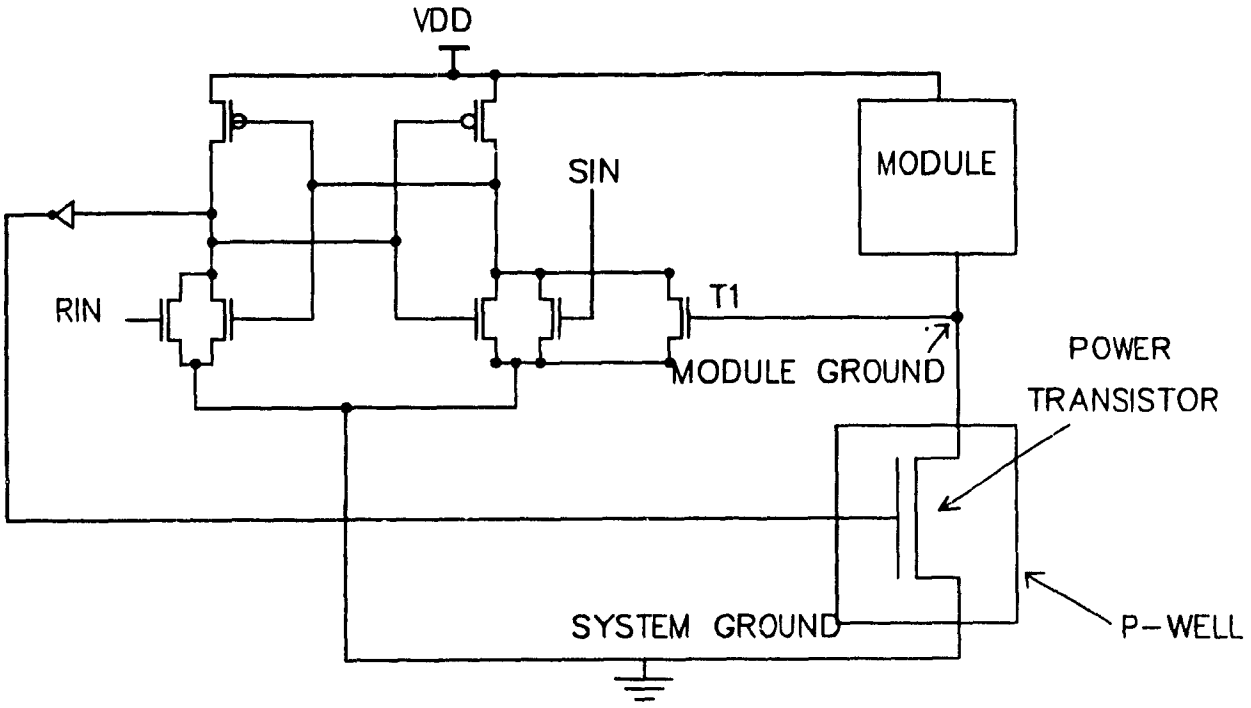

Figure 1.1 A Schematic of the Circuit Breaker

Quite recently, Carley and Maly [20] proposed the use of the parasitic bipolar transistors, which occur in every bulk CMOS process, as an alternative to the MOS transistor switching element. Two types of circuit breakers were studied The first type interrupts the V_{dd} line and employs a vertical bipolar transistor. The second type uses a lateral bipolar transistor to interrupt the ground line. It was pointed out that both

these circuit breakers are prone to latch up. Moreover, the vertical breaker introduces an undesirable design constraint and provides only a partial solution. The lateral breaker, has an inherent parasitic vertical transistor built in its structure, which is active and thus leads to 3-4 times the normal power dissipation.

Several defect-tolerant techniques studied in the field of wafer scale memory are being currently applied to WSI circuits [21]-[26]. Recently a 202Mb memory was realized on a six inch wafer [27] which incorporates breakers to prevent power line shorts in a module. This wafer consists of an array of 202 identical modules. Each module consists of a DRAM core of 1Mb density and additional configuration logic(Conlog). Each Conlog incorporates a switching transistor to cut off the DRAM power supply in the event of power line shorts in the RAM. Although no details on the design aspects of the switch are given, this is an excellent demonstration of using on-chip circuit breakers to prevent power line shorts in a module.

The objective of this work is primarily to design and characterize a nMOS transistor acting as a ground circuit breaker and to evaluate it against its bipolar counterpart. The design considerations involved in using these circuit breakers in an array of modules, are formulated. Finally the need to determine the instantaneous current through the module to design an optimum size switch is addressed, and a method to estimate this current is presented.

The original contribution of this thesis is the design of the MOS switching element and theoretical extraction of its equivalent transistor size. The design considerations evolved during group meetings with Prof. Savaria, Prof. Rumin and Mr. Mandava. Prof Savaria came up with the solution of using a circuit breaker with multiple independent transistors to prevent the system from failing due to metal-to-poly short between the drain and gate. He also proposed the idea of grouping the gates into ranks for current estimation. This idea was then developed and refined by the author into a preliminary technique to estimate the peak instantaneous current through a typical combinational circuit.

The thesis is organized in the following manner. The introduction is followed by a brief discussion of the origin, characterization and prevention of latch-up in Chapter 2. This discussion provides a basis for latch-up related issues discussed in Chapter 3.

In Chapter 3, circuit breakers employing the parasitic bipolar transistors are critically evaluated and serious objections against their use are raised. The rules which must govern the design of circuit breakers in bulk CMOS process are then addressed.

Chapter 4 describes the design of a "waffle-iron" MOS transistor using Manhattan geometry. A procedure for the extraction of the equivalent transistor width from the Manhattan-style waffle-iron transistor is developed here. The finer design changes due to the electromigration limit of metal layers are described next. The results of HSPICE simulations to determine the MOS transistor dc characteristics and switching time are then included. Finally the details of the various steps in a power transistor design are given. The results of two test chips as experimental validation of the design method are presented.

Chapter 5 is devoted to a preliminary analysis of a possible technique to estimate the magnitude of worst case peak current for a CMOS circuit. This is an important but difficult issue that must be solved before one can design a MOS circuit breaker that is near optimal in size for a particular module. Obtaining a solution to this problem is beyond the scope of the present thesis work. The chapter begins with a brief survey of the work done in this area, and is followed up by a description of the proposed method. An algorithm which estimates the worst case peak current in a combinational block is presented. The method is illustrated for a 4-bit ripple combinational adder

The thesis ends with conclusions and future directions in Chapter 6. The main part of the thesis, concerned with the design and experimental validation of MOS circuit breakers for short-circuit protection of large area ICs was presented in the Third Wafer-Scale-Integration Workshop [28].

Chapter 2 Latch-up

2.1 Latch-up in CMOS

The purpose of the following brief discussion on latch-up is to provide a basis for the discussion in Chapter 3. This Chapter is summarized from a book titled "Latch-up in CMOS Technology" by R.R Troutman. All the references pertaining to the material in this Chapter can be found in the book.

CMOS ICs using n and p wells have inherent problems due to their structure which produces parasitic p-n-p-n devices that can exhibit in addition to high impedance state, a fatal low impedance latched state which can destroy the entire chip. Latch-up occurs when a stimulus triggers the p-n-p-n to switch to its low impedance state. The current/voltage characteristic of such a p-n-p-n structure is shown in Figure 2.1.

The thyristor configuration that is inherent to the CMOS structure is shown in Figure 2.2 which superposes the bipolar equivalent circuit of a CMOS inverter on its cross-section [29]. There are two vertical parasitic n-p-n bipolar transistors, V_{T1} and V_{T2} formed by the n^+ source/drain diffusion, the p-well and the n-type substrate. When forward biased , the n^+ diffusion serves as an emitter and injects electrons into the p-well base, and the reverse biased p-well/substrate junction collects the unrecombined electrons. Likewise there are also two lateral p-n-p bipolar transistors, L_{T1} and L_{T2} formed by any p^+ source/drain diffusion, the n-type substrate, and the p-well. Likewise,

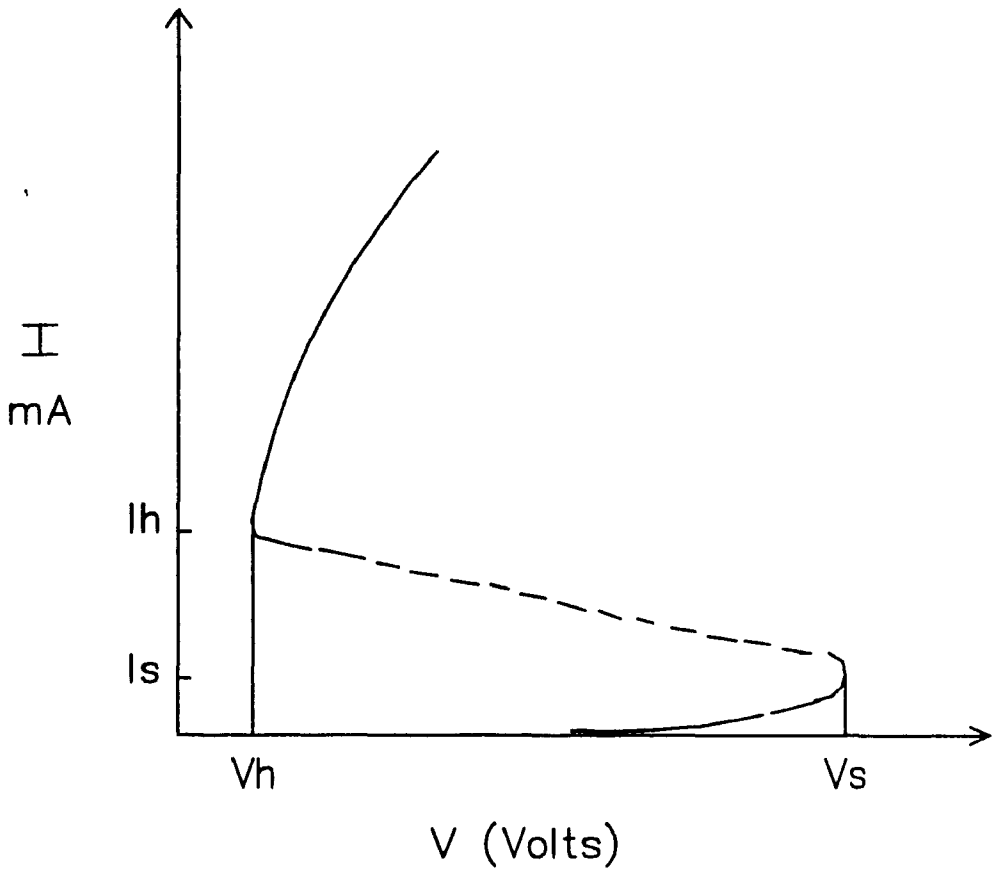

Figure 2.1 p-n-p-n Current/Voltage Characteristics

the n-type substrate serves as a base for lateral p-n-p(s) and the collector for vertical n-p-n(s). From Figure 2.2 it can be seen that when substrate current flows, a voltage drop will be developed across the resistance R_{s1}, R_{s2}, R_{s3} and R_{s4}. This drop, if large enough, can forward bias the emitter/base junction of the p-n-ps L_{T1} and L_{T2}. In a similar fashion, any p-well current can turn on the vertical n-p-ns. This condition can lead to latch-up when the sum of current gains (α) of n-p-n and p-n-p exceeds unity and the current through the p-n-p-n device reaches the switching value I_s, shown in Figure 2.1. Latch-up is sustained if the p-n-p-n structure continues to remain in the low-impedance state even after the triggering stimulus is removed.

The current/voltage characteristic shown in Figure 2.1 is observed for a specific p-n-p-n structure and depends on how switching is initiated [29]. Since a p-n-p-n

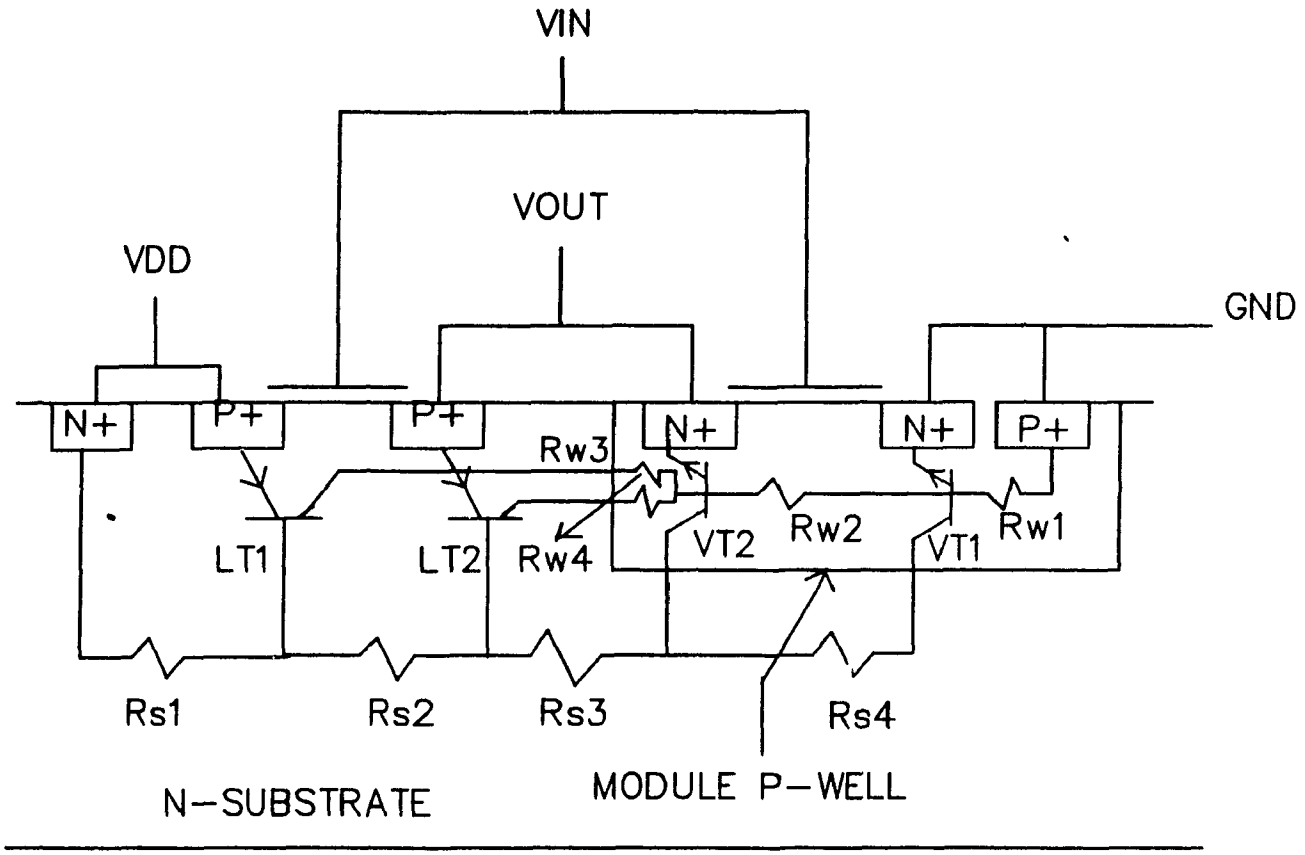

Figure 2.2 Parasitic Bipolar Portion of a p-well CMOS Inverter

structure is really a 4-terminal device, the observed characteristic also depends on the terminal conditions of the p-well and substrate contacts. Different connections for these terminals could produce qualitatively different characteristics.

2.2 Triggering Modes

Various excitations can trigger latch-up[29]. The more common triggering modes are

(i) External initiation of a bipolar transistor [30].

The excitation is often generated by an overshoot or by undershoot at an

input and/or output node. This results in the injection of charge carriers into the well or substrate, causing an ohmic drop. If large enough, such a drop can turn on one of the bipolar transistors and latch-up follows if this transistor turns on the other parasitic bipolar transistor.

(ii) Normal bypass current initiation of both bipolar transistors

In this type of triggering, the excitation causes current to flow through both bypass transistors, V_{T1} and L_{T1}. If large enough , the bypass current turns one of the parasitic bipolar transistors, whose collector current then supplements the bypass current to turn 'ON' the other. The excitation in this case is usually avalanche current, photocurrent [31] or displacement current through the well/substrate junction. The avalanche current is due to a rise in power supply voltage across the reverse biased p-well/substrate junction high enough to cause a substantial avalanche current that will trigger latchup. Various forms of radiation can produce hole/electron pairs throughout the silicon substrate. These photo-induced electron-hole pairs can produce majority carriers in the substrate and the p-well leading to latch-up. An extremely rapid ramping of the power supply or an extremely large transient on the power supply line causes a displacement current through the RC circuit formed by the two bypass resistors, R_{s1} and R_{w1} and the p-well/substrate junction capacitance. This displacement current can turn on either the lateral p-n-p or the vertical n-p-n, depending on the magnitude of the associated bypass resistor [31], [32].

2.3 Prevention of Latch-up

Considerable effort is being made to reduce this problem. Latch-up can be prevented by holding below unity the sum of effective small- signal, common base current gains (α) for the two transistors This ensures that the parasitic p-n-p-n structure is in the blocking state. This can be accomplished by the following two general strategies, 1) bipolar spoiling and 2) bipolar decoupling. All latch-up protection techniques follow

at least one of these strategies. In the former, one deliberately includes steps in CMOS fabrication to spoil transistor action by either reducing carrier lifetime or injection. Spoiling techniques attempt to either reduce base minority carrier lifetime [33],[34] or degrade emitter injection efficiency[35],[36] to prevent latch-up.

In the latter strategy, processing techniques (alone or in combination with layout techniques) are used to decouple the bipolars so that collector current of one transistor cannot turn 'ON' the other. Several processing techniques to achieve bipolar decoupling are possible. A highly doped substrate beneath a lightly doped epitaxial layer very effectively shunts the parasitic bipolar [37]. A retrograde well can also be used to reduce the well sheet resistance thereby lowering the bypass resistances. [38], [39],[40].

The layout techniques, used to decouple parasitic bipolar transistors, are the only tools available for the CMOS circuit designer to assist in reducing the latch-up. Two types of guard structures have been used: majority carrier guards, and minority carrier guards, and the decoupling action differs for the two. Minority carrier guards are used to collect injected minority carriers before they can cause a problem. A minority carrier guard ring can be a reverse-biased source/drain diffusion or an additional well diffusion Since carriers injected by a parasitic emitter in the well travel primarily downward to the collector, minority carrier guards at the surface have little effect on the vertical transistor. Hence the minority carrier guards are more frequently placed in the substrate than in the well. The guard encloses the potential emitter to prevent all possible latch-up paths. The majority carrier guard ring, on the other hand, decouples the bipolars by minimizing the voltage drop created by majority carrier currents. A majority guard ring is of the same doping type as the background, for example a p^+ diffusion in a p-well or an n^+ diffusion in an n-type substrate The p^+ and n^+ guard rings are connected to ground and power supply respectively.

Chapter 4, discusses the precautions taken in the design of circuit breaker to prevent latch-up.

Chapter 3 Design Considerations of Circuit Breakers

This chapter begins with a comparison and evaluation of MOS and bipolar circuit breakers. In the next section the design considerations for MOS circuit breakers are discussed.

3.1 MOS versus Parasitic Bipolar Breakers

Bipolar transistors exhibit a lower dynamic resistance than MOSFETs of similar feature size [41]. This should make the bipolar circuit breaker inherently superior and preferable to the MOS breakers. However in CMOS circuits the bipolar parasitic transistors offer no big advantages as discussed below. A p-well process is considered here for the sake of discussion. A similar analysis holds for a n-well process without loss of generality. Carley and Maly [20] provide two solutions of circuit breakers employing parasitic bipolar transistors inherent in every bulk CMOS process shown in Figures 3.1 and 3.2. A vertical n-p-n transistor is used as a V_{dd} breaker and a lateral n-p-n as a V_{ss} (ground) breaker.

The breaker incorporating the lateral n-p-n transistor is a ground breaker and so it is compared with the nMOS solution shown in Figure 1.1, which also interrupts ground. The serious drawback is that for V_{ss} breaker, a vertical n-p-n exists along with the lateral n-p-n. The vertical n-p-n is formed due to the forward biased emitter base diode of lateral n-p-n, and the n-substrate. This vertical transistor is active and it

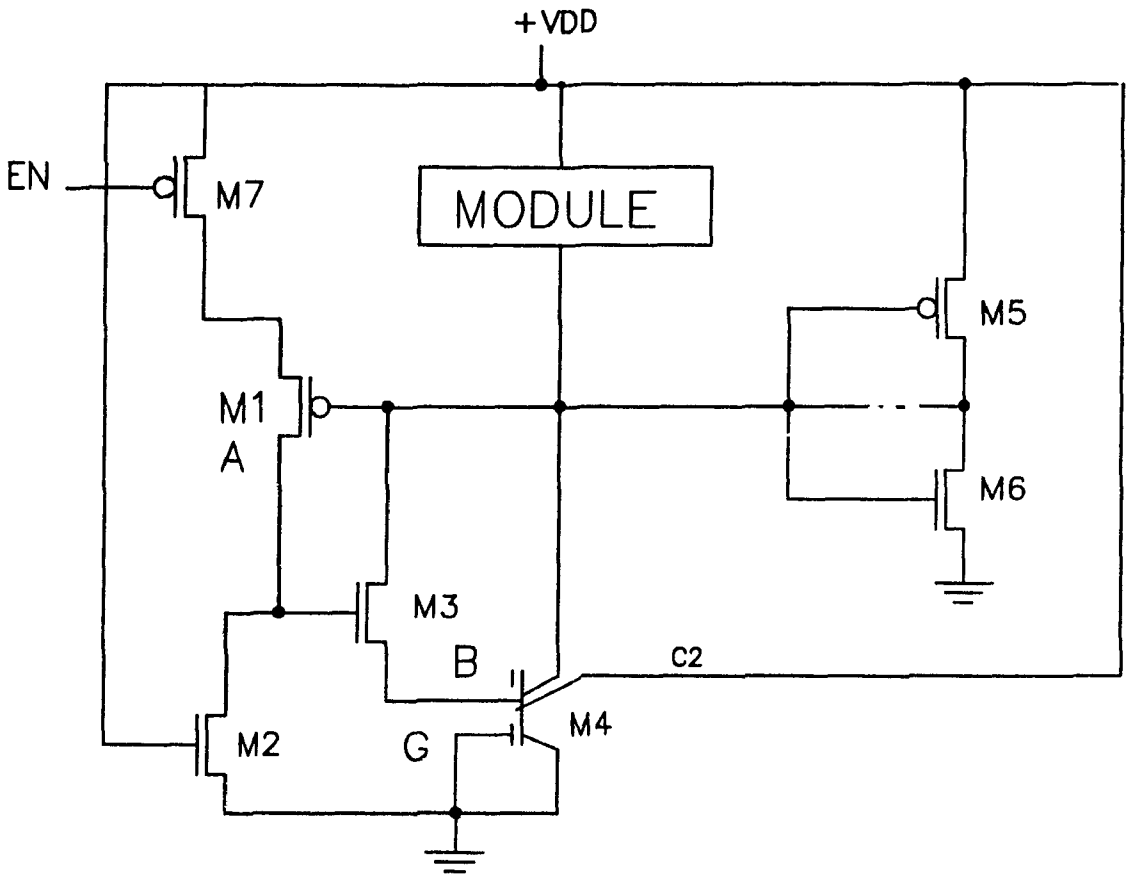

Figure 3.1 Schematic of the Vss Breaker (Bipolar)[20]

detracts from the performance of the lateral transistor. The results of Carley and Maly indicate that the substrate current injected by the vertical n-p-n is typically greater than the lateral current and at some base voltages, injects into the substrate 2 to 3 times the current it does into the modules. Therefore the system power dissipation will increase by a factor of 3 or 4 over the normal power required. This rise in power consumption is significant and obviously undesirable since a wafer can easily dissipate power in excess of 100 W. In addition, the substrate current can lead to latch-up by forward biasing the collector/base junction of the lateral p-n-p. Therefore the current has to be collected very efficiently by placing the guard ring close to the n-p-n transistor for maximum efficiency. This poses the threat of a hot spot problem when large currents are handled by the switch. The adverse effect of the vertical bipolar transistor increases

with the emitter area of the lateral transistor. Thus there is a limit on the emitter area and hence the maximum current that can be handled by the switch.

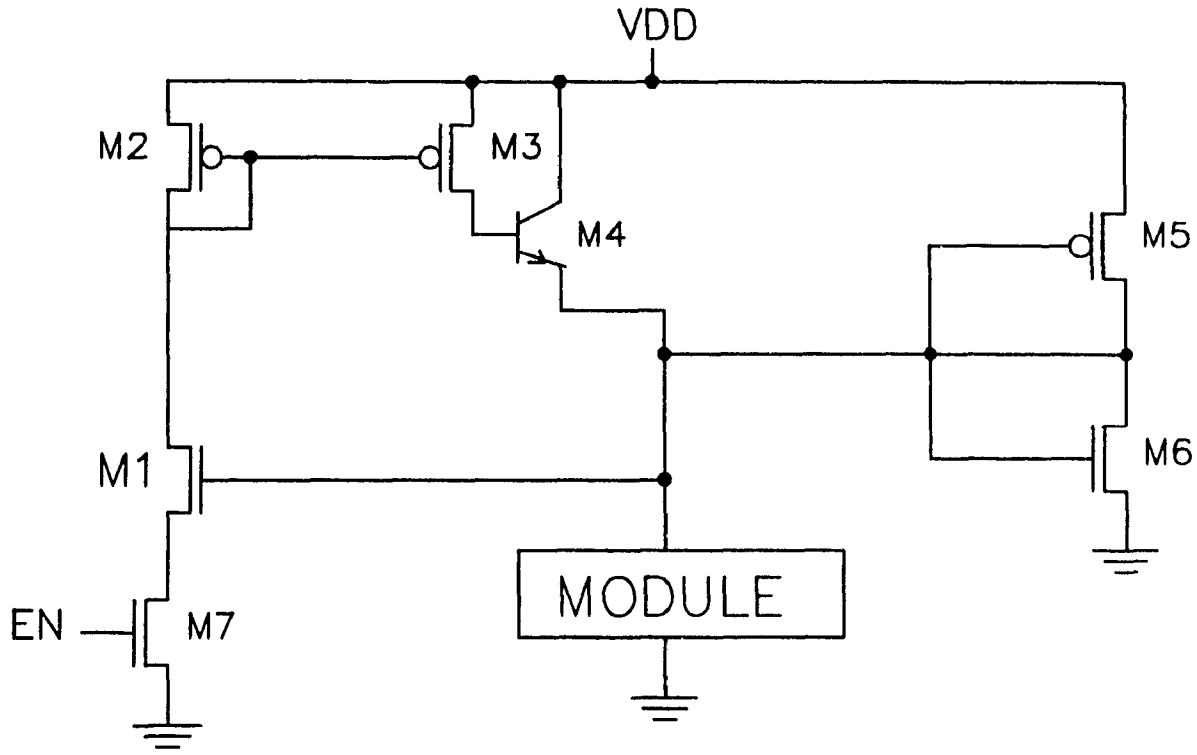

Figure 3.2 Schematic of the Vdd Breaker (Bipolar)[20]

Next we consider the vertical n-p-n, V_{dd} circuit breaker. Carley and Maly mention that since the circuit breakers interrupt the V_{dd} line, the power distribution network has to be separated from the substrate bias network. If the substrate is shorted to V_{dd} within any module, a large current will be drawn directly through the substrate into the shorted module which would induce latch-up by forward biasing the collector/base junction of the lateral p-n-p. There is no way of avoiding this current flow through the substrate in the event of a V_{dd} to V_{ss} short, even if the V_{dd} and the substrate are routed separately. Since there is no practical solution to this problem, the substrate bias network, which occupies a large area, remains unprotected against a short to V_{ss}.

Thus, use of the vertical n-p-n circuit breaker is an incomplete solution to prevent V_{dd} - V_{ss} short. Also routing the V_{dd} and the substrate contacts separately introduces an undesirable design constraint and a severe area overhead unaccounted for in [20].

In conclusion, parasitic bipolar transistors, cannot be considered as a practical solution for implementing circuit breakers, despite the potential area savings associated with the better transconductance.

3.2 Design Considerations of Circuit Breakers

The MOS circuit breakers do not suffer from any of the serious drawbacks discussed above for bipolar circuit breakers. The following set of design rules if strictly adhered to, will result in an optimum size circuit breaker which is almost latch-up free. Bus clamping by a shorted module is also prevented using one of the design rules, as explained in this section[28].

- **Rule 1 : Only the well bias potential can be safely interrupted.**

Figure 3.3 shows the consequence of trying to interrupt the substrate potential by using V_{dd} circuit breakers for a p-well process. A pMOS switch would be used as a breaker if defective modules were to be disconnected from V_{dd}. However, since the n substrate in a p-well process is shared by the entire wafer the substrate would still be pulled to ground even if only one module had a short between V_{dd} and ground. Hence the breaker must be in the well, which means that V_{dd} breakers are used in the n-well process, while ground is disconnected in a p-well process. An alternative to avoid interrupting the well bias potential is a separate distribution of the supply voltage to the module and to the substrate But this is an incomplete solution, because the wiring for the distribution of the substrate potential cannot be protected and, in the presence of a short, it is not possible to avoid large currents flowing through the substrate. In CMOS, a safe protection is ensured by interrupting a well bias potential. To realize this, a nMOS switch in a p-well process and a pMOS switch in an n-well process should

be employed. Since the electron mobility is 2.5 times the hole mobility in silicon, the area overhead associated with MOS circuit breakers in n-well processes will tend to be 2.5 times higher.

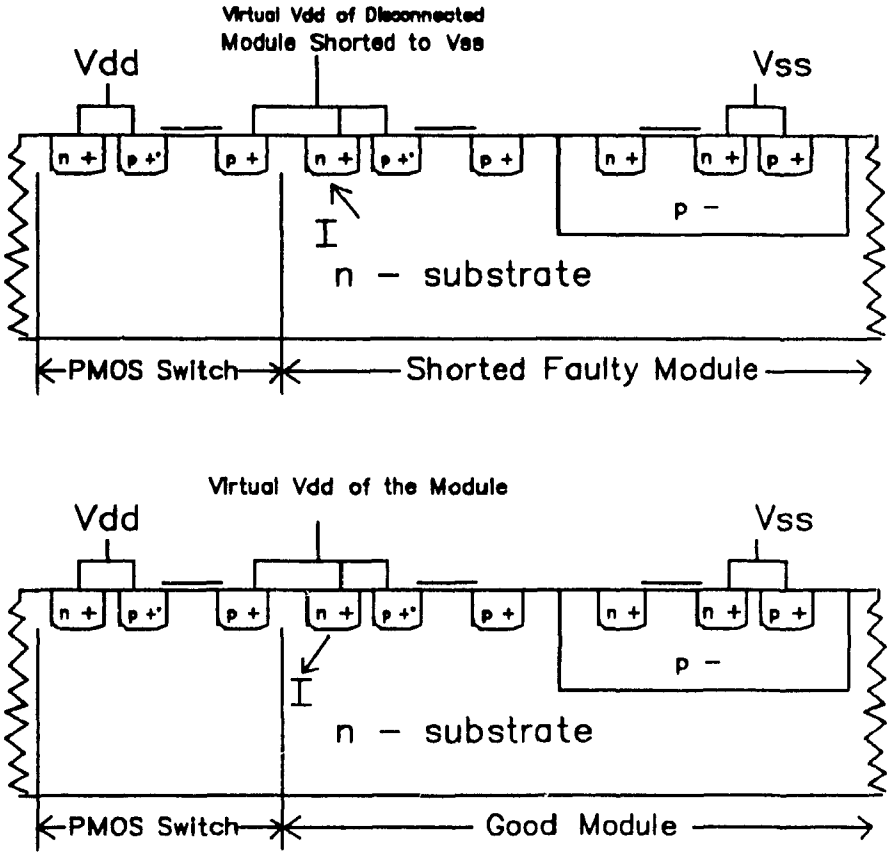

Figure 3.3 Structure Depicting the Possible Existence of Shorts Through the Substrate

- **Rule 2 : Interconnecting transistor drains outside a module is not permitted.**

Figure 3.4 shows modules interconnected, through their respective buffers, in parallel to a bus. Each buffer is in a different module having n-transistors located in the p-wells, with different virtual ground potentials. If one of the breakers is turned off because of a supply-to ground short, its virtual ground will float up to a maximum of V_{dd} due to the short. In this case a voltage equal to the forward biased drop of a

diode is observed across the drain-to-well junction of the n transistor belonging to this shorted module. This results in the clamping of the bus at one diode drop below V_{dd}. Hence this type of interconnections between the modules has to be strictly avoided.

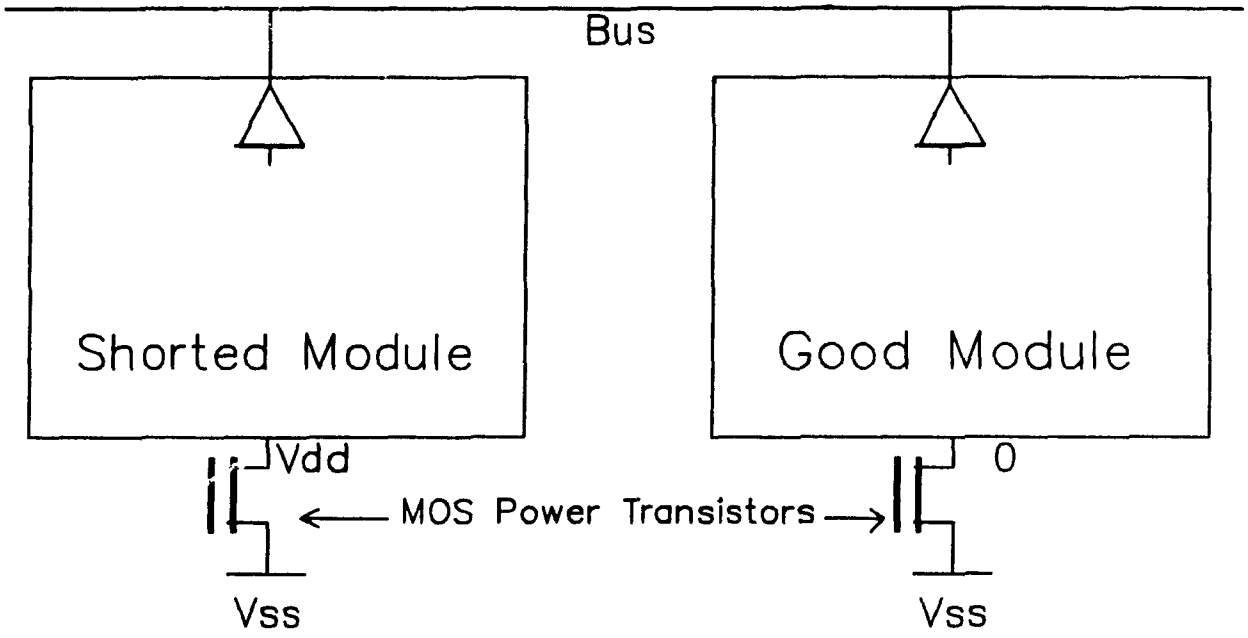

Figure 3.4 Diffusion-Interconnected Modules Which Result in Bus Clamping

The above situation cannot occur if the modules are connected via the gates of the transistors. Figure 3.5 illustrates the poly-interconnected modules. Here the link from a module is terminated on gates, so there does not exist a low impedance path between drains of switches on separate modules.

Consequently, if a bus is required to interconnect separate modules, the bus and the associated drivers are placed in a separate module as depicted by Figure 3.6. This bus implementation no longer has the diffusions in separate modules connected. Alternatively, the drivers connected in parallel can remain in their respective modules, if the last transmission gate in every signal path is kept in the bus module. In the above cases the signal which shuts off the power transistor should be used to put the tristate output buffers/transmission gates in a high impedance mode.

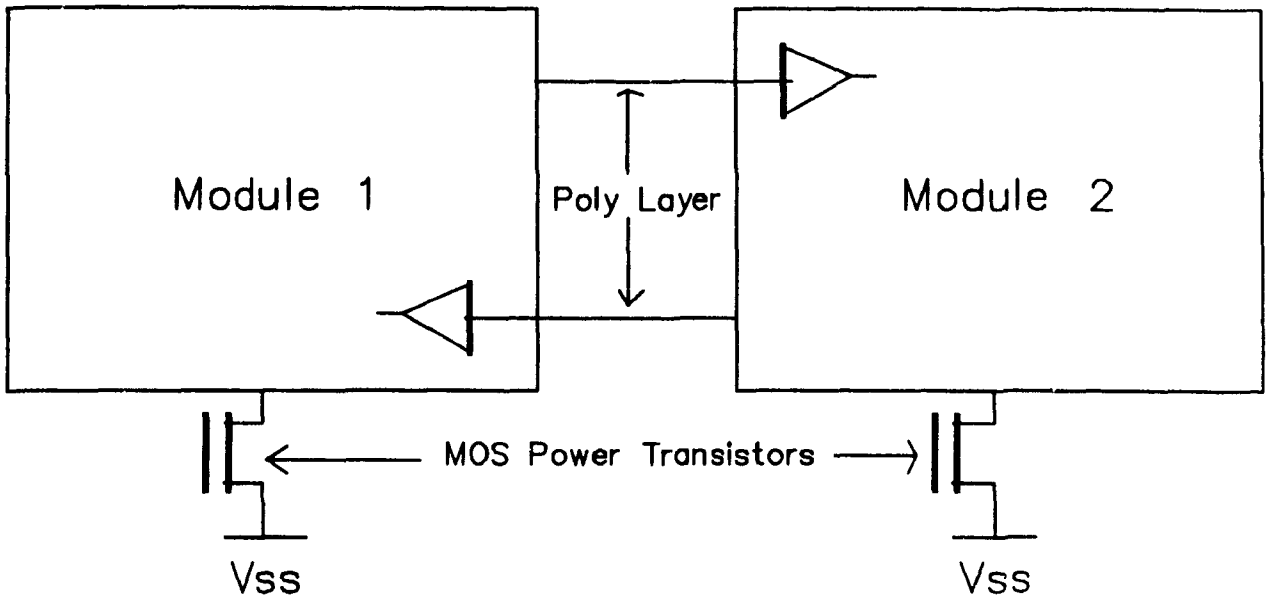

Figure 3.5 Poly-Interconnected Modules

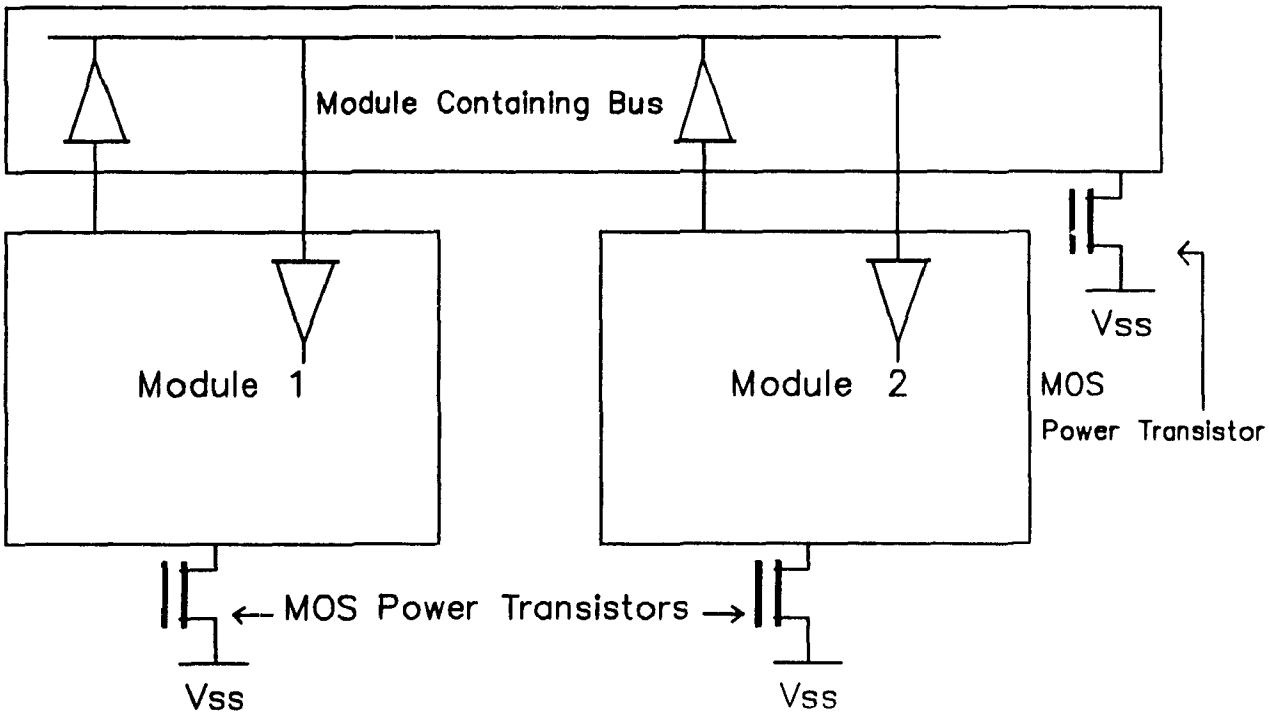

Figure 3.6 Bus Implemented Without Connecting Diffusions in Separate Modules

• **Rule 3 : The maximum peak (dynamic) voltage drop across the breaker must be limited to 700mV.**

The presence of dynamic storage nodes, as shown in Figure 3.7, is a factor limiting the peak breaker drop that can be safely tolerated. Whenever there is a large dynamic node with a capacitance to the common substrate potential , any noise temporarily raising the virtual ground potential above 700 mV can trigger latch-up if the parasitic capacitance to the substrate is large enough. The reason is when the virtual ground potential exceeds 700mV due to substrate noise, the well/drain junction with a dynamic node acts as the forward biased base/emitter junction, charging the associated capacitance w.r.t the substrate. This would then cause electron injection into the well giving rise to a current through the well. If the charging capacitance is large enough, the magnitude of this current will be large, which in turn can cause latch-up by turning on the vertical n-p-n in the well. It should be noted that though this carrier injection is most likely momentary and so, latch-up may not be sustained due to the capacitive nature of the load, there is still a definite possibility.

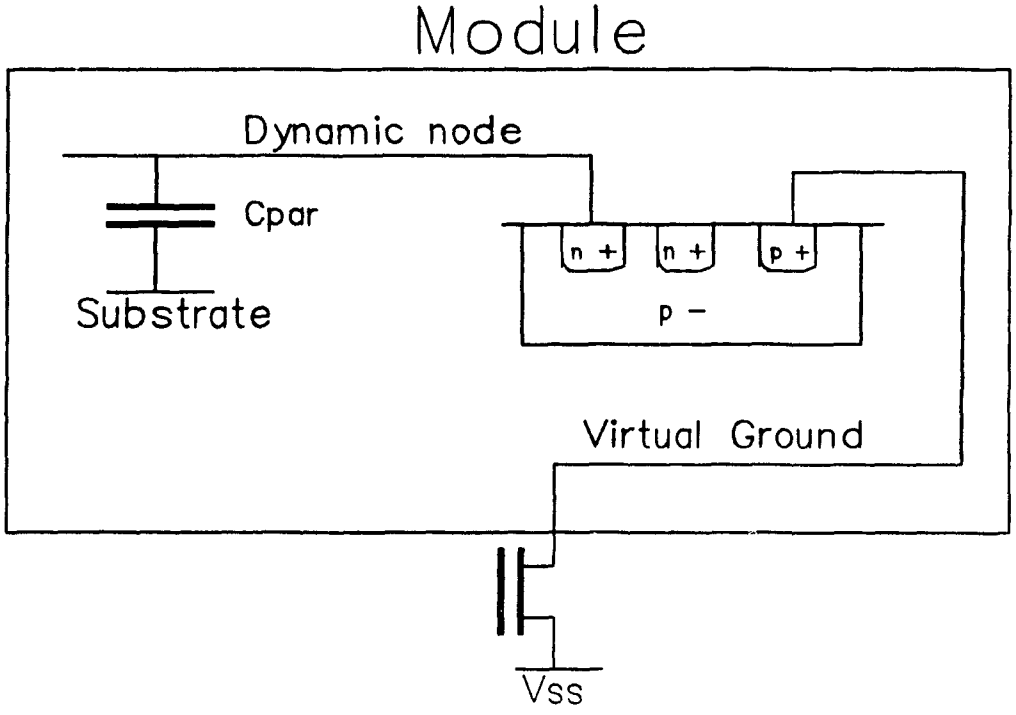

Figure 3.7 A Module With Large Dynamic Nodes

We can see in Figure 3.7 that a pair of n-diffusions along with the well p-region can constitute a lateral n-p-n parasitic transistor. Consider the case where one

diffusion is connected to a dynamic node storing V_{dd} while the adjacent diffusion is a dynamic node at 0. In the presence of a virtual ground noise over 700mV even if latch-up is not initiated, the resultant bipolar can leak. A dynamic node storing V_{dd} can leak down to almost 0 V in some situations. The presence of dynamic nodes thus imposes the principal limit on the peak virtual ground noise. Considering that significant leakage could result well before the base to emitter junction of the lateral n-p-n is fully turned on, the use of dynamic nodes would thus require a peak virtual ground noise smaller than 700mV (500mV for example).

Interestingly, if the modules contain no dynamic nodes and if they are connected through transistor gates as shown in Figures 3.5 and 3.6, they could safely be operated with virtual ground potentials that differ by more than 700mV since the voltage developed inside the well will not be sufficient to turn on the parasitic bipolar transistor discussed above.

The size of the breaker decreases with the increase in the maximum drop that can be safely tolerated in normal conditions. This tradeoff between the size and peak voltage drop decides a lower bound to safe operating peak voltage drop across the breaker. At lower supply voltage, a lower voltage may be desirable. Large voltage drops may of course be tolerable if their duration is short in comparison with the clock period.

Considering rules 2 and 3, a maximum peak voltage drop of 300 mV drop across the power transistor was considered as reasonable. This maximum peak voltage provides adequate margin to prevent any inadvertent triggering of the latch and requires a reasonable size transistor.

- **Rule 4 : The maximum peak current must be computed**

Clearly the maximum peak current associated with a module fixes the size of the circuit breaker for an acceptable peak drop across it. So the breaker cannot be optimized unless this instantaneous peak current is known. Predicting this current is

a difficult problem which is still open. An attempt has been made here to determine an upper bound to the peak current of a combinational block. Chapter 6 gives more details on this current estimation method.

- **Rule 5 : After testing a module, turning off power via the breaker is a latch-up hazard**

Referring again to Figure 3.7, one remarks that, if a large dynamic node is set to 0 during testing, and the module containing the node is later turned off via the breaker, latch-up can be triggered when the virtual ground potential rises. This is again due to the charges injected as a result of a forward biased well-to-drain junction as explained earlier. This phenomenon is inherently transient and is only harmful if latch-up spreads beyond a module's boundary. Assuming that the parasitic capacitance is not extremely large and that each module is surrounded by guard rings to prevent spreading, that mechanism should not be a problem.

If it does happen to be a problem, a robust solution exists. This consists of ensuring that, after testing, the system is turned off via the main supply for a time sufficient to allow all the internal nodes to discharge. The system is repowered with all breakers in the off state, and only the modules which will be part of the final configuration are turned on. This sequence guarantees that no dynamic node can charge to 0 in a module that will not be used. In summary, testing can be followed by a cold restart rendering the described latch-up induction mechanism impossible.

Chapter 4 Design and Test of Circuit Breakers

This chapter discusses the relevant aspects of a MOS power transistor design. The equivalent width of the MOS transistor to achieve the type of low "ON" resistance discussed earlier can be several millimeters. To reduce the area overhead associated with the circuit breaker, an efficient method such as the "waffle-iron" was used [42] The power transistor is built by replicating an elementary cell composed of a contact surrounded by four gate segments. The CMOS 3DLM single poly double metal process rules were used to layout the power transistor.

4.1 Cell Dimensions

The first step in the design phase was to determine the dimensions of this elementary cell. Figure 4.1 shows a typical cell of an "waffle-iron" layout. A simple calculation indicates that a cell with smallest dimensions, L and W as allowed by the design rules, maximizes the ratio of the equivalent transistor width (ETW) of the MOS transistor to the area utilized.

L and W are the minimum dimensions allowed by design rules

$$\frac{ETW}{Area} = \frac{2(L+W)}{L*W} \tag{4.1}$$

Factoring the right hand side of the above equation

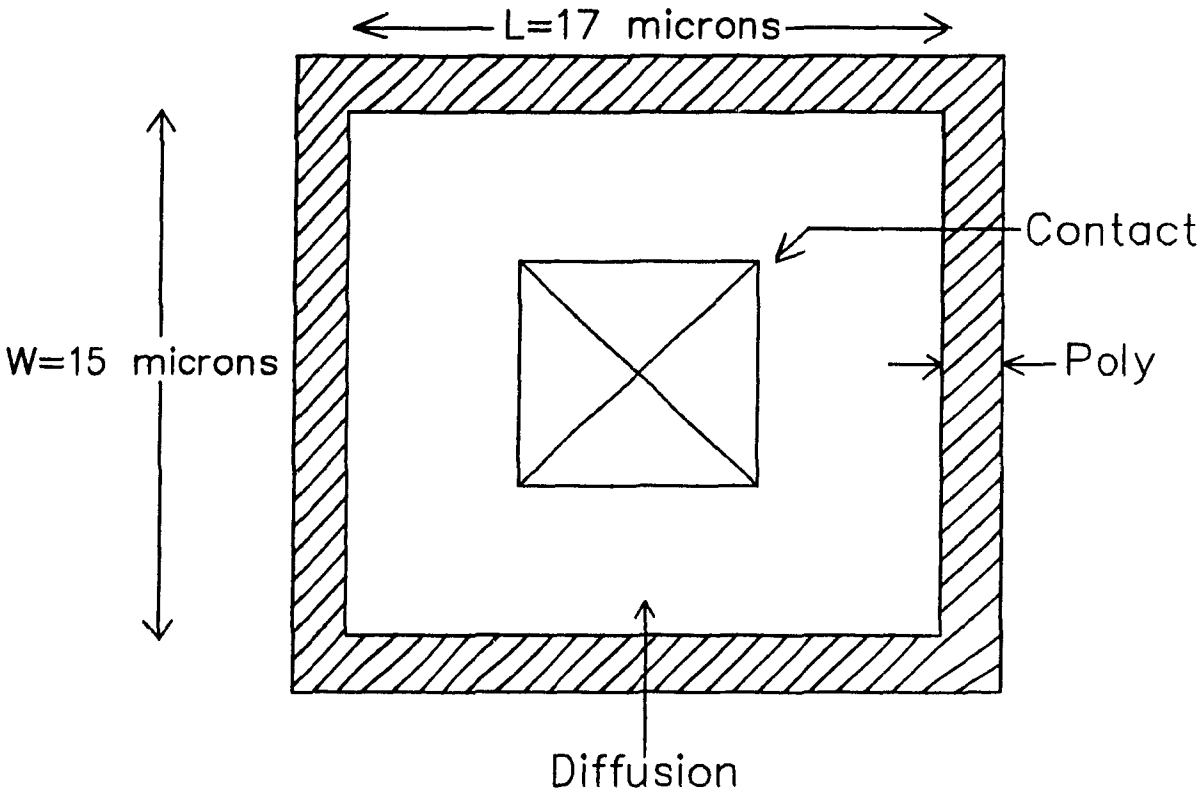

Figure 4.1 Typical Cell of a "Waffle-Iron" Layout (enlarged)

gives

$$\frac{ETW}{Area} = \frac{2}{L} + \frac{2}{W} \tag{4.2}$$

Now if L and W are increased by $e_1 > 0$ and $e_2 > 0$ respectively

$$\frac{NewETW}{Area} = \frac{2(L + W + e_1 + e_2)}{(L + e_1)(W + e_2)} \tag{4.3}$$

The right hand side can be factored to give

$$\frac{NewETW}{Area} = \frac{2}{(L + e_1)} + \frac{2}{(W + e_2)} \tag{4.4}$$

For any $e_1 > 0$ and $e_2 > 0$

$$\frac{2}{(L+e_1)} < \frac{2}{L} \qquad (4.5(a))$$

$$\frac{2}{(W+e_2)} < \frac{2}{W} \qquad (4.5(b))$$

from (4.2), (4.4), (4.5)

$$\frac{NewETW}{Area} < \frac{ETW}{Area} \qquad (4.6)$$

Equation 4.6 clearly shows that the area used is most efficient if the basic cell has the smallest allowable dimensions.

Two design variations of waffle-iron layout as shown in Figure 4.2 were considered. The Manhattan-style in Figure 4.2(a) has a higher ETW/Area equal to (.046) compared to .036 of the version in Figure 4.2(b). So the Manhattan-style design was adopted for laying out the power transistor.

4.2 Equivalent Transistor Width Extraction

Figure 4.4 depicts the three types of cell that the layout is composed of. Core cells are surrounded by 4 cells. The peripheral cells, are further grouped into edge and corner cells which are surrounded by 3 and 2 cells respectively. Therefore the number of transistors, contributed by each of the corner, edge and core cells are 2/2, 3/2 and 4/2 respectively. The factor 1/2 appears as every transistor is counted twice, once for the cell containing the source contact and once for the drain contact. Extraction of the ETW from the Manhattan-style waffle-iron transistor, which is nominally 10 mA @

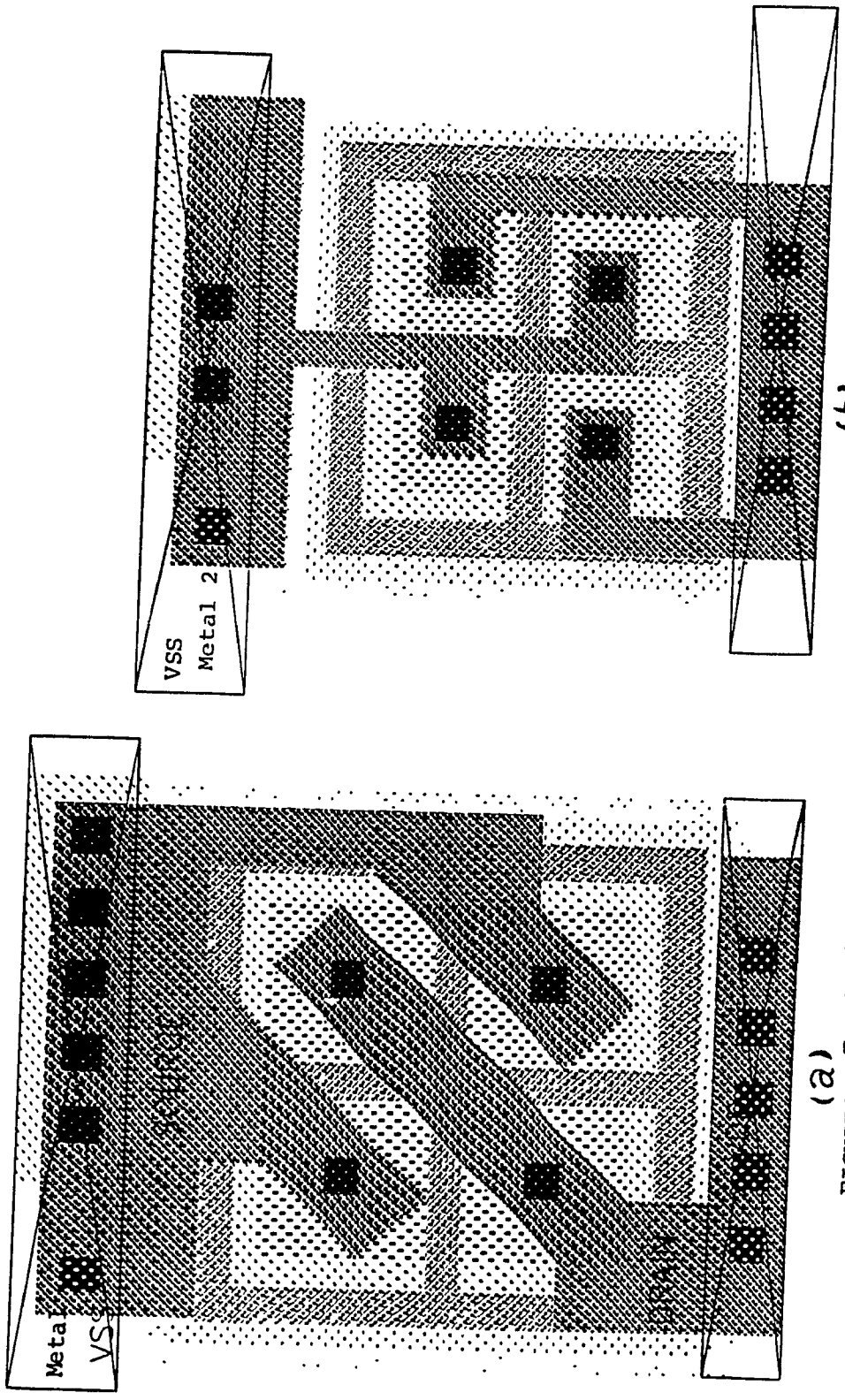

FIGURE4.2 Two Design Variations Of Waffle-iron Layout

300 mV device, proceeds as follows. A layout with X and Y cells in x and y directions respectively has 4 corner cells, 2(X+Y-4) edge cells and (X-2)(Y-2) core cells.

The number of individual transistors the layout is made up of is equal to

$$\left(2/2 * \#\text{of corner cells} + 3/2 * \#\text{of edge cells} + 4/2 * \#\text{of core cells}\right) \tag{4.7}$$

Substituting the unknowns in the above equation

$$N = \left(2/2 * 4 + 3/2 * 2 * (X + Y - 4) + 4/2 * (X - 2)(Y - 2)\right) \tag{4.8}$$

The dimensions of a single cell are L and W in x and y directions respectively. From (4.8) the equivalent transistor width W_{eqvt} is given by

$$W_{eqvt} = \left(2/2 * (2L + 2W) + 2 * (X - 2) * \frac{(2L + W)}{2} + 2 * (Y - 2) * \frac{(2W + L)}{2} + \right.$$

$$\left. + (X - 2)(Y - 2)(L + W)\right) \tag{4.9}$$

A unit cell in the Manhattan-style waffle-iron transistor layout has the minimum dimensions of 17 and 15 microns respectively in the x and y directions respectively. Therefore the equivalent transistor width in a 5 micron design scale is given by

$$W_{eqvt}(5\mu m) = 2 * (17 + 15) + 2 * (X - 2) * (17 + 15/2) + 2 * (Y - 2) * (15 + 17/2) +$$

$$+ (X - 2) * (Y - 2) * (17 + 15) \tag{4.10}$$

$$W_{eqvt}(3\mu m) = W_{eqvt}(5\mu m) * 0.6 \tag{4.11}$$

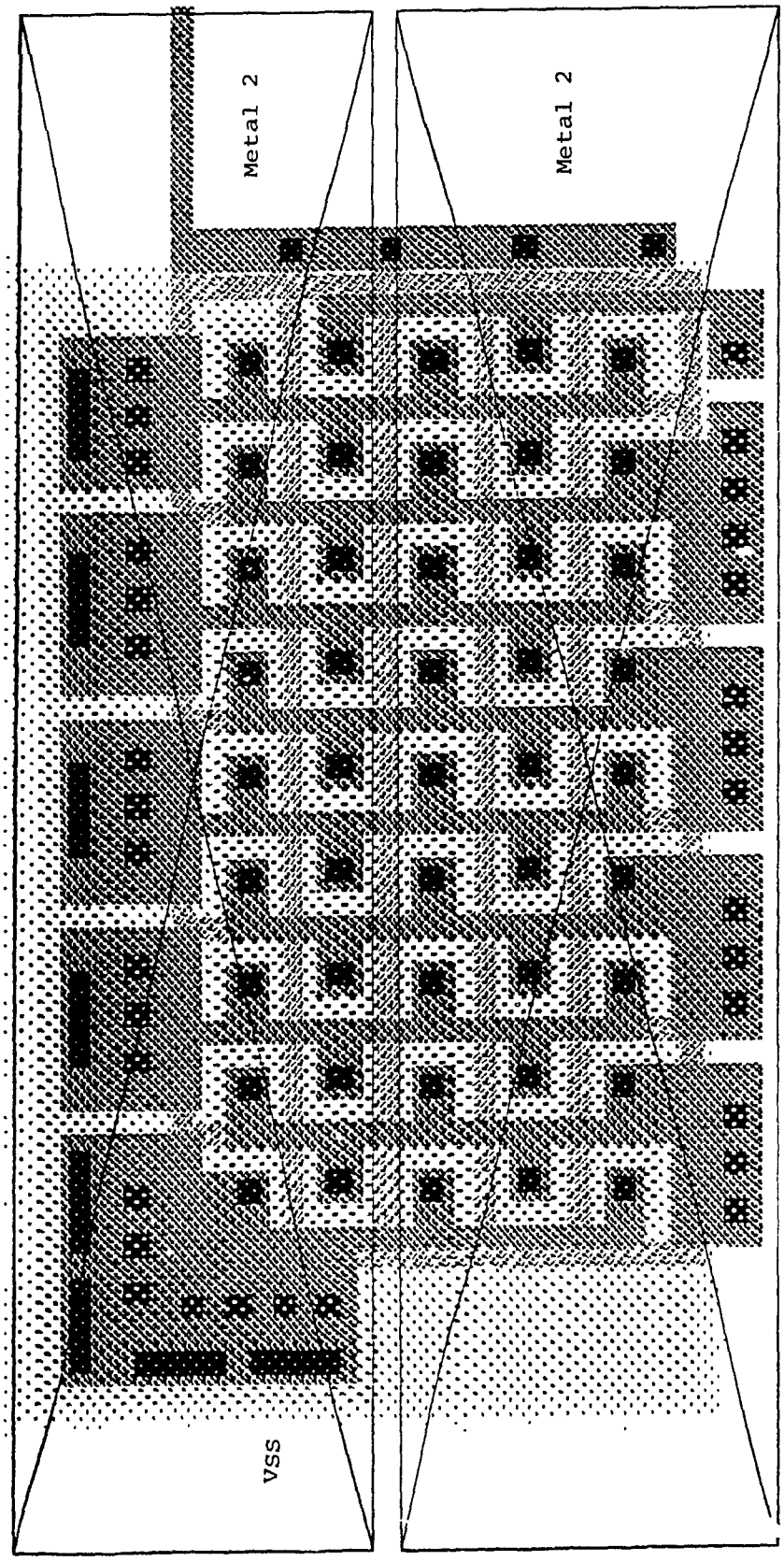

Figure 4.3 Layout of A Manhattan Waffle-iron MOS Transistor

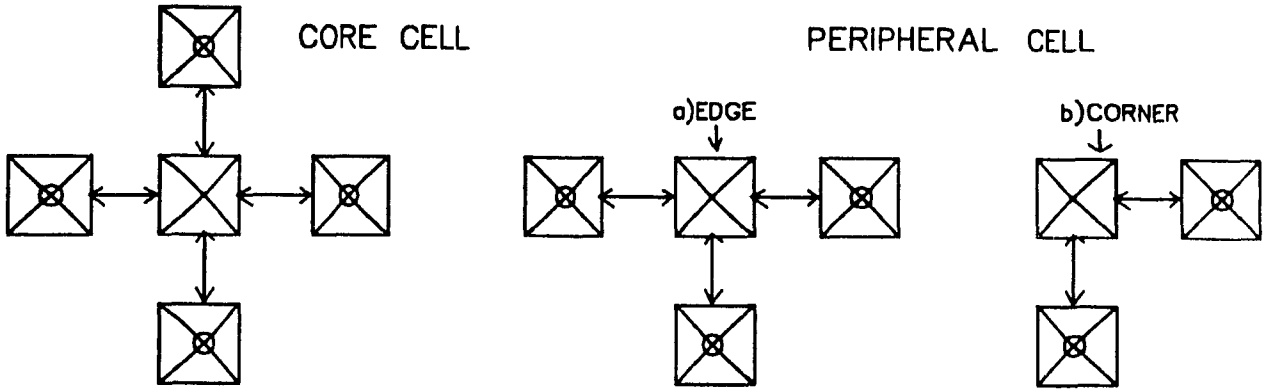

Figure 4.4 Three types of cells

4.3 Corrections to the Equivalent Transistor Width

4.3.1 Lateral Diffusion

Since the power transistor is comprised of a large number of parallel transistors, the increase in width due to lateral diffusion associated with each transistor contributes significantly to the width of the power transistor. Figure 4.5 shows the effect of lateral diffusion on a single cell. The dashed lines indicate the enlargement of the diffusion area due to lateral diffusion. The gate length is shrunk by twice L_{dl} (lateral diffusion parameter) and the width is increased by twice L_d. Applying this correction, (4.10) changes to

$$W_{eqvt}(5\mu m) = 2 * (17 + 15 + 4L_{dl}) + 2 * (X - 2) * (17 + 15/2 + 3L_{dl}) +$$

$$2 * (Y - 2) * (15 + 17/2 + 3L_d) + (X - 2) * (Y - 2) * (17 + 15 + 4L_{dl}) \qquad (4.12)$$

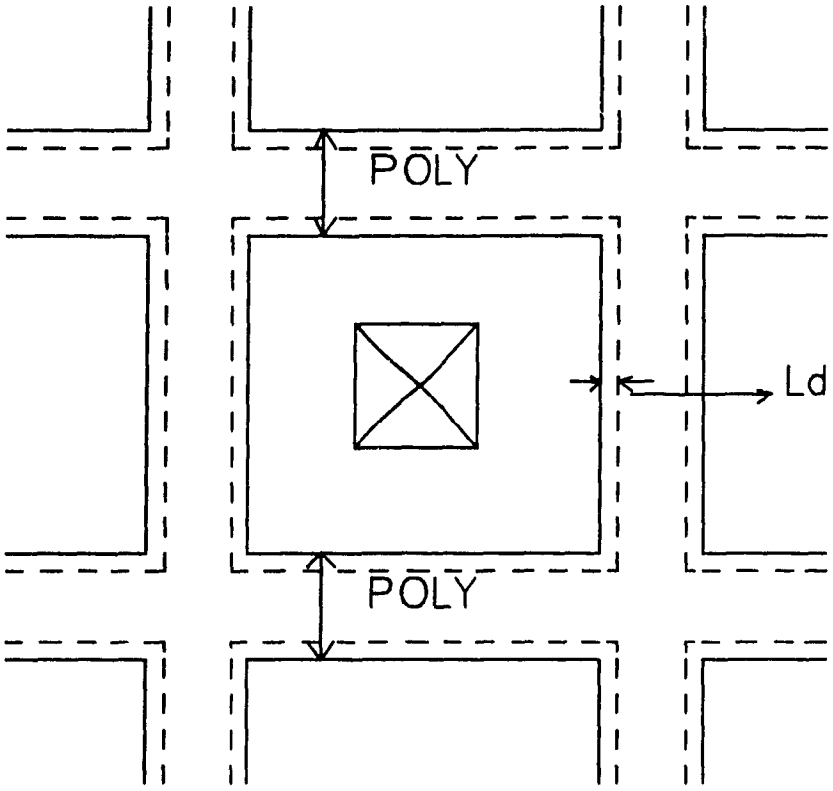

Figure 4.5 Lateral Diffusion in a Cell

4.3.2 Polysilicon Cross-over

From the layout of the waffle-iron transistor we observe that the region of the MOSFET under the polysilicon cross-over is inverted. The current flowing through these regions due to fringing field between drain and source will increase the total current of the equivalent transistor. This current can be estimated by a field calculation.

Figure 4.6 shows the region of the boundary value problem to be solved. The hatched portion is the bounded area S as described by a polysilicon cross-over

We have to solve the Poisson equation

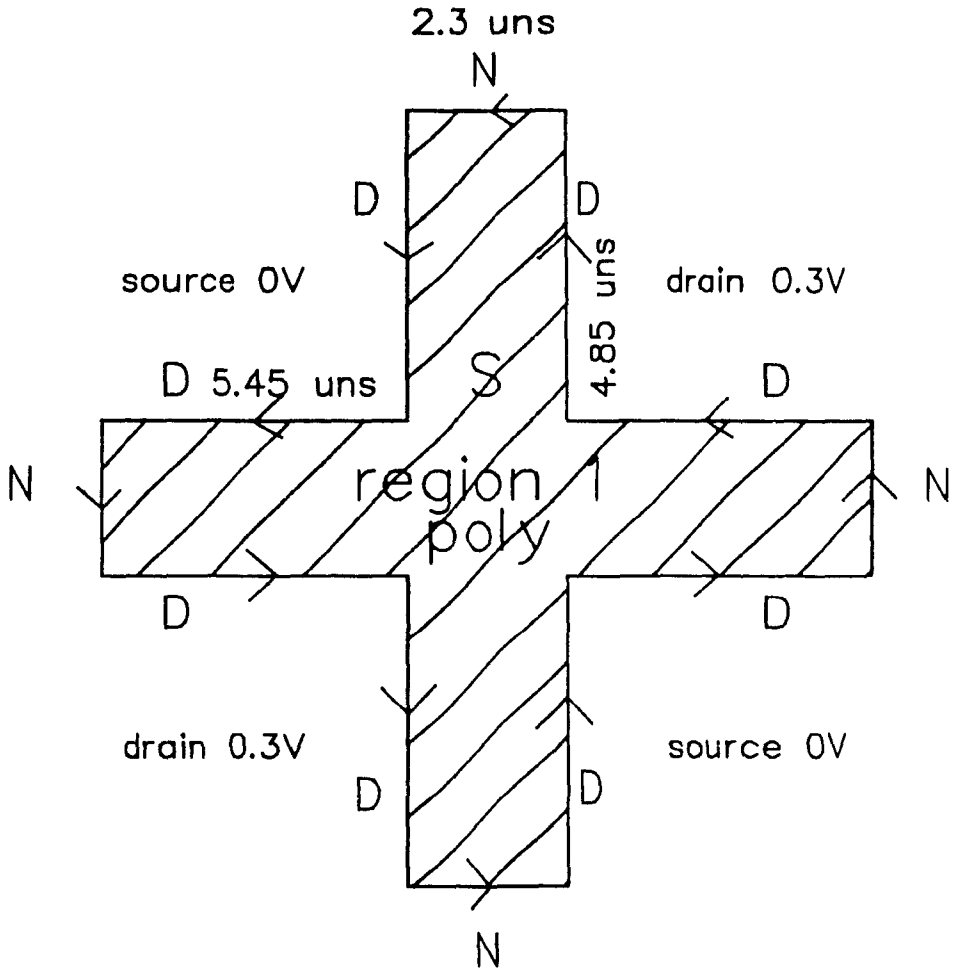

Figure 4.6 Regions of the Boundary Value Problem

$$div(p(grad\ \ u)) = q \qquad (4\ 13a)$$

in the area S where p is the relative permittivity and q is the negative of the charge density divided by permittivity of the free space. u is the unknown potential throughout S. Since grad u is equal to electric field $\vec{E}$, this equation reduces to

$$divp\,\vec{D} = 0 \qquad (4.13b)$$

in the bounded area S in the x-y plane. subject to the following two boundary conditions,

$$u = v \qquad (4.14)$$

which is along D (Dirichlet boundary condition) as shown in Figure 4.6, where v is a known (specified) potential along D. D corresponds to a boundary condition where the potential is known. The power transistors are designed to have a drain voltage not exceeding 0.3 V when the worst case peak current of the module is sunk by them. In this problem, v corresponds to the voltage at the drain of the power transistor, and therefore it is equal to 0.3 V.

The second condition given in equation 4.15 is along N (Neumann boundary condition), where N corresponds to one or more lines of symmetry. u is an unknown potential on S.

$$\frac{du}{dn} = 0 \qquad (4.15)$$

Using EMSOLV [43],a software package for solving boundary value problems, the potential and field distributions of figure 4.6 were obtained. Figure 4.7 shows the equipotential lines in the single polysilicon cross-over region as shown in Figure 4.6.

Source and drain regions are assumed to be good conductors in these calculations. Details are included in Appendix A The calculations indicate that 22.6 μA is the current flowing into one source from a single polysilicon cross-over. The remaining current of the polysilicon cross-over flows into the second source. By symmetry of the problem we can assume equal currents flowing into each source. Therefore the total current flowing into the sources due to a single crossover is equal to 45.2 μA.

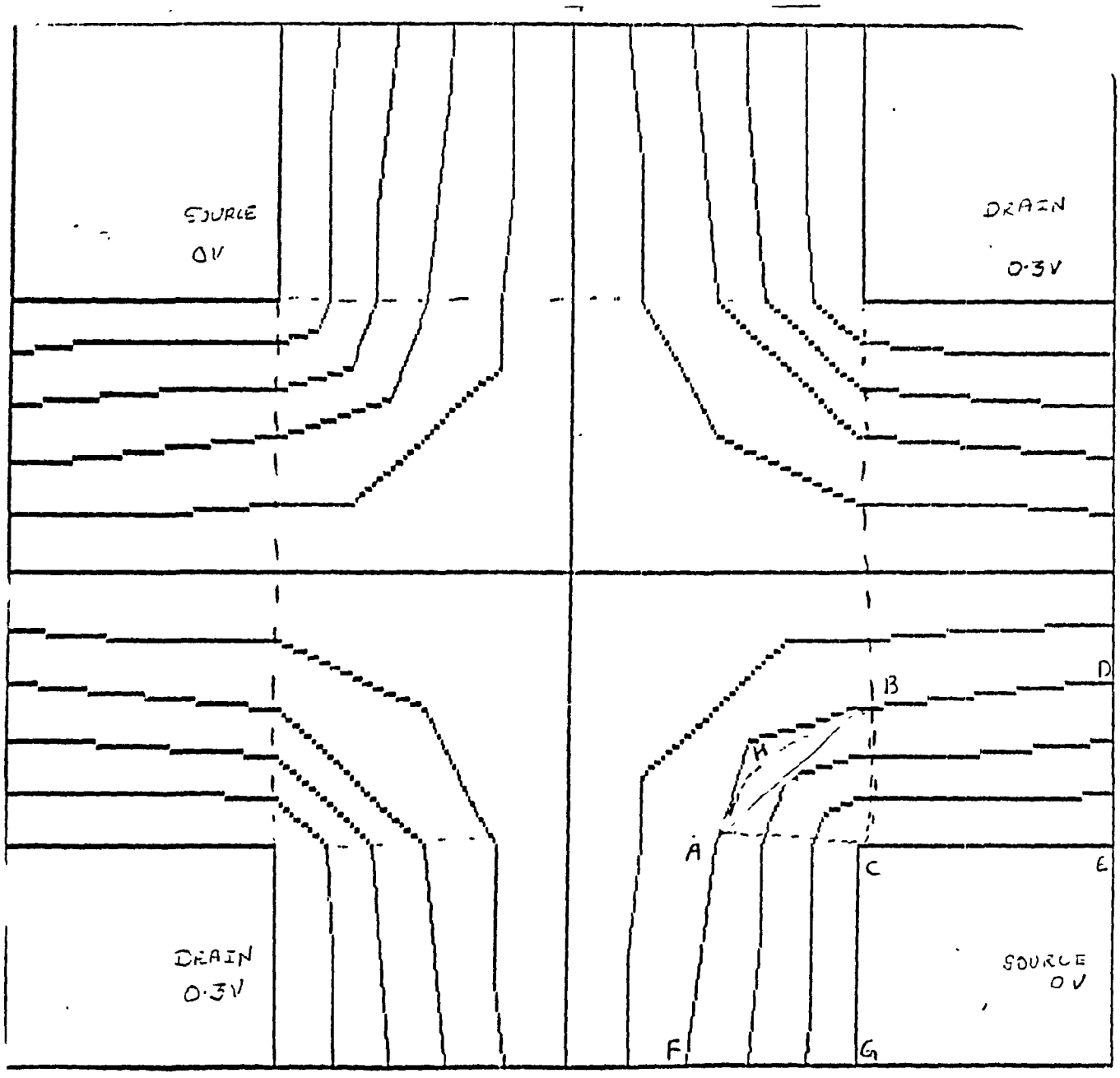

Figure 4.7 Equipotential Lines in the Polysilicon Cross-over Region

The SPICE simulated current for a 3 μm length and 2.3 μm width transistor is equal to 41 μA at 0.3 V. Thus the current for a single crossover is almost equal to the current value of a 3×3 transistor.

The width enhancement due to the polycrossovers is incorporated in (4.12) and expressed as

$$W_{eqvt}(5\mu m) = 2(17 + 15 + 4L_d) + 2 * (X - 2)(17 + \frac{15}{2} + 3L_d) +$$

$$+2 * (Y - 2)(15 + \frac{17}{2} + 3L_d) +$$

$$+(X - 2) * (Y - 2) * (17 + 15 + 4L_d) + numberofcrossovers \times 5 \qquad (4.16)$$

4.4 Electromigration

The details of the power transistor layout are governed by potential electromigration problem. Electromigration limit of metal 1, which for the present design is a conservative value of 1mA/μm, decides the number of the cells that can be stacked in each column. A minsize metal 1 (3μm in our process) layer can carry safely the current from 5 cells (dimensions 15μm×17μm) stacked in a column. Several columns of cells are grouped to form an array. If the array becomes too large (more than 15mA with our fabrication process) several arrays are stacked as electromigration of metal 2 becomes a limiting factor. For example power transistors designed nominally at 50mA and 100mA @300mV have 2 and 3 arrays stacked respectively. The ETW for each array is calculated using (4.16). At the interface of two arrays the geometry is different and

there are only a few transistors. Two transistors of width 9μm each are formed at every alternate cell along the single row of the interface. If there are X cells in a row then the number of additional transistors of width $(9+2L_d)\mu$m (L_d is the lateral diffusion) are

$$2 \times \frac{X}{2} = X \tag{4.17}$$

Therefore the extra width due to these interface transistors are $(9+2L_d)\mu$m $\times$X. So for the power transistors with stacked arrays, this correction for the interface has to be added to (4.16).

4.5 SPICE Simulation

SPICE simulations were carried out using northern telecom CMOS3DLM process parameters to determine the dc characteristics of nMOS transistors. The widths of three power transistors of nominal ratings 10 mA, 50 mA and 100 mA at V_{DS}=0.3 V were determined from the simulated I_{DS} versus V_{DS} (@ V_{GS}=5 V) dc characteristics. Substituting these width into Equation 4.16, the only unknown X (since Y=5, from section 4.4) corresponding to each width was determined. It is obvious that the unknown X, obtained after solving Equation 4.16, will in general have a fractional part. So X, the number of cells in a row is the integer part incremented by 1. The new width obtained by substituting this integer value of X back in Equation 4.16 is slightly higher than the simulated width. The new widths are used to obtain the drain current I_D for V_{DS}=0.3 V at V_{GS}=5 V. SPICE simulations were also carried to appropriately size the sense transistor T1 of circuit breaker depicted in Figure 1.1, for the desired trip point. Variation of the Vinv with k, defined as the width/length of the sense transistor is shown in Figure 4.8. With the aid of this plot, for the trip point around 2.1 V, the size of the sense transistor T1 was fixed as minsize. The time taken to turn off the power transistors by a minimum size sense transistor is also determined. The results are shown in the table 4.1. Here Power1t, Power2t and Power3t are nMOS power transistors of nominal current ratings 10, 50 and 100 mA respectively, at 0.3 V V_{ds}.

	nMOS Power Transistor Characteristics		
Transistor	Power1t	Power2t	Power3t
Nominal Rating	10	50	100
Effective Transistor Width(from Eq 4.16)(3μm)	780	3316	7646
Drain I (mA)for V_{ds} =.3 V (simulated)	12.5	53	122
Switching Time(simulated nanosec)	200	450	880

Table 4.1 nMOS Power Transistor Characteristics

4.6 Steps in a Power Transistor Design

The main considerations in the design of a power transistor can be summarized as follows.

1. *Compute the maximum peak current of the module.*

The maximum peak current of any module flowing through the breaker must be known before one can design a breaker that is near optimal in size. With a knowledge of the maximum peak current, the maximum peak (dynamic) voltage across the breaker can be fixed, for an acceptable area overhead. Predicting this current is a difficult problem which is receiving a growing amount of attention.

2. *Select the appropriate maximum peak (dynamic) voltage drop across the power switch.*

As discussed in Chapter 3 on design considerations of the circuit breaker, the maximum peak (dynamic) voltage drop across the breaker must be limited to 700 mV. If this rule is violated, then in the presence of dynamic storage nodes and considerable parasitic capacitance to the substrate, any switching noise temporarily exceeding 700 mV at the virtual ground will trigger latchup, or at best inject current into the p-wells. There is also a direct trade-off between the size of the switching transistor and its maximum drop under normal conditions. For V_{dd}=5V, a drop around 300 mV guarantees a good noise margin without incurring an unacceptable area overhead. The

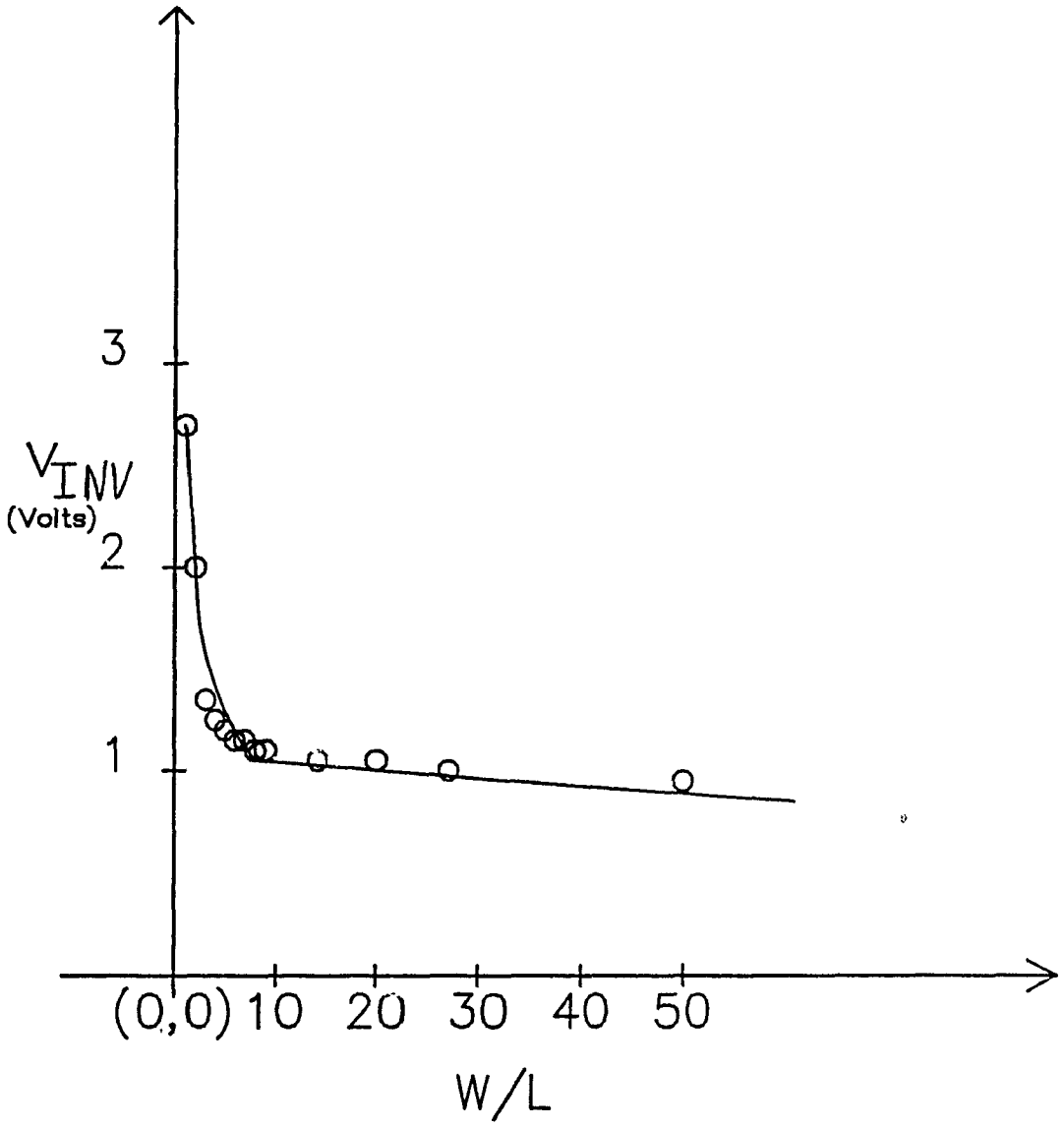

Figure 4.8 V_{inv} versus K(W/L)

magnitude of the voltage drop also has a direct impact on all timing performance of a module. However at lower supply voltage, 300 mV may be too large. However, the effect of large voltage drops on propagation delay may of course be tolerable if their duration is short in comparison with the clock period.

3. *Determine the width of the power transistor for a given current rating @ maximum peak voltage drop from SPICE simulations.*

	Resistance and Current Evaluation		
Transistor	Power1t	Power2t	Power3t
Drain Current(mA)(with only R_{ch})for V_{ds} =.3 V	12.5	53	122
Channel Resistance R_{ch} (Ωs)	24	5.66	2.46
Total Parasitic Resistance R_{par} (Ωs)	3.928	1.23	.992
Pad Contact Resistance R_{pad} (Ωs)	.708	.708	.708
Total Resistance(R_{ch}+R_{par}+R_{pad}) (Ωs)	28.64	7.6	4.16
Drain Current(mA)(with R_{ch}+R_{par}+R_{pad}) for V_{ds}=.3 V	10.5	39.5	72

Table 4.3 Parasitic Resistance and Expected Currents

As explained in Section 4.5, the width of the transistor at the desired nominal rating is obtained from SPICE simulations. The rating is determined in steps 1 and 2.

4. *Determine X and Y, the cells in x and y directions respectively.*

The number of cells in the y-direction, namely Y can assume a maximum value of 5, due to electromigration considerations of metal layers, as described in Section 4.4. The other unknown X is determined from Equation 4.16 by substituting the transistor width obtained in step 3. If the maximum peak current obtained in step 1 is smaller than 15 mA (for our fabrication process), a single array of X and Y cells in the x and y directions respectively is designed. For module peak currents exceeding 15 mA, several arrays have to be stacked as explained in Section 4.4. Three power transistors power1t, power2t and power3t were designed. Table 4.2 gives the details of their dimensions.

Power Transistor Dimensions(3μm Process)			
Transistor	Power1t	Power2t	Power3t
Transistor Effective Width (μm)	780	3316	7646
Transistor Size (μm^2)	151*92	270*187	389*246
Transistor Area (μm^2)	13900	50500	95700
Control Area (μm^2)	8000	8000	8000
Total Area (μm^2)	21900	58500	103700

Table 4.2 Power Transistor Dimensions

5. *Correction for parasitics*

Parasitics or parasitic resistance is the unwanted resistance in a device or circuit which masifests itself during processing. Parasitics become significant as the size of the transistor increases. This can be seen from Table 4.3 where the parasitics, for a 100 mA device, degrade the expected current to 72 mA. The estimation of these parasitics depend on the process and the layout. The parasitics shown in Table 4.3 were calculated for a waffle-iron layout, using the characterized electrical parameters for the CMOS 3DLM process.

4.7 Test Chips and Experimental Results

Two test chips were designed, fabricated and tested. The first one which was designed according to Figure 1.1 incorporates a 100mA @ 300mV (nominal) device. The second test chip was designed according to Figure 4.9 where the same sensor controls two power transistors of different ratings (10 mA and 50 mA @ 300mV). This second design would be of interest when some portions of a circuit are less sensitive to ground noise. A good example is the noisy peripheral drivers in contrast to the comparatively quiescent internal logic with dynamic nodes. Figure 4.11 is the layout of second test chip fabricated in a 3μm double metal double-well (with n-substrate) CMOS process.

Tests were carried out for 10 samples to confirm the design stability. The dc characteristics of the device was measured using a HP 4145A parameter analyzer. Table 4.4 shows a comparison of measurements with predicted results. Here the expected current includes the effect of all parasitic resistances, viz diffusion, metal, contacts etc. The relative area is obtained by comparing the total area to a standard library I/O pad of dimensions 234 μm^2 420 μm. As can be seen, there was a good correlation between the measured and expected currents when the parasitics are included. The parasitics become significant as the power transistor increases in size. This can be noted from Table 4.4 for the 100 mA device where the expected current is only 72 mA.

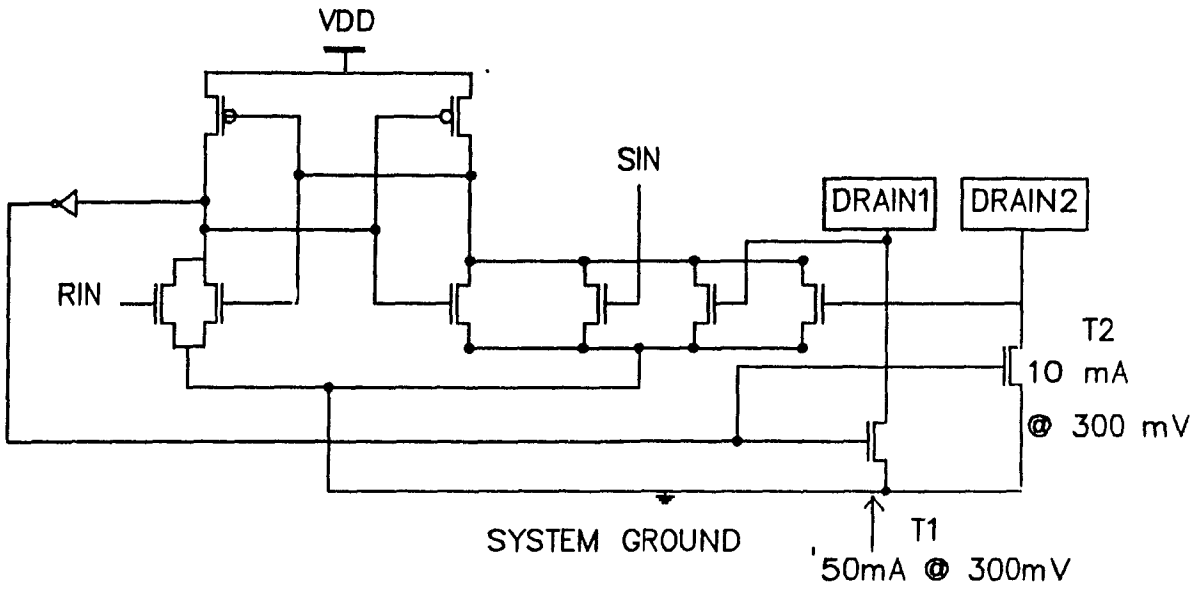

Figure 4.9 A Modified Circuit Breaker

	Test Results		
Transistor	Power10t	Power50t	Power100t
Expected Drain Current(mA)for V_{ds} =.3 V	10.5	39.5	72
Measured Drain Current(mA)for V_{ds} =.3 V	13	50	82
Switching Time(Expected nanosec)	200	450	880
Switching Time(Measured nanosec)	330	500	1020
Total Area (μm^2)	21900	58500	103700
I/O pad Area(μm^2)	98280	98280	98280
Relative Area=Total Area/I/O pad	0.224	0.6	1.06

Table 4.4 Test Results

Figure 4.10 depicts the test circuit used to measure the switching time of the power transistor. The power transistor turns "ON" ("OFF") when there is 1 at RIN (SIN). Two non overlapping square wave pulses of rise time around 10 ns and frequency 10 Khz were applied to RIN and SIN inputs. The switching "OFF" ("ON") time was defined as the time taken for the voltage across power transistor to fall (rise) from V_{ON} (approx V_{DD}) to approx V_{DD} (V_{ON}). This was monitored by placing the probes of an oscilloscope across the power transistor. Testing showed that a minimum size device in the control circuit is sufficient to turn off the largest power transistor in less than 1.5

μs. This switching time is rather long but perfectly adequate considering the normal rise time of a power supply and the amount of heat that would be dissipated in less than 2 μs, even in the presence of a dead short.

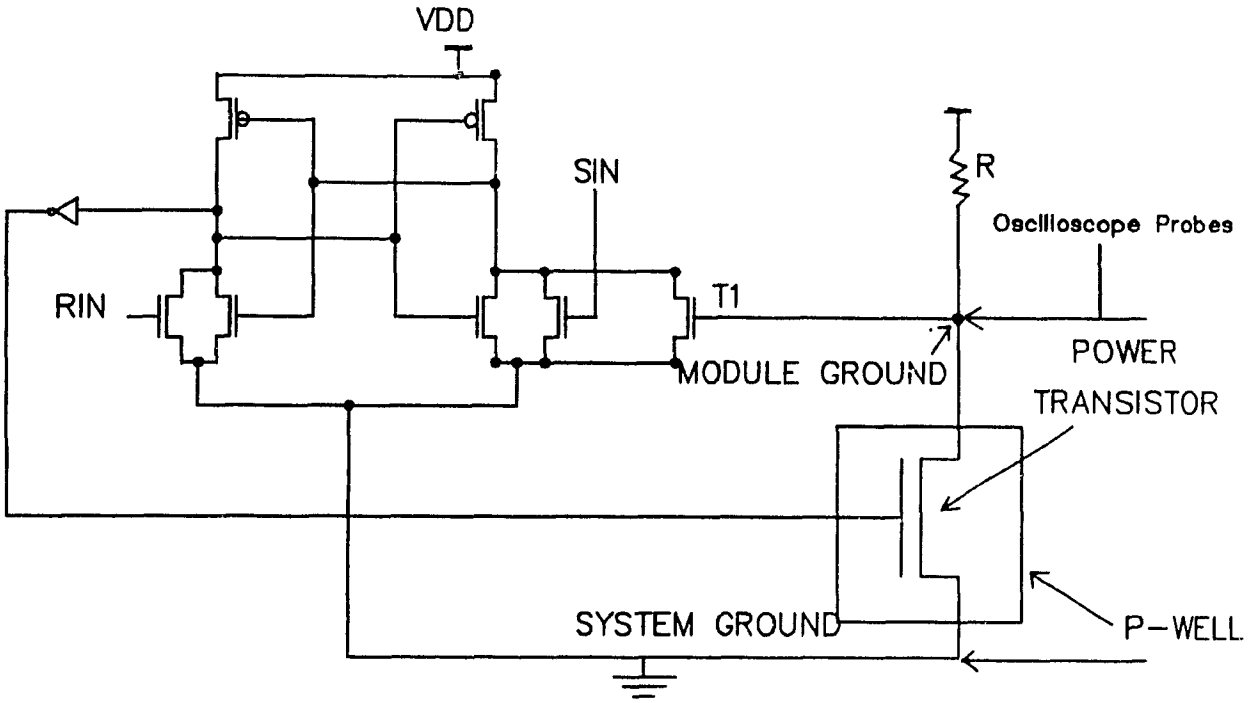

Figure 4.10 A Test Circuit

	Area Comparisons	
Transistor	10 mA MOS	10 mA Vertical n-p-n [20]
Transistor Area (μm^2)	13900	7300
Total Area (μm^2)	21900	18000
Relative Area (μm^2)	0.224	0.183

Table 4.5 Comparison of Areas of Breakers

Table 4.5 shows a comparison of sizes of a parasitic bipolar [20] and MOS circuit breaker. Several interesting points can be noted from Table 4.5. First and foremost, the 10 mA nMOS transistor is 1.9 times larger than the 10 mA vertical n-p-n transistor proposed in [20]. Considering that the MOS transistor was actually a 13 mA @ 300mV device, where as the bipolar transistor was a 10mA @ 250 mV (dynamic

drop) device, the comparison is 1.75 factor in favor of the bipolar device. This is to be compared with the factor of 7 predicted in [20]. It is also interesting that, for small transistors, the size of the control circuit becomes significant as shown in Table 4.5 for a 10 mA vertical bipolar n-p-n. The smaller size of control circuit of MOS circuit breaker reduces the area advantage of the bipolar approach from 1.75 to a mere 13%.

A meaningful figure of merit for a circuit breaker is to compare its size to a normal I/O pad. This can be seen from Table 4.4 and Figure 4.10. Interestingly, the 82 mA device has an area roughly equal to one of our library I/O pads. Although the area devoted to circuit breakers is significant in a large area circuit, the relative area would clearly be much smaller than what is currently devoted to pads at the VLSI level of complexity, where circuits with more than 100 pins are common.

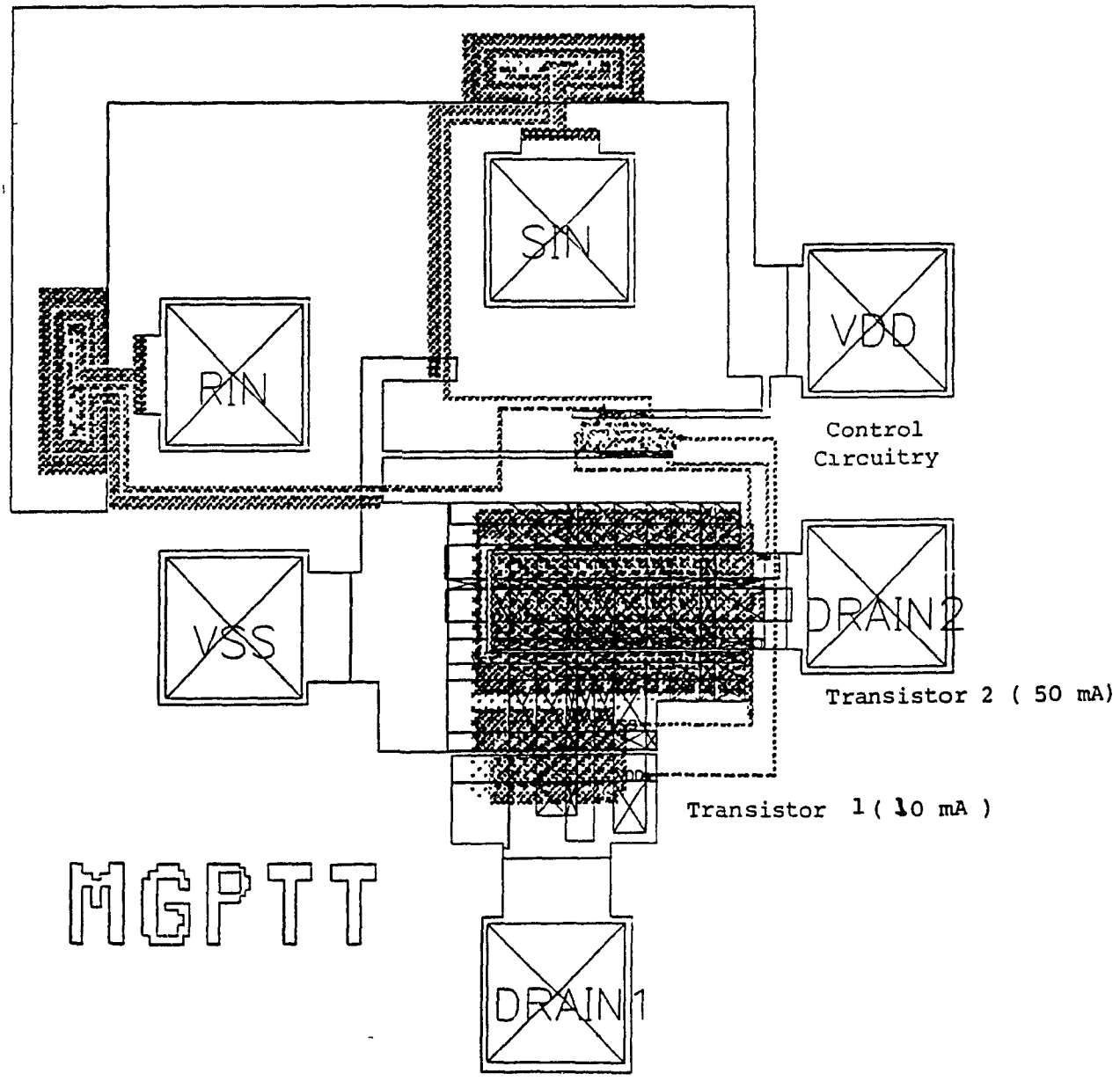

Figure 4.11 Layout of the Modified Circuit Breaker

Chapter 5 Current Estimation

5.1 Introduction

This chapter deals with the problem of estimating the peak current through a CMOS circuit. This is an important issue for large area ICs which employ a circuit breaker for reconfiguration. The actual current waveform through a module is not steady but exhibits peaks when logic transitions occur. Certain transitions involve more logic gates, and determine the maximum peak current of the module. Such current surges might cause the voltage at the drain end of the breaker to rise above the V_T of the sense transistor, thereby erroneously shutting off the module. It is therefore essential to make an estimate of the peak current through a module to design a circuit breaker which can handle currents of these magnitudes. This estimate can also be used to size the power/ground routes so that metal migration is prevented [44]-[50], to analyze dynamic power consumption, and to reduce within safe limits the noise spikes due to excessive voltage drops in the power bus thereby ensuring reliable circuit operation.

Most of the previous work on power bus design and analysis have concentrated on global routing and sizing of power lines between the modules of a chip, [51] -[53], or emphasized the power consumption problem [54]

The problem of current estimation has been addressed only in the past few years [57]-[63]. A brute force approach to determine the maximum peak current for a

circuit with n inputs, is to exercise all possible input vectors (2^n for n inputs) to derive an accurate worst case waveform. By contrast, an input pattern-independent approach can be taken. A good example of the first method is the SPIDER [56] program developed by Hall et al which uses SPICE to calculate the current accurately for all the possible input patterns for a module. In general, performing this kind of analysis for a large number of inputs is prohibitively expensive in terms of computer time, so the pattern independent approach[57]-[63] is usually preferred. Among the pattern-independent methods, the HERCULES program by Tyagi[57] assumes all the series paths connecting a power/ground node to an output node to be fully on. The approach though quite simple is very pessimistic since there may exist no input excitation for which two nodes may draw currents at the same time. Another program called CREST by Farid et al [63], achieves pattern-independence using probabilistic simulation by replacing logic values by signal probabilities and logic transitions by transition probabilities. The expected current waveform is determined as the mean of all the values that the actual current can take at that time. A recent program, ARIEL, by Stark and Horowitz[60], avoids the large number of test vector problem by using the pattern-independence of a timing analyzer in conjunction with a resistance extracter and network analyzer. The idea of exploring the pattern-independence of a timing analyzer to determine the worst case current patterns in power buses, was earlier proposed by M. Dagenais [61] With minor modifications the timing analyzer, TAMIA described in [61], can be adapted to predict worst case currents.

Here we present a preliminary analysis of a possible technique to estimate the magnitude of worst case peak current for a CMOS combinational block Though this scheme tries to determine the input pattern which correspond to the peak current through the module, it does not suffer from the problems generally associated with circuits having large number of inputs Instead of the tedious process of transistor level current estimation, the faster estimation of current at the logic gate level is carried out. This method is based on the observation that not all inputs of a gate switch simultaneously and on an extension of the concept of controllability, well known in fault

simulation. The idea is to determine the time intervals at which the logic transition of each gate in a combinational circuit occur. The gates in the circuit which switch at the same time interval are grouped together. By assigning appropriate current values from SPICE simulations to the gates in each interval we can deduce the current waveforms and hence, worst case peak current value for the circuit. An algorithm is developed and tests are presented for a INV-NAND and a INV-NAND-NOR implementation of a 4-bit ripple combinational adder. A comparison with SPICE is carried out for a few circuits. Interesting observations and comments are made based on the results obtained. The method provides the worst case peak current, and the corresponding signal transitions at the primary inputs. This worst case current waveform can also be used to estimate the median-time-to-failure, which is a measure of electromigration failure and voltage drops in the power buses. A implementation of the algorithm is beyond the scope of the present work.

It is well known that in a CMOS IC the supply current consists of charging/discharging pulses as CMOS gates in the quiescent state draw very small current. The current in a complementary CMOS gate consists of three components (a) static current due to leakage, (b) V_{dd}-V_{ss} short circuit current, (c) current due to charging and discharging the load capacitance [63]. Static current due to leakage is usually small and thus can be ignored. During transition from either 0 to 1 or 1 to 0, both the p and n transistors are "ON" for a short period of time giving rise to the V_{dd}-V_{ss} short circuit current. When a CMOS gate switches, the capacitance connected to its output charges or discharges. SPICE simulations were carried out for a 2 input NAND gate with widths of n and p transistors equal to 12 and 9 microns respectively and for a load capacitance of 0.25 pf. The input signal rise time was 3ns. The results show that the supply-ground short-circuit current is at most 1/6th of the charging discharging current as the time of overlap of the p and n transistors is short. We are concerned here with a ground circuit breaker and so only the worst case ground current is estimated. And since the dominant ground current is the current due to the discharging of the load capacitor to ground when the gates switch to zero, the gates that switch to one are ignored since a relatively

lower supply-ground short-circuit current flows during this switching. Without loss of generality the same procedure can be carried out for gates switching to one.

Before we go into the details of current estimation, it is important to introduce the concept of a rank which groups the gates of a circuit which switch together. Signal transitions at the primary inputs of a combinational logic circuit causes the gates of the circuit to switch at different instants of time. The time taken for the primary input pattern to give rise to an output pattern can be divided into intervals based on the time taken for the logic elements in each path to switch. For the sake of simplicity we take these intervals to be equal, i.e. all gates are assumed to have equal delays. Further these gate delays are normalized to unity, where unity is a arbitrary unit of time. Each of these intervals which corresponds to one gate delay is designated as a rank

The method of estimating the peak current consists of four steps. First the gates that switch simultaneously (within time interval Δt at most equal to unity) are grouped and assigned to different ranks. In the second step, the appropriate signals and initial conditions at the primary inputs of the combinational block to produce a 1-0 transition at the output of every gate of every rank are determined. In the third step the maximum number of gates in every rank that switch to zero simultaneously are determined by a selection process which eliminates gate with conflicting primary input signal transitions. Finally we assign appropriate current values to each logic gate in a rank and the current flowing through the circuit during each time interval/rank is calculated. The worst case peak current corresponds to the maximum of these current values. The details of each step are discussed separately. The following assumptions are made throughout this work:

1) All the primary inputs of the block receive input signals at the same time

2) The propagation delay of every gate is equal to unity.

3) The interconnection delays are neglected.

4) The signal rise times at the inputs of all the gates belonging to a rank are equal.

The first assumption is generally valid for the register transfer logic. However if the primary inputs receive signals at different times, each input will now be assigned to a different rank which will slightly complicate the procedure. The magnitude of the ground current for any logic element is found, by SPICE simulation, to depend on the signal rise times at the input nodes. In order to simplify the problem at hand, the input signal rise time of all the gates of a a given rank are assumed to be equal.

5.2 Step 1 : Gate Distribution

The following procedure is adopted to group the gates into logical depths differing by unit delay in time. By doing this we assume that the inputs of a gate, except the gates connected to the primary inputs, do not in general change at the same time. A sequence of numbers at the gate inputs indicates the instants at which the input may change. The sequence at the outputs are the instants at which the gate could switch.

1) Extract the netlist of the given combinational circuit. The netlist contains the following information for every gate.

a) Gate identification.

b) The identification of gates that drive the inputs.

c) The identification of gate inputs to which the output is connected.

2) Assign rank 0 for the primary inputs. Here we assume that all the primary inputs change at the same time. In reality the signal at each primary input may arrive at different time. If the precise time of input change is known, then each primary input can be assigned to a different rank.

3) Consider a gate. If all the inputs of the gate have a number or a sequence of numbers then assign a number or a sequence of numbers to the output of the gate. The output number or sequence is obtained by incrementing every element of the input number/sequence by one (since the propagation delay is unity for every gate.)

Union of the resulting sequence of numbers due to all inputs gives the output sequence. This sequence is propagated to all its fanouts without modification since the interconnection delay is neglected. This procedure is repeated till all the gates are exhausted.

4) The final netlist will provide in addition to the input and output details for every gate, a sequence of numbers for inputs and outputs of every gate.

5) Place each gate (with its input and output information) in every number (rank) of its output sequence.

Table 5.1 shows the gates of the combinational circuit in Figure 5.1 placed in the respective ranks. An important point to note is that many gates appear in several ranks. For example gate 40 appears in rank 4 to rank 16. This is due to the reason that not all inputs of a gate change at the same time and this effect gets propagated. This indicates that there is a possibility of gate 40 switching in any of these ranks and not necessarily in all the ranks for a given input excitation. As can be seen from the Table, the ranks 6,7 and 8 have the maximum number of gates.

5.3 Step 2 : Determination of the Primary Input Signal Transition

The second step in the current estimation is based on the concept of controllability that is used in fault simulation. The appropriate signal and initial conditions at the primary inputs of the combinational block, to produce a 1-0 transition at the output of each gate of every given rank are determined. This is achieved by backward propagation of the transitions, step-by-step from the output of the desired gate until

	Rank Numbers															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	1	2	5	5	6	5	6	7	8	21	22	23	24	37	38	39
	3	4	7	6	7	7	8	18	21	22	23	24	37	38	39	40
	9	10	13	8	15	8	17	20	22	23	24	34	38	39	40	50
	11	12	15	14	17	16	19	21	23	24	33	36	39	40	49	52
	13	14	21	16	19	18	21	22	24	32	35	37	40	48	51	53
G	17	18	23	21	22	20	22	23	31	34	38	38	47	50	53	54
A	19	20	24	22	23	21	23	24	33	36	39	39	49	52	54	55
T	25	26	29	24	24	23	24	30	34	37	40	40	51	53	55	56
E	27	28	31	30	29	24	29	32	35	38	45	46	53	54	56	62
	33	34	37	32	31	30	31	34	37	39	47	48	54	55	61	64
	35	36	38	37	33	32	33	36	38	40	49	50	55	56	63	
N	41	42	39	38	35	34	35	37	39	46	51	52	56	62		
U	43	44	45	39	38	36	37	38	40	48	53	53	61	64		
M	49	50	47	40	39	37	38	39	45	50	54	54	63			
B	51	52	53	46	40	39	39	40	47	52	55	55	24			
E	57	58	55	48	45	40	40	46	49	53	56	56	37			
R	59	60	61	53	47	46	45	48	51	54	61	62				
S			63	54	49	48	47	50	53	55	63	64				
				55	51	50	49	52	54	56	64					
				56	54	52	51	54	55	62						
				62	55	53	52	55	61							
				64	61	55	53	56	62							
					63	56	56	62	63							
						62	61	64								
						64	63									

Table 5.1 Gate Distribution

the primary inputs are reached. This information is stored for every gate of the given rank. This procedure is then repeated for all the ranks

The rules of backward propagation for signal transitions are as follows.

While the ranks are not exhausted

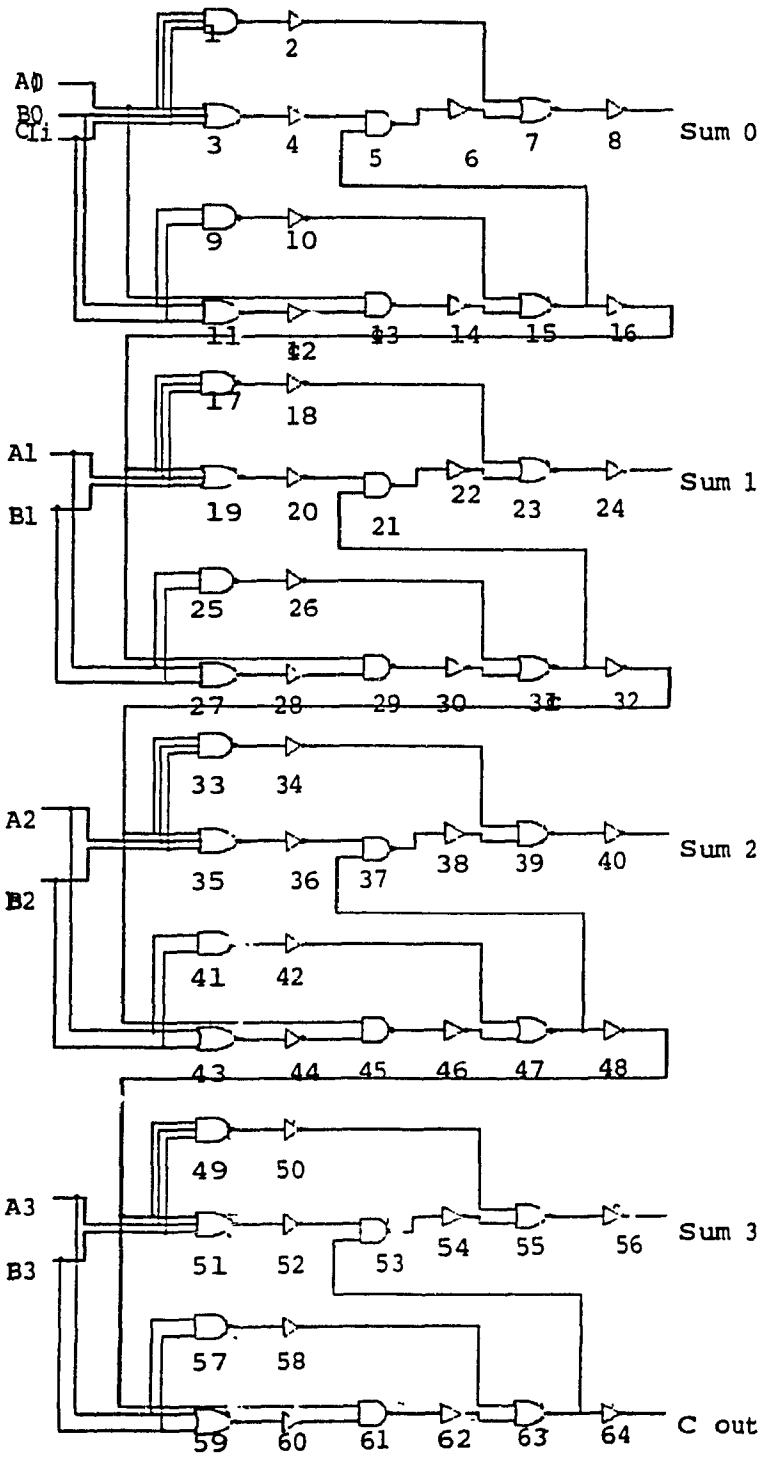

Figure 5.1 A 4-bit Combinational Adder

While the gates of a rank are not exhausted

While the primary input is not reached

RULES FOR PROPAGATING SIGNAL TRANSITIONS:

(Ia) If Inverter: A 0-1(1-0) signal transition at rank (n) at the output is obtained by a 1-0 (0-1) signal transition at the input or inputs containing rank (n-1).

(Ib) If NAND: A 1-0(0-1) transition at its output at rank (n) is realized by a 0-1(1-0) transition of at least one of its inputs at rank (n-1) ; with the other inputs remaining at 1.

(Ic) If NOR: A 1-0(0-1) signal transition at rank (n) is achieved by transition 0-1(1-0) of at least one one of its inputs at rank (n-1) ; with the other inputs remaining at 0. As an example, Figure 5.2 illustrates rule (I). Here the input signal transitions, viz. the 0-1 transitions of inputs a and b of NAND 1 and NOR 5 and the input of the inverter cause a 1-0 transition at rank 8 at the output of the three gates. It is to be noted that though both inputs, a and b of NAND 1 and NOR 5 contain rank 7, at least one of them should switch from 0-1 to cause a 1-0 at the output at rank 8. In case of NAND or NOR, it is essential to consider inputs other than those which cause an output transition, since we assume

these inputs to be initially at a 1 or 0 state. This point will be illustrated in rule (II).

(II) Again we consider here the 1-0 transition of a gate at rank n. Suppose k, the smallest number of the sequence of any input of this gate is greater than (n-1), this indicates that the earliest transition for this input occur at a later instant/rank (k > n-1),than the rank n being considered. So in order to have a 1-0 transition at the output at rank n, we have to initialize the input to a 1 or 0 state. This is illustrated in Figure 5.3. Figure 5.3 shows the gates connected to NAND 1 and NOR 5 of Figure 5.2. Both these gates have the sequence 9,10 at their input d. The earliest time interval (rank) at which the input 'd' can have a transition corresponds to the smallest number in the sequence, that is 9. Therefore the initial condition 1 (0) is assigned to the input d of NAND 1 (NOR 5) for the gate to switch from 1-0 at rank 8.

(III) If any input has a sequence which does not include rank (n-1) but contains ranks less than (n-1), then the logical value at the rank/number from the sequence closest but less than rank (n-1) must be defined (''ON'' equal to 1) in order and to have a 1-0 transition at rank 'n' Therefore we now propagate this signals backwards till the primary inputs are reached. The example in Figure 5.3, one considers the possibility

that NAND 1 and NOR 5 to switch at rank 8. The input 'c' of NAND 1 (NOR 5) does not include rank 7 as can be seen from the sequence associated with it and hence the value of the closest rank smaller than 7 is rank 5, for which the logical value should be 1 (0). This signal is now propagated backwards to the primary inputs. This propagation will involve both steady signals as well as logic transitions. The logic value of 'c' is held constant from rank 5 to rank 7 which constitutes a steady signal while it might involve a 1-0 transition for the input 'h' of NOR 7. This propagation will give rise to the possible input pattern which corresponds to a transition of NOR 5 at rank 8.

Consider the next gate belonging to the rank being investigated.

End While (when all gates belonging to a rank are exhausted.)

Consider next rank

End While (when all ranks are exhausted.)

Since it takes a considerable amount of time to carry out backward propagation manually, only the rank 7, which is one of the ranks containing the maximum number of gates and rank 1 are chosen. This rank has 25 gates. For every gate belonging to this rank the primary input transitions required to switch it to zero are determined. As an example the signal transitions at the primary inputs needed for the gate 23 in rank 7 to switch to zero are illustrated below. Figure 5.4 which is part of the 4-bit adder in Figure 5.1, shows the path of backward propagation of these signals from gate 23 to the primary inputs. The signal transitions are obtained by repeated application of the

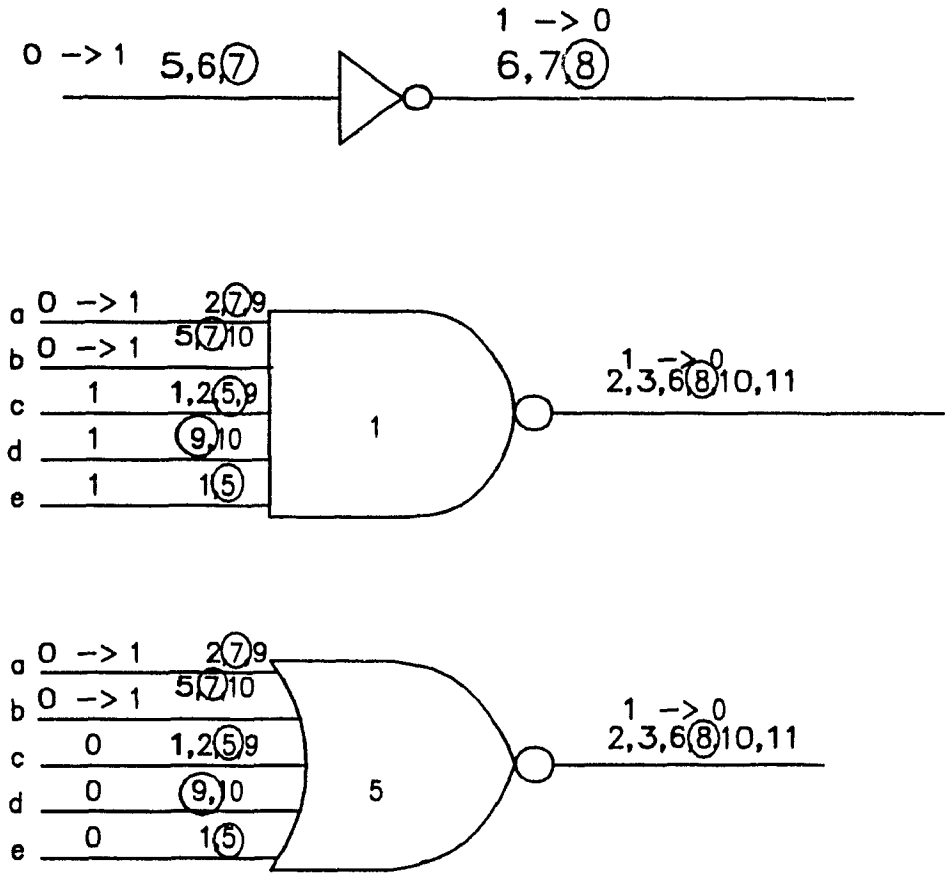

Figure 5.2 Three Types of Gates with Input and Output Details

above rules. These are the primary input transitions and initial conditions required at instant 0 to cause the gate 23 to switch to 0 at rank 7. The same procedure is repeated for all the gates in rank 7.

.IC and O/P correspond to initial conditions and output respectively.

GATE 23

1) [(.IC(O/P 30) = 1); Initial condition at the output of gate 30 is 5V

OR

1) (A1,B1 = 1, 1)] ; Both the primary inputs A1 and B1 are at 5V at the instant 0. (CHOSEN)

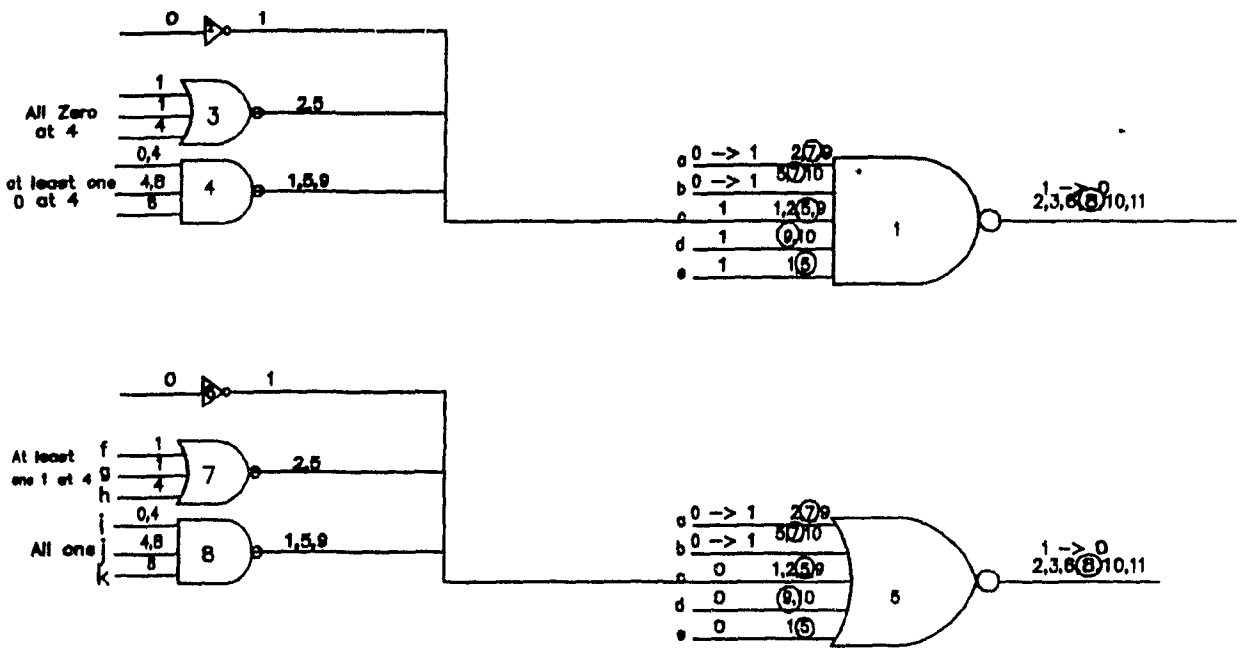

Figure 5.3 An Example of Backward Propagation

OR

1) [(A1, B1 = 0, 0

.IC(O/P 16) = 0]

2) A1, B1 = 1, 1 (CHOSEN)

3) [(.IC(A0 or B0) = 0

A0, B0 = 1, 1

.IC(O/P 12) = 1

.IC (Ci) = 0

Ci = 1]

OR

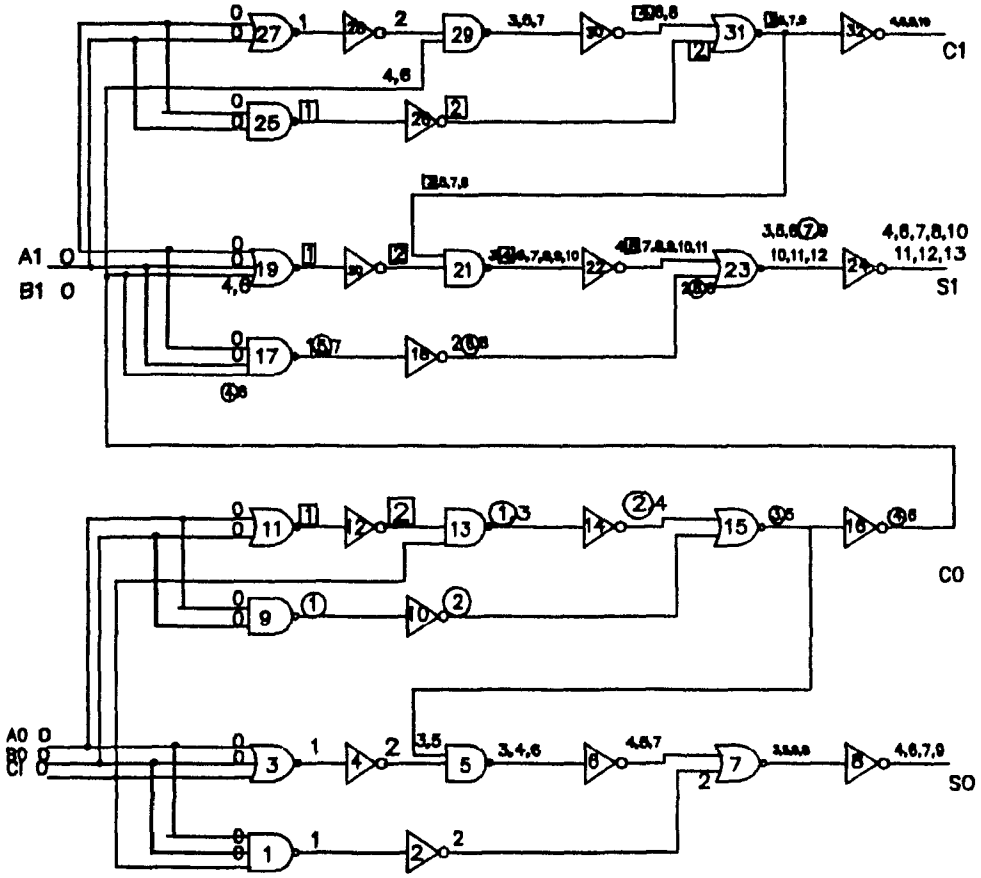

Figure 5.4 Another Example of Backward Propagation

3) (.IC(O/P 12) = 1 (CHOSEN)

.IC(Ci) = 0 (CHOSEN)

Ci = 1 (CHOSEN)

4) A0, B0(at least one) = 0) (CHOSEN)

OR

4) (.IC(A0 or B0) = 0

A0, B0 = 1, 1

.IC(O/P 12) = 0

OR

4) Ci = 0)

5.4 Step 3 : Gate Selection

The next step is to select the maximum number of gates that can switch to zero from every rank based on the signal transitions obtained in step 2. The procedure is as follows.

1) For every gate, if there is any contradiction in the initial conditions or primary input signal transitions, delete the gate.

2) The gates of a given rank which require contradictory primary inputs are determined. No algorithm is formally provided in this thesis. However here the gates which require contradictory inputs are seen by inspection from Table 5.2 which gives the primary inputs and initial conditions for the 1-0 transition of all gates in rank 7. For example, here gate 47 requires a logical 0 value for the input A_2 while the other gates require a logical 1. So we eliminate gate 47 from the rank. This elimination process is carried out for all the inputs. It should be mentioned that though it is quite possible that some primary inputs for a given circuit can have a 0 or 1 value for particular gate transitions, the circuit of Figure 5.4 fortuitously had unique logical values.

3) Repeat this for all the ranks.

The primary input signal transitions necessary for switching the individual gates of rank 7 to zero are summarized in Table 5.2. The signal transitions and initial conditions for worst case peak currents are chosen by inspection. To choose the signals for A_2 and B_2 and have maximum gates switching for the worst peak current we have to choose A_2 and B_2 equal to one and eliminate gates 47 and 61. By similar reasoning we assign A_3 and B_3 equal to 1 and 0 respectively and eliminate gates 53 and 61. The

signal transitions for worst case peak current for the rank 7 can be seen from Table 5.2 as A_0=1, B_0=0, A_1=1, B_1=1, A_2=1, B_2=1, A_3=1, B_3=0, .IC(gate 16 output)=1, .IC(gate 32 output)=0. These input signal conditions cause 10 gates of rank 7 to switch simultaneously. The same procedure is carried out for the rank 1. In this case it is possible to switch all the 17 gates of rank 1 from 1-0 for a particular input condition.

Assignment of Primary Input Transitions															
	6	8	17	23	24	33	47	39	45	40	53	54	56	61	63
.IC(C_i				0											
.IC(A_0	0	0	0												
.IC(B_0	0	0	0												
.IC(A_1					0	0	0	0	0						
.IC(B_1					0	0	0	0	0						
.IC(A_2										0	0			0	0
.IC(B_2										0	0			0	0
.IC(A_3												0	0		
.IC(B_3												0	0		
.IC(12)				1											
.IC(16)					0	1			1						
.IC(30)					0		0	0							
.IC(32)								0		0				1	
.IC(46)										0	0		0		0
.IC(48)												1	1	1	
.IC(62)													0		
C_i	1	1	1	1											
A_0	1	1	1	1											
B_0	0	0	0	0											
A_1			1	1	1	1	1	1	1						
B_1			1	1	1	1	1	1	1						
A_2						1	0	1	1	1	1			1	1
B_2						1	0	1		1	1			0	1
A_3											0	1	1	1	1
B_3											0	0	1		0

Table 5.2 Assignment of Primary Input Transitions

The same procedure was repeated for NAND-INV implementation of the four bit adder of Figure 5.1. Here rank 1 was seen to have maximum number of gates after step 1. After backward propagation and gate reduction, it was seen that for a particular set of the primary input signal transitions all the 26 gates of rank 1 could be switched to zero simultaneously. The results are shown in Table 5.3.

5.5 Step 4: Current Evaluation

In step 4 the evaluation of the peak current for every rank is carried out. We begin by assigning appropriate current values for different gates with different input rise times. The input rise time for a given rank is obtained by simulating a chain of inverters using SPICE.

The signal rise time at the input of the first inverter corresponds to the input signal rise time of all the gates in rank 1, similarly the input rise times of inverter n corresponds to the rise time of rank n. Using a reasonable primary input rise time of 0.2ns, the rise times corresponding to the various ranks are determined by SPICE.

Simulations were run for inverter, NOR and NAND gates for these different input voltage rise time with a typical output load (C_L=0.1pF). By assigning these precomputed current values of different logical elements to the gates of each rank which switch simultaneously (obtained from step 3) we determine the peak ground current for each rank. The maximum of all these current values give the maximum peak value current for the combinational block.

5.6 Results and Discussion

SPICE simulations to evaluate the worst case ground current were carried out for the NAND-INV and NAND-NOR-INV implementations of the four-bit adder with the primary input signal transitions obtained from the above described method.

Rank 1 was considered for both implementations, while Rank 7 was considered only for NAND-NOR-INV implementation since it was the rank with maximum gates after step 1.

	Comparison With Spice					
Adder	Total Gates	Rank	After Step 1	After Step 2	I Estimated	I from SPICE
NAND,NOR,INV	64	7	25	10	5 mA	2 mA
NAND,NOR,INV	64	1	17	17	7 mA	4.8 mA
NAND,INV	64	1	26	26	12 mA	7.5 mA

Table 5.3 Comparison With Spice

Comparing the computed values with SPICE results revealed the following. The simulated value was much lower thar the value obtained by this method. This is expected since if gates in a rank do not switch quite simultaneously over the time interval Δt the switching current of the gates tends to be distributed over the interval. By choosing smaller ranks/time intervals the method might yield values closer to SPICE simulated values. The analysis can be further refined by assigning different propagation delays to different logic elements depending on their size and load.

For both implementations, rank 1 exhibits the maximum value of ground current. This is not surprising since all the primary inputs belong to the same rank and in addition have the fastest signal rise times. Thus for register transfer logic, it may not be necessary to find the signal transitions for all ranks if it is found that one of the initial ranks has the maximum number of gates after gate elimination in step 3. It may be sufficient to calculate the worst case ground current only for this rank.

The aim here was to investigate the possibility of a current estimation method. It will be hard to conclude the specific advantages of this method unless further work is done. However caution must be exercised in applying this method to larger circuits. The number of gates in the example were 64 and further refinement of the technique will be necessary for LSI or VLSI circuits.

Chapter 6 Conclusions and Future Work

Several aspects relevant to the design of circuit breakers for protection against V_{dd} to V_{ss} shorts in large area devices were presented in this thesis. Circuit breakers [20] employing parasitic bipolar transistors, inherent in every bulk CMOS process, were analyzed and compared with the MOS counterpart. The bipolar circuit breakers were seen to have a severe latchup problem, excessive power dissipation and design constraints rendering them impractical for short circuit protection. On the other hand these shortcomings can be alleviated or completely eliminated in MOS circuit breakers, by adhering to a set of design rules [28].

A design method for a large MOS transistor, using an area-efficient layout method such as the "waffle-iron", [42] was developed. Two variations of circuit breakers incorporating power transistors of different ratings were designed, fabricated and tested. Testing revealed extremely good agreement with predictions. Test results also offered some interesting comparisons of the circuit breakers employing MOS transistors and parasitic bipolar transistors with regards to area utilization. The smaller size of the control circuit of the MOS transistor, reduces the area advantage of the bipolar solution[101] to a mere 13 % for a 10 mA V_{ss} circuit breaker.

An attempt to analyze a possible technique to estimate the magnitude of worst case peak current for a CMOS combinational block was made in this thesis. A procedure for implementing this technique was outlined along with some rules. This

method was used to estimate the worst case peak current of a 4-bit full adder and compared with SPICE simulation results. However, a complete solution of this problem is beyond the scope of this work. This algorithm appears to be a very promising method to estimate the worst case current value for a circuit.

The work on circuit breakers remains incomplete if nothing is mentioned about the defect-tolerance of these breakers themselves. In fact these breakers are tolerant to a majority of defects[28]. Any "stuck-at" defect is indeed tolerated since the breaker is either permanently 'ON' or 'OFF'. When permanently 'OFF', a module is lost and when permanently 'ON' the protection is lost. Loosing the protection is of consequence only if there is also a short in the corresponding module, and adequate partitioning can be used to ensure that this event has a low probability

The power transistor comprises a large number of parallel transistors and therefore it is inherently tolerant to a break in the poly or in the metal, as well as to missing contacts. Shorts in the polysilicon gate is of no consequence since it is an equipotential. Shorts in the metal could cause the breaker to be permanently 'ON' resulting in loss of protection. A drain-to -well excessive leakage current could have a similar effect. Thus, none of the above mentioned defect types is capable of failing a system using circuit breakers.

There is one failure mechanism, however, which could defeat the system A metal-to-poly short between the drain and gate would put a breaker in a medium impedance mode where the gate voltage is above the threshold of the n-device, but is not high enough to provide a good virtual ground at the drain The waffle-iron layout, which superimposes the drain metal wiring and the gate enhances the probability of this defect mode. Trying to turn off the breaker would only work if the module is designed for essentially no current when inactive, since the breaker would be self-polarizing. This solution is feasible but would impose additional precautions in the design of a module to avoid unpredictable and potentially malicious behaviour. A more robust solution would consist of fragmenting the power transistor into a multiplicity of independent

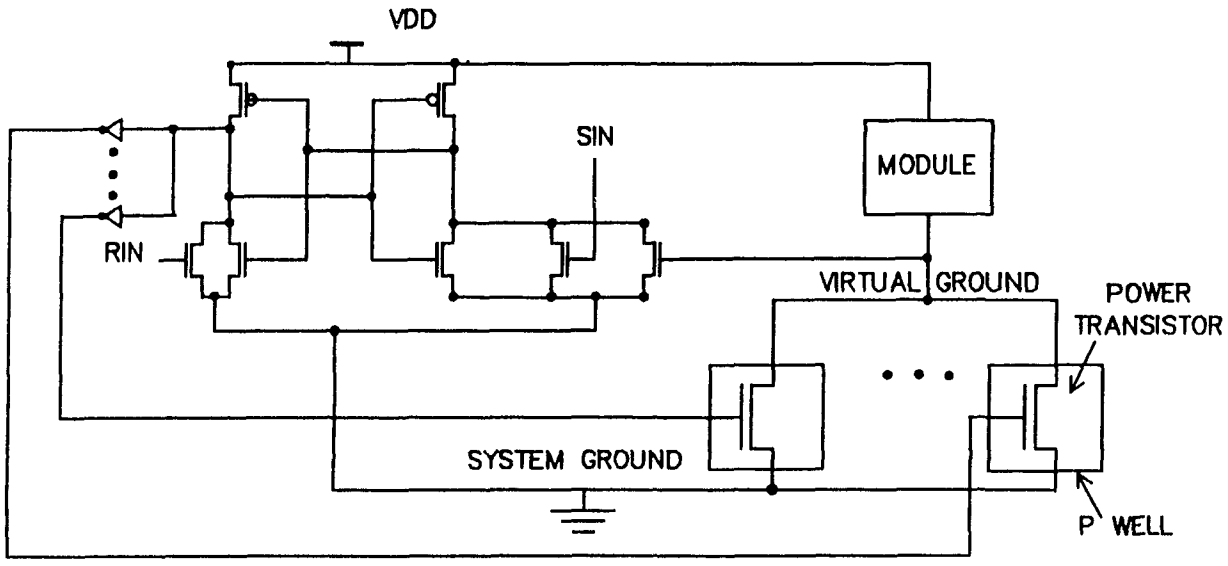

Figure 6.1 The Circuit Breaker with Multiplicity of Independent Transistors

transistors, each of which is individually controlled by independent drivers as shown in figure 6.1 [28]. The same drain to gate short would then simply result in an increased dynamic resistance in a breaker that cannot be turned off.

The current estimation method described in this thesis just presents a preliminary analysis. Further work has to be done before this technique can be evaluated with respect to existing ones. Future work involves developing the algorithm presented here for current estimation of typical modules in large area ICs.

A test chip which uses a processing element PE with a ground circuit breaker has already been submitted for fabrication. The test results will help in refining the current estimation technique.

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Appendix A

The details of the current estimation for the polycrossover is presented here. The electric current density $\vec{J}$ is defined as the

$$\lim \frac{\Delta I}{\Delta S} as \Delta S \longrightarrow 0 \tag{4.17}$$

Here ΔI is the current passing through an element of area ΔS. There is a particular orientation of this area, namely the one perpendicular to the lines of current flow for which ΔI is maximum. For this orientation $\frac{\Delta I}{\Delta S}$ is the magnitude of the average current density, and its limit as $\Delta S \longrightarrow 0$ is the magnitude $\vec{J}$ of the current density at the point in question. The direction of the vector is the direction of the flow at that point.

For any other orientation of the elementary area

$$\Delta I = J(\Delta S)\cos(\vec{J}, \hat{n}) \tag{4.18}$$

where $(\vec{J}, \hat{n})$ is the angle between $\vec{J}$ and the normal $\hat{n}$ to the area ΔS

If the vector element area is defined by

$$\overrightarrow{\Delta S} = (\Delta S)\hat{n} \tag{4.19}$$

We can write (4.18) as follows

$$\Delta I = \vec{J}.\overrightarrow{\Delta S} \tag{4.20}$$

Where the current density $\vec{J}$ is integrated over a closed surface surrounding the block.

The current density is proportional to the electric intensity $\vec{E}$.

$$\vec{J} = \sigma \vec{E} \tag{4.21}$$

Substituting (4.21) in (4.20)

$$\Delta I = \sigma \vec{E} . \vec{\Delta S} \tag{4.22}$$

$$I = \Sigma \Delta I = \Sigma \sigma \vec{E} . \vec{\Delta S} \tag{4.23}$$

Let us consider a single equipotential shown in Figure A.1 Figure A.2 gives the close up view of the encircled region in Figure A.1.

Now

$$\vec{E} = -grad\phi \tag{4.24}$$

, where ϕ is the scalar potential.

Figure 4.7 shows the equipotential lines in the region 1. The current flowing across AF and BD is known through simulations. So the only unknown is the current flowing across arc AHB. Figure A.2 is a part of a bigger layout shown in Figure A.1. Here a part of the equipotential, FAHBD is shown. Let us approximate the equipotential surface (arc AHB times depth of the channel(BR)) as shown in Figure A.2 by a

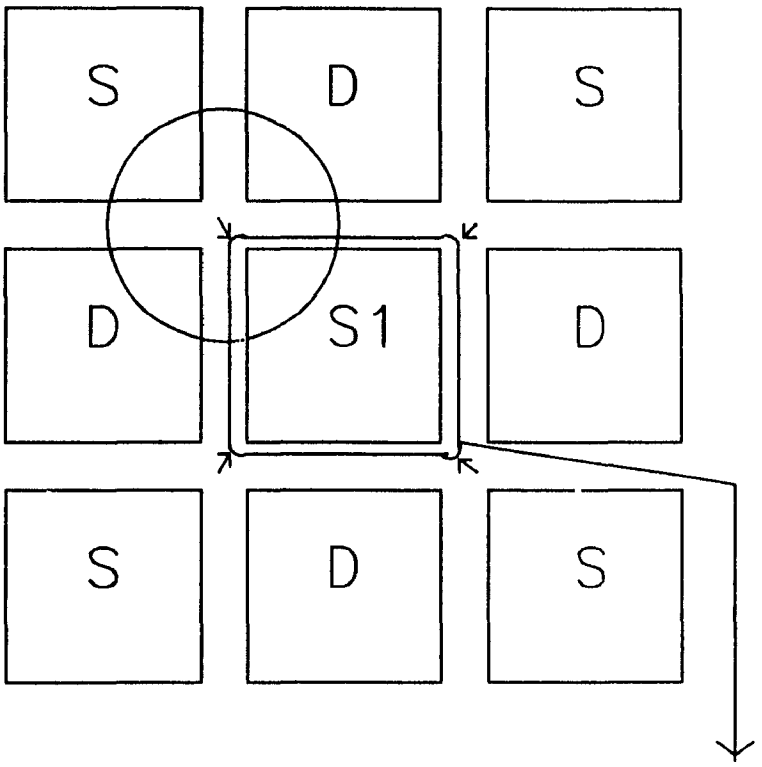

Figure .1 A Single Equipotential Line Under Consideration

concentric surface of a sphere with c as centre. The direction of the gradient of potential is along the radius.

Now the equation 4.24 can be written as

$$\sum\left(\sigma \vec{E} \cdot \vec{\Delta S} \cos(\vec{E}, \hat{n})\right) \tag{4.25}$$

where n is the unit vector normal to the surface of S. The equipotential line AHB associated with channel depth BR can be assumed as part of a sphere, the normal vector to the area and electric field are along the radial direction hence

$$\cos(\vec{E}, \hat{n}) = 1 \tag{4.26}$$

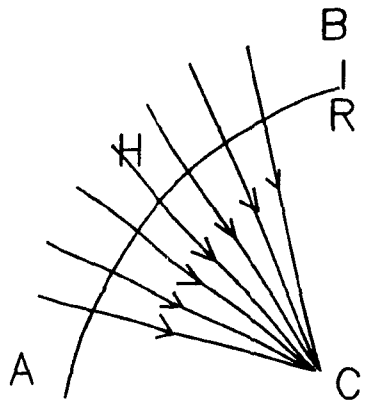

FIG 3
BR --depth of channel=150 -200 A
FIG 3 not drawn to scale
arc AHB =33000A
the arrows indicate the direction of field and normal

Figure .2 A Close Up View

Therefore (4.25) becomes

$$I = \Sigma\sigma \vec{E} \cdot \vec{\Delta} S \tag{4.27}$$

Since the charges are contained only in the channel, the area

ΔS =depth of the channel BR $\times$ small segment of arc AIIB(dr)

For a quick hand calculation, the electric field for 15-20 points on $A\hat{I}B$ is determined. Therefore (4.27) effectively reduces to

$$I = \sigma \times \text{depth of channel} \times Edr \tag{4.28}$$

Now

$$\sigma = ne\mu \tag{4.29}$$

Where ne is the charge contained in the channel per unit volume which is denoted by Q_n.

$$ne = Q_n = \frac{C_{ox}(V_g - V_t - V_x)}{\text{depth of the channel}} \tag{4.30}$$

substituting (4.29) and (4.30) in (4.28) we get

$$I = C_{ox}(V_g - V_t) \times \left(\sqrt{E_{1x}^2 + E_{1y}^2} * dr_1 + \right.$$

$$\sqrt{E_{2x}^2 + E_{2y}^2} * dr_2 + \sqrt{E_{3x}^2 + E_{3y}^2} * dr_3 +$$

$$\left.\sqrt{E_{20x}^2 + E_{20y}^2}\right) \times \mu \tag{4.31}$$

Edx is substituted by above expression for hand calculation. V_j is neglected as $V_{ds} = 0.3V$. Hence the conductivity σ is assumed to be constant all over the poly region which is a reasonable assumption since V_{ds} is very low(0.3V).

Therefore

$$I = 22.6\mu A \tag{4.31}$$

Therefore 22.6 μA is the current flowing into one source from a single poly-crossover. The remaining current of the polycrossover flows into the second source

By symmetry of the problem we can assume equal currents flowing into each source. Therefore the total current flowing into the sources due to a single crossover is equal to 45.2 μA.