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Design and Distortion Analysis of Fully Integrated Image Reject RF CMOS Frontends

by
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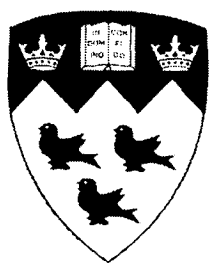

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A Thesis submitted to the Faculty of Graduate Studies and Research in partial fulfilment of the requirements for a degree of Doctor of Philosophy

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Abstract

This thesis presents the design and experimental results of a 7.3GHz notch image reject filter, combined with a 5.8GHz low-noise amplifier (LNA), for integrated heterodyne receiver front-ends. A new image reject filter implementation is proposed. Q-enhancement circuitry for on-chip inductors are used to optimize the depth of image rejection. Experimental results show that more than 62dB of image rejection at 7.3GHz can be obtained in a standard CMOS 0.18μm technology, while operating from a 1.8V supply. The LNA exhibits a gain of 15.8dB and an IIP3 of -5.3dBm while consuming 9mW of power. With maximum image rejection, the LNA-notch combination circuit achieves a 4.1dB noise figure at 5.8GHz. The proposed notch filter alone can operate from a 1V supply voltage. It is shown analytically how circuit stability can be ensured.

The implementation of new robust and stable high-Q CMOS image reject filters, which enables the realization of fully integrated heterodyne 5GHz RF receivers is also presented. A cascade of two notch filters with their image reject frequencies slightly offsetted is proposed, in order to obtain a wide image rejection bandwidth, without having to resort to the overhead of automatic tuning circuitry. Thus, power consumption, area, and complexity are significantly reduced. Experimental results show that more than 30dB of image rejection can be obtained in a standard 0.18μm CMOS technology, over a 400MHz bandwidth centered at 7.4GHz.

Finally, an approach to estimate the distortion in CMOS short-channel

Résumé

Cette thèse discute le design et les résultats expérimentaux d'un 7.3GHz filtre "notch" combiné à un amplificateur à bas-bruits (RF LNA) opérant à 5.8GHz, intégrés tous deux spécifiquement pour les receveurs hétérodynes implémentés avec la technologie submicronique de type métal-oxyde-semiconducteur complémentaire (CMOS). Une nouvelle topologie de filtre notch est proposée. Des circuits pour améliorer le facteur de qualité des inductances sur puce ont été utilisés afin d'obtenir la meilleure réponse possible du filtre de rejet. Les résultats expérimentaux démontrent que plus que 62dB de rejet peuvent être atteints à 7.3GHz dans une technologie 0.18μm CMOS standard, tout en opérant d'une source de tension de 1.8V. 15.8dB de gain, -5.3dBm de distorsion de modulation à l'entrée et 4.1dB de facteur de bruits (NF) ont été mesurés à 5.8GHz.

De nouveaux filtres robustes et stables dans la technologie CMOS, qui permettent l'intégration sur puce de receveurs hétérodynes opérant à 5GHz, sont aussi présentés. Deux filtres notchs, avec leur fréquence de résonance respective légèrement séparée, sont cascadés stratégiquement pour qu'ils procurent une large bande de rejet, sans l'utilisation des circuits complexes. Ceci permet une réduction significative de la complexité, de la dimension, et de la consommation d'énergie des receveurs hétérodynes. Les résultats expérimentaux prouvent que l'obtention de plus que 30dB de rejet d'image sur une bande de fréquence de 400MHz centrée à 7.4GHz peut être obtenue avec une technologie

0.18μm CMOS standard.

Finalement, une méthodologie pour estimer la distorsion dans la technologie CMOS submicronique dans les amplificateurs à bas-bruits est présentée. Des équations compactes et précises qui décrivent les effets de plusieurs paramètres parasites du transistor CMOS sur la distorsion sont dérivées. Pour la première fois, la distorsion du second ordre, qui est cruciale pour certains systèmes tel que les receveurs homodynes, est étudiée. Des équations décrivant la distorsion de modulation du troisième ordre dans les LNA sont aussi dérivées. Les équations dérivées sont vérifiées via des simulations et des résultats expérimentaux obtenus en testant un LNA opérant à 5.8GHz et alimenté à partir d'une source de tension de 1V. L'analyse suggérée prouve que la distorsion dans un LNA est indépendante du condensateur parasite C_{gs}. Des régles de conception pour optimiser la distorsion dans les CMOS LNA sont fournis.

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Table of Contents

Chapter 1 - Introduction - Wireless Systems

Since Hertz experimentally verified Maxwell's equations in the 1880s, Marconi developed the first commercial radio in 1898, and Fessensden transmitted voice and music via radio in 1900 [1] - a more than a $100 billions market for radio communication systems was born [2].

Recently, designing and integrating RF and microwave circuits has received considerable interest due to the explosive growth in the wireless telecommunication field [3]-[26]. An RF transceiver (transmitter/receiver) has the task of detecting a physical channel and transforming it into a low-frequency analog/digital signal for further processing at the receiver end. It also modulates the baseband signal and converts it into a high-power RF signal at the transmitter end (Fig. 1.1). As such, the transceiver performs RF, analog, and digital processing.

Analog and mixed-signal circuits were developed in the Complementary Metal Oxide Semiconductor (CMOS) technology in the mid-1970s [27]. It was only in the beginning of the 1990s that researchers in universities suggested using this low cost technology for RF applications. A fully integrated CMOS low noise amplifier was reported for the first time by Chang et al. in 1993 [28]. Almost a decade later, in 2001, the first fully integrated CMOS transceiver was published in the literature [29].

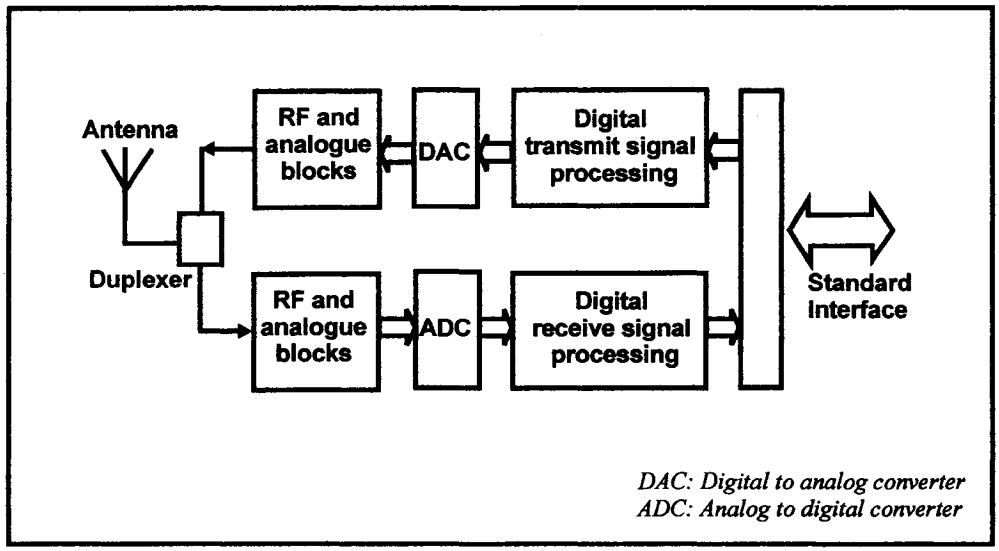

Figure 1.1 RF transceiver functions.

State-of-the-art CMOS technologies offer competitive performance in terms of noise and cutoff frequencies. With a 0.18μm gate length standard CMOS process, a minimum noise figure (NF) of less than 0.5dB was measured at 5.1GHz with an associated 16dB of gain [30], and an f_{max} of 150GHz was obtained by careful layout techniques [31]. Also, an f_{max} of more than 150GHz with a 0.8dB NF at 6GHz [32], and 64GHz and 100GHz oscillating frequencies [33] have as well been achieved using a CMOS 90nm gate length process. These performances are sufficient to allow the integration of circuits operating in the lower giga-Hertz range, and to cover most of today's consumer wireless applications. As a result, many efforts are ongoing on the integration of RF receivers in low-cost CMOS technologies. Such integration is necessary in order to enable the implementation of the RF front-ends alongside the digital signal processors, and allow low-cost single-chip fully integrated solutions.

Today, the CMOS technology is the dominant choice in applications such as wireless local area networks (WLAN) and Bluetooth. Its rapid evolution and the high level of integration it offers have made it an attractive candidate for wireless applications. It is also gaining popularity in GSM cellular circuits and Global Positioning Systems (GPS) [34]. In this Ph.D. thesis, two research topics related to the integration of CMOS

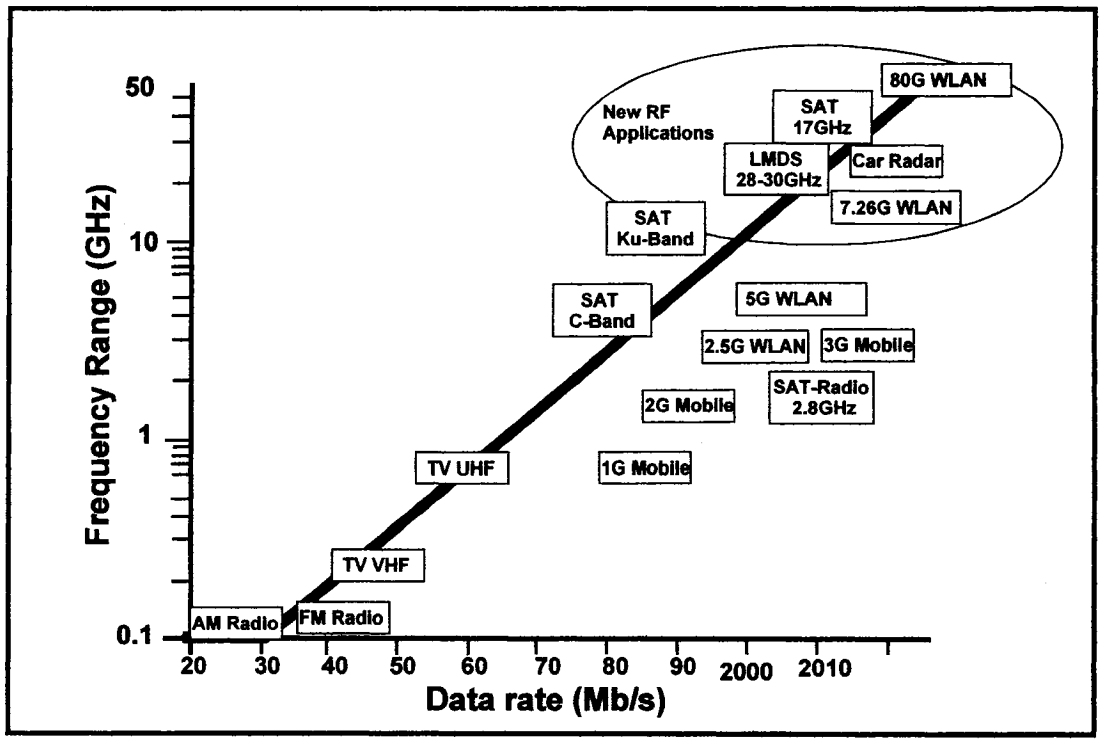

Figure 1.2 Radio frequency trends.

RF circuits are discussed, namely the design, fabrication, and test of CMOS image reject notch filters for 5GHz heterodyne receivers [35]-[40], and the distortion analysis of RF CMOS low noise amplifiers (LNAs) [41]-[42].

1.1 - Introduction to RF Applications

Nowadays, consumer applications are demanding an increasing amount of storage and memory, faster processors, higher resolution images and displays, etc. As a result, devices' speed and storage capabilities are increasing exponentially year after year, i.e. following Moore's law (Fig. 1.2). Therefore, higher data rate transfers between consumer devices are needed. For wireless communication systems, increasing data rates involves employing new modulation schemes to transfer more efficiently data in the available spectrum, and integrating RF circuits operating at higher frequency bands (5GHz and above). The first option is limited to data transfer rates of about 2.5bits/s/Hz, which might not be sufficient for future consumer demands. Higher data rates are currently obtained

by moving towards higher frequency bands. Following, a representative set of RF consumer applications are introduced.

1.1.1 - 400MHz and 900MHz ISM Bands

Besides the well-know wireless products such as cellular phones and pagers, examples of RF consumer products are many. For example, remote keyless entry (RKE) systems are implemented in more than 70% of today's vehicles. A transmitter using built-in authentication mechanisms is integrated on a remote key. The receiver is placed inside the vehicle. These systems operate in the Industrial, Scientific and Medicine (ISM) band at 400MHz or 900MHz [44]. RKE systems, including start and car finder, theft alarm, lock and unlock doors, are a high volume after-market accessories.

1.1.2 - Wireless Local Area Networks (WLAN)

In order to obviate the need for wired networks in offices, coffee shops, hotels, hospitals, homes, factories, airports, etc., communication between people or equipment can be made through a Wireless Local Area Network [45]. IEEE 802.11a/b/g WLANs standards are allowing wireless connectivity in network consumer electronic devices. Thanks to the convenient access to network resources they provide for portable computers and handheld devices, they are becoming key elements of many enterprise networks. Based on the current explosive growth of wireless networking, analysist predict that wireless connections could reach 40% of LAN networks by 2008.

1.1.3 - Cordless Phones

More and more households are using cordless phones. They operate in the 900MHZ, 2.4GHz or 5GHz frequency bands. Unfortunately, the 2.4GHz and 5GHz frequencies fall in the same frequency bands as the wireless 802.11b/g local area network standards. The 2.4GHz cordless phones standard is implemented based on the frequency hopping spread spectrum (FHSS) technology. FHSS hops from frequency-to-frequency across the entire 2.4GHz spectrum. On the other hand, 802.11b WLANs use direct sequence spread spectrum (DSSS) modulation, which transmits within approximately one

third of the 2.4 GHz spectrum. Therefore, since FHSS hops across the entire spectrum while DSSS remains in a single frequency band, a 2.4GHz cordless phone may clobber on an 802.11b network, causing the latter to fail. Hence, special care should be taken when installing WLAN networks.

1.1.4 - Global Positioning Systems

According to the Industrial Economics and Knowledge Center (IEKC) of the Industrial Technology Research Institute (ITRI), the Global Positioning System (GPS) production market may reach $21.5 billions worldwide by 2008 [46]. Originally intended for military use only, and funded by the US Department of Defense with more than $12 billions of investment, the GPS network became available for civilian use in 1980. Since then, GPS products have been developed for many commercial applications. With the continuous advancements in technologies, the prices and sizes of GPS systems are decreasing. GPS signals are currently used to determine or monitor objects' and people's locations, to facilitate marine, plane, and vehicle navigation, to create world maps, and to bring precise timing to the world. The system consists of a constellation of 24 satellites in six orbits. These satellites travel on pre-determined circular trajectories around the earth. Operating in the 1500MHz frequency band, they transmit coded positional and timing information continually. A receiver on earth picks up the signals and uses triangulation to calculate the user's exact location. Typically, three satellites are needed to provide the location, and a fourth one is used to determine the timing.

1.1.5 - Home Satellites

The home satellite television network is yet another RF application that has undergone an explosive growth in the last decade. It is still gaining popularity and is competing with cable TV. In the United States only, the market share for home satellites was 25 billions dollars as of December 2002 [47]. Frequency bands, such as 6, 14 and 17GHz, are currently being used for broadcasting the television signals.

1.1.6 - RFID Tags

The worldwide market for radio frequency identifications (RFID) tags is expected to jump from $300 millions in 2004 to $2.8 billions in 2009. During this period, RFID tags are expected to be used in many consumer applications, such as supply chains, livestock, domestic pets, pharmaceutical products, large freight containers, package tracking, etc. For example, the international Walmart chain started to mandate its suppliers to use this technology [48]. However, privacy issues related to many consumer RFID applications are currently being debated in courts and governments around the world.

Other consumer applications, such as wireless smart implants [49], are currently being investigated as well.

1.2 - Front-End Receivers

Until very recently, most of the RF 5GHz transceivers (transmitter/receiver) employed discrete building blocks, mainly based on high-cost technologies, such as the GaAs technology. To decrease the cost and the size of the circuits, researchers have been putting significant efforts to fully integrate transceivers on silicon (e.g. SiGe or CMOS technologies) [3]-[26]. The challenges for integrating systems operating at frequencies higher than 5GHz are numerous: The packages, the interconnections, the bonding wires, noise, the quality of the on-chip passive devices, the available transistors models, the parasitics, the input and output matching circuitry, etc., all need to be taken simultaneously into account early on during the design stage, in order to obtain the required system performance [50]-[51].

A simplified structure of a receiver is shown in Fig. 1.3. It mainly consists of an antenna, a duplexer, filters, mixers, amplifiers, detectors, and voltage controlled oscillators. The receiver needs to process very weak signals. Therefore, the noise generated by the receiver itself should be as small as possible. The performance of each component affects the sensitivity, the overall gain, and the noise behavior of the receiver.

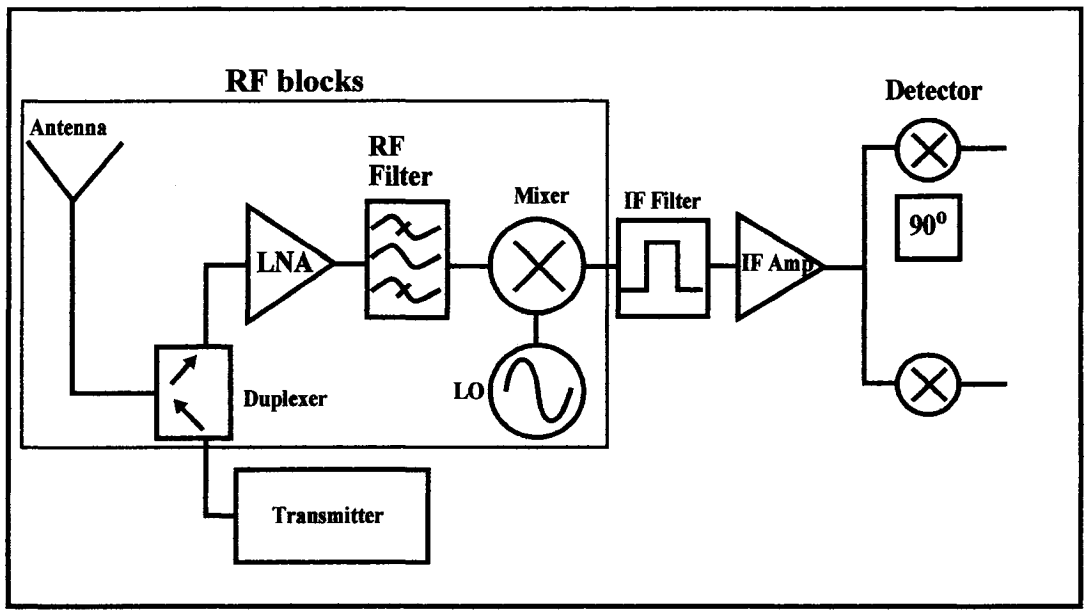

Figure 1.3 Simplified structure of a receiver front-end.

The following is an overview of the main RF blocks in a receiver.

1.2.1 - Antenna

The first block in the receiver chain is the antenna. The antenna, a conductive physical device, has the task of capturing and radiating RF signals, i.e. electromagnetic energies. It is an interface between the receiver's input and free space. It is characterized by its gain, bandwidth, radiation loss, beamwidth, resistive loss, noise, and size parameters. Typically, the output impedance of an antenna is set to 50Ω .

1.2.2 - Duplexer

The antenna is usually followed by a duplexer. The duplexer allows transmitting and receiving signals using a single antenna. An ideal duplexer provides infinite isolation between the receiver and the transmitter, and a 0dB loss for the transmitted and received signals. In order to minimize leakage from the transmitter to the receiver and vice-versa, 80 to 100 dBs of isolation may be required. For RF applications, a duplexer can be implemented using an RF switch, single-ended terminated filters, or circulators. The RF

switch allows toggling the antenna back and forth between the transmitter and the receiver. Typically, the toggling is controlled by a microprocessor or by a simple "push to talk" button. Single-ended terminated filters are also commonly used as duplexers. They are designed such as one of the filters provides a low impedance termination on the receiver port, and a high impedance termination on the transmitter port, while the second filter performs the inverse operation. They are employed in systems where the receiver and the transmitter operate at different frequency bands. Finally, circulators are three-port RF devices that allow signal propagation in one direction only. Signals appearing at port 1 can only flow to port 2 without reaching port 3, and signals appearing at port 2 transmit to port 3 and are isolated from port 1.

1.2.3 - Low Noise Amplifiers (LNA)

The LNA needs to provide enough gain to boost the desired signal above the noise floor, while adding minimal amount of noise and distortion. It is usually the first active circuit in the receiver chain: it is typically implemented with transistors and passive components, such as inductors and capacitors. The noise figure of the receiver depends heavily on the gain and on the noise behavior of the LNA. A high gain reduces the effect of noise on subsequent blocks in the receiver chain, which in turns enhances the overall receiver noise performance. However, too much gain can saturate the following stages.

Being inherently nonlinear, the transistors used to implement the LNA add distortion to the amplified signal. Thus, the output signal of an LNA is not perfectly linear. Intermodulation distortion, gain compression, and harmonic distortion are therefore observed, affecting the quality of the amplified signal. Besides gain, noise, and linearity, power consumption and size are important issues that need to be considered as well. Design considerations of low noise amplifiers are discussed in details in Chapters 2 and 4.

1.2.4 - Filters

Filters are commonly used in RF receivers. For example, preselect filters have the task of attenuating out of band channels, in order to prevent nearby strong interferers from producing intermodulation distortion and saturating the front-end receiver. They can be ceramic, lumped elements (inductors and capacitors) or Surface Acoustic Wave (SAW) filters. Image reject filters are used in heterodyne receivers. Traditionally, they have 50Ω input impedances, and are placed off chip. In order to increase the level of integration of receivers, on-chip filters with performances meeting specifications are needed. Moreover, decreasing the supply voltage and the power consumption is a great challenge in analog and RF filters [52]-[53]. Fully integrated single-ended and differential CMOS image reject filters are presented in this thesis. The problem of image rejection in heterodyne receivers is discussed in details in Chapter 3.

1.2.5 - Mixers

Mixers perform the frequency downconversion and upconversion tasks. In a simplified way, they can be viewed as multipliers of two signals. At the receiver end, the downconversion task consists of translating the RF signal to a lower intermediate frequency (IF) for further processing [54]. Typically, a mixer needs to handle large signals without adding distortion. At the transmitter end, upconverting the signal involves converting the IF signal to much higher frequencies. At the receiver and at the transmitter, new frequency components are generated at the output of the mixer, thus the transfer function of a mixer is inherently nonlinear.

1.2.6 - Local Oscillators (LO)

Local oscillators generate large sinusoidal reference signals operating at specific frequencies. In most RF receivers, a voltage controlled oscillator (VCO) is used [55]: A VCO is an oscillator, the frequency of which can be varied by changing the voltage on a control port of the circuit. The voltage on this port is usually set by a phase-locked-loop (PLL) system. Beside the frequency, key specifications for VCO designs are phase noise,

tuning range, spurious output levels, and lock time.

1.3 - Motivations of this Thesis

With the advances in CMOS technologies, it is now feasible to integrate low-cost and small-size multi-giga-Hertz receivers in CMOS [17]-[26]. For a fully integrated heterodyne system, many issues such as on-chip image rejection still need to be addressed. Homodyne and low-IF receivers do not suffer from image-rejection. However, the *1/f* noise and DC offsets can degrade the overall performance of a receiver and increase its complexity.

Typically, a heterodyne receiver employs off-chip image reject filters, which increase the cost and the complexity of the overall design. Image rejection of 30 to 80dB can be required, depending on the application. Research is currently being conducted on using active filters to suppress the signal at the image frequency in integrated heterodyne receivers [56]-[64]. Two elegant multi-GHz notch filters, which use a negative resistance to compensate for the on-chip inductor losses, were proposed by Macedo et al.[15] and by Rogers et al. [58]. Shown in Fig. 1.4-a and b, these circuits were integrated and demonstrated in a bipolar technology. When directly mapped to a CMOS implementation, the overall performance of the circuit proposed in [15] is limited by many factors. For example, the first limitation identified was related to the fact that the DC current of the notch circuit affects the DC behavior of the LNA. The depth of the notch is controlled by varying the biasing current of transistor B3. By varying the biasing of B3, the DC biasing of B2 is also altered. Due to the strong channel length modulation effect in modern submicron CMOS technologies (λ can be as large as 0.4 in a CMOS 0.18μm standard technology), the response of the LNA is therefore affected when tuning the notch depth. Preferably, the DC current of the notch filter should be independent of that of the LNA. A detailed discussion of this circuit's limitations is carried out in Chapter 3, along with the proposal for a novel notch filter circuit that does not suffer from this limitation and others.

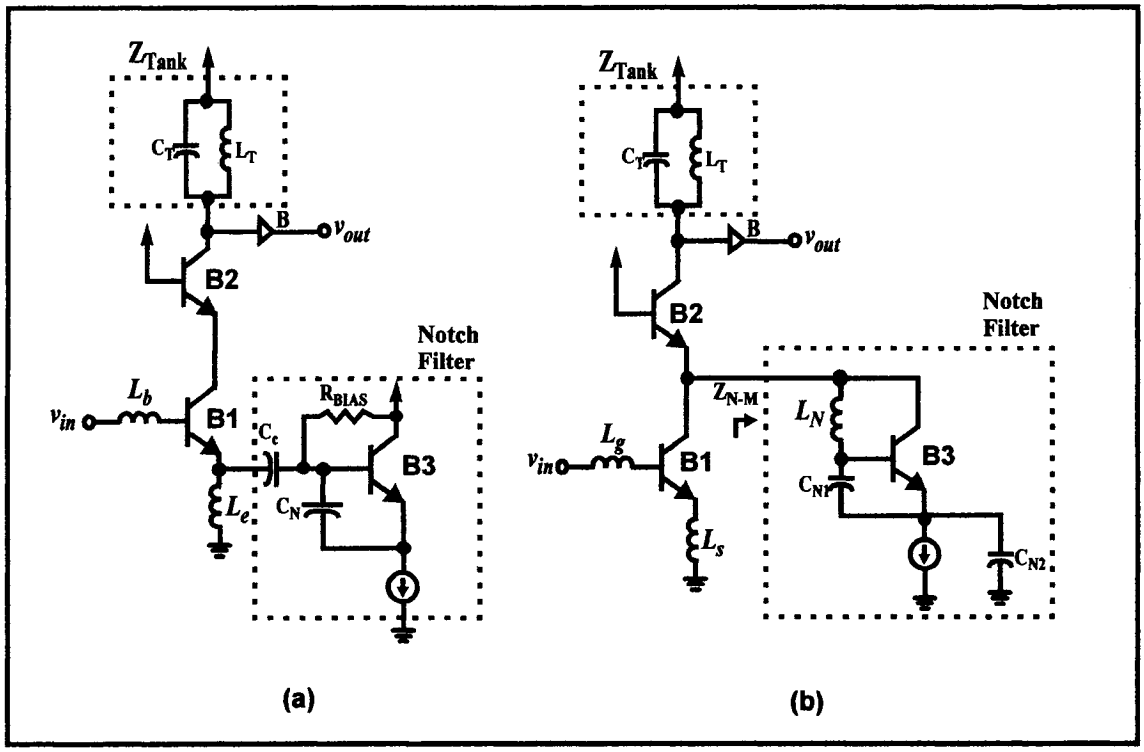

Figure 1.4 LNA-notch circuits proposed by a) Rogers et al. [58], and b) Macedo et al. [15].

The highest frequency of a CMOS notch filter reported to date is at 4.2GHz ([18],[63]), and the highest image rejection obtained was 50dB at 2.2GHz [60]. Most of the CMOS notch filters reported employ differential topologies, and are based on cross-coupled differential pairs connected in parallel with the on-chip inductors, in order to enhance their quality factors (e.g. transistors M5 and M6 in Fig. 1.5). Two new differential CMOS notch filters operating above 7GHz are presented in this thesis in Chapter 5.

One of the objectives of this work was to demonstrate the feasibility of implementing image-reject filters in the 7.3GHz range in CMOS for a 5GHz high IF heterodyne receiver, without using any off-chip component. A prototype chip incorporating a single notch image reject filter (IRF) operating at 7.3GHz, combined with a 5.8GHz low noise amplifier, was first implemented and tested. Chapter 3 of this thesis presents the design and experimental results of this chip. This design is then used to

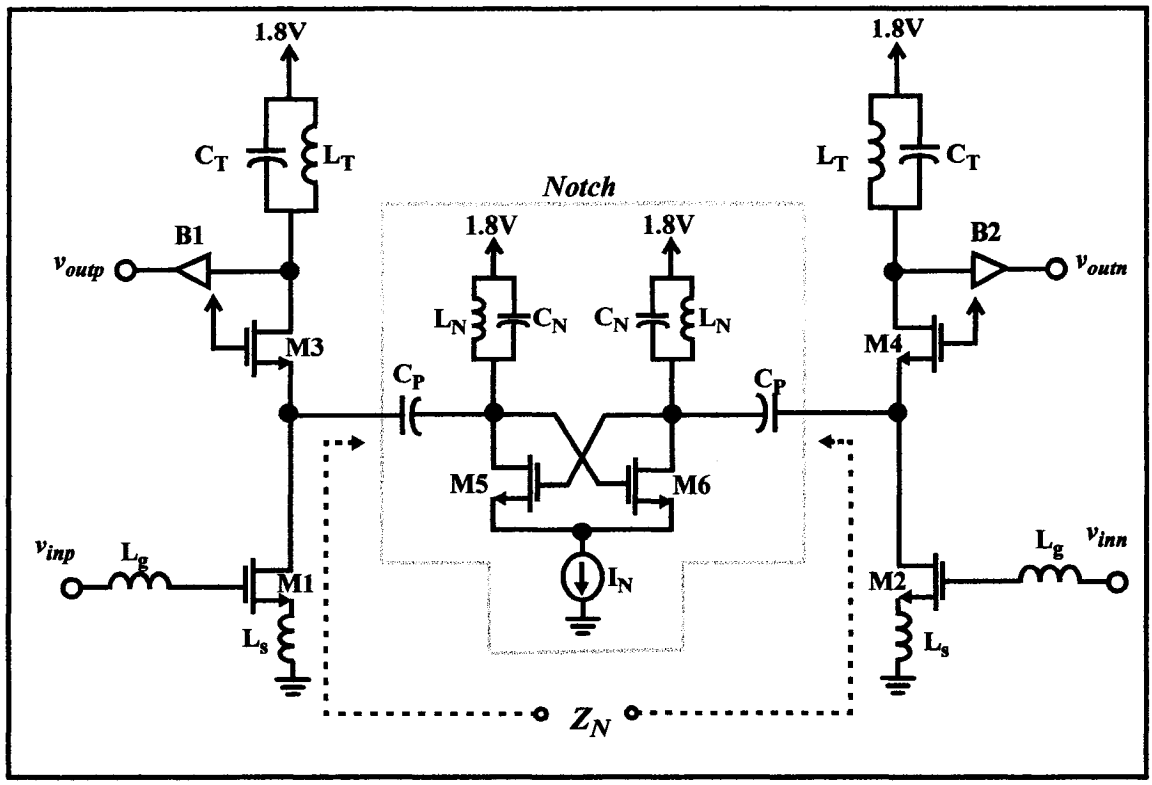

Figure 1.5 Structure of the LNA image reject filter proposed in [61].

implement a double IRF front-end receiver.

The proposal of a novel heterodyne front-end receiver architecture, that allows a simple implementation of fully integrated heterodyne 5GHz RF receivers, is then presented. It is one of the major contributions of this work. The front-end circuitry consists of a low noise amplifier and of a cascade of two notch filters. The notch filters, which use on-chip inductor Q-factor enhancement techniques, are designed to provide a strong and wide bandwidth of image rejection (IR), eliminating the need for accurate IR tuning circuitry. Traditionally, a single image reject filter is used. Automatic tuning circuits are then needed to properly set the image reject frequency, which considerably increases the power consumption and the complexity of the receiver. The objective of this work is to demonstrate the feasibility of implementing fully integrated heterodyne 5GHz front-end receivers in a standard CMOS 0.18μm technology, without using PLL-based automatic tuning [65]-[78], or calibration circuits [79] for tuning the image rejection frequency. Thus, the cost and the power consumption of the front-end receiver can be

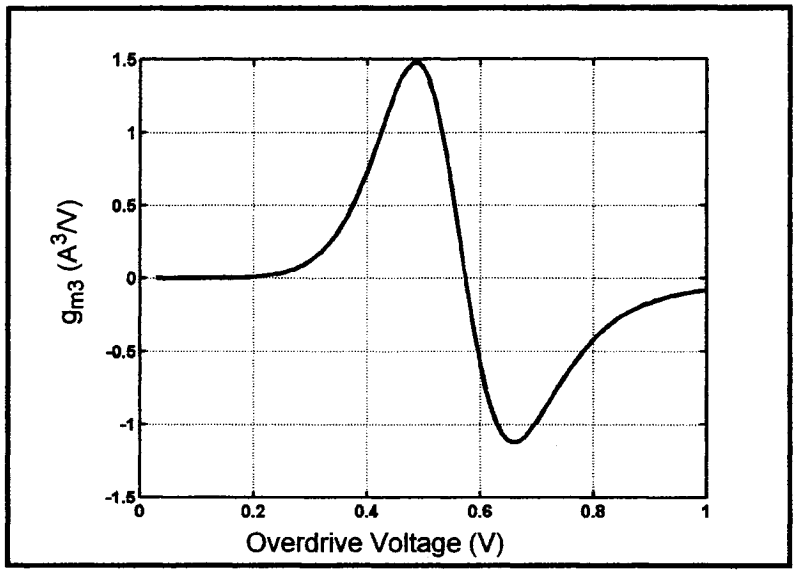

Figure 1.6 Characteristics of g_{m3} vs. the overdrive voltage of a standard 100μm width CMOS 0.18μm gate length transistor.

considerably reduced.

LNAs are widely used in telecommunication systems (e.g. [3]-[26], [80]-[81]). Their linearity is becoming of prime importance for modern RF receivers [82]-[88]. Even order harmonics generate DC offsets in homodyne receivers, while third-order intermodulation harmonics resulting from mixing with interferers in adjacent channels can corrupt the desired downconverted signal.

Several studies of the effects of CMOS transistors characteristics on RF LNAs have already been reported, e.g. by Kang et al. [82] and Toole et al. [83]. The analysis reported in [82] discusses the third order distortion behavior of CMOS transistors for RF applications. The results presented were based on empirical coefficients obtained from measurements of specific devices. The analysis in [83] attempted to exploit a "sweet-spot" in the third-order distortion response, without providing practical detailed equations relating specific transistor parameters to distortion. In a CMOS transistor, the third-order transcondunctance term (g_{m3}) tends to zero at a certain biasing condition, when the transistor is operating in the moderate region, as shown in Fig. 1.6. At this biasing point, also known as the "sweet-spot" point, theoretically, the third-order harmonic distortion

would tend to be zero, which would result in an infinite third-order output intercept point (OIP3). In reality, due to the cross-modulation between higher order terms, the OIP3 turns out to be finite, as will be demonstrated in Chapter 4. It will also be shown that this biasing point does not necessarily optimize the distortion level in *practical* RF CMOS LNAs.

The analysis in [84] provided distortion models for high-frequency CMOS transistors, without providing distortion-aware design guidelines for LNAs. Up to date, all reported studies do not provide closed form frequency-dependent expressions describing the second-order harmonic distortion in RF CMOS LNAs, which is a major problematic issue in modern homodyne receivers. An approach to estimate the distortion in CMOS short-channel (0.18μm gate length) RF low noise amplifiers, based on Volterra's series, is presented. Compact and accurate frequency-dependent closed form expressions describing the effects of the different transistor parameters on harmonic distortion are derived. For the first time, the second order distortion (HD2), which is crucial for some systems such as homodyne receivers, is studied. Equations describing third-order intermodulation distortion in RF LNAs are reported. Distortion-aware design guidelines for RF CMOS LNAs are also provided.

1.4 - Thesis Outline

Chapter 2 gives an overview of the main design issues in CMOS LNAs. Issues such as distortion, noise, RF layout optimization techniques, and on-chip inductors are discussed.

The design procedure and specifications of a 7.3GHz CMOS notch filter, along with experimental results, are presented in Chapter 3. The image reject (IR) problem in heterodyne receivers is summarized in Section 3.2.1. Special focus in this chapter is given to the negative resistance technique which was used by Macedo et. al. in [15] to implement a bipolar notch filter. As previously mentioned, when the latter is integrated in a CMOS technology, its overall performance is limited by many factors, which are

discussed in details in Section 3.3. A proposed novel notch circuit capable of mitigating these limitations is presented in Section 3.4. Experimental results are reported in Section 3.5. Section 3.6 outlines the design procedure of the proposed cascade image reject filter architecture. Experimental results and discussions are reported in Section 3.7, followed by a comparison between the proposed implementation and other state-of-the-art designs.

Distortion analysis of LNAs is carried out in Chapter 4. An overview of the limitations of the use of the sweet-spot approach for RF applications is first provided. The procedure to obtain closed-form expressions describing the distortion in nonlinear circuits using Volterra's series is presented. The distortion analysis of a single-transistor amplifier and of a folded cascode amplifier are discussed in details. Distortion-aware design guidelines for RF LNAs are provided in Section 4.5. This chapter concludes with a comparison of the analytical results with measured results from an LNA chip prototype.

Differential CMOS IR filters are discussed in Chapter 5. PLL systems are also introduced, along with the implementation of a new charge pump circuit.

Finally, this thesis concludes with a summary of the proposed work and with suggestions for future research topics.

1.5 - Summary of Thesis Contributions

The following is a summary of the contributions of this thesis:

1- Chapter 3: New CMOS Circuit Implementation of a Notch Filter (7.3GHz) with 62dB of Image Rejection[1] [36], [38]:

1.1- A new image reject filter (IRF) circuit in CMOS is proposed. The design and experimental results of a 7.3GHz CMOS implementation, combined with a 5.8GHz low-noise amplifier (LNA) for integrated heterodyne receiver front-ends, are presented. Experimental results show that more than 62dB of image rejection at 7.3GHz can be obtained in a standard CMOS 0.18μm technology, while operating from a 1.8V supply voltage. The proposed notch filter alone can operate from a 1V supply voltage.

1.2- Q-enhancement circuitry for on-chip inductors are used to optimize the depth of the image reject filters. It is shown analytically that the latter can be designed to be inherently stable with the added circuitry.

Main contribution:

R. A. Baki and M.N. El-Gamal, "A CMOS notch filter (7.3GHz) with 62dB of image rejection for wireless receivers", *Presented at the 2004 IEEE Asia Pacific Microwave Conference (APMC 2004) - Paper number APMC/04/I/540, Dec. 2004.*

2- Chapter 3: RF CMOS Fully-Integrated Heterodyne Front-End Receivers Design Technique for 5GHz Applications [35]-[37].

2.1 The implementation of a robust, unconditionally stable, and high-Q image reject filter in standard CMOS is presented, enabling the realization of on-chip heterodyne receivers at 5GHz and beyond.

1. Second position - The Canadian Microelectronic Cooperation (CMC) award annual research competition MR&DCAN, September 2004.

2.2 The use of two cascaded notch filters is proposed, with slightly offsetted frequencies, resulting in a wide rejection bandwidth, thus eliminating the overhead of automatic tuning.

Main contributions:

R. A. Baki and M.N. El-Gamal, "Robust multi-GHz (7.4GHz) on-chip image rejection in CMOS", *the 2005 IEEE Custom Integrated Circuits Conference, accepted, San Diego, USA, to be presented in September 2005.*

R. A. Baki and M.N. El-Gamal, "Robust multi-GHz (7.4GHz) on-chip image rejection in CMOS", *Submitted to the IEEE Journal of Solid-State Circuits, June 2005.*

3- Chapter 4: Distortion Analysis of RF CMOS Short Channel Low Noise Amplifiers [41]-[42]:

3.1- An approach to estimate the distortion in CMOS short-channel (0.18μm gate length) RF low noise amplifiers (LNA), based on Volterra's series, is presented.

3.2- For the first time, the second order distortion (HD2), which is crucial in homodyne receivers, is studied.

3.3- Compact and accurate frequency-dependent closed form expressions describing the effects of the different transistor parameters on harmonic distortion are derived. The analytical analysis is verified through simulations and measured results from a 0.18μm CMOS 5.8GHz folded-cascode LNA prototype chip geared towards sub-1V operation.

3.4- Distortion-aware guidelines for designing LNA's are presented, and are verified through simulation and analytical results.

Main contribution:

R. A. Baki, T.K. Tsang, and M.N. El-Gamal, "Distortion in RF CMOS short channel low noise amplifiers", *the IEEE Transactions on Microwave Theory and Techniques, accepted, to appear in September 2005.*

4- Chapter 5: Other contributions:

4.1- A novel low-voltage CMOS charge pump, intended for 5GHz and above phase locked-loop system, is proposed. Design techniques to decrease the glitches in the charge pump output signal are reported. The circuit was designed when investigating the possibility of designing very-low voltage PLLs **[43]**.

4.2- The design and the simulation results of two new differential image reject filters are presented **[39]-[40]**.

Chapter 2 - Issues In Implementing RF CMOS LNAs

In wireless receivers, the first active circuit following the antenna is the low noise amplifier (LNA). The signal received at the antenna is typically in the micro-volts range, which explains the need of amplifying it before any further processing. The LNA has the task of providing gain, ideally without adding noise and distortion. Noise deteriorates the sensitivity of the receiver. Even order harmonics generate DC offsets in homodyne receivers, while third-order intermodulation distortions, resulting from mixing with interferers in adjacent channels, can corrupt the desired downconverted signal channels. This chapter discusses the main design issues of CMOS LNAs.

This chapter begins with definitions of the performance metrics for LNAs. In heterodyne receivers, an image reject filter follows the LNA. The performance of an integrated filter depends mainly on the quality of the on-chip inductors. The quality of integrated inductors in standard CMOS technologies is discussed in Section 2.2. An overview of Q-enhancement techniques for on-chip inductors is presented in Section 2.2.2. In order to optimize the performance of RF integrated circuits, the layouts of the inductors, of the interconnections, and of the transistors need to be carefully considered. This subject is addressed in Section 2.3. The three LNA topologies used in this thesis are then presented, namely the single transistor amplifier, the cascode amplifier and the folded-cascode amplifier, with a derivation of their design equations.

2.1 - Performance Metrics

2.1.1 - Noise Sources in CMOS Transistors

A- Thermal noise

Thermal noise, also referred to as Johson or Nyquist noise, is one of the dominant noise sources in CMOS transistors at high frequencies. Randomly varying motion of charge carriers due to the thermal agitation in conductors and resistors give rise to a random voltage. Its amplitude increases with increasing resistance or temperature. For a resistance R, the generated thermal noise voltage in root mean square (*rms*) is given by

$$\overline{v_n^2} = 4kTR\Delta f, \tag{2.1}$$

where k is the Boltzmann's constant and Δf is the noise bandwidth in Hertz. For a 50Ω resistor, about $1nV/\sqrt{Hz}$ of thermal noise is generated. It is modelled as a voltage source in series with an ideal resistor, or as a current source in shunt with the resistor. For a specific resistance value, thermal noise can be optimised by decreasing the temperature, if possible, and by limiting the bandwidth Δf.

In a MOSFET transistor, thermal noise is mainly generated by the fluctuations of charges in the channel. The channel itself has an internal resistance, with the current noise given by

$$\overline{i_n^2} = 4kT\gamma g_{do}\Delta f, \tag{2.2}$$

where g_{do} is the drain source conductance at zero drain to source voltage (V_{DS}). γ is a parameter that equals 1 at zero V_{DS}, and tends in saturation towards 2/3 and 2-3 in long- and short-channel CMOS devices, respectively. The distributed gate resistance in MOS transistors also adds thermal noise. However, this noise contribution can become insignificant with proper transistor layout.

B- Shot noise

When a current is flowing in a MOSFET transistor, the random arrival times of charges crossing the source and the drain junctions generate shot noise. This source of noise is mainly due to the non-uniform flow of charge carriers crossing potential barriers. It can be modelled as a noise current source, connected between the drain and the source of a MOSFET transistor. The shot noise of a transistor with an average biasing current I_{DC} is given by (in *rms*)

$$\overline{i_n^2} = 2qI_{DC}\Delta f, \tag{2.3}$$

where q is the electronic charge. It can be seen from Eq. (2.3) that the shot noise depends mainly on the biasing current of the active device and on the noise bandwidth. Reducing it is possible by decreasing the biasing current of the active device.

C- 1/f noise

The random release and trapping of charges in MOSFET transistors due to lattice defects and surface impurities generate *1/f* noise, also referred to as flicker noise. The *1/f* noise in MOSFETs is modelled as a current source, and its mean-square value is given by

$$\overline{i_n^2} = \frac{K}{f} I_{DC}^a \Delta f, \tag{2.4}$$

where K and a are device-specific constants. Typically, K for NMOS transistors is 50 times larger then for PMOS transistors. Intuitively, using a larger transistor may decrease the effect of the *1/f* noise, since larger transistors offer a larger gate capacitance, which in turn helps decreasing charge fluctuations in the channel. Finally, it should be noted that for RF LNAs, the *1/f* noise does not play a major role since the signal amplification occurs in a narrow bandwidth at very high frequencies. However, this source of noise is problematic in receiver designs in general, since it corrupts the desired signal at baseband.

D- Noise figure

In LNA designs, the noise performance is characterized by the noise factor parameter. The noise factor measures the degradation of the input signal to noise ratio caused by a given network. It is defined as

$$F = \frac{SNR_i}{SNR_o} = \frac{S_i/N_i}{S_o/N_o}, \tag{2.5}$$

where SNR_i and SNR_o are the input and output signal to noise ratios, respectively. In RF circuits, the noise factor is more commonly expressed in dB as

$$NF = 10\log F \text{ dB}, \tag{2.6}$$

where NF stands for Noise Figure.

2.1.2 - Distortion

When applying a sinusoidal input to a linear circuit, it is well known that the output signal will also be a sinusoidal waveform, with the same frequency. However, since many of the basic electronic devices are nonlinear (e.g. bipolar and MOS transistors), most circuits will distort the input signal to a certain extend. The output will consist of the same input frequency, also referred to as the fundamental, accompanied by higher-order harmonics at multiples of the input frequency. Assuming a weakly nonlinear system, i.e, a system for which the output signal v_o converges with the first few terms, v_o can be expressed in terms of the input signal v_i as

$$v_o = a_o + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \ldots, \tag{2.7}$$

where a_0 represents the DC term, a_1 is the fundamental component, a_2 and a_3 correspond to the second and third order distortions, respectively. The sizes of these high-order harmonics set an upper limit on the largest acceptable input signal that can be processed by a circuit.

In RF circuits, a high level of distortion deteriorates the overall performance of

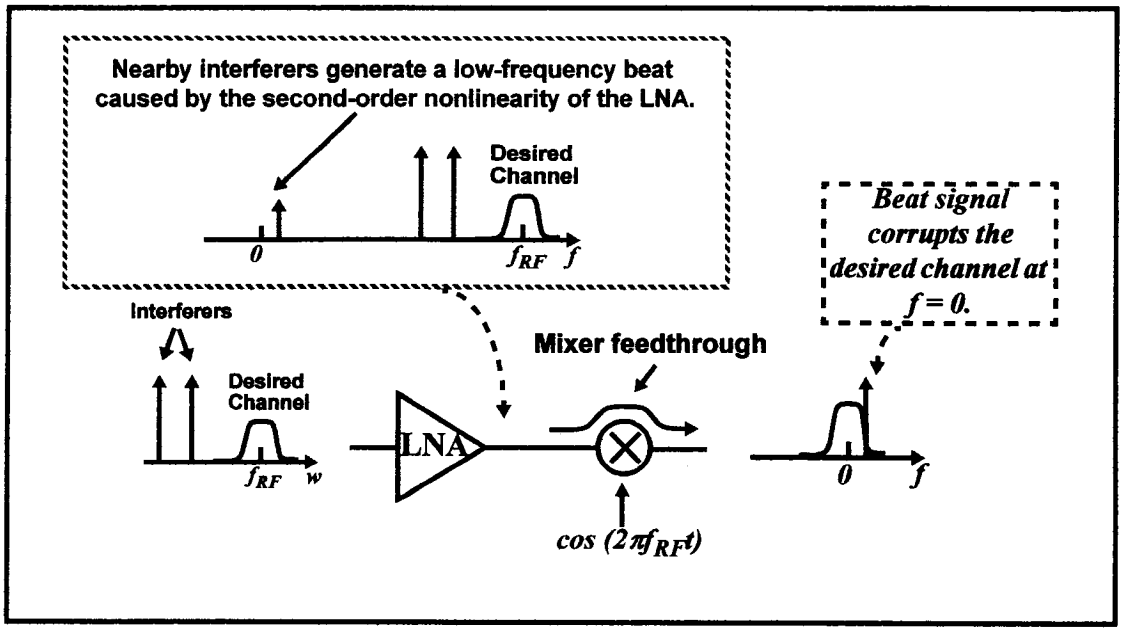

Figure 2.1 Corruption in a direct-conversion receiver due to second-order distortion.

the receiver. For example, the second-order harmonic distortion can severally affect the performance of direct-conversion receivers. This phenomenon is illustrated in Fig. 2.1. Suppose that alongside the desired channel, two strong interferers in adjacent channels appear at the input of the low-noise amplifier, as show in Fig. 2.1. Due to the second-order distortion behavior of the LNA, these interferers cross-modulate and generate a low-frequency beat. If an ideal mixer follows, this low frequency beat will not corrupt the down-converted signal. Unfortunately, mixers have a finite amount of feedthrough. As a result, a portion of this beat appears at low frequencies and corrupts the desired channel. Design guidelines to enhance the second-order distortion behavior in LNAs will be provided in this thesis in Chapter 4.

In RF LNAs and filters, distortion is typically quantified by the 1dB compression point and the third-order intercept point (IP3). Consider an amplifier with a linear gain G (dB) at a certain frequency for small input signals (Fig. 2.2). By increasing the power of the input signal, a point is reached where the output signal stops following asymptotically the linear gain, due to devices saturation. The input power that causes a 1dB drop in the linear gain is called the 1dB compression point. The 1dB compression point is approximately equal to

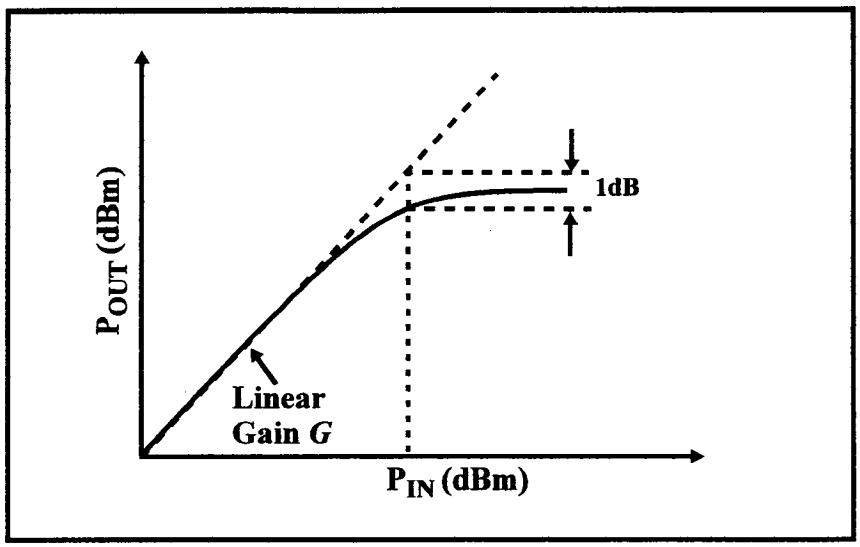

Figure 2.2 1 dB compression point.

$$G_{1dB} = \sqrt{0.145\left|\frac{a_1}{a_3}\right|}, \tag{2.8}$$

where the coefficients a_1 and a_3 are defined in Eq. (2.7).

Applying a two-tone input signal $v_i = A(\cos 2\pi f_1 t + \cos 2\pi f_2 t)$ to a system with a function given by Eq. (2.7), results in an output signal of the following form

$$v_o = a_o + a_1 A(\cos 2\pi f_1 t + \cos 2\pi f_2 t) + a_2 A^2(\cos 2\pi f_1 t + \cos 2\pi f_2 t)^2 + a_3 A^3(\cos 2\pi f_1 t + \cos 2\pi f_2 t)^3 + \ldots \tag{2.9}$$

The spectrum of v_o is shown in Fig. 2.3, where IM and HD stand for intermodulation and harmonic distortion, respectively. Expanding equation (2.9), the output tones at the frequency $f = f_2 - f_1$, also referred to as the second-order intermodulation product (IM_2), and the output tones at frequencies $f = 2f_1 - f_2$ and $f = 2f_2 - f_1$, also referred to as the third-order intermodulation products (IM_3), are given by:

$$\text{at } f = f_2 - f_1 : v_2 = a_2 A^2 \cos(2\pi f_1 - 2\pi f_2)t, \tag{2.10}$$

$$\text{at } f = 2f_1 - f_2 : v_3 = \frac{3}{4} a_3 A^3 \cos(4\pi f_1 - 2\pi f_2)t, \tag{2.11}$$

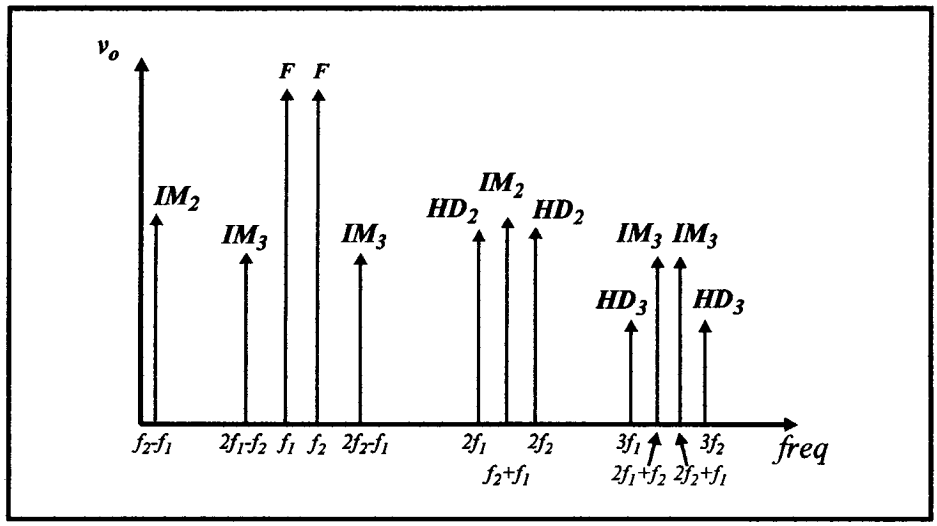

Figure 2.3 Output spectrum of a nonlinear system with a two-tone input signal at frequencies f_1 and f_2.

$$\text{and at } f = 2f_2 - f_1 : v_3 = \frac{3}{4}a_3 A^3 \cos(4\pi f_2 - 2\pi f_1)t. \tag{2.12}$$

If f_1 is close to f_2, the IM_3 tones appear in the vicinity of the f_1 and f_2 signals.

The problem that arises from the third-order intermodulation distortion products is illustrated in Fig. 2.4 . Consider the front-end section of a receiver. The antenna selects a weak signal, shown as the desired channel signal. Two strong interferers operating at nearby channels are partially selected by the antenna and appear at the input of the LNA as well. If the amplifier is nonlinear with a strong third order distortion behavior, the two interferers generate a third-order intermodulation distortion term, which might fall in the same frequency band as the desired amplified channel. This phenomenon corrupts the desired signal and degrades the overall selectivity of the receiver. It is characterized in RF circuits by the third-order input intercept point (IIP3) performance metric. In Fig. 2.4-b, the linear output power and the third-order intermodulation are plotted versus the input signal power on a logarithmic scale. The IIP3 is defined as the power of the input signal at which the extrapolations of the linear output and of the third-order intermodulation product lines intercept. The second-order input intercept point (IIP2) can be determined

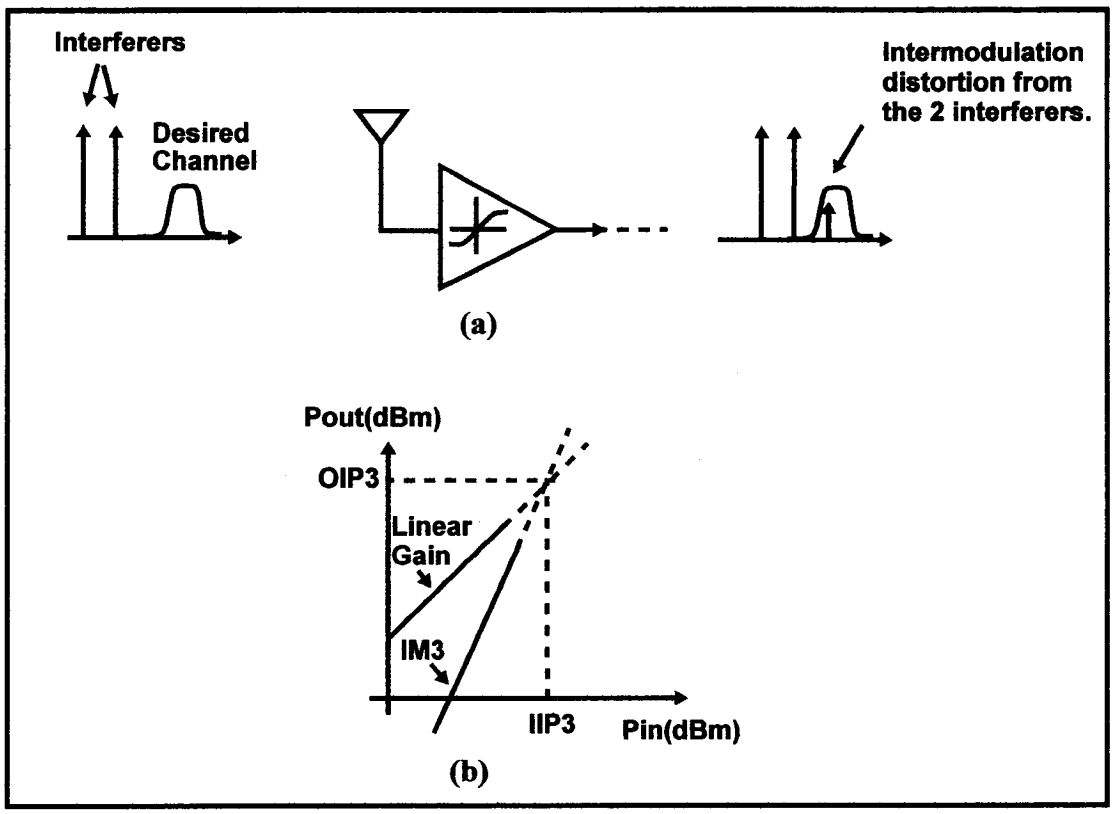

Figure 2.4 a) Corruption in a receiver due to third-order intermodulation distortion from two strong interferers. b) Concept of the third-order intercept point.

in a similar way.

In short-channel CMOS transistors, the main source of distortion comes from the nonlinear behavior of the transconductance. The AC current in a MOS transistor can be modelled as

$$\begin{aligned} i_{ds}(v_{gs}, v_{ds}) &= g_m v_{gs} + g_d v_{ds} \\ &+ g_{m2} v_{gs}^2 + g_{md} v_{gs} v_{ds} + g_{d2} v_{ds}^2 \\ &+ g_{m3} v_{gs}^3 + g_{m2d} v_{gs}^2 v_{ds} + g_{m2d} v_{gs}^2 v_{ds} + g_{d3} v_{ds}^3 \cdots \end{aligned} \quad , \qquad (2.13)$$

where g_{mn} is the n^{th} order transconductance term, g_{dn} is the n^{th} order output conductance term, and the g_{md} term represents the cross modulation between g_{mn} and g_{md}. Assuming the output transconductance to be linear, and the cross modulation between the transconductances is negligible, equation (2.13) is simplified to

$$i_{ds}(v_{gs}, v_{ds}) = g_m v_{gs} + g_d v_{ds} + g_{m2} v_{gs}^2 + g_{m3} v_{gs}^3 + \ldots \quad . \tag{2.14}$$

The second order harmonic distortion would depend on the even-order terms, while the third order distortion on the odd-order ones. The output third-order intermodulation point (OIP3) is related to the input third-order intermodulation point (IIP3) as follows

$$OIP3 = IIP3 + Gain = 20\log\left(2\sqrt{\frac{g_{m1}}{3g_{m3}}}\right) + Gain \quad \text{(dB)}, \tag{2.15}$$

where *Gain* is the LNA gain at the frequency of interest. Note that Eq.(2.15) is only accurate at low-frequencies and at low-distortion levels. At RF frequencies, where parasitic capacitors and inductors heavily affect the behavior of a circuit, the expression for the IIP3 term in Eq. (2.15) does not hold - The IIP3 becomes frequency dependent, as it will be discussed later on.

Figure 2.5 shows the behavior of g_{m1}, g_{m2}, and g_{m3} for a typical 0.18μm gate length, 100μm width transistor, obtained by differentiating the drain current of the MOS transistor from BSIM3v3 simulations. Fager et al. demonstrated that these plots accurately represent the transconductances measured experimentally, and that they can be used to model the behavior of distortion in MOSFET circuits [89]. As it can be seen in Fig. 2.5, the second-order transconductance g_{m2} starts off around $0A^2/V$ at zero V_{gs}, then increases before reaching a maximum value at a small overdrive voltage (V_{gs}-V_t). Further increase in V_{gs} results in decreasing g_{m2}. As a result, g_{m3}, obtained by differentiating g_{m2} with respect to V_{gs}, decreases to zero at a very small overdrive voltage, i.e. when the transistor is still operating in the moderate inversion region. Therefore, theoretically, if the transistor is biased at this operating point, also known as the "sweet-spot" point [83], the third-order harmonic distortion would tend to be zero, which would result in an infinite third-order output intercept point (OIP3). It is an attractive line of thought to follow for analog circuit designs in general. Besides, the corresponding biasing current is small, which minimizes the overall power consumption. In reality, due to the cross-modulation between higher order terms, the OIP3 turns out to be finite, as it will be demonstrated in Chapter 4. The latter discusses in details the distortion behavior in short-

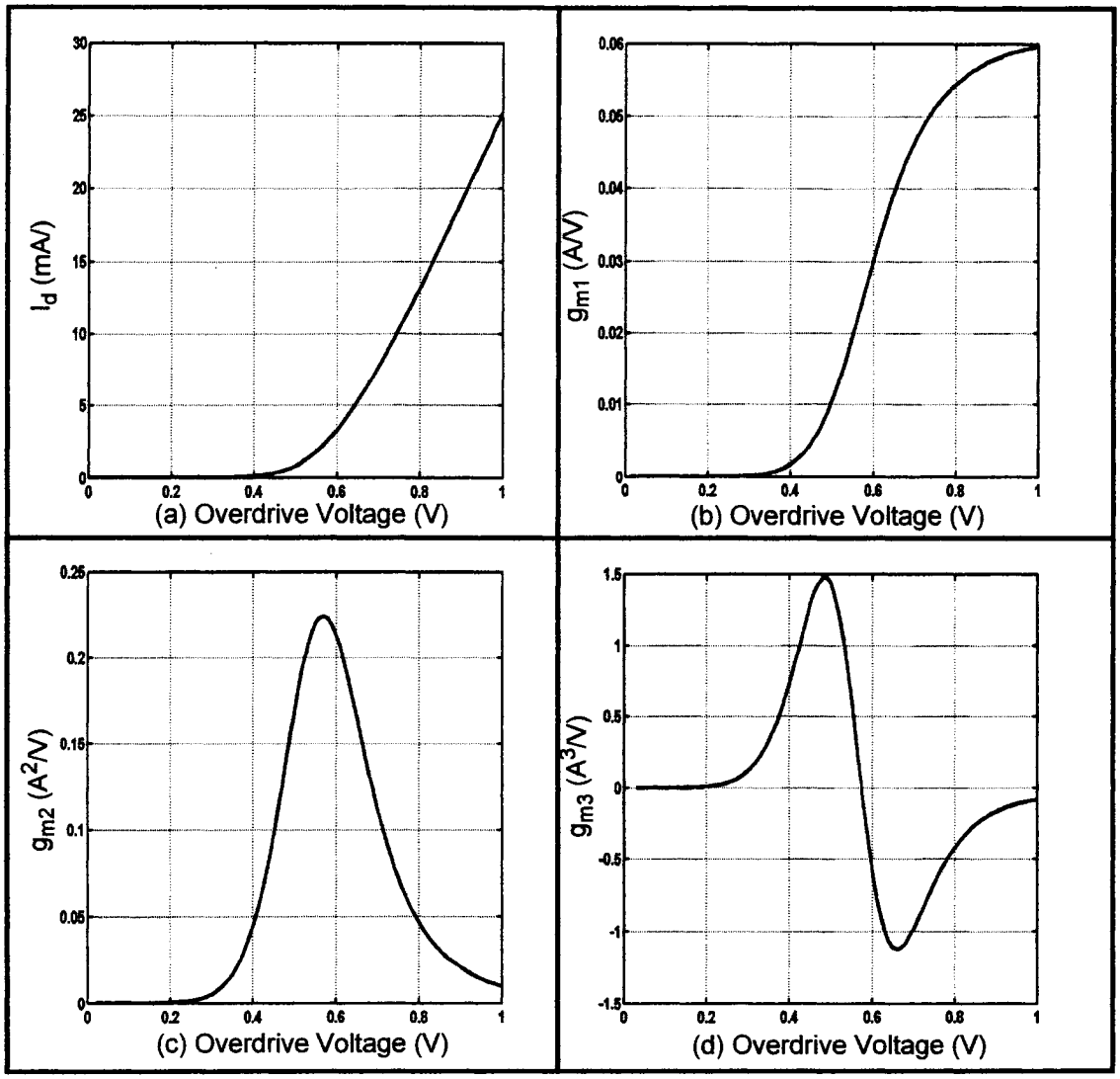

Figure 2.5 Characteristics of *(a)* i_d, *(b)* g_{m1}, (c) g_{m2}, and (d) g_{m3} vs. the overdrive voltage of a standard 100μm width CMOS 0.18μm gate length transistor [83].

channel RF CMOS LNAs. Design guidelines for decreasing distortion, along with closed-form expressions describing the second and third orders harmonic distortions are provided.

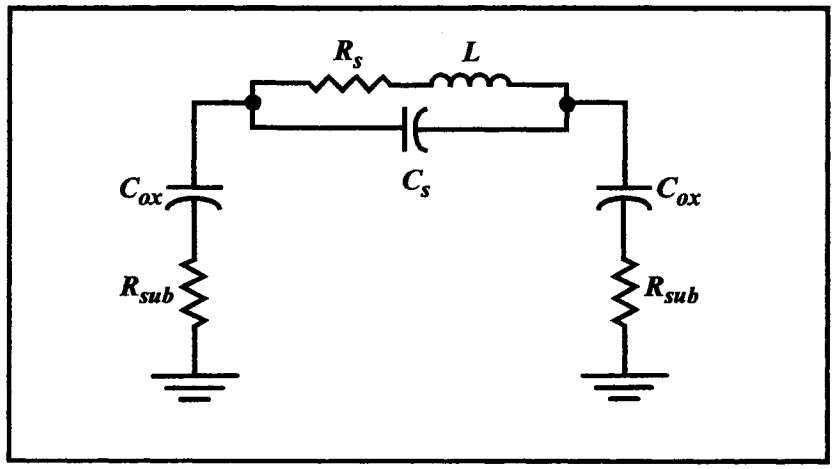

Figure 2.6 Onchip inductor model.

can be implemented using the top metal interconnect, in order to decrease substrate coupling effects. Circular spiral inductors are known to provide a better Q-factor, when compared to square or polygon structures. However, not all standard technologies support round interconnect structures. As a result, octagonal shapes, such as the one shown in Fig. 2.7, can be used.

To decrease the series resistance, the width of the metal lines of an inductor should be made as large as possible. However, a large metal width increases the area of the inductor for a given inductance value and, as a result, increases its parasitic capacitances. This in turns increases the substrate coupling effect and decreases the self-resonant frequency of the inductor. A typical optimum width of 20μm was measured for the standard CMOS 0.18μm process used by Tsang [90] and in this thesis. Traces connected to inductors are made wide to decrease their parasitic resistances. To isolate inductors from substrate noise, ground shielding can be added under the inductors. Finally, inductors in general create large magnetic fields. They should be placed as far as possible from each other, and from the rest of the layout, in order to avoid interference with nearby signals and circuits. A minimum distance of 30μm between the inductors and the rest of the circuit components was used throughout all layouts presented in this thesis.

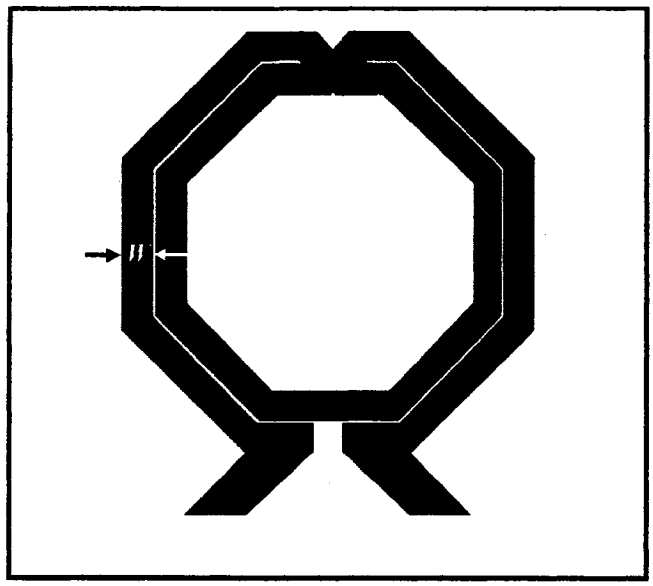

Figure 2.7 Octagonal shape inductor.

2.2.2 - On-Chip Q-Enhancement Techniques

For silicon-based RF circuits, the poor inductor Q-factor is mainly due to metal and substrate losses. For example, for a 1nH inductor at 5GHz, the inductor series resistance can be as large as 10-15Ω, which would result in a quality factor between Q = 5 to 6. This limits the performance of circuits employing on-chip inductors in general. Difficult Q-enhancement techniques are often used to overcome this shortcoming.

Simple layout optimization techniques for CMOS on-chip inductors were reported in [91] and [92]. The method explained in [91] consists of decoupling the inductor from the substrate by adding patterned ground shields to reduce substrate losses, as shown in Fig. 2.8-a. This technique enhances the Q-factor of the inductor at the cost of increasing the parasitic substrate capacitance. The latter has the effect of decreasing the inductor self-resonance frequency, and therefore is not suitable for multi-giga-Hertz RF circuits. In [92], symmetric dual layer spiral inductors, which were designed as a cascaded connection of two layer inductors, were reported. These inductors have the advantage of providing almost four times the inductance of a single layer inductor, while doubling the Q-factor for a given area. However, since lower metal layers are needed to implement the

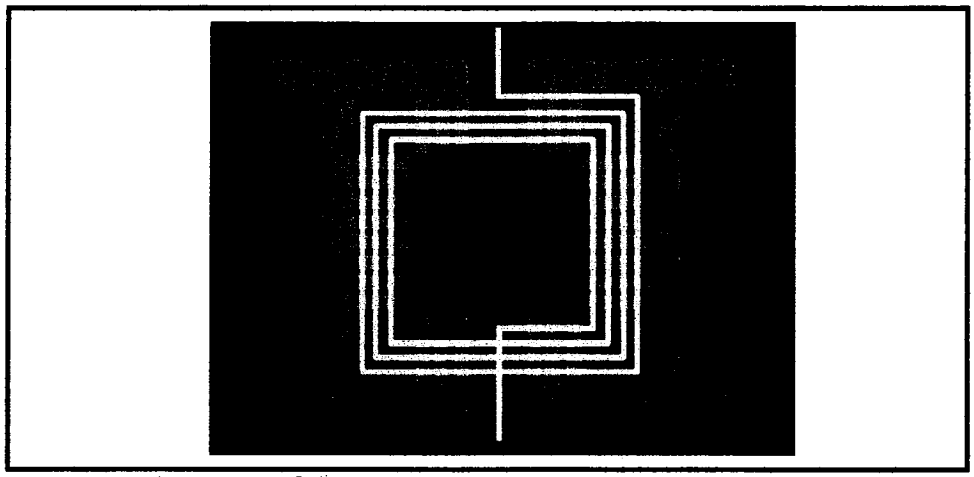

Figure 2.8 Example of Q-enhancement techniques: Decoupling the inductor from the substrate by adding patterned ground shields.

inductor, compared to the top layer-only inductors, substrate losses are also increased due to parasitic coupling.

Other Q-enhancement techniques exist, such as etching the substrate below the inductor to decrease substrate losses [93], or the use of thicker top metal for inductor implementation. These special fabrication techniques are expensive, which makes them not suitable for low-cost solutions. In differential designs, a 50% enhancement in the quality factor and a wider operating bandwidth can be obtained by differentially exciting the on-chip inductor [94].

A typical active approach to enhance the Q-factor of an on-chip inductor is to connect current-sourcing devices in parallel with the inductor, in order to produce a parallel negative resistance circuit (e.g. [15]). This concept is illustrated in Fig. 2.9-a. The on-chip inductor has a series resistance r_s which can be modeled by a parallel resistance R_{Loss}. To restore the energy lost in the tank due to this resistance, a compensation circuit is added in parallel with it. The input resistance R_{in} looking into the transconductance cell is negative and is given by

$$R_{in} = -1/g_m. \tag{2.18}$$

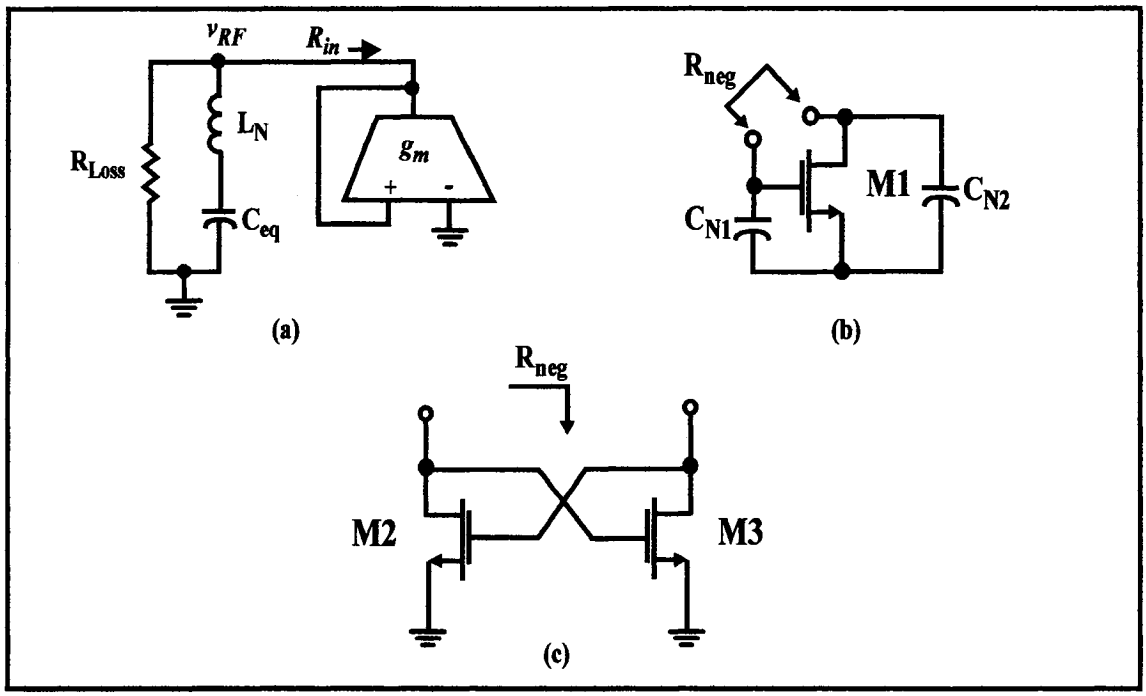

Figure 2.9 An approach for active Q-enhancement: the transconductor g_m will compensate for the energy lost in R_{Loss}. b) Negative resistance provided by capacitive feedbacks around transistor M1. c) Negative resistance provided by a cross-coupled pair.

A practical example of implementing such a negative resistance circuit is shown in Fig. 2.9-b [95]. It consists of a transistor with capacitive feedback between its gate and source and its drain and source, commonly used in single-ended voltage controlled oscillator designs. Analyzing the circuit in Fig. 2.9-b, R_{neg} is found to be

$$R_{neg} = -\frac{g_{m1}}{((2\pi f)^2 C_{N1} C_{N2})}, \tag{2.19}$$

where g_m is the transconductance of the transistor, and f is the operating frequency.

The cross-coupled pair shown in Fig. 2.9-c may also be used to generate a negative resistance. It consists of a cross-coupled amplifier, commonly used in differential voltage controlled oscillator designs. The negative resistance is approximately given by

$$R_{neg} = -\frac{2}{g_m} \quad . \tag{2.20}$$

2.3 - RF Layout Techniques

The layout of an RF circuit affects greatly its performance. Simple layout techniques, which are summarized in this section, can be adopted in order to achieve minimal amount of discrepancies between the expected performance and the actual one.

First of all, the layout should be designed in a uni-directional fashion, in order to limit the effect of crosstalk between the RF input and output signals. If a differential topology is used, a ground pad should be added between the differential input and differential output pads, to better isolate the signals. To filter substrate noise, ground shielding is a must around all transistors and capacitors (Fig. 2.10). DC traces should be made as thin as possible, such that they appear as high impedances for the RF signals. AC interconnect traces are made wide in order to decrease their series parasitic resistances. To limit RF signal substrate coupling, AC traces are implemented using the top two metal layers. Interconnection carrying RF signals should be made as short as possible, in order to reduce their parasitic capacitances.

Coupling capacitors between stages are widely used in RF front-end receivers. The value of these capacitors should be adequately selected, such that they provide low impedances for the RF signals, while blocking the DC biasing. Large coupling capacitors would produce higher substrate coupling, and are therefore not recommended for high frequency operation.

For designs housed in standard packages, which is the case for the circuits presented in this thesis, all of the grounds pads, including the pads connected to the probes for on-chip measurements, should be connected together. Moreover, many ground pins should be used in order to decrease the sensitivity of the circuits to ground inductances. RF pads are implemented using the top metal layer, while DC pads are made with all metal layers connected together with the maximum amount of vias. Finally, all DC pads are connected to large grounded-capacitors, in order to filter noise and interference in the DC interconnections.

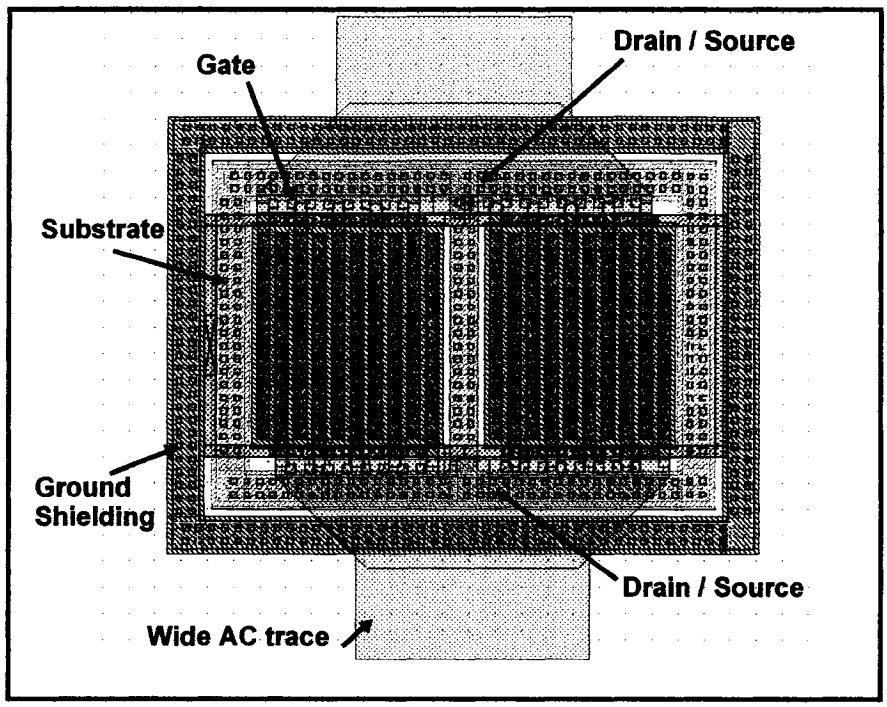

Figure 2.10 Transistor layout, with a 144μm width and 0.18μm gate length.

2.4 - LNA Topologies

The three LNA structures used in this thesis, namely the single transistor LNA, the cascode LNA, and the folded-cascode LNA are shown in Fig. 2.11. The cascode LNA was used to integrate the LNA-notch combination circuits, while the single transistor LNA and the folded cascode were used for distortion analysis. A differential folded-cascode LNA-notch filter was also investigated. Every structure has its own advantages and disadvantages. The single transistor structure allows low-voltage operation. However, due to the gate to drain parasitic capacitance of the MOSFET transistor, and due to the Miller effect, a low impedance appears at high frequencies between the gate (the input node) and the drain (the output node) of the transistor. As a result, the single-transistor LNA provides poor isolation between its input and output ports, which makes it prone to instability.

Cascode amplifiers require a relatively higher voltage headroom, compared to

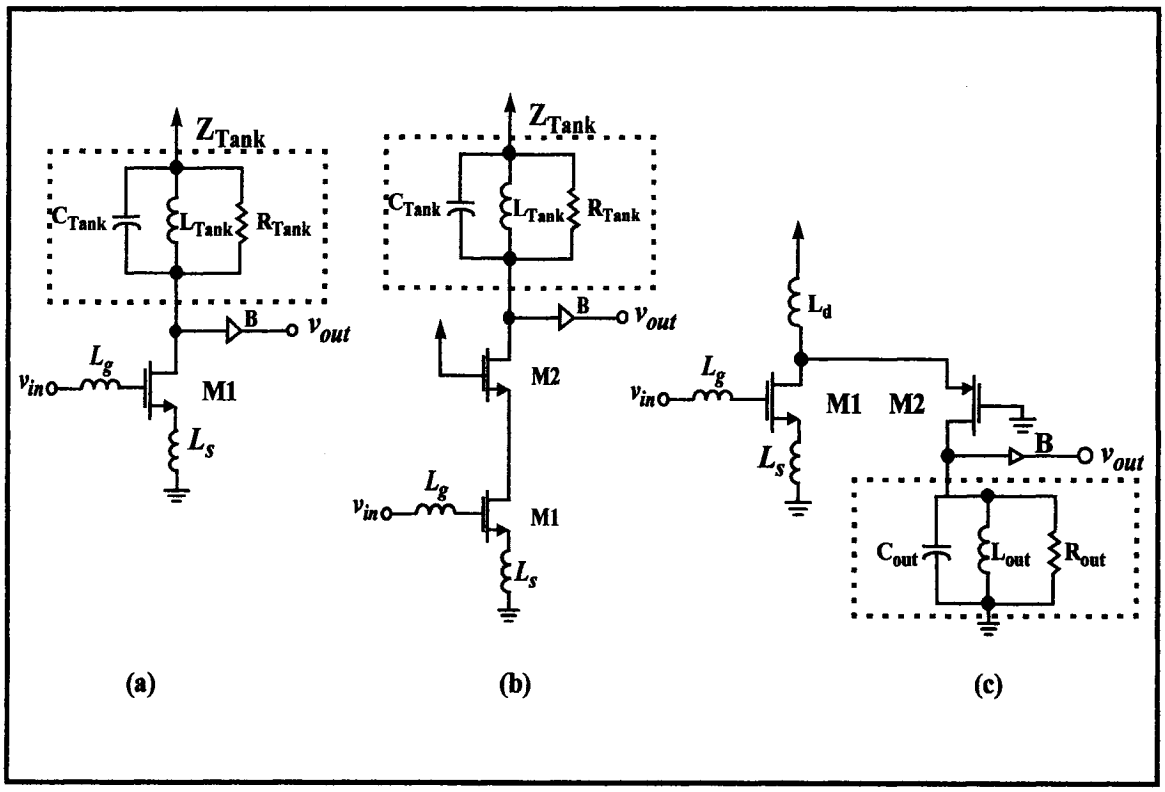

Figure 2.11 a) Common source LNA. b) Cascode LNA. c) Folded-cascode LNA [96].

single-transistor LNAs, since they involve stacking two transistors. However, the higher isolation they provide between the input and output ports make them less prone to instability. Moreover, as the feature sizes of CMOS technologies downscales, this topology can operate at relatively low-voltages.

The folded cascode amplifier can operate with power supplies lower than 1V since only one transistor is stacked between ground and the supply voltage [96]. Transistor M1 transforms the input voltage signal into a current signal. Inductor L_d is a relatively large inductor: it behaves as an RF choke to block the AC current signal in the frequency band of interest. As a result, the AC current generated from transistor M1 is almost totally transferred to transistor M2.

In most wireless systems, the LNA is preceded by an off chip filter and/or by an RF antenna. These blocks are typically designed with a 50Ω output impedance. Therefore, to maximize the power transfer between them and the LNA, input matching

becomes critical. Hence, matching inductors L_g and L_s were added Fig. 2.11. Inductor L_s provides source degeneration, and is needed to match the real part of the characteristic input impedance (typically 50 Ω). Inductor L_g is added to cancel the reactance effect of the parasitic gate to source capacitance of transistor M1. The small-signal equivalent circuit of the input transistor of the LNAs is shown in Fig. 2.12. Note that, in the cascode and folded-cascode amplifiers, C_{gd} does not affect much the behavior of the LNA, since there are no Miller effects. Analyzing the circuit shown in Fig. 2.12, the following set of equations are obtained

$$i_{in} = sC_{gs1}v_{gs1}, \tag{2.21}$$

$$v_s = v_{in} - L_g i_{in} - v_{gs1}. \tag{2.22}$$

Neglecting the channel modulation effect, and performing KCL at node 1, results in

$$i_{in} = \frac{v_s}{L_s} - g_{m1}v_{gs1}. \tag{2.23}$$

Rewriting Eqs (2.21)-(2.23), the input impedance Z_{in} of the LNA is found to be

$$Z_{in} \equiv \frac{v_{in}}{i_{in}} = s(L_g + L_s) + \frac{1}{sC_{gs1}} + \frac{g_{m1}L_s}{C_{gs1}}. \tag{2.24}$$

At resonance, the input impedance is real and is given by $Z_{in} = g_{m1}L_s/C_{gs1}$. In the above analysis, the series resistances of the on-chip inductors were neglected. In reality, as explained in previous sections, on-chip inductors have a relatively large series resistances, especially at high-frequencies. Including these resistances and re-analyzing the circuit in Fig. 2.12 results in an input impedance given by

$$Z_{in} = s(L_g + L_s) + R_g + R_s + \frac{1}{sC_{gs1}}(1 + g_{m1}R_s) + \frac{g_{m1}L_s}{C_{gs1}}, \tag{2.25}$$

where R_g and R_s are the series parasitic resistances of the L_g and L_s inductors, respectively. Adding these resistances complicates the input matching task, since their values depend on the layout and on process parameters.

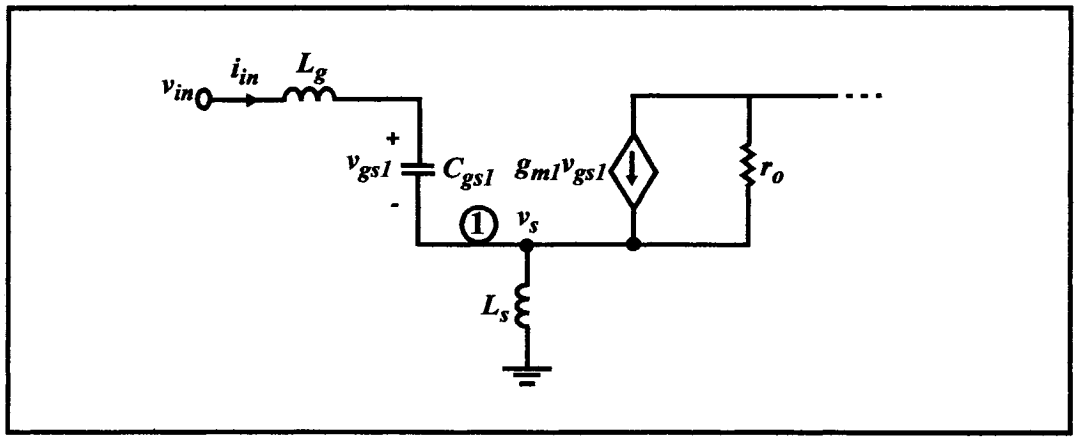

Figure 2.12 Small signal equivalent model of the input stage of an LNA.

The output buffer stages, represented by "B" in Fig. 2.11, are added for measuring purposes: They were designed to match the input impedance of the test equipment (typically 50Ω). For the cascode amplifier, a class A cascode output stage was used (Fig. 2.13-a). Capacitor C is a coupling capacitor. Resistance R_c is a large resistor used to block the AC signal from leaking to the biasing circuit of the output stage. The cascode structure was preferred to the single-transistor common-source structure (Fig. 2.13-b) in order to better isolate the LNA's tank from the test equipment.

On the other hand, the folded cascode LNA was integrated with a common drain output buffer, implemented with a PMOS transistor and a 50Ω resistance (Fig. 2.13-b). In this case, since the folded-cascode LNA targeted very low-voltage operation, a cascode structure was not an option. When the LNA is connected to a mixer in a heterodyne receiver, these output buffers become redundant. They are employed to characterize and test all prototype chips presented in this thesis.

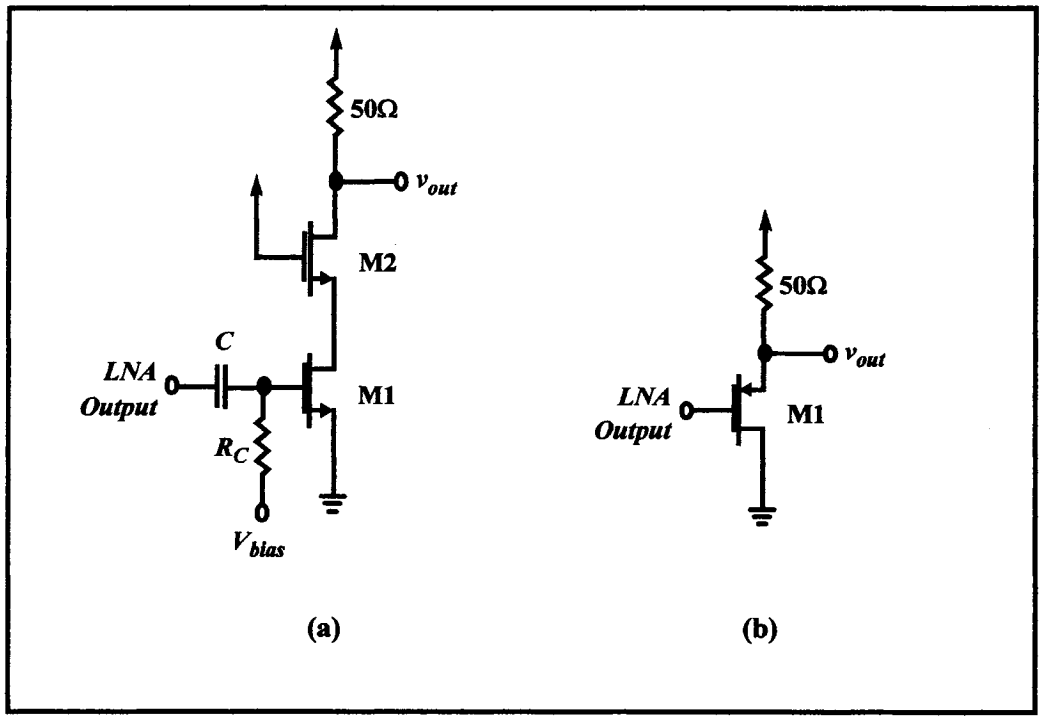

Figure 2.13 a) Cascode output buffer used here. b) Common drain output buffer used here.

Chapter 3 - Robust RF CMOS Image Reject Filters

3.1 - Introduction

Research has been conducted on using active notch filters to suppress the signal at the image frequency in heterodyne receivers (e.g. [59]-[64]). The highest frequency of a CMOS notch filter reported to date is at 4.2GHz ([18],[63]), and the highest image rejection obtained was 50dB at 2.2GHz [60].

The specifications of 5GHz RF receivers for the 802.11a WLAN applications are summarized in Table 3.1. A minimum of 30dB of image rejection is required, while the maximum noise figure and minimum receiver sensitivity are 10dB and -65dBm, respectively. Different RF receiver architectures that could meet these requirements have been introduced in the literature and are discussed in Appendix A. In summary, the receiver has three main tasks:

1- It provides sufficient amplification for the incoming signal, such that the signal acquires sufficient gain before passing through the analog to digital converter for further digital processing.

2- It demodulates the signal in order to retrieve the transmitted information.

3- It suppresses the undesired noise and distortion as much as possible.

Frequency range	**5.18-5.32 GHz** **5.745-5.805 GHz**
Modulation	**64 QAM**
Noise Figure (NF)	**10 dB**
Sensitivity	**-65 dBm**
Image rejection	**30 dB**

Table 3.1: IEEE 802.11a WLAN receiver specifications.

Receivers can be divided into two main categories: homodyne receivers and heterodyne receivers. In homodyne receivers, the signal is downconverted directly to DC. In heterodyne structures, the signal is first translated to an intermediate frequency, before being translating to baseband.

This chapter begins with an introduction of heterodyne receivers, followed by a discussion of the image problem. An elegant multi-GHz notch filter, which uses a negative resistance to compensate for the on-chip inductor losses, was proposed by Macedo et al. [15]. When integrated in a CMOS technology, its overall performance is limited by many factors, which will be discussed in details in Section 3.3. A proposed novel notch circuit capable of mitigating these limitations is presented in Section 3.4. Experimental results and discussions are summarized in Section 3.5. Section 3.6 proposes an architecture that extends the bandwidth of image rejection and eliminates the need for automatic tuning.

3.2 - Heterodyne Structures

Shown in Fig. 3.1-a, the heterodyne receiver translates the RF signal to baseband by employing multiple downconversions. The signal is first translated to a first intermediate frequency (IF) at $f_{in} - f_{lo1}$. The signal is then transferred to baseband by a second downconversion. Every downconversion is preceded by image filtering.

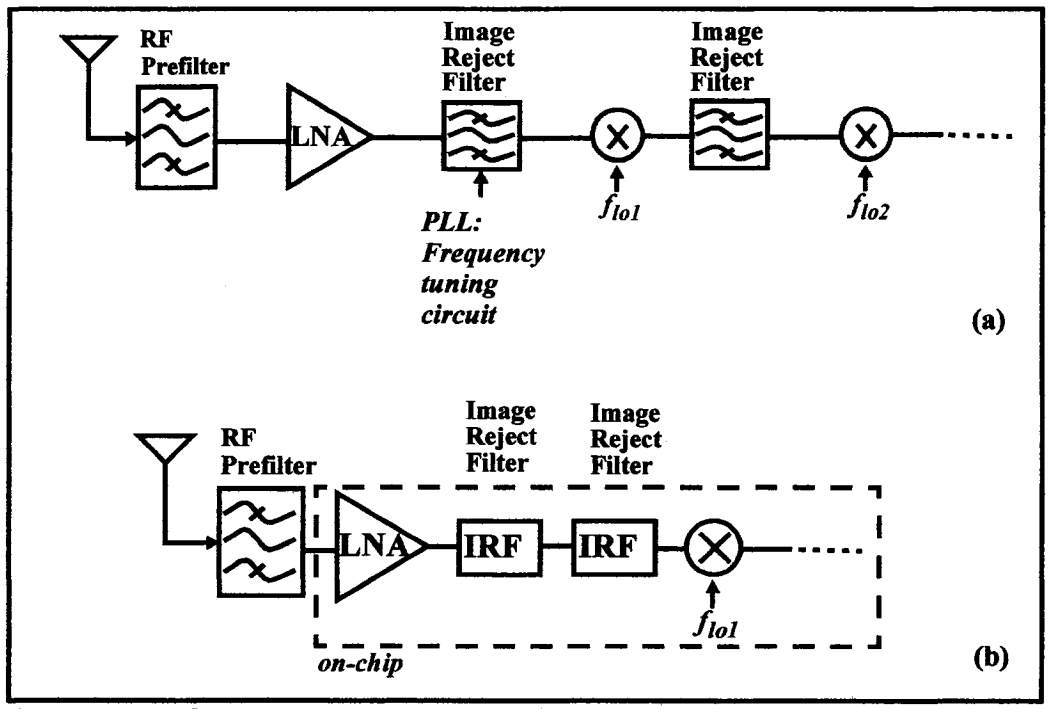

Figure 3.1 a) Structure of traditional IRF-based receiver front-ends. b) Structure of the proposed double notch IRF-based receiver architecture

The heterodyne structure is known to be the most reliable structure in RF receivers. The sensitivity and the selectivity it offers have made it the dominant choice for RF receivers. However, for fully integrated designs, on-chip image reject filters with automatic frequency tuning, i.e. with a PLL, are needed (Fig. 3.1-a). Employing a PLL system for tuning the frequency of the image reject filter involves integrating a frequency divider, a phase detector, a charge pump, and a VCO.

The RF front-end receiver architecture proposed in this thesis is shown in Fig. 3.1-b. It does not employ a PLL system for IR tuning. Instead, it consists of cascading two notches after the LNA, with their image reject frequencies slightly offsetted. As a result, a wide image rejection bandwidth can be obtained, without the need for extra notch tuning circuits. Thus, the cost, the complexity, and the power consumption of the front-end receiver can be reduced.

3.2.1 - The Image Problem

Consider the simplified front-end receiver shown in Fig. 3.2-a. Right after the antenna, the bandpass filter selects the desired frequency band. Usually, the signal at the antenna has a very small amplitude, which explains the need of amplifying it before any further processing. This task is performed by the LNA.

The operation of the mixer can be viewed as a simple analog multiplier, i.e. the incoming RF signal is multiplied by a $\cos(2\pi f_{LO}t)$ signal. At the output of the mixer, the signal has two frequency components: one at $f_{LO}-f_{RF}$, referred to the intermediate frequency (f_{IF}), and the other one at $f_{LO}+f_{RF}$. If the antenna picks up a strong interferer at the frequency $f_{LO}+f_{IF}$, this signal, referred to the image signal, is going to get partially amplified by the LNA, and appears at the output of the LNA, as shown in Fig. 3.2-b. The image signal gets modulated by the mixer, and is translated to the $f_{LO}-f_{RF}$ frequency, i.e. it appears in the same IF frequency band as the downconverted RF signal, corrupting the desired channel. Note that, since the power of the image signal can not be determined beforehand, it may be strong enough to seriously damage the desired channel. The image signal can be in the form of noise or simply a strong interferer.

The image rejection ratio (IRR) is typically used to characterize the amount of image suppression a receiver (or a filter) provides with respect to the desired signal. It is expressed as

$$IRR = 10\log\frac{P_{out-IM}}{P_{out-Si}} - 10\log\frac{P_{in-IM}}{P_{in-Si}}, \tag{3.1}$$

where P_{out-IM} and P_{out-Si} are the output powers of the image and of the desired signals, respectively, and P_{in-IM} and P_{in-Si} represent the powers of the input signals.

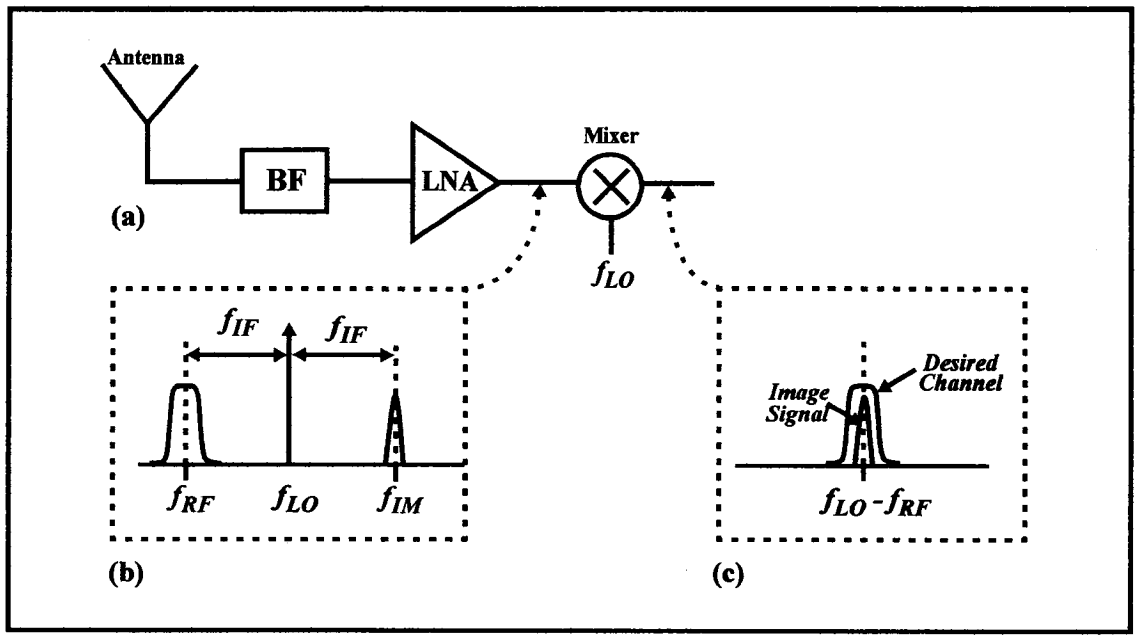

Figure 3.2 The image problem. a) A simplified structure of a front-end receiver. b) The RF and the image signals. c) The downconverted signals at the intermediate frequency.

Traditionally, a high-Q image-reject filter is placed before the mixer. Off-chip image reject filters are typically used. SAW filters, with 50Ω input impedances, are the most common choice for this application. Unfortunately, off chip filters introduce many restrictions on the overall receiver design. In such a scenario, the output impedance of the LNA and the input impedance of the mixer must be matched to 50Ω, in order to maximize power transfer. At 5GHz, this matching procedure is hard to realize, since the slightest parasitic would considerably affect it. This added complexity comes with an added cost as well, which is not desirable in wireless consumers products. Fully integrated solutions are therefore needed.

3.2.2 - Image Reject Filters

Consider the LC network shown in Fig. 3.3-a. At resonance, i.e. when the negative impedance of the capacitor equates in amplitude that of the inductor, a low impedance path is created from the input RF signal node to ground, thus shunting the RF signal at a

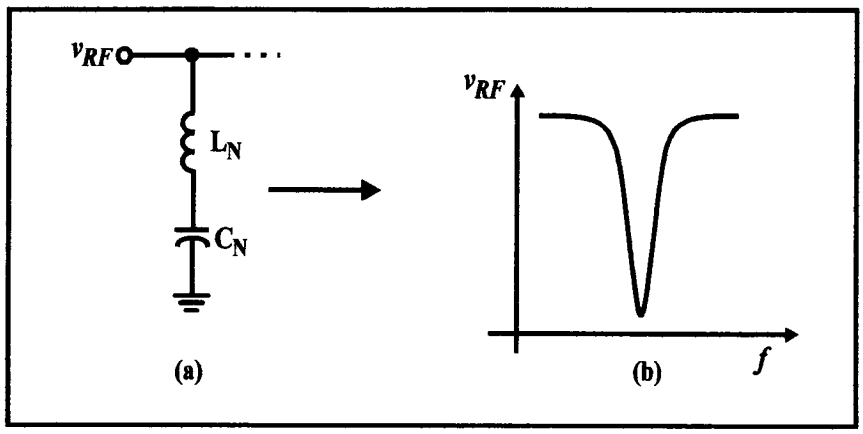

Figure 3.3 a) Notch filter, and b) its transfer function.

specific frequency. The transfer function of this tank is shown in Fig. 3.3-b, with the notch resonant frequency given by

$$f_N = \frac{1}{2\pi\sqrt{L_N C_N}}. \tag{1}$$

Assuming ideal devices, the quality factor of the LC tank would be infinite, resulting in an infinite notch depth. In reality, the series parasitic resistances of the devices dramatically affect the tank's quality factor. For silicon-based RF circuits, the poor inductor Q-factor is dominant. This would limit the notch filter's depth to a few dBs, and does not allow sufficient image rejection. To obtain acceptable image rejection, on-chip Q-enhancement techniques, such as the ones suggested in Section 2.2.2, are therefore needed.

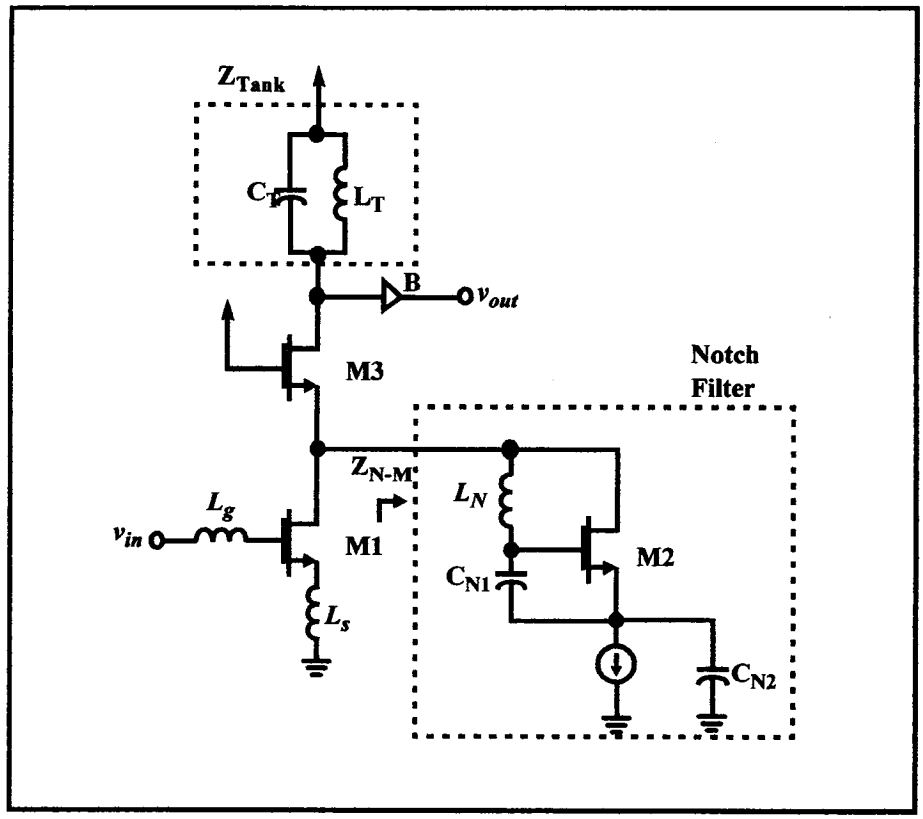

Figure 3.4 Schematic of the CMOS equivalent circuit for the LNA and notch filter proposed by Macedo et al. [15].

3.3 - Macedo's Notch Filter and its Limitations When Implemented in a CMOS Technology

An image reject filter which uses the negative resistance concept was reported by Macedo et al. [15]. The circuit was integrated and demonstrated in a 0.5μm bipolar technology. When mapped to a CMOS technology, it results in the circuit shown in Fig. 3.4. Its operation can be summarized as follows:

i-Transistors M1 and M3 form a cascode low noise amplifier with an overall gain set by the L_TC_T resonant tank, and by the sizes and biasing currents of the transistors. A cascode amplifier stage was chosen to isolate the input port from the output one, which improves stability. By modifying the DC voltage at the gate of M1, i.e. by varying the biasing current, gain controllability can be achieved.

ii-Within the frequency band of the L_TC_T resonant tank, the impedance $Z_{N\text{-}M}$ looking into the notch filter is relatively large. Thus, the overall circuit operates like a regular LNA with L_s as inductor degeneration.

iii-Capacitors C_{N1} and C_{N2}, along with inductor L_N, implement the notch filter. Their sizes were chosen such that the combination of C_{N1}/C_{N2} and inductor L_N set the notch frequency. When the absolute values of the reactances of capacitors C_{N1} and C_{N2} equal the reactance of inductor L_N, a low impedance connection to ground is created. This results in shunting the AC signal to ground, and therefore obtaining a notch response at this frequency. Transistor M2 provides the negative resistance that compensates for the losses of inductor L_N.

Inductor L_s provides source degeneration. It also matches the real part of the characteristic input impedance (typically 50Ω). Inductor L_g cancels the reactance effect of the parasitic gate to source capacitance C_{gs} of transistor M1.

The first limitation that was identified in the circuit of Fig. 3.4 was related to the fact that the DC current of the notch circuit affects the DC biasing of the LNA. Transistor M2 obtains its current through transistor M3. The depth of the notch is controlled by varying the biasing current of transistor M2. By varying the biasing of M2, the biasing of M3 is also altered. Due to the strong channel length modulation effect in modern submicron CMOS technologies (λ can be as large as 0.4 in a CMOS 0.18μm standard technology), the response of the LNA is therefore affected, when tuning the notch depth. Preferably, the DC current of the notch filter should be independent from that of the LNA.

A small-signal analysis was performed to derive the input impedance $Z_{N\text{-}M}$ of the notch circuit in Fig. 3.4. The equivalent-circuit is shown in Fig. 3.5. For simplicity, the dynamic elements are ignored (i.e. the output transconductance and the parasitic drain to source capacitor). Only the parasitic series resistance r_s of the inductor is considered. The gate to source parasitic capacitor of transistor M2 is included in the value of C_{N1}. Since

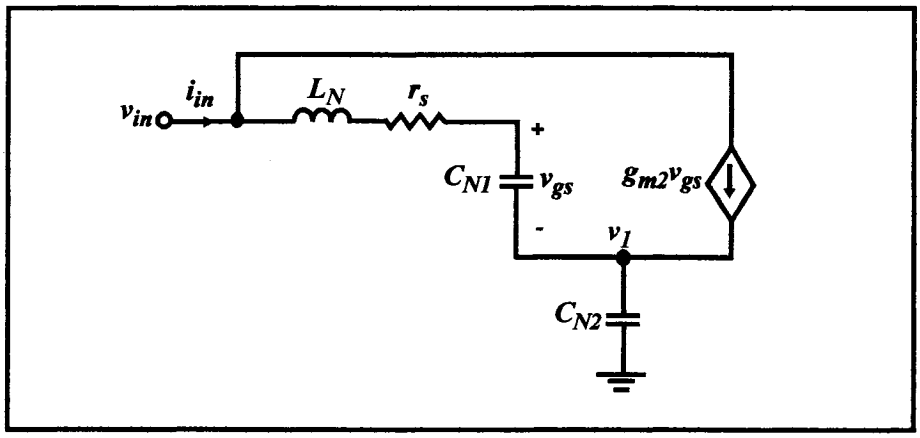

Figure 3.5 Small-signal model of the notch filter in [15].

capacitors C_{N1} and C_{N2} are at least an order of magnitude larger than the parasitic drain to bulk (C_{db}), source to bulk (C_{sb}), and the gate to drain (C_{gd}) capacitors, C_{db}, C_{sb}, and C_{gd} were not included in the following analysis. The input impedance of the notch filter is obtained by solving for $Z_{N-M} = v_{in}/i_{in}$. The real and imaginary parts of the input impedance are then derived. The real part gives the resistance that needs to be compensated for. The imaginary part of $Z_{N\text{-}M}$ sets the frequency of the notch. Analyzing the small-signal equivalent circuit shown in Fig. 3.5, we get

$$i_{in} = sC_{N1}v_{gs} + g_{m2}v_{gs}, \tag{3.2}$$

$$v_1 = \frac{i_{in}}{sC_{N2}}, \tag{3.3}$$

and

$$v_{in} = v_{gs} + v_1 + (L_N + r_s)sC_{N1}v_{gs}, \tag{3.4}$$

where g_{m2} is the transconductance of transistor M2, and v_{gs} is its gate to source voltage. Solving the above set of equations, the real and imaginary parts of $Z_{N\text{-}M}$ are found to be

$$Re\{Z_{N-M}\} = \left(r_s + \frac{g_{m2}}{(2\pi f)^2 C_{N1}^2} - \frac{L_s g_{m2}}{C_{N1}}\right)\frac{1}{(1 + g_{m2}^2/(2\pi f)^2 C_{N1}^2)}, \tag{3.5}$$

and

$$Im\{Z_{N-M}\} = -\left(\frac{(C_{N1}+C_{N2})}{2\pi f C_{N1}C_{N2}} + \frac{g_{m2}^2}{(2\pi f)^3 C_{N1}^2 C_{N2}} - 2\pi f L_N - r_s \frac{g_{m2}}{(2\pi f)^2 C_{N1}^2}\right) \times \frac{1}{(1+g_{m2}^2/(2\pi f)^2 C_{N1}^2)} \quad . \quad (3.6)$$

From equation (3.5), the negative resistance is given by $\frac{L_s g_{m2}}{C_{N1}}$. In order to obtain an infinite notch depth, this negative resistance needs to compensate not only for r_s, but also for the $\frac{g_{m2}}{(2\pi f)^2 C_{N1}^2}$ term. This results in higher power consumption than necessary. Compensation is further complicated due to the dependence of this additional resistive term on g_{m2}. Moreover, equation (3.6) suggests that the frequency of the notch does not depend only on C_{N1}, C_{N2}, and L_N. It also depends on r_s and g_{m2} [1]. The dependency on r_s introduces an undesirable additional design constraint. The dependency on g_{m2} is rather detrimental. As g_{m2} is varied to control the depth of the image rejection, the notch frequency will shift! This makes the design and control of such a circuit very difficult. As discussed in the following section, the circuit proposed here does not suffer from any of the limitations above.

1. For the notch circuit proposed here (Section 3.4), the negative resistance needs only to compensate for r_s, simplifying the control of the circuit and minimizing power consumption.

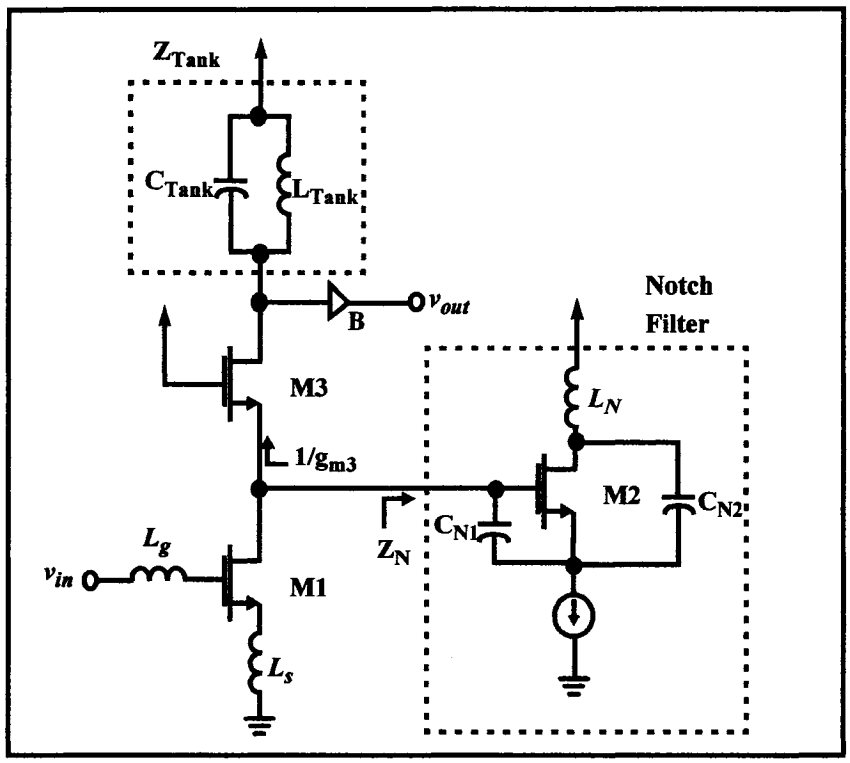

Figure 3.6 Schematic of the LNA and proposed notch filter.

3.4 - Proposed LNA- Notch Circuit and Design Equations

Fig. 3.6 shows the new notch filter circuit, connected to a cascode LNA. Similar to the circuit in Fig. 3.4, the impedance Z_N looking into the gate of M2 is larger than $1/g_{m3}$ at the midband frequency of the LNA, thus not affecting its operation in this frequency band. At the resonant frequency of the notch circuit, Z_N is low and the RF current is steered away from transistor M3, resulting in signal attenuation at the output. Transistor M2 compensates for the losses in the *LC*-tank of the notch circuit. It should be noted that the biasing of the notch filter is not obtained through transistor M3, and thus it does not affect the LNA DC biasing.

The sizes of transistors M1 and M3 were carefully chosen to provide more than 15dB of gain at the center frequency of the LNA, while minimizing the noise figure. Transistor M1 was chosen to be relatively large. Large transistors have the advantage of pro-

viding high transconductances at relatively small biasing currents, and therefore achieving the desired gain with minimum power consumption. Also, since this results in a larger C_{gs}, a smaller inductor for the input matching circuit can be used. On the other hand, using a large transistor results in higher substrate coupling and parasitic losses. Transistor M1 is 200μm/0.18μm, while the size of transistor M2 was chosen to be 50μm/0.18μm. A cascode common-source amplifier with a 50Ω load resistance was used to implement the buffer for output matching measurement purposes.

3.4.1 - The Notch Filter

The notch circuit is highlighted in Fig. 3.6. At the desired resonance frequency of the filter, impedance Z_N can be set to be much smaller than $1/g_{m3}$. The smaller Z_N is, the higher the RF signal suppression will be. Analyzing the small-signal equivalent circuit of the notch filter (Fig. 3.7), the following equations are obtained

$$i_{in} = sC_{N1}v_{gs}\,, \tag{3.7}$$

$$v_1 = (sL_N + r_s)i_{in}\,, \tag{3.8}$$

$$v_{CN2} = \frac{i_{in} + g_{m2}v_{gs}}{sC_{N2}}\,, \tag{3.9}$$

and

$$v_{in} = v_{gs} + v_{CN2} + v_1\,. \tag{3.10}$$

Solving the above set of equations, the real and imaginary parts of Z_N were found to be

$$Re\{Z_N\} = -\frac{g_{m2}}{(2\pi f)^2 C_{N1}C_{N2}} + r_s\,, \tag{3.11}$$

$$Im\{Z_N\} = -\frac{(C_{N1} + C_{N2})}{2\pi f C_{N1}C_{N2}} + 2\pi f L_N\,. \tag{3.12}$$

Comparing equations (3.11) and (3.12) to equations (3.5) and (3.6), we note the following:

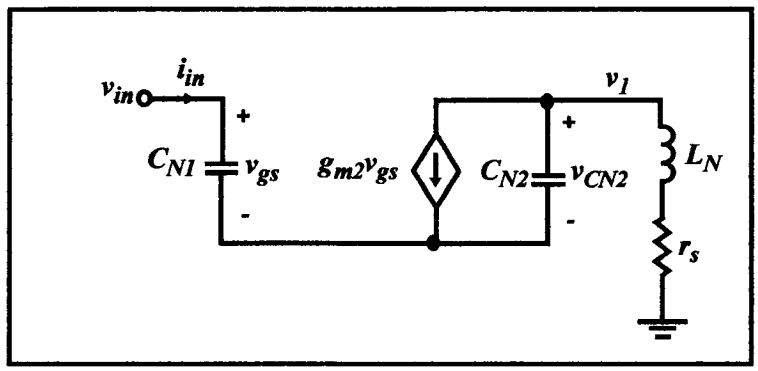

Figure 3.7 Small-signal model of the proposed notch filter.

1- Both circuits generate similar impedances. The circuit in [15] offers a smaller real impedance by a factor of $\frac{1}{(1+g_{m2}^2/(2\pi f)^2 C_{N1}^2)}$, which may result in an enhanced image rejection. However, the same way this factor decreases the impedance of $Z_{M\text{-}N}$ at the resonant frequency of the notch, it also decreases it around the LNA midband range, resulting in a decrease of the LNA gain.

2- Equation (3.11) suggests that the proposed circuit generates a negative resistance given by $R_{neg} = -\frac{g_{m2}}{(2\pi f)^2 C_{N1} C_{N2}}$, which needs to compensate *only* for the inductor ohmic loss (r_s), which is not the case for the circuit in Fig. 3.4.

3- From equation (3.12), the frequency of the notch is given by:

$$f_N = \frac{1}{2\pi}\sqrt{\frac{C_{N1}+C_{N2}}{L_N C_{N1} C_{N2}}} \quad , \tag{3.13}$$

which is independent of g_m and r_s, as opposed to the case of the circuit in Fig. 3.4.

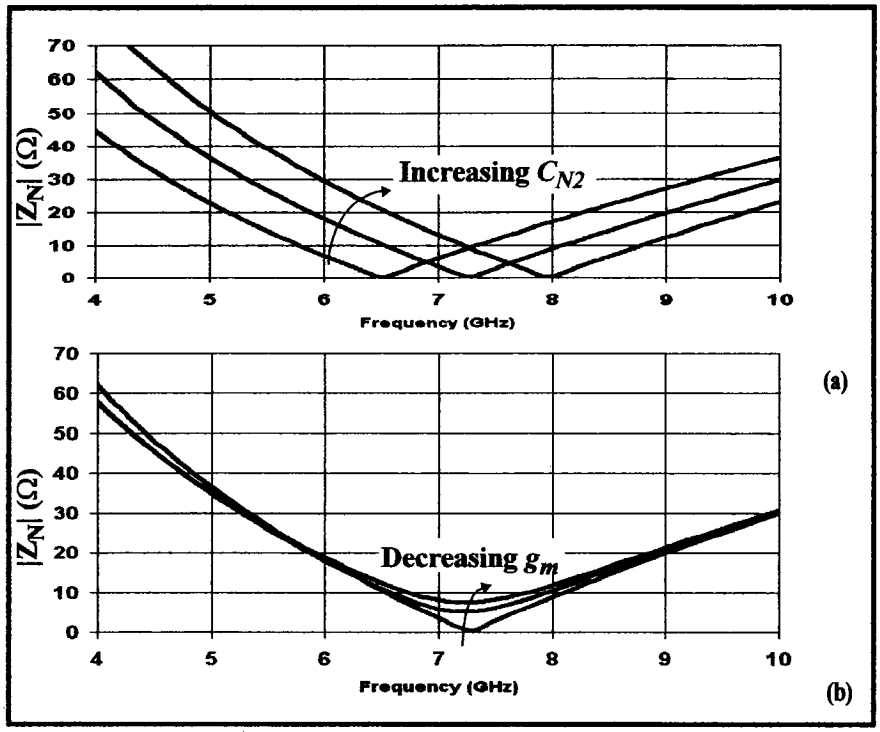

Figure 3.8 Tuning of the magnitude of Z_N by varying (a) C_{N2}, and b) g_m.

The magnitude of Z_N (Eq. 3.11-3.12) is plotted versus frequency in Fig. 3.8. As demonstrated in the figure, by varying capacitor C_{N2} (e.g. using a varactor), the frequency of the minimum input impedance would vary, thus tuning the frequency of the notch (f_N). Keeping the notching frequency constant, while varying the transconductance of transistor M2 (e.g. by varying its bias current), results in controlling the input impedance, thus tuning the depth of the filter's notch (Fig. 3.8.b).

3.4.2 - Stability of the Notch Filter

Since capacitor C_{N2} in Fig. 3.6 implements positive feedback, ensuring stability under all biasing conditions is of prime importance. Stability was first verified by deriving the transfer function of the overall LNA-notch circuit, including the input matching inductors L_s and L_g, in order to obtain the positions of the poles and zeroes[1]. First, the LNA gain was fixed and set to 15dB. Under this biasing condition, two of the poles were real and negative. The other two poles were complex conjugates, and a locus plot is shown Fig. 3.9-a. The transconductance of transistor M2 was varied from 0 to 100mA/V, i.e. with the negative resistance value tuned from 0 to -75Ω. This is much larger than the maximum negative resistance needed to theoretically achieve an infinite-Q notch. As expected, by keeping the LNA biasing constant while increasing the biasing of the notch filter, the complex poles move towards the right-half plane. The poles locations for two important transconductance values are highlighted in the figure, namely the transconductance needed to generate an infinite-Q notch, and the one which makes the circuit reach instability. It is interesting to note that the g_{m2} needed for ideal compensation is almost 5 times smaller than the one at which the complex conjugate poles reach the right-half plane, i.e. before the system reaches instability. This fact proves that the proposed circuit can, in theory, generate an infinite notch depth, while remaining stable. Moreover, if the notch bias is even increased above that point, the circuit still provides a large safe margin before instability occurs. In modern submicron CMOS technologies, the transconductances of the transistors increase with increasing the gate to source voltages, then reach a maximum value, before starting to decrease. Therefore, one can choose the size of the transistor that provides the necessary g_m for an infinite notch depth, while ensuring that this size never provides the transconductance value which would make the system reach instability. As a result, the filter can be designed to be always stable.

1. A complete analysis is summarized in Appendix B.

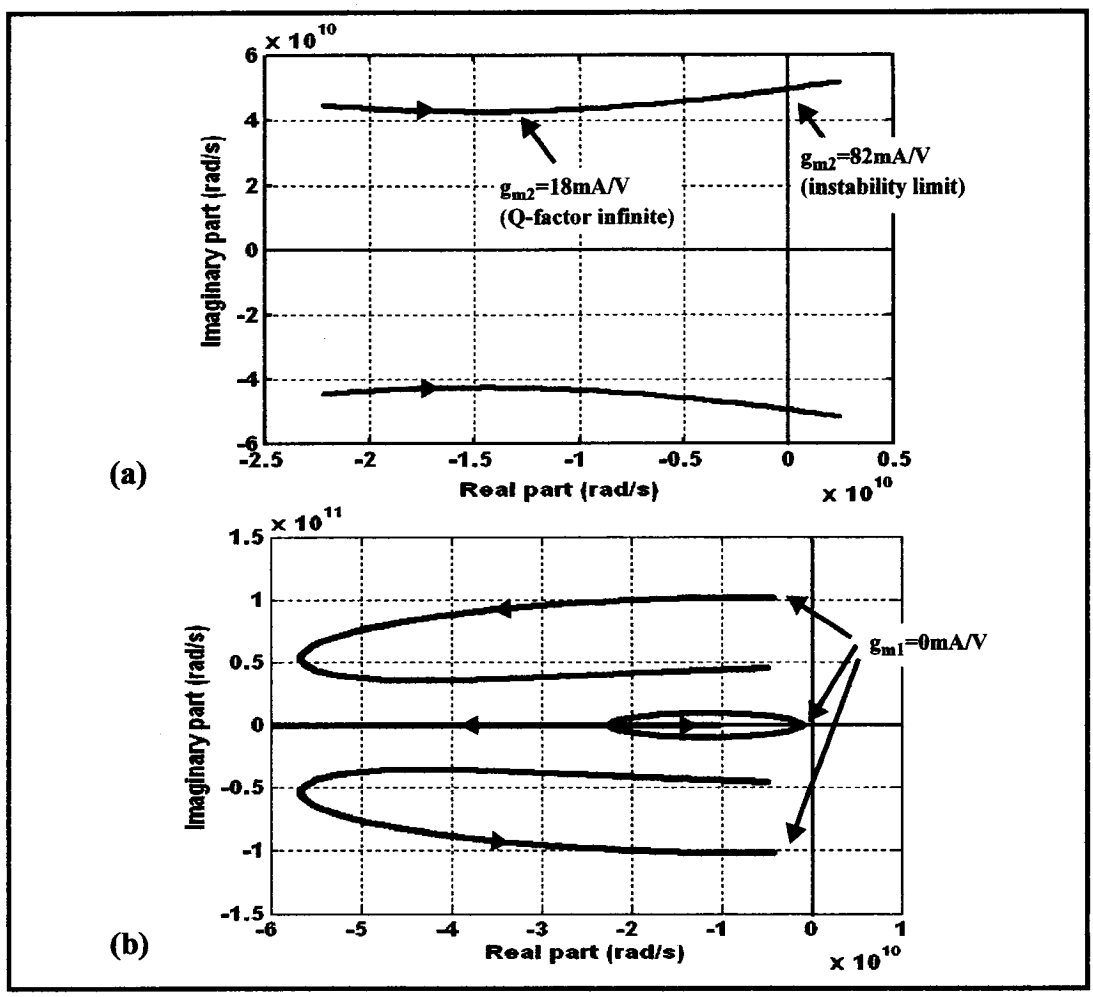

Figure 3.9 Locations of the poles of the LNA-notch circuit. Locus of the poles when tuning the biasing current of a) the notch filter (M2), and b) of the LNA (M1).

The biasing of the LNA (transistor M1) was then varied, with the notch depth fixed to more than -50dB. As demonstrated in Fig. 3.9-b, the poles remained in the left-hand plane under all LNA biasing conditions.

A simpler and maybe more practical approach for verifying stability, which yields the same results as above, while providing more insight, was considered as well. It consists of modelling the notch filter as shown in Fig. 3.10, where R_{gm3} is the source resistance of transistor M3, R_{Loss} is the equivalent parallel parasitic resistance of the L_N, C_{N1},

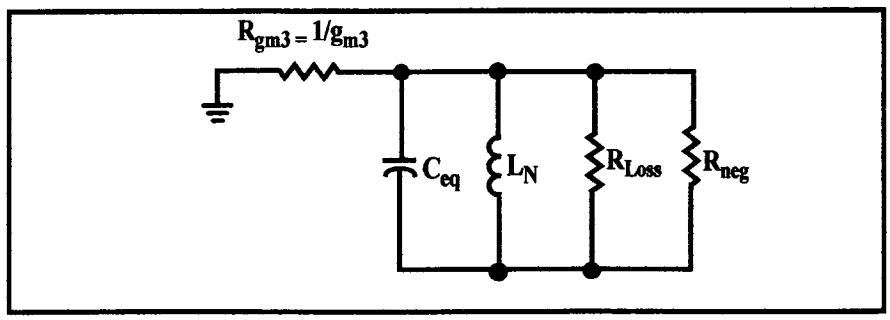

Figure 3.10 A simple model of the proposed notch filter, used to study stability.

and C_{N2} resonant tank, and R_{neg} is the negative resistance generated by the transistor. One can argue that R_{neg} can be equal in magnitude, or even larger than R_{Loss} without compromising stability, since R_{gm3} provides sufficient damping to the system. This means that an infinite-Q notch can be practically obtained, without compromising stability.

3.5 - Experimental Results

A prototype chip was implemented using a 0.18μm gate length CMOS process, and was housed in a standard CFP24 package. Ground and DC signals are connected to the package through regular bonding wires, while on-chip probing is used for the RF input and output signals.

S-parameters were measured using a 20GHz Agilent 8720ES vector network analyzer. Figure 3.11 shows the transfer function of the LNA plus one image reject filter. A 15.8dB LNA gain is obtained at 5.8GHz, and up to 62dB of *stable* image rejection at 7.3GHz is demonstrated. The corresponding measured input and output reflection coefficients, S11 and S22 (Fig. 3.12), are -6.5dB and -13.5dB at 5.8GHz, respectively. Tunability of the notch depth (Fig. 3.11) is achieved by varying the biasing of transistor M2 (Fig. 3.6). The corresponding variation in S11 and S22 is shown in Fig. 3.12. Clearly, tuning the Q-factor of the notch filter has minor effects on the system's S11 and S22.

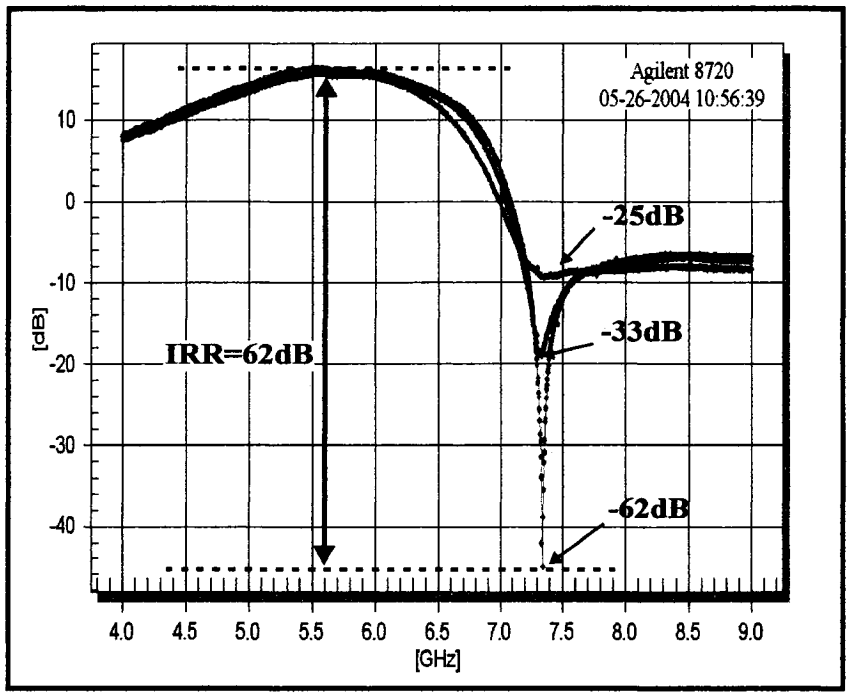

Figure 3.11 Measured forward transmission (S21), showing the image rejection depth tunability.

Many approaches for automatic Q-tuning have been introduced in the literature. For example, a master-slave technique, which consists of controlling the notch filter (slave) by correlating its response to that of a voltage controlled oscillator (master), can be added to the circuitry proposed here (e.g. [65]). This technique was implemented by Li and Tsividis in bipolar [65], but can be adopted for CMOS filters as well. For automatic Q-tuning, the image rejection should not be sensitive to *small variations in the notch's biasing current* [15]. The image rejection of the single IRF filter proposed in this chapter with respect to the biasing current of transistor M2 is plotted in Fig. 3.13, with the current varied from 1.6mA up to 2.1mA. As it can be seen from the figure, biasing currents ranging from 1.68mA to 2.0mA generate more than 35dB of image rejection. This suggests that the current in the notch can deviate as much as 10% around 1.82mA, while providing reasonable image rejection. This supports the practical feasibility of adding automatic Q-tuning to the circuit proposed here.

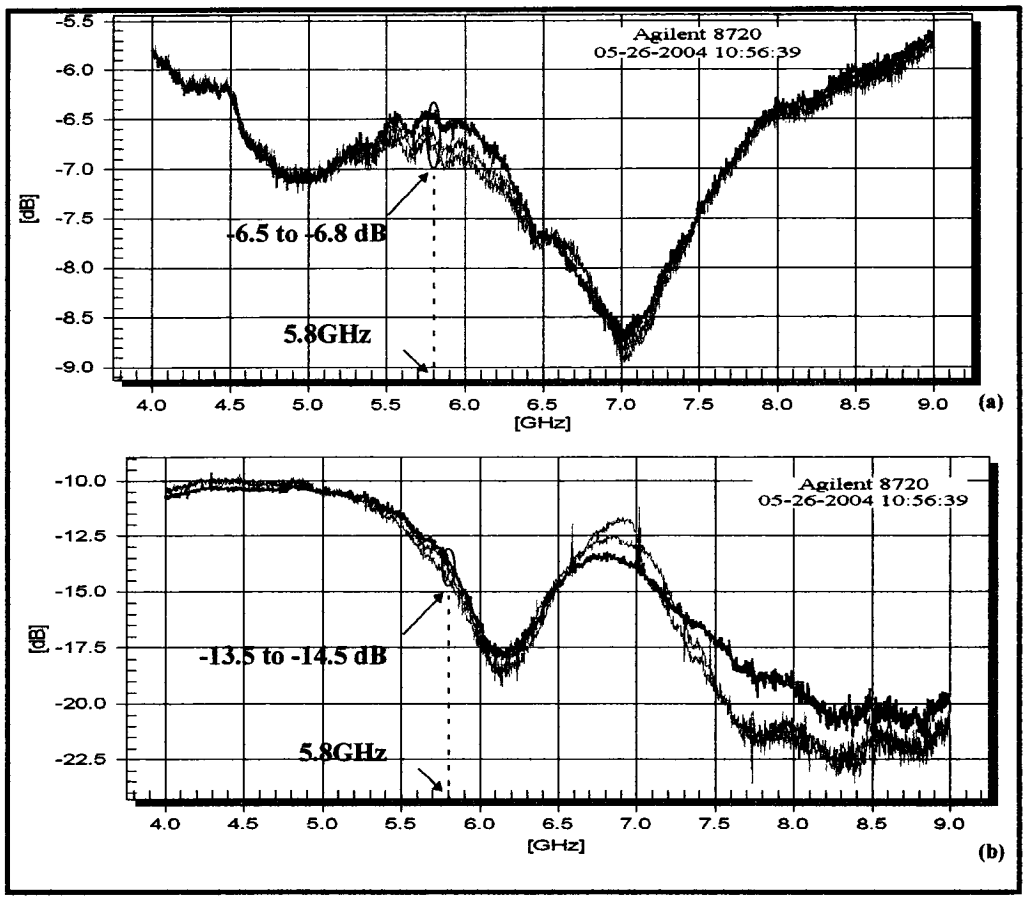

Figure 3.12 a) Measured input reflection coefficients (S11), and b) measured output reflection coefficients (S22) for different image rejection bias settings.

Figure 3.14.b shows the midband gain behavior of the LNA as the notch depth is tuned (Fig. 3.14.a): it is interesting to note that only a maximum deviation of 1dB in the gain is observed over a wide tuning range, demonstrating that the notch filter does not affect much the behavior of the LNA. With the image rejection set to -62dB, the noise figure of the LNA-notch combined circuit is 4.1dB at 5.8GHz. With the notch circuit turned off, the measured noise figure is 3.3dB. With the LNA gain set to 15.8dB, a 1dB compression point of -15dBm is measured.

Excluding the output buffers, the circuit consumes 9mW of power. Power consumption can be further minimized by using a folded cascode structure for the LNA [96]. The proposed notch filter alone can operate from a 1V supply voltage. Tuning of the

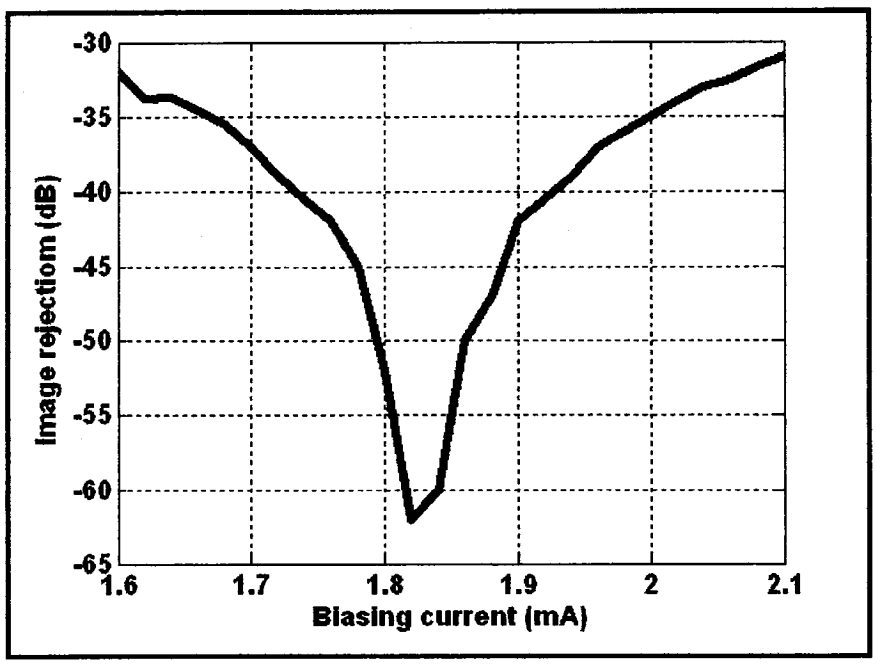

Figure 3.13 Image rejection versus the biasing current (I_{M2}) of the notch filter, showing that more than 35dB of IR can be obtained with I_{M2} tuned from 1.65mA to 2mA.

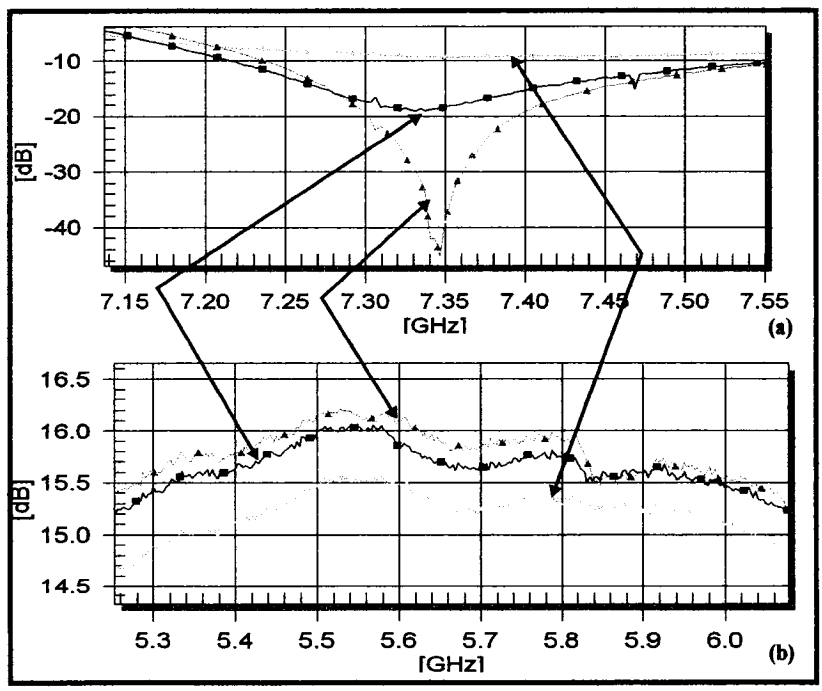

Figure 3.14 A maximum of 1dB deviation in the bandpass gain of the LNA is observed, for maximum image rejection tuning. a) Image rejection tuning. b) Corresponding LNA midband gain.

Table 3.2: Summary of the measured and simulated performance of the combined LNA-notch circuit.

	Simulated	Experimental
Technology	CMOS 0.18μm	CMOS 0.18μm
f_o . LNA	5.8GHz	5.8GHz
LNA gain	17.5dB	15.8dB
S11 @5.8GHz	-10dB	-6.5dB
S22@5.8GHz	-13dB	-13.5dB
NF @ 5.8GHz	3.3dB	3.6 dB
f_o - Notch	7.4GHz	7.3GHz
Maximum image rejection	-65dB	-62dB
VDD	1.8V	1.8V
Power consumption	11mW	11mW
Input 1dB compression point	-16dBm	-15dBm
IIP3	-4.5dBm	-5.3dBm

notching frequency may be obtained by replacing capacitor C_{N2} by an accumulation mode varactor. The circuit measured performance is summarized in Table 3.2. Also shown in the table are the simulation results of the prototype layout, including all devices, interconnect, and packaging parasitics.

3.6 - Proposed Receiver RF Front-End Architecture

Consider the band-reject filters shown in Fig. 3.15-a. Assume that the passive devices have acceptable quality factors, such as their transfer functions generate a maximum image rejection of -30dB (Fig. 3.15-b). The IR frequencies of the filters are slightly offsetted, and are centered at 4.8 and 5.1GHz, respectively. In this case, each filter has a 3dB bandwidth of 84MHz. Cascading them with care could result in the transfer function shown in Fig. 3.15-c: A maximum image rejection of 55dB is obtained, with a -3dB bandwidth of 160MHz. More than 30dB of image rejection can now be obtained over a 400MHz bandwidth.

Let's see how this idea can be exploited in RF heterodyne receiver front-ends.

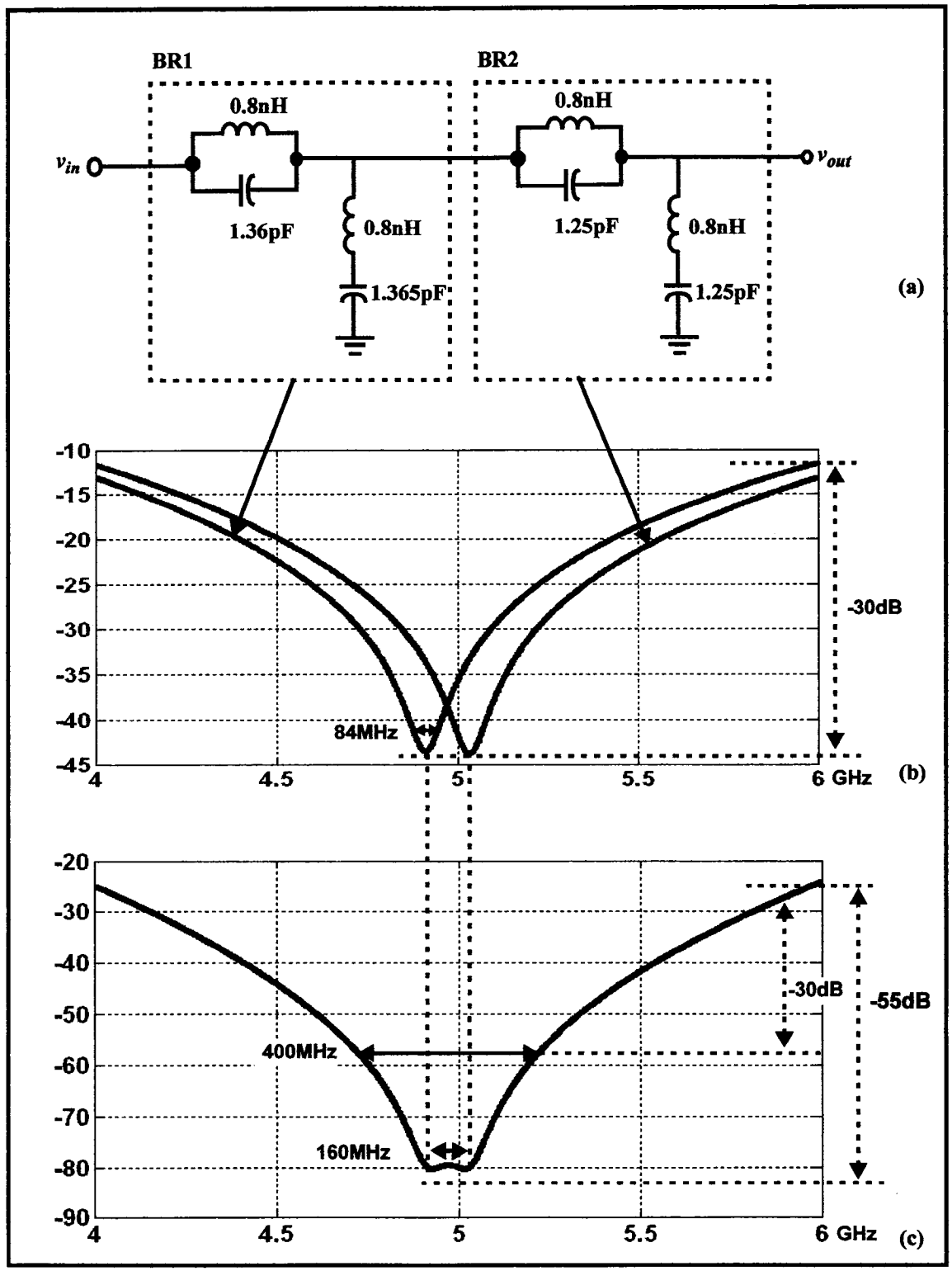

Figure 3.15 a) Image reject filters using passive devices. b) Transfer function of the individual image reject filters. c) The response of the cascaded filters.

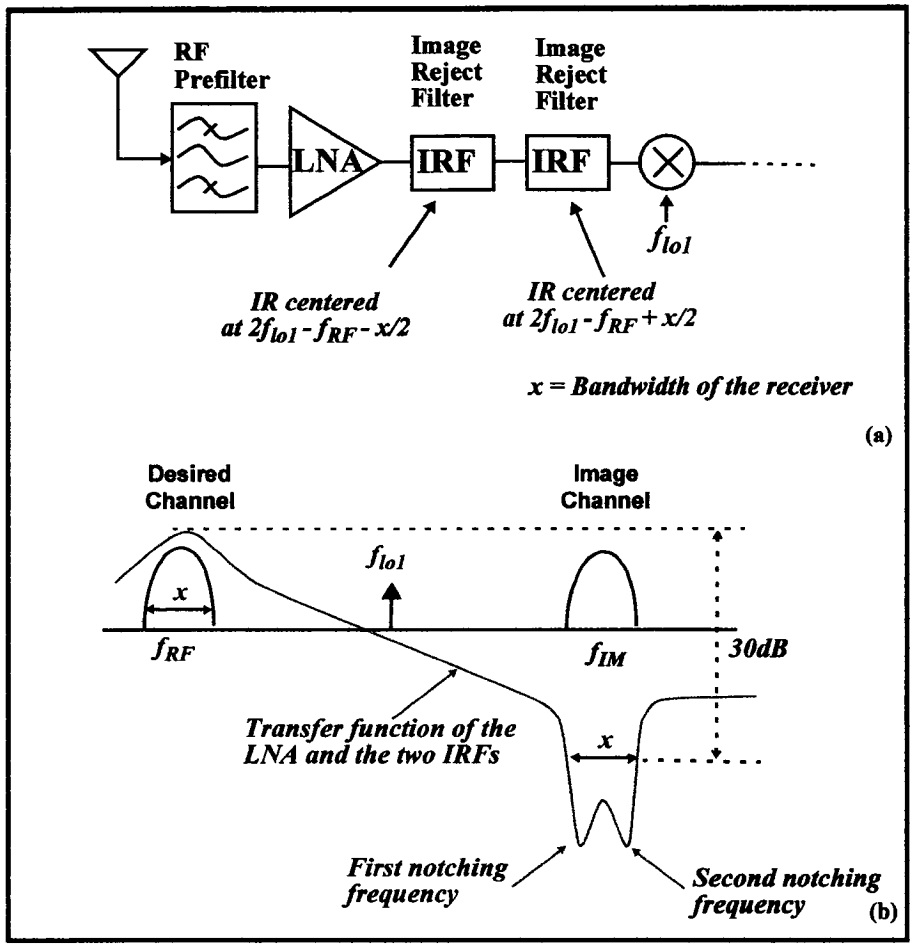

Figure 3.16 a) Structure of the proposed receiver architecture.
b) Transfer function of the LNA plus the two IRF's.

Figure 3.16 shows the proposed front-end receiver architecture, aimed at reducing circuit complexity by eliminating the need for tuning the notch filter, while ensuring adequate performance over PVT variations. The front-end does not employ a PLL for tuning the notch (e.g. Fig. 3.1-a). Instead, it consists of cascading two notches after the LNA, with their image reject frequencies slightly offsetted. As a result, a wide image rejection bandwidth can be obtained, without the need for extra notch frequency tuning circuits.

For a 5.8GHz receiver with an 800MHz IF, and a VCO frequency of 6.6GHz, the image signal would lie in the vicinity of 7.4GHz. For an image rejection bandwidth of 200MHz, the first and second notching frequencies are set to 7.3GHz and 7.5GHz, respectively. The rejections at the notching frequencies can be sharpened by using on-chip active Q-factor enhancement for each notch independently. This solution

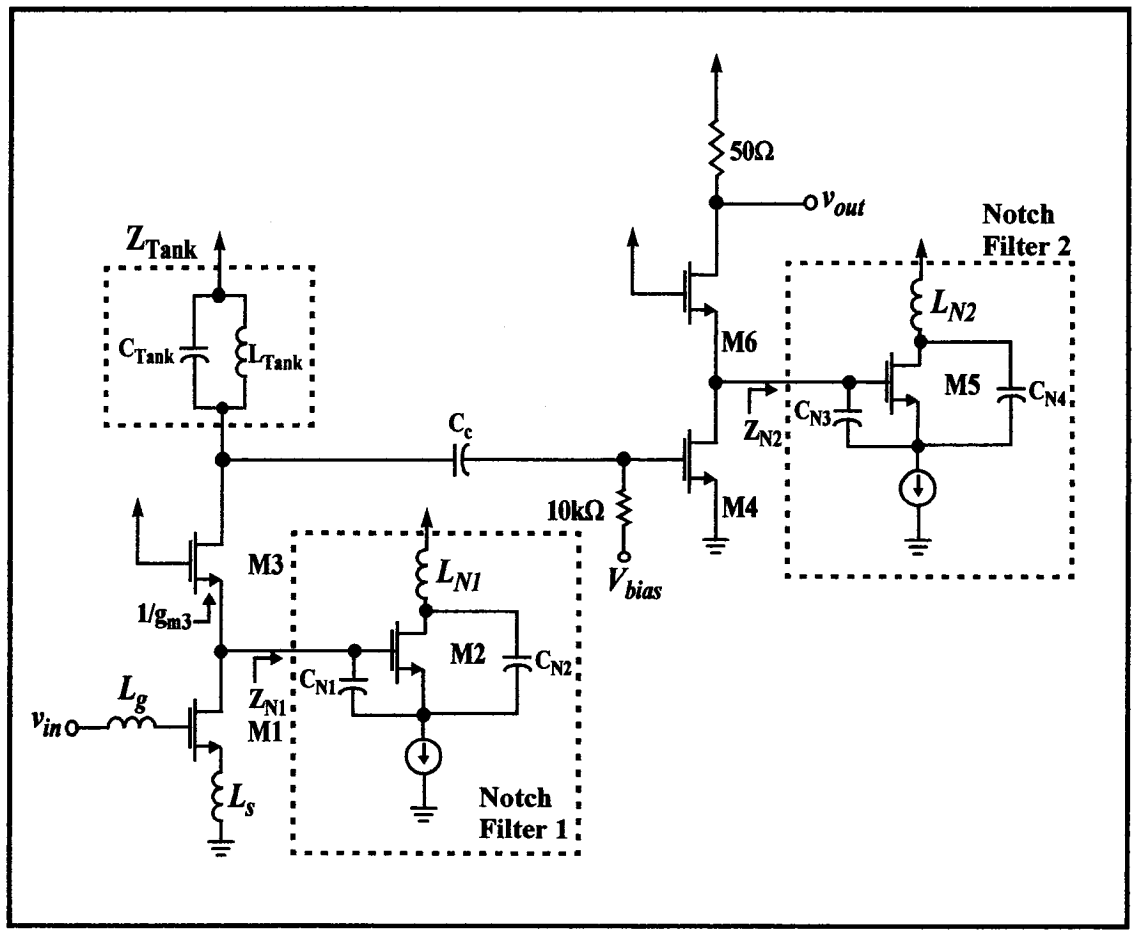

Figure 3.17 Schematic of the LNA and the double IRFs circuit.

considerably decreases the power consumption and the complexity of the receiver.

The LNA-notch filters combination in Fig. 3.17 was designed using the circuits reported in Section 3.4. The circuit operates as follow:

i- Transistors M1 and M3 form a cascode LNA.

ii- The first notch filter is connected at the drain of transistor M1.This filter was designed to nominally resonate at 7.3GHz.

iii- Transistors M4 and M6 along with the 50Ω resistance form a cascode output buffer. The second notch filter was connected at the drain of transistor M4. This filter was designed to nominally resonate at 7.5GHz.

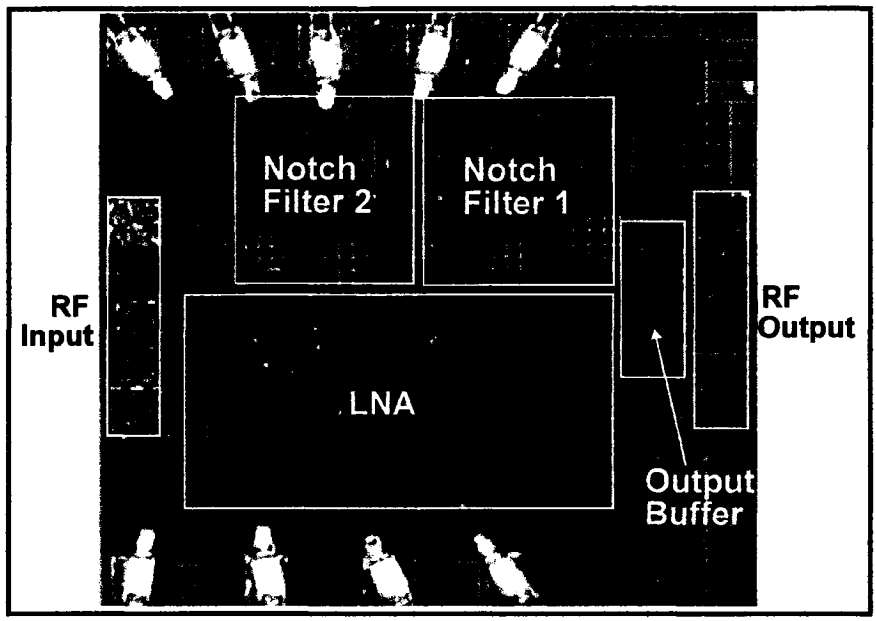

Figure 3.18 Photomicrograph of the double IRF LNA-notch combination.

Capacitor C_c is a large decoupling capacitor. The 10kΩ resistance was used to block the AC signal from leaking to the biasing circuitry of the output buffer.

Calibration of the wide image rejection bandwidth over process variation can be performed at power-up, thus eliminating the overhead of integrating a 7.4GHz PLL to track the image reject frequency. For example, an array of digitally controlled switch-capacitors can be added to adjust the center frequency of the filters [66]-[69]. As a result, the power consumption of the front-end is minimized during receive mode. Since a PLL is not required to tune the image rejection frequency of the front-end, the power consumption during receive mode is significantly reduced.

3.7 - Experimental Results

The proposed front-end receiver was designed and integrated using a 0.18μm CMOS process from TSMC. The prototype chip was housed in a standard CFP24 package. The micrograph of the LNA double-notch combined circuit is shown in Fig. 3.18. This chip occupies 1.2mm^2, including all bonding pads.

The PCB board is shown in Fig. 3.19. Microstrip lines were manually designed. Parallel surface-mount capacitors were connected to all BNCs in order to filter out the DC lines and the power traces. The BNCs were placed on opposite sides of the board, in order to liberate enough space for on-chip probing, as shown in Fig. 3.20.

Figure 3.21 shows the transfer function of the LNA plus the two IRFs. A +15dB LNA gain at 5.8GHz, and a minimum of 30dB of image rejection over a 400MHz bandwidth centered at 7.4GHz, are obtained. This is much wider than the 200MHz bandwidth specification for the 802.11a WLAN standard. Also, 40dB of IR is obtained for over a 250MHz bandwidth. To the best of our knowledge, there has not been any reported measurements with such a wide image rejection bandwidth for CMOS RF heterodyne receivers, operating in this frequency range. The measured input and output reflection coefficients, S11 and S22, are -15dB and -12.4dB at 5.8GHz, respectively (Fig. 3.22).

A comparison between the circuit performance in [60], which included automatic tuning for the IR filter, and the LNA double-notch circuit proposed here is summarized in

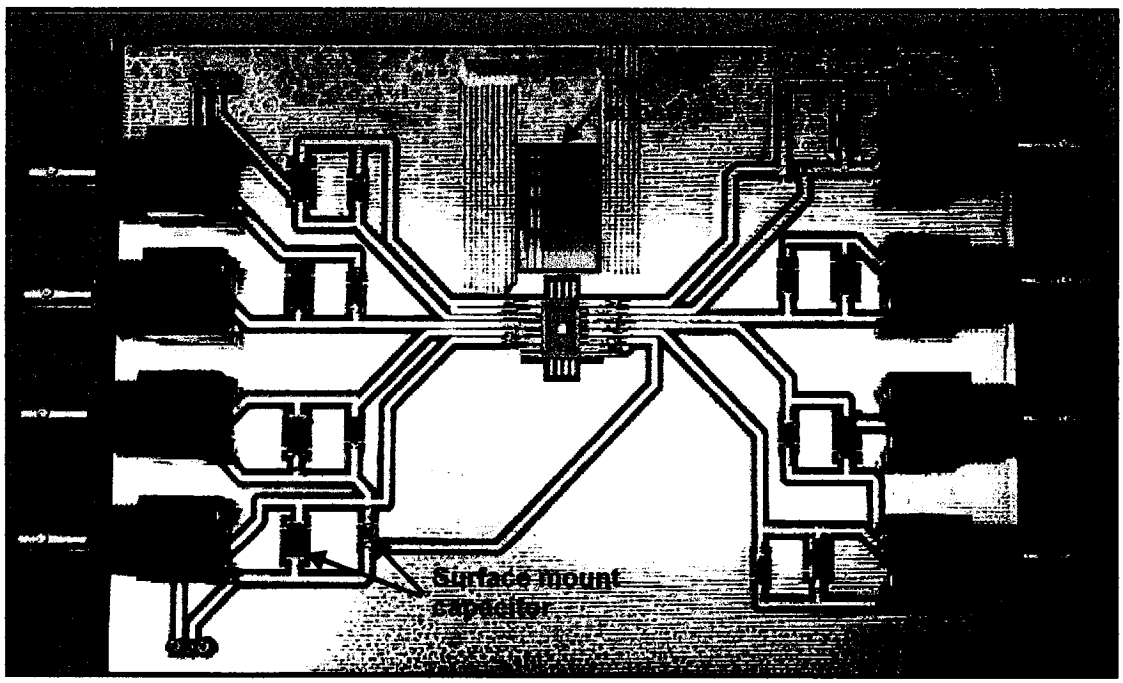

Figure 3.19 PCB of the LNA-double notch circuit.

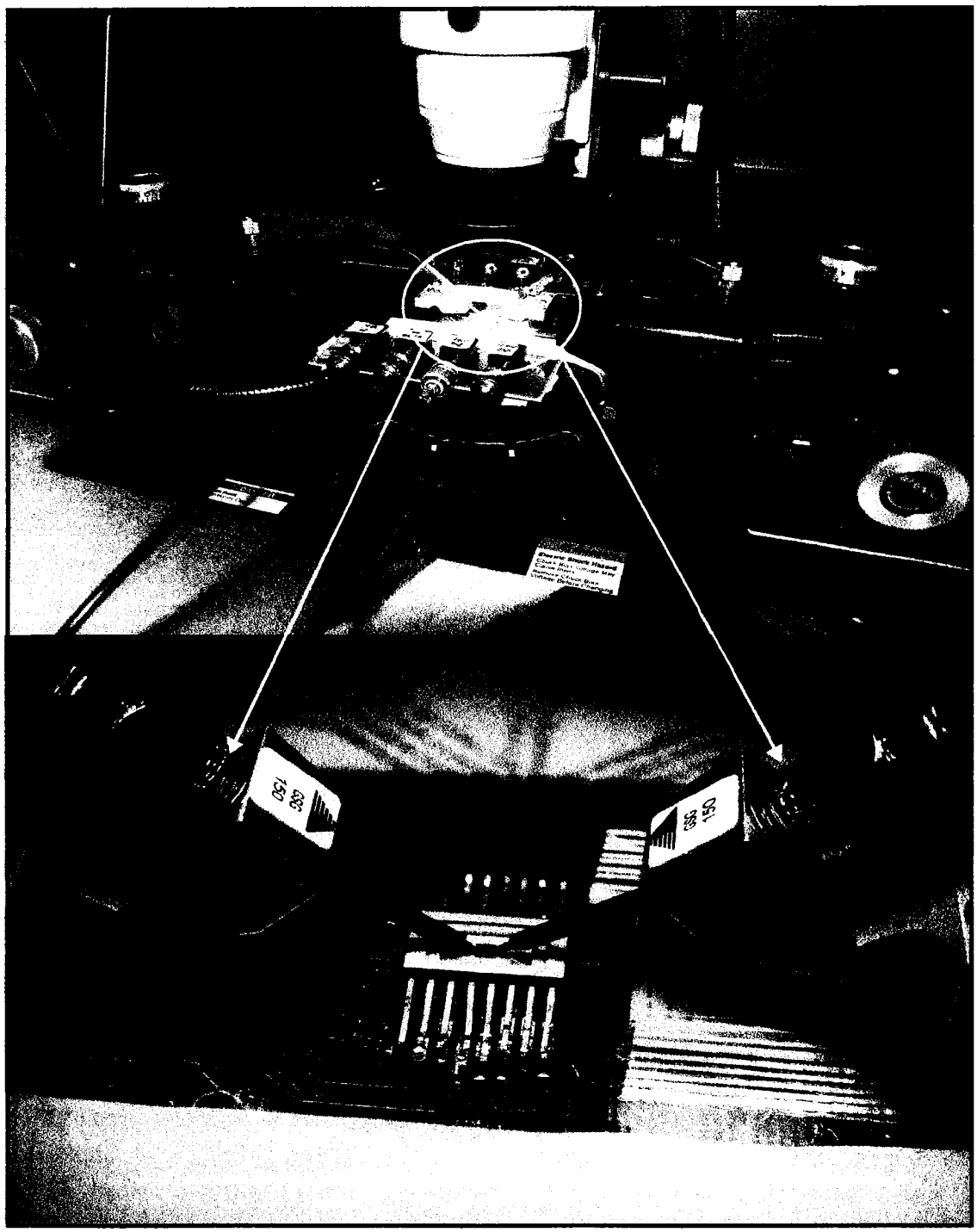

Figure 3.20 Test setup showing combined wire bonding biasing and on-chip RF probing.

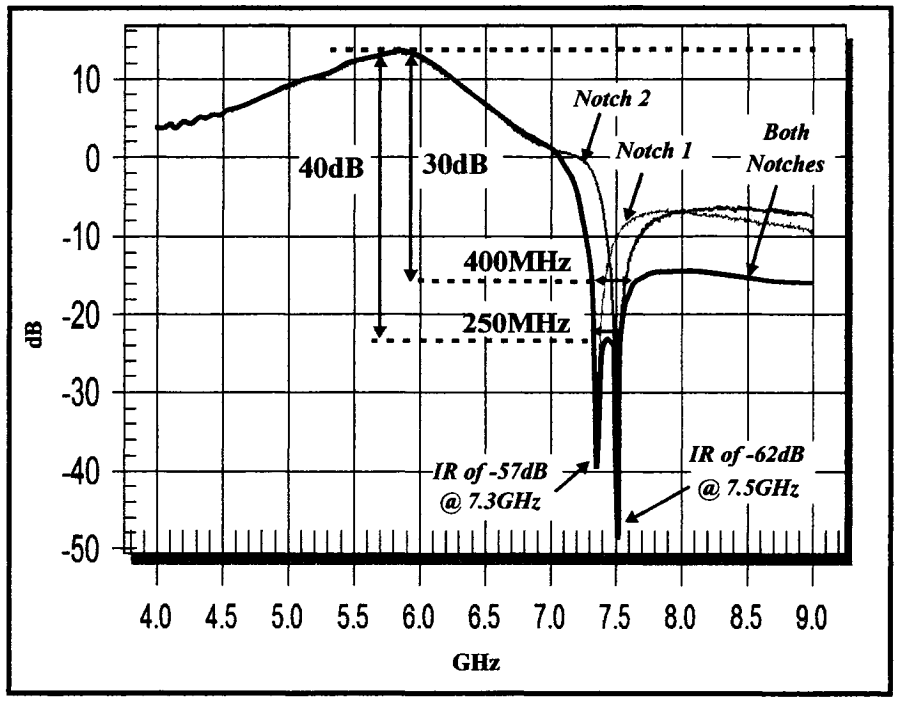

Figure 3.21 Measured forward transmission (S21) of the LNA-IRF front-end, showing 30dB of image rejection over a 400MHz bandwidth.

Table 3.3. First, the double IRF architecture greatly decreases the overall complexity of the heterodyne front-end since an entire PLL for tuning the filter's frequency was replaced by one extra notch filter (i.e. one transistor, two capacitors, and an inductor). Moreover, the power consumption of the image reject filter in [60] and of its automatic tuning circuitry sums up to 12.5mW[1], while the combined IR filters proposed in this thesis consume only 4mW, combined. Finally, the frequency of the image reject filter and the maximum amount of RF signal suppression obtained here are higher than the ones reported in [60].

3.8 - Conclusion

A new implementation of a CMOS notch filter was reported earlier in this chapter. Then, a simple and robust implementation of on-chip image rejection, based on the cascade of two slightly offsetted image reject filters, was proposed in this chapter.

1. The power consumption of the notch in [60], which is a differential circuit, was divided by 2 for a fair comparison.

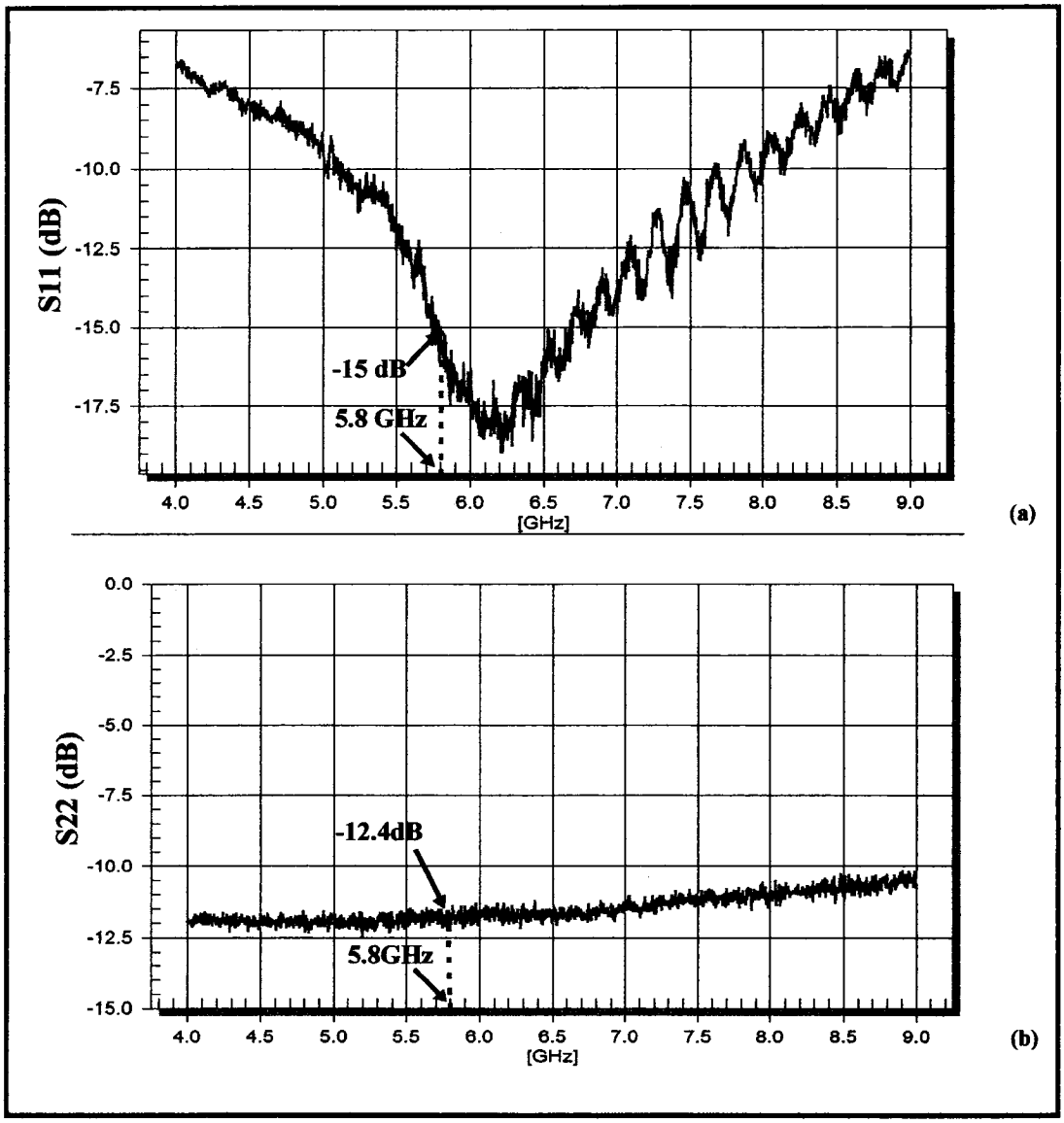

Figure 3.22 Measured a) S11 and b) S22 parameters.

The circuit does not require on-chip frequency automatic circuits nor off-chip components. The LNA and double IRF front-end demonstrated more than 30dB of IR over a 400MHz bandwidth centered at 7.4GHz in a standard CMOS technology.

Table 3.3: Summary of the measured performance of the combined LNA-two IRF circuit, and comparison to state-of-the-art.

	This work	Koroglu et al. [60]
Technology	0.18μm CMOS	0.15μm CMOS
VDD	1.8V	1.5V
f_o - LNA	5.8GHz	1.8GHz
LNA gain	15dB	23.5
f_o - Notch	7.3-7.5GHz	2.0-2.2GHz
30dB IR bandwidth	400MHz	-
Maximum IR	-62dB @ 7.5GHz (from Fig. 3.21)	-49dB @ 2.2GHz
NF	4.1dB @ 5.8GHz	4.5dB @1.8GHz
Power consumption of the IR filters	4mW (for both filters)	12.5mW (including tuning circuitry)
Input 1dB compression point	-15dBm	N/A[1]
IIP3	-5.3dBm	N/A[1]

1. The values reported in [60] are for the entire front-end.

Chapter 4 - Distortion in RF CMOS Short Channel LNAs

4.1 - Introduction

The linearity of LNAs is becoming of high importance for modern RF receivers. Even order harmonics generate DC offsets in homodyne receivers, while third-order intermodulation distortions, resulting from mixing with interferers in adjacent channels, can corrupt the desired downconverted signal channels.

Several studies of the effects of the CMOS transistors characteristics on the linearity of RF LNAs have already been reported, e.g. by Kang et al. [82], Toole et al. [83], Wambaq et al. [85], and Kim et al. [86]. The analysis reported in [82] discusses the third order distortion behavior of CMOS transistors for RF applications. The results presented are based on empirical coefficients obtained from measurements of specific devices. It focused mainly on the effect of the output transconductance of the transistors on distortion. The analysis in [83] attempted to exploit a "sweet-spot" in the third-order distortion response, without providing practical detailed analytical equations relating specific transistor parameters to distortion. In Section 4.2, we are going to discuss this work, which is the latest distortion analysis reported in the literature for RF CMOS amplifiers. The analysis in [85] provides models to compute the distortion in CMOS LNAs, without

providing closed form simple expressions describing the effect of specific transistor parameters, and thus without suggesting design guidelines to enhance the distortion behavior. The analysis in [86] proposes a technique to enhance the IIP3 of RF amplifiers by using multiple gated transistors, without focusing much on the fundamental behavior of distortion in the transistor itself. Besides, only the transconductance nonidealities were discussed in details. The effects of technology variations and of technology scaling were investigated in [87]-[88]. A model was proposed in [89] for large signal distortion analysis and was applied to RF CMOS power amplifiers. Linearity analysis of switching pairs operating in the weak inversion region was presented in [97]. Distortion analysis for long channel RF CMOS amplifiers was reported in [98]. In that analysis, only the effect of C_{gs} was considered. Up to date, all reported studies do not provide *closed form frequency-dependent* expressions describing the *second-order harmonic distortion in RF CMOS short-channel based LNAs*, which is becoming a major problematic issue in modern homodyne receivers. Studies of second-order distortions in MESFET and HBT devices have already been reported (e.g. [99], [100]).

In this chapter, a complete method to estimate the distortion in RF low noise amplifiers is presented. Compact equations relating distortion to the CMOS transistors' design parameters are derived. The approach used is based on the theory of Volterra's series [101]-[107]. Volterra's series are time dependent power series which can be used to describe systems with memory, i.e. employing capacitors and inductors. The CMOS transistors characteristics considered in this work include the source resistance (r_s), the output resistance (r_o), the parasitic gate-to-drain (C_{gd}), gate-to-source (C_{gs}), and drain-to-source (C_{ds}) capacitances [108]. For simplicity, the substrates of the MOS transistors are assumed to be connected to the sources, and substrate leakage currents are not included, since they do not produce considerable amount of distortion [82]. The analysis is per-

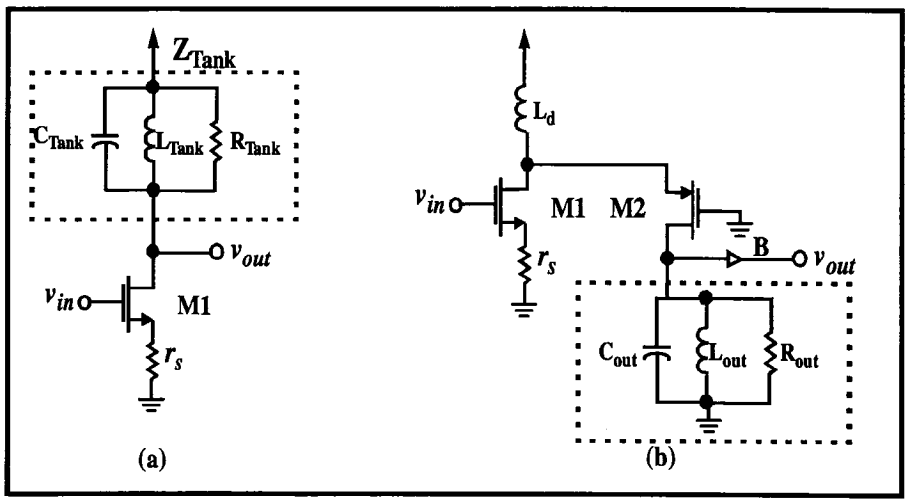

Figure 4.1 a) Common source LNA. b) Folded cascode LNA.

formed on a common source RF amplifier and on a folded cascode amplifier (Fig. 4.1).

The chapter is organized as follows: Section 4.2 gives an overview of the limitations of the use of the sweet-spot point for RF applications. The procedure to obtain closed-form expressions describing the distortion in nonlinear circuits using Volterra's series is presented in Section 4.3. Distortion analysis of a single-transistor amplifier and of a folded cascode amplifier is then discussed in details in Section 4.4. Distortion-aware design guidelines for RF LNAs are provided in Section 4.5. The chapter concludes with a verification of the analytical results proposed through a comparison with measured results from an LNA chip prototype.

4.2 - Limitations of Using the Distortion Sweet-Spot Point for RF Applications

A summary of the work presented in [83] is discussed in this section. To the best of our knowledge, it is the most recent distortion analysis of RF CMOS amplifiers reported in the literature. In short-channel CMOS transistors, the main source of distortion comes from the nonlinear behavior of the transconductance. Assuming the output transconductance to be linear and that the cross modulation between the transconductances is negligible, the AC current in a MOS transistor can be modeled as:

$$i_{ds}(v_{gs}, v_{ds}) = g_m v_{gs} + g_d v_{ds} + g_{m2} v_{gs}^2 + g_{m3} v_{gs}^3 + \dots \quad . \tag{4.1}$$

As explained in Chapter 2, the second-order transconductance g_{m2} equals 0A/V at zero V_{gs}, then increases before reaching a maximum value at a small overdrive voltage (V_{gs}-V_t) (Fig. 2.5). Further increase in V_{gs} results in decreasing g_{m2}. As a result, g_{m3}, which is obtained by differentiating g_{m2} with respect to V_{gs}, decreases to zero at a very small overdrive voltage, i.e. when the transistor is still operating in the moderate inversion region. Therefore, theoretically, if the transistor is biased at this operating point, known as the "sweet-spot" point [83], the third-order harmonic distortion would tend to be zero, which would result in an infinite third-order output intercept point (OIP3). It is an attractive line of thought to follow for analog circuit designs in general.

Typical structures of low-noise, low-power, RF amplifiers are shown in Fig. 4.2, and are used in the following analysis. For simulation purposes, the tank impedance was set such that the LNA midband gain is maximized at around 5GHz. Capacitor C_T models the parasitic capacitances of the on-chip inductor and all of the parasitic capacitances that appear at the tank from wiring connections. It also includes the parasitic capacitances of subsequent stages that are usually connected to the output node of the LNA. After evaluating C_T, L_T was chosen to resonate the tank at 5GHz. R_T models the parasitic resistances of the *LC* tank. In standard CMOS processes, the typical quality factors of on-chip induc-

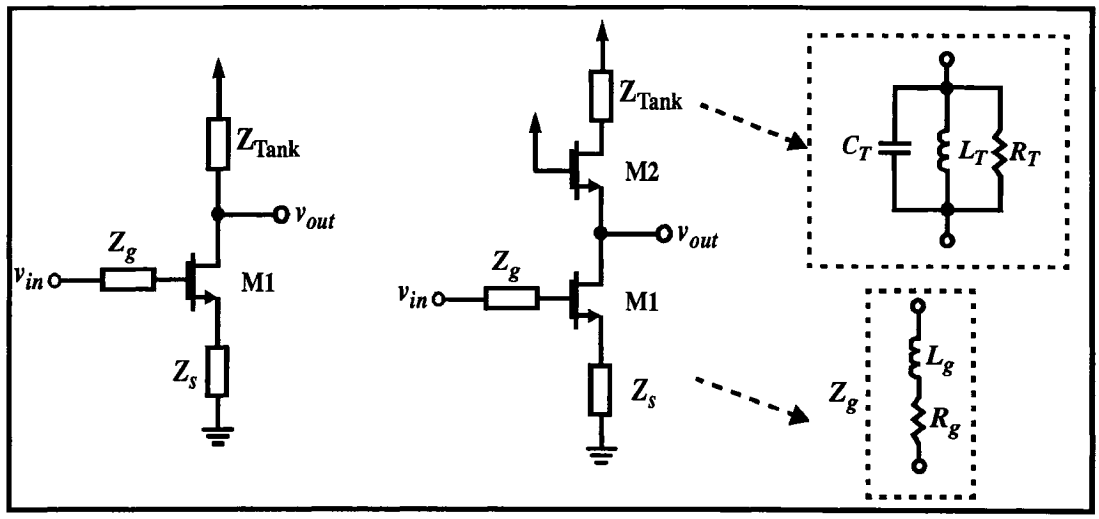

Figure 4.2 Circuits used for analysing the "sweet-spot" point in RF CMOS LNAs.

tors at 5GHz are in the range of Q=4-8. The sizes of the transistors were set to 125μm/0.18μm, which is reasonable for RF LNA designs. First, the circuit was simulated without using any degeneration impedances or input matching inductors. The output intercept point was then obtained from transient simulations based on the BSIM transistor models in HSPICE. As expected and as obtained in [83], the OIP3 is maximized at the biasing point where the third-order transconductance reaches zero (Fig. 4.3). At that point, the maximum RF LNA midband gain obtained, without degeneration impedances, was 6dB. The circuit was then simulated after adding a small degeneration resistor (20Ω). As demonstrated in the plot, the OIP3 results changed - the maximum OIP3 in the moderate inversion region has decreased by 5dB and shifted to a lower bias current value. The latter is obviously desirable from a power point of view.

In most wireless systems, the LNA is preceded by an off chip filter or by an RF antenna. These blocks are typically designed with 50Ω output impedances. Therefore, to maximize the power transfer between them and the LNA, input matching becomes critical. Hence, an input matching inductor L_g with a Q of 5 was added to the circuits in Fig. 4.2, and the degeneration resistor was replaced by an inductor L_s. The corresponding OIP3 is shown in Fig. 4.3. The value of the gate inductor L_g was chosen such that the

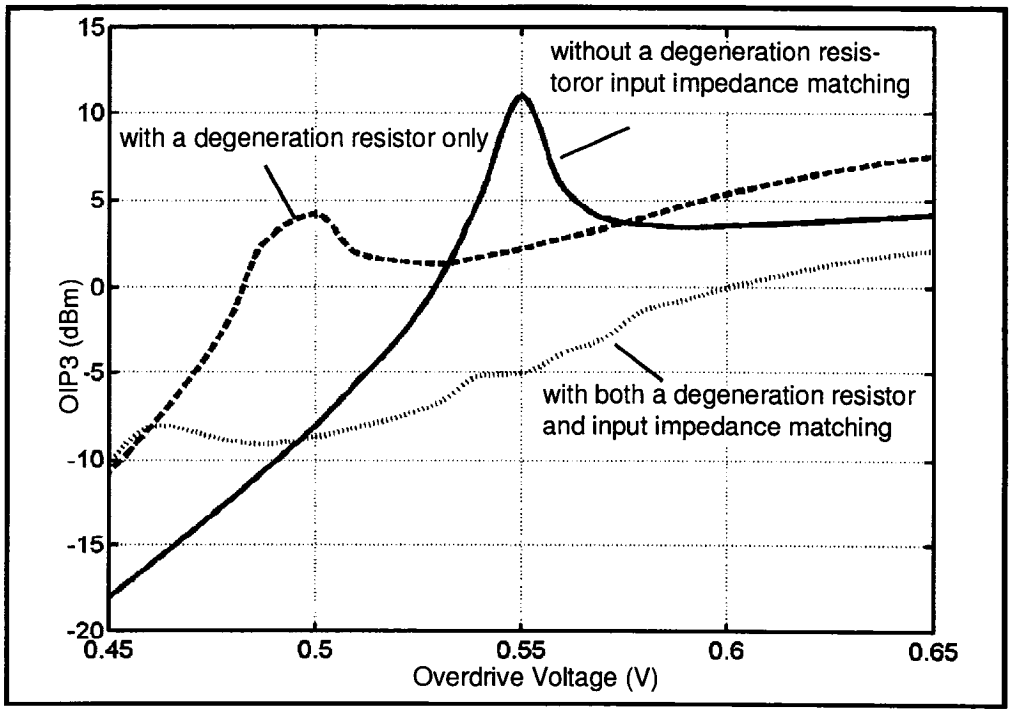

Figure 4.3 OIP3 simulations of a single transistor amplifier i) without degeneration and input matching, ii) with a degeneration resistor, and iii) with a degeneration resistor and input impedance matching. Note that varying the overdrive voltage is equivalent to biasing the transistor at different current bias points.

input reflection is less than -10dB at 5GHz. It is interesting to note that by adding L_g, the OIP3 in the moderate inversion region decreased by about 15dB from its original peak (Fig. 4.3).

The OIP3 decreases with the addition of the input impedance matching and the degeneration impedance due to the feedback path created between the output voltage v_o and the fundamental tone of the input signal (Fig. 4.4). The OIP3 depends mainly on three responses: the third-order response of the circuit, the cross-modulation between the second-order harmonic distortions and the fundamental tone, and the cross-modulation of higher order terms. In LNA designs, when the circuit is stable and the transistor is operating in the deep saturation region, the current in the MOS transistor converges within the first few terms of its Taylor's expansion (Eq. 4.1). Thus, high-order harmonics are rela-

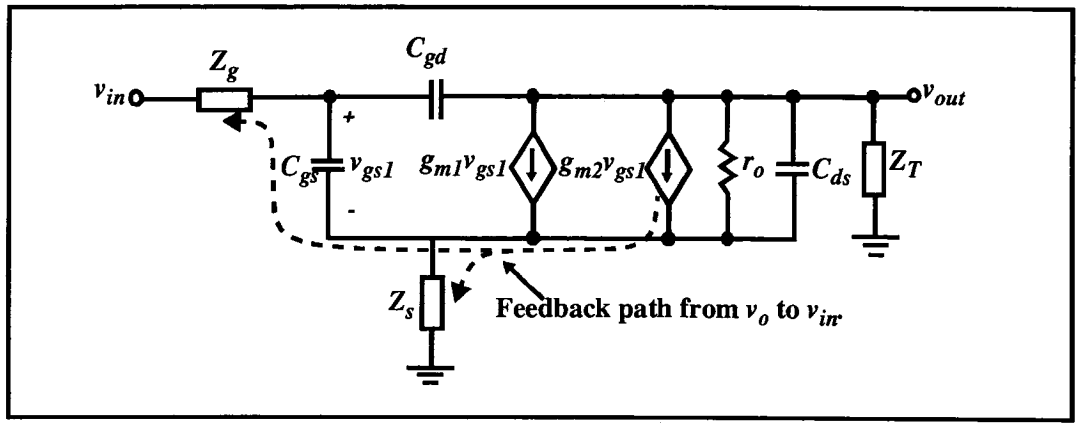

Figure 4.4 Small signal model of a FET transistor, showing the effect of input impedance matching and the degeneration impedance as a feedback path.

tively small and can be neglected. If a degeneration impedance is used in the LNA, an AC ground appears at the source of the input transistor, such that the second-order harmonic output response is isolated from the input node. A small feedback path however still exists through the parasitic gate to drain capacitor C_{gd}. Since the value of C_{gd} is typically very small, only slight cross-modulation between the fundamental tone and the second harmonic occurs and does not affect much the OIP3. However, as illustrated in Fig. 4.4, with degeneration, the output second-order response of the LNA is fed back to the input node via Z_s and the large parasitic capacitance C_{gs}. Hence, the second-order response mixes with the fundamental tone and greatly degrades the third order intercept points [109]. It is interesting to note that at the bias operating point where g_{m3} equals zero, g_{m2} (the second-order non-linear response of the transconductance) reaches a maximum. As a result, at this sweet-spot point, the second-order harmonic distortion and the cross-modulation of the second-order response with the fundamental tone are large.

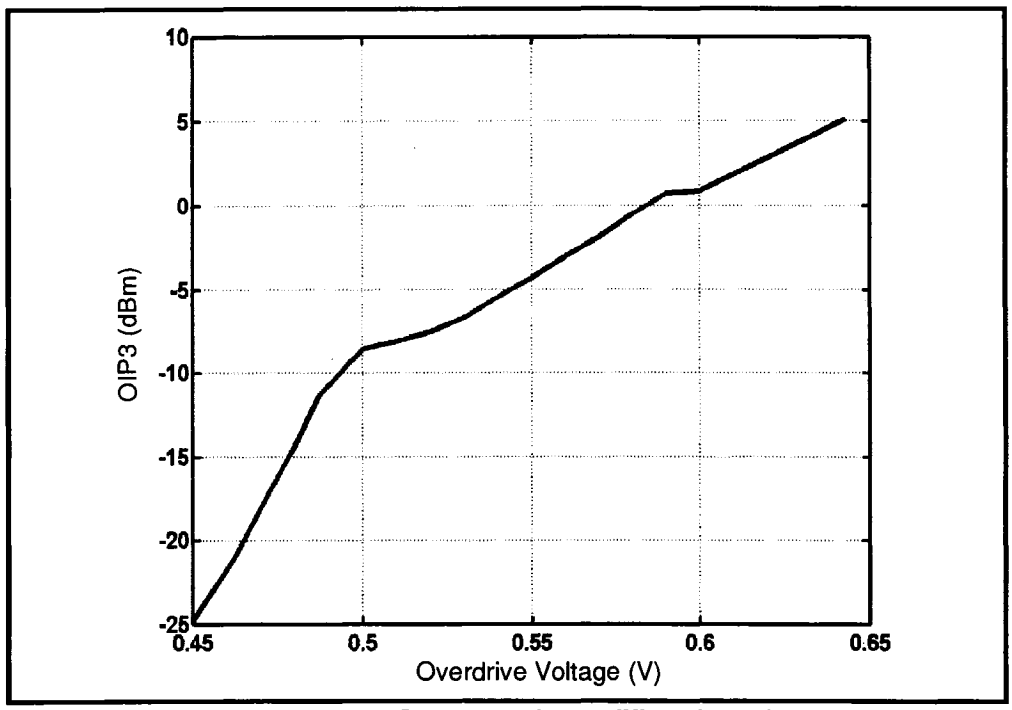

Figure 4.5 OIP simulation of a 5GHz cascode amplifier with a degeneration inductor of 200pH, a load inductor of 1.2nH, and a transistor sizing of 125μm/0.18μm.

By simulating a more typical RF LNA structure, namely a cascode structure with a degeneration inductor of 200pH and a 1.2nH load inductor with a quality factor of 5, the maxima in the OIP3 response in the moderate inversion region disappears, as demonstrated in Fig. 4.5.

The above suggests that the use of the "sweet-spot" point in the moderate inversion region for CMOS short channel transistors might not be easily applicable for RF LNA designs. However, it can be greatly appreciated in amplifiers operating at lower frequencies [83].

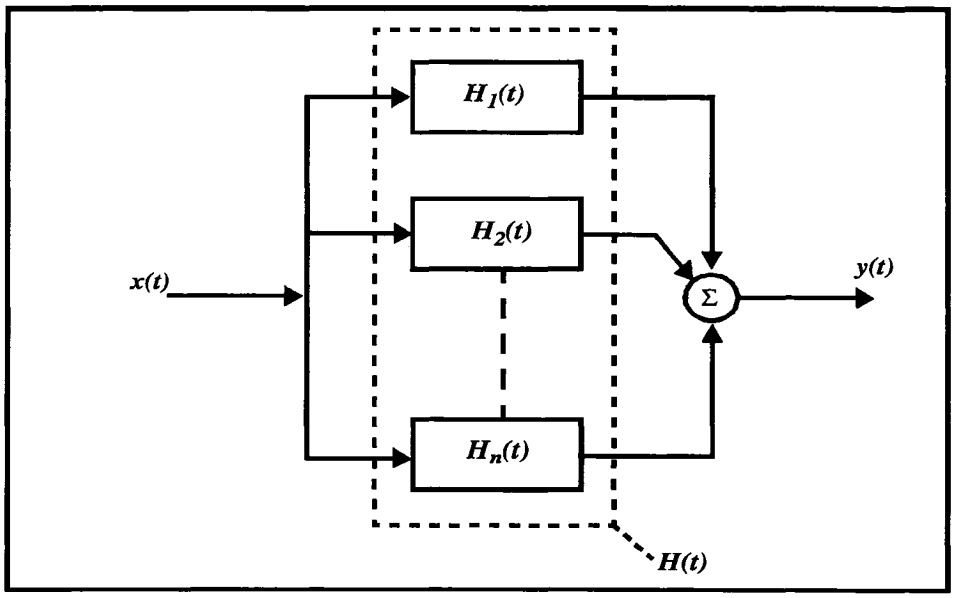

Figure 4.6 Schematic representation of an n-th order system response [85].

4.3 - Basics of Volterra Series

Under some general continuity requirements, i.e. the function and its *n* first derivatives are continuous and differentiable, the output of a nonlinear system can be expanded into a Volterra series. The Volterra series can be seen as the sum of the responses of a first-order operator, a second-order operator, etc. (Fig. 4.6). Assuming ***H(t)*** is a nonlinear system and *x(t)* is its input, the output *y(t)* can be expanded as

$$y(t) = \boldsymbol{H}_1(x(t)) + \boldsymbol{H}_2(x(t)) + \ldots + \boldsymbol{H}_N(x(t)) \ , \tag{4.2}$$

where

$$H_i(x(t)) = \int_{-\infty}^{\infty} \ldots \int_{-\infty}^{\infty} (h_i(\tau_i, \ldots \tau_i) \cdot x(t-\tau_1) \ldots x(t-\tau_i) d\tau_1 \ldots d\tau_i) \ , \tag{4.3}$$

is the i^{th} Volterra operator, and $h_i(.)$ is the i^{th} Volterra kernel. The Laplace transform of a multi-dimensional function $h_n(.)$ is

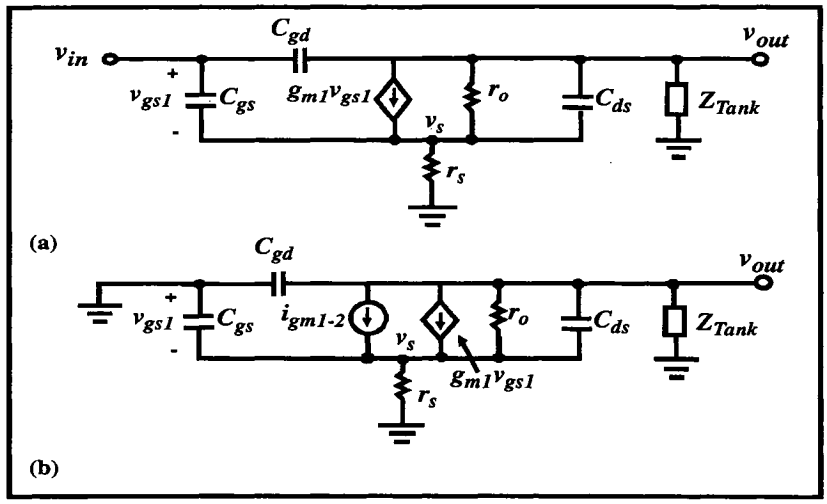

Figure 4.7 Small-signal equivalent circuit of the LNA in Fig. 4.1a: a) the circuit used for the first-order kernel analysis, and b) the circuit used for the second order kernel analysis.

$$H_n(s_1, \ldots, s_1) = \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \ldots \tau_n) e^{-(s_1\tau_1 + \ldots + s_n\tau_n)} d\tau_1 \ldots d\tau_n, \qquad (4.4)$$

where s_i is the Laplace variable in the i^{th} dimension. The n^{th} order Laplace transformed Volterra kernel defines entirely the n^{th} order behavior of the system in the frequency domain.

A method based on Volterra series to study the nonlinear effects of transistors in continuous time analog circuits was presented in [101] and is adopted for our analysis. It can be summarized as follows:

1- A small-signal nodal analysis is initially performed to obtain the first-order response of the circuit (e.g. Fig. 4.7-a). The set of transfer functions relating the input voltage v_{in} to the nonlinear internal voltages (the gate-source voltages v_{gsk}) is then derived. The equations obtained can be arranged in a matrix format as follows

$$\underbrace{\begin{bmatrix} a_{11} & a_{12} & \dots & \dots & a_{1K} \\ a_{21} & \dots & \dots & \dots & \dots \\ \dots & \dots & \dots & \dots & \dots \\ \dots & \dots & \dots & \dots & \dots \\ a_{K1} & \dots & \dots & \dots & a_{KK} \end{bmatrix}}_{\mathbf{A(s)}} \underbrace{\begin{bmatrix} v_{out} \\ v_{gs1} \\ v_{gs2} \\ \dots \\ v_{gsK} \end{bmatrix}}_{\mathbf{B(s)}} = \underbrace{\begin{bmatrix} C_1 v_{in} \\ 0 \\ 0 \\ \dots \\ 0 \end{bmatrix}}_{\mathbf{C(s)}}, \tag{4.5}$$

where a_{lm} is a function of the circuit's parameters in the frequency domain, and K is the number of transistors. Dividing through by v_{in}, and taking the Laplace transform, the column vector on the left hand side becomes

$$\left[H_{nout}(s)\ H_{nvgs1}(s)\ H_{nvgs2}(s)\ H_{nvgs3}(s)\dots\ H_{nvgsK}(s)\right]^T, \tag{4.6}$$

where $H_{nvgsk}(s)$ is the n^{th}-order transfer function between the input voltage and the gate-source voltage of the k^{th} transistor. Using Kramer's rule, we can then solve for $H_{nout}(s)$ and for $H_{nvgs1}(s)$ up to $H_{nvgsK}(s)$.

2- To obtain the second-order nonlinear response, the circuit is then analyzed as in step 1 with the nonlinear inputs i_{gmk-2} placed in parallel with each nonlinear element, and with the linear input v_{in} short circuited (Fig. 4.7-b). The value of the second-order nonlinear current source i_{gmk-2} is given by [110]

$$i_{gmk-2} = K_{g_{mk-2}} H_{vgsk}(s_1) H_{vgsk}(s_2), \tag{4.7}$$

where $K_{g_{mk-2}}$ is the second coefficient in the Taylor expansion of the relationship between the voltage and the current in a CMOS transistor. For CMOS devices with width W and length L, when the transistor is operating in the deep-inversion saturation region, the drain current is approximately given by:

$$I_d = \frac{1}{2a(1 + V_{ds}/(E_{SAT}L))} \frac{W}{L} C_{ox} \mu_{eff} (V_{gs} - V_T)^2 \left(1 + \frac{V_{ds}}{V_A}\right), \tag{4.8}$$

where a is related to the subthreshold slope factor, E_{SAT} is the critical electrical field, C_{ox} is the capacitance per unit gate area, V_T is the threshold voltage, V_A is the Early voltage, and μ_{eff} is the effective mobility modeled as

$$\mu_{eff} = \frac{\mu_o}{1 + (u_a + u_c V_{sb})\left(\frac{V_{gs} + V_T}{T_{ox}}\right) + u_b\left(\frac{V_{gs} + V_T}{T_{ox}}\right)^2} \tag{4.9}$$

for short channel MOS devices. In Eq. (4.9), u_a and u_b represent the first and second mobility degradation coefficients respectively, u_c is the body-effect of the mobility degradation coefficient, T_{ox} is the oxide thickness, and μ_o is the charge's mobility [110]. For the derivation of the n^{th} nonlinear response, the terms $K_{g_{mk-n}}$ can then be obtained by deriving n times the expression of the current I_d with respect to V_{gs} (Appendix C1).

Note that it is possible to write the system's equations such that the resulting square matrix A(s) and its determinant $\Lambda(s)$ have the same format as that of Eq. (4.5). In fact, only the input vector (matrix C(s) in Eq. (4.5)) becomes a function of the nonlinear current sources i_{gmk}.

3- With the frequency variable s replaced by s_1+s_2 in the A(s) matrix, and using Kramer's rule, the second-order output response of the circuit can be calculated as follows:

$$H_{out2}(s_1, s_2) = \frac{1}{2}\left|\frac{E(s_1, s_2)}{\Lambda(s_1, s_2)}\right| v_{in}, \tag{4.10}$$

where $E(s_1,s_2)$ is the determinant of the square matrix in (4.5) when the first column is replaced by the nonlinear input vector. In order to calculate the magnitude of the second-order harmonic distortion for a sinusoidal input with amplitude v_{in}, it is sufficient to evaluate the magnitude of

$$HD2(s) = \left|\frac{1}{2} v_{in} \frac{H_{out2}(s_1, s_2)}{H_{out1}(s)}\right|_{s_1, s_2 = s}, \tag{4.11}$$

where $H_{out1}(s)$ is the linear transfer function of the circuit.

4- The third harmonic distortion is calculated by following a similar procedure to that described in the previous steps, with s replaced by $s_1+s_2+s_3$, and with i_{gmk-3} given by:

$$i_{gmk-3} = K_{g_{mk-3}} H_{1vgsk}(s_1)H_{1vgsk}(s_2)H_{1vgsk}(s_3) + \frac{2}{3}K_{g_{mk-2}} \times [H_{1vgsk}(s_1)H_{2vgsk}(s_2, s_3) + H_{1vgsk}(s_2)H_{2vgsk}(s_1, s_3) + H_{1vgsk}(s_3)H_{2vgsk}(s_1, s_2)] \quad . \tag{4.12}$$

For $s_1 = s_2 = s_3$, Eq. (4.12) simplifies to:

$$i_{gmk-3} = K_{g_{mk-3}}(H_{1vgsk}(s))^3 + 2H_{1vgsk}(s)H_{2vgsk}(2s) \ , \tag{4.13}$$

where the second term of the right-hand side represents the intermodulation effect of the first- and second-order harmonics on the third-order one. The third-order response of the circuit can be evaluated as is the second response of the circuit, with the frequency variables (s_1, s_2) replaced by (s_1, s_2, s_3). It is thus given by

$$H_{out3}(s_1, s_2, s_3) = \frac{1}{4}\left|\frac{E(s_1, s_2, s_3)}{\Lambda(s_1, s_2, s_3)}\right| v_{in}^2 \ . \tag{4.14}$$

The third-order intermodulation distortion can then be evaluated using

$$IM3 = \frac{3}{4}v_{in}^2\left|\frac{H_{out3}(jw_1, -jw_2, -jw_2)}{H_{out1}(jw_1)}\right| \ , \tag{4.15}$$

where w_1 and w_2 are the frequencies of a two-tone input test signals with equal amplitudes. Finally, the IIP3 is given by:

$$IIP3 = \frac{(v_{out(1,2)} - IM3)}{2} + v_{in} \ , \tag{4.16}$$

where $v_{out(1,2)}$ is the amplitude of the output signal at the w_1 or w_2 frequencies, and can be estimated by $v_{out(1,2)} = H_{out1}v_{in}$.

Although it will not be done in this thesis, this method can be extended to calculate the n^{th} kernel of the Volterra series [85]. This would require using nonlinear current sources of the n^{th} order, and repeating the process described in the previous two steps. For low-noise amplifiers, the input signal is usually small, and thus the small-signal cur-

rent in the MOSFET transistor (Eq. (4.1)) normally converges within the first few terms. Moreover, the transfer functions of LNAs typically have low-pass or bandpass responses, which helps filtering out high-order frequency terms generated in the transistors. It is therefore sufficient to describe the distortion behavior in LNAs with only the second and third-order responses.

The remainder of this chapter studies the second and third-order harmonic distortions in RF CMOS short-channel LNAs operating in the deep inversion region. The analysis shows the effects of transistor parasitics such as the source resistance (r_s), the output transconductance (modelled by a linear resistor r_o), the parasitic gate-to-drain (C_{gd}), gate-to-source (C_{gs}), and drain-to-source (C_{ds}) capacitances, and the transconductance nonidealities on distortion. Distortion aware design guidelines are suggested throughout.

4.4 - Distortion Analysis of RF CMOS LNAs Using Volterra's Series

As explained earlier, small-signal analysis of the circuit of interest has to be performed first in order to obtain the n^{th}-order behavior. The equivalent circuit for the common source RF amplifier in Fig. 4.1-a with degeneration is shown in Fig. 4.7-a. The following set of equations are obtained for this circuit by performing nodal analysis[1]:

$$v_s = \frac{(sC_{gs} + g_{m1})v_{gs1} + v_{out}/Z_{ds}}{1/r_s + 1/Z_{ds}}, \tag{4.17}$$

$$v_{dg1} = -\frac{sC_{gs}v_{gs1} + v_{out}(1/Z_{ds} + 1/Z_{Tank}) - v_s/Z_{ds}}{sC_{gd}}, \tag{4.18}$$

$$v_{out} = v_s + v_{dg1} + v_{gs1}, \tag{4.19}$$

1. Note that in order to reduce the complexity of the equations reported, the effect of C_{gd} was neglected. It is however included in the final model and its effect is studied, as will be shown later in this chapter.

$$(sC_{ds} + g_{m1})v_{gs} + \left(s(C_{ds} + C_T) + \frac{1}{sL_T} + \frac{1}{R_p}\right)v_{out} = s(C_{ds} + C_{gd})v_{in} \ , \qquad (4.20)$$

where g_{m1} is the transconductance of M1, $Z_{ds} = 1/(1/r_o + sC_{ds})$, and Z_{Tank} is the parallel combination of R_{Tank}, C_{Tank}, and L_{Tank}. All capacitors in Fig. 4.7 are assumed to be linear [108]. Equations (4.17) to (4.19) were first rearranged in a matrix format, then expressions for the second and third-order harmonic responses were obtained, as explained in steps 2- to 4- in Section 4.3. The same analysis was performed for the folded cascode LNA shown in Fig. 4.1-b, and interestingly yielded equivalent results. Expressions describing the third-order intermodulation distortion in the LNA were also derived and are summarized in Appendix C2.

Although exact closed-form expressions for the second and third-order distortions dependencies on the ***combined*** CMOS transistor characteristics were obtained using the mathematical tool Maple and were verified experimentally (Section 4.6), they were very complex, providing no insight or value for hand analysis. In order to provide the reader with practical design guidelines, we derived compact analytical expressions for distortion, taking into account ***only one*** CMOS parameter at a time. Due to the fact that the system is nonlinear, one could argue that superposition can not be used, in theory. However, since the circuit is actually weakly nonlinear, and it normally handles relatively very small signals, the cross-modulation terms resulting from the interactions between the different CMOS nonidealities were found to always be very small, compared to the other distortion terms considered and reported in this paper. Thus, these cross-modulation terms could be neglected, and a superposition-like analysis could safely be carried out, as supported by numerous simulations and measurements presented here.

4.4.1 - Effect of the CMOS Transconductance (g_m) on Distortion

Considering the effect of g_{m1} alone, the following HD2 and HD3 expressions were derived:

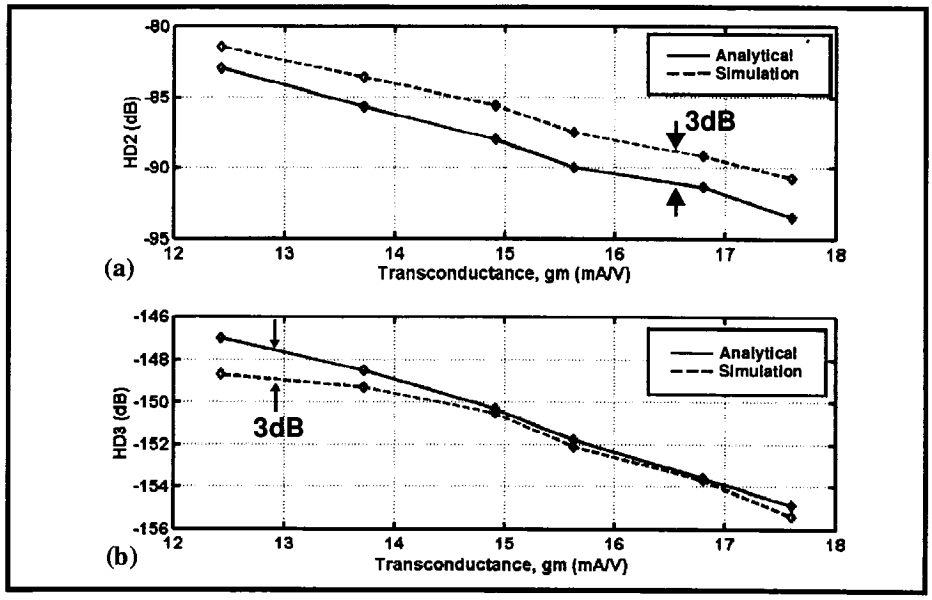

Figure 4.8 Effect of g_m: Analytical and simulated distortions a) HD2, and b) HD3. [W/L = 50μm/0.18μm, R_{tank} = 300Ω].

$$HD2(s) = \left|\frac{1}{2}v_{in}\frac{K_{gm-2}}{g_{m1}}\right|, \tag{4.21}$$

$$HD3(s) = \left|\frac{1}{12}v_{in}^2\frac{K_{gm-3}}{g_{m1}}\right|, \tag{4.22}$$

where $K_{gm\text{-}2}$ and $K_{gm\text{-}3}$ are the second and third coefficients of the taylor expansion of $I_d(V_{gs})$, as explained in Section 4.3, and are constant for a given bias point. Note that, since the $K_{gm\text{-}i}$ terms depend on the biasing current, for every g_m value, the $K_{gm\text{-}i}$ terms have to be, and are, re-evaluated. By increasing the transconductance of transistor M1, the harmonic distortions can be significantly decreased[1] (Fig. 4.8). For example, an increase of 30% in g_{m1} results in a 9dB decrease in HD2. It is interesting to note that both $K_{gm\text{-}i}$ (Appendix C1) and g_{m1} are proportional to W/L, and therefore **the second and third order harmonic distortions due to g_{m1} are <u>independent</u> of the W/L ratio, and are only inversely proportional to V_{gs}.** In a distortion aware design context, this translates to a preference of selecting a relatively small transistor size, capable of providing the necessary g_m when biased at the highest possible overdrive voltage (V_{gs}-V_t), in order to

1. Note that, for all simulation results presented in this section, v_{in} = 1mV unless otherwise specified.

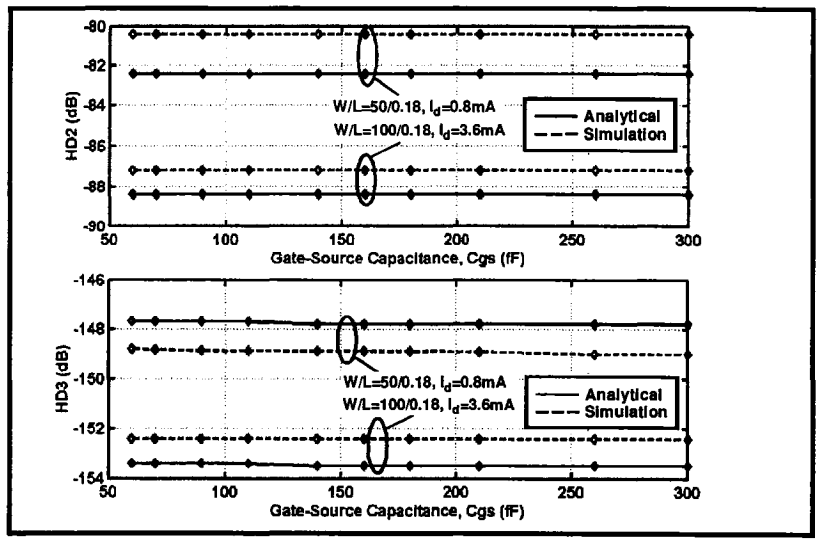

Figure 4.9 Analytical and simulated distortions: Effect of C_{gs} for two different transistor sizings.

decrease the effect of g_m on distortion.

4.4.2 - Effect of the Gate-Source Capacitance (C_{gs}) on Distortion

Expressions for HD2 and HD3 caused by C_{gs} were obtained using Maple:

$$HD2(s) = \left| \frac{1}{2} v_{in} \frac{K_{gm-2}(1 + 2sr_s C_{gs})}{(1 + sr_s C_{gs} + r_s g_{m1})(1 + 2sr_s C_{gs} + r_s g_{m1}) g_{m1}} \right| , \text{ and} \qquad (4.23)$$

$$HD3(s) = \left| \frac{1}{24} v_{in}^2 \left(2K_{gm-3} + \frac{3r_s K^2_{gm-2}}{(1 + 2sr_s C_{gs} + r_s g_{m1})} \right) \times \frac{(1 + 3sr_s C_{gs})}{(1 + 3sr_s C_{gs} + r_s g_{m1}) g_{m1} \times (1 + sr_s C_{gs} + r_s g_{m1})^2} \right| . \qquad (4.24)$$

The source resistance r_s was set to a typical value (i.e. 2Ω). From equations (4.23) and (4.24), setting f= 5GHz, C_{gs} = 60fF, and W/L =50μm/0.18μm, we have $sr_s C_{gs} = 0.0037$ << 1. It can therefore be concluded that **increasing C_{gs} will almost have no effect on HD2 or HD3.** This statement was verified using HSPICE and Maple, for different transistor sizes and bias currents (Fig. 4.9). This suggests that it is possible to decrease the size of the input matching inductor of an LNA, while maintaining the same resonant fre-

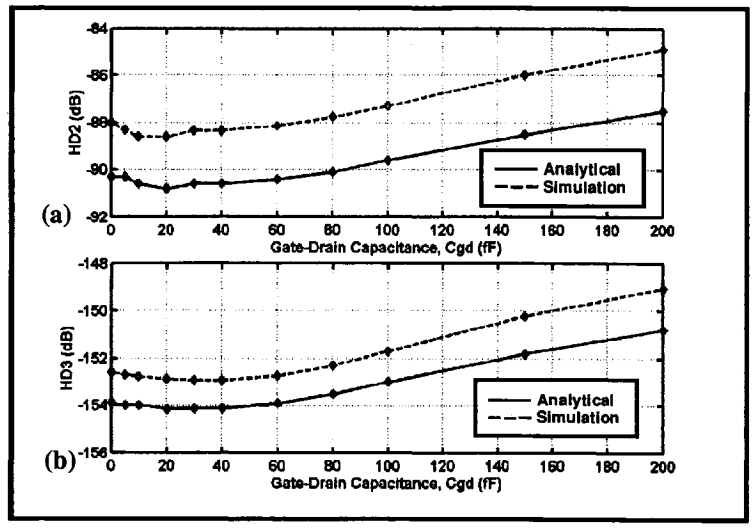

Figure 4.10 Effect of C_{gd}: Analytical and simulated distortions a) HD2, and b) HD3. [W/L = 50μm/0.18μm, R_{tank} = 300Ω].

quency at the input, by simply adding a capacitor in parallel with C_{gs} , all without affecting the linearity of the circuit. Figure 4.9 also suggests that C_{gs} has no impact on HD2 and HD3, for different transistor sizings and bias currents.

4.4.3 - Effects of Parasitic Capacitances C_{ds} and C_{gd} on Distortion

When considering C_{ds} alone, HD2 and HD3 were found to be:

$$HD2(s) = \left| \frac{1}{2} v_{in} \frac{K_{gm-2}(1 + sC_{ds}Z_{Tank})}{(1 + 2sC_{ds}Z_{Tank})g_{m1}} \right|, \tag{4.25}$$

$$HD3(s) = \left| \frac{1}{12} v^2_{in} \frac{K_{gm-3}(1 + sC_{ds}Z_{Tank})}{(1 + 3sC_{ds}Z_{Tank})g_{m1}} \right|. \tag{4.26}$$

Similar expressions were obtained for C_{gd} and are given by:

$$HD2(s) = \left| \frac{1}{2} v_{in} \frac{K_{gm-2}(1 + sC_{gd}Z_{Tank})}{(1 + 2sC_{gd}Z_{Tank})(sC_{gd} - g_{m1})} \right|, \tag{4.27}$$

$$HD3(s) = \left| \frac{1}{12} v^2_{in} \frac{K_{gm-3}(1 + sC_{gd}Z_{Tank})}{(1 + 3sC_{gd}Z_{Tank})(sC_{gd} - g_{m1})} \right|. \tag{4.28}$$

The term $(sC_{gd}-g_{m1})$ in the denominator of HD2(s) and of HD3(s) in the above equations represents the feedback that the parasitic capacitor C_{gd} introduces between the input and the output of a single-transistor LNA. As the sC_{gd} increases and gets closer in value to g_m, the term $(sC_{gd}-g_{m1})$ decreases, which results in an increase in the second and third-order distortions. Theoretically, the above equations imply that for a specific biasing condition, the distortion generated due to the feedback through C_{gd} can be infinite. However, when the transistor is operating in the saturation region, as generally is the case in LNA designs, the parasitic capacitor C_{gd} is mainly due to the lateral diffusion of the drain region below the gate's oxide, giving rise to an overlap region between them. This capacitor is linearly dependent on the width of the CMOS transistor and is given by $C_{gd} = WC_{ox}x_d$, where x_d is the width of the overlap. The value of this overlap is relatively small. For example, for a 100μm width 0.18μm length transistor, with frequencies up to 10GHz, the term sC_{gd} is always smaller than g_m. Therefore, practically, the distortion in RF LNAs due to C_{gd} is limited. Figure 4.10 suggests that the effect of C_{gd} on distortion is higher than that of C_{gs} (Fig. 4.9), but it remains relatively weak, compared to, for an example, the effect of g_m. **By varying C_{gd} from 0fF to 200fF, the distortion deteriorates only by about 4dB**.

4.4.4 - Effects of the Output Resistance r_0 and of the Source Resistance (r_S) on Distortion

The output resistance of the MOSFET transistor is modelled as r_o in Fig. 4.7. It is assumed linear, in order to keep the analysis simple [83]. It introduces a certain amount of distortion, since it creates a signal path between the source and the drain of the transistor [109]. Note that without including r_s in this analysis, r_o would appear between v_{out} and V_{dd}, in parallel with the tank impedance, and we would not be able to derive its parasitic effect on the circuit. In reality, the parasitic resistance r_s at the source of a MOSFET is typically around 2Ω. When considering r_o, HD2(s) and HD3(s) were found to be

$$HD2(s) = \left| -\frac{1}{2} v_{in} \frac{K_{gm-2}(Z_{Tank}(s) + r_o + r_s)^2}{(Z_{Tank}(s) + r_o + r_s + g_m r_s r_o)(Z_{Tank}(2s) + r_o + r_s + g_m r_s r_o)} \right| , \quad (4.29)$$

$$HD3(s) = \left| \frac{1}{8} v_{in}^2 \frac{K_{gm-3} G(2s) + K_{gm-2} r_s r_o}{G(s)^2 G(2s) G(3s)} (Z_{Tank}(s) + r_o + r_s)^3 \right| , \quad (4.30)$$

where

$$G(s) = Z_{Tank}(s) + r_o + r_s + g_m r_s r_o . \quad (4.31)$$

Analytical and simulation results demonstrating the effect of the output resistance are shown in Fig. 4.11. As expected, the distortion decreases when increasing the output resistance.

Taking only r_s into account, HD2 and HD3 are given by:

$$HD2(s) = \left| \frac{1}{2} v_{in} \frac{K_{gm-2}}{(1 + r_s g_{m1})^2 g_{m1}} \right| , \text{ and} \quad (4.32)$$

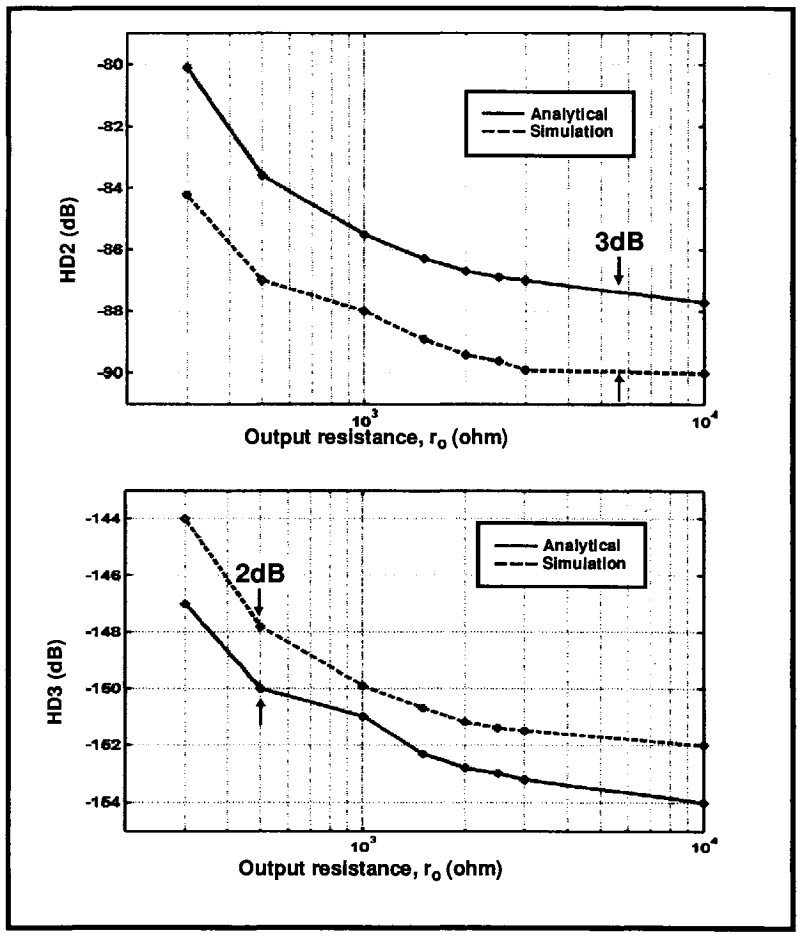

Figure 4.11 Analytical and simulated distortions: Effect of r_o a) HD2, and b) HD3. [W/L = 50μm/0.18μm, R_{tank} = 300Ω].

$$HD3(s) = \left| \frac{1}{24 g_{m1}} v_{in}^2 \left[\frac{2K_{gm-3}}{(1 + r_s g_{m1})^3} + \frac{3 r_s K^2_{gm-2}}{(1 + r_s g_{m1})^4} \right] \right| . \tag{4.33}$$

Equation (4.32) suggests that HD2 is almost inversely proportional to the square of the degeneration resistor r_s, while Eq. (4.33) shows an inversely proportional cubic relationship between HD3 and r_s. The LNA in Fig. 4.1-a was simulated with a bias current of 2mA and a gain of 15dB, while r_s was varied from 2Ω to 80Ω. As shown in Fig. 4.12, **a source resistance of only 20Ω can decrease HD2 and HD3 by 6dB and 10dB, respec-**

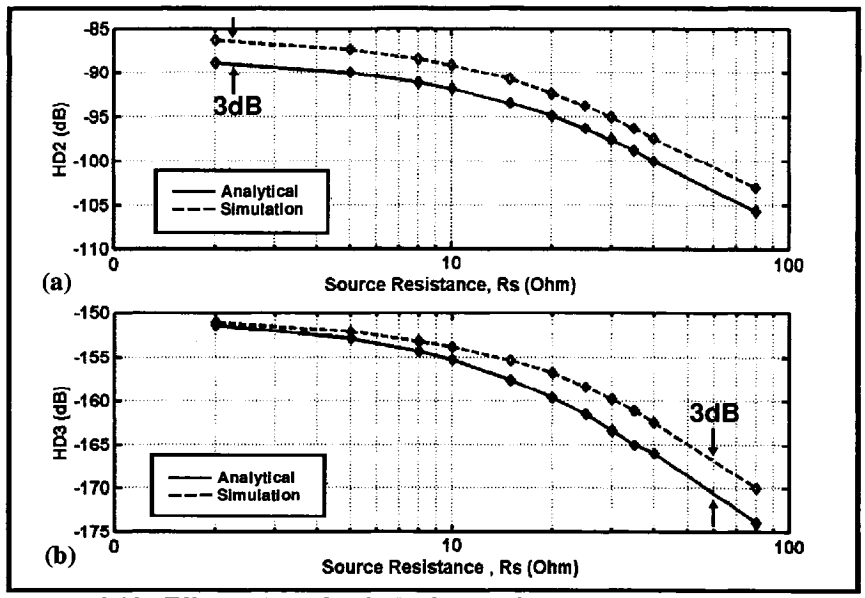

Figure 4.12 Effect of r_s: Analytical and simulated distortions a) HD2, and b) HD3. [W/L = 50μm/0.18μm, I_d = 2mA, R_{tank} = 300Ω].

tively. This asserts the common knowledge that, in a distortion-aware design, adding a degeneration impedance to the source of the input transistor significantly decreases distortion, since the latter is square/cubic inversely proportional to it. This can practically be achieved using a small resistor or inductor. While both elements will have the same effect in terms of distortion, inductors are invariably the elements of choice, due to their minimal effects on the noise figures of LNAs.

4.5 - Practical Considerations in Distortion-Aware LNA Designs

From the analysis presented earlier, it is possible to summarize the distortion-aware design guidelines for RF CMOS LNAs as follows:

1- **Select the smallest possible transistor which will provide the necessary g_m when biased at the highest possible overdrive voltage (V_{gs}-V_t):** A small transistor will minimize the effects of C_{ds} and C_{gd} (Section 4.4.3), while a large (V_{gs}-V_t) will decrease the distortion caused by g_m (Section 4.4.1).

2- **Add a capacitor in parallel with the C_{gs} of the input transistor:** This is to mitigate the use of a small transistor. The addition of C_{gs} would lower the input impedance and ease input matching, without having any effect on distortion (Section 4.4.2).

3- **Add a degeneration impedance to the source of the input transistor:** Only a small degeneration impedance will significantly decrease distortion, since the latter is square/cubic inversely proportional to it (Section 4.4.4).

To demonstrate the value of the above design considerations, three low-noise amplifiers were designed and simulated. Their respective parameters are shown in Fig. 4.13. They were chosen such that all circuits provide similar gains, using similar degeneration impedances and resonant LC tanks. However, the sizes of the transistors were varied. Similar gains were obtained by only tuning the gate to source voltage V_{gs}. For example, a 10dB gain was achieved by setting V_{gs} to 0.55V in Design 1, 0.5V in Design 2, and 0.475V in Design 3. To mitigate the use of small transistors while ensuring a reasonable size of the input matching inductor, a capacitor was added in parallel to C_{gs} for the LNAs with smaller transistor sizes (designs 1 and 2), such that similar S11 parameters were obtained for the three circuits. Fig. 4.14 shows the distortion behaviors in terms of IIP3 and OIP3 for the three amplifiers with respect to their gains. As it can be seen, for

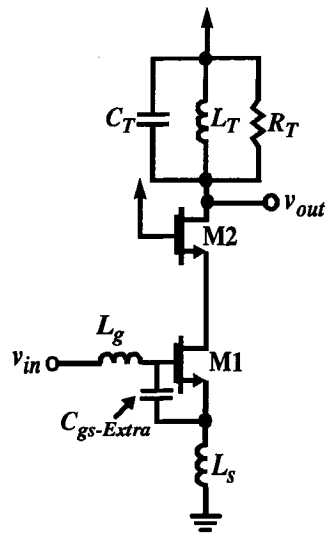

Table 4.1: Three LNA design parameters.

Parameter	Design 1	Design 2	Design 3
Tx size (µm/µm)	75 / 0.18	150 / 0.18	300 / 0.18
L_g (H)	2.5n	2.5n	1.8n
L_s (H)	0.3n	0.3n	0.3n
C_T (F)	650f	600f	550f
L_T (H)	1.5n	1.5n	1.5n
R_T (Ω)	125	125	125
$C_{gs\text{-}Extra}$ (F)	200f	100f	0
Gain (dB)	16	16	16
OIP3 (dBm)	14	4.5	-1.5
NF (dB)	1.8	2.3	2.5
V_{gs} (V)	0.7	0.55	0.5
Power consumption (mW)	9.8	7.2	5.8

Figure 4.13 Schematic of a cascode LNA with different design parameters, used to demonstrate the effect of different transistor sizings on distortion. Also shown, for a 16 dB gain, the OIP3, V_{gs}, the power consumption, and the NF.

all gain values, the distortion was minimum for the smallest transistors LNA (i.e. W = 75µm). For higher gains, even greater than 12dB, the smallest transistors amplifier surpassed the distortion performances of the other two designs (i.e. higher IIP3). With the gain set to 16dB, OIP3s of +14, +4.5 and -1.5 dBm were measured for the 75µm, 150µm, 300µm transistor widths, respectively. It should be noted that by using a small transistor, the 10dB enhancement in distortion came at the cost of increasing the overall power consumption to 9.8mW for the 75µm/0.18µm LNA, compared to 7.2mW and 5.8mW. These results demonstrate that, for a given acceptable LNA gain, the distortion can be minimized by using smaller transistors driven by large overdrive voltages while employing degeneration impedances, at a moderate increase of power consumption. Note that similar results were observed for the folded cascode LNA operating from a 1V power supply (Fig. 4.1-b).

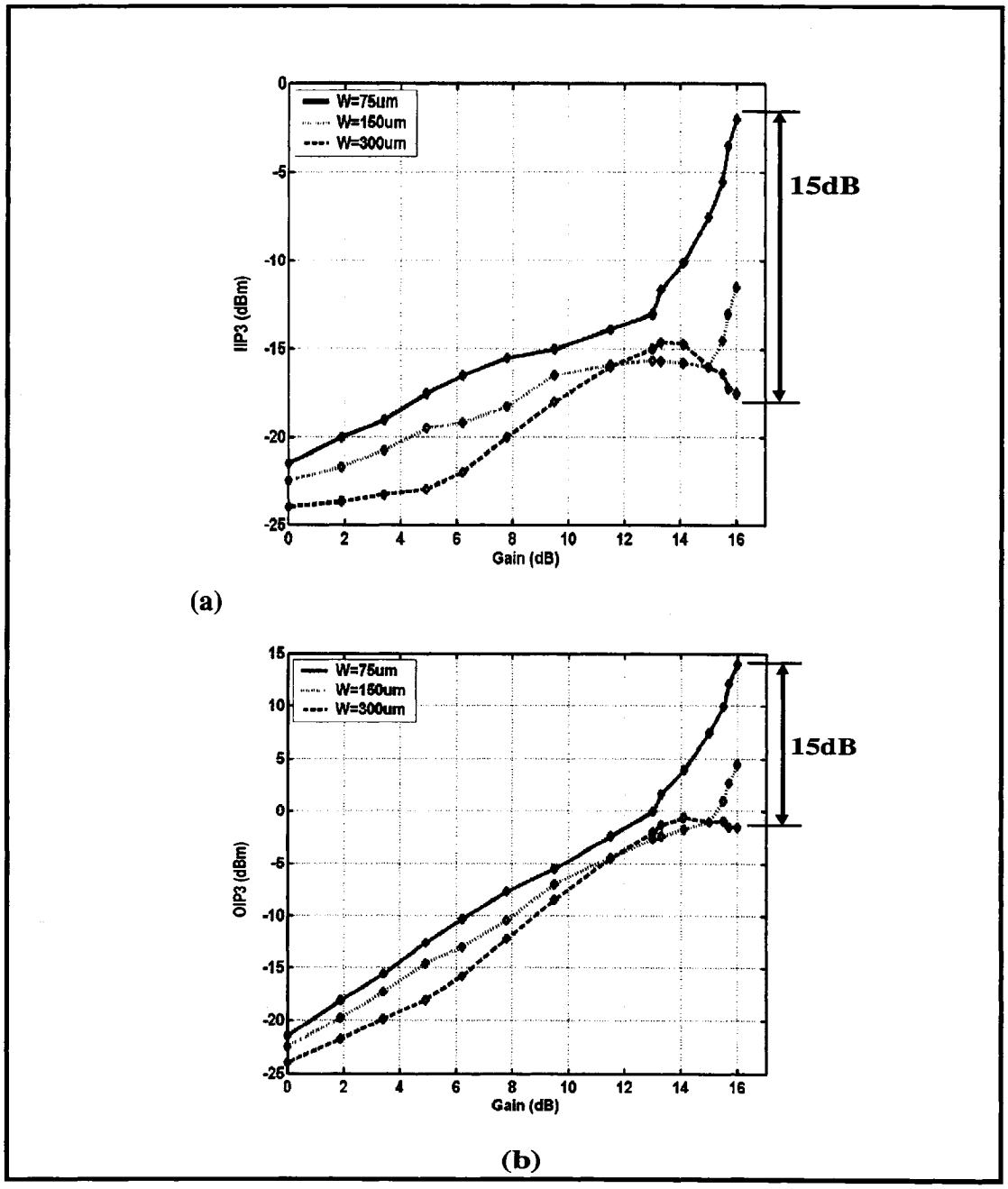

Figure 4.14 a) IIP3 and b) OIP3 for three LNAs with different transistor sizes. The smallest transistor consistently results in lower distortion (higher IP3).

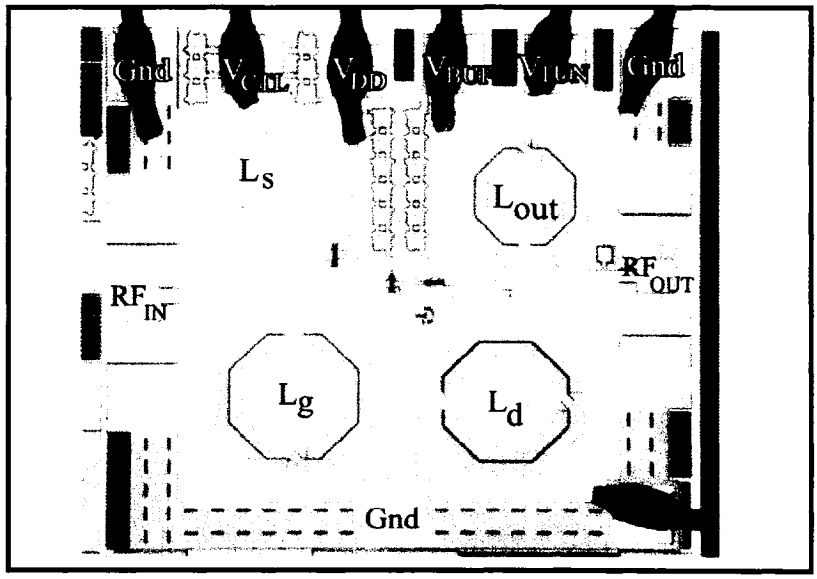

Figure 4.15 Photomicrograph of the folded cascode LNA [96].

4.6 - Experimental Results

The folded-cascode structure in Fig. 4.1-b was implemented in a standard CMOS 0.18μm process [96]. A specific layout implementation is shown in Fig. 4.15. It operates from a 1V power supply. The LNA exhibits a 13.2dB of gain at 5.8GHz. Including the output stage, the circuit consumes 22mW of power and has a noise figure of 2.5dB. The measured input and output reflection coefficients were less than -5 dB and -10 dB, respectively. The layout occupies $0.9mm^2$, including the bonding pads. Harmonic and intermodulation distortions were measured on wafer using Cascade GSG probes.

Figure 4.16 shows the measured and simulated results for HD2 and HD3, and compares them to the values computed analytically using Maple. For the simulations, HSPICE was used: a transient analysis was performed over 50 periods, and only the last period was considered to avoid transients. The second- and third-order harmonics were then estimated through post-processing using the FFT algorithm of Matlab. Coherent testing conditions were observed all along in order to ensure maximum accuracy.

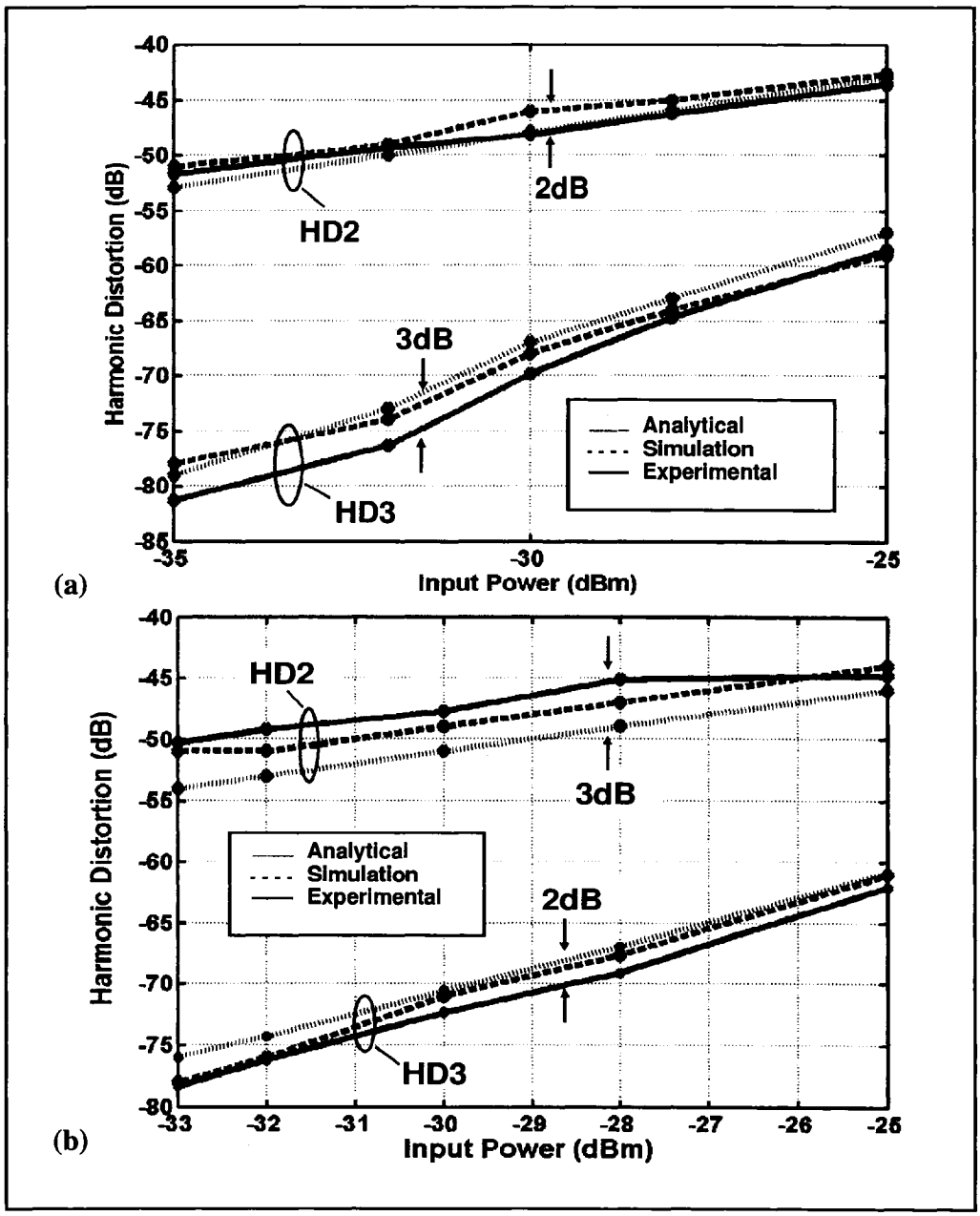

Figure 4.16 Comparisons of experimental, analytical, and simulation results of HD2 and HD3 of the 5.8GHz folded-cascode LNA with different bias currents of (a) I_d = 11.3mA, and (b) I_d = 5.8mA.

The analytical results were obtained by modeling the distortion following the approach described in Section 4.3 using Maple, while taking into account all of the CMOS transistor parameters affecting distortion. The validity of this analytical approach

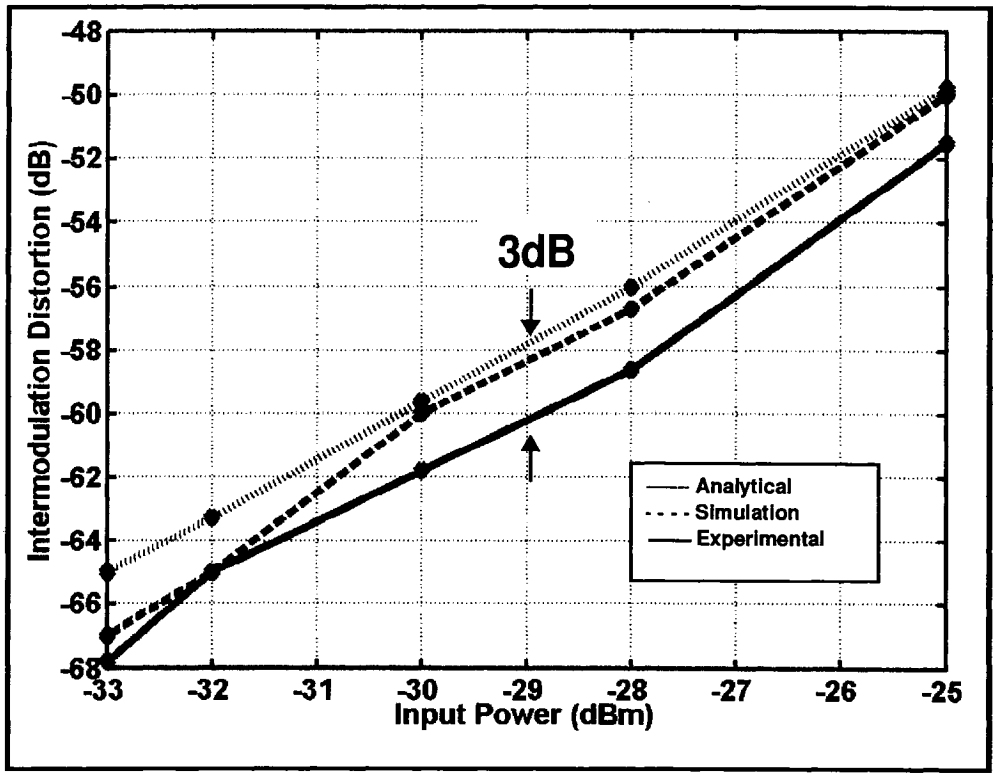

Figure 4.17 Experimental, analytical, and simulation results of the 5.8GHz LNA's 3rd-order intermodulation distortion.

is well demonstrated by the results in Fig. 4.16: the maximum deviation between the experimental, simulated, and analytical distortions, for two different biasing currents, namely $I_d = 11.3mA$ (Fig. 4.16.a) and $I_d = 5.8mA$ (Fig. 4.16.b), is 3dB. Also, a good agreement regarding trends and slopes between all corresponding curves is evident.

Finally, Fig. 4.17 compares the in-band third-order intermodulation distortion obtained from measurements and simulations to the analytical results computed by Maple. Once again, the good agreement between all curves supports the validity of the entire analysis procedure proposed in this chapter.

4.7 - Conclusion

Nonlinearity equations in terms of Volterra's series have been derived, allowing the investigation of the distortion in short-channel CMOS RF LNAs. Closed-form and frequency-dependent equations describing distortion were derived and compared to simulation and experimental results. Simple practical design considerations were suggested and verified by comparing the distortion behavior of three LNA setups. Results showed that the distortion is lowered for LNA designs using smaller transistors while operating with larger overdrive voltages, without impacting much the power consumption. To the best of our knowledge, this is the first time this design approach is proposed and demonstrated along with simple closed-form equations demonstrating the effect of C_{gs} on distortion in LNAs.

Chapter 5 - Miscellaneous Circuits

This chapter summarizes research work that was conducted at different stages over the span of the last three years. Namely, the design of low-voltage, low-glitch phase locked loops (PLL) and the implementation of differential image reject filters. Initially, we considered the use of a PLL to automatically tune a notch filter. The complexity of the system, and the several design issues that we faced, prompted us to consider a more simple approach, which resulted in the two-notch implementation proposed earlier in Chapter 3. Extending the work presented in Chapter 3 to a differential implementation is a natural progression of this research. The feasibility and performance of a differential system is addressed in this chapter as well.

Over the last decade, PLLs have been successfully integrated in a variety of technologies, e.g. bipolar, SiGe, MESFET, and CMOS, with frequencies of operation from the mega-Hertz to the giga-Hertz ranges [68]-[74]. Shown in Fig. 5.1-a, a PLL system generates a sinusoidal output signal with its frequency directly related to the difference of phase/frequency between a feedback signal (f_{fb}) and an incoming reference signal (f_{ref}). The difference in phase/frequency between the two signals is detected by a phase/frequency detector (PFD). The PFD produces two outputs denoted by UP and DN in Fig. 5.1. The three possible states of the PFD are shown Fig. 5.1-b. Depending on the state produced, the charge pump (CP) generates a DC voltage. This DC signal controls the frequency of operation of the voltage controlled oscillator (VCO). Accordingly, a

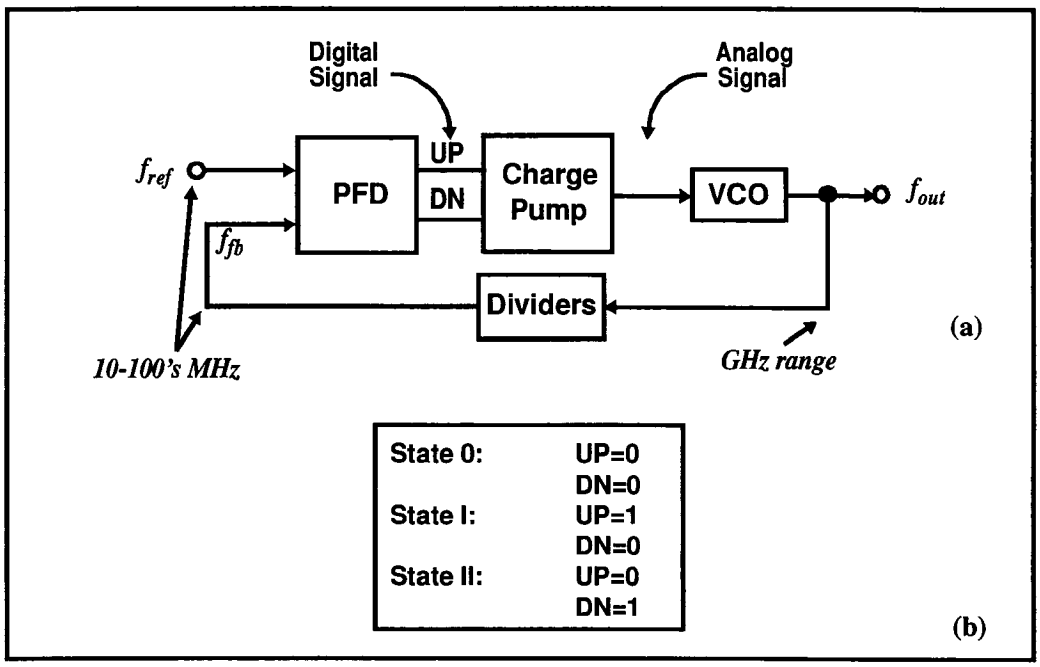

Figure 5.1 a) Charge-pump based PLL. b) States of the PFD.

reference signal with a frequency f_{out} is produced at the output of the VCO. After being processed by a frequency divider, this signal is fedback to the PFD, and is compared again to the reference signal.

The implementation of integrated PLL charge pump circuits faces many challenges. Decreasing clock feedthrough from the charge pump to the local VCO is a crucial issue [68]. Obtaining a large output voltage range, while operating from a low power supply, is another interesting research issue [112].

In this chapter, the feasibility of implementing a charge pump (CP) capable of operating from a very low voltage supply, with ***minimum glitching*** is demonstrated. As previously mentioned, the CP converts the digital output of the PFD to a stable analog output voltage. Any spike in this voltage produces undesirable spurious tones in the VCO output signal. The proposed charge pump operates from a 1V power supply, with 60μW power dissipation, and does not suffer from the common spurious jump phenomenon [76]. Section 5.1.1 begins with an overview of charge pump circuits. Section 5.1.2

discusses the evolution of the proposed topology. Simulation results are presented in Sections 5.1.3. General challenges in PLL designs are discussed in Section 5.1.4.

Differential implementations of CMOS notch filters are also investigated in this chapter. In Section 5.2, an overview of differential CMOS image reject filters is provided. Two novel differential CMOS multi-GHz IR filters are then presented.

5.1 - A New 1 V CMOS Charge Pump

5.1.1 - Overview of Charge Pumps

Figure 5.2-a shows the conceptual model of a charge pump, along with the three possible states of the PFD outputs. The charge pump employs two current sources, which are connected to capacitor C through switches S1 and S2. For state I, when UP is high and DN is low, switch S1 conducts and S2 is open, allowing the current I_{up} to charge the capacitor, and therefore raising the voltage V_C. In state II, when DN is high and UP is low, switch S2 connects C to the current source I_{dn}, which results in discharging the output voltage V_C. In state 0, both switches are open, and the voltage V_C, ideally, remains constant.

The conventional charge pump circuit shown in Fig. 5.2-a has many limitations. For example, when the PFD output switches to state 0, the voltage at capacitor C is left floating, while the voltages at the sources of S1 and S2 are rapidly pulled to VDD and ground, respectively. Due to the non-ideal characteristics of the MOS switch, such as charge injection and clock feedthrough, this rapid change in the source voltages creates glitches in the capacitor current, which can result in a jump in the stored voltage V_C. Any jump in V_C adds undesirable spurious tones and phase noise to the output signal of the VCO.

A possible approach, used to mitigate this problem, consists of adding an op-amp, connected as shown in Fig. 5.2-b, to the conventional charge pump circuit [75]. The feedback amplifier stabilizes the voltages at nodes 1 and 2, preventing the voltage jump

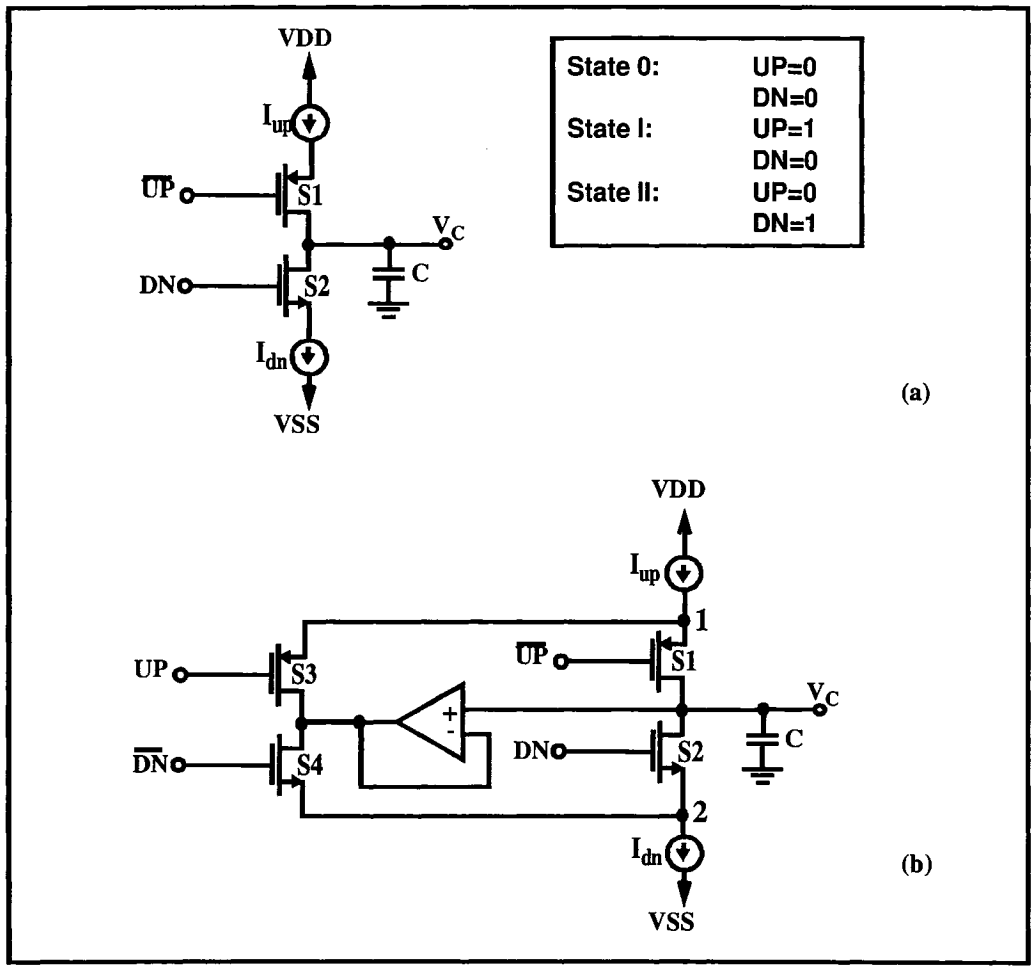

Figure 5.2 a) Schematic of the conventional charge pump, along with the three possible PFD states. b) Improved charge pump.

phenomenon at *C* to occur. Enhancing the performance of the charge pump using this method comes at the expense of extra complexity, area, and power consumption.

Different novel charge pump circuits with a reduced jump phenomenon were recently proposed in [76]-[78]. Their supply voltages were 1.5, 2V, and 3.3V, respectively.

5.1.2 - Proposed Architecture

To implement a very low voltage charge pump, we start by designing and testing a low-voltage switched push-current source, as shown in Fig. 5.3. It operates from a 1V

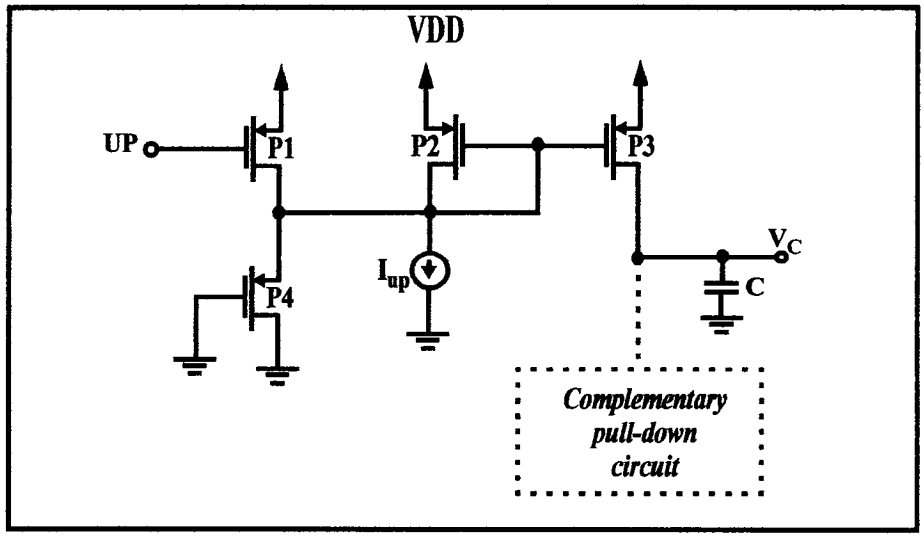

Figure 5.3 Proposed switched push-current source.

power supply as follow:

1-When the signal UP is at a high logical level:

i- Transistor P1 is OFF, and the current I_{up} is steered to transistor P2.

ii- Since the power supply is 1V, when transistor P2 is ON, transistor P4 will not have enough voltage headroom between its gate and source to be ON.

iii- Since transistors P2 and P3 form a current mirror, a current I_{up} will be pushed into the capacitor C, raising the voltage V_C. For current matching purposes, P2 and P3 are made relatively large.

2-When the signal UP is at logical zero:

i - Transistors P1 and P4 turn ON.

ii - The current in P2, and therefore P3, will be negligible. The voltage at the capacitor should, ideally, remain stable.

For the proposed structure, the minimum power supply that can be used is given by

$$VDD = V_{SG-P2} + V_{SAT}, \tag{5.1}$$

where V_{SG-P2} is the source to gate voltage of transistor P2. By simulating the circuit in Fig. 5.3 using HSPICE, it was observed that the switching speeds of the PMOS

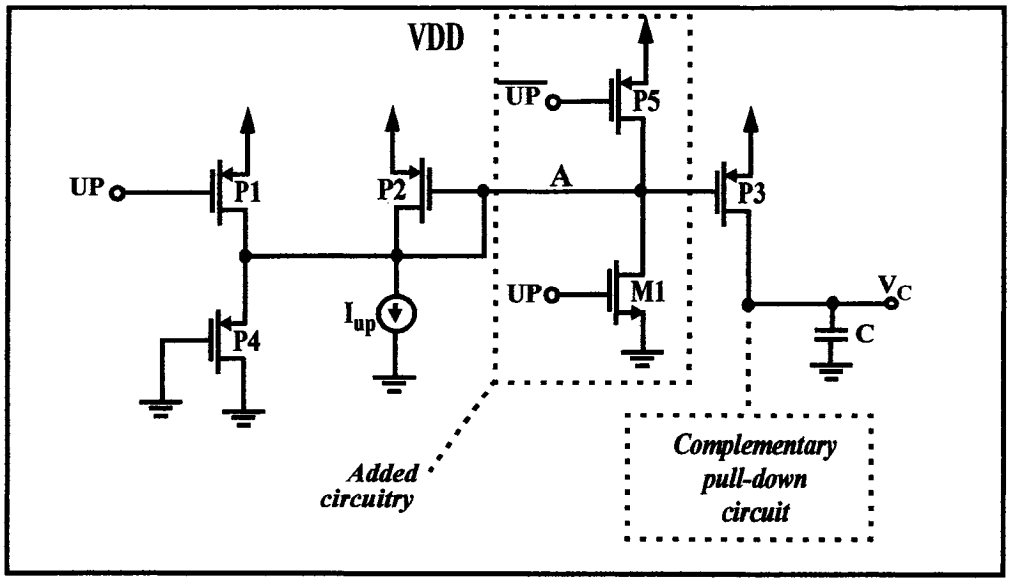

Figure 5.4 Schematic of the improved switched current source. Transistors P5 and M1 speed up switching at A.

transistors were the limiting factors of the overall speed of the circuit: when the UP signal is switched from 0 to 1, the charging time of transistor P2 is relatively long, which results in a slow switching speed at the gate of P3. To overcome this problem, transistors P5 and M1 (Fig. 5.4) are inserted at the gate of transistor P3. With the addition of these transistors, as the UP signal switches from 0 to 1, the voltage at the gate of P3 is rapidly pulled down, turning ON transistor P3 in a shorter time. Note that the voltage at node A is set by transistor P2. Therefore, when P2 is on, the voltage at the gate of P2 forces transistor P5 to operate in the saturation region, which means that P5 behaves as a current source, and not as a switch.

To carry the same currents, transistors M1 and P5 have to be perfectly matched. When they are both ON, they operate in the saturation region. Since, in the CMOS 0.18μm technology, the electrons mobility is approximately three times that of the holes, the size of P5 was chosen to be 3.2 times the size of M1 to ensure current matching. Moreover, in order not to add extra parasitic capacitances at node A, the sizes of M1 and P5 were minimized. A comparison of the switching speeds of the voltage at the gate of P3 for the circuits in Figs. 5.3 and 5.4 is demonstrated in Fig. 5.5

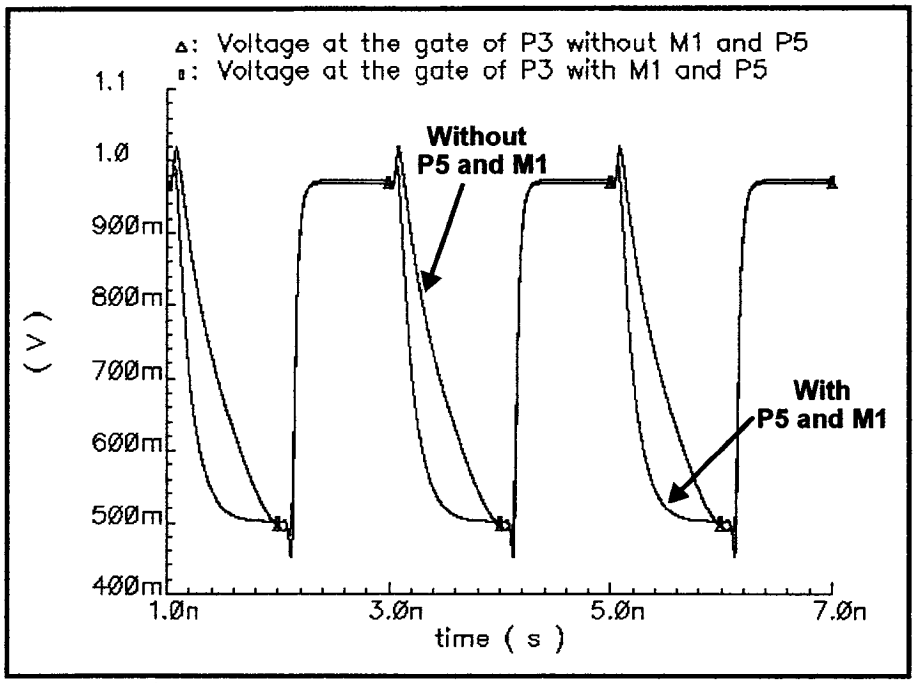

Figure 5.5 The voltage at the gate of transistor P3 switches faster when M1 and P5 are added.

For the circuit in Fig. 5.4, glitches due to charge sharing with P3 will appear at the output capacitor (Fig. 5.6-a). To eliminate this problem, the circuit was modified as shown in Fig. 5.7. The additional buffer stage acts as a small delay element: It ensures the switching of transistor P3 before transistor P6 by a certain period of time, t_d (Fig. 5.6). During t_d, any glitches generated by transistor P3 will not be transferred to the capacitor. Also, the added parasitic capacitances of transistor P6 in the current path, along with capacitor C_d, cause the glitches in the output current to be further attenuated. Figures 5.6-a and 5.6-b show the current in the output capacitor with and without the extra buffer stage, when the frequency of the input UP signal equals 500MHz. As evident from the figure, with the added delay buffer, the current in the capacitor has almost no glitches. Note that only transistors P2 and P3 need to operate in the saturation region, in order to behave as a current mirror. All other transistors are allowed to go into triode, enabling operation from a very low voltage headroom.

The circuit in Fig. 5.7 performs the pull-up function (i.e. the function of S1 in Fig. 5.2-a). For pull-down, an identical complementary circuit is used.

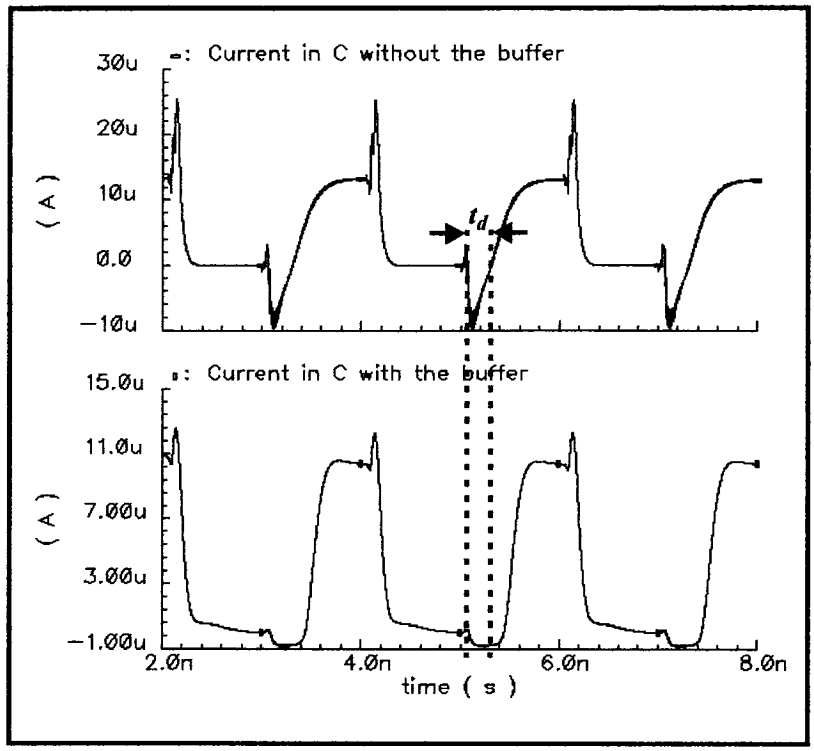

Figure 5.6 Current in capacitor C a) without the buffer in Fig. 5.7, and b) with the buffer, for a 500MHz signal.

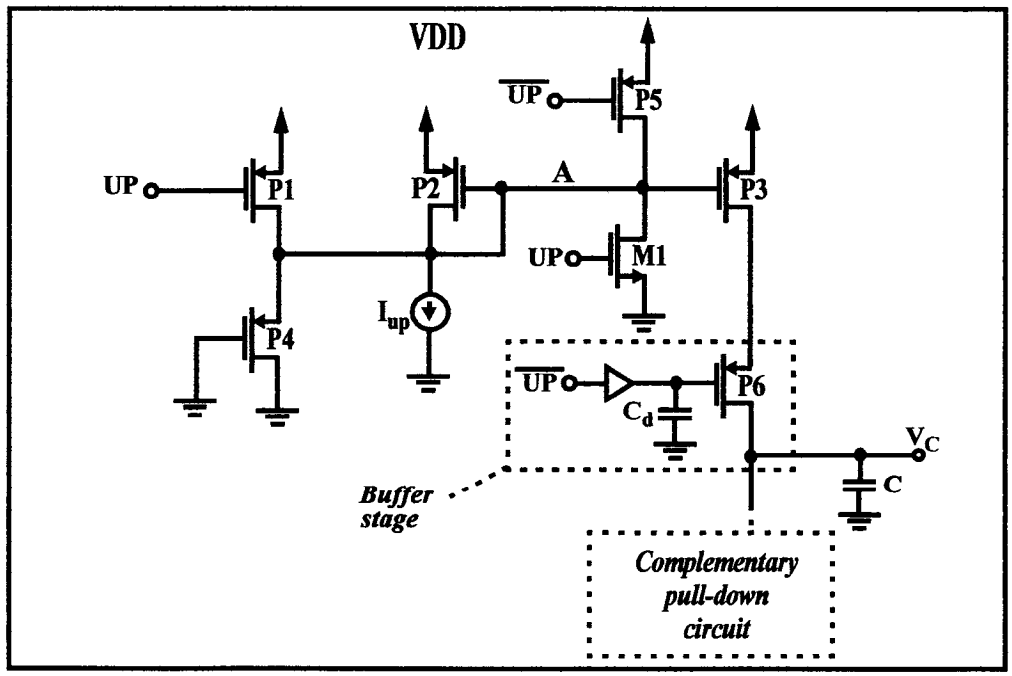

Figure 5.7 Final structure of the proposed charge pump. The extra buffer stage results in considerable reduction of the output glitches.

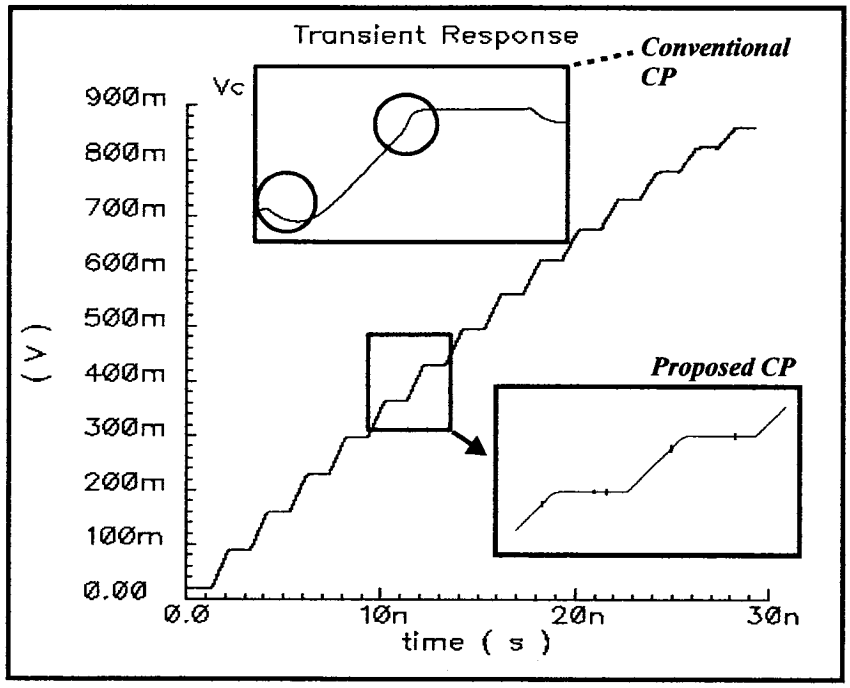

Figure 5.8 Pumping up the output voltage.

5.1.3 - Simulation Results

The proposed charge pump was designed using a 0.18μm CMOS process. All results reported are with a 1V power supply. Simulations were done using HSPICE, with device models from TSMC. The pull-up current I_{up} and the pull-down current I_{dn} were set to 10μA.

Figure 5.8 shows the pumping up of the circuit. The 900mV maximum output voltage, along with the stable (jump free) voltage steps, are demonstrated and compared to the output voltage from a conventional charge pump. For the pump-down circuit, the results are shown in Fig. 5.9. Finally, the circuit was simulated with the temperature varying from 0o to 100°C. A maximum deviation of 0.056V was observed in the output voltage, as shown in Fig. 5.10. The average power consumption of the circuit is 60μW.

5.1.4 - Challenges in PLL Systems

In the previous section, a novel charge pump circuit, optimized for very low

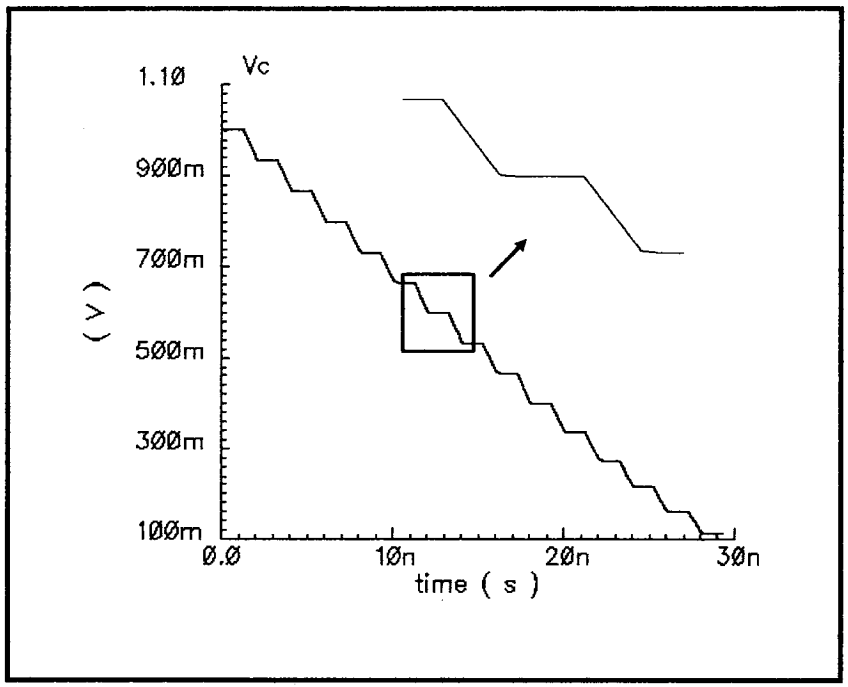

Figure 5.9 Pumping down the output voltage.

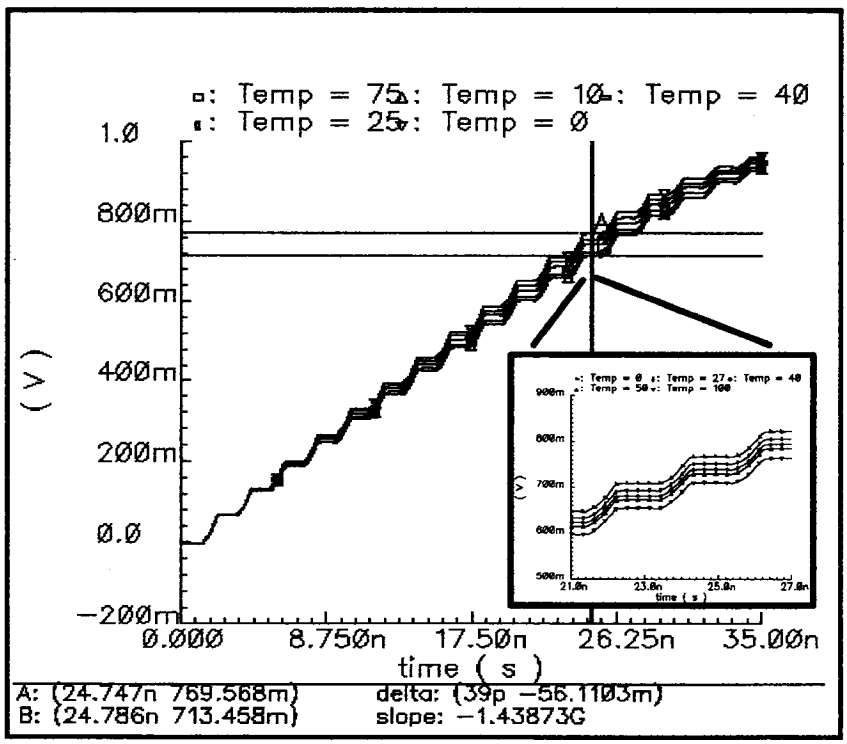

Figure 5.10 Maximum deviation of the output voltage with the temperature ranging from 0 to 100°C.

voltage PLLs, was presented. The requirements on the frequency divider, the VCO, and the PFD are even more stringent. For example, the performance of a PLL depends greatly on the bias current and on temperature variations, which affect the tuning of the VCO. As a result, PLL calibration techniques might be required, which further complicate the overall design. With the 802.11a WLAN standard, the subchannel separation is 20MHz, which imposes very stringent frequency specifications and phase noise requirements on the PLL and on the VCO.

The power consumption in PLL systems is yet another critical issue. As much as 200mW may be required for the PLL system alone [113]. To the best of our knowledge, at 5GHz, the smallest power consumption reported for a CMOS frequency synthesizer system is 13.5mW [114]. Therefore, even though CMOS PLLs have been successfully integrated at multi-GHz frequencies, avoiding using them, as it was done in this thesis for wireless receiver front-ends, is an attractive line of thought, since the power consumption, the complexity, and the chip area can be greatly reduced.

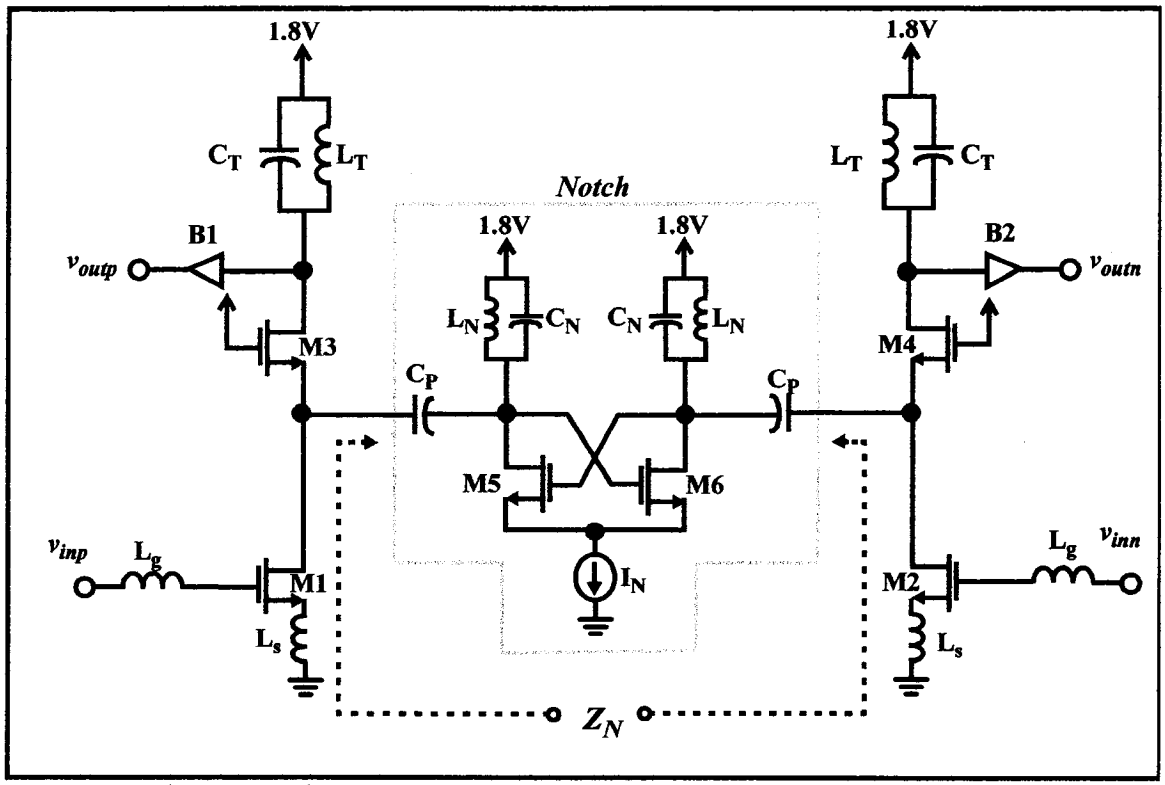

Figure 5.11 Structure of the LNA image reject filter proposed in [61] implemented in CMOS.

5.2 - CMOS Differential LNA-Notch Combination

It is well known that differential circuits are more robust, benefit from common mode rejection, and suppress second-order harmonics. Fig. 5.11 shows a differential LNA-notch combination circuit proposed in [61]. As discussed in Section 2.2.2, a negative resistance is formed by the cross-coupled pair (transistors M5 and M6) for inductors Q-enhancement - a topology commonly used in voltage controlled oscillators. Stability issues of the notch filter become of primary concern. The notch is formed by M5-M6, C_N, C_P, and L_N. The input impedance Z_N of the notch circuit is given by

$$Z_N = \frac{L_N(C_P + C_N)s^2 + 1}{L_N C_N C_P s^3 + C_s s}. \tag{5.2}$$

In the midband of the LNA, the impedance Z_N looking into capacitors C_P is larger than $1/g_{m3}$ and $1/g_{m4}$, therefore not affecting the behavior of the amplifier. At the resonant

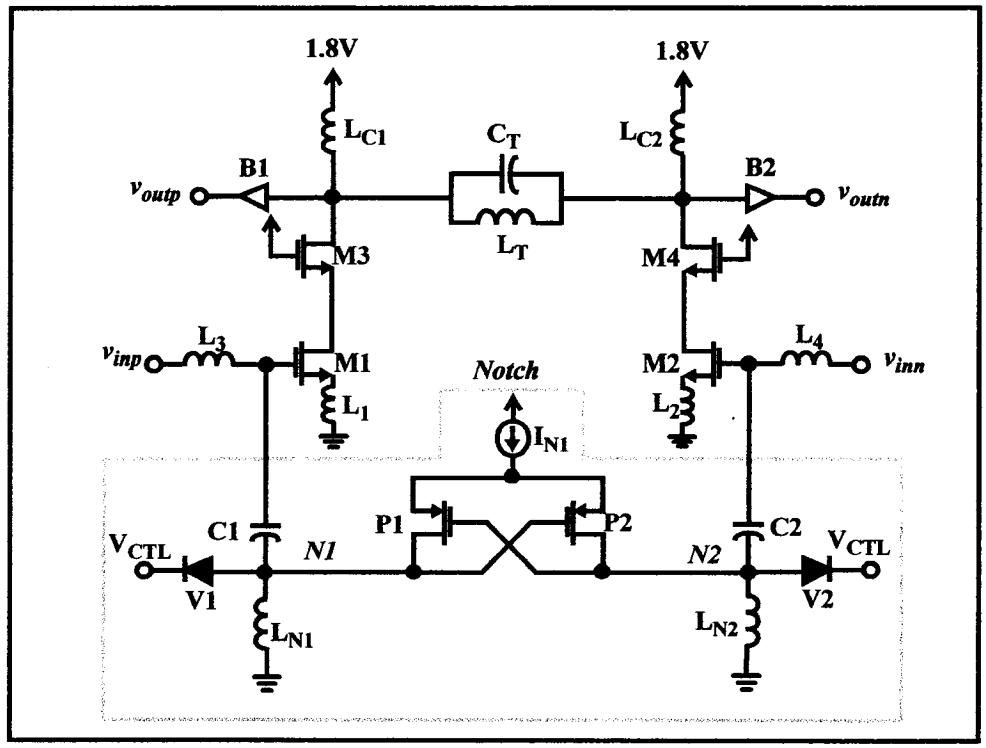

Figure 5.12 Structure of the LNA-PMOS image reject filter [40].

frequency of the notch filter, Z_N becomes low. This results in steering the RF current away from transistors M3 and M4, thus rejecting the AC signal at the output. This circuit generated 50dB of image rejection at 950MHz in CMOS [61].

5.2.1 - Differential Cascode LNA-PMOS Notch Combination Circuit

Knowing that PMOS devices produce less noise compared to NMOS transistors, the circuit in Fig. 5.11 was modified to the one shown in Fig. 5.12, in which the notch filter was implemented using PMOS transistors [37]. This notch has a similar function as that of the circuit shown in Fig. 5.11. However, the filter is now connected at the gates of the input transistors of the LNA. The inductor tank L_T is differentially excited to improve its quality factor. The frequency of the LNA was set to 6.5GHz.

Capacitors *C1* and *C2*, along with the two varactors *V1* and *V2*, and inductors L_{N1} and L_{N2} implement the notch filter. Their sizes were chosen such that the combination of

V1/V2, *C1/C2* and the parasitic transistors capacitances of P1/P2 and inductors L_{N1}/L_{N2} provides a notch tuning range from 10.5 to 11GHz, set by the total capacitance of the varactors at nodes N1 and N2. When the absolute values of the reactances of the capacitances at N1 and N2 are equal to the reactances of inductors L_{N1} and L_{N2} respectively, low impedance connections to ground are thus created. This results in rejecting the AC signal at the input ports of the LNA, and therefore obtaining a notch filter. The cross-coupled pair PMOS transistors P1 and P2 provides the negative resistance that compensates for the on-chip inductor losses.

In the frequency band around 6.5GHz, the impedance seen at the input ports of the notch filter is relatively large, which means that the circuit operates like an LNA with inductor degeneration. The effect of the notch is observed at much higher frequencies, and therefore can be neglected when designing the input matching circuit.

The notching frequency tuning varactors were implemented as PMOS transistors, by shorting the substrate to the drain and to the source. This results in PN junction-based varactors. The gate lengths of the PMOS transistors were minimized to reduce their effective resistances.

The scattering S-parameters were estimated using the Spectre RF simulator. Figure 5.13-a shows the +12dB LNA gain, along with the gain tunability obtained by varying the bias currents of M1 and M2. The input and output reflection coefficients, S11 and S22, are below -10dB at 6.5GHz (Figure 5.13-b). By simultaneously varying the biasing currents in the Q-enhancement circuit and the voltages across varactors V1 and V2, tuning of the notching frequency is obtained, as demonstrated in Fig. 5.14. The power consumption of the circuit and the noise figure are 22mW and 2.4dB, for a +12dB LNA gain and a -50dB image rejection. The performance of this circuit is summarized in Table 5.1.

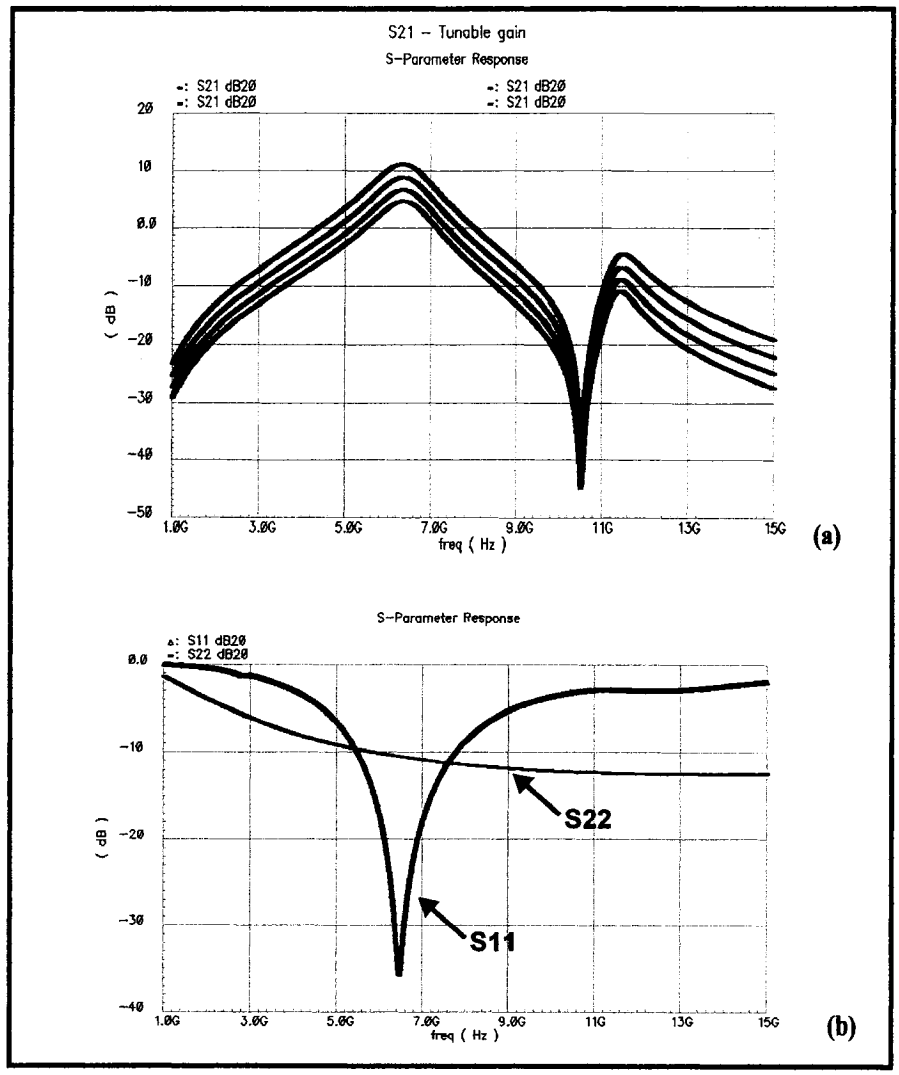

Figure 5.13 a) Simulated S21 showing the gain tunability of the LNA. b) The S11 and S22 parameters showing input and output matching.

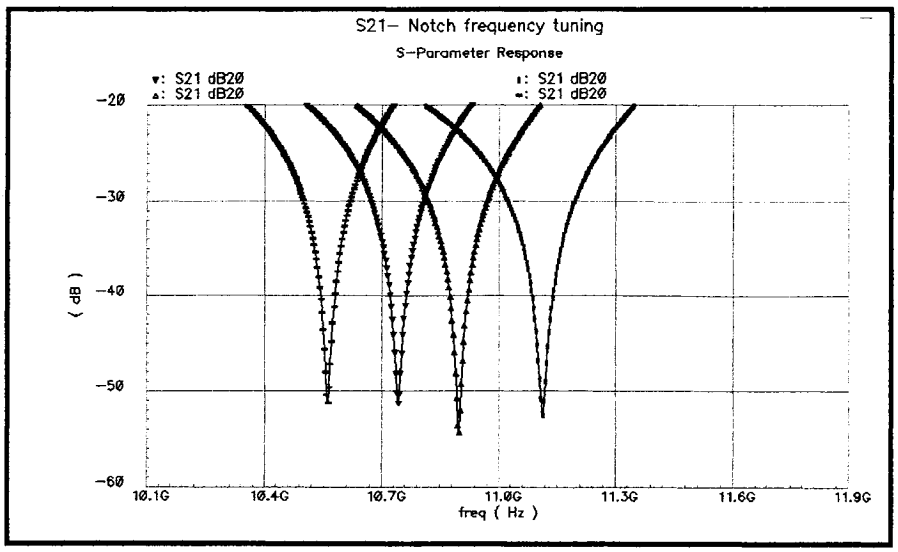

Figure 5.14 Tuning of the notch frequency response (600MHz).

Table 5.1: Summary of the simulated performance of the circuit proposed in Fig. 5.12.

Technology	**CMOS 0.18μm**
f_o - LNA	**6.5GHz**
LNA gain	**12dB**
S11 @6.5GHz	**-35dB**
S22@6.5GHz	**-10dB**
NF @ 6.5GHz	**4.4dB**
f_o - Notch	**10.5-11.1GHz**
Maximum image rejection	**-50dB**
VDD	**1.8V**
Power consumption	**22mW**
IIP3	**-12.5dBm**

5.2.2 - Differential Very Low Voltage LNA-Notch Combination Circuit

Growing consumer demand for smaller, lighter and cheaper wireless products is driving engineers to investigate new technologies and to enhance the performance of existing ones. The continuous down scaling of deep-submicron technologies imposes a reduction in the supply voltage of the analog, RF, and digital circuits in portable devices. A possible approach to reduce the supply voltage in LNAs is to use a folded-cascode topology (Fig. 5.15). As it can be seen in the figure, a maximum of one transistor and a current source are stacked between the power supply and ground. As a result, a supply voltage as low as 1V can be used. A notch filter, operating from a 1V supply voltage as well, is connected to the LNA (Fig. 5.15-b). This notch has a similar function as that of the circuits shown in Fig. 5.11 and Fig. 5.12.

The small-signal equivalent circuit of the notch filter is shown in Fig. 5.16, where the cross-coupled pair is replaced by $R_{Neg} = -2/g_m$. R_L is the series parasitic resistance of L_N. Analyzing the circuit, the input impedance of the notch is found to be

$$Z_N = \frac{2(sC_N(R_L + sL_N) + 2 - sL_N g_m - R_L g_m)}{sC_N(2 - sL_N g_m - R_L g_m)}, \tag{5.3}$$

where $g_m = g_{m5} = g_{m6}$.

The magnitude of Z_N is plotted versus frequency in Fig. 5.17. As demonstrated in the figure, by varying capacitor C_N, the frequency of the notch can be set. Keeping the notching frequency constant while varying the transconductance of transistors M5 and M6 results in changing the input impedance Z_N (Fig. 5.17-b), thus tuning the depth of the filter's notch. As it can be seen in the figure, a zero $|Z_N|$ can be achieved theoretically by properly biasing the cross-coupled pair, resulting in an infinite notch depth. In reality, due to parasitic capacitances and resistances, the image rejection is limited to -58dB.

The image reject filter must always be stable, which means that the gain of the

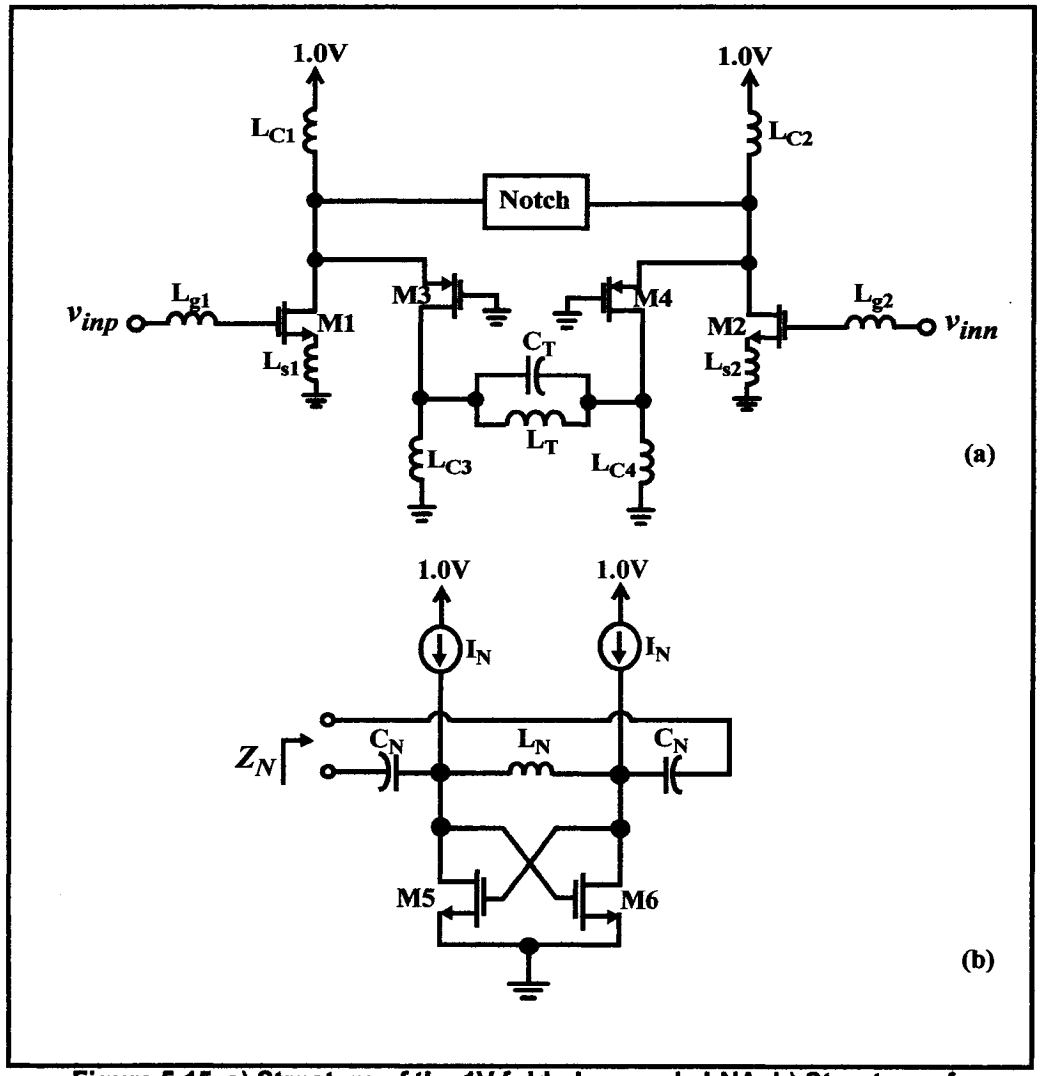

Figure 5.15 a) Structure of the 1V folded cascode LNA. b) Structure of the 1V image reject filter [39].

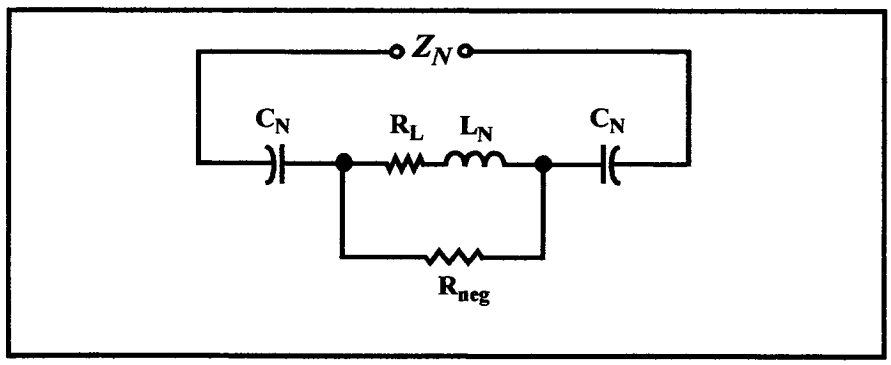

Figure 5.16 Simple model of the notch filter of Fig. 5.15.

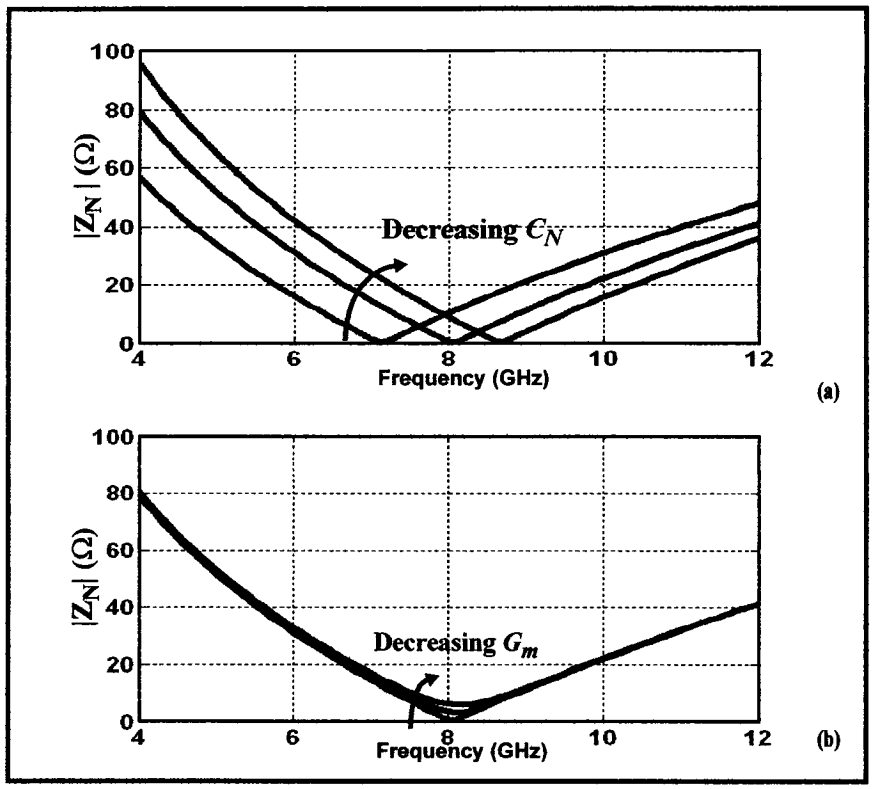

Figure 5.17 Tuning of Z_N by varying (a) C_N to set the frequency, and b) g_m to set the rejection.

cross-coupled pair should not exceed a certain level. We found that it was possible to obtain infinite Q-notch depth without compromising stability. Assume that the cross-coupled pair is biased such that the negative resistance produced equals in magnitude the resistive loss of the notch resonant tank. In that case, the source input impedances of transistors M3 and M4 ($1/g_{m3}$ and $1/g_{m4}$, respectively) would ensure the circuit stability, by providing damping. The gain of the cross-coupled pair should not be increased much beyond this biasing point, otherwise oscillation might occur.

The proposed circuit was implemented using a standard CMOS 0.18μm gate length process. The sizes of the transistors and of the inductors used are shown in Table 5.2.

Table 5.2: Sizes of the transistors and inductors for the folded-cascode LNA-IR filter of Fig. 5.15.

Transistors M1 - M4	**200μm/0.18μm**
Transistors M5 - M6	**50μm/0.18μm**
L_N	**1nH**
C_N	**PMOS varactors**
L_T	**1.3nH**
L_{s1}, L_{s2}	**0.15nH**
L_{g1}, L_{g2}	**2.3nH**
L_{C1}, L_{C2}, L_{C3}, and L_{C4}	**3nH**

Figure 5.18 shows a 13dB LNA gain at 5.8GHz, along with the gain tunability obtained by varying the bias currents of M1 and M2. Figure 5.19-a shows the notch depth tunability. As it can be seen in the figure, the notch depth can be tuned by varying the biasing current of the filter, i.e. by varying I_N. A maximum notch depth of -58dB is

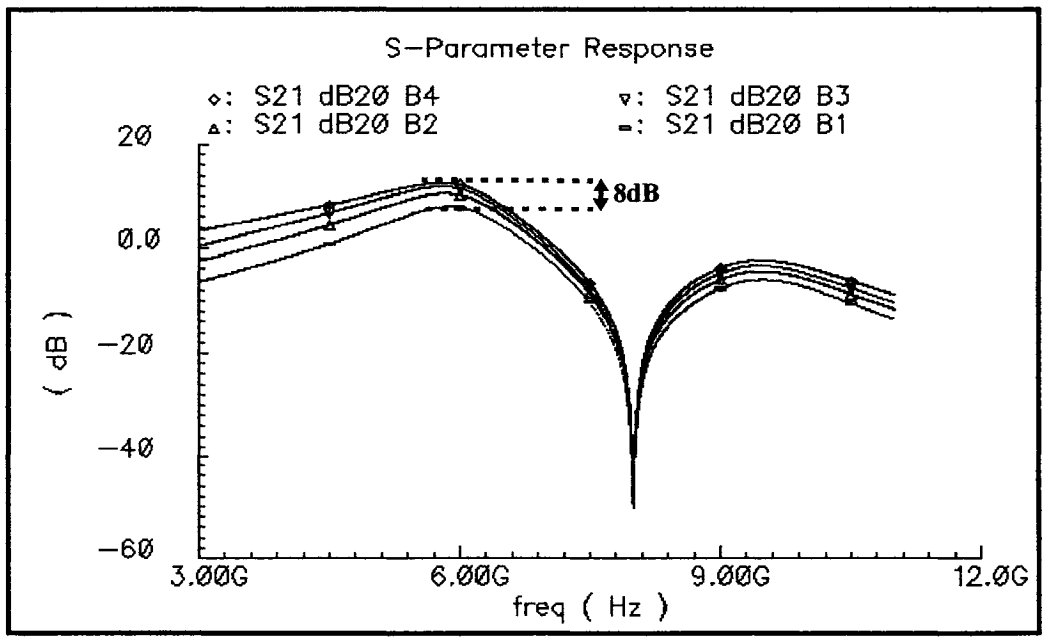

Figure 5.18 S21 parameter showing gain tunability of the LNA.

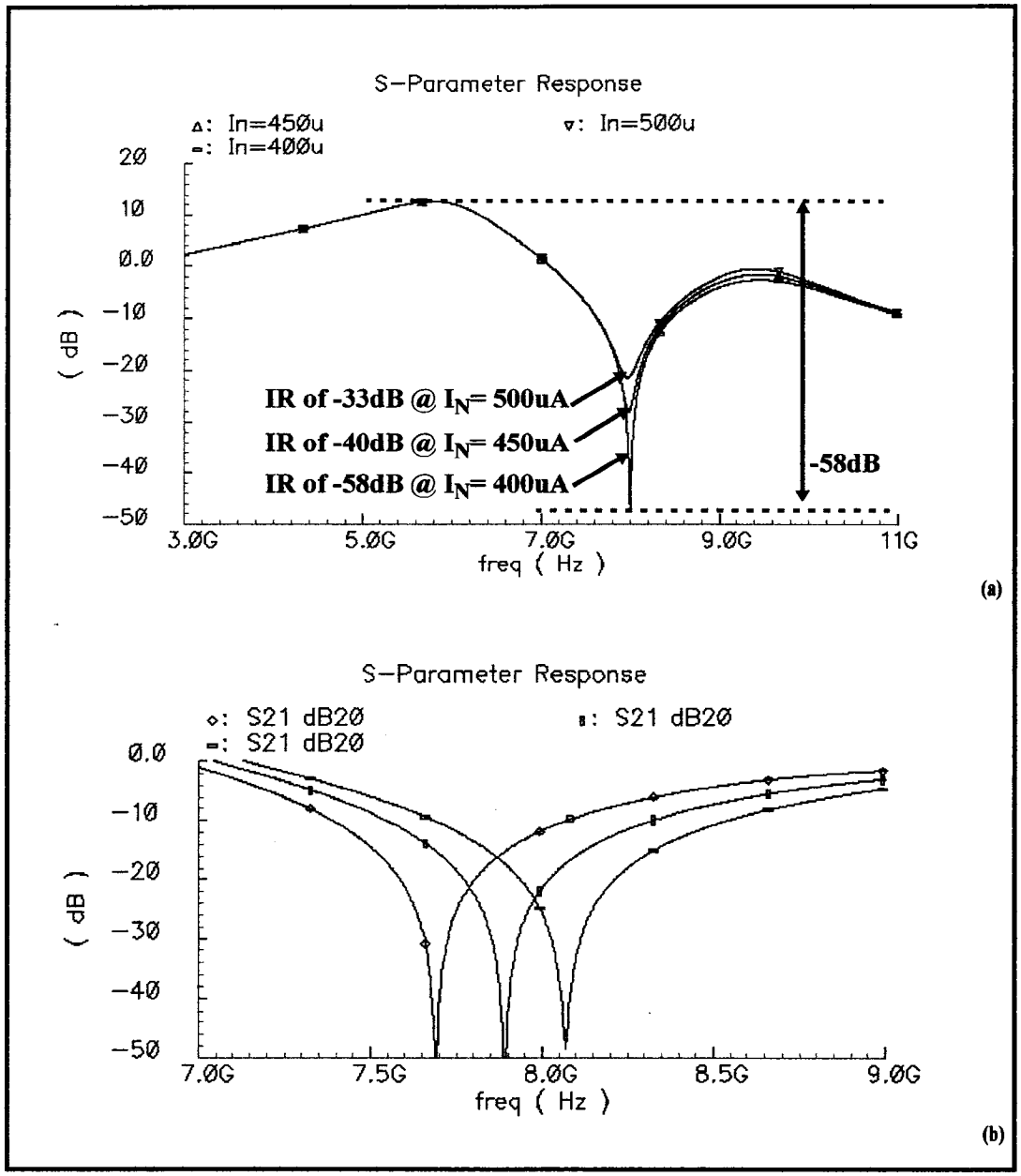

Figure 5.19 a) Tuning the notch depth. b) Tuning the notch frequency, for the 1V circuit in Fig. 5.15.

obtained, when the notch filter is biased at 400μA. Under this biasing current, the power consumption of the filter is 0.8mW only. It is interesting to note that the filter remained stabled and provided sufficient image rejection, even when it was biased with higher currents. This demonstrates an earlier argument that the biasing of the cross-coupled pair could be increased above the current required for infinite IR, before instability occurs.

Table 5.3: Summary of performance of the 1V circuit proposed in Fig. 5.15.

Technology	CMOS 0.18μm
f_o - LNA	5.8GHz
LNA gain	13dB
S11 @5.8GHz	-14dB
S22@5.8GHz	-15dB
NF @ 5.8GHz	4.2dB
f_o - Notch	8.0GHz
Maximum image rejection	-58dB
VDD	1.0V
Power consumption of the notch @ -58dB of IR	0.8mW
IIP3	-13dBm

The frequency of the IR filter can be made tunable by replacing one of the C_N capacitors by a PMOS varactor (Fig. 5.19-b). Table 5.3 summarizes the LNA-notch circuit performance.

5.3 - Conclusion

A low-voltage, low-glitch charge pump was designed when investigating the possibility of designing very-low voltage PLLs for automatic filter tuning. The chapter concluded with a the presentation of two novel differential CMOS multi-GHz IR filter implementations, one of them designed for very low-voltage operation.

Chapter 6 - Conclusion

6.1 - Summary

We presented a new notch filter topology combined with a low noise amplifier. Experimental results demonstrated the feasibility of obtaining 62dB of image rejection at 7.3GHz in a standard CMOS technology, along with an LNA exhibiting 15.8dB of gain at 5.8GHz. Stability analysis of the proposed notch circuit was presented, and the conditions for stability were derived. Comparisons to other recently reported image reject filters in the literature are shown in Fig. 6.1. It is interesting to note that the frequency of operation reported here is almost double that of state-of-the-art CMOS implementations, with a higher image rejection of -62dB at 7.5GHz in this work compared to- 50dB at 2.2GHz in [60].

A new approach for implementing 5GHz front-end heterodyne receivers was proposed. A simple and robust implementation of on-chip image rejection, based on the cascade of two slightly offset image reject filters, was implemented and tested. The circuit does not require on-chip automatic circuits nor off-chip components. The LNA and double IRF front-end demonstrated more than 30dB of IR over a 400MHz bandwidth centered at 7.4GHz in a standard CMOS technology. These experimental results showed that the specifications for the IEEE 802.11a WLAN standard can be met using a standard CMOS technology.

Nonlinearity equations in terms of Volterra's series have also been derived,

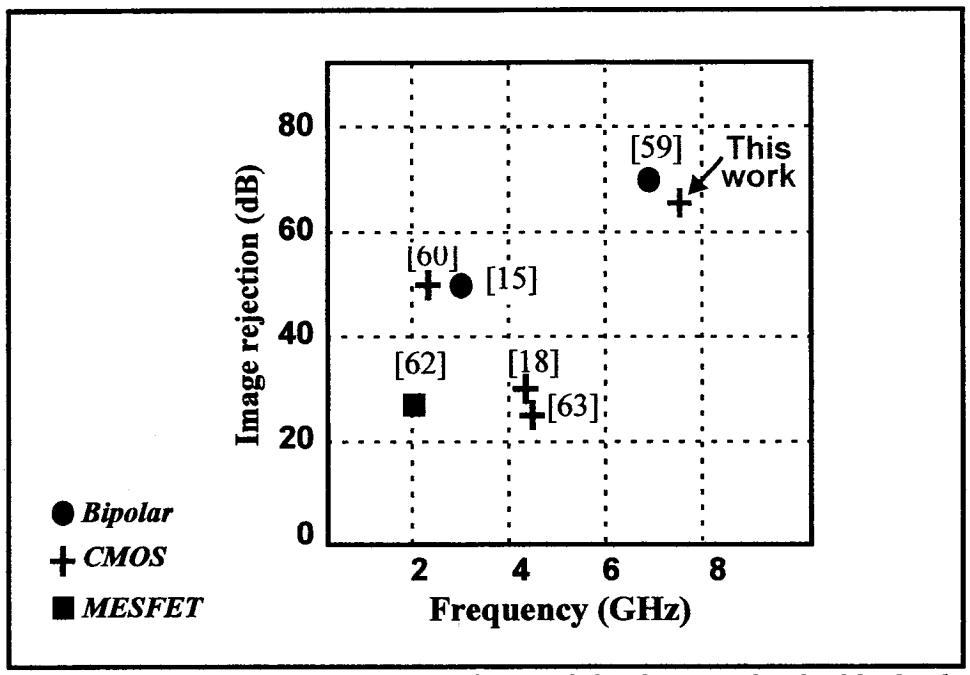

Figure 6.1 a) Comparison between the notch implementation in this thesis and state-of-the-art implementations.

allowing the investigation of the distortion in short-channel RF CMOS LNAs. Closed-form and frequency-dependent equations describing distortion were derived and compared to simulation and experimental results. Simple practical design considerations were suggested and verified by comparing the distortion behavior of three LNA setups. Results showed that the distortion is lowered for LNA designs using smaller transistors while operating with larger overdrive voltages, without impacting much the power consumption. To the best of our knowledge, this is the first time this design approach is proposed and demonstrated, along with simple closed-form equations demonstrating the effect of C_{gs} on distortion in LNAs.

6.2 - Topics for Future Research

This thesis presented several circuit innovations circuits and ideas: i) A new IRF circuit that has minimal effect on the gain of the preceding LNA was proposed. ii) Tuning the sharpness of the proposed IRF is simple and practical. iii) We demonstrated that the IRF circuit is unconditionally stable for all practical settings of its Q-factor. iv) We

proposed a front-end architecture that enables the realization of a large image rejection bandwidth. v) We provided design guidelines for optimizing the distortion behavior in CMOS LNAs. The following is a list of proposed future research topics:

1. **Distortion analysis:** With respect to the distortion analysis, the distortion-aware guidelines proposed throughout the text shall be verified experimentally. This can be done by integrating the LNAs analyzed in Section 4.5, and experimentally measuring their distortion responses.

2- **Distortion and IR filters**: Design techniques for optimizing distortion in RF LNAs were suggested in this thesis. It will be interesting to see if these design guidelines apply for the IR filters proposed in Chapter 3.

3. **Differential IR filters:** The maximum frequency of a CMOS differential image reject filter reported to date is around 4.2GHz, with an IR less than 30dB [18]. Therefore, the differential multi-giga-Hertz CMOS IR filters proposed in Chapter 5 shall be integrated and tested. The challenges that will be faced are many. First, there is a limited access to differential RF equipment operating at high frequencies (above 5GHz). Moreover, generating differential signals to test differential circuits is a complicated task at multi-GHz frequencies. Differential transformers with cut-off frequencies above 5GHz are not readily available. One way of producing differential signals consists of implementing off-chip baluns. At RF frequencies, the parasitics have a significant effect on the overall circuit performance. Designing perfectly symmetrical layouts for the integration of the differential notch filters is a great challenge.

4- **MEMS IR filters**: Recently, high-Q varactors and resonators (e.g. [115]-[116]) were successfully used in RF applications, such as in LNAs and in VCOs [117]-[118]. The Q-factors of MEMS components can be much higher than the Q-factors of passive devices integrated in standard CMOS technologies. Therefore, using MEMS components along with CMOS active devices to integrate IR filters may result in very efficient circuits, and shall be

investigated.

5- **Double IR receiver:** The double IR receiver architecture shall be integrated and tested in an entire heterodyne receiver, i.e. with active mixers, voltage controlled oscillators, ADCs, etc.

Appendix A - Receivers Architectures

RF circuit designers are facing an increasing demand for low-cost and small size circuits. Many efforts are ongoing on the integration of RF receivers in low-cost CMOS technologies. Fully integrated 5GHz RF receivers have recently been implemented in a variety of technologies and architectures, e.g. [3]-[26]. For a fully integrated heterodyne system, many problems such as on-chip image rejection still need to be addressed. Homodyne and low-IF receivers do not suffer from image-rejection. However, *1/f* noise and DC offsets can degrade the overall performance of a receiver and increase its complexity.

This appendix briefly describes homodyne, low-IF, and digital receiver architectures.

A.1 - Homodyne Receivers

Figure A.1 shows the basic structure of a homodyne receiver. In this scheme, the RF signal is directly downconverted by the mixer to DC. As a result, the image signal is the same as the RF signal, and this type of architecture does not suffer from the image problem. Moreover, since the downconverted signal lands at very low frequencies, the

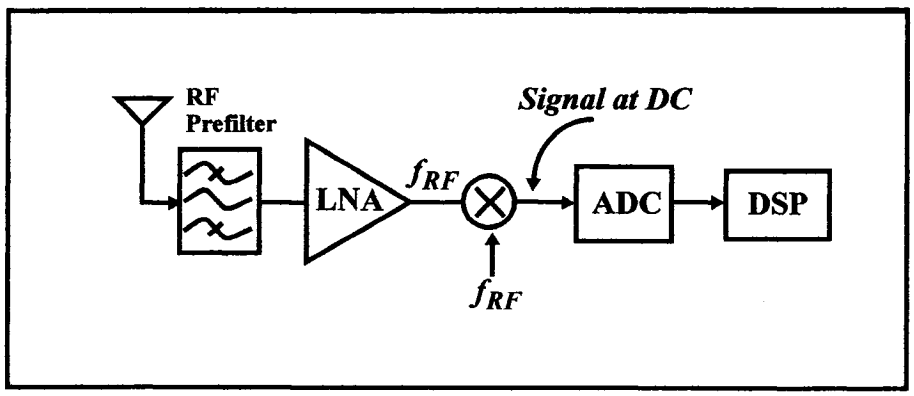

Figure A.1 Structure of a homodyne receiver.

digital processing circuits can operate at very low speeds.

On one hand, the simplicity of this structure makes it an attractive solution. On the other hand, it is not a very popular scheme for RF systems integrated on-chip, because it is inherently sensitive to DC and low-frequency beat signals. First, mixer leakage, self-mixing of the LO signal, and of strong interferers can generate DC offsets. The latter can saturate subsequent circuits due to their high gain. As a result, DC offset cancellation circuits are required. Second, homodyne receivers employ quadrature mixing. Mismatches between the I and Q signals affect the downconverted signal. Finally, the performance of homodyne receivers is severely affected by even-order distortions and *1/f* noise. The noise limitations of homodyne receivers can be mitigated by employing architectures with a low intermediate frequency (IF), such as the Weaver architecture or the Hartley topology.

A.2 - The Weaver Architecture

Shown in Figure A.2, the Weaver receiver exploits the fact that the image and the desired signal are out of phase after downconversion. Therefore, by downconverting the detected RF signal through two different paths using a set of quadrature mixers, cancellation of the image signal can be realized. This architecture is less sensitive to DC offsets, LO leakage and 1/f noise. This technique would offer a suitable solution for implementing 5GHz front-end receivers, if perfect gain and phase matching in the

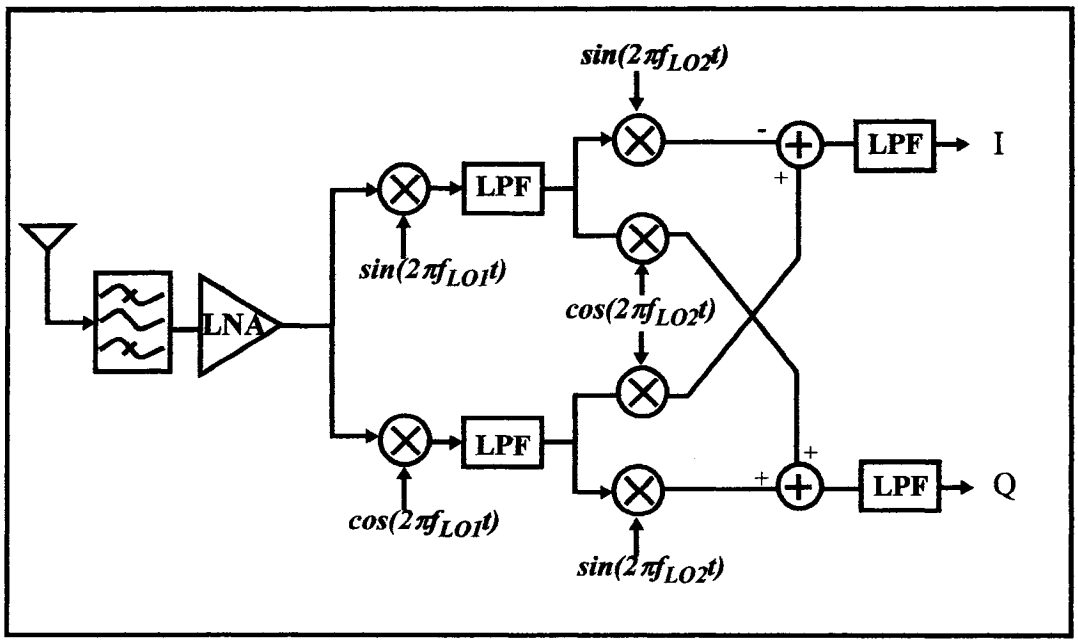

Figure A.2 Quadrature Weaver architecture.

quadrature outputs could be achieved. The image rejection ratio (IRR) for this architecture is given by

$$IRR \approx \frac{4}{\theta^2 + \varepsilon^2}, \tag{A.1}$$

where θ is the fractional gain mismatch, and ε is the phase matching error in radians between the RF signal paths in the receiver chain. For example, a θ of 0.1% and an ε of 1° limit the IRR to 41dB, which might not be sufficient for many wireless applications. At 5GHz, due to increasing parasitic effects, large phase and gain mismatches can easily occur. As reported in [18], a CMOS Weaver architecture practically achieves between 25 to 35 dB image rejection.

This architecture also suffers from a secondary image problem. The problem is illustrated in Fig. A.3. Suppose a signal appears at the frequency $2f_{LO1} + 2f_{LO2} - f_{RF}$, alongside the RF signal, at the input of the first mixer. The image signal is first translated to $f_{LO1} + 2f_{LO2} - f_{RF}$ after the first downconversion. Since this image signal falls at a

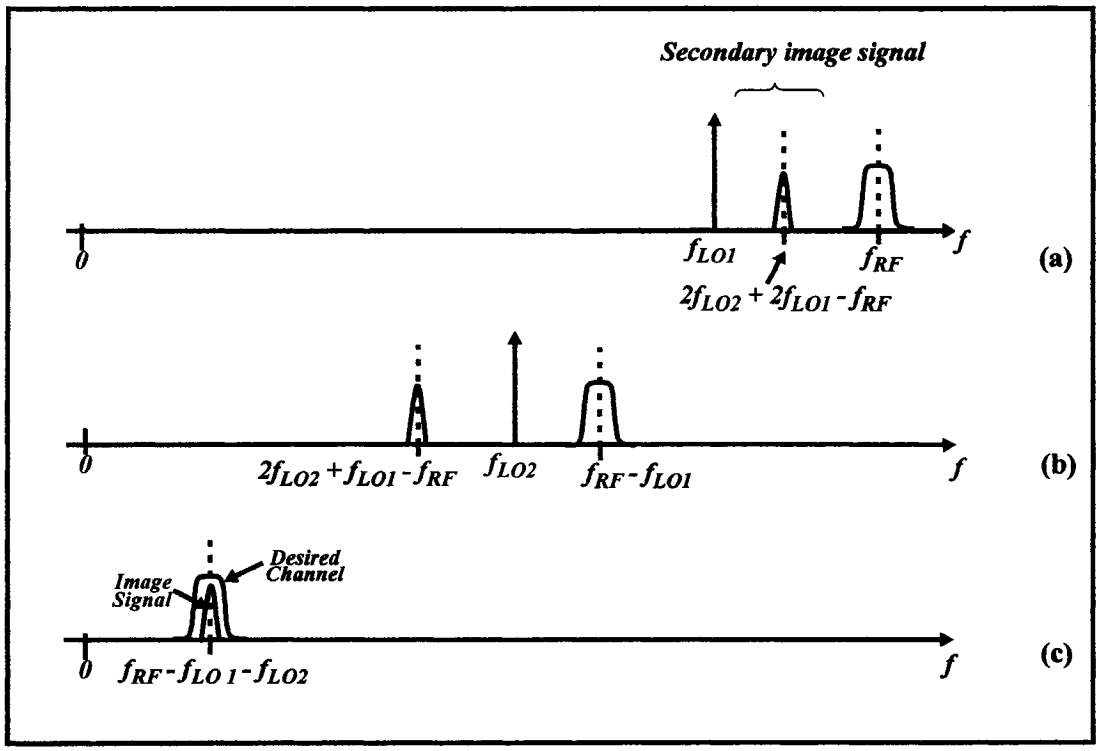

Figure A.3 Secondary image problem in Weaver receivers.

frequency lower than the downconverted RF signal (Fig. A.3-b), it is not rejected by the low pass filter. Therefore, after the second downconversion, it falls in the same frequency band as the desired channel, as shown in Fig. A.3-c. An image reject filter or a high-Q selective bandpass filter are needed to suppress this image signal.

A.3 - The Hartley Architecture

Shown in Fig. A.4, the image-reject downconverter is yet another implementation of an IF homodyne receiver. The RF signal is first mixed with a quadrature phase local oscillator. Low-pass filtering is then performed to remove the high frequency terms. To see how image rejection is obtained, assume that the signal at the LNA output is of the form

$$x_A(t) = x(t)e^{j2\pi f_{RF}} + x_{IM}(t)e^{-j2\pi f_{IM}}, \qquad \text{(A.2)}$$

where $x(t)$ is the desired RF amplified signal, and $x_{IM}(t)$ represents the image signal.

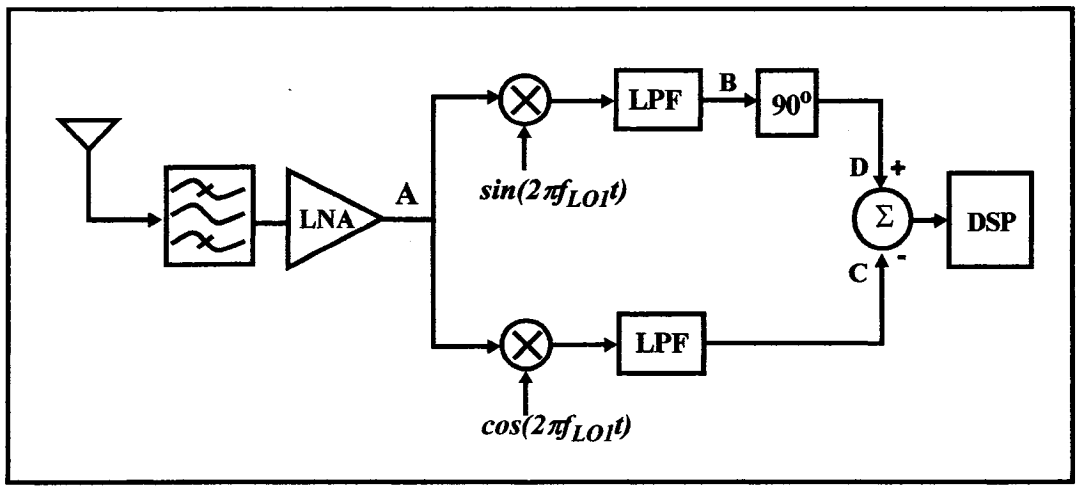

Figure A.4 An image-reject mixer based architecture: The Hartley architecture.

After the quadrature downconversions, the signals at nodes B and C are given by

$$x_B(t) = \frac{1}{2}x(t)e^{j2\pi f_{if}} + \frac{1}{2}x_{IM}(t)e^{-j2\pi f_{if}}, \tag{A.3}$$

$$x_C(t) = -\frac{1}{2j}x(t)e^{j2\pi f_{if}} - \frac{1}{2j}x_{IM}(t)e^{-j2\pi f_{if}}, \tag{A.4}$$

where $f_{if} = f_{LO} - f_{RF}$. The signal at node B is shifted by 90°. At node D, it becomes

$$x_D(t) = \frac{1}{2}x(t)e^{j2\pi f_{if}} - \frac{1}{2}x_{IM}(t)e^{-j2\pi f_{if}}. \tag{A.5}$$

At the output of the summer, the image signals cancel each other out, and the resulting IF signal is given by

$$x_{IF}(t) = x(t)e^{j2\pi f_{if}}. \tag{A.6}$$

As a result, image rejection is obtained. The major drawback of this architecture relies on the fact that it uses a constant gain broadband 90° phase shifter, which is typically hard to implement, especially in CMOS at 5GHz. Also, the phase shifter exhibits a significant amount of loss and noise, which affects the overall performance of the receiver. For this architecture, the IRR is also given by Eqn. (A.1), which means that, the image rejection is

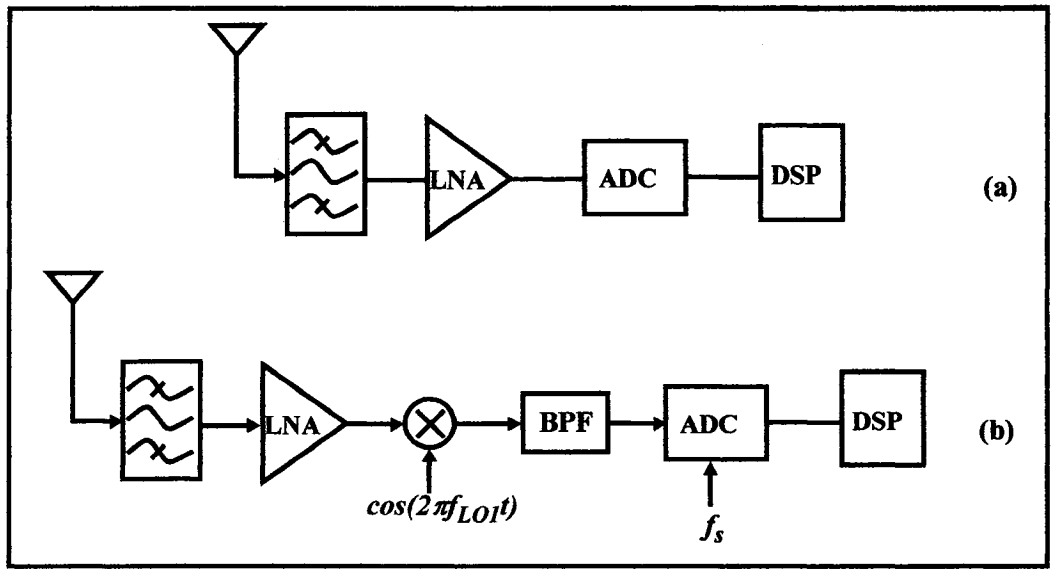

Figure A.5 a) Structure of a digital RF receiver. b) Structure of a digital IF receiver.

mainly dependent on the phase and gain mismatches of the two RF signal paths.

A.4 - Digital Receivers

Shown in Fig. A.5-a, an ideal digital receiver does not suffer from I and Q mismatches or from the image problem. After filtering and amplification, the RF signal is sampled by an analog to digital converter (ADC). Aliasing the desired signal through the sampling process results in downconverting the RF signal, without using any mixers.

The performance of this structure depends mainly on the ADC characteristics. First, the frequency bandwidth of the ADC should be at least twice that of the RF carrier frequency [111]. Second, its least significant bit should be about 9dB below the minimum receiver sensitivity. Third, its thermal and quantization noise must not exceed few tens of microvolts. Moreover, the ADC should be as linear as possible not to distort the downconverted signal. Finally, a large dynamic range is required in order to accommodate for variations in the signal levels. These stringent requirements are very hard to achieve. Note that 5GHz CMOS digital receivers have not been reported yet.

Also shown in Fig. A.5-b is a digital IF receiver. In such a structure, the signal is

first downconverted with a mixer to an IF frequency. The signal is then processed by an ADC and the second downconversion is performed in the digital domain. The ADC's specifications are also very stringent, however it operates at lower frequencies.

Appendix B - Stability Analysis of the Proposed LNA-Notch Combination

As mentioned in Section 3.4.2, the stability of the proposed circuit was first verified by deriving the transfer function of the overall LNA-notch circuit, including the input matching inductors L_s and L_g, in order to obtain the positions of the poles and zeroes. The circuit was modelled as shown in Fig. B.1, where Z_{Tank} is the parallel combination of R_T, C_T, and L_T, given by

$$Z_T = \frac{1}{(sC_T + 1/sL_T + 1/R_T)}. \tag{B.1}$$

Performing nodal analysis, the following set of equations is obtained

$$v_{out} = -Z_{tank} g_{m3} v_{gs3}, \tag{B.2}$$

$$v_{gs3}\left(g_{m3} + sC_{gs3} + \frac{1}{Z_N}\right) = g_{m1} v_{gs1}, \tag{B.3}$$

and

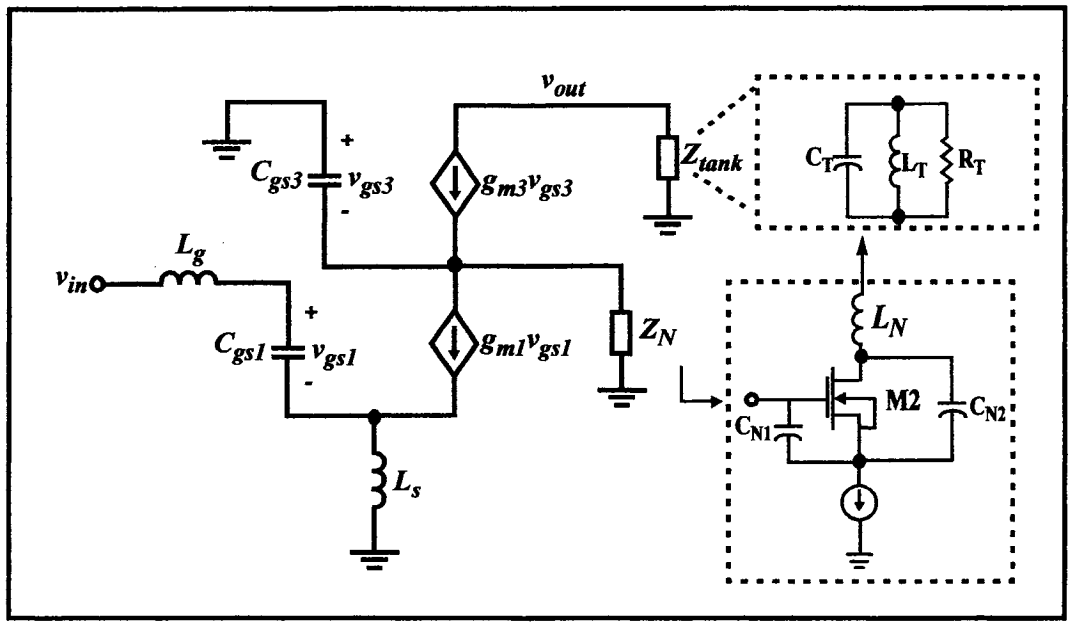

Figure B.1 Small-signal model of the LNA-notch combination circuit of Fig. 3.6.

$$v_{gs1}\left(g_{m1}+sC_{gs1}+\frac{1}{sL_s}+\frac{sL_gC_{gs1}}{L_s}\right)=\frac{v_{in}}{sL_s}. \tag{B.4}$$

Combining equations (B.2)-(B.4), the transfer function $v_{out}(s)/v_{in}(s)$ of the LNA-notch combination circuit is found to be

$$\frac{v_{out}(s)}{v_{in}(s)}=\frac{g_{m1}g_{m3}Z_{tank}Z_N}{(s^2C_{gs1}(L_g+L_s)+sg_{m1}L_s+1)(Z_N(g_{m3}+sC_{gs3})+1)}. \tag{B.5}$$

Using equations (3.11), (3.12) and (B.1), the transfer function can be expressed as

$$\frac{v_{out}(s)}{v_{in}(s)}=\frac{sL_Tg_{m1}g_{m3}\left(\frac{g_{m2}}{s^2C_{N1}C_{N2}}+\frac{(C_{N1}+C_{N2})}{sC_{N1}C_{N2}}+r_s+sL_N\right)}{\left(s^2C_TL_T+\frac{sL_T}{R_T}+1\right)(s^2C_{gs1}(L_g+L_s)+sg_{m1}L_s+1)G(s)}, \tag{B.6}$$

where $G(s)$ is given by

$$G(s) = \left(\frac{g_{m2}}{s^2 C_{N1} C_{N2}} + \frac{(C_{N1} + C_{N2})}{sC_{N1} C_{N2}} + r_s + sL_N\right)(g_{m3} + sC_{gs3}) + 1 . \qquad \text{(B.7)}$$

We start by examining the numerator of Eq. (B.6) in order to obtain the zeroes of the system. Note that the zeroes of the LNA-notch transfer function provide the notching frequency of the circuit. As explained in Section 3.4.1, the term $\left.\frac{g_{m2}}{s^2 C_{N1} C_{N2}}\right|_{s = j2\pi f}$ is negative and it compensates the effect of r_s. As a result, the sum of these two terms tends toward zero, and the numerator of Eq. (B.6) can be simplified to:

$$H(s) = sL_T g_{m1} g_{m3}\left(\frac{(C_{N1} + C_{N2})}{sC_{N1} C_{N2}} + sL_N\right). \qquad \text{(B.8)}$$

The positions of the zeroes are then derived by setting *H(s)* to zero, resulting in

$$s_{Z(1,2,3)} = 0, \pm\sqrt{\frac{C_{N1} + C_{N2}}{L_N C_{N1} C_{N2}}}, \qquad \text{(B.9)}$$

which is in agreement with equation (3.13).

The denominator of equation (B.6) reveals that this is an eighth order system. Two poles come from the $\left(s^2 C_T L_T + \frac{sL_T}{R_T} + 1\right)$ term and are generated from the tank's LC network at the output node. As expected, the positions of these poles are in the left half plane, and are independent of the notch depth tuning. Their locations are given approximately by

$$s_{P(1,2)} \approx -\frac{1}{2C_T R_T} \pm \frac{j}{\sqrt{C_T L_T}} . \qquad \text{(B.10)}$$

Two other poles are generated at the input node of the LNA, and are dependent on the input matching inductors and on the parameters of transistor M1. They are given by the

$(s^2 C_{gs1}(L_g + L_s) + s g_{m1} L_s + 1)$ term in the denominator of equation (B.6). Their locations are found to be

$$s_{P(3,4)} \approx -\frac{L_s g_{m1}}{2C_{gs1}(L_g + L_s)} \pm \frac{j}{\sqrt{C_{gs1}(L_g + L_s)}}. \tag{B.11}$$

Once again, these poles are well within the left half plane and do not cause instability. The last four poles of the system are derived by considering the polynomial *G(s)*. However, the resulting equations are too complex, providing no useful insights. Instead, the poles' location were plotted (Fig. 3.9).

Appendix C - Distortion Analysis

APPENDIX C1 - DERIVATION OF THE K_{gmk-n} TERMS

The derivation of the K_{gmk-n} terms is shown in this appendix. Deriving I_d (Eq. (4.8)) once with respect to V_{gs} results in an equation describing the transcondanctance g_m of the transistor. For the second order response, we need to obtain K_{gmk-2}, which is the second order derivative of I_d with respect to V_{gs}. It is given by:

$$K_{gm-2} = \frac{K}{mob}\left(1 - \frac{u_b(5V_{gs}^2 - 2V_{gs}V_T - 3V_T^2) + 2u_a(V_{gs} - V_T)}{mob} + \frac{(2u_b(V_{gs} + V_T) + u_a)^2(V_{gs} - V_T)^2}{mob^2}\right), \quad \text{(C.1)}$$

where

$$K = \frac{1}{2a(1 + V_{ds}/(E_{SAT}L))}\frac{W}{L}C_{ox}\mu_o \quad \text{(C.2)}$$

and

$$mob = 1 + (u_a + u_c V_{sb})\left(\frac{V_{gs} + V_T}{T_{ox}}\right) + u_b\left(\frac{V_{gs} + V_T}{T_{ox}}\right)^2 . \quad \text{(C.3)}$$

The third-order term K_{gmk-3}, which is the third-order derivative of I_d with respect to V_{gs}, is found to be:

$$K_{gm-3} = \frac{K}{mob^2}\left(3u_a - 12u_b V_{gs} + \frac{3(2u_b(V_{gs}+V_T)+u_a)^3(V_{gs}-V_T)^2}{mob^2} + \frac{6(V_{gs}-V_T)(2u_b(V_{gs}+V_T)+u_a)(u_b(3V_{gs}+V_T)+u_a)}{mob}\right) \quad . \quad (C.4)$$

As it can be seen from equations (C.1)-(C.4), the terms $K_{g_{mk-n}}$ depend mainly on constant MOSFET model parameters, such as u_a , T_{ox} , etc., on the transistor's size (W and L), on the biasing voltages ($V_{gs,}$ V_{ds} and V_{sb}), and on the threshold voltage V_T. Under a specific biasing condition, all of these terms are constant and frequency independent. Moreover, it is interesting to note that $K_{g_{mk-2}}$ and $K_{g_{mk-3}}$ are effectively inversely proportional to V_{gs}. This is because the highest order term of V_{gs} is 5 in the denominator of $K_{g_{mk-2}}$ and 4 in its numerator. Similarly, the highest orders of V_{gs} are 8 and 7 in the denominator and in the numerator of $K_{g_{mk-3}}$, respectively. Finally, as it is the case for the biasing current I_d and for the transconductance g_m, the $K_{g_{mk-n}}$ terms are linearly dependent on the W/L ratio.

APPENDIX C2- IM3 DISTORTION IN THE LNA

Using Volterra's series (Section 4.3) and equations (4.17)-(4.20), expressions describing the third-order intermodulation distortion in the LNA were derived and are summarized as follows:

The output IM3 voltage is given by:

$$IM3 = \frac{3}{4}v_{in}^2\left|\frac{H_{out3}(jw_1, -jw_2, -jw_2)}{H_{out1}(jw_1)}\right| , \quad (C.5)$$

where

$$H_{out1}(s) = \frac{1}{\Lambda(s)}\left(\frac{sC_{ds}+g_{m1}}{1/r_s + sC_{ds}} + 1\right)sC_{ds} , \quad (C.6)$$

$$\Lambda(s) = \left(s(C_{ds}+C_T) + \frac{1}{sL_T} + \frac{1}{R_p}\right)\left(\frac{sC_{ds}+g_{m1}}{1/r_s + sC_{ds}} + 1\right) + \frac{sC_{ds}+g_{m1}}{1+sC_{ds}r_s} \quad (C.7)$$

and

$$H_{out3}(jw_1, -jw_2, -jw_2) = i_{gm1-3}(jw_1, -jw_2, -jw_2)\frac{\Theta(jw_1, -jw_2, -jw_2)}{\Lambda(jw_1, -jw_2, -jw_2)} \quad \text{(C.8)}$$

where

$$\Theta(s_1, s_2, s_3) = \left.\frac{1 + sC_{gs}r_s}{1 + sC_{ds}r_s}\right|_{s = s1 + s2 + s3}, \quad \text{(C.9)}$$

$$i_{gm1-3} = K_{g_{m1-3}}H_{1vgs1}(jw_1)H_{1vgs1}(-jw_2)H_{1vgs1}(-jw_2) + \frac{2}{3}K_{g_{mk-2}} \quad \text{(C.10)}$$
$$\times [H_{1vgs1}(jw_1)H_{2vgs1}(-jw_2, -jw_2) + 2H_{1vgs1}(-jw_2)H_{2vgs1}(jw_1, -jw_2)]$$

$$H_{1vgs1}(s) = \frac{1}{\Lambda(s)}\frac{sC_{ds}}{1 + sC_{ds}r_s} \quad \text{(C.11)}$$

$$H_{2vgs1}(s_1, s_2) = \frac{1}{1 + sC_{ds}r_s\Lambda(s)}\left(1 - r_s\left(s(C_{ds} + C_T) + \frac{1}{sL_T} + \frac{1}{R_p}\right)\right)\Bigg|_{s = s1 + s2}, \quad \text{(C.12)}$$

where K_{gm-2} and K_{gm-3} are the second and third coefficients of the Taylor expansion of $I_d(V_{gs})$, (derived in Appendix C1), and are constant for a given bias point.

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