THE DESIGN AND CONSTRUCTION OF A DISC ORIENTED GRAPHICS SYSTEM

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by

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CHAPTER I

INTRODUCTION

In recent years, computer graphics has grown from an experimental science to a powerful tool used in research and design. Fields benefiting from such a development are process control (1) , pattern recognition (2) , computer-aided circuit design (3,4) , as well as man-machine communication studies (5) , to name but a few. The full power of such systems lies in their interactive potential, that is, to allow two-way communication between the system and the operator. For this purpose, special devices such as light pens , joysticks, sketch pads and function switches have been developed and are in use. For example the Electronic Systems Laboratory at the Massachussetts Institute of Technology has developed a system (6) which uses every one of these devices for maximum interaction and flexibility. Other systems (1) , however, use but a small number of such devices. These systems are generally special-purpose in nature and require but a limited amount of interaction.

In the fall of 1968 it was decided , for a variety of reasons, to develop a graphics system, centered about a DEC PDP-8 computer with a link to an IBM 360/75 , in the Department of Electrical Engineering at McGill University. First there was considerable interest in the application of graphics facilities to research work being carried out in the department. Personnel required for such an undertaking was fortunately available and sufficient funds to cover hardware expenses were assimilated. Finally there was an interest in extending the state of the art and in gaining expertise in system design.

A growing number of graphics systems are commercially available (IBM , CDC , ADAGE , DEC). Unfortunately, such units are very expensive even though they may be supported by varying amounts of software. By specially tailoring a system to complement facilities already available, it may be possible to significantly reduce the cost of computer graphics or to design a system achieving special performance. Both of the above considerations apply in our design.

A block diagram of the equipment already in existence in the department, as well as the graphics system, is shown in Figure 1. The scheme includes a hierarchy of processors, capable of operating in parallel, which are optimized at each level for maximum throughput and man-machine interaction. At the lowest level, the PDP-8 controls the various I/O peripherals as well as the scanning and hybrid systems. Graphics software is being developed on the PDP-15/20 which is also available for a certain amount of computational work. At the highest level, the 360/75 is involved with computations that are too extensive for the PDP-15/20 and also provides access to the many special purpose programs available to the 360 system. The versatility and power of the available software and hardware of the PDP-15/20 will allow very sophisticated task sharing between computers.

The heart of the display system is the DATA DISC (model FDP-16) which is a 16-track disc with parallel read/write heads. Display files, consisting of eight-bit words serially written on the disc, can be generated in any of the three computers. The philosophy behind this approach is to avoid computer refreshment of the CRT so that the computers can be dedicated exclusively to computation and interaction. This philosophy is also shared by the designers of the MIT system mentioned earlier (6). The

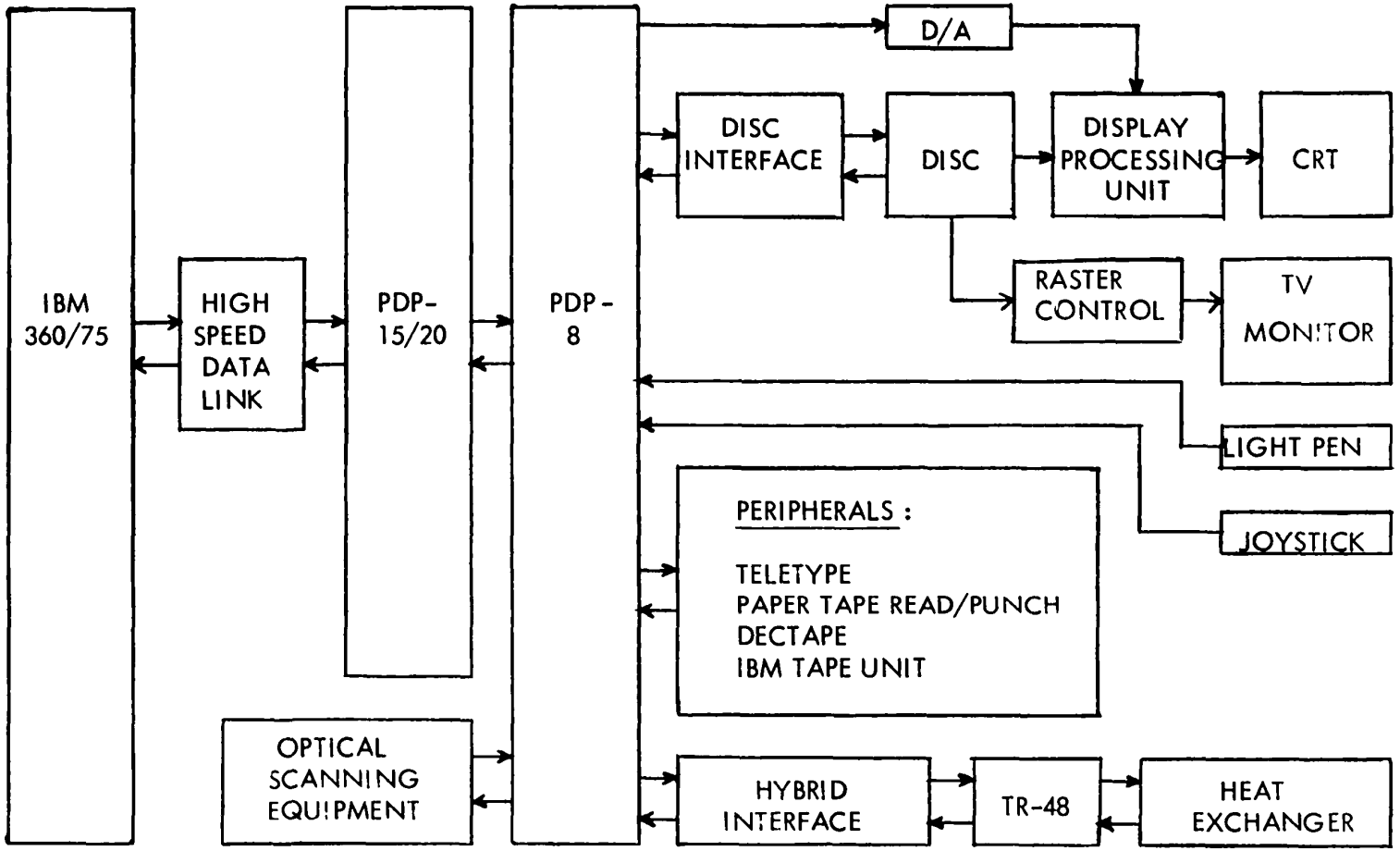

FIGURE 1 : THE MCGILL COMPUTER SYSTEM

image files on the disc are processed by the Display Processing Unit (DPU) , or graphics unit, thirty times per second and displayed on a Dumont Model 737 CRT. Should flicker be a problem, an image may be processed several times per disc revolution, by repeating the file on the disc. This operation may also be used to increase the illumination of the image. A distinctive feature of the system is that it has the capability of displaying optically scanned pictures on a CONRAC TV monitor, including those obtained from the output of a microscope. The latter property is believed to be unique in Canada. It is possible to interact in real time with the DPU display file by means of a Sanders Photopen Light Scanning and a DEC joystick.

This thesis describes the design and construction of the necessary hardware for the graphics unit. Before any design was undertaken on this device, typical systems (1,5,6) where examined. A popular method of drawing lines is to plot a series of points or short vectors. This results in a variable drawing time. Since our design philosophy included drawing a variable length line in a fixed amount of time, it was decided to use analog integrators for drawing vectors; of course, when very long vectors are required, several short ones will have to be drawn in succession, in order to preserve sufficient illumination.

Due to the relatively large amount of storage space afforded by the disc, a track selection feature was incorporated. This feature is generally not found in graphics systems. It allows a manual choice of files, by selection of any of the sixteen tracks. Program control of track switching is also available, using a BRANCH statement. An assortment of files may be stored on the disc and any of these may be selected at will. This could be especially useful where interactions are involved. The absence of a hard-

ware character generator is not considered to be a serious drawback, since characters may be constructed from software subroutines with comparable speed.

Another important feature which was implemented is that of scaling. A SCALE statement causes succeeding parts of a picture to be magnified up to 128 times in powers of 2. The ability to use standard files at different magnifications, is particularly attractive. The overall intensity of a picture or parts thereof is controlled by an INTENSITY statement. This permits shading. Automatic beam intensity compensation is also included since the fixed drawing time of a vector move would normally cause shorter vectors to be brighter.

When a new file is begun, the program has the ability of interrupting the computer. Succeeding action is then determined by a computer-stored program.

The decision to store commands serially on the disc results from experiments conducted on the CRT . The short single-bit time of 300 nanoseconds was found insufficient to plot a vector longer than a thirty-second of an inch. Thus a serial eight-bit word length, resulting in 2.4 microseconds, permits a quarter-inch vector to be displayed with excellent illumination. Also, 12,500 commands can be stored on one track. Assuming that 50% of these commands are quarter-inch vectors, 1500 inches of line drawing is possible per disc revolution. This certainly appears to be enough to produce the most formidable picture ! Timing pulses are derived from the disc's clock tracks, since the latter is the only input device to the graphics unit.

Chapter II describes the operation of the system from a software viewpoint. The design of the main logic functions of the system are described in Chapter III .

Chapter IV describes the choice of hardware components along with their more important specifications, while Chapter V describes the testing of the various parts of the system. Finally, Chapter VI presents a collection of test routines to aid in detecting and locating possible faults. These are written in a proposed assembler language. Also, an example using binary or machine language instructions is shown .

CHAPTER II

INSTRUCTION FORMATS

In this chapter, we shall discuss the formats of machine-coded (binary) instructions. They are divided into two classes. The first, denoted COMMAND instructions, are the following:

HEADER	the first instruction of every file. Contains file name and other pertinent infomation.
BRANCH	instructs DPU to process information from another disc track.
OPERATE	informs DPU that subsequent statements are DATA instructions, as well as which type.

The second class of instructions are of the DATA type:

POINT	plots a point on the screen.
VECTOR	draws a line on the screen.
INTENSITY	increases or decreases the relative illuminations of subsequent portions of the image.
SCALE	increases or decreases the relative size of subsequent portions of the image.

Both types of instruction are described in more detail below.

Nominal instruction size is eight-bits (1 word). However some instructions require more bits and are therefore allotted sixteen bits (2 words).

2.1 COMMAND Instructions

The system interprets instructions to be HEADER , BRANCH or OPERATE only when the system is in the COMMAND mode. This can be ensured by an instruction whose uppermost bits (F8 and F7) are 11 (binary) , issued when the system is in the DATA mode. Each of the COMMAND instructions is described below.

2.1.1 HEADER

Figure 2.1.1 shows the bit configuration for the HEADER instruction. It is identified by bits F8 and F7 being 1 and 0 respectively. F6 = 1 instructs the system to interrupt the PDP-8. In this case the PDP-8 reads the information in the FILE NAME REGISTER (FNR). Bits in the FNR are a copy of the file name portion of the HEADER statement, bits F4 to F1 plus the eight bits of the next word. The FNR is updated each time a HEADER statement is processed, providing an indication of the file currently being displayed. F6 = 0 results in no interrupt.

F5 = 0 allows the following file to be displayed, while a 1 in this bit position inhibits display.

2.1.2 BRANCH

Programmed track switching is achieved using this instruction. It is another two-word command, as shown in Figure 2.1.2 . F8 and F7 = 0, 1 informs the

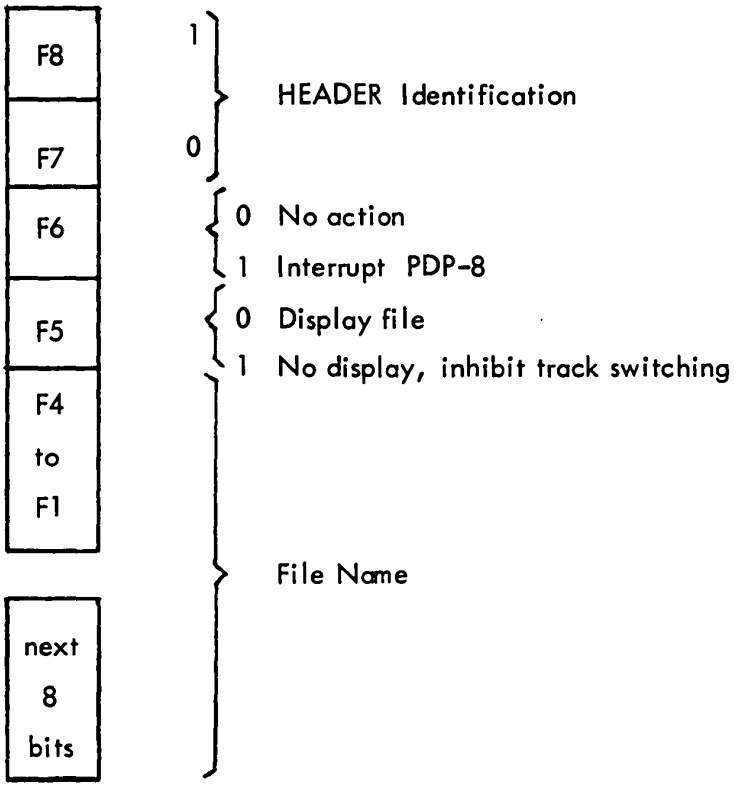

FIGURE 2.1.1 : HEADER INSTRUCTION

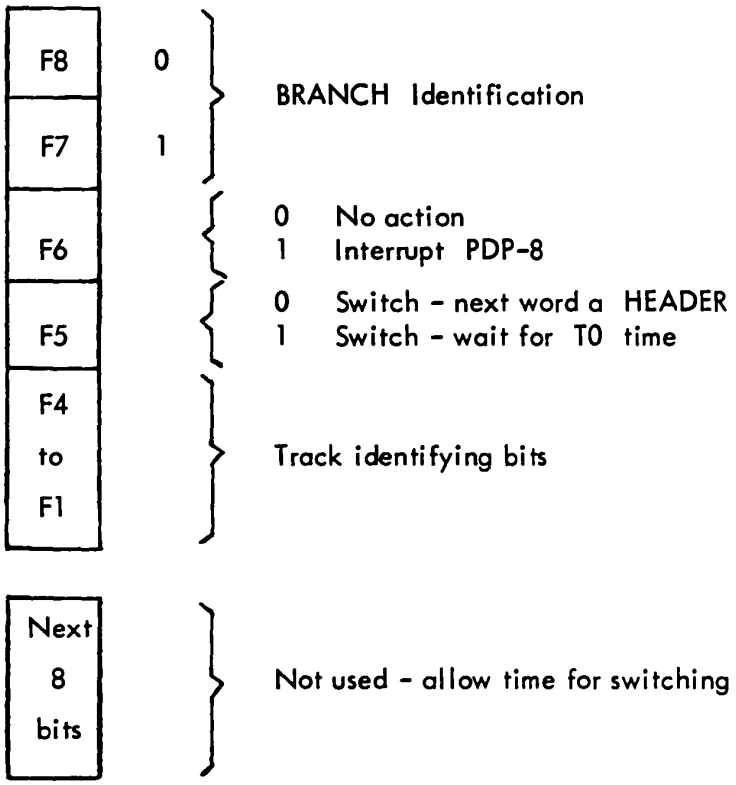

FIGURE 2.1.2 : BRANCH INSTRUCTION

system that this is a BRANCH statement. When F6 is 1, a PDP-8 interrupt and subsequent reading of the file name results, as in the HEADER statement. F5 = 0 causes switching over to the track specified by bits F4 to F1. The system remains in the COMMAND mode and the first word of the new track should be a HEADER statement. F5 = 1 results in similar action, with the exception that the system clock is inhibited and all action ceases until track origin (TO) time. The eight bits of the second word are not decoded but simply allow time for the switching to take place.

2.1.3 OPERATE

The function of this single-word instruction is to place the system in one of the four DATA states. It is identified as an OPERATE statement when F8, F7 = 0,0 , as shown in Figure 2.1.3 . F6 and F5 select the type of DATA format that follows (POINT, VECTOR, INTENSITY or SCALE). Bits F4 to F1 are not used.

After choosing a data format using the OPERATE instruction, the system is no longer in the COMMAND mode and subsequent statements are processed as DATA information. It is returned to the COMMAND mode by using the return option of a DATA instruction .

2.2 DATA Instructions

The operations performed by these instructions permit clearing and/or incrementing of a register. The register(s) to be operated on depend on the type of

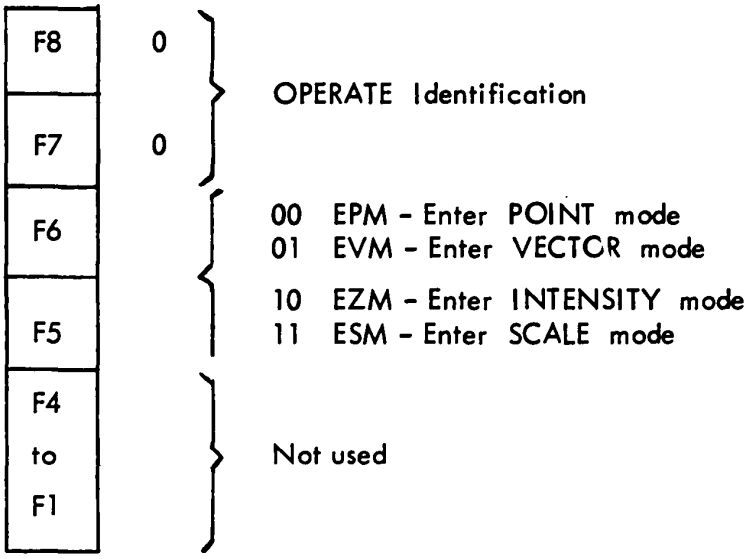

FIGURE 2.1.3 : OPERATE INSTRUCTION

DATA instructions (POINT, VECTOR , etc.) . A return to the COMMAND mode is an option in any DATA instruction. Action to be taken is determined by the bit assignment of F8 and F7 (operation field) of the statement, as described below.

2.2.1 POINT

In this mode, a point may be plotted on the screen after the beam position has been moved in one (and only one) of the coordinate directions (X,Y). A single-word POINT instruction permits the beam position to be moved a maximum of 1/4" (3 bits) in one direction. A two-word instruction allows the move to be as long as a full screen length (10 bits). A move is made relative to a reference point, defined as the point at which the beam came to rest after a preceeding POINT or VECTOR move has been completed. An exception to this rule is when the system has been instructed to clear the register before incrementing. In this case, a move is made relative to the origin (point 0,0) , which is defined as the lower, left-hand corner of the screen.

F8 and F7 (operation field) are interpreted as follows. 00 clears the appropriate (X or Y) reference point register (RPR) and adds to it the increment (defined later). The beam position is advanced on amount determined by the increment and a point may be plotted on the screen. 01 results in similar action, except that the RPR is not cleared first. 10 causes subtraction of the increment from the RPR without clearing it first. 11 returns the system to the COMMAND mode. See Figure 2.2.1.

F6 indicates the axis (0 for X, 1 for Y) along which the point is to be moved. If F5 is 0, the point is plotted after the beam position has been moved. F5 = 1 inhibits plotting (blanked move). If F4 is 0, a single-word POINT instruction

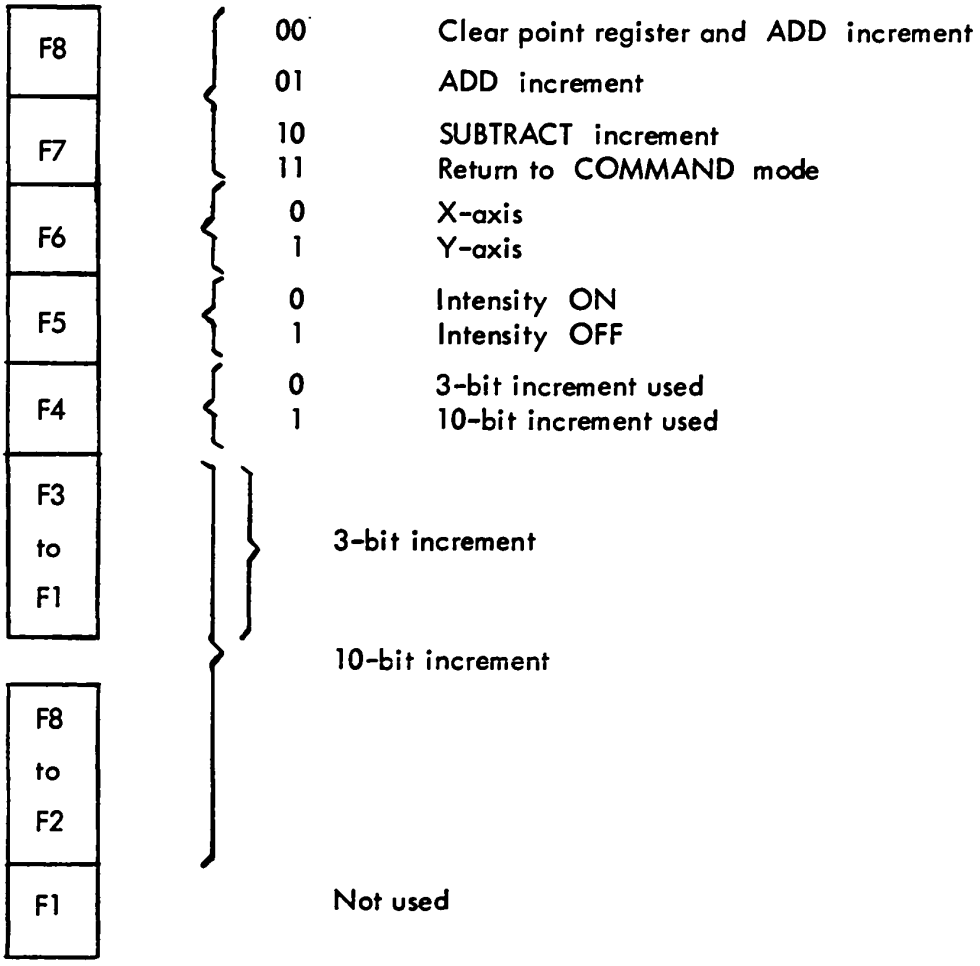

FIGURE 2.2.1 : POINT INSTRUCTION

is denoted and bits F3 to F1 are decoded as the increment to be added to, or subtracted from, the RPR and a short move results. Otherwise, these same bits, plus bits F8 to F2 of the next word form a 10-bit increment. This 2-word version of the POINT instruction allows a long move.

Diagonals require two operations. The first is a blanked move along one axis direction. The second is a move along the other axis direction and the point may then be plotted.

2.2.2 VECTOR

This instruction is expected to be the most useful statement. It has the ability to draw a line of variable length in any direction by specifying both X and Y arguments.

Figure 2.2.2 shows that the functions of the four uppermost bits (F8 to F5) are identical to those in the POINT instruction previously discussed. F4 = 0 indicates a 1-word VECTOR instruction. This results in a short vector (3 bits = 1/4" max.) in the coordinate direction specified by F6. When F4 = 1, a 2-word VECTOR instruction is implied. In this case bits F3 to F1 of the first word are decoded as the X-component of the vector move. F8 of the second word specifies the sign of the Y-component of the move and bits F3 to F1, its magnitude. The remaining bits are not used.

Longer vectors may be drawn by making use of the scale feature. However, some caution is required since too high a drawing speed will result in poor illumination. Long vectors are best handled by drawing a series of shorter ones, or else by drawing them several times per disc revolution.

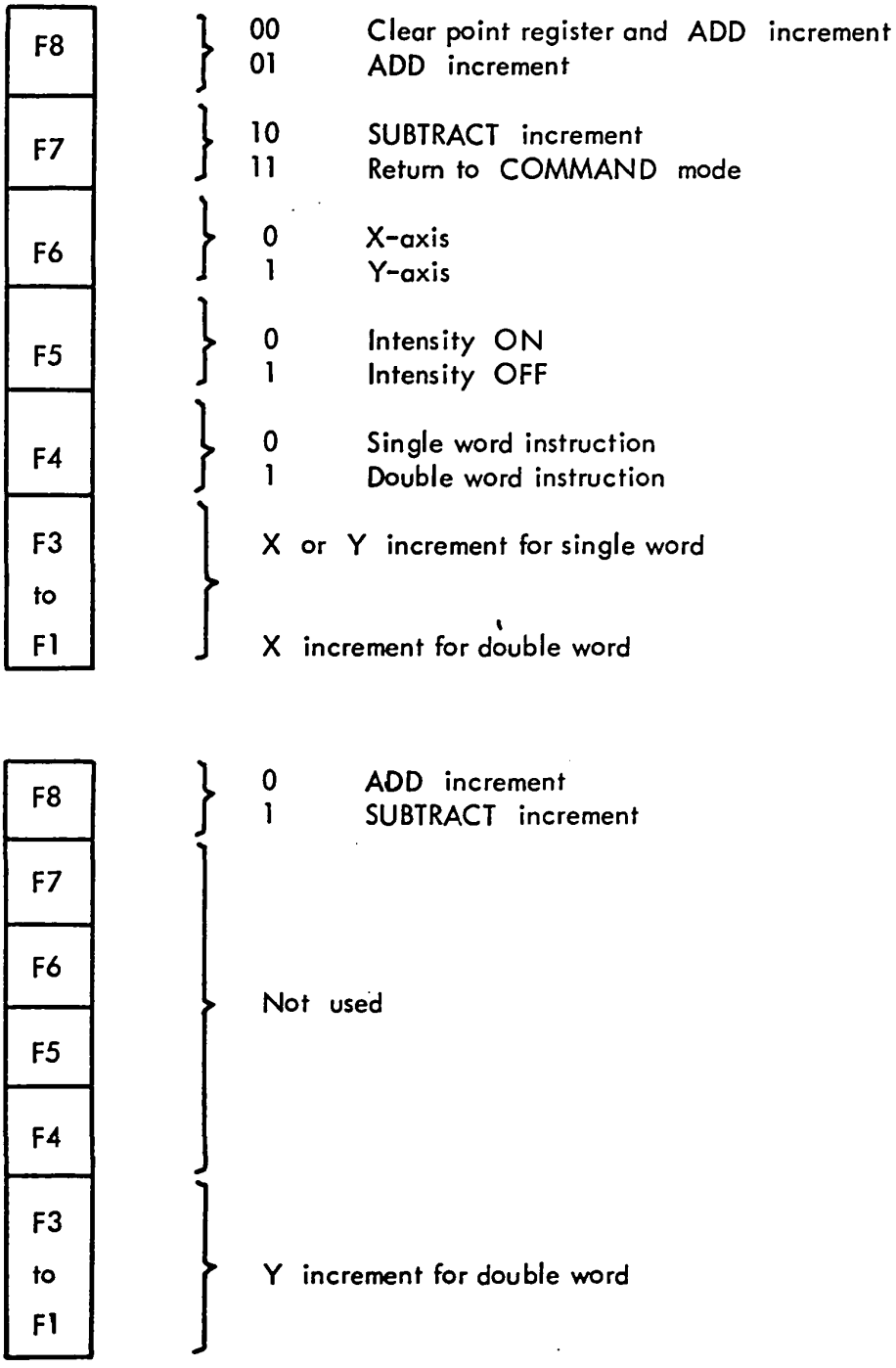

FIGURE 2.2.2: VECTOR INSTRUCTION

2.2.3 INTENSITY

This instruction controls the illumination of a point or vector on the screen. It must be set at the beginning of the first file after track origin and may be modified at will during a revolution of the disc.

Figure 2.2.3 shows the structure of the statement. The operation field bits (F8 and F7) have the same function as previously described. However, they now operate on the intensity registers (IR's) instead of on the RPR's.

F6 and F5 determine which of four IR's is to be modified. Up to four black and white (B & W) CRT's or one colour and one B & W CRT could therefore be driven. The four increment bits, F4 to F1, allow sixteen levels of brightness, including zero (blanked moves).

2.2.4 SCALE

This instruction permits changing the relative size of subsequent portions of an image. This is accomplished by shifting the X or Y increments up the register before processing them. Since there are two scale registers (SR's), one for each axis, the magnification in each direction may be different.

Figure 2.2.4 shows the format of the SCALE instruction. Bits F8 and F7 perform the same functions as previously described. However, they operate on the SR's this time. F6 specifies which SR is to be updated, 0 for X and 1 for Y. When F5 = 1, moves corresponding to the axis specified by F6 are performed in the opposite direction ($-\Delta X$ or $-\Delta Y$ instead of $+\Delta X$ or $+\Delta Y$). Setting

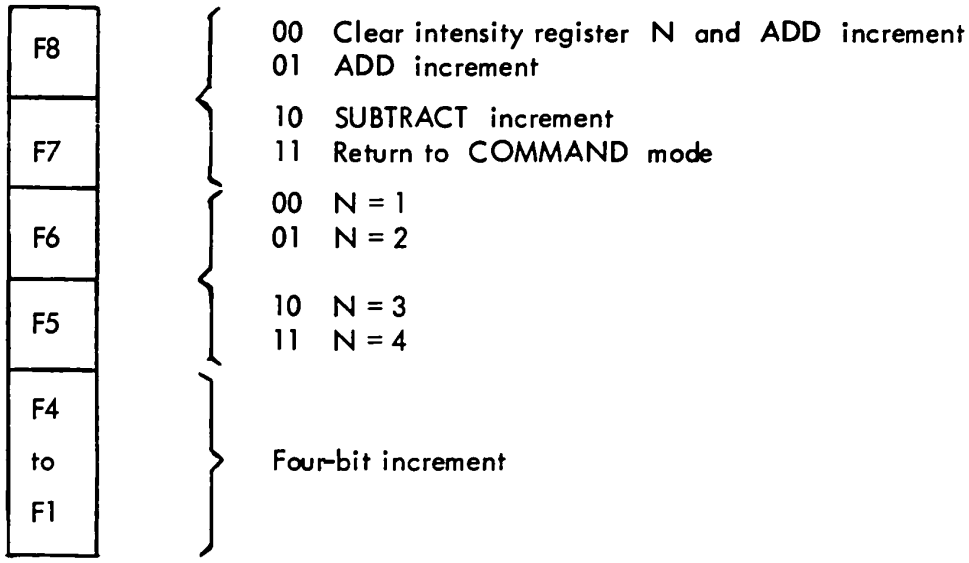

FIGURE 2.2.3 : INTENSITY INSTRUCTION

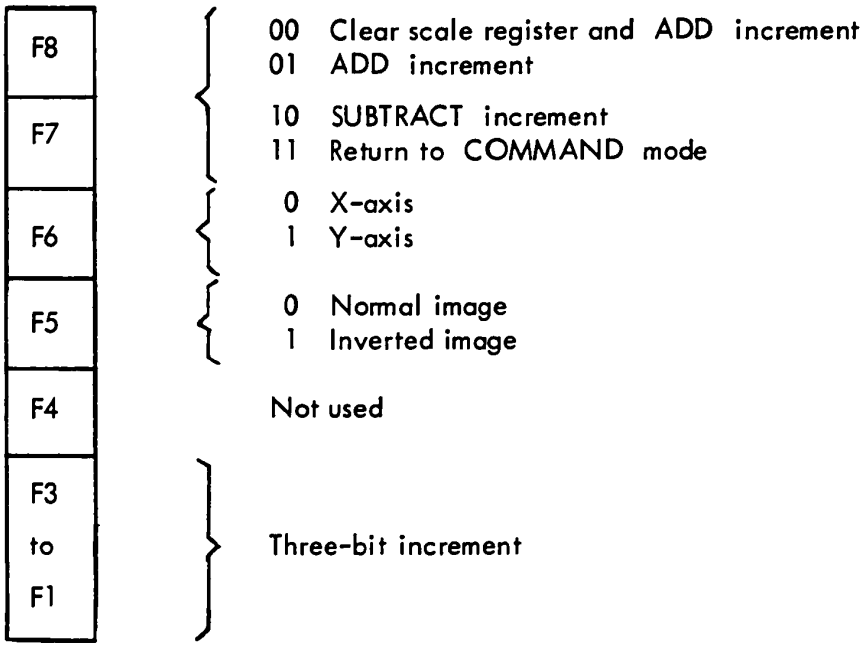

FIGURE 2.2.4 : SCALE INSTRUCTION

both (X and Y) to the negative direction results in an inverted image. New SCALE instructions with F5 = 0 restore image processing to normal directions. F4 is ignored.

The SCALE increment, bits F3 to F1 allow the X and Y increments to be shifted seven times. Thus if a particular bit pattern results in a 1/8" vector, this same pattern will produce a 1/4" vector when shifted up once.

CHAPTER III

DESIGN OF THE DISC PROCESSING UNIT

In this Chapter, the design of the Disc Processing Unit for the graphics system is presented in block diagram form and the philosophy of operation of the main parts is explained.

The circuits to be described here are: track selection, serial to parallel conversion, system clock, scaling, points and vectors and analog circuitry.

The complete set of circuit diagrams is included in the appendix.

3.1 Track Selection

The system control panel consists of two power switches, with corresponding fuses and pilot lights, as well as a rotary sixteen-position track selection switch (TSS) and a three-position toggle switch (SWT).

The function of the rotary switch is to select one of sixteen disc tracks. It feeds four bits (0-15) of information to the track number decorder, shown in Figure 3.1 .

When SWT is in the position marked CONT. (UP) , it allows the T0 pulse to gate the four bits into the decoder. After an appropriate delay, this information is clocked into the track number register where it is held. In this mode, the system always returns to the track specified by the TSS at T0 time. If SWT is in

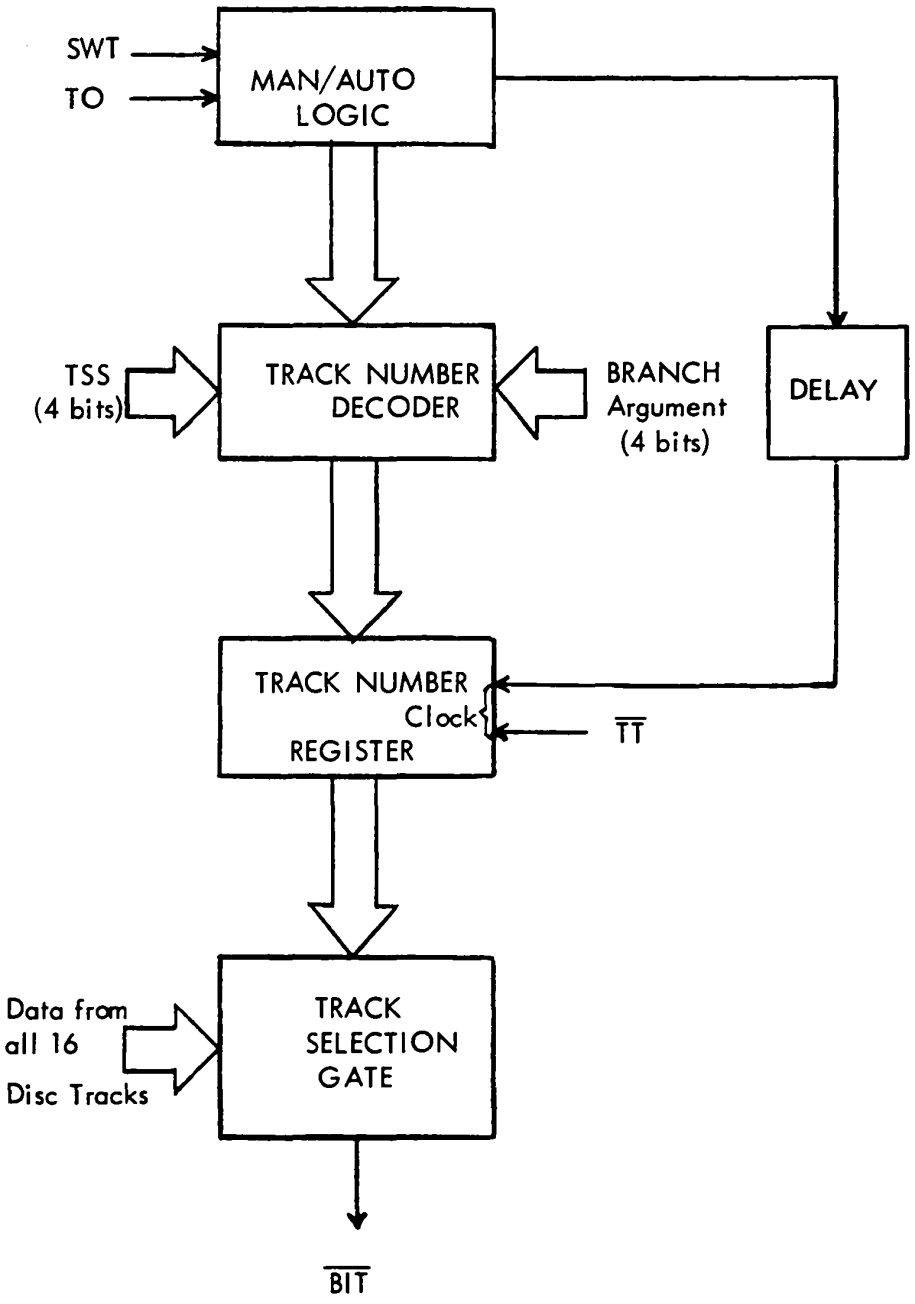

FIGURE 3.1 : TRACK SELECTION

the MOM. (momentary) position (DOWN), the same action takes place for as long as SWT is held in this position. Once SWT is released, it returns to the OFF (MIDDLE) position. In this OFF position, T0 has no effect on track switching. The only way to switch tracks is under program control by using a BRANCH statement.

In any case, the argument (4 bits) of the BRANCH statement is fed to the track number decoder. A trigger pulse ($\overline{TT}$) , produced by the BRANCH mechanism then clocks this infomation into the track number register.

The track selection gate accepts data from all sixteen disc tracks. However, only one track is selected to generate the output, $\overline{BIT}$. The particular track selected depends on information from the track number register. A string of bits is now available as input to the system.

3.2 Serial to Parallel Conversion

Throughout this Chapter, it will be found that many system variables are of the form $\overline{X \ldots X}$. The bar signifies that a logical inverse of the true variable is being used. There are two reasons for this. First, a variable entering a subsystem is generally inverted at each logical stage. Typically, NAND and NOR gates , very common in the type of logic (TTL) being used, inherently invert the true result. Secondly, a TTL output is able to drive ten unit loads. An input to a NAND or NOR gate is defined as one unit load. Inputs to flip-flops and other logic devices represent from one to four unit loads. If many such devices are to be driven from a particular output, its driving capability must be increased. This is achieved by feeding the

output to two or more inverting gates. Each of these gates is able to drive ten unit loads. However, the signal is inverted and this must be considered at design time.

The function of the unit shown in Figure 3.2 is to convert the serial bit string $\overline{BIT}$ to a parallel eight-bit word. $\overline{BIT}$ enters an eight-bit shift register. Each time a Read Shift Clock ($\overline{RSC}$) pulse occurs (every 300 nanoseconds) , $\overline{BIT}$ is shifted one binary position and a new $\overline{BIT}$ is entered. After eight $\overline{BIT}$'s have been processed, the contents of the shift register are transferred to an eight-bit register called the Word Buffer and held for 2.4 μsec . The contents of this buffer form the eight-bit instruction words. Transfer of information occurs at time 8 (TM8). Times 1 to 8 are obtained from a clock described below.

3.3 System Clock

The system clock, shown in Figure 3.3a , produces eight timing pulses. They are labelled $\overline{TM1}$ to $\overline{TM8}$, $\overline{TM1}$ corresponding to time 1, etc . . $\overline{TM2}$ follows $\overline{TM1}$, $\overline{TM3}$ follows $\overline{TM2}$ and so forth. After pulse $\overline{TM8}$ has occurred, the clock repeats itself, starting at $\overline{TM1}$. These pulses are shown in Figure 3.3 b.

A 3-bit counter, consisting of three type J-K flip-flops, is the main element of the clock circuit. The counter is triggered (updated) from a variable called CLCK. This variable is obtained from RSC. It differs from RSC in that it is rendered inactive (no pulse train) when a BRANCH statement (Section 2.1.2) instructs the system to wait for T0 before processing another file. The counter is reset to zero ($\overline{TM8}$) at T0 time.

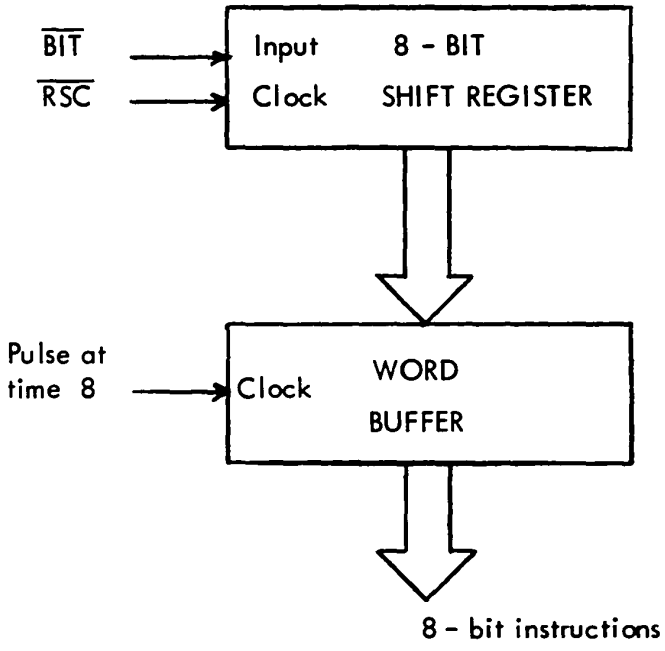

FIGURE 3.2 : SERIAL TO PARALLEL CONVERSION

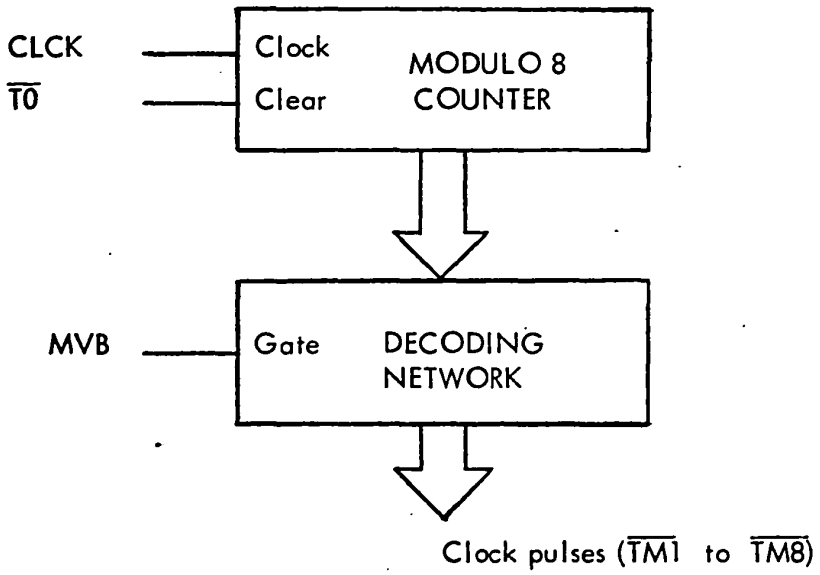

FIGURE 3.3a : SYSTEM CLOCK

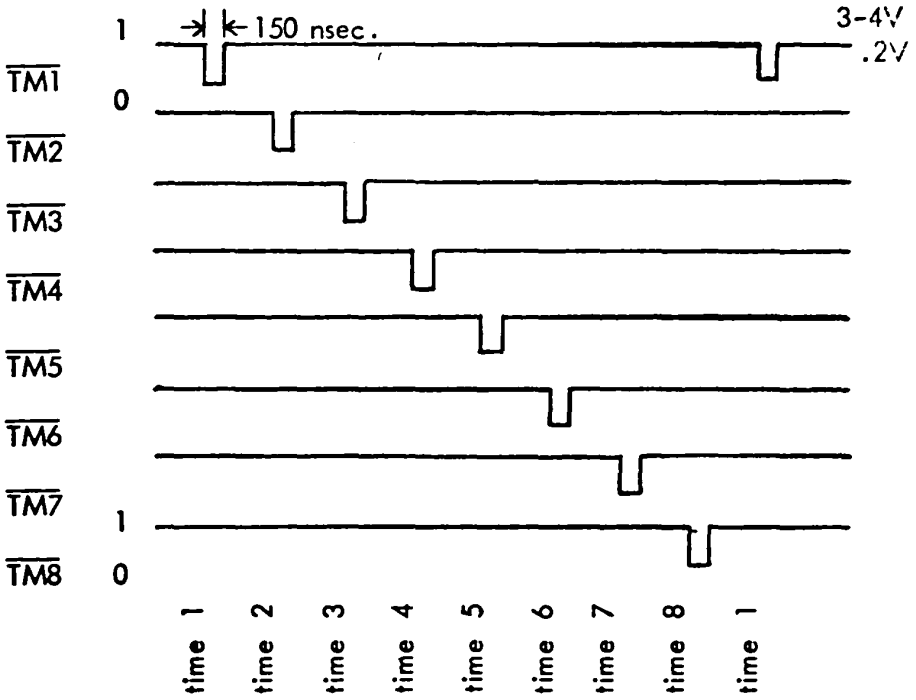

FIGURE 3.3b : CLOCK PULSES

The three bits resulting from the counter enter a decoding network where they are converted to eight timing pulses ($\overline{TM1}$ to $\overline{TM8}$) . MVB is formed by delaying RSC and is used to ensure that the decoding network has settled before issuing the timing pulses.

3.4 Arithmetic Units

Before considering other principal parts of the system, let us discuss a circuit called an Arithmetic Unit (AU) and shown in Figure 3.4 . A thorough description of the device is given since it is used in several parts of the system. The circuitry of the AU , when it is used in different parts of the system, may differ in two ways. First, its bit capacity depends on where it is used. The SCALE system requires a 3-bit AU . The POINT and VECTOR system requires a 10-bit unit. The four INTENSITY systems each require a 4-bit AU. Second, the output of register 1 may or may not be made available to the system. This depends on whether or not the system requires this information.

Increments from DATA type instructions (after scaling in the case of POINT or VECTOR) are presented to register 1. They are clocked by a control signal and held there. Where necessary, the contents of this register are made available to the system. These same bits serve as an input to an ADDER/SUBTRACTOR (A/S) . A second input to the A/S is the output of register 3 . The sum or difference of the two inputs is temporarily clocked into register 2. Finally, the contents of register 2 are clocked into register 3. Register 3 is defined as an absolute value register when

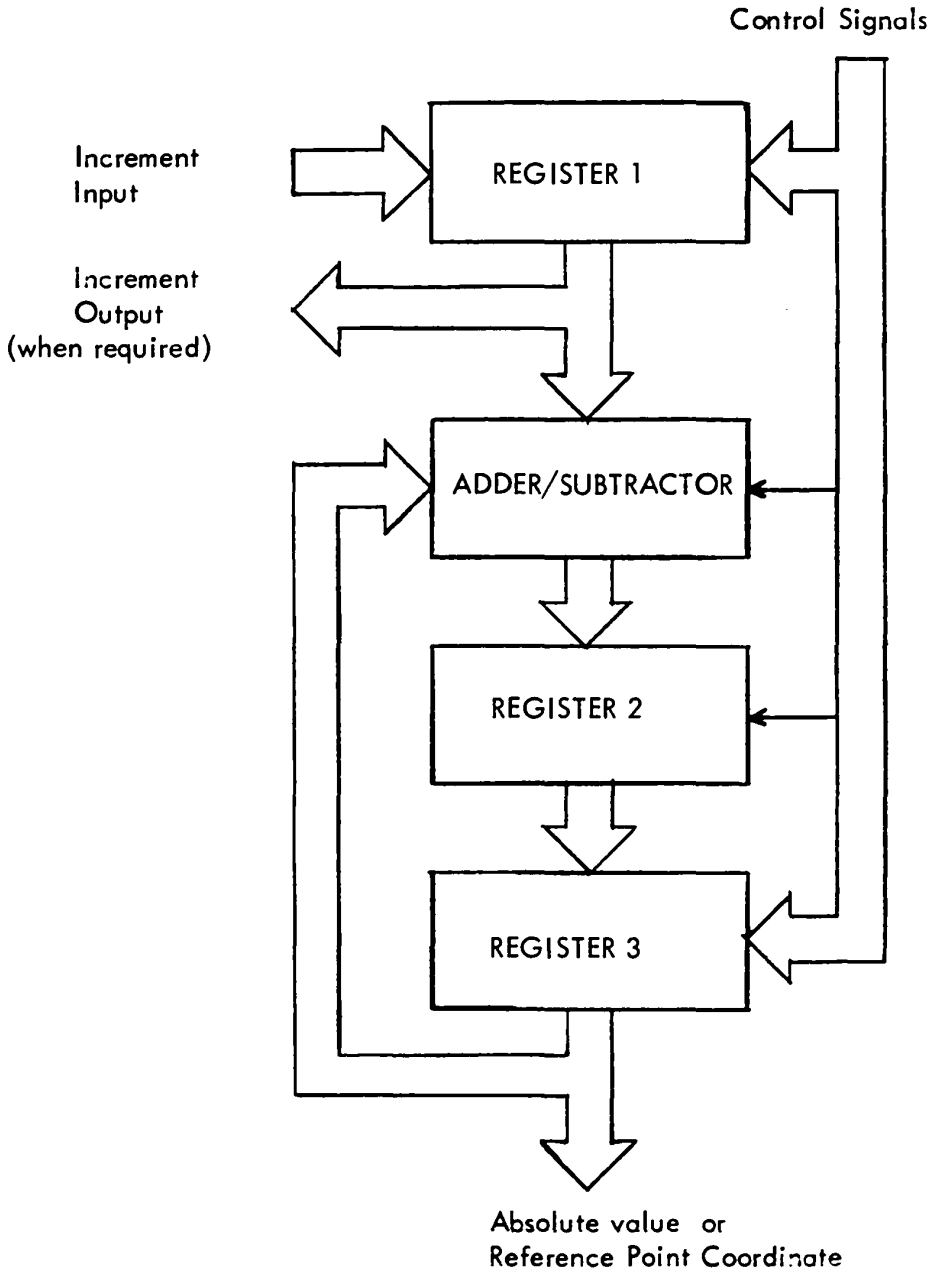

FIGURE 3.4 : ARITHMETIC UNIT

the AU is used in the SCALE or INTENSITY systems. It's contents indicate the number of times a POINT or VECTOR increment is to be shifted (SCALE) or the intensity level of a particular screen plot (INTENSITY) . When AU's are used in the POINT and VECTOR system, their contents are defined as reference point coordinates. This point is the origin of any CRT beam incremental move. It is updated after a move has been completed.

Register 2 is necessary for the following reason. Assume a clock pulse occurs to update register 3. It's contents are fed back to the A/S. The output of the A/S changes and cannot therefore be an input to register 3 until the clock pulse has ended. Thus register 2 serves as a buffer between the A/S and register 3.

3.5 Scaling

Figure 3.5 shows a block diagram of the SCALE system. Appropriate bits from the Word Buffer of Figure 3.2 are presented to a Control Unit. If the statement is found to be a SCALE instruction, clock pulses are issued as well as sign and axis information for the AU's. There are two AU's in the SCALE system, one for each axis. However, only one is logically connected to the Decoder, depending on the axis being processed. The appropriate AU accepts bits from the increment field of the SCALE instruction and is updated. The resulting three bits are decoded into eight bits, B0 to B7. Only one of these bits is "1" while all others are "0". Let us assume that B_n is "1" . The assembled bits of a POINT or VECTOR instruction (A1 to A10) enter the Shifter where they are shifted upward n binary positions. The magni-

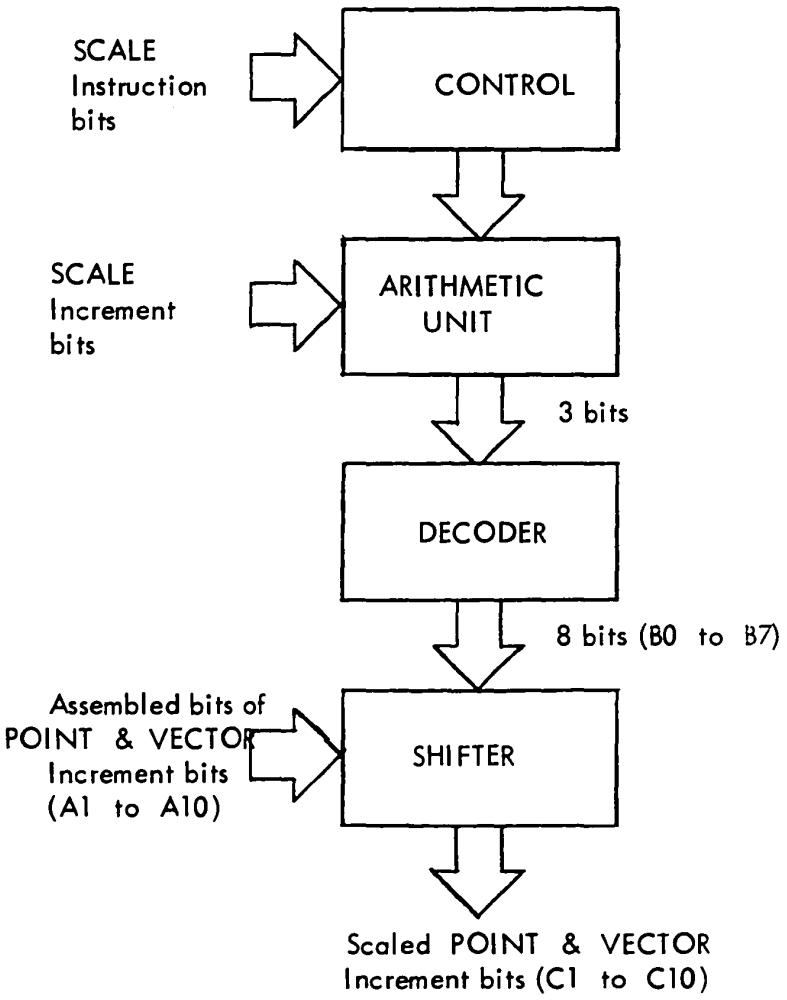

FIGURE 3.5 : SCALE SYSTEM

fication is then 2^nX. The output of the shifter is a scaled POINT or VECTOR increment. These bits, denoted C1 to C10 are fed to the X or Y AU shown in the next section.

3.6 Points and Vectors

In this section, the circuitry which produces digital point and vector signals is described. The analog circuitry which processes this information and drives the CRT is discussed in the next section.

Consider Figure 3.6.1 . Instruction bits from a POINT or VECTOR instruction enter a control unit. This device produces control signals for the circuit shown, as well as for the corresponding analog circuits. The increment bits of the instruction are fed to the A-register. Here they are assembled as follows:

- For a short (1-word) "point move", the increment bits are placed into the lower three bits (1 to 3) of the A-register. The remaining seven bits are set to zero (cleared).
- A short "vector move" results in the same action.
- For a long (2-word) "point move" , the least significant increment bits (from word 1) are placed in bits 1 to 3 of the register. Then, when word 2 is processed, the remaining seven increment bits are entered into bits 4 to 7 of the register.

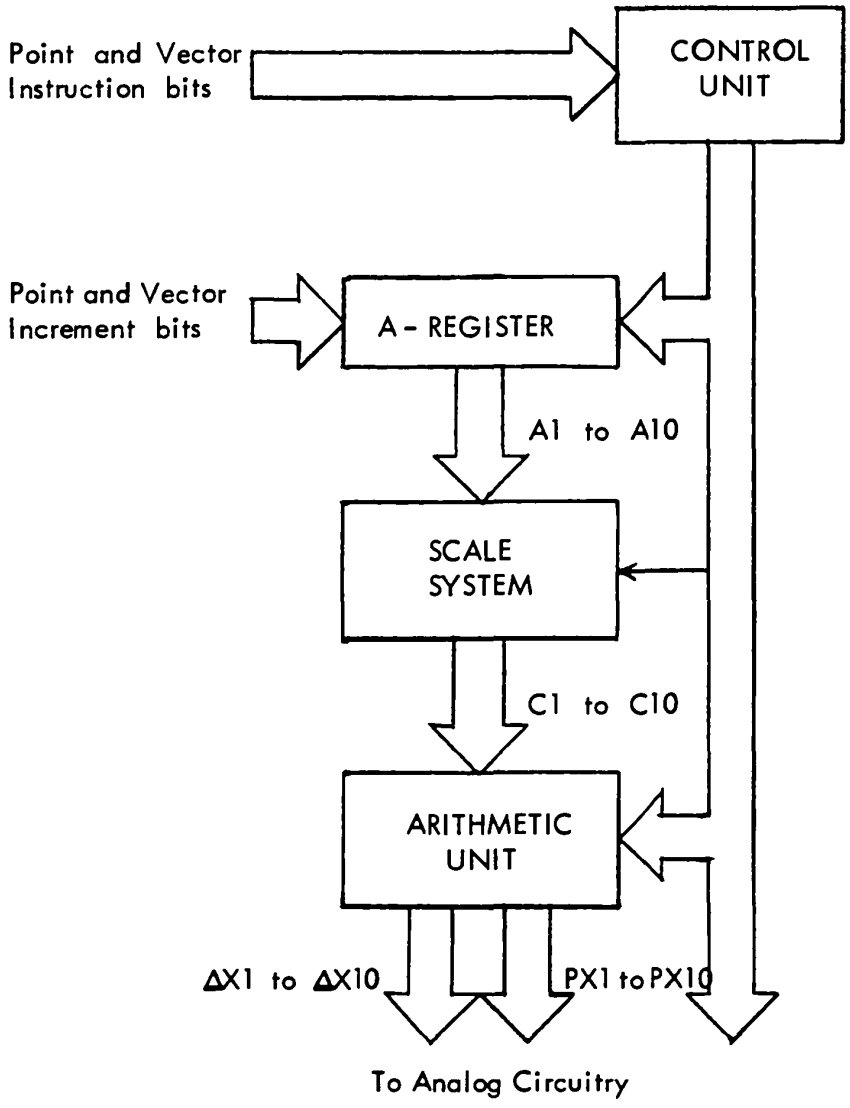

FIGURE 3.6.1 : POINTS AND VECTORS

- For a long "vector move" , the X-increment (from word 1) is placed in bit positions 1 to 3. Bits 4 to 10 are cleared and this information is processed. The Y-increment in word 2 is treated in the same manner.

The contents of the A register are fed to the scale system. The resulting information, C1 to C10 , represents a scaled move along one axis and enters an arithmetic unit (see Figure 3.4) . There are two such units, one for each axis. Both "increment" (ΔX1 to ΔX10)* and "reference point" (PX1 to PX10)* are available from each unit. "Increment" is the magnitude of a move along one axis. "Reference point" is the origin of such a move.

X- and Y-axis "reference points" are updated after each move has been completed. The increment registers of the arithmetic units are cleared before any information is entered. Thus, for a move along a single axis, both "increments" are used, one of them being zero.

Instructions are available to the system at TM8 (time 0). The time interval between TM8 and TM4 is used to decode the instruction, assemble the increment, scale it, enter it into the increment register and update the "reference points". Drawing on the CRT thus begins at TM4. However, the arithmetic unit registers only change at TM3. Therefore there is no need to terminate a move at TM8. Drawing is allowed to continue until TM3 of the next instruction, regardless of the type of instruction . Drawing time is thus at its maximum (2.1 μsec.). The interval between TM3

---

* ΔY1 to ΔY10 and PY1 to PY10 for Y-axis.

and TM4 , when no drawing occurs, allows the AU registers to settle to their new values and the integrator capacitors (see next section) to be discharged. This timing sequence is shown in Figure 3.6.2.

3.7 Analog Circuitry

Figure 3.7.1 is a schematic of the ramp generator used to drive the X-axis of the CRT. A similar device exists for the Y-axis and will not be described. The "increment" bits, $\Delta X1$ to $\Delta X10$ of Figure 3.6, enter a D/A converter. The resulting analog signal is used as is for point mode moves and for intensity modulation (Section 3.8.2) in the case of vector mode moves. When a vector move is required, this signal is integrated. The integrator consists of an operational amplifier (OA) , a feedback capacitor and an analog switch (S) to discharge the capacitor and thus reset the integrator. The switch is controlled by the logic variable INTSW (integrator switch).

However a problem is encountered when opening it to permit integration. A large transient at the gate drive is coupled into the integrating capacitor as shown in the model of Figure 3.7.2 . This distorts the desired perfect ramp yielding the waveform of Figure 3.7.4 . This was restored by a compensation which consists of feeding the positive going signal INTSW into the network of Figure 3.7.3 and then into the second OA. This yields the waveform shown in Figure 3.7.5. By applying a bias signal derived from the power supply, this ramp was raised to obtain the result shown in Figure 3.7.6 . A small bias is also applied at the input of the integrator to compensate for summing junction offset current.

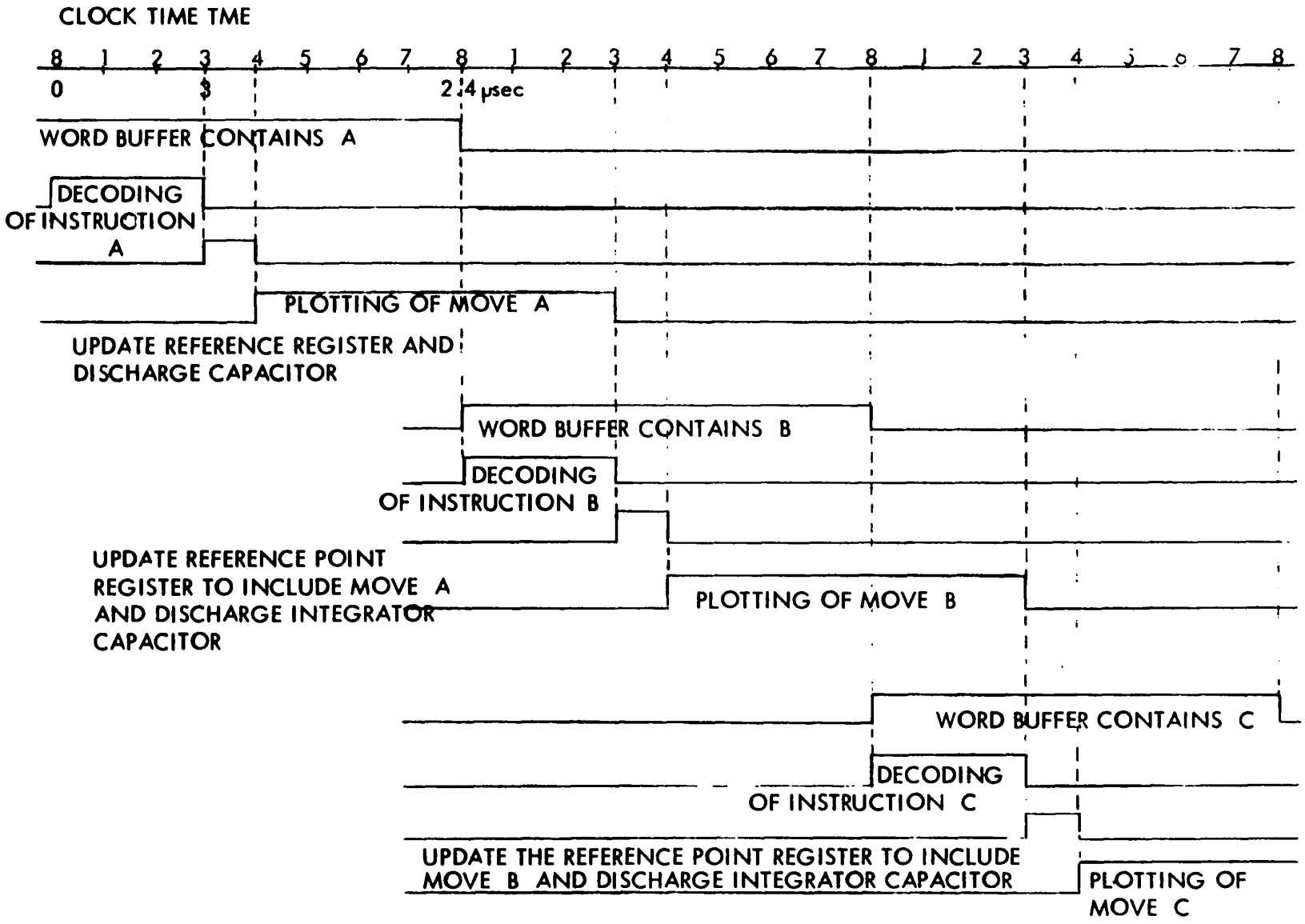

FIGURE 3.6.2 : TIMING SEQUENCE FOR THREE SUCCESSIVE POINT OR VECTOR MOVES : A , B , C.

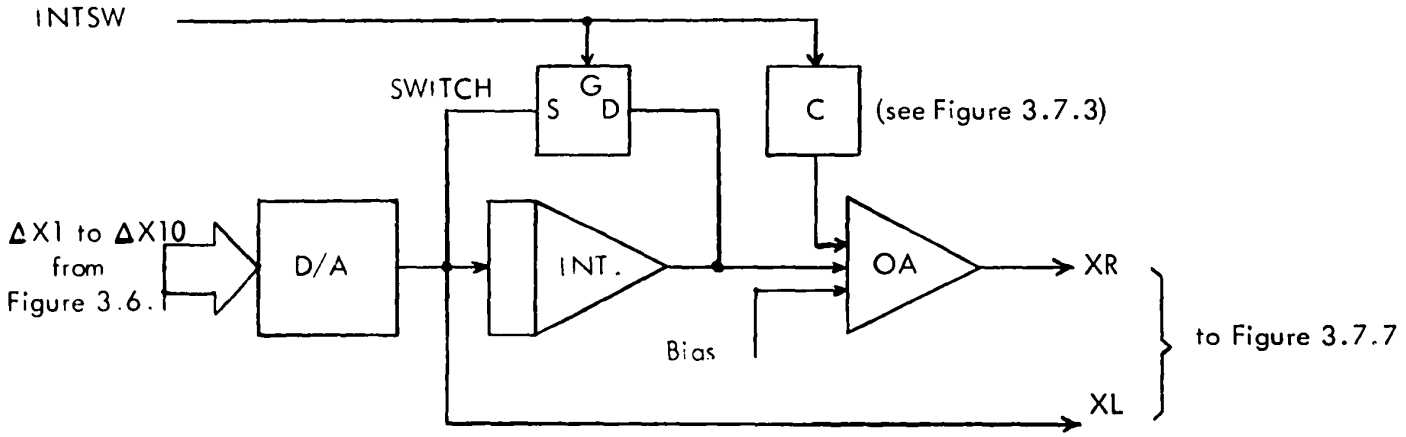

FIGURE 3.7.1 : RAMP GENERATOR

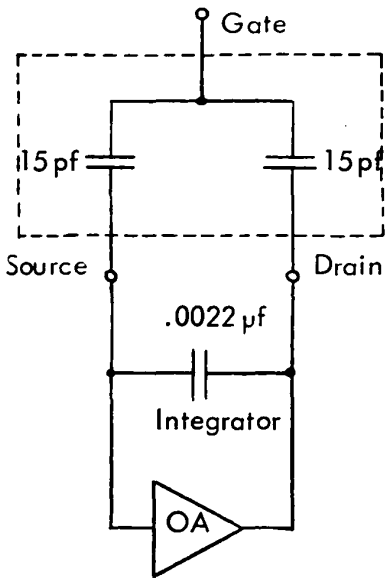

FIGURE 3.7.2 : SWITCH MODEL

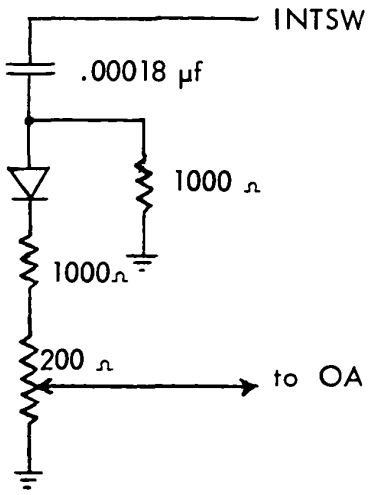

FIGURE 3.7.3 : COMPENSATION

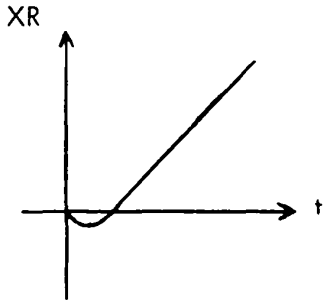

FIGURE 3.7.4

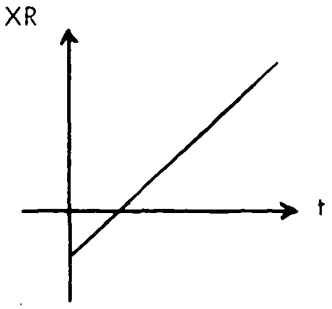

FIGURE 3.7.5

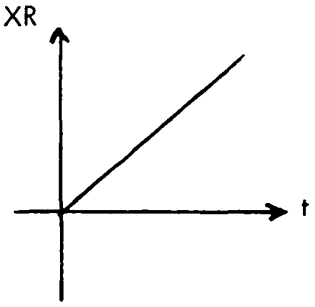

FIGURE 3.7.6

Both the ramp signal XR* and the constant signal XL* are brought to the summing circuit shown in Figure 3.7.7 . One of these signals is fed to an OA, XR being used for vector moves while XL is used for point moves. If the move is in the positive X-direction, the upper OA is used. The lower OA implements moves in the negative X-direction. The gating is accomplished by the four analog switches (S). Only one of these conducts at a time. Each has its own control signal which is not shown. The "reference point" bits PX1 to PX10 are converted to an analog signal and fed to the lower OA. Every input to the OA's is adjusted for gain by a trimmer potentiometer (T). The analog circuitry is greatly simplified by using two OA's. This is possible since the input stage of the CRT uses a differential amplifier and both input polarities are accepted. A duplicate summing circuit is used for the Y-axis.

3.8 Intensity Control

The illumination of the screen may be specified in the program. This allows some points and vectors to be made brighter than others. It was stated in Section 3.6 that drawing is allowed to proceed for 2.1 μsec. Since different length vectors may be drawn, this results in a variable writing rate (inches/μsec) on the CRT. Thus short vectors would be brighter than long ones. For simplicity, it is obviously desirable to keep the same INTENSITY specification when vectors of different lengths are to be drawn with equal brightness. Therefore it is necessary to provide some compensation whereby the Z-axis signal is automatically modulated.

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* YR and YL for Y-axis .

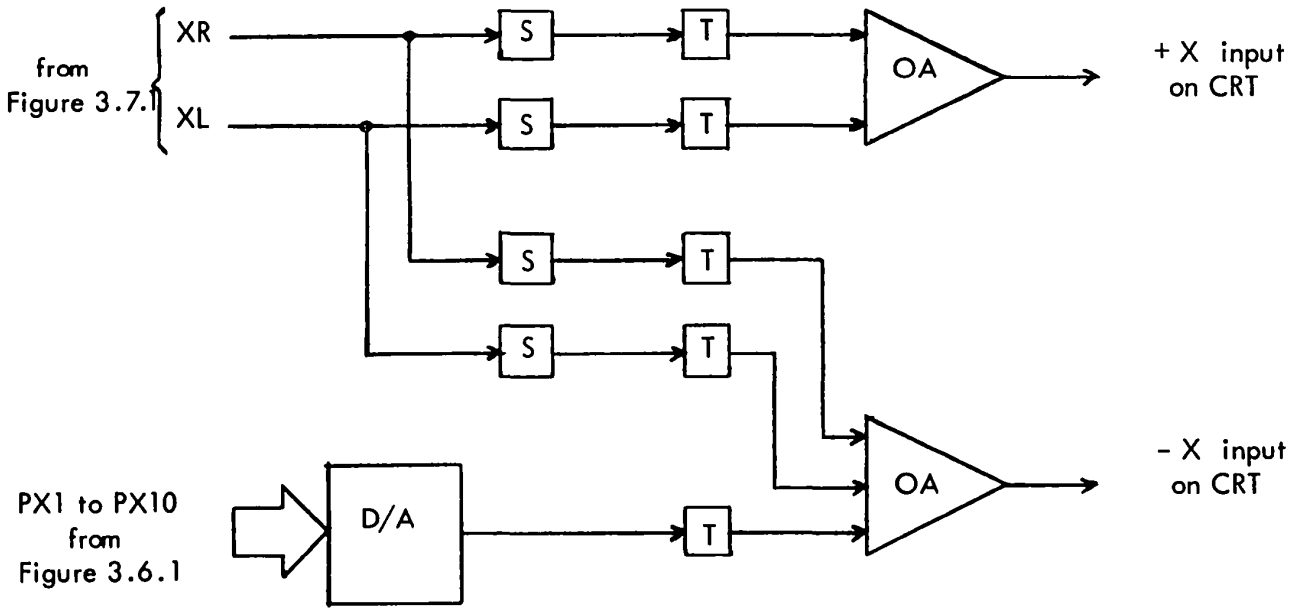


FIGURE 3.7.7 : SUMMING CIRCUIT

Experimentally, it was found that the maximum vector length which could be drawn, at a reasonable level of brightness in 2.1 μsec was 1/4 inch. Therefore the compensating circuit was designed to operate such that a 1/4" vector yields the full Z-register intensity being programmed (Section 3.8.1) . Shorter lines are drawn at a lower rate and thus the intensity of the beam is correspondingly decreased to result in a constant illumination. These features are discussed below.

3.8.1 Program Control

Instruction bits from the INTENSITY statement and timing pulses enter a control unit. This device provides control signals for four arithmetic units. There is an AU for each of the four possible CRT beams, mentioned in Section 2.2.3. In this way the increment bits of the statement are presented to the proper AU. The outputs of the AU's feed a decoder and switch control unit as shown in Figure 3.8.1 . The function of this unit is to decode the output bits of the AU's , determine which CRT beam is presently being driven and feed the output of the proper AU to the D/A converter. This sharing arrangement was chosen because of the high cost of this D/A unit. Only one CRT beam is driven at a time, however , all CRT's may be driven by drawing on each one sequentially. Since the DPU design decodes only one program this sharing does not impose any real limitations. The decoder and switch control unit also produces control signals for the four analog switches. Depending on which CRT beam is being driven, one of these switches conducts and allows the D/A output to drive this beam. The D/A converter is a special unit, whose output may be modulated as explained in the next section.

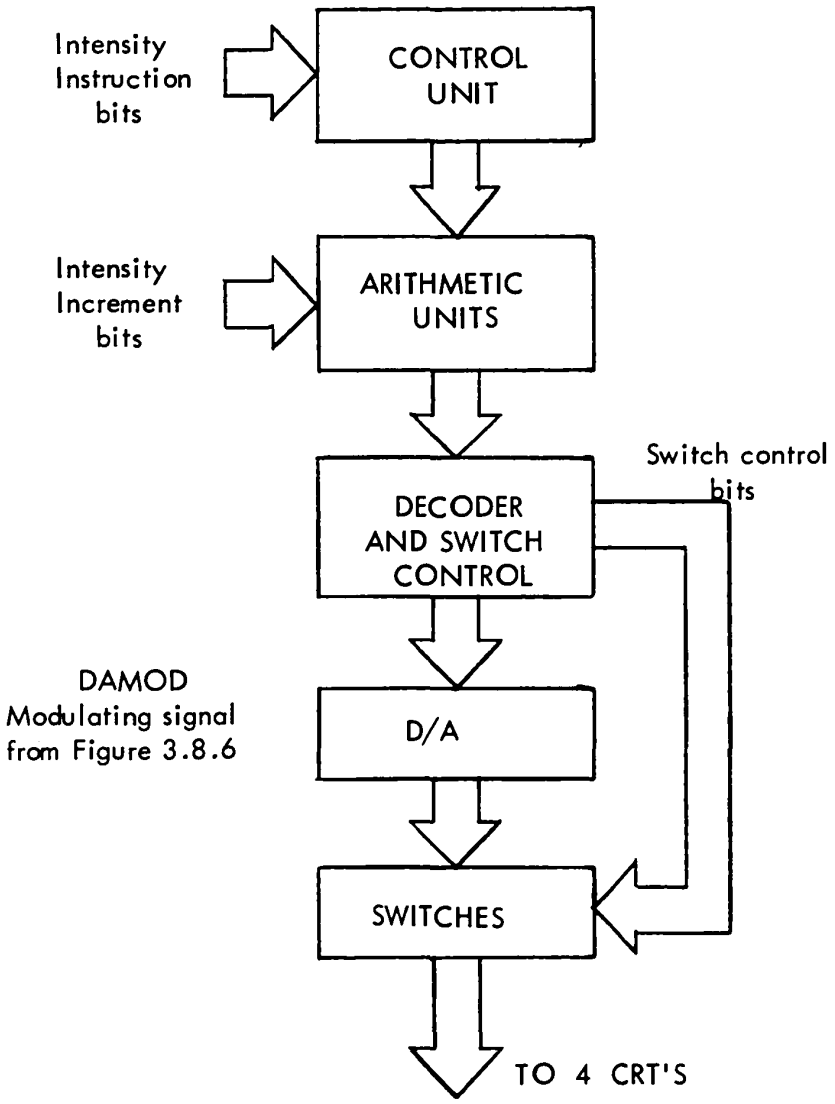


FIGURE 3.8.1 : INTENSITY CONTROL

3.8.2 Intensity Modulation

An analysis of the light emitting characteristics of the CRT was made. For this the following symbols are defined:

I - the visual brightness of a vector on the CRT face.

V - the voltage applied to the Z-axis of the CRT .

R - the rate (inches/μsec) at which a vector is drawn.

L - the length of a vector.

a,b,c - positive constants of any value, where $a < b < c$.

Figure 3.8.2. shows the relationship between I and V for different values of R. These curves are deduced from the following. First, for a given R , I must increase as V increases. I tends to the limit I_{max} at high V as the amount of light emitted by the phosphor reaches a maximum. Secondly, I increases faster, with increasing V as R is decreased (curve 3 to curve 1).

Figure 3.8.3 represents the same information in a different form. Again I is limited between zero and I_{max} .

In order to obtain a relationship between V and R, the curves of Figure 3.8.2 or 3.8.3 are translated to obtain those of Figure 3.8.4 . These curves show that, for a given I, V should be proportional to R. Although these curves are shown as straight lines, they may in fact be slightly curved. This is not serious however for reasons explained later.

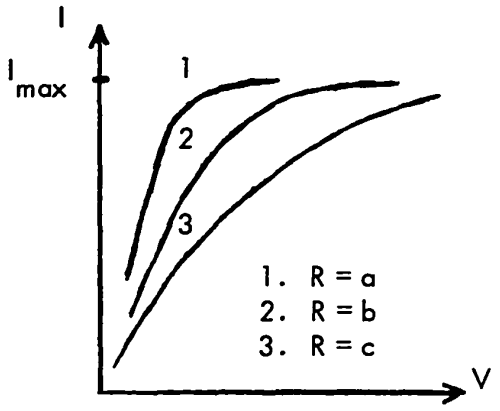


FIGURE 3.8.2.: I VS V FOR CONSTANT R

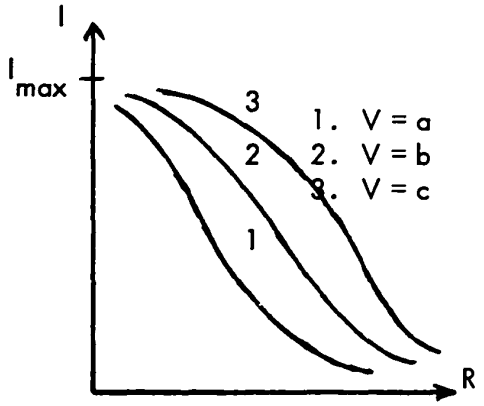


FIGURE 3.8.3 : I VS R FOR CONSTANT V

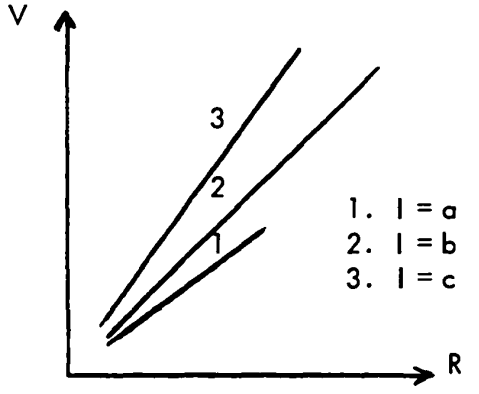


FIGURE 3.8.4 : V VS R FOR CONSTANT I

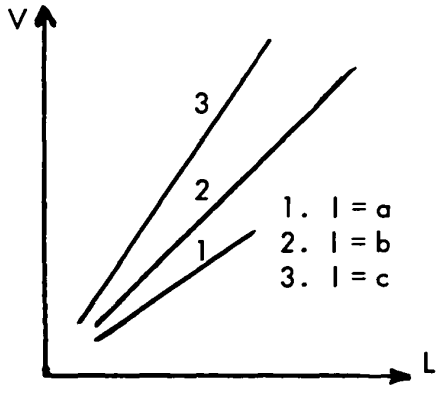


FIGURE 3.8.5 : V VS L FOR CONSTANT I

Finally R is exactly proportional to L and the curves of Figure 3.8.5 are obtained. The interpretation of these curves is as follows. For a given desired illumination, the voltage applied to the CRT Z-axis input must be proportional to the length of the vector being drawn.

Let XL and YL represent the X- and Y- components of a vector move. The true length VL of such a vector would be

$$VL = \sqrt{(XL)^2 + (YL)^2} \quad .$$

The implementation of such a function would require two squaring and one square root elements. Each of these elements would consist of an operational amplifier with diode input or feedback. Due to the high speed requirements, this circuit would become quite expensive.

The circuit of Figure 3.8.6 was implemented instead. It is a simple summing circuit with a limiting network to prevent overloading the succeeding stages. In this case, VL is represented by

$$VL = XL + YL \quad .$$

For moves along one axis, the result is true. For moves at an arbitrary angle, the difference (error , E) between computed VL and true VL is

$$E = XL + YL - \sqrt{(XL)^2 + (YL)^2} \quad .$$

It may be shown that E reaches a maximum of 41.5% for a 45° vector move. However,

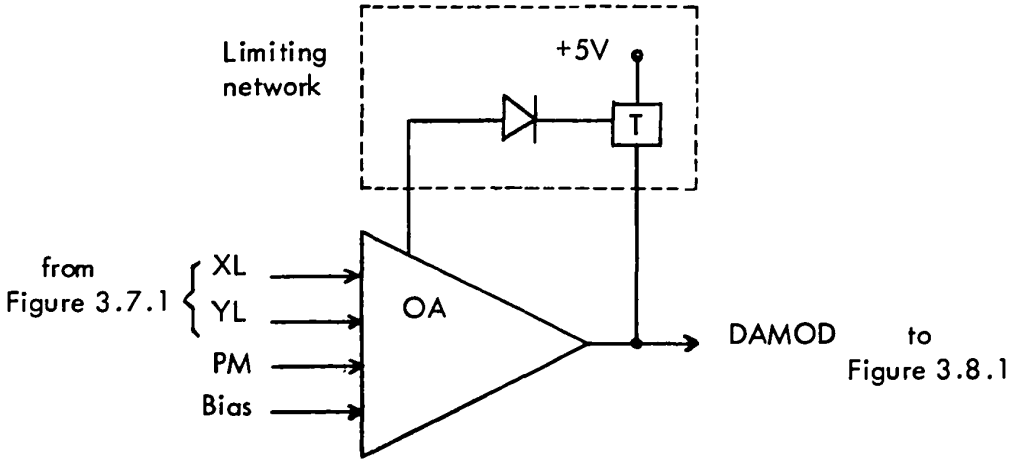


FIGURE 3.8.6 : INTENSITY MODULATION

due to the highly logarithmic quality of the eye, such an error is hardly noticeable.

The output of the circuit of Figure 3.8.6 is used to modulate the D/A of Figure 3.8.1 , providing even illumination for different length vectors.

Since all points are plotted during a constant time interval, there is no need to modulate the intensity. Instead, a point mode signal (PM) is also applied to the summing circuit of Figure 3.8.6 to saturate the output and make it independent of XL and YL variations.

3.9 PDP-8 Interface

Since both HEADER and BRANCH statements may interrupt the PDP-8 , their interrupt pulses are fed to a logic circuit which allows either of them to set a flip-flop. The output is an interrupt level to the interface which accepts the file name register bits and sends them on to the computer. (See Figure 3.9) . The flip-flop is reset by a pulse from the PDP-8, once it has accepted the information. The computer may also transmit 12 bits of information to the interface. Presently, these are not used but are simply available on a panel of connectors.

The circuitry and operation of the interface are discussed in Reference (7).

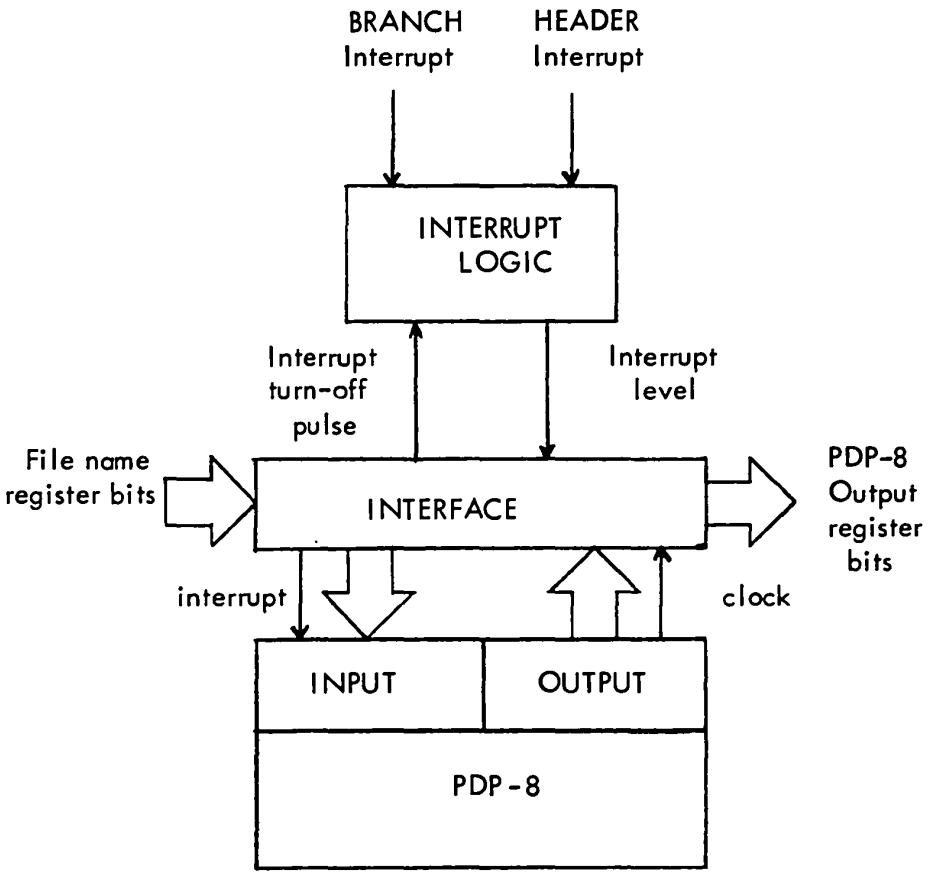


FIGURE 3.9: PDP-8 INTERFACE

CHAPTER IV

THE HARDWARE

This section deals with the various components that were used to construct the system. Some of them were purchased as complete units, for example the power supplies and the Z-axis D/A converter, while others such as the digital integrated circuits, D/A units, operational amplifiers, were purchased as modules to be mounted on printed circuit boards. The circuit boards were etched and assembled at the University as will be described in Section 4.2 . Other aspects of the system construction which will be discussed include wiring, cabling and cooling.

4.1 Selection of Components

In designing a system, it is often difficult to select components on the basis of quality or price. Other criteria which influence the selection include previous experience on existing equipment, sales literature and availability from a local supplier. Thus different components are selected for different reasons. In discussing these reasons, we shall separate the components into two groups: first the circuit boards and the wiring panel, and secondly the electronics proper, including power supplies.

4.1.1 Panel and Boards

It is obvious, at this particular point in history, that the electronics necessary to build the system will be of the integrated circuit type. It was estimated

that roughly three-hundred integrated circuits would be used. Six such IC's can easily be placed on an average size circuit board, requiring fifty such boards.

Because of previous experience in building and interfacing to the DEC computer and accessories, DEC circuit boards were selected. It was decided that the IC's would be mounted on DEC W993 (5 3/16" x 3 5/8") and W992 (2 7/16" x 3 5/8") circuit boards; these boards are copper-clad on one side, with gold-plated contacts, and are ready for etching. The purchase of DEC logic boards (pre-assembled circuits) was considered and found to be quite expensive. In addition, a lesser degree of compactness and increased wiring complexity would have resulted so this alternative was discarded.

A mounting panel is also available from DEC to accept the circuit boards on one side and provides wire-wrapping pins on the other. Each panel (DEC 1943) accepts thirty-two W993 boards, so two were sufficient for the circuit and were purchased . Busing strips were used for power connections and hold-down bars for securing the boards in place.

4.1.2 Electronics

The selection of the electronic components was a much more difficult task. Since the speed of the system is quite high, quality components were needed which often reflected the state of the art. The digital to analog conversion modules selected are the Minidacs manufactured by Pastoriza Electronics Inc. (now a division of Analog Devices Inc.) which have a settling time of 200 nsec.

A fast D/A converter whose output could be modulated was then needed to control the beam intensity. A Computer Labs model HS2425 was examined, found suitable for this purpose and purchased. It has a settling time of 80 nsec. The operational amplifiers used by Computer Labs in obtaining these impressive results are their own OA-125 op amps. These OA's have a gain-bandwidth product of 125 MHz, a slew rate of 250 volts/μsec, with an output range of ±1 volt into a 100 ohm load. These units were then chosen to implement the ramp generator, summing and intensity compensation circuits.

The switches obviously had to be electronic in nature since switching speeds in the low nanosecond range were required to minimize the picture deterioration. Extremely low ON resistance was required to discharge the integrator capacitor of Figure 3.7.2 in a relatively short time. As it turns out, the 200 nsec settling time for the Minidac has dictated a 300 nsec discharge time with a 2.1 μsec drawing time. Crystallonics FET analog switches, with a settling time of 50 nsec and 6 Ω ON resistance were purchased despite their high cost. Several other switches, with slightly higher ON resistance but lower in cost were also purchased from Crystallonics for use in the summing circuit of Figure 3.7.7.

The digital devices (gates, flip-flops, etc) were chosen in the dual-in-line package for easy mounting. Several companies manufacture these but the choice was narrowed down to two, due to local availability. Both Motorola and Texas Instruments offer a complete line of logic devices with speed characteristics within system specifications. Texas Instruments was finally chosen because of faster delivery in the Montreal area. All digital circuitry used is TTL (transistor-transistor-logic) . Indi-

vidual resistors, capacitors and diodes are used in the analog portion of the system only. Wirewound trimmers caused some problems because of their associated inductance so carbon resistors were preferred. In general, mylar capacitors and carbon resistors were used. Should system stability be poor on account of this, they could be replaced by higher quality types.

Many manufacturers offer a wide range of power supplies. Lambda power supplies were used. The digital circuitry requires a five-volt supply. It was estimated that four to five amperes would be required and a model LM-CC5-Y unit was purchased, with a current rating of 5.5A . The analog circuitry required two fifteen-volt supplies at one ampere so two model LM-B15-Y units, rated at 1.3A , were purchased. Overvoltage protectors were installed on each unit. The supplies are rack mounted, using a model LRA-3 rack adapter and an LBP-40 blank cover panel.

4.2 Construction

Building the system was an experience in itself and required the learning of new skills. The main part, certainly the most time-consuming, was making the printed circuits. Most of this work was done by the author. Other chores such as wiring the system and making cables for interconnection to other devices were done in the electronics workshop, or by undergraduate students, hired on a temporary basis.

4.2.1 Printed Circuits

As previously explained, it was decided that the printed circuit boards would be constructed here at the University. This involved the following steps.

1. Layout : After deciding which components to place on a board, their spacing is roughly determined and jumper wires are shown since only one side of the board is copper-clad.

2. Scaling: The above layout is reproduced to scale to ensure that all components and wires fit onto the board. This diagram also shows the exact location of drill holes.

3. Drilling: The above diagram is taped to the board and all required holes are drilled .

4. Taping: Once drilled, the board is taped. Specic! tape, 0.31" wide for signal lines and .080" wide for power lines, is laid onto the board where conductors are to be left.

5. Etching: A solution of ferric chloride is prepared in a photo developing tray. The taped boards are then placed in this tray which must be agitated. The agitation process was motorized, as shown in Figure 4.1 . Here, up to four large boards may be etched at a time with one solution.

6. Tinning: Some form of protection against oxidation of the copper must be provided once the boards are etched since a fair amount of time elapses between the etching and the soldering of components. It was found that tinning was the best method. In order to avoid the long and tedious process of hand tinning, a bath was constructed in the machine shop, as shown in Figure 4.2 . The bath consists of a

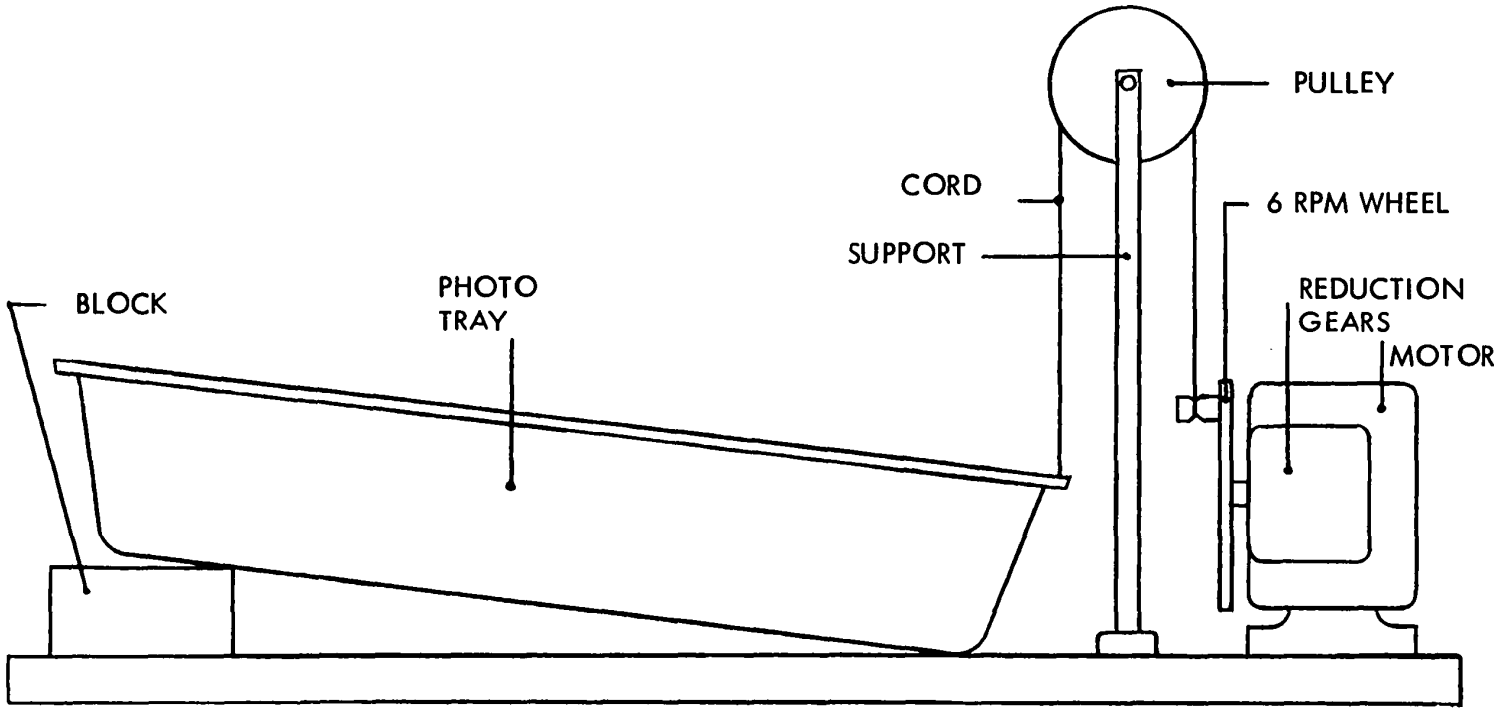


FIGURE 4.1 : AGITATION PROCESS

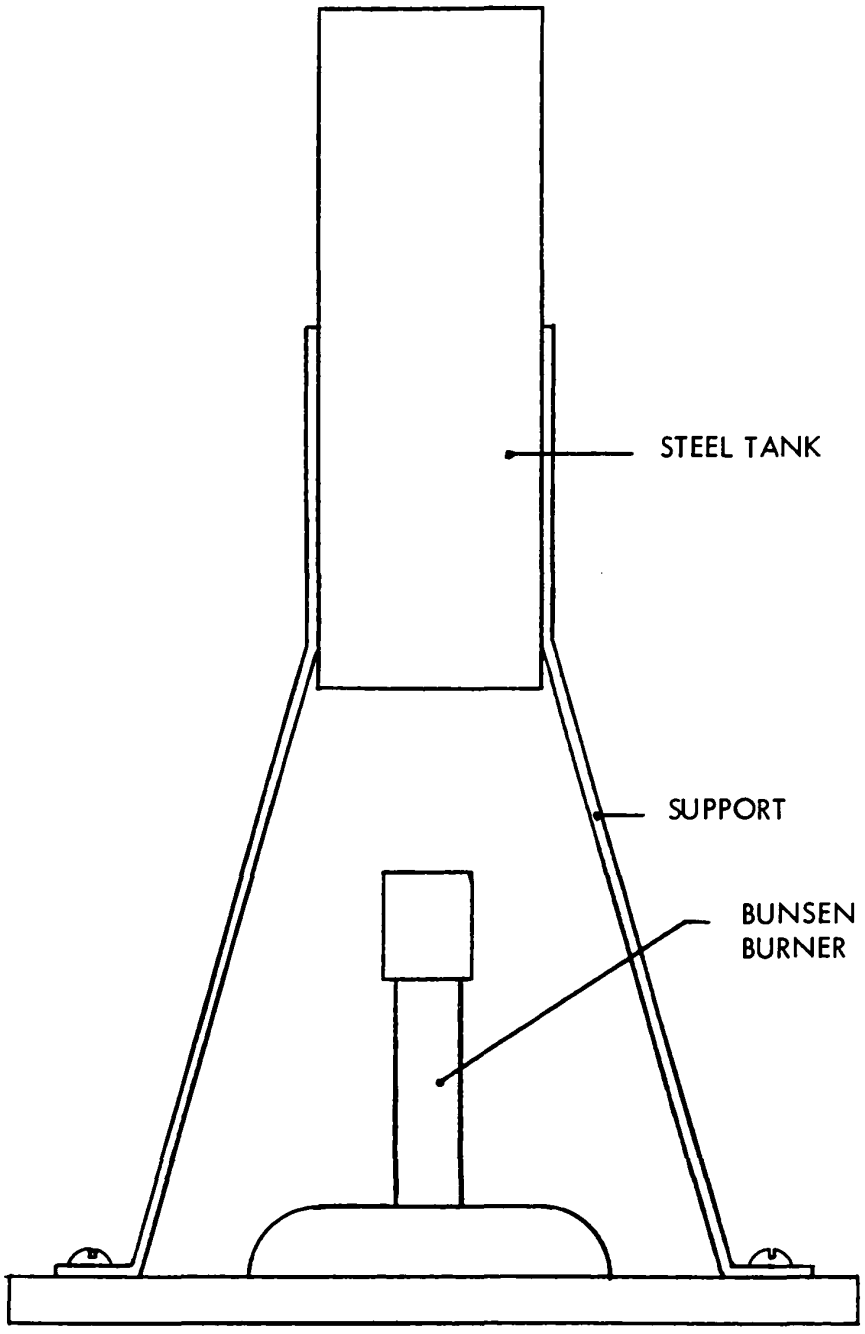


FIGURE 4.2 : TINNING TANK

steel tank, supported over a bunsen burner, into which is melted 60/40 alloy bar solder. The boards are first painted with non-corrosive solder flux on both sides to avoid blistering when they are dipped, one by one, in the molten solder. They are then cleaned in chlorethene to remove excess flux, leaving them ready to accept components.

7. Mounting: The components (IC's , wires, resistors, capacitors, sockets) are now soldered onto the boards using a low-power (25 to 50 watts) iron.

The Digital Equipment boards are provided with handles which were riveted on, and onto which were affixed pre-made labels identifying the circuit in question. Once completed the circuits were tested as described in Chapter V and plugged into the appropriate location in the panel. After completion, a hold-down bar clamps down on all the boards to hold them securely in place.

4.2.2 Wiring

As mentioned earlier, the rear of the mounting panel contains pins suitable for interconnecting the circuit baords by the wire-wrapping technique. Using a special tool, two inches of the wire are skinned bare and twisted around the pin. This is an approved method, providing excellent and reliable contact and is considered safer than soldering, where insulation may melt.

4.2.3 Cables

Various cables were required to interconnect the system to other apparatus. The input lines from the disc as well as connections to the D/A converter and the CRT are high-speed lines. For this reason coaxial cable (RG - 59 C/U) was used. Wherever possible, the connectors were made using a circuit board onto which the cables were clamped and soldered. Where required by commercially purchased items, BNC connectors were used.

Nine-conductor shielded cable was used for I/O to the track selection switches and to the PDP-8 interface.

4.2.4 Mounting

The complete system was mounted as shown in Figure 4.3 in a standard nineteen-inch rack mounting cabinet, with forty-nine inches of vertical mounting space. Nominal panel height is 5 1/4 inches; the CRT is 15 3/4 inches high, occupying three rack spaces and was located first, to allow comfortable viewing, in space C of the figure. Below it is placed the control panel (space D) and the D/A converter (space E). This arrangement permits the mounting of a shelf in front of the D/A converter without interference.

Enough space remains for the two racks of electronics and the power supplies. The power supplies were placed at the bottom (H) since they should require the minimum of maintenance and adjustment. Spaces F and G accept the logic circuits.

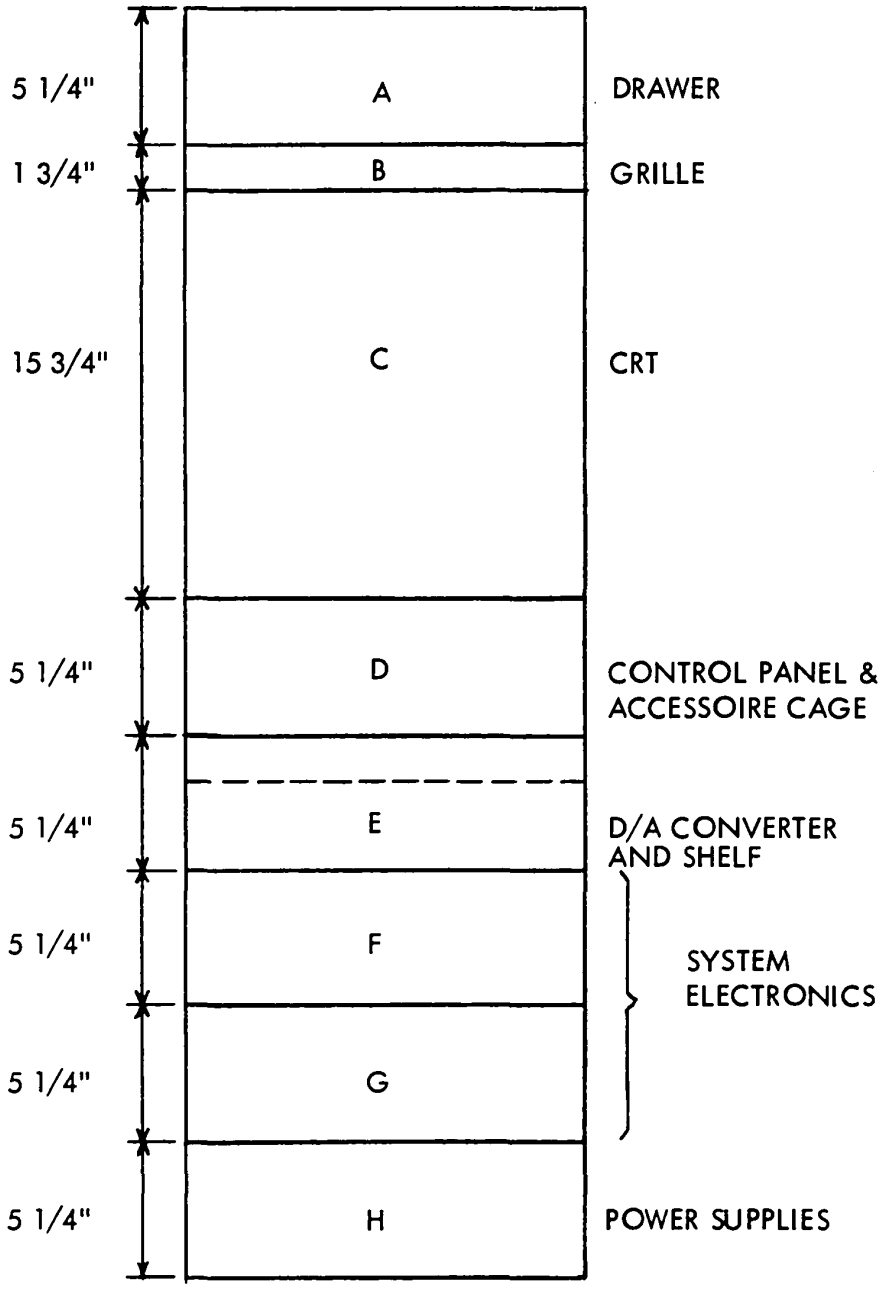


FIGURE 4.3 : CABINET MOUNTING

Finally a drawer was placed in A, the remaining 1 3/4" being filled by a ventillation grille. The power supply of the CRT is placed behind those of space H.

Forced ventillation is accomplished using a pair of small a.c. fans placed as shown in Figure 4.4 . This diagram also shows the direction of air flow. It should be noted that the CRT is equipped with its own fan, drawing air from below and expelling it at the rear. Thus the fans blow cool air from outside onto the logic and power supplies. This air is drawn upward, around the D/A and through the accessary cage by the CRT and is then expelled out the rear of the cabinet through the lowered door. A generally upward path was chosen on account of the CRT fan and also not to work against natural convection.

A single input power line leads to the control panel where it is split into two circuits. Each is fused (15A) , switched and provided with an indicator light. One circuit is labelled GRAPHICS LOGIC and feeds the power supplies as well as the ventillation fans. The other, labelled CRT & ACC feeds the CRT power supply and the light pen. The joystick does not require a.c. power but uses a special multi-circuit connector to obtain d.c. power from the graphics system's power supplies.

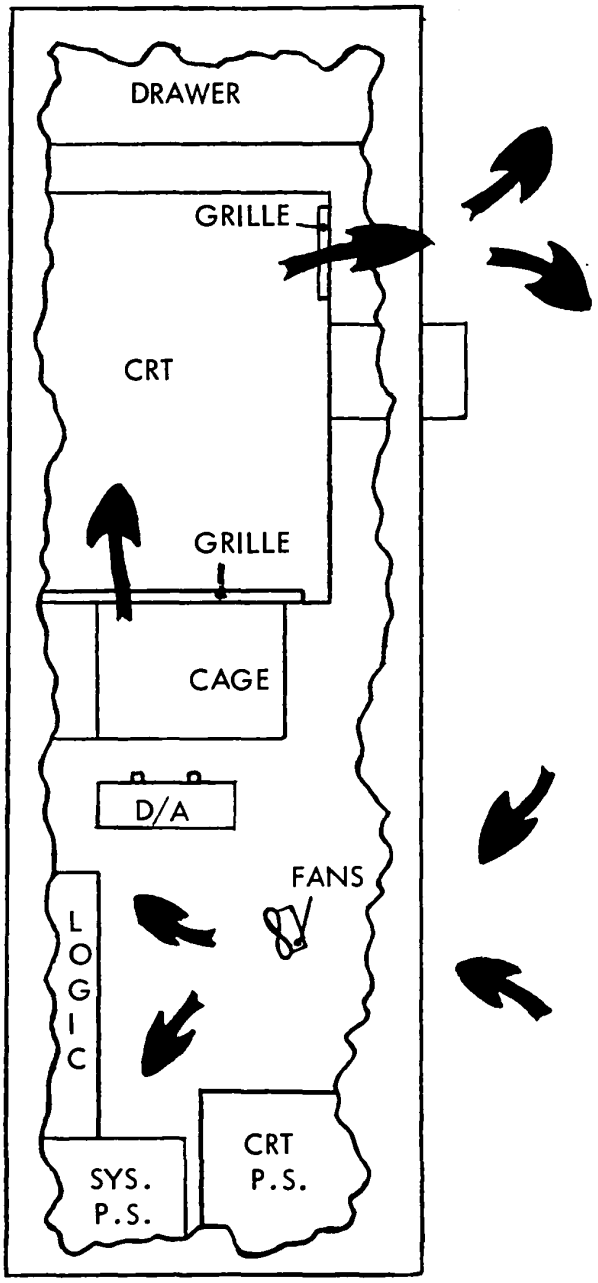


FIGURE 4.4 : VENTILLATION

CHAPTER V

TESTING

Considerable time was spent testing the various parts of the system before final completion. Most components were tested individually to assure that they met the manufacturer's published specifications. Later, as individual circuit boards were assembled, these were also tested to assure that the design was correct. Finally the wiring of the panel was also verified.

It is unfortunate that at this time it was impossible to test the system as a whole since the interface between computer and disc was not complete. However, it is hoped that this will be possible in the near future.

5.1 The Components

The components which were tested individually are the D/A converter, the D/A modules, the operational amplifiers and the analog switches. The power supplies were simply turned on and the overvoltage protector adjusted according to instructions. All were found to be in good operating condition. As for the digital integrated circuits, these were not tested until a circuit board was complete.

5.1.1 D/A Converter

This device, purchased as a unit was tested for accuracy by providing level inputs to the unit and measuring the output voltage. The RANGE and

BIAS controls were varied and found to be operating satisfactorily. Next, fast pulses were fed to the unit which settled to .1% accuracy in the specified time of 80 nsec.

5.1.2 D/A Modules

These devices were tested by constructing a test board of ten toggle switches, each representing one bit and gating a level or a pulse. Each unit was tested for accuracy and speed.

5.1.3 Operational Amplifiers

Into each op-amp was fed a square wave. The outputs were checked for rise-time and maximum voltage and all were satisfactory.

5.1.4 Analog Switches

Each unit was tested for speed of response and resistance by applying a one-volt square wave to the source terminal and resistively loading the drain terminal. Results were within specifications .

5.2 Circuit Boards

Each circuit was individually tested by plugging it into the wire-wrapped panel and providing the necessary input levels by means of toggle switches and a pulse generator. The output was read using a vacuum tube voltmeter and a high-speed sampling oscilloscope.

5.2.1 Digital Circuits

These boards were plugged into the panel which was to be used in the system. Generally, only one board was tested at a time, except in cases where a group of boards performed a simply-tested function. Most gate inputs were wired to ground or to +5V and a pulse generator, in its single pulse mode, provided a clock input to the flip-flops. Preset and Clear inputs were left open and touched to ground when necessary. The outputs were read on a voltmeter. Every possible combination of inputs was tried to assure that the circuit was working well. This also provided a test for the integrated circuits, roughly two percent of which were found to be defective and replaced. There were very few mistakes in the etching of the boards, since each had previously been checked with an ohm-meter for continuity and possible short circuits.

5.2.2 Analog Circuits

These boards were inserted into another blank panel which was temporarily wire-wrapped for the specific purpose of testing these circuits. The test board of ten toggle switches provided inputs to the D/A modules and the pulse generator controlled the integrator capacitor; the sampling scope was used to monitor the output as well as intermediate stages. The boards containing the integrator were tested first, at which point a great deal of re-designing was required to correct for unwanted transients from the analog switches, offset of the op-amps and improper loading of the D/A modules. Then the following board, containing the switches for point or vector mode and positive or negative increment, was added and the combination was tested. As expected this offered little difficulty, only the required trimming to provide the proper output voltage levels.

Finally, the circuit which allows the D/A converter to be modulated was tested and trimmed.

5.3 Wiring

A tester, consisting of a buzzer in series with a battery and two test probes, was constructed to check the wire-wrapping of the panel. A few mistakes were found and corrected. Cables were checked with an ohm-meter for continuity and correctness.

CHAPTER VI

DISCUSSION AND OPERATION

6.1 Conclusion

Since the inception of this project, nearly two years ago, the author has gained valuable experience and learned many things. First, that careful design of the system, the preparation of the method of construction, the lengthy search for and subsequent selection of components can yield fruitful results. By following this systematic approach, many hours of work were saved and the various parts of the system were found to be logically correct the first time they were tested. Secondly, what seemed like excessive or wasted effort spent in making a piece of equipment easy to use, logically laid out down to the smallest detail, as well as aesthetically pleasing to the eye, does provide a pride of workmanship which is infinitely rewarding. However, the implementation of the project did give rise to certain questions. For example, one such aspect was the construction and assembly of circuit boards when such circuits could be purchased, already assembled, commercially. Although a saving in space and dollars was achieved, this took its price in other ways. The author estimates that as much as six months were devoted to building and testing these circuits. It is hoped that the reduction in space and wiring complexity results in an improvement in the operation of the circuit, although this can never be proven. However the benefits realized by having the opportunity to exercise and develop one's mechanical skills as well as his intellectual capacity cannot be overlooked.

6.2 An Example

In order to illustrate the operation of the system, an example will now be given. The object of the exercise is to draw a triangle on the screen as shown in Figure 6.2.1. The triangle is a right-angled one, for simplicity, and is centered on the screen, that is at X = 6" and Y = 5" . The origin is the lower left-hand corner of the screen.

The program is listed in Table 6.1 . Instructions 1 to 8 prepare the system for operation and may be replaced by HEADER , INTENSITY and SCALE assembly language statements. Instructions 9 to 12 bring the CRT beam to reference point A of Figure 6.2.1 . A POINT statement would be required . Instructions 13 to 30 execute three vector traces on the screen and thus may be replaced by three VECTOR statements. Finally, instruction 31, which returns the system to the COMMAND mode, in order that the next instruction, if any, may be decoded as a HEADER, would simply be an END statement in mnemonic code.

Thus, although the program of Table 6.1 appears lengthy for a mere triangle (31 statements), an assembly language version might consist of the eight statements of the test routine of Section 6.3.3.

6.3 Test Routines

In order to provide the operator with a quick test of the system several test routines are presented in mnemonic code. This code, which is not a final design,

TABLE 6.1

SAMPLE PROGRAM

No.	Statement	Explanation
1	10100000 001010011	HEADER. File name=0123. Display file. Interrupt PDP-8.
2	11000000	Put system in COMMAND mode.
3	00100000	Enter INTENSITY mode.
4	00001111	Turn INTENSITY of CRT1 full ON.
5	11000000	Return to COMMAND mode.
6	00110000	Enter SCALE mode.
7	00000001	Scale of 1 on X-axis.
8	00100001	Scale of 1 on Y-axis.
9	11000000	Return to COMMAND mode.
10	00000000	Enter POINT mode.
11	00011000 00101100	Move 5.5" to the right. No plot.
12	00111000 00100100	Move 4.5" upward. No plot. (Point A)
13	11000000	Return to COMMAND mode.
14	00010000	Enter VECTOR mode.
15	01000111	Draw VECTOR 7/32" to the right.
16	01000111	Draw VECTOR 7/32" to the right.
17	01000111	Draw VECTOR 7/32" to the right.

TABLE 6.1 (continued)

No.	Statement	Explanation
18	01000111	Draw VECTOR 7/32" to the right.
19	01000100	Draw VECTOR 1/8" to the right.(Point B)
20	01100111	Draw VECTOR 7/32" upward.
21	01100111	Draw VECTOR 7/32" upward.
22	01100111	Draw VECTOR 7/32" upward.
23	01100111	Draw VECTOR 7/32" upward.
24	01100100	Draw VECTOR 1/8" upward. (Point C)
25	10010000	Establish negative direction for X.
26	10101111 11100000	Draw VECTOR to the left and downward, 7/32" in each direction.
27	10101111 11100000	Draw VECTOR to the left and downward, 7/32" in each direction.
28	10101111 1110000	Draw VECTOR to the left and downward, 7/32" in each direction.
29	10101111 1110000	Draw VECTOR to the left and downward, 7/32" in each direction.
30	10101100 10000000	Draw VECTOR to the left and downward, 1/8" in each direction. (Point A)
31	11000000	Return to COMMAND mode.

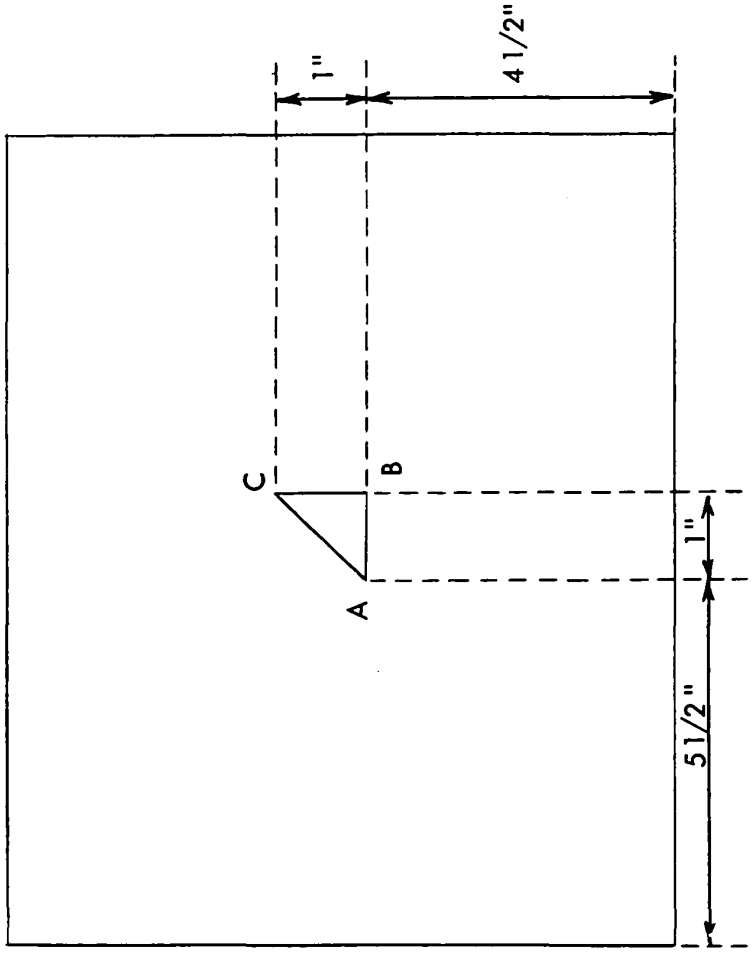


FIGURE 6.2.1 : AN EXAMPLE

TABLE 6.2

MNEMONIC CODE

Statement	Parameters	Explanation of Parameters
HEADER	n_1 , n_2 , n_3 , n_4	File name (0 to 7777 octal)/track number (1 to 16)/ display file (1) or not (0)/ interrupt PDP-8 (1) or not (0) .
BRANCH	n_1 , n_2 , n_3	Track number (1 to 16)/ wait for track origin (1) or not (0)/ interrupt PDP-8 (1) or not (0).
INTENSITY	n_1 , n_2 , n_3	Clear (1) or not (0)/ increment (-15 to +15 ; +15 = full ON)/ CRT number (1 to 4).
SCALE	n_1 , n_2 , n_3 , n_4	Clear (1) or not (0)/ X-increment (-7 to +7 ; +7 = max.)/ Y-increment/ picture upright (0) or inverted (1).
POINT	n_1 , f_2 , f_3 , n_4	Clear (1) or not (0)/ X-increment (-12.0 to +12.0 ; +12.0 = max.)/ Y-increment (+10.0 = max)/ Display (1) or not (0).
VECTOR	n_1 , f_2 , f_3 , n_4	Clear (1) or not (0) X-increment (-12.0 to +12.0 ; +12.0 = max.)/ Y-increment (+10.0 = max) / Display (1) or not (0).
END		

should serve well for that purpose. In any case it does contain a full set of instructions. The code is explained in Table 6.2 . Parameters " n " signify a signed or unsigned integer, whereas "f" represents a signed or unsigned decimal number.

Certain limits are set in the explanation of the table; they should be strictly adhered to lest erroneous results occur. While increments may be positive or negative, care should be taken that the result of such an instruction does not cause a variable to become negative nor to exceed its maximum permissible value (= max) .

6.3.1 HEADER

In order to test the operation of the HEADER statement, the following routine is proposed:

```
HEADER , 0123, 1 , 0 , 1
END
```

The result of the above is to interrupt the PDP-8, at which time it may read the file name register and print it on the teletype; it is also possible to obtain the file name at the PDP-8 interface.

6.3.2 POINT

The following routine is a test of the accuracy of the POINT plot mechanism:

```
HEADER , 0123, 1 , 1 , 0
SCALE , 1 , 1 , 1 , 0
INTENSITY , 1 , 15 , 1
```

```
POINT , 1 , 5.5 , 4.5 , 1
POINT , 0 , 1. , 0. , 1
POINT , 0 , 0. , 1. , 1
POINT , 0 , -1. , 0. , 1
POINT , 0 , 0. , -1. , 1
END
```

A set of four points, representing the four corners of a one-inch square should appear on the screen. The lower left-hand point is plotted twice and of course, both plots must coincide; failure to do so is an indication that the arithmetic units are not functioning properly. Separation of exactly one inch between adjacent points shows the gain of the analog circuits to be properly calibrated.

6.3.3 VECTOR

The following test is to verify that the integrators are functioning properly.

```
HEADER , 0123 , 1 , 1 , 0
SCALE , 1 , 1 , 1 , 0
INTENSITY , 1 , 15 , 1
POINT , 1 , 5.5 , 4.5 , 0
VECTOR , 0 , 1. , 0. , 1
VECTOR , 0 , 0. , 1. , 1
VECTOR , 0 , -1. , -1. , 1
END
```

Since the arithmetic units are those used for POINT , this test should only be performed once the preceeding one has been successfully completed.

The pattern displayed in the center of the screen is a right-angled triangle, with one-inch sides. Failure of all sides to meet exactly signifies that the analog circuitry is in need of calibration.

6.3.4 INTENSITY

This routine is to verify the operation of the INTENSITY instruction.

```
HEADER , 0 123, 1 , 1 , 0
SCALE , 1 , 1 , 1 , 0
INTENSITY , 1 , 1
POINT , 1 , 4., 4., 0
VECTOR , 0 , 0., 1., 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25, -1., 0
VECTOR , 0 , 0., 1., 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25, -1., 0
VECTOR , 0 , 0., 1., 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25, -1., 0
VECTOR , 0 , 0., 1., 1
```

```
INTENSITY , 0 , 1 , 1
POINT , 0 , .25 , -1. , 0
VECTOR , 0 , 0. , 1. , 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25 , -1. , 0
VECTOR , 0 , 0. , 1. , 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25 , -1. , 0
VECTOR , 0 , 0. , 1. , 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25 , -1. , 0
VECTOR , 0 , 0. , 1. , 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25 , -1. , 0
VECTOR , 0 , 0. , 1. , 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25 , -1. , 0
VECTOR , 0 , 0. , 1. , 1
INTENSITY , 0, 1 , 1
POINT , 0 , .25 , -1. , 0
VECTOR , 0 , 0. , 1. , 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25 , -1. , 0
```

```
VECTOR , 0 , 0. , 1. , 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25, -1. , 0
VECTOR , 0 , 0. , 1. , 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25, -1. , 0
VECTOR , 0 , 0., 1. , 1
INTENSITY , 0 , 1 , 1
POINT , 0 , .25, -1. , 0
VECTOR , 0 , 0. , 1. , 1
END
```

Fifteen vertical one-inch bars should appear on the screen. An increase in illumination of the bars, from left to right, indicates proper functioning of the INTENSITY circuitry.

6.3.5 SCALE

This feature may be tested by the following routine:

```
HEADER , 0123, 1 , 1 , 0
SCALE , 1 , 1 , 1 , 0
INTENSITY , 1 , 15 , 1
POINT , 1 , 5.5, 4.5, 0
VECTOR , 0 , 0. , 1. , 1
POINT , 0 , 1. , -1.5, 0
```

```
SCALE , 0 , 2 , 2 , 0
VECTOR , 0 , 0. , 1. , 1
END
```

Two vertical lines will appear on the screen, the first, one inch in length and the second, two inches. A difference in illumination should be ignored.

6.3.6 BRANCH

Finally, the following routine is a check on the BRANCH feature of the system.

```
HEADER , 0123, 1 , 1 , 0
SCALE , 1 , 1 , 1 , 0
INTENSITY , 1 , 15 , 1
POINT , 1 , 4.5, 5. , 0
VECTOR , 0 , 1. , 0. , 1
POINT , 0 , 1. , 0. , 0
BRANCH , 2 , 0 , 1
HEADER , 1234, 2 , 1 , 0
VECTOR , 0 , 1. , 0. , 1
END
```

The same two horizontal lines as in the INTENSITY check should appear on the screen, but equal in illumination this time. This indicates that the BRANCH feature is operating properly. Its interrupt capability is also verified by ensuring that the file name reaches the PDP-8 interface (see HEADER test).

6.4 Maintenance

Should more information on the system be required, the reader is referred to the "Maintenance Manual" prepared by the author. It contains the printed circuit layouts for locating components, timing diagrams and a complete list of system variables. The latter indicates the circuit board from which each variable originates, the circuit boards to which each is an input and the number of TTL loads (maximum 10) each is driving.

Finally it is hoped that after final testing, the system will operate satisfactorily and will be used as often and with as much enthusiasm as was planned.

APPENDIX

TABLE I

LIST OF DIGITAL INTEGRATED CIRCUITS USED

Type	Description	Page no.*
SN7400N	Quad 2-input positive NAND gate	2-5
SN7402N	Quad 2-input positive NOR gate	2-9
SN7410N	Triple 3-input positive NAND gate	2-13
SN7420N	Dual 4-input positive NAND gate	2-14
SN7430N	Single 8-input positive NAND gate	2-15
SN7451N	Expandable dual 2-wide 2-input AND-OR-INVERT gate	2-17
SN7473N	Dual J-K master-slave flip-flop	2-29
SN7474N	Dual D-type edge-triggered flip-flop	2-32
SN7475N	Quad bistable latch	6-1
SN7482N	2-bit binary full adder	7-11
SN7483N	4-bit binary full adder	7-19
SN7496N	5-bit shift register	9-33
SN74121N	Monostable Multivibrator	2-38

* Page numbers in Reference (8).

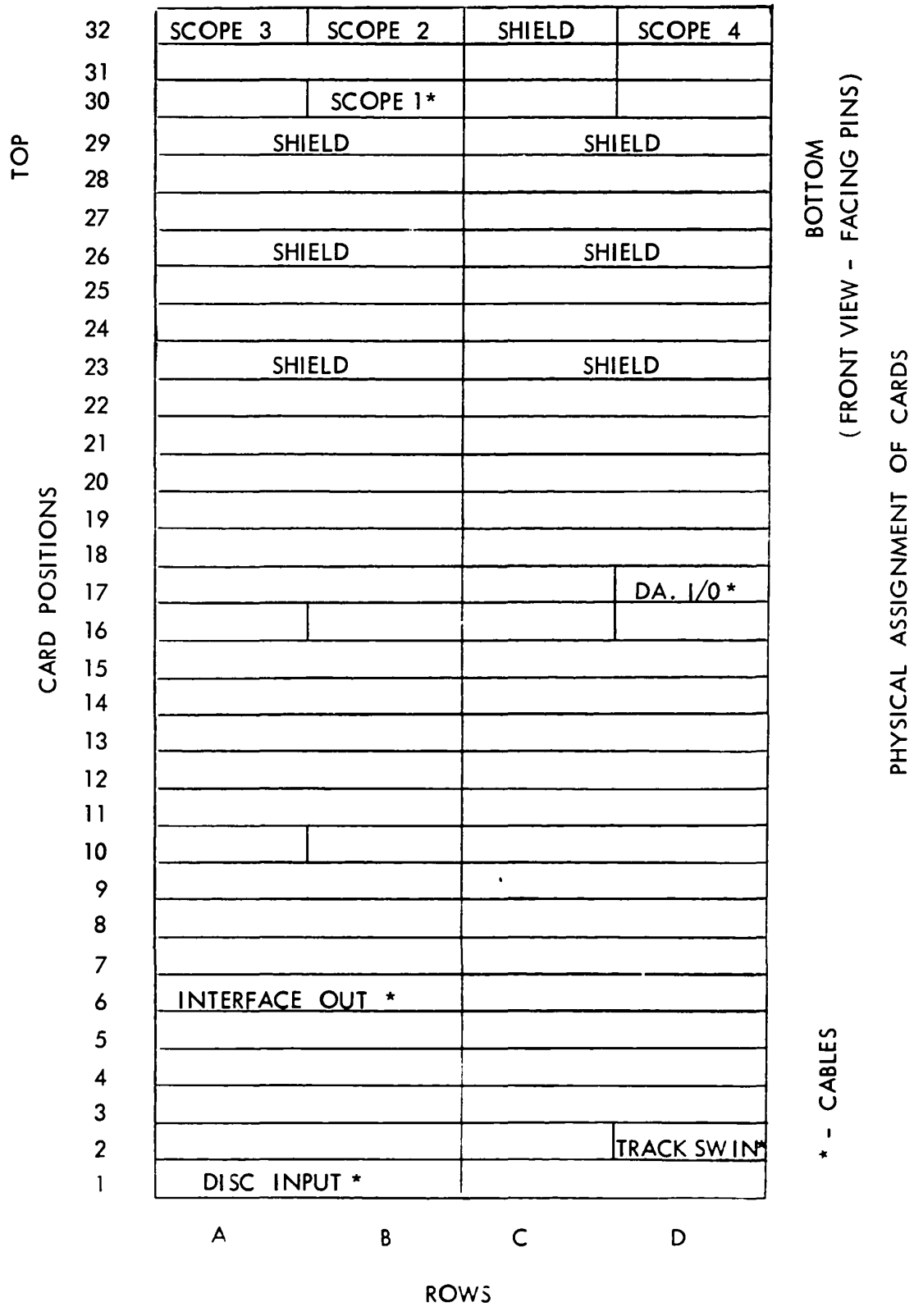

PHYSICAL ASSIGNMENT OF CARDS
(FRONT VIEW - FACING PINS)
TOP
BOTTOM
CARD POSITIONS
32
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
SCOPE 3
SCOPE 2
SHIELD
SCOPE 4
SCOPE 1*
SHIELD
SHIELD
SHIELD
SHIELD
SHIELD
SHIELD
DA. I/O *
INTERFACE OUT *
TRACK SWIN*
DISC INPUT *
A
B
C
D
ROWS
* - CABLES

TABLE II

LIST OF CIRCUIT BOARD FUNCTIONS

Board	Description	Page
AB1	Connector , disc input	*
CD1	Track Selection -1	83
AB2	Track Selection -2	84
C2	Multivibrators	85
D2	Connector , track switch input	*
AB3	Track Selection -3	84
CD3	Word buffer	86
AB4	Header	87
CD4	Scale system control	88
AB5	File name register	89
CD5	Scale system register -1	90
AB6	Connector , PDP-8 I/O	*
CD6	Scale system register -2	91
AB7	System clock	92
CD7	Scale system shift number	93
AB8	Branch	94
CD8	Scale shift -1	95
AB9	Main	96
CD9	Scale shift -2	97
A10	Point & vector mode control -2	98
B10	Mode	99
CD10	Scale shift -3	100
AB11	Point & vector mode control -1	101
CD11	Scale shift -4	102
AB12	Point & vector mode control -3	103
CD12	Scale shift -5	104
AB13	Intensity control	105
CD13	A - register	106
AB14	Z1 - axis register -1	107
CD14	Z3 - axis register -1	107
AB15	Z2 - axis register -1	107
CD15	Z4 - axis register -1	107

* For cable diagrams , refer to the Assembly Manual.

TABLE II (cont'd.)

Board	Description	Page
A16	Z1 - axis register -2	108
B16	Z2 - axis register -2	108
C16	Z3 - axis register -2	108
D16	Z4 - axis register -2	108
AB17	Z-axis decoder and switch control	109
C17	PDP-8 – interrupt	110
D17	Connector , D/A I/0	*
AB18	X - axis arithmetic -1	111
CD18	Y - axis arithmetic -1	111
AB19	X - axis arithmetic -2	111
CD19	Y - axis arithmetic -2	111
AB20	X - axis arithmetic -3	112
CD20	Y - axis arithmetic -3	112
AB21	X - axis arithmetic -4	113
CD21	Y - axis arithmetic -4	113
AB22	X - axis arithmetic -5	113
CD22	Y - axis arithmetic -5	113
AB25	X - axis ramp generator	114
CD25	Y - axis ramp generator	114
AB28	X - axis driver	115
CD28	Y - axis driver	115
B30	Connector , CRT1	*
AB31	Switches and Z-axis control	116
C31	Modulator (D/A)	117
A32	Connector , CRT 3	*
B32	Connector , CRT 2	*
D32	Connector , CRT 4	*

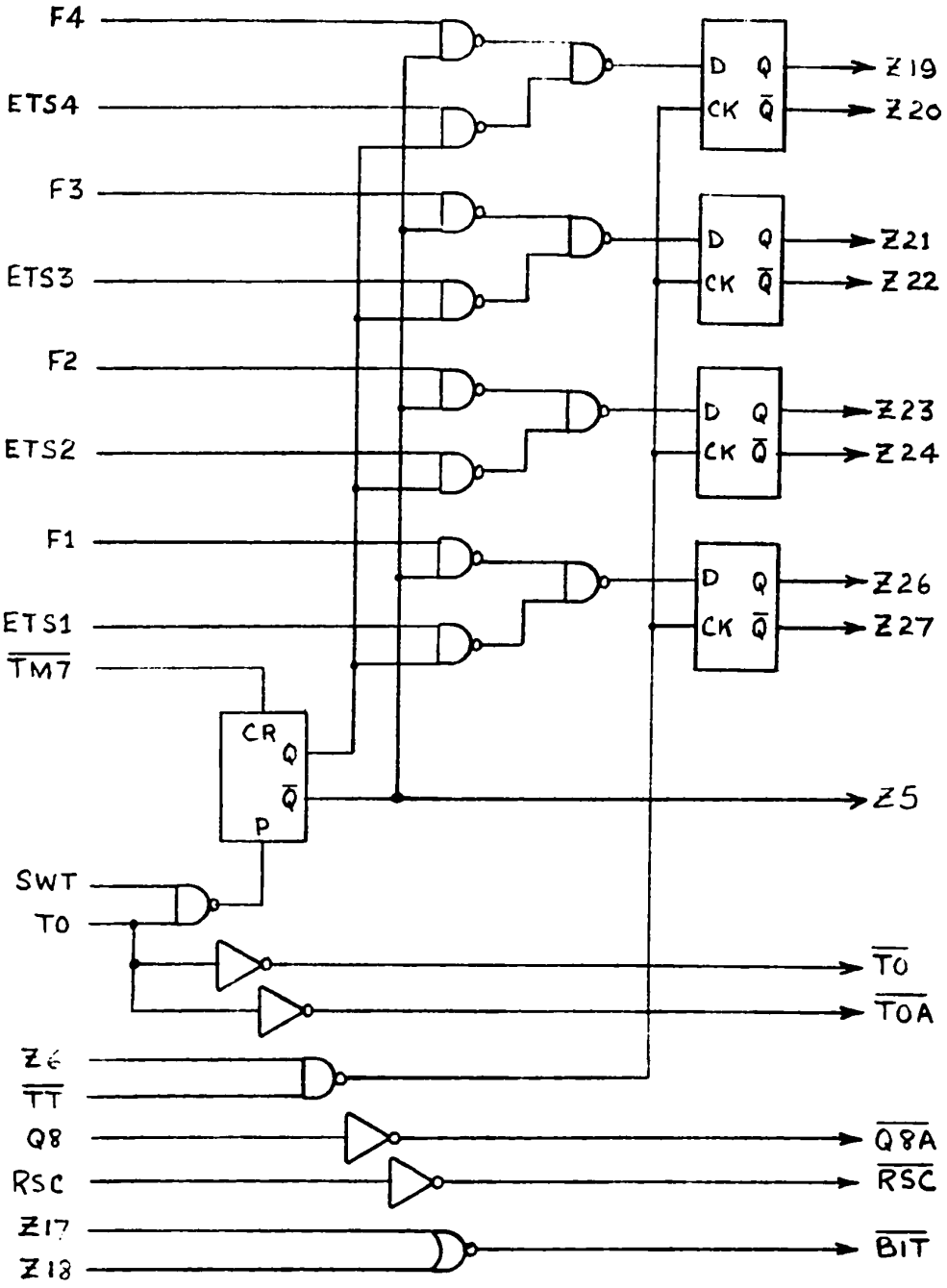
* For cable diagrams, refer to the Assembly Manual.

TABLE III

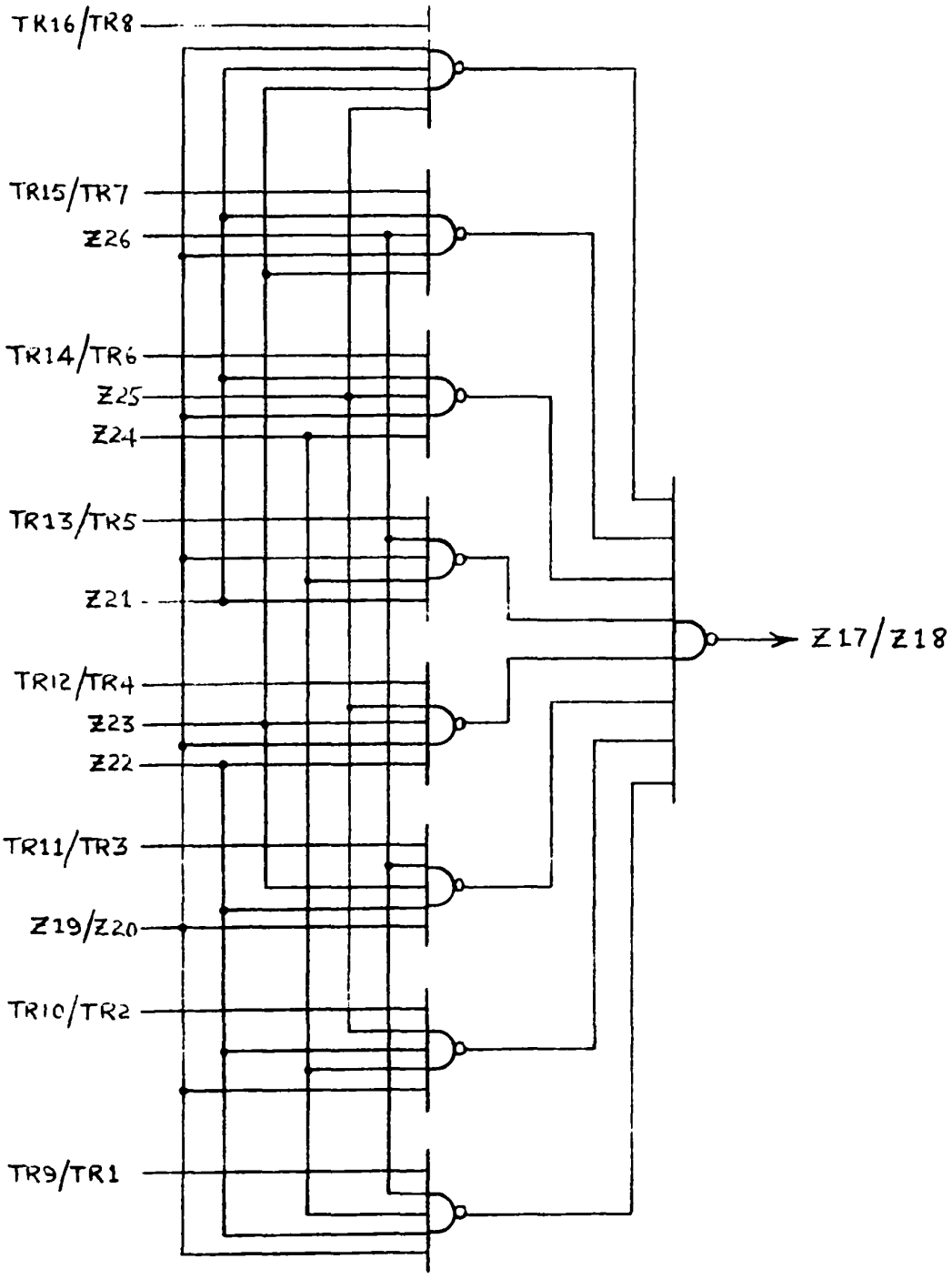
SYSTEM FUNCTION BOARD ASSIGNMENT

Function	Boards	Page
A - register	CD13	106
Branch	AB8	94
Connectors, CRT1, CRT2, CRT3, CRT4	B30, B32, A32, D32	*
Connector, D/A I/O	D17	*
Connector, disc input	AB1	*
Connector, PDP-8 I/O	AB6	*
Connector, track switch input	D2	*
File name register	AB5	89
Header	AB4	87
Intensity control	AB13	105
Main	AB9	96
Mode	B10	99
Modulator (D/A)	C31	117
Multivibrators	C2	85
PDP-8 interrupt	C17	110
Point & vector mode control -1, 2 & 3	AB11, A10, AB12	101, 98, 103
Scale shift -1, 2, 3, 4 & 5	CD8, CD9, CD10, CD11, CD12	95, 97, 100, 102, 104
Scale system control	CD4	88
Scale system register -1 & 2	CD5, CD6	90, 91
Scale system shift number	CD7	93
Switches and Z-axis control	AB31	116
System clock	AB7	92
Track selection -1, 2 & 3	CD1, AB2, AB3	83, 84
Word buffer	CD3	86
X-axis arithmetic -1, 2, 3, 4 & 5	AB18, AB19, AB20, AB21, AB22	111, 112, 113
X-axis driver	AB28	115
X-axis ramp generator	AB25	114
Y-axis arithmetic -1, 2, 3, 4, 5	CD18, CD19, CD20, CD21, CD22	111, 112, 113
Y-axis driver	CD28	115
Y-axis ramp generator	CD25	114
Z-axis decoder & switch control	AB17	109
Z1-axis register -1 & 2	AB14, A16	107, 108
Z2-axis register -1 & 2	AB15, B16	107, 108
Z3-axis register -1 & 2	CD14, C16	107, 108
Z4-axis register -1 & 2	CD15, D16	107, 108

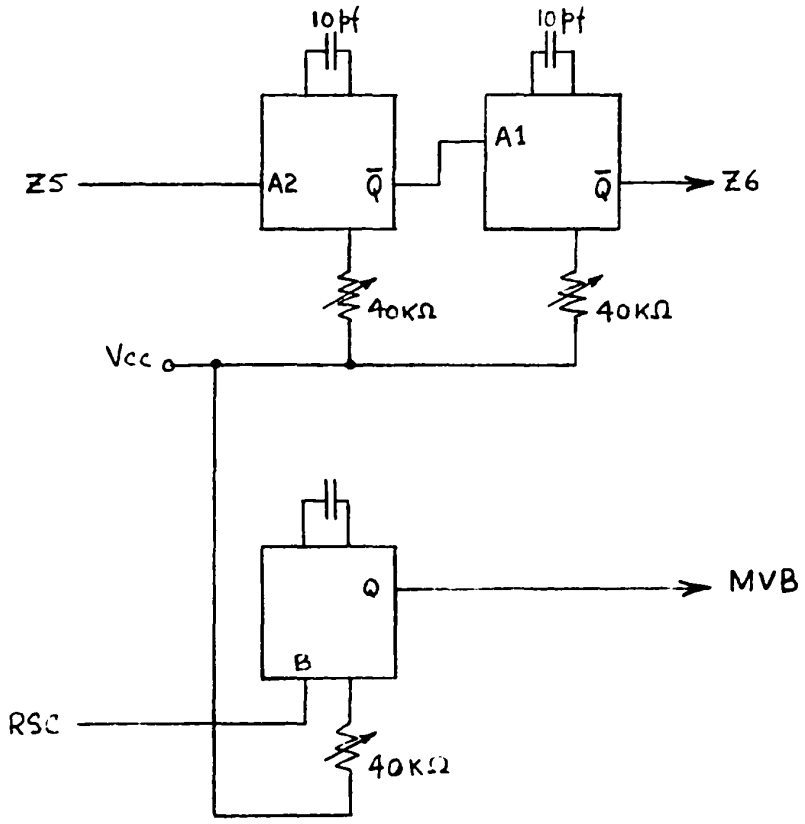
* For cable diagrams, refer to the Assembly Manual.


F4
ETS4
F3
ETS3
F2
ETS2
F1
ETS1
TM7
SWT
T0
Z6
TT
Q8
RSC
Z17
Z18
CR
Q
Q
P
D Q
CK Q
Z19
Z20
Z21
Z22
Z23
Z24
Z26
Z27
Z5
T0
T0A
Q8A
RSC
BIT

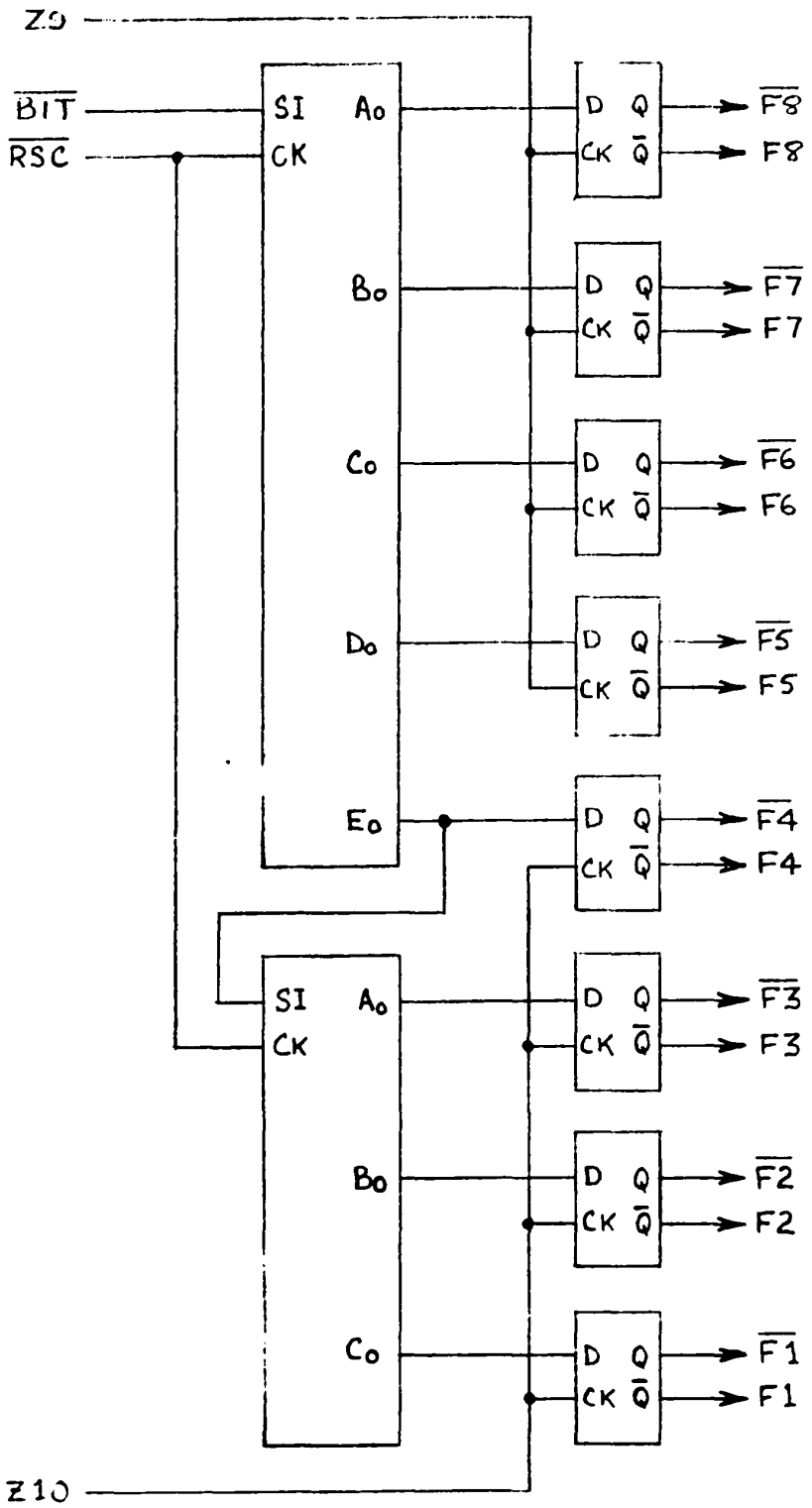
CARD CD1



CARDS AB2/AB3



CARD C2


Z9
BIT
RSC
SI
CK
A0
B0
C0
D0
E0
D Q
CK Q
F8
F8
F7
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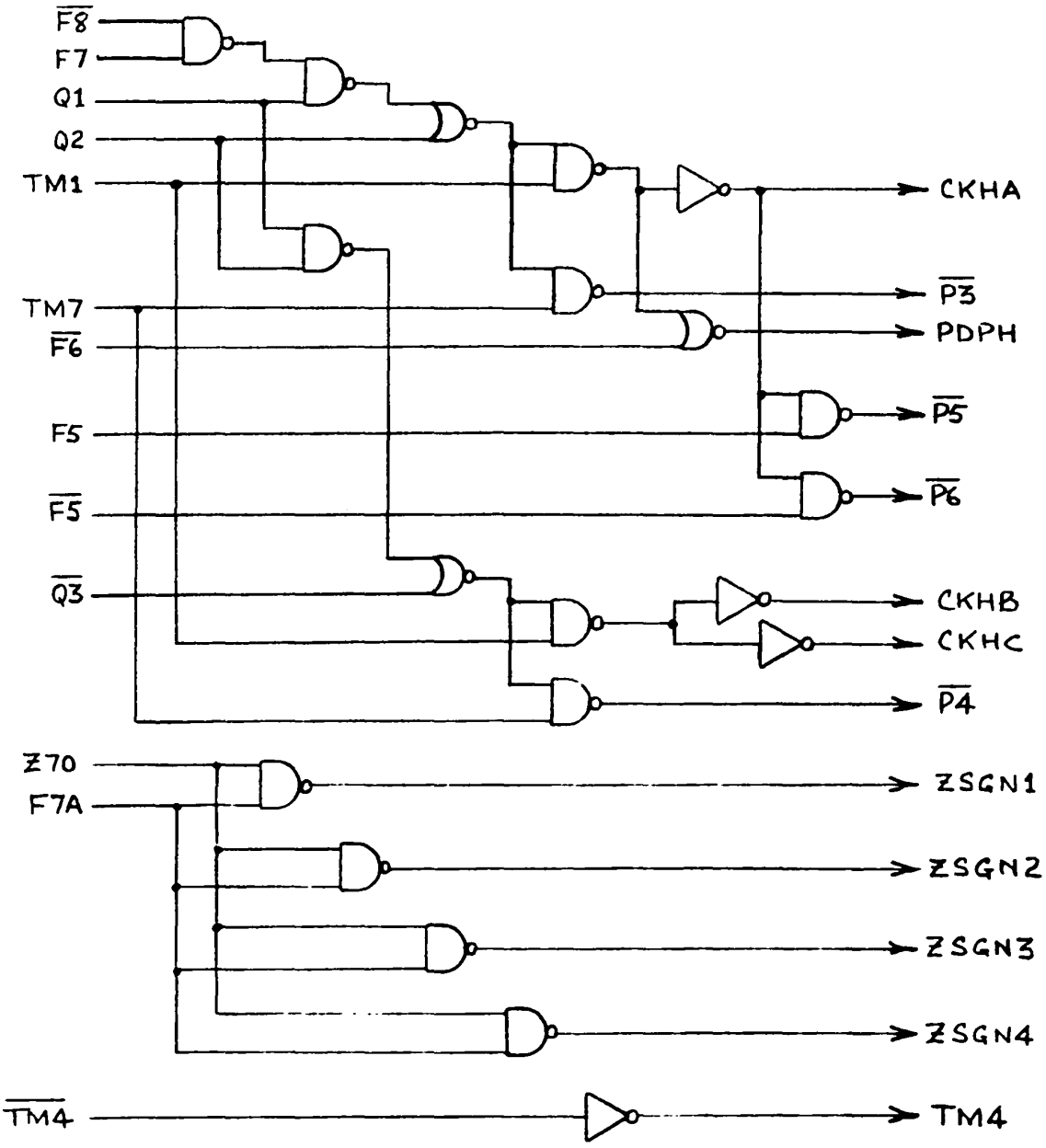
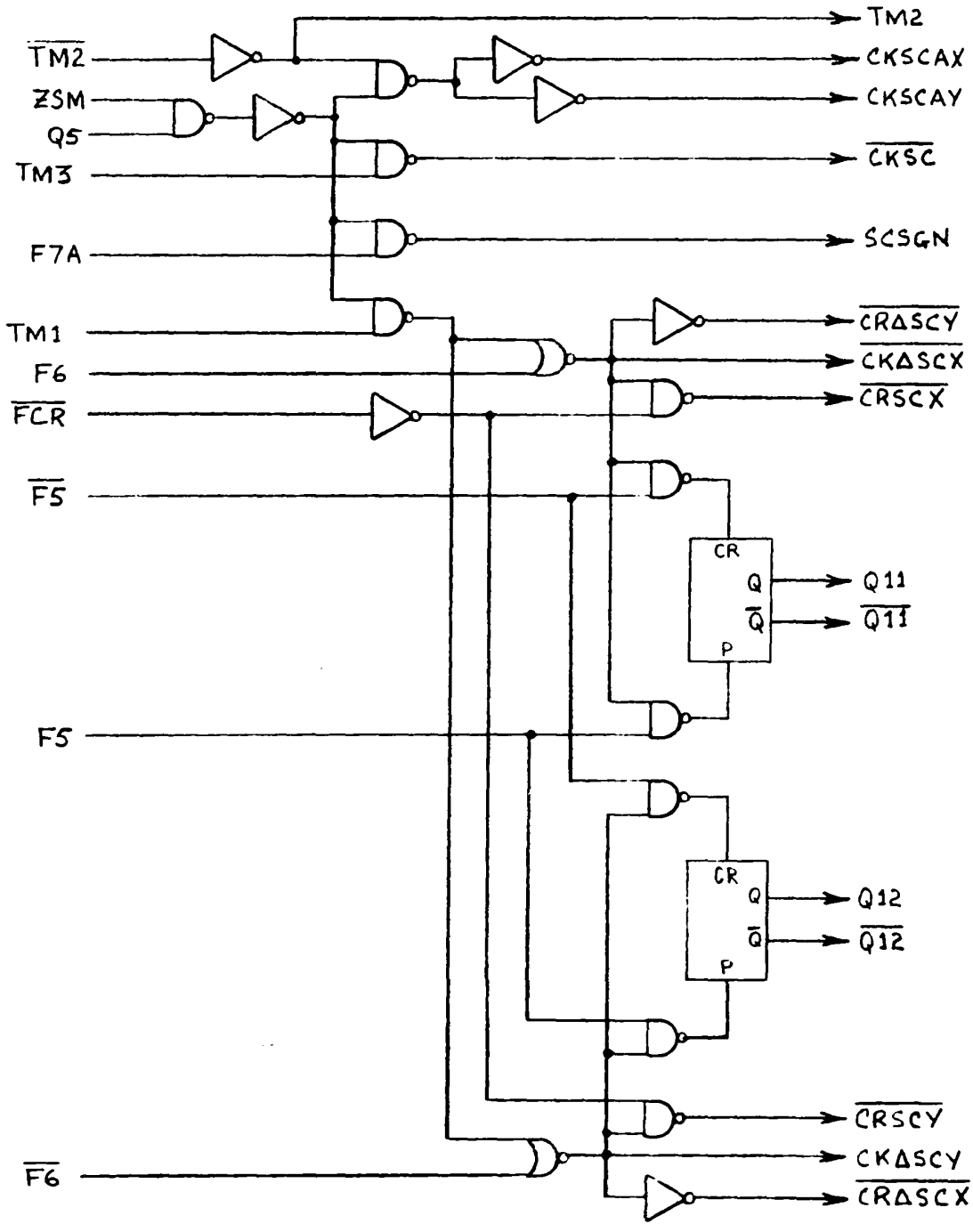
F6
F6
F5
F5
F4
F4
SI
CK
A0
B0
C0
F3
F3
F2
F2
F1
F1
Z10

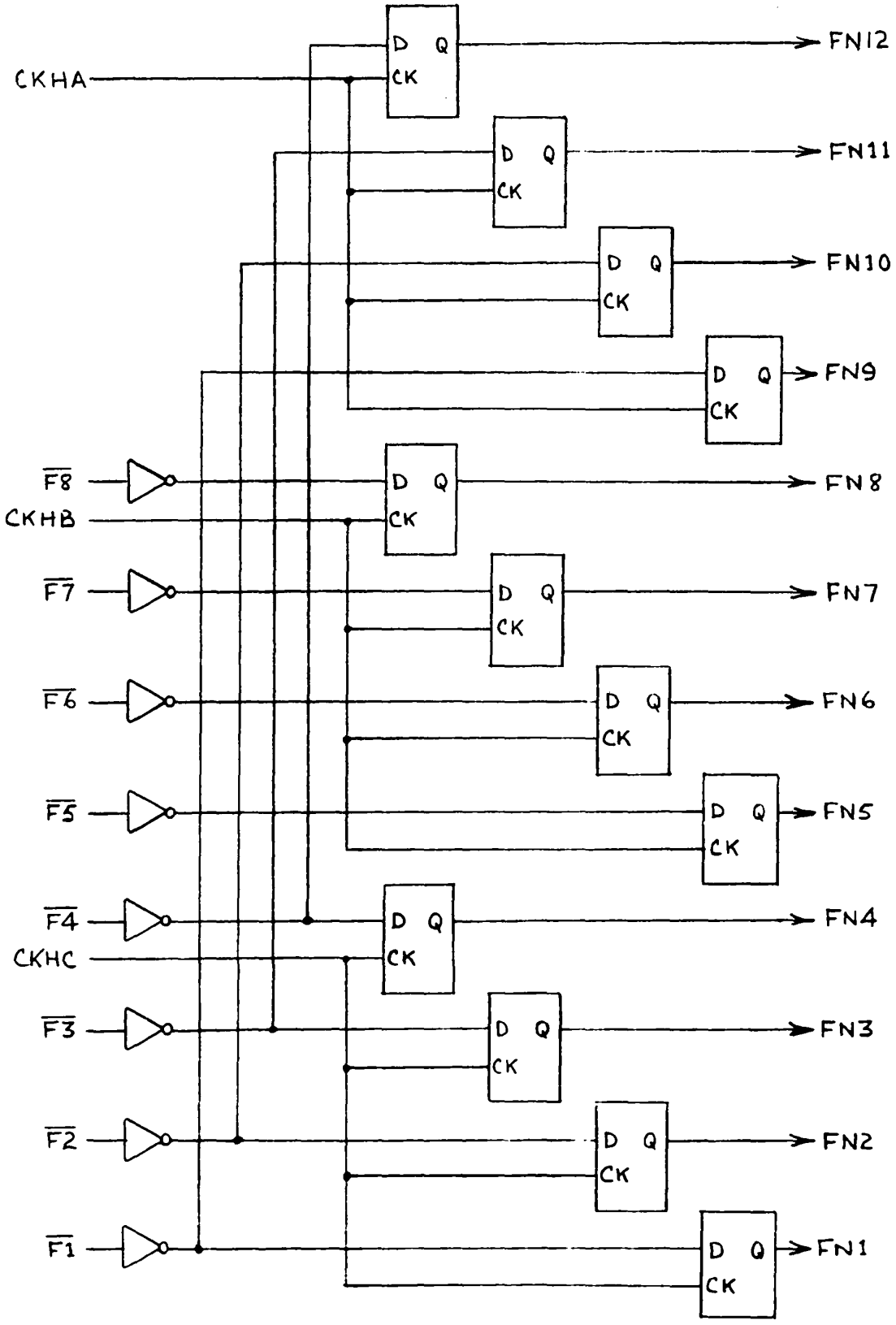
CARD CD3


F8
F7
Q1
Q2
TM1
TM7
F6
F5
F5
Q3
CKHA
P3
PDPH
P5
P6
CKHB
CKHC
P4
Z70
F7A
ZSGN1
ZSGN2
ZSGN3
ZSGN4
TM4
TM4

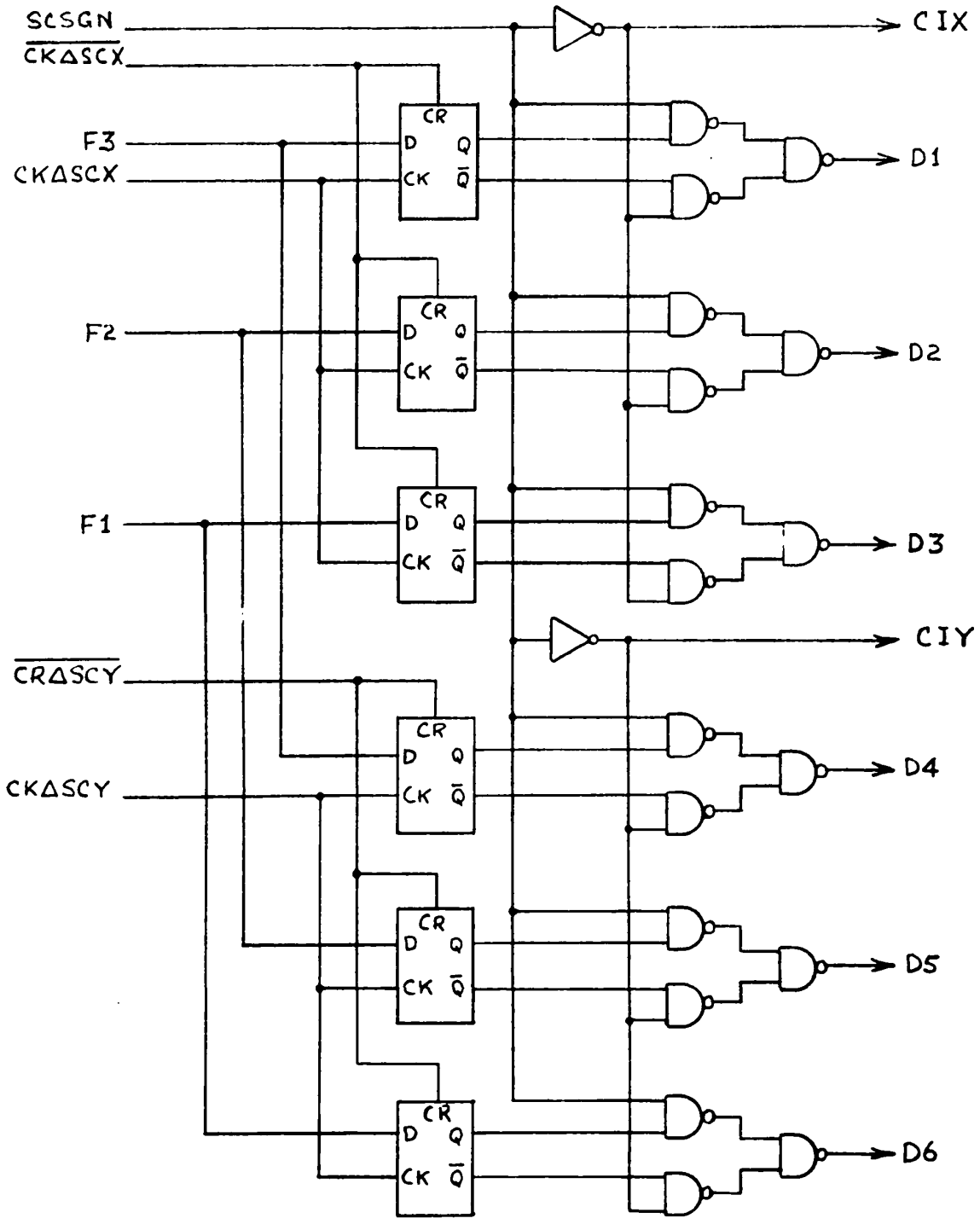
CARD AB4


TM2
CKSCAX
CKSCAY
CKSC
SCSGN
CRΔSCY
CKΔSCX
CRSCX
CR
Q
Q̄
P
Q11
Q11
CR
Q
Q̄
P
Q12
Q12
CRSCY
CKΔSCY
CRΔSCX
TM2
ZSM
Q5
TM3
F7A
TM1
F6
FCR
F5
F5
F6

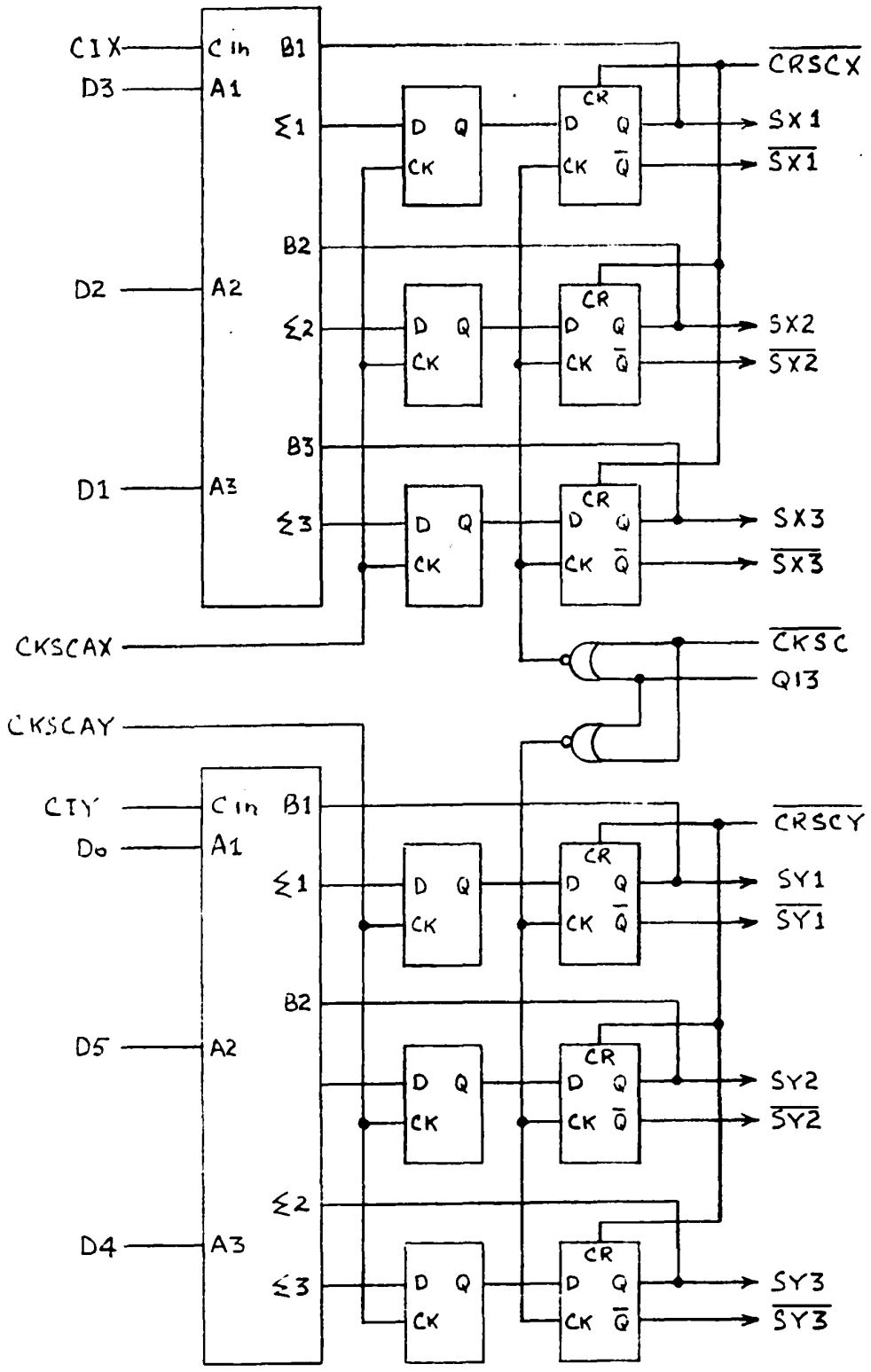
CARD CD4


CKHA
CKHB
CKHC
F8
F7
F6
F5
F4
F3
F2
F1
D Q
CK
FN12
FN11
FN10
FN9
FN8
FN7
FN6
FN5
FN4
FN3
FN2
FN1

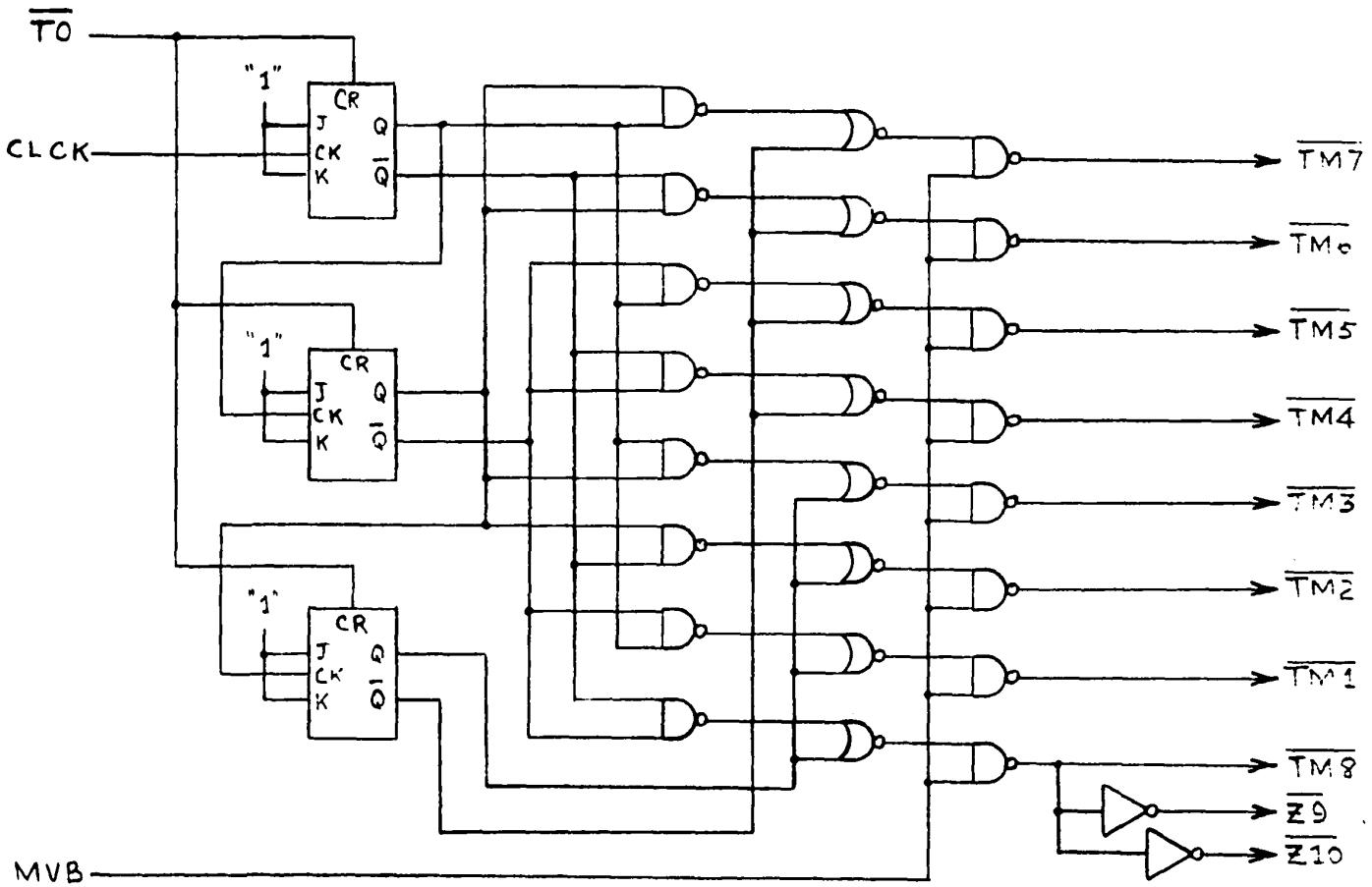
CARD AB5


SCSGN
CKΔSCX
F3
CKΔSCX
F2
F1
CRΔSCY
CKΔSCY
CR
D
CK
Q
Q̄
CIX
CIY
D1
D2
D3
D4
D5
D6

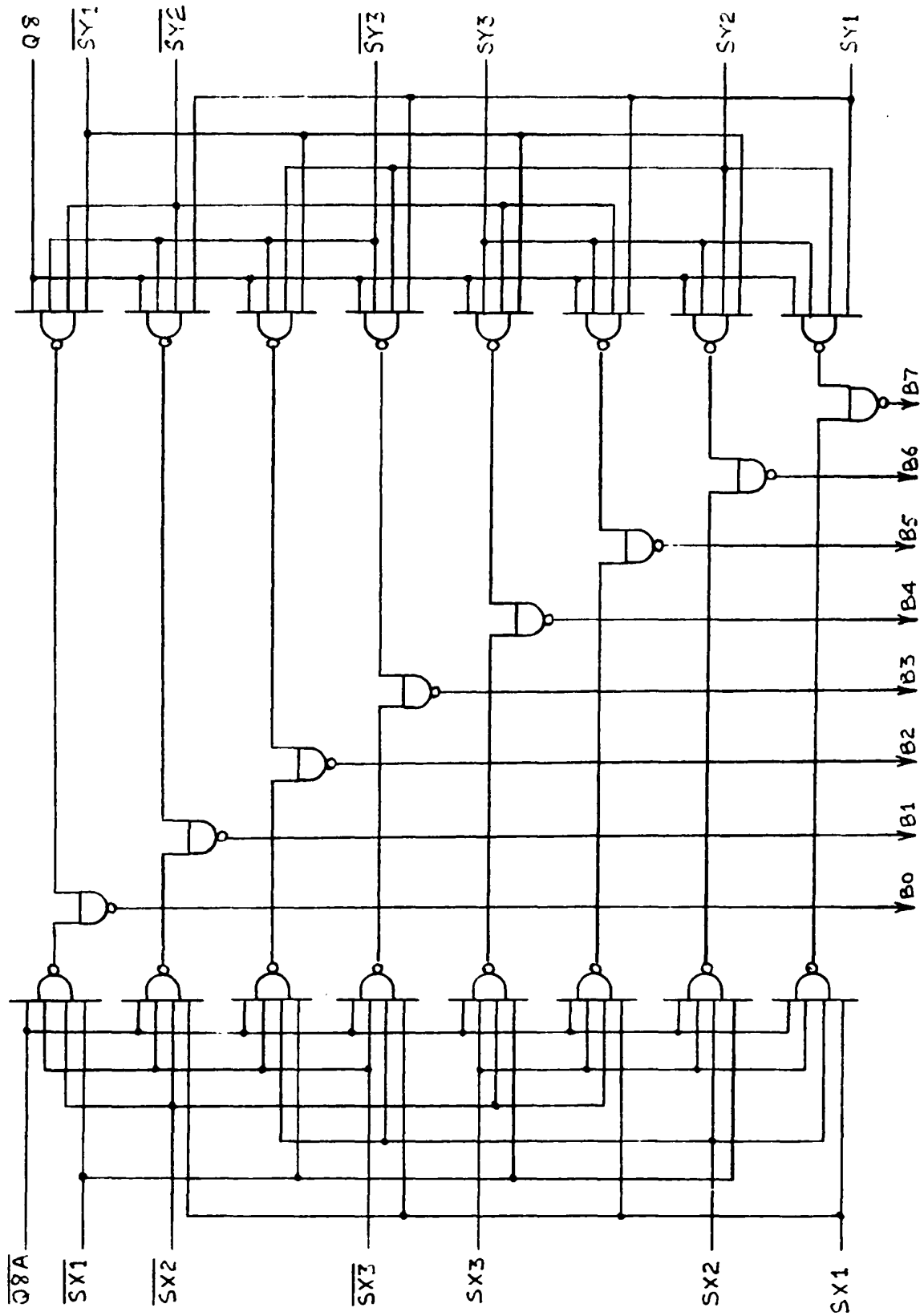
CARD CD5


CIX
Cin
B1
D3
A1
Σ1
D Q
CK
CR
D Q
CK Q̄
CRSCX
SX1
SX1
B2
D2
A2
Σ2
SX2
SX2
B3
D1
A3
Σ3
SX3
SX3
CKSCAX
CKSC
Q13
CKSCAY
CIY
Cin
B1
Do
A1
Σ1
CRSCY
SY1
SY1
B2
D5
A2
SY2
SY2
Σ2
D4
A3
Σ3
SY3
SY3

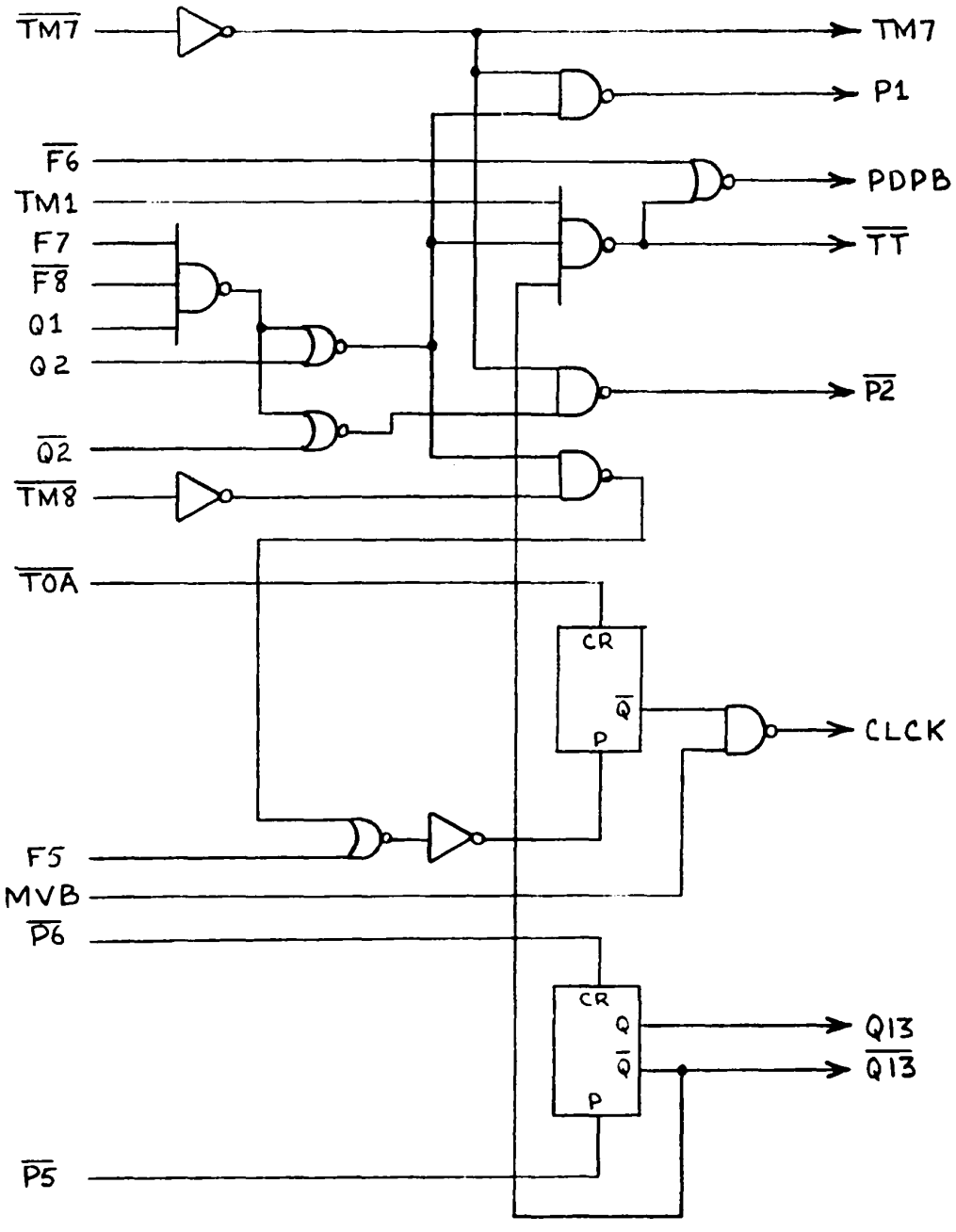
CARD CD6


$\overline{T0}$
CLCK
MVB
"1"
CR
J
CK
K
Q
$\overline{Q}$
$\overline{TM7}$
$\overline{TM6}$
$\overline{TM5}$
$\overline{TM4}$
$\overline{TM3}$
$\overline{TM2}$
$\overline{TM1}$
$\overline{TM8}$
$\overline{Z9}$
$\overline{Z10}$

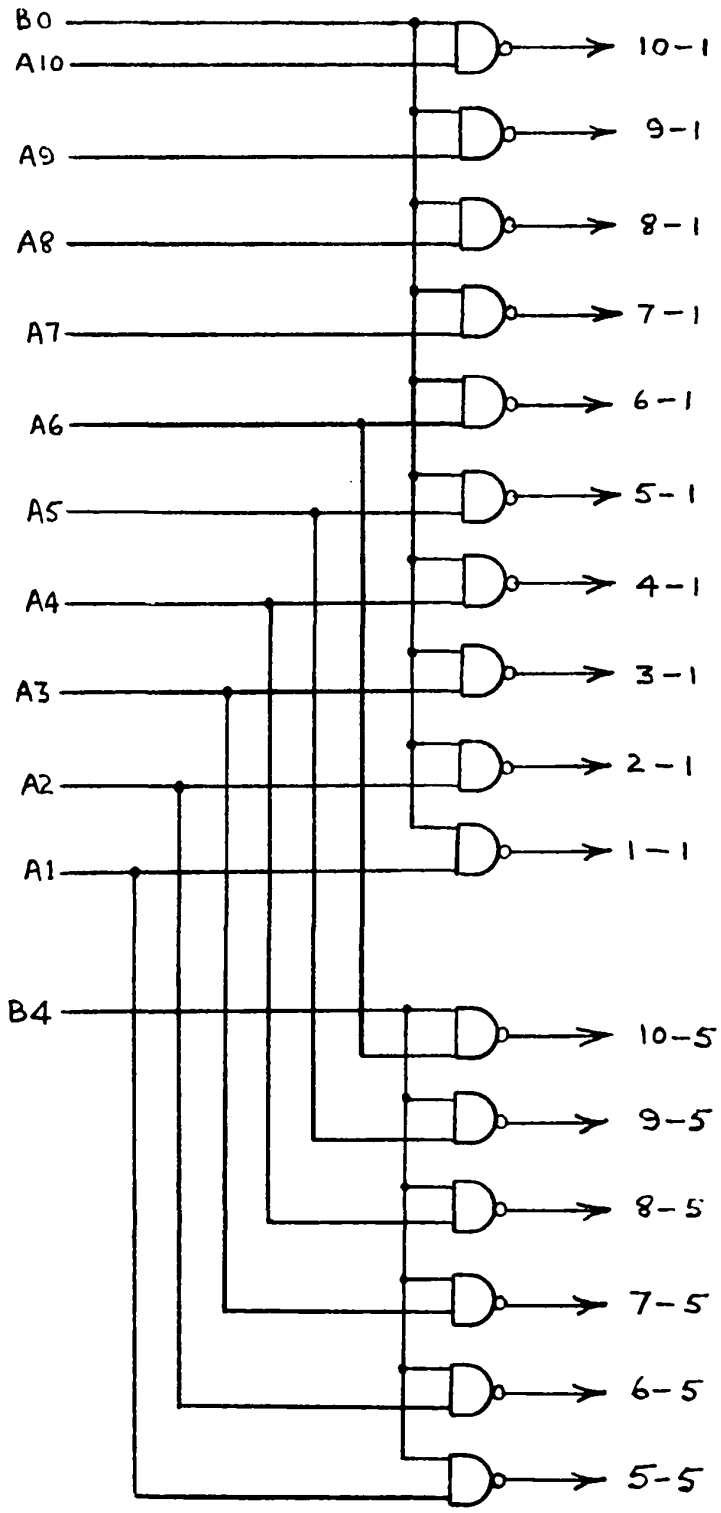
CARD AB7


Q8
SY1
SY2
SY3
SY3
SY2
SY1
B7
B6
B5
B4
B3
B2
B1
B0
Q8A
SX1
SX2
SX3
SX3
SX2
SX1

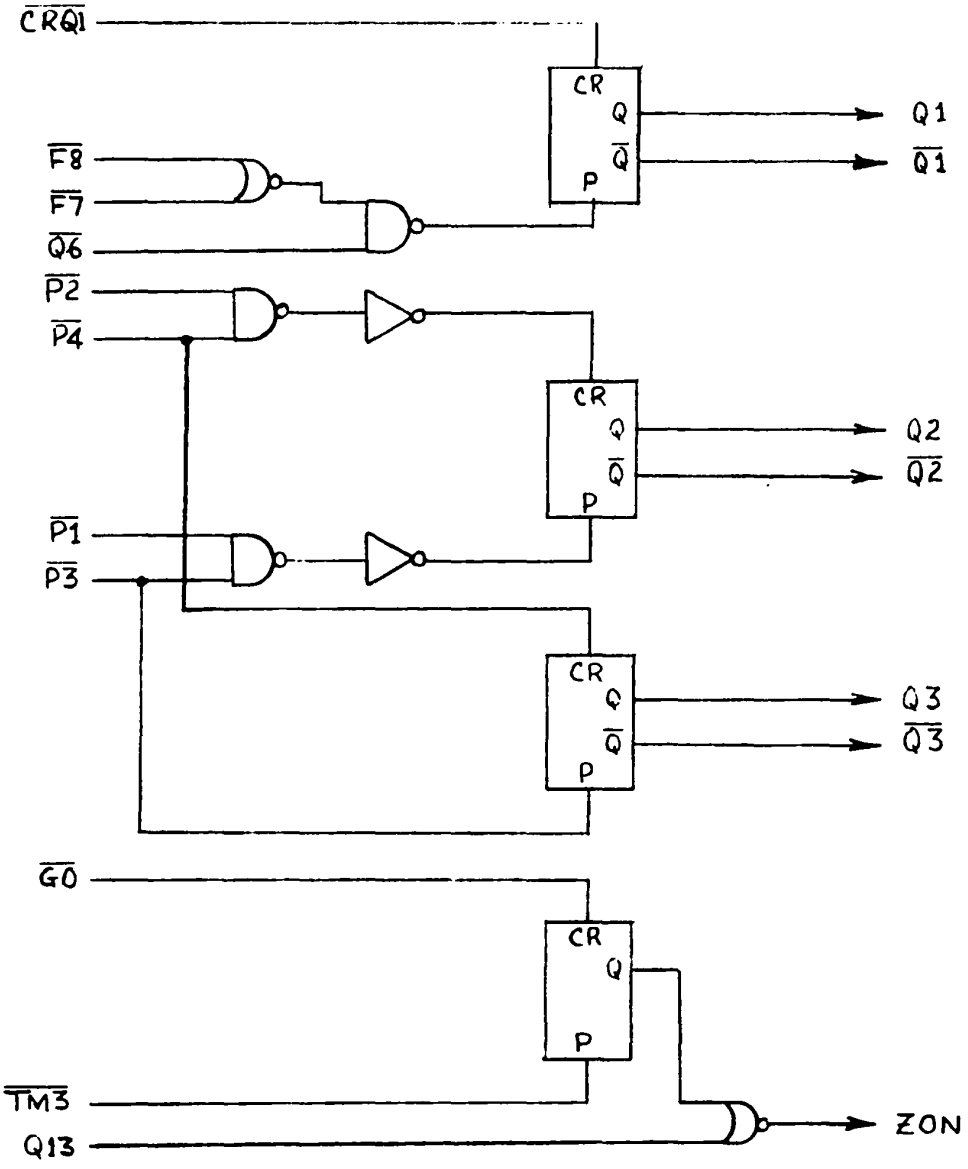
CARD CD7


TM7
TM7
P1
F6
PDPB
TM1
F7
TT
F8
Q1
Q2
P2
Q2
TM8
T0A
CR
Q
P
CLCK
F5
MVB
P6
CR
Q
Q
P
Q13
Q13
P5

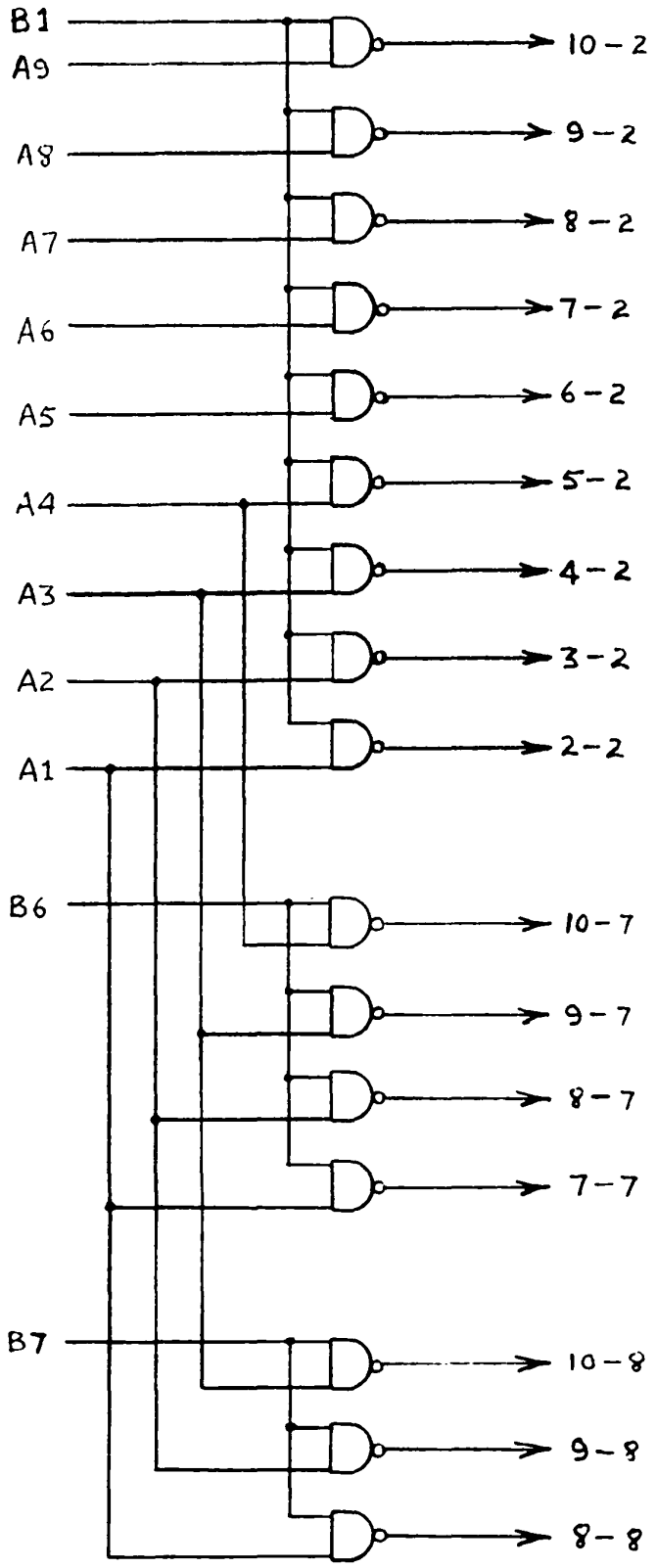
CARD AB8


B0
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
B4
10-1
9-1
8-1
7-1
6-1
5-1
4-1
3-1
2-1
1-1
10-5
9-5
8-5
7-5
6-5
5-5

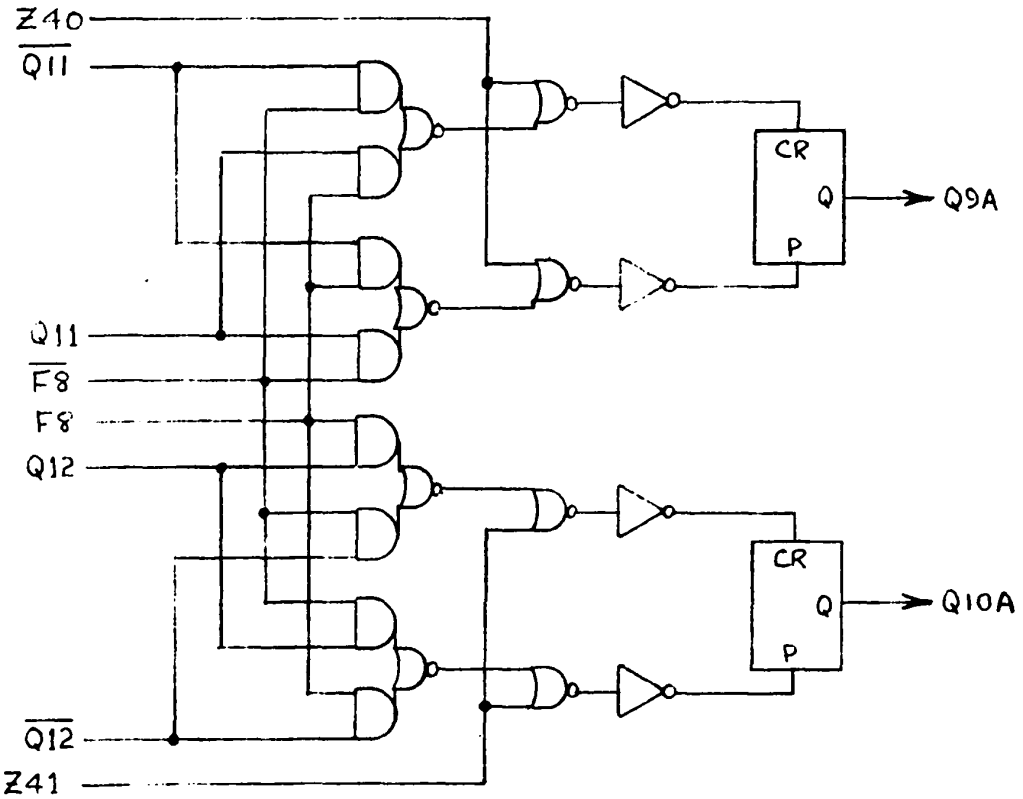
CARD CD8


CRQ1
CR
Q
Q̄
P
Q1
Q̄1
F8
F7
Q6
P2
P4
CR
Q
Q̄
P
Q2
Q̄2
P1
P3
CR
Q
Q̄
P
Q3
Q̄3
G0
CR
Q
P
TM3
Q13
ZON

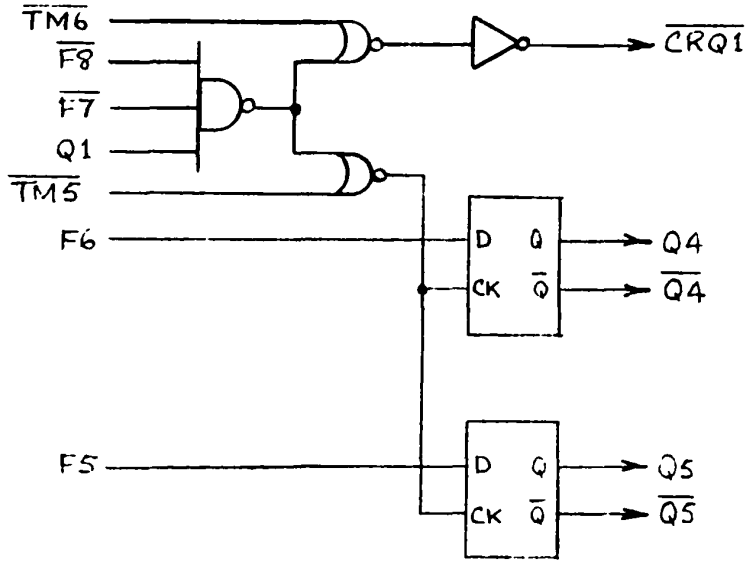
CARD AB9


B1
A9
A8
A7
A6
A5
A4
A3
A2
A1
B6
B7
10 - 2
9 - 2
8 - 2
7 - 2
6 - 2
5 - 2
4 - 2
3 - 2
2 - 2
10 - 7
9 - 7
8 - 7
7 - 7
10 - 8
9 - 8
8 - 8

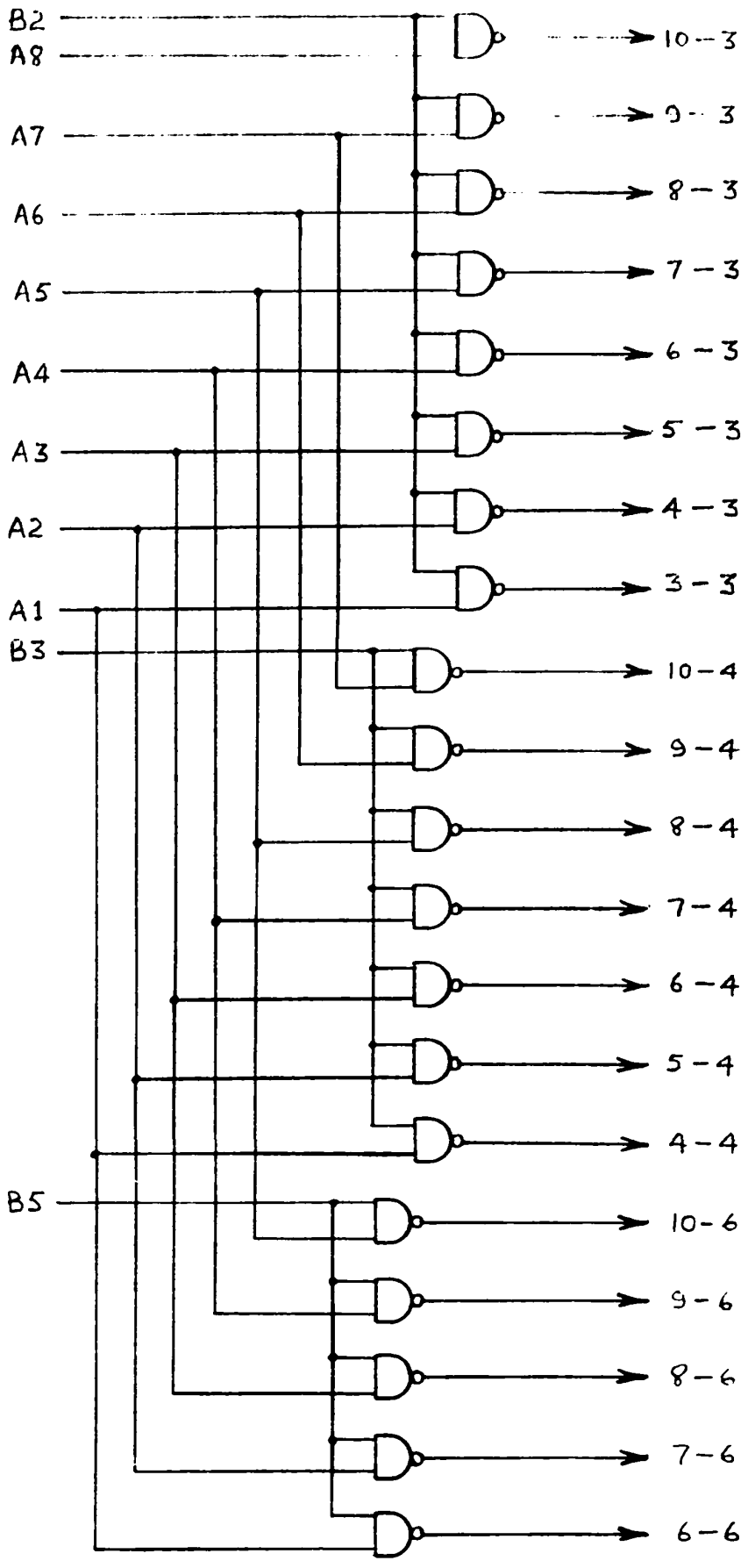
CARD CD9


Z40
$\overline{Q11}$
Q11
$\overline{F8}$
F8
Q12
$\overline{Q12}$
Z41
CR
Q
P
Q9A
CR
Q
P
Q10A

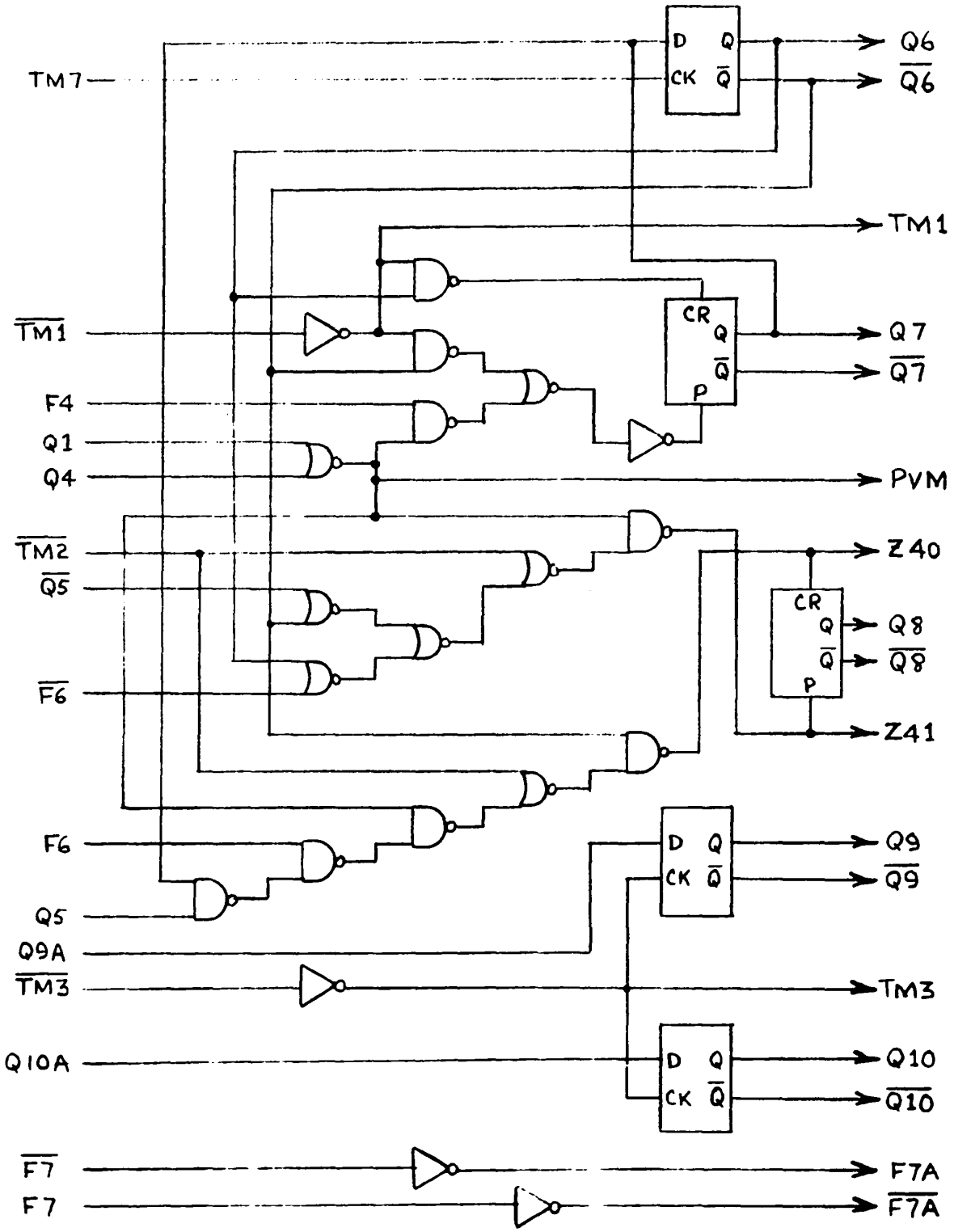
CARD A10



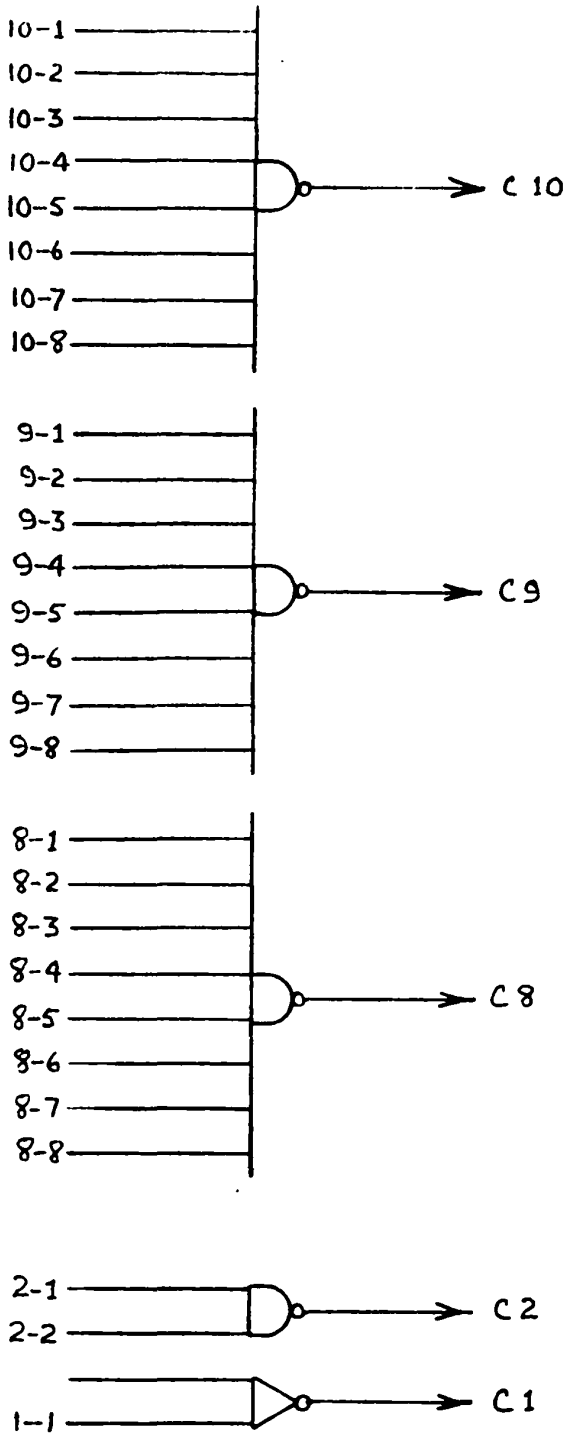
CARD B10


B2
A8
A7
A6
A5
A4
A3
A2
A1
B3
B5
10-3
9-3
8-3
7-3
6-3
5-3
4-3
3-3
10-4
9-4
8-4
7-4
6-4
5-4
4-4
10-6
9-6
8-6
7-6
6-6

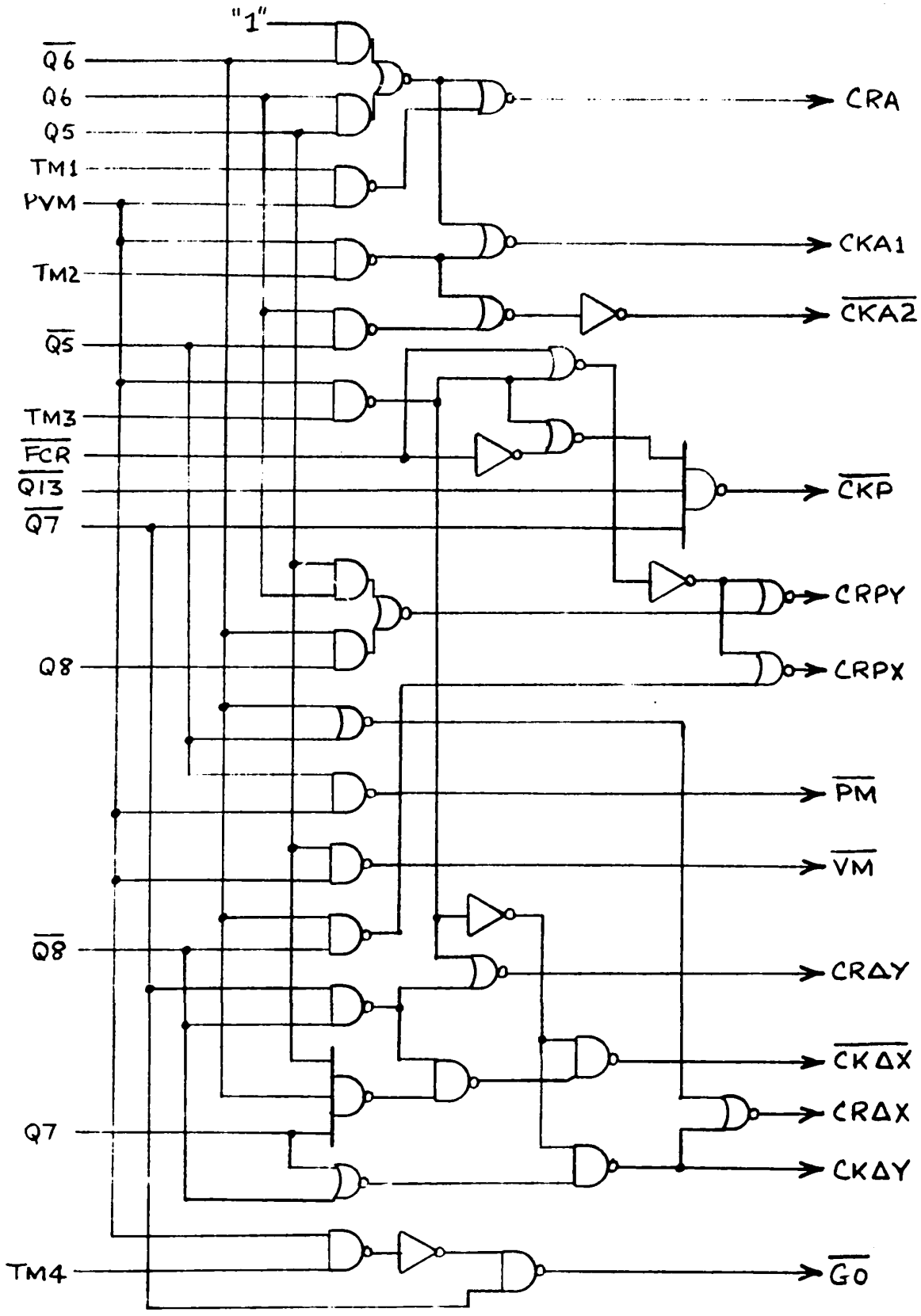
CARD CD10


TM7
D Q
CK Q̄
Q6
Q̄6
TM1
TM1̄
CR
Q
Q̄
P
Q7
Q̄7
F4
Q1
Q4
PVM
TM2̄
Q5̄
Z40
CR
Q
Q̄
P
Q8
Q̄8
F6̄
Z41
F6
D Q
CK Q̄
Q9
Q̄9
Q5
Q9A
TM3̄
TM3
Q10A
D Q
CK Q̄
Q10
Q̄10
F7̄
F7
F7A
F7̄A

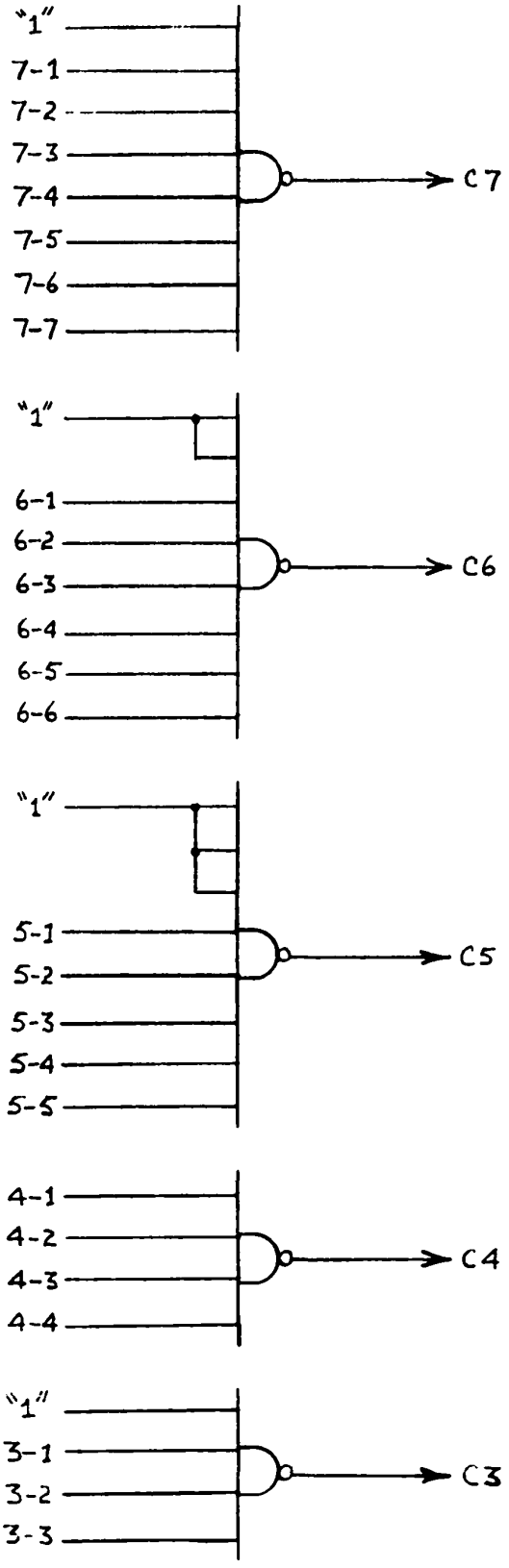
CARD AB11


10-1
10-2
10-3
10-4
10-5
10-6
10-7
10-8
C 10
9-1
9-2
9-3
9-4
9-5
9-6
9-7
9-8
C 9
8-1
8-2
8-3
8-4
8-5
8-6
8-7
8-8
C 8
2-1
2-2
C 2
1-1
C 1

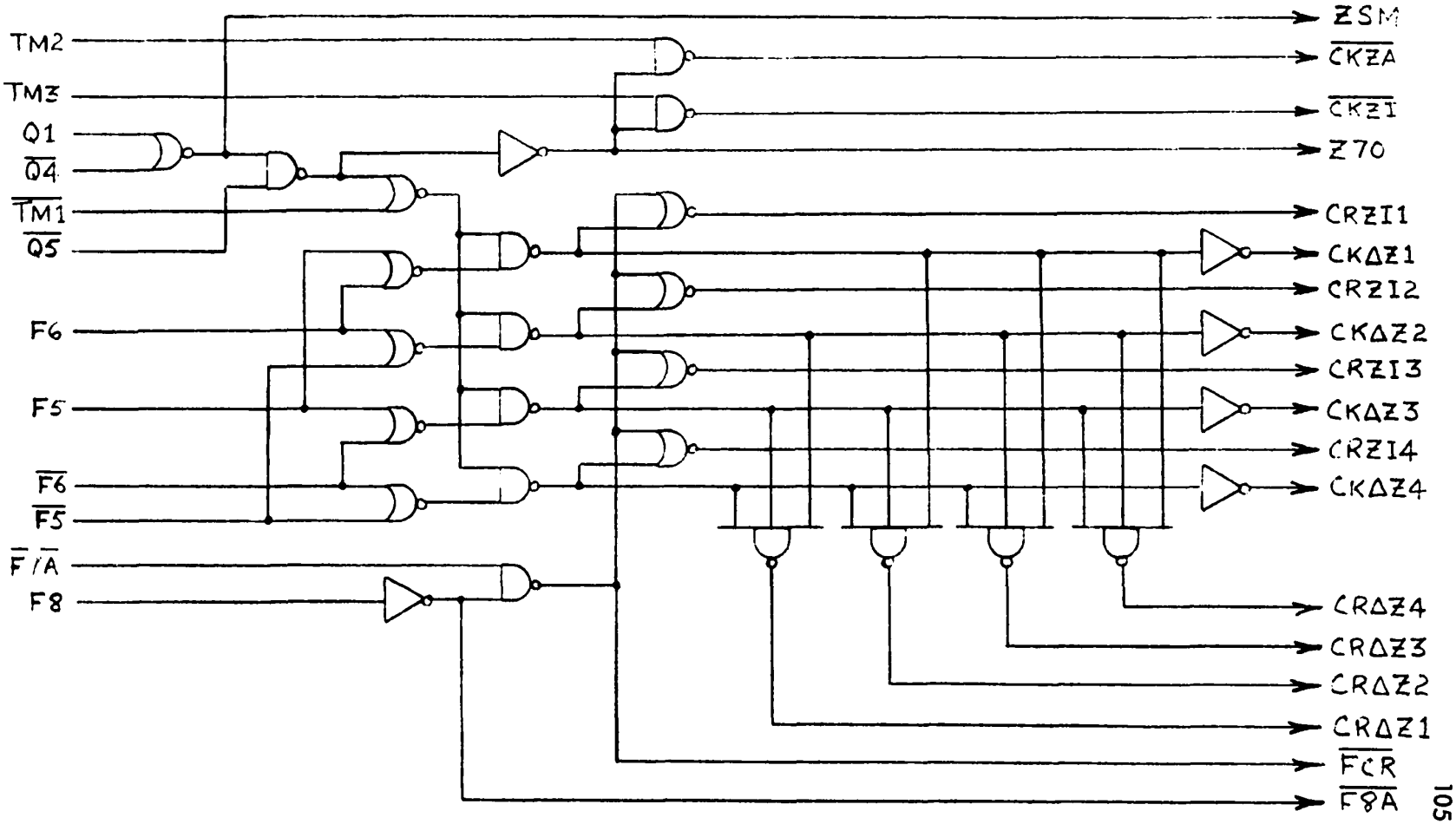
CARD CD11


"1"
$\overline{Q6}$
Q6
Q5
TM1
PVM
TM2
$\overline{Q5}$
TM3
$\overline{FCR}$
$\overline{Q13}$
$\overline{Q7}$
Q8
$\overline{Q8}$
Q7
TM4
CRA
CKA1
$\overline{CKA2}$
$\overline{CKP}$
CRPY
CRPX
$\overline{PM}$
$\overline{VM}$
CRΔY
$\overline{CKΔX}$
CRΔX
CKΔY
$\overline{Go}$

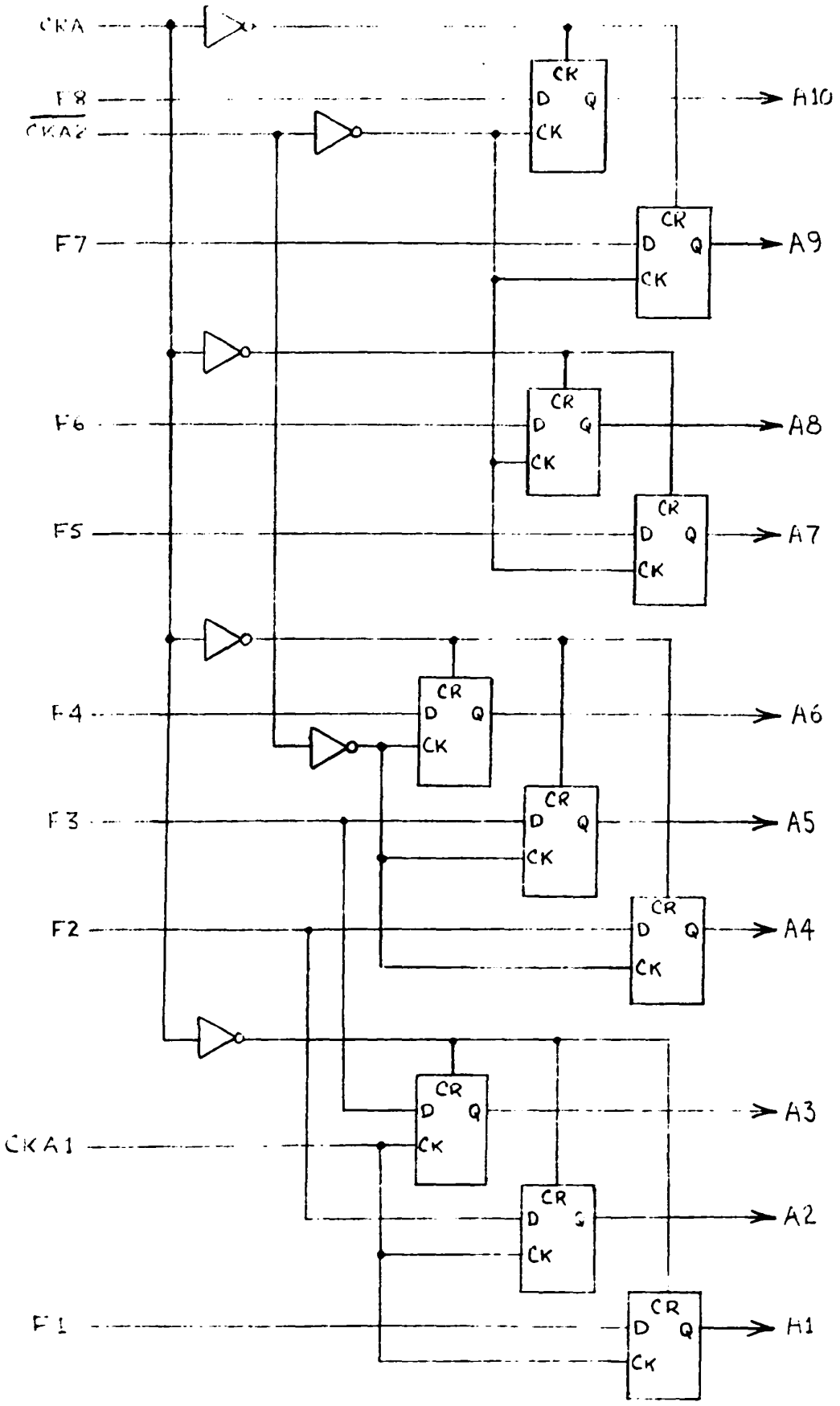
CARD AB12


"1"
7-1
7-2
7-3
7-4
7-5
7-6
7-7
C7
"1"
6-1
6-2
6-3
6-4
6-5
6-6
C6
"1"
5-1
5-2
5-3
5-4
5-5
C5
4-1
4-2
4-3
4-4
C4
"1"
3-1
3-2
3-3
C3

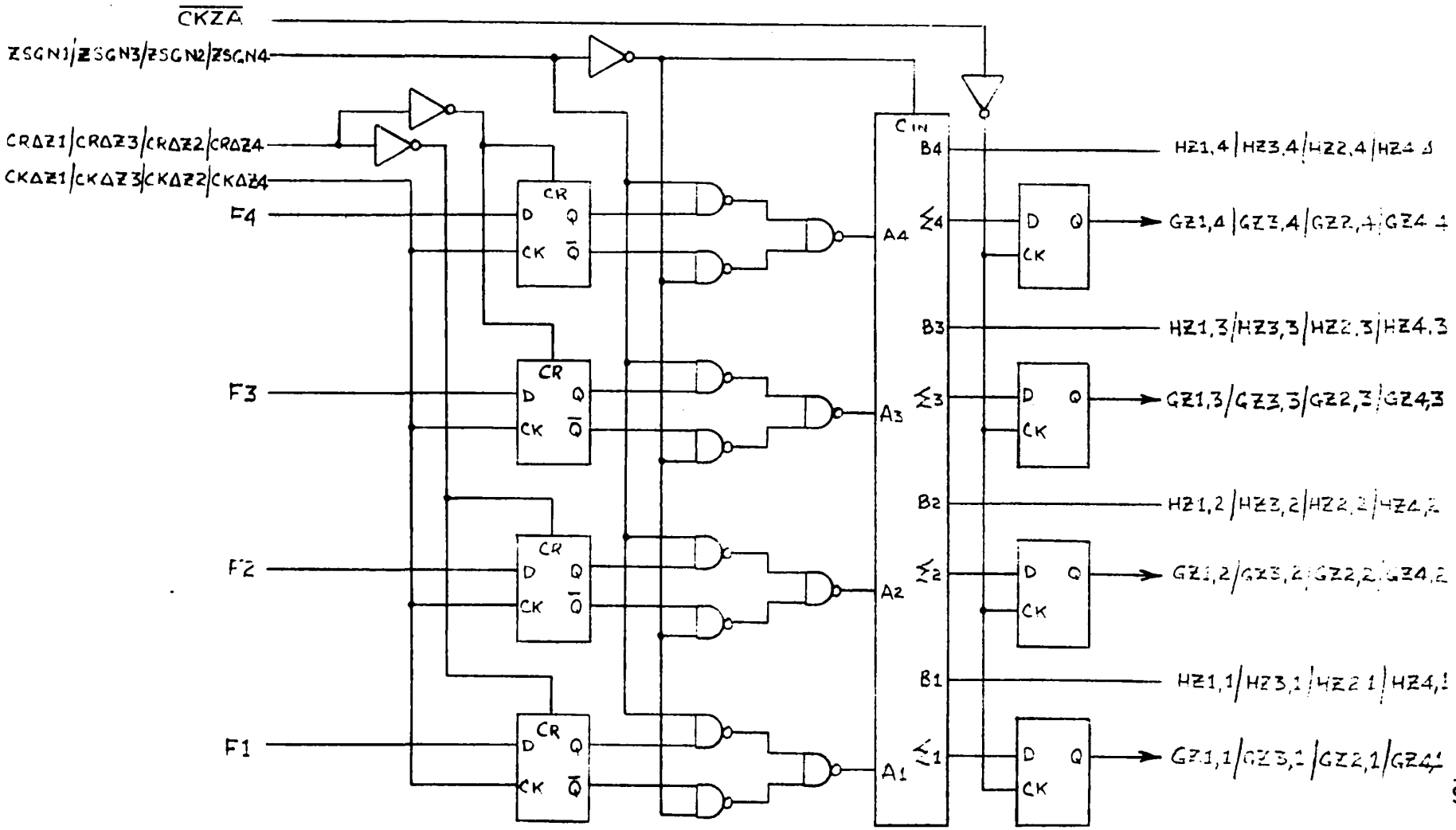
CARD CD12


TM2
TM3
Q1
$\overline{Q4}$
$\overline{TM1}$
$\overline{Q5}$
F6
F5
$\overline{F6}$
$\overline{F5}$
$\overline{F}/\overline{A}$
F8
ZSM
$\overline{CKZA}$
$\overline{CKZI}$
Z70
CRZI1
CKΔZ1
CRZI2
CKΔZ2
CRZI3
CKΔZ3
CRZI4
CKΔZ4
CRΔZ4
CRΔZ3
CRΔZ2
CRΔZ1
$\overline{FCR}$
$\overline{F8A}$

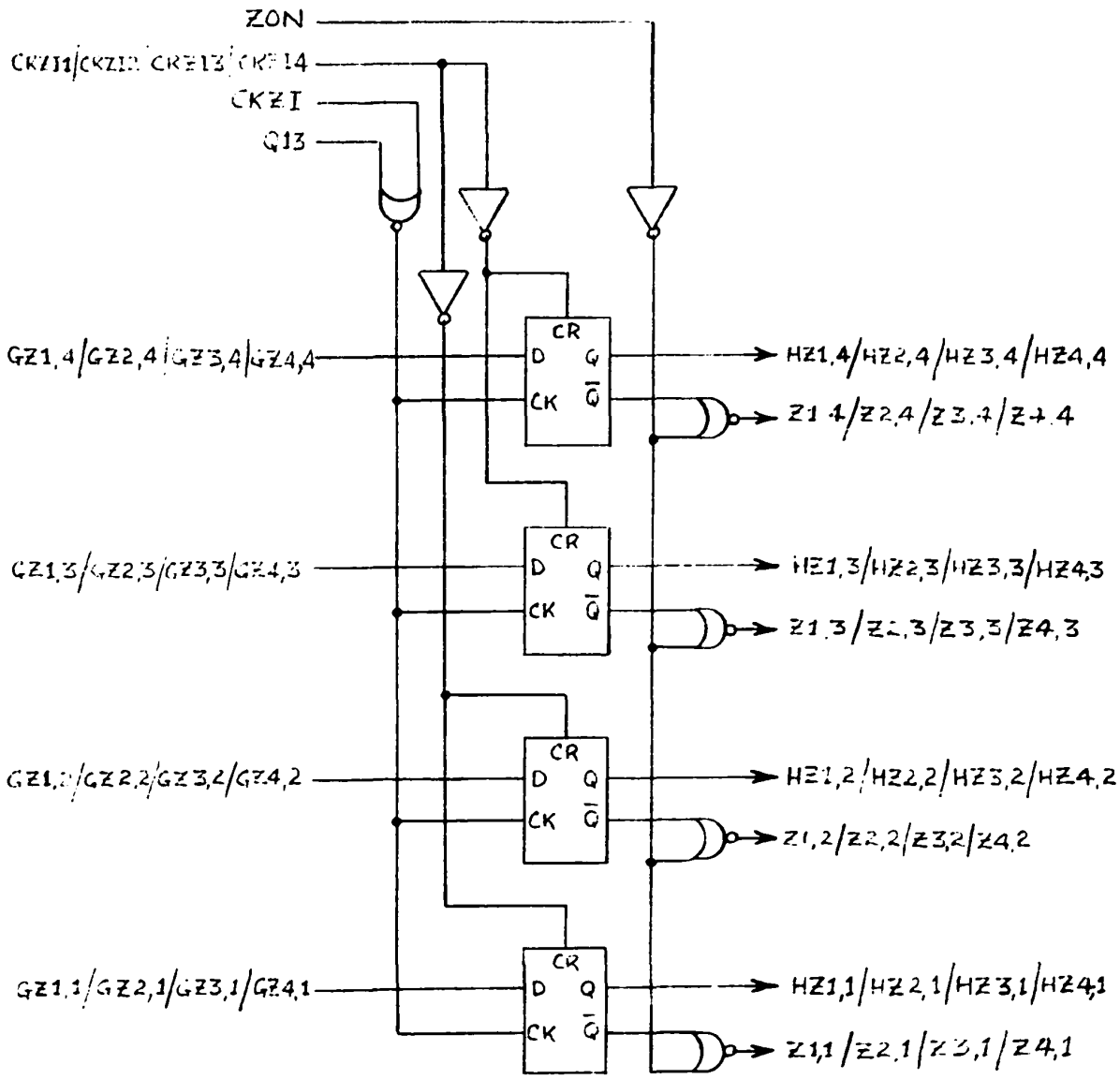
CARD AB13


CKA
F8
CKA2
F7
F6
F5
F4
F3
F2
CKA1
F1
CR
D
Q
CK
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1

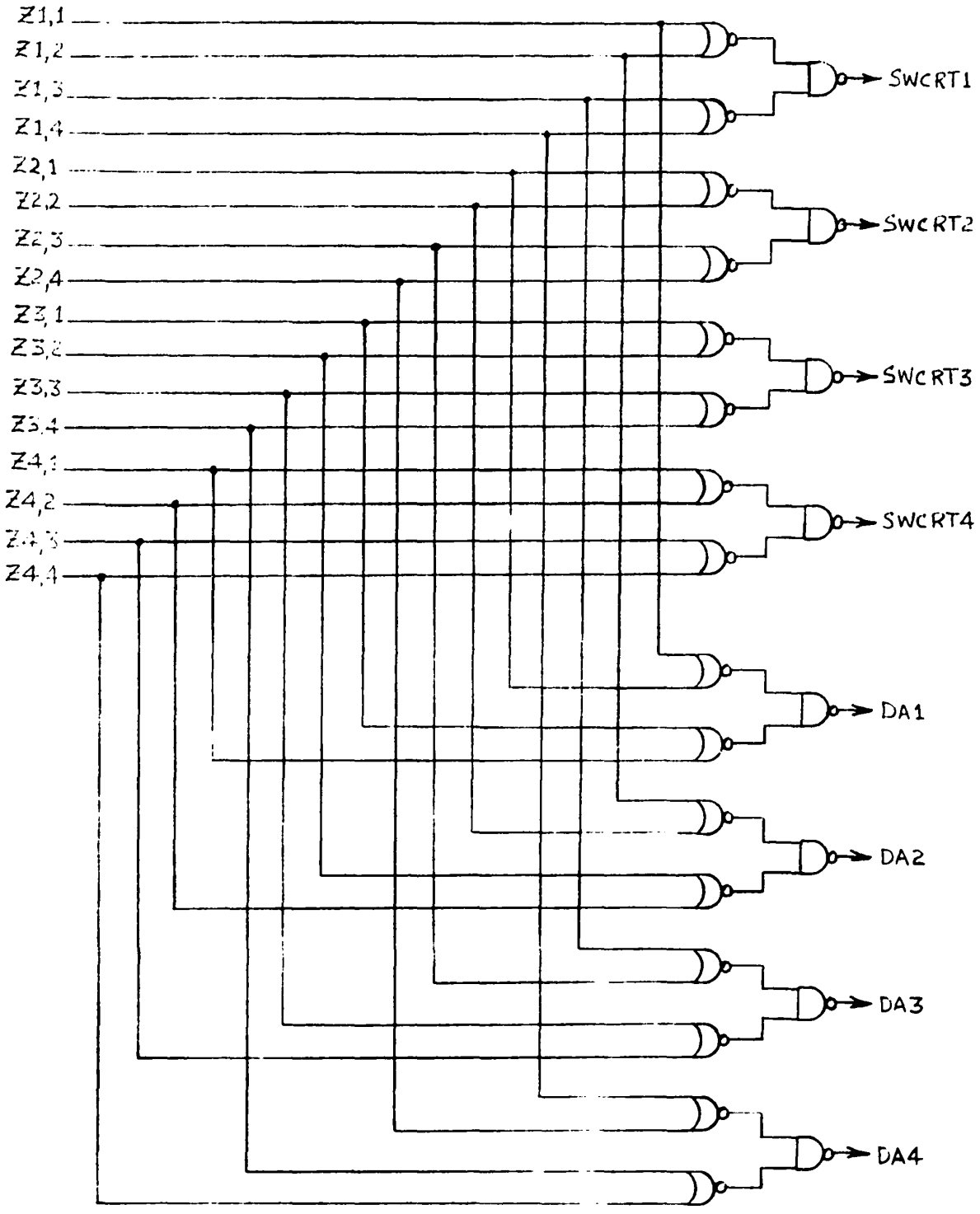
CARD CD13



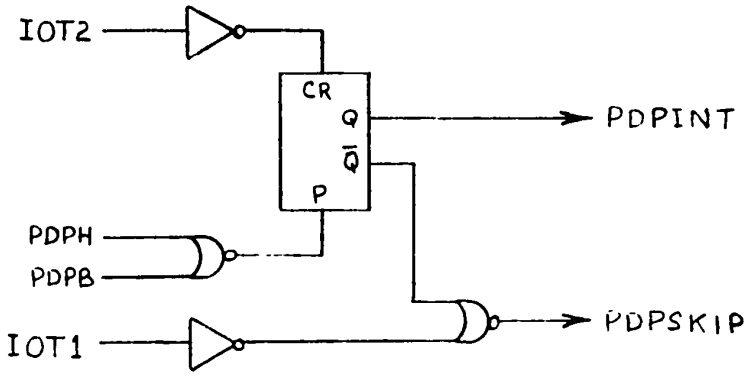
CARDS AB14/CD14/AB15/CD15



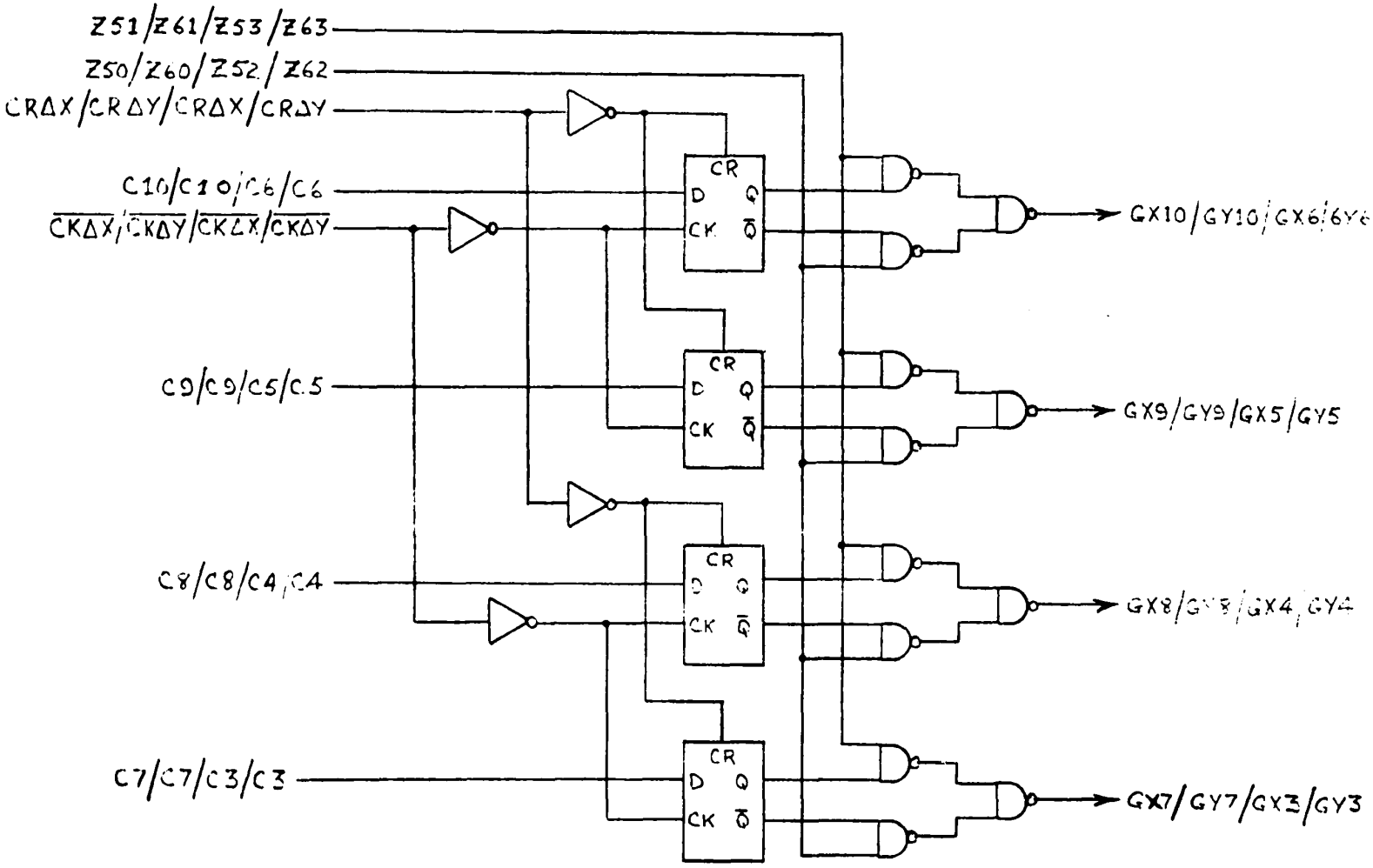
CARDS A16/B16/C16/D16


Z1,1
Z1,2
Z1,3
Z1,4
Z2,1
Z2,2
Z2,3
Z2,4
Z3,1
Z3,2
Z3,3
Z3,4
Z4,1
Z4,2
Z4,3
Z4,4
SWCRT1
SWCRT2
SWCRT3
SWCRT4
DA1
DA2
DA3
DA4

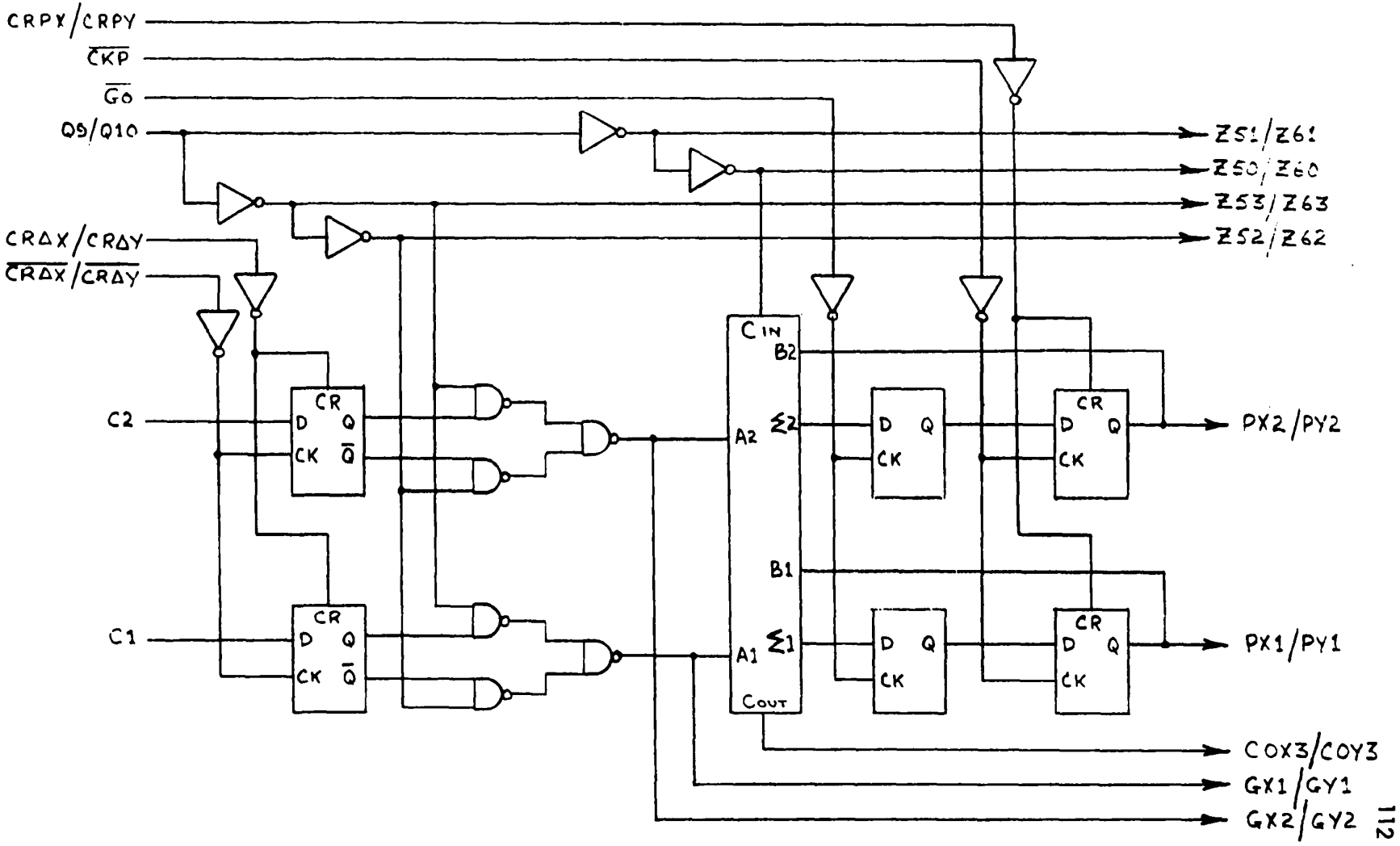
CARD AB17



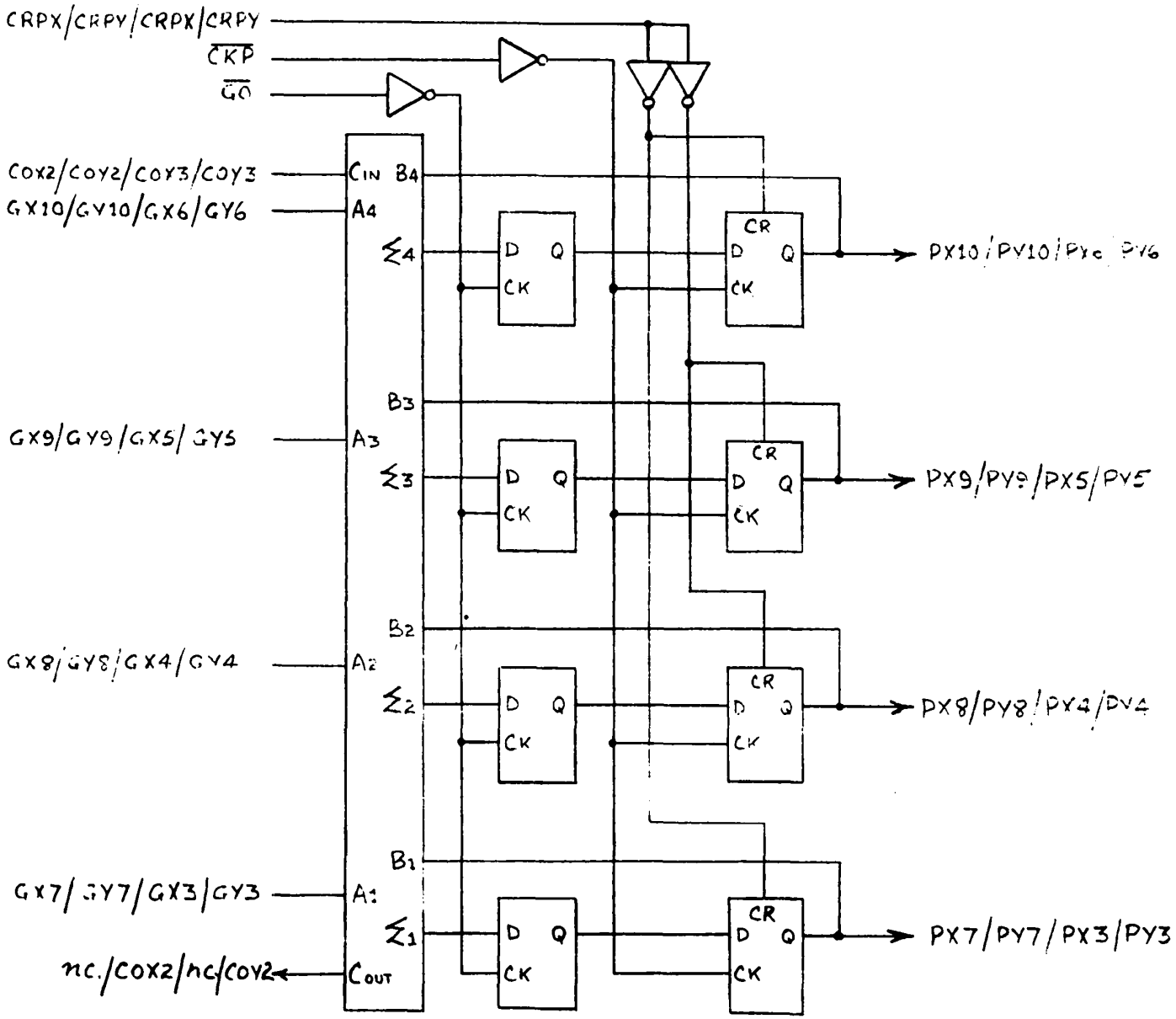
CARD C17



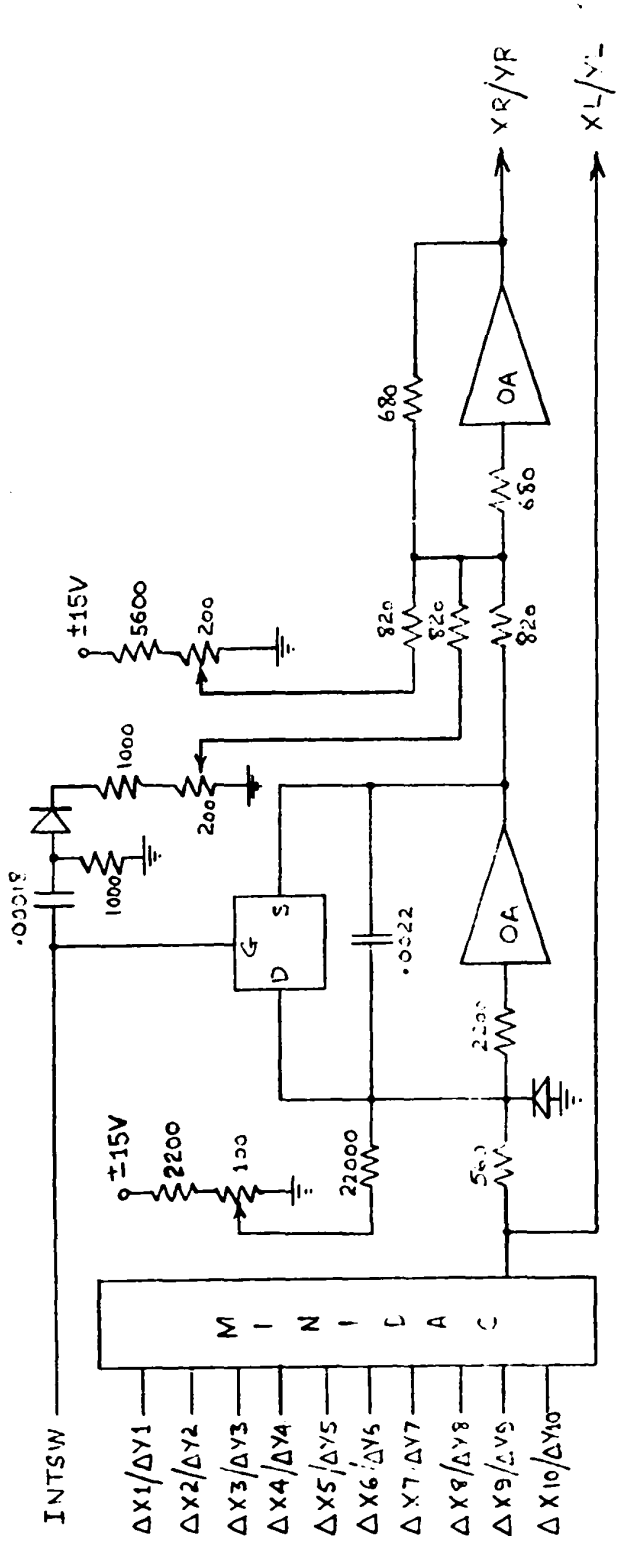
CARDS AB18/CD18/AB19/CD19



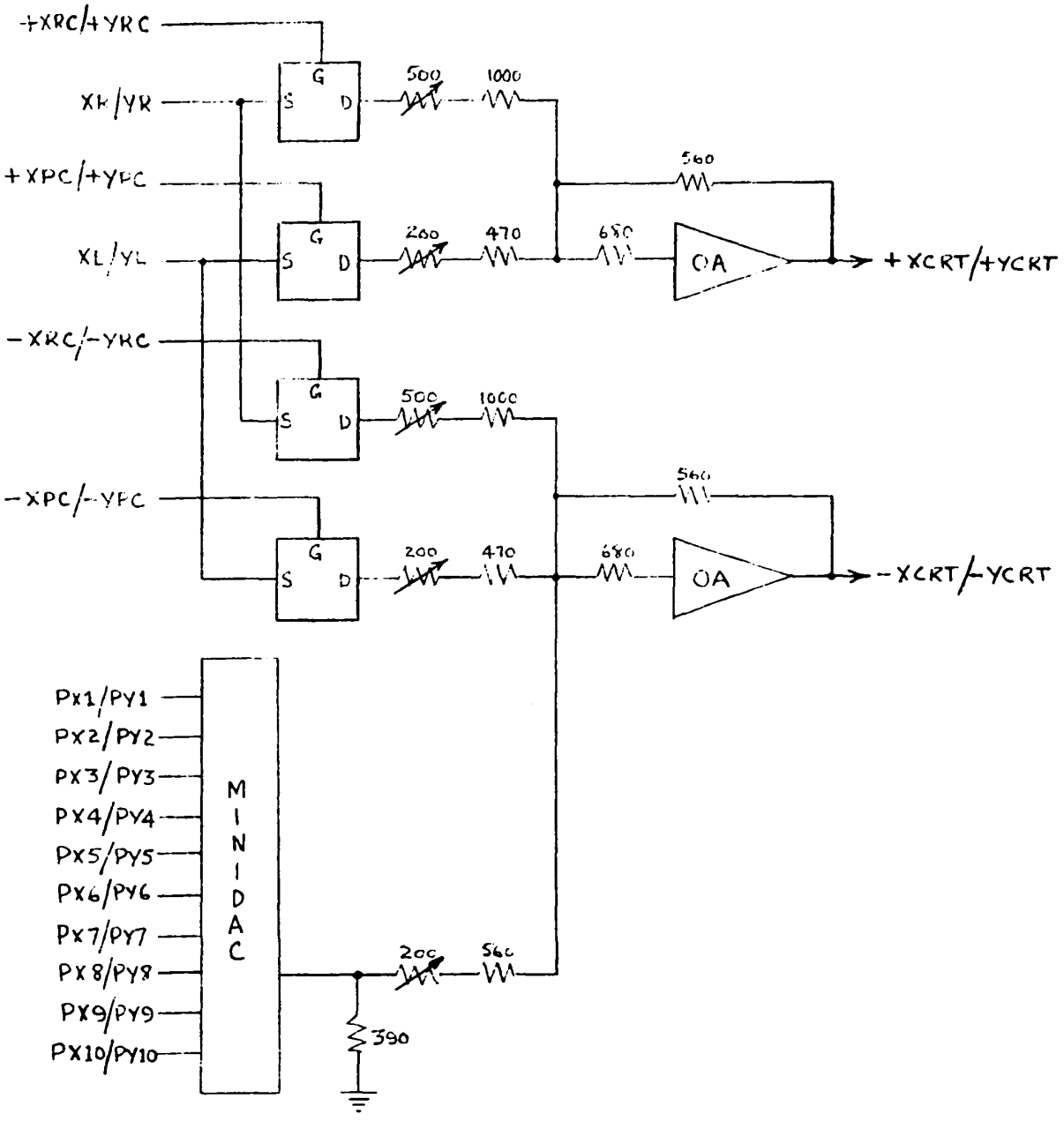
CARDS AB20/CD20



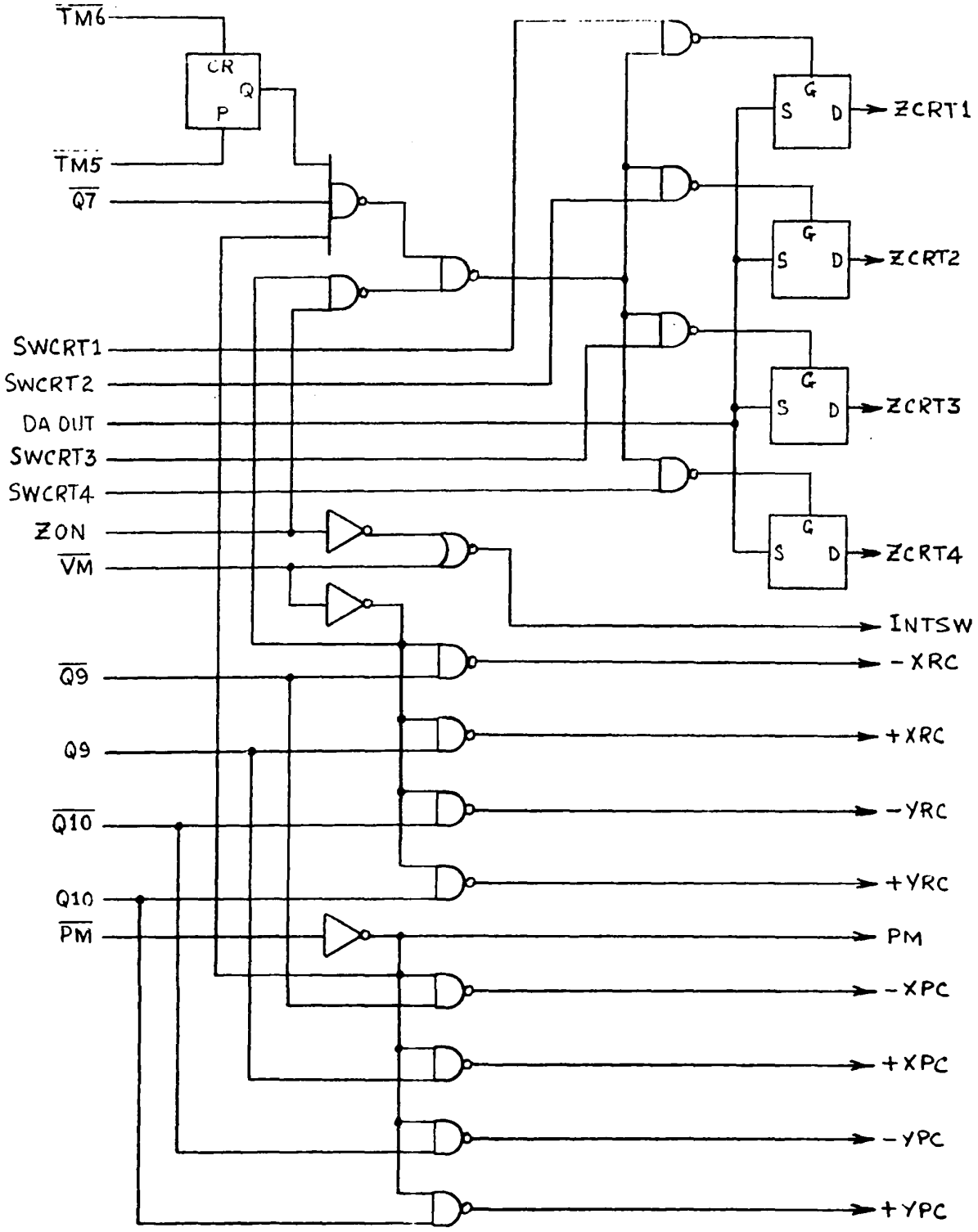
CARDS AB21/CD21/AB22/CD22



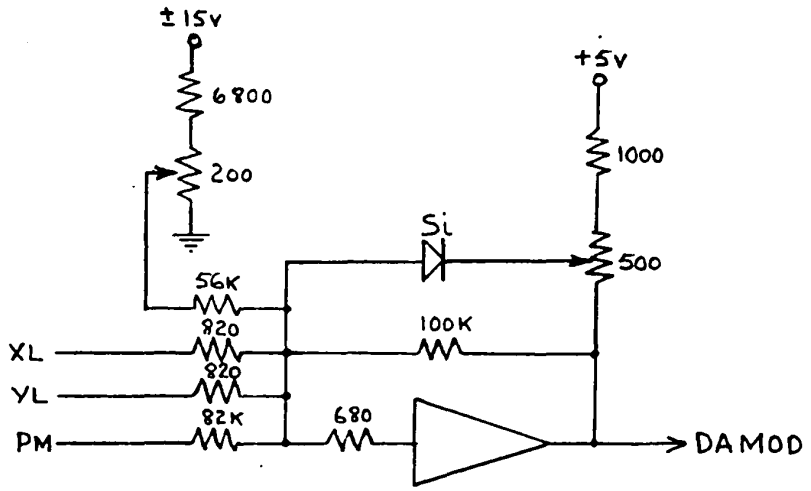
CARDS A825/CD25



CARDS AB28/CD28


TM6
CR
Q
P
TM5
Q7
SWCRT1
SWCRT2
DA OUT
SWCRT3
SWCRT4
ZON
VM
Q9
Q9
Q10
Q10
PM
G
S
D
ZCRT1
ZCRT2
ZCRT3
ZCRT4
INTSW
-XRC
+XRC
-YRC
+YRC
PM
-XPC
+XPC
-YPC
+YPC

CARD AB31


±15v
6800
200
+5v
1000
Si
500
56K
820
100K
XL
820
YL
82K
680
PM
DA MOD

CARD C31

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