SERIES AND PARALLEL VOLTAGE SOURCES SPWM CONVERTERS

BY

Jinbo Kuang

B. Eng., M. Eng. (Tsinghua University, Beijing, China)

Department of Electrical Engineering

McGill University

Montreal, Canada

December 1992

A Thesis submitted to the Faculty of Graduate Studies and Research in partial fulfilment of the requirements for the degree of

Master of Engineering

ABSTRACT

This research work examines how the presently available gate-turn-off thyristors (GTOs), which are still relatively slow, may be used in force-commutated High Voltage Direct Current transmission (HVDC) and Static Var Compensation (SVC) converters by employing series and/or parallel connected multi-converter modules in conjunction with a phase-shifting principle which cancels the undesirable switching harmonics. It points to the advantages of incorporating the well-known Sinusoidal Pulse Width Modulation (SPWM) technique because it enables feedback control, active filtering and regulatory functions to be performed by the converters. This is because a reasonable bandwidth of the modulating signal is transmitted by the multi-converter station in spite of the low switching rates of the GTO valves.

RÉSUMÉ

Ce travail de recherche examine comment les GTO disponibles présentement, qui sont encore relativement lents, peuvent être utilisés pour la transmission haute tension en courant continu en commutation forcée et pour les convertisseurs SVC en employant des modules multi-convertisseur branchés en série et/ou en parallèle en conjonction avec un principe de changement de phase qui annule les harmoniques de commutation indésirables. Il indique les avantages d'incorporer la technique bien connue de modulation sinusoïdale de la largeur d'impulsion parce qu'elle permet un contrôle en boucle fermée, une filtration active et des fonctions regulatrices qui sont accomplies par les convertisseurs. Cela provient du fait qu'une largeur d'onde raisonnable du signal modulé est transmise par la station multi-convertisseur en dépit du faible taux de commutation des valves GTO.

ACKNOWLEDGEMENTS

The author wishes to express his sincere gratitude and appreciation to Dr. Boon Teck Ooi for his valuable guidance and assistance throughout the course of this work. He also thanks to his colleagues Xiao Wang, Yan Guo, Mehrdad Kazerani and Jim Tsai and Professor Zhongchao Zhang for their many helpful advice and assistance. Thanks are also given to Benoit Picard for his translation of Résumé. Many thanks also go to all the professors and colleagues in the power group at McGill University for their helps and friendship.

A special word of appreciation must be offered to my wife Ying Wang for her understanding and encouragement during this work.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CHAPTER I

INTRODUCTION

The valves in the converters of the proposed PWM (Pulse Width Modulation) - HVDC (High Voltage Direct Current transmission) [1-8], the shunt-type PWM-SVC (Static Var Compensation) [9-12], the series-type PWM-SVC [13-15], will consist of gate-turn-off (GTO) thyristors which are connected in series and/or in parallel in order to attain the high MVA ratings. This technique can be supplemented by connecting modules of the PWM-converters in series and/or in parallel [16]. In Ref. [17], it is pointed out that the necessity for the multiple-converter module connections can be turned into an advantage. By phase-shifting the switching instants of the valves in the different modules, the effect of very high frequency switching is created even though the switching rate of the individual valve is low. This method enables the available GTOs, which are still relatively slow, to be employed. With the reduced switching frequency, the switching loss ceases to be a serious problem. Further research in active snubber circuits can improve the efficiency further.

The method of phase-shifting multi-converter modules to eliminate switching harmonics is already in use in the shunt GTO-SVC [9, 10] and in the GTO Power Conditioner [18]. This research work makes further contribution to the existing knowledge by presenting the results of applying this method to one class of the PWM techniques: namely the Sinusoidal Pulse Width Modulation (SPWM) [19]. The SPWM technique is widely known in the literature of power electronics and

furthermore, it rests on solid analytical foundations based on the Double Fourier Series [20]. However, there remains the unexplored territory which has not been covered previously because the requirements of the HVdc or the SVC station are different from those of the Industry Applications Society and the Industrial Electronic Society. The new problems are posed as follows: (1) For the high power GTO valves to operate efficiently, the ratio of the triangular carrier frequency, K_c, to the sinusoidal modulating frequency, K_m, has to be as low as (K_c/K_m) = 2, 3, 4.... For some of the low ratios, the sampling theorem is transgressed. (2) And yet, the PWM-converter stations have been vaunted as being capable of fulfilling diverse "dynamic' duties such as: (a) regulation of dc voltage or of real ac power and/or reactive ac power, (b) active filtering, (c) stabilization and dynamic performance enhancement of the system. Do the PWM-converter stations have the bandwidth to convey the necessary input control information when the GTOs are switching at the low rates?

An important conclusion of Chapter 2 is that when N_m converter modules are operated with the phase shifting technique, the equivalent carrier frequency becomes $N_m K_c$. In consequence, the "dynamic" duties can be fulfilled by making N_m large even though the individual converter module operates with a low value of (K_c/K_m).

It is useful to be reminded that the bipole thyristor HVdc station consists of 4 converter modules connected in series. In addition, the phase shifting technique is already applied in eliminating the 6th harmonic on the dc side. Whereas the phase shifts are obtained through the transformer connections in the line-commutated HVdc, in the force-commutated converters the phase shifts are obtained simply by

delaying the triggering of the valves.

Section 2-1 describes the implementation of the Sinusoidal PWM Strategy using the multi-converter/phase-shifting concept. Section 2-2 presents the properties of SPWM for the single phase converter and the single-phase multi-converters. Section 2-3 presents the results for a 3-phase converter station. The study considers the factors which determine the sizing of the valves and the ability to meet harmonic standards.

Chapter 3 is a feasibility study of the series connection. For the series connection to build up adequate dc voltage withstand, it is necessary to ensure that the voltage stresses are equally distributed in the valves and the diodes. The passive circuits which are normally used for voltage equalization contribute to losses. For this reason, the controllability of the individual modules should enable the dc voltages across the dc link capacitors C to be equalized by local feedback. In this research, the capability of active local feedback equalization of the voltage is assumed.

Chapter 3 concentrates on the potential difficulty that the dc link capacitor C may have to be very large so as to be able to filter out the low harmonic ripples in the dc link voltage, V_{cj}. This is because the existing harmonic elimination principle [16, 25] requires that the dc link voltages to be all ripple-free and equal. This has not been a problem in the parallel-connected converter modules [9, 17, 24, 25] because their dc link currents meet at two common nodes. Thus the low harmonic components of their dc currents have been self-cancelling so that the dc link capacitor has been economically small. The concern of this research is whether the

Total Harmonic Distortion limits (*THD*) for voltages can be met for the low K_c/K_m ratios when economic size capacitors are used.

The happy conclusion of Chapter 3 is that the dc link voltage of the individual converter module can contain significant harmonics so that an economic size capacitor is adequate. Harmonic eliminations by cancellations do take place on both the ac side voltages and dc side voltages thus yielding high quality ac and dc resultant voltage waveforms.

This surprising conclusion shows that the theoretical base of harmonic elimination in Ref. [17, 24, 25] is not sufficiently comprehensive. The harmonic elimination appears to be a property of the symmetrical phase shifting of the triangular carriers signals. The comprehensive theory has still to be worked out.

This research work is based on digital simulations. The number of converter modules connected in series is N_m=8. The dc link voltage is about 32KV or 96KV depending on whether the valve is made up of 1 GTO or 3 GTOs in series. The Total Harmonic Distortion (*THD*) limit for voltage in the 2.3 - 69KV range is 5% [19]. Future study will consider the higher dc voltage rating.

CHAPTER II

PARALLEL CONNECTED MULTI-CONVERTERS

2-1 SPWM MULTI-CONVERTERS

Fig.2-1 shows the voltage-source, 3-phase bridge converter which forms the basic module. The triggering of the valves, in the *a*-phase of the bridge say, is based on the relationship of the modulating signal $S_{maj}(t)$ and its triangular carrier signal $S_{caj}(t)$ as illustrated in Fig.2-2(a). The valves of the same phase operate in the complementary manner: the Upper valve is ON when the Lower valve is OFF, and vice-versa. The states of the valves are described by the switch function $S_{waj}(t)$ which is illustrated in Fig.2-2(b). The switch function takes on either of two values:

$$\begin{aligned} S_{waj}(t) &= +1 \qquad for \quad S_{maj}(t) > S_{caj}(t) \\ S_{waj}(t) &= -1 \qquad for \quad S_{maj}(t) < S_{caj}(t) \end{aligned} \tag{2-1}$$

The terminal voltage on the ac side of the converter of Fig.2-1 is:

$$v_{aj}(t) = 0.5 V_c \, S_{waj}(t) + V_N \tag{2-2}$$

V_c is the dc link voltage and V_N is an unknown voltage which fluctuates according to the switching states of all the valves. V_N can be solved by assembling the circuit theory equations of the converter network and by imposing the constraints describing the physics of the problem.

The attractiveness of the SPWM strategy lies in the fact that the spectrum of

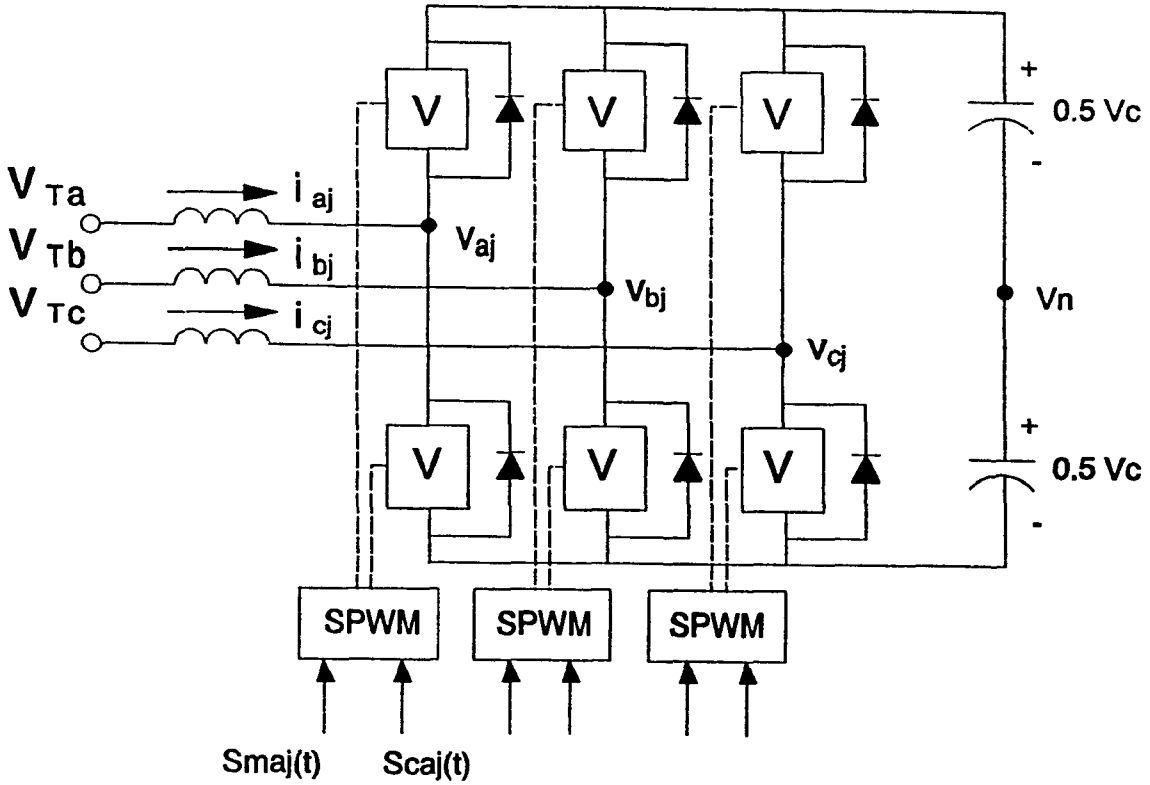

Fig.2-1 3 Phase Voltage Source Converter with SPWM Control

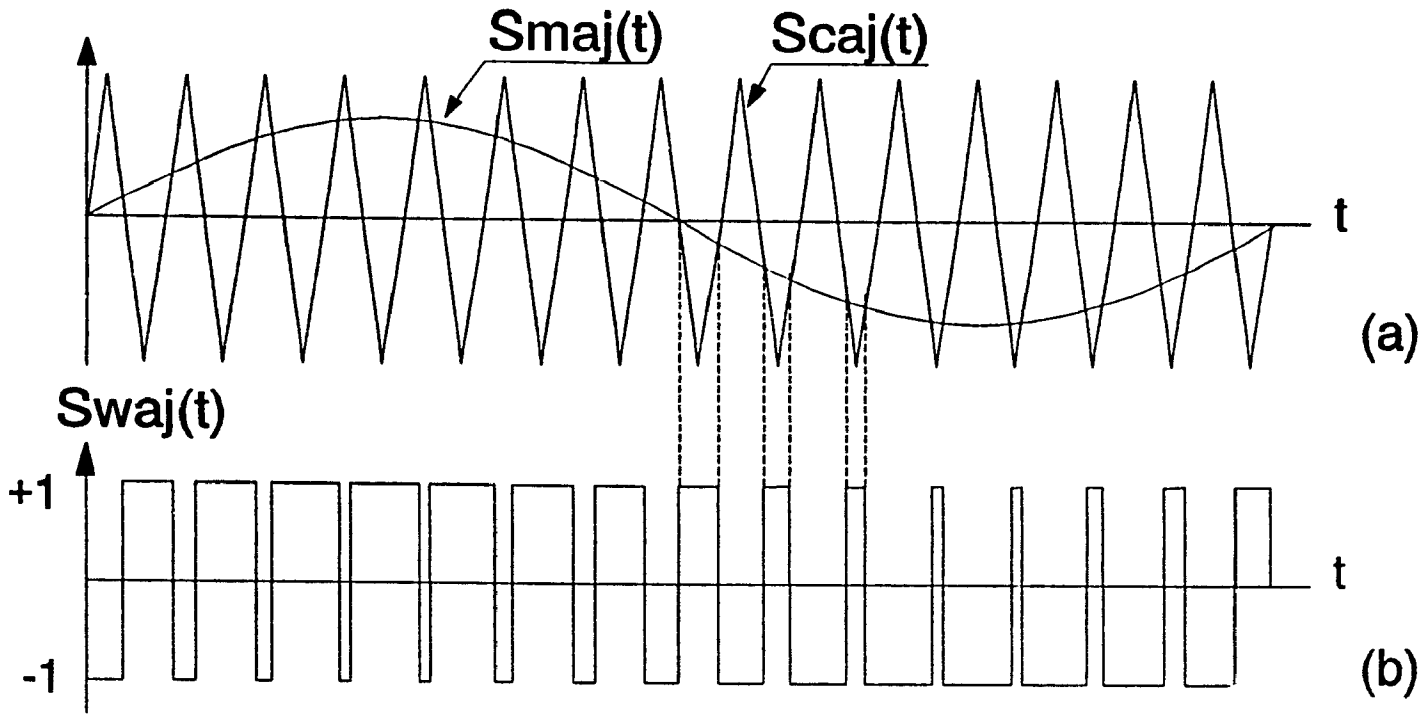

Fig.2-2 (a) SPWM technique - modulating signal $S_{maj}(t)$, triangular carrier signal $S_{caj}(t)$
(b) Switching Function $S_{waj}(t)$

the switching function $S_w(t)$ contains the spectrum of the modulating waveform $S_m(t)$ together with the harmonics of the carriers and the upper and the lower sidebands [19, 20].

Matrix of Converter Modules

It is envisaged that for high power applications, a matrix of identical converter modules as shown in Fig.2-3 is required to build up the voltage ratings by the N_V rows in series and the current ratings by the N_C columns in parallel.

Phase Shifting of Triangular Carrier

Instead of switching the valves in the $N_m = N_C \times N_V$ modules in unison, the effect of a high sampling rate can be achieved by staggering the switching instants of the valves in the individual modules [3, 17]. The method, which is advocated here, consists of dividing the period of the triangular carrier by N_m and assigning each module with a phase delay $\theta_{shj} = 2\pi jK_m /(N_m K_c)$, $j = 1, 2 \ldots N_m$ as shown in Fig.2-5. The routing of the modulating signals of the 3 phases and the carrier signals is illustrated in Fig.2-4. All the SPWM boxes (which determines the switching logic) receive identical modulating signals of the 3 phases. The triangular carrier signal is produced by a triangle waveform template which is read from the EPROM for the jth module. The contents in the carrier waveform EPROMs differ from each other

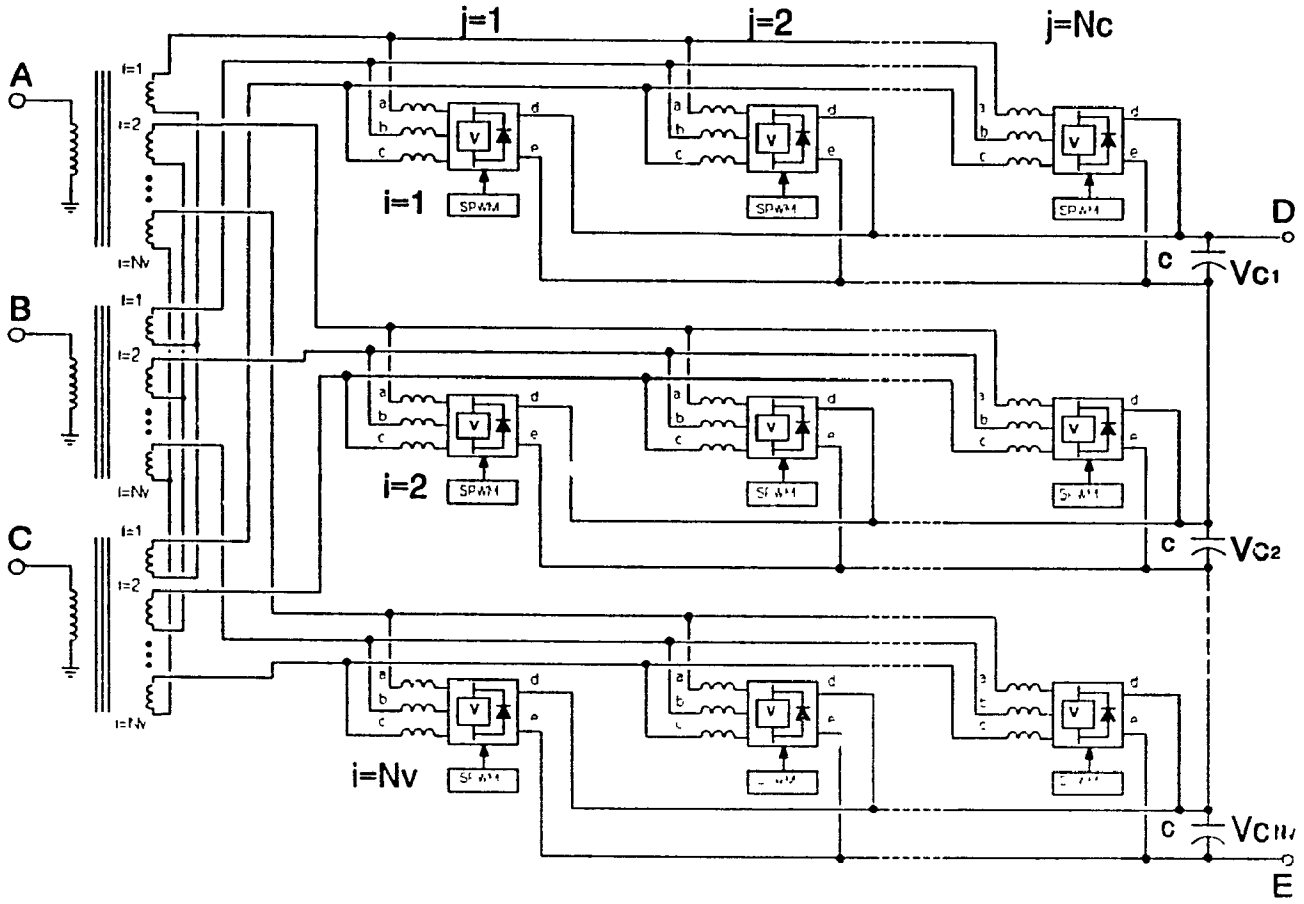

Fig.2-3 Matrix of ($N_m = N_v \times N_c$) 3-phase converters

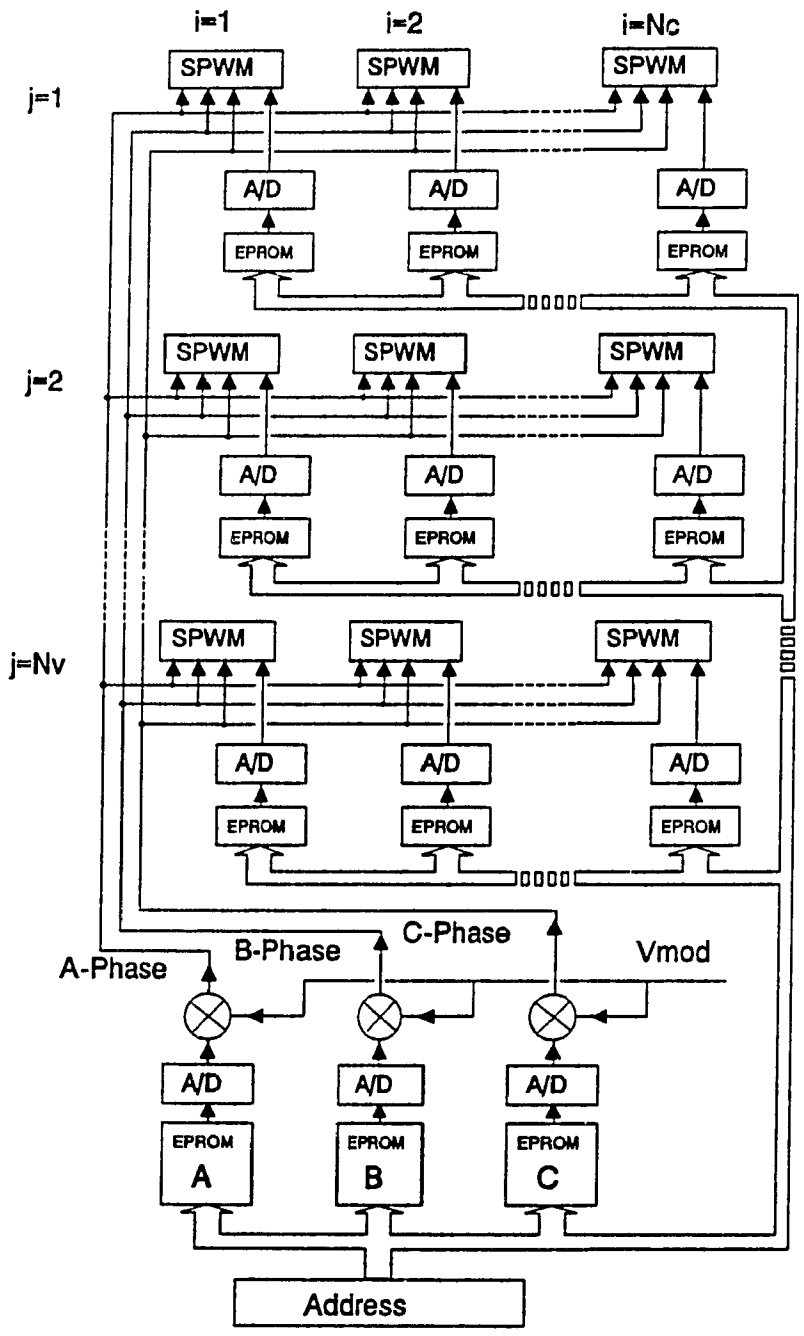

Fig.2-4 Method of implementing SPWM with phase shifted carrier in multi-converter matrix

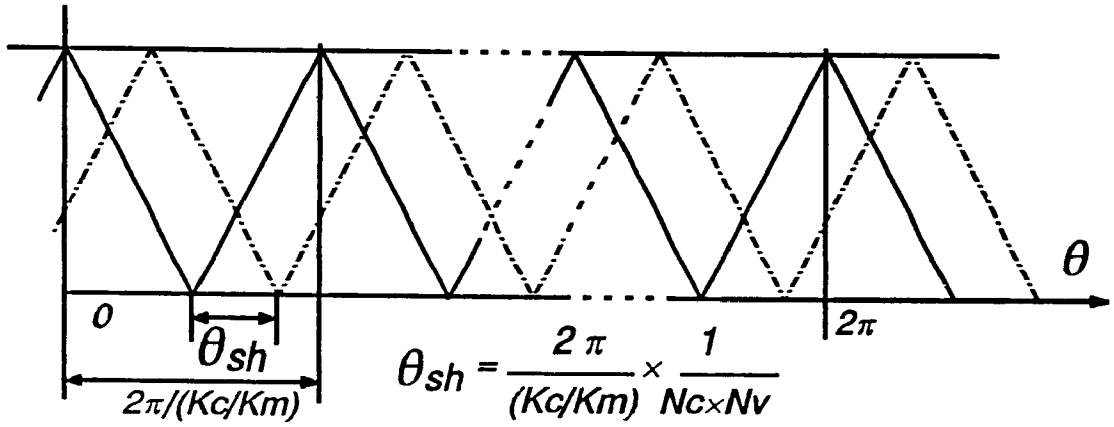

Fig.2-5 Phase shifted triangular carrier for harmonic elimination

by the phase shifts, θ_{shj}, j = 1, 2, ... N_m. The EPROMs are all addressed by the same counter signal.

2-2 PROPERTIES OF SINGLE PHASE SPWM

This section begins by presenting the properties of SPWM from the familiar situation of a high (K_c/K_m) ratio of 21 and then descends to the candidates for GTO applications where (K_c/K_m) = 2, 3, 4... . At such low ratios, the carriers and the sidebands abound in the low order harmonics. Worse still, they interfere with the modulating signal and even create the dc voltage component.

It is shown that by phase shifting the triangular carriers of the multi-converter modules as illustrated in Fig.2-5 many of the carriers and the sidebands can be eliminated. The theoretical principle of harmonic cancellations has been demonstrated in Ref. [17].

Finally, it remains to show that: (1) the magnitude of the modulating signal exercises linear control. (2) the Total Harmonics Distortion in the Voltage is substantially constant as the Modulation Index is varied. (3) the modulating signal waveform can occupy a reasonable frequency bandwidth.

2-2-1 INDIVIDUAL MODULES

In the harmonic spectra presented here, the Fourier Series base is chosen to

be the period of the modulating signal. Thus $M = 1$ corresponds to the frequency of K_m.

High Frequency Carrier SPWM $(K_c/K_m) = 21$

The spectrum in Fig.2-6 for $(K_c/K_m) = 21$ of the waveform of Fig.2-2(b) shows that the harmonics consist of [19, 20]:

(1) $M = 1$, the amplified modulating signal

(2) $M = (K_c/K_m), 3(K_c/K_m), 5(K_c/K_m)...$, the carrier harmonics at odd multiple of (K_c/K_m)

(3) $M = (K_c/K_m) \pm 2$, upper and lower side band

$M = 2(K_c/K_m) \pm 1, 2(K_c/K_m) \pm 2$, harmonics

etc.

Low Frequency Carrier SPWM $(K_c/K_m) = 2$

The spectrum for the case $(K_c/K_m) = 2$ in Fig.2-7 shows the undesirable presence of the dc component, which arises from the lower sideband, $M = (K_c/K_m) - 2$. Although this component can be eliminated by the multi-converter phase shifting technique, $(K_c/K_m = 2)$ cannot be used because the dc voltage in each individual converter gives rise to very large ramp currents.

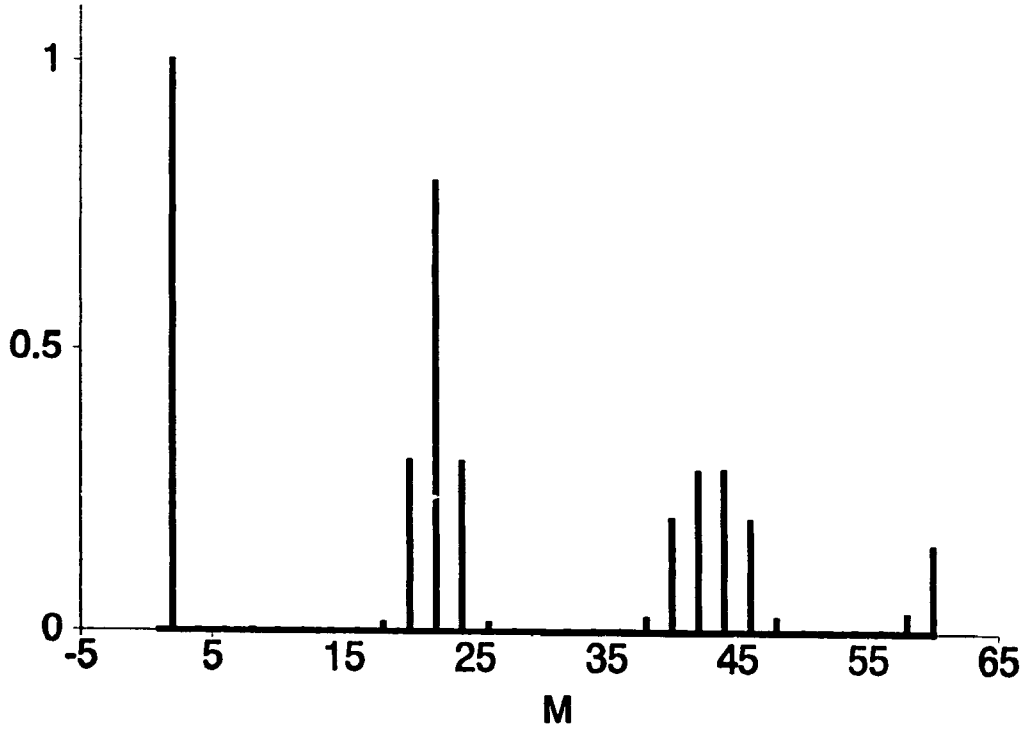

Fig.2-6 Harmonic spectrum. Single Phase (K_c/K_m) = 21, N_m=1

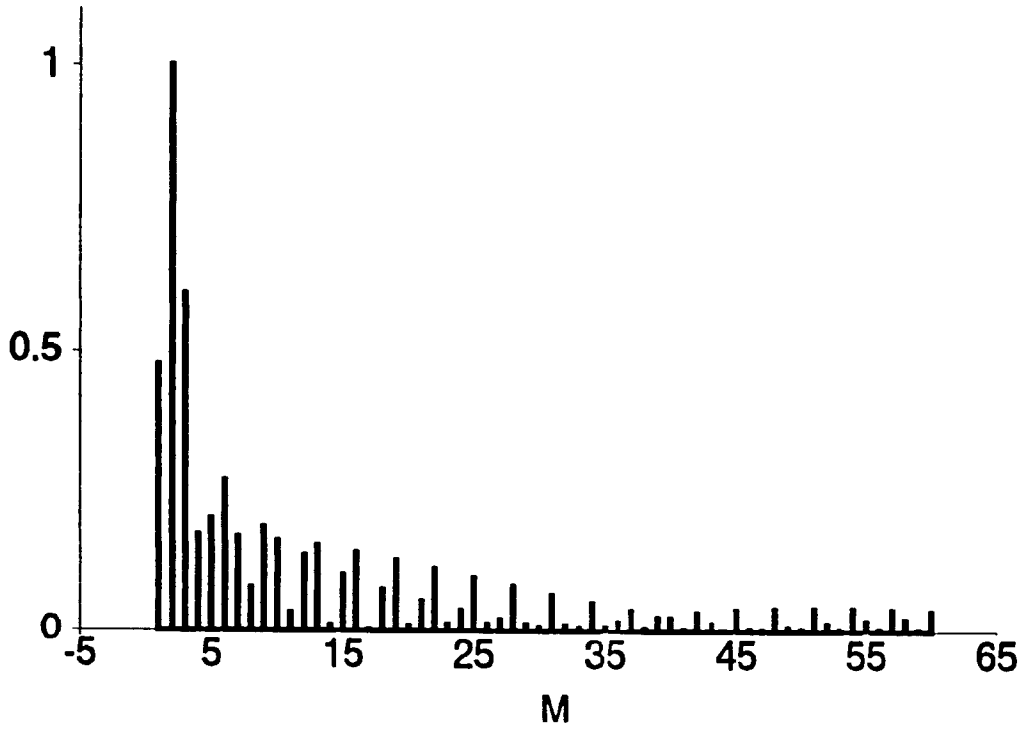

Fig.2-7 Harmonic spectrum. Single Phase $(K_c/K_m) = 2$, $N_m = 1$

$(K_c/K_m) = 3$

The spectrum for the case $(K_c/K_m) = 3$ in Fig.2-8 shows the switching harmonics at $M = (K_c/K_m) = 3$. The first upper sideband harmonic $M = (K_c/K_m) + 2 = 5$ is evident. The lower sideband, $M = (K_c/K_m) - 2 = 1$, is included with the modulating signal $M = K_m = 1$.

The pattern of the remaining significant harmonics are the same as described in conjunction with Fig.2-6 for the case $(K_c/K_m) = 21$. However, because (K_c/K_m) is small, the upper sidebands of one integral multiple of (K_c/K_m) are mixed up with the lower sidebands of the next set. As there is no average component, $(K_c/K_m) = 3$ is an acceptable candidate.

$(K_c/K_m) = 4$

The dc component is present for $(K_c/K_m) = 4$ so that this ratio cannot be used.

$(K_c/K_m) > 4$

The dc voltage component is not present for $(K_c/K_m) > 4$.

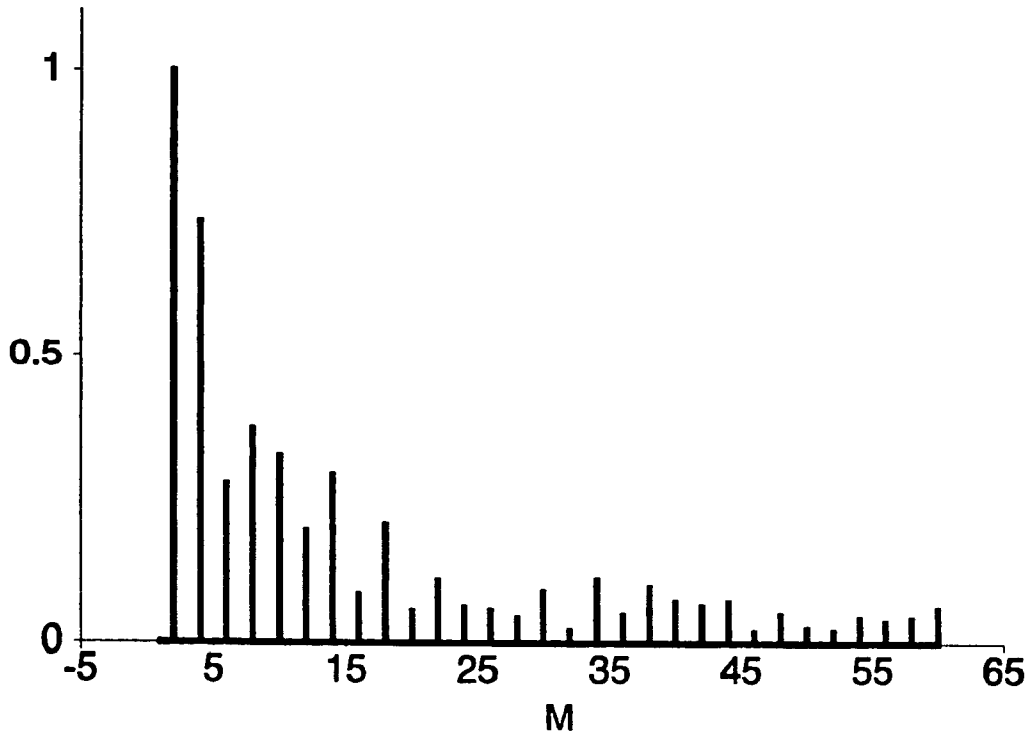

Fig.2-8 Harmonic spectrum. Single Phase $(K_c/K_m) = 3$, $N_m = 1$

2-2-2 MULTIPLE MODULES

$(K_c/K_m) = 3,\ N_m = 7$

Fig.2-9(a) and (b) show respectively the output voltage waveform and the spectrum of N_m (= 7) converters when the phase shifting technique is implemented. One sees that the large low order harmonics in Fig.2-8 are eliminated by the phase shifting technique.

The signal/noise ratio of Fig.2-9(b) is superior to that of Fig.2-6, (K_c/K_m) = 21, N_m = 1 even though both have comparable switching rates.

Modulation Index

The Modulation Index or M.I. is defined [19] as the ratio of the amplitude of the modulating signal $S_{maj}(t)$ in Fig.2-2(a) to the amplitude of the triangular carrier signal $S_{caj}(t)$. Fig.2-10 and 2-11 plot the fundamental harmonic component of Fig.2-2(b) (for (K_c/K_m) = 21, N_m = 1) and of Fig.2-9(a) (for (K_c/K_m) = 3, N_m = 7) as a function of the Modulation Index (M.I.). From the straight line relationship, one concludes that there is a good chance that linear feedback can be implemented by using the magnitude of the modulating signal as a lever of control. In Fig.2-4, this magnitude control is V_{mod}, which is multiplied electronically to the outputs of A, B and C-phase EPROMs which contain the balanced 3-phase sinusoidal waveforms

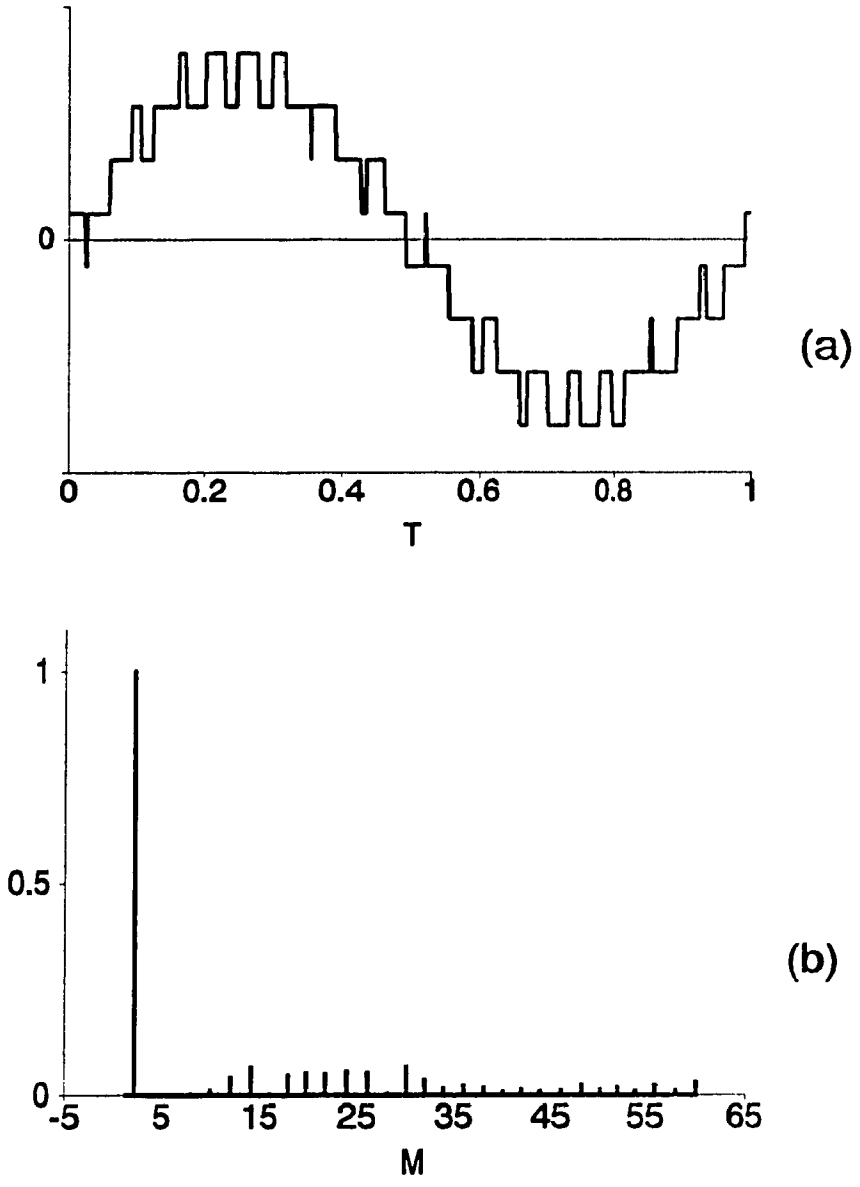

Fig.2-9 Harmonic Spectrum. Single Phase (K_c/K_m) = 3, N_m=7

templates.

Total Harmonic Distortion

Fig.2-10 and 2-11 also show the Total Harmonic Distortion (THD) as a function of the Modulation Index. The THD is per-unitized with respect to the fundamental harmonic component H_1 evaluated at M.I. = 1.0.

$$THD = \frac{1}{H_1} \times \sqrt{\sum_{M=2}^{\infty} H_M^2} \qquad (2\text{-}3)$$

The THD of Fig.2-11 is significantly lower than in Fig.2-10. Fig.2-11 has the desirable feature that the THD remains relatively insensitive to M.I. variation.

Modulating Signal Bandwidth

The question asked next is whether the phase-shifting technique of these slowly switching individual converter modules is capable of amplifying the modulating signal which occupies a reasonable bandwidth, and not just for the single frequency of Fig.2-11. In answering this question, an impulse response test is used. Fig.2-12(a) shows a modulating signal which is a periodic series of alternating impulses, truncated at the 7th Fourier Series component. Fig.2-12(a) depicts the modulating

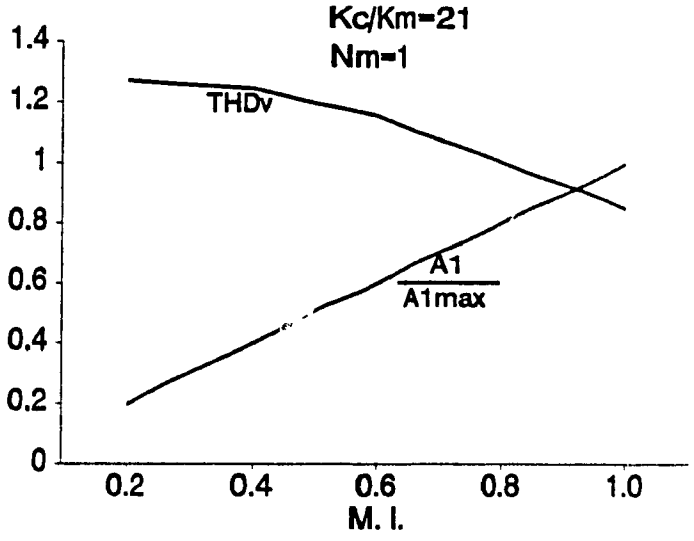

Fig.2-10 Fundamental Harmonic and Total Harmonic Distortion (THD) as a function of Modulation Index (M.I.)
$(K_c/K_m) = 21$, $N_m = 1$

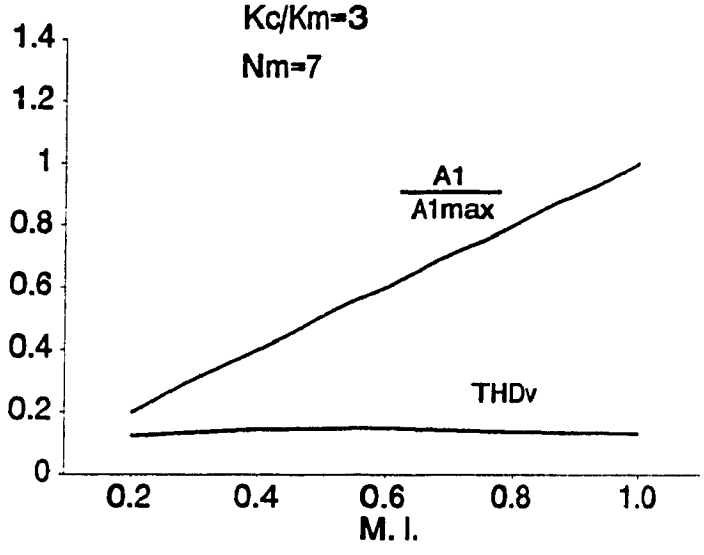

Fig.2-11 Fundamental harmonic and Total Harmonic Distortion (THD) as a function of Modulation Index (M.I.)
$(K_c/K_m) = 3$, $N_m = 7$

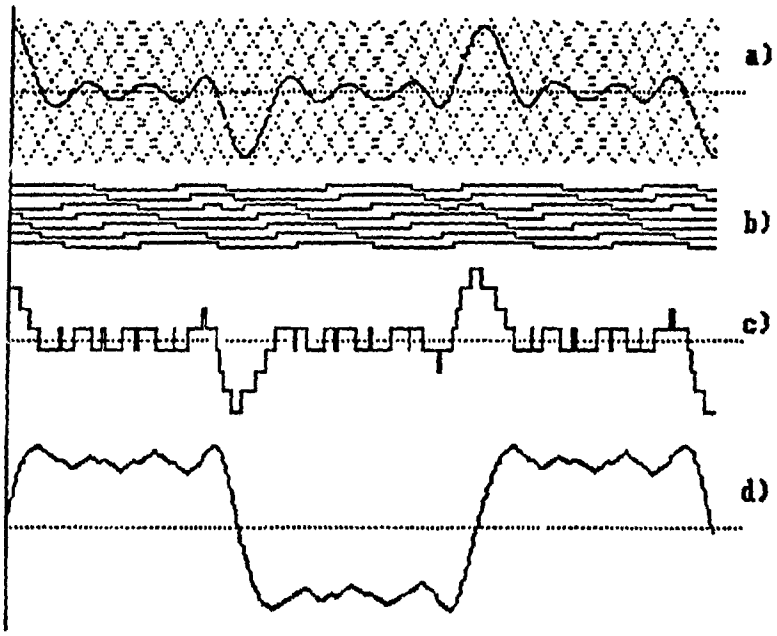

Fig.2-12 (a) Phase shifting technique applied to alternating impulse function truncated at 7th harmonic
(b) SPWM waveforms of N_m (=7) converters switching at $(K_c/K_m)=3$
(c) Summation of voltages of N_m (= 7) converters
(d) Current waveform of inductive load

signal, which is expressed in Fourier Series as:

$$S_M(t)=0.225\sum_{M=1,3,}^{7}\cos(Mwt) \qquad (2\text{-}4)$$

being triangulated by 7 phase-shifted carrier signals which produce 7 sets of square-waveforms as shown in Fig.2-12(b). Their sum is shown in Fig.2-12(c) which resembles the modulating signal in Fig.2-12(a). Fig.2-12(d) depicts the current flowing through an inductive load with the waveform of Fig.2-12(c) as the applied voltage. One recognizes Fig.2-12(d) as an approximation of a square wave based on truncating its Fourier series representation at the 7th harmonic. Fig.2-12(d) is obtained by integrating the waveform of Fig.2-12(c). Fig.2-12(d) shows in a very convincing way that the bandwidth extends to the 7th harmonic.

The equivalent carrier frequency the 7 converters at $(K_c/K_m) = 3$ is $7 \times 3 = 21$. The theoretical limit of the modulating frequency is (1/3) of the equivalent carrier frequency. Fig.2-13 shows the spectrum of the waveform of Fig.2-12(c). The harmonics $M = 1, 3, 5, 7$ are measured as being about 0.225. There is no 8th harmonic. The 9th harmonic, which arises from the switching sideband harmonics, misses interfering with the modulating signal harmonics.

These results show that the bandwidth of the information channel is not limited by the low carrier frequency, K_c, in each individual module. Instead, the effective carrier frequency is $N_m K_c$.

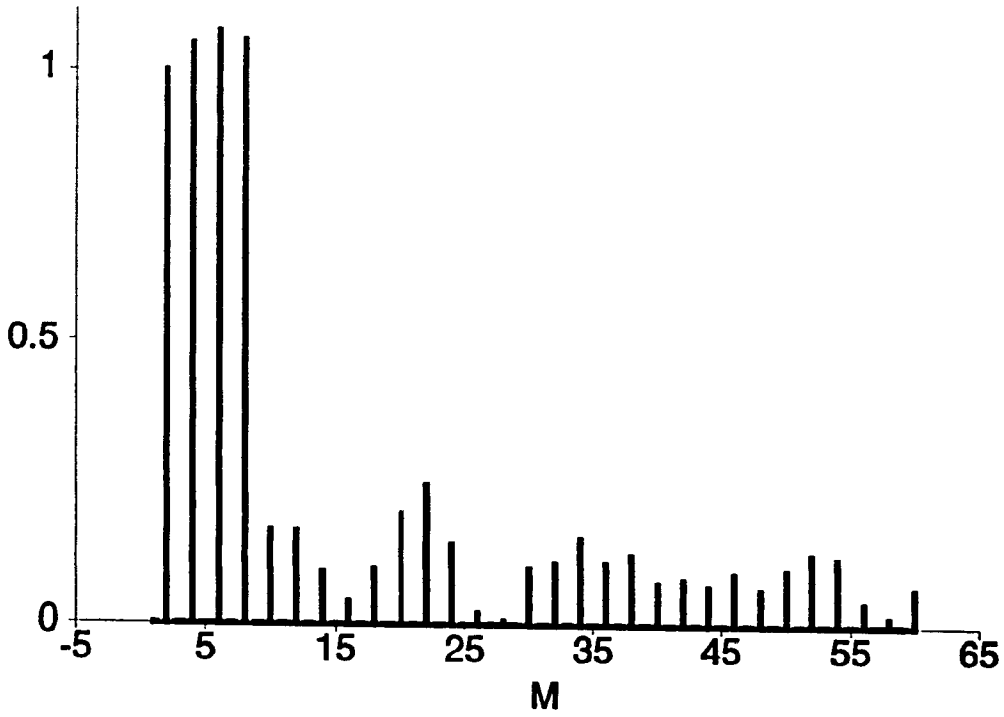

Fig.2-13 Fourier spectrum of Fig.12(c), (K_c/K_m) C, $N_m = 7$

2-3 THREE - PHASE MULTI - CONVERTERS

In our case-study, N_m (=8) three-phase converter modules are connected in parallel as shown in Fig.2-14 to form a station for HVdc or SVC application. The station is connected by way of transformers to the ac side which is represented by ideal 3-phase balanced ac voltages e_a, e_b and e_c and the transmission line resistance R_1 and inductive reactance X_1.

The concern of engineers is to know the size of the reactance X_2 in order that:

(1) the valves do not have to be excessively over-rated.

(2) the THD of the station voltage can meet the harmonic standards. (The THD of the station current is always better than the voltage THD so that the current THD is not evaluated here.)

As shown in Fig.2-14, the transformer primaries are in the wye-connection with a grounded neutral. The study has examined the wye-connected and the delta-connected secondaries and has found little difference between them so that only the results for the wye-connected secondaries are given.

The study consists of assembling the circuit theory equations based on Kirchhoff's Current and Voltage Laws. The transformers are represented as ideal transformers with a magnetizing reactance X_m. The circuit parameters are listed in Appendix A. The valves are each described by the switch function of eq.(2-1). The terminal voltages of the converter phases are described by eq.(2-2). The equations are solved by numerical integration until the steady-state is reached. Accelerated

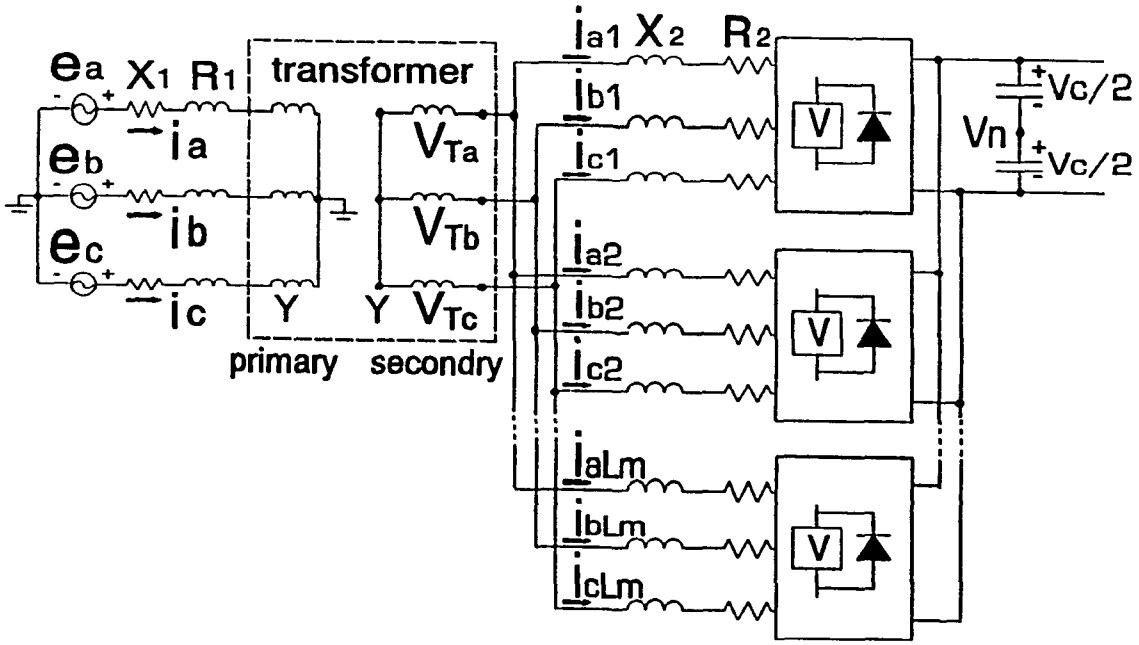

Fig.2-14 Case-study of 3-phase converter station

convergence is achieved by using a large resistance R_f. The number of integration steps per 60 Hz cycle is 6000.

The voltage THD is evaluated at the transformer primary terminal. The results are obtained for 1.0 p.u. dc rectifier power output, keeping V_c = 1.0 p.u. and ac voltage at 1.0 p.u. The modulation Index is M.I. = 0.8.

2-4 CASE - STUDY RESULTS

In the study results of Fig.2-15 and 2-16, the p.u. values are referred to the base values of a single 3-phase converter module, described in Appendix C. The base enables the sizing of the valves to be made from Fig.2-15 using the rms current-vs - X_2' graph. The 1.0 p.u. current corresponds to the base current of the converter module.

Fig.2-16 shows the voltage THD as a function of X_2'. Fig.2-15 and 2-16 are based on assuming that the dc voltage V_c is constant, coming from an ideal voltage source.

The results in Fig.2-17 are based on replacing the ideal voltage source representation of V_c by the voltage charged across the dc link capacitor. The size of the capacitor is given as the reactance X_c, per-unitized with respect to Z_{base} of the entire ac system. Fig.2-17 plots the THD of V_{Ia} and V_c as a function of X_c (keeping X_2' = 0.2).

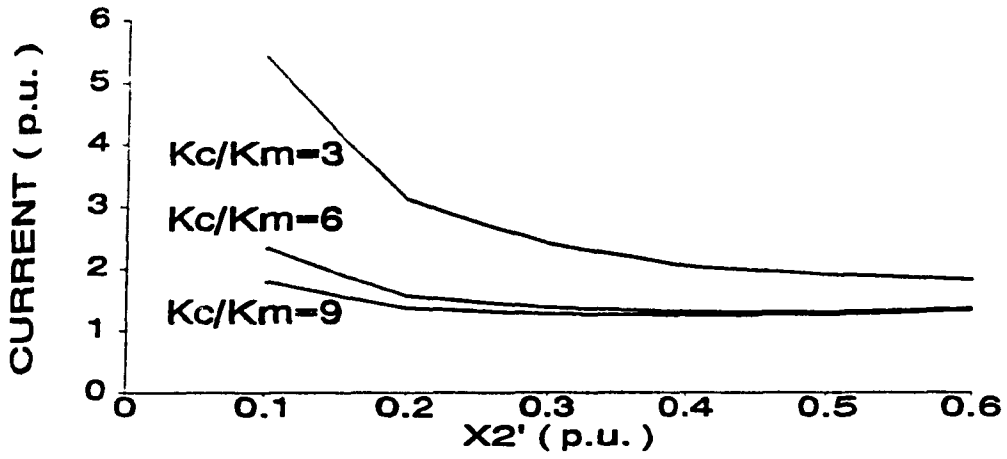

Fig.2-15 Converter phase current vs X_2', (K_c/K_m = 3, 6, 9)

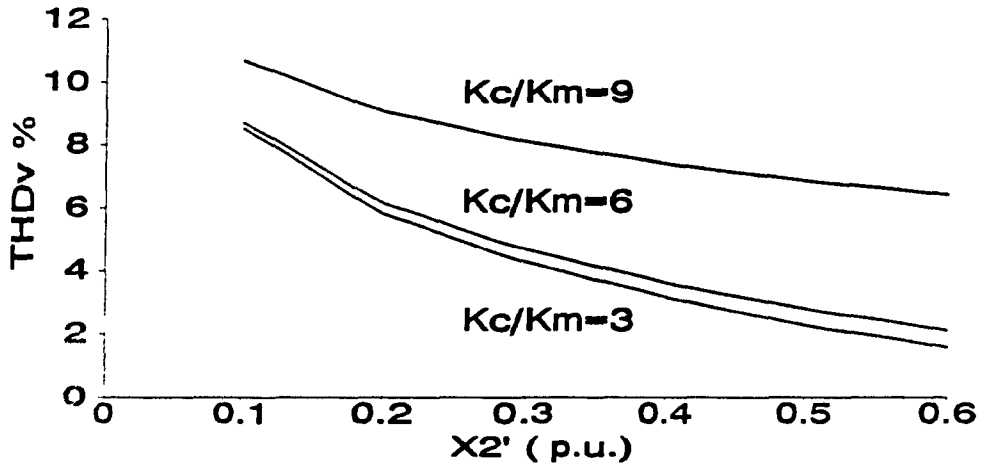

Fig.2-16 Total Harmonic Distortion (Voltage) vs X_2'
(K_c/K_m = 3, 6, 9)

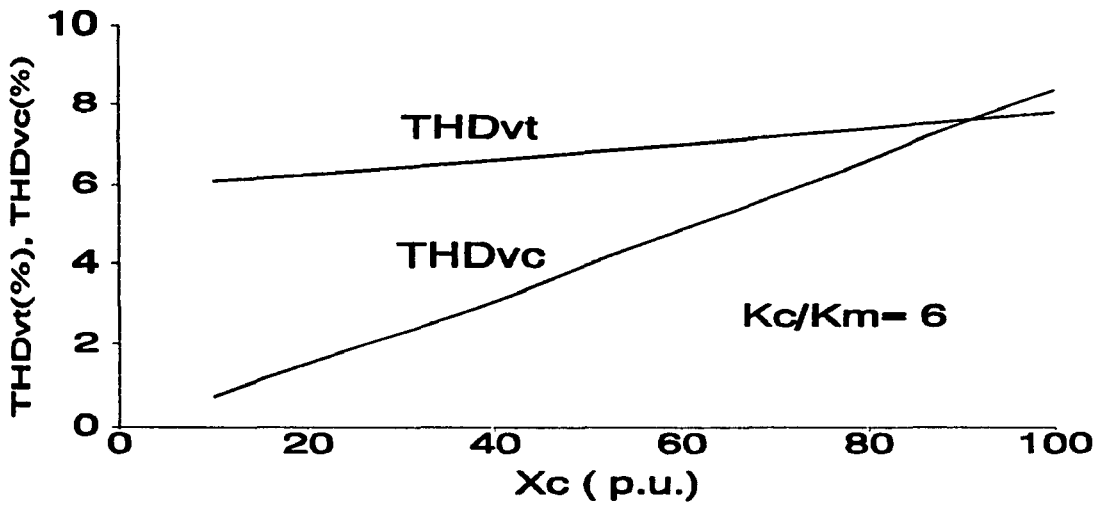

Fig.2-17 THD_v of AC Voltage and V_c as a function of X_c (X_2' = 0.2 p.u.)

2-5 REMARKS

Using data such as those given in Fig.2-15, the designer has to optimize the total cost. The cost of X_2' (based on its VA rating, which corresponds to the p.u. value of X_2') is less expensive than the cost of the valves (p.u. rms current).

The cost of X_2' is already paid for, in part, because it serves the function of reducing the THD_v as shown in Fig.2-16. The phase-shifting technique applied to N_m modules has cancelled the low harmonic components (illustrated in Fig.2-8) leaving behind the residual high harmonic components (illustrated in Fig.2-9), which expressed as THD has the approximate figure given in Fig.2-11. The further attenuation of the THD_v in Fig.2-16 is a consequence of the voltage division, approximately in the ratio of $X_1/(X_1+X_2')$, for the case-study of Fig.2-14.

Fig.2-16 shows that for the low values of X_2', the THD_v exceeds the harmonic standards [19, 21]. A high frequency filter, such as the one presently used in thyristor technology, can remove the residual high frequency harmonic components. The cost of X_2' is offset by the savings from the conventional tuned harmonic filters, which are no longer necessary.

On the dc side, the conventional tuned harmonic filters are replaced by a single dc capacitor, the size of which is given as X_c in Fig.2-17. Fig.2-17 presents the results for the conservative case, $X_2' = 0.2$.

There are improvements to be gained by increasing $N_m = 8$ to a larger number.

Notes on Per-Unitizing

In Appendix C, the system bases are chosen on the transformer primary side. The secondary to primary turns ratio is n. The P.U. Bases of each converter module reflect the fact that there are N_m modules connected in parallel. Using the Z'_{base} of Appendix C, X_2'($=X_2 / Z'_{base}$) in Fig.2-15 and 2-16 gives an estimate of its comparative cost irrespective of wye-wye or wye-delta connections. The ordinate in Fig.2-15 is a guide as to over-rating of the valves needed to accommodate harmonic losses. On the dc side, the capacitor size C is per-unitized as $X_c = 1/(377C \cdot Z_{base})$ in Fig.2-17. Power engineers are familiar with cost based on per-unitized reactances.

CHAPTER III

SERIES CONNECTED MULTI - CONVERTERS

3-1 SERIES MULTI - CONVERTERS

Fig.3-1 shows the converter station based on the series connection of N_m voltage-source PWM converter modules. The detail schematic of each converter module block diagram of Fig.3-2(a) is shown in Fig.3-2(b). The triggering of the valves, of the a-phase of the *jth* module say, is based on the Sinusoidal Pulse Width Modulation strategy which uses the intersections of the sinusoidal modulating signal $S_{maj}(t)$ and the triangular carrier signal $S_{caj}(t)$, as illustrated in Fig.3-3(a), to determine switching instants of switching function $S_{waj}(t)$ in Fig.3-3(b). The valves of the *a-j* phase are triggered as follows in response to the switching function:

$$\begin{aligned} S_{waj}(t) = 1 \quad & \textit{upper valve ON} \\ & \textit{lower valve OFF} \\ S_{waj}(t) = -1 \quad & \textit{upper valve OFF} \\ & \textit{lower valve ON} \end{aligned} \tag{3-1}$$

In this chapter, the utility system is modelled by the ideal voltage sources e_a , e_b , e_c and equivalent impedances R_1 and jX_1. The transformer connections are wye-delta, with the secondary impedances N_mR_2 , jN_mX_2 connected as shown in Fig.3-1.

The dc voltage V_{dc} is based on the sum of the voltage V_{cj} across the capacitor C between the terminals d_j - e_j.

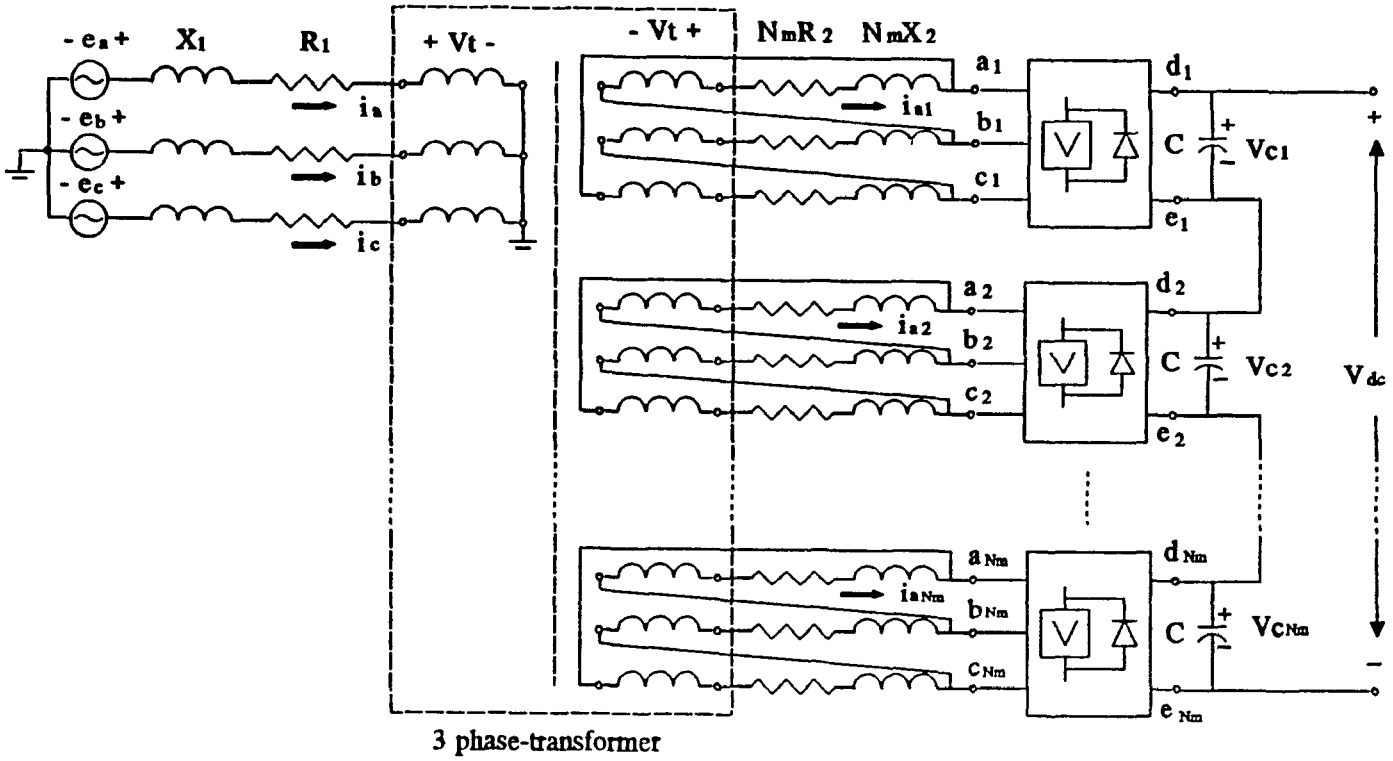

Fig.3-1 Schematic of series-connected, voltage-source PWM bridge converters

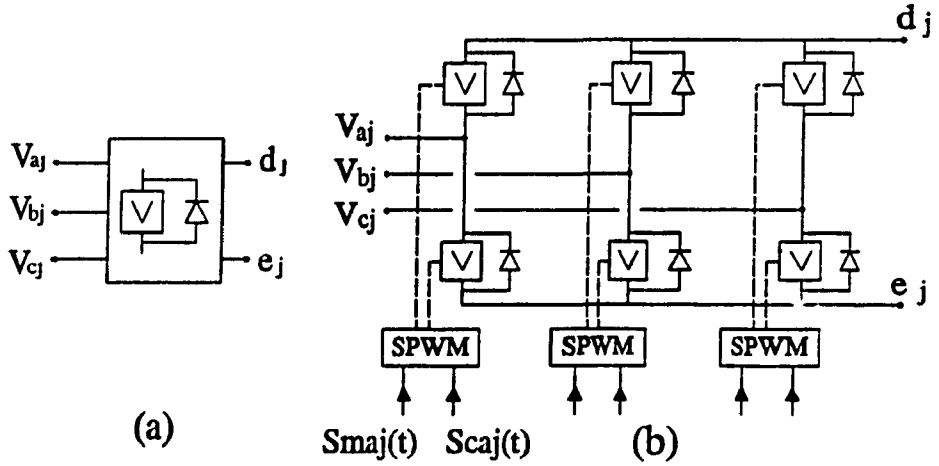

Fig.3-2 (a) Symbol of Voltage-Source PWM bridge converter
(b) Detail schematic of bridge converter

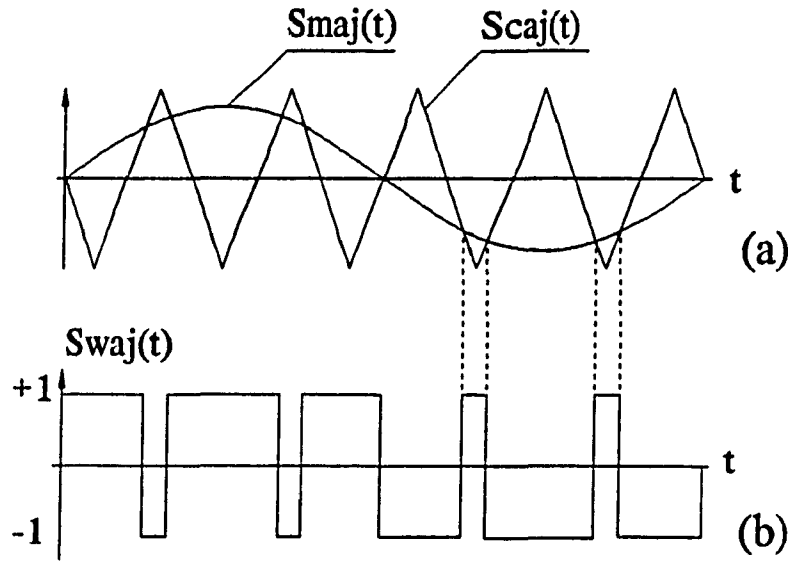

Fig.3-3 SPWM control of a-phase, jth converter module
(a) Modulation Signal $S_{maj}(t)$, Triangular Carrier Signal $S_{caj}(t)$
(b) Switching Function $S_{waj}(t)$

$$V_{dc}=\sum_{j=1}^{N_m} V_{cj} \tag{3-2}$$

In sizing the capacitor C, its capacitive reactance at 60Hz is per-unitized as $Xc=1/(377CZ_{base})$.

3-1-1 HARMONICS OF SPWM

The voltage at the a-terminal, say, of the *jth* converter module is:

$$V_{aj}=0.5S_{waj}(t)V_{cj}(t) \tag{3-3}$$

where $V_{cj}(t)$ is the voltage across the dc link capacitor C, and $S_{waj}(t)$ is the switching function of Fig.3-3(b). The analysis of the Sinusoidal Pulse Width Modulation strategy is based on expressing $S_{waj}(t)$ as a Double Fourier Series [25]. In the analysis here, the Double Fourier Coefficients are expressed in the polar form (S_{mn}, φ_{mn}), which are respectively the magnitude and the phase angle of the *(m,n)th* harmonic.

Eq.(3-3) is then expressed as:

$$V_{aj}=0.5V_{cj}(t)\sum_{m}^{\infty}\sum_{n}^{\infty} S_{mn}\cos[(nK_c+mK_m)\omega t+\varphi_{mn}] \tag{3-4}$$

where K_c = frequency of the triangular carrier (Hz)

K_m = frequency of the modulation signal (Hz)

$\omega=2\pi$ rad/s

m,n = Double Fourier series integers

3-1-2 PHASE SHIFTED TRIANGULAR CARRIERS

The multi-converter switchings are based on sending identical modulation signals $S_{ma}(t)$, $S_{mb}(t)$, $S_{mc}(t)$ to the SPWM blocks of Fig.3-2(b) of every converter module. However, the *jth* module receives the triangular carrier signal which is phase shifted by $j\theta_{sh}$, $j = 1, 2 \cdots N_m$. The phase-shift angle is defined as:

$$\theta_{sh} = \frac{2\pi}{(K_c/K_m)N_m} \tag{3-5}$$

as illustrated in Fig.3-4. The effect of the $j\theta_{sh}$ phase shift in the triangular carrier signal is to introduce a phase shift of $(jn2\pi/N_m)$ in the cosine argument in eq.(4). As viewed from the primary side, the effect of the contributions of all the N_m modules is the summation:

$$\begin{aligned} V_{at} &= \sum_{j=1}^{N_m} V_{aj} \\ &= 0.5 \sum_{j=1}^{\infty} \{V_{cj}(t) \sum_{m}^{\infty} \sum_{n}^{\infty} S_{mn} \cos[(nK_c + mK_m)\omega t + \\ &\varphi_{mn} + (jn2\pi/N_m)]\} \end{aligned} \tag{3-6}$$

The $(jn2\pi/N_m)$ term in eq.(3-6) is introduced by the triangular carrier phase shift.

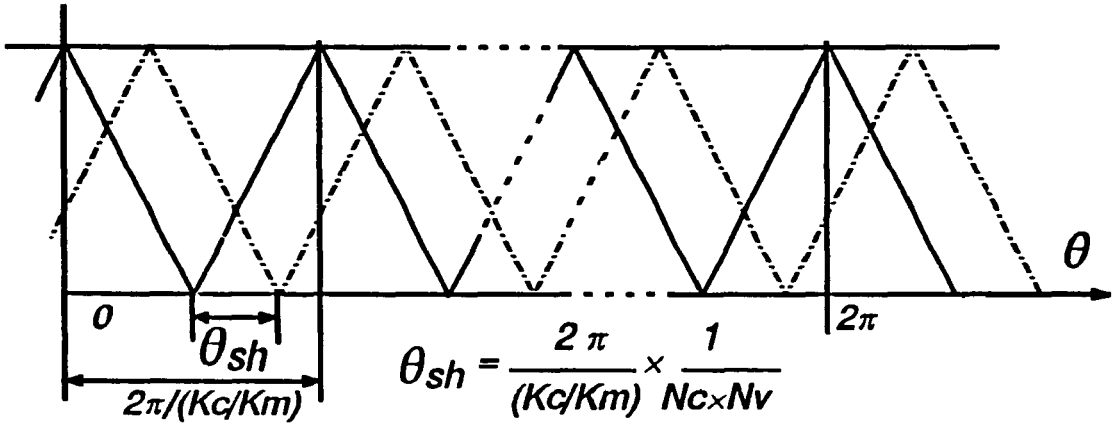

Fig.3-4 Phase shifted triangular carrier for harmonic elimination

3-2 Method I: HARMONIC ELIMINATION - EQUAL AND CONSTANT DC LINK VOLTAGES

By making the dc link voltages of all the modules equal and constant, that is:

$$V_{cj}(t) = V_{cc} \qquad j=1,\ 2\cdots N_m \tag{3-7}$$

it is possible to interchange the order of the triple summation in eq.(3-6) so that:

$$V_{at}=0.5V_{cc}\sum_{m}^{\infty}\sum_{n}^{\infty}S_{mn}\left(\sum_{j=1}^{N_m}\cos[(nK_c+mK_m)\omega t + \varphi_{mn}+(jn2\pi/N_m)]\right) \tag{3-8}$$

The innermost summation of eq.(3-8) yields:

$$\sum_{j=1}^{N_m}\cos(\xi+jn2\pi/N_m) = N_m\cos\xi \qquad for\ j = LN_m \tag{3-9-a}$$

$$= 0 \qquad for\ j \neq LN_m \tag{3-9-b}$$

$$L=1,\ 2,\ 3\ \cdots$$

where

$$\xi = (nK_c + mK_m)\omega t + \varphi_{mn} \tag{3-10}$$

Fig.3-5(a) and (b) show the phasor representation of the summation of eq.(3-9-a) and (3-9-b) which lead respectively to non-cancelling addition and harmonic cancellation.

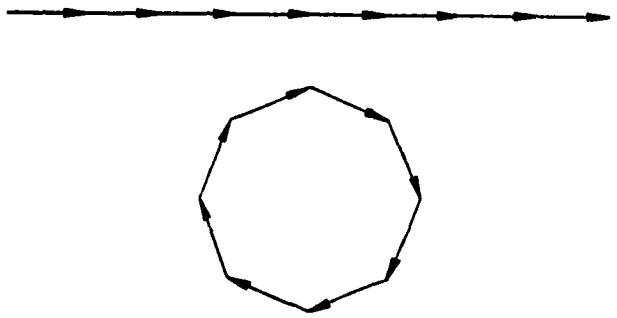

Fig.3-5 Principle of harmonic cancellations
(a) Additive phasors
(b) Phasor additions leading to cancellations

Practical Implications

Since the harmonic cancellation principle of eq.(3-9-b) depends on the dc link voltages of all the N_m converter modules being equal and constant, it is anticipated that the dc link capacitance C must be large so as to be a constant voltage. To keep the switching losses low, the (K_c / K_m) ratio has to kept low. The filtering of the low harmonics is generally expensive.

Fig.3-6 shows that for $Xc = 1.0$ p.u., $K_c / K_m = 5$, V_{cj} is almost ripple free. The *THD* of V_{dc} and Vt are respectively 0.06% and 4.7%. The high quality waveform of Vt is a consequence of the harmonic elimination based on eq.(3-9-b) as illustrated by the phasor diagram of Fig.3-5(b).

It is worth remembering that Xc is the capacitive reactance of the capacitor C for one module of Fig.3-1 per-unitized with respect to the Z-base of the primary side.

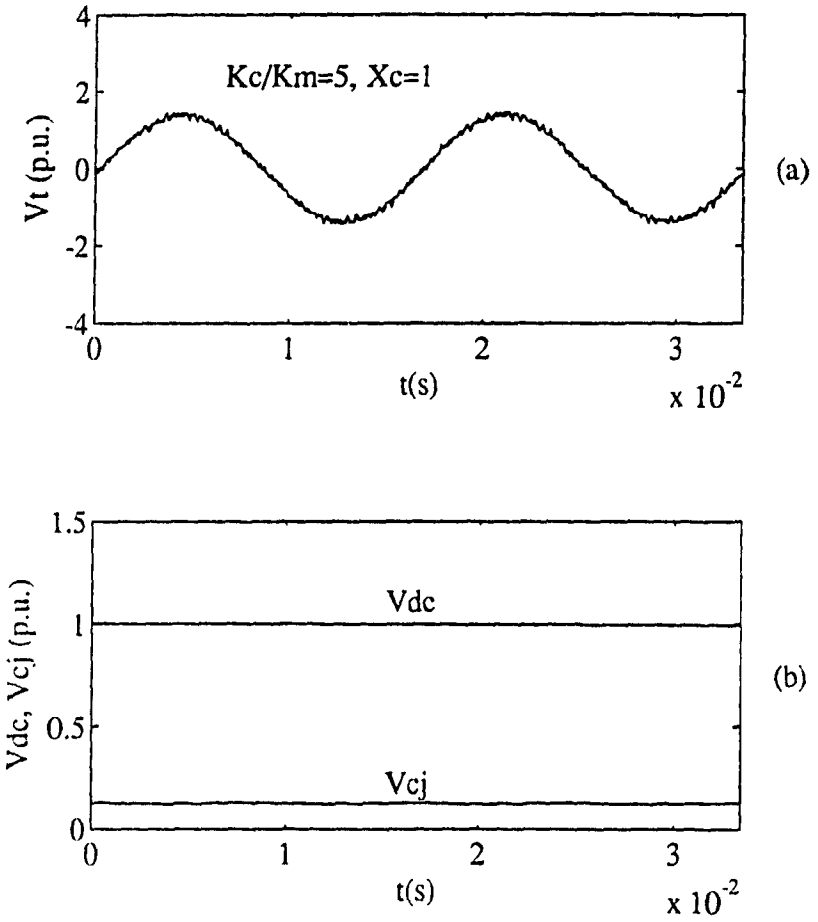

Fig.3-6 (a) Transformer terminal voltage
(b) DC link voltage
V_{dc} , V_{cj} - total, jth module
K_c / K_m = 5, X_c = 1 p.u.

3-3 Method II: HARMONIC ELIMINATION-SYMMETRICAL PHASE SHIFTING

From consideration of symmetry, there is a possibility that harmonic cancellation will take place simply from the scheme of symmetrical phase shifting of the triangular carriers by the amount $j\theta_{sh}$, $j=1, 2, 3 \cdots N_m$. Thus the constant dc voltage assumption of eq.(3-7) may not be a necessary condition of harmonic elimination. It is true that eq.(3-7) will ensure the mathematical cancellation described by eq.(3-9-b). But it is possible that eq.(3-9-b) is a special case of a more general theory of harmonic elimination which has yet to be worked out.

Fig.3-7 and 3-8 present the results of an investigation on the effects of increasing Xc (decreasing C) to the extent that the dc link voltage V_{cj} will not be constant. One sees that after passing the resonance peaks around $Xc \approx 7$ p.u., the *THD* of the ac voltage at $Xc = 10$ p.u. is comparable to that of the more costly $Xc = 1.0$ p.u. The *THD* of the dc voltage deteriorates although it is still below the 5% limit

Fig.3-9 and 3-10 show respectively the time and the frequency domain representations of the voltages Vt , V_{dc} and V_{cj} for $K_c/K_m = 5$. One sees that for $Xc = 10$ p.u., the voltage V_{cj} carries significant harmonics. Nevertheless, harmonic eliminations take place to yield a high quality total ac voltage, Vt, and total dc voltage, V_{dc} . V_{dc} carries a 6th harmonic of 2.58%. The 6th harmonic in V_{cj} in Fig 3-10(b) is also around 2.58%, indicating that it has been additive from the $N_m = 8$ converter modules.

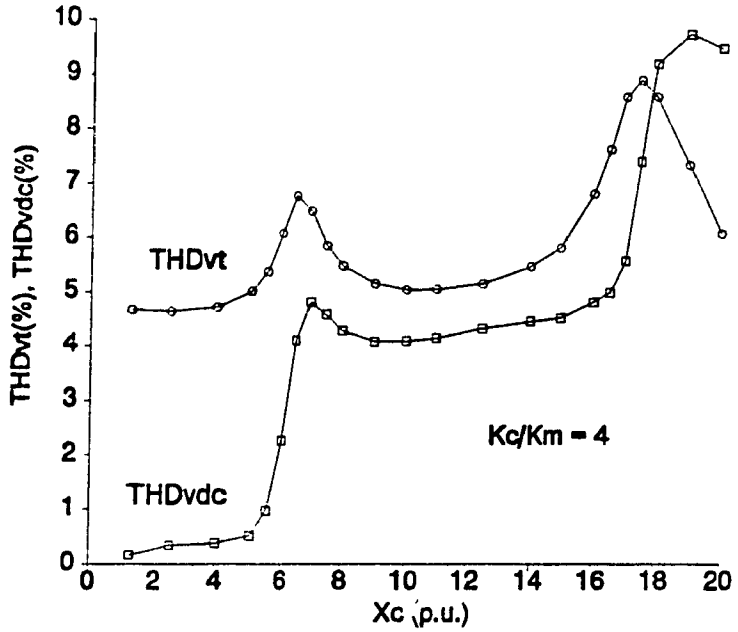

Fig.3-7 Total Harmonic Distortion -vs- X_c , K_c /K_m = 4

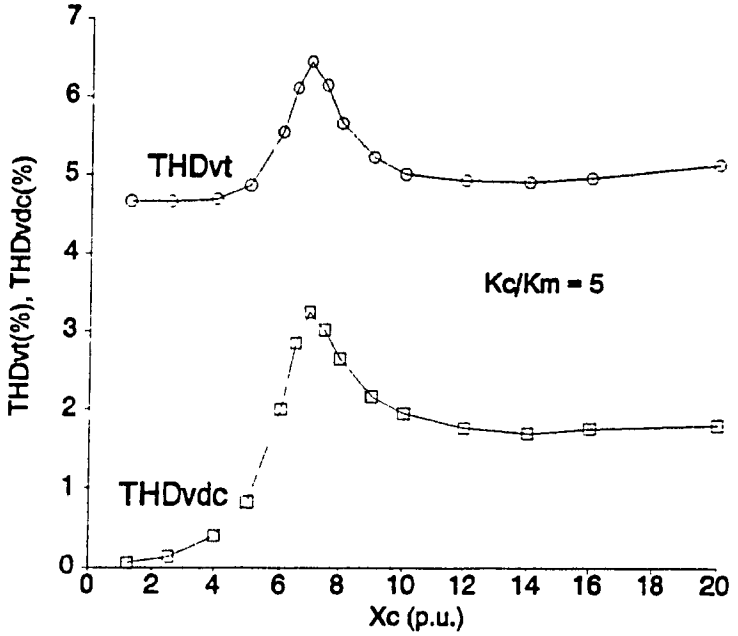

Fig.3-8 Total Harmonic Distortion -vs- X_c , K_c /K_m = 5

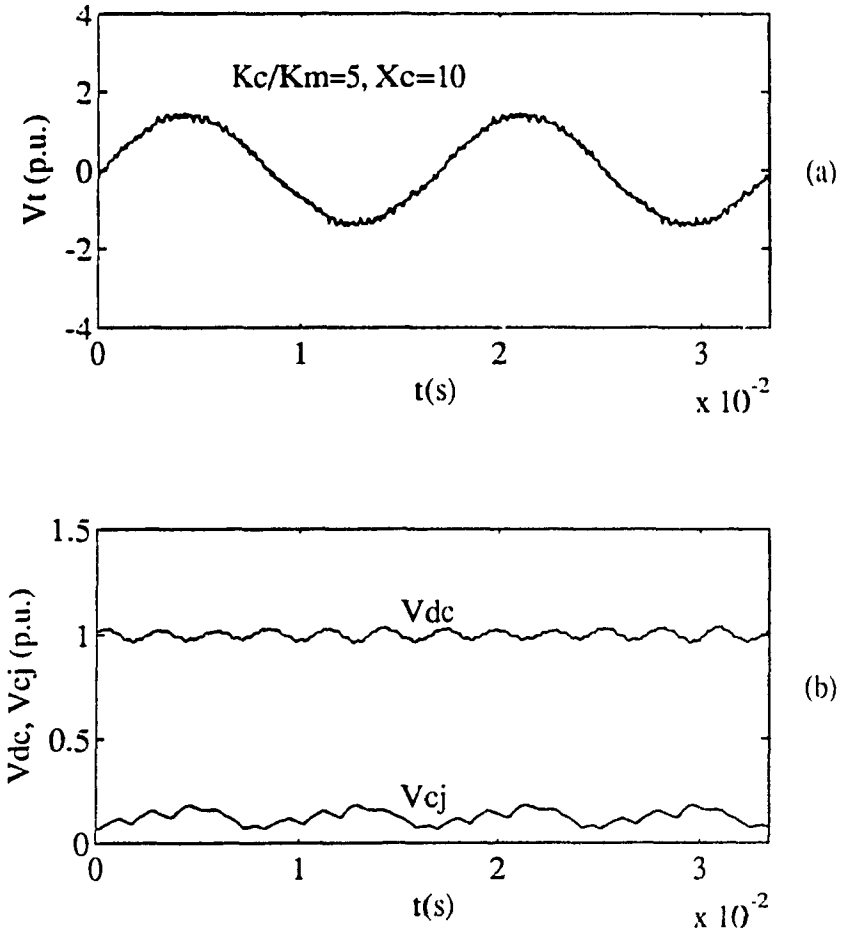

Fig.3-9 (a) Transformer terminal voltage
(b) DC link voltage
V_{dc} , V_{cj} - total, jth module
K_c / K_m = 5, X_c = 10 p.u.

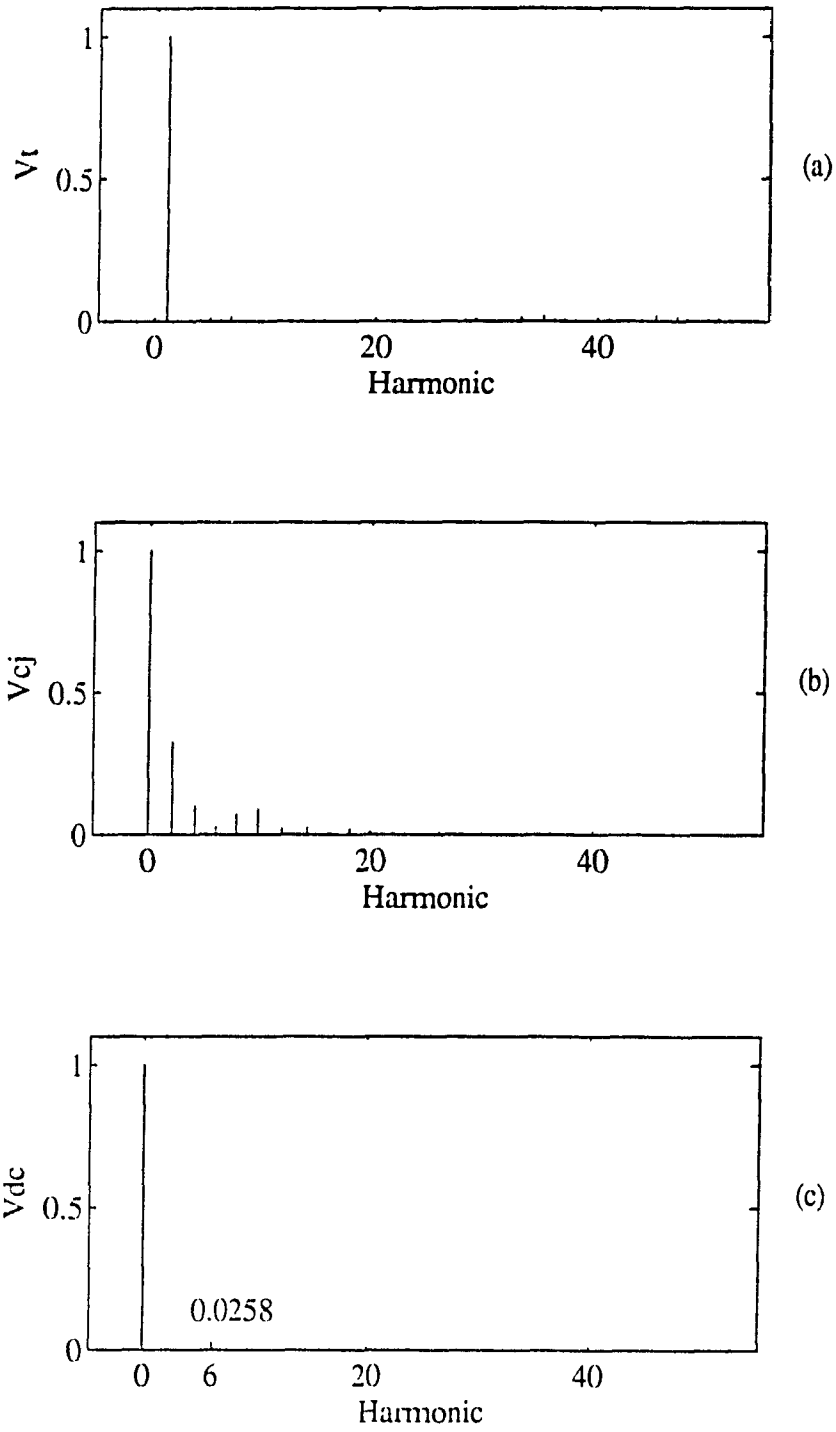

Fig.3-10 Harmonic Spectrum
(a) Transformer terminal voltage
(b) jth module - dc voltage
(c) total dc voltage
K_c / K_m = 5, X_c = 10 p.u.

3-4 PARAMETRIC STUDIES

The cost of the converter system of Fig.3-1 will be determined by the size and the ratings of the components: the capacitive reactance Xc, the inductive reactance X_2, the GTOs, the diodes and the transformers. As the manufacturers have the cost estimates for the different items, it is felt that a useful purpose is served by gathering data of the necessary sizes and ratings from simulation runs.

Fig.3-11 shows the dependence of the *THD* of the ac voltage Vt on X_2, for K_c/K_m=4, 5 and Xc=1, 10 p.u. To meet the 5% limit, X_2 can be as low as 0.175 p.u. for Xc=1.0 p.u. On the other hand X_2 has to be in the 0.225 p.u. range when Xc = 10 p.u. Part of X_2 comes from the leakage reactance of transformer secondaries.

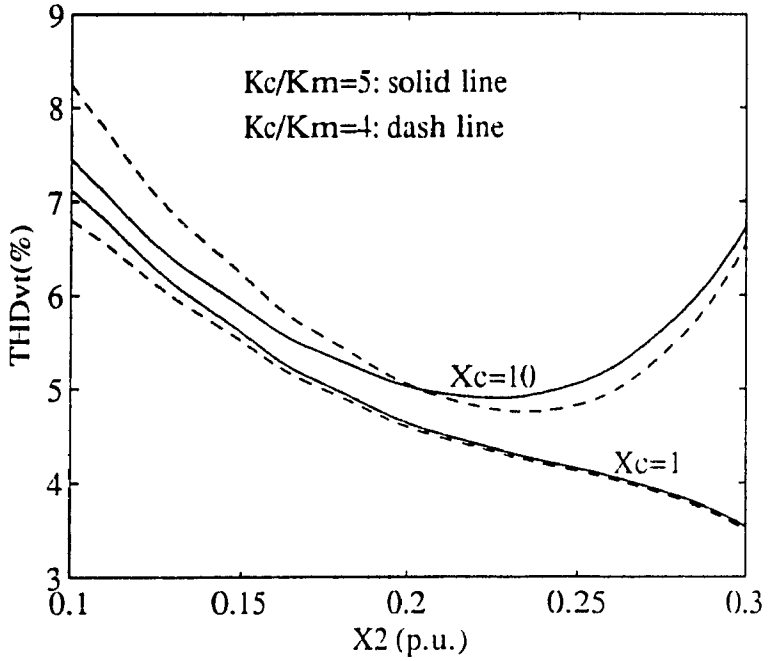

Fig.3-11 Dependence of Transformer Voltage THD on X_2, X_c and K_c/K_m

Fig.3-12 and 3-13 show the rms current ratings of the GTOs and the antiparallel diodes as functions of X_2 for K_c/K_m=4, 5 respectively. The base current is the rated current of one of the N_m=8 converters. In the simulations from which the data of Fig.3-12 and 3-13 have been extracted, the system of Fig.3-1 has been operated as a rectifier delivering 1 p.u. power. Under rectifier operating condition, the diode rms current tends to be larger than the GTO current.

One phase of the 3 transformers is illustrated in Fig.3-14. Since the terminal voltage Vt is already of high quality as shown in Fig.3-6(a) and 3-9(a), the magnetic flux in the core (which is a time integral of the voltage) is of a higher quality sinusoidal waveform still. Since most the low order harmonic cancellations occur in the summation of secondary currents, the *mmf* contains the fundamental harmonic and negligible residual harmonics.

The transformer cost increases with the number of bushings needed for the $2N_m$ secondary terminals. In addition, each secondary winding has a V_{dc}/N_m dc voltage difference from its immediate neighbour. The insulation must be co-ordinated with these dc voltage differences in mind.

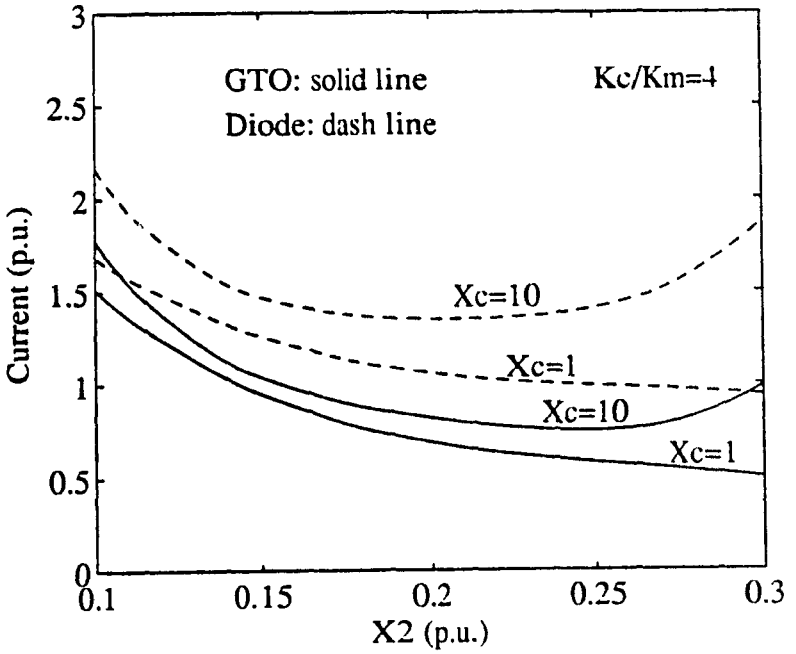

Fig.3-12 Dependence of RMS current of GTO and Diode on X_2 and X_c, $K_c/K_m = 4$

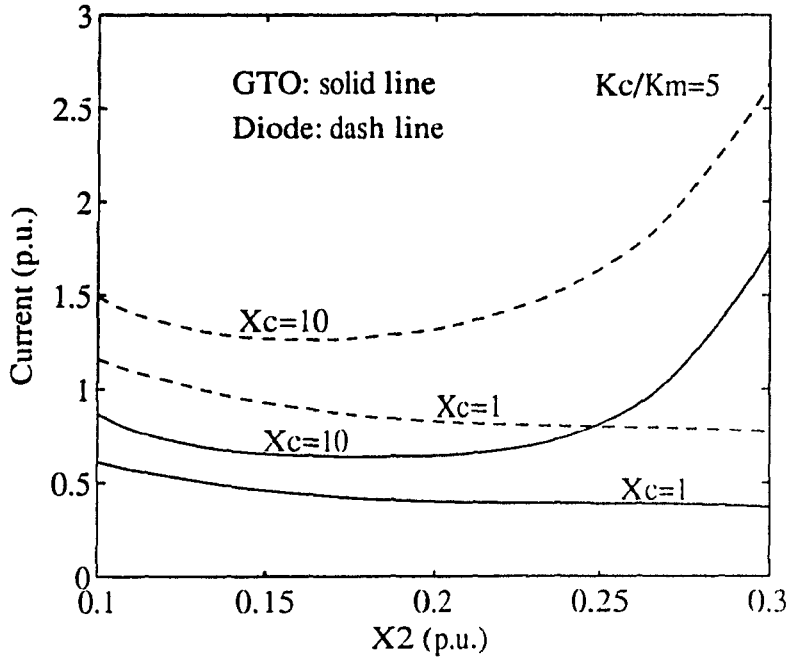

Fig.3-13 Dependence of RMS current of GTO and Diode on X_2 and X_c, $K_c/K_m = 5$

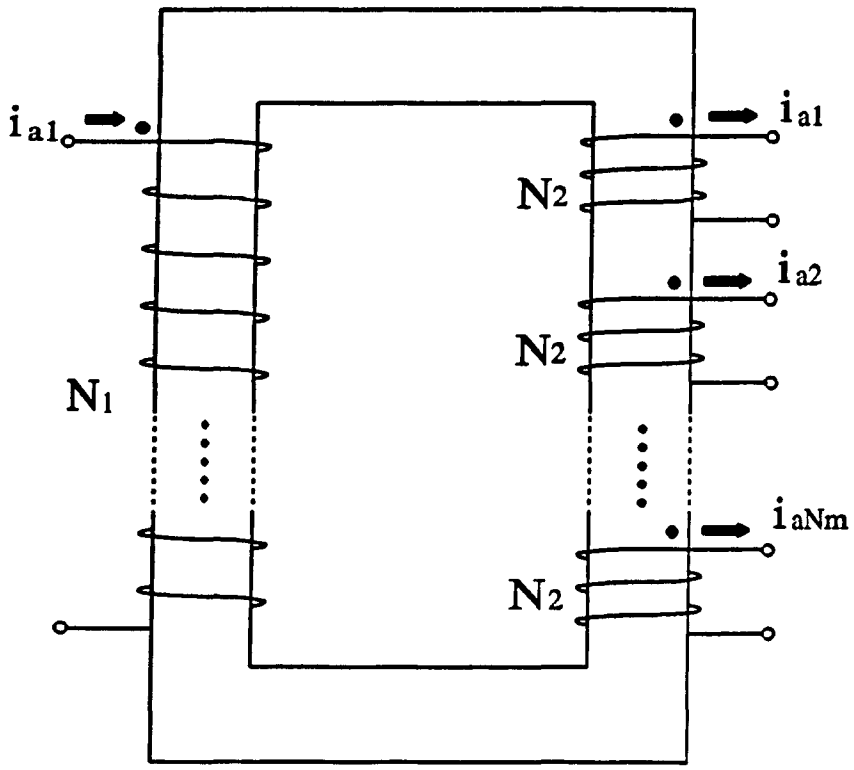

Fig.3-14 Multi-secondary winding transformer

3-5 BROAD FREQUENCY BANDWIDTH OF LINEAR AMPLIFICATION

It has already been established that the SPWM controlled bridge converter functions as 3 linear amplifiers, one for each phase, provided the bandwidth of the modulating signals $S_{maj}(t)$, $S_{mbj}(t)$, $S_{mcj}(t)$ are less than $N_m K_c /3$ [23 - 25]. In the proof of the frequency bandwidth being $N_m K_c /3$ [25], the tacit assumption used is the constant and equal capacitor voltage assumption of eq.(3-7).

Since the mathematical basis for Method II - the Symmetrical Phase Shifting Method has yet to be developed, it is necessary to use simulation runs to find out if the linear gain for the case of $Xc = 10.0$ p.u. has a broad frequency bandwidth also. A contrived situation was simulated based on adding a 5th harmonic to the 60Hz fundamental frequency of e_a to the system of Fig.3-1. Fig.3-15 shows the voltage waveform of the source voltage e_a and the line current i_a. The modulating waveform S_{maj} consists of the 60Hz fundamental frequency only. The carrier frequency is $K_c = 300$Hz. The current waveform in Fig.3-15 contains the fundamental and the 5th harmonic current components.

The same simulation was repeated and the results appear in Fig.3-16. In addition to the 60Hz fundamental frequency in the modulating waveform S_{maj}, a fifth harmonic component was added and adjusted until the line current i_a contains the fundamental frequency only. This simulation experiment shows that the fifth harmonic signal has been amplified as a harmonic voltage in Vt which has been equal

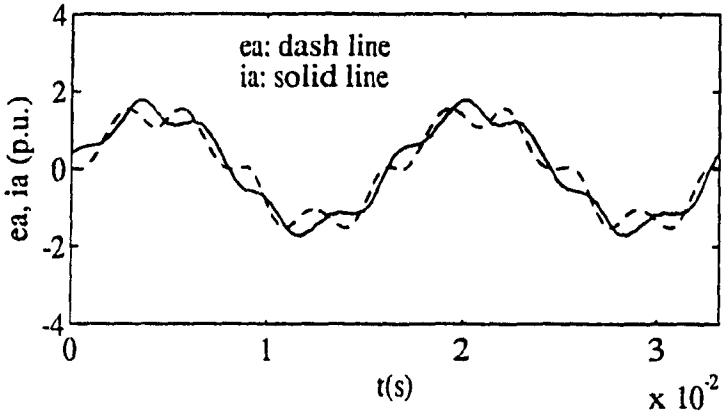

Fig.3-15 5th harmonic added to source voltage e_a. Current i_a contains 5th harmonic

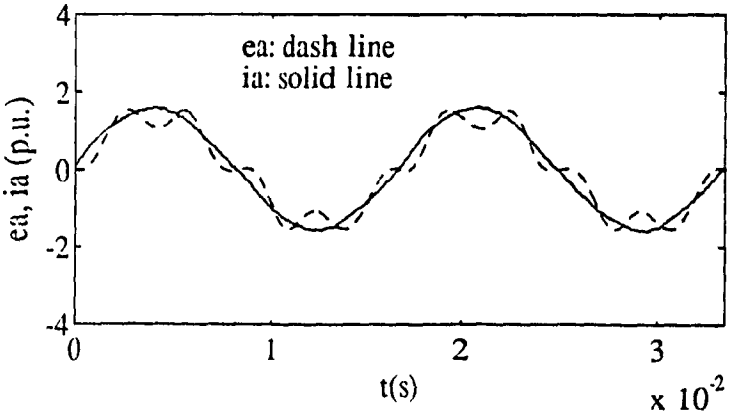

Fig.3-16 5th harmonic in i_a cancelled by 5th harmonic voltage in converter

to and in phase with the fifth harmonic voltage in e_a so that no 5th harmonic current can flow. This simulation run has demonstrated that for $Xc=10$ p.u., where V_{cj} is not constant, linear amplification extends at least to $5\times60=300$Hz. The equivalent carrier frequency is $N_m K_c = 8\times300 = 2400$Hz and the bandwidth of 800Hz is assured from the existing theory [25] for Method I.

3-6 SWITCHING FREQUENCY

In the interest of minimizing the switching losses, the K_c/K_m ratio must be kept at low values. As explained in Ref.[24, 25], certain low values cannot be used because the lower sideband harmonics can appear as dc voltages, or as the modulating frequency voltages, on the ac terminals. The dominant lower sideband harmonic has its frequency at $K_c - 2K_m$ [25].

$K_c/K_m=2$ Since $(K_c - 2K_m)=0$, the individual converter modules have large dc voltage components. Since the circuit resistances are low, the resultant very large dc currents make the ratio of 2 unusable.

$K_c/K_m=3$ The dominant sideband harmonic has the same frequency as the modulating signal. As the amplified signal and the dominant sideband are at the same frequency their voltages add as phasors. Because of the phase shifting of the sidebands, the resultant ac voltages are different for the individual modules. In

consequence, the amounts of power transferred to the dc side are different and the capacitors in the different converter modules are charged to different dc voltage levels. It has been found that by using local negative feedback to phase shift the modulating signal in the individual converter module, the dc link voltages can be equalized. However, because the modulating signals are no longer all equal (because of the phase shift from the feedback error), the cancellation in eq.(3-9-b) is not perfect. In consequence the *THD* is slightly poorer than for $K_c / K_m = 4, 5$.

This ratio has promise but requires in depth study as the local feedback loop may interfere with the outer feedback loops.

$K_c/K_m=4$ This ratio yields dc offset currents of different magnitudes in the different converter modules. The dc voltages have their origins from a relatively small lower sideband harmonic at $(K_c - 4K_m)$. Because the dc offset currents differ in the $N_m = 8$ converter modules, the rms current ratings for the GTOs and diodes in Fig.3-12 are taken from the worst case.

As the dc current components flow through the secondaries of the transformers as shown in Fig.3-14 and as they are self-cancelling by virtue of eq.(9-b), there is no dc component in the *mmf*. Thus, there is no fear of transformer core dc saturation.

It has also been shown that the dc currents in the individual phases of each converter module can be nulled using local current feedback.

$K_c/K_m = 5$ is found to be straight-forward.

CHAPTER IV

CONCLUSIONS

Multi-converter phase-shifting using the Sinusoidal Pulse Width Modulation (SPWM) technique at low frequency switching rates has been studied. In addition it is shown that in spite of the slow switching rate of the GTOs, the information carrying capacity is not impaired. The effective carrier frequency is $N_m K_c$ so that a sufficiently broad band information channel can be made available for control purposes.

Chapter II has shown that no difficulties have been encountered in the parallel connection.

In Chapter III, the data gathered from the digital simulations of 8 series-connected, voltage-source type converter modules, show that the low voltage *THD* requirement of 5% can be achieved with not unreasonable size components.

Further increase in the number of series/parallel connected converter modules in order to meet higher dc voltage and current ratings should also enable it to meet the higher voltage *THD* requirement of 1%.

In the series and parallel connection, this is assured in Method I ($Xc = 1.0$ p.u.) because the harmonic cancellation principle [25] assures that the equivalent carrier frequency is $N_m K_c$.

However, for the series connection, further research is required to find out whether this is applicable to the more economical Method II ($Xc = 10.0$ p.u.). The

disturbing note is seen in Fig.3-10(b) and (c) where the 6th harmonic in the dc voltage is additive.

APPENDIX A

SYSTEM PARAMETERS FOR SIMULATIONS IN CHAPTER II

$AC\ Voltage = 1.0\ p.u.$

$R_1 = 0.1\ p.u.$

$X_1 = 0.2\ p.u.$

$R_2 = 0.01\ p.u.$

APPENDIX B

SYSTEM PARAMETERS FOR SIMULATIONS IN CHAPTER III

$AC\ Voltage = 1.0\ p.u.$

$R_1 = 0.03\ p.u.$

$X_1 = 0.1\ p.u.$

$R_2 = 0.03\ p.u.$

APPENDIX C

SYSTEM:

V_{base}, I_{base}

$Z_{base} = V_{base} / I_{base}$

n - secondary /primary turns ratio

P.U. BASE OF EACH CONVERTER MODULES

$$V'_{base} = nV_{base}$$

$$I'_{base} = I_{base} / (nN_m)$$

$$Z'_{base} = n^2 N_m Z_{base}$$

REFERENCE

[1] A.M. Gole and R.W. Menzies, "Analysis of Certain Aspects of Force Commutated HDVC Inverters", IEEE Trans. Vol. PAS-100, No. 5, May 1981, pp. 2258-2262.

[2] H.M. Turani, R.W. Menzies and D.A. Woodford, "Feasibility of DC Transmission with Forced Commutation to Remote Loads", IEEE Trans. PAS-103, June 1984, pp. 1256-1262.

[3] B.T. Ooi, "Pulse Width Modulation Power Transmission", U.S. Patent 4,941,079 July 10, 1990.

[4] B.T. Ooi and X. Wang, "Voltage Angle Lock Loop Control of Boost Type PWM Converter for HDVC Application", IEEE Transactions on Power Electronics, Vol. 5, No. 2, April 1990, pp. 229-235.

[5] X. Wang and B.T.Ooi, "High Voltage Direct Current Transmission System Based on Voltage Source Converters", Record of the 21st Annual Institute of Electrical and Electronics Engineers/Power Electronics Specialists Conference 1990, San Antonio, Texas.

[6] B.T. Ooi, X. Wang and J.W. Dixion, "Voltage Source Type HVDC Transmission System", Proceedings of 1990 International Power Electronics Conference, Tokyo, pp. 1251-1257.

[7] Y. Sun and R.W. Menzies, "Harmonic Control and Losses of a Current Source GTO Inverter Supplying Load Without AC Generation", IEEE Transactions

on Power Delivery, Vol.6 No.1, January 1991, pp. 208-215.

[8] B.T. Ooi and X. Wang, "Boost Type PWM HVDC Transmission System", IEEE/PES 1991 Winter Meeting New York. Paper No. 91WM 119-8'PWRD.

[9] Y. Sumi, Y. Harumoto, T. Hasegawa, M. Yano, K. Ikeda and T. Matsura, "New Static VAR Control Using Force-Commutated Inverters", IEEE Trans., Vol. PAS-100, No. 9, September 1981, pp. 4216-4223.

[10] T. Hasegawa, T. Betsui, M. Takeda, Y. Hosokáwa, S. Murakami, F. Ishiguro and T. Khoan, "Development of GTO-SVG for Improving Power System Stability", Proceedings of 1990 International Power Electronics Conference, Tokyo, pp. 1031-1037.

[11] L. Morán, P.D. Ziogas and G. Joos, "Analysis and Design of a Three-Phase Current Source Solid-State VAR Compensator", IEEE Trans. Ind. Appl., Vol. IA-25, No.2, March/April 1989, pp. 356-365.

[12] L. Morán, P.D. Ziogas and G. Joos, "Analysis and Design of a Synchronous Solid-State VAR Compensator", IEEE Trans. Ind. Appl., Vol. IA-25, No. 4, July/August 1989, pp. 598-608.

[13] L. Gyugyi, "Solid-State Control of Electric Power in AC Transmission Systems", Paper No. T-IP.4 International Symposium on Electric Energy Converters in Power Systems, Capri, Italy 1989.

[14] B.T. Ooi and S.Z. Dai, "Series-Type Solid-State Static VAR Compensator", Power Electronics Specialists Conference, Boston, 24-27th, June 1991.

[15] B.T. Ooi, S.Z. Dai and X. Wang, "Solid-State Series Capacitive Reactance

Compensators", IEEE Transactions on Power Delivery, Vol.7, No.2, April 1992.

[16] J.W. Dixon and B.T. Ooi, "Series and Parallel Operation of Hysteresis Current Controlled PWM Rectifiers", IEEE Transactions on Industry Applications, Vol.25 No.4, July/August 1988, pp. 644-651.

[17] J.W. Dixon and B.T. Ooi, "Dynamically Stabilized Current Controlled SPWM Boost Type Three-Phase Rectifier", IEEE Industry Application Society Annual Meeting Conference Record, October 1988, Pittsburgh.

[18] S. Hirose, N. Seki, O. Higa, Y. Miguchi, K. Takahashi nd T. Shibata, "Multi-Microcomputer-based Controller for 12 MW GTO Power Conditioning Systems", IEEE Power Electronic Specialists Conference Record 1988, pp. 611-618.

[19] N. Mohan, T.M. Undeland, W.P. Robbins, "Power Electronics", John Wiley 1989.

[20] S.R. Bowes, "Novel Approach to the Analysis and Synthesis of Modulation Processes in Power Converters", Proceeding IEEE (London), Vol.122 No.5, May 1975, pp. 507-513.

[21] B.T. Ooi, S-Z. Dai and F.D. Galiana, "A Solid-State PWM Phase Shifter", IEEE/PES 1992 Winter Meeting, New York, January 1992, 92WM 260-0 PWRD.

[22] R.H. Lasseter and S.G. Jalai, "Power Conditioning Systems for Superconductive Magnetic Energy Storage", IEEE Transactions on Energy

Conversion, Vol.6, No.3, 1991, pp.381-397.

[23] Z-C. Zhang and B.T. Ooi, "Multi-Modular Current-Source SPWM Converter for Superconducting Magnetic Energy Storage System", Power Electronics Specialists Conference, Toledo, Spain, 1992.

[24] Z-C. Zhang, J.B. Kuang, X. Wang, B.T. Ooi, "Force Commutated HVDC and SVC based on Phased-Shifted Multi-Converter Modules", IEEE, PES 1992 Winter Meeting, New York, New York, January 1992, 92WM 290-7 PWRD.

[25] B.T. Ooi and Z-C. Zhang, "Gain-Bandwidth of SPWM Converter as Linear Amplifier", submitted to Institute of Electric Engineers, (London), Proceedings B.