NOTE TO USERS

An Ultra Low-Power 5Gbps Vertical-Cavity Surface-Emitting Laser-Based Optical Transmitter for Optical Interconnect Applications and Access Networks

Jean-Philippe Thibodeau

Department of Electrical and Computer Engineering
McGill University
Montréal, Québec, Canada
August 2005

A thesis submitted to McGill University in partial fulfillment of the requirements of the degree of Master of Engineering

Your file Votre référence
ISBN: 978-0-494-22674-2
Our file Notre référence
ISBN: 978-0-494-22674-2

ABSTRACT

The bandwidth bottleneck present in the access level of optical networks stimulated research, leading to novel topologies, including passive optical networks. In parallel, the increasing processing power of digital systems led to a similar bottleneck in chip-to-chip and board-to-board communications. Guided-wave optical interconnection on printed-circuit boards is viewed as a potential solution.

This thesis outlines the design, implementation, and testing of a vertical-cavity surface-emitting laser (VCSEL)-based optical transmitter in 0.18μm CMOS usable for both applications. Optical transmitter architectures are reviewed and a suitable topology is proposed. The implementation includes an original dual power-rail layout for reduced power consumption. A detailed bias-dependent VCSEL model is developed from experimental data.

Experimental results presented in this thesis are in good agreement with simulations. An errorless data rate of 3.125Gbps is achieved for a total power consumption of 18.35mW, at an average optical output power of 2mW. An error-corrected channel using the proposed optical transmitter can operate at 5Gbps.

RÉSUMÉ

L'effet d'entonnoir créé par la bande passante limitée au niveau de l'accès des réseaux optiques stimula la recherche, résultant en de nouvelles topologies dont les réseaux optiques passifs. Parallèlement, l'augmentation de la capacité de traitement des systèmes numériques créa un effet similaire au niveau des communications puce à puce et carte à carte. Les interconnexions optiques à ondes guidées sur cartes de circuit imprimé représentent une solution potentielle.

Cette thèse décrit la conception, la réalisation et l'évaluation d'un transmetteur optique en CMOS 0.18μm combiné à un VCSEL (vertical-cavity surface-emitting laser). Ce transmetteur peut être utilisé pour les deux applications citées ci haut. Une revue des différentes architectures de transmetteurs optiques est conduite. Une topologie de transmetteur appropriée est sélectionnée. La réalisation inclut une distribution de puissance à deux rails novatrice. Le développement d'un modèle de VCSEL dépendant de la polarisation est détaillé.

Les résultats expérimentaux présentés sont en accord avec les simulations. Un débit sans erreur de 3.125Gbps est atteint à une consommation de puissance de 18.35mW, pour une émission de puissance optique moyenne de 2mW. Un canal avec correction d'erreur peut opérer à 5Gbps.

ACKNOLEDGEMENTS/REMERCIEMENTS

This research was supported partially by the National Science and Engineering Research Council (NSERC) and industrial partners, through the Agile All-Photonic Networks (AAPN) research network. It was also supported by the Canadian Microelectronics Corporation (CMC), through CMOS die fabrication, and by Emcore Corporation Inc. which supplied the vertical-cavity surface-emitting laser dies. Financial support was also received from NSERC through post-graduate studies research scholarships.

My sincere thanks are given to numerous people who helped me, directly or not, to enjoy the last two years at the masters level and achieve exciting outcomes. First and most importantly, I would like to thank my research supervisor, Professor David Plant, for his great support. In my sense, Professor Plant is the ideal supervisor, leaving a great deal of autonomy while contributing with his tremendous research experience at key moments. The research environment he has created really made the completion of this degree a fascinating and rewarding experience.

In addition, several individuals helped me greatly in various stages of this project. Especially, I would like to thank my second mentor, Julien Faucher, for the numerous discussions we had on various aspects of theory, design or testing. I probably would not be the same researcher without his help. I also thank him for his help in reviewing this thesis and for giving me the figure on PONs in chapter 1.

I would also like to thank Eric Bisaillon and Madelaine Mony for their help in setting up optical systems in the laboratory. This was a real challenge to me and they helped mitigate the various issues related to those capricious systems. Thanks to Bob Thompson of the department's electrical workshop for teaching me numerous soldering tips, and for soldering some packages. I also thank Charlie Wang and Chris Murray at Emcore for supplying high quality VCSEL dies in a swift manner. Administrative issues could have been painful without the help of Chris Rolston and Kay Johnson. They were

always extremely responsive to various administration requests I had over the years, they're McGill's best!

I met a number of people during my years who have become personal friends. J'aimerais remercier tout spécialement les membres du ghetto francophone du PSG, Rhys Adams, Michäel Ménard, Cristina Marinescu, Julien Faucher, Éric Bisaillon et Madelaine Mony. Le bon temps que nous avons passé ensemble est à jamais gravé dans ma mémoire. Grâce à vous, j'ai pu apprécier mon séjour à McGill au maximum. I also had great moments with several others, including Alan Li, Reuven Gordon, Ehab Shoukry, and Chris Rolston. Keep it up guys, you're great!

Je désire remercier mes parents, Michel et Danielle, pour l'éducation qu'ils m'ont donné, leur support inconditionnel et leur amitié. Ils ont su éveiller et moi le goût du savoir et la curiosité qui ont faits de moi un chercheur heureux et un individu épanoui. Ils m'ont donnés sans compter, j'espère un jour pouvoir leur rendre.

Finalement, je remercie mon amour Amélie, contre son gré. Même si elle croit qu'elle n'a rien à faire dans une thèse de maîtrise, c'est en partie grâce à elle que tout ceci fut écrit. Son amour et sa joie de vivre sont pour moi une motivation constante à me dépasser, à nourrir des projets toujours plus grands et intéressants.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 Introduction

1.1 Background and Motivation

1.1.1 Optical Interconnections and Access Networks

For countless centuries, human beings have sought novel processes for communicating information with more efficiency. The need for sharing ideas and acquiring knowledge has led to pivotal inventions such as writing, telegraphy and telephony. More recently, developments including computers and the internet have drastically changed the portrait of communications. Millions of individuals now have access to up-to-date information from around the world in a few seconds. Corporations share billions of bits of information between their offices quickly and securely.

The numerous user applications and growing interest for the internet have generated an unprecedented growth in the bandwidth requirements of communications networks [1]. In particular, internet traffic has approximately doubled every year during the 1990's and early 2000's [2]. The bandwidth bottlenecks present in already deployed metropolitan and long-haul networks led to intense research and development efforts in long-reach optical interconnection technologies and network architectures. As a result, a very mature technology for long distance communications, including low-loss single-mode optical fibre, optical amplifiers and wavelength division multiplexing, emerged and was deployed during the last decade of the twentieth century [3].

The bandwidth of these state-of-the art networks soon exceeded the traffic demand growth. In addition, the apparition of a new bottleneck at the access network level prevented increases in traffic growth [2]. The late realisation of this issue led to the technological industry downturn shortly after the beginning of the new millennium. Since then, researchers have been directing more efforts into developing new access network architectures. In particular, passive optical networks (PON) show great promise

in solving the access bottleneck at low costs [4]. A simplified architectural view of a PON is shown in Figure 1.1 (OLT=optical line terminal, PS/PC=power splitter/combiner, CO=central office, ONT=optical network terminal). On the other hand, enabling technologies for next-generation access networks are still immature. Especially, transceivers topologies for such networks need to be investigated.

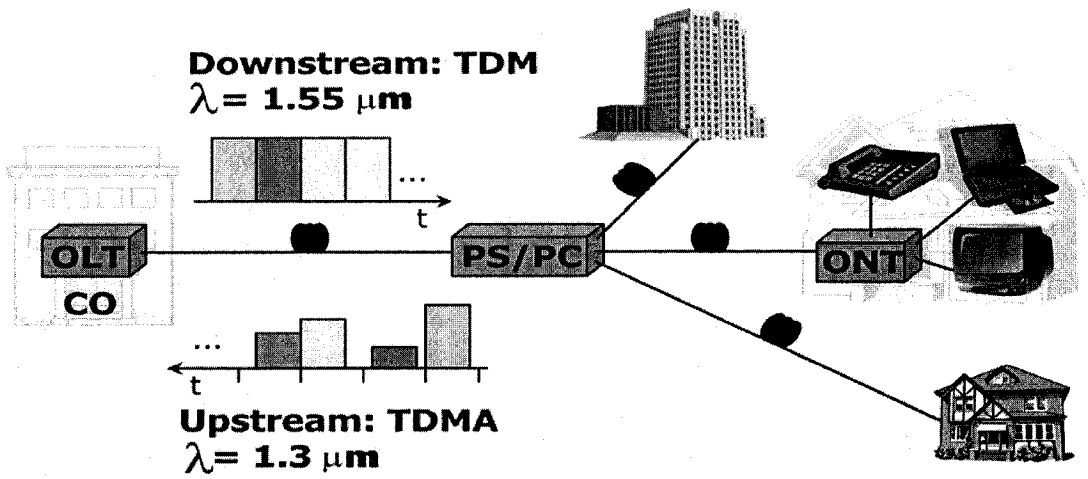


Figure 1.1: Simplified architectural view of a passive optical network.

1.1.2 Short-reach Optical Interconnects

In parallel, the processing power of digital systems has exponentially grown in the past four decades, directly related to the reduction of feature sizes on silicon integrated circuits (ICs), according to Moore's law [6]. On the other hand, the performance of electrical interconnections between or even inside electronic chips cannot keep up with this evolution. The International Technology Roadmap for Semiconductors (ITRS) predicts that the industry will run out of material solutions for some sectors of electrical interconnections by 2007 [7]. This issue commonly referred to as the "Red Brick Wall" problem, as illustrated in Table 1.1, will force researchers to come up with replacement interconnection technologies for both intra-chip and chip-to-chip communications [7]. The dark grey areas highlight sectors where manufacturable solutions are not currently

known, while the light grey areas show sectors where solutions are known but not yet implemented in a production context.

Year of Production	**2006**	**2007**	**2008**	**2009**	**2010**	**2012**
Total interconnect length (m/cm^2), excluding global levels	1002	1117	1401	1559	1784	2214
Jmax (A/cm^2) (at 105°C)	7.8E5	1.0E6	1.4E6	2.5E6	3.0E6	3.7E6
Interconnect RC delay (ps) for 1mm global line at minimum pitch	87	92	112	139	143	220
Interlevel metal insulator - bulk dielectric constant (κ)	<2.7	<2.4	<2.4	<2.4	<2.1	<2.1
Power density ($Watts/mm^2$) - cost-performance packages	0.7	0.74	0.79	0.83	0.85	0.89
Off-chip bus data rate (Mbits/s)	4800	6400	7500	8600	9600	12800

Table 1.1: Excerpt of ITRS technology requirement predictions [7].

Already, short-reach optical interconnects (OI) have been identified as a promising candidate solution [8]. The physical advantages of OI are numerous and have been thoroughly investigated [10]. In recent years, OI demonstrators have focused on exploiting the technology's suitability for parallelism. Systems with hundreds to thousands of optical channels operating at medium speeds linking two silicon chips have been implemented [11]. Although such systems present huge bandwidth potential, the free-space nature of their optical links, high power consumption and size make them unpractical and unreliable for near future applications.

The implementation of OI with a limited number of channels, operating at very high data rates, and the use of optical waveguides on printed-circuit boards (PCB) constitutes an appealing alternative to such huge systems [15]. It has been validated recently that the bandwidth of a single OI will exceed that of an electrical interconnect longer than 10 cm around the year 2010 technology node [17]. This motivates the development of high-speed and low-power transceivers for waveguide-based board-to-board and chip-to-chip OI.

1.2 Scope of the Thesis

We have highlighted the need for novel transceiver designs, applicable for both access networks and short-reach OI, in the previous section. Traditionally, researchers dedicate more efforts at the receiving end of the link. The complexity and stringent performance requirements of receivers justify this unbalance [18]. On the other hand, as data rates increase and other issues such as cost efficiency and power conservation come into consideration, the design complexity of optical transmitters becomes apparent. In particular, design and modeling approaches, layout techniques and testing apparatus specifically oriented at optical transmitters must be devised.

This thesis reports the design, simulation, modeling, layout and testing of an optical transmitter applicable in both access networks and short-reach OI contexts. The transmitter is based on a 0.18μm complementary metal-oxide-semiconductor (CMOS) driver chip combined with an 850nm vertical-cavity surface-emitting laser (VCSEL). In order to achieve high versatility in our design, issues such as data rate, power consumption, nature of the data, suitability for parallelism, integration, layout area, cost, and yield have been considered. The multiple design decisions related to those issues will be highlighted throughout the thesis. Complete discussions on the modeling of the VCSEL and testing of the packaged optical transmitter will also be included.

In addition, we will propose new architectures where our optical transmitter could be used efficiently. This includes applications such as PON or the testing of future optical packet-based networks, such as the Agile All-Photonic Network [19].

1.3 Thesis Organisation

The various subjects covered by this thesis are organised as follows. Chapter 2 includes an in-depth literature review of optical transmitters. The design issues particular to optical transmitters are given and general characteristics of such systems are exposed. Existing optical transmitter topologies are divided into three categories, and are analysed

based on the characteristics given in the first section. In particular, transmission line drivers, edge-emitting laser drivers, and, with greater focus, VCSEL drivers will be considered.

In chapter 3, the design of a versatile three-stage VCSEL driver in 0.18um CMOS technology is outlined. We enumerate preliminary design choices which represent one of the main focuses of the project. The design of the pre-amplifier, pulse-shaping and current-steering stages is covered in detail. In addition, a unity-gain frequency (f_T) analysis of the technology used for this project, leading to a best-performance circuit biasing, is given.

Chapter 4 focuses on the layout, extraction and simulation of the VCSEL driver. This includes discussions on layout techniques for minimizing substrate and power-rails switching noise. We also introduce a double power-supply rail layout for power consumption reduction. Also, an extensive discussion on the modeling of the VCSEL, test fixture and package is given. This leads to accurate simulation results, which are exposed in the last section of this chapter.

The fixturing, packaging and testing of the CMOS-VCSEL based optical transmitter is covered in details in chapter 5. A test plan and test algorithm is outlined [20]. Details on the packaging and wire-bonding of the CMOS and VCSEL dies in a ceramic package are given. The options for inputting the electrical signals are given. In particular, through-printed-circuit-board or direct-probing options are investigated. In addition, the testing setup is described through its multiple transformations. A free-space optical relay and a multimode fibre-based setup are covered. Experimental results are given throughout the chapter to illustrate the evolution of our testing apparatus. Final experimental results, compared to simulation predictions, conclude this chapter.

In chapter 6, architectures where our versatile optical transmitter could be used efficiently are highlighted. A topology suitable for access networks is covered at a high-level perspective. In addition, we illustrate how our driver could be used to test switches or other devices to be incorporated in future packet-based optical networks. Finally, a

brief conclusion is given in chapter 7. We summarise the thesis contents and suggest future research directions.

1.4 Research Contributions

This master's thesis project has led to several significant contributions to the research community. These are enumerated in the following list.

- Lowest reported power consumption for a CMOS 0.18μm based current-steering VCSEL driver, at 18.35mW. This is due in part to a novel dual-power-ring layout topology which reduces power consumption by restricting the use of a high power supply voltage to the VCSEL.

- A rigorous procedure for deriving a bias-dependent electrical model for VCSEL based on experimental data of reflection parameter and voltage versus current curves.

- State-of-the-art packaging and testing of the CMOS driver and VCSEL combination in a ceramic quad-flat package with CMOS bond pads of 40μm on the side using 1mil gold bonding wire.

- The assembly of a versatile and reliable optical transmitter test setup by butt-coupling VCSEL-emitted light into a multimode-mode fibre with simple alignment equipment.

1.5 References

[1] Leon-Garcia, and I. Widjaja, *Communication Network.* Boston, MA: McGraw-Hill, Inc., 2000.

[2] A. M. Odlyzko, "Internet traffic growth: Sources and implications," *in Proc. SPIE Int. Soc. Opt. Eng.,* September 8-11, 2003, Orlando, pp. 1-15.

[3] G. Keiser, *Optical Fiber Communications.* 3rd ed., Boston, MA: McGraw-Hill, Inc., 2000.

[4] G. Kramer, and G. Pesavento, "Ethernet passive optical network (EPON): Building a next-generation optical access network," *IEEE Commun. Mag.,* vol. 40, pp. 66-73, February 2002.

[5] P. Ossieur, X. Z. Qiu, J. Bauwelinck, D. Verhulst, Y. Martens, J. Vandewege, and B. Stubbe, "An overview of passive optical networks," *in Proc. Int. Symp. on Signals, Circuits and Systems,* July 10-11, 2003, vol. 1, pp. 113-116.

[6] G. E. Moore, "Cramming more components onto integrated circuits," *Proc. IEEE,* vol. 86, pp. 82-85, January 1998.

[7] Semiconductor Industry Association. (2003, December). The International Technology Roadmap for Semiconductors, 2003 Edition. [Online]. Available: http://public.itrs.net/Files/2003ITRS/Home2003.htm

[8] D. A. B. Miller, "Rationale and challenges for optical interconnects to electronic chips," *Proc. IEEE,* vol. 88, pp. 728-749, June 2000.

[9] D. V. Plant, and A. G. Kirk, "Optical interconnects at the chip and board level: Challenges and solutions," *Proc. IEEE,* vol. 88, pp. 806-818, June 2000.

[10] D. A. B. Miller, "Physical reasons for optical interconnection," *Int. J. Optoelectronics,* vol. 11, pp.155-168, May-June 1997.

[11] D. V. Plant, M. B. Venditti, E. Laprise, J. Faucher, K. Razavi, M. Châteauneuf, A. G. Kirk, and J. S. Ahearn, "256-channel bidirectional optical interconnect using VCSELs and photodiodes on CMOS," *J. Lightwave Technol.,* vol. 19, pp. 1093-1103, August 2001.

[12] M. B. Venditti, E. Laprise, J. Faucher, P.-O. Laprise, J. E. A. Lugo, and D. V. Plant, "Design and test of an optoelectronic-VLSI chip with 540-element receiver-transmitter arrays using differential optical signaling," *IEEE J. Select. Topics Quantum Electron.,* vol. 9, pp. 361-379, March-April 2003.

[13] A. L. Lentine, K. W. Goosen, J. A. Walker, L. M. F. Chirovsky, L. A. D'Asaro, S. P. Hui, B. J. Tseng, R. E. Leibenguth, J. E. Cunningham, W. Y. Jan, J.-M. Kuo, D. W. Dahringer, D. P. Kossives, D. D. Bacon, G. Livescu, R. L. Morrisson, R. A. Novotny, and D. B. Buchholz, "High-speed optoelectronic VLSI chip with >4000 optical I/O based on flip-chip bonding of MQW modulators and detectors to silicon CMOS," *IEEE J. Select. Topics Quantum Electron.,* vol. 2, pp. 77-84, April 1996.

[14] M. B. Venditti, "Receiver, transmitter, and ASIC design for optoelectronic-VLSI applications," *Ph.D. Dissertation,* McGill University, Montreal, QC, Canada, 2003.

[15] C. Berger, R. Beyeler, G.-L. Bona, R. Dangel, L. Dellmann, P. Dill, F. Horst, M. A. Kossel, C. Menolfi, T. Morf, B. Offrein, M. L. Schmatz, T. Toifl, and J. Weiss, "Optical links for printed circuit boards," *in Proc. 16th Annual Meeting of the IEEE LEOS,* October 27-28, 2003, vol. 1, pp. 61-62.

[16] M. Francke, and F.-P. Schiefelbein, "Optical interconnects on printed circuit board level - Results based on the German funded project OPTICON," *in Proc. Electronic Components and Technology Conf.,* June 1-4, 2004, pp. 1542-1546.

[17] A. Naeemi, J. Xu, A. V. Mule, T. K. Gaylord, J. D. Meindl, "Optical and electrical interconnect partition length based on chip-to-chip bandwidth maximization," *IEEE Photon. Technol. Lett.,* vol. 16, pp. 1221-1223, April 2004.

[18] B. Razavi, "Challenges in portable RF transceiver design," *IEEE Circuits Devices Mag.,* vol. 12, pp. 12-25, September 1996.

[19] D. V. Plant, "Agile all-photonic networks," *in Proc. 16th Annual Meeting of the IEEE LEOS,* October 27-28, 2003, vol. 1, p. 227.

[20] M. Burns, and G. W. Roberts, *An introduction to mixed-signal IC test measurement.* New-York, NY: Oxford University Press, Inc., 2001.

2 Overview of Optical Transmitters

2.1 General Characteristics

Optical transmitters are usually composed of multiple stages, each having very specific functions. In general, all but the last stage serves two purposes, amplification and shaping of the input signal. The design of these stages is not specific to optical transmitters as they are present everywhere in mixed-signal and radio-frequency (RF) circuits. On the other hand, the last stage, commonly called the laser driver, presents design issues and challenges unique to optical transmitters. This chapter focuses on reviewing the various laser driver topologies present in the literature, with less attention given to the other stages. We will first define two classes of laser drivers, namely current- and voltage-drivers. An overview of electrical and optical signaling options will then be given. Finally, we will introduce current-driver topologies and investigate other architectural and high-speed considerations.

2.1.1 Laser Driver Classes

Although a large number of laser driver topologies exist in several technologies, all can be categorized in one of two classes, being current-drive or voltage-drive topologies. Current-drivers are by far the most commonly used in published designs, due to their simplicity of implementation and flexibility. For this class of drivers, the current pushed/pulled in/out of the laser is varied by a driving transistor, and the voltage at the anode/cathode of the laser adjusts itself in consequence. The current level is dictated by a current source. An illustration of this topology is given in Figure 2.1 (a) for a current-pulling driver [1]. For a current-pushing driver, a PMOS transistor would be used and the laser would be located at the bottom (in the drain of the PMOS).

Voltage-drive topologies are much less frequently used, due to their relative complexity. Such a driver is illustrated in Figure 2.1 (b) [1]. For this class, the voltage

applied at the anode/cathode of the laser is varied, resulting in a change in laser current. This usually requires the laser to be located in the source of MOS transistors or in the emitter of bipolar transistors. A resistor must also be present between the transistor and laser or in the drain/collector, in order to insure voltage flexibility at the source/emitter and respect fundamental biasing requirements of the transistor. The complexity of this design results in part from the need to implement a resistor on-chip. In highly integrated silicon technologies, such resistors use a lot of chip area and can be quite capacitive, resulting in lower modulation speeds.

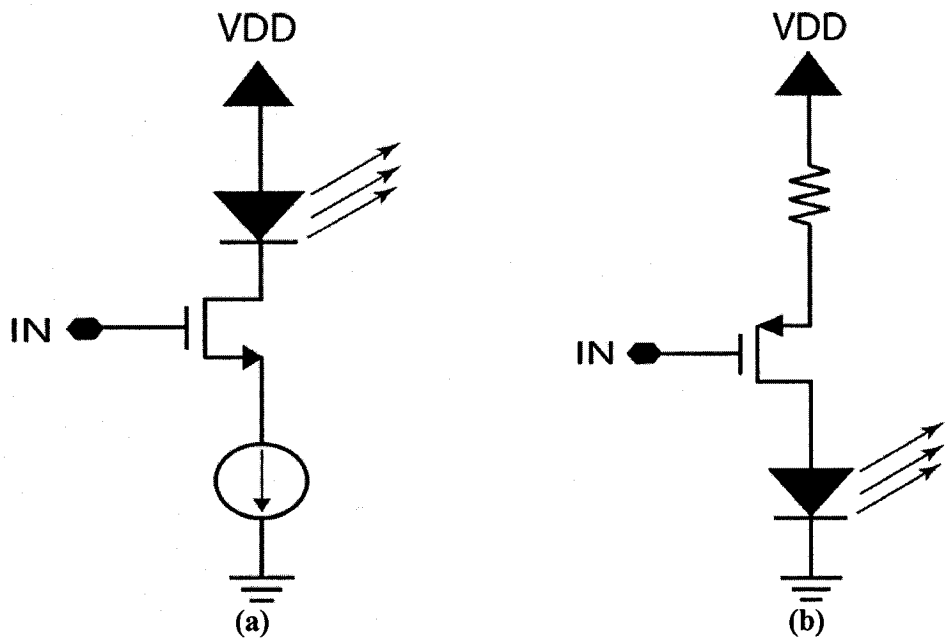


Figure 2.1: Typical current-drive (a) and voltage-drive (b) laser driver topologies.

The difference between current-drive and voltage-drive circuits is subtle. Fundamentally, we must determine if the modulation is initiated by a current or a voltage variation at the laser. More specifically, a variation of the input voltage in figure 1 (a) will modify the drain current of the NMOS transistor (since the source voltage is fixed due to the current source), which will in turn modify the voltage at the cathode of the laser. Alternatively, a variation of the input voltage in figure 1 (b) will modify the anode voltage of the laser, resulting in a change of current. Due to the widespread use and simplicity of current-drivers, we will focus on this topology for the remainder of this section.

2.1.2 Electrical and Optical Signaling Architectures

Laser drivers are by definition electrical-to-optical (E2O) converters, taking an electrical signal at its input and emitting an optical output signal. At both ends of the driver, signaling can be single-ended or differential. For single-ended signaling, the input/output (IO) is restricted to a single channel. Differential signaling uses two IO channels, which are complementary in nature. Laser drivers can use a combination of the two signaling architectures. For example, electrically differential and optically single-ended IO can be implemented.

Both architectures have their own advantages and disadvantages, electrically and optically, such that numerous combinations have been used in actual designs, depending on the application. Electrically differential topologies are more resistant to noise, although they generally consume more power. Optically differential circuits are less subject to switching noise through the use of a current-steering topology, although it is possible to implement single-ended current-steerers, using a dummy load in one branch. This will be exposed in greater details in the next subsection. In order to illustrate possible signaling architectures, two laser driver circuits are given in Figure 2.2. In Figure 2.2 (a), an electrically and optically differential driver is shown [2]. The complementary input signals INP and INN are applied to the inputs of the laser driver, resulting in a complementary operation of the lasers present in each branch of the current-steering driver. In Figure 2.2 (b), an electrically and optically single-ended current-driver is shown [3]. Only one input switches the current into the single laser between the ON and OFF states.

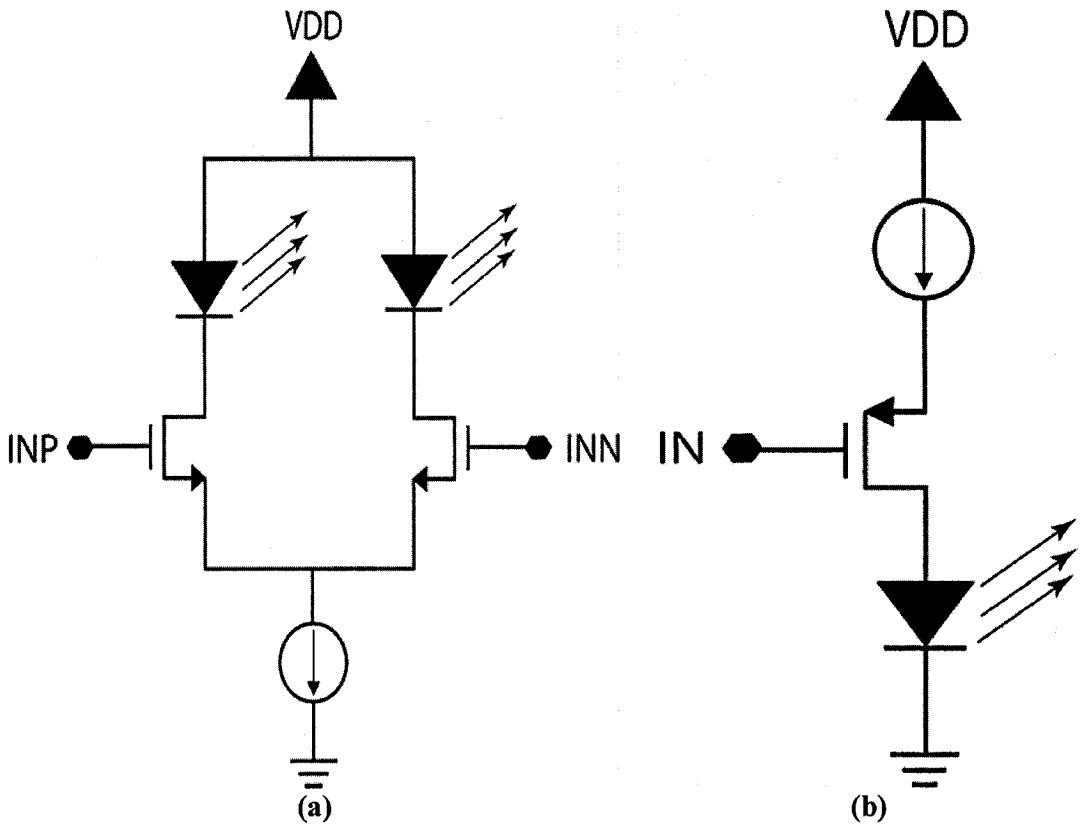


Figure 2.2: Common laser driver signaling architectures: (a) Electrically and optically differential, (b) Electrically and optically single-ended.

2.1.3 Current-Driver Topologies

Most current-drivers are either current-switching or current-steering topologies. Current-steerers are differential in nature, giving them additional noise immunity, in particular to switching noise. This is due to the constant current consumption of such a circuit. The current supplied by a high-impedance current source is steered between the two branches of a differential pair using complementary inputs, as illustrated in Figure 2.3 [4]. The total current flowing in the driver is always equal to IMOD. For an optically differential solution, a laser is placed in each branch of the differential pair. For an optically single-ended version, a laser is placed in one branch and a load emulating the behaviour of the laser is placed in the other branch, as shown in Figure 2.3 [4].

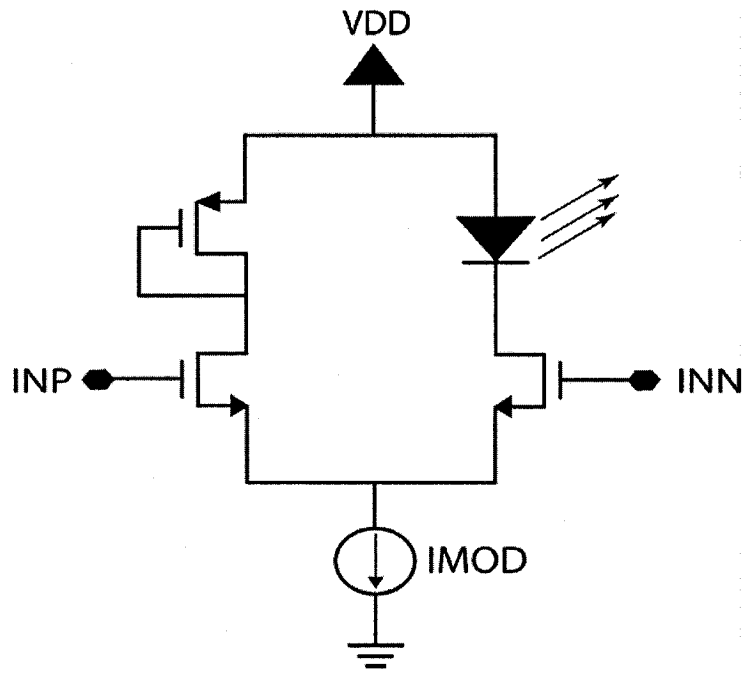


Figure 2.3: Optically single-ended current-steering laser driver.

In comparison, a current-switching driver completely or partially shuts down the modulation current source, resulting in variations in power supply current consumption. This can produce noise on power supply rails, commonly called ground-bounce. This noise can couple to the input and output nodes of the driver through the transistor channels or the substrate, degrading performance. On the other hand, such drivers are quite power efficient, consuming the exact amount of power required by the laser.

2.1.4 Other Considerations

Current drivers can either push current into the laser or pull current from the laser. Although both approaches are as valid from the laser perspective, other considerations introduce significant performance differences between the two methods. A current-pulling driver is shown in Figure 2.1 (a), while a current-pushing driver is included in Figure 2.2 (b). A current-pushing driver uses PMOS or PNP transistors, which are intrinsically slower than their NMOS/NPN opposites, thus establishing a significant performance disadvantage for the current-pushing topology [5]. On the other hand, the laser in the current-pushing topology is connected directly to the ground rail, as opposed

to the power rail for the current-pulling topology. The ground rail is typically of higher quality with respect to noise robustness in most high-speed designs, giving the current-pushing design a slight edge in this area.

As the performance of PMOS/PNP devices continue to get closer to NMOS/NPN devices, current-pushing drivers might become more attractive. For the moment, current-pulling drivers are the preferred choice, unless other architectural limitations strip the designer of this choice. For example, VCSEL bars where the cathode is common to all lasers must be combined with a current-pushing driver.

The general characteristics of laser drivers outlined in this section will help us analyse the multiple optical transmitter designs present in the literature. Such an analysis will give a good perspective of the achievements and limitations of existing transmitters before commencing with the design of our own, and enable us to take accurate and informed design and layout decisions.

2.2 Transmission Line and Edge-Emitting Laser Drivers

Research efforts on edge-emitting laser drivers have exploded with the deployment of new fibre-based long-haul networks about 15 years ago. Various topologies have been proposed in several technologies, including silicon bipolar, gallium-arsenide (GaAs), and silicon-germanium (SiGe). Drivers in CMOS were rare because its performance was deemed insufficient. This situation changed when the digital semiconductor industry pushed CMOS performance to improve at a greater pace than other technologies [6]. Even with slight performance disadvantages, CMOS offers low cost and high integration capabilities for mixed-signal systems.

The edge-emitting lasers used for optical networks are high-power and are usually impedance-matched at a particular frequency. As a result, most edge-emitting laser driver experimental results are reported using ohmic transmission lines instead of actual lasers. Although edge-emitting lasers generally present low parasitic capacitance and inductance, such a practice limits our capacity to evaluate these drivers in an actual setting. On the other hand, it allows researchers to obtain intrinsic performance limits for particular driver topologies and technologies.

While modulator driver designs operating between 20Gbit/s and 40Gbit/s have been reported [7], the higher impedance and parasitics of edge-emitting lasers results in lower limits, even for costly technologies. Electrically differential and optically single-ended current-steering driver designs running between 5Gbit/s and 12Gbit/s have been reported in silicon bipolar [9] and AlGaAs/GaAs hetero-junction bipolar transistor (HBT) [11] technologies. While these figures are impressive, those drivers were not tested with actual lasers. An interesting driver based on a cascode differential amplifier was reported in [4], as illustrated in Figure 2.4. This driver, implemented in a GaAs technology, operates at 2.5Gbit/s using an actual edge-emitting laser diode. However, this driver needs a large voltage headroom, leading to a high power supply and rendering it inapplicable for low voltage CMOS.

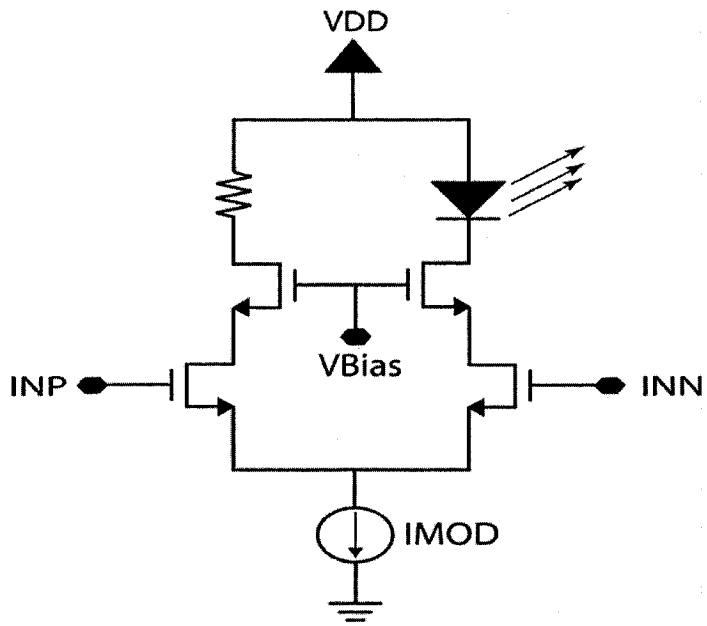


Figure 2.4: Cascode differential amplifier-based laser driver [4].

Early laser diode drivers in CMOS were reported by Shastri in [12]. A performance of 4Gbit/s was demonstrated with a 1.3um wavelength edge-emitting laser, although the reported bit-error rates (BER) were clearly insufficient. Recent CMOS drivers with data rates of 2.5Gbit/s [14] and 10Gbit/s [15] were reported in conferences, although these drive an ideal 50Ω termination. Generally, little work has been reported with actual lasers, particularly with respect to power consumption and BER figures. In the upcoming section, we will analyze VCSEL driver designs. As VCSEL are quite different from edge-emitting lasers, both electrically and optically, we will treat them in a separate section.

2.3 Vertical-Cavity Surface-Emitting Laser Drivers

With the emergence of VCSEL in short-to-medium reach optical transmitters, the development of drivers adapted to these applications become important. As the electrical characteristics of VCSEL are very different from edge-emitters, a specifically designed driver must be implemented. In particular, the input impedance of a VCSEL varies significantly with frequency, partially due to the non-negligible parasitics present in the

structure [16]. Many VCSEL driver designers assume a similar context to edge-emitting drivers, and test their driver with an ideal 50Ω impedance trace as the load, resulting in 10Gb/s operation with 45mW power consumption in CMOS 0.18μm [17]. As the VCSEL input impedance significantly departs from 50Ω at gigahertz frequency, this assumption is inaccurate. As a consequence, the performance of drivers tested in this fashion is overrated and not realistic from a practical perspective.

Innovative driver designs have been proposed to adapt to the new challenges introduced by VCSEL. In particular, two versions of a current-peaking driver in CMOS have been proposed by Annen in [18], as illustrated in Figure 2.5 [18]. Using this scheme, an additional current component, IPEAK, is added or subtracted during logic state transitions to decrease the rise and fall times. IPEAK is removed just following the transition. This can improve performance significantly, close to eight times in the presented case. On the other hand, using current-peaking techniques create significant noise on the power supply rails. Therefore, multiple channel drivers cannot use these techniques without unreasonable penalties in noise and data rate performance.

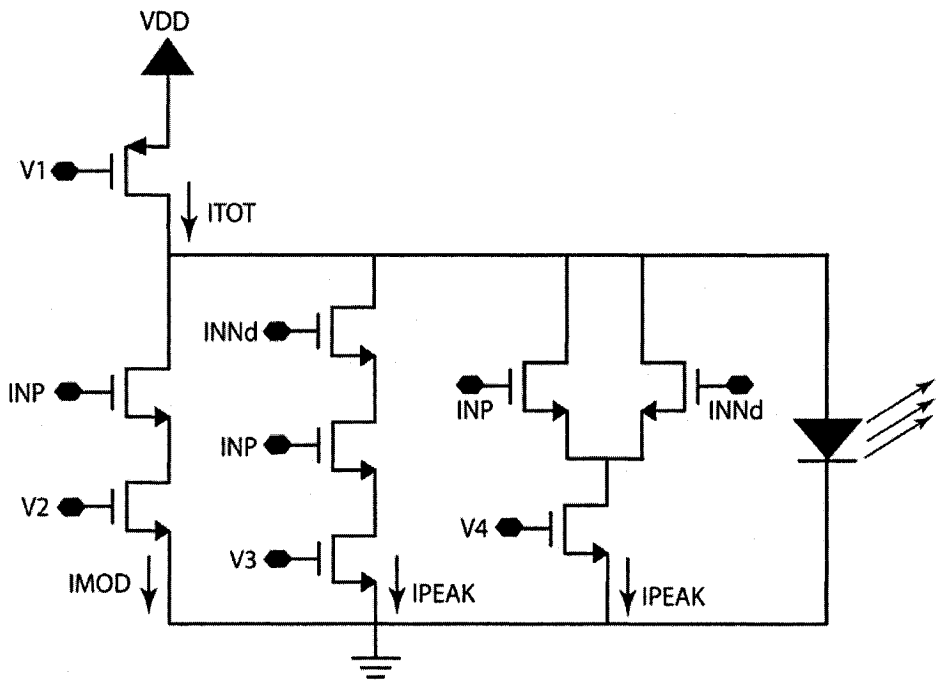


Figure 2.5: Two current-peaking VCSEL driver topologies [18].

Another approach involves the active addition and removal of the modulation current using both current sources and current sinks [20]. This approach, referred as a push-pull laser driver, is illustrated in Figure 2.6 [20]. Actively sourcing and sinking the modulation current is an interesting proposition as it allows fast and equal charging and discharging of the VCSEL junction parasitics. On the other hand, this driver includes four stacked transistors at minimum, which require large voltage supply headroom. For example, the regular 1.8V supply in 0.18um CMOS is not sufficient and a 3.3V supply must be used. This almost doubles the power consumption of the driver.

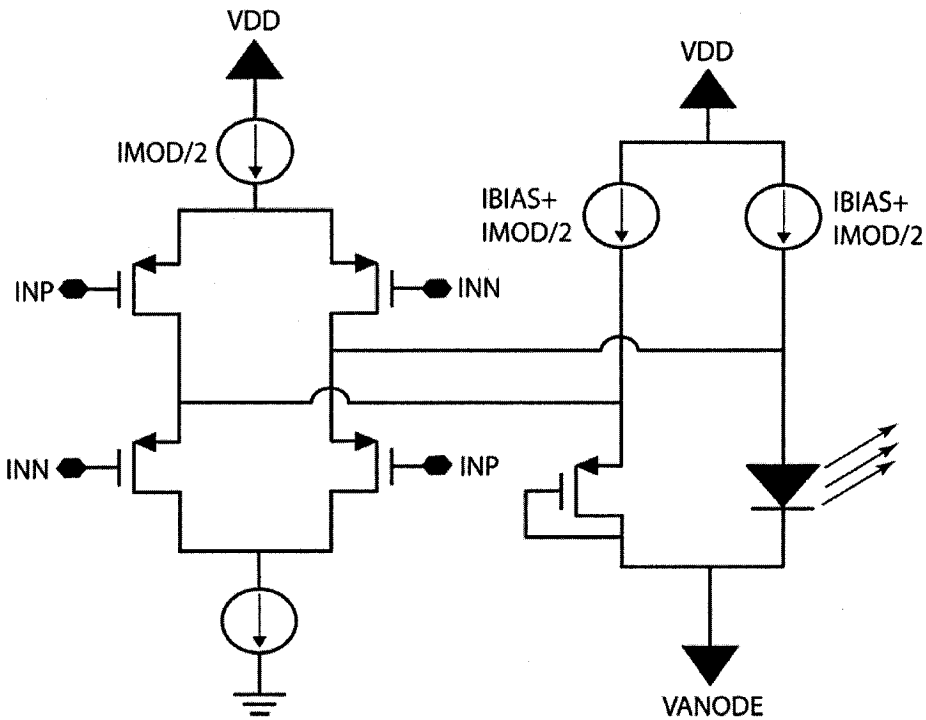


Figure 2.6: Push-pull VCSEL driver including bias current sources [20].

Achieving high data rates with a CMOS/VCSEL based optical transmitter poses great and unique challenges. Data rates of 1.25Gbit/s and 2.5Gbit/s have been reported in recent years [20]. This is clearly insufficient for next-generation short and medium-reach optical interconnections. Higher data rates have been achieved with other technologies, including InGaP/GaAs HBT [23]. However, the cost of these technologies is too high for many applications. As we have outlined in this chapter, many design options are available depending on the application requirements. In the following chapters, the

design of a versatile VCSEL driver targeted at short and medium-reach optical applications will be presented. Low power consumption, high data rate, and low cost will be given special consideration.

2.4 References

[1] R. Coppoolse, H. Van Parys, J. Codenie, and J. Vandewege, "Burst mode bipolar laser driver for a multipoint to point passive optical network at 155.52 Mbit/s," *in Proc. LEOS Summer Topical Meeting,* August 7-11, 1995, pp. 14-15.

[2] M. B. Venditti, E. Laprise, J. Faucher, P.-O. Laprise, J. E. A. Lugo, and D. V. Plant, "Design and test of an optoelectronic-VLSI chip with 540-element receiver-transmitter arrays using differential optical signaling," *IEEE J. Select. Topics Quantum Electron.,* vol. 9, pp. 361-379, March-April 2003.

[3] F. E. Kiamilev, and A. V. Krishnamoorthy, "A high-speed 32-channel CMOS VCSEL driver with built-in self-test and clock generation circuitry," *IEEE J. Select. Topics Quantum Electron.,* vol. 5, pp. 287-295, March-April 1999.

[4] J. Riishoj, "2.5 Gb/s laser-driver GaAs IC," *J. Lightwave Technol.,* vol. 11, pp. 1139-1146, July 1993.

[5] A. S. Sedra, and K. C. Smith, *Microelectronic Circuits.* 4th ed., New-York, NY: Oxford University Press, Inc., 1998.

[6] B. Razavi, *RF Microelectronics.* Upper Saddle River, NJ: Prentice-Hall, Inc., 1998.

[7] R. Schmid, T. F. Meister, M. Rest, and H.-M. Rein, "SiGe driver circuit with high output amplitude operating up to 23 Gbit/s," *IEEE J. Solid-State Circuits,* vol. 34, pp. 886-891, June 1999.

[8] R. Schmid, T. F. Meister, M. Rest, and H.-M. Rein, "40Gbit/s EAM driver IC in SiGe bipolar technology," *Electron. Lett.,* vol. 34, pp. 1095-1097, May 1998.

[9] R. H. Derksen, and H. Wernz, "Silicon bipolar laser driving IC for 5 Gb/s and 45-mA modulation current and its application in a demonstrator system," *IEEE J. Solid-State Circuits,* vol. 28, pp. 824-828, July 1993.

[10] H.-M. Rein, E. Bertagnolli, A. Felder, and L. Schmidt, "Silicon bipolar laser and line driver IC with symmetrical output pulse shape operating up to 12 Gbit/s," *Electron. Lett.,* vol. 28, pp.1295-1296, July 1992.

[11] K. Runge, D. Daniel, R. D. Standley, J. L. Gimlett, R. B. Nubling, R. L. Pierson, S. M. Beccue, K.-C. Wang, N.-H. Sheng, M.-C. F. Chang, D. M. Chen, and P. M. Asbeck, "AlGaAs/GaAs HBT IC's for high-speed lightwave transmission systems," *IEEE J. Solid-State Circuits,* vol. 27, pp. 1332-1341, October 1992.

[12] K. R. Shastri, K. N. Wong, and K. A. Yanushefski, "1.7 Gb/s NMOS laser driver," *in Proc. Custom Integrated Circuit Conf.,* 16-19 May, 1988, pp. 5.1.1-5.1.4.

[13] K. R. Shastri, K. A. Yanushefski, J. L. Hokanson, and M. J. Yanushefski, "4.0Gb/s NMOS laser driver," *in Proc. Custom Integrated Circuit Conf.,* 15-18 May, 1989, pp. 14.7/1-14.7/3.

[14] N. Haralabidis, and G. Halkias, "A CMOS laser driver with independently adjustable DC and modulation currents for data rates up to 2.5 Gb/s," *in Proc. Int. Symp. On Circuits and Systems,* May 28-31, 2000, vol. 5, pp. 425-428.

[15] K. Petersen, K. Kiziloglu, T. Yoon, F. Williams, Jr., and M. R. Sandor, "Front-end CMOS chipset for 10 Gb/s communication," *in Proc. IEEE Radio Frequency Integrated Circuit Symp.,* 2-4 June, 2002, pp. 93-96.

[16] C.-H. Chang, L. Chrostowski, and C. J. Chang-Hasnain, "Parasitics and design considerations on oxide-implant VCSELs," *IEEE Photon. Technol. Lett.,* vol. 13, pp. 1274-1276, December 2001.

[17] R. Tao, M. Berroth, and Z. G. Wang, "Low power 10Gbit/s VCSEL driver for optical interconnect," *Electron. Lett.,* vol. 39, pp. 1743-1744, November 2003.

[18] R. Annen, H. Melchior, R. King, and K. J. Ebeling, "Fully integrated 0.25um CMOS 4x8 VCSEL driver array IC with 2.5 Gbit/s/channel bit rate and low cross talk," *in Proc. 14th Annual Meeting of the IEEE LEOS,* November 12-13, 2001, vol. 2, pp. 449-450.

[19] R. Annen, and H. Melchior, "Fully integrated 0.25um CMOS VCSEL driver with current peaking," *Electron. Lett.,* vol. 38, pp. 174-175, February 2002.

[20] D. V. Plant, A. E. L. Chuah, M. B. Venditti, and A. Isac, "0.18-um complementary metal-oxide semiconductor push-pull vertical-cavity surface-emitting laser driver operating at 2.5 Gb/s with symmetric rising and falling edges," *Applied Optics,* vol. 43, pp. 2730-2733, May 2004.

[21] B. Madhavan, and A. F. J. Levi, "Low-power 2.5Gbit/s VCSEL driver in 0.5um CMOS technology," *Electron. Lett.*, vol. 34, pp. 178-179, January 1998.

[22] F. Delpiano, B. Bostica, M. Burzio, P. Pellegrino, L. Pesando, "10-channel optical transmitter module operating over 10 Gb/s based on VCSEL and hybrid integrated silicon optical bench," *in Proc. 49th Electronic Components and Technology Conf.*, June 1-4, 1999, pp. 759-762.

[23] J. Y. Eo, S. Kang, H.-H. Park, D. Y. Jung, C. S. Park, and K. S. Yoon, "A low-power-consumption VCSEL driver IC for 10Gb/s direct modulation using InGaP/GaAs HBT," *in Proc. 5th Pacific Rim Conf. on Lasers and Electro-Optics,* December 15-19, 2003, vol. 2, p. 434.

3 Versatile Low-Power Optical Transmitter Design

3.1 Architectural Design Decisions

The last chapter included a detailed characterization of optical transmitters with a focus on the driver stage. Based on the numerous observations made in that chapter and the targeted applications for our design, namely short and medium-reach optical interconnects, several design decisions were required. We will first highlight these design choices and introduce the basic principles behind our versatile low-power optical transmitter. In the following sections, a detailed description of the design steps involved in each stage of the transmitter will be given.

Although chip area utilisation is not really a factor for access network optical transmitters, except for cost issues, it is very important in multiple channel short-reach optical interconnects. Commercial VCSEL arrays generally have an individual device pitch of 125μm to 250μm, such that the optical transmitter circuitry must fit within a square of 125μm by 250μm [1]. This prevents the designer from using widely used radio-frequency (RF) techniques such as on-chip inductors or resistors that consume large amounts of chip area. For that reason, a voltage-driver could not be used in order preserve the versatility of our design, and a current-drive topology was chosen.

It has been demonstrated by Venditti et al. that an electrically and optically differential optical transmitter have better noise performance than its single-ended counterpart for multiple channel short-reach optical interconnects [2]. On the other hand, the overhead cost of using two fibres per user for implementing optically differential signaling is too large, with negligible gains as we are dealing with a single channel. Nevertheless, this does not prevent us from using electrically differential signaling, which conserves some of the benefits of fully differential signaling, mainly its noise robustness [3]. Consequently, electrically differential and optically single-ended signaling was implemented.

The low-voltage differential signaling (LVDS) standard was chosen for the inputs of the optical transmitter [4]. This standard is widely used and is simple to implement. The interfacing between CMOS digital circuitry and the optical transmitter is simple using a LVDS driver, which converts complementary railed signals of the digital CMOS to voltage swings of 0.4V feeding the optical transmitter. As a result, the optical transmitter is easily integrated with digital processing circuits on the same chip. In addition, LVDS can be used in combination with AC or DC coupling, whatever option we choose to implement.

Current-switching drivers are simple to implement and consume very low power. On the other hand, they generate significant amounts of switching and substrate noise, to a level where it significantly reduces performance for multiple channel transmitters. As a result, we implemented a current-steering driver, which consumes from 10% to 30% more power than current-switching drivers (dependent on bias current and modulation current relative levels, transistor sizing, etc.) but generates little switching noise. Again, versatility was of premium importance in this design choice.

Finally, a current-pulling driver was implemented to achieve maximum performance using NMOS transistors for current-steering. As will be shown in the next section, the performance of PMOS transistors is significantly lower. We reduced their presence in our design to a minimum. Some innovative approaches mentioned in chapter 2 where considered but none fitted in our design goals. Current-peaking techniques enhance performance but are not applicable for multiple channel applications, as they generate a lot of switching noise. The cascode or push-pull laser drivers require large voltage supply headroom and significantly increase power consumption. As we targeted the lowest power consumption while being versatile, we could not use these topologies.

The resulting high-level architecture of the VCSEL-based optical transmitter is illustrated in Figure 3.1. The LVDS inputs are fed into a differential pre-amplifier, which brings the 0.4V inputs close to the power supply rail of 1.8V. A pulse-shaping stage is inserted between the pre-amplifier and the optically single-ended current-steering laser driver [5]. This stage will be described in greater details in section 3.4. It essentially

shapes the output of the pre-amplifier to improve the performance of the laser driver stage, which is the performance limiting section of our optical transmitter, due to high currents, larger transistors and parasitic loading of the VCSEL diode. The inputs are matched to 50Ω using a differential 100Ω input resistor, which will be implemented on-chip.

The design choices described above ensure the proposed optical transmitter is easily scalable to smaller gate length CMOS or to multiple channel applications. A multiple channel implementation will not require additional design work. Only minor layout modifications to convert the transmitter into a standard cell would be needed. The proposed topology is easily transferable to 0.13μm or smaller CMOS technologies.

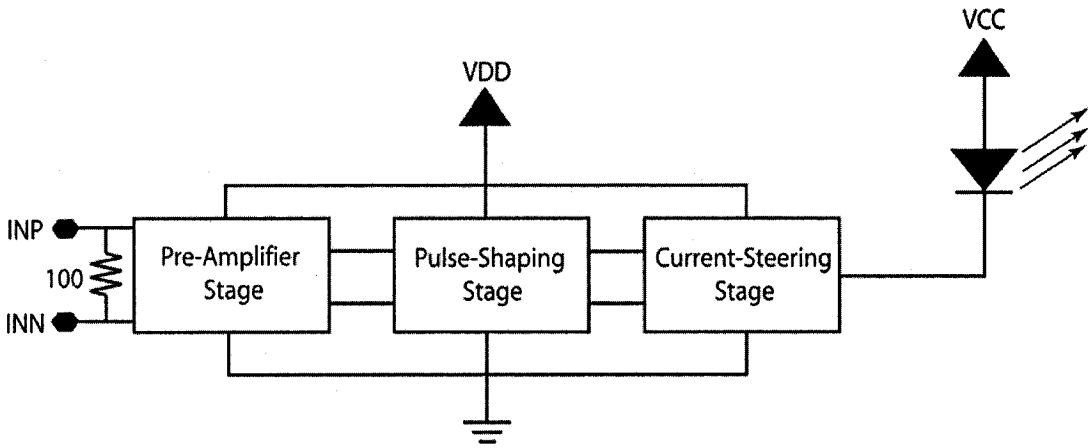


Figure 3.1: High-level architecture of the VCSEL-based optical transmitter.

3.2 Optimum Performance Bias Analysis

In order to obtain maximum performance with the minimum bias currents possible to save power, a detailed analysis of the transistors for the technology used for this project must be conducted. A 0.18μm CMOS technology offered by the Taiwan Semiconductor Manufacturing Corporation (TSMC) and supplied through the Canadian Microelectronics Corporation (CMC) was chosen for this project. Its low cost and wide availability makes it a perfect choice for implementing end-user transmitters applicable to next-generation access networks. In addition, CMOS transmitters can be integrated with

digital signal processing (DSP) circuits on the same chip, further reducing costs and design complexity.

Performance was evaluated using current-gain curves analysis. This technique is commonly used to determine the optimum biasing level in circuits operating in the small-signal regime. It is unclear in literature if applying it to large-signal circuits yields optimum performance biasing. From the curves that will be shown in this section, using an average current close to the maximum unity-gain frequency insures operation of the circuits in a wide region of best performance. Instead of using pure trial and error as is usually the case in large-signal circuit biasing, using current-gain curves analysis provides a good starting point. Further simulations showed that this approach yielded the best performance for every section of the optical transmitter.

Using the simulation setup shown in Figure 3.2, the frequency where the current gain I_{out}/I_{in} (or $|h_{fe}|$) is equal to 0dB was evaluated. This frequency is commonly called the unity-gain frequency or f_T and is typically used as measure of the maximum usable frequency a technology can perform [6]. The gain curve for a MOS transistor follows equation 3.1 [3]. This means we expect the curve in decibels to start at an initial gain value and drop by 20dB/decade until it reaches f_T. For various biasing conditions, a current-gain curve was simulated and f_T was obtained. Based on those results, a curve of the unity gain frequency versus bias current can be plotted and the optimum bias point for a particular transistor size can be obtained.

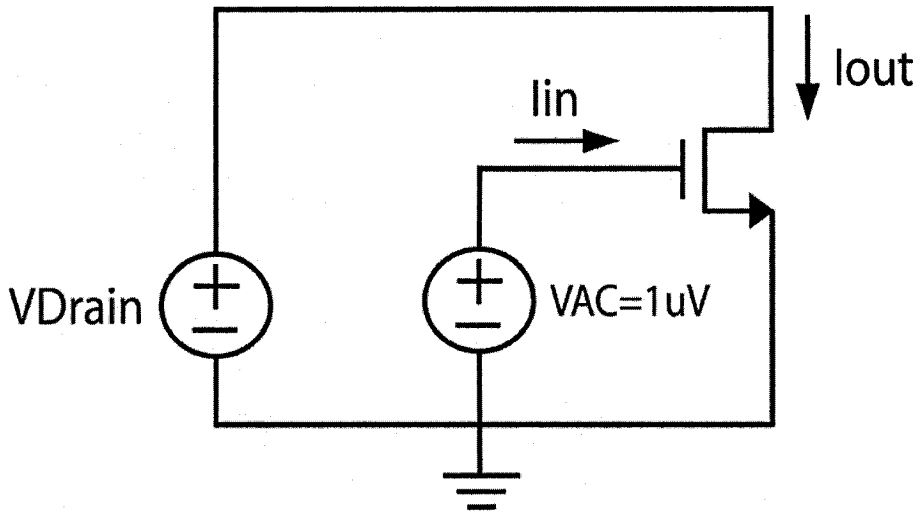


Figure 3.2: Simulation setup for current-gain curve analysis [6].

$$\frac{I_O}{I_I} = \frac{g_m}{j\omega(C_{gs} + C_{gd})} \quad \textbf{(3.1)}$$

As our optical transmitter was targeted for multi-gigabit per second applications, it is strongly recommended by TSMC that we use the RF models available in the simulation libraries [7]. Unfortunately, that model is valid for a single width of 2.5µm, such that it is not possible to use smaller transistors while using this model. On the other hand, we did not want to use a more generic model and smaller transistors and risk having unreliable simulation results, such that we chose to use transistor widths of 2.5µm and use the RF model in the high-speed path. It is obvious that using smaller transistors would have resulted in higher performance, especially in the pre-amplifier and pulse-shaping stages, which will be described shortly. Using this model and the procedure detailed earlier, a curve for f_T versus bias current at 27°C was derived, as shown in figure 3.3. It can be observed from this curve that a bias current of 0.5mA is required in order to attain maximum performance and a f_T of approximately 45 GHz. By using a bias current of approximately 0.400mA, we still achieve near optimum performance while saving some more power. In addition, as will be exposed in Figure 3.6, the maximum f_T of PMOS transistors is reached at a bias current around 0.400mA. At this current, both NMOS and PMOS transistors operate optimally. Consequently, this is the bias current that will be used for the design of the optical transmitter.

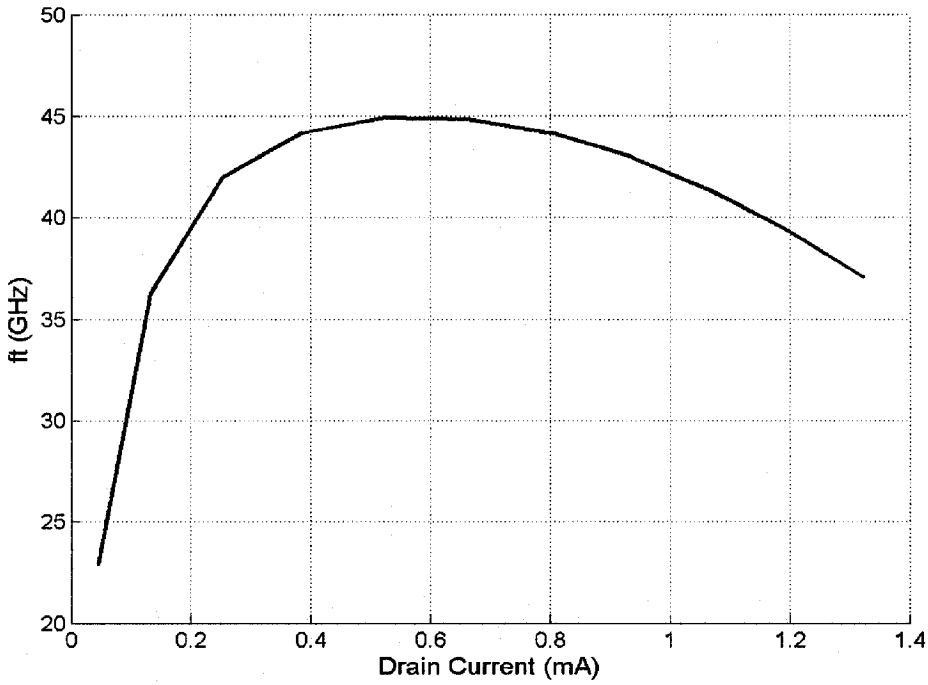


Figure 3.3: Unity gain frequency versus bias current for the RF transistor model with width=2.5μm and length=0.18μm at 27°C.

Unity gain frequency curves were also simulated for multiple gate lengths to evaluate the impact of longer gate dimensions on performance. For convenience in comparing the various lengths, the drain current was normalized by multiplying it by the length. Unity gain frequency curves for gate lengths of 0.18μm, 0.3μm, and 0.5μm are given in Figure 3.4. The maximum unity gain frequency is drastically reduced as the gate length is increased. This is expected as larger gate lengths increase the gate capacitance significantly. As a result, the use of gate lengths larger than the minimum value of 0.18μm should be avoided in the high-speed path at all costs.

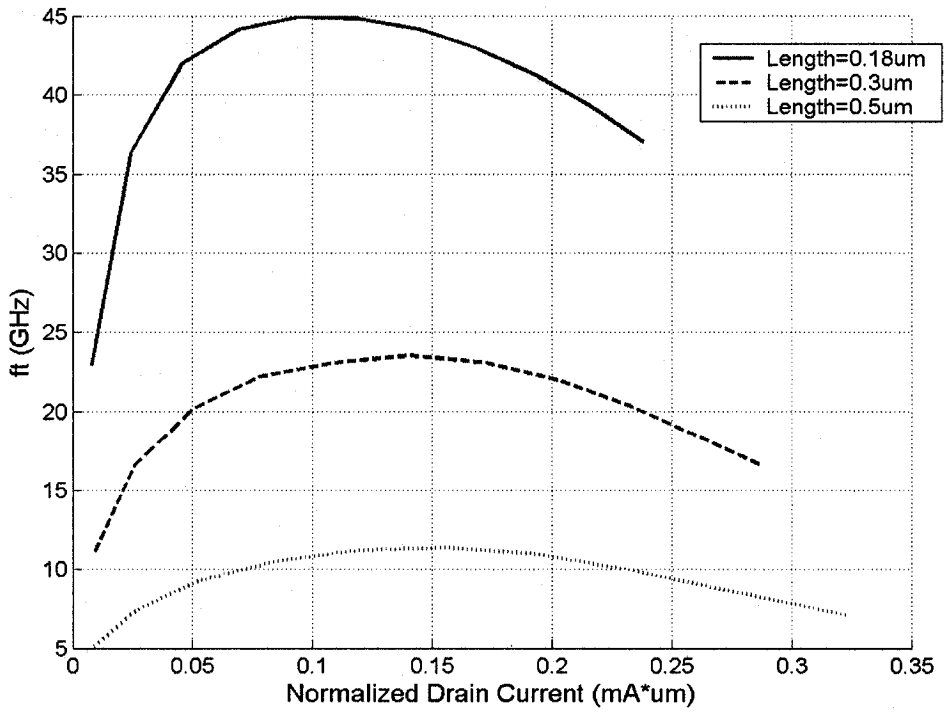


Figure 3.4: Unity gain frequency curves for various transistor gate lengths at 27°C.

Finally, unity gain frequency curves were obtained at multiple temperatures for a gate length of 0.18μm and a width of 2.5μm. Curves for temperatures of 27°C, 50°C and 75°C are given in Figure 3.5. The maximum unity gain frequency reduces significantly as the operating temperature increases. Consequently, it is important to evaluate the expected operating temperature prior to simulating the optical transmitter to obtain accurate simulation results.

The performance of a PMOS transistor was also evaluated using the same methodology. Figure 3.6 shows the unity gain frequency curves for an NMOS and a PMOS device with a length of 0.18μm and a width of 2.5μm at 27°C using the RF models for both devices. The maximum f_T of PMOS devices is close to 23GHz. It is obvious from those curves that NMOS devices outperform PMOS devices significantly. This confirms the initial assumption that NMOS are faster and validates the use of NMOS in the transmitter wherever possible to increase performance.

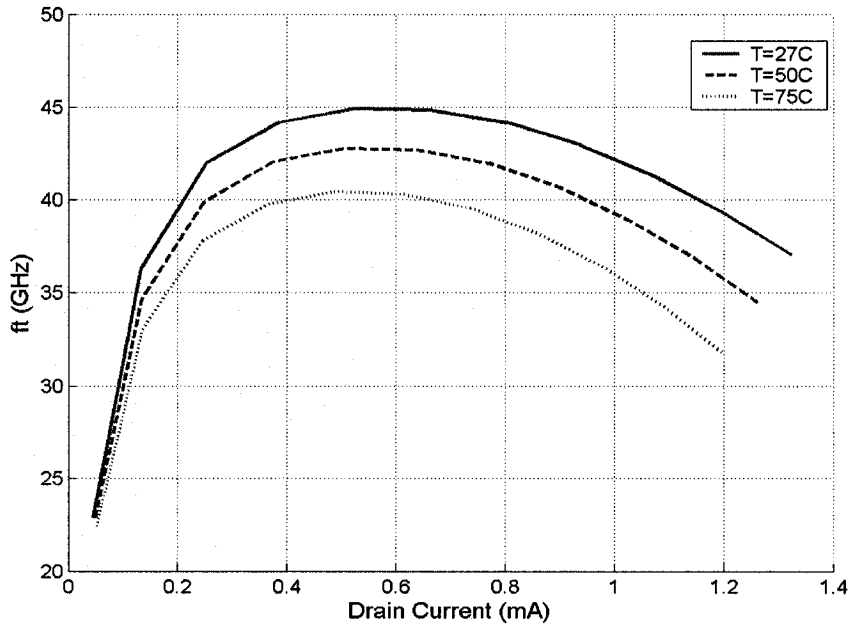


Figure 3.5: Unity gain frequency curves for various operating temperatures for a transistor gate length of 0.18um and width of 2.5um.

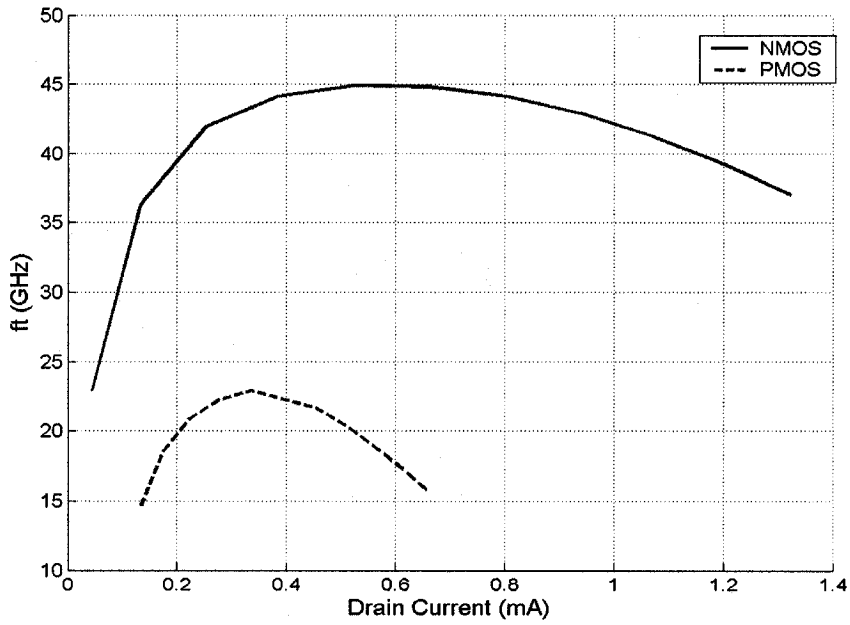


Figure 3.6: Comparison of NMOS and PMOS unity gain frequency curves using a typical RF transistor at 27°C.

3.3 Pre-Amplifier Design

The design of the optical transmitter pre-amplifier was kept simple to minimize power consumption and chip area utilization. Two design options were considered, namely a common-source differential amplifier and a common-gate differential amplifier. As the complementary input signals are fed into the pre-amplifier through a 50Ω transmission line (coplanar probe or printed-circuit board trace), the chip inputs were matched to 50Ω using a differential 100Ω on-chip resistor between the two input points of the pre-amplifier, as illustrated in Figure 3.10.

It is commonly known that a common-gate amplifier has a higher 3-dB frequency than its common-source counterpart, mainly due to the fact that the Miller effect is not present in common-gate design [3]. This was verified through simulation by designing both topologies and comparing them. The maximum gain was also evaluated. This process is detailed in the following subsections.

3.3.1 Common-source Amplifier

A typical common-source pre-amplifier was designed using the TSMC CMOSP18 kit supplied by CMC in Cadence Virtuoso and simulated through Affirma Analog Circuit Design Environment with SpectreS simulator. A diagram of the amplifier is shown in Figure 3.7. The transistor sizes were chosen such that the RF models could be used in the high-frequency path. The current source transistors were made bigger in order to minimize the drain-source voltage drop of the current source and increase the voltage headroom available for the transistors. All transistor sizes are summarized in Table 3.1. All simulations were conducted at 50°C, which is the expected temperature of operation, based on projections from the VCSEL specifications sheet [8].

Transistor	Width (μm)	Length (μm)
M1, M2, M3, M4	2.5	0.18
M5	7.5	0.18

Table 3.1: Transistor sizes for the common-source amplifier.

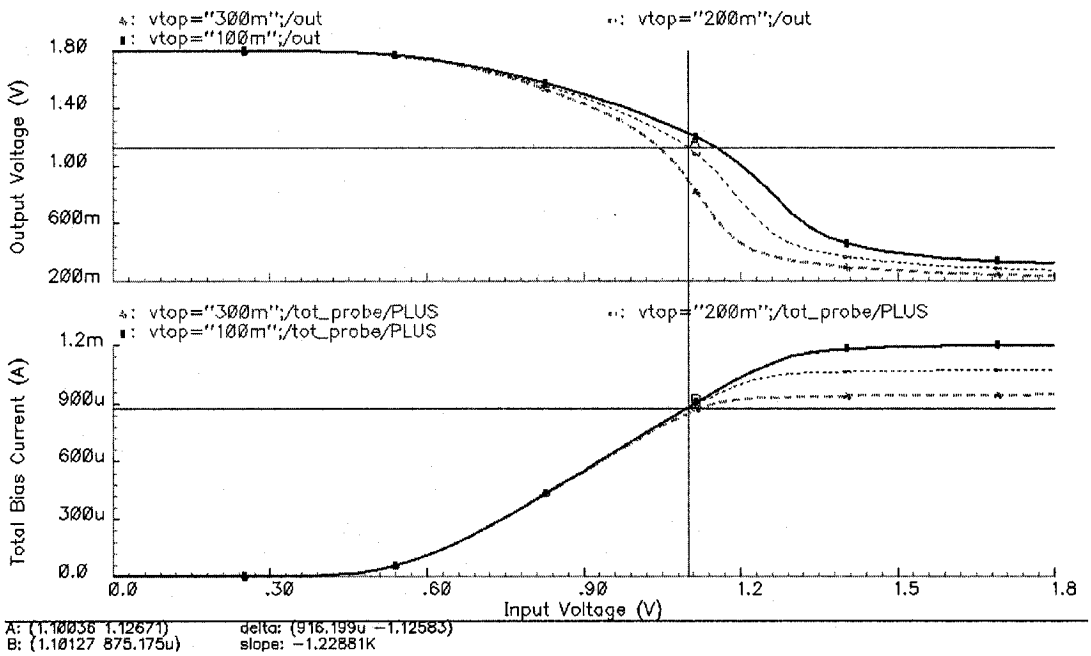


Figure 3.8: DC biasing transfer curves for the common-source amplifier.

Using the biasing conditions stated above with a sinusoidal signal of amplitude equal to a LVDS input signal of 0.4V and a 100Ω resistor between the pre-amplifier inputs for matching to 50Ω transmission lines, multiple transient analyses were conducted to determine the -3dB frequency of the amplifier. The gain was computed manually at every operation frequency and a gain curve was plotted. A loading capacitor of 10fF (the extracted parasitic capacitance of the next stage input transistor) is connected at the outputs of the amplifier to emulate the gate capacitance of a RF transistor, which will be the input of the next stage. The AC transfer function curve under these conditions is given in Figure 3.9. The -3dB frequency is located at approximately 6GHz or 12Gbit/s, with a DC maximum gain of 8.3dB. This gain yields a voltage swing at the output between 0.32V and 1.36V. As we will see in the next sub-section, this performance is quite reasonable but slightly less than the common-gate configuration. For this reason, the common-source topology was discarded as a candidate for the pre-amplifier stage.

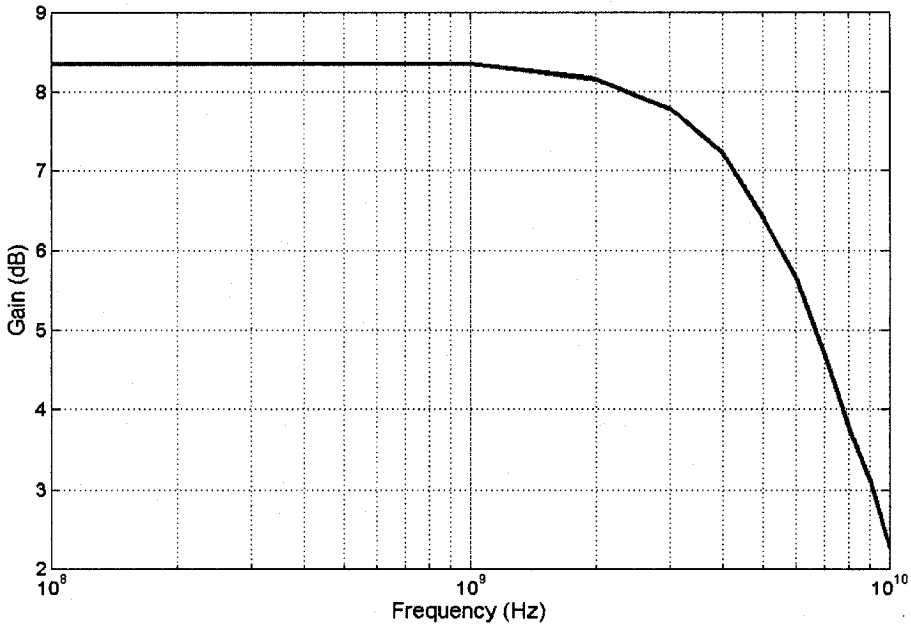


Figure 3.9: AC transfer function of the common-source amplifier.

3.3.2 Common-gate Amplifier

The same simulation conditions were used to evaluate the potential of the common-gate topology for the optical transmitter pre-amplifier. The diagram of the differential common-gate amplifier considered for this project is given in Figure 3.10. As with the common-source topology, three voltages can be varied to set the bias level, namely VTOP, VBOT, and VBIAS. The input nodes DC level should be set to the equilibrium point of the chosen biasing condition such that no DC current flows in or out of the inputs when DC coupling is used. Under AC coupling circumstance, this issue does not arise as the input nodes are isolated from the amplifier at DC using a capacitor. The transistor sizes are summarized in Table 3.2 below.

Transistor	Width (μm)	Length (μm)
M1, M2, M3, M4	2.5	0.18
M5, M6	5.0	0.18

Table 3.2: Transistor sizes for the common-gate amplifier.

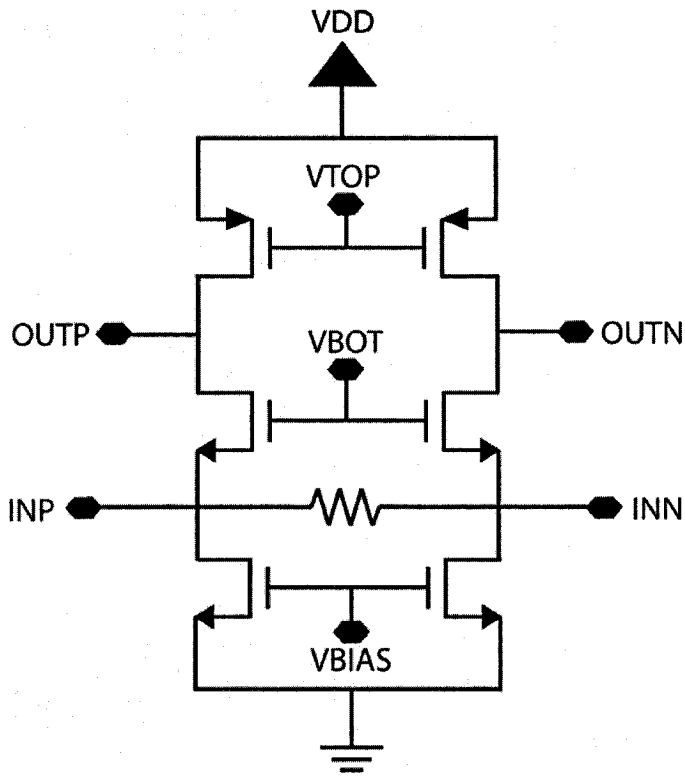


Figure 3.10: Diagram of the common-gate amplifier.

As for the common-source topology, the bias current in each branch of the differential common-gate amplifier was set close to the maximum performance value, at 340uA. The biasing was chosen to get maximum linearity in the output voltage transfer curve. Bias voltages VTOP of 0.4V, VBOT of 1.2V, and VBIAS of 0.8V were chosen. This yields a DC input value of 0.226V, above which the LVDS signal swings between 0.026V and 0.426V. The chosen DC voltage values are illustrated in Figure 3.11 and compared with different values of VTOP.

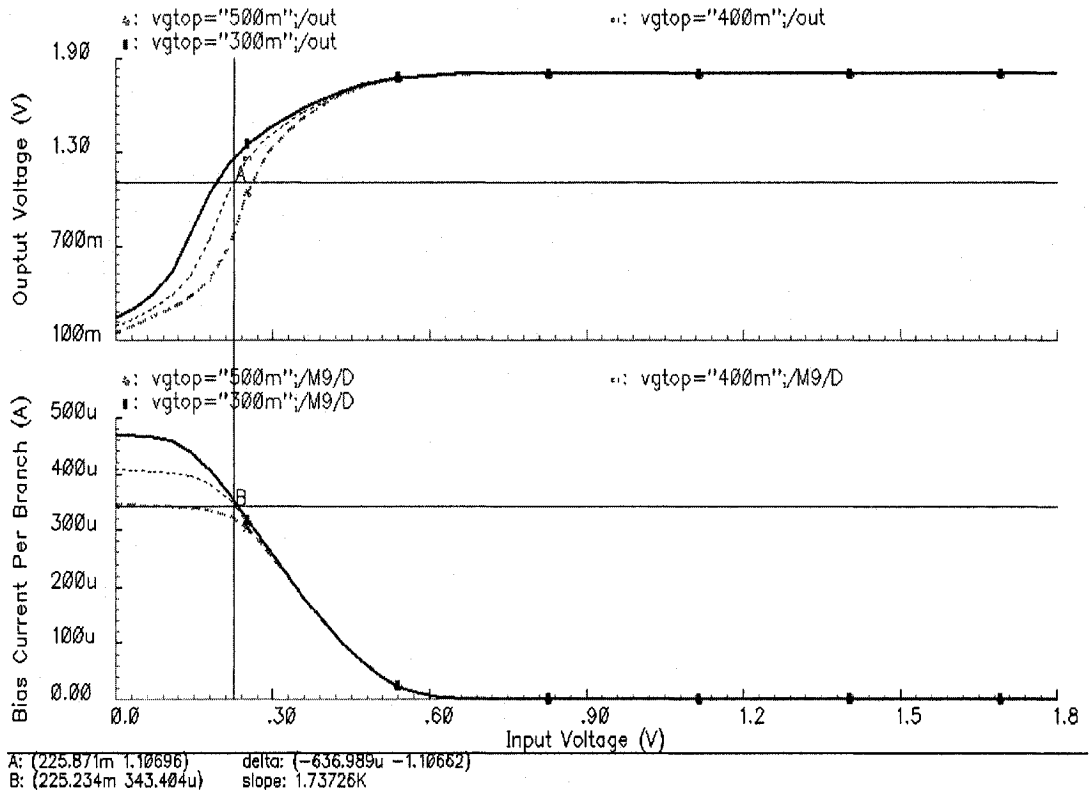


Figure 3.11: DC biasing transfer curves for the common-gate amplifier.

The AC transfer function was derived using a sinusoidal input signal with a 400mV peak-to-peak swing. Multiple transient analyses were conducted, as with the common-source amplifier. Again, the inputs are matched to 50Ω using a 100Ω differential resistor. With a loading capacitor of 10fF at each outputs, the -3dB frequency is at 6GHz or 12Gbit/s, as was the case with the common-source amplifier. On the other hand, the maximum gain is almost 3dB higher, implying that the gain-bandwidth product of the common-gate topology is higher than the common-source amplifier. The AC transfer function is provided in Figure 3.12. The voltage swing for the output voltage is between 0.23V and 1.67V. The amplifier consumes a total current of 685μA.

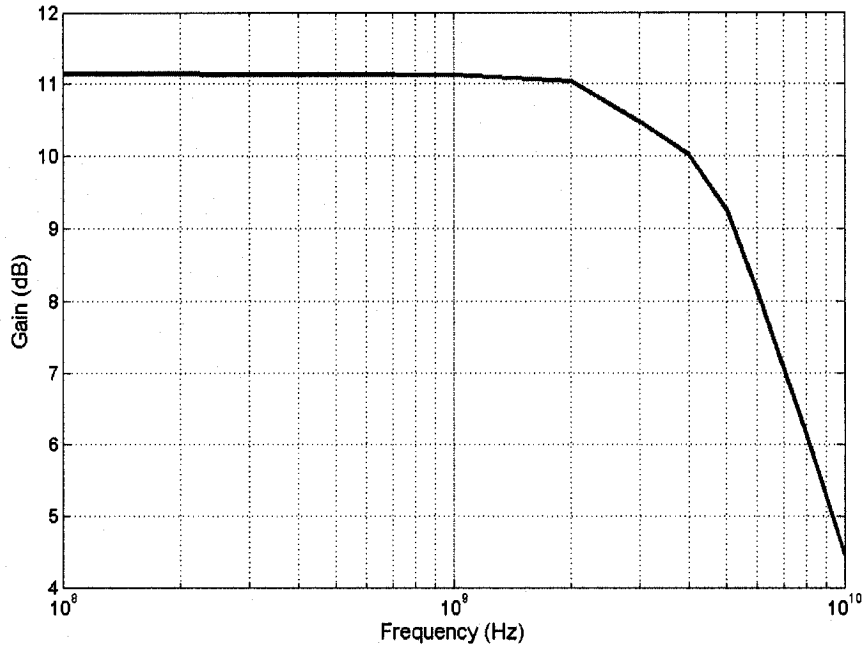


Figure 3.12: AC transfer function illustrating the -3dB frequency of the common-gate amplifier.

This analysis isolated the common-gate architecture as the best choice for the pre-amplifier stage. The bandwidth is the same as the common-source topology while the gain is 2dB higher. This will enable the implementation of a single-stage pre-amplifier, thus saving power consumption and reducing chip area usage. In the next section, the design of the two following stages of the optical transmitter is presented.

3.4 Pulse-Shaping and VCSEL Driver Design

The amplified signal can be applied directly to a VCSEL driver stage that converts the signal to current. This very simple approach has the advantage of consuming little power. On the other hand, in order to achieve high data rates with low switching noise, the signal must be shaped prior to the final stage, such that the optimum signal is applied to the driver. Both the pulse-shaping and the driver stages are described in this section.

3.4.1 Pulse-Shaping Stage

In a differential current-steering driver stage, applying a full-swing signal at the inputs will cause ringing to occur at the current output. In order to illustrate this behaviour, a typical current-steerer illustrated in figure 3.13 is analyzed. Initially, as INP is high and INN is low, ILEFT is IMOD, the modulation current, and IRIGHT is zero. During switching, as the voltage at INP is reduced, ILEFT goes down, while IRIGHT does not go up until the voltage at INN reaches V_X+V_T. Midway through the switching process, both ILEFT and IRIGHT almost reach zero, since INP and INN are lower than V_X+V_T. At that point, the current source discharges the node at V_X, and the voltage drops. When IRIGHT finally rises, this node must be recharged, causing significant overshoot before settling down. This behaviour is illustrated in figure 3.14 [5]. In order to eliminate this undesirable effect, the voltages at INP and INN must be kept above V_X+V_T at all times. This could be achieved by tweaking the pre-amplifier to have exactly the right voltage swing at its output. On the other hand, it is highly desirable to have a driver with an adjustable IMOD than can adapt to various transmission requirements. Because of this, V_X will also vary such that the lower limit of V_X+V_T will vary depending on the modulation current we use. Consequently, an additional stage that has a variable low voltage output is inserted between the pre-amplifier and the VCSEL driver [5].

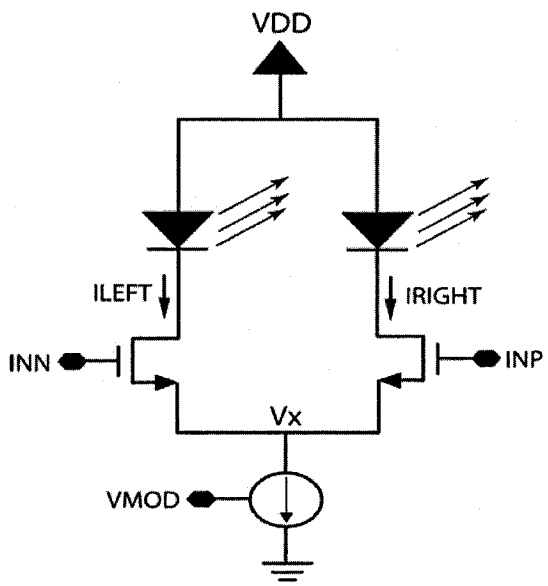


Figure 3.13: Differential current-steering laser driver with voltage and current references.

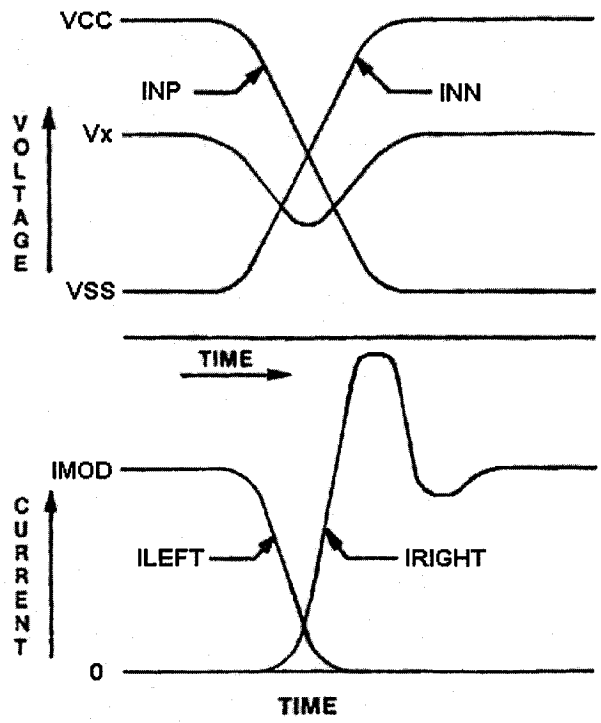


Figure 3.14: Analysis of a typical current-steerer switching behaviour [5].

The pulse-shaping stage is implemented as a simple common-source amplifier with a fixed gain by connecting the PMOS gates to ground. This topology is illustrated in figure 3.15, with the transistor sizes given in table 3.3. With this configuration, the output voltage varies between 1.35V and 1.8V for a VSOURCE of 0.8V and between 0.36V and 1.8V for a VSHAPE of 1.2V. This flexibility enables the use of a wide range of modulation currents at the VCSEL driver without incurring significant ringing of the VCSEL current. As we will see in the next subsection, depending on the modulation current, V_X varies between 0.1V and 0.4V. With a V_T of approximately 0.6V, an appropriate low voltage can be applied to the VCSEL driver. The current consumption of this stage varies depending on the bias conditions. For an average modulation current swing of 2mA, the pulse-shaping stage draws 660μA.

Transistor	Width (μm)	Length (μm)
M1, M2, M3, M4	2.5	0.18
M5	5	0.18

Table 3.3: Transistor sizes for the pulse-shaping stage.

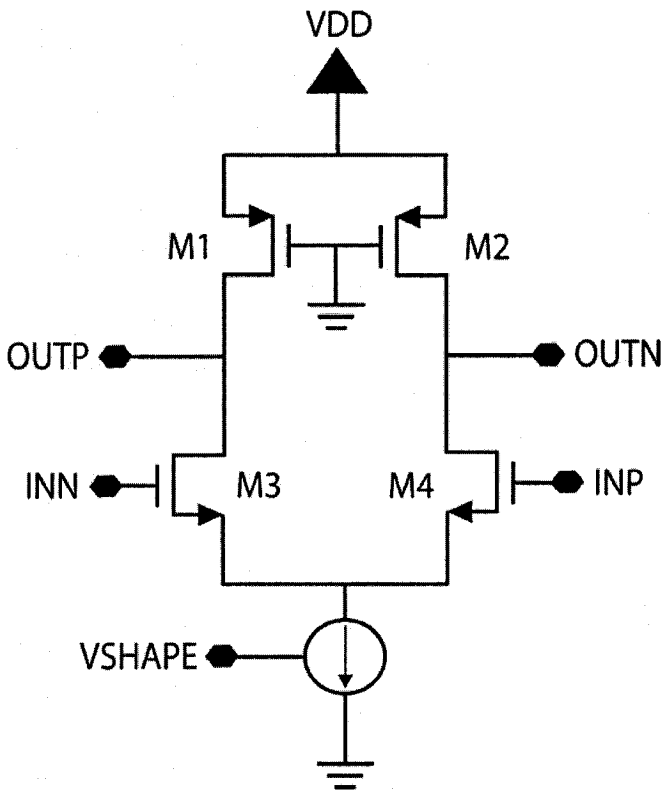


Figure 3.15: Pulse-Shaping stage implemented as variable bias common-source differential pair.

3.4.2 VCSEL Driver Stage

The last stage of the optical transmitter converts the voltage signal outputted by the pulse-shaping section to a current modulated signal that is directly applied to the VCSEL. It is implemented as an optically single-ended current steerer with an on-chip adjustable biasing current source that applies the optimum performance bias current to the VCSEL depending on the targeted bit rate. The range of currents achieved by the bias current source is 0mA to 8mA. Since the VCSEL maximum rated DC current is 9mA, all biasing possibilities are covered [8]. The diagram of the VCSEL driver stage is provided in Figure 3.16. In addition, the transistor dimensions are given in Table 3.4.

Transistor	Width (μm)	Length (μm)
M1, M2, M3	10	0.18
M4	15	0.18
M5	15	0.18

Table 3.4: Transistor sizes for the VCSEL driver stage.

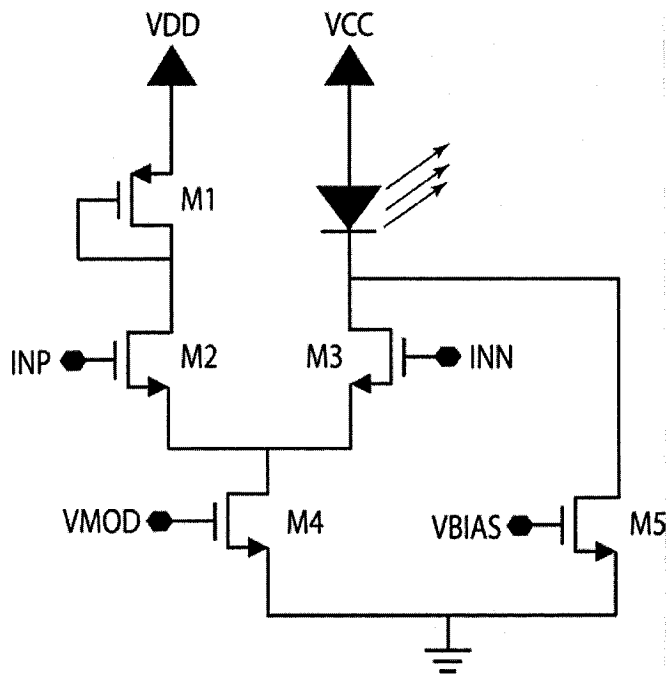


Figure 3.16: VCSEL driver stage implemented as a current-steerer.

A dummy load is implemented in the left branch of the current steerer as a diode-connected PMOS. This load is used to mimic the behaviour of the VCSEL, such that both branches of the circuit are as balanced as possible. In order to achieve this, the saturation differential resistance of the diode-connected PMOS should be equal to the differential resistance of the VCSEL, derived from its V-I curve. This must be true for currents between approximately 1mA and 4mA, as this is the range of modulation currents that can be applied by the modulation current source to the differential current-steering pair. This range of currents was chosen as large as possible given the VCSEL specifications [8]. On the other hand, the voltage supply above the PMOS load is 1.8V while the voltage supply at the VCSEL is 3.3V, since the forward voltage of the VCSEL is approximately 2V. In addition, the above threshold voltage drops are different for both elements. In order to have the same voltage swings at the drains of transistors M2 and M3, all these factors must be taken into account.

Actual physical VCSEL devices were not available at design time, such that we relied on specification sheets to obtain the VCSEL differential resistance and forward voltage. This proved to be the highest source of error in the initial design approach, as

will be demonstrated in the next section. This resulted in slight unbalance of the voltages at M2 and M3, although the impact on performance in negligible. On the other hand, additional switching noise is generated, such that this should be corrected before implementing this design in a multi-channel optical interconnection. In addition, the VCSEL differential resistance is quite low at around 70Ω, according to the specifications sheet [8]. In order to get such a low resistance with a diode-connected PMOS, the size of the transistor would have to be very large. This would have a negative impact on the performance of the driver due to high capacitive parasitics. We tried to equilibrate those two considerations and selected a medium sized PMOS with a width of 10μm, yielding a differential resistance of approximately 350Ω. Since the VCSELs have a forward voltage drop of approximately 2V, it must be biased to a voltage of approximately 3.3V (VCC), in order to have sufficient voltage headroom at the drain of M3. We will detail in the next chapter how we dealt with the dual voltage supply structure. Finally, preliminary simulations were conducted with the complete optical transmitter schematic, modeling the VCSEL as an ideal 50Ω load. The simulation results, obtained through SpectreS, are given in Figure 3.17 for a data rate of 2.5Gbit/s and a maximum modulation current swing and bias current of 4mA and 8mA respectively.

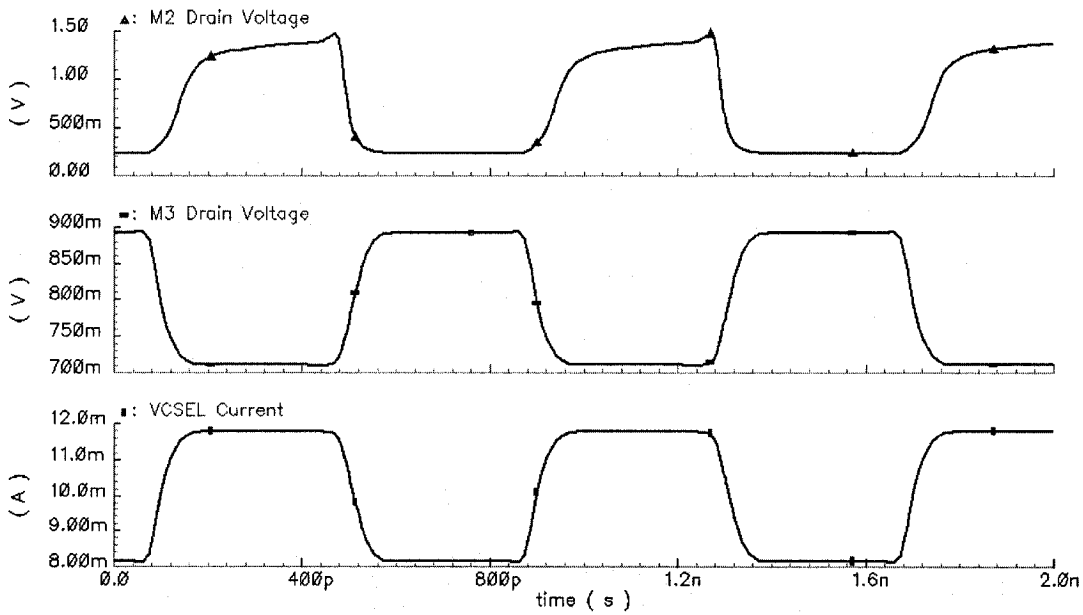


Figure 3.17: Preliminary simulation results showing 2.5Gbit/s performance and unbalance between the two branches of the current-steerer.

We see that a data rate of 2.5Gbit/s is easily attained under those ideal conditions. On the other hand, parasitics present in the VCSEL, package and test fixture, as well as the layout parasitics of the transmitter itself will significantly reduce the maximum performance. In the following section, layout procedures and careful modeling procedures for the VCSEL, package and fixture will be presented. This will lead to accurate simulations of the optical transmitter performance.

3.5 References

[1] M. B. Venditti, E. Laprise, J. Faucher, P.-O. Laprise, J. E. A. Lugo, and D. V. Plant, "Design and test of an optoelectronic-VLSI chip with 540-element receiver-transmitter arrays using differential optical signaling," *IEEE J. Select. Topics Quantum Electron.*, vol. 9, pp. 361-379, March-April 2003.

[2] M. B. Venditti, and D. V. Plant, "On the design of large receiver and transmitter arrays for OE-VLSI applications," *IEEE J. Lightwave Technol.*, vol. 21, pp. 3406-3416, December 2003.

[3] A. S. Sedra, and K. C. Smith, *Microelectronic Circuits.* 4th ed., New-York, NY: Oxford University Press, Inc., 1998.

[4] Institute of Electrical and Electronics Engineers (IEEE), "IEEE standard for low-voltage differential signals (LVDS) for scalable coherent interface (SCI)," IEEE Std. 1596.3-1996, March 26, 1996.

[5] K. R. Shastri, K. N. Wong, and K. A. Yanushefski, "1.7 Gb/s NMOS laser driver," *in Proc. Custom Integrated Circuit Conf.*, 16-19 May, 1988, pp. 5.1.1-5.1.4.

[6] G. Gonzalez, *Microwave Transistor Amplifiers.* Upper Saddle River, NJ: Prentice-Hall, Inc., 1997.

[7] Taiwan Semiconductor Manufacturing Corporation (TSMC), "TSMC 0.18um mixed-signal 1P6M salicide 1.8V/3.3V RF spice models," Document no. T-018-MM-SP-001, March 5, 2002.

[8] Emcore Corporation, "10Gbit VCSEL oxide singlet specifications," Document no. 8585-8084, April 28, 2003.

4 Optical Transmitter Layout, Extraction and Simulation

Following the schematic-based simulations and design procedures presented in the last chapter, the optical transmitter was implemented in layout with Cadence Virtuoso™ tools. In the first section of this chapter, an overview of the layout techniques used to optimize performance is presented. This included substrate noise reduction, parasitics minimization, testing structures, output pad design and general floor-planning. The VCSEL modeling approach and results follows. Finally, simulations results including layout parasitics, VCSEL, package and fixture models are included.

4.1 Layout Approach and Techniques

Careful layout is always a key in achieving the expected performance for a specific design in any technology. All transistors wider than 2.5um in the optical transmitter were divided into multiple sections using a parallel-finger approach [1]. This insured that the substrate underneath the transistors is uniformly biased to the desired voltage, ground for NMOS and VDD (1.8V) for PMOS. Strong and uniform bias of the substrate reduces substrate noise considerably. This is illustrated in Figure 4.1 where the layout of the common-gate pre-amplifier is shown. The layout was made as compact as possible to reduce interconnect parasitics. In particular, the wide metal lines, carrying large amounts of current, were made as short as possible to reduce parasitic capacitance. The layout of individual sections of the optical transmitter were done independently and grouped afterwards to form the optical transmitter block. The power and ground rails were placed in a single spatial direction, forming stripes along the optical transmitter layout in a single direction, similar to techniques used in digital circuit cell layouts. The optical transmitter layout cell was encased in double guard rings, composed of alternating n-well and p-well regions. This structure is widely used in high-speed electronic design to isolate a section of the die substrate from elements outside the ring. This technique is used as another method for reducing substrate noise in the optical transmitter. In addition, the matching 100Ω differential resistor is implemented on-chip as a polysilicon-

based structure. With substrate noise reduction again in perspective, the resistor was deployed between the two guard rings, such that it is reasonably substrate-isolated from both the optical transmitter and the rest of the die. The optical transmitter layout, including the double guard rings, is shown in Figure 4.2.

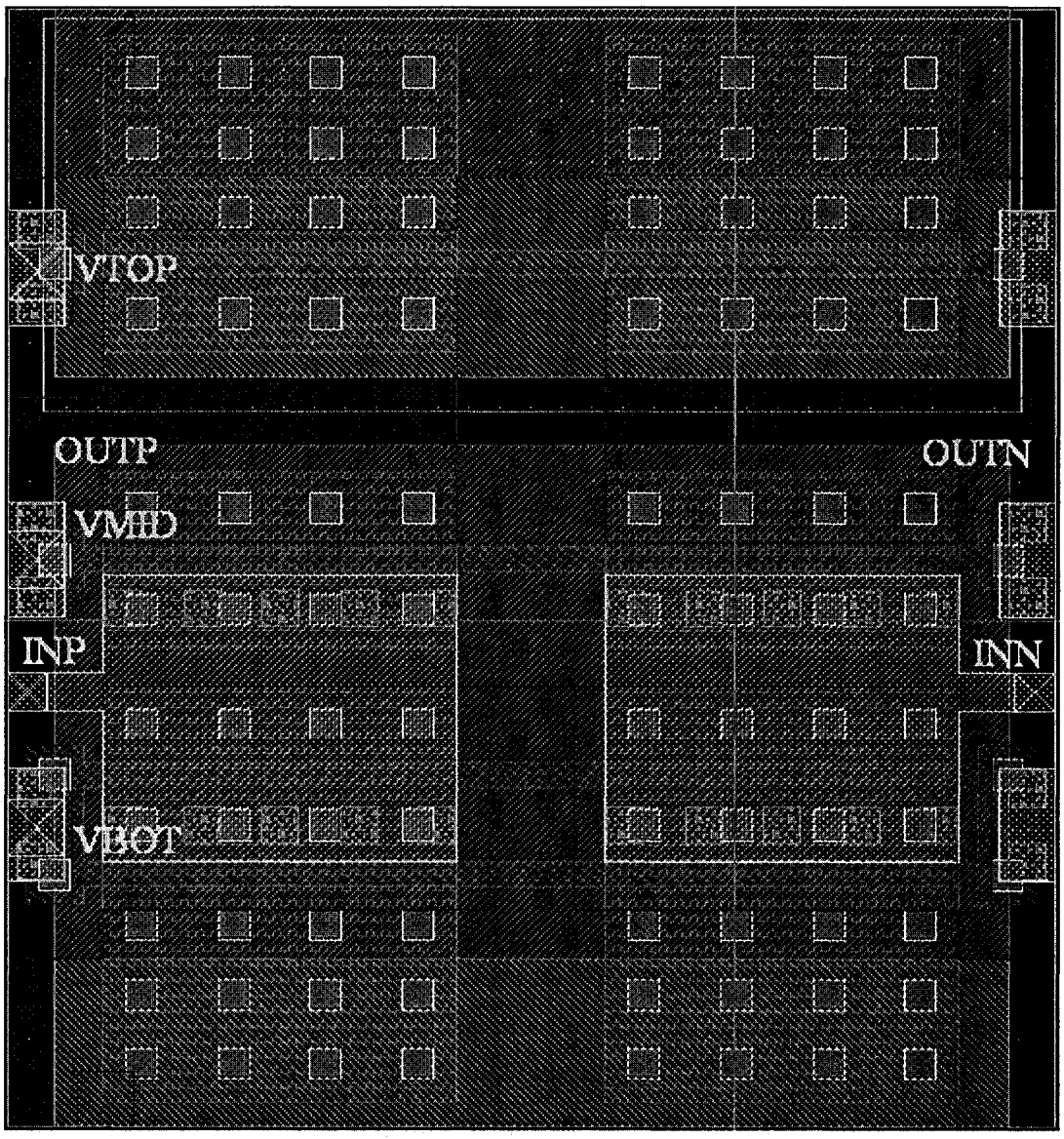


Figure 4.1: Common-gate pre-amplifier layout with pin names.

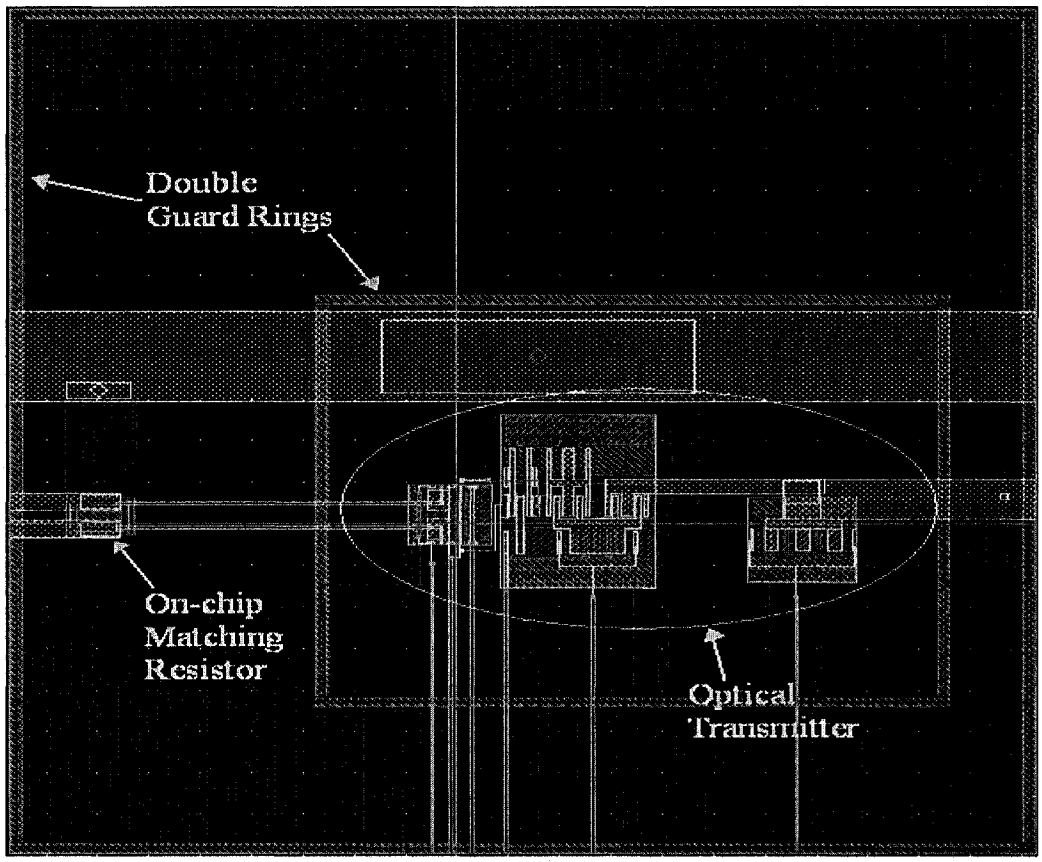


Figure 4.2: Optical transmitter layout with highlighted structures.

Two instances of the optical transmitter where implemented on a 1.45mm on the side CMOS die. The first version of the circuitry is fully adjustable through external voltage control. All biasing voltage ports are connected to the exterior through output pads. The second version is biased on chip to the simulated optimal voltage levels using simple circuits composed of several NMOS transistors connected in series. An example of such a circuit is illustrated in Figure 4.3 [2]. The size of the transistors is adjusted to yield the desired voltage level at the output port. This voltage generator topology is stable with respect to temperature, with variations in output voltage lower than 10% over temperature swings above 100°C. On the other hand, the output voltage is quite dependent on the transistor sizes such that process variations might have significant impact. In addition, the bias and modulation voltages are generated on-chip using the digital-to-analog converter (DAC) shown in Figure 4.4 [3]. The inputs can be set to either 1.8V (1) or 0V (0). By varying which inputs are 1s and which are 0s, the output

voltage varies between 0V and 1.8V. The inputs are scanned-in the chip using a digital scan chain composed of D-flip-flops and applied to the DAC. The output voltages for all possible input combinations for the modulation voltage DAC are shown in Table 4.1. Testing those circuits implemented on a fabricated chip will evaluate the reliability of the concepts proposed above.

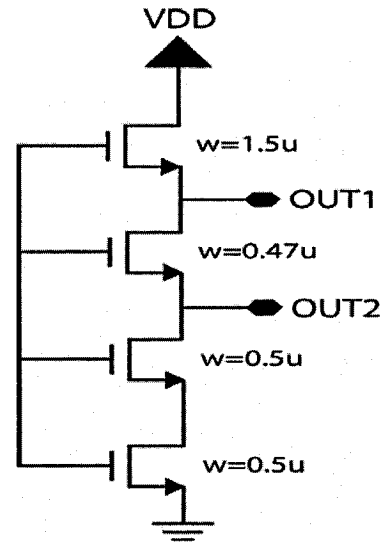


Figure 4.3: On-chip analog voltage generator.

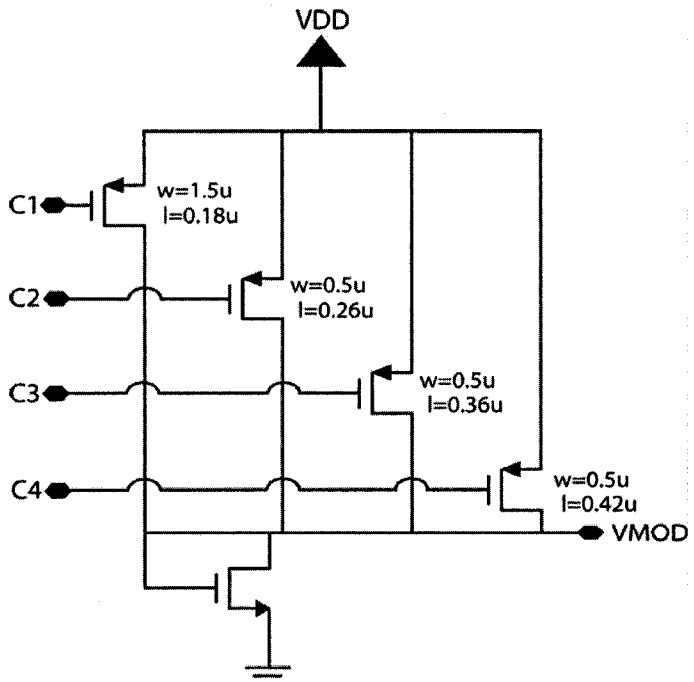


Figure 4.4: Digitally-controlled modulation current bias generator.

[C1 C2 C3 C4]	VMOD
[0 0 0 0]	1.48
[0 0 0 1]	1.46
[0 0 1 0]	1.45
[0 0 1 1]	1.42
[0 1 0 0]	1.45
[0 1 0 1]	1.41
[0 1 1 0]	1.40
[0 1 1 1]	1.36
[1 0 0 0]	1.12
[1 0 0 1]	1.02
[1 0 1 0]	1.00
[1 0 1 1]	0.87
[1 1 0 0]	0.93
[1 1 0 1]	0.79
[1 1 1 0]	0.76
[1 1 1 1]	0.03

Table 4.1: Output voltages for all digital input combinations of the modulation current bias generator.

The two instances of the optical transmitter, surrounded by their guard rings, were disposed in two opposed quadrants of the die. Surrounding the transmitters, a triple rail ring was implemented. The ring distributed the rail voltage levels uniformly around the chip. The exterior ring is biased to VCC (3.3V), the middle ring is grounded and the interior ring is at VDD (1.8V). The VCC ring can then be connected to the VCSEL die through an output pad and a short wire-bond. This novel approach to biasing VCSEL-based optical transmitters allows for substantial power consumption reduction, as it will be shown in the next chapter. The dual power rail ring allows for a limited use of the high voltage supply (VCC) to the VCSEL only. This results in approximately 50% power consumption savings for the rest of the optical transmitter.

A huge coupling capacitor is implemented in the middle of the die by superposing VDD and ground plates in two consecutive metal layers separated by silicon oxide. The parasitic capacitance of the structure filters high-frequency switching noise on the VDD rail to ground and helps keeping a clean supply voltage. Finally, the power supply rings are surrounded by input/output pads at the edge of the die. A layout view of the die, with highlighted structures and pad names, is provided in Figure 4.5. The scan chain pads used to control version 1 optical transmitter are located at the top (SCIN, CLK, RST, and SCO). The pads used to control version 2 optical transmitter are located at the bottom

(VBI, VMO, VSO, VG3, VG2, and VG1). There are several VCC, VDD, and ground pads to provide stable power rail levels to the chip. Only one version can be tested at a time. As a result, only half of the pads on the left and right sides of the chip are used at a time. The other half is ignored, such that the pad pitch is similar all around the chip. Interleaving pads in this fashion, we were able to implement two versions of the optical transmitter and have a sufficient number of pads to test them, even with a restricted chip perimeter. As with most analog experimental systems, the chip is pad limited in nature, such that we had to find ways to implement as many pads as possible with the chip size at our disposition. In addition, the inputs and output of both transmitter versions were made probe-able with a cascade coplanar ground-signal-ground 40GHz microprobe by adding ground pads on each side of inputs and outputs at a 150um pitch. As a result, the testing fixture can be bypassed and signals can be applied directly to the input pads if the fixture limits the performance of the system. Before giving simulations results of the extracted layout of the optical transmitter, a description of the modeling work on the VCSEL will be given in the next section.

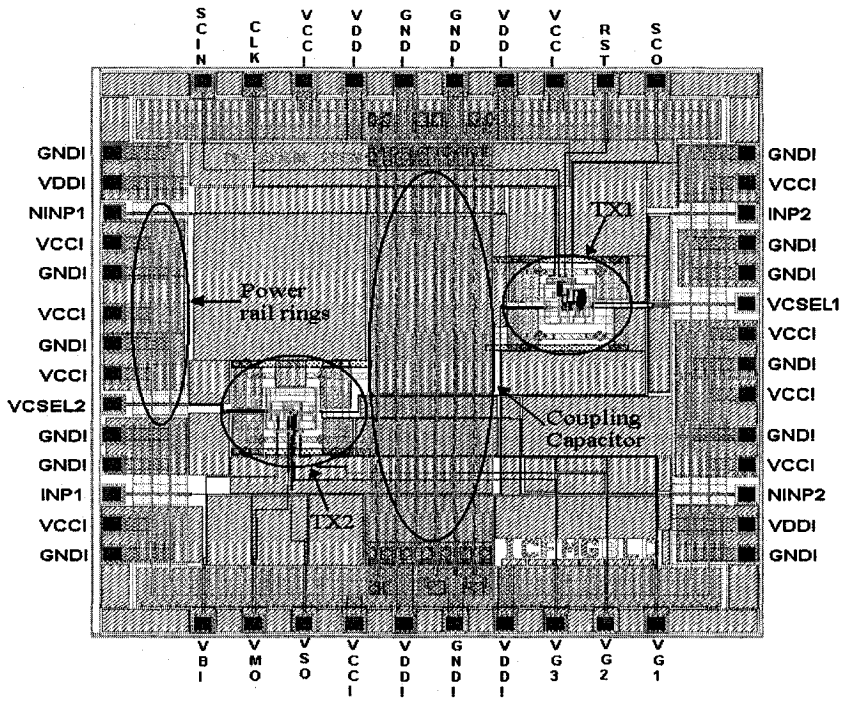


Figure 4.5: Optical transmitter chip layout with highlighted structures and pad names.

4.2 Bias-Dependent VCSEL Modeling

In order to obtain precise simulation results, and accurately predict the performance of the packaged optical transmitter, an accurate electrical model of the VCSEL must be developed for all biasing and modulation conditions. As the structural characteristics of the Emcore 10Gbps Gigalase VCSEL used for the system were not available, a modeling approach based on experimental measurements was adopted. The circuit topology of the electrical model is given in Figure 4.6, and is based on various model topologies previously published [4]. It includes pad capacitance and resistance, junction capacitance and resistance and two additional resistors to give more freedom in adjusting the model to experimental measurements.

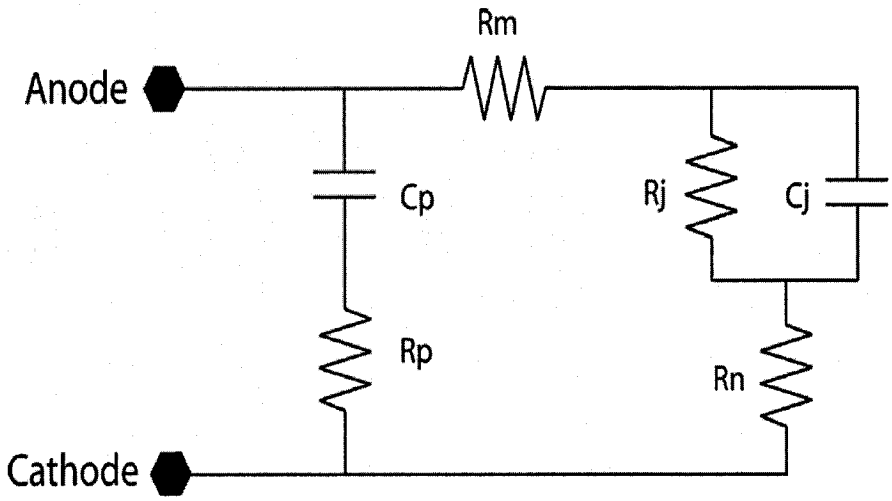


Figure 4.6: VCSEL electrical model topology.

An experimental setup was built to accurately measure the voltage versus current transfer curve and the reflection parameter (S11) versus frequency at multiple biasing currents. The S11 essentially embodies the impedance characteristics through frequency of the VCSEL as will be seen by the current driver of the optical transmitter. It is important to get accurate measurements of this figure to design a driver with predictable behaviour. A block diagram representation of the setup is shown in Figure 4.7. Several VCSEL dies were glued into a CFP80 package and mounted on a test fixture. The bottom of the carrier is biased to ground. The DC bias and high-frequency signal are combined with a bias tee and applied directly to the VCSEL using a 40GHz Cascade

coplanar microprobe. The bias current is measured with a Keithley multimeter, while the S11 measurements are conducted using the 8703B Agilent lightwave component analyzer. Measurements were taken on three different VCSEL dies in order to increase confidence in the experimental setup and test repeatability.

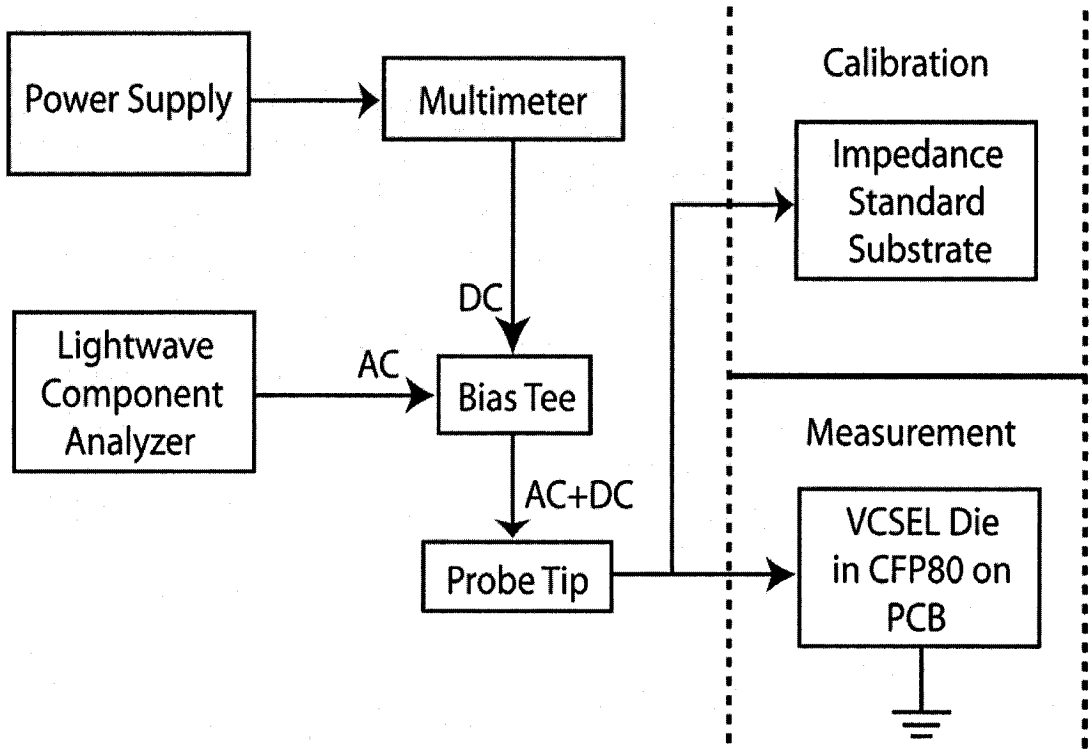


Figure 4.7: VCSEL test setup block diagram representation.

V-I curves were obtained for the three VCSEL dies and are shown in Figure 4.8. The three curves are extremely close and the average will be used subsequently to derive the electrical model of the VCSEL. In particular, the slope of the average V-I curve above threshold around four current levels were computed, using the least-squares error method, and are given in Table 4.2. These values represent the desired DC differential resistance of the electrical model at each bias current, easily calculated with Equation 4.1 through ohm's law. The pad resistance is excluded from the equation since the pad capacitor is open-circuited at DC.

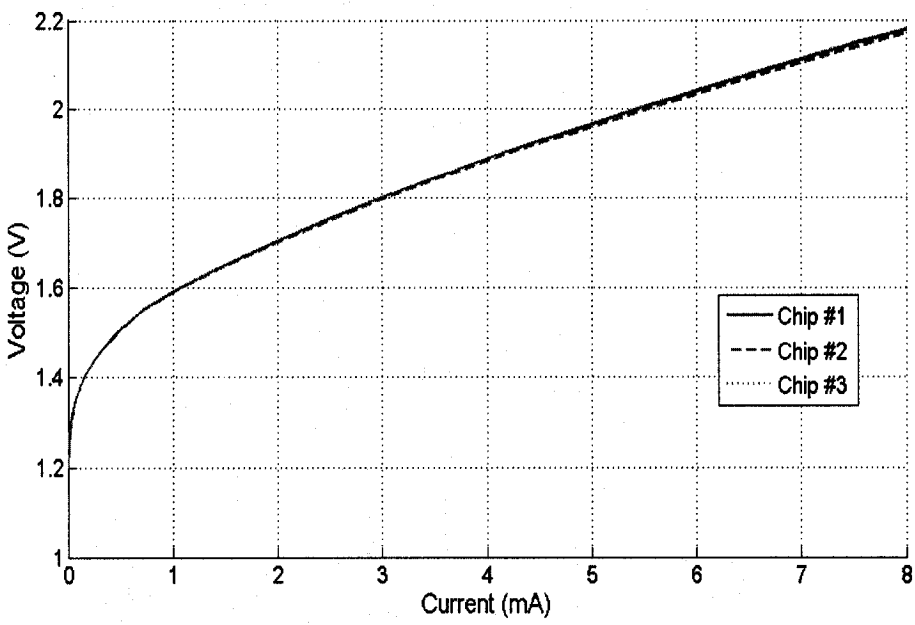


Figure 4.8: Measured V-I characteristics of three VCSEL dies.

Bias Current (mA)	Slope (V/mA)	δR_{DC} (Ω)
2	0.1034	103.4
4	0.0833	83.3
6	0.0731	73.1
8	0.0670	67.0

Table 4.2: Calculated VCSEL differential resistance at multiple bias currents.

$$\delta R_{DC} = Rm + Rn + Rj \quad \textbf{(4.1)}$$

The high-speed aspect of the electrical model is based on S11 measurements performed on the same three VCSEL dies. For bias currents of 2mA, 4mA, 6mA, and 8mA, the S11 parameter was measured between 50MHz and 20.05GHz in increments of 100MHz. The resulting measurements, along with the averaged S11 curve for each bias condition, are illustrated in Figure 4.9 to Figure 4.12. Obtaining accurate measurements up to 20GHz was challenging and special care was taken to isolate the test setup from external noise sources. In addition, calibration was conducted using an impedance standard substrate (ISS) to de-embed the cabling and probe parasitics.

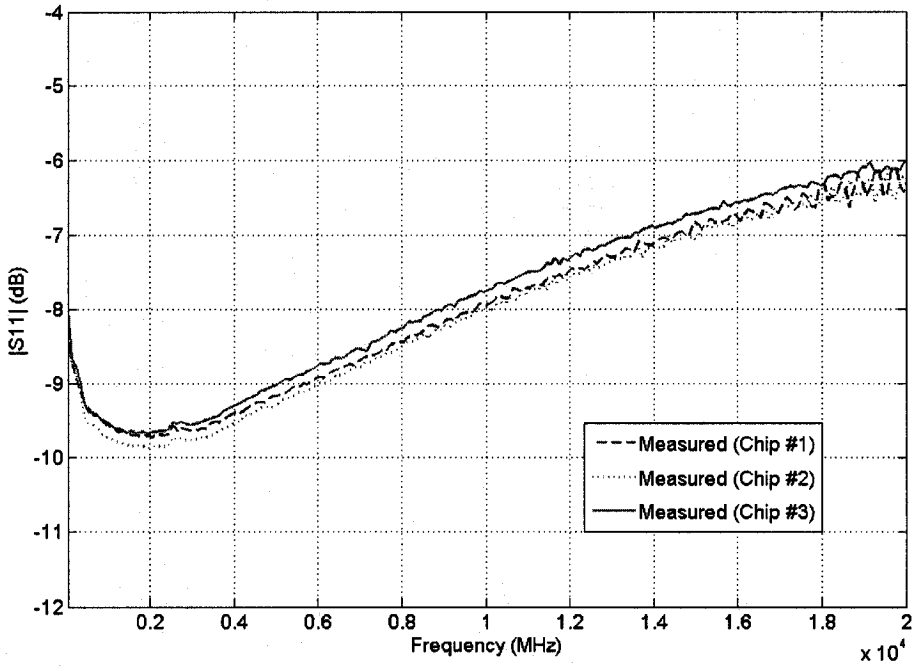


Figure 4.9: Reflection parameter measurements at 2mA bias current.

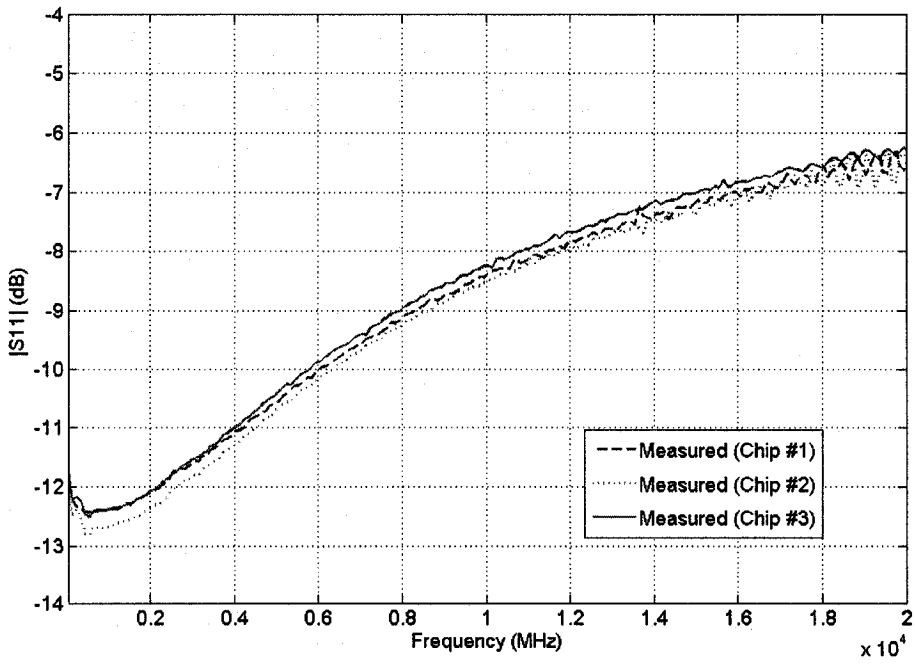


Figure 4.10: Reflection parameter measurements at 4mA bias current.

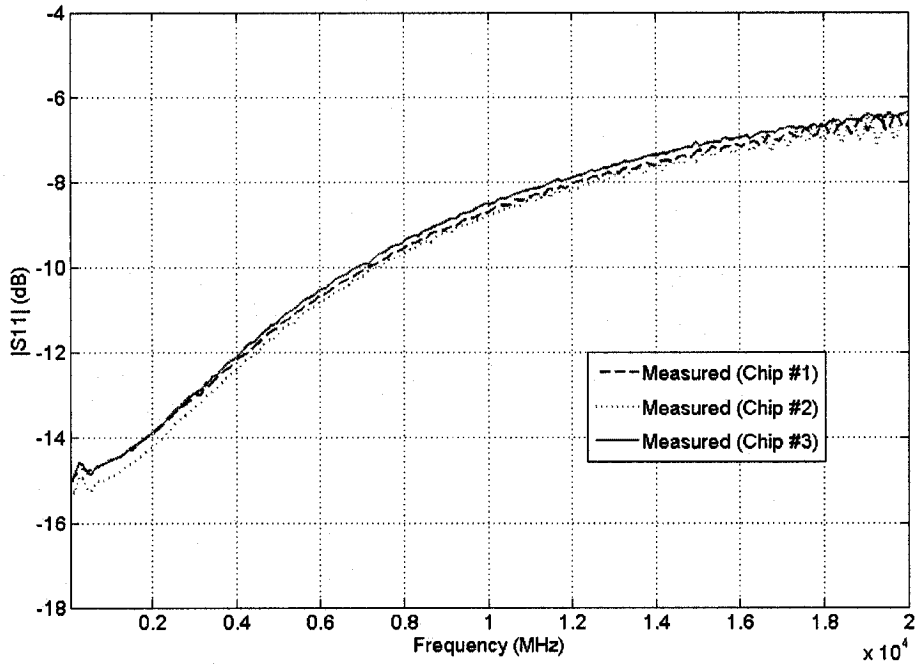


Figure 4.11: Reflection parameter measurements at 6mA bias current.

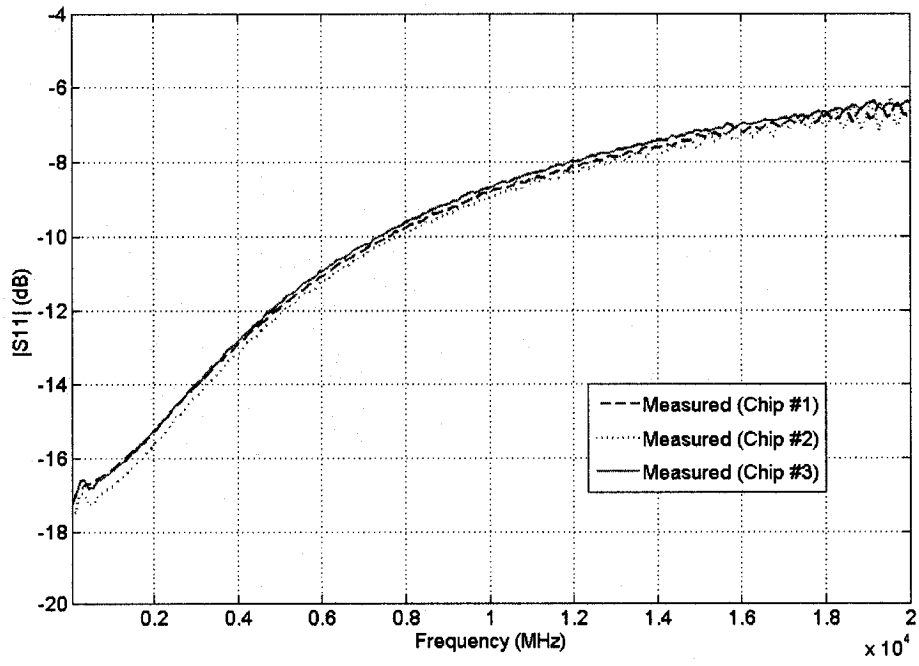


Figure 4.12: Reflection parameter measurements at 8mA bias current.

Using data from the averaged S11 curves and the V-I slope (embodying the differential DC resistance) at the four bias points, the electrical model resistor and capacitor values were derived using the Agilent Advanced Design Systems (ADS) simulation setup shown in Figure 4.13. This setup extracts the measured S11 in (A) from a sp1 formatted data file and tries to match the simulated S11 of the electrical model in (B) to the extracted value for all frequencies. In addition, it tries to match the differential resistance of the model, computed with Equation 4.1, to the experimental value taken from Table 4.2. This process is repeated manually for all four bias current levels under consideration. The model is optimized using both random and quasi-Newton search methods with the least-squares error function (C). Optimization is conducted until the total error function reduces below 0.02 (D), yielding a VCSEL model with reflection and differential resistance parameters almost identical to the experimental data. The resulting values for the electrical model resistors and capacitors are given in Table 4.3 for all biasing conditions considered.

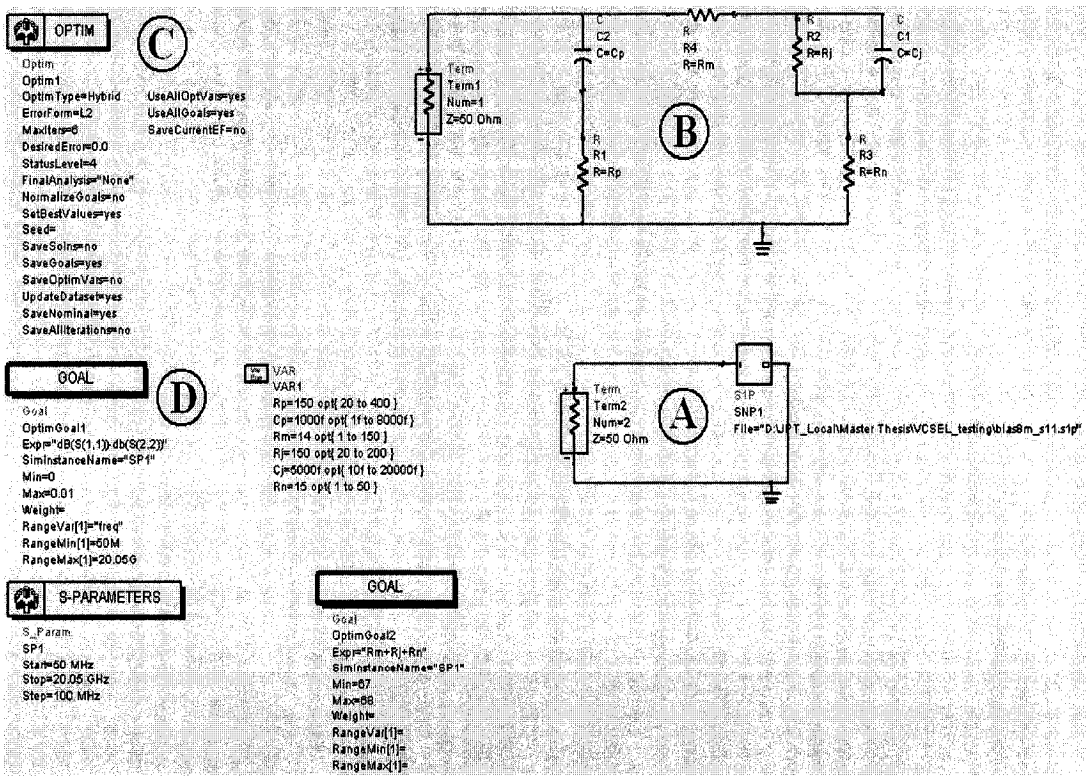


Figure 4.13: ADS VCSEL modeling optimizer.

Model Parameter	Units	2mA Bias	4mA Bias	6mA Bias	8mA Bias
Rp	Ω	40.76	27.04	146.58	391.38
Rj	Ω	84.66	50	55.88	51.25
Rn	Ω	9.51	30.54	16.12	14.74
Rm	Ω	9.83	2.46	1.00	1.00
Cj	fF	341.38	14177.1	504.10	490.55
Cp	fF	2572.4	268.49	520.03	139.03

Table 4.3: VCSEL model parameter values for all biasing conditions.

The S11 curves for the electrical model were computed using Equations 4.2 and 4.3 and plotted with the averaged experimental curves in Figure 4.14. Very good correlation can be observed between the model and the experimental data. The experimental and modeled differential resistance of the VCSEL at the various bias currents are summarized in Table 4.4. Again, the accuracy of the bias-dependent VCSEL model is demonstrated. At a particular frequency, a higher bias current means a higher reflection parameter. It is important to use the right curve in simulations to reproduce mismatch conditions between the driver and the VCSEL realistically and get accurate results. The electrical model presented in this section was implemented in the optical transmitter simulation model and the resulting performance predictions are presented in the following section. The 2mA bias current model was used for simulations as we plan to modulate the current between 2mA and 4mA.

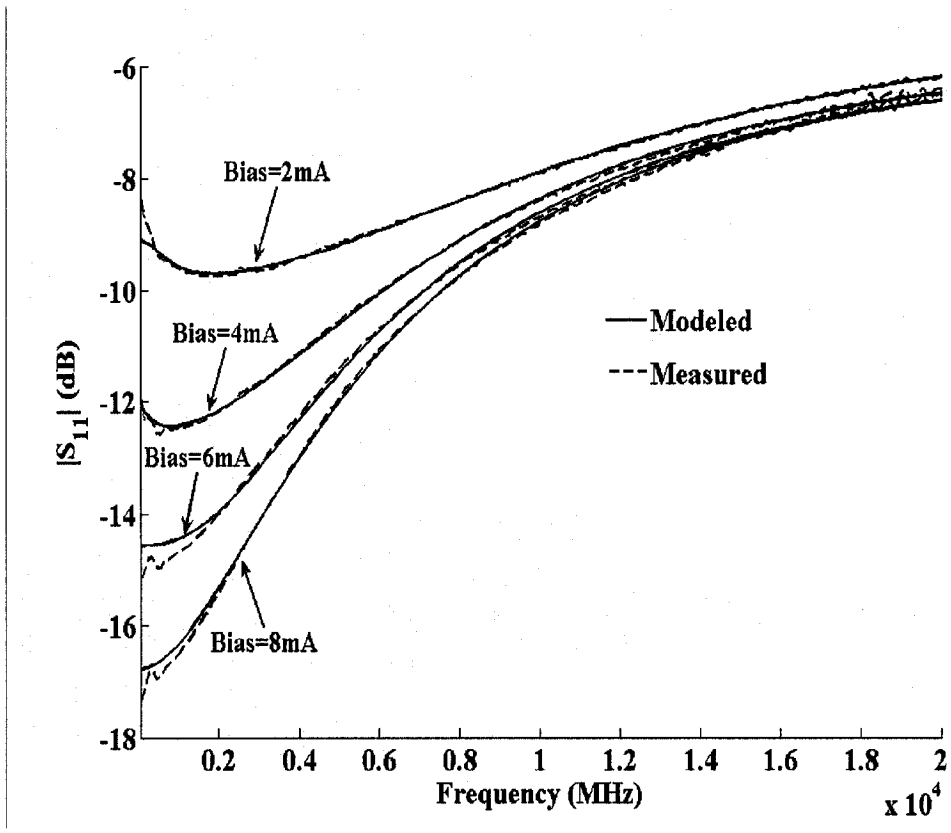


Figure 4.14: Comparison between modeled and measured reflection parameter curves at four bias currents.

$$Zin = \left\{ \left[\left(\frac{1}{Rj} + i\omega Cj \right)^{-1} + Rm + Rn \right] + \left[\frac{1}{i\omega Cp} + Rp \right]^{-1} \right\}^{-1} \qquad (4.2)$$

$$|S_{11}| = \left| \frac{Z_{in} - 50}{Z_{in} \_ 50} \right| \qquad (4.3)$$

Bias Current (mA)	Modeled δR_{DC} (Ω)	Measured δR_{DC} (Ω)
2	104.0	103.4
4	83.0	83.3
6	73.0	73.1
8	67.0	67.0

Table 4.4: Comparison of modeled and measured VCSEL DC differential resistance.

4.3 Simulation Results

The optical transmitter layout presented earlier was extracted with parasitic capacitances and included in a simulation bench. The expected testing environment was modeled as precisely as possible to obtain reliable simulation predictions. A block diagram including all elements of the simulator is shown in Figure 4.15. In addition to the optical transmitter die, the model for the VCSEL detailed in the previous section, models for the package and test fixture leads developed by CMC, and bond wire models are included. Also, a Verilog-A block was developed to generate eye diagrams from the simulated output bit stream. The code for this block is included in Appendix A. The bond wire model is based on the equations given in [9] and represents the parasitics of the bond wire with respect to its physical dimensions and its relation to surrounding structures. By entering the bond wire length, height difference between the starting and ending points, and height of the wire with respect the nearest ground plane, the model computes the parasitic inductance, capacitance and resistance of the structure. The package and test fixture leads are modeled as a distributed network of resistors and capacitors derived from measurements conducted by CMC. Two models are available, one for PCB short traces and one for long traces. According to the floorplan of the design, only long trace models were used.

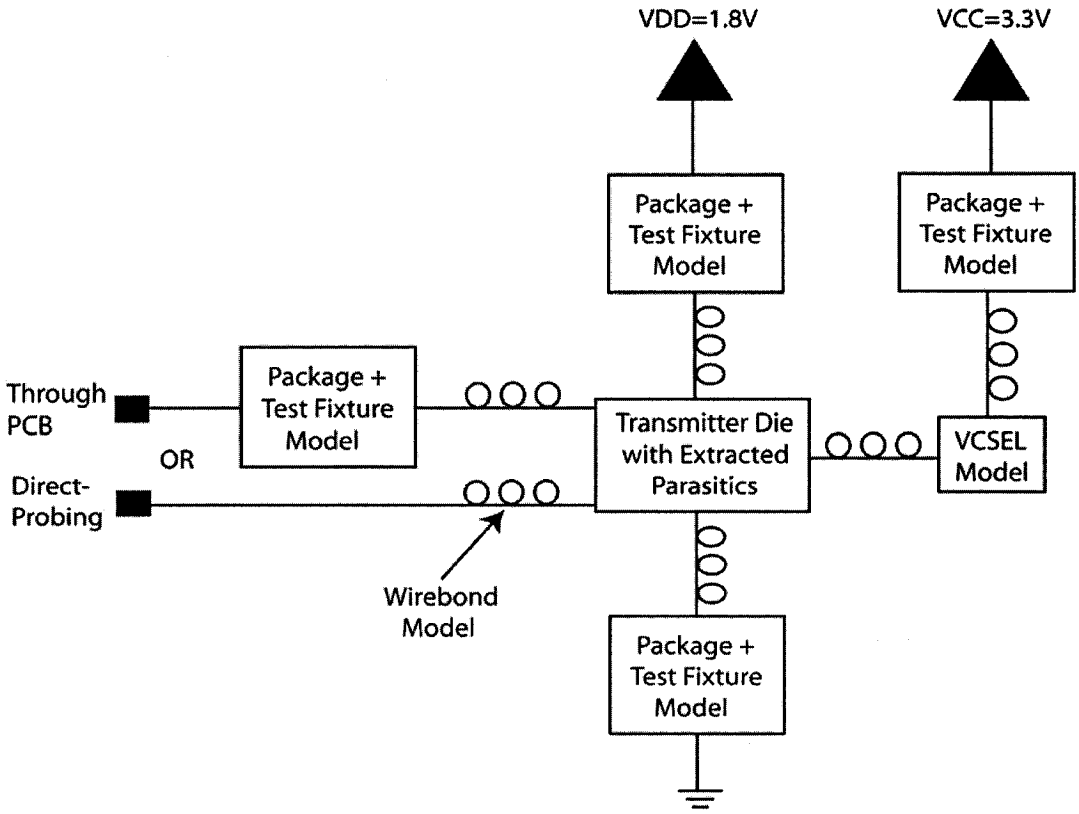


Figure 4.15: Block diagram of the optical transmitter simulation bench.

A complementary 2^{10}-1 pseudo-random bit sequence (PRBS) is fed to the differential inputs of the optical transmitter, either through the package and test fixture models or directly to the die inputs to mimic a direct-probing approach. The PRBS is generated in MATLAB and formatted in an appropriate Cadence stimulus file. The optical transmitter bias and modulation currents were set to 2mA and 4mA respectively. A bias current sufficiently high is needed to reach maximum performance for the VCSEL die, while keeping the bias current low minimizes power consumption. A bias current equivalent to two times the threshold current of 1mA is the minimum to reach multi-gigabit per second data rates. The modulation current was set at the highest possible level. A sufficiently high voltage swing at the receiver end is needed to perform bit-error rate (BER) measurements. A 4mA driver current swing yields a receiver voltage swing of approximately 200mV, giving sufficient headroom above the 50mV threshold of the BER tester for accurate measurements. Simulations were conducted at 2.5Gbps and 5Gbps with the input signals applied through the PCB or directly to the die. Eyes at

2.5Gbps for PCB and directly probed inputs are given in Figure 4.16 and Figure 4.17, respectively. A rise time of 130ps and a fall time of 120ps are observed at this data rate (direct-probing). Using the PCB at the inputs severely degrades performance, in particular with respect to timing jitter. Although it is still acceptable at 2.5Gbps, going to higher rates will require direct-probing. Performance at 5Gbps is evaluated through the eye diagram supplied in Figure 4.18 for directly probed inputs. The rise and fall time are now of 120ps and 110ps (direct-probing). A 5Gbps bit occupies a 200ps time slot, thus half the sum of the rise and fall times must be lower than this figure for correct operation. From this, we deduce that the optical transmitter operates near its maximum data rate at 5Gbps. On the other hand, noise might degrade performance in a real system below the maximum prediction, and an error-free data rate of approximately 4Gbps is a reasonable expectation for the implemented system. From simulations, the proposed optical transmitter is suitable for error-corrected 2.5Gbps optical interconnections, Gigabit Ethernet, or Ethernet passive optical networks (EPON). Reaching 10-Gigabit Ethernet operation would require scaling to smaller gate length CMOS technologies, which can be easily achieved.

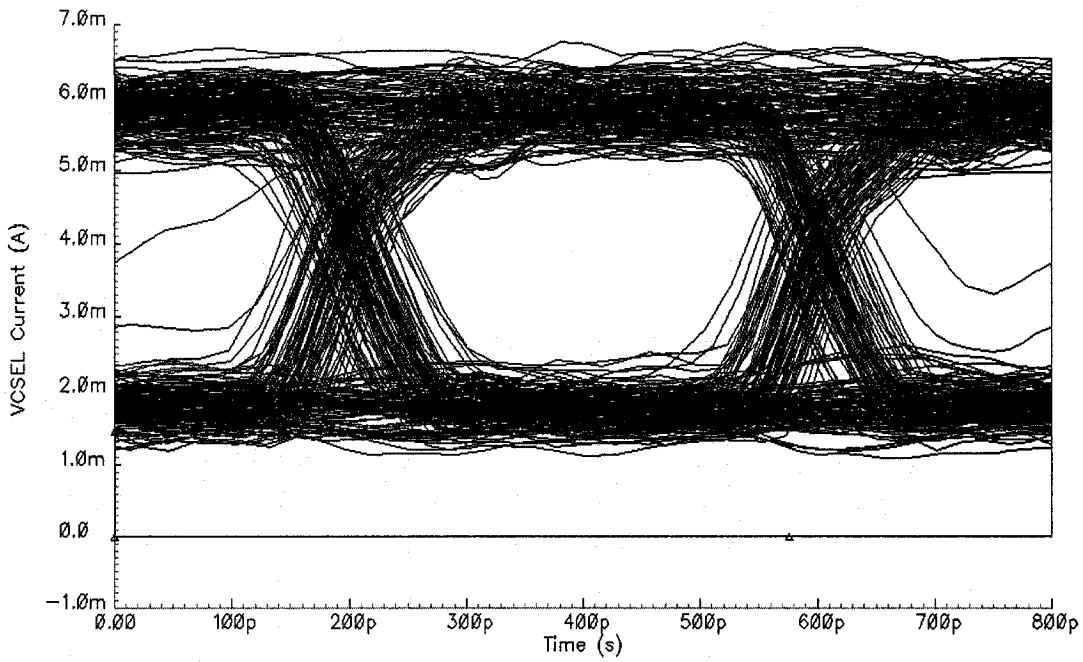


Figure 4.16: 2.5Gbps simulated eye diagram with inputs applied through the PCB.

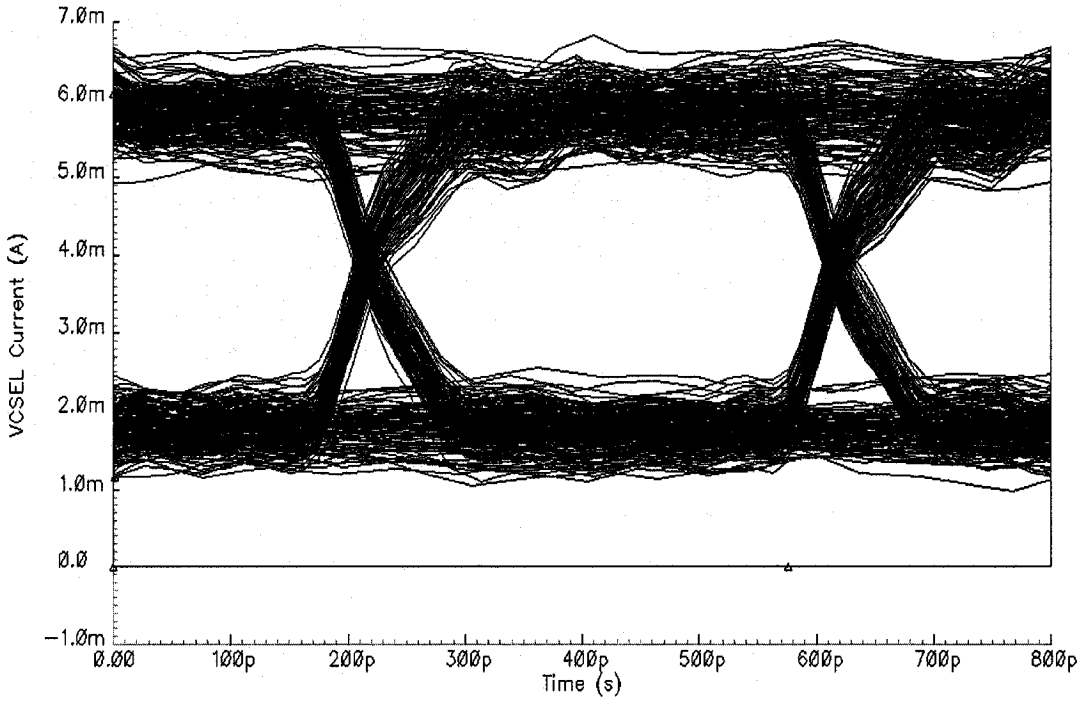


Figure 4.17: 2.5Gbps simulated eye diagram with directly probed inputs.

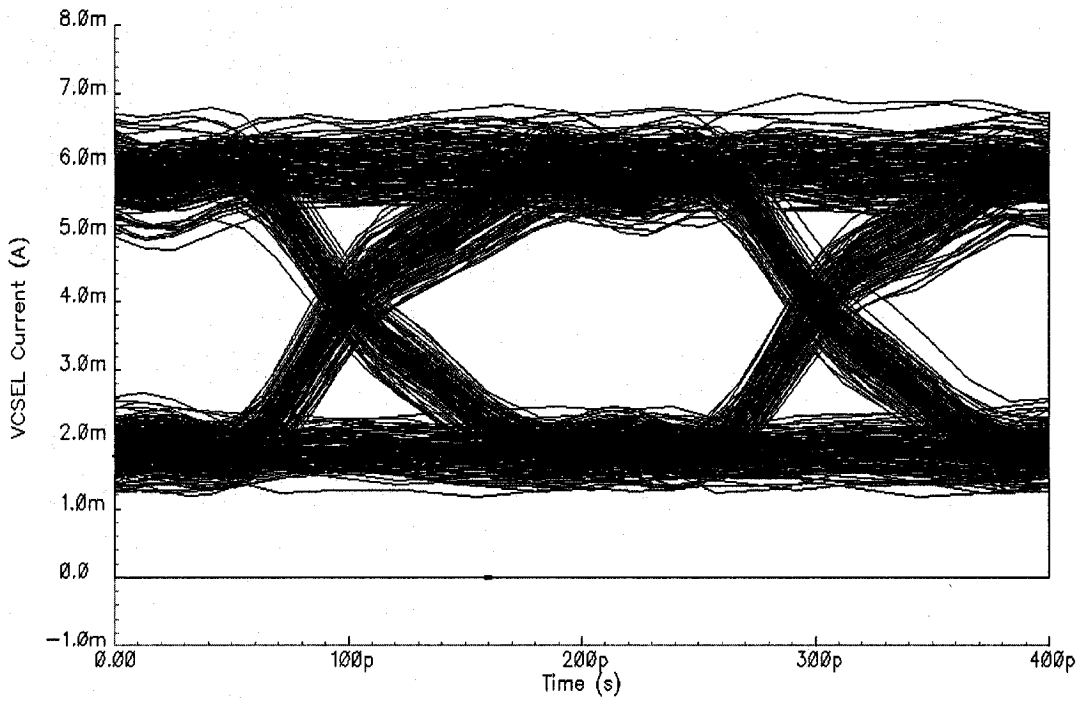


Figure 4.18: 5Gbps simulated eye diagram with directly probed inputs.

Under the previously stated simulation conditions, the optical transmitter consumes a total of 21.75mW, with 16.8mW coming from the VCSEL bias and modulation currents. This results in a pre-amplifier and pulse-shaping stage power consumption of 4.95mW. The total power consumption is independent of the data rate and is composed of 4mA from VCC (3.3V) and 4.75mA from VDD (1.8V). In the next chapter, the testing process of the optical transmitter will be described. The experimental results will be compared to the simulation results presented in this section.

4.4 References

[1] J. M. Rabaey, *Digital Integrated Circuits.* Upper Saddle River, NJ: Prentice-Hall, Inc., 1996.

[2] M. B. Venditti, E. Laprise, L. Malic, J. Schwartz, E. Shoukry, J.-P. Thibodeau, and D. V. Plant, "Design for testability and system level test for OE-VLSI chips," *in Proc. Optics in Computing Conf.,* April 8-11, 2002, pp. 144-146.

[3] M. B. Venditti, "Receiver, Transmitter, and ASIC design for optoelectronic-VLSI applications," *Ph.D. Dissertation,* McGill University, Montreal, QC, Canada, February 2003.

[4] D. Wiedenmann, R. King, C. Jung, R. Jäger, R. Michalzik, P. Schnitzer, M. Kicherer, and K. J. Ebeling, "Design and analysis of single-mode oxidized VCSEL's for high-speed optical interconnects," *IEEE J. Select. Topics Quantum Electron.,* vol. 5, pp. 503-511, May/June 1999.

[5] P. R. Brusenback, S. Swirhun, T. K. Uchida, M. Kim, and C. Parsons, "Equivalent circuit for vertical cavity top surface emitting lasers," *Electron. Lett.,* vol. 29, pp. 2037-2038, November 1993.

[6] M. Ochiai, K. L. Lear, V. M. Hietala, H. Q. Hou, "Modulation properties of high-speed vertical cavity surface emitting lasers," *in Device Research Conf. Digest,* June 23-25, 1997, pp. 102-103.

[7] D. H. Lim, S. M. Hwang, and S. H. Nam, "High-speed modulation of 850-nm vertical-cavity surface-emitting lasers", *in Proc. 14th Annual Meeting of the IEEE LEOS, November 12-13,* 2001, vol. 2, pp. 724-725.

[8] V. M. Hietala, K. L. Lear, M. G. Armendariz, C. P. Tigges, H. Q. Hou, and J. C. Zolper, "Electrical characterization and application of very high speed vertical cavity surface emitting lasers (VCSELs)," *in Microwave Symp. Digest,* June 8-13, 1997, vol. 1, pp. 355-358.

[9] G. Gonzalez, *Microwave Transistor Amplifiers.* Upper Saddle River, NJ: Prentice-Hall, Inc., 2nd edition, 1997.

5 Optical Transmitter Testing and Experimental Results

5.1 Experimental Approach

The optical transmitter CMOS 0.18um die was fabricated by Taiwan Semiconductor Manufacturing Corporation (TSMC) through CMC and delivered unpackaged. Similarly, the Emcore VCSEL dies were unpackaged for maximum flexibility. The experimental procedure was organized following the test process flow illustrated in Figure 5.1. Prior to evaluating the performance of the optical transmitter die, all other entities of the test setup must be characterized. More precisely, the VCSEL die properties must be evaluated. Most of this process was explained in detail in the previous chapter. In addition, the test fixture (PCB + package) performance is determined. This will help evaluate the necessity of direct probing at the input for maximum performance. Finally, the optical-to-electrical section of the setup must be built and evaluated. Following thorough evaluation, leading to increased confidence in the test setup, the optical transmitter is packaged with the VCSEL die and applied to the PCB through soldering or press-fit. The transmitter is incorporated in the test setup and performance is evaluated. Depending on the experimental results and their relation to simulation results, several iterations might be needed. Improvements to the test setup and/or control voltage levels can be introduced. In case of optical transmitter die failure, at the beginning or during the performance evaluation, the process must start over at the packaging step. As we will see in the following sections, this has occurred numerous times through the entire experimental process, due to the lack of robustness of the transmitter CMOS die. Implementing electro-static discharge (ESD) protection in the die pads would significantly increase robustness, probably solving this issue. In the next section, preliminary evaluations of the VCSEL die and test fixture will be given in detail. In addition, the two design iterations of the optical-to-electrical conversion setup will be detailed.

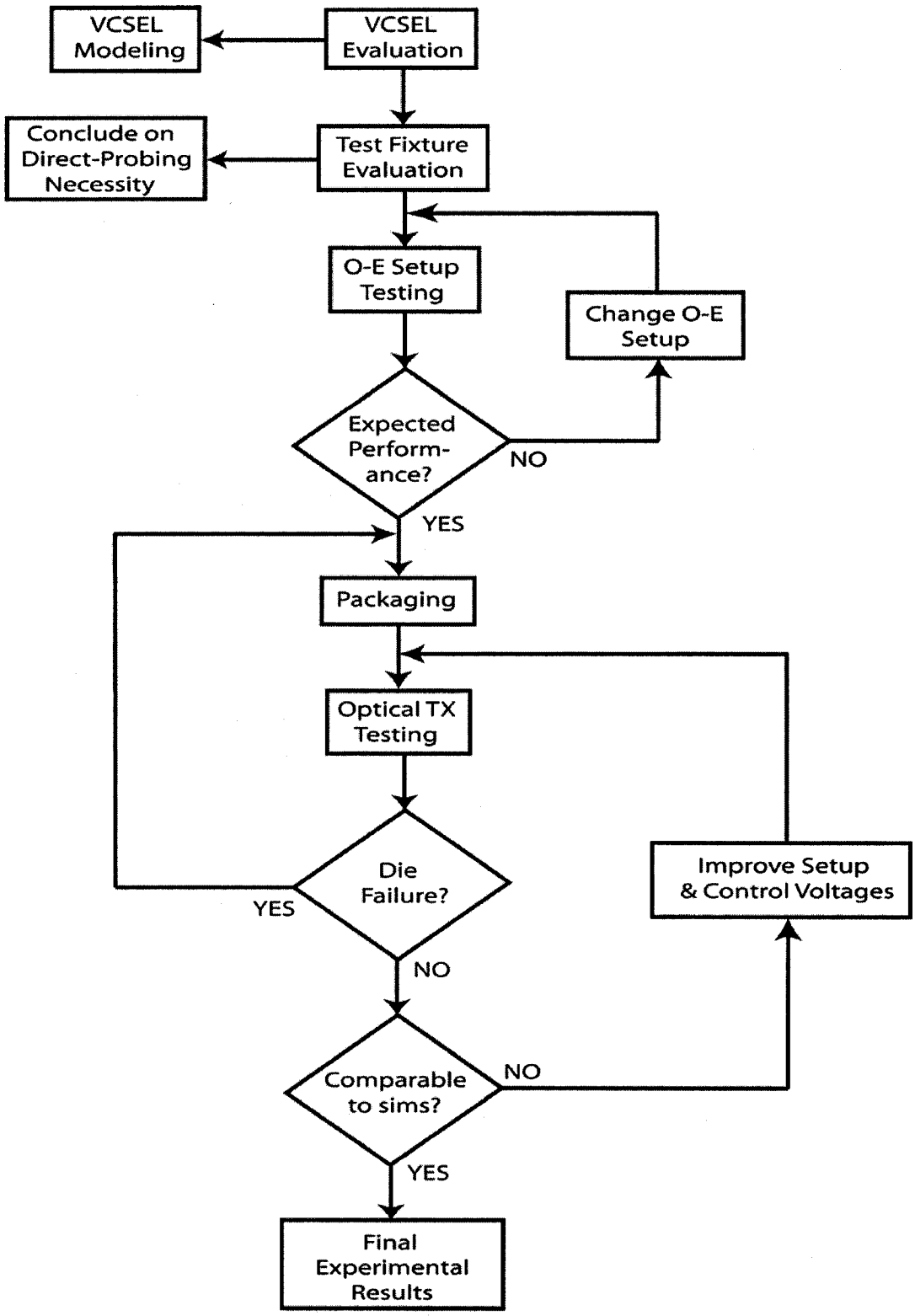


Figure 5.1: Testing process flow diagram.

5.2 Preliminary Testing and Evaluation

5.2.1 VCSEL Evaluation

Most of the VCSEL die testing procedure was discussed in Chapter 4. In addition to the S11 and V-I curve measurements previously presented, the L-I curve of three VCSEL dies was measured using the same setup in combination with a Newport optical power wand and power meter. The wand was mounted on a translation stage and brought as close as possible to the die to avoid clipping the beam edges and lose power. The resulting L-I curves are shown in Figure 5.2. These curves are essential for evaluating the efficiency of the optical-to-electrical conversion setups presented in section 5.2.3. From the curves, a slope efficiency of 0.53W/A and a threshold current of 0.8mA are observed.

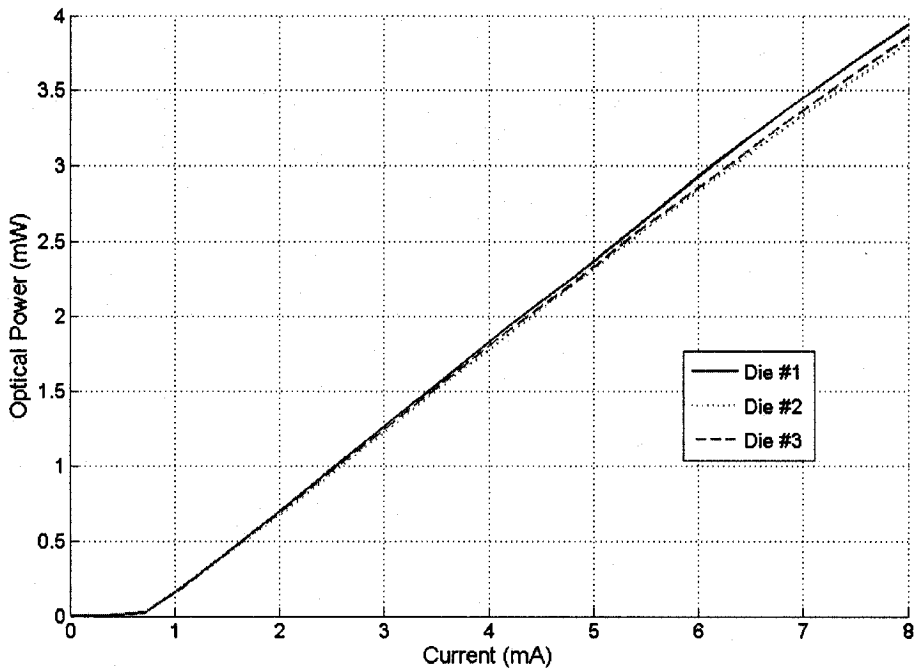


Figure 5.2: Measured L-I curve for three sample VCSEL dies.

5.2.2 Test Fixture Evaluation

The test fixture is composed of a generic PCB combined with an 80-pin ceramic quad-flat package (CQFP) provided by CMC. Models developed by CMC were used to simulate the test fixture in Cadence, as explained in Chapter 4. In order to evaluate the accuracy of those models, bond wires of various lengths were installed to join RF traces of the PCB together. A signal is applied to one RF trace, through the bond wire, and is received at the other RF trace port for measurement. The PCB has two types of traces, classified as short and long. For floor planning reasons, only long traces could be used for the optical transmitter design. A high-speed digital signal similar to the one applied to the optical transmitter was used to measure the performance of the test fixture. Bond wires of 0.5mm and 2.5mm were placed between long traces and measurements were taken for those two cases. Figure 5.3 and Figure 5.4 show the eye diagrams at 2.5Gbps for those two bond wire lengths. It is obvious from these measurements that even with a short bond wire, the test fixture performance is not sufficient for data rates above 2.5Gbps. The rise and fall times are too slow, timing jitter and ranging is significant. This validates the need for directly probing the inputs of the optical transmitter for achieving the limits of the transmitter die.

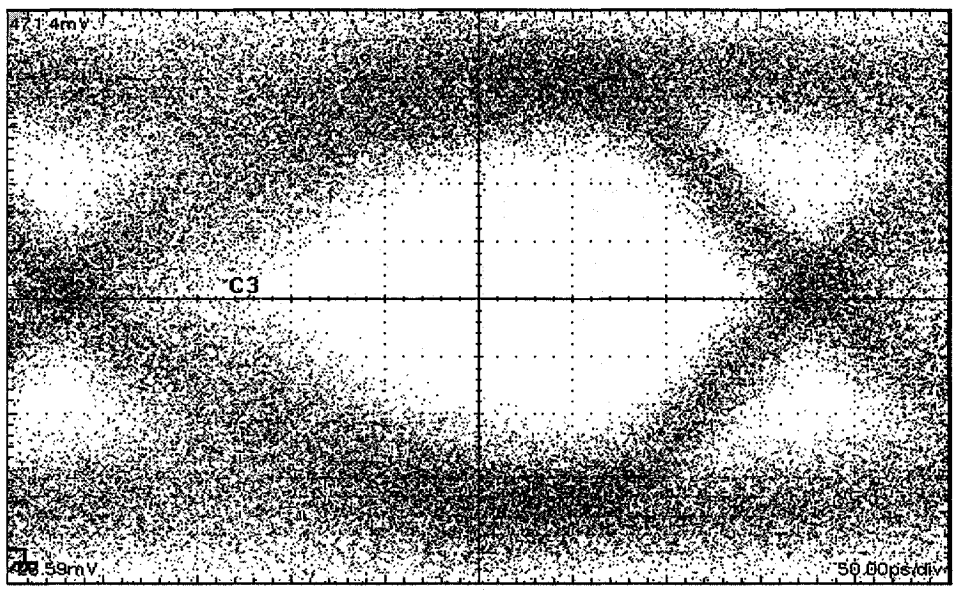


Figure 5.3: Test fixture evaluation eye diagram at 2.5Gbps with 2.5mm bond wire.

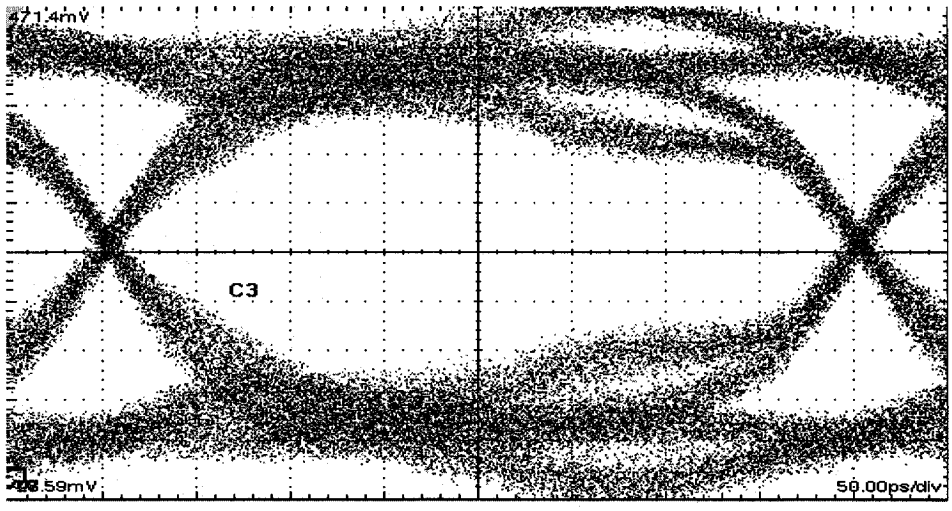


Figure 5.4: Test fixture evaluation eye diagram at 2.5Gbps with 0.5mm bond wire.

5.2.3 Optical-to-Electrical Conversion Setup Design and Test

The optical output of the VCSEL must be converted back to an electrical signal for evaluating the performance of the optical transmitter. Two setup options were considered for achieving the optical-to-electrical conversion. First of all, a free-space telecentric (4F) system was build with two microscope objective lenses [1]. As the VCSEL beam divergence angle is high (over 25 degrees), the objective had to be installed very close the VCSEL to minimize losses and keep the required objective aperture relatively small. Since direct-probing of the inputs is required, an objective aperture sufficiently small was needed to allow the probes enough physical space. An objective with a working distance of approximately 15mm and an aperture diameter of 15mm (50X objective with 0.45NA) is used to collimate the VCSEL beam. The collimated beam is focused to a New Focus free-space 12GHz photoreceiver with an active area diameter of 25um by a second microscope objective. This second objective has a 10X magnification, such that the beam spot size is theoretically 5 times bigger than the original spot size at the VCSEL, which is evaluated to be around 5um. As a result, the spot size after the free-space relay is the same as the photoreceiver active region size, yielding the best performance. A picture of the free-space relay is shown in Figure 5.5. The relay and free-space receiver were mounted on translation stages for alignment purposes.

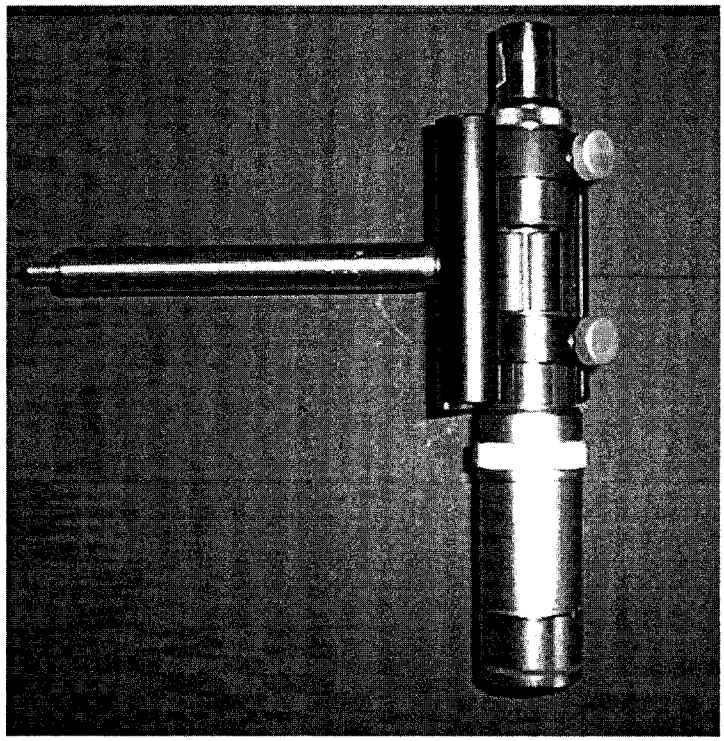


Figure 5.5: Picture of free-space telecentric system.

The performance of the free-space relay was evaluated by directly modulating a packaged VCSEL die and looking at the eye diagram outputted by the free-space photoreceiver. The eye diagram at 5Gbps is shown in Figure 5.6. The coupling efficiency is quite reasonable at 60%. On the other hand, the rise and fall times are around 150-175ps, which is more than 3 times greater than the quoted 30ps rise time and 45ps fall time in Emcore specification sheet. We hypothesized that this degradation was due to optical path differences within the free-space optical system or to reflections at interfaces within the system. Essentially, we suspected the optical setup to be the cause of this degradation. In order to verify this statement, a second optical-to-electrical conversion setup was considered.

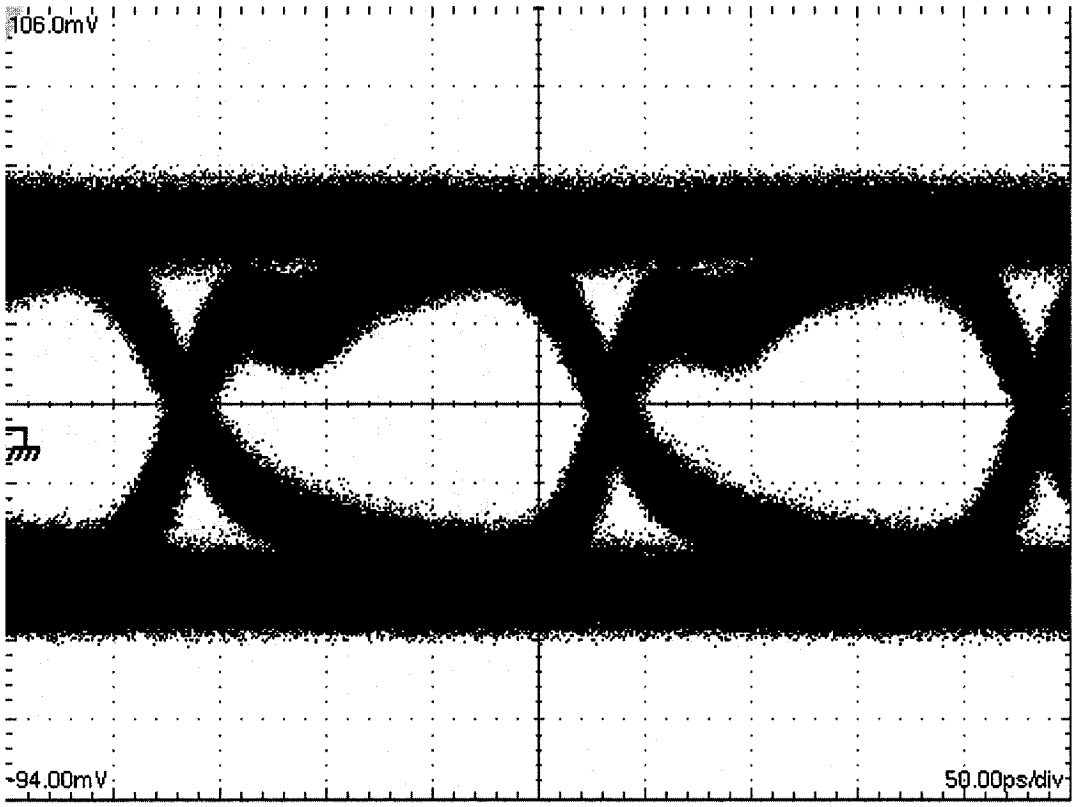


Figure 5.6: Directly-modulated VCSEL eye diagram with free-space setup at 5Gbps.

The second solution involves the butt-coupling of the VCSEL optical output into a 50um-core multimode fibre with a 0.25NA [2]. This number is slightly low with respect to the NA of the VCSEL such that radiation losses are expected. On the other hand, confining the beam to a 50um size should solve the issues related to the free-space setup. A fibre pigtail with a FC/PC connector at one end and cleaved on the VCSEL end was mounted in a Newport fibre holder (on a rail) and XYZ translation stage for alignment. The length of bare fibre extruding from the holder was kept as short as possible to eliminate vibrations-induced movements. The cleaved end of the fibre was aligned to the VCSEL output, with the help of a CCD camera at an angle, and brought as close as possible to the VCSEL surface without touching it (<10um). The link was evaluated through the same methodology as the free-space setup, the only difference being a fibre-connectorized 12GHz New Focus photoreceiver replacing the free-space photoreceiver. The eye diagram at 5Gbps is shown in Figure 5.7. A quick glance confirms the significant performance improvements of the fibre-based setup over the

free-space one. More quantitatively, the rise and fall times are now 90ps and 70ps, respectively, half of the free-space figures and not more than 1.5 times the quoted figures. As a result, fibre-based optical-to-electrical conversion will be used in the final test setup presented in the following section.

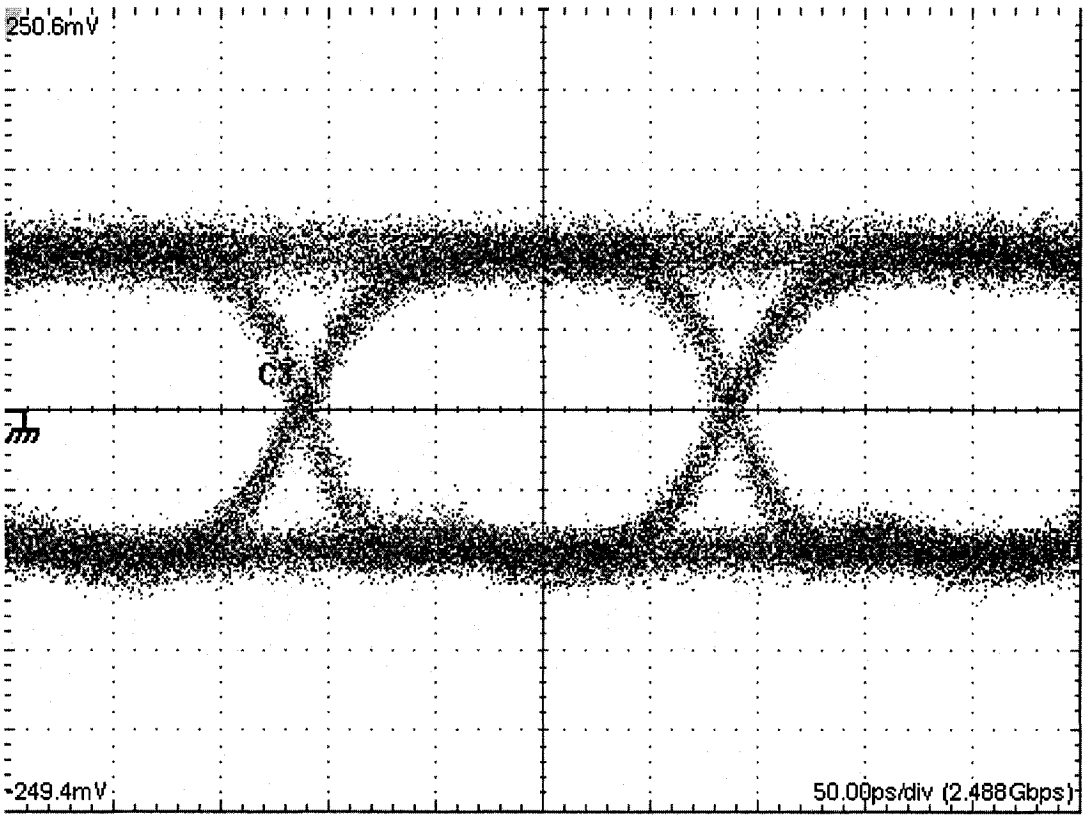


Figure 5.7: Directly-modulated VCSEL eye diagram with fibre-based setup at 5Gbps.

5.3 Final Test Setup

The transmitter and VCSEL dies were installed in an 80-pin ceramic quad-flat package with Epotek H20E conductive epoxy and wire-bonded with 0.17mil gold wire using an ultrasonic wirebonder. The package was soldered to the test PCB and mounted in the test setup shown in Figure 5.8 and illustrated in Figure 5.9. Other pictures of the setup, emphasizing on various aspects, are shown in Appendix B. The inputs were connected to a 12.5Gbps Anritsu pattern generator through SMA cables or Cascade coplanar ground-signal-ground microprobes, depending on the selected approach. Power

and control signals were applied to the board with multiple HP DC voltage sources. The fibre-based optical system was aligned grossly to the VCSEL using the bias monitor of the photoreceiver and optimized with a RF signal for maximum voltage swing at the output. Preliminary visual alignment of the probes and fibre was conducted using a CCD camera used in combination with a 4X microscope objective. The electrical output signal of the photoreceiver is measured with a Tektronix communication signal analyzer for eye diagrams and an Anritsu bit-error rate tester for BER measurements. The currents through the VDD and VCC power rails are measured with a Keithley multimeter.

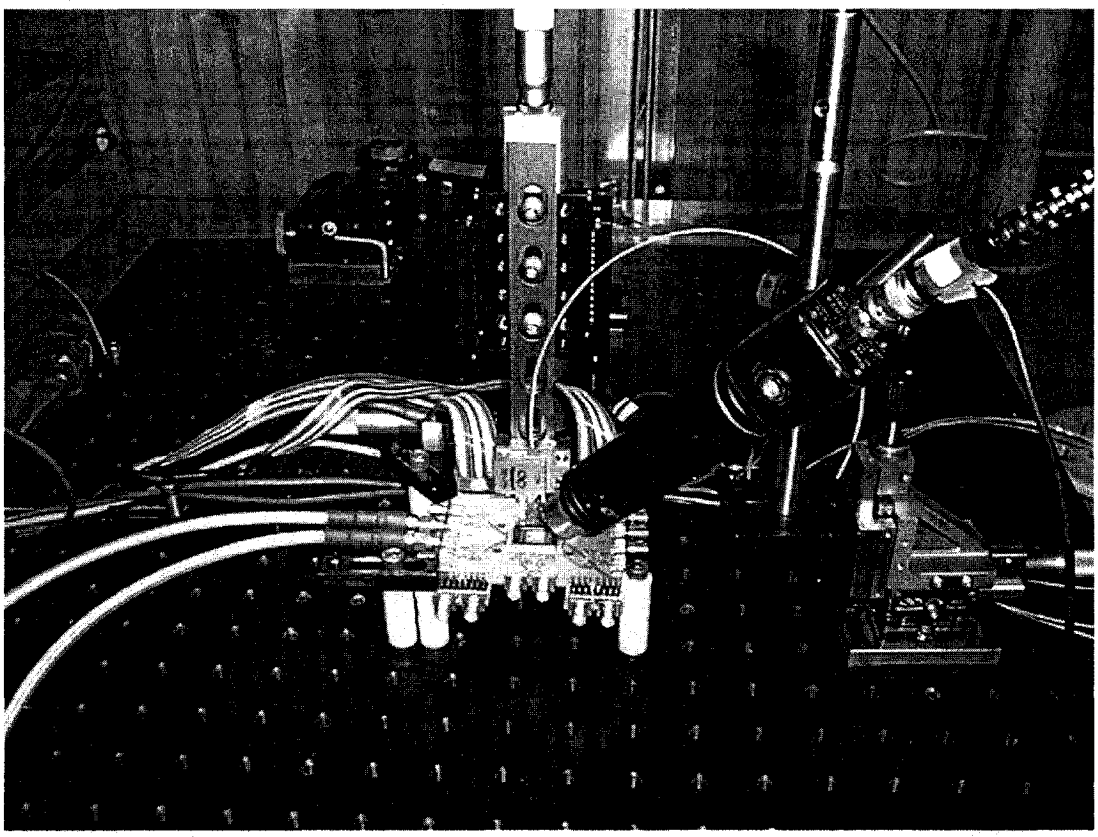


Figure 5.8: Picture of final experimental setup.

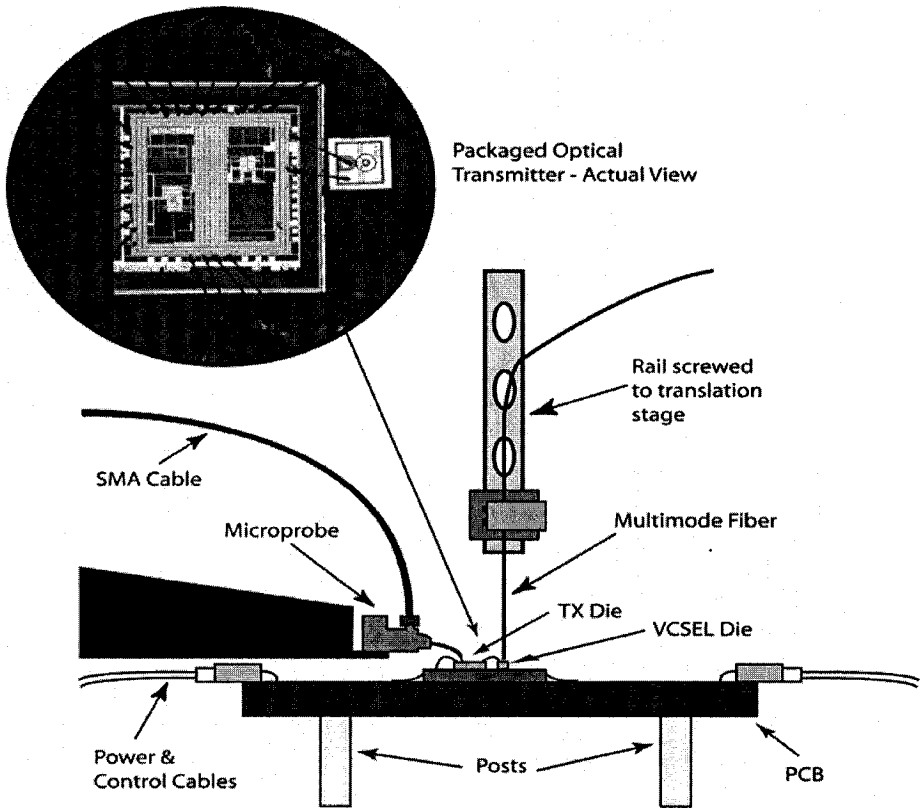


Figure 5.9: Illustration of the experimental setup pictured in figure 5.9.

5.4 Experimental Results

The testing was conducted on several optical transmitter dies for repeatability validation but also because the reliability of the CMOS dies was low. As electro-static discharge (ESD) protection was not implemented on the die pads, because of time constraints and performance issues, it was very easy the burn chips during various steps of the experimental process. This usually manifested itself by a short being created at the gate of the current source, effectively removing all control on the bias current level. This malfunction also appeared occasionally at other control transistor gates. The only solution to this problem was to be very careful in order to avoid ESD (grounding mats, straps, anti-static gloves) and replace the chip and package when the die under test burned out. A picture of the 15 optical transmitters tested for this thesis is shown in Appendix B.

The voltage control settings were adjusted constantly through the experimental procedure and those yielding the best eye diagrams and BER are given in Table 5.1. These are slightly different from the simulation values, as can be seen from the table. Many factors can explain this discrepancy, including process and temperature variation, losses in wires connecting the test fixture to the DC sources, and differences between the actual VCSEL and model at low frequencies (<50MHz).

Control Voltage	Experimental Value (V)	Simulation Value (V)
VBIAS	0.85	1.0
VMOD	1.8	1.8
VSHAPE	1.4	1.2
VBIAS (Pre-Amp)	0.8	0.8
VTOP	0.52	0.4
VBOT	1.38	1.2

Table 5.1: Experimental control voltages values and comparison with simulation values.

Experimental eye diagrams at 1.25Gbps, 2.5Gbps, 3.125Gbps, 4Gbps, and 5Gbps are shown in Figure 5.10 to Figure 5.14. All measurements were conducted using the direct-probing approach, following our conclusions regarding the performance of the test fixture. The rise and fall times are 180ps and 160ps, respectively, at 2.5Gbps. This is appropriate for operation at this data rate. Such figures tend to predict reasonably good BER performance up to 5Gbps. On the other hand, noise on the upper and lower rails is significant, such that the eye at 5Gbps in Figure 5.14 is significantly closed. Isolating the source of this noise is extremely difficult in practice. The noise on the ground rail was measured to be 50mV. Although this might not couple in its entirety to the output of the optical transmitter, the impact can be significant. The setup was moved to a Faraday cage to evaluate the possibility of the noise coming from electro-magnetic interference (EMI) coupling into the circuit and test fixture. Experiments show that the impact was negligible. As a result, we can say confidently that the noise comes from internal sources, not external interferers. Because of the dual power rail nature of the VCSEL driver, power rail bouncing and switching noise might be significant. In addition, the thickness of the upper and lower rails can result from ringing after the transitions. Low impedance mismatches at the SMA/microprobe/die interfaces or slightly different path lengths between the differential channels might induce such ringing. As this noise could

not be eliminated, BER measurements will show that good performance can be attained at 4Gbps. This is still very close to the simulated prediction of 5Gbps.

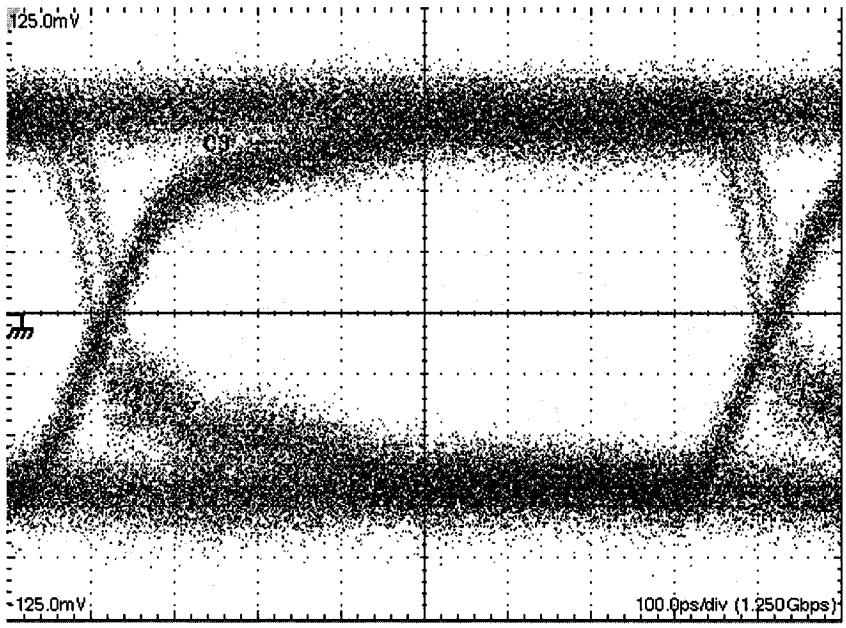


Figure 5.10: Optical transmitter experimental eye diagram at 1.25Gbps.

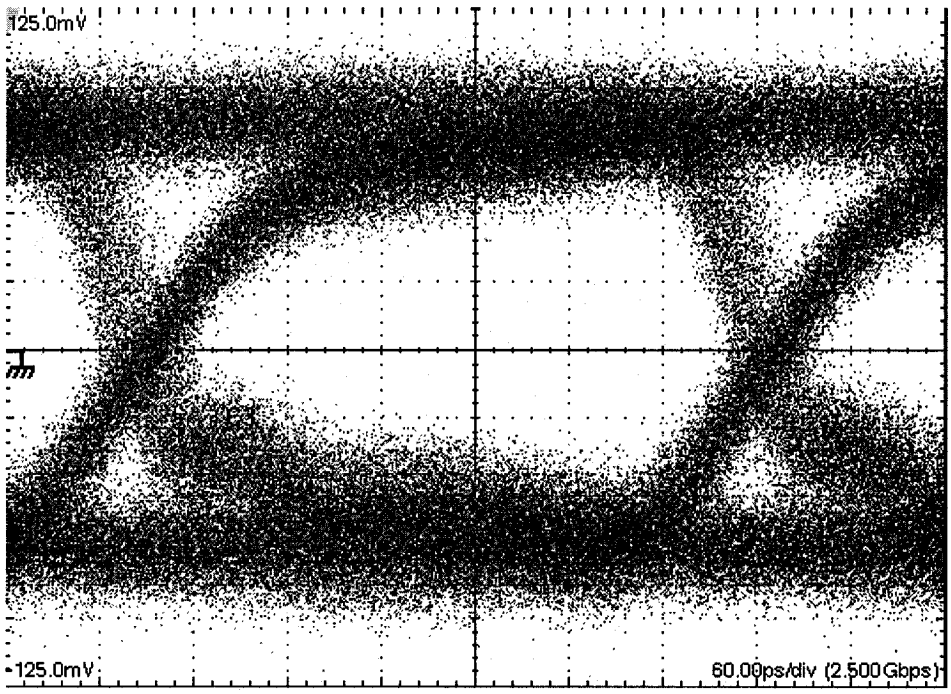


Figure 5.11: Optical transmitter experimental eye diagram at 2.5Gbps.

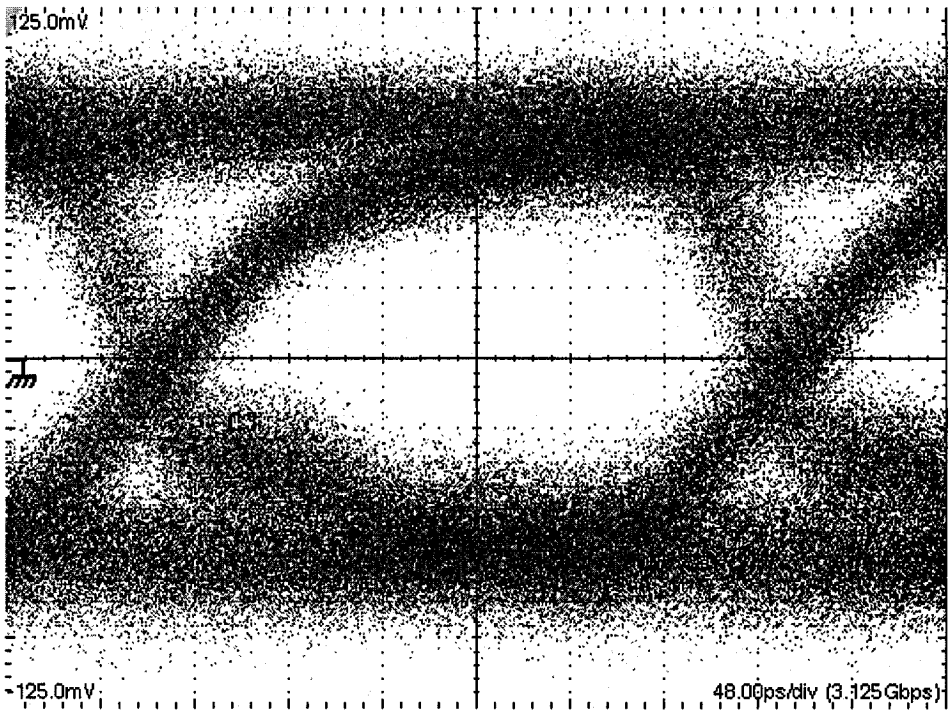


Figure 5.12: Optical transmitter experimental eye diagram at 3.125Gbps.

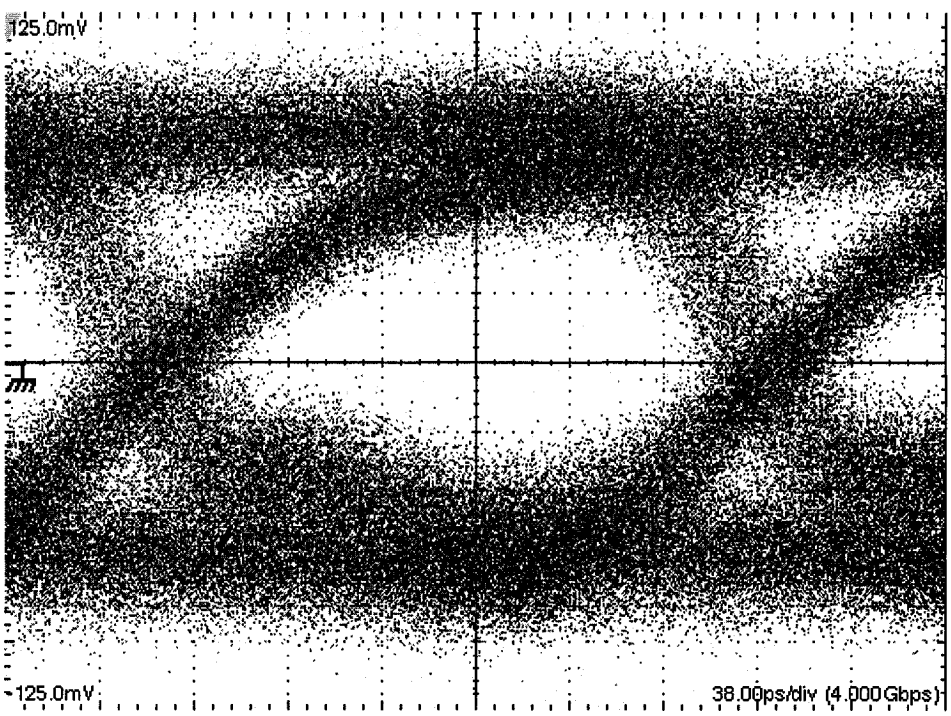


Figure 5.13: Optical transmitter experimental eye diagram at 4Gbps.

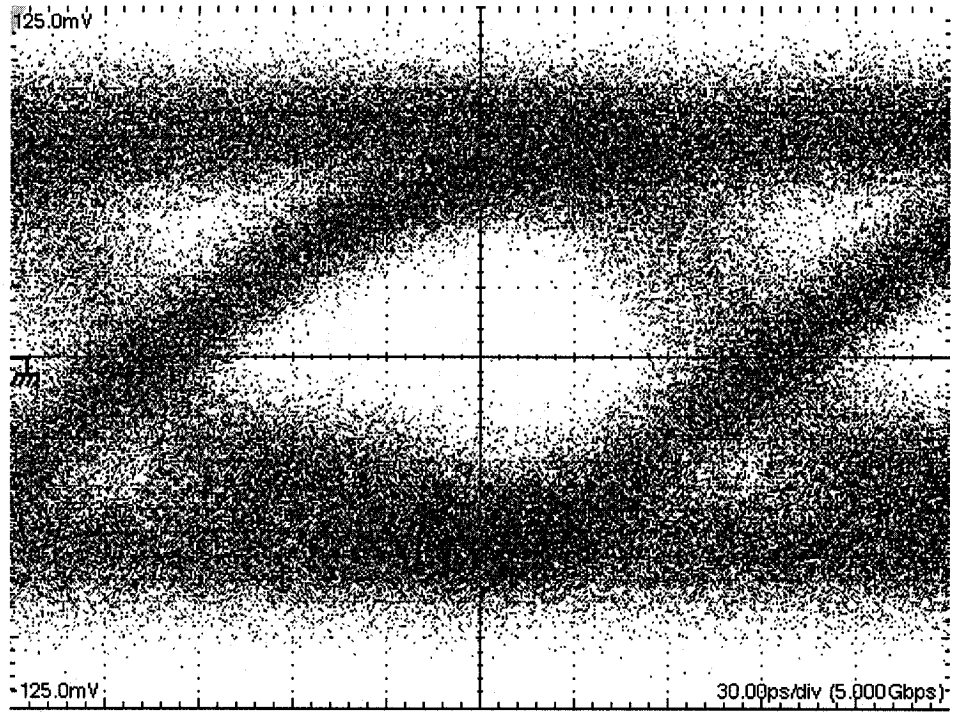


Figure 5.14: Optical transmitter experimental eye diagram at 5Gbps.

BER measurements were conducted at every bit rates given in the previous figures for various pseudo-random bit sequence (PRBS) lengths. The results are summarized in Table 5.2. Errorless operation is considered to be achieved when no errors are detected by the BERT in 10 minutes. This condition is fulfilled for bit rates as high as 3.125Gbps with a PRBS length of 2^{31}-1. As the bit rate increases above this value, the BER starts to increase steadily for the maximum PRBS length of 2^{31}-1. By reducing the PRBS length, the BER decreases by one to several orders of magnitude, as can be expected. At 5Gbps, a BER of $1x10^{-9}$ can be achieved with a minimum PRBS length of 2^7-1. This is the performance limit of the optical transmitter for useful transmission of data. The power consumption was measured simply by monitoring the DC currents pulled by the VDD and VCC power supplies. Because of the analog nature of the optical transmitter, the average current can be used with good precision to evaluate power consumption, as opposed to a digital circuit. All measured data is given in Table 5.3, and compared with the simulated figures. Because of the difference in control voltage levels between the simulation and experimental settings, the power consumption is also different. The biggest source of discrepancy comes from the lower bias current in

experiments compared to the simulations. If not for the difference, power consumption figures would be very close. Nevertheless, simulations predicted with reasonably good accuracy the power consumption of the optical transmitter.

Data Rate (Gbps)	PRBS Length	Bit Error Rate
1.250	2^{31}-1	Error Free
2.500	2^{31}-1	Error Free
3.125	2^{31}-1	Error Free
4.000	2^{31}-1	$<1x10^{-10}$
4.000	2^{15}-1	$<1x10^{-11}$
4.000	2^{7}-1	$<1x10^{-12}$
5.000	2^{15}-1	$<1x10^{-7}$
5.000	2^{7}-1	$<1x10^{-10}$

Table 5.2: Experimental BER for multiple data rates and PRBS lengths.

	Experimental	Simulation	Discrepancy (%)
VDD Current (mA)	4.50	4.75	-5.4
VCC Current (mA)	3.10	4.00	-25.4
Total Power (mW)	18.35	21.75	-16.9
VCSEL Power (mW)	13.35	16.80	-22.9
TX Power (mW)	5.00	4.95	1.0

Table 5.3: Optical transmitter experimental power consumption and comparison with simulations.

We have presented the experimental setup and performance results of the versatile optical transmitter. A maximum error-free bit rate of 3.125Gbps is achieved for a PRBS length of 2^{31}-1. For the same PRBS length, a BER $<1x10^{-10}$ is attained at 4Gbps. Finally, a BER of $1x10^{-10}$ at 5Gbps could enable the transmission of error-correction-coded data. The power consumption of the optical transmitter is extremely low with a total of 18.35mW drawn from the two power supplies. Of this figure, 13.35mW is consumed by VCSEL currents (bias and modulation) and only 5mW for remaining the circuitry.

Although good performance has been demonstrated, higher data rates should be achievable in the CMOS technology used for the presented optical transmitter. Given accurate RF models, it would be beneficial to use smaller transistor widths in some stages of the design. In addition, a high quality PCB with well filtered power and ground rails should help reduce noise in the system. Finally, a higher coupling efficiency at the fibre

interface through the use of 62.5μm core multimode fibre would allow the use of a smaller modulation current and potentially increase performance. Before concluding this thesis, additional potential applications for our versatile optical transmitter are detailed in chapter 6.

5.5 References

[1] D. V. Plant, A. E. L. Chuah, M. B. Venditti, and A. Isac, "0.18-um complementary metal-oxide semiconductor push-pull vertical-cavity surface-emitting laser driver operating at 2.5 Gb/s with symmetric rising and falling edges," *Applied Optics,* vol. 43, pp. 2730-2733, May 2004.

[2] R. Annen, and S. Eitel, "Low power and low noise VCSEL driver chip for 10Gbps applications," in Proc. 17th Annual Meeting of the IEEE LEOS, November 7-11, 2004, pp. 312-313.

6 System Integration Possibilities

6.1 Bursty Network Components Evaluation Bench

The suitability of our versatile optical transmitter for access networks and short-reach optical interconnects was demonstrated in the first three chapters of this thesis. All design choices were taken with those two commercial applications in mind. The resulting optical transmitter has great potential for other applications. In particular, the transmitter could be used for test and measurements of other components or systems. In this section, we demonstrate the potential of our transmitter for testing next-generation networks with bursty transmission profiles, such as the Agile All-Photonic Networks.

Most commercial optical transmitters are targeted at Synchronous Optical Networks (SONET), which transmit a steady flow of information. These transmitters have AC-coupled inputs, which poses a problem for bursty flows. A phenomenon referred to as baseline wandering occurs when the data flow is interrupted for a certain period in an AC-coupled system [1]. The AC coupling capacitor requires an amount of time roughly equivalent to one RC time constant to charge. During this period of time, the baseline of the data sequence varies exponentially until it reaches steady-state. This period of time can be quite long, in the microseconds range. This transition period renders data transmission error prone and unreliable for that interval. For systems such as SONET, this is not an issue as this transition occurs only once at start-up. On the other hand, bursty networks experience this transition every time one or several packet slots do not contain information. This leads to very erratic performance of SONET receivers in bursty networks [2]. The optical transmitter presented in this thesis is DC-coupled and does not suffer from this drawback. Consequently, it could be used efficiently to test bursty network components such as switches or burst-mode receivers.

An evaluation bench for bursty network components is outlined in Figure 6.1. A digital section composed of a controller, digital delay lines, multiplexers, and linear

feedback shift registers (LFSR) generates packets to be fed to our DC-coupled transmitter. This digital section can be implemented with the transmitter on a single mixed-signal die (as CMOS technology is used for the TX) or separately on a field-programmable gate array (FPGA) chip and connected to the optical TX with a custom-made PCB. Four channels are implemented to mimic a four user operation. The multiplexer switches between channels at defined intervals set by the controller. Each channel generates packets with bits that are either pre-programmed in on-chip registers or pseudo-randomly generated by LFSRs of various lengths. The controller also controls if certain packets contain information or not. In addition, delay lines can be adjusted to vary the delay between packets in order to test certain features, receiver lock acquisition time for example. The controller can also be connected to the optical TX control voltages to vary the amplitude between packets, to emulate path length differences in a network. This bench would be valuable tool for evaluating bursty network components like burst-mode receivers and optical switches.

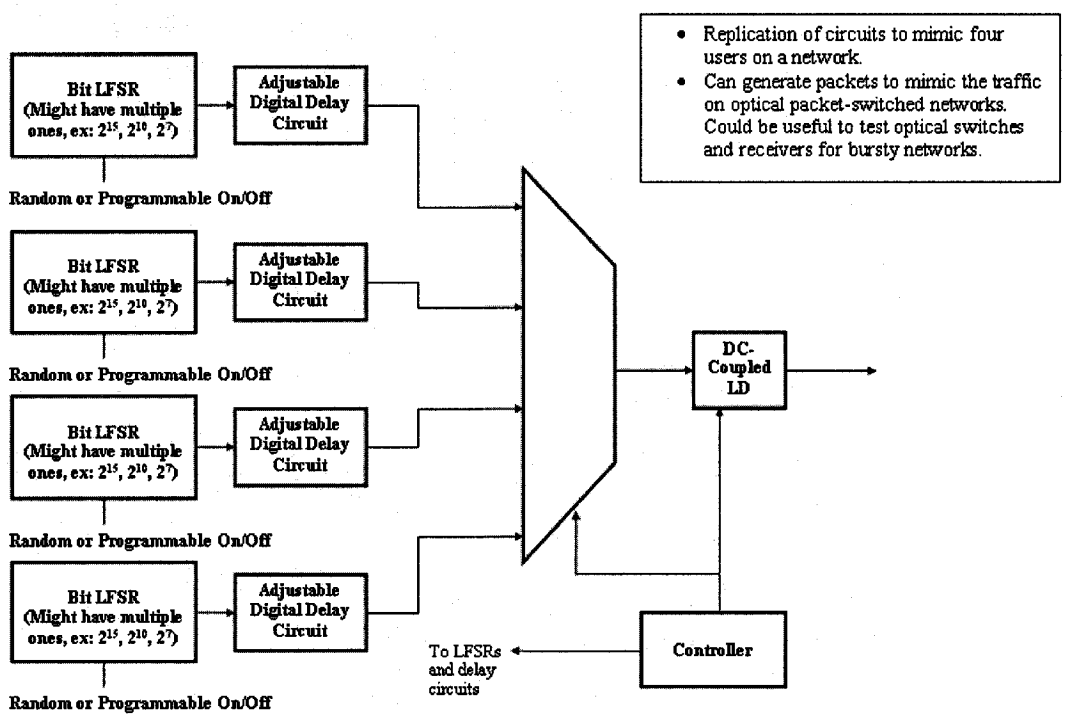


Figure 6.1: Versatile optical transmitter incorporated in a bursty network component evaluation bench.

6.2 Versatile Optical Transmitter-Based Bursty Network Demonstrator Proposal

A bursty network demonstrator based on our versatile optical transmitter and feedback from the burst-mode receiver in given in Figure 6.2. The same concepts of testability found in the previous section are applied in this proposal. We see electrical feedback from the burst-mode receiver as a solution to numerous issues and design complexities related to the implementation of bursty networks. As variable delay and intensity between packets can severely impact the performance of the receiver, we propose to displace some aspects of those problems to the transmitter through feedback, in order reduce the stress put on the receiver design. By feeding some information to the transmitter, delay and intensity variations can be reduced by dynamically controlling those parameters at the transmitter. Intensity feedback from the receiver would eliminate the need for automatic power control (APC) at the transmitter. In addition, it would account for system aging mechanisms and variations in optical path lengths. If VCSELs were used in such a network, this system would work around the lack of back-facet emission of those structures, a feature commonly used to implement APC for edge-emitting lasers [3]. Finally, it would compensate for seasonal temperature variations were the transmitter not encased in a temperature controlled environment. Phase delay feedback from the receiver could be used to potentially improve the locking time of the receiver.

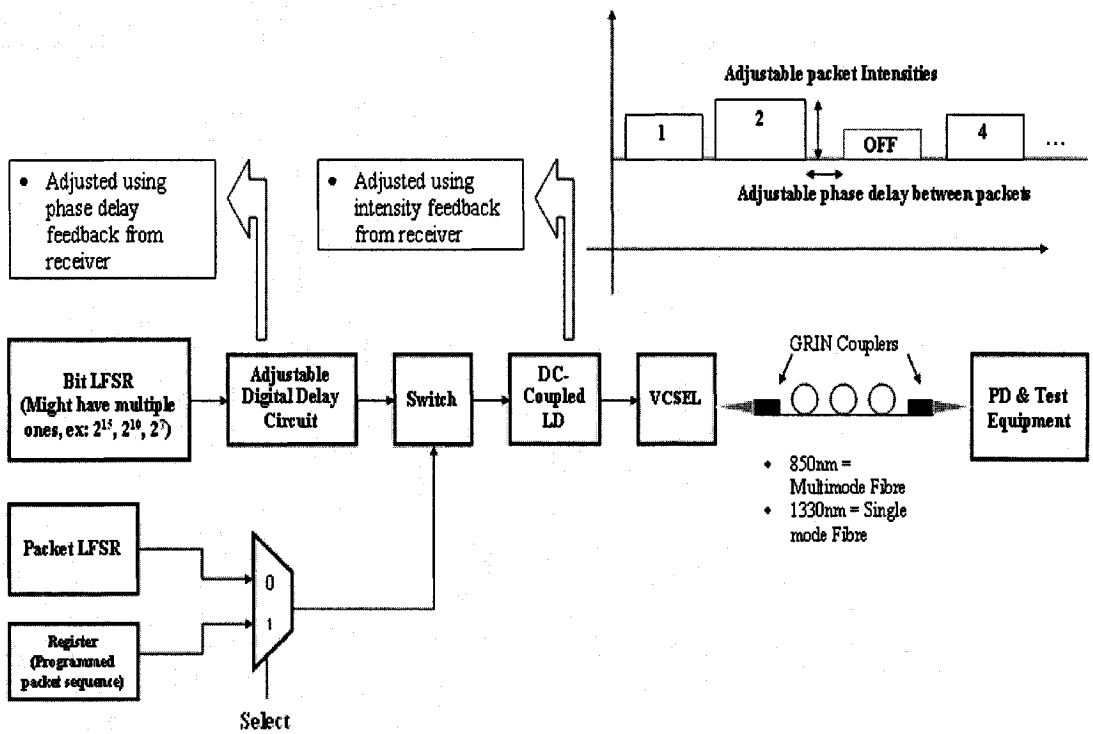


Figure 6.2: Block diagram of bursty network demonstrator proposal.

6.3 References

[1] Y. Ota, and R. G. Swartz, "Burst-mode compatible optical receiver with a large dynamic range," *J. Lightwave Technol.,* vol. 8, pp. 1897-1903, December 1990.

[2] J. Faucher, "Design and test of burst-mode receivers for optical multi-access networks," *Ph.D. Thesis Proposal,* McGill University, Montreal, QC, Canada, July 2003.

[3] E. Säckinger, Y. Ota, T. J. Gabara, and W. C. Fischer, "A 15-mW, 155-Mb/s CMOS burst-mode laser driver with automatic power control and end-of-life detection," *IEEE J. Solid-State Circuits,* vol. 35, pp. 269-275, February 2000.

7 Conclusion

7.1 Summary and Conclusions

This thesis investigated 850nm VCSEL-based optical transmitters design, layout, simulation and testing. Efforts were targeted at designing a versatile optical transmitter suitable for multiple applications, in particular optical access networks and short-reach optical interconnects. The main focus was to develop a low-power, low-cost, and multi-gigabit data rate optical transmitter for such applications. In addition, devising VCSEL electrical characteristics modeling approaches and VCSEL-based transmitter testing methodologies were important objectives.

Chapter 2 includes a broad literature review of optical transmitters. First, general characteristics and classes of optical transmitters were presented in detail. A discussion on the advantages and disadvantages of current and voltage drivers, single-ended and differential signaling (both optically and electrically), steering and switching drivers, and other considerations is given. Secondly, transmission line and edge-emitting driver designs are reviewed. This includes a discussion on cascode differential amplifier-based drivers. Finally, VCSEL drivers are investigated. In particular, current-peeking and push-pull approaches are described.

Chapter 3 outlines the numerous design choices related to the implementation of a versatile, low-power optical transmitter. The CMOS technology is characterized using transition frequency simulations and optimal bias points are determined. A detailed description of the design of the three optical transmitter stages, with simulations, transistor sizing, and diagrams is given. Preliminary simulation results at 2.5Gbps and 5Gbps are presented. Chapter 4 covers the layout and final simulation steps of the optical transmitter design process. Layout techniques used for noise reduction and parasitics reduction are presented. A novel layout approach with dual power rail rings for reduced power consumption is also given. By isolating the use of a high power supply (3.3V) to

the VCSEL port, power consumption is reduced by approximately 25%, as opposed to the common approach where the high power supply is used for the entire optical transmitter. On the other, this approach possibly increases power rail noise. A detailed procedure for modeling VCSEL electrical characteristics based on reflection parameter and I-V curve measurements is outlined. The resulting bias-dependent VCSEL model is presented. Finally, the final optical transmitter simulation bench is described in detail. This includes models for the test fixture (PCB and package), wirebonds, and extracted CMOS die layout. Simulation results at 2.5Gbps and 5Gbps are presented.

Chapter 5 describes in length the experimental process used to evaluate the performance of the optical transmitter and compares the measurements to the simulations. Additional VCSEL characterization, as well as experimental evaluation of the test fixture is given. Two optical-to-electrical conversion setup options are evaluated and results are shown. In particular, the butt-coupled multimode fibre-based setup is selected, showing efficiency above 60% and no apparent degradation of rise and fall times. Finally, experimental results are given. The optical transmitter operates up to 3.125Gbps error-free and to 4Gbps with a BER $<1x10^{-10}$ with maximal length PRBS. Power consumption is measured at 18.35mW in total, with 13.35mW coming from VCSEL modulation and bias currents. This is significantly lower than all VCSEL drivers reported in literature, regardless of the technology.

Chapter 6 considers additional applications where the versatile optical transmitter could be used efficiently. This includes a bursty network components evaluation bench and a bursty network transmitter demonstrator. High-level diagrams and discussions of those two proposals are given.

7.2 Future Directions

The present thesis has generated several tools, both in simulation and experimental settings, for developing VCSEL-based optical transmitters. This knowledge base can be used to further develop this research theme in the Photonic

Systems Group at McGill University. Higher data rates could be achieved by going to smaller feature size CMOS technologies such as 0.13um. In order to have a complete set of tools for developing high data rate circuits, it would be essential to develop a generic 10Gbps compatible PCB with chip-on-board feature. Further circuit design improvements can be brought to the dual power-ring concept to reduce switching noise effects of this topology. It would be interesting to undertake work with 1310um VCSEL and associated drivers to increase compatibility with future access network protocols (PONs).

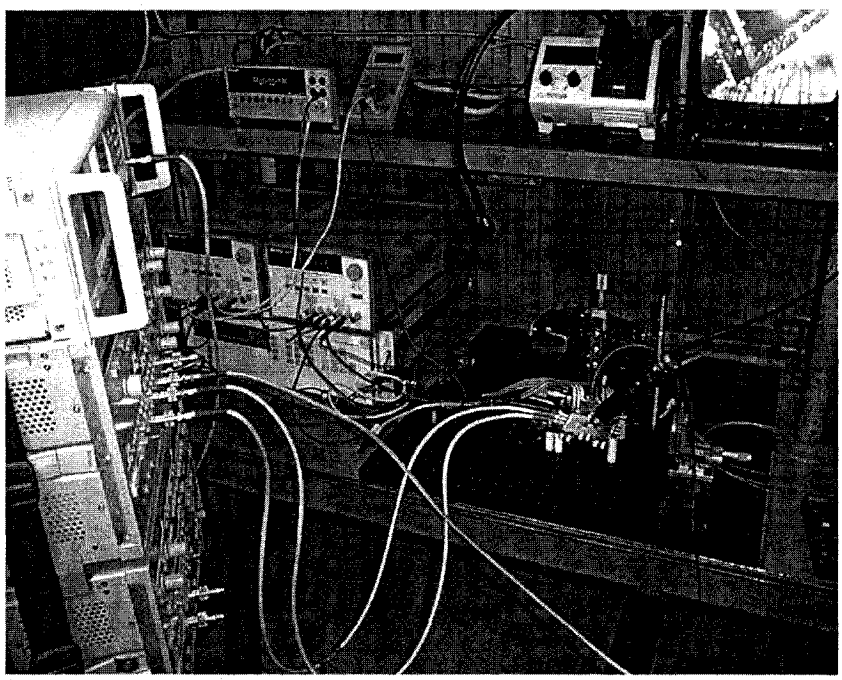
Finally, implementing the bursty network components evaluation bench would be a challenging enterprise. The usefulness of such a system is undeniable and has reasonable commercial potential, especially if bursty traffic networks finally get deployed at the access layer in the near to medium term. This is an overview of potential projects that could result from the present thesis. The future of optical transmitters for numerous applications lies in versatility and low power consumption. The data rate and power figures achieved for this thesis demonstrate the potential of such a design approach.

Appendix A

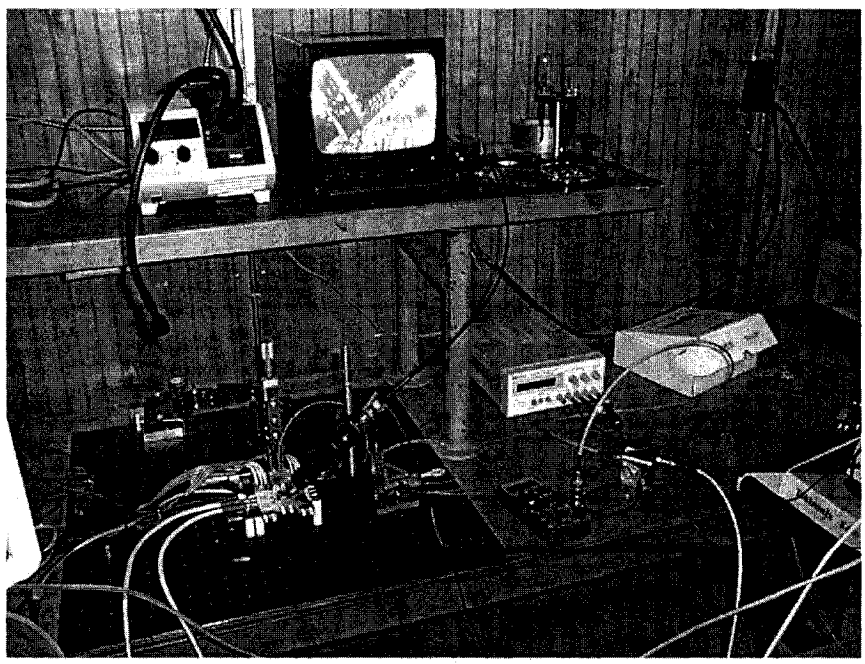
```
// VerilogA for BlockLib, eye_gen, veriloga

/*
This module generates traces that can be displayed as eye diagrams

Inputs:
=======
in                      = Input Signal

Outputs:
=======
sawtooth                = horizontal axis for all eye-diagrams.
out                     = Output Path
plot_out        = Output modified for eye diagram plotting.
To generate the eye-diagram, plot "sawtooth" and "plot_out" and change
the horizontal axis to "sawtooth".

Parameter definitions
=====================
symbol_rate             = Rate at which symbols arrive.
number_of_symbols       = Number of symbols to display in the eye diagram.
*/

`include "constants.h"
`include "discipline.h"
module eye_gen(in, out, plot_out, sawtooth);
inout in;
electrical in;
inout out;
electrical out;
inout plot_out;
electrical plot_out;
output sawtooth;
electrical sawtooth;
parameter real symbol_rate = 5e9 from (0:inf);
parameter integer number_of_symbols = 2 from (0:inf);
real delta;
real  up_time;
real  down_time;
integer blank;
real total_period;
real symbol_period;
analog begin
  if (analysis("static")) begin
    blank = 1;
    symbol_period = 1/symbol_rate;
    delta = symbol_period/1000.0;
    total_period = symbol_period*number_of_symbols;
    up_time = total_period - delta;
    down_time = delta;
  end
// The "blank" variable forces all eye traces to return along zero.
```

```
  @(timer(0, total_period)) begin
     blank = 1;
  end
  @(timer(total_period-1.01*delta, total_period));
  @(timer(total_period-delta, total_period)) begin
     blank = 0;
  end
// Output the data;
  V(in,out) <+ I(in,out)*0.1;
  V(sawtooth) <+ transition(blank*total_period,0,up_time,down_time/2);;
  I(plot_out) <+ blank*I(in,out);

end

endmodule
```

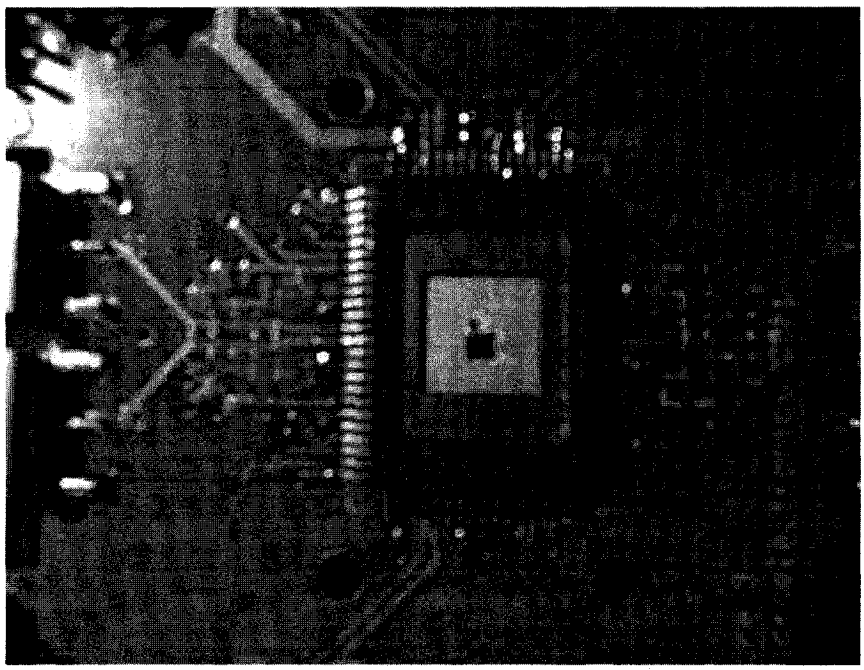
Appendix B



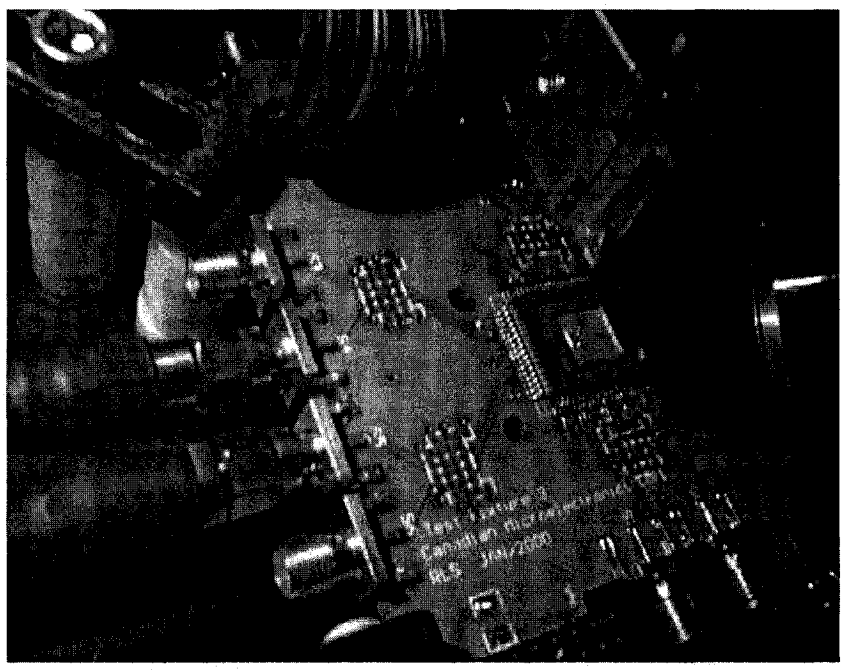
Picture of the test setup, with emphasis on BERT and power supplies.



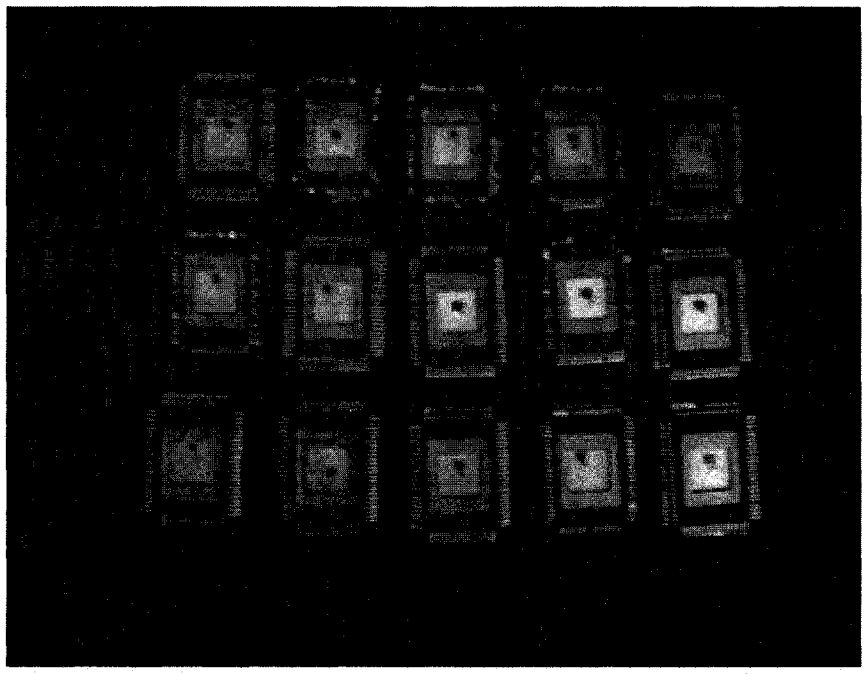
Picture of test setup, with emphasis on photoreceiver and imaging system.



CMOS transmitter and VCSEL die in CFP80 package soldered on PCB.



Close up view on optical transmitter and butt-coupled fibre.



Fifteen packaged CMOS/VCSEL dies used for experimental measurements.

Appendix C

Publications resulting from this work

1) Conference proceeding of the 2004 IEEE LEOS Summer Topical Meeting on VLSI Photonics, San Diego, USA.

A 24mW 2.5Gb/s VCSEL Driver in 0.18um CMOS

Jean-Philippe Thibodeau[1], Chris Murray[2] and David V. Plant[1]
[1]Department of Electrical and Computer Engineering, McGill University, Montreal, Canada
[2]Emcore Corporation, Albuquerque, New Mexico, USA

1 Introduction

With the ever increasing processing capacity of digital systems, electrical interconnects linking CMOS chips have become the limiting performance factor. Optical interconnects have been proposed as a promising alternative to increase interconnect capacity [1]. Vertical-cavity surface-emitting lasers (VCSEL) are well suited for such an application [1], but high-speed VCSEL drivers reported in the literature generally consume a significant amount of power [2,3]. In this paper, the design and testing of a low-power 2.5 Gb/s VCSEL driver for short-to-medium reach optical interconnects is presented.

2 Circuit design

The driver is designed in a TSMC CMOS 0.18um process made available through the Canadian Microelectronics Corporation (CMC). The system-level topology of the driver is illustrated in figure 1 [4]. A low-voltage-differential-signal (LVDS) is applied to the inputs of the pre-amplifier stage, implemented as a common-gate amplifier. The pre-amplifier has a gain of 11dB and a 3dB bandwidth exceeding 2GHz. The pulse-shaping stage further amplifies the signal and distorts it to prevent the current steering transistors of the laser driver stage from entering into full cut-off. This leads to better symmetry in the rise and fall times of the generated optical signal. The laser driver consists of a conventional current-steering differential pair with a dummy PMOS load in one of the branches. The resulting modulated current is combined with a bias current generated on-chip and pulled directly from the VCSEL. All stages are designed in NMOS with PMOS loads and biased at maximum f_T for optimum performance. A system simulation model, including models for the printed-circuit board (PCB) leads, ceramic quad-flat package (CFP) leads, VCSEL die, bond wire and extracted chip parasitics, was developed in Cadence and simulated using SpectreS. The simulated eye diagram of the current through the VCSEL is shown in figure 2(a) at 2.5 Gb/s. Although the driver can perform in excess of 5 Gb/s, laboratory experiments on the test fixture show eye closure and significant jitter around 3 Gb/s, which limit the performance of the system.

3 Experimental setup and measurement results

The fabricated driver chip was packaged in a CFP 80-pin package, along with a 10Gb/s VCSEL die provided by Emcore Corporation, and mounted on an RF test PCB. The VCSEL has a threshold current of 1mA and a slope efficiency of 0.5W/A. The LVDS input is applied with an Anritsu MP1763B pulse pattern generator through RF cables. The modulated optical signal is relayed to a New Focus 12GHz photoreceiver through a free-space two lens telecentric system with focal lengths of 15mm. In order to perform bit-error rate (BER) measurements, the photoreceiver output signal was further amplified with an RF amplifier. Eye diagram measurements were taken using a Tektronix 8000 communications signal analyzer. Measured eyes diagrams at 1.25Gb/s, 1.5Gb/s and 2.5Gb/s are provided in figures 2(b), 2(c) and

2(d) respectively. BER measurements at various pseudo-random bit sequence lengths for the three bit rates mentioned above along with power consumption measurements are included in table 1. BER measurements at 2.5Gb/s were unavailable at the time of submission due to measurement issues. Power consumption measurements include the VCSEL modulation and bias currents, which represent 75% of the total power consumption. The average optical power emitted by the VCSEL is 2mW at 2.5Gb/s. We expect to achieve better data rates and BER in the future by probing the inputs of the driver or using a higher bandwidth test fixture.

4 CONCLUSIONS

We have outlined the design and test of a 2.5Gb/s VCSEL driver in 0.18um CMOS. It consumes an average power of 24.2mW at 2.5Gb/s at an average emitted optical power of 2mW, which compares advantageously with other published designs [2,3].

5 REFERENCES

[1] D.A.B. Miller, "Rationale and challenges for optical interconnects to electronic chips," Proc. IEEE, vol. 88, no. 6, pp.728-749, June 2000.

[2] F. Delpiano, B. Bostica, M. Burzio, P. Pellegrino, and L. Pesando, "10-Channel optical transmitter module operating over 10Gb/s based on VCSEL and hybrid integrated silicon optical bench," Proc. Electronic Components and Technology Conference, 1999, pp.759-762.

[3] D.V. Plant, A.E.L. Chuah, M.B. Venditti, and A.D. Isac, "2.5 Gb/s CMOS push-pull VCSEL driver with symmetric rising and falling edges," Applied Optics, in press.

[4] K.R. Shastri, K.A. Yanushefski, J.L. Hokanson, and M.J. Yanushefski, "4.0Gb/s NMOS laser driver," Proc. IEEE Custom IC Conference, 1989, pp. 14.7.1-3.

Acknowledgments: This work was partially supported by the National Sciences and Engineering Research Council (NSERC) and industrial partners, through the Agile All-Photonic Networks (AAPN) Research Network, the Canadian Microelectronics Corporation (CMC), and a NSERC graduate scholarship. We also thank Julien Faucher and Eric Bisaillon for their help in setting up the experiments.

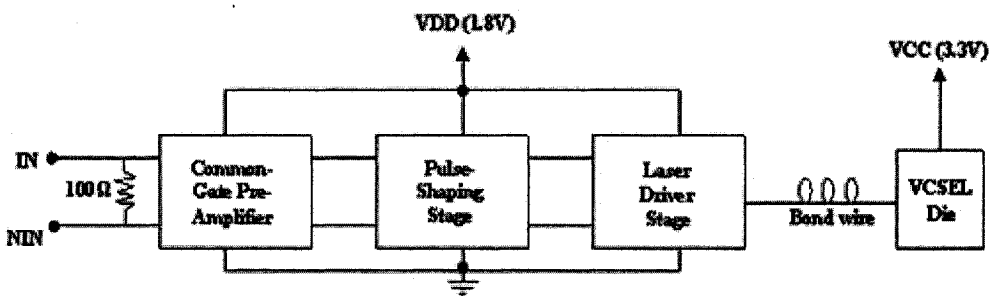
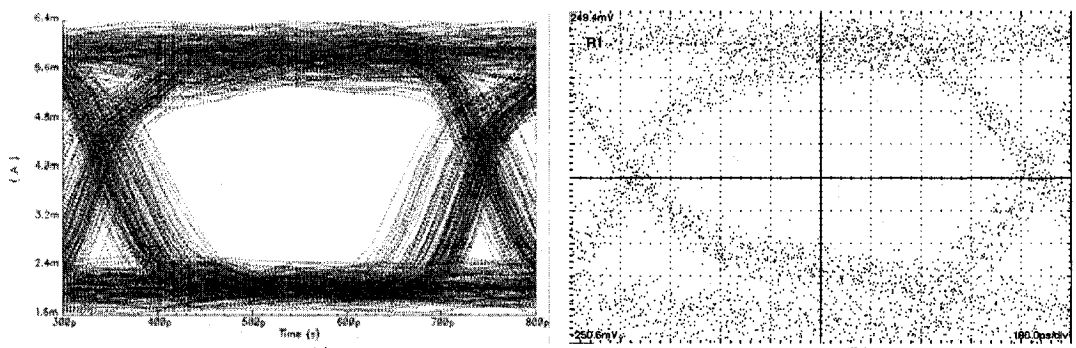
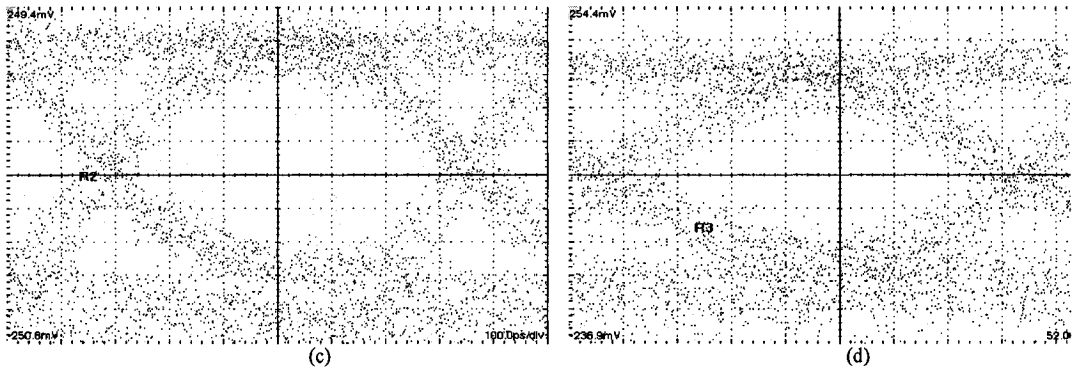


Figure 1: System-level topology of the VCSEL driver



(a) (b)



(c) (d)

Figure 2: Eye diagrams at various data rates (a) Simulated at 2.5Gb/s (b) Measured at 1.25Gb/s (c) Measured at 1.5Gb/s (d) Measured at 2.5 Gb/s

Data Rate	PRBS Length	BER	Total Power Consumption
1.2 Gb/s	2^{31}-1	$< 10^{-10}$	19.8mW
1.5 Gb/s	2^{15}-1	$< 10^{-9}$	22.9mW
1.5 Gb/s	2^{9}-1	$< 10^{-12}$	22.9mW
2.5 Gb/s	TBD	TBD	24.2mW

Table 1: Bit-error rate and power consumption measurements for three data rates