PHASE-LOCKED LOOP SIMULATION

IN TRANSIENT STABILITIES STUDIES

by

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ABSTRACT

The objective of this thesis was to develop and validate a phase-locked loop (PLL) model suitable for transient stability studies of power systems. Such a model is to be implemented in transient stability programs. This objective has been achieved through the following phases:

The phase-locked loop was modelled in details by means of the *PSPICE* simulation software. Three types of PLL were simulated: PLL with PI controller, PLL with PI controller including a filter and PLL with PI controller including the synchronous (Fourier) filter. The PLL dynamics was evaluated by means of step responses to phase and amplitude perturbations, while the PLL harmonic performance was evaluated using the second harmonic component added to the input signal.

In order to validate the PLL detailed models, the PLL circuits were realized in electronic components. The test were performed and step responses to the phase and amplitude perturbations were recorded as well as to steady-state second harmonic excitation. The very close agreement between laboratory recordings with the simulation results, was achieved.

PLL reduced models suitable for transient stability studies of power systems were analytically developed. Nonlinear PLL reduced model is suitable for transient stability studies based on numerical integration, while the linear PLL reduced model is suitable for transient stability studies based on eigenvalue analysis.

The dynamics of the PLL reduced models was evaluated by means of step responses to phase and amplitude perturbation. The close agreement between the obtained results with those obtained by detailed simulation fully validated the developed PLL reduced models. The development of such models represents an original contribution to phase-locked loop modelling in transient stability studies of power systems.

The development procedure of this thesis, demonstrated that the *PSPICE* simulation program could be applied for development of reduced models of other analog circuits and control systems which are to be used in power system stability programs.

RÉSUMÉ

L'objectif de cette thèse est de développer et de vérifier un modèle pour les boucles d'accrochage de phase, utilisable dans les études de stabilité transitoire des réseaux de transport. Cet objectif a été atteint au moyen des phases suivantes:

La boucle de phase a été simulée au moyen du logiciel de simulation *PSPICE*. Trois types de boucles de phase ont été réalisés: avec contrôleur PI (proportionnel intégrale), PI avec filtre, et PI avec filtre synchronne (Fourier). La dynamique des boucles de phase a été évalué au moyen de leur réponse à des perturbations en échelon de la phase ou de l'amplitude, tandis que la performance harmonique a été étudié en ajoutant du deuxième harmonique au signal d'entrée.

Pour valider les modèles détaillés, les boucles de phase ont aussi été réalisés avec des composants électroniques et soumis aux même perturbations. Des résultats très semblables ont été obtenus au moyen de ces deux méthodes.

Des modèles simplifiés pour les études de stabilité transitoire ont été developpés de façon analogique. Le modèle nonlinéaire est utilisable dans les programmes basés sur l'intégration numérique, tandis que le modèle linéaire simplifié l'est dans les programmes d'étude de stabilité au moyen des valeur propres.

La dynamique des modèles simplifiés a été évaluée de la même façon que pour les modèles détaillés. La très bonne concordance obtenue entre les résultats des modèles détaillés et simplifiés valide entièrement ces derniers. Le développement de ces modèles représente une contribution originale pour la simulation des boucles de phase dans l'étude de la stabilité transitoire des réseaux de transport d'énergie.

De plus, le développement effectué pour cette thèse a permis de montrer que le programme de simulation *PSPICE* pourraît être efficacement utilisé pour developper des modèles de circuit analogique de contrôle utilisé dans les programmes de stabilité des réseaux de transport d'énergie.

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TABLE OF CONTENTS

Chapter 3: VCO and Filter Design Considerations

Chapter 4: Modelling of Electronic Components

Chapter 5: Phase-Locked Loop Simulation

Chapter 6: Experimental Analysis of the Phase-Locked Loop

NOMENCLATURE

ϕ_i	PLL input signal phase
ϕ_o	PLL output signal phase
ϕ_e	Phase error
ω	Angular frequency
ω_o	Free running angular frequency
ω_i	Frequency of the input voltage
$\Delta\omega$	Error frequency
τ_1	First time contact of the RC oscillator
τ_2	Second time contacat of the RC oscillator
τ_f	Time contact of the low-pass filter
k	Control gain
B_γ	Resultant susceptance of the compensator
B_c	Capacitive susceptance of the compensator
B_l	Inductive susceptance of the compensator
f_o	Central frequency of the oscillator
I_D	Drain curent
I_{DSS}	Drain-Source saturation current
I_f	Feedback current of the law-pass filter
I_1	Input current of the low-pass filter
I_m	Maximunx value of the voltage controlled current source
K_c	Dc gain of the regulator
Kd	Gain of the phase detector model
K_f	DC filter gain
K_i	Gain of the I controller
K_p	De gain of the P controller
K_v	Forward loop gain
Ko	Gain of the VCO model
K_{osc}	Voltage controller oscillator gain

LPF	Low-pass filter
PD	Phase detector
PLL	Phase-Locked Loop
R_f	Low-pass filter resistance
s	Laplace transform operator
SR	Saturated-reactor compensatror
TCR	Thyristor-controller reactor compensators
TCR/TSC	Hybrid compensator
TSC	Thyristor-switched capacitor compensators
V_o	2nd Output voltage of the RC oscillator
V_1	First output voltage of the RC oscillator
V_c	Control voltage of the voltage controlled oscillator
VCO	Voltage controlled oscillator
V_{GS}	Gate-Source voltage
$\|V_i\|$	Voltage magnitude of the input signal
$\|V_o\|$	Voltage magnitude of the output signal
V_p	Pinch-off voltage
V_f	Output voltage of the integrator filter
V_e	Error voltage
V_{ref}	Reference voltage
V_T	Peak value of the timming wave
X_c	Compensator capacitive reactance
X_l	Compensator inductive reactance
X_t	Compensator transformer impedance

INTRODUCTION

Static Var Compensators are new components which are applied in power systems for a variety of functions: to stabilize the system voltage, to increase the transfer capability and transient stability margin of long transmission systems, to provide reactive power at ac-dc converter stations, to damp power oscillations, etc.

Present modelling of static var compensators (SVC) in transient stability studies does not include phase-locked loop circuits, though they affect significantly upon SVC dynamics. The main objective of this thesis was to develop models of such circuits. The developed models were validated by comparison with the actual electronic circuits as well as their detailed models realized in *PSPICE* simulation program. Implementation of such models will further improve the transient stability programs.

The thesis is organized as follows:

Chapter 1 gives a review of the literature of the static var system (SVS), typical configurations and control system with a brief description of different components of the regulator; more specifically, the phase-locked loop and its role in the synchronizing unit.

In chapter 2, the principles which governs this feedback loop are outlined as well as the linearized model in order to apply linear control theory.

In chapter 3 a special concern is given to the VCO, where the solution of a second order differential equation is derived in order to describe its dynamic behavior.

The RC oscillator incorporates an automatic amplitude control circuit to keep under control the voltage amplitude under any perturbation and a dc voltage to keep in synchronism the oscillator. This voltage is the phase difference between the input and feedback signals of the phase-locked loop.

Finally, we switch to filters, whose funtion is to discriminate againts unwanted frequencies. Fundamentals steps are given to design a first order active filter as well as an introduction of the synchronous filter.

Chapter 4 provides an overview of the modelling of essential components to be used in the computer simulation. i.e. electonic switch, simplified model for the operational amplifier and the analog multiplier.

Finally, we switch to filters, whose funtion is to discriminate againts unwanted frequencies. Fundamentals steps are given to design a first order active filter as well as an introduction of the synchronous filter.

Chapter 4 provides an overview of the modelling of essential components to be used in the computer simulation. i.e. electonic switch, simplified model for the operational amplifier and the analog multiplier.

Chapter 5 deals with the phase-locked loop modelling. The PLL is simulated in details by means of *PSPICE* simulation program. Three PLL configurations are considered: PLL with PI controller, PLL with PI controller including the first order filter and the PLL with PI controller including the synchronous (Fourier) filter. Their dynamic response is evaluated for step phase perturbation and step amplitude perurbation of the input voltage.

The PLL harmonic performance was evaluated using the input voltage including the steady-state second harmonic component. In addition, the combination of such perturbations signals were also applied. Fourier analysis was used in order to asses the harmonic generation of the PLL itself as well as when excited by the second harmonic component at its input.

In Chapter 6, the validation of models developed in the previous chater, is realized in electronic components. The step perturbation signals are applied to the PLL circuits as done in simulation.

In Chapter 7, the PLL for stability studies is analytically developed.

Two PLL models were developed: one-linearized for small signal, the other-nonlinear for large signal analysis. The nonlinear PLL reduced model is suitable for transient stability studies based on numerical integration, while the linear PLL reduced model is suitable for studies based on eigenvalue analysis.

The thesis concludes with an overall conclusion in Chapter 8.

GENERAL BACKGROUND

CHAPTER 1

STATIC VAR COMPENSATORS

1.1 — Introduction

The *Static Var Compensator* can be thought of a functional adjustable shunt susceptance. A compensator can be controlled in such a way as to improve the power system performance during all four periods as defined in Fig 1.1. to achieve one or more of the following objectives:

- Voltage stabilization for normal network operation
- Load balancing
- Power transmission capacity increase
- Transmission stability improvement
- Improvement of system damping
- Subsynchronous resonance damping
- Reactive compensation of ac-dc converters
- Reduction of temporary overvoltages

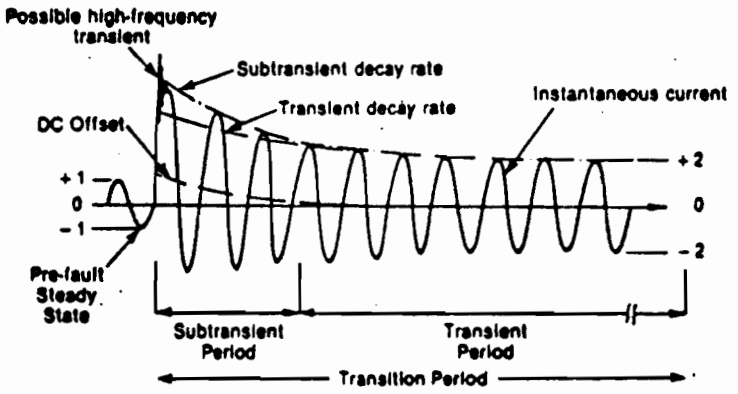


Fig. 1.1 Characteristic time period in a.c. system

1.2 — Structure of the Compensators

The main types of compensators are the following:

- Thyristor-Controlled Reactor (TCR) Compensators
- Thyristor-Switched Capacitor (TSC) Compensators
- Saturated-Reactor (SR) Compensators
- Hybrid (TCR/TSC) Compensators

1.2.1 — Thyristor-Controlled Reactor (TCR) Compensators

These basically comprise linear reactors in series with high voltage a.c. thyristors. The Thyristors are back-to-back(or inverse parallel) connected for bidirectional current in each phase and the reactor current is controlled by adjusting in each half-cycle the firing angle delay from voltage zero in each phase, from 90°,full conduction to 180°,no conduction. The controller includes the thyristor firing sinchronizing system, the regulator and the meassuring system is shown in Fig. 1.2.

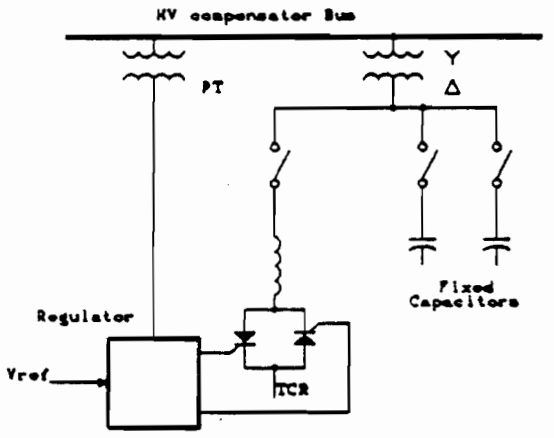


Fig. 1.2 Single-line circuit for thirystor controlled reactor compensator

1.2.2 — Thyristor-Switched Capacitor (TSC) Compensators

Although similar in concept to the TCR, thyristor control of capacitors is only possible as an ON/OFF switched action. Continuons firing angle control is not possible with a TSC which unlike a TCR produces a large switching inrush current which are minimun if it is switched in each half cycle at an instant when the voltage across the thyristor switch is minimun.

The TSC compensator gives essentially a discrete form of control of the reactive power, and if used alone requires a number of relatively small capacitor banks each switched by directional thyristor similar to the TCR (Fig. 1.3).

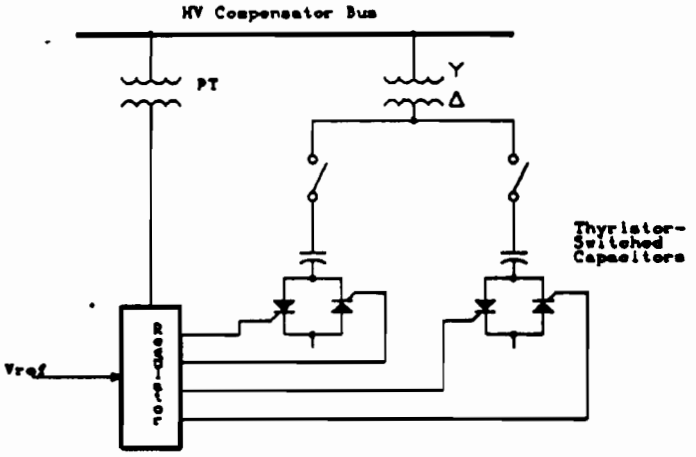


Fig. 1.3 Thyristor switched capacitor

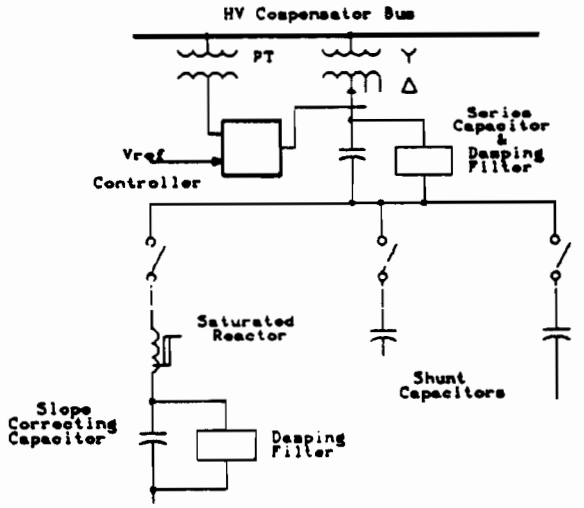


Fig. 1.4 Saturated-Reactor

1.2.3 — Saturated-Reactor (SR) Compensators

Saturated-reactor compensator consists of a saturated reactor, with a slope correcting capacitor, a shunt capacitor and a standard transformer for coupling to HV or EHV systems. It is often provided with and on-load tap charger to enable adjustment of the operating point according to the system requirements. Slope conection capacitors are connected in series with the satured reactor to reduce the internal reactance Xs of the whole compensator, including transformer, to a required level. Damped bypass filters are always applied across these capacitors to damp oscillations at subsynchronous frequencies, as well as inrush current transients of the saturated reactor, in order to eliminate the risk of ferrromagnetic resonance. The slope correction capacitor has to be protectred by a protective device such as a nonlineal resistor or spark-gap against overvoltages.

Shunt capacitors, conected in parallel to the slope-corrected saturated reactor, can extend the operating characteristic into the leading power factor region. These may be designed as filters if the system resonance conditions requires such a measure.

1.2.4 — Hybrid (TCR/TSC) Compensators

The basic scheme of a TCR/TSC compensator consists of thyristor switched capacitor banks connected in parallel with one or more 6 pulse thyristor controlled reactors units of equal rating. In some configurations a fixed or mechanically switched capacitor bank is provided as well as a filter capacitor bank, if required, and a step-down transformer, as shown in Fig. 1.5.

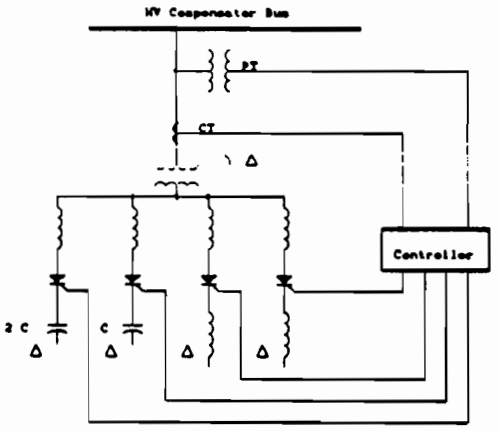


Fig. 1.5 TSC/TSR static var compensator

1.3 — Controller

It generates firing pulses for the thyristor valves in such a way that the reactive power required to meet the control objective at the primary terminal of the compensator is obtained.

The controller comprises the following subsystems:

- The measuring device, which measures relevant system variables such as voltage, curent, active power flow, etc
- The control signal processor,which automatically computes the necessary firing angle α for the thyristors valves
- The synchronizer, a device which generates the time reference
- The firing angle generator, which generates the firing pulses from the α signal
- The pulse generator, which generates the pulses necessary for the primary side of the pulse transformer

Fig. 1.6 shows the block diagram of a controller with two closed-loop circuits. A voltage error (i.e. the difference between the actual system voltage and a reference voltage) is measured and used to cause the susceptance of the compensator to increase or decrease until the voltage error is reduced to an acceptable level.

The ratio of the compensator current to the voltage error determines the slope of the voltage/current characteristic. The speed of response and stability are determined by the total loop gain and time constants of the regulating system. The loop gain is a function of the system impedance. This means that as the system impedance increases, the compensator will have a faster response but, will also have a smaller margin of stability. Since the relationship between the conduction angle and compensator current is not linear, a linearizing network is required if a better dynamic performance is desired.

The current-loop provides the accuracy. This means that the controlled reactive current will be proportional to the voltage error, independent of the particular values of X_L, X_C, X_T, the gains of the conduction angle calculators, the linearizing network, and the delays of the gating pulse generator. The slope of the V-I characteristic is determined by the gain K_1. The current error is zero since K_2 is an integrator.

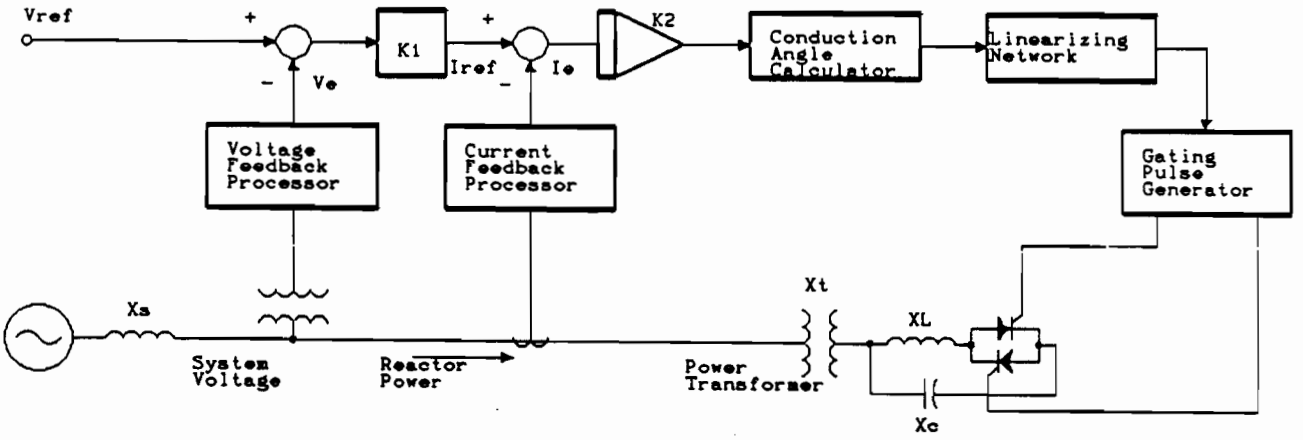


Fig 1.6 SVC with voltage and current control unit

1.3.1 — Synchronization Circuit

A number of methods can be used to obtain the reference signals required by this circuit:

- zero-crossing detectors
- zero-crossing detector with filtering
- phase-locked loop circuit

The phase-locked loop circuit provides timing signals to the timing circuit which are used for reference in generating the firing pulses. The PLL itself is a feedack control system; therefore it is essential its response to change in phase angle be fast and stable and that it can operate in presence of harmonics in the power frequency voltage. It is equally important that this circuit remains stable during the loss of control voltage (i.e. a fault at control bus). Let us take a look at the control principle of the cosine wave zero-crossing synchronization circuit . In particular, the interface of the timing signal with the firing angle and more precisely, how a frequency variation in the network will affect the dynamic performance of the compensator, that is, the operating point of the V-I characteristic, shown in Fig. 1.7.

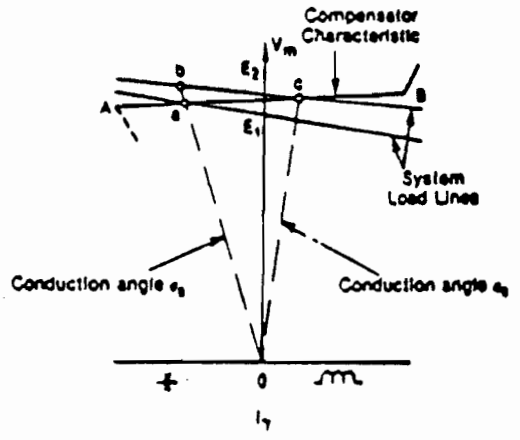


Fig. 1.7 V-I characteristic of SVC

1.3.1.1 — Zero-Crossing Principle

Figure 1.8 illustrates the block-diagram of the circuit for thyristor firing at the required angle α. In each channel, a cosine time wave, obtained from the PLL, is applied to one input terminal of a comparator; the voltage representing the inverse of the susceptance is applied to the other input of the comparator.

The output voltage of the comparator changes level at the intersection point of the cosine timing wave with the reference voltage, and this produces a corresponding clock pulse at the output of the associated clock pulse generator. The clock pulse sets the associated pulse output flip-flop, thereby initiating a firing pulse in this output channel. The pulse output flip-flop is reset by the clock pulse from the following channel.

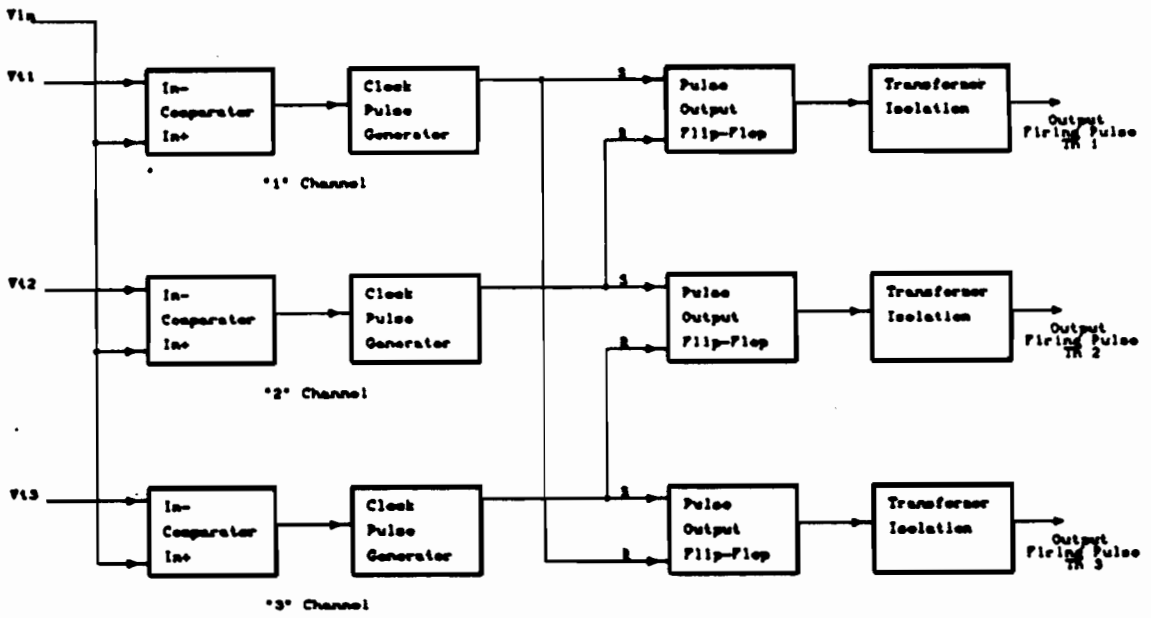


Fig. 1.8 Zero-crossing PLL-based firing circuit

By condition each firing pulse is initiated at the point at which the the amplitude of the associated cosine wave becomes equal to the reference voltage, that is when:

$$V_T \cos \omega t = V_{ref} \tag{1.1}$$

where

$|V_T|$ is the peak value of the timming wave

By definition, at this instant, ωt is equal to α. Therefore,

$$\cos \alpha = \frac{V_{ref}}{V_T} \tag{1.2}$$

Hence

$$\alpha = \cos^{-1} \frac{V_{ref}}{V_T} \tag{1.3}$$

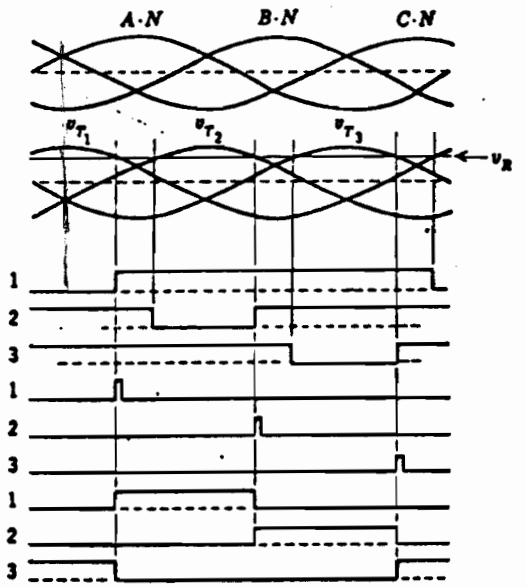


Fig. 1.9 Waveform of cosine principle

Thus, from Fig. 1.9, the firing angle α depends on the phase difference between the two signals applied to the detector of the PLL which means: the larger the phase angle, ϕ the larger the firing angle α, and a smaller conduction angle σ. Therefore, the reactive current of the compensator will also decrease.

1.4 — Nonlinear characteristic of the TCR susceptance

The nonlinear characteristic of the TCR susceptance is the relationship between the conduction angle σ of the thyristor valve and the inductive susceptance of the compensator.

The intantaneous current i(t), through the reactor of Fig. 1.6 is given by

$$i(t) = \begin{cases} \frac{\sqrt{2}V}{X_l}(\cos\alpha - \cos\omega t) & \text{if } \alpha < \omega t < \alpha + \sigma \\ 0 & \text{if } \alpha + \sigma < \omega t < \alpha + \pi \end{cases} \tag{1.4}$$

where

V	is the rms voltage
X_l	is the fundamental-frequency reactance of the reactor
α	is the gating delay angle
σ	is the conduction angle

σ is related to α by the equation

$$\alpha + \sigma/2 = \pi \tag{1.5}$$

The fundamental component is found by Fourier analysis and is given by

$$I_1 = \frac{\sigma - \sin\sigma}{\pi X_L} V \tag{1.6}$$

This equation can be written as

$$I_1 = B_L(\sigma)V$$

where $B_L(\sigma)$ is an adjustable fundamental-frequency susceptance controlled by the conduction angle according to the law,

$$B_L(\sigma) = \frac{\sigma - \sin\sigma}{\pi X_L} \tag{1.7}$$

This control law is shown in Fig. 1-10

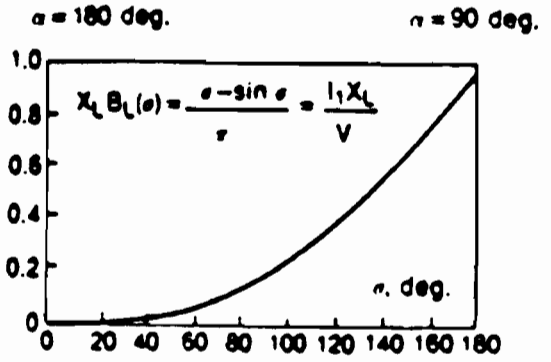


Fig. 1.10 Nonlinear characteristic of the TCR susceptance

The resultant susceptance of the compensator, Fig. 1-6, is given by

$$B_\gamma = B_C - B_L(\sigma) \tag{1.8}$$

The expression (1.7) is a nonlinear function of σ. In order to linearize this relationship, a linearizing function block has to be included in the control system. This function is an inverse of f(σ), therefore, its general form is $\sigma = f^{-1}(B_\gamma)$.

Since the equation (1.7) can not be resolved explicitely for σ, on the control system this is usually done by means of a lock-up table.

1.4 — Summary

We have described the *static var compensator*, its main configurations and applications with an emphasis on the control system. The controller and components were described with regard to the closed-loop control and a general idea of how it works. Hence, we learnt the PLL plays an important role in the feedback control system of the compensator for which reasons it has to be modelled correctly.

CHAPTER 2

GENERAL ANALYSIS OF THE PHASE-LOCKED LOOP

2.1 — Introduction

Our application is concerned with a modelling of the PLL phase response to a step-phase perturbation in the power network. Switching of transmission lines, reactors, capacitors, transformers and loads in and out, as well as fault incidents give rise to such a perturbation. The system voltage will be the input to the phase-locked loop. Thus, the fundamental concepts of this circuit will be given in this chapter.

2.2 — Principles of the Phase-Locked Loop (PLL)

The function of the phase-locked loop system is to track in phase (and frequency) an incomming sinusoidal signal. As shown in Fig. 2.1, the PLL is basically an electronic servo loop consisting of a phase detector (PD), a low-pass filter (LPF), and a voltage controlled oscillator (VCO).

As the loop tracks the input signal, the PD compares the phase of the input signal with the phase output from the VCO. A change in the phase of the circuit signal indicates that the incoming frequency is begining to change.

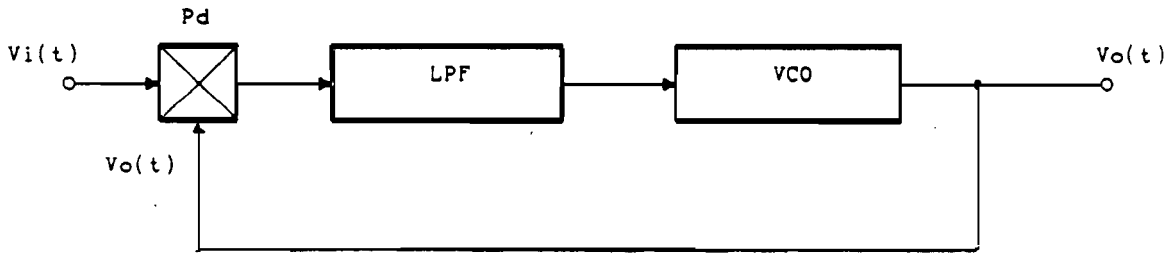


Fig. 2.1 Block diagram of the PLL

2.3 — PLL Linear Model

Although this circuit is nonlinear because of the nonlinearity of the phase detector (analog multiplier) and the VCO, it can be accuratly modelled as a linear device when the phase difference between the PD inputs is small.

Using the techniques and philosophy of linear control system theory, the PLL can be analized as a conventional feedback loop.

If linearization is not considered, then the phase-plane method should be applied to study the performance of this circuit. Let us assume that

$$V_i(t) = |V_i| \sin(\omega_i t + \phi_i) \tag{2.1}$$

$$V_0(t) = |V_0| \cos(\omega_0 t + \phi_0) \tag{2.2}$$

then the output of the PD will be

$$V_e(t) = |V_e|\{[\sin(\omega_i + \omega_0)t + \phi_i + \phi_0)] + \sin[(\omega_i - \omega_0)t + (\phi_i - \phi_0)]\} \tag{2.3}$$

where

$$|V_e| = \frac{1}{2}|V_i||V_0| \tag{2.4}$$

The component $(\omega_i + \omega_o)$ is eliminated by the filter while the component $(\omega_i - \omega_o)$ passes through the low-pass filter. Hence,

$$V_c(t) = |V_c| \sin[(\omega_i - \omega_0)t + \phi_i(t) - \phi_0(t)] \tag{2.5}$$

2.3.1 — Case I

When the two input frequencies to the phase detector are not synchronized, the loop is not locked.

Equation (2.5) describes the signal voltage which is applied to the VCO to control its output frequency. This equation shows that this signal sets at a beat frequency ω_i-ω_0, causing the VCO's frequency to change from ω_0 in proportion to the signal amplitude $V_c(t)$ passing through the filter. If the amplitude of $V_i(t)$ is sufficiently large, the oscillator output frequency will be shifted from the free running frequency, ω_0' until locking is established,that is, when $\omega_i = \omega_o' + \Delta\omega$.

2.3.2 — Case II

At synchronism, when ω_i becomes equal to ω_0 the output signal from the LPF becomes proportional to the phase shift between synchronized signals:

$$V_c(t) = |V_e| \sin(\phi_i - \phi_0) \tag{2.6}$$

Then, applying linearization with regard to

$$\phi_i - \phi_0 \tag{2.7}$$

the equation (2.6) reduces to

$$V_c(t) = |V_c|[\phi_i(t) - \phi_0(t)] \tag{2.8}$$

Thus, multiplier as a phase detector can now be represented by its linear equivalent, a phase discriminator to the inputs $\phi_i(t)$ and $\phi_0(t)$.

The VCO is assumed to change in frequency as the control voltage changes, the integral being proportional to the change in phase.

The transfer function relating the phase and voltage is given by

$$\phi_0(s) = \frac{K_{osc}}{s} V_c \tag{2.9}$$

where s is the Laplace operator.

Thus, the linearized loop of the phase-looked loop is illustrated in Fig. 2.2

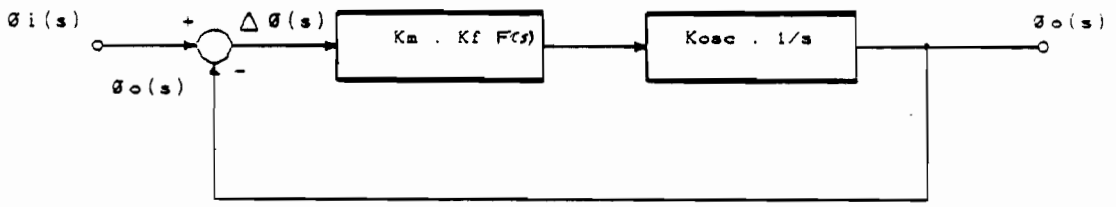


Fig. 2.2 PLL linear model

Hence, the transfer function becomes:

$$\frac{\phi_0(s)}{\phi_i(s)} = \frac{\frac{K_M K_f K_{osc}}{s} F(s)}{1 + K_M K_f K_{osc} F(s)/s} \tag{2.10}$$

2.4 — Transient Performance

The PLL is a nonlinear device over its operating range. The performance of the loop depends especially on the type of phase comparator used in the system. An approximate analysis of the linearized system provides an insight providing generalized design guidelines. Before considering the dynamic performance of the loap, it is instructive to consider the range of input frequencies over which the loop can remain looked.

Feedback systems whose open-loop transfer function has one pole at the origin are known as type I systems.

The PLL has an open-loop pole at the origen because of its VCO, so the system is at least type I. A second pole at the origin is often added to the filter to eliminate steady-state velocity error increasing the noise suppression. In this case, the system is the type II. If the open-loop system has N poles at the origin it is a type N system.

First, consider a type I loop. If the circuit is in lock, small changes in the input frequency will cause a change in the phase-detector output voltage in the direction that drives the error signal back toward zero.

The change in frequency will be the forward loop gain times the error voltage, or

$$\Delta\omega = K_M K_f K_{osc} \sin\phi_e(t) \tag{2.11}$$

where

ϕ_e is the phase error

This equation assumes that signals change so slowly that there is no attenuation in the low-pass filter. Since

$$\sin\phi_e(t) \leq 1 \tag{2.12}$$

and

$$\Delta\omega \leq K_M K_f K_{osc} = K_v \tag{2.13}$$

That is, the maximum charge in frequency for wich a type I loop can remain locked, refered to as the *lock range or tracking range*, is less than, or equal to, the forward loop gain. Lock range refers to how far the input frequency can change without the loop lossing synchronism. *Capture range* refers to how close the input frequency must come to the free-running frequency of the VCO before locking-up can occur.

When the frequency error is other than zero, the PD output voltage is somewhat attenuatted by the low-pass filter before it reaches the VCO. Therefore, the capture range is less than the lock range. The actual value depends on the type of low-pass filter used. A general expression for loop capture range is not available since the system is highly nonlinear.

For type II loops, K_v could be considered as infinity. The phase detector output is integrated until the phase error reduces to zero. The tracking range of type II loops is limited by the dynamic range of the voltage-controlled oscillator. The loop capture range can not exceed the frequency range of the VCO.

2.4.1 — Time-Domain Equation

From the transfer function derived from the PLL linear model, we can obtain the algebraic equation in the s-plane describing the transient performance of the loop. Thus

$$\phi_0(s)[s + K_v F(s)] = K_v F(s)\phi_i(s) \tag{2.14}$$

Then, applying inverse Laplace transform, we get

$$\frac{d\phi_0(t)}{dt} + K_v L^{-1}[\phi_0(s) * F(s)] = K_v L^{-1}[F(s) * \phi_i(s)] \tag{2.15}$$

This is the general time domain equation of the circuit-model which will be analized in detail in Chapter 5. From this equation,we can say that the transient performance of the PLL will depend on the type of filter, F (s).

2.5 — Steady-State Error Analysis

This analysis determines the final error in response to inputs, which can be expressed as a time polynomial:

$$\phi_i(t) = \begin{cases} \sum_{n=0}^{k} \phi_n t^n & \text{at } t > 0 \\ 0 & \text{at } t < 0 \end{cases} \tag{2.16}$$

It is important to know what the steady-state error will be in response to these inputs. This can be readely determined for the linear model already derived.

The error signal $\phi_e(s)$,defined as $\phi_i(s) - \phi_0(s)$ can be expressed in the following way

$$\phi_e(s) = \frac{\phi_i(s)}{1 + K_v F(s)/s} \tag{2.17}$$

If the system is stable, the steady-state error for polynomial inputs given by eqn(2.16) can be obtained from the final value theorem.

$$\lim_{t\to\infty} \phi_e(t) = \lim_{s\to 0} s\phi_e(s) \tag{2.18}$$

If $\phi_i(t)$ is a step function representing a sudden increase in phase of $\phi°$,

$$\phi_i(s) = \frac{\phi}{s} \tag{2.19}$$

Then, applying eqn(2.18) into eqn(2.17) yields to

$$\lim_{s\to 0} \phi_e(s) = 0 \tag{2.20}$$

F(s) is either a constant or a low-pass filter that may include poles at the origen or a PI controller as will be one of our cases. Let us see one case to illustrate this analysis.

Setting

$$F(s) = \frac{K_i}{s} + \frac{K_f}{1 + \tau_f s} \tag{2.21}$$

and applying the final value theorem, we also get a zero steady-state error. In addition, the steady-state velocity error becomes also zero.

2.6 — Summary

In this chapter a general background of the phase-locked loop has been considered. In the decription of this system we began with a nonlinear model and then a linearization was performed in order to to apply linear control system analysis. Finally a steady- state error analysis in general,is given with two examples as an illustration.

CHAPTER 3

VCO AND FILTER DESIGN CONSIDERATIONS

3.1 — Introduction

This chapter deals with design aspects of a VCO, low-pass and a synchronous filter, as part of the synchronizing unit PLL, and the background necessary for the the digital computer simulation, by means the *PSPICE* program.

3.2 — RC Oscillator

For a free running oscillator the following amplitude and phase conditions must be simultaneously satisfied:

3.2.1 — Amplitude Condition

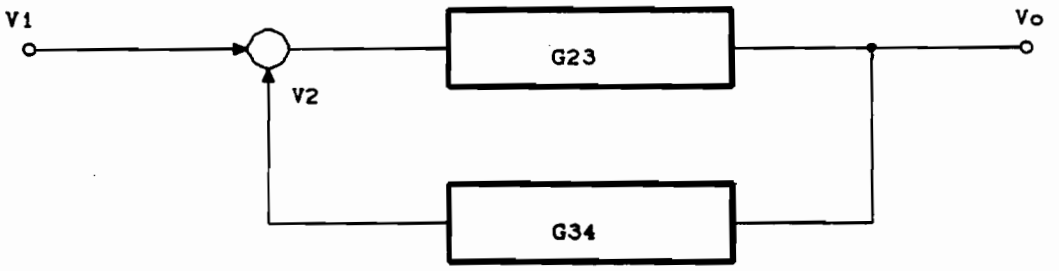


Fig. 3.1 Typical feedback circuit

The block diagram of an oscillator is shown in Fig. 3.1. Its transfer function is given by the following expression

$$G_{10} = \frac{V_0}{V_1} = \frac{G_{23}}{1 - G_{23}G_{34}} \tag{3.1}$$

In order for free oscillations to occur, its open-loop gain must assume -1 at its frequency of oscillation . The oscillators are designed to operate at one frequency only. Therefore, the denominator $1 + G_{23}G_{34}$ will have a pair of zero on the imaginary axis, $s_{1,2} = \pm\hat{\jmath}\omega$, where ω is the oscillating frequency.

The magnitude of the oscillating output is determined by the initial conditions of the oscillator.

From here, we deduce the first condition for oscillation: the absolute value of the open-loop gain should be:

$$|G_{23}(\hat{\jmath}\omega)||G_{34}(\hat{\jmath}\omega)| = 1 \tag{3.2}$$

at the oscillation frequency ω_0, which is called the *amplitude condition* .

3.2.2 — Phase Condition

Let

α be the phase of $G_{23}(\hat{\jmath}\omega)$

and

β be the phase of feedback $G_{34}(\hat{\jmath}\omega)$

at the frequency of oscillations.

Then, we can establish the second condition for oscillation, which is given at

$$\alpha + \beta = \pi \tag{3.3}$$

which is called the *phase condition* . In terms of the Bode diagram we can say that the phase margin must be zero while the magnitude must be equal to zero dB (at the frequency of oscillations).

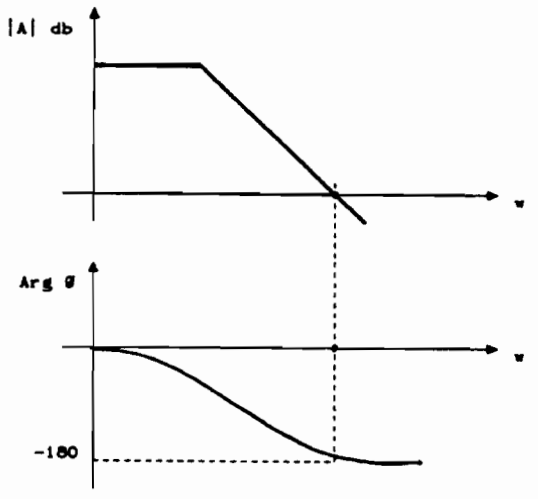


Fig. 3.2 Bode diagram for oscillating conditions

3.3 — Sinewave Generation

Let us consider the 2_{nd} order differential equation

$$\frac{d^2U_0(t)}{dt^2} + 2\delta\omega_n \frac{dU_0(t)}{dt} + \omega_n^2 U_0(t) = 0 \tag{3.4}$$

Applying Laplace transform, we get

$$s^2U_0(s) + 2\delta\omega_n sU_0(s) + \omega_n^2 U_0(s) = 0 \tag{3.5}$$

assuming the zero initial conditions. Hence, the eigenvalues are

$$s_{1,2} = -\delta\omega_n \pm \hat{\jmath}\omega_n\sqrt{1-\delta^2} \tag{3.6}$$

$$s_{1,2} = \alpha \pm \hat{\jmath}\omega \tag{3.7}$$

where: δ is the damping ratio; ω_n is the natural frequency; α is the damping constant; ω is the frequency.

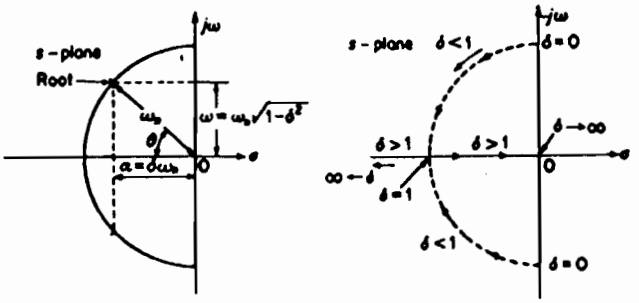


Fig.3.3 Locus of roots with δ

The eigenvalues as function of the damping ratio are

$$0 < \delta < 1 \mapsto s_{1,2} = -\delta\omega_n \pm \hat{\jmath}\omega_n\sqrt{1-\delta^2} \tag{3.8}$$

$$\delta = 1 \mapsto s_{1,2} = \delta\omega_n \tag{3.9}$$

$$\delta > 1 \mapsto s_{1,2} = -\delta\omega_n \pm \omega_n\sqrt{\delta^2-1} \tag{3.10}$$

$$\delta = 0 \mapsto s_{1,2} = \pm\hat{\jmath}\omega_n \tag{3.11}$$

$$-1 < \delta < 0 \mapsto s_{1,2} = \delta\omega_n \pm \hat{\jmath}\omega_n\sqrt{\delta^2-1} \tag{3.12}$$

$$\delta < -1 \mapsto s_{1,2} = \delta\omega_n \pm \omega_n\sqrt{\delta^2-1} \tag{3.13}$$

3.3.1 — Solution for $U_0(t)$

If the eigenvalues are complex, the solution is given by the following expression:

$$U(t) = e^{-\delta\omega_n t}K_1(\cos xt + \hat{\jmath}\sin xt) + K_2(\cos xt - \hat{\jmath}\sin xt) \tag{3.14}$$

where

$$x = \omega_n\sqrt{1-\delta^2} \tag{3.15}$$

If

$$K_1 + K_2 = K\sin\phi \tag{3.16}$$

$$\hat{\jmath}(K_1 - K_2) = K\cos\phi \tag{3.17}$$

then

$$U_0(t) = e^{-\delta\omega_n t}(K\sin\phi\cos xt + K\cos\phi\sin xt) \tag{3.18}$$

Therefore, $U_0(t)$ becomes as follows

$$U_0(t) = Ke^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}t + \phi) \tag{3.19}$$

Once we have got the solution of the 2nd order differential equation for the oscillatory case, the next step will be to obtain the analog implementation of this equation in order to simulate an oscillator. Rigth after this, we will study a technique to control the amplitude and frequency of oscillation of $U_0(t)$.

If the equation (3.5) is integrated twice:

$$U_0(t) + 2\delta\omega_n\int_0^t U_0(t)\,dt + \omega_n^2\int_0^t\int_0^t U_0(t)\,dt\,dt = 0 \tag{3.20}$$

This equation can be simulated using two integrators and an inverting amplifier as is shown in Fig. 3.4.

For this circuit, the damping and the natural frequency are:

$$\omega_n = \frac{1}{RC} \tag{3.21}$$

$$\delta = \frac{1}{2K} \tag{3.22}$$

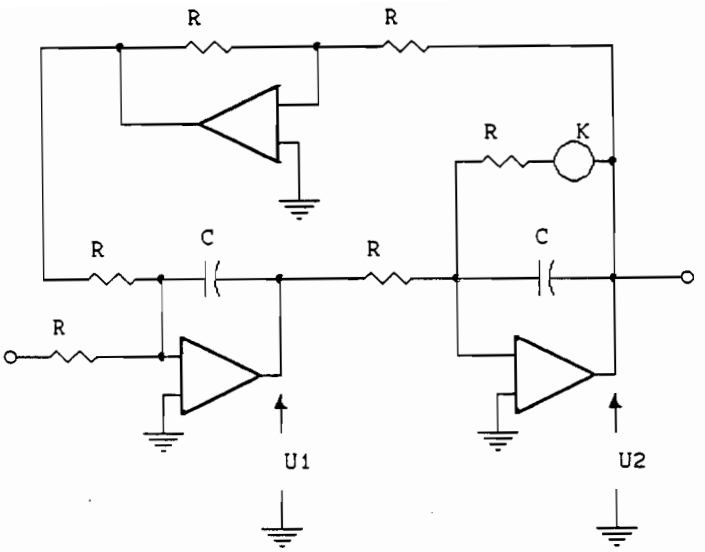


Fig. 3.4 Analog circuit to solve $U_0(t)$

For $K = 0$ an undamped oscillation will occur. For $0 < K < 1$, the oscillations are damped. For $-1 < K < 0$ the oscillation amplify. Thus in order to keep the amplitude constant, one must apply *automatic amplitude control.*

3.3.2 — Automatic Amplitude Control

The automatic amplitude control method is the one which the output amplitude is sensed and used to control the loop damping. In the case of an undamped oscillation,

$$U_0(t) = |U_0| \sin \omega_n t \tag{3.23}$$

and

$$U_1 = \frac{-1}{RC} \int_0^t U_o \, dt = |U_0| \cos \omega_n t \tag{3.24}$$

The amplitude can now be determined at any instant by solving the following expression:

$$U_0^2 + U_1^2 = |U_o^2|(\sin^2 \omega_n t + \cos^2 \omega_n t) \tag{3.25}$$

$$U_0^2 + U_1^2 = |U_0^2| \tag{3.26}$$

It is obvious that the expression 3.26 depends only on the amplitude of the output signal and not on its angle ωt. One obtains, therefore, a pure d.c. voltage which needs no filtering and which can be directly compared with the reference voltage.

A supplementary control based on this principle is shown in Fig. 3.5.

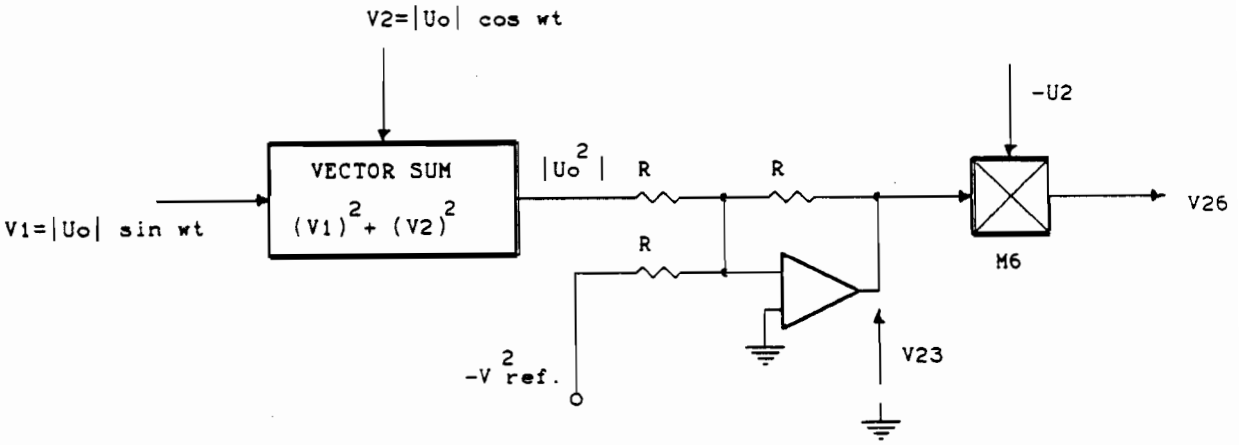


Fig. 3.5 Amplitude control circuit

The vector sum is implemented by the following circuit

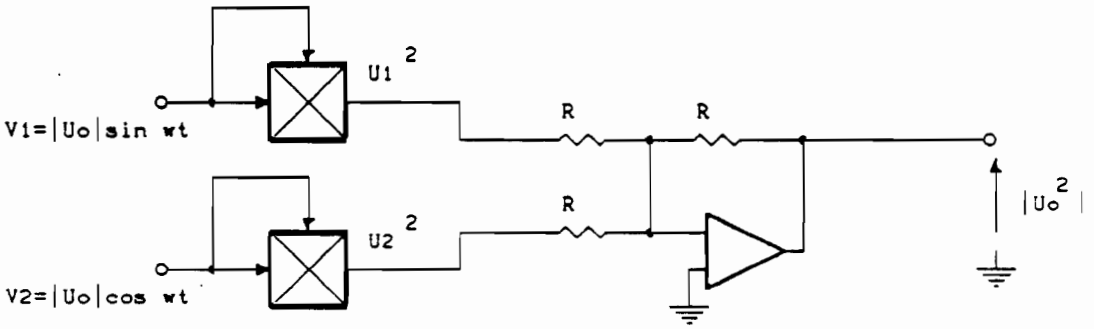


Fig. 3.6 Vector sum circuit

The voltages $U_0(t)$ and $U_1(t)$ are applied to the input of a circuit (as in Fig. 3.6) which produce the voltage $|U_0^2|$ at the output. The P controller compares this voltage with the reference U_{ref}^2 and adjusts its output voltage V_{23} so that

$$U_1^2 + U_0^2 = V_{ref}^2 \tag{3.27}$$

Therefore

$$|U_0^2| = V_{ref}^2 \tag{3.28}$$

The voltage

$$V_{26} = \frac{U_0 V_{23}}{K_M} \tag{3.29}$$

appears at the output of the multiplier M_6 to control the amplitude. If the amplitude is greater than the reference,

$$|U_0|^2 > V_{ref} \tag{3.30}$$

the oscillations decrease. If the amplitude is less than the reference, V_{23} becomes positive and the oscillations increase.

The case when the eigenvalues are located at the left-hand side of the imaginary axis is shown in Fig. 3.7. The oscillator case, when the poles are located on the imaginary axis is shown in Fig. 3.8.

The diagram corresponding to the VCO with the amplitude control circuit is illustrated in Fig. 3.9.

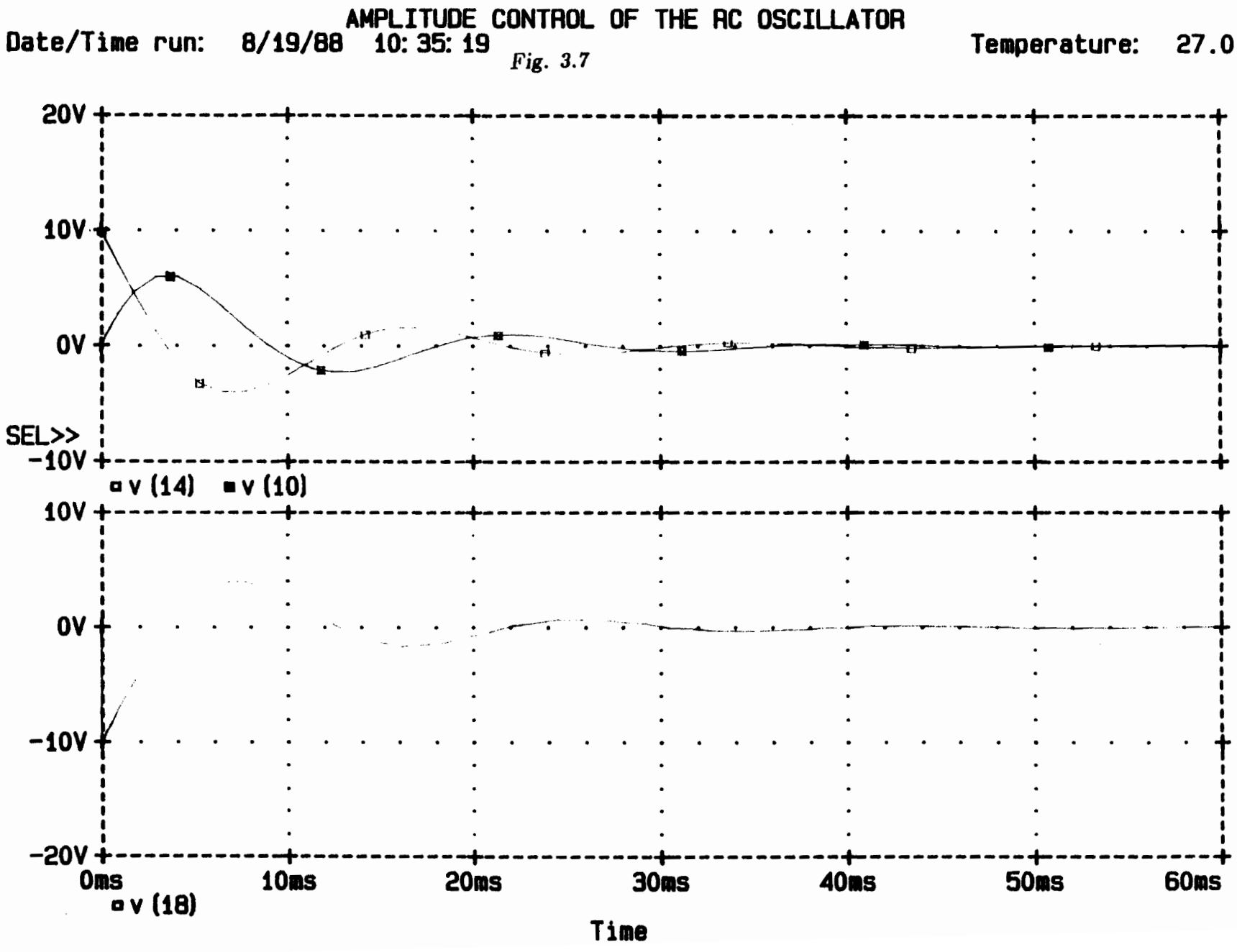

AMPLITUDE CONTROL OF THE RC OSCILLATOR
Date/Time run: 8/19/88 10:35:19
Temperature: 27.0
20V
10V
0V
SEL>>
-10V
v (14) v (10)
10V
0V
-10V
-20V
0ms
10ms
20ms
30ms
40ms
50ms
60ms
v (18)
Time

Fig. 3.7

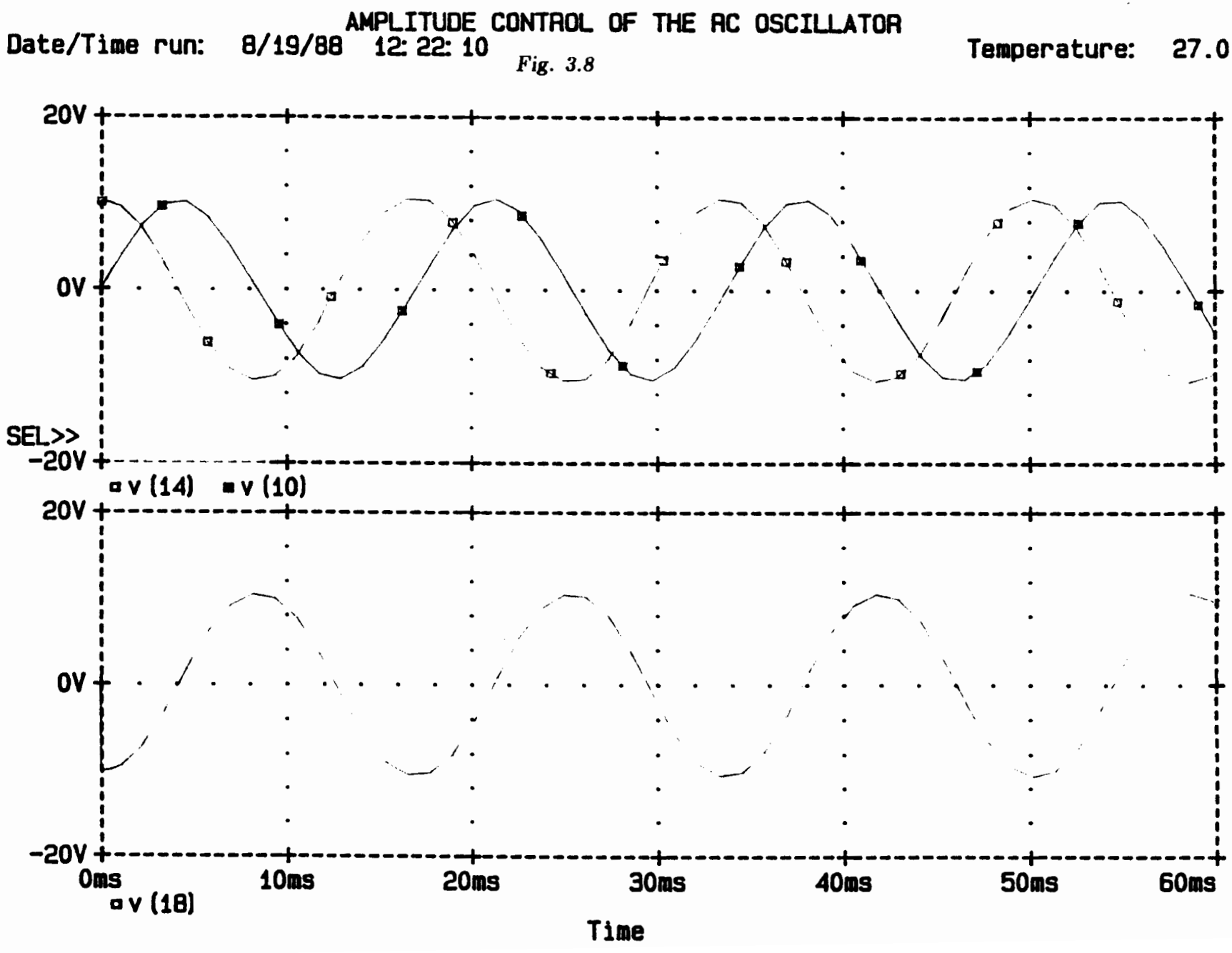

AMPLITUDE CONTROL OF THE RC OSCILLATOR
Date/Time run: 8/19/88 12:22:10
Temperature: 27.0
20V
0V
SEL>>
-20V
v (14)
v (10)
20V
0V
-20V
0ms
10ms
20ms
30ms
40ms
50ms
60ms
v (18)
Time

Fig. 3.8

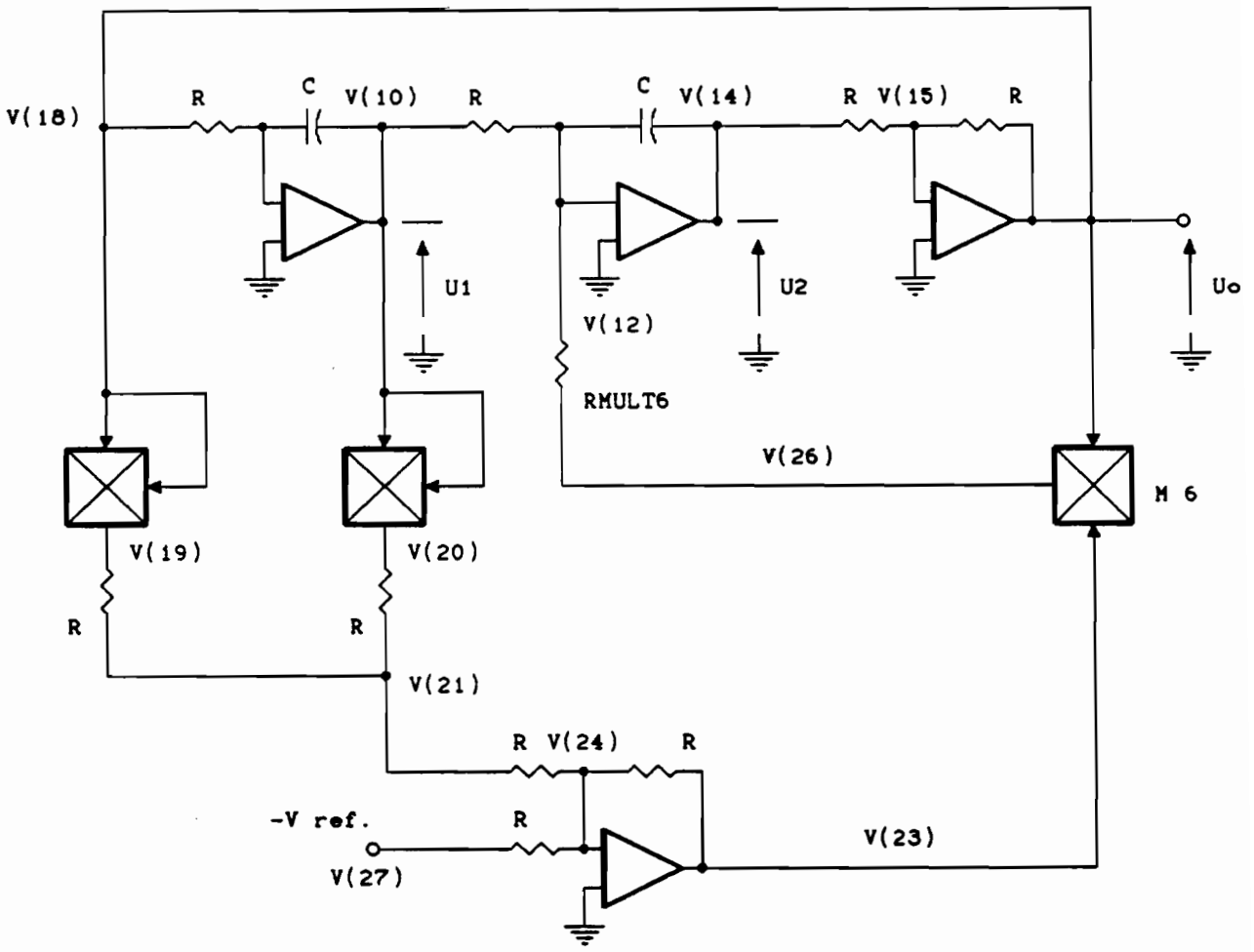


Fig. 3.8 Two-phase harmonic oscillator with the circuit for voltage amplitude control for precise amplitude control

3.4 — Analog Filter

The function of the filter is to eliminate the unwanted frequency $(f_1 + f_2)$ as well as any other noise signal without affecting the phase signal, which enables locking.

The first type of filter to be considered is a low-pass analog filter whose time constant has a direct influence on the capture frequency, f_c.

3.4.1 — Properties

An analog Butterworth low-pass filter characteristic is given by Fig. 3-9. It represents a smoth transition between the passband and stopband with monotonically decreasing gain. The filter should, in general, meet the following criteria:

- At $\omega = 0, \forall$ n, $|F_n(j\omega)|^2 = 1$
- Monotonically decreasing
- As $n \rightarrow \infty$ its characteristic approaches ideal LPF
- Ideally flat at origin
- Roll-off $-20\,log|\frac{\Omega}{\Omega_c}|$

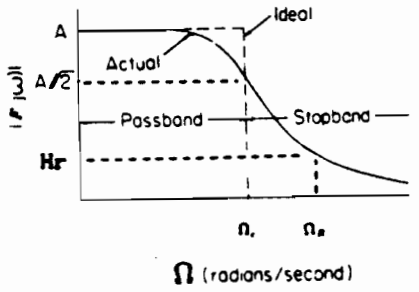


Fig 3.9 Low-pass characteristic

where

Ω_c	is the cutt-off frequency at $\|F_n(j\omega)\|^2 = 0.707$
Ω_R	is the stopband critical frequency at the end of passband freq.
n	indicates the filter order

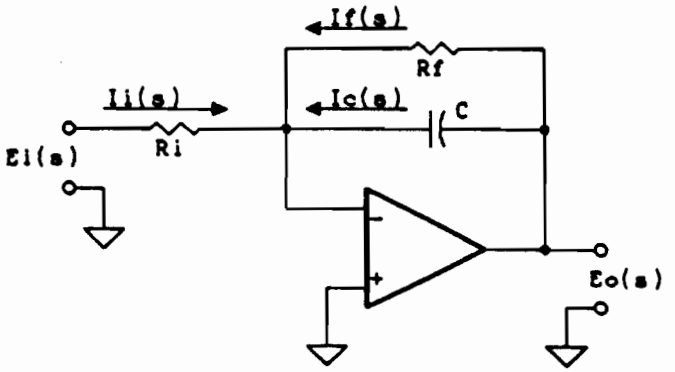


Fig. 3.10.1 Low-pass filter

For the filter given in Fig. 3.10.1, we can obtain the folowing transfer function, F(s)

$$I_i(s) + I_f(s) + I_c(s) = 0 \tag{3.31}$$

$$\frac{E_i(s)}{R_i} + \frac{E_0(s)}{R_f} + sCE_0(s) = 0 \tag{3.32}$$

then

$$\frac{E_0(s)}{E_i(s)} = F(s) = -\frac{K_f}{R_fCs + 1} \tag{3.33}$$

where

K_f : dc gain of the filter

Setting $s = \hat{\jmath}\omega$, we get the transfer function in the frequency domain

$$F(\hat{\jmath}\omega) = \frac{-K_f}{1 + \hat{\jmath}R_fC\omega} \tag{3.34}$$

Hence

$$|F(\hat{\jmath}\omega)| = \frac{K_f}{\sqrt{1 + (R_fC\omega)^2}} \tag{3.35}$$

The filter order can be estimated as follows

Let

$$|F_n(\hat{j}\omega)|^2 = \frac{1}{1+(\Omega/\Omega_c)^{2n}} \tag{3.36}$$

be the normalized filter transfer function.

Given specifications

Ω_1,Ω_2 : critical frequencies
K_1,K_2 : gains

and constraints

$$0 \leq \Omega \leq \Omega_1, 0 \geq 20log|F_n(\hat{j}\omega)| \geq K_1 \tag{3.37}$$

$$\Omega > \Omega_2, 20log|F_n(\hat{j}\Omega))| \leq K_2 \tag{3.38}$$

Then, to satisfy both constraints

$$10\,log\left[\frac{1}{1+[\Omega_1/\Omega_c]^{2n}}\right] = K_1 \tag{3.39}$$

$$10log\left[\frac{1}{1+[\Omega_2/\Omega_c]^{2n}}\right] = K_2 \tag{3.40}$$

Solving for Ω_1/Ω_c and Ω_2/Ω_c, we get

$$\left[\frac{\Omega_1}{\Omega_c}\right]^{2n} = 10^{-K_1/10} - 1 \tag{3.41}$$

$$\left[\frac{\Omega_2}{\Omega_c}\right]^{2n} = 10^{-K_2/10} - 1 \tag{3.42}$$

Dividing eqn (3.42) by eqn (3.41), yields to

$$\left[\frac{\Omega_1}{\Omega_2}\right]^{2n} = \frac{10^{-K_1/10}-1}{10^{-K_2/10}-1} \tag{3.43}$$

Therefore

$$n = \frac{log_{10}\left[(10^{-K_1/10}-1)/(10^{-K_2/10}-1)\right]}{2log_{10}(\Omega_1/\Omega_2)} \tag{3.44}$$

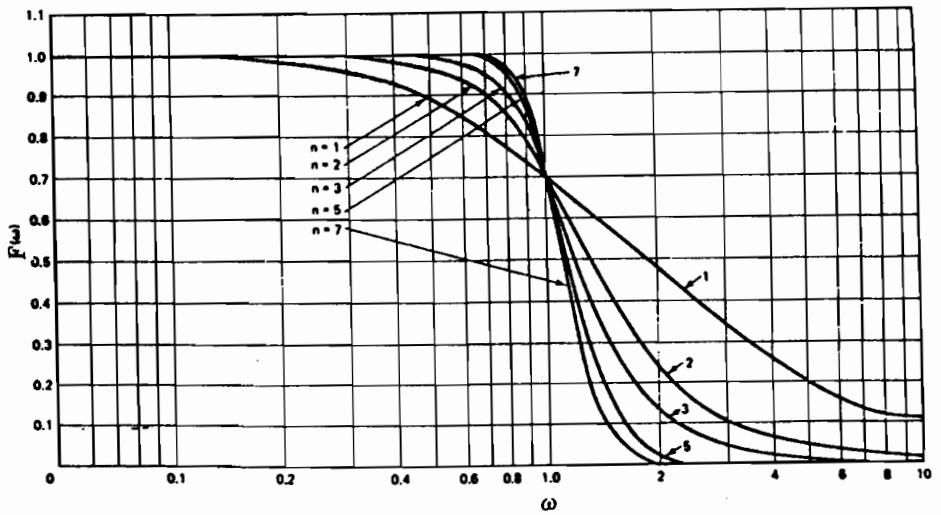


Fig. 3.11 Frequency response of the Butterworth filter

Fig. 3.11 shows the frequency response of the Butterworth filter for n stages.

We can see that the greater is number n of sections, the flater is the frequency response of the filter.

3.5 — Synchronous (Fourier) Filter

The circuit illustrated in Fig. 3.12, filters out all harmonics. Its basic architecture is formed of the following three elements:

- Integrator switch, S_{w1}
- Fourier integrator, S_{w3}
- Sample and hold circuit, S_{w2}

The integrator switch, S_{w1}, determines the period of time at which the input signal is to be integrated.

The second component, integrates the input voltage as given

$$V(T) = V_0 + \frac{1}{C}\int_{t_0}^{t_0+T} i_{in}\,dt = \frac{1}{RC}\int_{t_0}^{t_0+T} V_{in}\,dt \tag{3.45}$$

We see that in the absence of the switch, S_{w3}, the integrated voltage will become increasingly pronounced as time increases. To prevent this from happening it is therefore desirable to reset the circuit periodically by turning ON S_{w3} to discharge the capacitor. When S_{w3} is OFF again, the integration process will start all over again.

The purpose of the sample-and-hold circuitS_{w2} is to hold the signal during the integration process. The most common hold circuit, is the zero-order hold.

Let

$$V(t) = V_0 + \sum_{k=1}^{\infty} V_k\ sin\left[k\frac{2\pi}{T}t - \phi_k\right] \tag{3.46}$$

and

$$V_{ref}(t) = |V_{ref}|\cos\left[\frac{2\pi}{T}t + \theta\right] \tag{3.47}$$

the input signals to the PLL multiplier.

Then, the error voltage is given by

$$V_e(t) = V_0|V_{ref}|\cos\left[\frac{2\pi}{T}t + \theta\right] + \sum_{k=1}^{\infty}|V_{ref}|V_k \sin\left[k\frac{2\pi}{T}t + \phi_k\right]\cos\left[\frac{2\pi}{T}t + \theta\right] \tag{3.48}$$

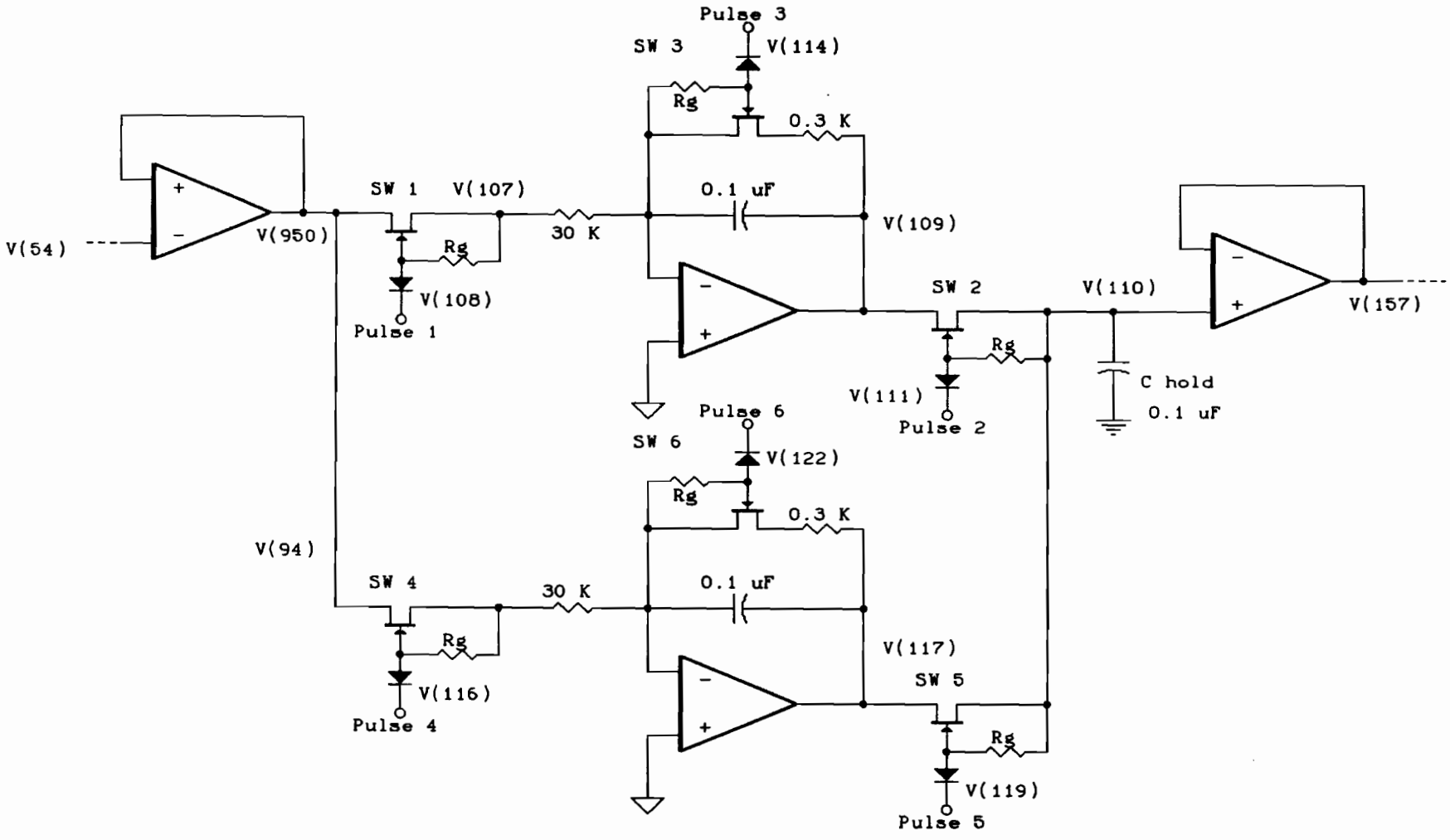


Fig. 3.12 Synchronous filter

This signal is to pass through the integrator filter. Thus

$$V_f(t_0+T) = \frac{1}{T}\int_{t_0}^{t_0+T} V_e(t)dt \tag{3.49}$$

Hence

$$V_f(t_0+T) = \frac{|V_{ref}|V_1}{2}\sin(\phi_1-\theta) \tag{3.50}$$

Due to the regulator loop

$$V_f(t_0+T) = 0 \tag{3.51}$$

and

$$\sin(\phi_1-\theta) = 0 \mapsto \phi_1 = \theta \tag{3.52}$$

The performance of the whole circuit is illustrated in Fig. 3.13. The upper part describes the sampled-input signal, V(107); the integrated voltage, V(109); and the data-hold voltage, V(110). The lower part, which is related to the second branch of Fig. 3.12, describes the same operation as before but with a time delay of $e^{-\frac{sT}{2}}$. In this case, the sampled-input, the integrated and the data-hold signals are represented by V(115), V(117) and V(110) respectively.

3.5.1 — Digital Control of the Filter

The filter is digitally controlled by the pulses applied to switches 1 to 6, shown in Fig. 3.14. Thus,

Pulses V(108,107) and V(116,115) control input voltages of the upper and lower branch respectively.

Pulses V(111,110) and V(119,0) control the data-hold circuit and

Pulses V(114,113) and V(122,120) control the operation of reset switches 3 and 6 respectively.

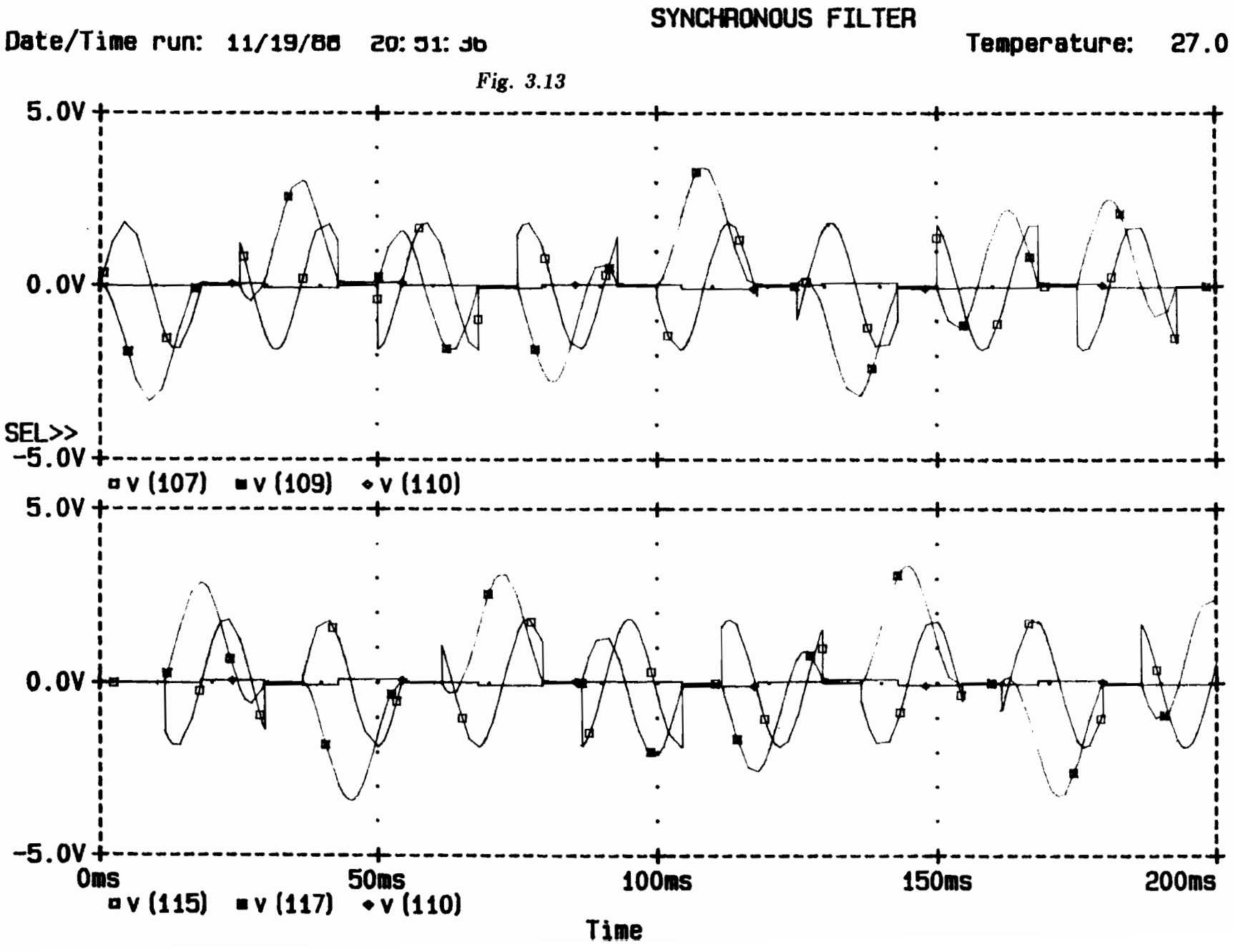

SYNCHRONOUS FILTER
Date/Time run: 11/19/88 20:51:36
Temperature: 27.0
5.0V
0.0V
SEL>>
-5.0V
v (107) v (109) v (110)
5.0V
0.0V
-5.0V
0ms
50ms
100ms
150ms
200ms
v (115) v (117) v (110)
Time

Fig. 3.13

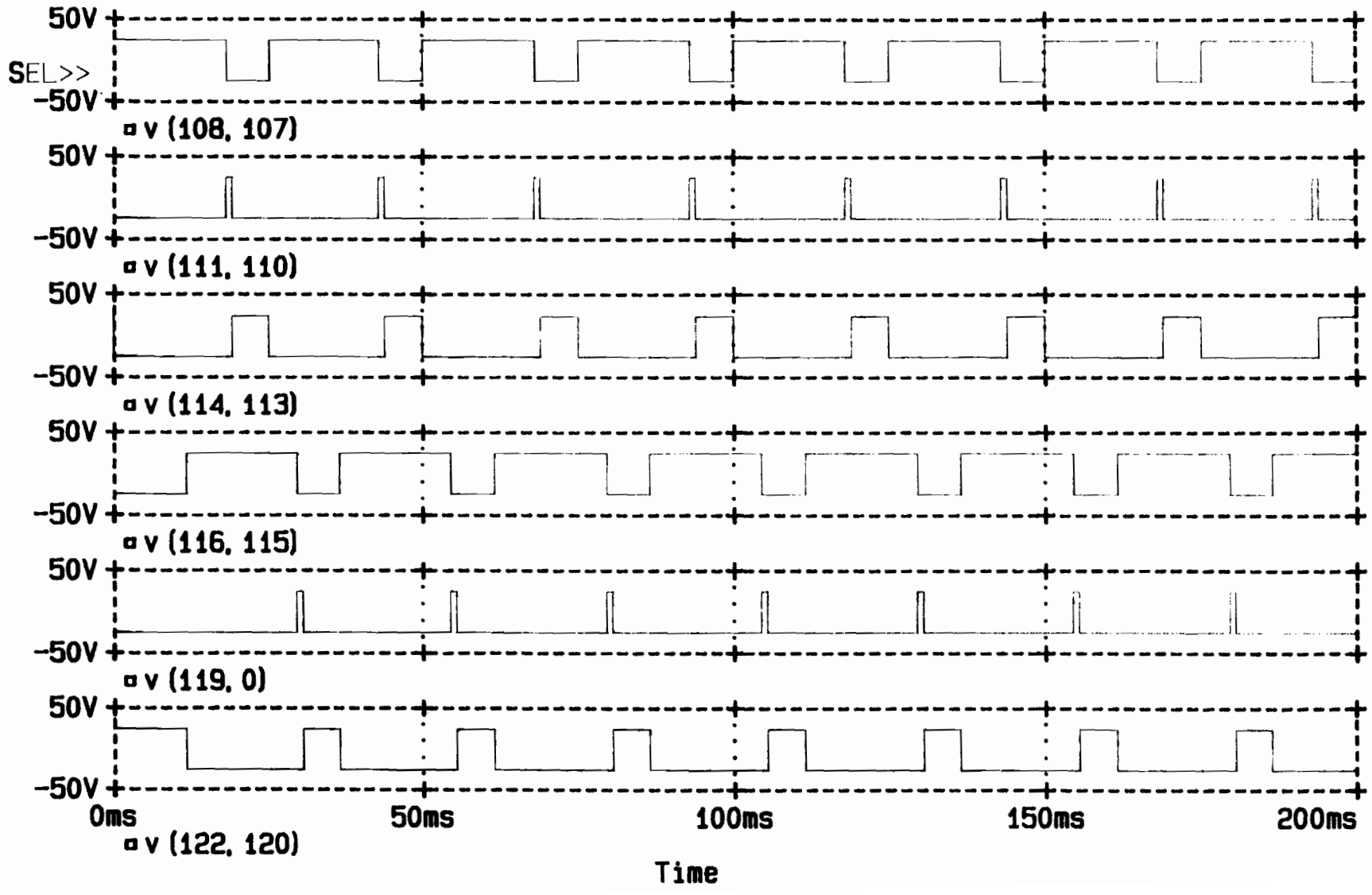

CONTROL PULSES OF THE SYNCHRONOUS FILTER
Date/Time run: 11/19/88 20:51:36
Temperature: 27.0
50V
SEL>>
-50V
v (108, 107)
50V
-50V
v (111, 110)
50V
-50V
v (114, 113)
50V
-50V
v (116, 115)
50V
-50V
v (119, 0)
50V
-50V
0ms
50ms
100ms
150ms
200ms
v (122, 120)
Time

Fig. 3.14

3.5.2 — Block Diagram of the Filter

Let $f_1(t)$ be a periodic signal applied to the first integrator of the filter (Fig. 3.13) which repeats itself with the period T starting at t=0. Then, such a function can be represented as a sum of aperiodic functions delayed by T, 2T, 3T, ..., nT,

$$f_1(t) = f_0(t) + f_0(t-T) + f_0(t+-2T) + \cdots + f_0(t-nT) + \cdots \tag{3.53}$$

Let

$$L[f_0(t)] = F_0(s)$$

and

$$L[f_1(t)] = F_1(s)$$

Using the time-shift property, we get

$$F_1(s) = F_0(s) + F_0(s)e^{-sT} + F_0(s)e^{-2sT} + \cdots\cdots \tag{3.54}$$

By factoring, the equation becomes

$$F_1(s) = F_0(s)[1 + e^{-sT} + e^{-2sT} + \cdots + e^{-nsT} + \cdots] \tag{3.55}$$

The infinite series appearing in this equation may be identified by the following expanssion from the geometric series,

$$\frac{1}{1-e^{-Ts}} = 1 + e^{-Ts} + e^{-2Ts} - e^{-3Ts} + \cdots \tag{3.56}$$

such that $F_1(s)$ becomes

$$F_1(s) = \frac{F_0(s)}{1-e^{-sT}} \tag{3.57}$$

As the second branch of the filter is delayed by $e^{\frac{-sT}{2}}$, the input applied to the second integrator of the filter is given by

$$F_2(s) = \frac{F_0(s)}{1-e^{-sT}} e^{-sT/2} \tag{3.58}$$

The block diagram is shown in Fig 3.15. It includes the reset and the zero-order hold circuits.

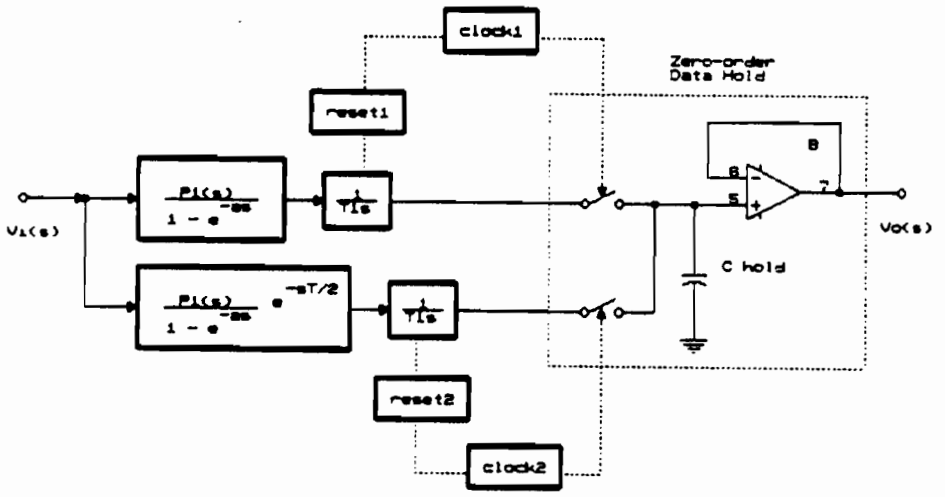


Fig. 3.15 Block diagram of the synchronous filter

3.6 — Summary

The phase-locked loop , introduced in the previous chapter, was considered as a feedback control system . The VCO was analyzed to some details with a focus on design considerations, begining with the oscillation condition, followed by the solution of the oscillator differential equation, an automatic amplitude control, to get finally, to the voltage controlled oscillator.

A special attention is given to the Butterworth filter, the first-order active filter as well as the synchronous (Fourier) filter as important component for a reliable phase-locked loop operation if harmonic distortion is present in the input signal.

MODELLING

AND

COMPUTER SIMULATION

CHAPTER 4

MODELLING OF ELECTRONIC COMPONENTS

4.1 — Introduction

The computer simulation was carried out using *PSPICE*. In order to implement the analog circuits simulation we needed to model electronic components like the switch, multiplier and the operational amplifier which, either they were available or they had to be simplified to save ram memory and run time. Since the simulation was run on the computers operating at 4.77 Mhz.

4.2 — Modelling of an Analog Switch

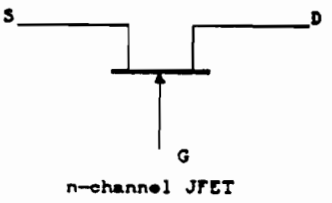


Fig. 4.1 Symbol of n-JFET transistor

Modelling of an analog switch is performed by means of a standard model of the n-channel JFET which has a low resistance in the cut-off region $\frac{dV_{DS}}{dI_D}$ and a very high dynamic resistance in the saturation region.

Fig. 4.1 shows the symbol of this n-channel transistor. The n-channel was chosen because it has lower ON-resistance than a p-channel of similar channel dimensions (n - channel has a higher carrier mobility).

4.2.1 — JFET ON-resistance

Fig. 4.2 illustrates the differents operating regions of the JFET transistor. In switching applications, ON-OFF transition occurs in the unsaturated or triode region, which is located to the left of the pinch-off voltage locus.

In the saturated region the current is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{4.1}$$

which is essentially independent of V_{DS} and the device has a very high dynamic resistance.

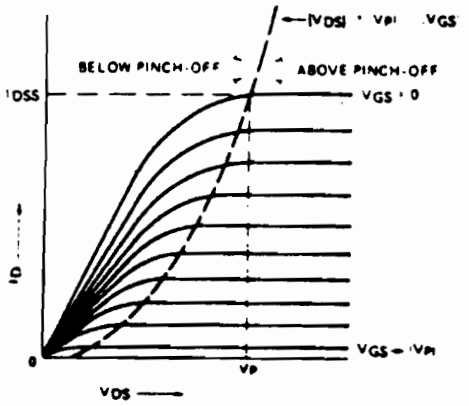


Fig. 4.2 Characteristic curve of the JFET

In the OFF-state, V_D is large but I_D becomes small ($\simeq 0$); Therefore, r_{DS} tend to be infinite. In the ON-state, r_{DS} is very small since V_D is very small and I_D is very large. This is valid whichever V_{GS} is. Fig. 4.3 illustrates the equivalent circuit for both states.

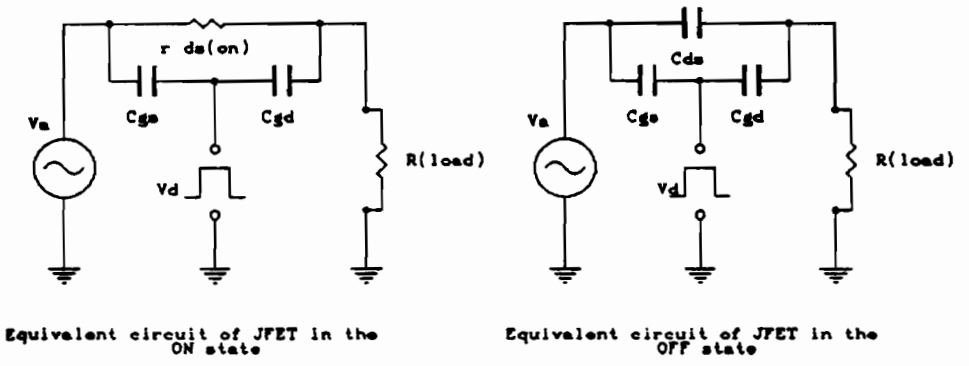


Fig.4.3 Equivalent circuits in the ON-state and OFF-state

where

R_{ds}	is the drain-source resistance
C_{gs}	is the gate-source capacitance
C_{gd}	is gate-drain capacitance
R_L	is the load resistance

4.2.2 — Driver Circuit

Fig. 4.4 shows the simplified form of a driver circuit. The switch in the gate circuit was implemented with the PULSE function available in the program.

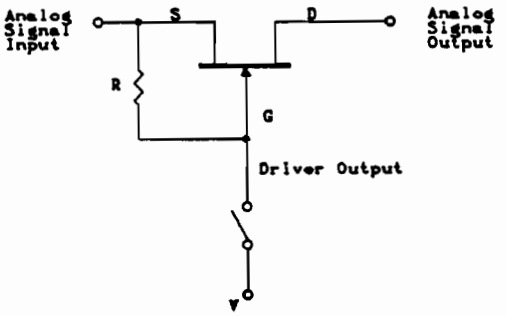


Fig. 4.4 Analog switch

4.2.3 — Operation of the Driver Switch

At the moment the gate switch closes, the gate voltage of T_1 assumes the negative rail voltage. The switch T_1 turns OFF, since the analog signal voltage is always higher than the negative supply rail for the V_{GS} (OFF) value, i.e.

$$|V_A| < |V^-| - |V_{Goff}| \tag{4.2}$$

where V_A is the peak (value) negative excursion of the analog signal, V^- is the negative supply voltage, V_G (OFF) is the pinch-off voltage of the JFET.

When the diode D is reverse biased the gate voltage of T_1 is the same as the source voltage. Hence, the analog switch is ON.

4.2.4 — Performance of the JFET Switch

Its performance is ilustrated in Fig. 4.5 : the upper waveform represents the input signal; the middle waveform shows the gate voltage while at the bottom, the output voltage.

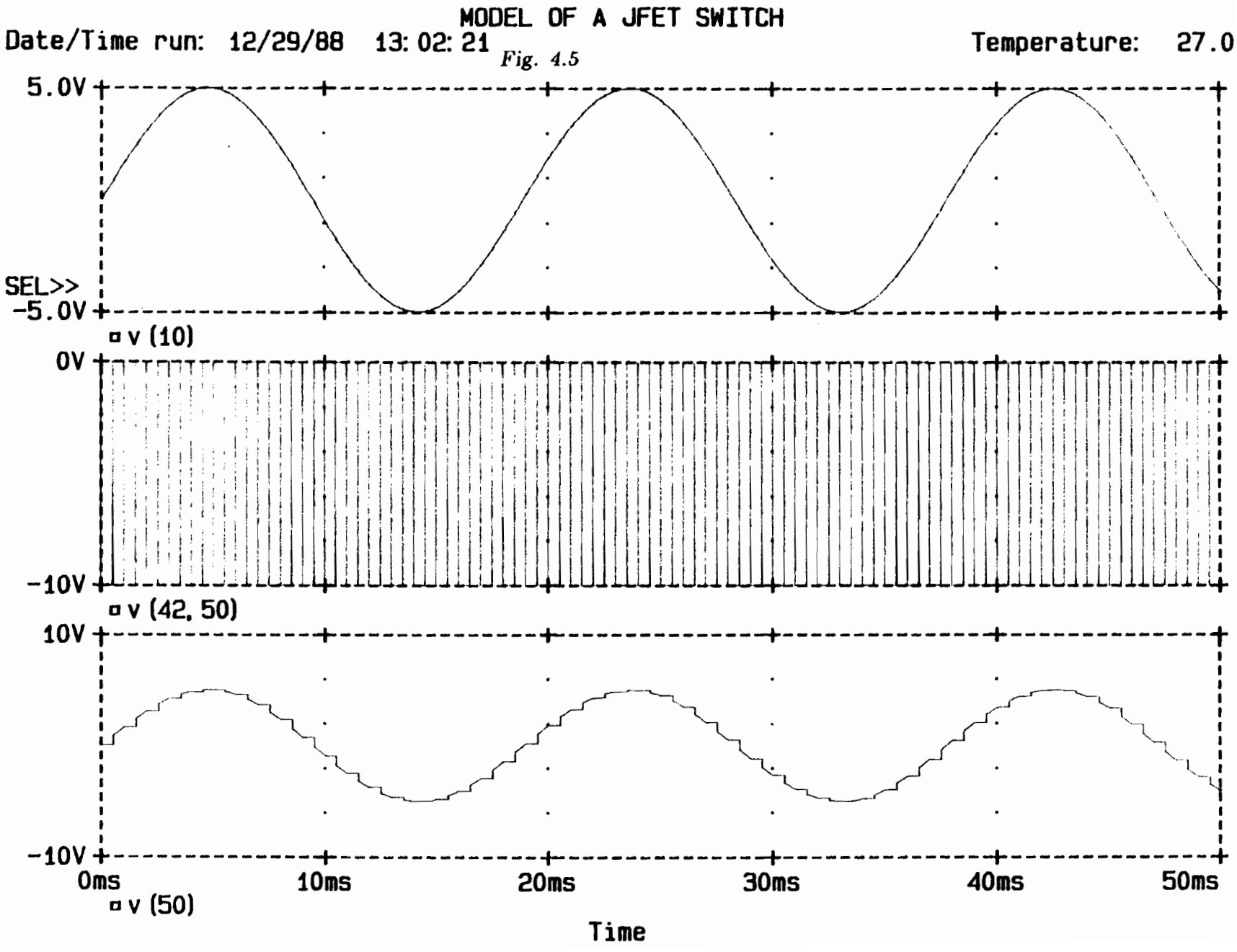

MODEL OF A JFET SWITCH
Date/Time run: 12/29/88 13:02:21
Temperature: 27.0
5.0V
SEL>>
-5.0V
v (10)
0V
-10V
v (42, 50)
10V
-10V
0ms
10ms
20ms
30ms
40ms
50ms
v (50)
Time

Fig. 4.5

4.3 — Operational Amplifier

Basically, two types of operational amplifiers were used in the simulation. The first model, the μA741, included in the Library, has about 24 components and the second one is a simplified version which shortens, considerably, the running time and save the ram memory.

— Simplified model

By definition

$$V_i = \alpha V_g + \beta I_L \tag{4.3}$$

where

α is the fraction of the source voltage applied to the input

β is a fraction of the load voltage applied to the input

α and β are dimenssionless

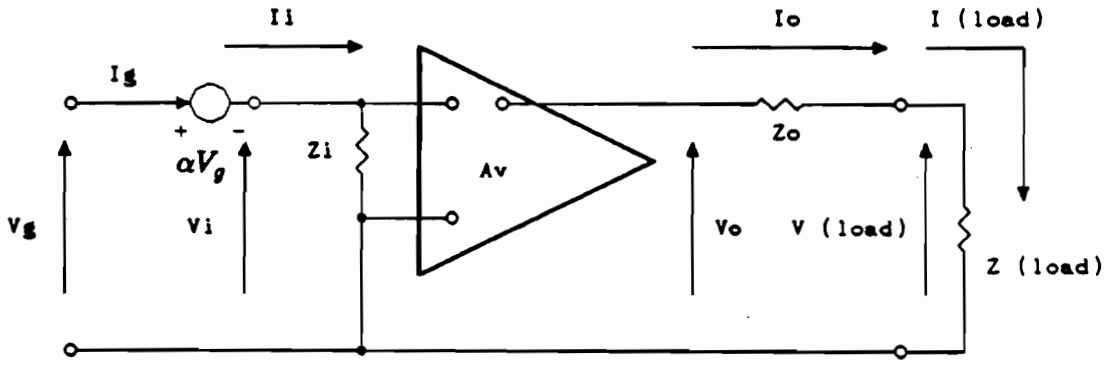


Fig. 4.6 Operational Amplifier

$$V_L = A_v V_i - Z_o I_o \tag{4.4}$$

Hence, we can derive an equivalent circuit

$$V_L = A_{vr} V - Z_{or} I_o \tag{4.5}$$

Substituting eqn (4.3) in eqn (4.4), we get

$$V_L = A_v(\alpha V_g + \beta V_L) - Z_o I_o \tag{4.6}$$

that is

$$V_L = V_g \frac{\alpha V_g}{1 - \beta A_r} - \frac{Z_o}{1 - \beta A_v} I_o \tag{4.7}$$

where

$$A_{vr} = \frac{\alpha A_v}{1 - \beta A_v} \tag{4.8}$$

and

$$Z_{or} = \frac{Zo}{1 - \beta Av} \tag{4.9}$$

where

A_{vr} is the gain of the amplifier

Z_{or} is the output feedback impedance

These equations yield to the circuit of Fig. 4.7

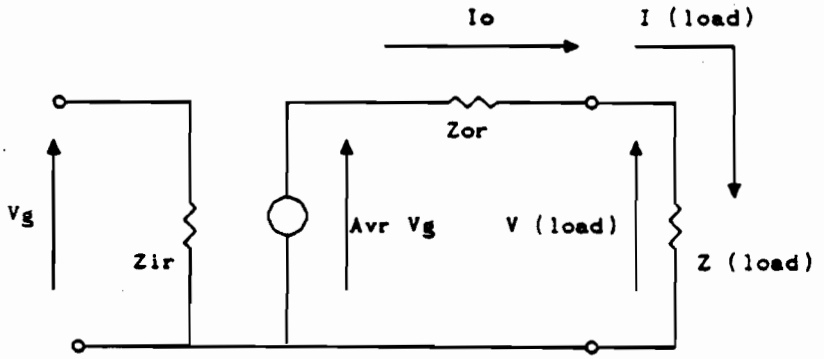


Fig. 4.7 Equivalent circuit of the operational amplifier

The input impedance is, by definition

$$Z_{ir} = \frac{V_g}{I_g} \tag{4.9}$$

but

$$I_g = I_i = \frac{V_i}{Z_i} \tag{4.10}$$

then

$$Z_{ir} = \frac{V_g}{V_i} Z_i \tag{4.11}$$

substituting V_g, from eqn(4.3), in eqn(4.11) yields to

$$Z_{ir} = \left[\frac{1}{\alpha} - \frac{\beta}{\alpha}\frac{V_L}{V_i}\right] Z_i \tag{4.12}$$

but

$$V_L = V_o - Z_o I_o \tag{4.13}$$

and

$$V_o = A_v V_i \tag{4.14}$$

therefore

$$Z_{ir} = \left[\frac{1 - \beta A_v}{\alpha} + \frac{\beta}{\alpha}\frac{Z_o I_o}{V_i}\right] Z_i \tag{4.15}$$

then, replacing

$$I_o = \frac{A_v V_i}{Z_o + Z_L} \tag{4.16}$$

into eqn(4.16), we get

$$Z_{ir} = \left[\frac{1 - \beta A_v}{\alpha} + \frac{\beta A_v}{\alpha}\frac{Z_o}{Z_o + Z_L}\right] Z_i \tag{4.17}$$

where Z_L is the total load impedance and

$$Y_{or} = \frac{1}{Z_{or}} \tag{4.18}$$

To complete our model, another important characteristic should be included: the finite "slew-rate" limitation ΔS_t. It expresses the speed with which the output of the operational amplifier can respond to a sudden change imposed upon the input.

To simulate the characteristic, we propose the nonlinear circuits building block shown in Fig. 4.8

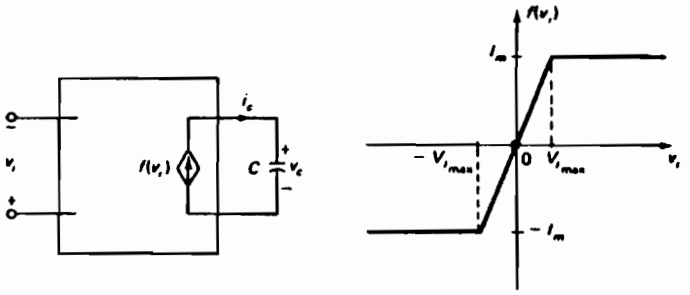


Fig. 4.8 Simple nonlinear circuit building block for simulating slew-rate limitation.

since the output current of the controlled source can not not exceed I_m, we have

$$\left|\frac{d_{vc}(t)}{dt}\right| = \frac{1}{C}\left|i_c\right| \leq \frac{I_m}{C} = \Delta S_t \tag{4.19}$$

Because I_m and C are fixed, they set a maximun value on the derivative. Therefore, a capacitor, C, must be connected to the circuit to take into account the slew-rate characteristic of the op-amp.

The macro model to be used in the simulation is shown in Fig. 4.9.

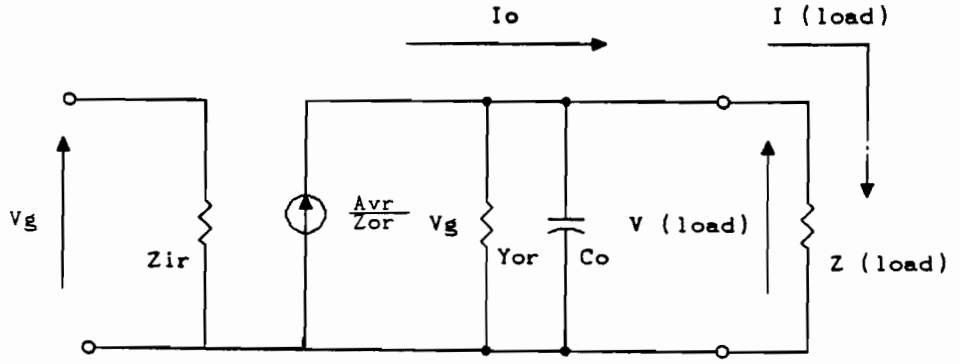


Fig. 4.9 Macro model of the op-amp

4.4 — Multiplier

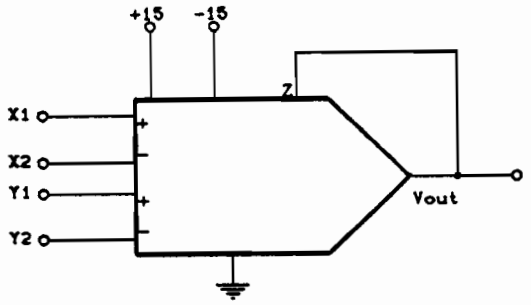


Fig. 4.10 Analog multiplier

Fig. 4.10 shows the symbol of the analog multiplier, element widely used in the program. Its implementation is obtained through a polynomial function given by

$$V_{out}(t) = K_0 + K_1V_1 + K_2V_2 + ... + K_nV_n + K_{n+1}V_1V_1 + K_{n+2}V_1V_2 + K_{n+N}V_1V_n + + K_{2n+1}V_2V_2 + K_{2n+1}V_2V_3 + ... \quad (4.20)$$

considering only the terms in V_1V_2, and setting

$$K_{n+2} = \frac{1}{10} = 0.1 \quad (4.21)$$

we get

$$V_{out}(t) = 0.1V_1V_2 \quad (4.22)$$

which is the linear equation of the multiplier to be implemented in PSPICE using the POLY function, that is,

$$EPLL\ 50\ 0\ POLY(2)\ 72\ 0\ 10\ 0\ 0\ 0\ 0\ 0\ 0.1 \quad (4.23)$$

4.5 — Summary

In this chapter new models have been developed to be applied to phase-locked loop simulation: a JFET switch, a simplified version of the operational amplifier and a multiplier.

CHAPTER 5

PHASE-LOCKED LOOP SIMULATION

5.1 — Introduction

In our study we are, mainly, concerned with the transient behaviour of the phase-locked loop. Therefore, steps will be given to accomplish the goals in this domain.

The analysis will be done for differents types of configurations. The modelling will include, the PLL with an analog or synchronous filter and PI controller for phase perturbation, amplitude perturbation, 2nd harmonic and a combination of them.

We shall also consider the the harmonic generation of PLL circuits without and with a harmonic excitation.

5.2 — Performance under Normal Operation

5.2.1 — Analog Filter

The test of the PLL under no perturbation was carried out using the circuit illustrated in Fig. 5.1.1. An analog filter is inserted between the PLL multiplier and the VCO. This model include an integrator where time constant is twice the one of the analog filter. A detailed configuration is shown in Fig. 5.1.2.

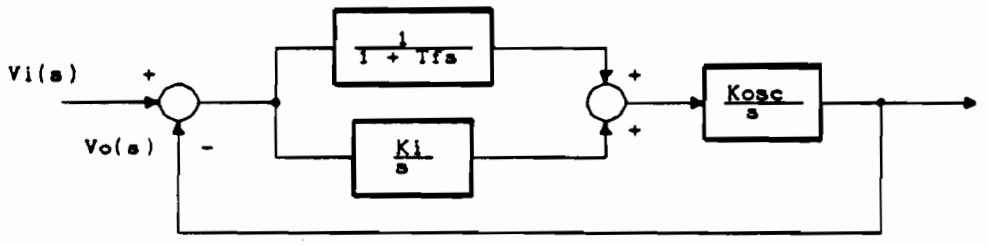


Fig. 5.1.1 Block diagram PLL with analog filter

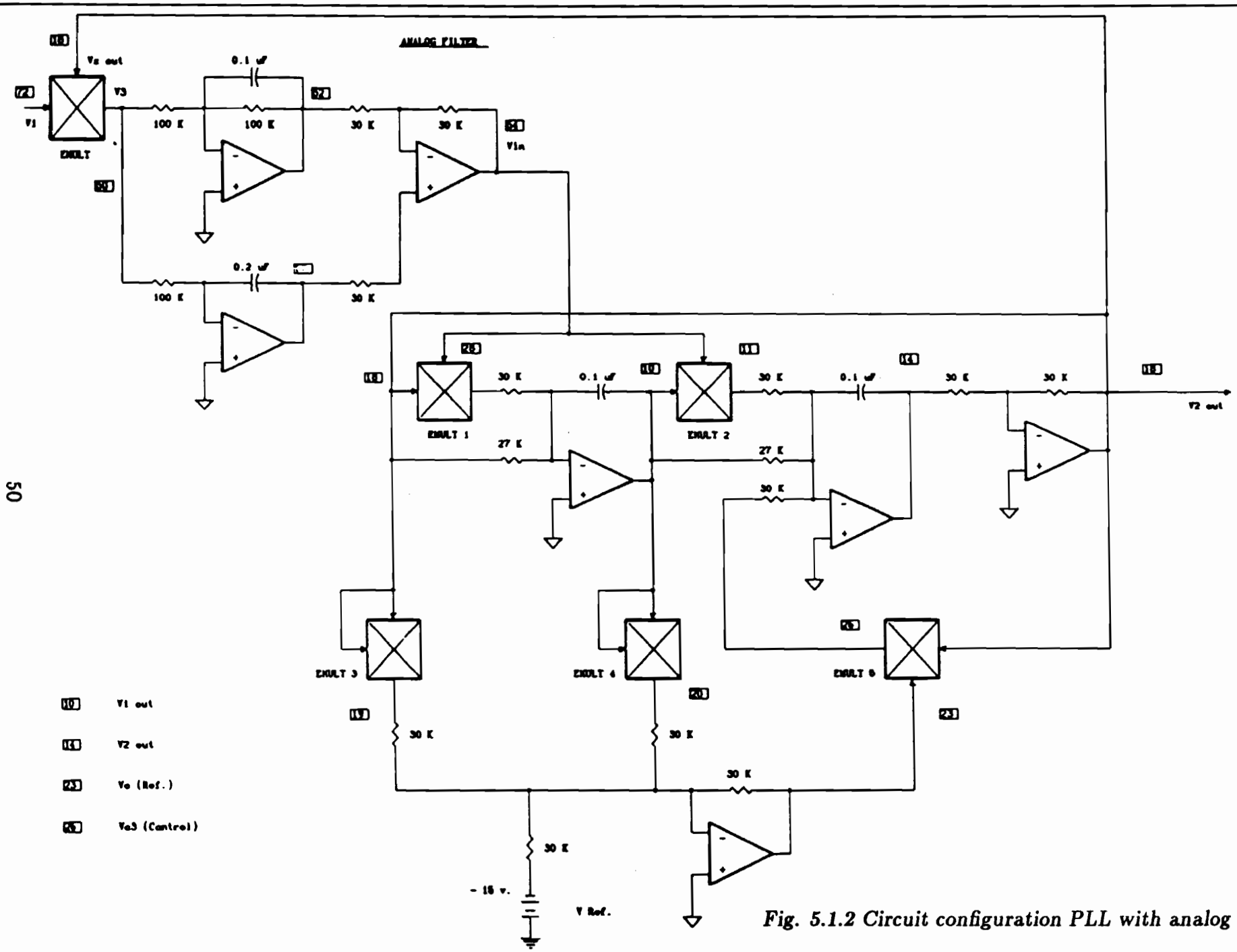
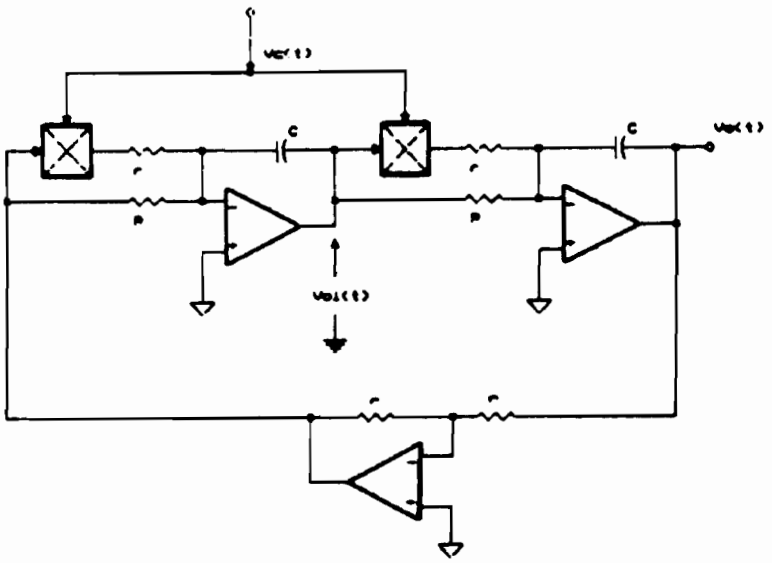


Fig. 5.1.2 Circuit configuration PLL with analog filter

5.2.2 — Frequency of Oscillation

In this section we will obtain an expression for the frequency of oscillation of the VCO, partially shown in Fig. 5.1.3. Thus,



$$V_0(t) = -\int_{-\infty}^{t} \frac{V_{01}(t)V_c(t)}{KrC}\,dt - \int_{-\infty}^{t} \frac{V_{01}(t)}{RC}\,dt \tag{5.1}$$

$$V_{01}(t) = \int_{-\infty}^{t} \frac{V_0(t)V_c(t)}{KrC}\,dt + \int_{-\infty}^{t} \frac{V_0(t)}{RC}\,dt \tag{5.2}$$

Applying the Laplace transform, these equations are transformed into the following algebraic equations

$$V_o(s) = -\frac{1}{s}\left(\frac{k}{\tau_1} + \frac{1}{\tau_2}\right)V_{o1}(s) + \frac{1}{s}V_o(s) \tag{5.3}$$

$$V_{o1}(s) = \frac{1}{s}\left(\frac{k}{\tau_1} + \frac{1}{\tau_2}V_o(s)\right) + \frac{1}{s}V_{o1}(s) \tag{5.4}$$

where

$$\tau_1 = rC \tag{5.5}$$

$$\tau_2 = RC \tag{5.6}$$

$$k = \frac{V_c}{K} \tag{5.7}$$

Solving equations (5.3) and (5.4), for V_o and V_{o1} while assuming the initial value $V_o(0) = 0$, we obtain the following expressions

$$V_o(s) = \frac{s}{s^2 + \omega^2} V_o(0) \tag{5.8}$$

and

$$V_{o1}(s) = \frac{\omega}{s^2 + \omega^2} V_o(0) \tag{5.9}$$

where

$$\omega = \frac{K}{\tau_1} + \frac{1}{\tau_2} \tag{5.10}$$

The inverse Laplace transform functions are

$$V_o(t) = V_o(0) \cos \omega t \tag{5.11}$$

$$V_{o1}(t) = V_o(0) \sin \omega t \tag{5.12}$$

When $V_c(t) = 0$, then $k = 0$, and $\omega = \frac{1}{\tau_2}$, giving the following frequency to the oscillator

$$f_0 = \frac{1}{2\pi} \frac{1}{RC} \tag{5.13}$$

which is the so-called the *central frequency* of the oscillator.

5.3 — Transient Performance

In this section, the waveforms corresponding to differents points of the circuit of Fig. 5.1.2 will be, briefly, analized.

As we saw in the previous chapter, for sinusoidal input, V(72), and feedback, V(10), the output of the PLL multiplier, V(50), is also a sinusoidal but of double frequency. This is illustrated in Fig. 5.2.

As we want stable amplitudes of V(18), V(14) and V(10), the voltages V(18) and V(10), are squared, added and compared to the reference voltage Vref = −10 V. Its output V(23) is multiplied by V(18) generating V(26) (negative of V(23) not shown in Fig. 5.3) which controls the voltage amplitude through the second integrator. In mathematical terms,

$$\frac{-1}{RC}\int_0^t V_{26}(t)dt - \frac{1}{rC}\int_0^t V_{10}(t)dt - \frac{1}{RC}\int K_M V_{11}(t)dt = V_{14}(t) \qquad (5.14)$$

where

K_M is the gain of the multiplier,that is,

$$K_M = \frac{1}{10} = 0.1 \qquad (5.15)$$

At t=0 thepower is applied to the PLL circuit, and a short delay after, the transient desappears. As illustrated in Fig. 5.4, it takes about 2 1/2 cycles. In this figure, V(52), V(57) and V(54) correspond to the output of the filter, integrator and frequency-control voltage of the oscillator respectively. The frequency-control voltage keeps the oscillator frequency locked to the frequency of the incoming signal from the network, V(72).

The synchronization of the PLL to the incoming network signal occurs very quickly as illustrated in Fig. 5.5. The output signal from the oscillator are either V(10), V(14) or V(18) as shown in Fig. 5.6.

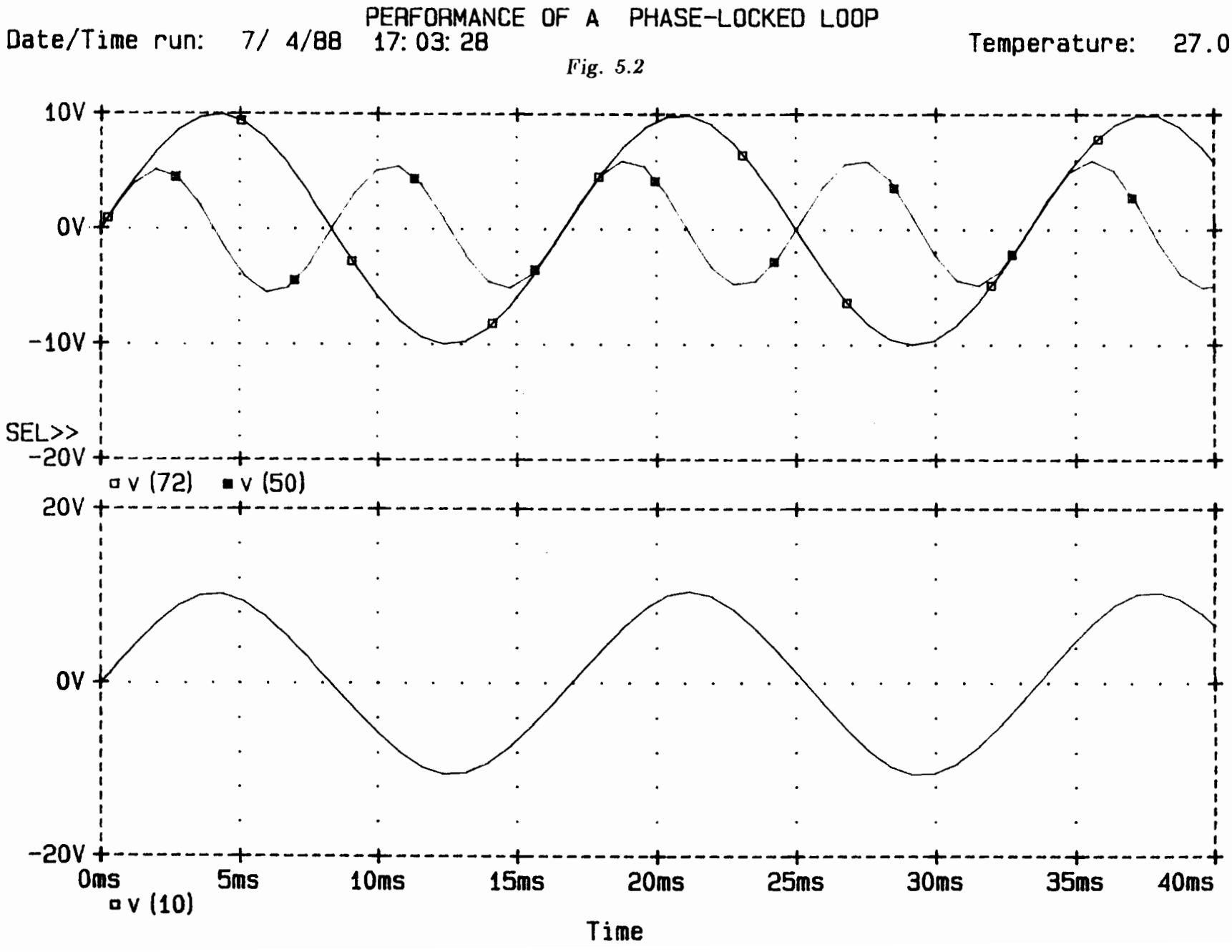

PERFORMANCE OF A PHASE-LOCKED LOOP
Date/Time run: 7/ 4/88 17: 03: 28
Temperature: 27.0
10V
0V
-10V
SEL>>
-20V
v (72)
v (50)
20V
0V
-20V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
v (10)
Time

Fig. 5.2

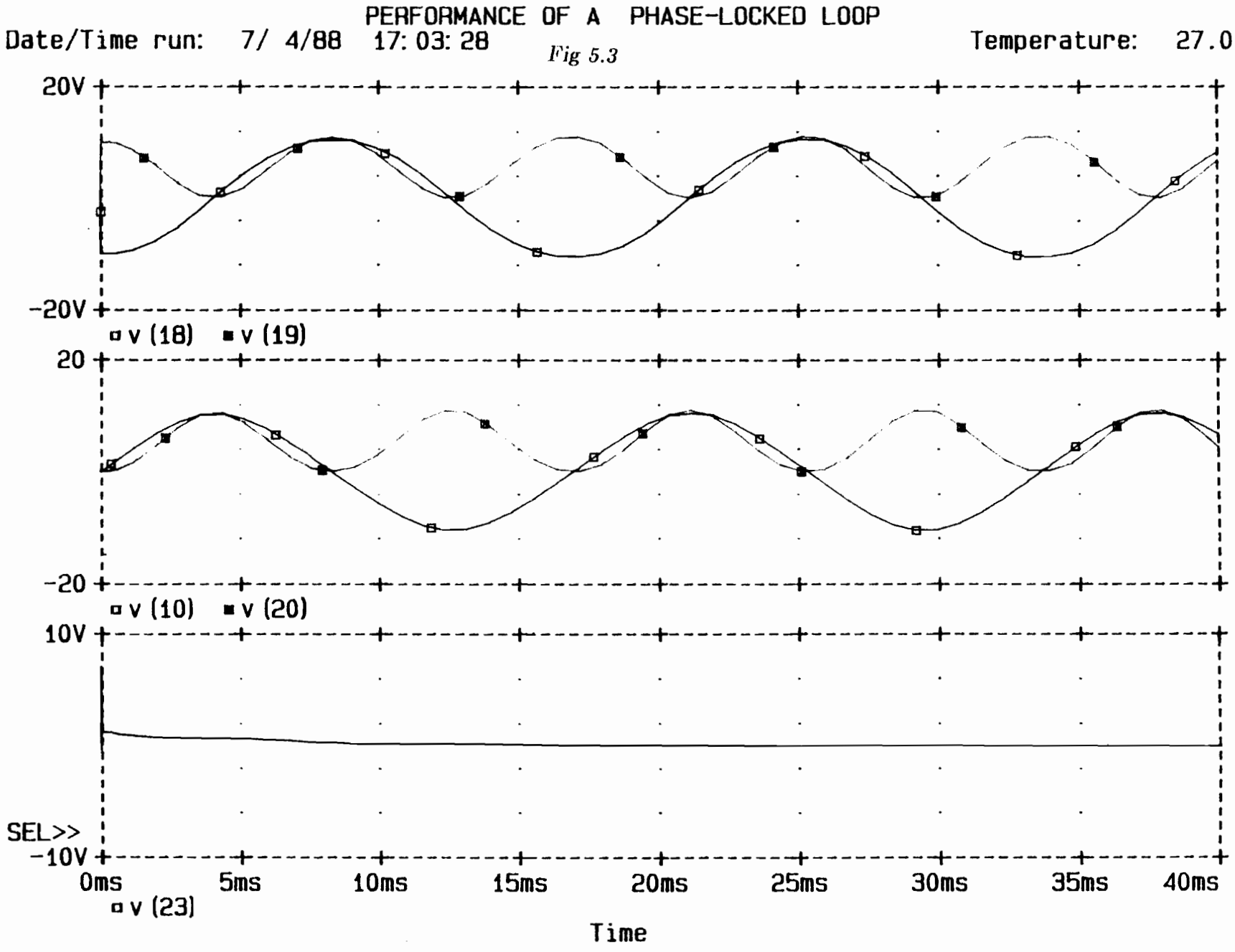

PERFORMANCE OF A PHASE-LOCKED LOOP
Date/Time run: 7/ 4/88 17: 03: 28
Temperature: 27.0
20V
-20V
v (18) v (19)
20
-20
v (10) v (20)
10V
SEL>>
-10V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
v (23)
Time

Fig 5.3

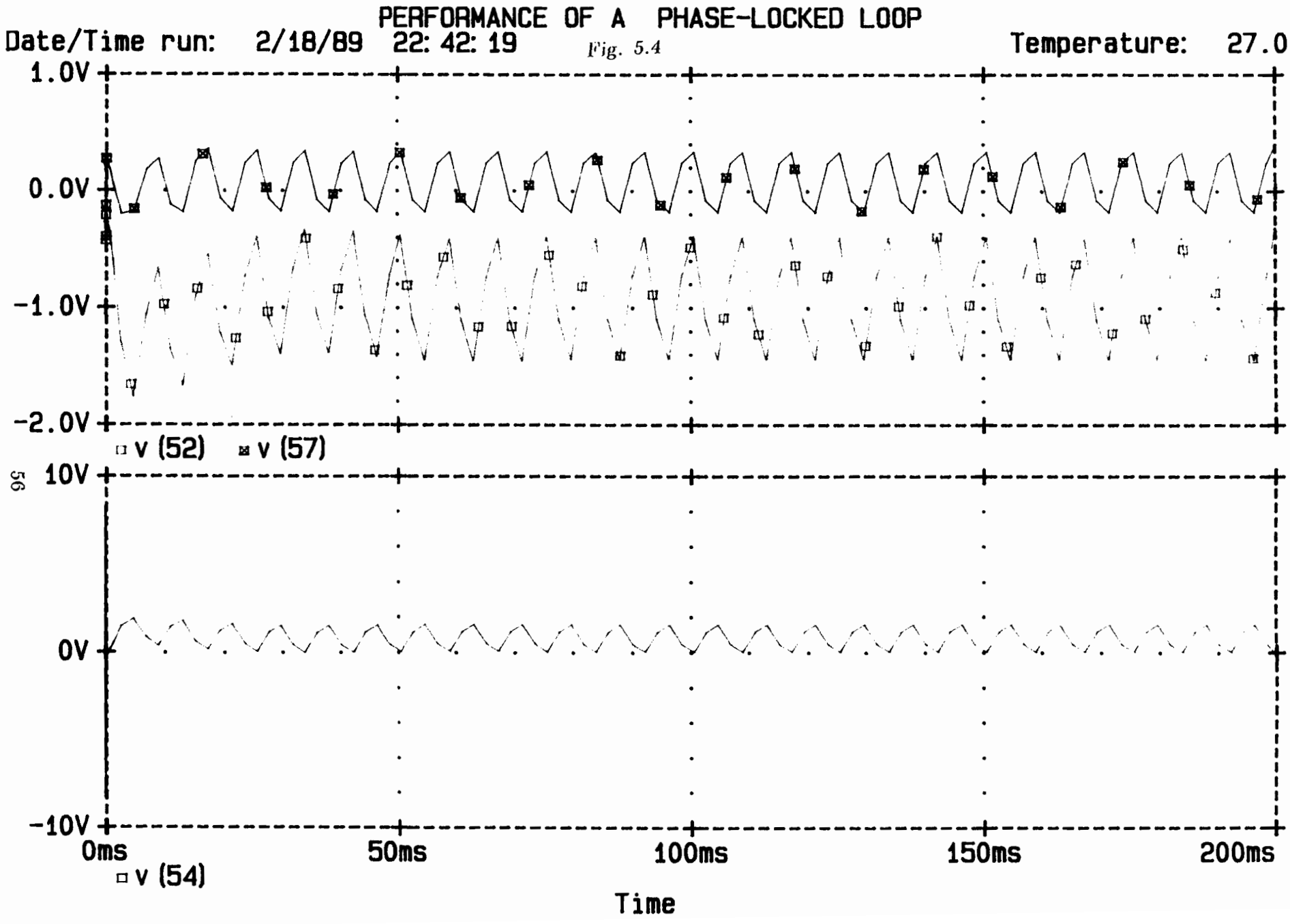

PERFORMANCE OF A PHASE-LOCKED LOOP
Date/Time run: 2/18/89 22:42:19
Temperature: 27.0
1.0V
0.0V
-1.0V
-2.0V
v (52)
v (57)
10V
0V
-10V
0ms
50ms
100ms
150ms
200ms
v (54)
Time

Fig. 5.4

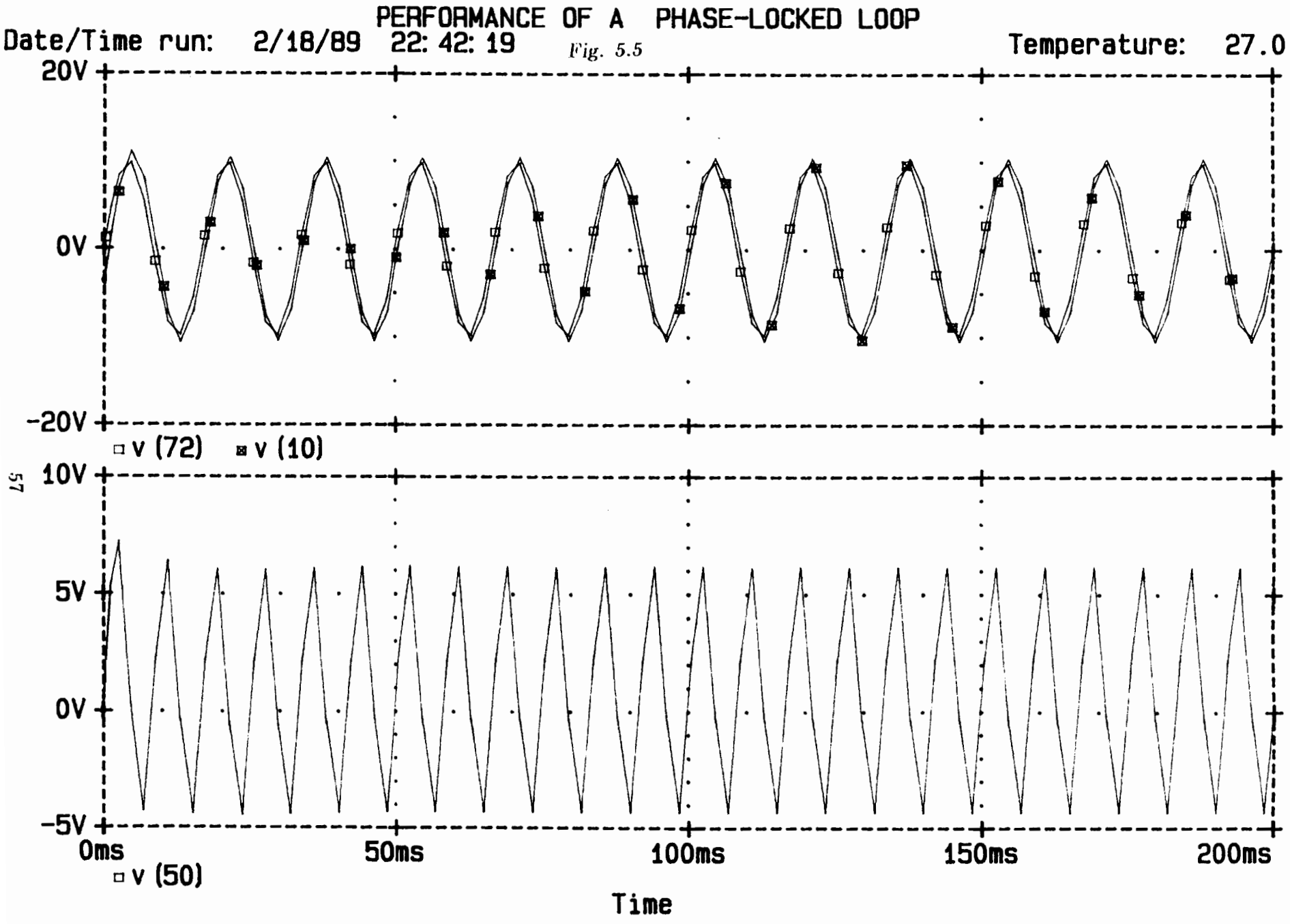

PERFORMANCE OF A PHASE-LOCKED LOOP
Date/Time run: 2/18/89 22:42:19
Temperature: 27.0
20V
0V
-20V
v (72)
v (10)
10V
5V
0V
-5V
0ms
50ms
100ms
150ms
200ms
v (50)
Time

Fig. 5.5

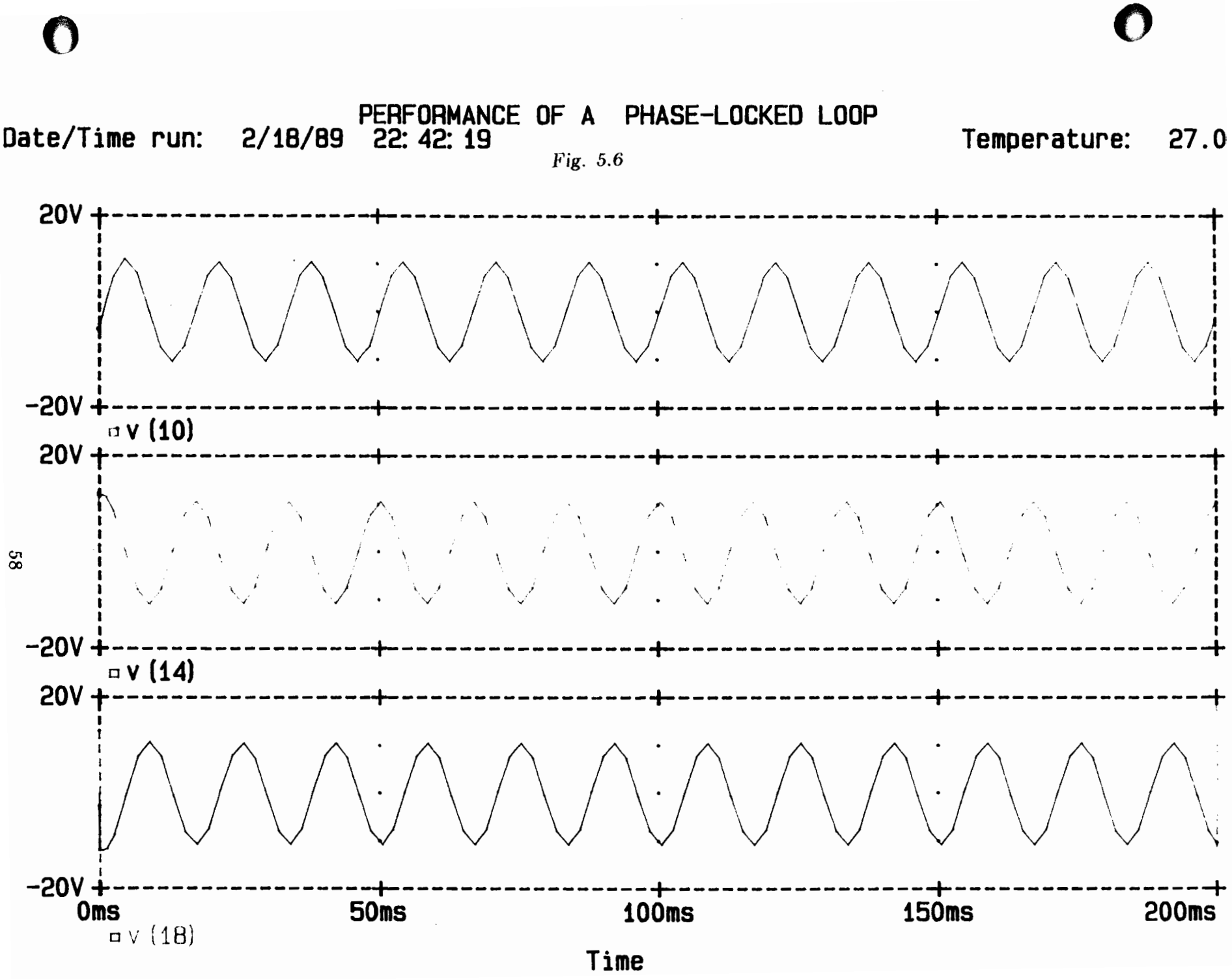

PERFORMANCE OF A PHASE-LOCKED LOOP
Date/Time run: 2/18/89 22: 42: 19
Temperature: 27.0
20V
-20V
V (10)
20V
-20V
V (14)
20V
-20V
0ms
50ms
100ms
150ms
200ms
V (18)
Time

Fig. 5.6

5.4 — Phase Perturbation

In this section we will analize the performance of the PLL under a phase perturbation. A phase perturbation is represented by a step phase in the input voltage, that is,

$$V_i(t) = V \sin(wt + \phi(t)) \tag{5.16}$$

$$\phi(t) = \phi_0(t) + \Delta\phi(t) \tag{5.17}$$

$$\Delta\phi(t) \rightarrow \Delta\phi(s) = \frac{K_\phi}{s} \tag{5.18}$$

where

K_ϕ is the amplitude of the phase-step perturbataion

The perturbation can occur at different instants and the system settling-down time depends on the time it ocurred.

Let us take for example, the following case

$$\Delta\phi = \begin{cases} 0 & \text{at } t < t_p \\ \frac{\pi}{4} & \text{at } t \geq t_p \end{cases} \tag{5.19}$$

Then, multiplying and adding the input signal by the step phase function

$$\sin(\omega t + \phi_o)\cos\Delta\phi + \cos(\omega t + \phi_0)\sin\Delta\phi = v_i(t) \tag{5.20}$$

we get

$$\sin\omega t\cos\Delta\phi + \cos\omega t\sin\Delta\phi = v_i(t) \tag{5.21}$$

Let the perturbation time tp be:

$$tp = \frac{7}{16}T \tag{5.22}$$

For $T = 18ms$, one obtains

$$tp = 7.875ms$$

Plots in Fig. 5.7 shows the phase perturbation, $\Delta\phi(t)$; Fig. 5.8, the terms corresponding $\sin wt \cos\phi$ and $\cos wt \sin wt$, while Fig. 5.9 shows the perturbation

$$v_i(t) = \sin(\omega t + \phi_0 + \Delta\phi(t)) \tag{5.23}$$

where

$$v_i(t) = -V(80) = V(72)$$

and

V(50) is the output of the PLL multiplier

The waveform illustrated in Fig 5.9, shows the case when the voltage jumps from $v(t) = \sin(\omega t)$ to $v(t) = \sin(\omega t + \phi)$.

The simulation of this perturbation is realized using the trigonometric identity

$$\sin(\omega t + \phi) = \sin \omega t \cos \phi + \cos \omega t \sin \phi \tag{5.24}$$

and the circuit which implements this in is shown in Fig. 5.10.

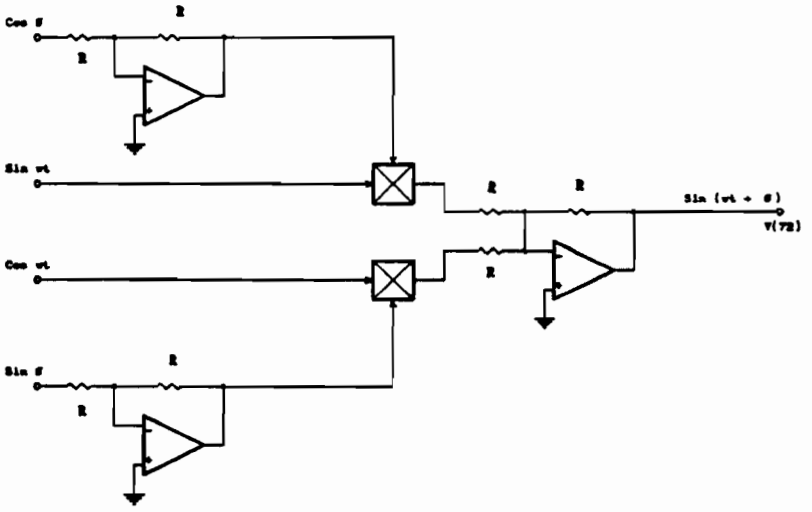


Fig. 5.10 Phase perturbation circuit

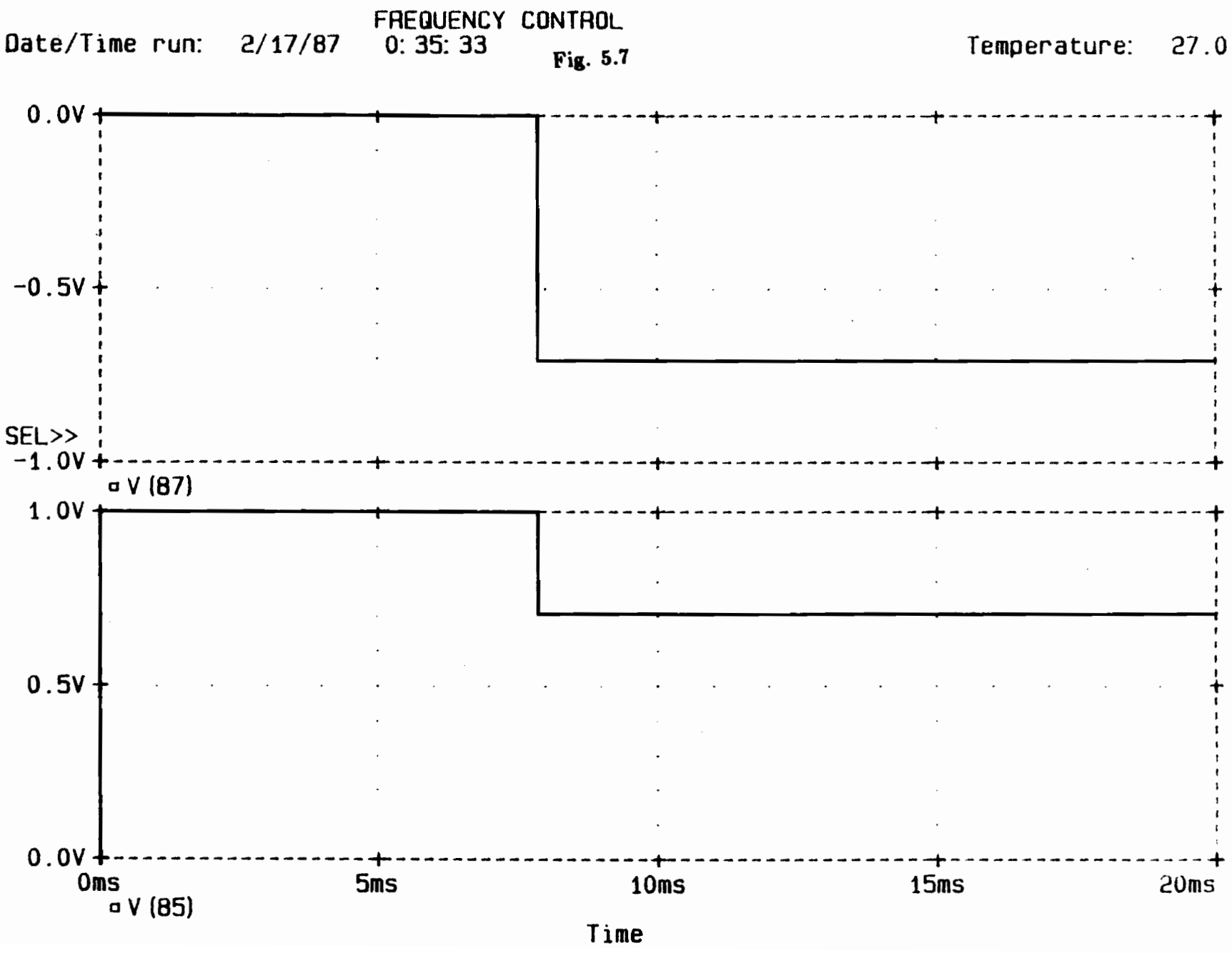

FREQUENCY CONTROL
Date/Time run: 2/17/87 0: 35: 33
Temperature: 27.0
0.0V
-0.5V
SEL>>
-1.0V
V (87)
1.0V
0.5V
0.0V
0ms
5ms
10ms
15ms
20ms
V (85)
Time

Fig. 5.7

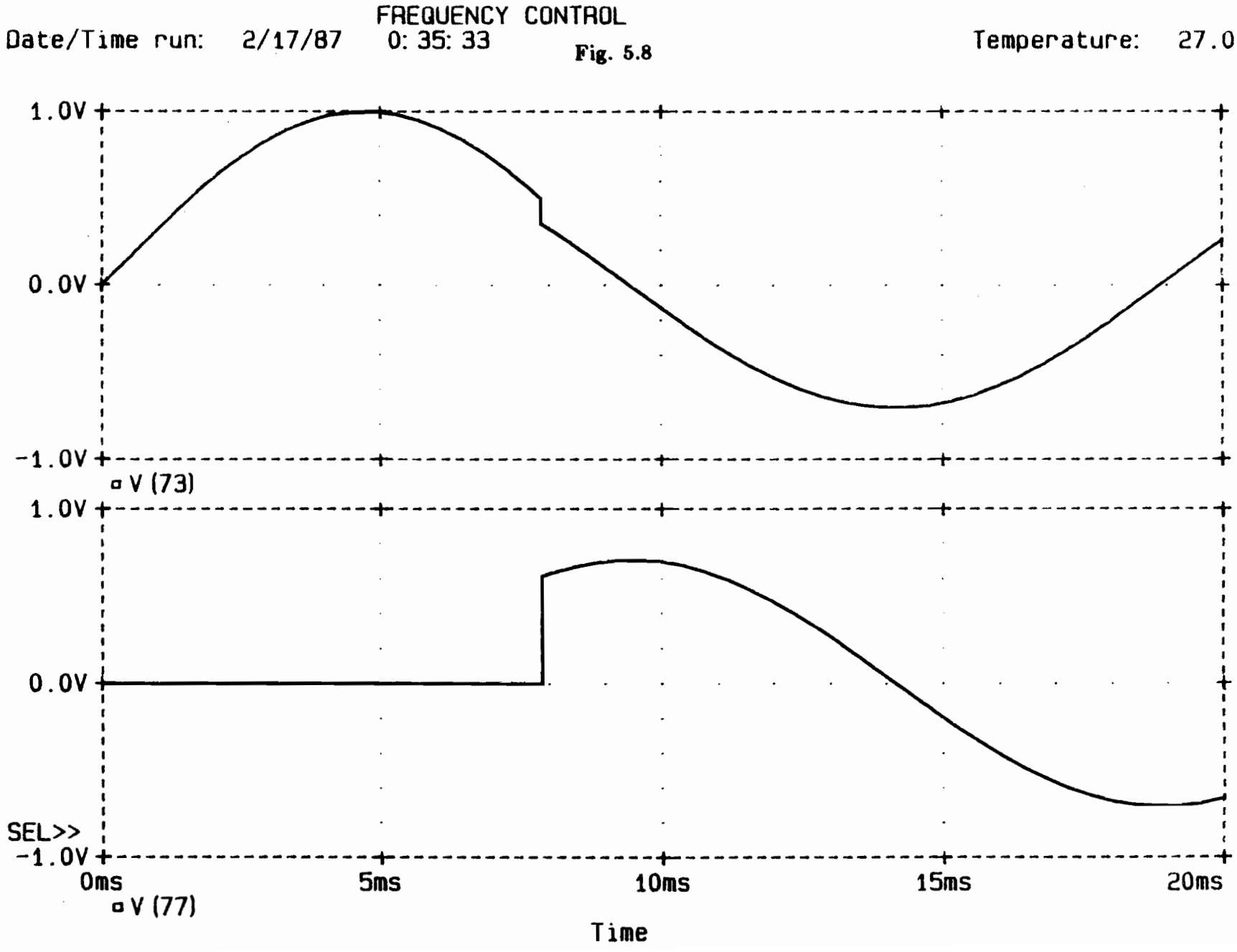

FREQUENCY CONTROL
Date/Time run: 2/17/87 0: 35: 33
Temperature: 27.0
1.0V
0.0V
-1.0V
V (73)
1.0V
0.0V
SEL>>
-1.0V
0ms
5ms
10ms
15ms
20ms
V (77)
Time

Fig. 5.8

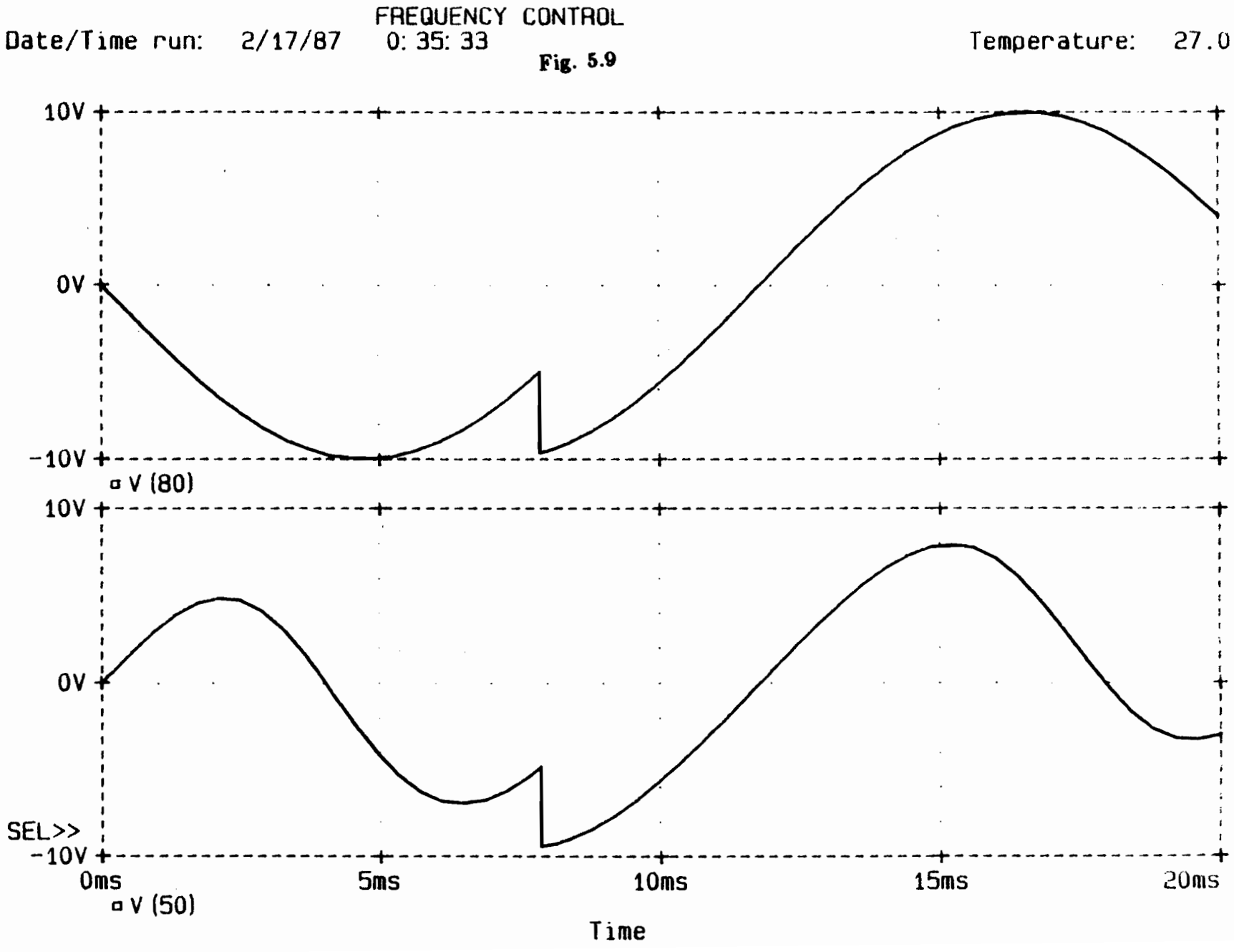

FREQUENCY CONTROL
Date/Time run: 2/17/87 0: 35: 33
Temperature: 27.0
10V
0V
-10V
V (80)
10V
0V
SEL>>
-10V
0ms
5ms
10ms
15ms
20ms
V (50)
Time

Fig. 5.9

5.5 — Phase Perturbation applied to PLL with Analog Filter

The first test, under a phase perturbation was carried out for a PLL with analog filter and an integrator in parallel in order to eliminate the steady-state error (Fig. 5.1). Fig. 5.13 shows the waveforms corresponding to the circuit given in Fig. 5.11. We can observe that the control voltage V(54) settles down in about 4 1/2 cycles while the signal V(10) is getting synchronized to the incoming signal V(72) from the network.

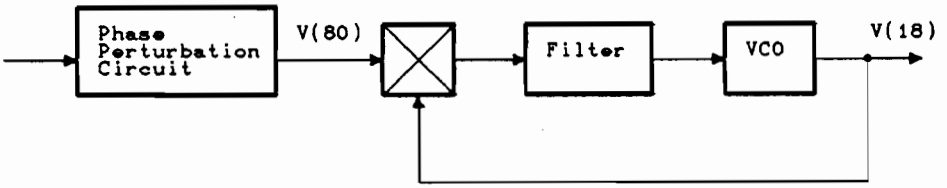
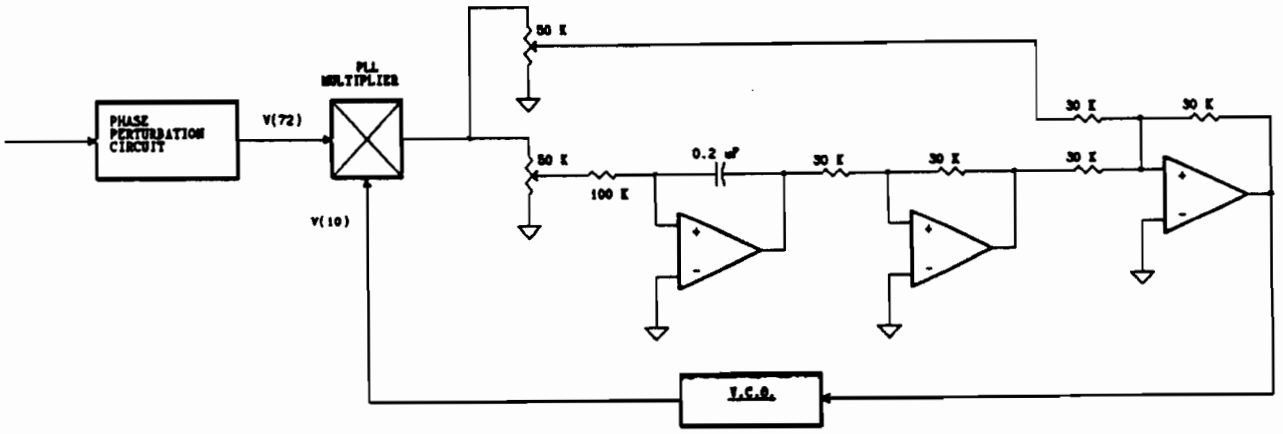


Fig. 5.11 PLL with analog filter

5.6 — Phase Perturbation applied to PLL without Filter



Using this configuration we have verified that the synchronism takes place, about a cycle later than the PLL with analog filter. The waveforms corresponding to this test are shown in Figs. 5.14.

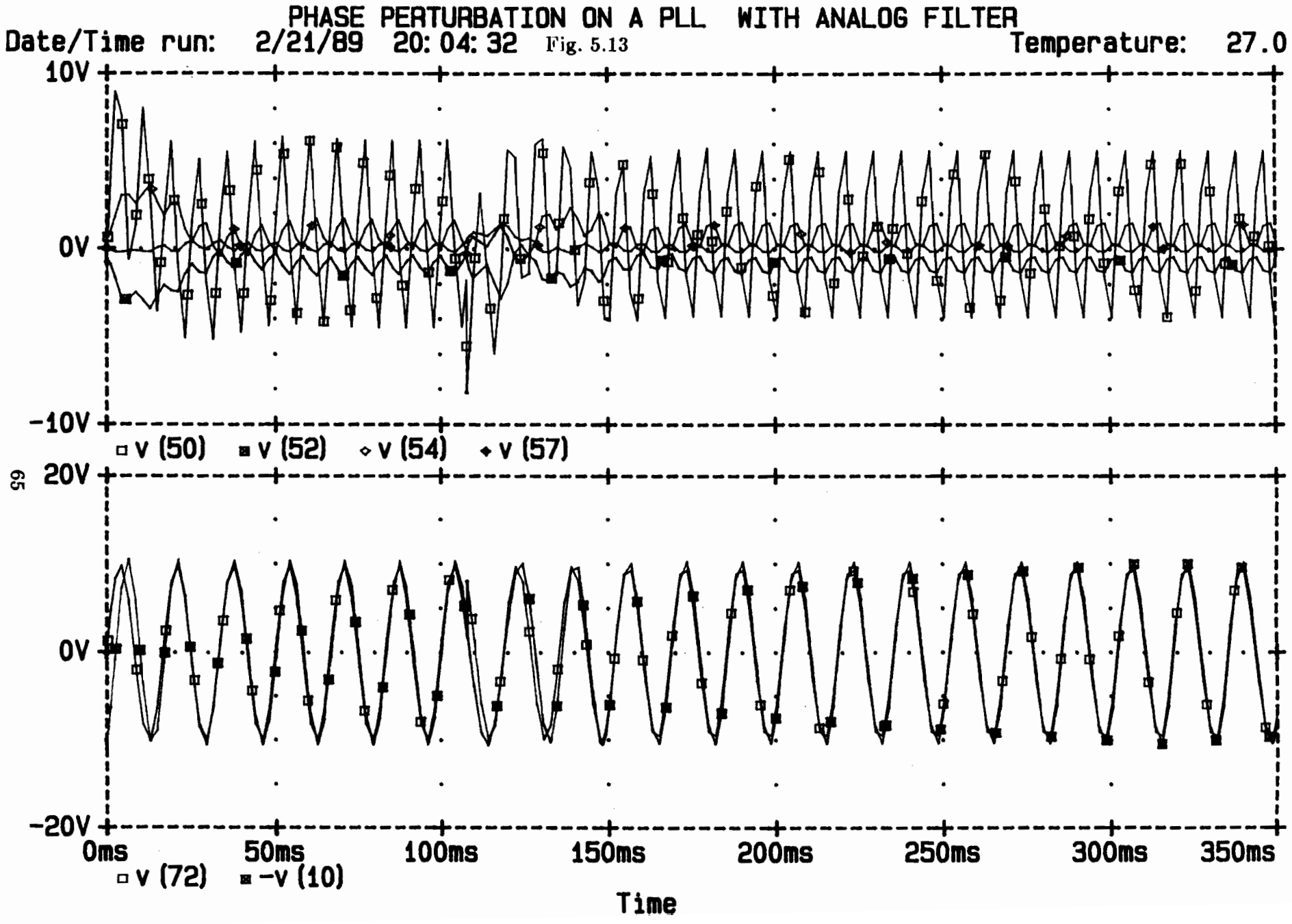

PHASE PERTURBATION ON A PLL WITH ANALOG FILTER
Date/Time run: 2/21/89 20:04:32
Temperature: 27.0
10V
0V
-10V
v (50)
v (52)
v (54)
v (57)
20V
0V
-20V
0ms
50ms
100ms
150ms
200ms
250ms
300ms
350ms
v (72)
-v (10)
Time

Fig. 5.13

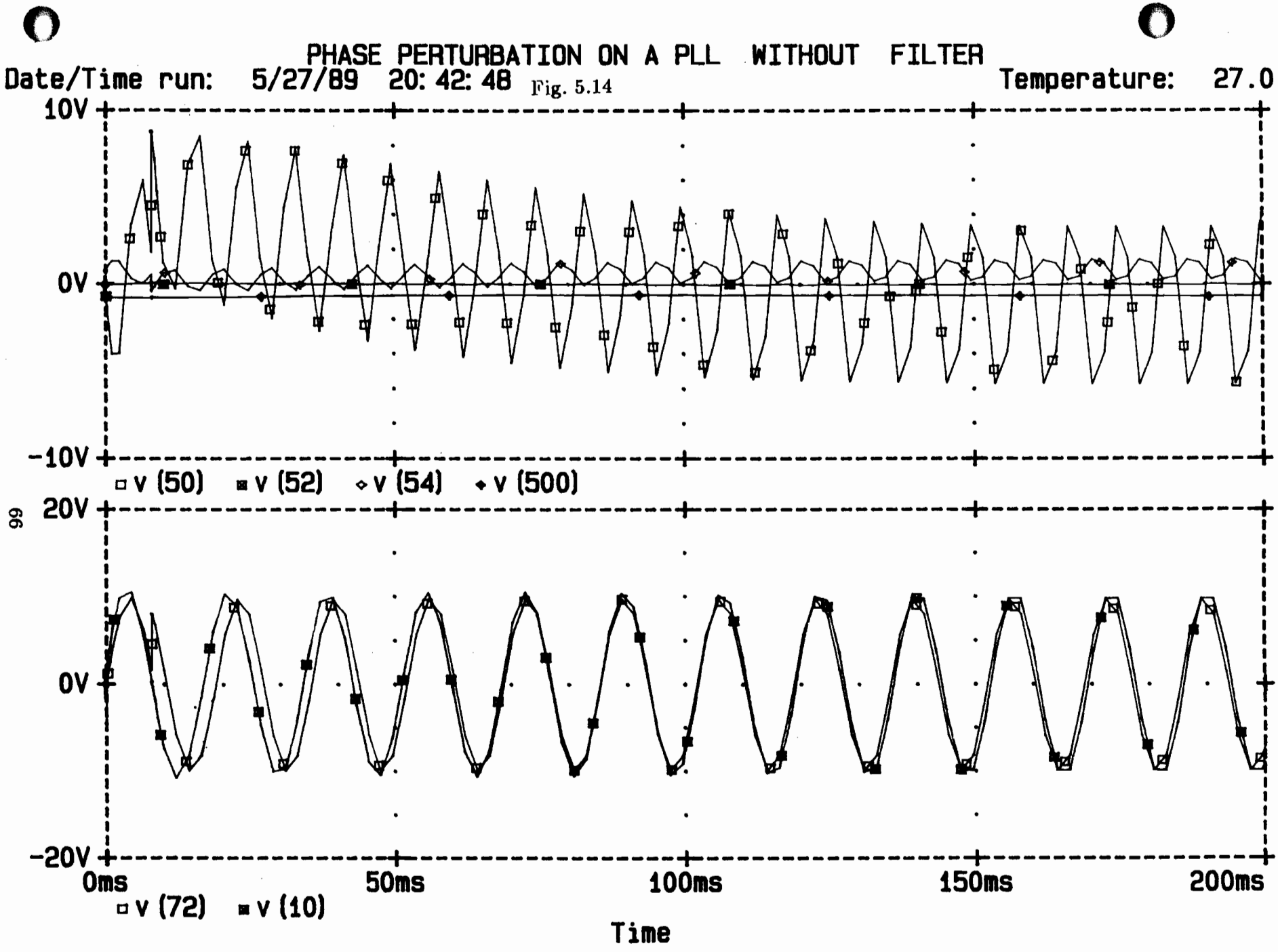

PHASE PERTURBATION ON A PLL WITHOUT FILTER
Date/Time run: 5/27/89 20: 42: 48
Temperature: 27.0
10V
0V
-10V
v (50)
v (52)
v (54)
v (500)
20V
0V
-20V
0ms
50ms
100ms
150ms
200ms
v (72)
v (10)
Time

Fig. 5.14

5.7 — PLL with Synchronous Filter

Simulation results presented in this section correspond to PLL with synchonous filter (described in the previous chapter). The block diagram for this PLL circuit is shown in Fig. 5.15.

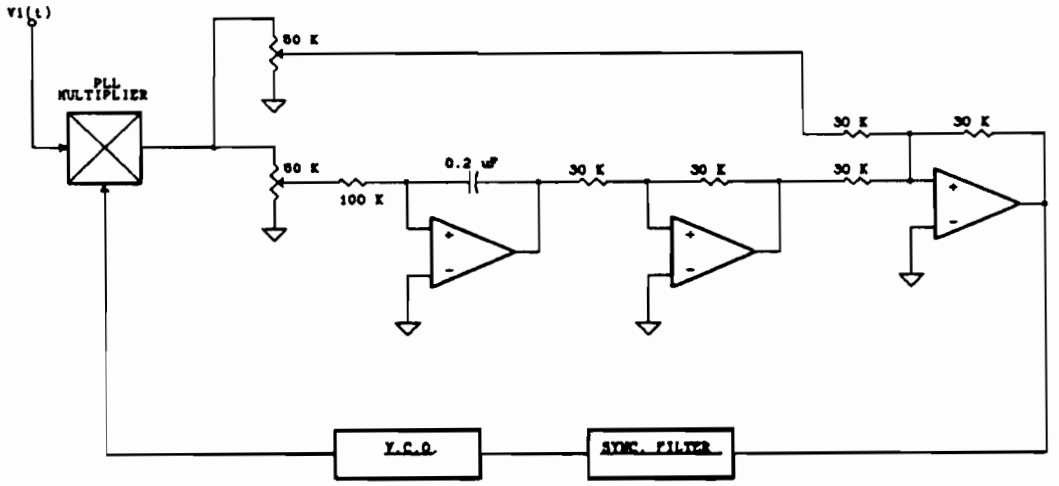


Fig. 5.15 Block diagram of PLL with synchronous filter

The output voltage of the PI controller V(54), shown in Fig. 5.16, is filtered out with a synchronous filter before it is applied to control the frequency of the voltage controlled oscillator. The waveform of the control voltage V(10) is illustrated in Fig. 5.17. The upper side of the figure shows us the output of the isolator amplifier connected between V(54) and the input of the filter. In this case, V(54) settles down quite later than in the case when an analog filter is applied. This is caused by the time delay of the synchronous filter.

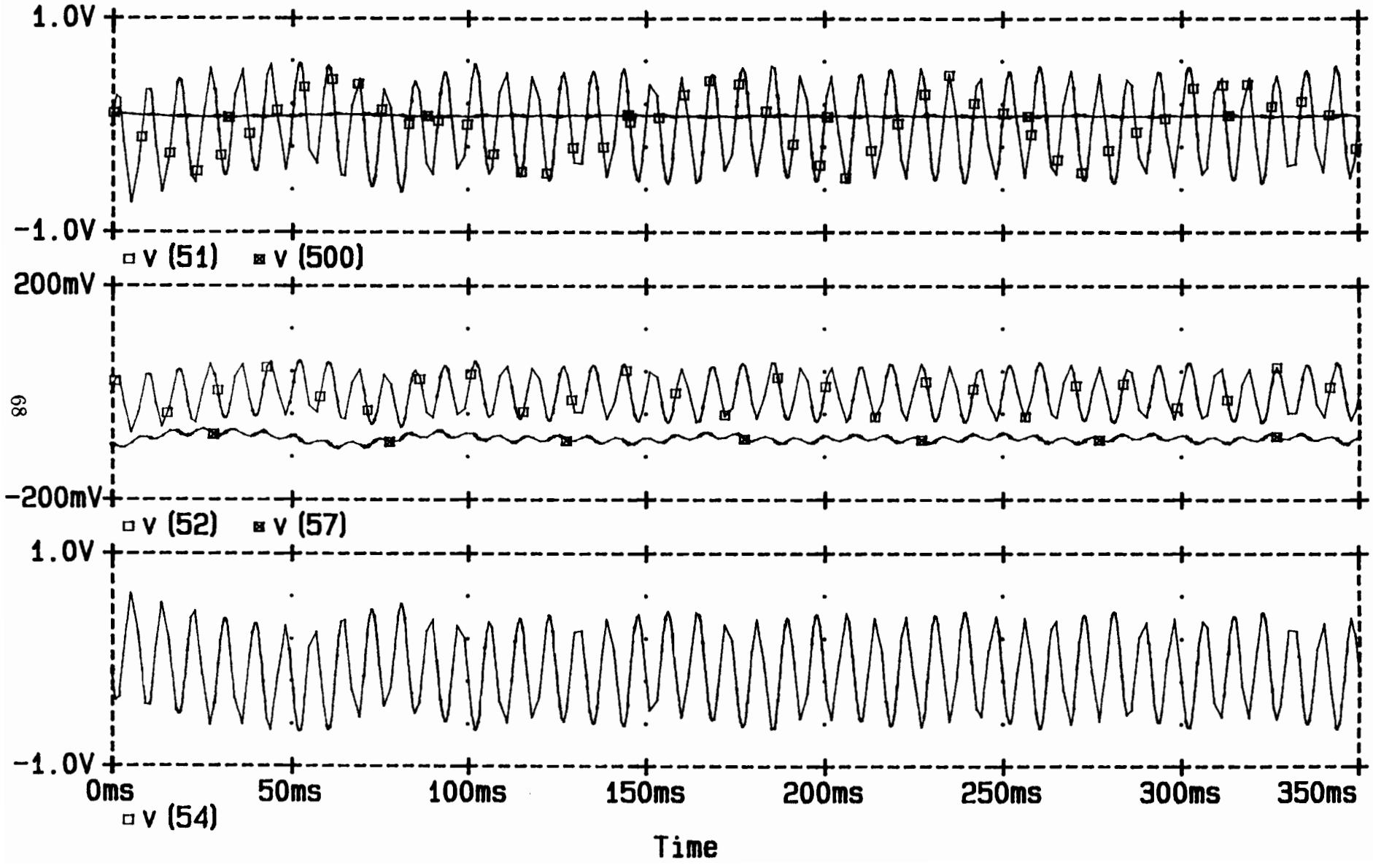
In order to see the time required to get the two signals in synchronism more clearly, a plot was made of V(72) and V(10). In this plot, given in Fig. 5.18, we see that these signals lock-in aproximately in 10 cycles. Later on we will analize the behaviour of this circuit under phase perturbation.

In the upper part of this figure is shown that voltages V(14) and V(10) are phase-shifted 180° before and after synchronism.

PHASE-LOCKED LOOP WITH SYNCHR. FILTER & PI CONTROLLER

Date/Time run: 2/19/89 8: 49: 56 Temperature: 27.0

Fig. 5.16



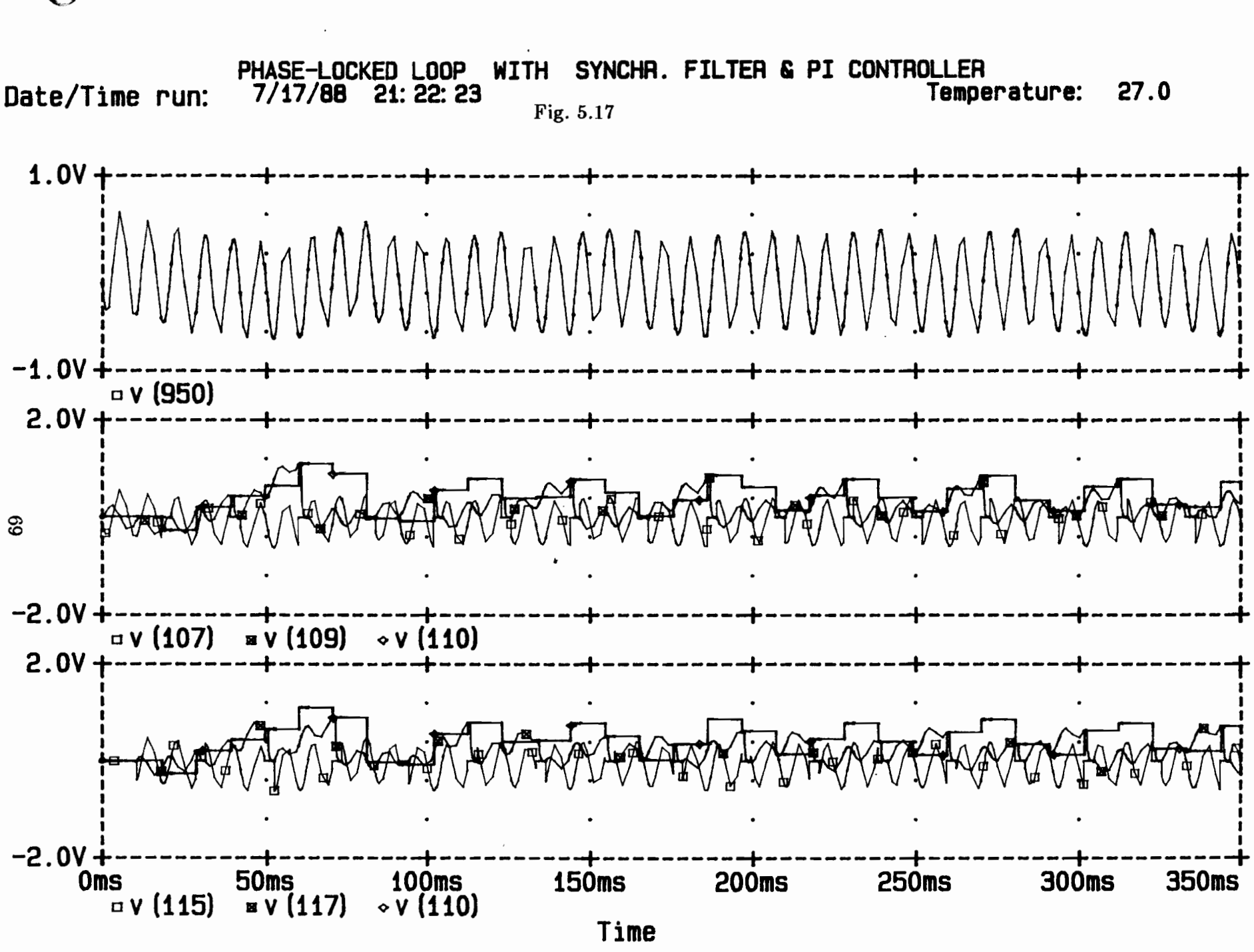

PHASE-LOCKED LOOP WITH SYNCHR. FILTER & PI CONTROLLER
Date/Time run: 7/17/88 21:22:23
Temperature: 27.0
1.0V
-1.0V
v (950)
2.0V
-2.0V
v (107) v (109) v (110)
2.0V
-2.0V
0ms
50ms
100ms
150ms
200ms
250ms
300ms
350ms
v (115) v (117) v (110)
Time

Fig. 5.17

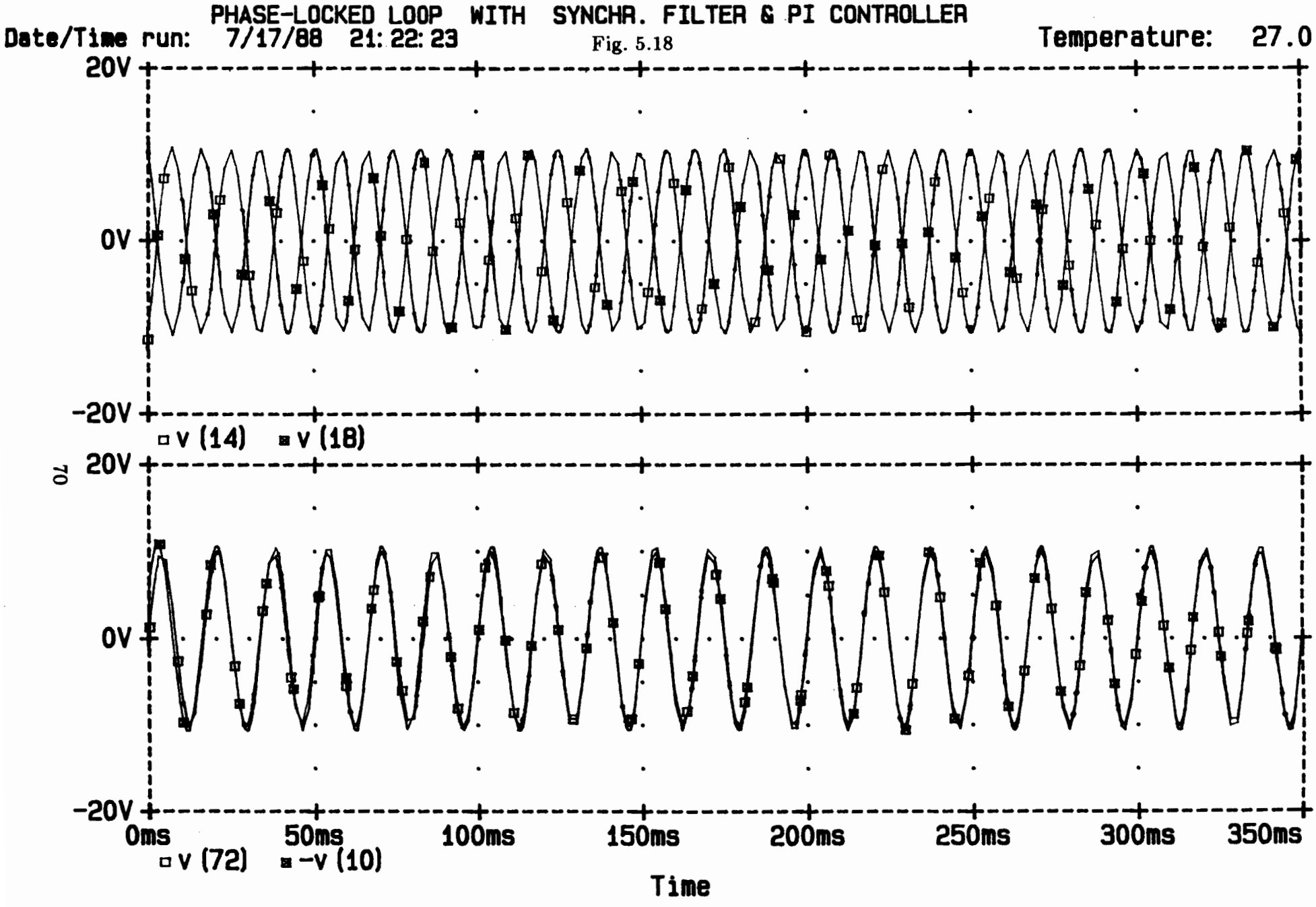

PHASE-LOCKED LOOP WITH SYNCHR. FILTER & PI CONTROLLER
Date/Time run: 7/17/88 21:22:23
Temperature: 27.0
20V
0V
-20V
v (14)
v (18)
20V
0V
-20V
0ms
50ms
100ms
150ms
200ms
250ms
300ms
350ms
v (72)
-v (10)
Time

Fig. 5.18

5.7.1 — PLL with Synchronous Filter exposed to Phase Perturbation

In order to explain the performance of the PLL in this particular case, we will refer to Fig. 5.19. In this case the step-wise perturbation in the phase of the voltage is applied. In this case the phase of the relevant voltage settles down after about 10 cycles (plots at the botton).

The waveform of the control voltage V(110) of the VCO is also shown in this figure. It could be seen this voltage leads V(10) to get in phase with the input voltage V(72). In the upper traces, voltages V(65) and V(72) are plotted. Both are the network signals, the first one is being the signal with no perturbation. In the middle, the controller output voltage V(950), with its second harmonic signal is shown.

5.8 — Effect of the Second Harmonic on the PLL Operation

Second harmonic is often present in the power network due to transformer inrush currents, static converters,static compensators, etc.

The PLL must responds very quickly to every change of the system voltage phase in order to provide an appropiate valve firing to an AC-DC converter or a SVC system.

5.8.1 — PLL with an Analog Filter: Phase Perturbation and Second Harmonic

The circuit diagram illustrated in Fig. 5.20 is applied in order to produce the specified perturbations. V(65) is passed through the amplifier A1 (with the gain Ka = 0.25) to give the signal V(67). After squaring this signal transforms into V(69). After filtering its dc component the second harmonic is obtained with an attenuation of 0.4 p.u.

Fig. 5.21 shows a combined perturbation which consists of a step-wise perturbation of the system voltage phase and the second harmonic . The plot at the bottom illustrates the incoming signal to the PLL.

The upper trace , shows the controller signals V(52), V(57), V(54) and V(50) and the VCO signal V(10). By inspection, we see that the signals V(10) and V(72) settle in about five cycles. The effect of the 2nd harmonic can be observed in Fig. 5.24. The upper traces show V(10) as compared to V(65) (a non-perturbated signal). The signals V(14) and V(18), are shown at the bottom traces performing as expected.

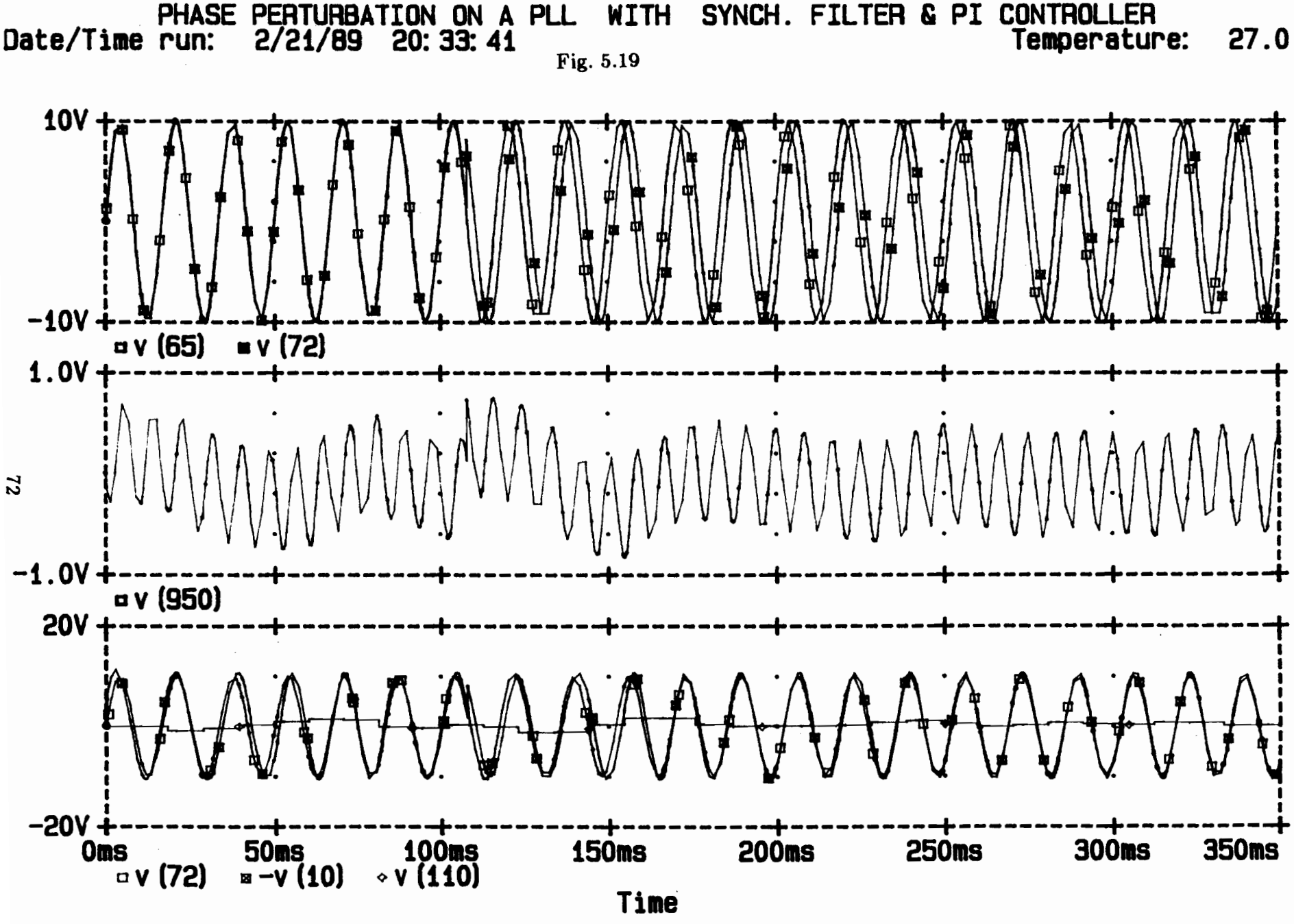

PHASE PERTURBATION ON A PLL WITH SYNCH. FILTER & PI CONTROLLER
Date/Time run: 2/21/89 20:33:41
Temperature: 27.0
10V
-10V
v (65)
v (72)
1.0V
-1.0V
v (950)
20V
-20V
0ms
50ms
100ms
150ms
200ms
250ms
300ms
350ms
v (72)
-v (10)
v (110)
Time

Fig. 5.19

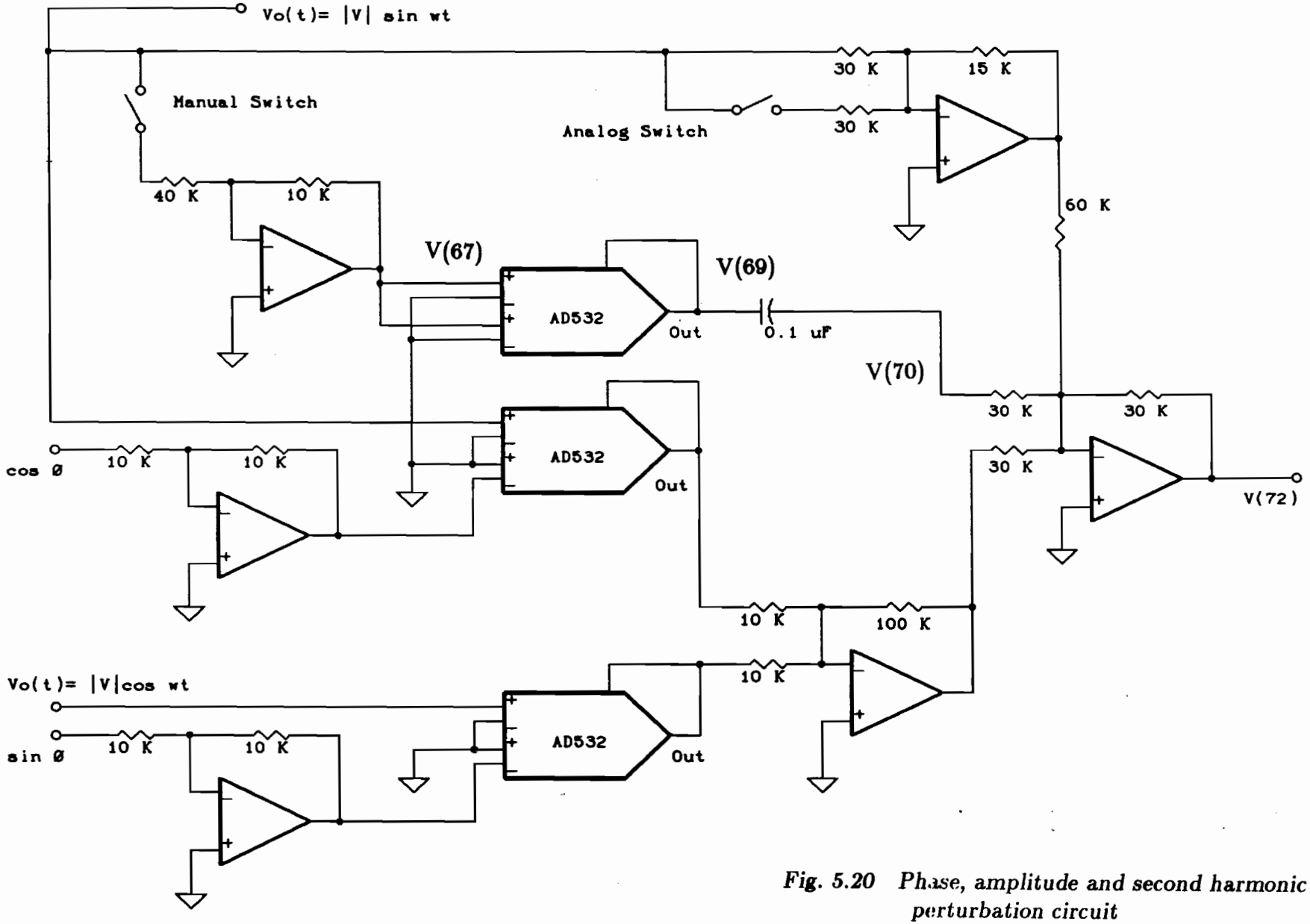


Fig. 5.20 Phase, amplitude and second harmonic perturbation circuit

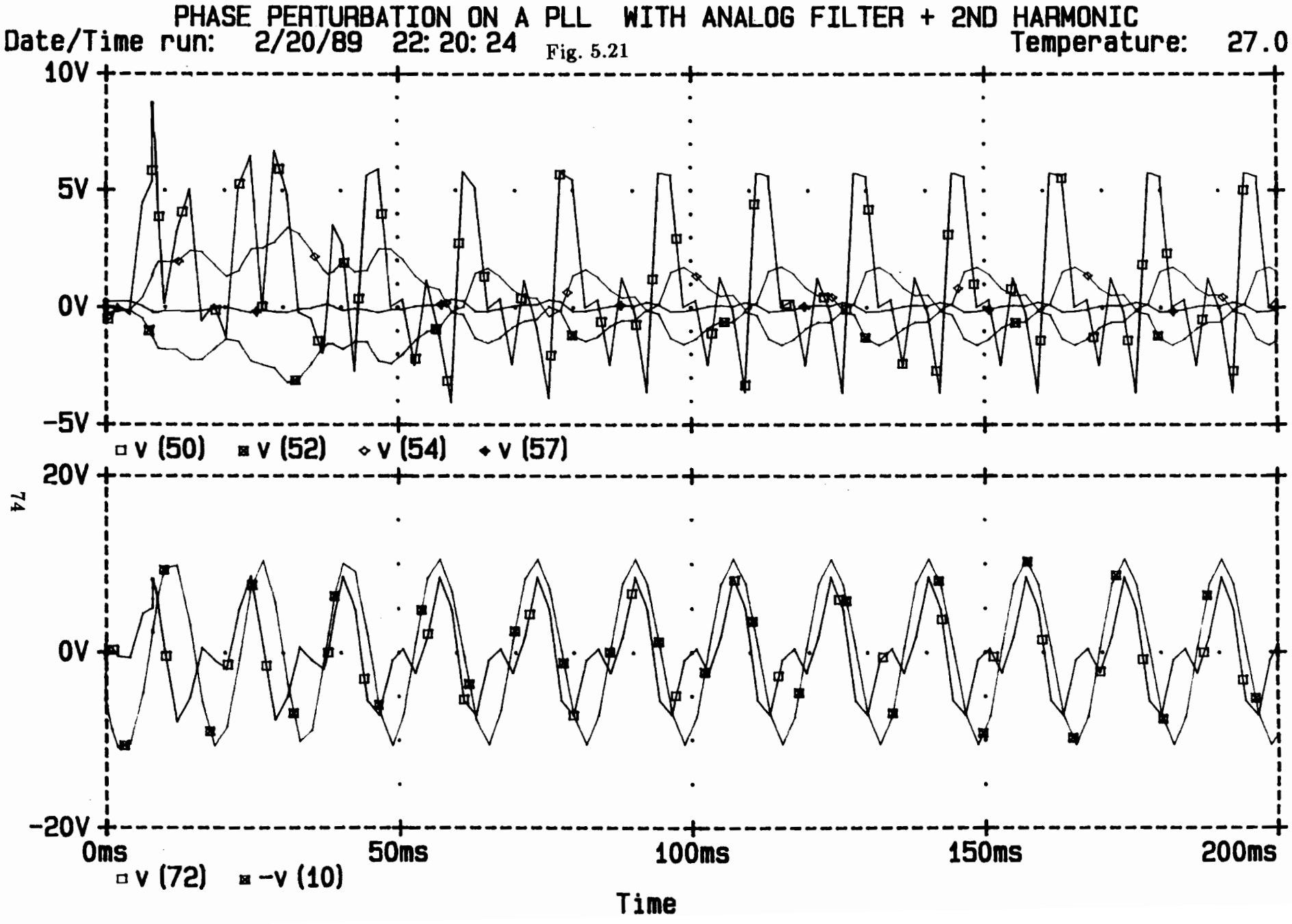

PHASE PERTURBATION ON A PLL WITH ANALOG FILTER + 2ND HARMONIC
Date/Time run: 2/20/89 22:20:24
Temperature: 27.0
10V
5V
0V
-5V
v (50)
v (52)
v (54)
v (57)
20V
0V
-20V
0ms
50ms
100ms
150ms
200ms
v (72)
-v (10)
Time

Fig. 5.21

5.9 — PLL with a Synchronous Filter: Phase Perturbation and Second Harmonic

The probe is placed at the point V(500) to observe the steady-state error and its shapewave. The upper side of Fig. 5.22 shows the output of the PI controller. The error is reaches its steady-state value after 12 cycles.

Evidently, there is a trade-off between the response time and the gain of the PI controller, since greater the controller gain is, longer is the system settling time. In order to control the overshoot the PI parameters can not be less than 0.1 and 1.0 for Kp and Ki, respectively, if we want to get the two main signals in synchronism, V(10) and V(72), in the shortest run. The effect is shown at the bottom of the Fig. 5.23.

In terms of the frequency domain, we also have to consider, the compromise between the overshoot and the phase-margin. In other words, as long as we decrease the overshoot, we approach to instability. Therefore, a carefully design approach has to be taken in order to meet these stability criterion.

5.10 — PLL with Synchronous Filter and Second Harmonic

Two points seem important to emphazise: firstly, the performance of the synchronous filter is tied-up to the presence of the harmonic. It is highly probably that the magnitude of this component will also have an incidence on the performance, which means, the larger the amplitude, the smaller the amplitude of the filter, V(110). In fact, this can be verified comparing PLL with synchronous filter to PLL with synchronous filter and second harmonic. Secondly, as a consequence of the filter response we will have a 1 cycle delay in getting the signal in synchronism as it can be seen in Fig. 5.24 at the bottom. In this case the lock-in is reached at about 7 cycles.

5.11 — Voltage Amplitude Perturbation with/without Second Harmonic

In weak power systems with a low short-circuit MVA level involving with long transmission lines, the voltage is significantly affected by load variations as well as by switching of system components such as transmission lines, reactors, capacitors and transformers. If there is a deficiency of reactive power suport the voltage at that point falls.

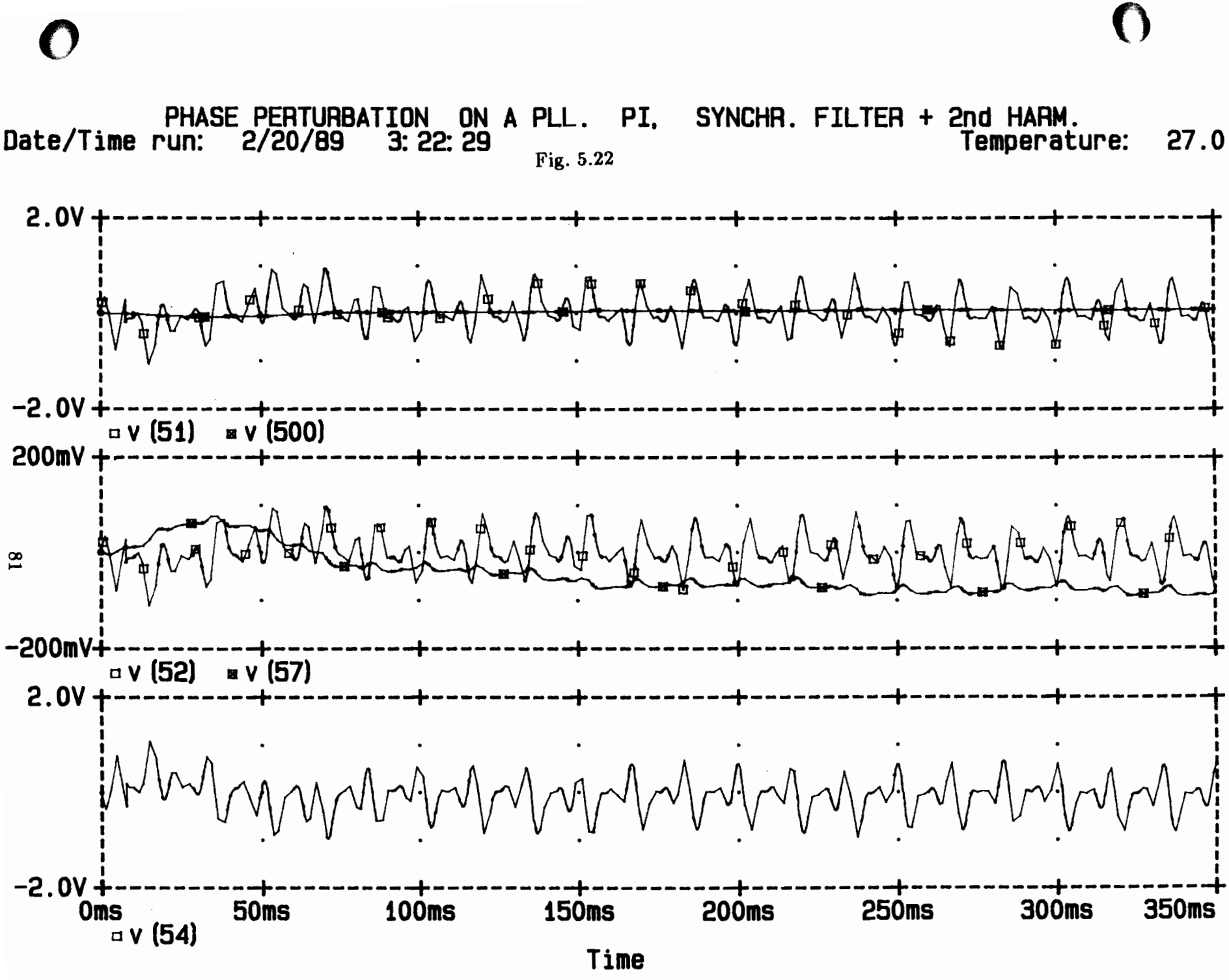
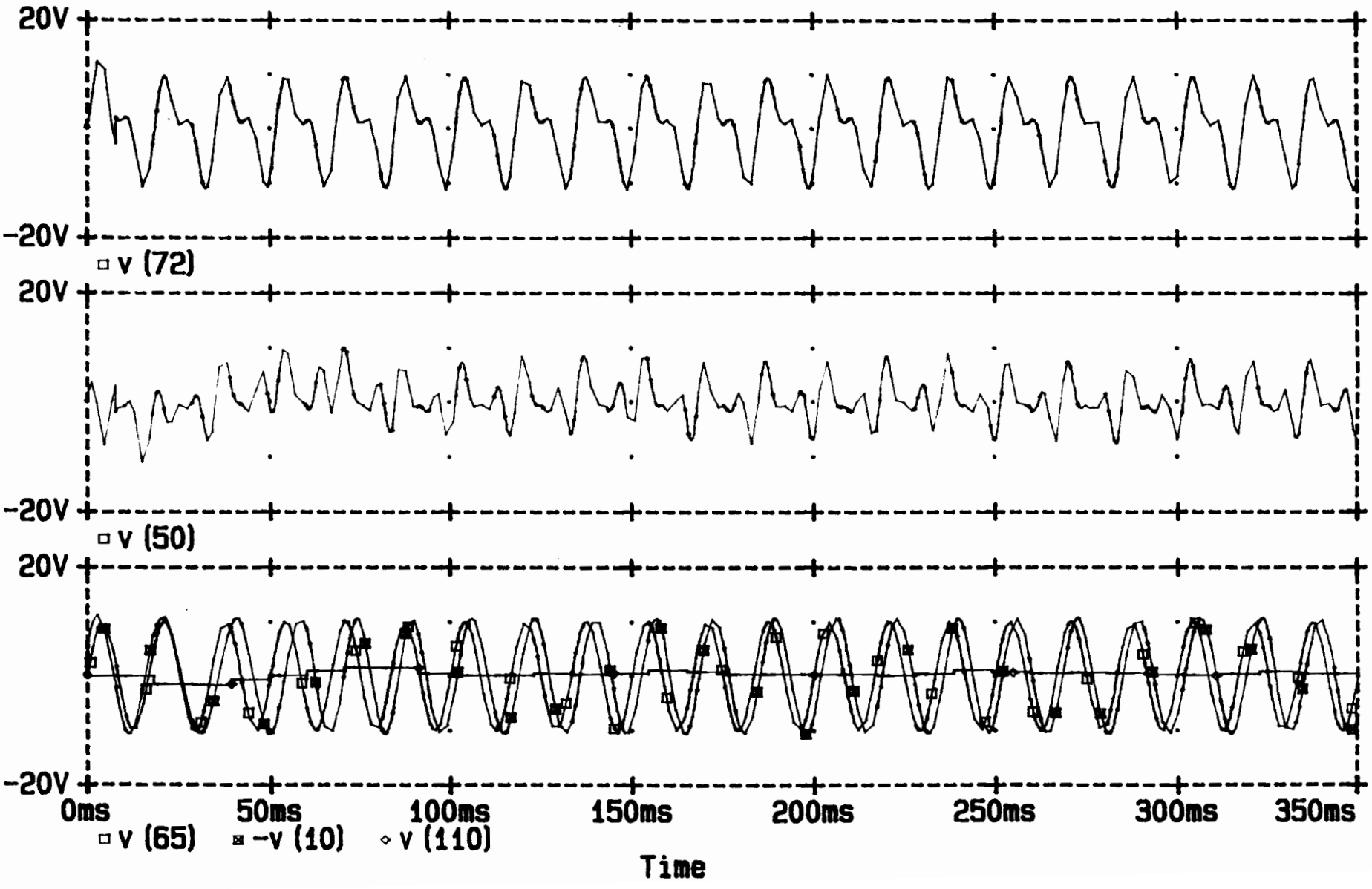

PHASE PERTURBATION ON A PLL. PI, SYNCHR. FILTER + 2nd HARM.
Date/Time run: 2/20/89 3:22:29
Temperature: 27.0
2.0V
-2.0V
v (51)
v (500)
200mV
-200mV
v (52)
v (57)
2.0V
-2.0V
0ms
50ms
100ms
150ms
200ms
250ms
300ms
350ms
v (54)
Time

Fig. 5.22

PHASE PERTURBATION ON A PLL. PI, SYNCHR. FILTER + 2nd HARM.

Date/Time run: 2/20/89 3:22:29 Temperature: 27.0

Fig. 5.23



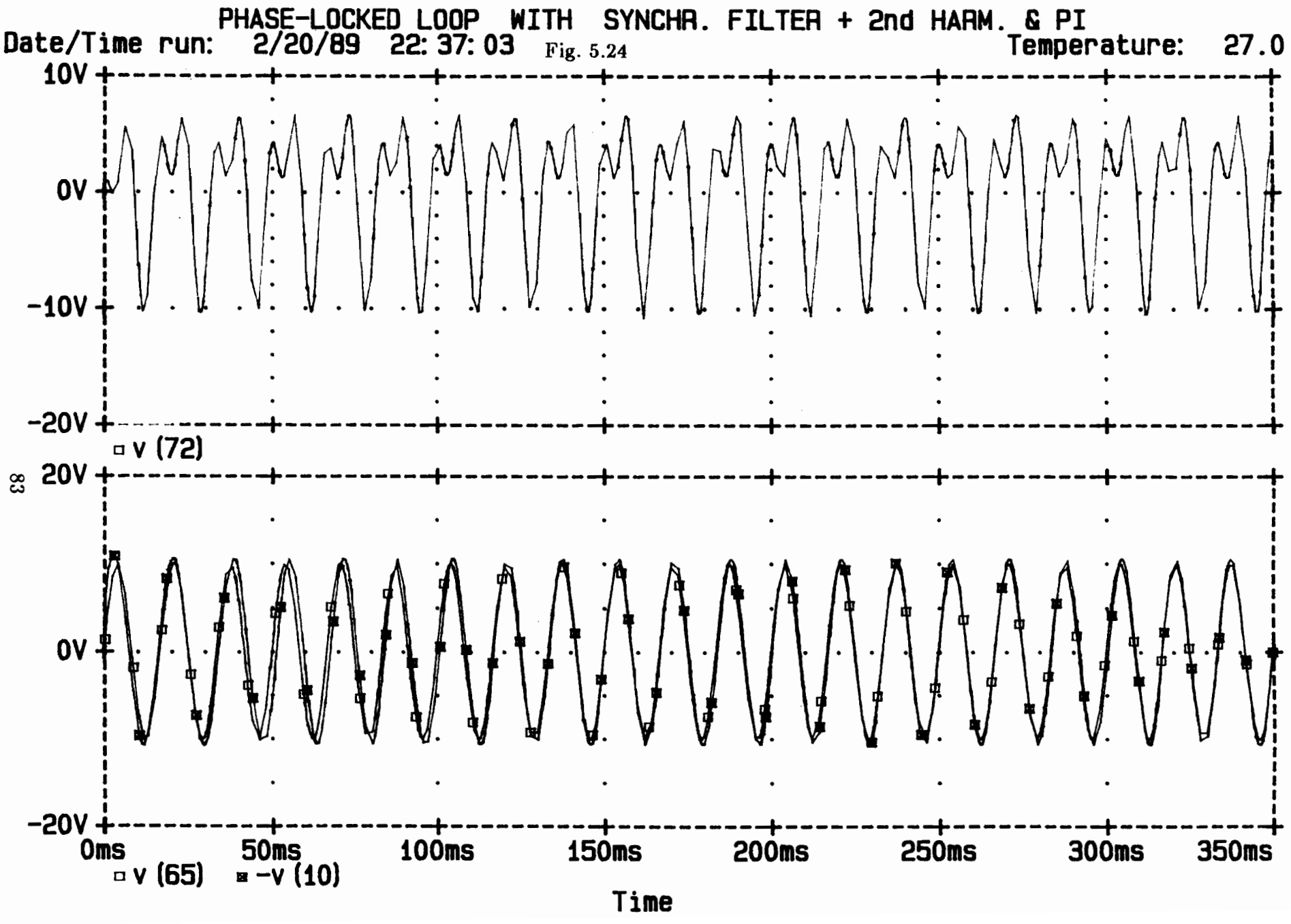

PHASE-LOCKED LOOP WITH SYNCHR. FILTER + 2nd HARM. & PI
Date/Time run: 2/20/89 22:37:03
Temperature: 27.0
10V
0V
-10V
-20V
v (72)
20V
0V
-20V
0ms
50ms
100ms
150ms
200ms
250ms
300ms
350ms
v (65)
-v (10)
Time

Fig. 5.24

The PLL unit has to be able to respond quickly (for control purposes) regardless of the network voltage variations.

5.11.1 — Voltage Amplitude Perturbation: PLL with Analog Filter

The perturbation circuit configuration is shown in Fig. 5.20 where the second harmonic perturbation is also included.

The perturbation is applied at tp = 10 ms, arbitrarily chosen, time at which the magnitude jumps from 5 V to 10 V and stays at that value. The control pulse of the switch and the input voltage to the PLL multiplier is illustrated in Fig. 5.25 where the transient is clearly shown. In the next figure, we can see the switch voltage V(115) which is added the network signal. V(72) and V(50) are the input and output signal of the PLL multiplier respectively. The second harmonic phase with respect to the network voltage phase is as given in the figure.

V(72) and V(10) settle in about 3 cycles after perturbation as shown in Fig. 5.25. It is easy to see from the figure that V(54) settles at about 50 ms.

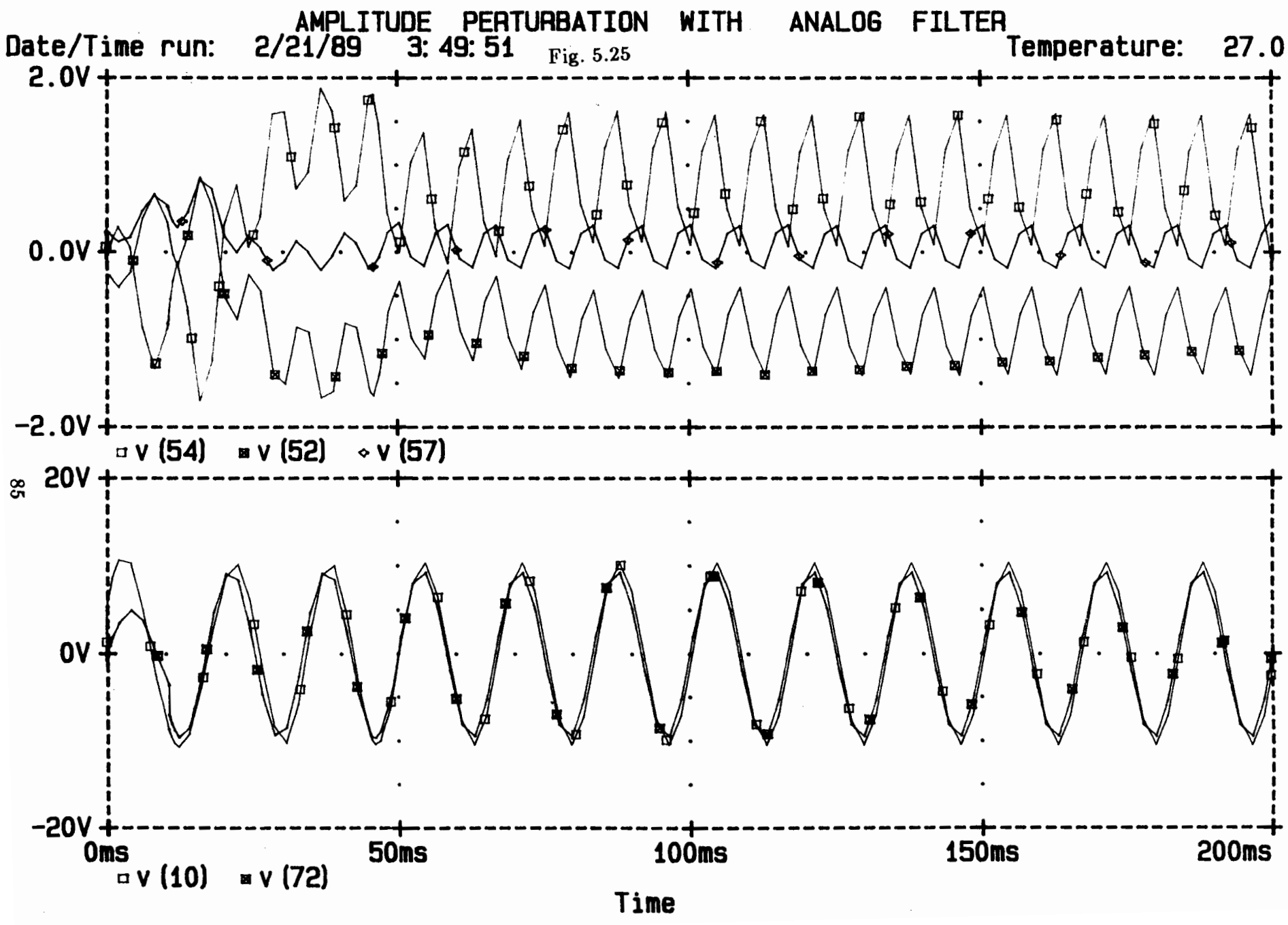

AMPLITUDE PERTURBATION WITH ANALOG FILTER
Date/Time run: 2/21/89 3:49:51
Temperature: 27.0
2.0V
0.0V
-2.0V
v (54)
v (52)
v (57)
20V
0V
-20V
0ms
50ms
100ms
150ms
200ms
v (10)
v (72)
Time

Fig. 5.25

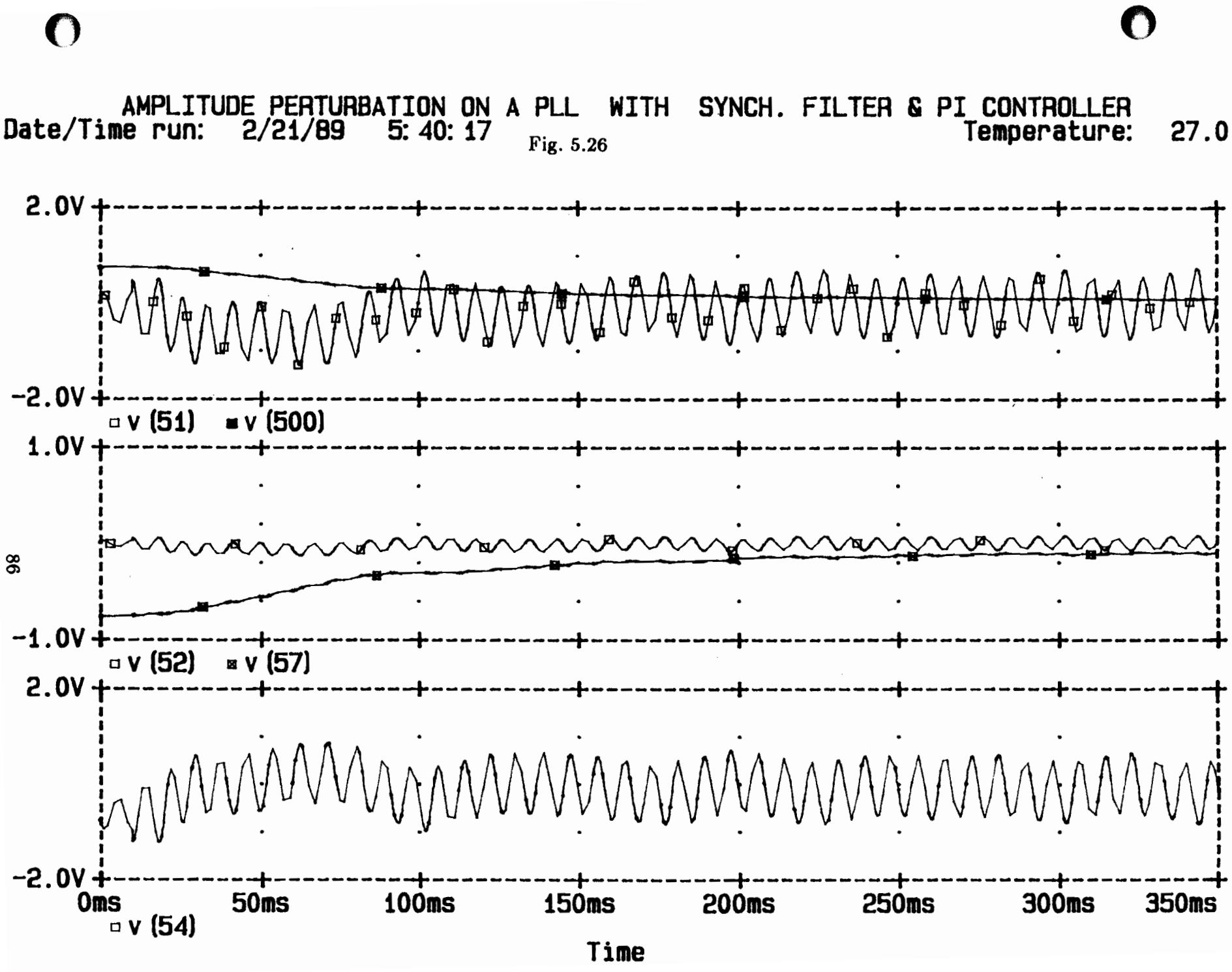

AMPLITUDE PERTURBATION ON A PLL WITH SYNCH. FILTER & PI CONTROLLER
Date/Time run: 2/21/89 5: 40: 17
Temperature: 27.0
2.0V
-2.0V
v (51)
v (500)
1.0V
-1.0V
v (52)
v (57)
2.0V
-2.0V
0ms
50ms
100ms
150ms
200ms
250ms
300ms
350ms
v (54)
Time

Fig. 5.26

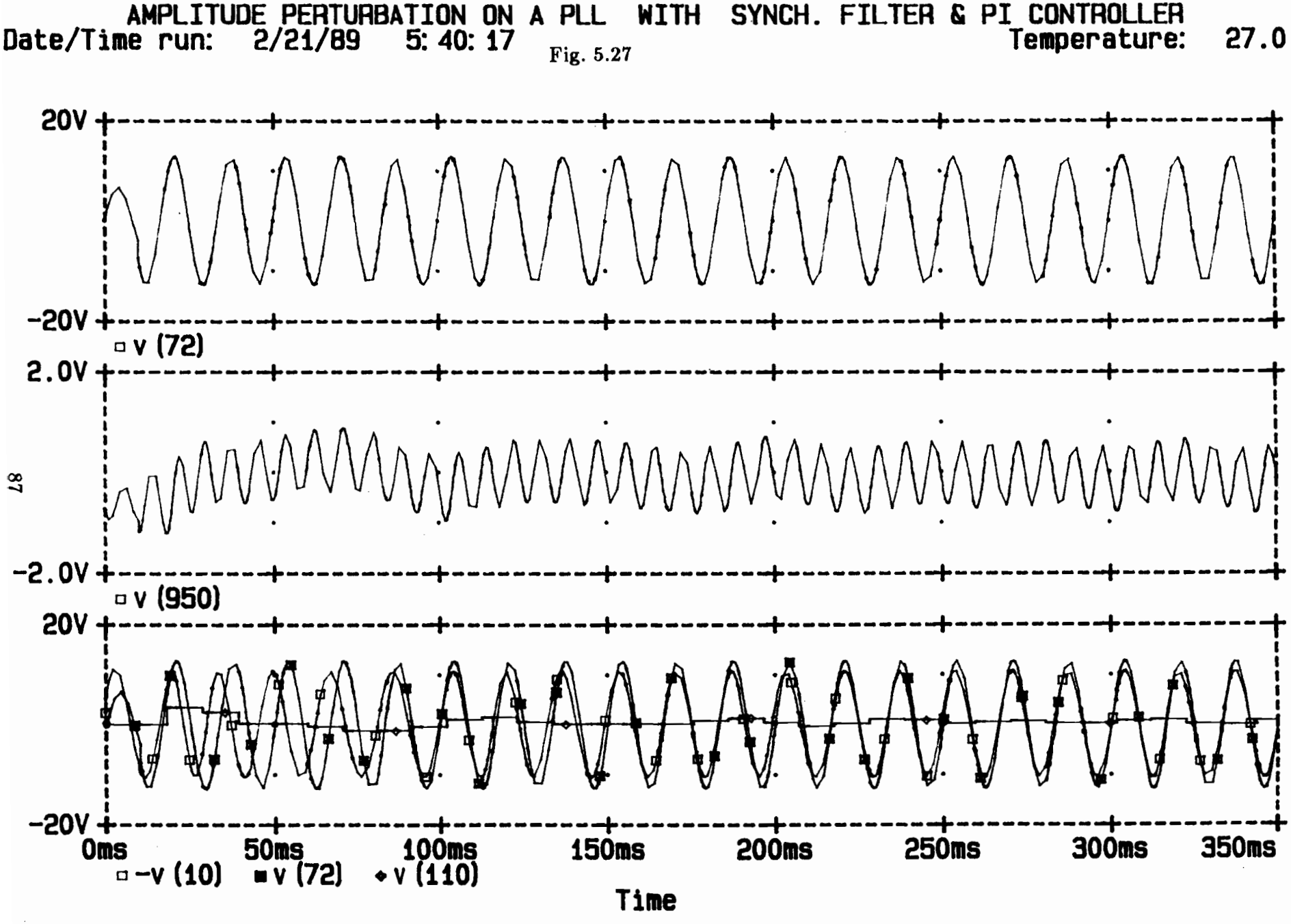

AMPLITUDE PERTURBATION ON A PLL WITH SYNCH. FILTER & PI CONTROLLER
Date/Time run: 2/21/89 5: 40: 17
Temperature: 27.0
20V
-20V
v (72)
2.0V
-2.0V
v (950)
20V
-20V
0ms
50ms
100ms
150ms
200ms
250ms
300ms
350ms
-v (10)
v (72)
v (110)
Time

Fig. 5.27

5.11.2 — Voltage Amplitude Perturbation with Second Harmonic: PLL with Analog Filter

Waveforms corresponding to the voltage amplitude perturbation with second harmonic are shown in Fig. 5.28 and its circuit diagram in Fig.5.19. The upper traces shown V(70) and V(80). The bottom trace, V(72), shows the perturbation signal.

The second harmonic produces a very significant phase displacement between the PLL multiplier output V(50) and the input V(72). If we compare this case (see Fig. 5.29) with the previous case when PLL is exposed to the Amplitude Perturbation only, we can see that the amplitude perturbation plays small roll as compared to the effect due to the second harmonic in the transient performance. The phase error between V(10) and V(72) can be clearly observed as the effect of the second harmonic perturbation at the bottom trace of Fig. 5.29.

The settling of the control voltage and therefore, the VCO output voltage V(10) is also illustrated, over a longer time period, in Fig. 5.30. The settling is achieved in about 8 cycles which is longer than in the previous case (3 cycles).

5.11.3 — Voltage Amplitude Perturbation: PLL with Synchronous Filter

The performance of the controller is shown in Fig. 5.31, by means of signals V(51), V(52), V(57) and V(500). The controller output V(54) settles in about 12 cycles. The PI gain was adjusted to $K_p = 0.1$, $K_I = 0.01$.

The settling of this PLL circuit takes longer than in the case of PLL whith analog filter. Fig. 5.32 illustrates the PLL input voltage as compared to the VCO output voltage, V(10). The VCO control voltage is also given.

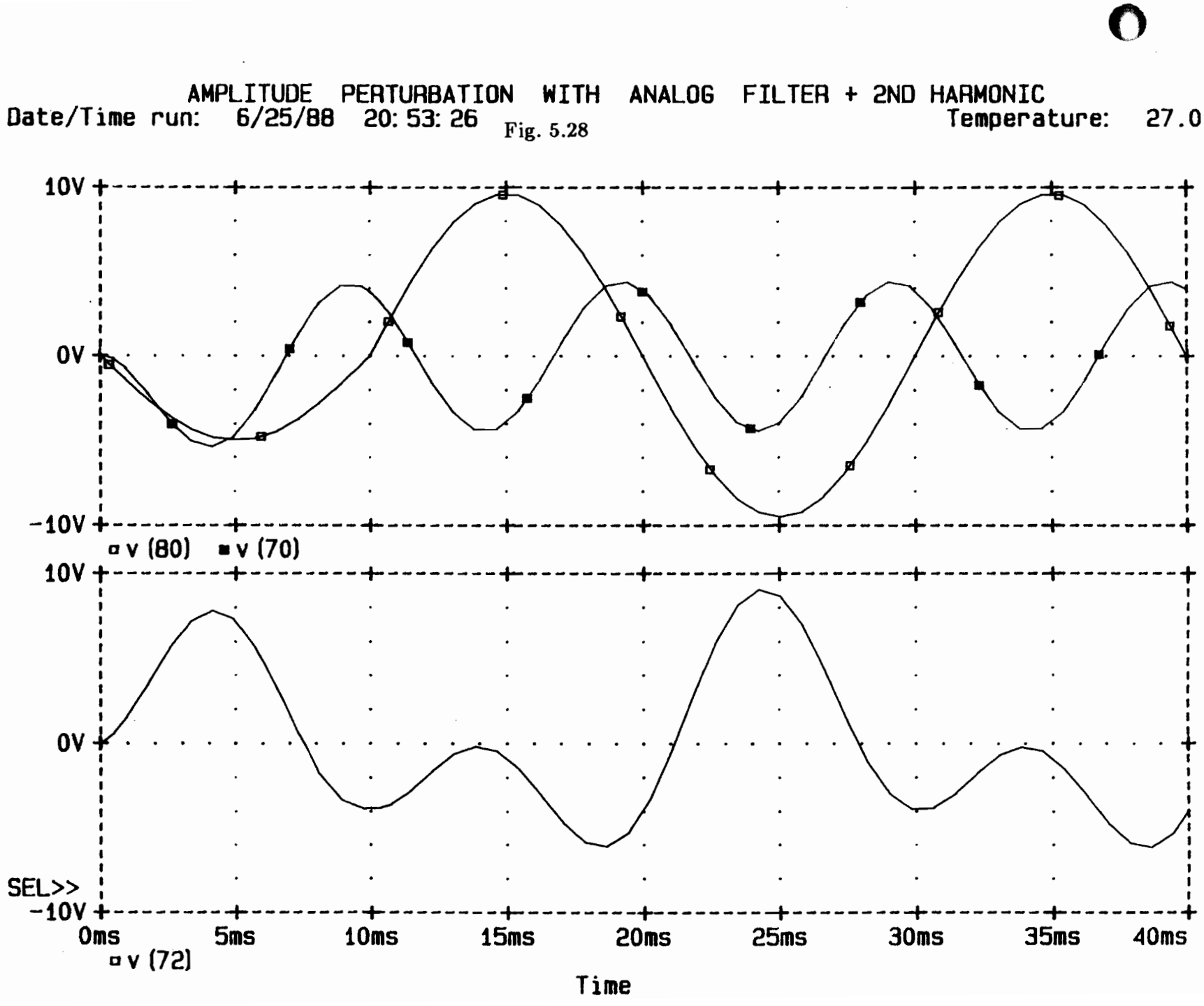

AMPLITUDE PERTURBATION WITH ANALOG FILTER + 2ND HARMONIC
Date/Time run: 6/25/88 20:53:26
Temperature: 27.0
10V
0V
-10V
v (80)
v (70)
10V
0V
SEL>>
-10V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
v (72)
Time

Fig. 5.28

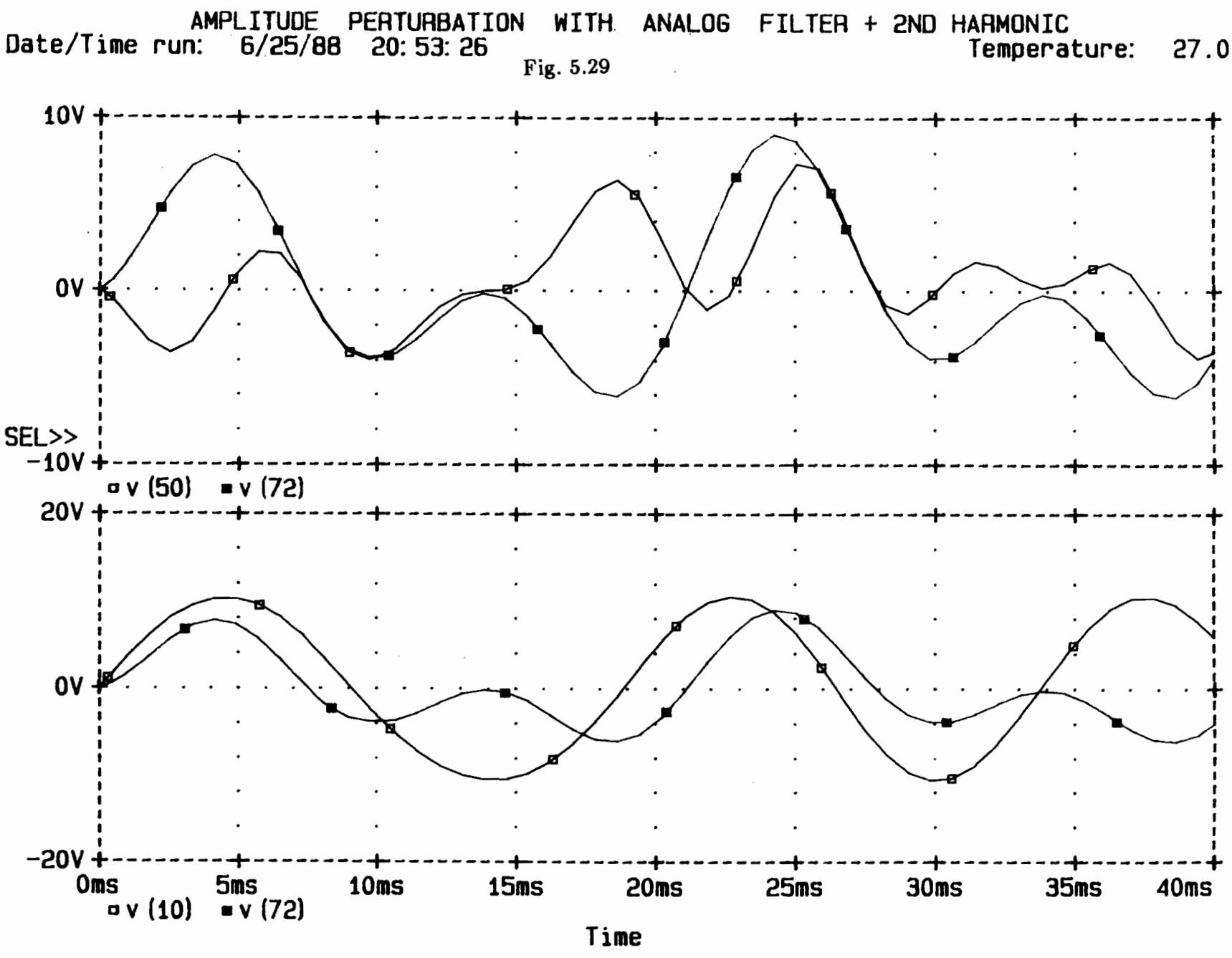

AMPLITUDE PERTURBATION WITH ANALOG FILTER + 2ND HARMONIC
Date/Time run: 6/25/88 20:53:26
Temperature: 27.0
10V
0V
SEL>>
-10V
v (50) v (72)
20V
0V
-20V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
v (10) v (72)
Time

Fig. 5.29

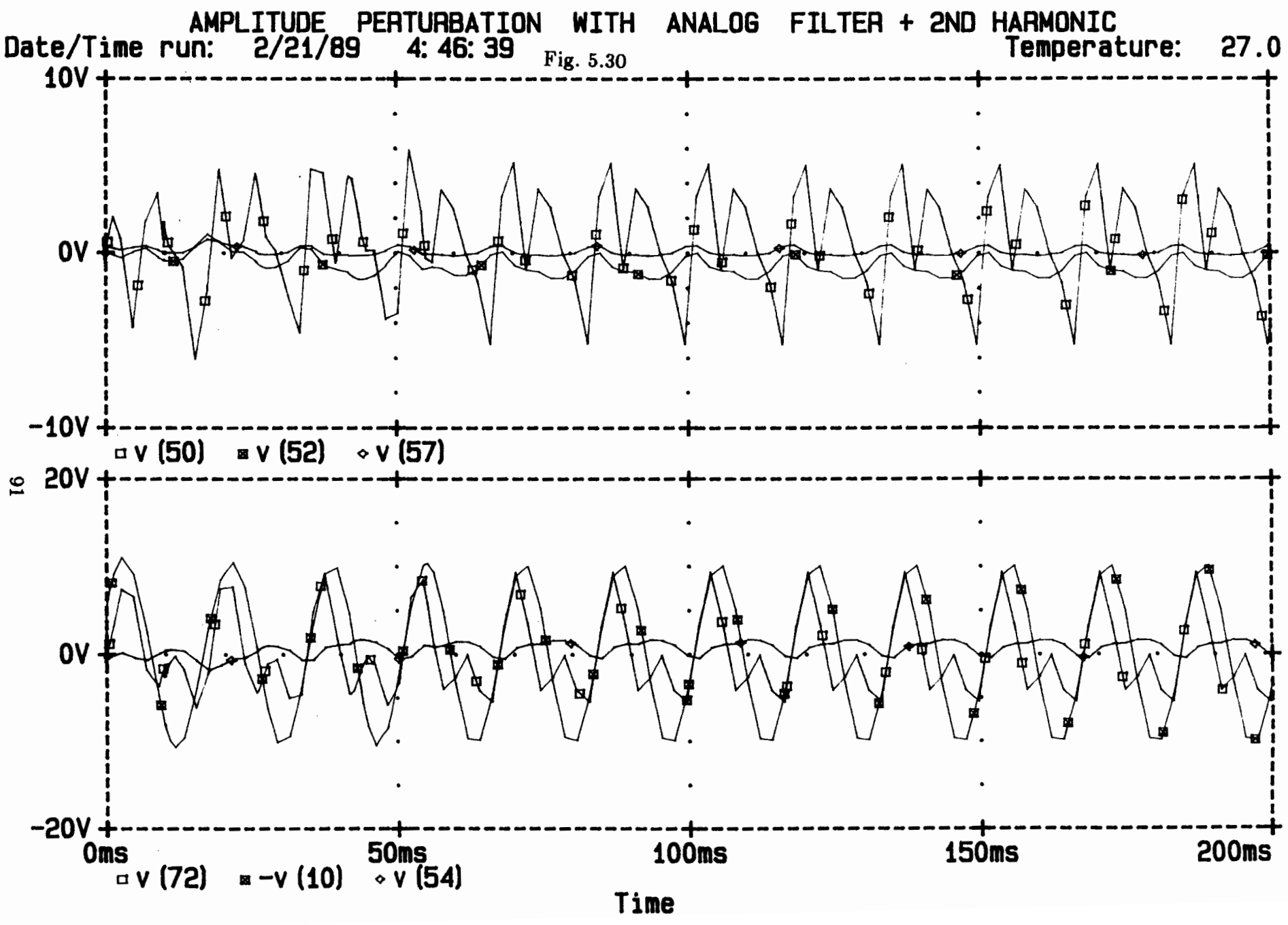
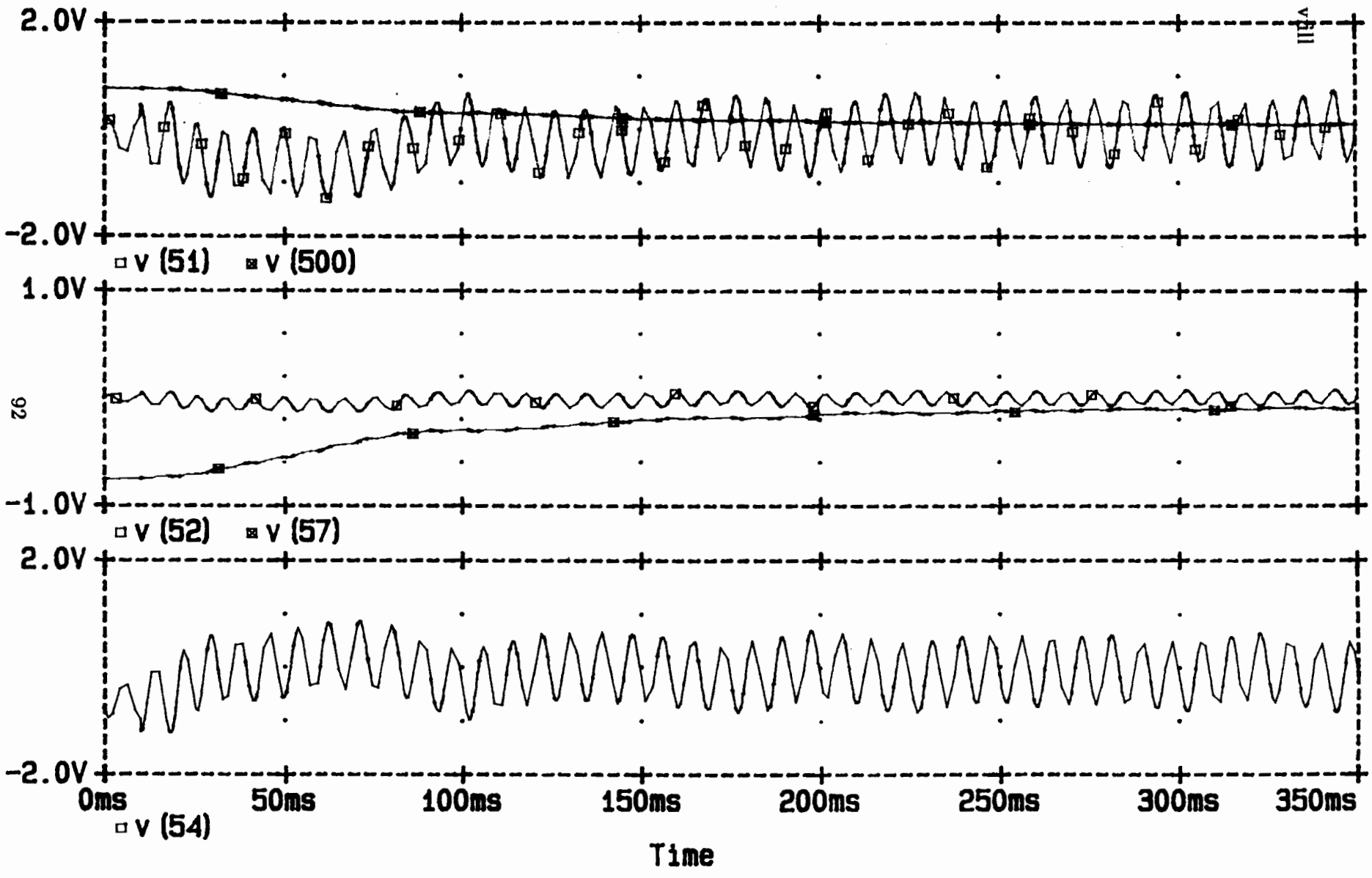

AMPLITUDE PERTURBATION WITH ANALOG FILTER + 2ND HARMONIC
Date/Time run: 2/21/89 4:46:39
Temperature: 27.0
10V
0V
-10V
v (50)
v (52)
v (57)
20V
0V
-20V
0ms
50ms
100ms
150ms
200ms
v (72)
-v (10)
v (54)
Time

Fig. 5.30

AMPLITUDE PERTURBATION ON A PLL WITH SYNCH. FILTER & PI CONTROLLER

Date/Time run: 2/21/89 5:40:17 Temperature: 27.0

Fig. 5.31



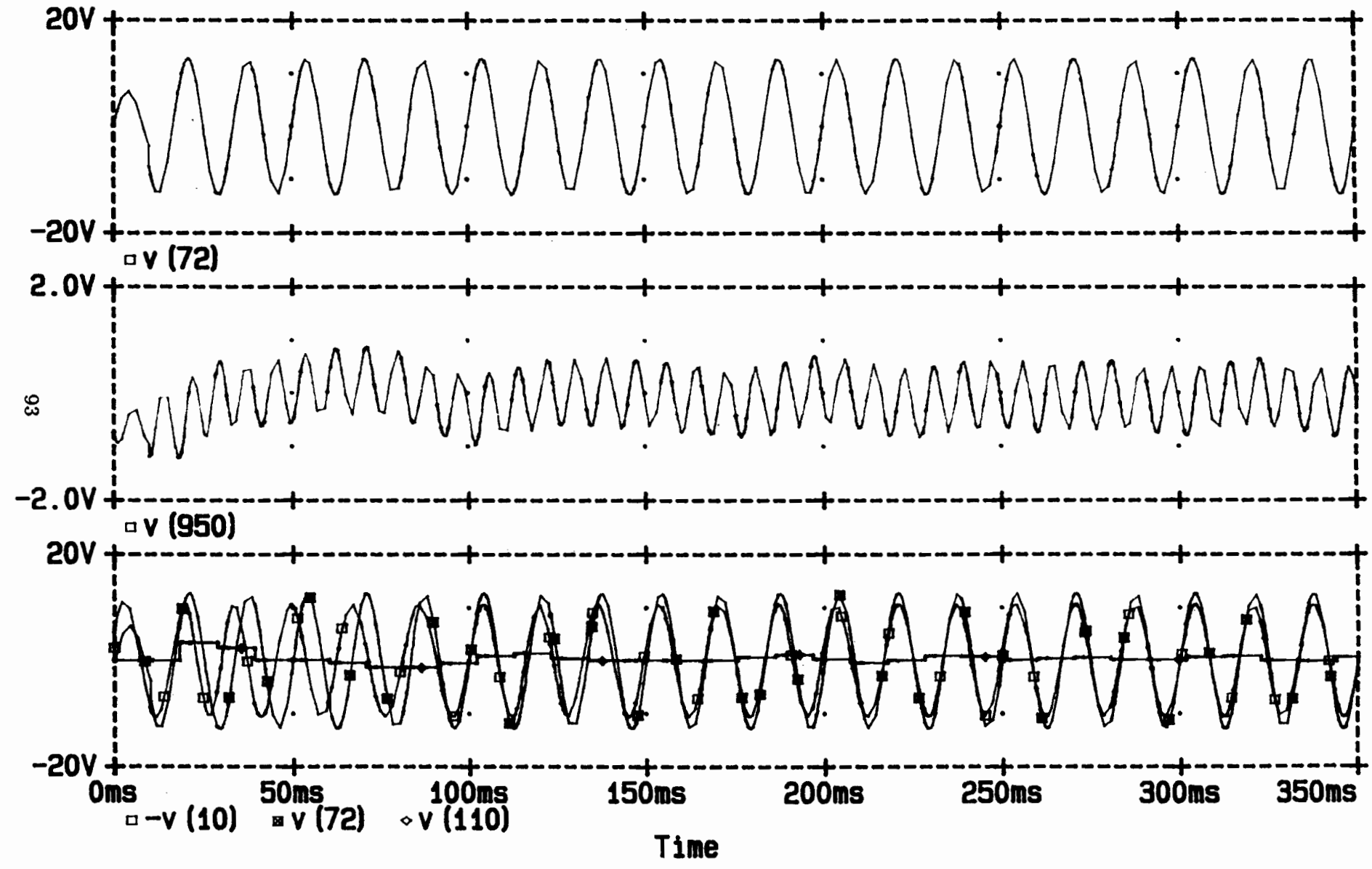

AMPLITUDE PERTURBATION ON A PLL WITH SYNCH. FILTER & PI CONTROLLER
Date/Time run: 2/21/89 5:40:17
Temperature: 27.0
20V
-20V
v (72)
2.0V
-2.0V
v (950)
20V
-20V
0ms
50ms
100ms
150ms
200ms
250ms
300ms
350ms
-v (10)
v (72)
v (110)
Time

Fig. 5.32

5.12 — PLL Harmonic Generation

5.12.1 — Harmonic Analysis

A harmonic analysis will be carried out in order to examen the deviation from the ideal sinusoids waveforms of the VCO outputs value since they are applied for valve firing of the static var compensator. For this, we will use the total harmonic distortion THD factor, as defined by the following expression

$$THD = \frac{100\left(\sum_{n=2}^{m} U_n^2\right)^{\frac{1}{2}}}{U_1} \tag{5.25}$$

where U_1 is the fundamental component of the signal and U_n, $n = 2, 3, \cdots m$ are the harmonic components.

5.12.2 — Fourier Series

The Fourier series of a periodic function f(t) is given by the following expression

$$f(t) = a_0 + \sum_{n=1}^{\infty}\left[a_n \cos\left(\frac{2\pi nt}{T}\right) + b_n \sin\left(\frac{2\pi nt}{T}\right)\right] \tag{5.26}$$

where

a_0 is the average value of the function f(t)

a_n, b_n are the rectangular components of the n_{th} harmonic

The corresponding n_{th} harmonic component vector is given as

$$A_n \angle \phi_n = a_n + \hat{\jmath} b_n \tag{5.27}$$

Its magnitude is

$$A_n = \sqrt{(a_n^2 + b_n^2)} \tag{5.28}$$

while its phase angle is

$$\phi_n = \tan^{-1}\left(\frac{b_n}{a_n}\right) \tag{5.29}$$

The coefficients of the Fourier series are given by

$$a_0 = \frac{1}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}} f(t)\,dt \tag{5.30}$$

$$a_n = \frac{2}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}} f(t)\cos\left(\frac{2\pi nt}{T}\right)\,dt \tag{5.31}$$

$$b_n = \frac{2}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}} f(t)\sin\left(\frac{2\pi nt}{T}\right)\,dt \tag{5.32}$$

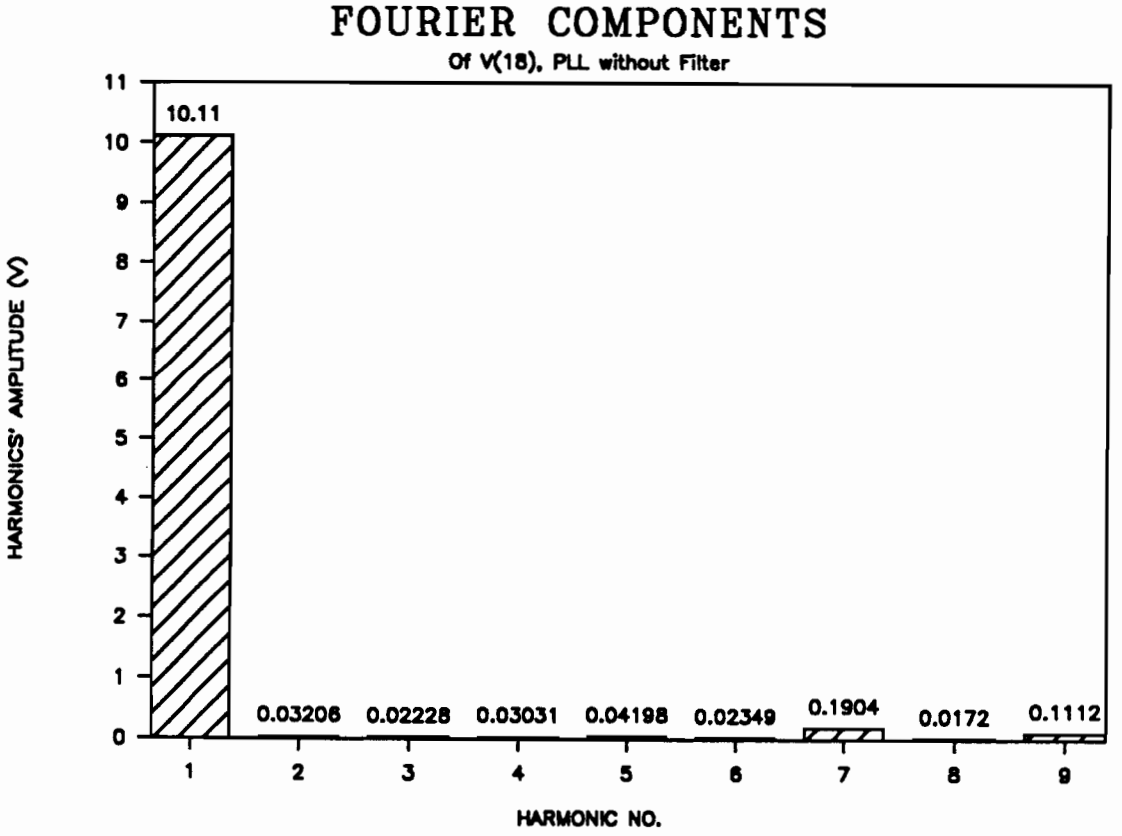
In our analysis, n takes values from 1 to 9 as it is shown by chart 1 and subsequents charts.

CHART No. 5.1
PLL WITHOUT FILTER

Tables No. 5.1 to 5.6 give the total harmonic distortion of the VCO outputs voltages V(18), V(14) and V(10), while charts No.5.1 to 5.6 give the harmonic voltage components of the same outputs signals.

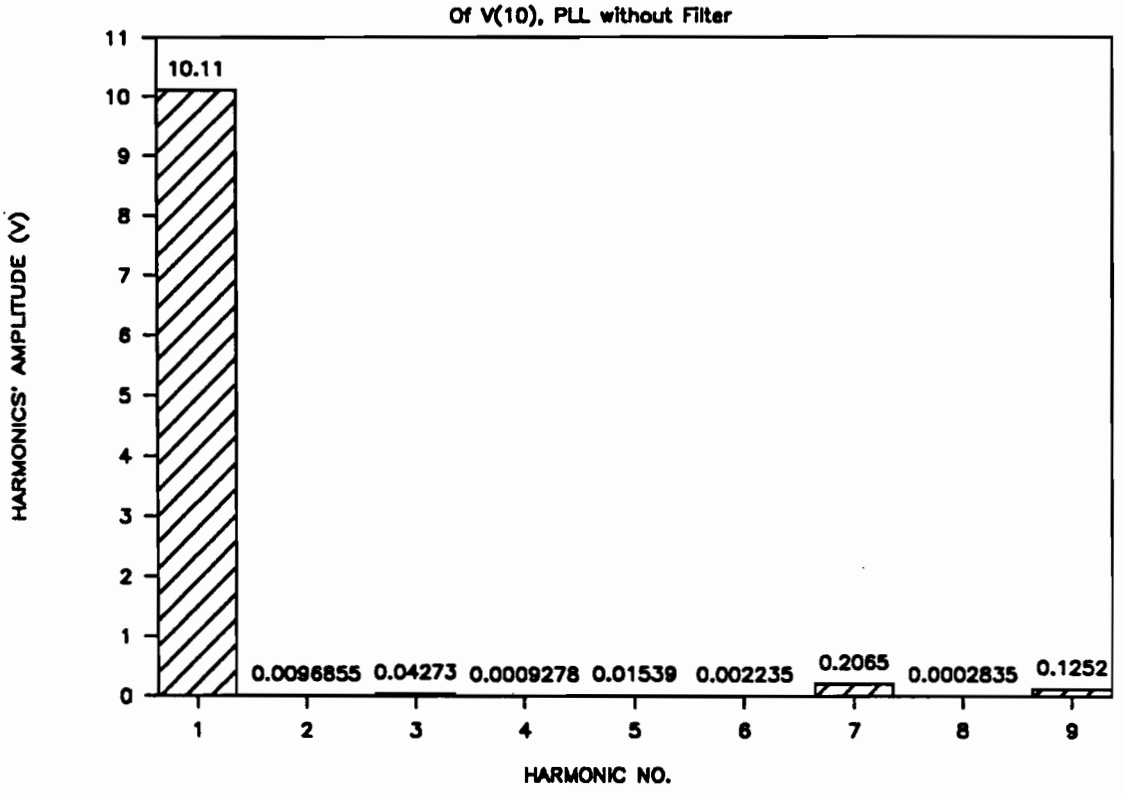
All the calculations were made for the PLL in steady state.

Table No. 5.1 — PLL without filter THD — Total Harmonic Distortion	
Signal	**THD [%]**
V(18)	2.292894
V(14)	2.292927
V(10)	2.433317



FOURIER COMPONENTS

Of V(10), PLL without Filter



FOURIER COMPONENTS

Of V(14), PLL without Filter

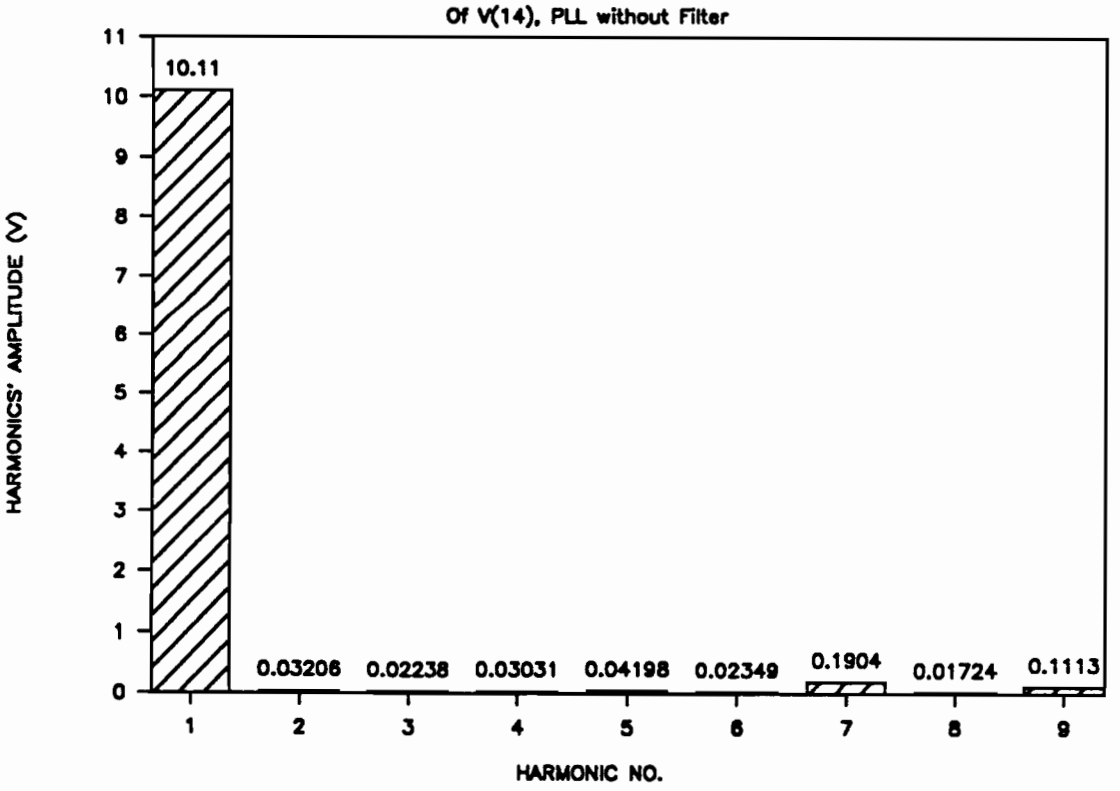
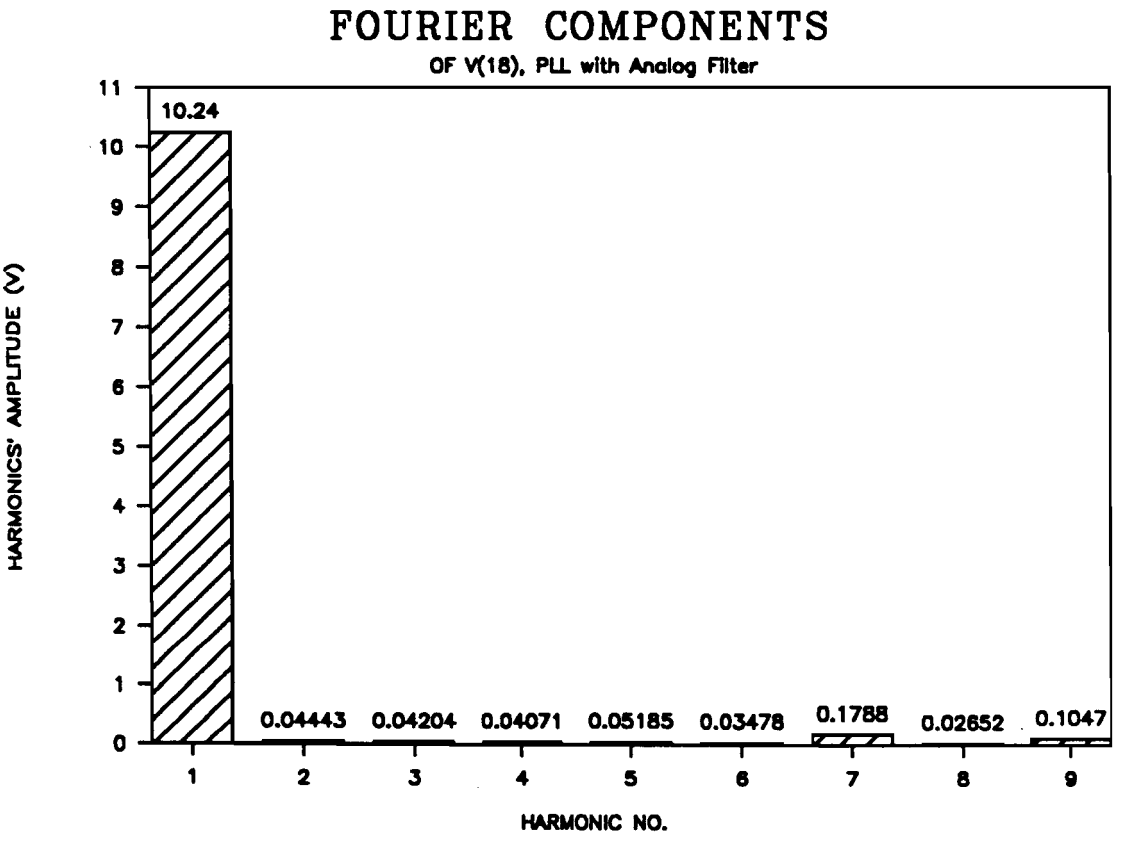


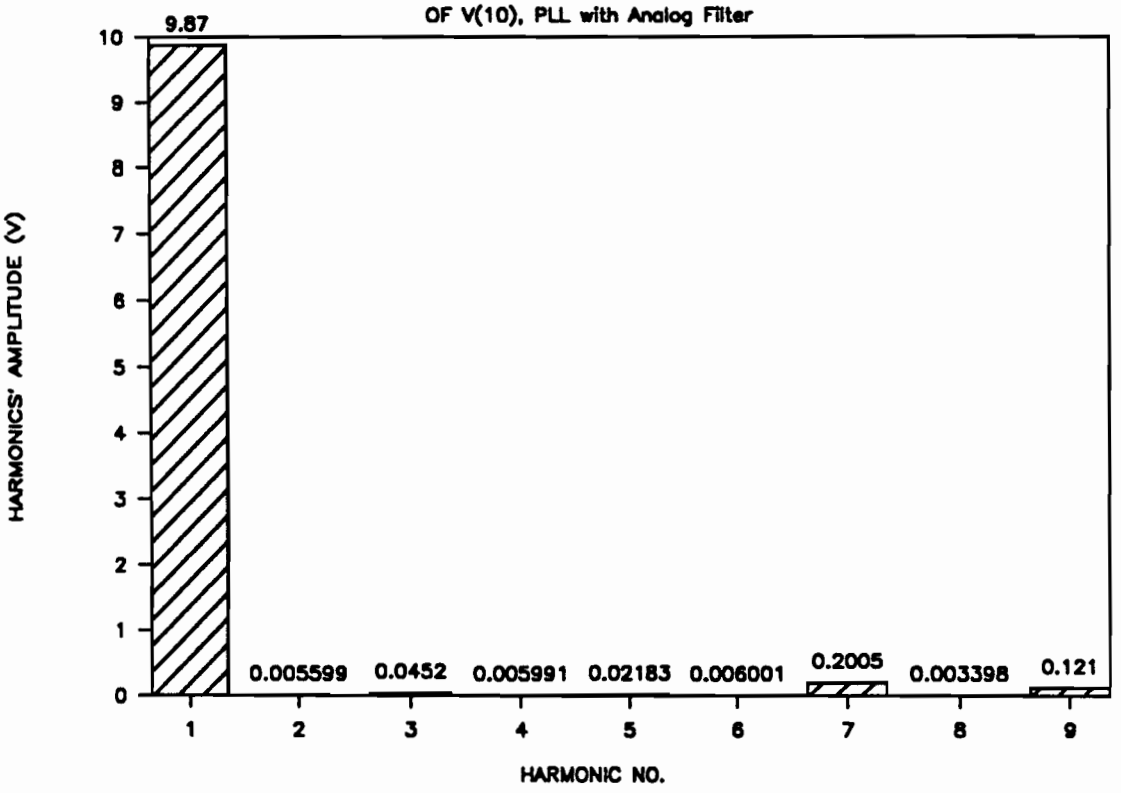
CHART No. 5.2
PLL WITH ANALOG FILTER

Table No. 5.2 — PLL with Analog Filter THD — Total Harmonic Distortion	
Signal	**THD [%]**
V(18)	2.247115
V(14)	2.246886
V(10)	2.428959



FOURIER COMPONENTS

OF V(10), PLL with Analog Filter



FOURIER COMPONENTS

OF V(14), PLL with Analog Filter

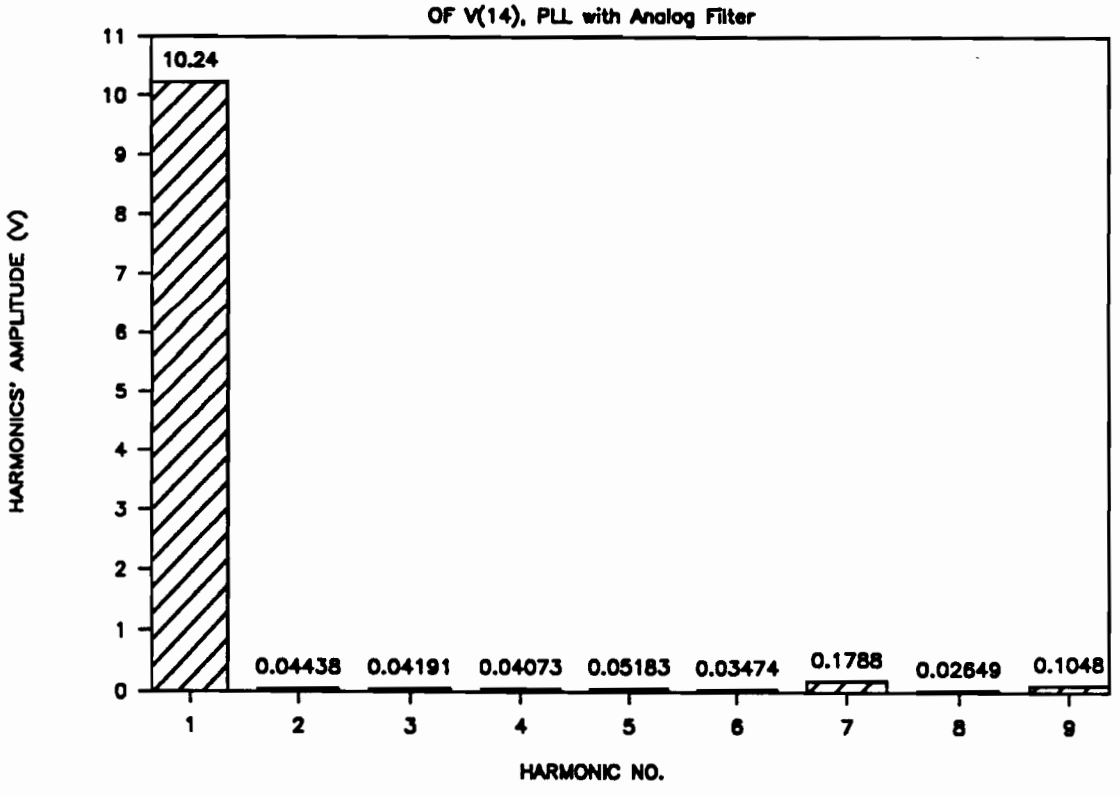
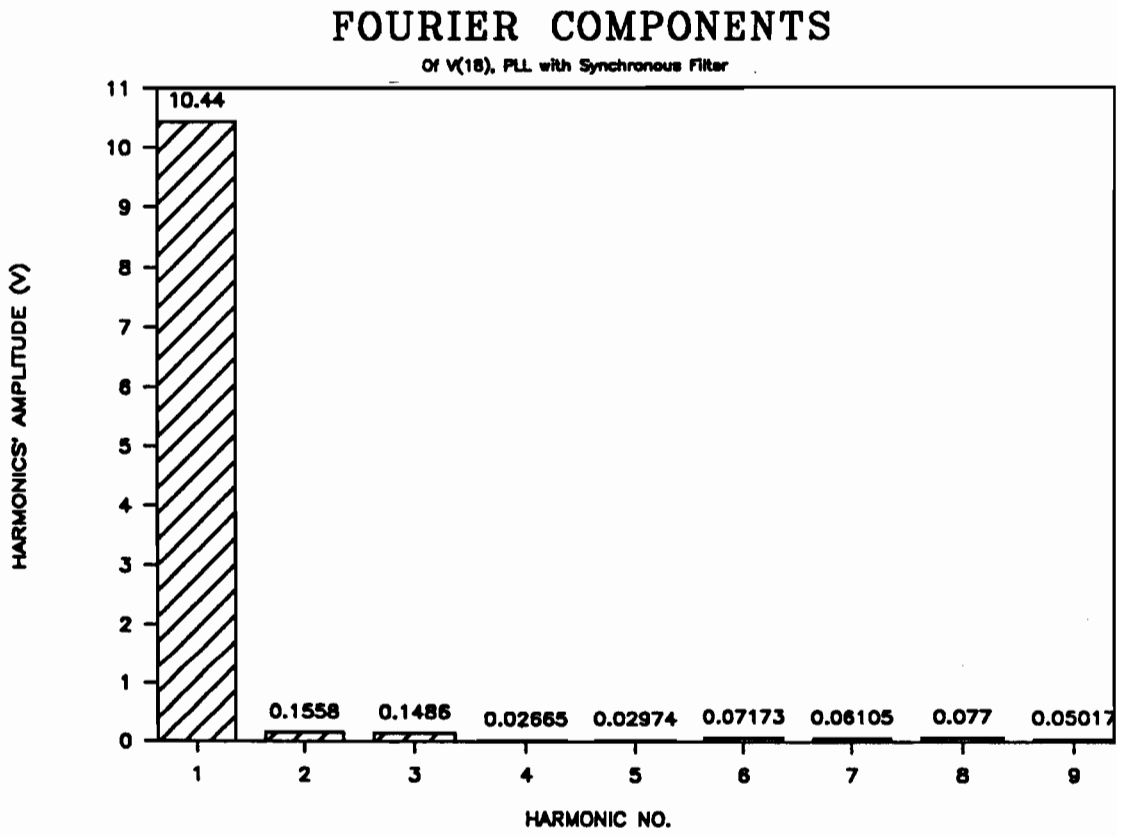
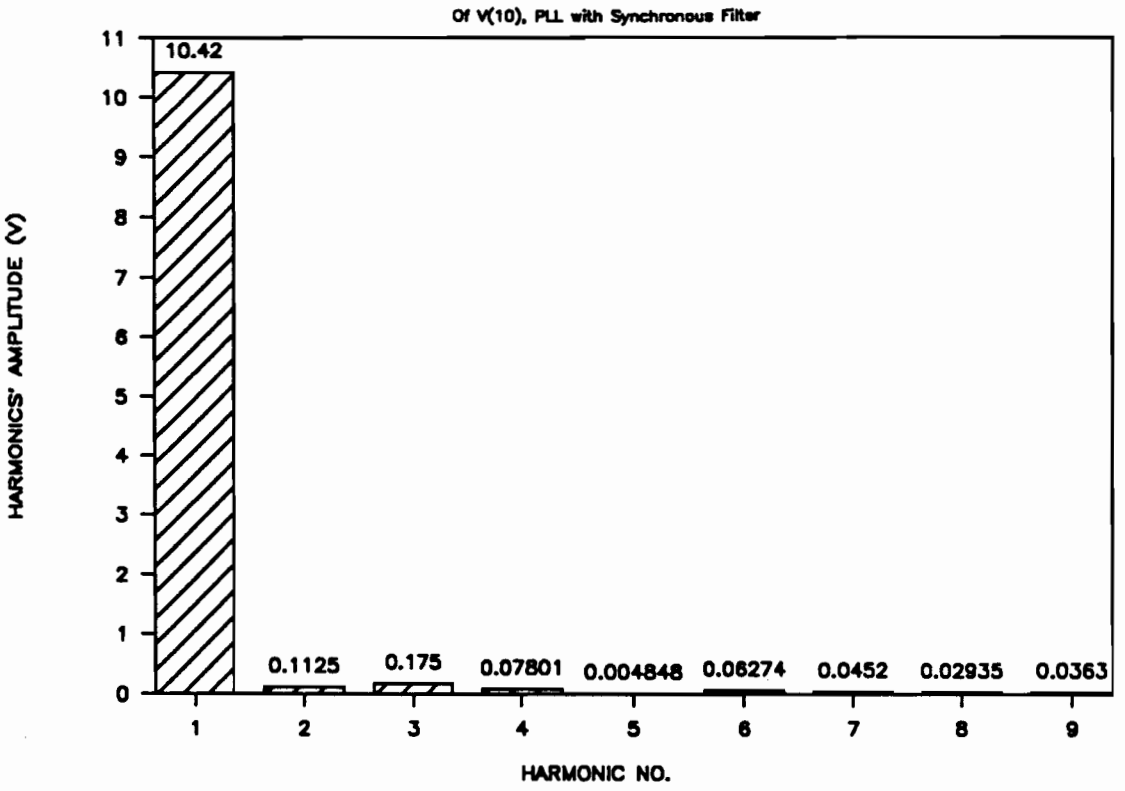


CHART No. 5.3
PLL WITH SYNCHRONOUS FILTER

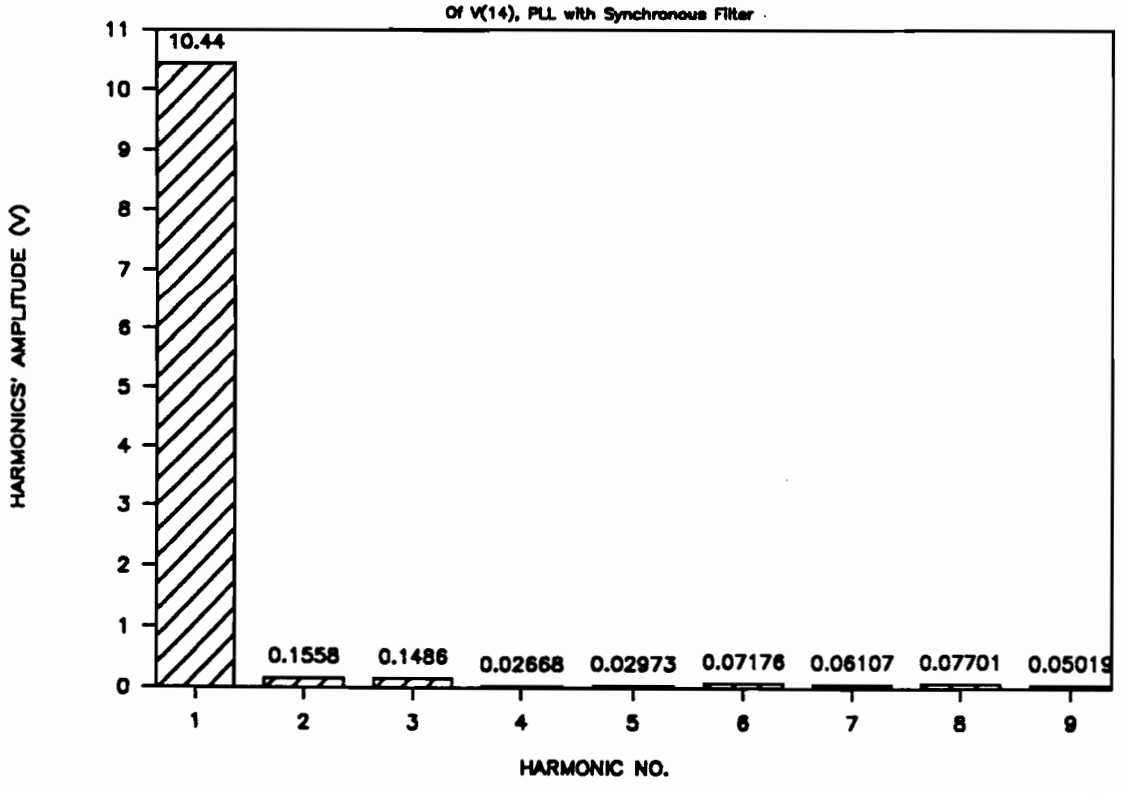
Table No. 5.3 — PLL with Synchronous Filter THD — Total Harmonic Distortion	
Signal	THD [%]
V(18)	2.447119
V(14)	2.447381
V(10)	2.301698



FOURIER COMPONENTS



FOURIER COMPONENTS



5.13 — Second Harmonic Effect on the PLL Circuit

Our interest in testing the effect of the second harmonic on the phase-locked loop, is due to the fact that this component can distort the VCO outputs.

In power systems the second harmonic voltages are generated by various system components. Transformers when energized generates a flux-density which can reach peak level in between 2 to 3 p.u.. For a normally designed transformer, this can create peak flux densities of about 3.4 or 4.7T respectively. When this is compared to the saturation flux density levels of around 1.8-2.0 it can be seen that transformer core will be driven to extreme saturation levels and will thus draw excesive exitation current of up to 5-20 p.u. on the rating (as compared to the normal magnetizing of a less than 1 percent) . This is the so-called Inrush Current. The second harmonic of this current is very significant as its evolution with time is shown in Fig. 5.33.

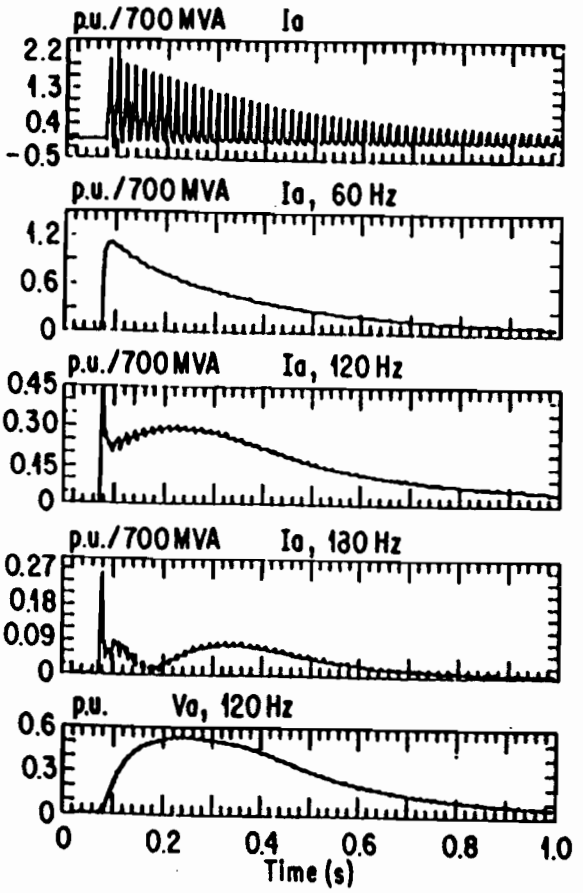
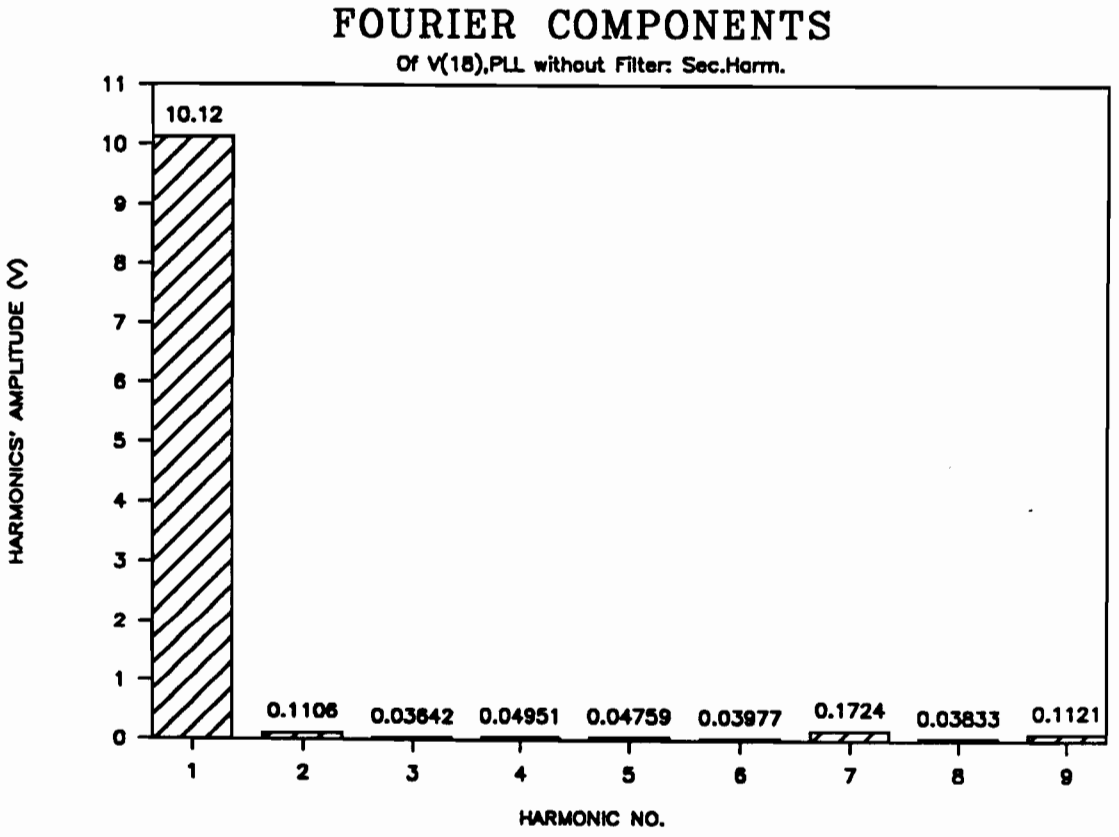


Fig. 5.33 Variation of Inrush current with time

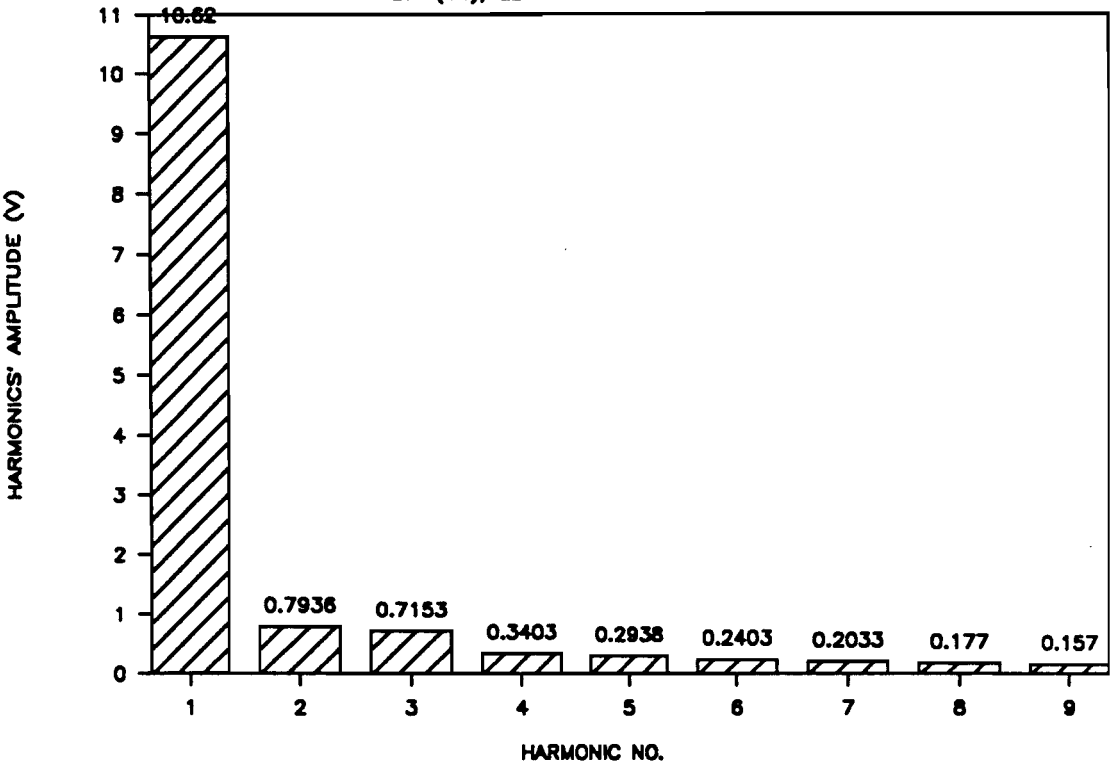
CHART No.5.4
PLL WITHOUT FILTER: SECOND HARM. EXCITATION

Table No. 5.4 — PLL without filter: Second harmonic excitation THD — Total Harmonic Distortion	
Signal	THD [%]
V(18)	2.492781
V(14)	2.492955
V(10)	2.709775



FOURIER COMPONENTS

Of V(14),PLL without Filter: Sec.Harm.



FOURIER COMPONENTS

Of V(10),PLL without Filter: Sec.Harm.

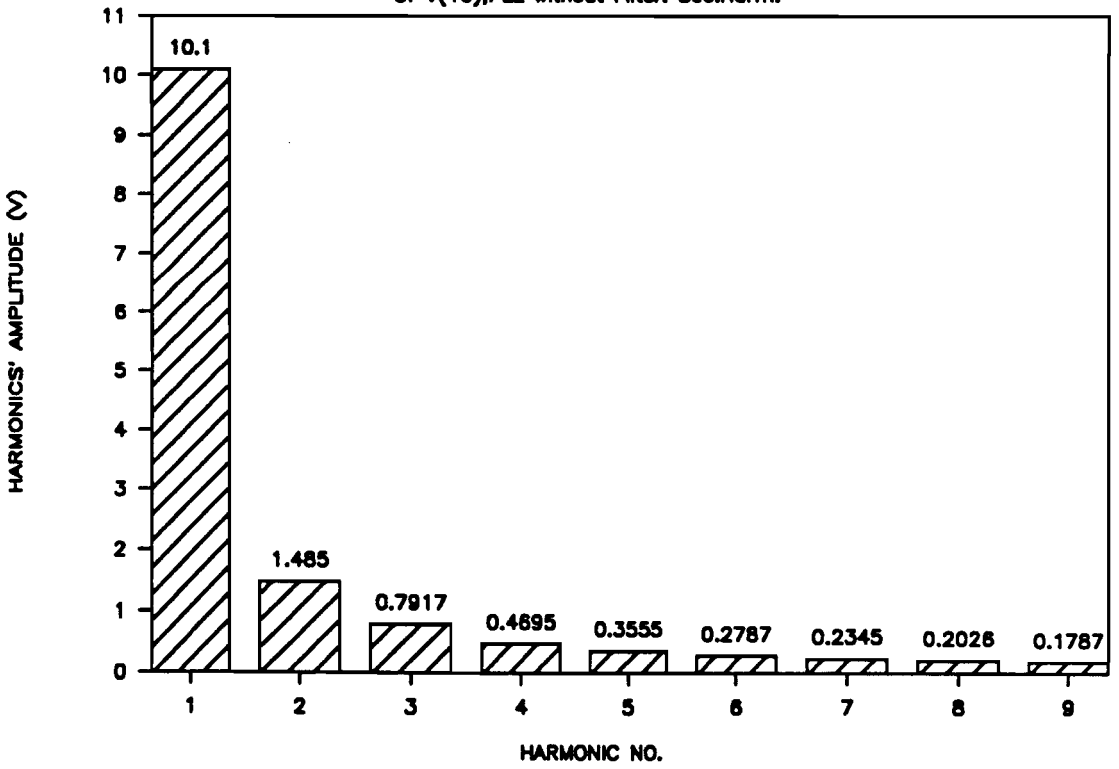
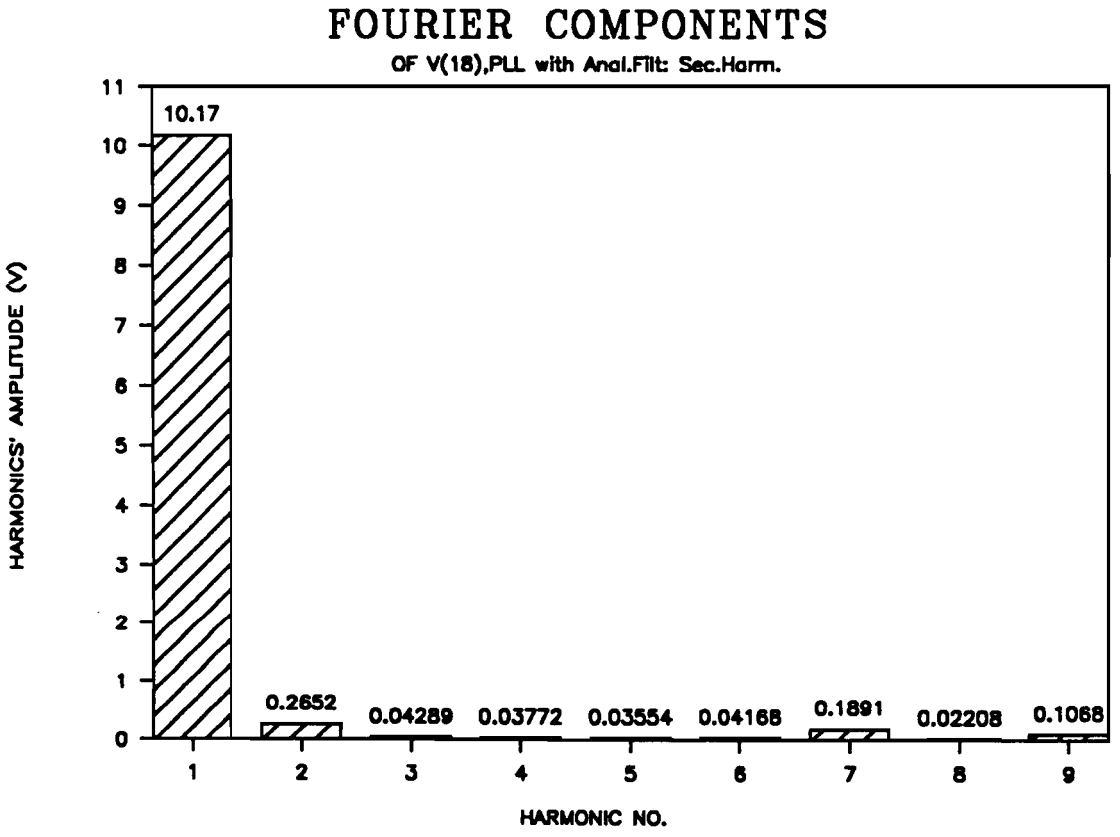
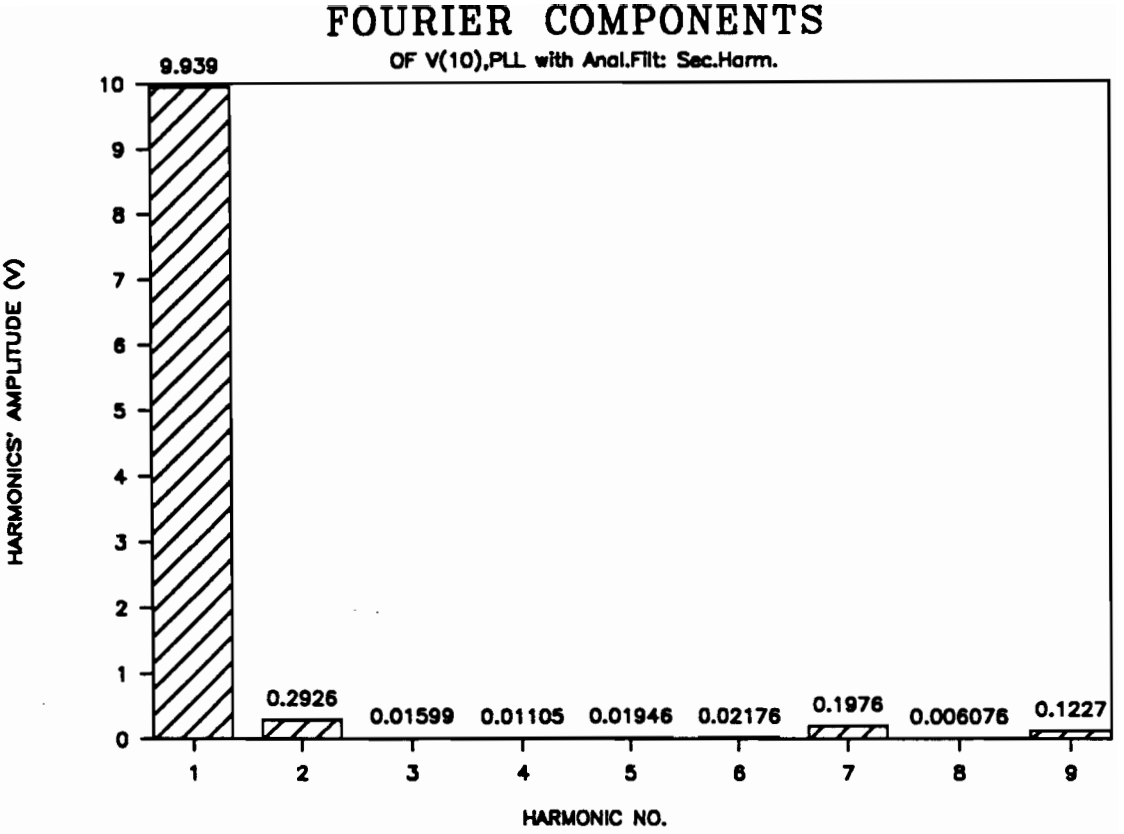


CHART No.5.5
PLL WITH ANALOG FILTER: SECOND HARMONIC EXCITATION

Table # 5.5 — PLL with Analog Filter: Second harmonic excitation THD — Total Harmonic Distortion	
Signal	**THD [%]**
V(18)	3.464653
V(14)	3.464679
V(10)	3.778089




FOURIER COMPONENTS
OF V(10),PLL with Anal.Filt: Sec.Harm.
HARMONICS' AMPLITUDE (V)
HARMONIC NO.
9.939
0.2926
0.01599
0.01105
0.01946
0.02176
0.1976
0.006076
0.1227

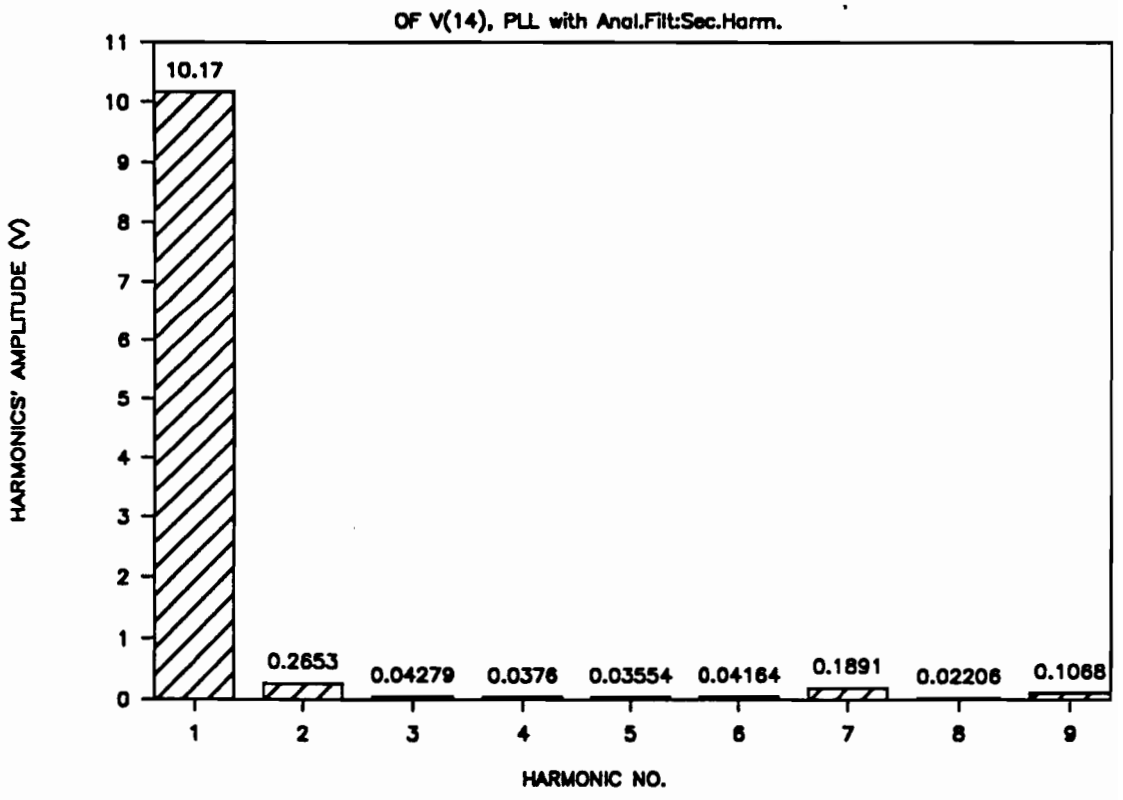
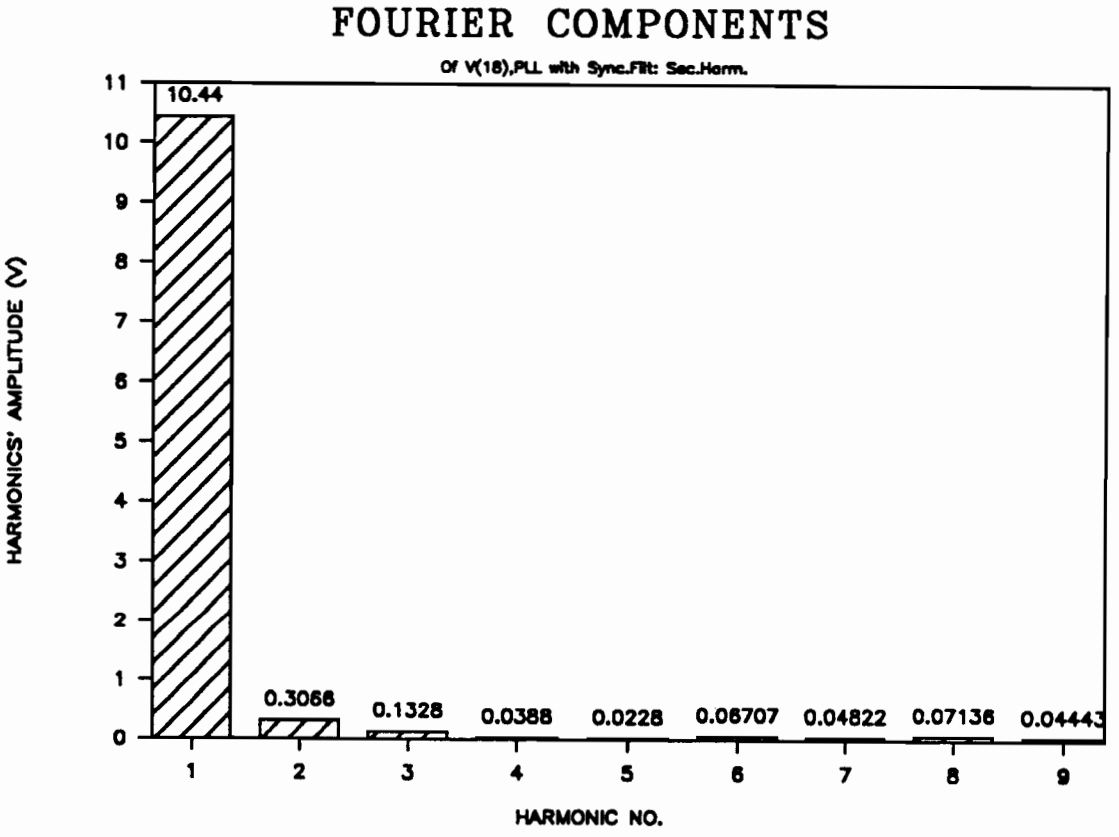
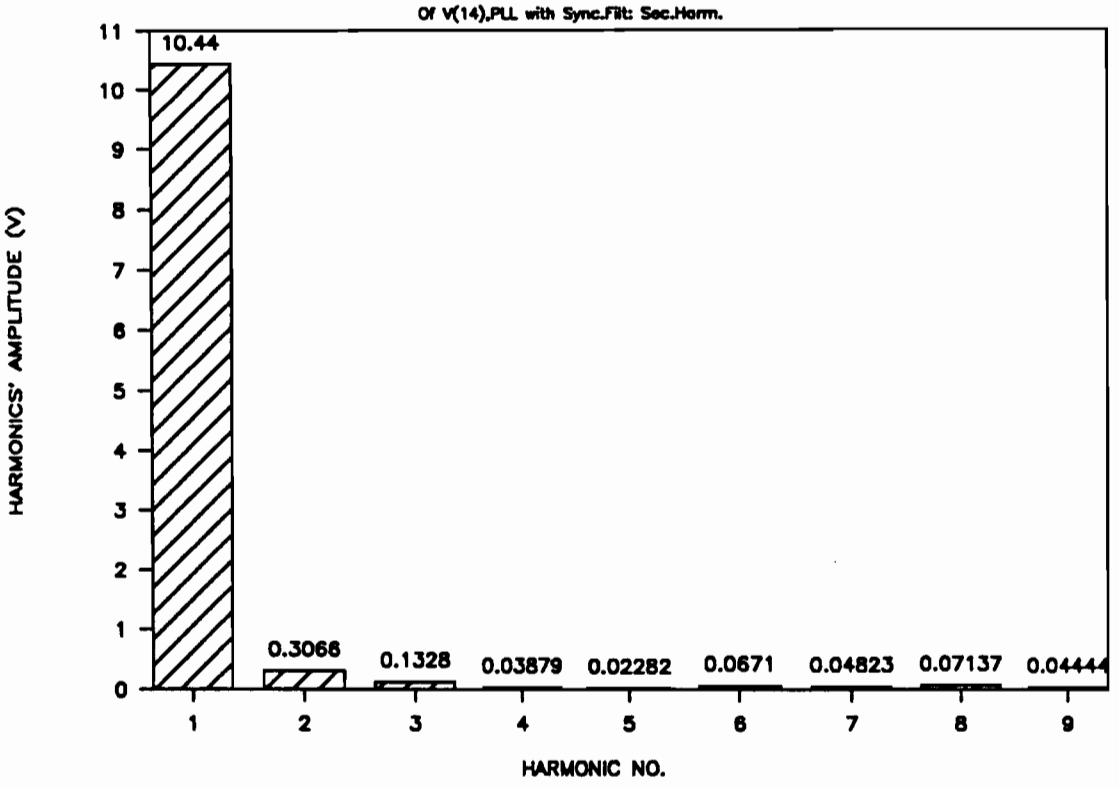

FOURIER COMPONENTS
OF V(14), PLL with Anal.Filt:Sec.Harm.
HARMONICS' AMPLITUDE (V)
HARMONIC NO.
10.17
0.2653
0.04279
0.0376
0.03554
0.04164
0.1891
0.02206
0.1068

CHART No. 5.6
PLL WITH SYNCHRONOUS FILTER: SECOND HARM. EXCITATION

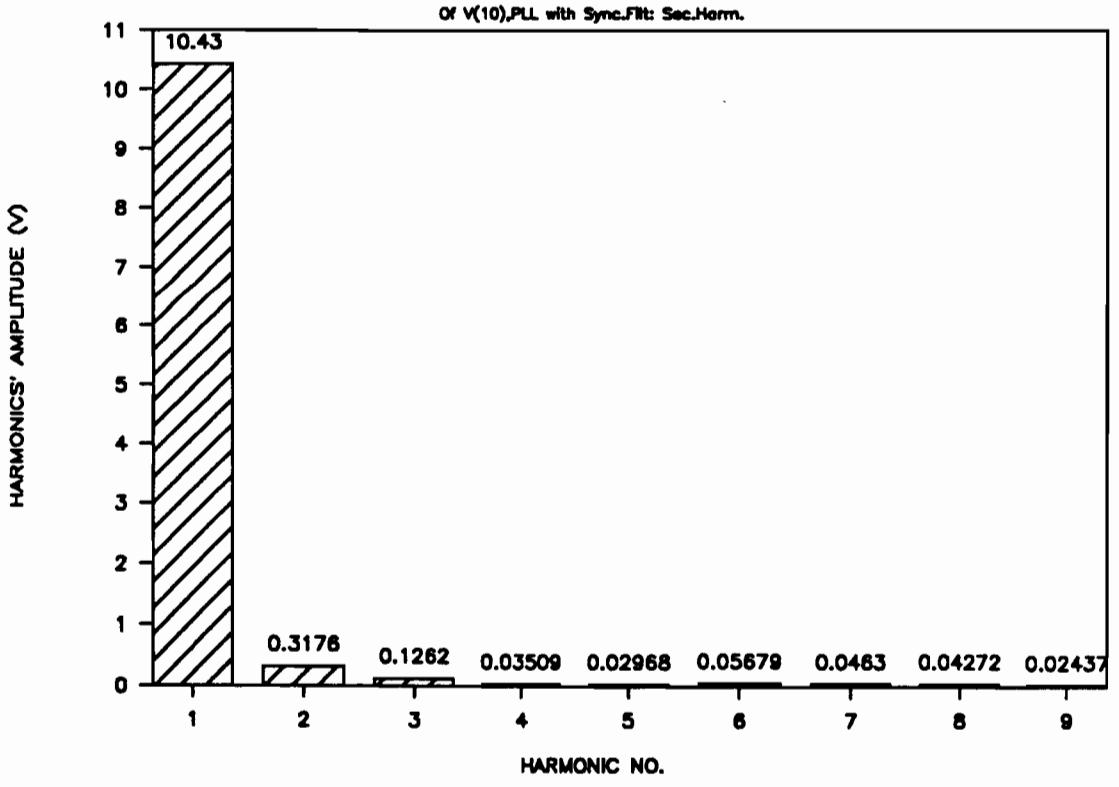
Table # 5.6 — PLL with Synchronous Filter: Second harmonic excitaton THD — Total Harmonic Distortion	
Signal	**THD [%]**
V(18)	3.422397
V(14)	3.422410
V(10)	3.412361



FOURIER COMPONENTS



FOURIER COMPONENTS



From charts and tables No. 5.1 to 5.6 the following conclusions can be drawn:

In general, the phase-locked loop without filter has a better performance (from the total harmonic distortion point of view) than the PLL with an analog and synchronous filter.

The total harmonic distortion is somewhat greater than 2% in the cases of the phase-locked loop without second harmonic excitation.

The total harmonic distortion is less affected in the case of the PLL without filter (it remains arround 2%)than the the two other cases.

The effect of the second harmonic excitation on the VCO output voltages is significantly increased in the of the PLL with analog and synchronous filter.

5.14 — Summary

This chapter has dealt with the phase-locked loop modelling. The PLL was simulated in details by means of *PSPICE* simulation program. Three PLL configurations were considered: PLL with PI controller, PLL with PI controller including the first order filter and the PLL with PI controller including the synchronous (Fourier) filter. Their dynamic response is evaluated for step phase perturbation and step amplitude perurbation of the input voltage.

The PLL harmonic performance was evaluated using the input voltage including the steady-state second harmonic component. In addition, the combination of such perturbations signals were also applied. Fourier analysis was used in order to asses the harmonic generation of the PLL itself as well as when excited by the second harmonic component at its input.

EXPERIMENTAL RESULTS

CHAPTER 6

EXPERIMENTAL ANALYSIS OF THE PHASE-LOCKED LOOP

6.1 — Introduction

In the previous chapter, we modelled a number of the phase-locked loop configurations. In most of these simulations we used simplified models for some types of electronic components as it was the case of the operational amplifiers (model μA 742, μA 743 and μA 744) and the multiplier.

In this chapter we are going to present test results of different PLL configurations realized in the laboratory. The prime objective of such tests is to validate our *PSPICE* models since their validity is an important factor to model development by simulation.

6.2 — PLL Steady-State Operation

In steady-state operation there is not any perturbation. Neither second harmonic exitation is present in the input signal.

We should recall also that the circuit implemented in the experiment corresponds fully to the one used in the simulation, with regard to its configuration as well as to its parameters.

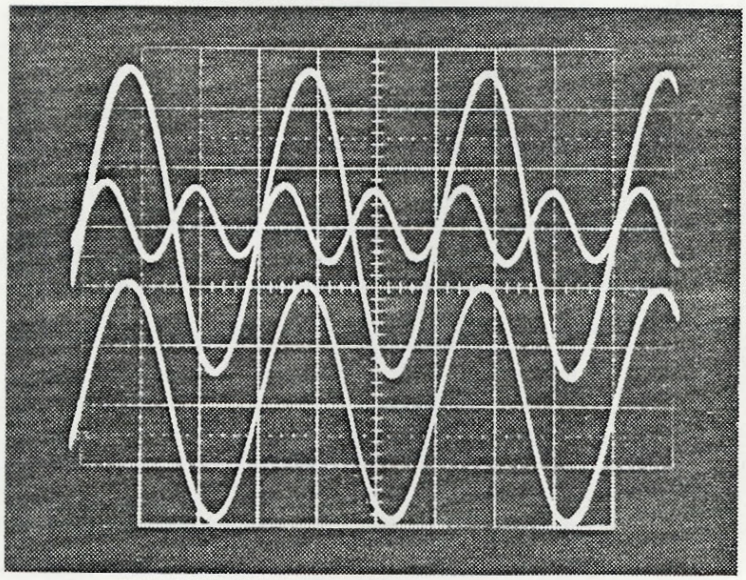


Fig. 6.1 Characteristic PLL signals

The waveforms concerning the PLL multiplier are shown in Fig. 6.1, where we can see the input signal from the network, the PLL multiplier output (on the top) and the feedback signal from the voltage contolled oscillator (VCO). They behave exactly according to what is to be expected: (1) the VCO output is in synchronism with the network voltage , (2) the multiplier output consists of a second harmonic component only, (3) the VCO output has a negligible harmonic distortion.

6.3 — VCO Voltage Amplitude Control

Figures 6.2 and 6.3 show the waveforms correponding to the voltage amplitude control circuit. The first one illustrates the square of $\sin \omega t$ and $\cos \omega t$ and the second one shows the voltage reference, the squared voltage derived as a sum of the two signals shown above and the error signal as a result of the comparison.

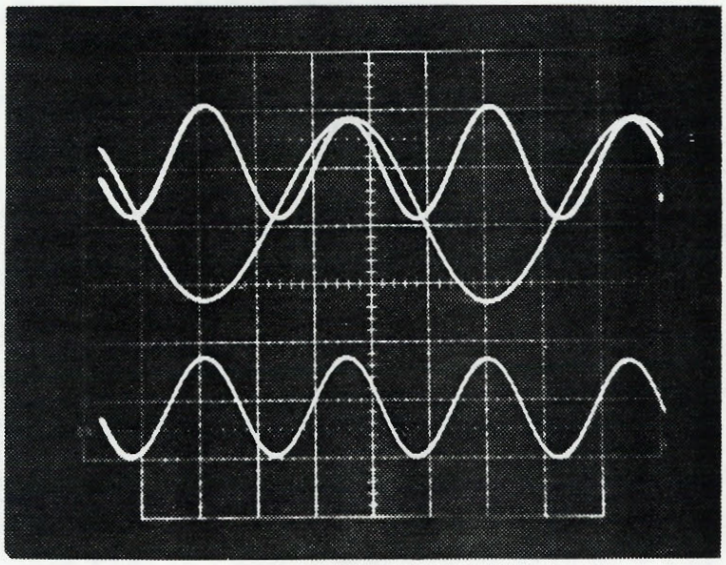


Fig. 6.2 Squared VCO voltages

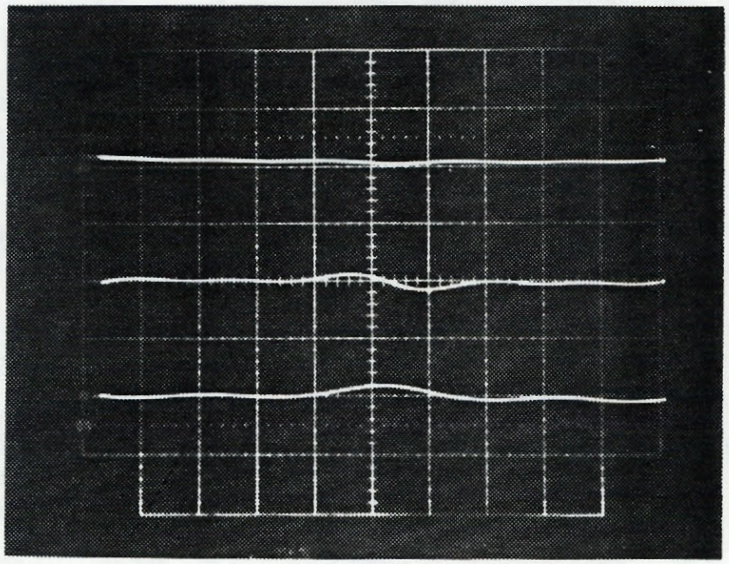


Fig. 6.3 Rectified VCO voltages

6.4 — Performance of the PI Controller

An excessive increase of the controller gain K_p or a decrease of the integration constant K_I, can lead to an unstable operation (see Fig.6.5).

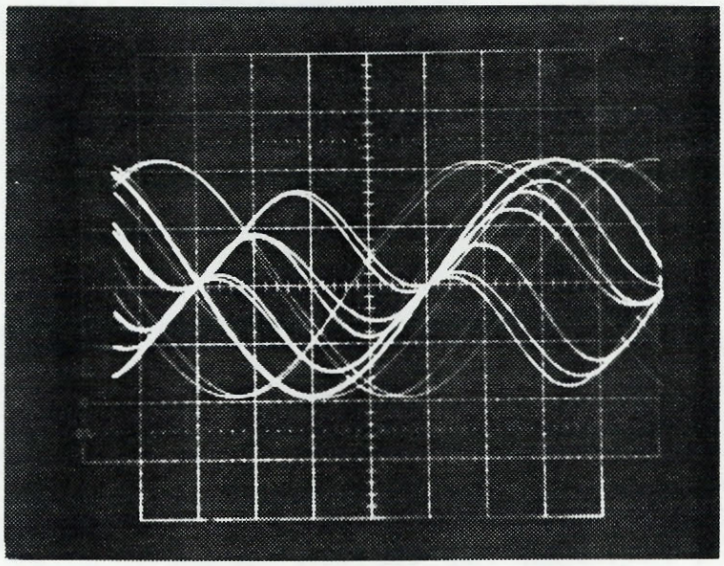


Fig. 6.4 Unstable operation of the VCO

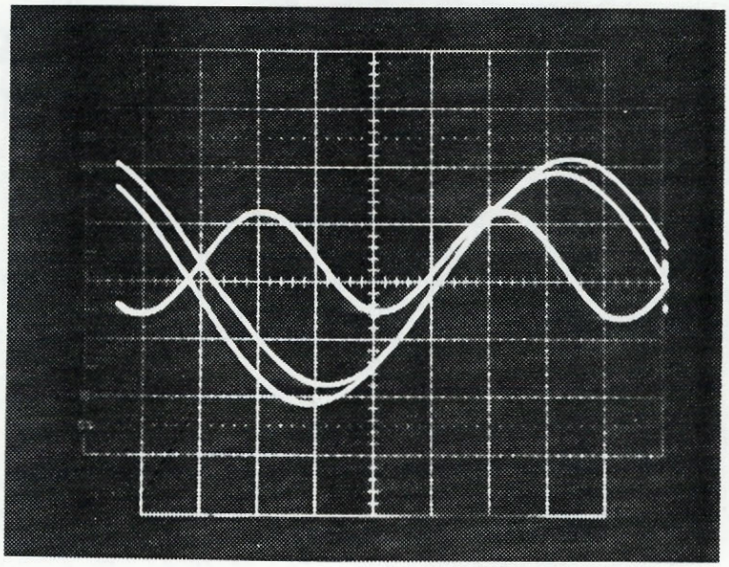


Fig. 6.5 Vin and Vosc phase error

An optimal P controller with its gain K_p, gives a rapid settling, as shown in Fig. 6.5 but the phase error remains non-zero. An optimal PI controller gives a fast settling with a steady-state phase error equal to zero. The values of K_I and K_p are taken according to those determined in the simulation.

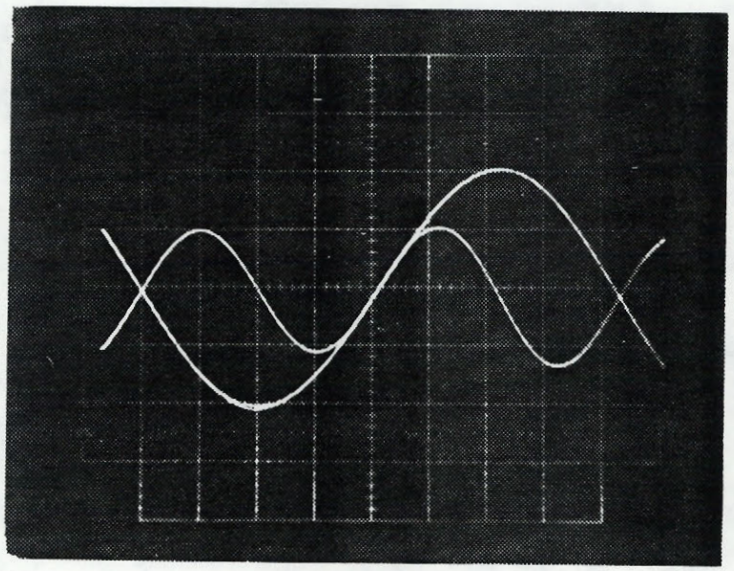


Fig. 6.6 Vin and Vosc in phase

Fig. 6.6 illustrates the network and the feedback signals in synchronism and in phase (overlaped traces) . The second harmonic shown in the picture corresponds to the output of the PLL multiplier.

6.5 — PLL with an Analog Filter: Second Harmonic Excitation

This test was carried out taking into account the excitation by the second harmonic component in the network voltage signal. The procedure was the same as the one performed in the simulation. The harmonic was added to the fundamental component. A distorsioned signal is then applied to the input of the phase-locked loop as it can be seen in Fig. 6.7.

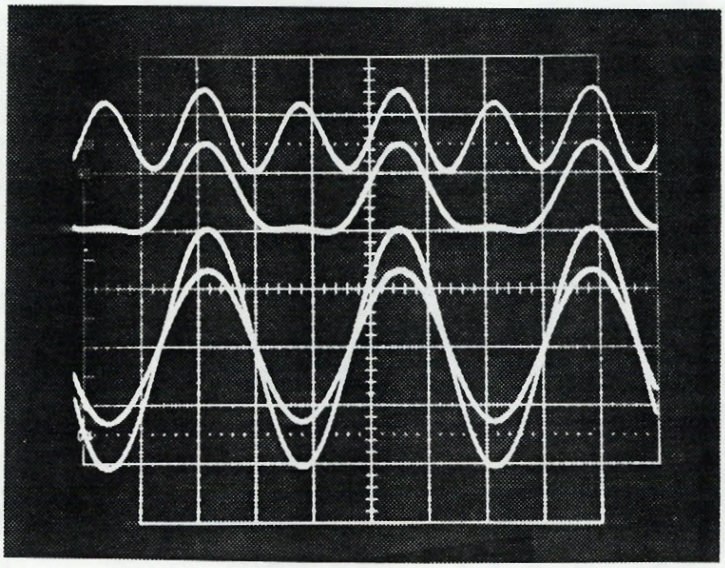


Fig. 6.7 Network and VCO signals of the PLL with analog filter

In this oscillogram, four waveforms can be distinguished: the second harmonic, the distorsioned input signal, the fundamental component of the input signal and the VCO output voltage.

The analog filter behaves very well since a little distorsion is present in the VCO output.

6.6 — PLL without Filter

In this case a PI controller without filter is considered. The effect on the VCO voltage is shown in oscillogram of Fig. 6.8.

The second harmonic effect becomes significant in this case as compared to the previous case when the filter is apllied without the PI controller.

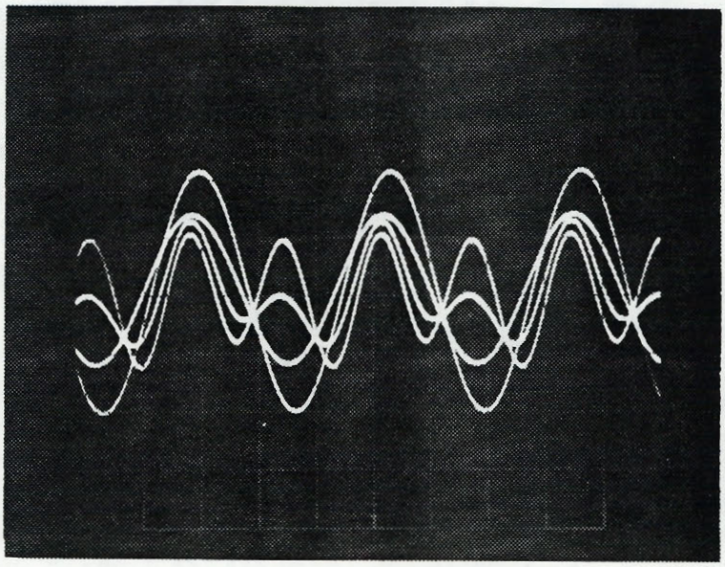


Fig. 6.8 Network and VCO signals of the PLL with PI controller without the filter

This distortion could affect the performance of the power circuit of the static var compensator since it shifts the voltage zero-crossing, and hence the thyristors firing. In Fig. 6.9, the phase displacement produced by this distortion, is more clearly distinguished.

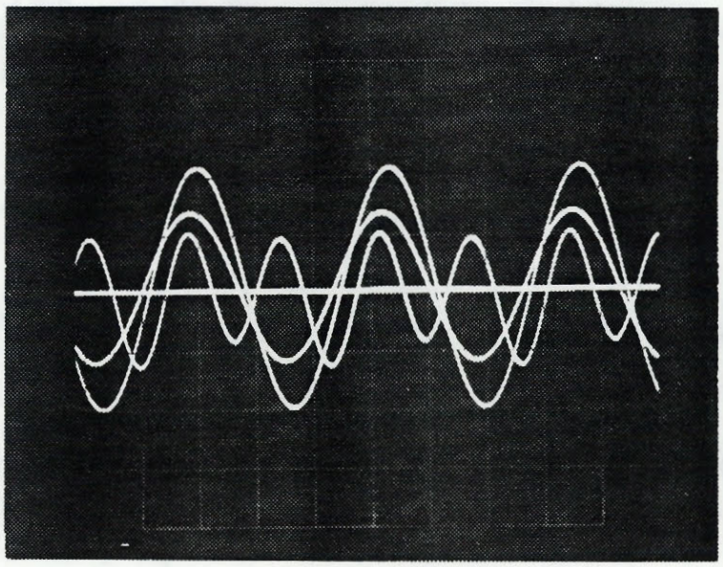


Fig. 6.9 PLL with PI controller exposed to the second harmonic excitation

In this test, we have also verified the approximate linear relation between VCO control voltage and VCO output frequency. The lock range was also found to be 10 Hz arround the nominal frequency of 60 Hz.

6.7 — Phase Perturbation

The circuit diagram, shown in Fig 6.10, utilized to perform the phase perturbation test is somewhat different, from the one implemented in *PSPICE*. The difference is with respect to some functions of the circuit.

In the particular $v(t) = |V| \cos \omega t$ has been realized by the circuit included in Fig. 6.10.

From Fig. 6.10, we deduce the following transfer functions for both stages

$$W_1(s) = -\frac{R_2}{R_1} \frac{1}{1 + R_2 C s} \tag{6.1}$$

and

$$W_2(s) = -\frac{R_{22}}{R_{21}} \frac{1}{1 + R_{22} C_{21} s} \tag{6.2}$$

For $s = \hat{\jmath}\omega$ and $R_{12}C_{11} = R_{22}C_{21} \simeq 1 + \epsilon_1$, $R_{12}/R_{11} = R_{22}/R_{21} \simeq 1 - \epsilon_2$, the total gain becomes

$$\frac{R_{12}}{R_{11}} \frac{R_{22}}{R_{21}} \simeq 1 - \delta_2 \tag{6.3}$$

while the phase-lag is given by

$$tan^{-1}(\omega R_{12} C_{11}) + tan^{-1}(\omega R_{12} C_{21}) \simeq \frac{\pi}{2} + \delta \tag{6.4}$$

The resistance R'_{11} tunes the value of the resistance R_{11} to yield the total gain equal to 1, while the resistance R'_{12} tunes the resistance R_{12} to yield the total phasor lag equal to $\frac{\pi}{2}$. Thus, the total transfer function is given by

$$W(s) = W_1(\hat{\jmath}\omega)\, W_2(\hat{\jmath}\omega) = \hat{\jmath} \exp^{-\frac{\hat{\jmath}\pi}{2}} \tag{6.5}$$

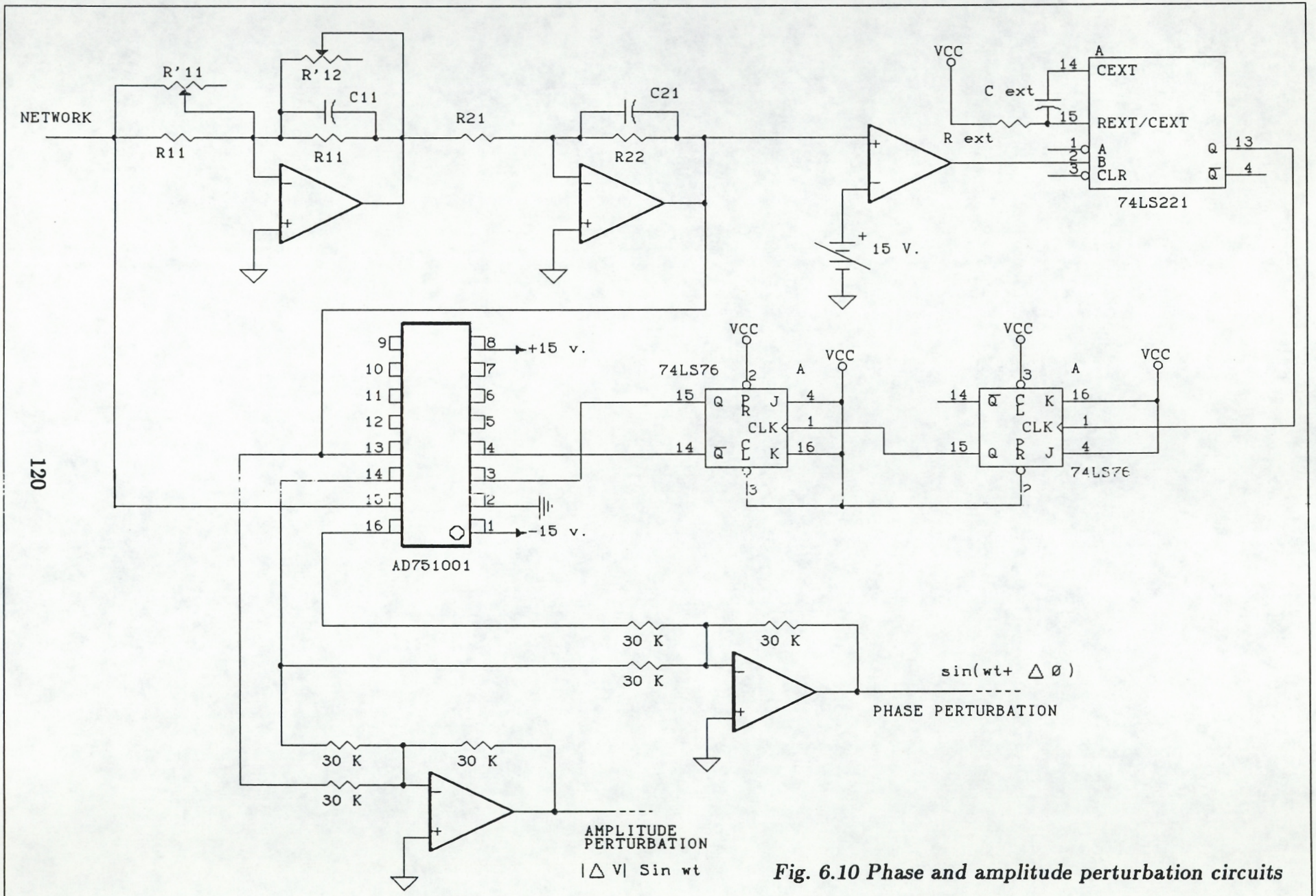


Fig. 6.10 Phase and amplitude perturbation circuits

6.7.1 — Phase Perturbation of the PLL with an Analog Filter

A step phase-perturbation is applied to the phase-locked loop. Such a perturbation is shown in Fig. 6.11 . The bottom trace shows the VCO control voltage.

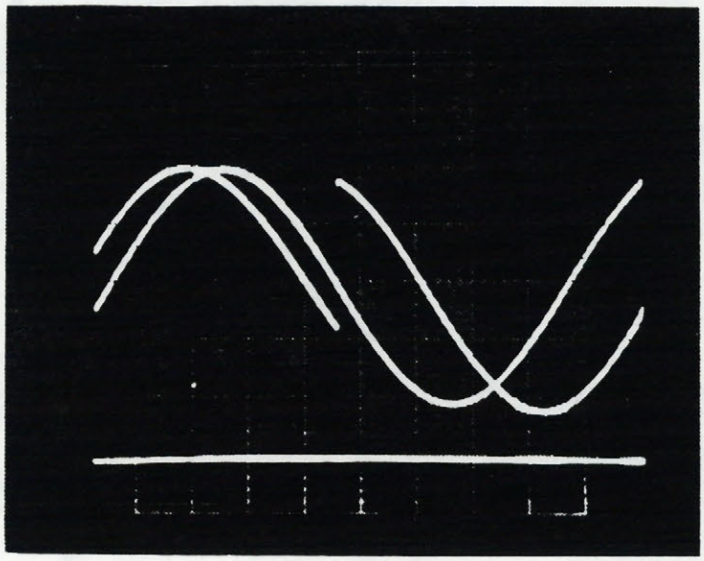


Fig.6.11 Step phase-perturbation / PLL with analog filter

The transient performance of this PLL configuration can be observed in Fig. 6.12 We see that the PLL settles very quickly in about 4 cycles after the disturbance.

A remarkable agreement of these tests with those performed by *PSPICE* simulation has been found.

The waveforms illustrated in figures 6.12 and 6.13 correspond to the PLL output (the top trace) and the network and VCO signals(overlaped traces). These oscillograms show the period of time before, during and after the phase perturbation.

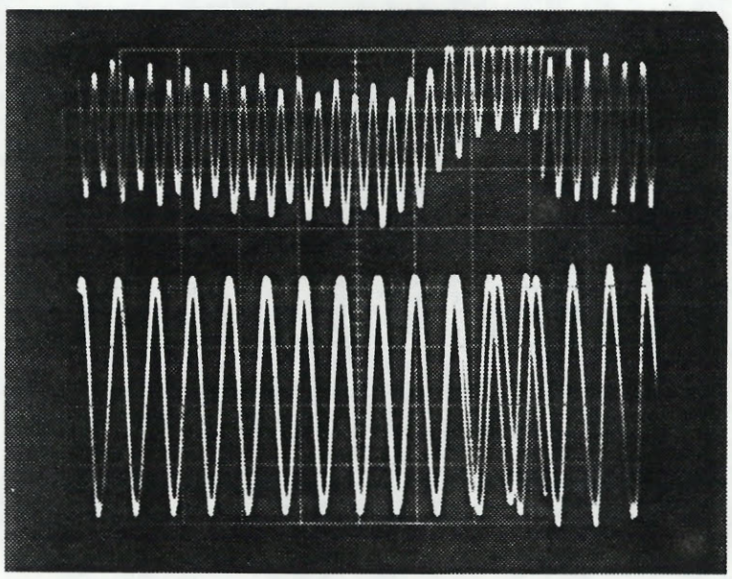


Fig. 6.12 Characteristic PLL waveforms before and after perturbation

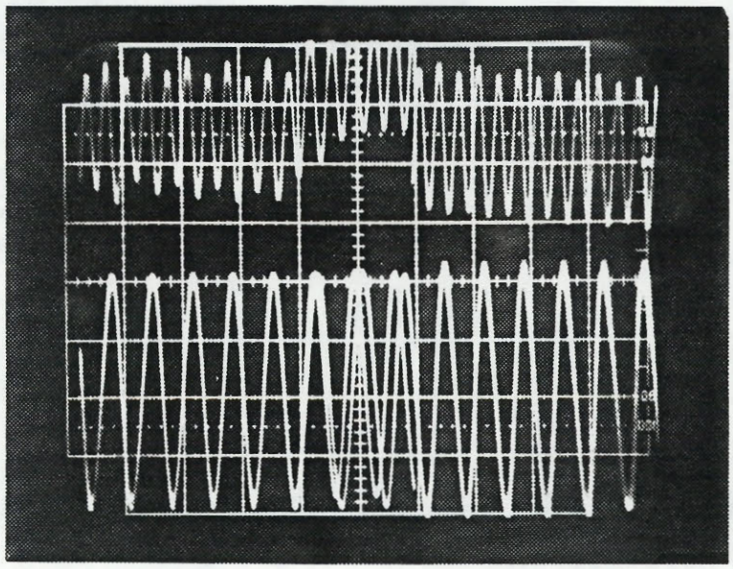


Fig. 6.13 Characteristic PLL waveforms before and after perturbation, another view

6.7.2 — Phase Perturbation of the PLL without Filter

The oscillogram of Fig. 6.14 shows that the PLL settles down in about 6 cycles. In comparison with the previos case, a two cycles longer settling time is due to the smaller gain Kv, for this PI controller. In other words, the larger Kv, the greater the close-loop bandwidth is, and thus the faster the loop response. Therefore to increase the response speed and to reduce the tracking error, the loop gain should be as large as the acceptable overshoot would permit.

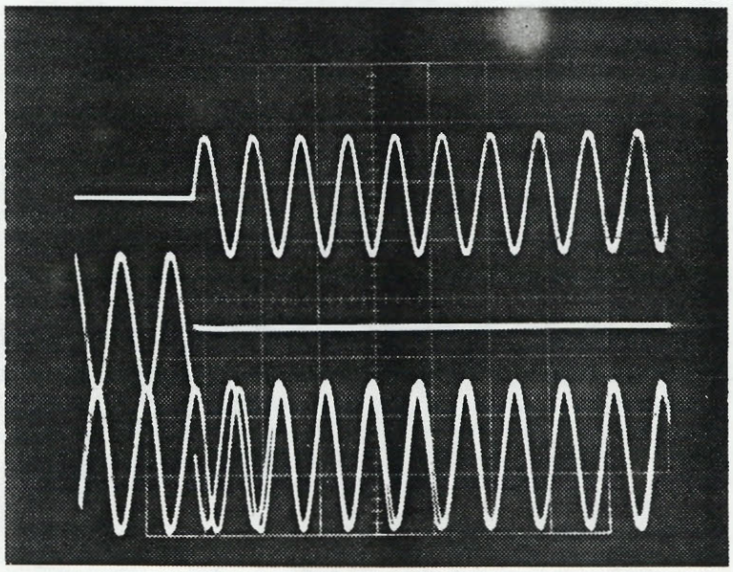


Fig. 6.14 Phase perturbation without filter

The two top traces of Fig. 6.14 show : $cos\omega t\, cos\phi$ and $\sin\omega t\, \sin\phi$, respectifully. The bottom trace shows the perturbated network voltage and VCO output response.

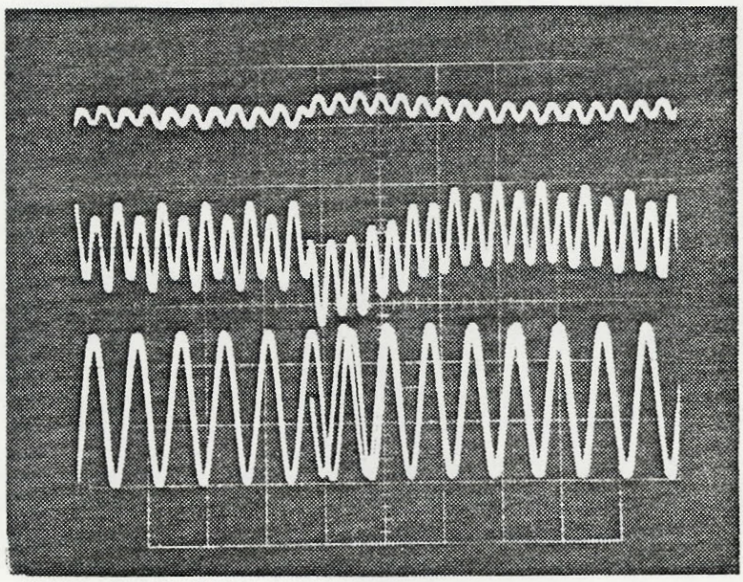


Fig. 6.15 Response waveforms of the PLL without Filter

The oscillogram of Fig. 6.15 (top trace) shows that the VCO control voltage has a second harmonic in addition to its DC component . In the previous case, the analog filter eliminates this second harmonic component. The middle trace shows the PLL multiplier output while the bottom overlaped traces show the voltage signal from the network and the VCO output voltage.

6.8 — Synchronous Filter

The computer simulation of the synchronous (Fourier) filter is represented by a discrete version implemented in the laboratory. The circuit configuration based on the two-interval integration is illustrated in Fig. 6.16 and in Fig 6.17 respectively.

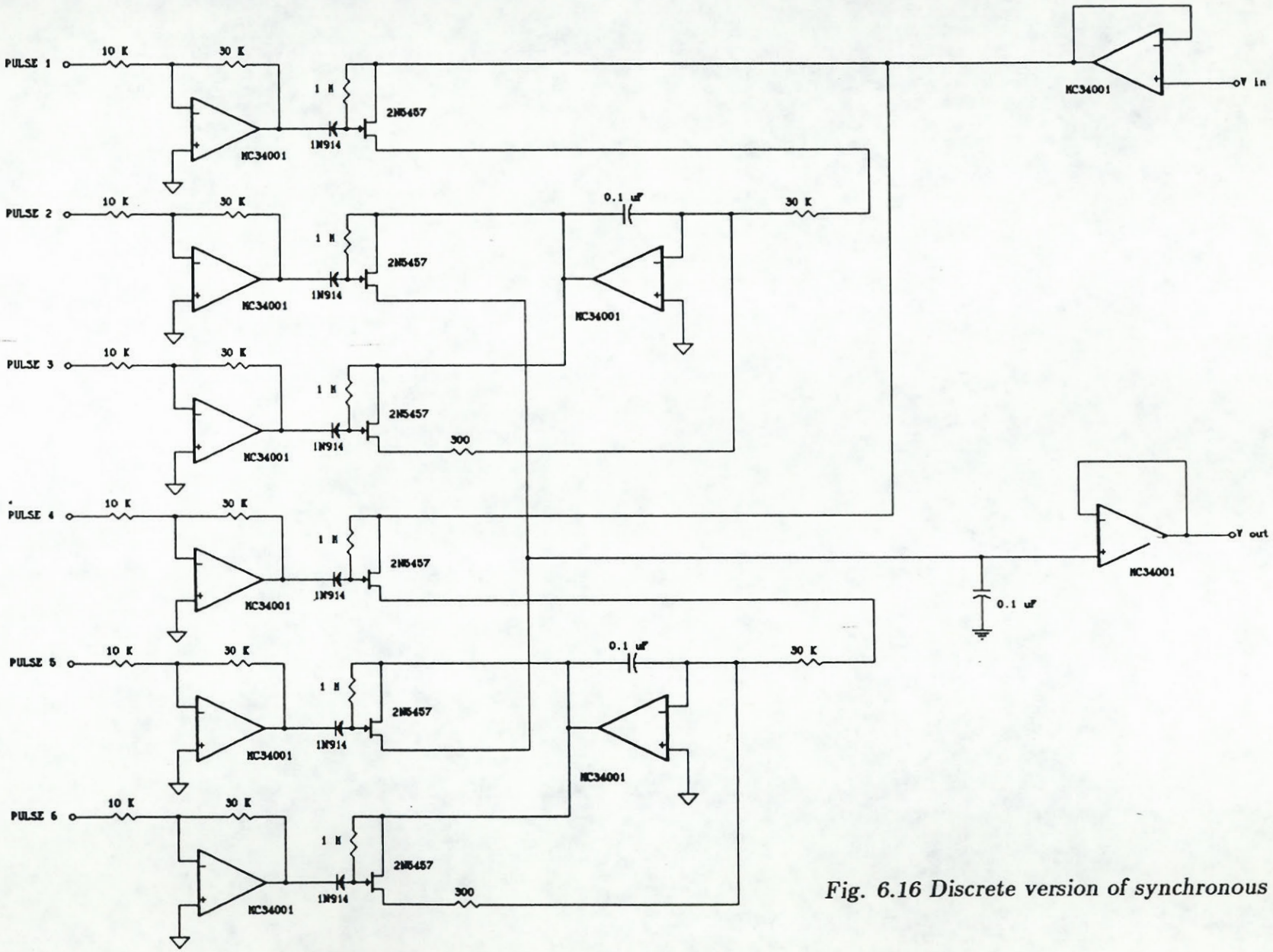


Fig. 6.16 Discrete version of synchronous filter

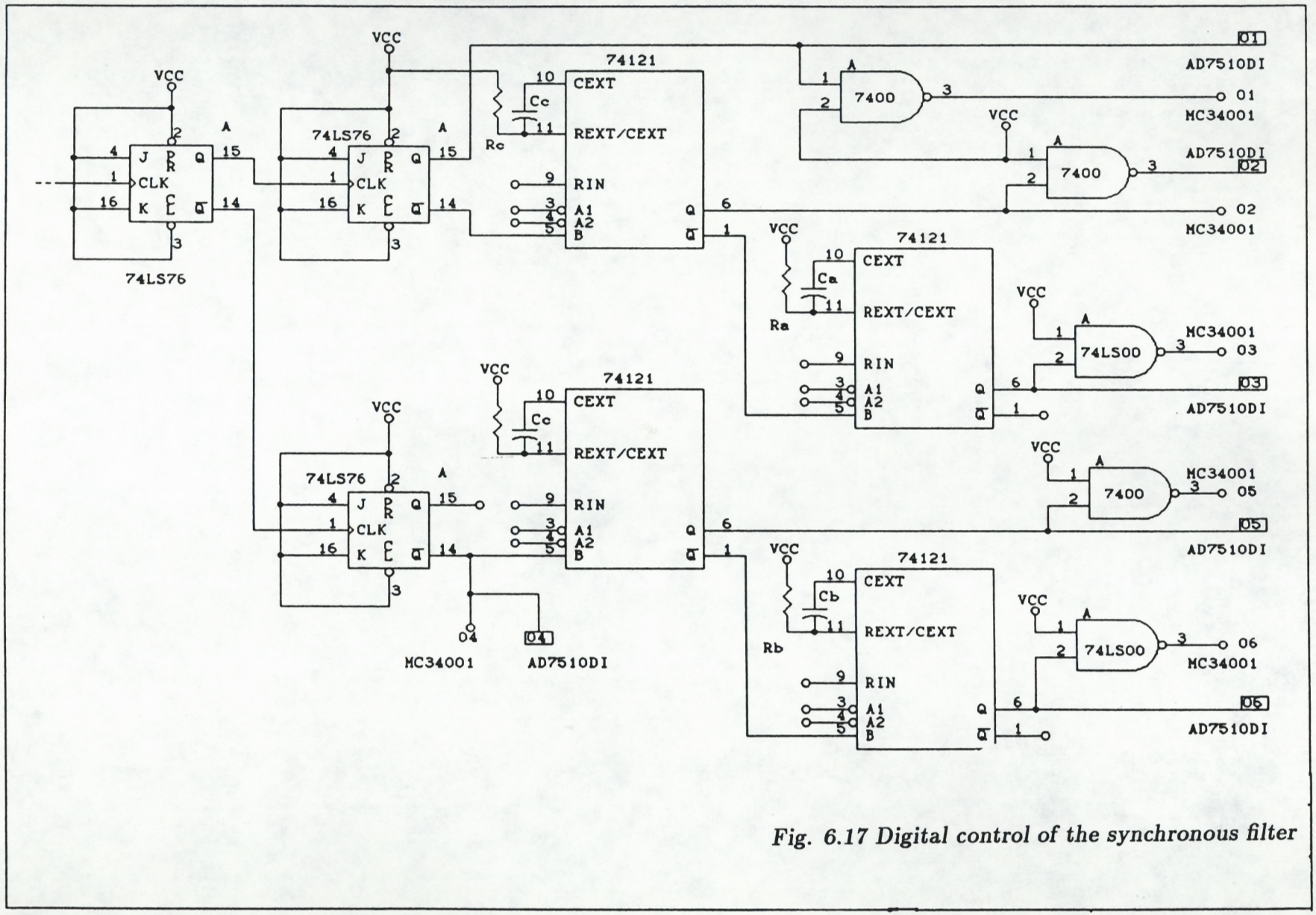


Fig. 6.17 Digital control of the synchronous filter

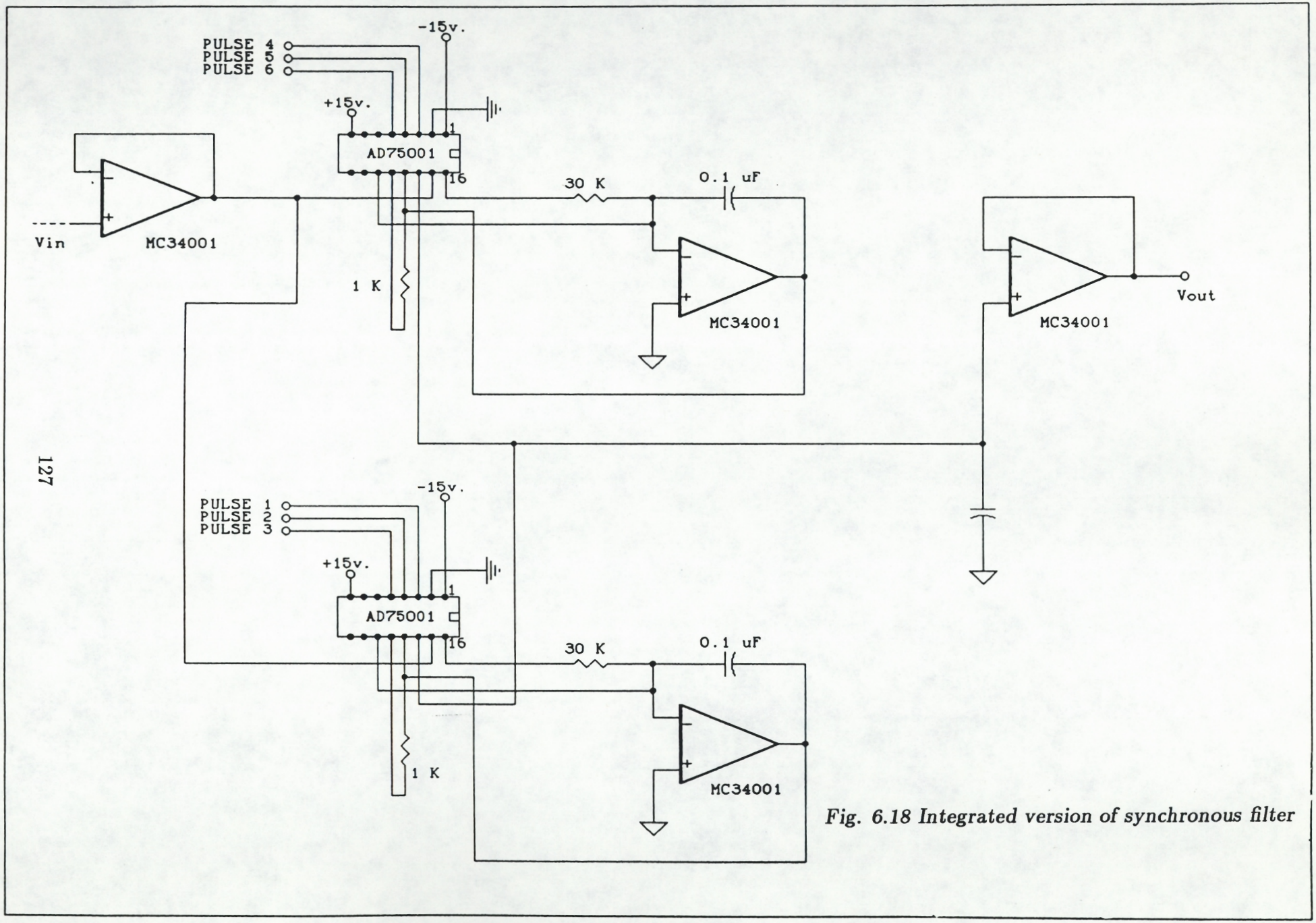


Fig. 6.18 Integrated version of synchronous filter

The discrete version of the filter worked according to our expectation.

The circuit complexity (number of components) increases with the number of integration intervals if implemented in analog technology. However, if digital technology is applied, the filter with a great number of integration intervals (approximating a continous integration within the period) could be realized relatively easily.

The circuit realization based on integrated circuits is shown in Fig. 6.18.

Control pulses 1, 2 and 3 as refered to in Fig. 6.18 are shown in oscillogram of Fig. 6.19. Control pulses 4, 5 and 6 are the same as the first three, except that they are shifted in for 90 electrical degrees as shown in Fig. 6.20. The figure shows the control pulses 1 and 6 as well as the corresponding input signals being switched.

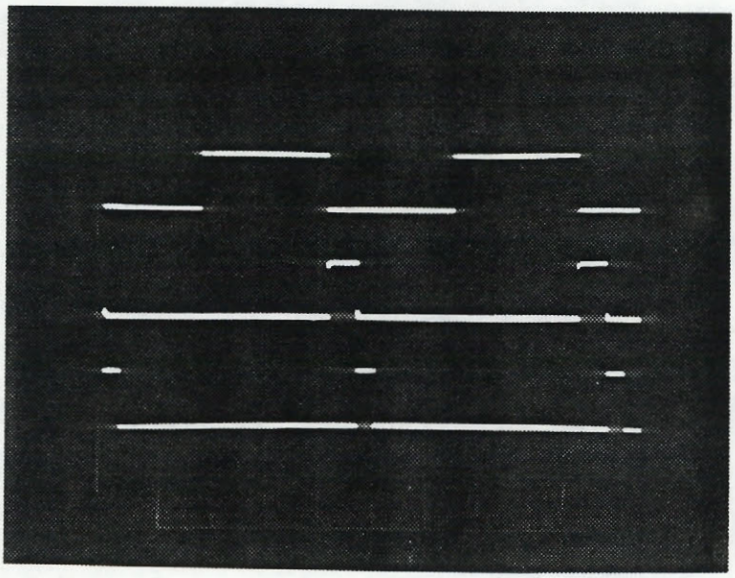


Fig. 6.19 Control pulses 1, 2 ,3 for the two-interval integration filter

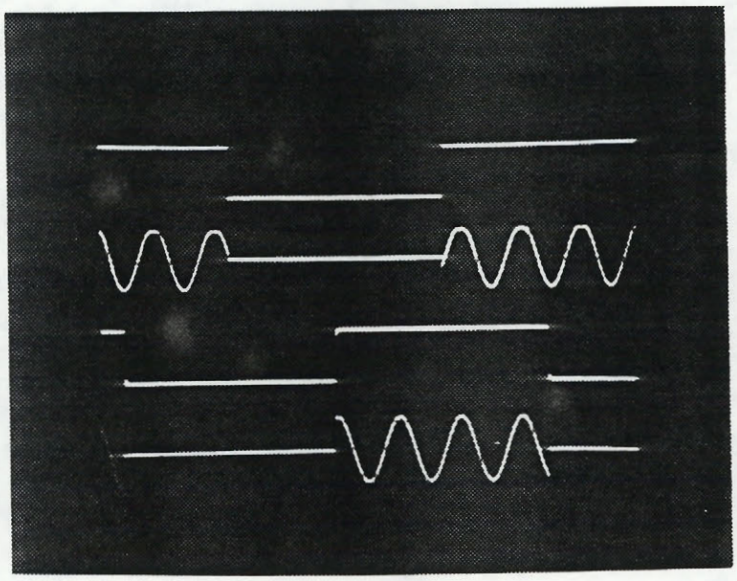


Fig. 6.20 Control pulses 1 and 4 with the corresponding input signals being switched

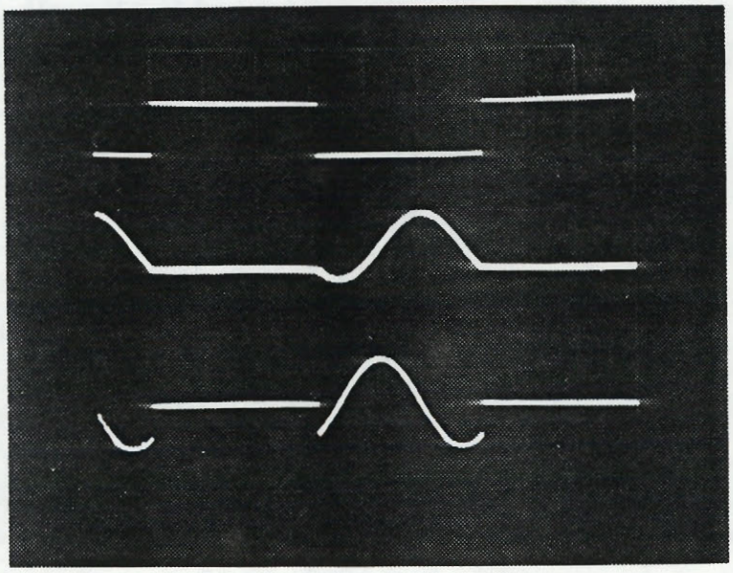


Fig. 6.21 Integrator input, output and control signals

The synchronous filter operation is illustrated by the oscillogram given in Fig. 6.21, where the input and output control voltage of one of the two integrators is given. The middle trace shows the output of the controlled integrator to be held by the hold circuit when the switch 2 and 5 are on.

6.8.1 — Phase-Perturbation of the PLL with Synchronous Filter

The parameters of the synchronous filter and the PI controller are chosen as those applied in simulation.

Fig. 6.22 gives the PLL response waveforms to a phase-step perturbation; the perturbated network voltage, the VCO output voltage as well as the synchronous filter output.

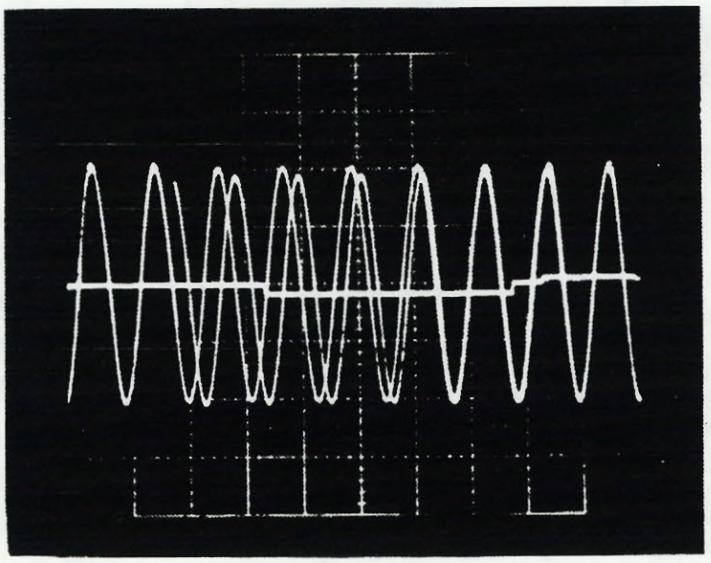


Fig. 6.22 PLL response waveforms to a step-phase perturbation

The settling of the VCO output is reached in about 7 cycles, four cycles faster than found by simulations and 2.5 slower than found in the PLL with analog filter.

Though the filter performs very well, for removing the harmonic frequencies, it does not remove other frequencies. Its time delay can be too long where an improved response is necessary in applications to fast reacting static compensator.

6.9 — Amplitude Perturbation of the PLL with an Analog Filter

The circuit of Fig. 6.10 was also implemented to perform the amplitude perturbation test. Controller and filter parameters are the same as in simulation.

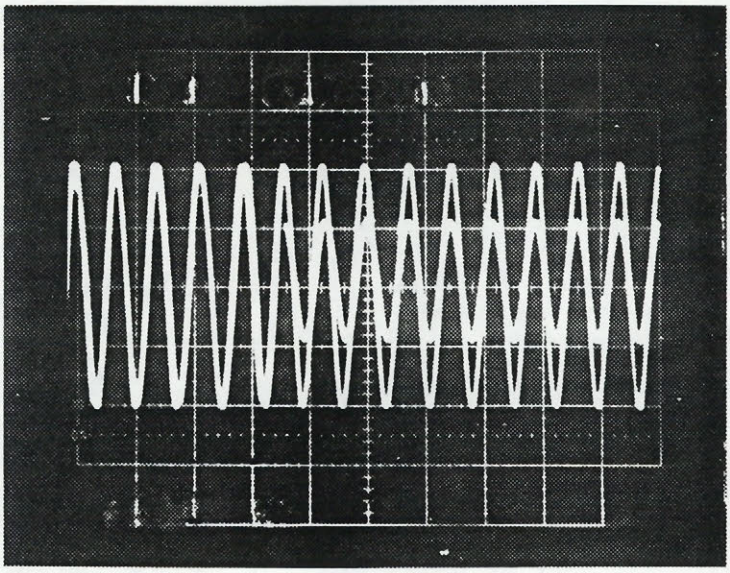


Fig. 6.23 Amplitude perturbation-analog filter

In response to a step amplitude perturbation, the VCO outputs settles in about 3 cycles (see Fig. 6.23) as compared to 3.5 cycles found by simulation. The difference is due to approximations assumed in simulation.

6.10 — PLL Amplitude Perturbation with Second Harmonic Excitation

6.10.1 — PLL with an Analog Filter

The second harmonic amplitude used in this test is about 50% of the fundamental voltage amplitude. Such a value was chosen to demonstrate more clearly the effect of this component on the phase-locked loop. The input signal is described by the following expression

$$v_i(t) = \begin{cases} V \sin(\omega t + \phi) + \frac{V}{2} \sin 2\omega t & \text{at } t < \tau \\ \frac{V}{2} \sin(\omega t + \phi) + \frac{V}{2} \sin 2\omega t & \text{at } t \geq \tau \end{cases} \tag{6.6}$$

before and after the perturbation respectively. The PLL responses are illustrated in Fig. 6.24 . The upper traces give, the fundamental and second harmonic components while the bottom traces give the VCO and network signals.

The settling time remains the same as in the previous case but a phase-shift is present between these two signals. The greater the second harmonic amplitude, the greater the phase shift.

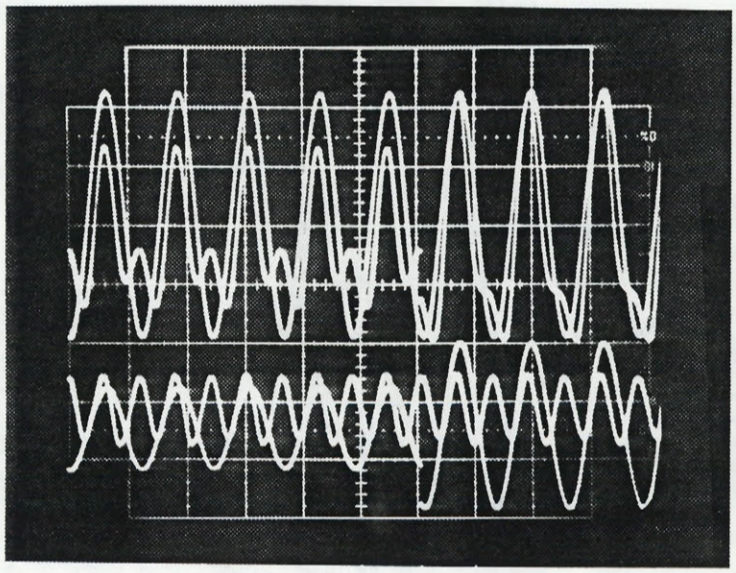


Fig. 6.24 Amplitude perturbation with the second harmonic excitation of a PLL with analog filter: Characteristic waveforms

6.10.2 — PLL without Filter

In this test, a PI controller has been applied without the filter. The results obtained were similar to those found in the previous case. However, the influence of the second harmonic is greater than before. This effect can be seen in Fig. 6.25.

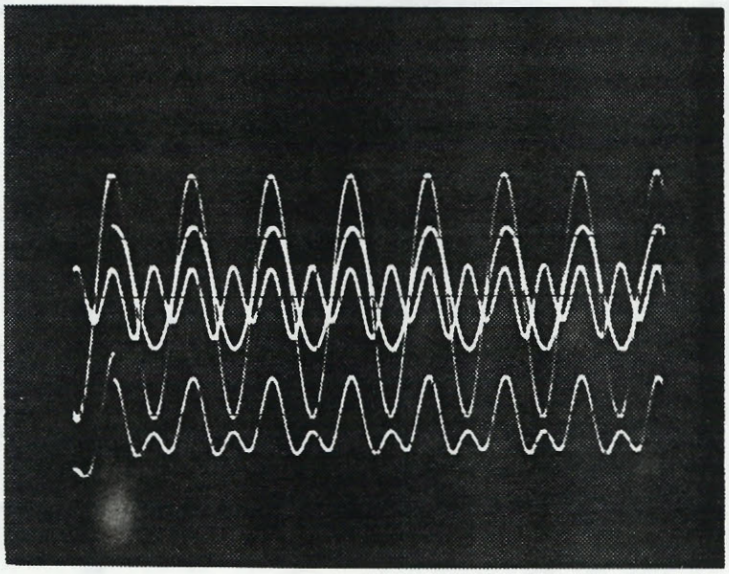


Fig. 6.25 Amplitude perturbation with the second harmonic excitation of a PLL without filter: Characteristic waveforms

6.10.3 — PLL with Synchronous Filter

In Fig. 6.26 we can see that the settling is reached in about 10 cycles as obtained by simulation.

The figure gives the second harmonic excitation (top trace), the perturbated input (second trace) and the VCO output (third trace).

The synchronous filter, under an amplitude perturbation and second harmonic excitation behaves very well since the second harmonic is completely filtered. The fundamental network component and VCO output signal are given in Fig. 6.27, the upper traces. The lower traces give the distorted network voltage and the VCO control voltage.

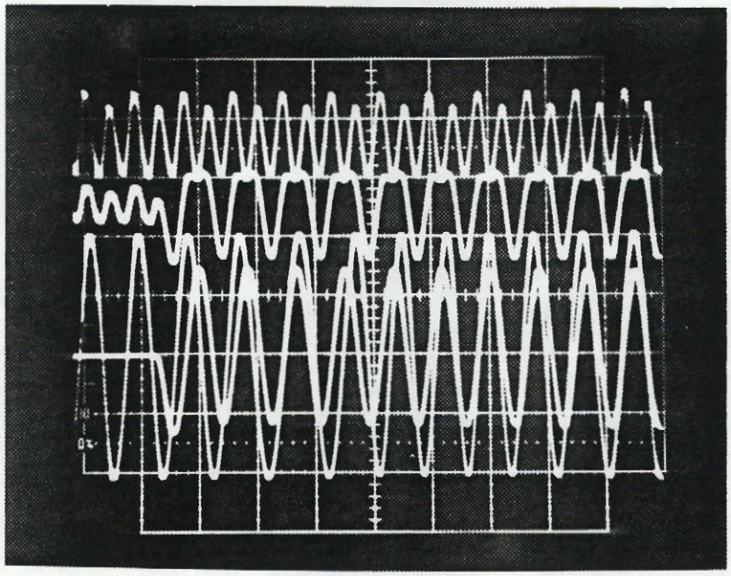


Fig. 6.26 Amplitude perturbation with the second harmonic excitation of a PLL with synchronous filter: Characteristic waveforms

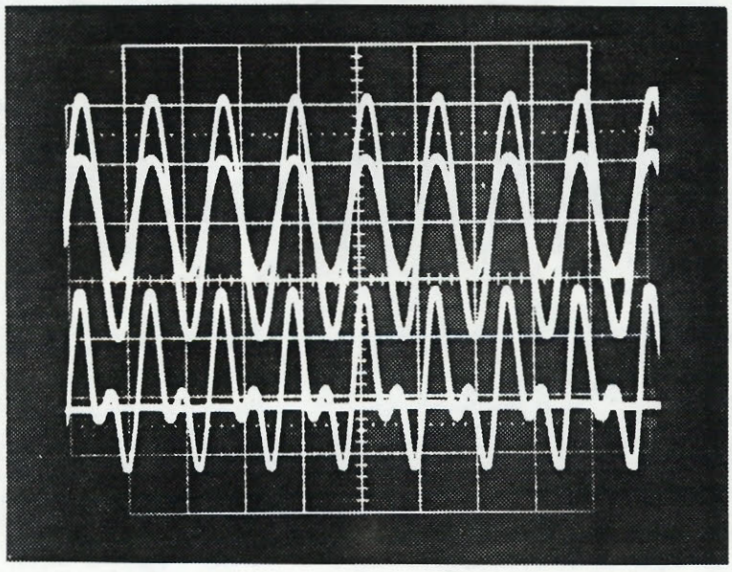


Fig. 6.27 PLL with synchronous filter: Steady-state operation in presence of the second harmonic excitation

6.11 — Summary

In this chapter we have performed tests with different PLL configurations as realized in simulation. The comparative analyses of the step responses of our *PSPICE*models and the PLL electronic circuits give a full evidence for the *PSPICE*model validation.

7.5 — PLL Linear Model for Stability Studies

Based on the previous analysis, we could build the linearized PLL model in the s - domain as given in the following figure

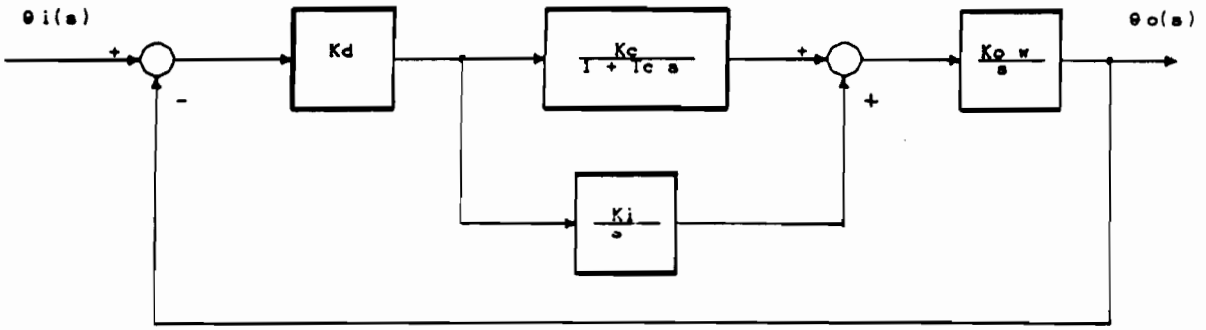


Fig.7.6 Block diagram of the linearized PLL

$$W(s) = \frac{K_d \frac{K_i + sK_f}{s(1+\tau_f s)} \frac{K_o \omega}{s}}{1 + K_d \frac{K_i + sK_f}{s(1+\tau_f s)} \frac{K_o \omega}{s}} \tag{7.32}$$

or

$$W(s) = \frac{K_d K_f K_o \omega s + K_d K_o K_i \omega}{\tau_f s^3 + s^2 + K_d K_f K_o \omega s + K_d K_i K_o \omega} \tag{7.33}$$

where $\tau_f = T_c$ and $K_f = K_c + K_i T_c$

7.6 — PLL Transient Response to Step Phase-Perturbation

In general, a control system driven by an input signal can be described by the following differential equation

$$\frac{d^n\phi_0}{dt^n} + a_1\frac{d^{n-1}\phi_0}{dt^{n-1}} + a_2\frac{d^{n-2}\phi_0}{dt^{n-2}} + \cdots + a_{n-1}\frac{d\phi_0}{dt} + a_n\phi_0 = b_0\frac{d^n\phi_i}{dt^n} + b_1\frac{d^{n-1}\phi_i}{dt^{n-1}} + \cdots + b_{n-1}\frac{d\phi_i}{dt} + b_n\phi_i \tag{7.34}$$

In our case, when W(s) is given by the equation (7.33), we obtain

$$\frac{d^3\phi_0}{dt^3} + a_1\frac{d^2\phi_0}{dt^2} + a_2\frac{d\phi_0}{dt} + a_3\phi_0 = b_2\frac{d\phi_i}{dt} + b_3\phi_i \tag{7.35}$$

where

$$\begin{aligned} b_0 &= 0 \\ b_1 &= 0 \\ b_2 &= \frac{K_d K_0 K_c \omega}{\tau_f} \\ b_3 &= \frac{K_d K_0 K_i}{\tau_f \omega}\,\omega \\ a_0 &= 1 \\ a_1 &= \frac{1}{\tau_f} \\ a_2 &= \frac{K_d K_f K_0 \omega}{\tau_f} \\ a_3 &= \frac{K_d K_i K_0 \omega}{\tau_f} \end{aligned} \tag{7.36}$$

Introducing new state and input variables

$$\begin{aligned} x_1 &= \phi_0 \\ x_2 &= \frac{dx_1}{dt} = \frac{d\phi_0}{dt} \\ x_3 &= \frac{dx_2}{dt} - b_2 u_1 \end{aligned} \tag{7.37}$$

The equation (7.35) transforms into the following set of differential equations of the first order

$$\frac{dx_1}{dt} = x_2 \tag{7.39}$$

$$\frac{dx_2}{dt} = x_3 + b_2 u_1 \tag{7.40}$$

$$\frac{dx_3}{dt} = -a_3 x_1 - a_2 x_2 - a_1 x_3 + (b_3 - a_1 b_2) u_1 \tag{7.41}$$

The matrix form of this set of equations is as follows

$$\frac{d}{dt}\begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ -a_3 & -a_2 & -a_1 \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix} + \begin{pmatrix} 0 \\ b_2 \\ b_3 - a_1 b_2 \end{pmatrix}(u_1) \tag{7.42}$$

The solution of this equation gives the PLL response to the input phase perturbation. The response of the PLL circuit simulated by *PSPICE* (as implemented by electronic components) to a step phase perturbation was recorded using the pase discrimination circuit as shown in Fig. 7.8.

The phase discrimination circuit gives the phase diference between the sinusoidal input signal and the PLL sinusoidal output.

Referring to Fig (7.7), the following signals are formed

$$V(80) = |V|(\sin\omega t\cos\phi + \cos\omega t\sin\phi) = |V|[\sin(\omega t + \phi)] \tag{7.43}$$

$$V(90) = |V|(\cos\omega t\cos\phi - \sin\omega t\sin\phi) = |V|[\cos(\omega t + \phi) \tag{7.44}$$

$$V(91) = |V|[\cos(\omega t + \phi)\cos(\omega t + \phi + \theta)] \tag{7.45}$$

$$V(98) = |V|[\sin(\omega t + \phi)\sin(\omega t + \phi + \theta)] \tag{7.46}$$

Hence

$$V(92) = V(91) + V(98) \tag{7.47}$$

$$V(92) = |V|\{\cos\alpha[\cos\alpha\cos\phi_0 - \sin\alpha\sin\phi_0] + \sin\alpha[\sin\alpha\cos\phi_0 + \cos\alpha\sin\phi_0\} \tag{7.48}$$

$$V(92) = |V|\cos(\phi_i - \phi_0) \tag{7.49}$$

where

$$\alpha = \omega t + \phi_i \tag{7.50}$$

Similarly

$$V(94) = |V|[\sin(\omega t + \phi_i)\cos\omega t + \phi_0)] \tag{7.51}$$

$$V(95) = -|V|[\cos(\omega t + \phi_i)\sin(\omega t + \phi_i + \phi_0)] \tag{7.52}$$

Hence

$$V(93) = V(94) + V(95) \tag{7.53}$$

$$V(93) = |V|\{\sin\alpha[\cos\alpha\cos\phi_i - \sin\alpha\cos\phi_i] - [\sin\alpha\cos\phi_i + \cos\alpha\sin\phi_i]\cos\alpha\} \tag{7.54}$$

$$V(93) = |V|\sin(\phi_i - \phi_0) \tag{7.55}$$

Further on

$$V(201) = V(82) + V(92)$$

$$V(201) = -|V|\sin\phi_i\cos(\phi_i - \phi_0) \tag{7.56}$$

$$V(202) = V(78)V(93) = -|V|\cos\phi_i\sin(\phi_0 - \phi_i) \tag{7.57}$$

Adding these two signals

$$V(205) = V(201) + V(202) = |V|\sin\phi_0 \tag{7.58}$$

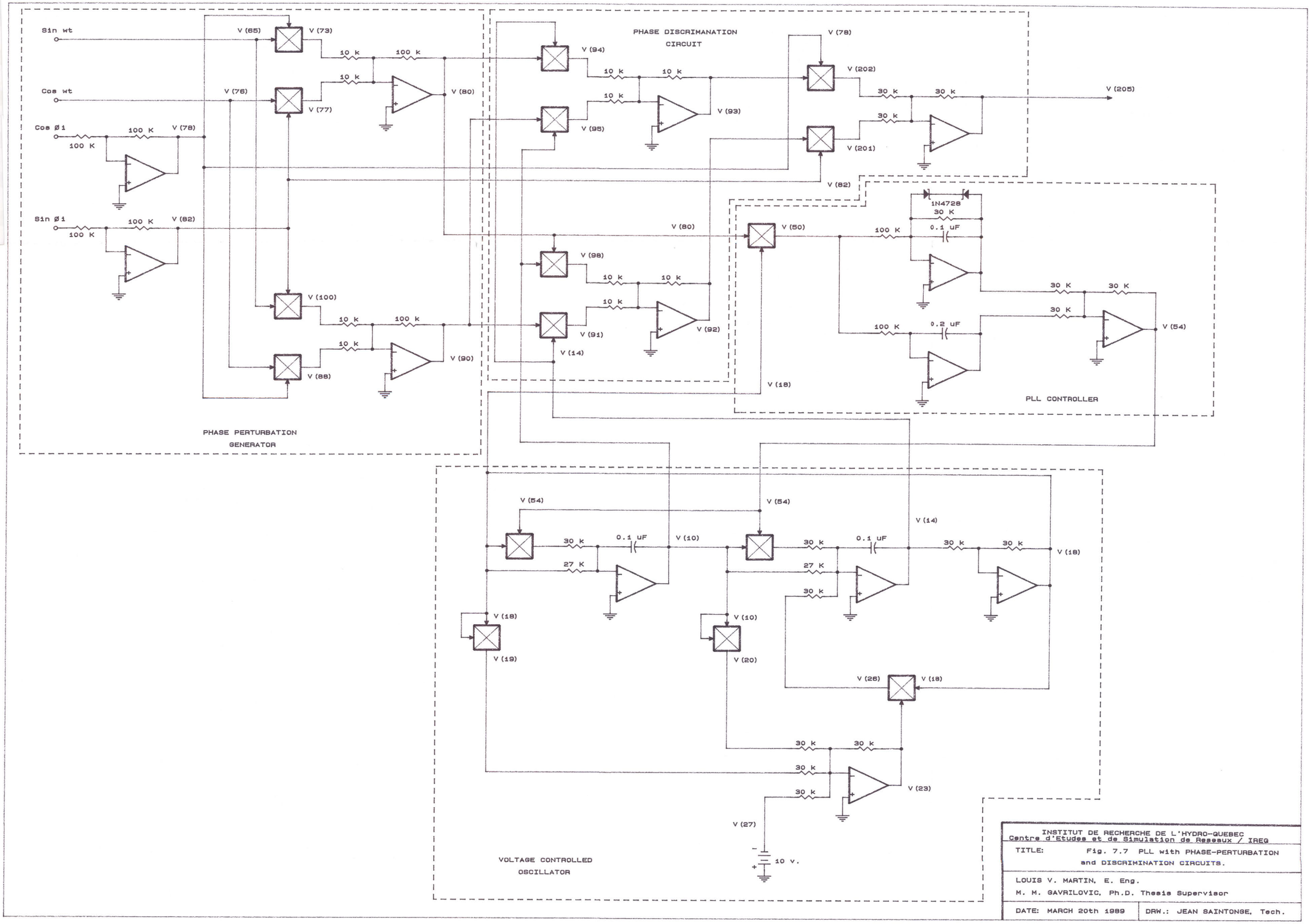
For a small angle, we can approximate

$$\sin\phi_0 = \phi_0 \tag{7.59}$$

Therefore

$$V(205) = |V|\phi_0 \tag{7.60}$$

This response signal to a step phase perturbation is displayed in Fig. 7.8.



INSTITUT DE RECHERCHE DE L'HYDRO-QUEBEC
Centre d'Etudes et de Simulation de Reseaux / IREQ

TITLE: Fig. 7.7 PLL with PHASE-PERTURBATION and DISCRIMINATION CIRCUITS.

LOUIS V. MARTIN, E. Eng.
M. M. GAVRILOVIC, Ph.D. Thesis Supervisor

DATE: MARCH 20th 1989 | DRW.: JEAN SAINTONGE, Tech.

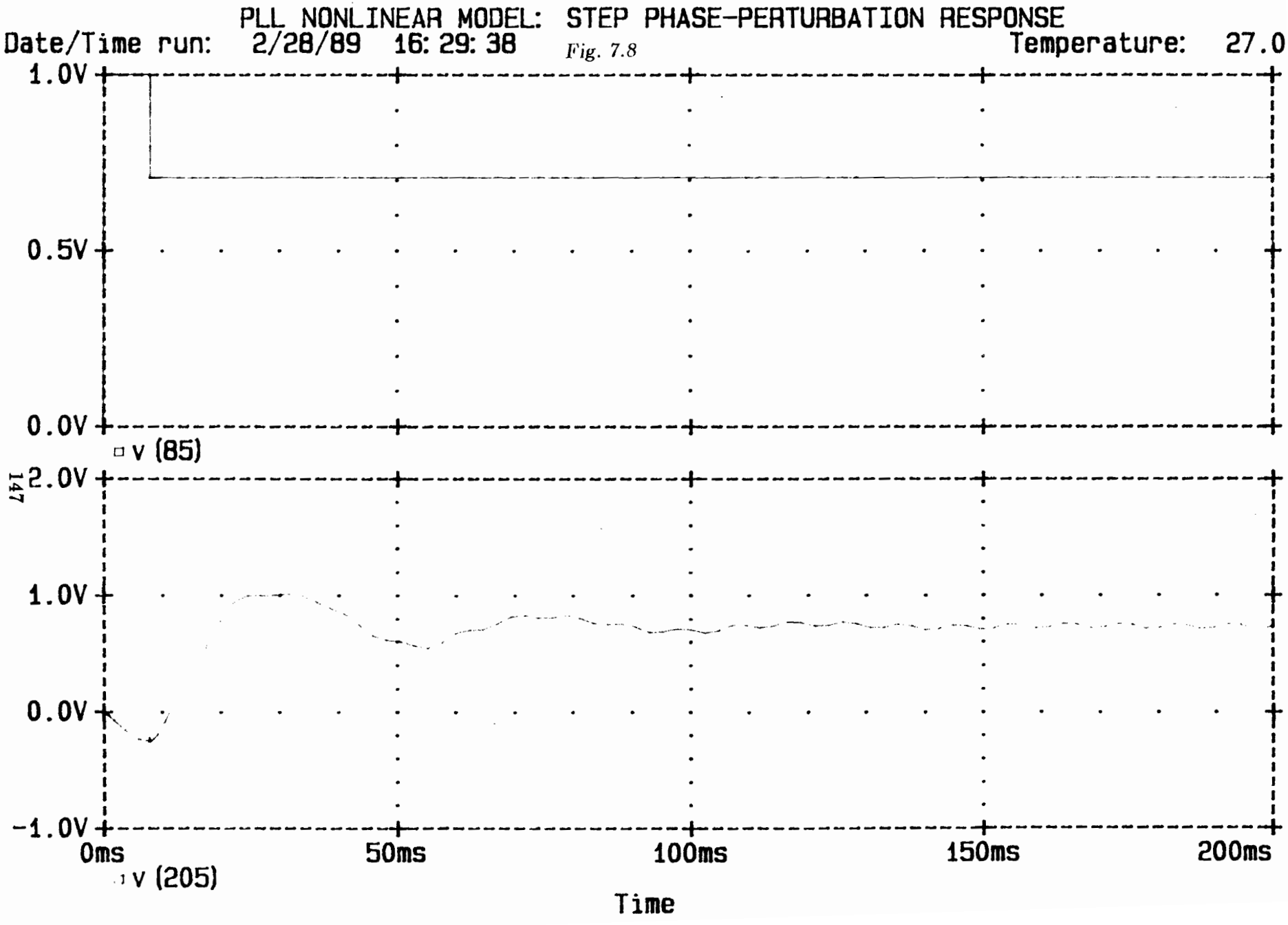

PLL NONLINEAR MODEL: STEP PHASE-PERTURBATION RESPONSE
Date/Time run: 2/28/89 16:29:38
Temperature: 27.0
1.0V
0.5V
0.0V
V (85)
2.0V
1.0V
0.0V
-1.0V
V (205)
0ms
50ms
100ms
150ms
200ms
Time

Fig. 7.8

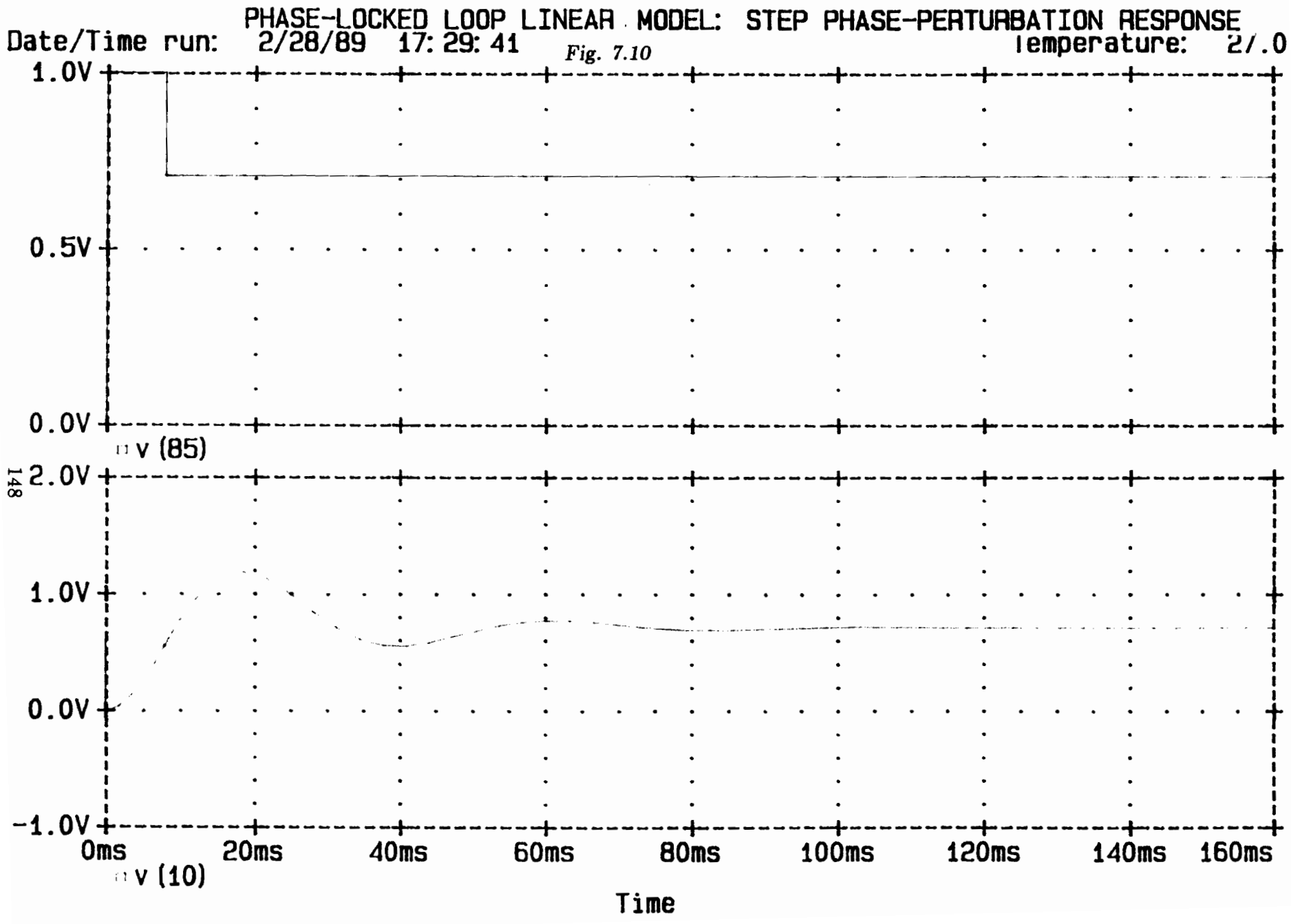

PHASE-LOCKED LOOP LINEAR MODEL: STEP PHASE-PERTURBATION RESPONSE
Date/Time run: 2/28/89 17:29:41
Temperature: 27.0
1.0V
0.5V
0.0V
v (85)
2.0V
1.0V
0.0V
-1.0V
0ms
20ms
40ms
60ms
80ms
100ms
120ms
140ms
160ms
v (10)
Time

Fig. 7.10

7.8 — Summary

The PLL linearized model for stability studies was derived on the basis of an analysis of its components. Thus, the phase detector is represented by an adder, the regulator by a low-pass analog or synchronous (Fourier) filter with a PI controller and the voltage controller oscillator by an integrator. In this model, the $\sin\phi$ function is approximated by ϕ (the first term of the Taylor series).

In order to validate the PLL linearization, the step phase-perturbation was also applied to the nonlinear model and its response obtained by means of a discrimination circuit which gives the phase difference between the sinusoidal input signal and the PLL sinusoiadl output.

By comparison, step phase-perturbation response of the PLL linear model is similar to the one obtained for the nonlinear model which demonstrates the validity of the PLL model for transient stability studies.

CHAPTER 8

CONCLUSION

Phase-locked loop are very often applied to as synchronization circuits in controllers of static var compensators and (AC-DC converters). Although the phase-locked loop affects the dynamic performance of such controllers, they are seldom included in the models.

The objective of this thesis was to develop and validate the phase-locked loop models suitable for implementation in transient stability programs of power systems.

First, the static var compensators, their configuartions, operation principles, controllers and synchronization circuits were considered in order to deduce the synchronization requirements for the phase-locked loop circuits.

In order to establish the basis for the development of PLL models, the realization of the voltage controlled oscillator (VCO) and two types of filters were considered in details as they are essential PLL components.

In order to determine its dynamic performance, the phase-locked loop has been simulated in details by means of *PSPICE* simulation program. Three PLL configurations were studied: PLL with the PI controller, PLL with the PI controller including the first order filter and the PLL with the PI controller including the synchronous (Fourier) filter. Their dynamic responses were evaluated for step perturbations of the following signals: the phase of the input voltage and the amplitude of the input voltage. The PLL harmonic performance was evaluated using the input voltage including the steady-state second harmonic component. In addition, the combination of such perturbations signals were also applied. Fourier analysis was used in order to asses the harmonic generation of the PLL itself as well as when excited by the second harmonic component at its input.

In order to validate such a detailed simulation, the PLL circuits were realized in electronic components. The step perturbation signals were applied to these circuits as done in previous simulation.

The close agreement of the responses of the actual phase-locked loop with those obtained by detailed simulation fully validated the previous *PSPICE* simulation. Minor differences found were due to simplification of some PLL component models.

The PLL model for transient stability studies were analitically developed. The modelling of the voltage controlled oscillator and the phase detector required special attention since the sinusoidal system voltages and currents are represented in complex numbers. Two PLL models were developed: one-linearized for small signal, the other-nonlinear for large signal analysis. The nonlinear PLL reduced model is suitable for transient stability studies based on numerical integration, while the linear PLL reduced model is suitable for studies based on eigenvalue analysis.

The dynamics of the PLL reduced models was evaluated by *PSPICE* simulation. The step response to the phase perturbation of these PLL models were obtained and compared to those obtained by previous detailed modelling. The close agreement of the two step responses demonstrates fully the validity of the developed PLL reduced models. *The development of such a models represents an original contribution to phase-locked loop modelling in transient stability studies of power systems.*

Based on this development, one could easily derive similar models for other types of phase-locked loop used for synchronization in static var controllers (and AC-DC converters).

The development procedure of this thesis demonstrates that the *PSPICE* simulation program could be used for development of reduced models of other analog circuits and control systems to be used in transient stability programs of power systems.

APPENDIX A

DATA SHEETS OF ELECTRONIC COMPONENTS

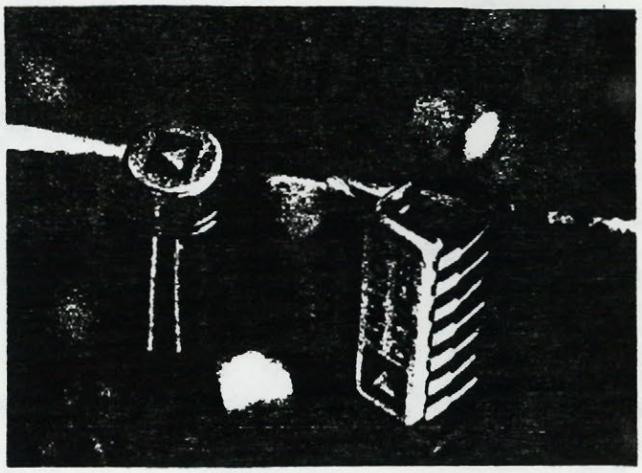
ANALOG DEVICES

Internally Trimmed Integrated Circuit Multiplier

AD532

FEATURES
- Pretrimmed To ±1.0% (AD532K)
- No External Components Required
- Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
- Diff Inputs For $(X_1-X_2)(Y_1-Y_2)/10$ Transfer Function
- Monolithic Construction, Low Cost

APPLICATIONS
- Multiplication, Division, Squaring, Square Rooting
- Algebraic Computation
- Power Measurements
- Instrumentation Applications



PRODUCT DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1-X_2)(Y_1-Y_2)/10$, divides in two quadrants with a $10Z/(X_1-X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10Z}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as $XY/10$, $(X^2-Y^2)/10$, $\pm X^2/10$, and $10Z/(X_1-X_2)$ are easily attained, and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer-generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at +25°C, and are rated for operation from 0 to +70°C. The AD532S has a maximum multiplying error of ±1% of full scale at +25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of -55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP packages.

ADVANTAGES OF ON-THE-CHIP TRIMMING OF THE MONOLITHIC AD532

1. True ratiometric trim for improved power supply rejection.
2. Reduced power requirements since no networks across supplies are required.
3. More reliable since standard monolithic assembly techniques can be used rather than more complex hybrid approaches.
4. High impedance X and Y inputs with negligible circuit loading.
5. Differential X and Y inputs for noise rejection and additional computational flexibility.

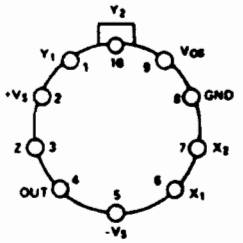
SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, V_{OS} grounded, unless otherwise specified)

PARAMETER	CONDITIONS	AD532J	AD532K	AD532S
ABSOLUTE MAX RATINGS				
Supply Voltage		±18V	•	±22V
Internal Power Dissipation		500mW	•	•
Input Voltage[1]				
X, Y, V_{OS}, Z		$\pm V_S$	•	•
Rated Operating Temp Range		0 to +70°C	•	-55°C to +125°C
Storage Temp Range		-65°C to +150°C	•	•
Lead Temperature	60 Sec Soldering	+300°C	•	•
Output Short Circuit	To Ground	Indefinite	•	•
MULTIPLIER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)(Y_1-Y_2)/10$	•	•
Total Error (% F.S.)	V_X = 0/±10V, V_Y = 0/±10V	±2.0% max [±1.5% typ]	±1.0% max [±0.7% typ]	±1.0% max [±0.5% typ]
	T_A = min to max	±2.5%	±1.5%	±4.0% max
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.04%/°C max [±0.01%/°C typ]
Nonlinearity				
X Input	V_X = 20V(p-p), V_Y = ±10V	±0.8%	±0.5%	••
Y Input	V_Y = 20V(p-p), V_X = ±10V	±0.3%	±0.2%	••
Feedthrough				
X Input	V_X = 20V(p-p), V_Y = 0, f = 50Hz	200mV(p-p) max [50mV(p-p) typ]	100mV(p-p) max [30mV(p-p) typ]	••
Y Input	V_Y = 20V(p-p), V_X = 0, f = 50Hz	150mV(p-p) max [30mV(p-p) typ]	80mV(p-p) max [25mV(p-p) typ]	••
vs. Temperature	T_A = min to max	2.0mV(p-p)/°C	1.0mV(p-p)/°C	••
DIVIDER SPECIFICATIONS				
Transfer Function		$10Z/(X_1-X_2)$	•	•
Total Error[2]	V_X = −10V, V_Z = ±10V	±2%	±1%	••
	V_X = −1V, V_Z = ±10V	±4%	±3%	••
SQUARER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)^2/10$	•	•
Total Error		±0.8%	±0.4%	••
SQUARE ROOTER SPECIFICATIONS				
Transfer Function		$-\sqrt{10Z}$	•	•
Total Error[2]	V_Z = 0/+10V	±1.5%	±1.0%	••
INPUT SPECIFICATIONS				
Input Resistance				
X, Y Inputs		10MΩ	•	•
Z Input		36kΩ	•	•
Input Bias Current				
X, Y Inputs		3μA	4μA max [1.5μA typ]	••
Z Input		±10μA	±15μA max [±5μA typ]	••
X, Y Inputs	T_A = min to max	10μA	8μA	••
Z Input	T_A = min to max	±30μA	±25μA	••
Input Offset Current				
X, Y Inputs		±0.3μA	±0.1μA	••
Input Voltage Diff/CM	T_A = min to max			
X, Y, Z Inputs	For Rated Accuracy	±10V	•	•
CMRR (X or Y Inputs)	X or Y = ±10V	40dB min	50dB min	••
DYNAMIC SPECIFICATIONS				
Small Signal, Unity Gain		1.0MHz	•	•
Full Power Bandwidth		750kHz	•	•
Slew Rate		45V/μs	•	•
Small Signal Amplitude Error		1% at 75kHz	•	•
Small Signal 1% Vector Error	0.5° phase shift	5kHz	•	•
Settling Time	±10V step	1μs to 2%	•	•
Overload Recovery		2μs to 2%	•	•
OUTPUT AMPLIFIER SPECIFICATIONS				
Output Impedance	Closed Loop	1Ω	•	•
Output Voltage Swing	T_A = min to max, $R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min [±13V typ]	•	•
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	•	•
	f = 5Hz to 5MHz	3.0mV(rms)	•	•
Output Offset Voltage				
Initial Offset	Trimmable To Zero	±40mV	±30mV max	••
vs. Temperature	T_A = min to max	0.7mV/°C	•	2.0mV/°C max
POWER SUPPLY SPECIFICATIONS				
Supply Voltage	Rated Performance	±15V	•	•
	Operating	±10V to ±18V	•	±10V to ±22V
Supply Current	Quiescent	±6mA max [±4mA typ]	•	•
Power Supply Variation				
Multiplier Accuracy		±0.05%/%	•	•
Output Offset		±2.5mV/%	•	•
Scale Factor		−0.03%/%	•	•
Feedthrough		±0.25mV/%	•	•

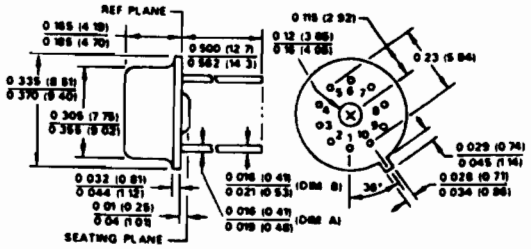
PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).

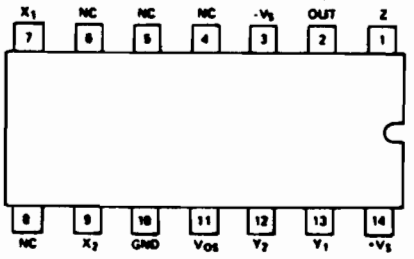
AD532H



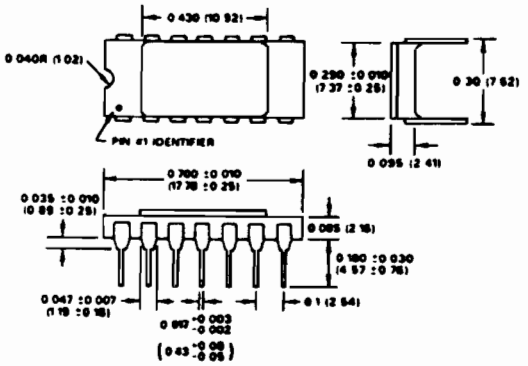
TO-100



AD532D



TO-116



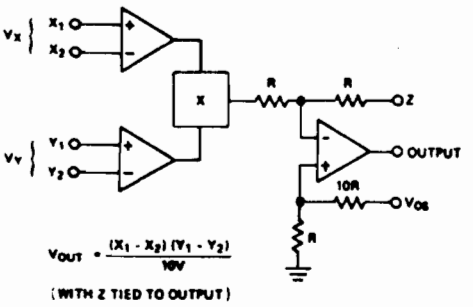


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown in Figure 1, and the complete schematic in Figure 2. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{out} = (X_1 - X_2)(Y_1 - Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{os} in critical applications . . . . otherwise the V_{os} pin should be grounded.

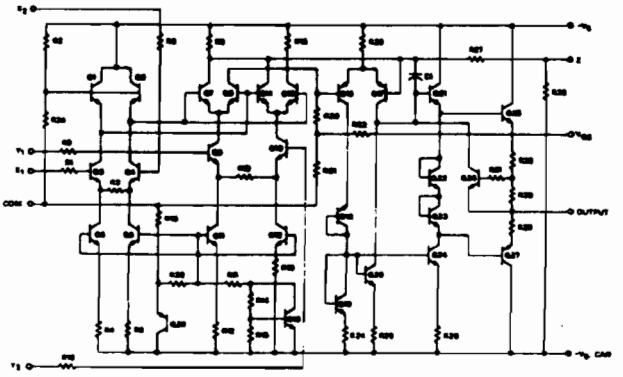


Figure 2. AD532 Schematic Diagram

AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components, since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output op amp as shown in Figure 13. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwidth and other multiplier cell errors are adversely affected. The divide error and drift are then $\epsilon_m \cdot 10/X_1 - X_2)$ where ϵ_m represents multiplier full scale error and drift, and $(X_1 - X_2)$ is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 3 and 4 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10V dc. In Figure 4 the sine wave amplitude is 20V(p-p).

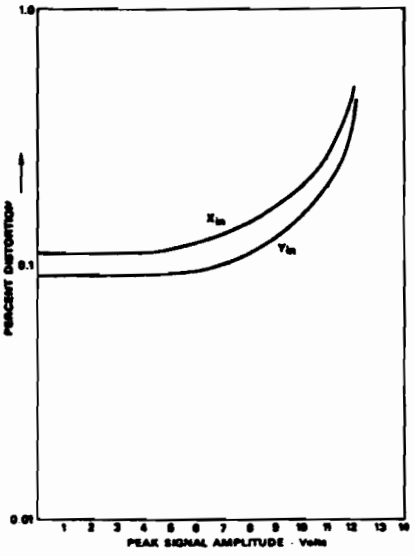


Figure 3. Percent Distortion vs. Input Signal

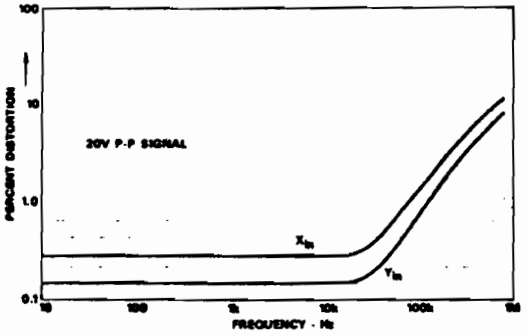


Figure 4. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC Feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 5. It is measured for the condition $V_X = 0$, $V_y = 20V(p\text{-}p)$ and $V_y = 0$, $V_X = 20V(p\text{-}p)$ over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

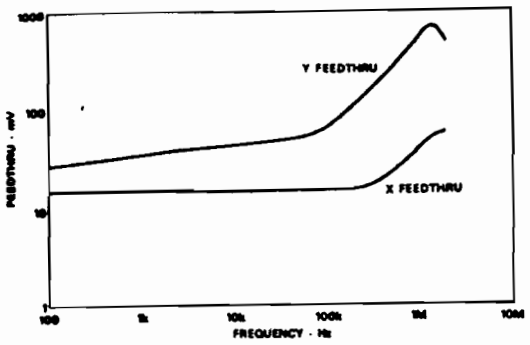


Figure 5. Feedthrough vs. Frequency

COMMON MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common mode rejection for both inputs as a function of frequency is shown in Figure 6. It is measured with $X_1 = X_2 = 20V(p\text{-}p)$, $(Y_1 - Y_2) = \pm 10V$ dc and $Y_1 = Y_2 = 20V(p\text{-}p)$, $(X_1 - X_2) = \pm 10V$ dc.

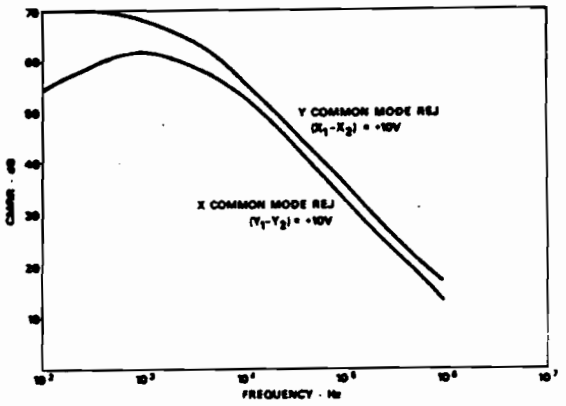


Figure 6. CMRR vs. Frequency

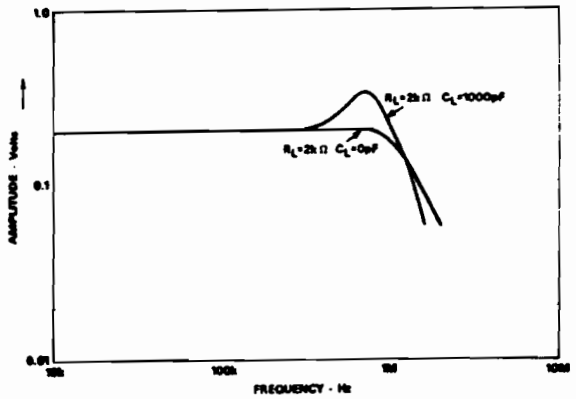


Figure 7. Frequency Response, Multiplying

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls off at 6dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 7. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 8.

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

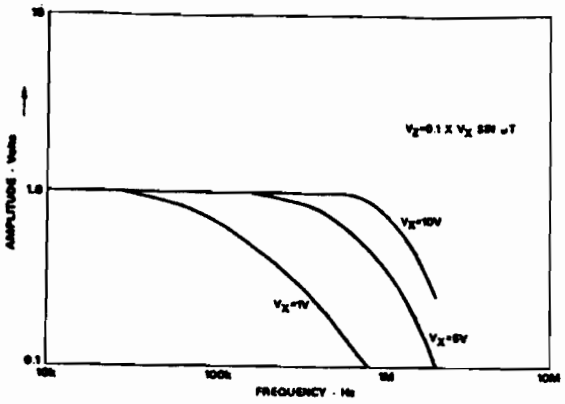


Figure 8. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15V dc supplies, it may be operated at any supply voltage from ±10V to ±18V for the J and K versions and ±10V to ±22V for the S version. The input and output signals must be reduced proportionately to prevent saturation, however, with supply voltages below ±15V, as shown in Figure 9. Since power supply sensitivity is not dependent on external null networks as in the AD530 and other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

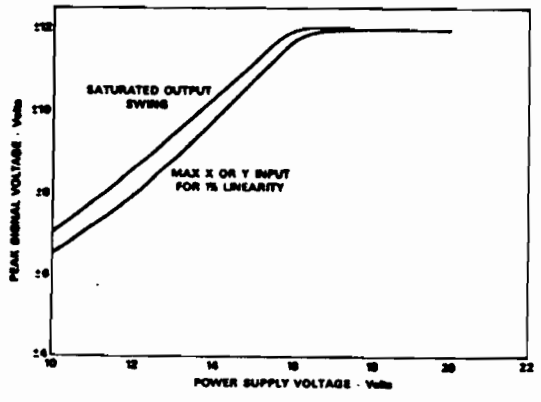


Figure 9. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532s are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 10.

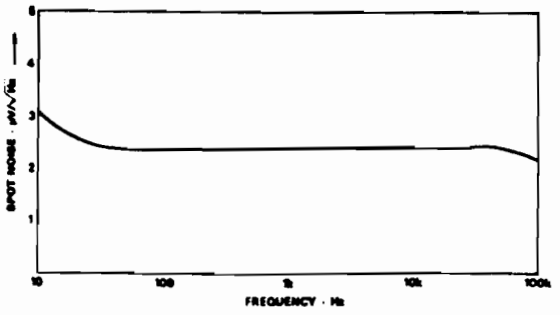


Figure 10. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks (e.g., AD530) have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks (such as the AD530) can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

APPLICATIONS

MULTIPLICATION

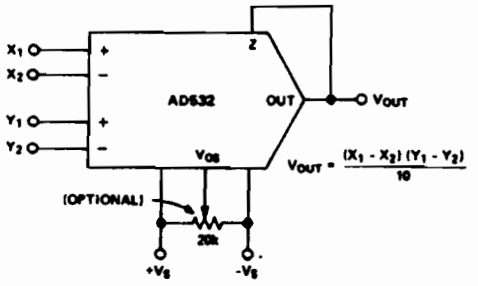


Figure 11. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 11. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see Figure 1). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

SQUARE

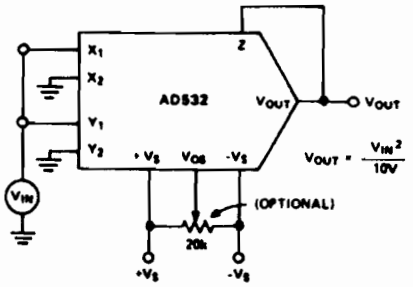


Figure 12. Squarer Connection

The squaring circuit in Figure 12 is a simple variation of the multiplier. The differential input capability of the AD532 can be used, however, to obtain a positive or negative output response to the input....a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

DIVISION

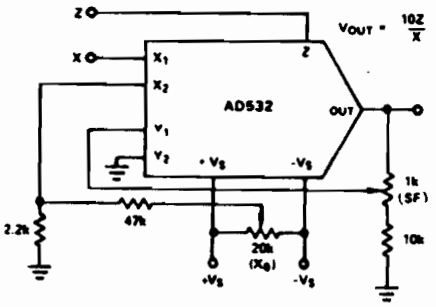


Figure 13. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 13. It should be noted, however, that the output error is given approximately by $10\epsilon_m/(X_1 - X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \cdot (X_1 - X_2)/10$, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0V to −10V), connect the input to X_1 and the offset null to X_2; for single-ended positive inputs (0V to +10V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_O) adjustments are recommended as shown and explained in Table I.

For practical reasons, the useful range in denominator input is approximately $500mV \leq |(X_1 - X_2)| \leq 10V$. The voltage offset adjust (V_{OS}), if used, is trimmed with Z at zero and $(X_1 - X_2)$ at full scale.

SQUARE ROOT

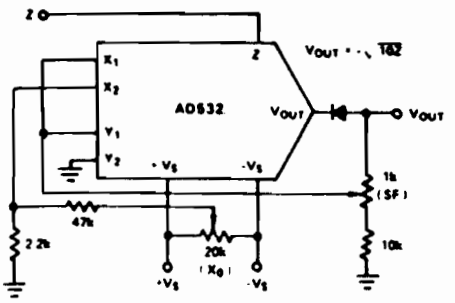


Figure 14. Square Rooter Connection

The connections for square root mode are shown in Figure 14. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{in} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{in} = +0.1V dc, adjusting V_{OS} to obtain -1.0V dc in the output, $V_{out} = -\sqrt{10Z}$. For optimum performance, gain (S.F.) and offset (X_O) adjustments are recommended as shown and explained in Table I.

DIFFERENCE OF SQUARES

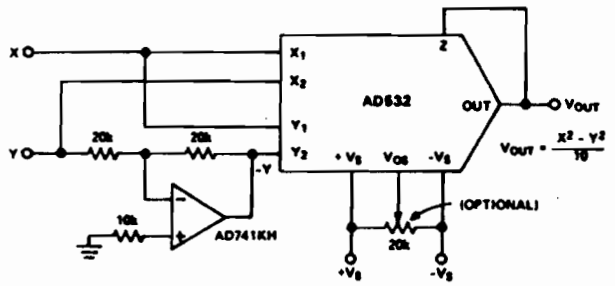


Figure 15. Difference of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X^2 - Y^2/10$. As shown in Figure 15, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{in}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

TABLE I

ADJUST PROCEDURE (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:		Adjust for:	With:	Adjust for:
Adjust	X	Z	V_{out}	Z	V_{out}
Scale Factor	−10V	+10V	±10V	+10V	−10V
X_0 (Offset)	−1V	+0.1V	±10V	+0.1V	−1V

Repeat if required.

26 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 12 V/μs Typ

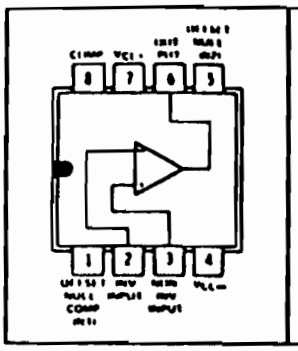
description

The TL080 JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL080 Family.

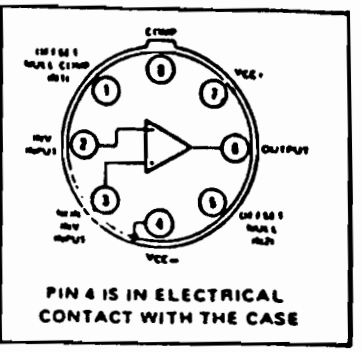
Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

TL080, TL080A

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



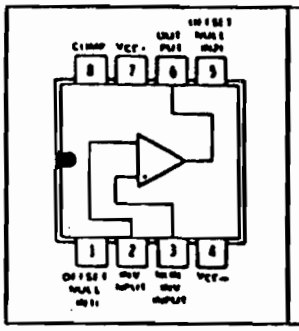
L PLUG-IN PACKAGE (TOP VIEW)



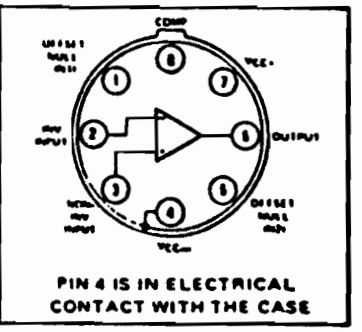
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TL081, TL081A, TL081B

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



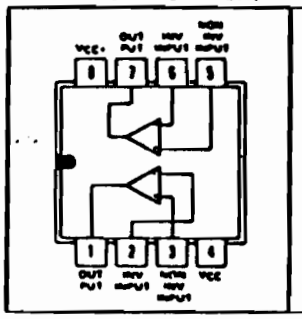
L PLUG-IN PACKAGE (TOP VIEW)



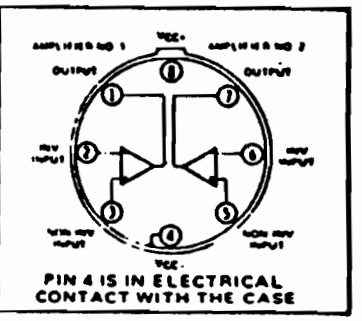
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TL082, TL082A, TL082B

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



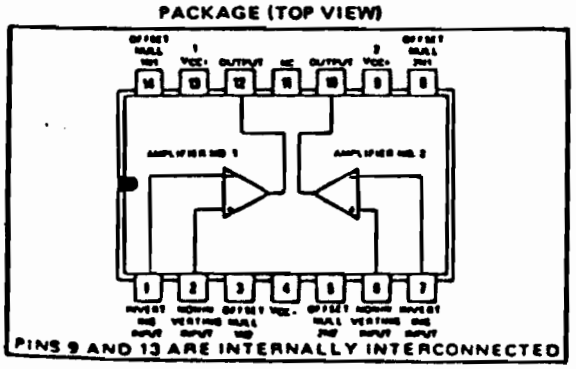
L PLUG IN PACKAGE (TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TL083, TL083A

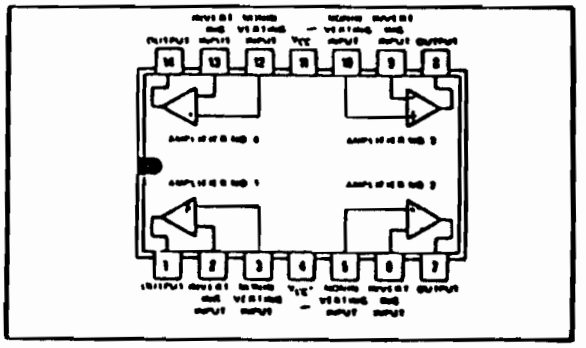
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



PINS 9 AND 13 ARE INTERNALLY INTERCONNECTED

TL084, TL084A, TL084B

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

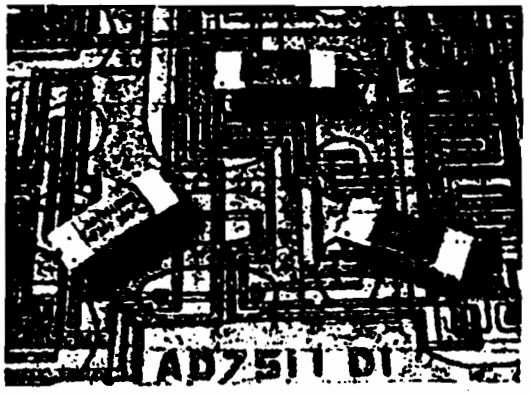


ANALOG DEVICES

DI CMOS Protected Analog Switches

AD7510DI, AD7511DI, AD7512DI

FEATURES
- Latch-Proof
- Overvoltage-Proof: ±25V
- Low R_{ON}: 75Ω
- Low Dissipation: 3mW
- TTL/CMOS Direct Interface
- Silicon-Nitride Passivated
- Monolithic Dielectrically-Isolated CMOS



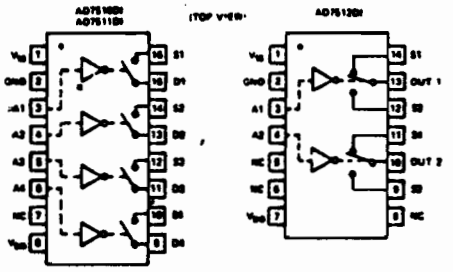
GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (400pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged in a 14-pin DIP.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

PIN CONFIGURATIONS



ORDERING INFORMATION

Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7510DIJN AD7510DIKN AD7511DIJN AD7511DIKN AD7512DIJN AD7512DIKN		0 to +70°C
	AD7510DIJD AD7510DIKD AD7511DIJD AD7511DIKD AD7512DIJD AD7512DIKD	-25°C to +85°C
	AD7510DISD AD7511DISD AD7511DITD AD7512DISD AD7512DITD	-55°C to +125°C

All ceramic versions are available screened to MIL-STD-883, method 5004 for a class B device. To order, add "/883B" to model number.

CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

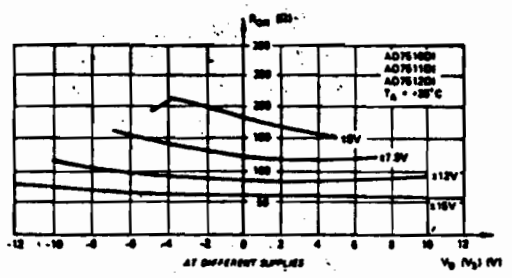
SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted)

		COMMERCIAL VERSIONS (J, K)			
PARAMETER	MODEL	VERSION	+25°C	0 to +70°C (N) −25°C to +85°C (D)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}	All	J, K	75Ω typ, 100Ω max	175Ω max	−10V ≤ V_D ≤ +10V
R_{ON} vs V_D (V_S)	All	J, K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	J, K	+0.5%/°C typ		
R_{ON} Match	All	J, K	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Drift Match	All	J, K	0.01%/°C typ		
I_D (I_S) OFF[1]	All	J, K	0.5nA typ, 5nA max	500nA max	V_D = −10V, V_S = +10V and V_D = +10V, V_S = −10V
I_D (I_S)$_{ON}$[2]	All	J, K	10nA max		V_S = V_D = +10V V_S = V_D = −10V
I_{OUT}[1]	AD7512DI	J, K	15nA max	1500nA max	V_{S1} = V_{OUT} = ±10V, V_{S2} = ∓10V and V_{S2} = V_{OUT} = ±10V, V_{S1} = ∓10V
DIGITAL CONTROL					
V_{INL}[1]	All	J, K		0.8V max	
V_{INH}[1]	All	J		3.0V min	
	All	K		2.4V min	
C_{IN}	All	J, K	3pF typ		
I_{INH}[1]	All	J, K	10nA max		V_{IN} = V_{DD}
I_{INL}[1]	All	J, K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	J, K	180ns typ		
	AD7511DI	J, K	350ns typ		V_{IN} = 0 to +3.0V
t_{OFF}	AD7510DI	J, K	350ns typ		
	AD7511DI	J, K	180ns typ		
$t_{TRANSITION}$	AD7512DI	J, K	300ns typ		
C_S (C_D)OFF	All	J, K	8pF typ		
C_S (C_D)ON	All	J, K	17pF typ		
C_{DS} (C_{S-OUT})	All	J, K	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})	All	J, K	0.5pF typ		
C_{OUT}	AD7512DI	J, K	17pF typ		
Q_{INJ}	All	J, K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to −10V
POWER SUPPLY					
I_{DD}[1]	All	J, K	800µA max	800µA max	All digital inputs = V_{INH}
I_{SS}	All	J, K	800µA max	800µA max	
I_{DD}[1]	All	J, K	500µA max	500µA max	All digital inputs = V_{INL}
I_{SS}	All	J, K	500µA max	500µA max	

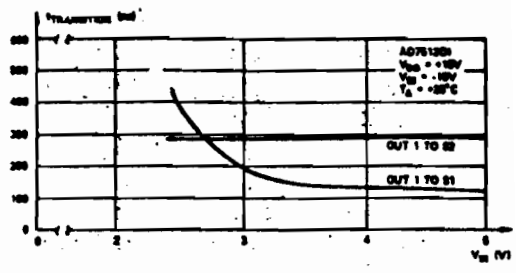
NOTES:
[1] 100% tested.
[2] Guaranteed, not production tested.
[3] A pullup resistor, typically 1-2kΩ is required to make "J" versions TTL compatible.

Specifications subject to change without notice.

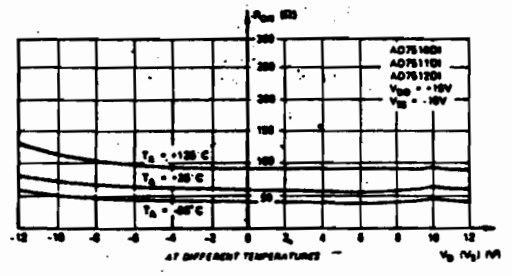
TYPICAL PERFORMANCE CHARACTERISTICS



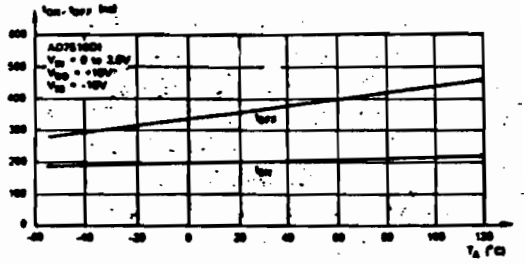
R_{ON} as a Function of V_D (V_S)



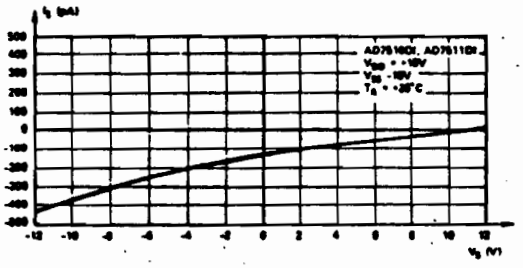
$t_{TRANSITION}$ as a Function of Digital Input Voltage



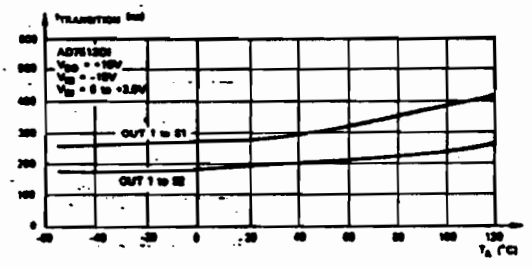
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature



I_S, $(I_D)_{OFF}$ vs V_S



$t_{TRANSITION}$ as a Function of Temperature

COS/MOS NOR Gates

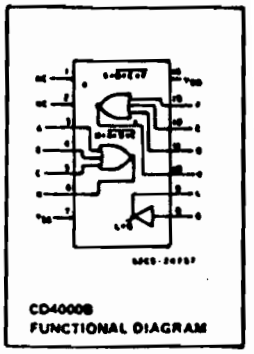
High-Voltage Types (20-Volt Rating)
Dual 3 Input
plus Inverter – CD4000B
Quad 2 Input – CD4001B
Dual 4 Input – CD4002B
Triple 3 Input – CD4025B

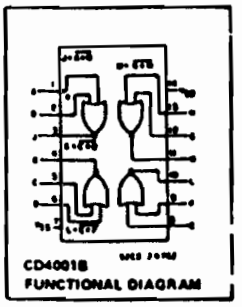
RCA-CD4000B, CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

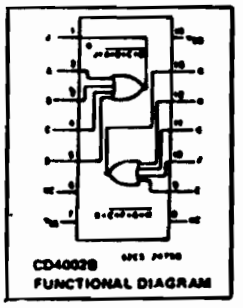
The CD4000B, CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

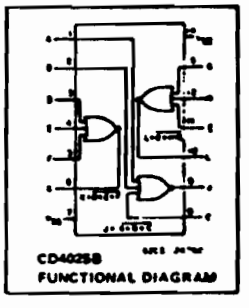
Features:

- Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"


CD4000B
FUNCTIONAL DIAGRAM


CD4001B
FUNCTIONAL DIAGRAM


CD4002B
FUNCTIONAL DIAGRAM


CD4025B
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	-	0,5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA
	-	0,10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0,15	15	1	1	30	30	-	0.01	1	
	-	0,20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage Low-Level, V_{OL} Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05					0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage High-Level, V_{OH} Min.	-	0,5	5	4.95				4.95	5	-	
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage, V_{IL} Max.	0.5,4.5	-	5	1.5				—	—	1.5	V
	1.9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min.	0.5	-	5	3.5				3.5	-	—	
	1	-	10	7				7	-	—	
	1.5	-	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	-	$±10^{-5}$	±0.1	μA

COS/MOS NAND Gates

High-Voltage Types (20-Volt Rating)

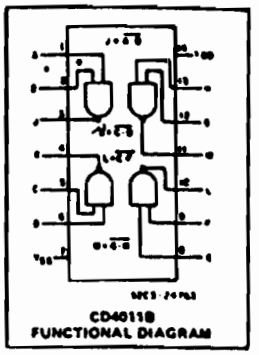
Quad 2 Input – CD4011B
Dual 4 Input – CD4012B
Triple 3 Input – CD4023B

RCA-CD4011B, CD4012B, and CD4023B NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

The CD4011B, CD4012B, and CD4023B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix) and in chip form (H suffix).

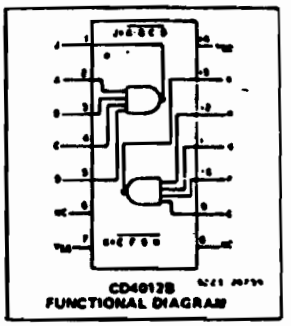
Features:

- Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"


CD4011B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

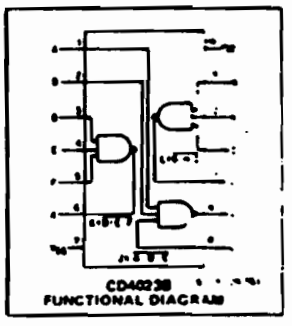
DC SUPPLY VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C


CD4012B
FUNCTIONAL DIAGRAM

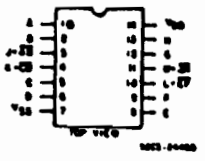
RECOMMENDED OPERATING CONDITIONS

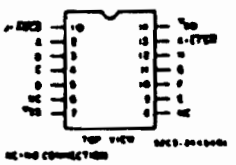
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

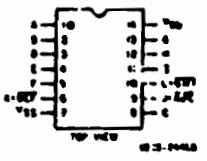
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V


CD4023B
FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS


CD4011B


CD4012B


CD4023B

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	-	0,5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA
	-	0,10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0,15	15	1	1	30	30	-	0.01	1	
	-	0,20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V_{OL} Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	-	0,5	5	4.95				4.95	5	-	
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage, V_{IL} Max.	4.5	-	5	1.5				-	-	1.5	V
	9	-	10	3				-	-	3	
	13.5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	-	5	3.5				3.5	-	-	
	1,9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	-	$±10^{-5}$	±0.1	μA

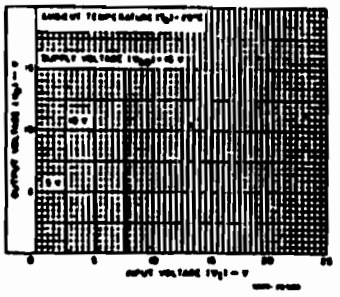


Fig.1 – Typical voltage transfer characteristics.

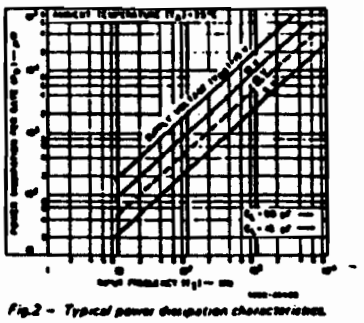


Fig.2 – Typical power dissipation characteristics.

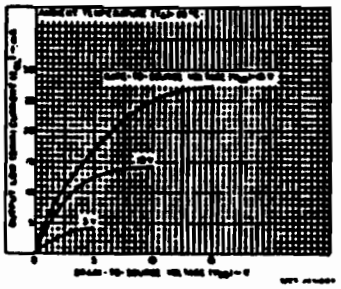


Fig.3 – Typical output low (sink) current characteristics.

Fig.4 – Minimum output low (sink) current characteristics.

Fig.5 – Typical output high (source) current characteristics.

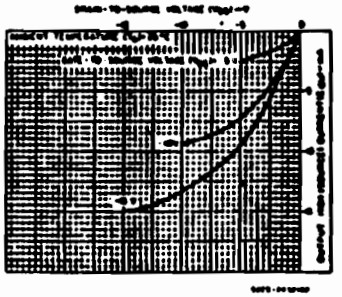


Fig.6 – Minimum output high (source) current characteristics.

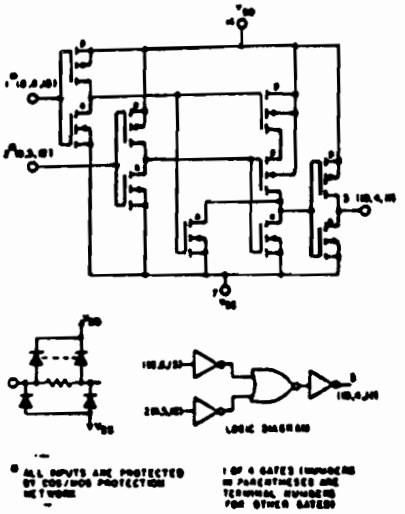


Fig.7 – Schematic and logic diagrams for CD4011B.

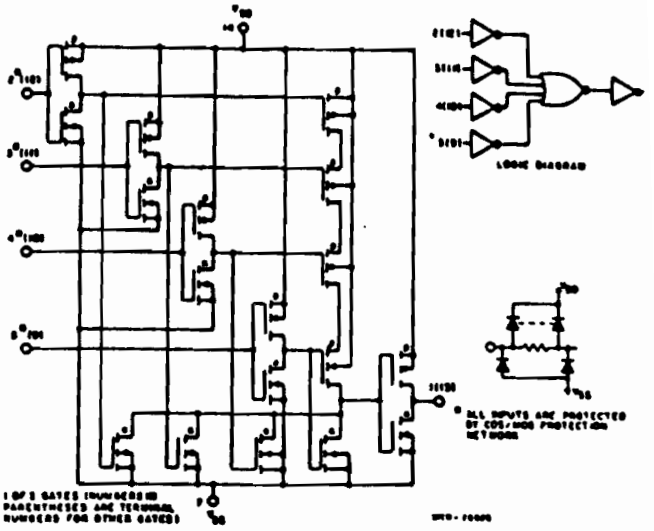


Fig.8 – Schematic and logic diagrams for CD4012B.

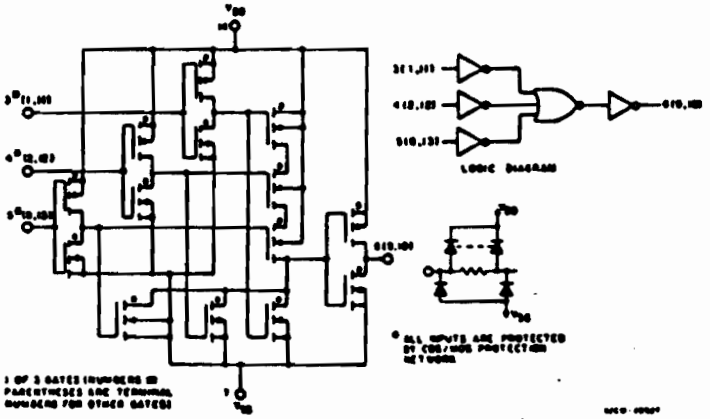


Fig. 9 – Schematic and logic diagrams for CD4023B.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS			UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

MOTOROLA

SEMICONDUCTORS

P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC34001,MC35001 MC34002,MC35002 MC34004,MC35004

TRIMFET FAMILY OF JFET INPUT OPERATIONAL AMPLIFIERS

These low cost TRIMFET operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices with a laser trimmed input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. The laser trimming technology provides input offset voltage specification options which range from 2.0 to 10 millivolts maximum.

The Motorola TRIMFET family offers single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC35001/35002/35004 series are specified over the military operating temperature range of -55°C to +125°C and the MC34001/34002/34004 series are specified from 0°C to +70°C.

- Laser Trimmed Input Offset Voltage Options of 2.0, 5.0, and 10 mV Maximum
- Low Input Bias Current – 40 pA
- Low Input Offset Current – 10 pA
- Low Input Noise Voltage – 16 $nV/\sqrt{Hz}$
- Wide Gain Bandwidth – 4 MHz
- High Slew Rate – 13 V/μs
- Low Supply Current – 1.8 mA per Amplifier
- High Input Impedance – $10^{12}\ \Omega$
- High Common-Mode and Supply Voltage Rejection Ratios – 100 dB
- Industry Standard Pinouts

ORDERING INFORMATION

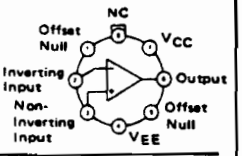
Op Amp Function	Device	Temperature Range	Package
Single	MC34001AG,BG,G	0 to +70°C	Metal Can
	MC34001AP,BP,P	0 to +70°C	Plastic DIP
	MC34001AU,BU,U	0 to +70°C	Ceramic DIP
	MC35001AG,BG	−55 to +125°C	Metal Can
	MC35001AU,BU	−55 to +125°C	Ceramic Dip
Dual	MC34002AG,BG,G	0 to +70°C	Metal Can
	MC34002AP,BP,P	0 to +70°C	Plastic DIP
	MC34002AU,BU,U	0 to +70°C	Ceramic DIP
	MC35002AG,BG	−55 to +125°C	Metal Can
	MC35002AU,BU	−55 to +125°C	Ceramic DIP
Quad	MC34004AL,BL,L	0 to +70°C	Ceramic DIP
	MC34004AP,BP,P	0 to +70°C	Plastic DIP
	MC35004,AL,BL	−55 to +125°C	Ceramic DIP

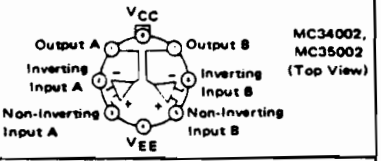
TRIMFET FAMILY OF BIFET OPERATIONAL AMPLIFIERS

LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUITS

G SUFFIX
METAL PACKAGE
CASE 601

MC34001, MC35001
(Top View)

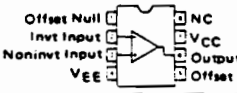




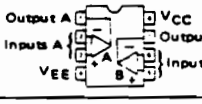
MC34002, MC35002
(Top View)

P SUFFIX
PLASTIC PACKAGE
CASE 626
(MC34001, MC34002 only)

U SUFFIX
CERAMIC PACKAGE
CASE 693

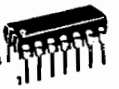


MC34001, MC35001
(Top View)

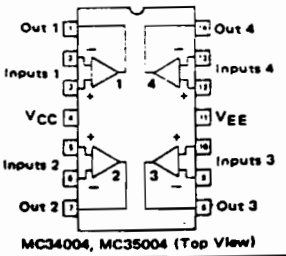


MC34002, MC35002
(Top View)

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC34004 only)



MC34004, MC35004 (Top View)

APPENDIX B

TABLE OF LAPLACE TRANSFORM

Laplace Transform Table

Laplace transform $F(s)$	*Time function* $f(t)$
$\frac{1}{s}$	$u(t)$ (unit step function)
$\frac{1}{s^2}$	t
$\frac{n!}{s^{n+1}}$	t^n (n = integer)
$\frac{1}{s+a}$	e^{-at}
$\frac{1}{(s+a)(s+b)}$	$\frac{e^{-at}-e^{-bt}}{b-a}$
$\frac{\omega_n^2}{s^2+2\delta\omega_n s+\omega_n^2}$	$\frac{\omega_n}{\sqrt{1-\delta^2}}e^{-\delta\omega_n t}\sin\omega_n\sqrt{1-\delta^2}t$
$\frac{1}{(1+sT)^n}$	$\frac{1}{T^n(n-1)!}t^{n-1}e^{-t/T}$
$\frac{\omega_n^2}{(1+Ts)(s^2+2\delta\omega_n s+\omega_n^2)}$	$\frac{T\omega_n^2 e^{-t/T}}{1-2\delta T\omega_n+T^2\omega_n^2}+\frac{\omega_n e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}t-\phi)}{\sqrt{(1-\delta^2)(1-2\delta T\omega_n-T^2\omega_n^2}}$, where $\phi=\tan^{-1}\frac{T\omega_n\sqrt{1-\delta^2}}{1-T\delta\omega_n}$
$\frac{\omega_n}{(s^2+\omega_n^2)}$	$\sin\omega_n t$
$\frac{\omega_n}{(1+Ts)(s^2+\omega_n^2)}$	$\frac{T\omega_n}{1+T^2\omega_n^2}e^{-t/T}+\frac{1}{\sqrt{1+T^2\omega_n^2}}\sin(\omega_n t-\phi)$ where $\phi=\tan^{-1}\omega_n T$
$\frac{\omega_n^2}{s(s^2+2\delta\omega_n s+\omega_n^2)}$	$1+\frac{1}{\sqrt{1-\delta^2}}e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}t-\phi)$ where $\phi=\tan^{-1}\frac{\sqrt{1-\delta^2}}{-\delta}$
$\frac{\omega_n^2}{s(s^2+\omega_n^2)}$	$1-\cos\omega_n t$
$\frac{1}{s(1+Ts)}$	$1-e^{-t/T}$
$\frac{1}{s(1+Ts)^2}$	$1-\frac{t+T}{T}e^{-t/T}$
$\frac{\omega_n^2}{s(1+Ts)(s^2+2\delta\omega_n s+\omega_n^2)}$	$1-\frac{T^2\omega_n^2}{1-2T\delta\omega_n+T^2\omega_n^2}e^{-t/T}+\frac{e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}t-\phi)}{\sqrt{1-\delta^2(1-2\delta T\omega_n+T^2\omega_n^2)}}$ where $\phi=\tan^{-1}(\sqrt{1-\delta^2}/-\delta)+\tan^{-1}[T\omega_n\sqrt{1-\delta^2}/(1-T\delta\omega_n)]$
$\frac{\omega_n^2}{s^2(s^2+2\delta\omega_n s+\omega_n^2)}$	$t-\frac{2\delta}{\omega_n}+\frac{1}{\omega_n\sqrt{1-\delta^2}}e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}t-\phi)$ where $\phi=2\tan^{-1}(\sqrt{1-\delta^2})/-\delta$

LAPLACE TRANSFORM TABLE (*cont.*)

Laplace transform $F(s)$	*Time function* $f(t)$
$\dfrac{\omega_n^2}{s^2(1+Ts)(s^2+2\delta\omega_n s+\omega_n^2)}$	$t - T - \dfrac{2\delta}{\omega_n} + \dfrac{T^2\omega_n^2}{1-2\delta\omega_n T+T^2\omega_n^2}\,e^{-t/T} + \dfrac{e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}\,t-\phi)}{\omega_n\sqrt{(1-\delta^2)(1-2\delta\omega_n T+T^2\omega_n^2}}$ where $\phi = 2\tan^{-1}(\sqrt{1-\delta^2}/-\delta) + \tan^{-1}[T\omega_n\sqrt{1-\delta^2}/(1-T\omega_n\delta)]$
$\dfrac{1}{s^2(1+Ts)^2}$	$t - 2T + (t+2T)e^{-t/T}$
$\dfrac{\omega_n^2(1+as)}{s^2+2\delta\omega_n s+\omega_n^2}$	$\omega_n\sqrt{\dfrac{1-2a\delta\omega_n+a^2\omega_n^2}{1-\delta^2}}\,e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}\,t+\phi)$ where $\phi = \tan^{-1}\dfrac{a\omega_n\sqrt{1-\delta^2}}{1-a\delta\omega_n}$
$\dfrac{\omega_n^2(1+as)}{(s^2+\omega_n^2)}$	$\omega_n\sqrt{1+a^2\omega_n^2}\sin(\omega_n t+\phi)$ where $\phi = \tan^{-1}a\omega_n$
$\dfrac{\omega_n^2(1+as)}{(1+Ts)(s^2+2\delta\omega_n s+\omega_n^2)}$	$\dfrac{\omega_n}{\sqrt{1-\delta^2}}\sqrt{\dfrac{1-2a\delta\omega_n+a^2\omega_n^2}{1-2T\delta\omega_n+T^2\omega_n^2}}\,e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}\,t+\phi) + \dfrac{(T-a)\omega_n^2}{1-2T\delta\omega_n+T^2\omega_n^2}\,e^{-t/T}$ where $\phi = \tan^{-1}\dfrac{a\omega_n\sqrt{1-\delta^2}}{1-a\delta\omega_n} - \tan^{-1}\dfrac{T\omega_n\sqrt{1-\delta^2}}{1-T\delta\omega_n}$
$\dfrac{\omega_n^2(1+as)}{(1+Ts)(s^2+\omega_n^2)}$	$\dfrac{\omega_n^2(T-a)}{1+T^2\omega_n^2}\,e^{-t/T} + \dfrac{\omega_n\sqrt{1+a^2\omega_n^2}}{\sqrt{1+T^2\omega_n^2}}\sin(\omega_n t+\phi)$ where $\phi = \tan^{-1}a\omega_n - \tan^{-1}\omega_n T$
$\dfrac{\omega_n^2(1+as)}{s(s^2+2\delta\omega_n s+\omega_n^2)}$	$1 + \dfrac{1}{\sqrt{1-\delta^2}}\sqrt{1-2a\delta\omega_n+a^2\omega_n^2}\,e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}\,t+\phi)$ where $\phi = \tan^{-1}\dfrac{a\omega_n\sqrt{1-\delta^2}}{1-a\delta\omega_n} - \tan^{-1}\dfrac{\sqrt{1-\delta^2}}{-\delta}$
$\dfrac{\omega_n^2(1+as)}{s(1+Ts)(s^2+\omega_n^2)}$	$1 + \dfrac{T\omega_n^2(a-T)}{1+T^2\omega_n^2}\,e^{-t/T} - \sqrt{\dfrac{1+a^2\omega_n^2}{1+T^2\omega_n^2}}\cos(\omega_n t+\phi)$ where $\phi = \tan^{-1}a\omega_n - \tan^{-1}\omega_n T$
$\dfrac{\omega_n^2(1+as)}{s(1+Ts)(s^2+2\delta\omega_n s+\omega_n^2)}$	$1 + \sqrt{\dfrac{1-2a\omega_n+a^2\omega_n^2}{(1-\delta^2)(1-2T\delta\omega_n+T^2\omega_n^2}}\,e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}\,t+\phi) + \dfrac{\omega_n^2T(a-T)}{1-2T\delta\omega_n+T^2\omega_n^2}\,e^{-t/T}$ $\phi = \tan^{-1}[a\omega_n\sqrt{1-\delta^2}(1-\rho\delta\omega_n)] - \tan^{-1}[T\omega_n\sqrt{1-\delta^2}/(1-T\delta\omega_n)] - \tan^{-1}(\sqrt{1-\delta^2}/-\delta)$
$\dfrac{1+as}{s^2(1+Ts)}$	$t + (a-T)(1-e^{-t/T})$
$\dfrac{s\omega_n^2}{s^2+2\delta\omega_n s+\omega_n^2}$	$\dfrac{\omega_n^2}{\sqrt{1-\delta^2}}\,e^{-\delta\omega_n t}\sin(\omega_n\sqrt{1-\delta^2}\,t+\phi$ where $\phi = \tan^{-1}\dfrac{\sqrt{1-\delta^2}}{-\delta}$

LAPLACE TRANSFORM TABLE (*cont.*)

Laplace transform $F(s)$	*Time function* $f(t)$
$\frac{s}{s^2 + \omega_n^2}$	$\cos \omega_n t$
$\frac{s}{(s^2 + \omega_n^2)^2}$	$\frac{1}{2\omega_n} t \sin \omega_n t$
$\frac{s}{(s^2 + \omega_{n1}^2)(s^2 + \omega_{n2}^2)}$	$\frac{1}{\omega_{n2}^2 - \omega_{n1}^2} (\cos \omega_{n1} t - \cos \omega_{n2} t)$
$\frac{s}{(1 + Ts)(s^2 + \omega_n^2)}$	$\frac{-1}{(1 + T^2\omega_n^2)} e^{-t/T} + \frac{1}{\sqrt{1 + T^2\omega_n^2}} \cos (\omega_n t - \phi)$ where $\phi = \tan^{-1} \omega_n T$
$\frac{1 + as + bs^2}{s^2(1 + T_1 s)(1 + T_2 s)}$	$t + (a - T_1 - T_2) + \frac{b - aT_1 + T_1^2}{T_1 - T_2} e^{-t/T} - \frac{b - aT_2 + T_2^2}{T_1 - T_2} e^{-t/T_2}$
$\frac{\omega_n^2(1 + as + bs^2)}{s(s^2 + 2\delta\omega_n s + \omega_n^2)}$	$1 + \sqrt{\frac{(1 - a\delta\omega_n - b\omega_n^2 + 2b\delta^2\omega_n^2)^2 + \omega_n^2(1 - \delta^2)(a - 2b\delta\omega_n)^2}{(1 - \delta^2)}}$ $e^{-\delta\omega_n t} \sin (\omega_n \sqrt{1 - \delta^2} t + \phi)$ $\phi = \tan^{-1} \frac{\omega_n \sqrt{1 - \delta^2}(a - 2b\delta\omega_n)}{b\omega_n(2\delta^2 - 1) + 1 - a\delta\omega_n} - \tan^{-1} \frac{\sqrt{1 - \delta^2}}{-\delta}$
$\frac{s^2}{(s^2 + \omega_n^2)^2}$	$\frac{1}{2\omega_n} (\sin \omega_n t + \omega_n t \cos \omega_n t)$

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