Variable-Speed Power Switch Gate Driver for Switching Loss Reduction in Automotive Inverters

By Alexey Sokolov

Master of Engineering

Department of Electrical and Computer Engineering

McGill University, Montreal, Quebec

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Abstract

In the present time, electrical power conversion is performed more and more widely using fully-controllable semiconductor devices such as IGBTs, MOSFETs, and Silicon-Carbide (SiC) MOSFETs, in conjunction with diodes made of the same materials. DC to AC conversion and vice-versa is required in brushless motor/generator drives powered by DC sources, such as batteries in electric and hybrid electric vehicles.

This thesis reviews modern gate drivers and performance testing methods for gate drivers. Based on hardware testing results, it introduces a new method of switching loss reduction for IGBT converters, implemented through a series of innovations on the gate driver operation principle and schematics. The switching loss reduction is achieved by varying the IGBT gate current across different switching transitions, depending on the load current and other factors. In particular, it has been shown that increasing the gate current (and switching transition speed) near load current zero-crossings results in more complete utilization density of the IGBT safe operating area, allowing a tradeoff to reduce switching losses, and to increase converter efficiency. The proposed method leaves motor harmonic losses completely unchanged and does not modify the pulse width modulation scheme.

Résumé

Dans le temps présent, la conversion de puissance électrique se fait de plus en plus en utilisant des appareils semi-conducteurs contrôlables, comme IGBT, MOSFET, et MOSFET à carbide de silicium (SiC), ensemble avec des diodes fabriqués des mêmes matériaux. La conversion CC à CA et vice-versa est nécessaire pour alimenter des moteurs et des génératrices sans balais par des sources CC, comme les batteries dans les véhicules électriques et hybrides.

Cette thèse examine les "gate drivers" modernes et méthodes de vérification de leur performance. Basé sur les résultats des tests de matériel, elle introduit une nouvelle méthode de réduction des pertes de commutation pour les convertisseurs à IGBT, réalisée par une série d'innovations sur le principe d'opération du "gate driver" et ses schémas. La réduction des pertes de commutation se fait en changeant le courant de gâchette parmi les différentes transitions de commutation, dépendamment du courant passant par la charge, et d'autres facteurs. En particulier, il a été montré qu'en augmentant le courant de gâchette (et la vitesse de transition de commutation) proche des moments quand le courant de charge passe par zéro, a comme résultat l'utilisation plus complète de l'aire d'opération sécuritaire du IGBT, ce qui permet de réduire les pertes de commutation et d'augmenter l'efficacité du convertisseur. La méthode proposée laisse les pertes harmoniques du moteur sans changements, et ne modifie pas le schéma de modulation de largeur d'impulsions.

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Finally, I dedicate the scientific value of this work to my parents, Alexey and Zhanna, who worked hard to support me all the way through my education, including the two years spent on this research.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

AC	*Alternating Current*
ADC	*Analog-to-Digital Converter*
BJT	*Bipolar Junction Transistor*
C-E	*Collector-Emitter*
CGD	*Conventional Gate Driver*
CPU	*Central Processing Unit*
CT	*Current Transformer*
CTL, CTRL	*Control Signal*
DAC	*Digital-to-Analog Converter*
DC	*Direct Current*
DPWM2	*Discontinuous Pulse-Width Modulation Type 2*
DSP	*Digital Signal Processor/Processing*
EMI	*Electro-Magnetic Interference*
GAL	*Gate-Array Logic*
G-C	*Gate-Collector*
G-E	*Gate-Emitter*
GND	*Ground Node*
I/O	*Input/Output*
IEEE	*Institute of Electrical and Electronics Engineers*
IGBT	*Isolated-Gate Bipolar Transistor*
INT	*Interrupt*
JEDEC	*Joint Electron Device Engineering Council*
LC	*Inductor-Capacitor*
MATLAB	*MATrix LABoratory (software)*
MOSFET	*Metal-Oxide-Semiconductor Field Effect Transistor*
PCB	*Printed Circuit Board*
PGD	*Proposed Gate Driver*
PN	*Positive and Negative semiconductor layers*
PSIM	*Power SIMulator (software)*
PSpice	*Personal Simulation Program with Integrated Circuit Emphasis*
PV	*Photo-Voltaic*
PWM	*Pulse-Width Modulation*
RC	*Resistor-Capacitor*
RLC	*Resistor-Inductor-Capacitor*
SiC	*Silicon Carbide*
SOA	*Safe Operating Area*
STDEV	*STandard DEViation*
SVPWM	*Space-Vector Pulse-Width Modulation*
TVS	*Transient Voltage Suppressor*

List of Acronyms

β	*DC current transfer ratio*
C_{CE}	*Collector-emitter capacitance*
C_{DS}	*Drain-source capacitance*
C_{GC}	*Gate-collector capacitance*
C_{GD}	*Gate-Drain capacitance*
C_{GE}	*Gate-emitter capacitance*
C_{GS}	*Gate-source capacitance*
C_{iss}	*Input capacitance*
C_{JO}	*Zero-bias capacitance*
C_{miller}	*Miller capacitance, common notation for C_{GC} and C_{GD}*
C_{oss}	*Output capacitance*
C_{rss}	*Reverse transfer capacitance*
D	*Duty cycle*
E_C	*Conduction loss*
E_{ON}	*Turn-on loss*
E_{OFF}	*Turn-off loss*
g_m	*Forward transconductance*
I_C	*Collector current*
I_D	*Drain current*
I_F	*Forward current*
I_G	*Gate current*
I_L	*Load current*
I_{MAX}	*Maximum current*
I_{OS}, I_{rr}	*Overshoot or reverse-recovery current*
I_S	*Saturation current*
K_F	*Triode region factor*
K_P	*Transconductance coefficient*
L_E	*Emitter inductance*
L_G	*Gate inductance*
L_S	*Source inductance, stray inductance*
M	*PN grading coefficient*
N	*Emission coefficient (in PSpice), buffer size (in DSP)*
Q_{rr}	*Reverse-recovery charge*
R_G	*Gate resistance*
R_S	*Series resistance*
t	*Time*
u	*Control input*
V_{CE}	*Collector-emitter voltage*
V_D, V_J	*Diode junction potential*

V_{DC}	*DC link voltage*
V_{DS}	*Drain-source voltage*
V_{GE}	*Gate-emitter voltage*
V_{GS}	*Gate-source voltage*
V_F	*Forward voltage*
V_{GE}	*Gate-emitter voltage*
V_{MAX}	*Maximum voltage*
V_{OV}	*Overdrive voltage*
V_{OS}	*Overshoot voltage*
V_T	*Threshold voltage (for transistor), thermal voltage (for diode)*

Chapter 1: Introduction

1.1. Background

In power electronic DC/AC converters the preferred switching devices in use nowadays are IGBTs and diodes, often assembled in modules, and operating typically with DC link voltages of several hundred Volts. Each phase of the AC side is usually connected to a so-called "inverter leg", which is a set of switching devices used to select which voltage level on the DC side will source or sink the current to the AC side. Depending on the AC side (load) current direction and the DC voltage level selected by the system controller, the current can flow through a transistor, a diode, or many sets of them in case of a multilevel converter.

A gate driver is a circuit providing electrical interface between the low-voltage system controller and high-voltage semiconductor devices. Its second most important function is to bring the conduction and switching losses of power switches as low as possible, while respecting maximum ratings of devices. The gate driver is usually omitted from system-oriented simulation software, e.g. MATLAB, PSIM. Therefore, other methods and software are required to perform research on gate drivers. These include more electronically-oriented tools like PSpice, and hardware testing.

1.2. Motivation

Ideally one would like to expect a zero propagation delay from the system controller to the power converter, have IGBTs and diodes switch in zero time with minimum switching loss and have zero on-state voltage drop with minimum conduction loss. The IGBTs have physical limitations, and the purpose of the gate driver is to make the IGBTs switch with optimal performance (i.e. minimize switching and conduction losses) given their limitations.

Semiconductor devices themselves went through many changes in their physical layer structure to achieve theoretically ideal switching. BJTs have good output characteristics, but

require a lot of control (base-emitter) current to flow during the entire conduction period of time. MOSFETs are fast and do not require constant gate current to conduct, but have large input capacitance and cannot support as much voltage in the off-state as BJTs can. Thyristors can support high voltage and do not require constant gate current, but cannot be turned off from the gate. Gate turn-off thyristors have the turn-off capability from the gate, but at the expense of large increase of switching and conduction losses, which limits the frequency of operation. IGBTs have the best features of BJTs and MOSFETs combined: they have BJT output characteristics, and MOSFET isolated gates, with gate capacitance of typically 1/10 of that of a MOSFET. All these features make the IGBTs approach the ideal characteristics closer than other devices in overall. The future of device development does not stop at IGBTs. A newly emerging technology of silicon-carbide (SiC) material to replace commonly used silicon will find applications in diodes, MOSFETs and IGBTs. Silicon-carbide MOSFETs might even outperform currently existing silicon IGBTs by some parameters.

For a specific switching application, device type selection is mostly based on voltage and frequency. To minimize losses, it is important to choose the device scale appropriately in the first place. If the device current rating is higher than required, switching losses increase because of higher junction capacitance. On the other hand, decreasing device current rating leads to increase of conduction losses.

Most datasheets and loss calculation tools are based on measurements taken while the device is driven by a conventional gate driver with a fixed gate resistance, provided in the datasheet as "optimal". The purpose of this research is to develop a new gate driving scheme that should result in lower average switching losses than what is provided in datasheets for a conventional gate driver.

1.3. Issues with electric traction drives

Complete motor drive systems currently have numerous issues subject to research and improvement. Traction applications require special attention and demand more requirements comparing to industrial drives, because of their wider range of rotor speeds in steady state. The motor drive system has two major stages of energy conversion: DC to AC, and AC to

mechanical. The first conversion is associated with converter losses, and the second one is associated with motor losses. Besides the tradeoffs that exist between converter and motor losses, other factors have to be taken into consideration when designing or improving a motor drive system: motor ripple current, DC link capacitor ripple current and voltage, capacitor size and weight, stray inductance of the loop joining the capacitor and the converter, maximum converter temperature, cooling requirements, allowed amount of EMI emissions, and others. The issues relevant to improvement of the gate driver are described below.

Because the switching losses become important at high switching frequencies, which are required to minimize motor losses, a method of reducing switching losses is required.

Stray inductance between the DC link capacitor and the converter has to be minimized because it has impact on the maximum turn-off speed of the IGBT, directly setting the lower limit on turn-off losses. Reduction of stray inductance can be achieved by proper mechanical design of the connection between the capacitor and the converter, and/or by arranging the connections inside the converter in groups by switching cells rather than by IGBT/diode pairs [1].

EMI emission spectrum depends on the converter and on the mechanical structure or casing (including shielding) where the drive system is installed (coupling path). The latter is not covered by the scope of the gate driver research, but can have an impact on the EMI requirements of the converter. On the other hand, better design of the coupling path can relax converter EMI restrictions.

1.4. Problem statement

The conversion losses dissipated by devices in form of heat consist of three sources: conduction losses, leakage current losses, and switching losses. The first two sources usually cannot be varied as long as appropriate extreme levels of gate-emitter voltage are applied to the IGBT. These losses are specific to the device selected, its die size, and generation of IGBT technology. The switching losses, on the contrary, can be widely varied by using different modulation schemes, switching frequencies, and gate drivers. Fast switching has been recently

discovered to cause current and voltage transients, and care should be taken not to exceed device maximum ratings.

The overall engineering task looks like a constrained optimization problem with objective function to minimize converter losses (and in case of a motor drive, motor losses as well), by selecting the right converter device and modulation scheme. This is the first level of optimization that usually takes place before gate driver design. The second level of optimization is to find a way to further decrease switching losses (the only variable), by varying gate control signals. The constraints are the maximum ratings of converter's IGBTs and diodes, and the device choice links back to the first optimization problem.

1.5. Objectives

Several tasks need to be performed in order to design a gate driver offering switching loss reduction:

- Understand switching mechanics and origin of switching losses.
- Determine factors influencing switching losses.
- Determine the best gate waveform generation methods using real hardware.
- Propose a closed-loop control system using a certain strategy of real-time switching loss constrained minimization, based on previous observations.
- Develop an algorithm representing the control system, with hardware features and constraints in mind.
- Verify the algorithm performance with simulations.
- Implement the new gate driver control system in hardware and compare switching losses to a conventional gate driver (not covered in thesis).

The ultimate goal of this research is to show the switching loss reduction using the proposed method. Switching loss reduction can bring the following benefits if used in an electric or hybrid vehicle application:

- Lower temperature of IGBT converter can improve switching device reliability.
- Smaller heatsink can reduce cost and weight of the converter.
- Saved energy slightly increases the electric vehicle range.
- Since the method works for both traction and regeneration, the turn-around energy loss for acceleration and deceleration is reduced.

1.6. Methodology

For analyzing switching losses, a PSpice model of an IGBT converter was created and tested with different gate resistors and load currents. Internal IGBT parameters were varied to observe effects on switching performance.

For experiments on switching loss reduction, a double-pulse test circuit has been implemented in hardware, and tested with six different types of gate drive techniques.

For control system development, MATLAB code was used to replicate code-like behaviour of a microcontroller, keeping in mind limited CPU resources, such as clock speed and memory.

For switching loss reduction estimation with the closed-loop control system, PSpice model equations derived earlier were reused, in conjunction with device datasheet parameters.

1.7. Claims of originality

This research work is based on many sources about switching device models, switching transient parameters, and gate driver circuit developments for IGBTs and MOSFETs. Like in any innovation-oriented research, a few contributions can be considered novel as of present time, to the best of the author's knowledge:

1. Design of gate driver output stage with continuously variable gate current, a new method of IGBT switching process control. It differs from existing methods of applying preset voltage waveforms on gate resistor, or using multi-stage drivers with timing control.
2. Proposal of a new method of switching loss reduction in IGBT converters, along with adaptive feedback control algorithm required for it.
    a. Filling IGBT SOA envelope with current and voltage overshoots for tradeoff with switching losses.

b. Formulation of the variable-speed gate driver control problem of not knowing the overshoot before a switching transient occurs, and the solution to it by estimating switching parameters from previous PWM pulses.

c. Development of procedures to ensure stable algorithm startup and performance: selective measurement filtering and slow switching speed pulse injection at regular intervals.

1.8. Thesis structure

The body of the thesis is organized as follows:

Chapter 2 presents a literature review on gate drivers, their classification by various criteria, and application. It also includes their development during recent history, evolution of topology of their output stages, based on objectives researchers were trying to achieve. Since any gate driver nowadays is being optimized for the switching device it controls, there is a review of most important MOSFET and IGBT parameters and their equivalent circuit models. Finally, an extra topic is dedicated to feedback control in modern gate drivers.

Chapter 3 focuses on development of IGBT inverter PSpice model, which has an objective of better modeling the switching processes (turn-on and turn-off) than built-in PSpice IGBT and diode models, and which are computationally faster and more robust than physical device models provided by some manufacturers. The new model has an objective of serving for switching loss estimation when used with PSpice models of gate drivers, and to determine gate driver factors influencing switching losses.

Chapter 4 describes how PSpice simulation results have been confirmed by running hardware tests of the switching process run on reduced-scale experimental setup, which is a double-pulse circuit with one semi-controlled 2-level inverter leg. After confirming the main "rule of thumb" of relationship between switching losses and switching speed, the double-pulse setup served as a test bench for more advanced types of gate driver output stages, in order to find gate signal waveforms that could reduce switching losses even further.

Chapter 5 is aimed to find ways from the control point of view how to exploit the major principle of switching loss reduction established in Chapter 4 using two types of tested gate driver output stages. The reduction is achieved by using a variable-speed gate driver on varying sinusoidal load current in each leg of the DC/AC converter. Multiple PWM pulses are therefore considered. The control strategy is explained backwards: first the ideal output waveforms are presented, then the mathematical relationships are derived, and finally the control algorithm is given along with flowcharts and timing charts.

Chapter 6 contains simulation results of the developed gate driver feedback control algorithm on a full-scale inverter and motor models. The simulation results demonstrate the stability of the algorithm for different PWM schemes at different motor torque and speed values, and that it closely follows the ideal waveforms in order to maximize the loss reduction effect. Switching losses are compared between a conventional and the proposed gate drivers, and conduction losses are also estimated for reference.

Finally, Chapter 7 discusses the overall advantages and disadvantages of the proposed switching loss reduction method in gate drivers, summarizes the results achieved, and lists possible paths of further research and development in the direction of current research.

Chapter 2:
Review of Conventional Technologies of Gate Drivers

2.1. Gate driver classification

2.1.1. Classification by architecture

One of the primary requirements of a gate driver is to provide an interface between a low-voltage system controller and a high-voltage power converter. In some cases the interface circuits can be made without using isolation devices, but in most other cases galvanic isolation is required. Depending on having isolation or not and a few other differences, one can distinguish between four main architectural classes of gate drivers:

- Non-isolated direct driver.
  This is the most basic driver by architecture, because it offers no level-shifting features.

- Non-isolated high-side driver with capacitive coupling.
  It is usually implemented in an integrated circuit for driving both high and low side transistors of 2-level converters.

- Isolated driver with power supply and input signal isolation.
  Both power and input signal isolation can be implemented using magnetic (transformer) or optical coupling. An example of optical power transmission to the gate driver would be a laser beam over fiber-optic cable to a small PV cell [2].

- Isolated driver with isolation in the output stage.
  This driver can take advantage of isolating transformer turn ratio to match the output characteristics of the driving transistors to the input characteristics of the power switch gate.

Simplified architecture diagrams are shown in Fig. 2-1 and 2-2. Table 2-1 summarizes which architectures can and cannot be used with transistors of common types of inverters.

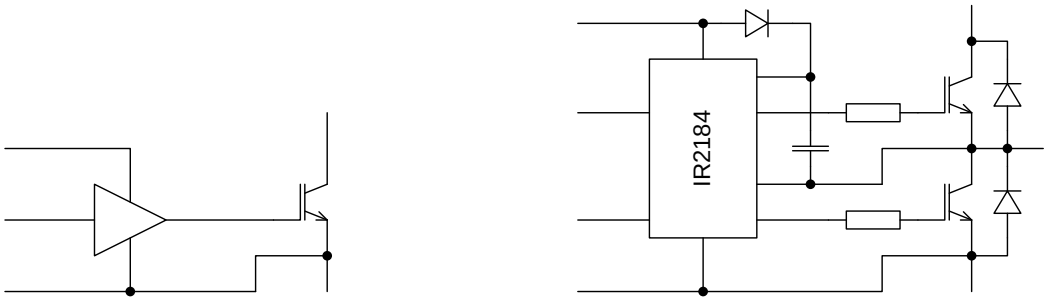


Figure 2-1: Non-isolated gate drivers: direct (left), with capacitive coupling (right)

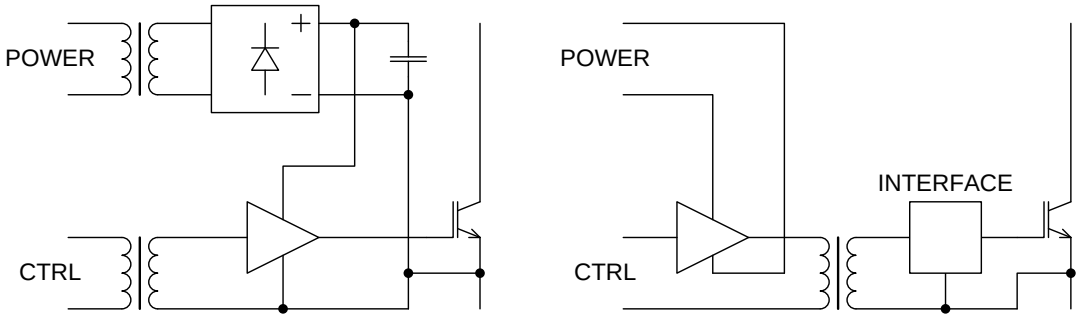


Figure 2-2: Gate drivers with isolation on: power and signal (left), output stage (right)

Table 2-1: Allowed gate driver architectures for use with inverter transistors

CONVERTER	TRANSISTOR	GATE DRIVER			
		NON-ISOLATED		ISOLATED	
		DIRECT (COMMON GND)	CAPACITIVE COUPLING (LEVEL SHIFT)	POWER SUPPLY & SIGNAL ISOLATION	OUTPUT STAGE ISOLATION
MULTI-LEVEL	ANY	☒	☒	☑	☑
2-LEVEL	HIGH-SIDE	☒	☑	☑	☑
	LOW-SIDE	☑	☑ (with high side)	☑	☑

For further classification it can be assumed that the non-isolated direct driver can make part of the isolated driver with power supply and input signal isolation. This research focuses on more detailed structure of the direct driver part, excluding the power supply and input signal isolation.

2.1.2. Classification by output stage

Depending on design scale, power switch type, and operating frequency, gate drivers can be classified by the type of output stage. Standard push-pull output stages can use either MOSFETs as switches, or BJTs as an amplifier to reproduce a pre-programmed voltage waveform (Fig. 2-3 a-b). More advanced resonant output stages use inductors to recover the switching control energy, especially for recharging power MOSFET gates with large input capacitance at high frequency. Examples of half-bridge and full-bridge inductor connection are shown in Fig. 2-3 c-d.

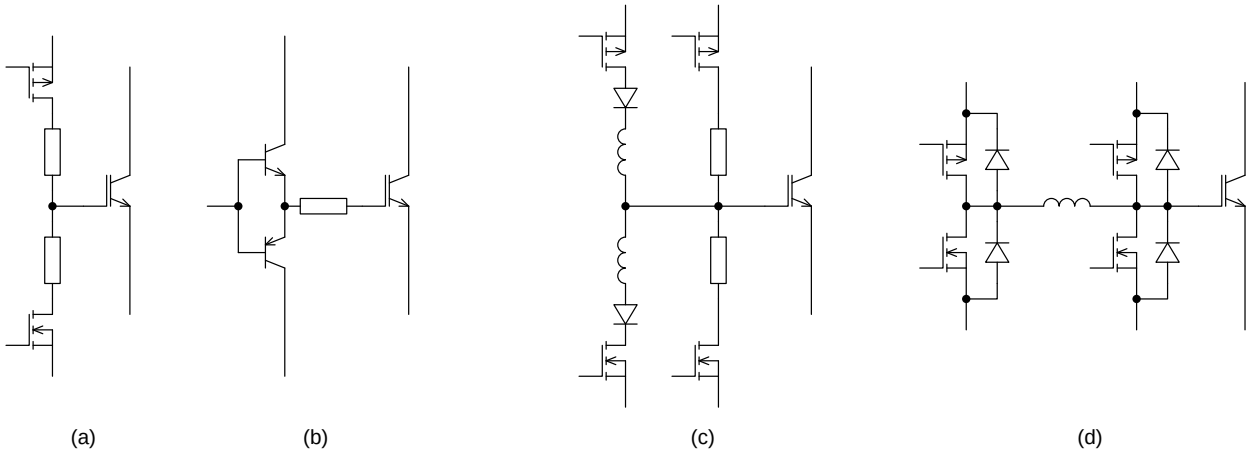


Figure 2-3: Gate driver output stages: push-pull (a)-(b), resonant (c)-(d)

Output stages can have other add-ons for increasing driving capabilities. Reference [3] describes a transformer-based add-on which assists the gate driver output stage by sending energy from the snubber to the gate in a positive feedback loop, thus increasing the gate current (Fig. 2-4). Other References [4-6] describe energy transfer between gates of power switches in applications where they always operate in a complementary mode.

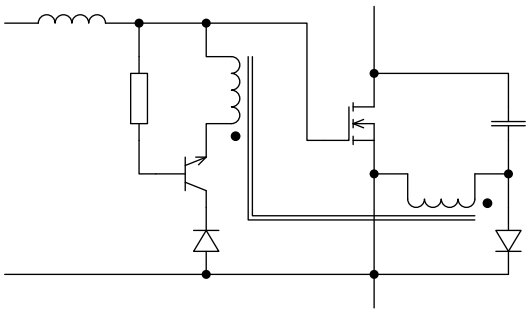


Figure 2-4: Gate driver add-on allowing energy transfer from snubber to gate

2.2. Converter loss measurement standards

Since gate driver performance is observed through the output of the switching circuit, there are no specific test conditions for all gate drivers. Each type of gate driver has to be appropriate for the ratings and speed grade requirements of IGBTs controlled. For a given IGBT/diode module or switching leg, different gate drivers could be compared in terms of power loss and efficiency of the converter. Most test results are obtained using a single value for voltage and current at which switching tests are performed. Those values are chosen arbitrarily and are usually around the half of device absolute maximum ratings.

2.2.1. Switching loss

Whatever the scales and types of switching devices are, and for any measurement conditions, the main switching loss expressions are defined according to the equations:

$$E_{ON} = \int_{t2}^{t1} V_{CE} I_C dt \tag{2.1}$$

$$E_{OFF} = \int_{t4}^{t3} V_{CE} I_C dt \tag{2.2}$$

where the events t_1 … t_4 are defined according to [27]:

- Leading edges (t_1 and t_3) are defined as where the rising parameter (voltage or current) reaches 10% of the final value.
- Trailing edges (t_2 and t_4) are defined as where the falling parameter (voltage or current) reaches 2% of the final value.

The typical waveforms are clearly demonstrated in Fig. 2-5.

2.2.2. Conduction loss

The conduction loss is defined as:

$$E_C = V_{CE} I_C (t_3 - t_2) \approx \int_{t3}^{t2} V_{CE} I_C dt \tag{2.3}$$

The integral is usually not evaluated in this case, since the current is considered constant between PWM transitions, and the rising and falling edges do not introduce significant errors.

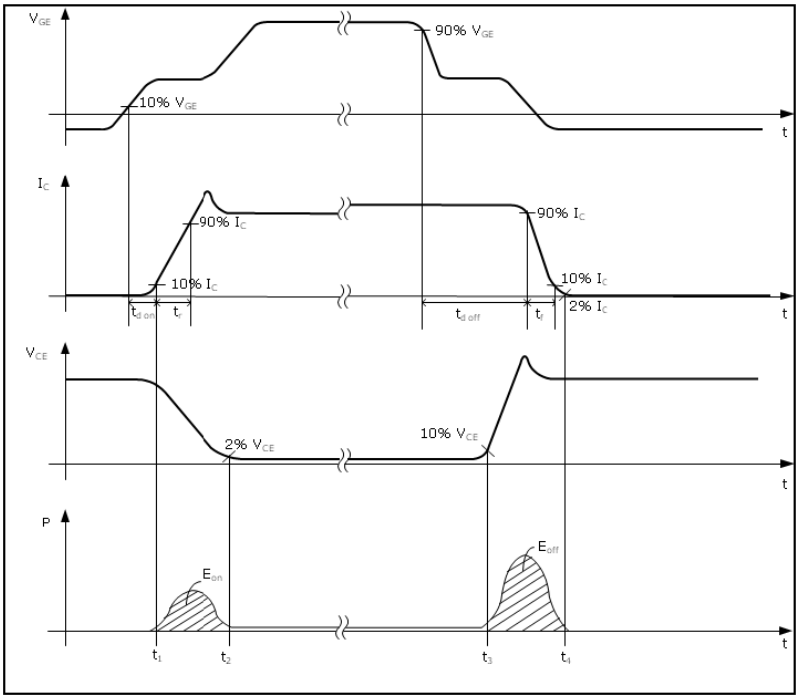


Figure 2-5: Switching and conduction loss definition waveforms and timings

2.3. Widely used IGBT and MOSFET models

In order to understand the advantages and disadvantages offered by various gate driver output stages listed above, this section presents the IGBT and MOSFET models with relevant key parameters which are necessary to consider for gate driver design. The models of IGBT and MOSFET in Fig. 2-6 include important parasitic effects, such as Miller capacitance, gate-emitter resistance and gate-emitter inductance [28].

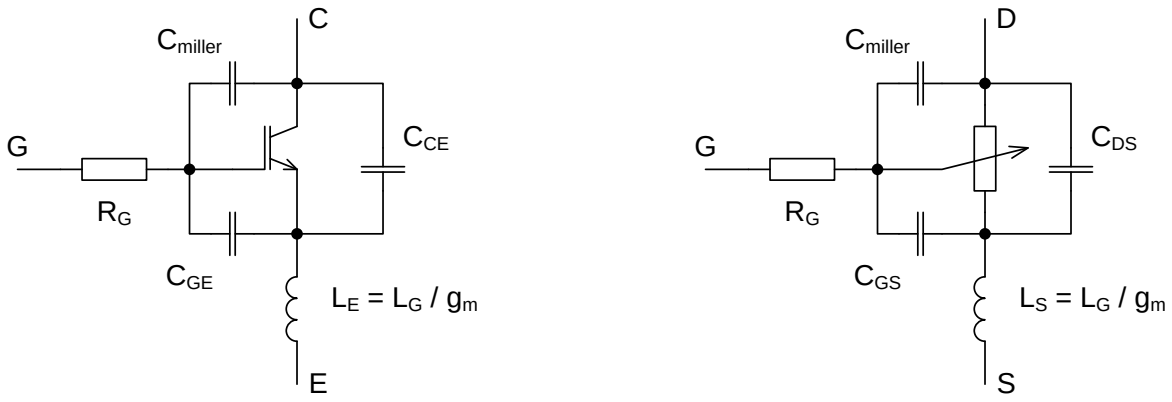


Figure 2-6: Equivalent circuits: IGBT (left), MOSFET (right)

It was mentioned earlier that recovery of driving energy is more important for MOSFET drivers than for IGBT drivers. This is because a MOSFET has an input gate capacitance about an order of magnitude larger than an IGBT having the same voltage and current ratings as the MOSFET. Nevertheless, even for IGBTs the primary input parameter is the gate-emitter capacitance.

In addition to the models represented with passive components, real devices also have maximum ratings:

- Maximum gate-emitter voltage
- Maximum collector-emitter voltage
- Maximum average current
- Maximum peak current
- Maximum switching time for given collector-emitter voltage and current

2.4. The history of IGBT gate driver development

2.4.1. Increasing driving capability and speed

The most basic and the first developed gate drivers work using push-pull techniques. The principle of operation assumes that the gate-emitter circuit is either a pure capacitor, or a series RC circuit. The switches are modeled as resistors, therefore making a first order low pass filter. That way, the gate is charged or discharged with a constant voltage. It follows from the power device transconductance curves that higher gate-emitter voltage leads to lower conduction losses. There is also a limit on the gate-emitter voltage magnitude. Exceeding it would cause the insulation breakdown, similar to a capacitor.

It is important to note that the gate-emitter voltage is allowed to be negative as much as positive, i.e. the gate capacitance behaves like a non-polarized capacitor. Another fact that follows from the transconductance curves is that the opening threshold voltage is around 2…3V for devices having ±20V gate voltage limit. If the gate was driven by a single-supply circuit having common ground with the emitter of the switching device, then dv/dt of the gate at the point of threshold would be much lower during discharge than during charge (Fig. 2-7). This observation is especially important when switching inductive loads because the turn-off usually involves higher currents than turn-on. It is preferable to have the device switched with the

highest possible speed in both directions (on and off). Therefore, using the fact that the threshold voltage is close to the middle of the operating range of the gate (in both directions), the gate should be pulled down to the most negative allowed voltage during turn-off, rather than simply discharging it to zero.

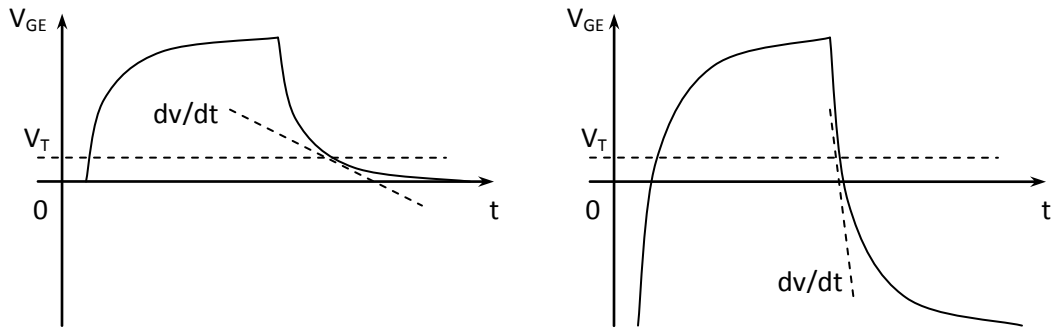


Figure 2-7: Gate charge / discharge process: to GND (left), to negative supply (right)

The next stage in development took necessary steps to reduce the time constant of the equivalent RC circuit of the gate by reducing the value of R, but there was a problem. The RC model did not account for the parasitic inductance present in the gate-emitter-driver loop. A part of this inductance is inside the power transistor, and the other part is due to the physical placement of the connecting tracks on the PCB or the connecting wires from the driver circuit to the power transistor. Now the model becomes a series RLC circuit, prone to oscillations if underdamped. This effect is called "gate ringing", and causes multiple gate recharge cycles after a single step change in the input voltage. This causes the power transistor to switch multiple times in the worst case, and remain in intermediate states between fully open or fully closed for a much longer period of time than expected with an RC circuit. The first solution to this problem was to experimentally estimate the optimal value of the external gate resistor, and even adjust it in place after the board has been built.

An important breakthrough came from the IEEE paper [7], which proposed to apply pre-calculated analog waveforms at the input of the equivalent RLC gate circuit, instead of step inputs. Since a step input introduces harmonics, the main goal was to reduce the harmonics while keeping the value of the gate resistor low, effectively avoiding the gate ringing effect. The problem with that design was that the external gate resistor still could not be completely

eliminated. It could only be reduced by a factor of a few times. And computing the best voltage waveform became an additional challenge to the industry, because the waveform had to be optimized for every single model of power transistor. In order to get the waveforms in practical implementations, a waveform generator was used, followed by a complementary pair of BJTs configured as a voltage follower.

The next important change in the topology of gate drivers was described in the IEEE paper [8], with the idea of completely eliminating the external gate resistor and exploiting the parasitic gate inductance as a main parameter (Fig. 2-8 left). Since the internal gate resistance and inductance are small, the idea was to introduce a series inductor in the gate path to create an LC resonant circuit with a small resistance and a high quality factor. The gate voltage during a switching transient took a shape of a half-cycle sinusoid between the minimum and the maximum values (Fig. 2-8 right). The advantage of this circuit as discussed in [8] is a significant reduction of losses due to gate recharging of MOSFETs, because they switch at higher frequencies than IGBTs and have much larger gate capacitances. IGBTs, however, can still benefit from this circuit because it reduces the gate recharge time, lowering the switching losses of the IGBT.

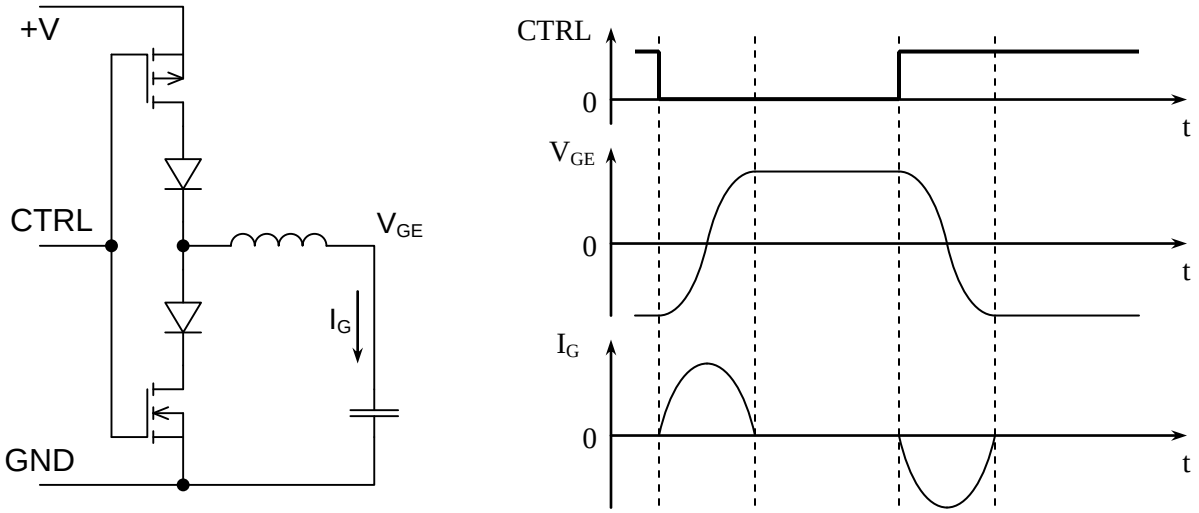


Figure 2-8: Resonant gate driver from [8]: schematic (left), waveforms (right)

The basic circuit has been improved and presented in the IEEE paper [9]. The objective was to regulate the energy compensation for the losses caused by gate recharging, in order to

make each recharge cycle reach the same final gate voltage. The solution has introduced control loops into the gate drivers, and the most typical arrangement of controlled switches is shown in Fig. 2-3 (d). It uses an H-bridge to charge the inductor with a controlled pulse duration and then to discharge it into the gate capacitance. Discharging the gate is performed by charging it with the opposite polarity in the same way. There exists a unipolar version of it, where the charging procedure is identical, but the discharge is done to ground (emitter) through a MOSFET only, without passing through the inductor. The disadvantage of these methods is that charge and discharge currents pass through two switching elements, which requires more pre-driving circuitry and imposes a lower limit on the maximum value of gate current. Also, the design of control loops is extremely challenging because of small time constants, especially if the power IGBT is to be driven at a high frequency.

The 2012 IEEE paper [10] proposes how to eliminate the control problem and to reduce the number of switches while providing bipolar control voltage to the gate. The topology uses a combination of a resonant driver and an active driver. The first is used to quickly charge or discharge most of the gate charge in the beginning of the pulse, and the latter is used to bring the final gate voltage to a defined value, thus compensating for the energy loss in the resonant charge transfer. The feedback control is not required anymore because the compensation is performed directly using a fixed value of voltage instead of time delay control, and happens at the end of the charge transfer rather than before it. The number of switches is reduced for each current path because it is possible to use the push-pull topology instead of an H-bridge. However, the practical implementation of the circuit in [10] uses very low-current BJTs to conduct both the compensation current and the resonant current. For driving high-power IGBTs, much higher currents are required. Other disadvantages of this circuit include:

- Each BJT has a diode in series with its collector to block the opposite current direction.
- The timing control is defined by RC delay chains, which causes slow commutation of BJTs.
- The inductor in the collector path of BJTs could be subject to forced commutation of BJTs, which could destroy the BJTs by inductive kickback effect.

This circuit needs more development to meet the requirements of driving high-power IGBTs and MOSFETs, and to practically outperform the previously developed topologies.

2.4.2. Implementing feedback control

In the last decade, important side effects of fast IGBT switching have been identified:

- IGBT current overshoot at turn-on due to reverse recovery of the complementary diode
- IGBT voltage overshoot at turn-off due to stray inductance of the loop through the module and the DC link capacitor

These two effects bring the IGBT close to its maximum ratings for short periods of time. The known nature of overshoots has allowed determining their approximate equations:

$$I_{rr} \approx \sqrt{Q_{rr} di/dt} \tag{2.4}$$

$$V_{OS} \approx -L_S di/dt \tag{2.5}$$

These equations demonstrate that the overshoots depend primarily on the rate of change of current in the main circuit, regardless of the gate driver type used. Therefore, many recent research papers [11-14] are based on overshoot limiting techniques using feedback control from di/dt through the IGBT.

The research objective of Ref. [11, 12] is to control di/dt and dv/dt during switching transients to obtain the desired overshoot. The proposed method of obtaining the variable gate drive signal consists of using a high-speed analog amplifier. The feedback loop also contains analog operational amplifiers, configured to implement the control transfer function developed in theory. One disadvantage of this approach is the gain-bandwidth limit of operational amplifiers, which might be too low to guarantee precise analog signals.

As described in [13, 14], shorter response time of digital circuits than settling time of analog circuits can improve timing performance. The gate driver output stage uses multiple gate resistor values, turned on and off by digital logic. The analog degree of freedom becomes the timing when each gate resistor is turned on or off. Lots of analog operational amplifiers are not required in this type of feedback. Instead, analog comparators or ADC (analog-to-digital converters) are used to feed the current and voltage signals to the digital controller.

Ref. [12] also provides an idea of switching speed control by the system controller by means of using a 2D PWM signal (Fig. 2-9), where the vertical amplitude of pulses sent from the controller to the gate driver determines the switching speed of every turn-on and turn-off transition. This transfers the complexity of gate driver design to the controller algorithm, but has other negative side effects of feedback loop length increase and loss of precision of analog signal magnitude when sent from the controller module to gate driver modules over long wires.

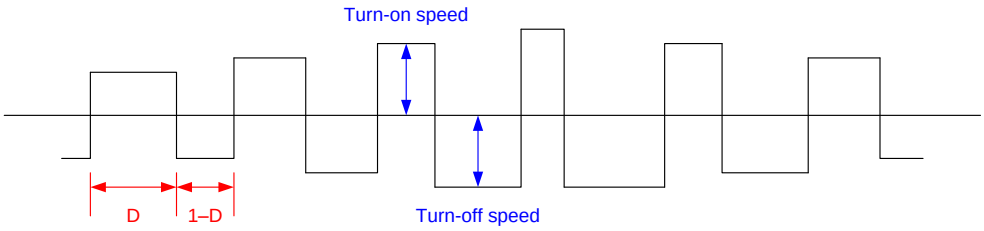


Figure 2-9: 2-D PWM signal

All feedback concepts described above require sensing of IGBT voltage and current. Measurements can be performed by the following methods, as described in [15]:

- Shunt resistor
- Current-sense IGBT with Kelvin emitter
- Rogowski coil
- Giant Magnetoresistive Sensor (GMR)
- Compensated voltage divider

Other feedback methods not requiring direct measurements of IGBT voltage and current can be applied for turn-off process only. The first method is a feedback Zener diode, directly mounted between IGBT's collector and gate. If IGBT voltage peak exceeds Zener voltage, current starts to flow from collector to gate, slowing down IGBT turn-off speed (Fig. 2-10 left). The second method is a Zener or TVS diode mounted directly between the emitter and the collector of the IGBT in order to limit the maximum voltage (Fig. 2-10 right). The problem with both methods is the requirement of physical location of the Zener diode close to the IGBT in order to reduce the inductance path in series with the Zener diode. These methods could only be effective if the Zener diodes were integrated into the inverter casing, which is not done in practice.

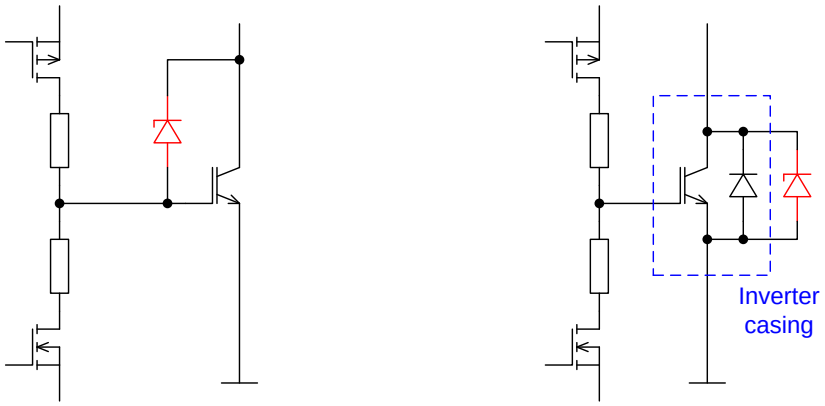


Figure 2-10: Zener diode feedback method (left), Zener diode clamp method (right)

2.4.3. Short-circuit protection

According to [18], a short circuit occurs when both low- and high-side IGBTs conduct current, typically when one of them is stuck ON, while the other one is driven ON by the gate control signal. As soon as the short-circuit condition occurs, the current through IGBTs and the DC supply linearly increases with no bound defined by system design. The rate of increase is defined by the IGBT module stray inductance, which prevents the current from becoming the short-circuit value instantaneously. One can differentiate between two possible ways of obtaining a short-circuit condition:

- Turning ON a functional IGBT, while the opposite is stuck ON
- An IGBT fails from the OFF state and becomes stuck ON, while the opposite is already ON

If the feedback control system has a current sensor, theoretically a short circuit could be detected by reading the current value. However, in most cases, the current is measured by applying integration on dv/dt across stray inductance, and thus can only be measured during the turn-on PWM transition, as in the situation when a working IGBT turns on into an existing short circuit. In the other case, when a short circuit happens in series with a working IGBT that's already on, the alternate method to detect it is to measure V_{CE}, which in the ON state is linked to I_C by the DC output characteristic curve of the IGBT device. As V_{CE} measurement is normally rated for the full voltage range across the IGBT, a more precise measurement of V_{CE} in the ON state can be obtained by using a desaturation diode in a separate circuit.

Chapter 3:
PSpice Inverter Model Design and Switching Process Simulations

3.1. Overview

The most popular and the most basic converter configuration for electric vehicle applications is the six-pack configuration, containing 6 IGBTs (2 per phase) and 6 anti-parallel diodes. This section focuses on creating a PSpice model of the 650V 800A converter module [29]. PSpice is a circuit simulator which supports both ideal components and complex nonlinear device models according to their governing equations. Using PSpice should reveal most electrical aspects of switching mechanics during turn-on and turn-off.

No model can be ever made to behave exactly as the physical device. In fact, even physical devices are slightly different from each other. The goal of this part of research is to create a model that replicates DC, AC, and switching characteristics provided in the device datasheet. The model should be more precise than generally accepted literature models, yet not computationally complex enough to create simulation problems.

3.2. Inverter modeling approach

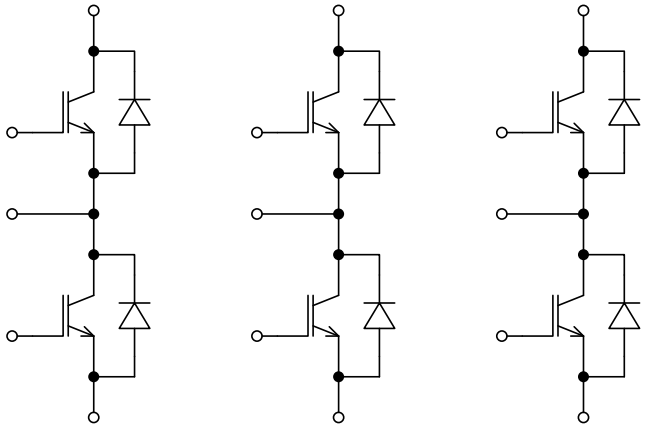


Figure 3-1: FS800R07A2E3 IGBT module schematic diagram

The converter module schematic is given in Fig. 3-1. Since the module contains three identical switching pairs, it is sufficient to create a model of one pair to investigate switching transients.

PSpice supports three kinds of models:

- Physical models: based on semiconductor sizes, position, and doping [17].
- Electrical models: based on built-in equations with configurable parameters.
- Behavioral models: based on user-defined equations between voltages and currents [18].

Physical models are usually the most precise models, but require knowing parameters of semiconductors set during the manufacturing process. Those parameters are never given in datasheets, which makes it impossible to use physical models. Even if some manufacturers do provide physical device models, those models represent a very high computational complexity for the simulator.

Electrical models are the most common models used for fast implementation in PSpice. They closely model the relationships between voltages and currents on device terminals. The simulator contains libraries of device parameters, and new libraries can be imported for new devices. However, PSpice does not contain the model for the inverter device [29], nor the manufacturer provides one.

Behavioral models are special circuit components in PSpice where the user can define custom relationships (equations) between voltages and currents of device terminals. This could extend the flexibility of electrical models, where the equations are hard-coded and cannot be changed.

The inverter datasheet, as most other datasheets, does not directly provide the values required by the device equations. It only provides graphs of dependence of one external variable on other one (or two) variables. The approach is therefore to create separate IGBT and diode models, first using electrical models, and then using behavioral models where the built-in equations are not flexible enough to closely replicate the performance graphs provided in the datasheet.

Device models can be broken up into the DC part and the AC (transient) part [19]. The DC model is nonlinear and is easily extracted by the device manufacturer, since most graphs provided in the datasheet cover the DC parameters. The AC models, however, model such parameters as capacitances between device terminals. Therefore, most of them are modeled linear first, and later could be changed to nonlinear if needed to enhance a certain parameter.

3.3. IGBT DC model

Earlier PSpice versions contained built-in electrical models for diodes, BJTs and MOSFETs only. The current PSpice version supports the new built-in IGBT device model, containing "five DC current components and six charge (capacitive) components" [30]. Unfortunately, the model schematic diagram contains too many parameters that need to be mapped on the datasheet parameters or on the physical device parameters. Methods that extract those parameters make use of special software and require various electrical tests to be performed on the physical device. Since the physical device is not available at the time, the only source of data is the datasheet. Therefore, an easier model is required, which follows directly from the most basic principle of operation of an IGBT (Fig. 3-2 left):

Figure 3-2: IGBT DC models: basic (left), simplified (right)

It follows from the basic model that the internal BJT can never go into saturation mode, even though the internal MOSFET can go into triode mode, because the MOSFET V_{DS} is always positive. Further assuming that the BJT DC current gain β is constant, the model can be simplified into the one in Fig. 3-2 right, because the BJT is always in active mode and acts as a current amplifier by β times. Being always in active mode is the reason why IGBTs turn off much faster than BJTs without desaturation diodes.

Let us recall the MOSFET equations:

$$I_D = \begin{cases} 0, \text{ if } V_{OV} \le 0 \\ K_P\left(V_{OV}V_{DS} - 0.5V_{DS}^2\right), \text{ if } V_{DS} \le V_{OV} \\ 0.5K_P V_{OV}^2, \text{ if } V_{DS} > V_{OV} \end{cases} \quad (3.1)$$

where $V_{OV} = V_{GS} - V_T$, also called the gate overdrive voltage. The datasheet provides the transfer characteristic (I_C vs. V_{GE} @ V_{CE} = 20V) and the output characteristic (I_C vs. V_{CE} @ several V_{GS}) curves. It follows that K_P and V_T parameters can be found from the transfer characteristic only. For K_P = 130 and V_T = 6.0V the transfer characteristic obtained (Fig. 3-3) closely matches the datasheet at 150°C (most data is provided for that temperature).

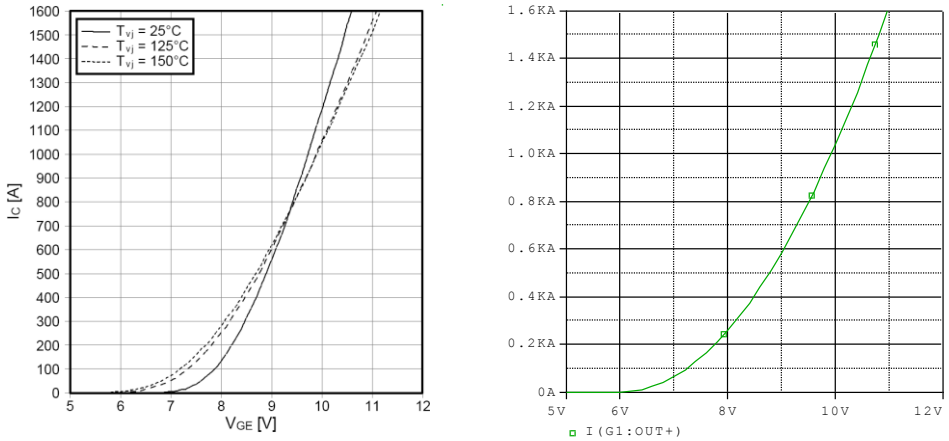


Figure 3-3: IGBT transfer characteristic (I_C vs. V_{GE} @ V_{CE} = 20V) comparison: datasheet (left), PSpice (right)

The series diode in the simplified IGBT model could be modeled using ideal diode equations with parameters I_S and N, but they turned out to be insufficient. The diode series resistance R_S needs to be added, which is represented by the connecting wire bonds in the physical device. But even the three parameters above are insufficient to replicate the output characteristic of the IGBT. The PSpice reference guide [30] reveals the missing parameter K_F (triode region factor), and provides IGBT transconductance equations. They look similar to MOSFET equations, but K_F modifies the curvature in the triode region, without affecting the maximum value of the current in the saturation region. Since the IGBT PSpice model could not be used due to lack of other parameters, the MOSFET was replaced with a behavioral model with these modified equations:

$$I_D = \begin{cases} 0, if\ V_{OV} \le 0 \\ K_F K_P \left(V_{OV} V_{DS} - 0.5 K_F V_{DS}^2\right), if\ V_{DS} \le V_{OV} / K_F \\ 0.5 K_P V_{OV}^2, if\ V_{DS} > V_{OV} / K_F \end{cases} \quad (3.2)$$

The four new parameters K_F = 1.7, I_S = 3A, N = 7, and R_S = 0.3 mΩ generate an output characteristic that closely matches the datasheet (Fig. 3-4):

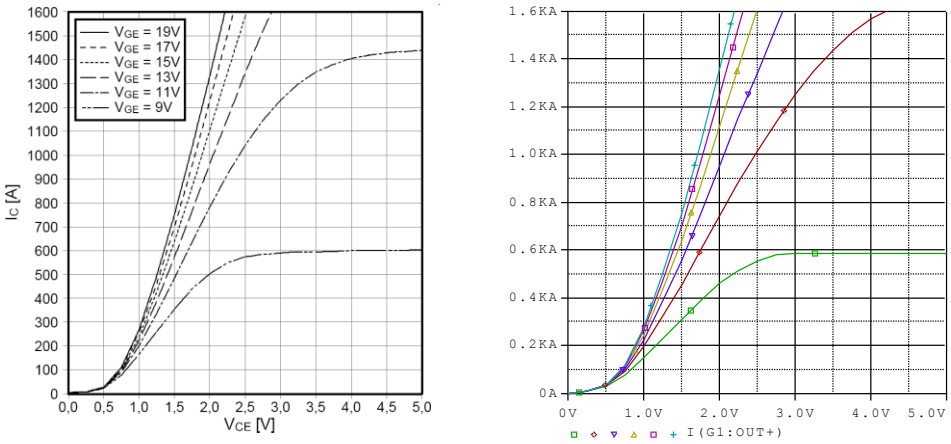


Figure 3-4: IGBT output characteristic (I_C vs. V_{CE}) comparison: datasheet (left), PSpice (right)

3.4. Diode DC model

Similarly to the model of the IGBT internal "diode", the reverse diodes have three main parameters: I_S, N, R_S. They relate to the diode forward voltage and current with the equation:

$$V = RI + NV_T \ln\left(I / I_S\right) \quad (3.3)$$

where V_T is the thermal voltage ≈25mV. It is different from 25mV at the modeling temperature of 150°C, but this degree of freedom is covered by the N parameter anyway. Since we have three unknowns, we need three points from the forward characteristic from the datasheet. The diode equation can be represented in the form of a 3 x 3 linear system, which simplifies the process of finding the parameters. One of the three linear equations (for one graph point) is:

$$V = (R)I + (NV_T)\ln I + \left(NV_T \ln(1/I_S)\right) \quad (3.4)$$

The values found are I_S = 0.43A, N = 5.5, R_S = 0.48 mΩ, and produce the result in Fig. 3-5. The voltage scale of the PSpice graph is negative because the test circuit also contained the IGBT, so the diode's anode was connected to GND.

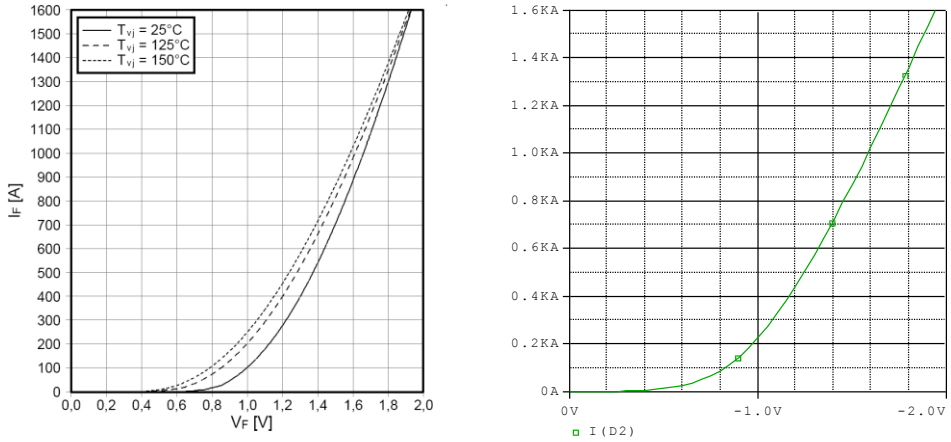


Figure 3-5: Diode forward characteristic (I_F vs. V_F) comparison: datasheet (left), PSpice (right)

3.5. IGBT AC model

3.5.1. Theory and calculations

The datasheet [29] provides "as is" three AC parameters of the IGBT: Gate capacitance C_{GE} = 52.0 nF, reverse transfer capacitance C_{GC} = 1.50 nF, and internal gate resistance R_G = 0.5Ω. It does not, however, provide two other important parameters: gate inductance L_G and collector-emitter capacitance C_{CE}. The gate inductance is important when using resonant gate drivers to calculate the quality factor of the RLC gate-emitter equivalent circuit. The collector-emitter capacitance is important to model switching transients, since it adds up to the reverse capacitance of the anti-parallel diode. The equivalent circuit of the IGBT AC model is shown in Fig. 3-6 below.

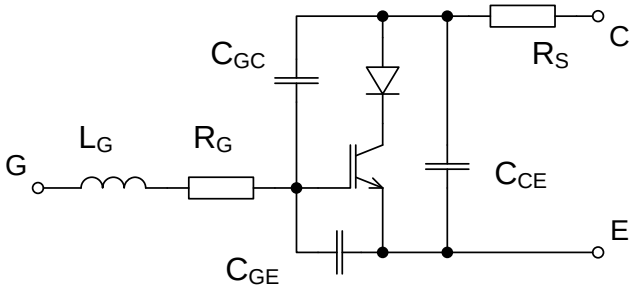


Figure 3-6: IGBT AC model

Experiments have shown that using linear models for the three capacitances (Fig. 3-6) is insufficient to accurately model switching transients. The datasheet [29] does not provide functions of capacitance vs. voltage. It only provides the three capacitance values at V_{GE} = 0V

and V_{CE} = 25V. The module uses IGBTs of type 3 (trench/fieldstop). The manufacturer provides capacitance curves for discrete IGBTs of type 3, as well as specific values for V_{GE} = 0V and V_{CE} = 25V. Discrete IGBTs are rated for a much lower current than modules, so the discrete device with the highest current has been selected for reference, rated for 600V 50A [31]. Furthermore, the manufacturer provides physical PSpice models for their discrete IGBTs. Even though they failed to converge in my implementation, examining the source code of the models revealed a lot of similarities between them. They are all based on the same sub-circuit, with the only difference in crystal area and gate resistor (3 examples) [32]:

```
*****************************************************************
.SUBCKT IGP50N60H3_L2 ano gate kat PARAMS: TJ = 27
LANO ano anol 5n
RLAN ano anol 100
LKAT katl kat 7n
RLK katl kat 100
XL75xxC anol gate katl L75XXC_L2h3a PARAMS: TJ = {TJ} Atotal = 0.2759 A = 0.19989 Rg = 1
.ENDS
*****************************************************************
.SUBCKT IGP30N60H3_L2 ano gate kat PARAMS: TJ = 27
LANO ano anol 5n
RLAN ano anol 100
LKAT katl kat 7n
RLK katl kat 100
XL75xxC anol gate katl L75XXC_L2h3a PARAMS: TJ = {TJ} Atotal = 0.1521 A = 0.1073 Rg = 1.5
.ENDS
*****************************************************************
.SUBCKT IGP20N60H3_L2 ano gate kat PARAMS: TJ = 27
LANO ano anol 5n
RLAN ano anol 100
LKAT katl kat 7n
RLK katl kat 100
XL75xxC anol gate katl L75XXC_L2h3a PARAMS: TJ = {TJ} Atotal = 0.1024 A = 0.0713 Rg = 2
.ENDS
*****************************************************************
```

Plotting the area vs. rated current gives nearly proportional relationships (Fig. 3-7):

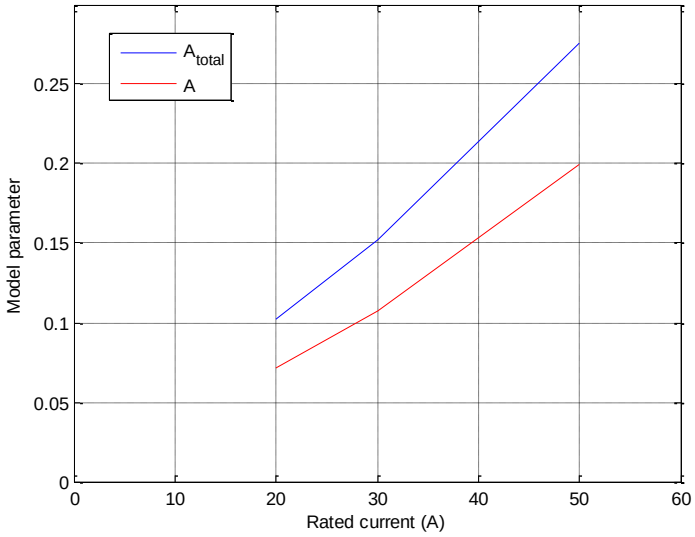


Figure 3-7: IGBT parameter scaling by rated current

This allows assuming that all capacitance curves could be scaled proportionally to the rated current, since the device area is also proportional to the current. Alternatively, they could be scaled by the ratio between reverse transfer capacitances of 800A module and 50A device.

It is important to note that the values provided in datasheets are not the internal capacitances, but rather the capacitances observed between each pair of device terminals (Fig. 3-8). For example, the measured capacitance between gate and emitter is not only C_{GE}, but also the series capacitance of C_{GC} and C_{CE}.

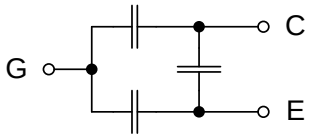


Figure 3-8: Approximate system of IGBT capacitances

That being said, a system of three equations can be set up:

$$\begin{cases} C_{iss} = C_{GE} + \left[1/C_{GC} + 1/C_{CE}\right]^{-1} \\ C_{oss} = C_{CE} + \left[1/C_{GC} + 1/C_{GE}\right]^{-1} \\ C_{rss} = C_{GC} + \left[1/C_{CE} + 1/C_{GE}\right]^{-1} \end{cases} \quad (3.5)$$

where C_{iss}, C_{oss} and C_{rss} are externally measured capacitances between G-E, C-E and G-C respectively. They are also called "input capacitance", "output capacitance" and "reverse transfer capacitance".

C_{CE} and C_{GC} originate from the PN junctions inside the IGBT and behave like diode reverse capacitance according to the equation [33]. The gate-emitter capacitance has a physical configuration similar to a capacitor, and is therefore almost linear. It is usually much larger than the other two capacitances, which allows simplifying the system of equations. If the curves for C_{oss} and C_{rss} are close to each other (which is the case for the 50A device), another simplification could be made: $C_{CE}(V_{CE}) = C_{GC}(V_{CE})$, and the system becomes symmetric:

$$\begin{cases} C_{iss} \approx C_{GE} + C_{CE}/2 \approx C_{GE} + C_{GC}/2 \approx C_{GE} \\ C_{oss} \approx C_{rss} \approx C_{CE} + C_{GC} \approx 2C_{CE} \approx 2C_{GC} \end{cases} \tag{3.6}$$

$$C_{GC} \approx C_{CE} \approx \frac{C_{oss} + C_{rss}}{4} \approx \frac{C_{oss}}{2} \approx \frac{C_{rss}}{2} \tag{3.7}$$

Having the approximate equations for C_{GC} and C_{CE}, the nonlinear parameters K, V_D and M can be derived by either solving a system of three nonlinear equations using three points of the capacitance curves C_{oss} and C_{rss}, either using more graph points with a curve-fitting algorithm. The values for the 50A IGBT obtained using a system of three equations are: K = 210 pF, V_D = 0.35V and M = 0.43.

To verify that the scaling principle still applies, there is one capacitance value given for the 800A module: C_{rss} = 1500 pF @ V_{GE} = 0V and V_{CE} = 25V. For the discrete 50A device the same parameter is C_{rss} = 96 pF @ V_{GE} = 0V and V_{CE} = 25V. The ratio is equal to 15.625, which is close to the ratio of their rated currents: 800A / 50A = 16. Therefore, the parameters for the module are: K = 210 pF * 15.625 = 3281 pF, V_D = 0.35V and M = 0.43.

3.5.2. Implementation

PSpice does not have a variable capacitor for which it is possible to set the capacitance as a function of voltage directly. In theory it would be possible to exploit the reverse capacitance function of the diode model, using its parameters C_{JO}, V_J and M [30]. However, the

problem in using a diode is that voltages of both polarities could be present across internal IGBT capacitances during switching transients. A diode would conduct in one direction, while the variable capacitances actually stay at the highest capacitance value in that direction and do not conduct DC current. Therefore, behavioral models are required, where custom equations relating voltage and current can be programmed.

We know the capacitance as a function of voltage, and we need to transform it into current as a function of voltage. The derivation follows below:

$$C = K\left(v + V_D\right)^{-M} = \frac{dq}{dv} \qquad q = \int_0^V C\,dv \qquad i = \frac{dq}{dt} = \frac{d}{dt}\left(\int_0^V C\,dv\right) \qquad \text{(3.8) – (3.10)}$$

$$q = \int_0^V K\left(v + V_D\right)^{-M} dv = \frac{K}{1-M}\left(v + V_D\right)^{1-M}\Big|_0^V = \frac{K}{1-M}\left(\left(v + V_D\right)^{1-M} - \left(V_D\right)^{1-M}\right) \qquad (3.11)$$

$$i = \frac{d}{dt}\left(\frac{K}{1-M}\left(\left(v + V_D\right)^{1-M} - \left(V_D\right)^{1-M}\right)\right) = \frac{K}{1-M}\frac{d}{dt}\left(\left(v + V_D\right)^{1-M}\right) \qquad (3.12)$$

The function of the behavioral block should include two cases for each voltage polarity. This is easily programmed using an IF operator, but computationally there should be absolutely no step change in the current during zero-crossing, so the calculated constants have to be programmed with all significant figures available. The capacitance used as the linear value in the reverse direction is the capacitance at V = 0 using the nonlinear equation. The final expression for C_{CE} and C_{GC} behavioral blocks is:

```
IF(V(%IN+, %IN-) < 0, 5.152962374n * DDT(V(%IN+, %IN-)), 5.756140351n * DDT((V(%IN+, %IN-)
+ 0.35) ** 0.57))
```

A few other adjustments were made in the simulation circuit. These include:

- Stray inductances were brought to values specified in the datasheet.
- A step change in C_{GE} was introduced at 8.5V to model the Miller plateau [34, 35]:

```
IF(V(%IN+, %IN-) < 8.5, 52n * DDT(V(%IN+, %IN-)), 150n * DDT(V(%IN+, %IN-)))
```

- External gate resistors were increased.

The resulting simulation circuit is provided in the Appendix A, including expressions of behavioral blocks and PSpice model descriptions used.

3.6. Diode AC model

A diode's most important transient behavior is the reverse recovery. It could be modeled by a reverse capacitance dependent on reverse voltage [33]. During transient tests almost all of the reverse recovery energy was released back into the circuit during turn-on of the diode, which is usually not the case for real devices.

A better reverse-recovery model is proposed in [20]. It replaces the reverse capacitance and requires a voltage-controlled current source, which is again modeled as a behavioral block. More importantly, the paper describing this model provides equations to obtain the model parameters from those given in most datasheets. The schematic diagram of the model is shown below in Fig. 3-9.

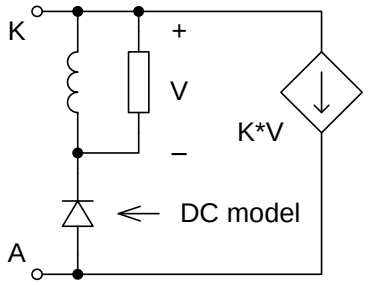


Figure 3-9: Diode reverse recovery model

The equations relating the datasheet parameters to the model parameters are:

$$L << \frac{V_F}{dI_F/dt} \qquad \frac{L}{R} = \tau = \frac{1}{\ln 10}\sqrt{\frac{Q_{rr}}{dI_F/dt}} \qquad K = \frac{1}{L}\sqrt{\frac{Q_{rr}}{dI_F/dt}} \qquad (3.13) – (3.15)$$

The first inequality is needed to set L to a value small enough to affect the voltage across the DC model of the diode during the maximum rate of change of current, which is provided in the datasheet. Reference [20] explains the use of L as a timing coil, also used to sense the rate of change of current.

In order to validate this model, a test circuit has been set up, containing the IGBT AC model with unknown parameters L_G and C_{CE} set to zero, in series with the diode AC model above. The test involved applying a DC current through the diode, and then turning the IGBT on, while the specified voltage is applied across the diode and the IGBT (Fig. 3-10).

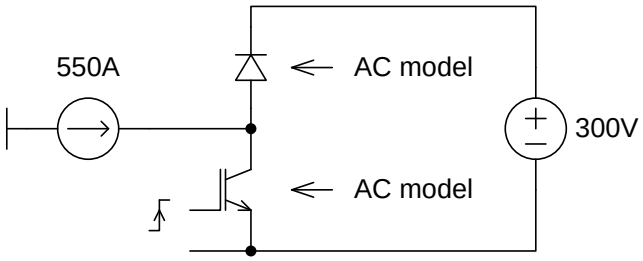


Figure 3-10: Test circuit for the diode reverse recovery model

With the calculated values of K, L and R, the reverse recovery energy did not match the datasheet value, although the reverse recovery charge did. Adjusting R in this model affects the energy and time, but has almost no effect on the charge. After tweaking the value of R to 50 μΩ and leaving the calculated values of L = 10 pH and K = 9000, the reverse recovery charge and energy match the datasheet values. The reason why the values of L and R are so small is, again, because they are used as sensing elements. The reverse recovery current waveform is shown in Fig. 3-11. The peak value of 231A is off by ≈15% from the datasheet value of 200A.

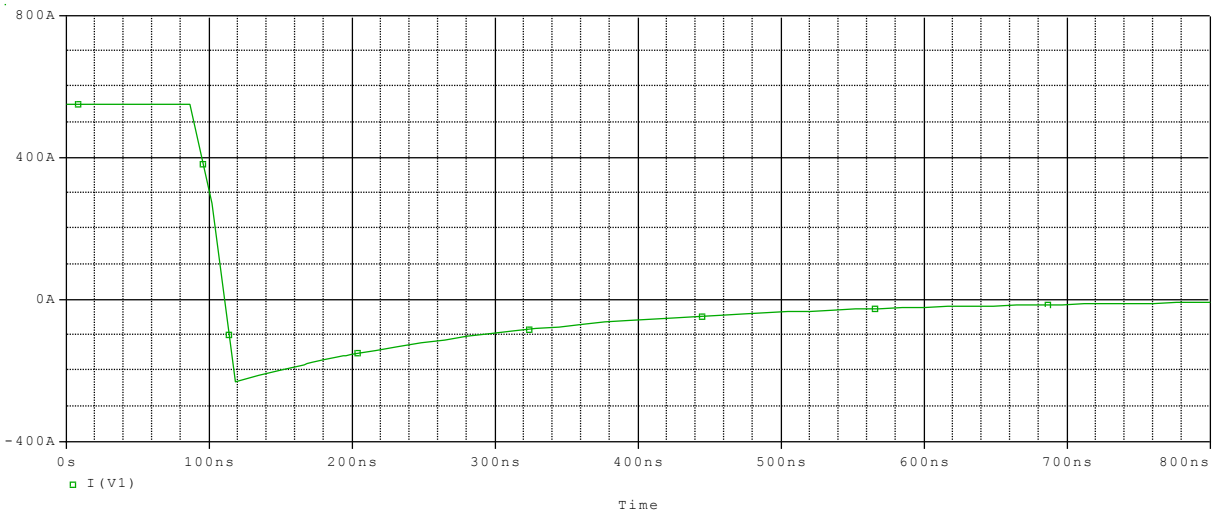


Figure 3-11: Diode reverse recovery current

3.7. Switching process simulation results

After making all adjustments, switching tests have been performed at a single value of DC link voltage (300V) for different values of load current and for different values of gate resistors. Switching waveforms for a single value of load current and gate resistor are shown in Fig. 3-12.

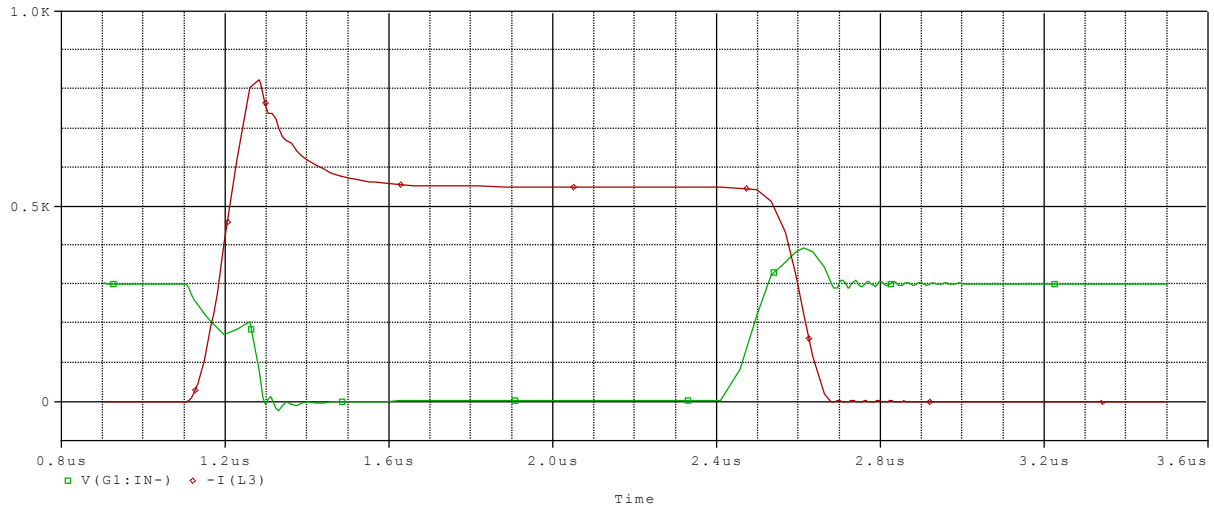


Figure 3-12: Output voltage (green) and current (red) waveforms with nominal gate resistors found in simulation

The waveform clearly shows the diode reverse-recovery current during turn-on and voltage overshoot during turn-off. The next graphs in Fig. 3-13 show how losses and overshoots depend on the gate resistor value.

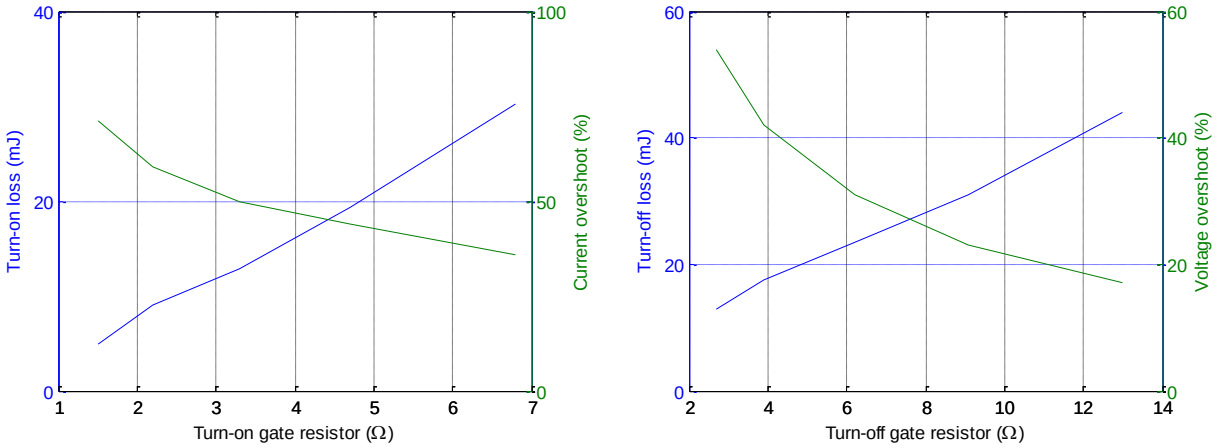


Figure 3-13: IGBT loss and overshoot: turn-on (left), turn-off (right)

The graphs confirm the literature results where the main idea is that driving the IGBT through a resistor in a way to reduce losses leads to increase of overshoots, which in turn decreases reliability due to approaching to device maximum ratings. But a typical inverter driving a motor does not always operate with the same value of current in the load. Considering the slow sinusoidal waveform of the load current (slow comparing to gate driver timings), we

can state that for at least 50% of the time the inverter does not operate at values of current close to maximum. This creates more room for overshoot closer to zero-crossings, and therefore switching can be performed faster with lower losses. The next Fig. 3-14 shows switching waveforms for four levels of load current.

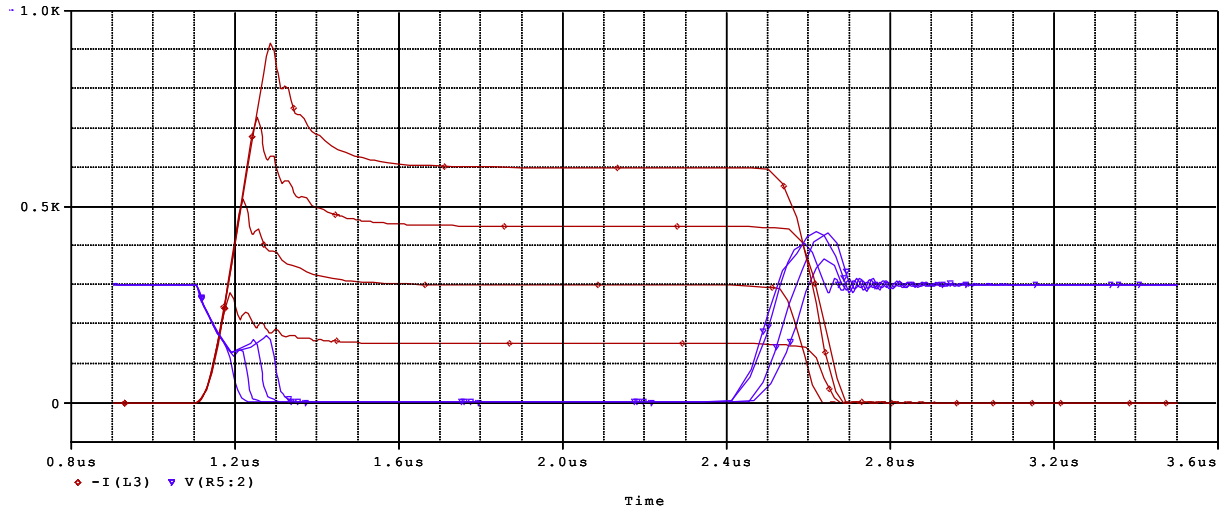


Figure 3-14: Simulated switching waveforms of 800A inverter for load currents of 150A, 300A, 450A and 600A

Chapter 4:
Hardware Testing of Gate Driver Output Stages in Open-Loop

4.1. Double-pulse experimental setup

For the purposes of better understanding switching mechanics, and to develop a gate driver output stage that could reduce switching losses, taking into account the effects of small time scale on circuit design, a double pulse test circuit [21] with 300V 20A ratings has been implemented. Effects of many output stages on switching losses are compared in this chapter.

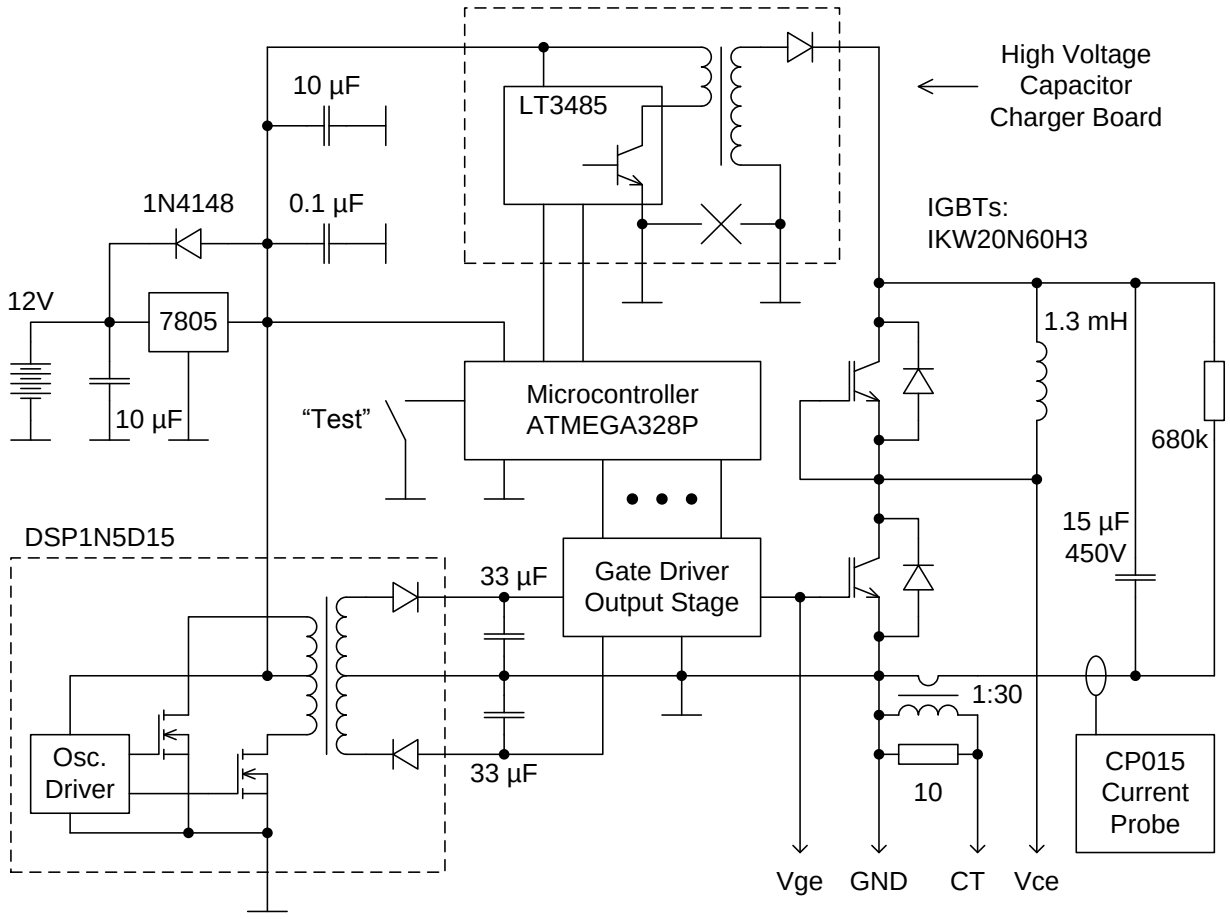


Figure 4-1: Implemented double pulse test circuit

After applying multiple modifications to the initial design, various types of gate driver output stages have been tested in place shown in Fig. 4-1. One of such modifications is marked with "X" in the high voltage capacitor charger board, which consists of cutting a PCB track in order to avoid a ground loop. The individual sub-circuits of output stages and their test results are presented in the next sections.

The double-pulse circuit consists of one IGBT switching leg made of two discrete IGBTs with built-in reverse diodes, rated for 600V 20A [36], storage capacitor of 15 µF, load inductor of 1.3 mH implemented on a 100 ft roll of wire with air core, high voltage capacitor charger board, symmetric ±15V gate driver power converter DSP1N5D15 [37], and microcontroller ATMEGA328P [38]. The IGBTs have been chosen to meet the test circuit ratings, and are made by the same manufacturer as the full-scale module. The collector-emitter voltage (V_{CE}) of the low side IGBT, its collector current (I_C) and gate-emitter voltage (V_{GE}) are monitored with a digital storage oscilloscope using the "single" acquisition mode initiated from a level trigger on the second falling edge of V_{CE}. The double pulse test pattern is generated by the microcontroller with microsecond precision upon closing the contacts of a switch connected to it, after charging the high voltage capacitor. The voltages V_{CE} and V_{GE} are monitored with 10x probes, while the current I_C is monitored with the current probe CP015. The second method of peak current measurement has also been implemented on a 30:1 current transformer. One feature not shown in Fig. 4-1 is the TTL-level serial connection to a computer, used to set the first pulse width and therefore the load current at which to perform the switching test.

A double-pulse sequence consists of the following steps, timed by the microcontroller:

- ATMEGA328P sends LT3485 [39] a signal to charge the 15 µF capacitor with pulses through the transformer on the charger board.
- When charged to 300…330V, LT3485 sends a "charge complete" signal back to ATMEGA328P. Then low-side IGBT is turned on, linearly increasing load current.
- After a preset delay, the current reaches a target value, and IGBT is turned off. This is where the turn-off waveforms are captured.
- Current then flows through the opposite diode, decaying very slowly. Shortly after, the IGBT is turned on again and the turn-on waveforms are captured.
- Shortly after, the IGBT is turned off for the last time to allow the inductor current slowly decay to zero through the opposite diode.

4.2. Switched-resistor output stage

The first output stage that has been tested is the switched-resistor push-pull circuit. It has been implemented to verify the effect of changing gate resistor value on switching loss and overshoot. The circuit is shown in Fig. 4-2.

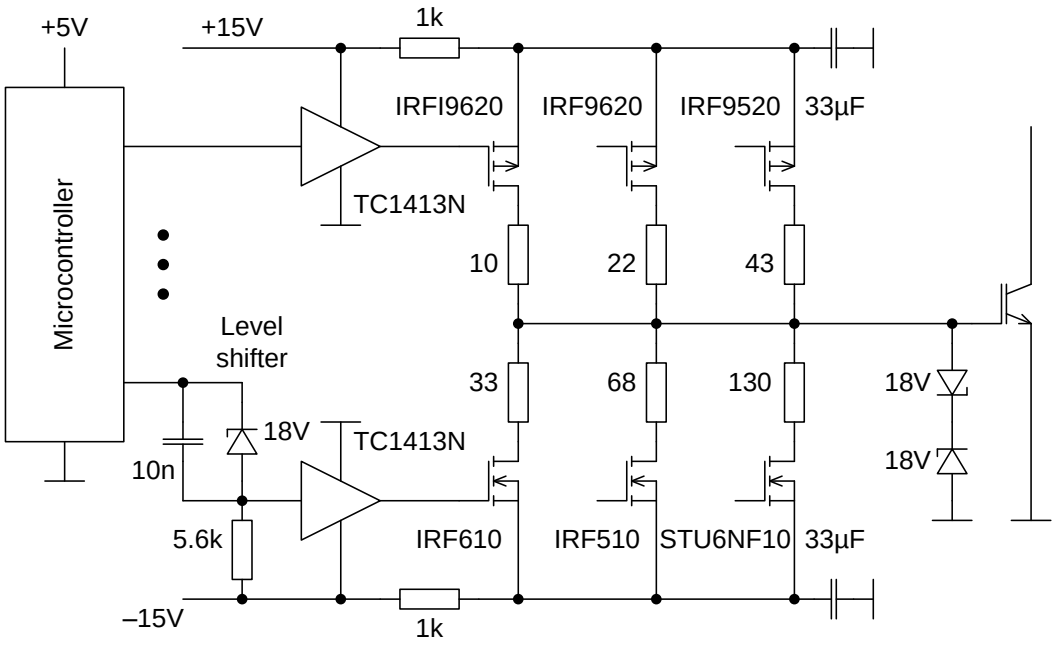


Figure 4-2: Multiple switching speed gate driver

Different speeds are obtained by 7 possible combinations of pull-up and pull-down MOSFETs being either ON or OFF. For example to obtain turn-on speed 3, all pull-down MOSFETs are turned off, as well as pull-up MOSFET in series with the 10Ω resistor, while the MOSFETs in series with resistors 22Ω and 43Ω are ON. The resistor ratios are approximately 1:2:4 in both pull-up and pull-down branches, which results in parallel addition of conductivity in proportion of 4:2:1, allowing almost linear distribution of switching speeds, as seen from Figures 4-3 and 4-4. The MOSFETs are driven by push-pull MOSFET drivers of a smaller size (TC1413N) and with lower supply voltage (15V instead of 30V). The low side drivers require level shift of voltage, which is performed by 18V Zener diodes with capacitive compensation for response time improvement.

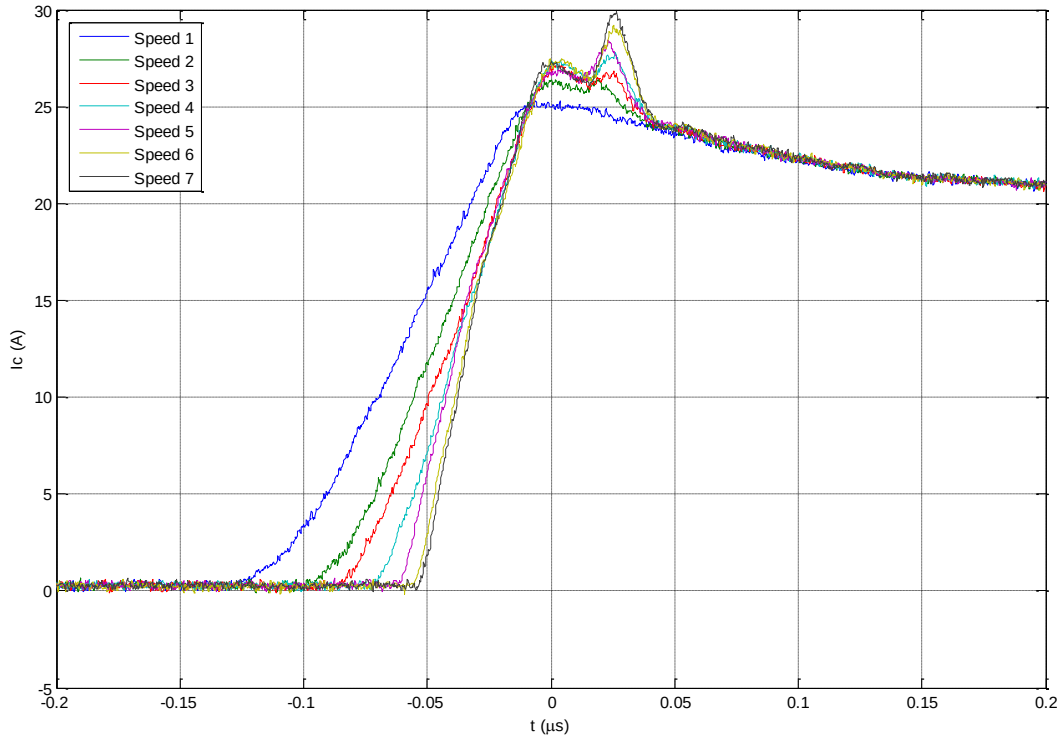


Figure 4-3: Turn-on currents for 7 possible turn-on speeds

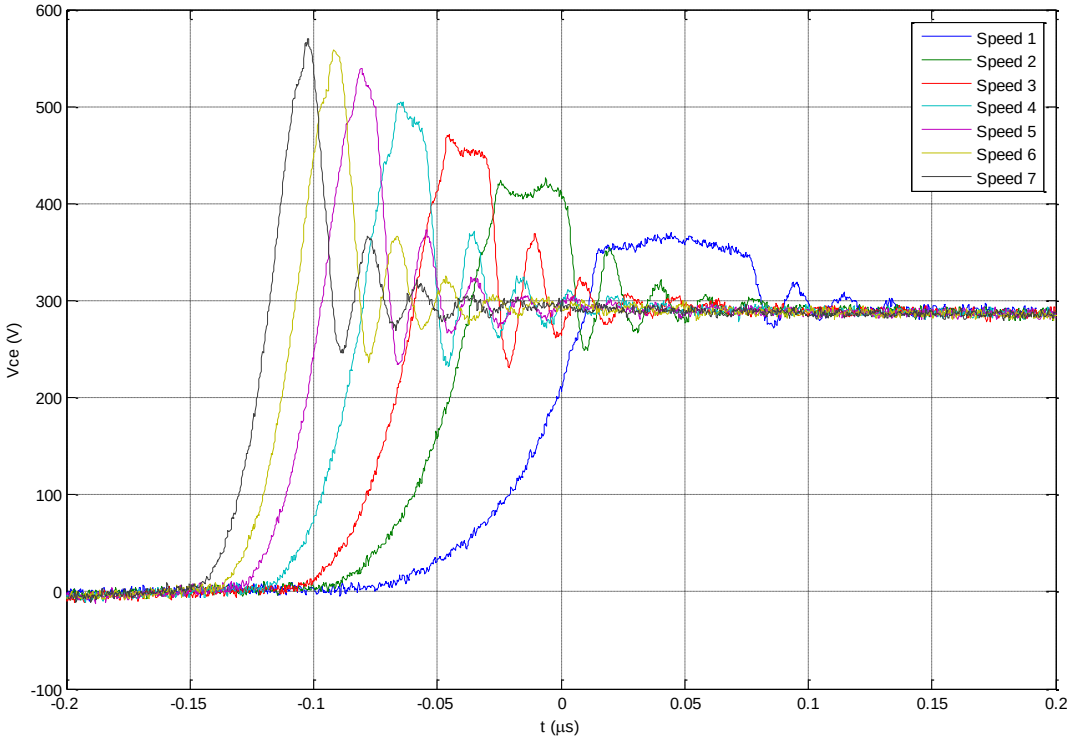


Figure 4-4: Turn-off voltages for 7 possible turn-off speeds

4.3. Dual-stage switched-resistor output stage

4.3.1. Dual-stage switching principle

As Ref. [14] mentions, the purpose of dual-stage switching is to split the IGBT gate control in two time stages, where the first stage uses a lower equivalent gate resistance than the second stage. The first stage has duration on the order of tens or hundreds of nanoseconds. This suggests a total of 4 states for every switching cycle (Fig. 4-5):

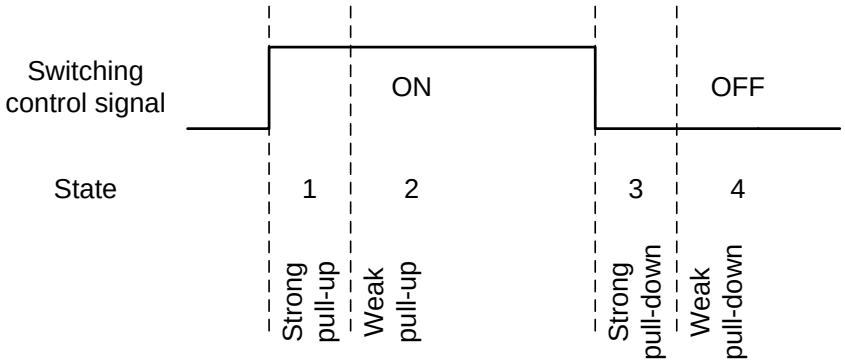


Figure 4-5: Dual-stage turn-on and turn-off state diagram

The duration of states 1 and 3 needs to be timed with high precision in order to choose the optimal point in time to change the equivalent gate resistance. States 2 and 4 are "steady states" and last until the next switching command from the system controller (Fig. 4-6).

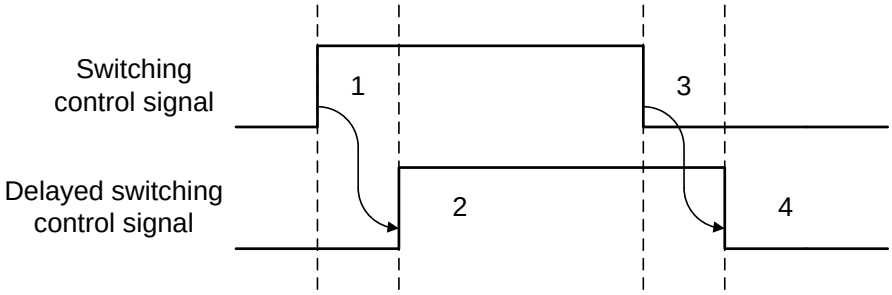


Figure 4-6: Generation of 4 switching states per cycle

A gate array logic (GAL) chip was introduced into the circuit in order to transform input signals into MOSFET control signals much faster than a microcontroller can do. The circuit for delaying the control signal is shown in Fig. 4-7. RC delay chain and a comparator are used to generate delays according to the equation: $t = RC \ln 2$.

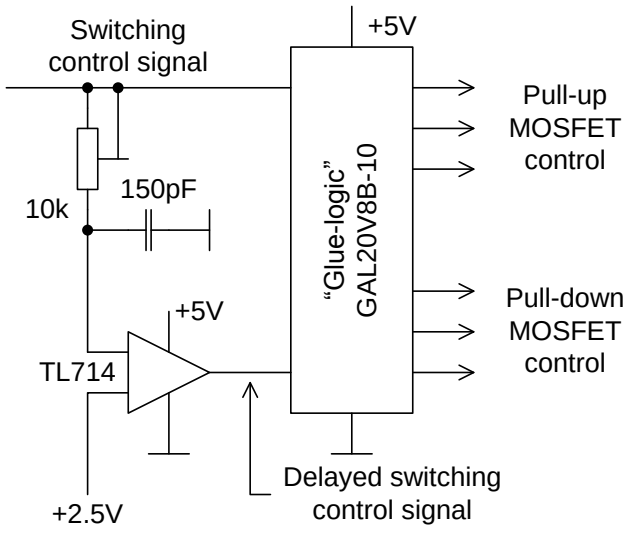


Figure 4-7: Circuit for variable delay generation from control signal, including GAL chip connection

4.3.2. Logic equation derivation for GAL chip

The dual-stage switching principle implies a step increase in gate resistance between the two stages. The first stage can be fixed to the lowest resistance (highest switching speed), and the second stage resistance can be programmed using 3 logic inputs to the GAL chip to set one of 7 possible speeds. Since both input speed setting and output MOSFET control signals are binary coded, the logic of the GAL chip can be split into 3 equivalent subcircuits for each of the 3 binary lines, having common input switching control signal and its delayed copy. The truth table is shown in Table 4-1, keeping in mind that pull-up MOSFETs need inverted control signals.

Table 4-1: Truth table for each binary line for GAL chip

SPEED_SET	CTL	DELAYED_CTL	PULLUP	PULLDN	PULLUP_OUT	PULLDN_OUT
0	1	0	ON	OFF	0	0
0	1	1	OFF	OFF	1	0
0	0	1	OFF	ON	1	1
0	0	0	OFF	OFF	1	0
1	1	0	ON	OFF	0	0
1	1	1	ON	OFF	0	0
1	0	1	OFF	ON	1	1
1	0	0	OFF	ON	1	1

Note that the sequence of signals "CTL" and "DELAYED_CTL" is listed according to the sequence of switching states 1 – 4 for easier representation. Using Karnaugh maps, the following equations can be derived for pull-up and pull-down MOSFET control outputs:

PULLUP_OUT = /CTL + /SPEED_SET * DELAYED_CTL (4.1)

PULLDN_OUT = /(CTL + /SPEED_SET * /DELAYED_CTL) (4.2)

4.3.3. GAL chip programming

The chip from the parts list, ATF22V10C-7 [40] from Atmel, could not be programmed with Stager Electric G540 Programmer-Tester [41] even though the chip is in the supported device list, most likely due to a hardware or software bug. The chip was replaced by another one, GAL20V8B-10 [42] from the original manufacturer Lattice Semiconductor, which has no problems with programming by G540. This chip has a lower amount of I/O lines and 10 ns maximum propagation delay comparing to Atmel's 7 ns.

According to an online guide on GAL chip programming [43], logic equations are associated with device pins in a .EQN file and then converted to a JEDEC (.JED) file by OPALjr PLD Development Package [44]. The .EQN file for gate driver implementation incorporates 3 sets of derived logic equations, 2 for each bit:

```
; 4-STATE 3-BIT DUAL SPEED SWITCHING

CHIP mux G20V8
nc=1    nc=2    nc=3    nc=4    nc=5    nc=6    del=7   ctl=8   sw1=9   sw2=10  sw3=11  gnd=12
nc=13   nc=14   pd3=15  pu3=16  pd2=17  pu2=18  pd1=19  pu1=20  nc=21   nc=22   nc=23   vcc=24

EQUATIONS
pu1 = /ctl + del * /sw1
pu2 = /ctl + del * /sw2
pu3 = /ctl + del * /sw3
pd1 = ctl + /del * /sw1
pd2 = ctl + /del * /sw2
pd3 = ctl + /del * /sw3
```

The GAL20V8B-10 datasheet [42] specifies that the outputs can be inverted, but this function is not supported by the compiler, so the JEDEC file with fuses had to be edited manually after compiling. Also, the generated JEDEC file was not properly read by the programmer software because the missing fuse information was interpreted by the

programmer as zeros, meaning "programmed", "connected", even though unprogrammed areas were selected to be filled with ones. In order to override this bug, a template JEDEC file has been created for GAL20V8B-10 with all fuses set to defaults, and comments were added on what certain lines of bits meant. To create the necessary JEDEC file, the lines in the template file were replaced with lines from the compiled JEDEC file. The resulting file was fed to the programmer.

4.3.4. Results

The dual-stage switching was mainly tested with the first stage speed hard-coded to 7, and the second stage speed was varied from 1 to 6. For second stage speeds between 2 and 6 the effect is less observable than for second stage speed 1. The first stage duration was adjusted manually to observe the effects.

For turn-on, the method suppresses the current overshoot as expected, but at the expense of raising the voltage for a longer duration, which results in a more energy loss compared to switching at the appropriately selected single speed. Fig. 4-8 right shows the voltage increase, comparing to switching at single maximum speed (Fig. 4-8 left).

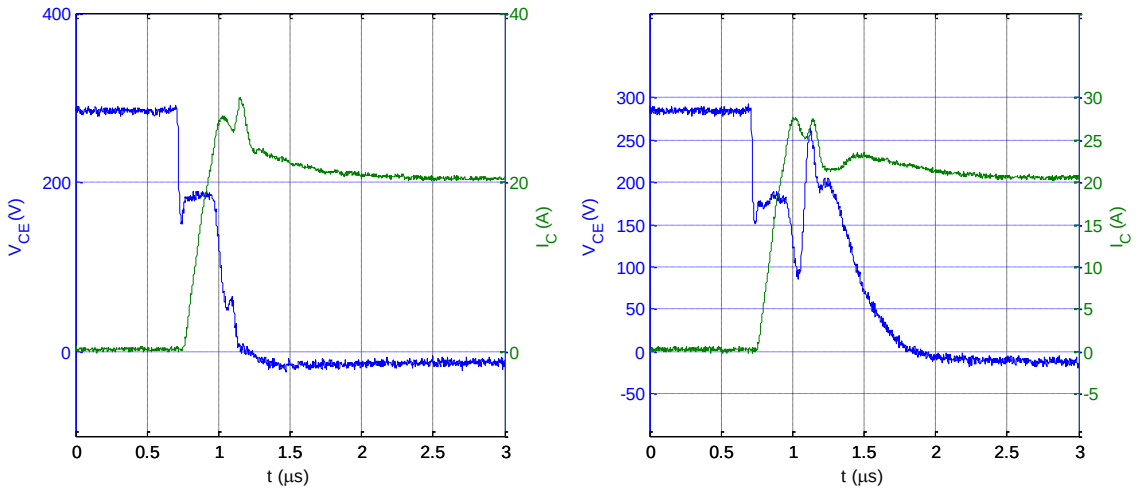


Figure 4-8: Turn-on waveforms: at speed 7 (left), with speed change from 7 to 1 (right)

For turn-off, the method suppresses the voltage overshoot as expected, and results in a decrease of energy loss, however the switching waveforms do not show the moment of speed change. By adjusting the duration of the first stage, the overshoot can be gradually adjusted,

unlike using discrete gate resistances. The turn-off performance of dual-stage switching is shown in Fig. 4-9 right, comparing to single-stage at maximum speed (Fig. 4-9 left).

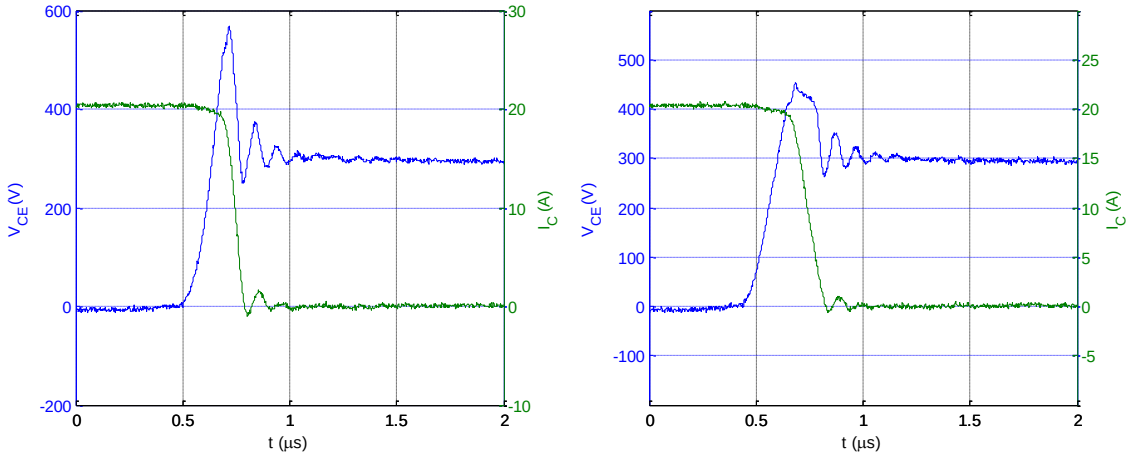


Figure 4-9: Turn-off waveforms: at speed 7 (left), with speed change from 7 to 1 (right)

During turn-on, if the first stage duration is increased, the switching process is the same as at single speed 7. If it is decreased, the switching process is the same as at single speed 1.

During turn-off, if the first stage duration is increased, the switching process gradually increases up to the equivalent of single speed 7. If it is decreased, the switching process gradually decreases down to the equivalent of single speed 1. This might create an additional degree of freedom for feedback control of turn-off voltage overshoot.

The dual-stage switching is only beneficial for turn-off because it cannot influence the reverse-recovery of the diode across the opposite IGBT. For turn-off, this method creates a possibility of using feedback control to choose the point in time when the switching speed can be decreased in order to obtain the desired value of voltage overshoot across the IGBT.

4.4. Multi-stage resonant (inductive) output stage

4.4.1. Resonant gate driver principle

The previous multi-speed gate driver circuit has been modified to convert a pair of resistive branches into a pair of inductive branches, which form a resonant circuit with the gate-emitter capacitance of the IGBT (Fig. 4-10). This method can be seen as capacitor voltage reversal around a reference voltage, which is typically zero, but can be slightly adjusted for the

turn-on branch. During capacitor voltage reversal process, some energy is lost in resistive elements, so the voltage after reversal is not fully restored. To compensate for this, weak resistive branches are engaged after the resonant ones, and keep pulling the gate up or down in steady state. Inductor values were calculated from the gate capacitance and from the required peak gate current, taken as several times the nominal gate current for the datasheet gate resistor value.

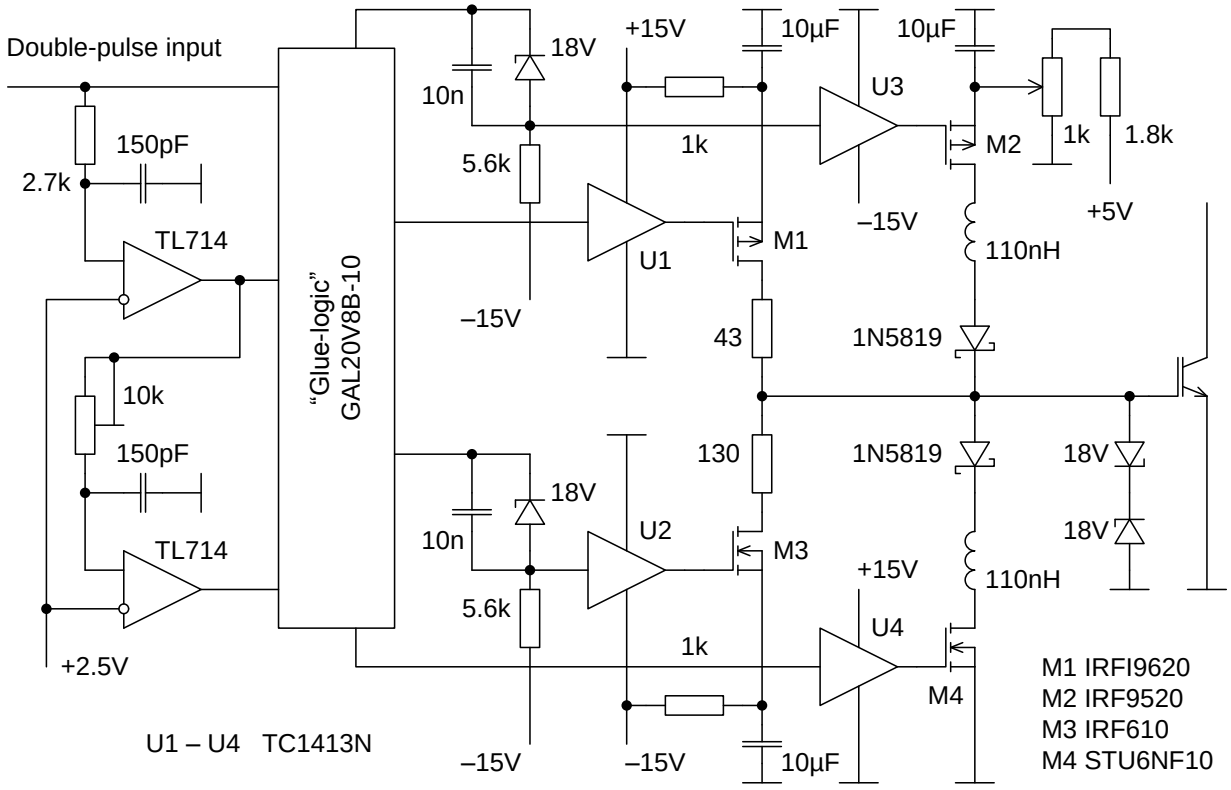


Figure 4-10: Resonant gate driver circuit

Since the resonant branches are controlled by MOSFETs in this implementation (for simplicity), series Schottky diodes (1N5819) are required to prevent the current from reversing direction after the voltage reversal. Unlike thyristors, MOSFETs have to be kept in the ON state for the whole resonant period of time, which ends after engaging a resistive branch (states 2, 3, 5, 6 in Fig. 4-11). ON states of resonant branches must not overlap, so a fixed dead time was introduced into the state diagram (states 1, 4 in Fig. 4-11). A total of 6 states is required, as well as introduction of another comparator TL714 into the circuit (Fig. 4-10).

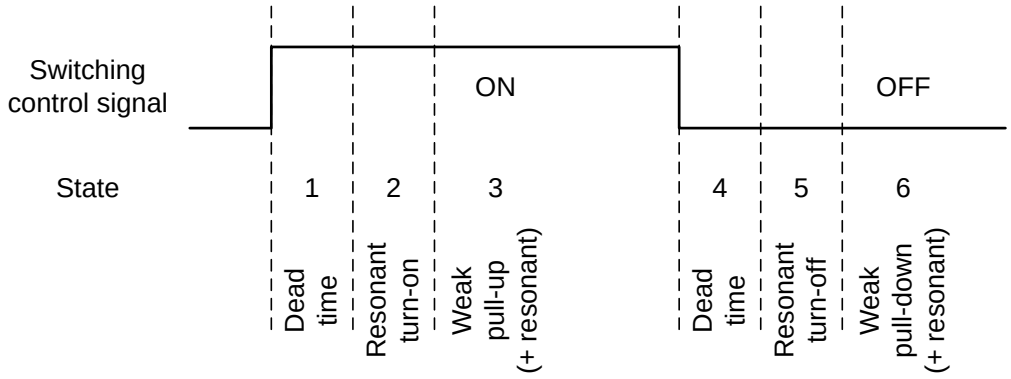


Figure 4-11: Resonant gate driver state diagram

Similarly to the multi-speed gate driver, logic equations have been derived for the resonant gate driver and have been programmed into the GAL chip. Table 4-2 summarizes the truth table of states of the resonant gate driver.

Table 4-2: Truth table for MOSFET states of the resonant gate driver

STATE	INPUT	COMP. 1 OUT	COMP. 2 OUT	M1	M2	M3	M4
1	1	0	0	OFF	OFF	OFF	OFF
2	1	1	0	OFF	ON	OFF	OFF
3	1	1	1	ON	ON	OFF	OFF
4	0	1	1	OFF	OFF	OFF	OFF
5	0	0	1	OFF	OFF	OFF	ON
6	0	0	0	OFF	OFF	ON	ON

4.4.2. Results

By adjusting the time delay between the start of resonant stage and the resistive stage, and by adjusting the reference point of capacitor voltage reversal, it was possible to obtain as result that for the same turn-on current overshoot as for the conventional gate driver, the resonant gate driver's switching loss could be brought down to almost exactly the same value as the conventional gate driver's switching loss. Fig. 4-12 shows that even though the switching waveforms are much different, the calculated switching losses of CGD and resonant gate driver match within 1% while the current overshoot and steady-state values also match within 1%.

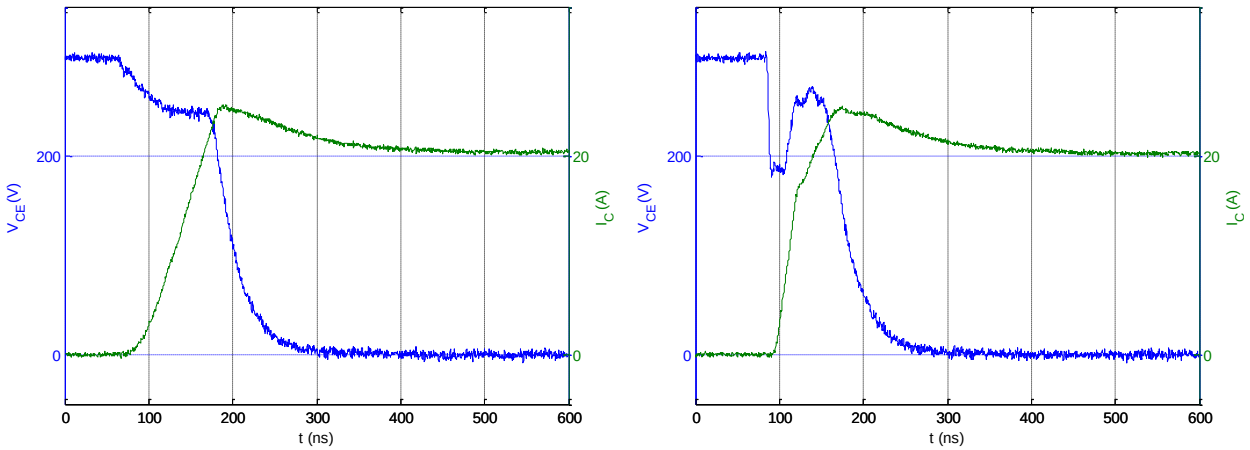


Figure 4-12: Turn-on waveforms: CGD (left), resonant gate driver (right)

Resonant gate driver cannot offer a decrease in turn-on losses, but its obvious 2-stage current waveform in Fig. 4-12 right (that could not be obtained using 2-stage resistive switching) could be used for continuous overshoot and speed control as opposed to several steps in gate resistance.

The turn-off resonant switching performance is almost the same as of a conventional gate driver, set to the maximum switching speed. This is because the gate-emitter voltage level corresponding to Miller plateau is passed near the peak of the sinusoidal gate current waveform.

4.5. Output stage with continuously variable current control

Switched resistors can only have discrete values, and the more precision is required in setting a desired gate resistance, the more resistors and MOSFETs are required. An alternative method [45] has been chosen to be tested for performance, which consists of varying the maximum IGBT gate current by BJTs in active mode (Fig. 4-13). Small resistances are used to sense the gate current for push and pull, and two differential amplifiers control BJTs in modified Darlington configuration. Both amplifiers share the same analog reference input, which allows using a microcontroller with only one DAC (digital-to-analog converter) to control the gate driver output stage. Fast and stable response is ensured by lead-lag compensation [46] performed by 10 pF capacitors parallel to resistors in feedback voltage divider branches.

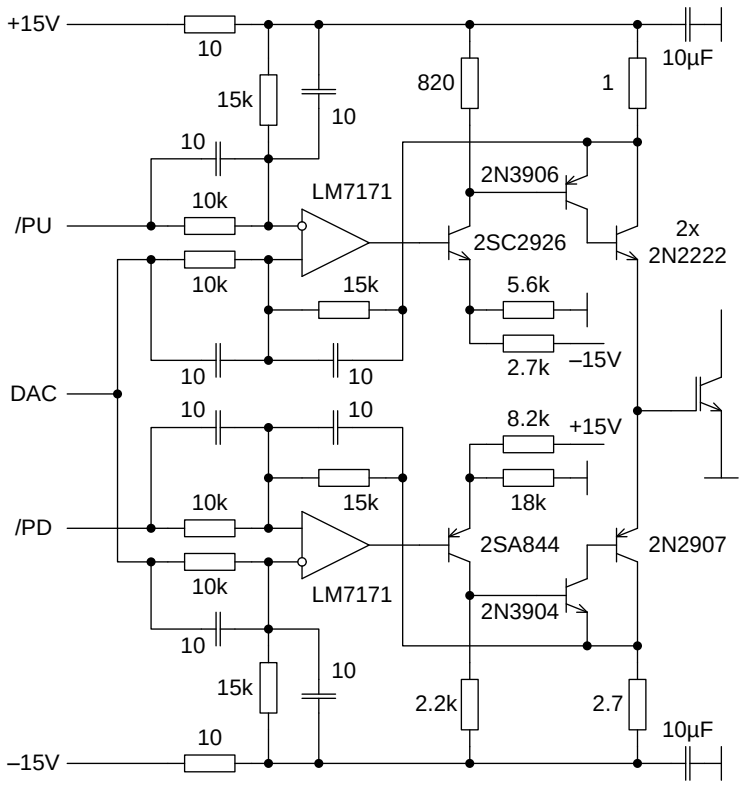


Figure 4-13: IGBT gate driver output stage circuit with continuously variable gate current

Either pull-up or pull-down function is selected by pulling /PU or /PD inputs to ground by a standard logic output. All three inputs are compatible with 5V or 3.3V logic.

During the design process, special attention was drawn to the choice of operating points of BJTs immediately following operational amplifiers. If their emitter voltages set by resistor dividers are too close to the power supply rails, the limited output swing of operational amplifiers will not be able to turn off these BJTs completely, which will in turn cause leakage current through the output stage. On the other hand, if their emitter voltages are too far from the power supply rails, the output swing of operational amplifiers will exceed the maximum allowed base-emitter reverse voltage of typically 5…6V when the corresponding push or pull branch needs to be disabled.

This output stage has been observed to have the same losses for the same overshoots as the switched-resistor output stage, because the gate current does not undergo rapid changes, as with dual-stage and resonant output stages.

4.6. Summary

The performance results of the four tested output stages can be summarized in the following Table 4-3 by circuit complexity, overshoot controllability, and how well this controllability can be used to reduce switching losses for a spread of load currents.

Table 4-3: Performance summary of tested gate driver output stages

OUTPUT STAGE	CIRCUIT COMPLEXITY	LOSS REDUCTION FOR SPREAD OF LOAD CURRENTS		OVERSHOOT CONTROLLABILITY	
		TURN ON	TURN OFF	TURN ON	TURN OFF
Switched-resistor	Low	Good	Good	Good	Fair
Dual-stage resistive	Medium	Bad	Good	Bad	Bad
Multi-stage inductive	High	Good	Good	Bad	Bad
Gate current control	High	Very Good	Very Good	Fair	Good

These results are supported by measurements obtained from testing the two best output stages: switched-resistor and with gate current control. The inverse relationship of switching losses and overshoots is observed in hardware, and matches the simulated behaviour in PSpice (Fig. 3-13). The switched-resistor loss functions are only shown, as the gate current control loss functions are very similar (Fig. 4-14).

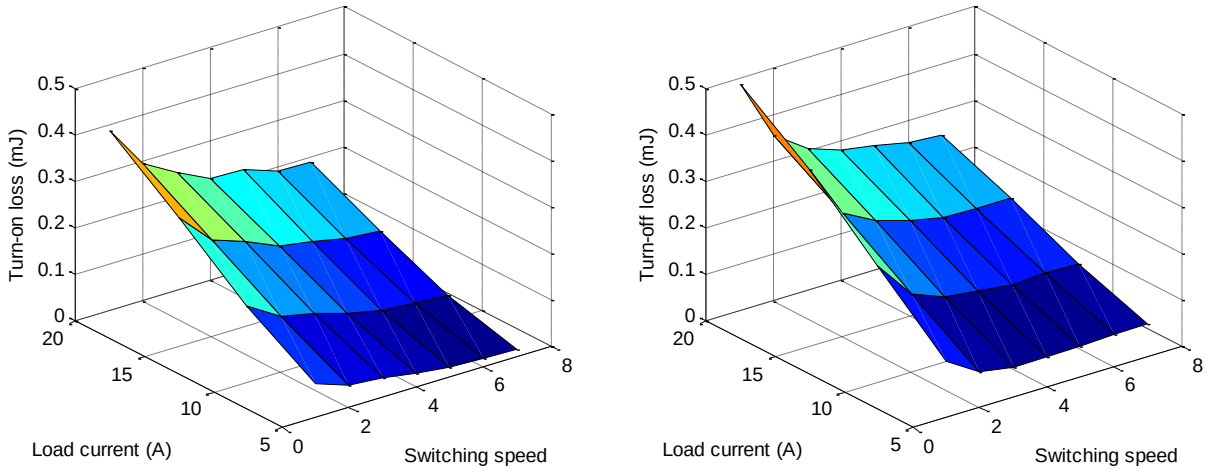


Figure 4-14: Energy loss for switched-resistor output stage: turn-on (left), turn-off (right)

The controllability is verified by checking the linearity of overshoot as function of the input variable (resistor index or DAC control voltage) for different load currents. The transfer functions are shown in Figures 4-15 and 4-16.

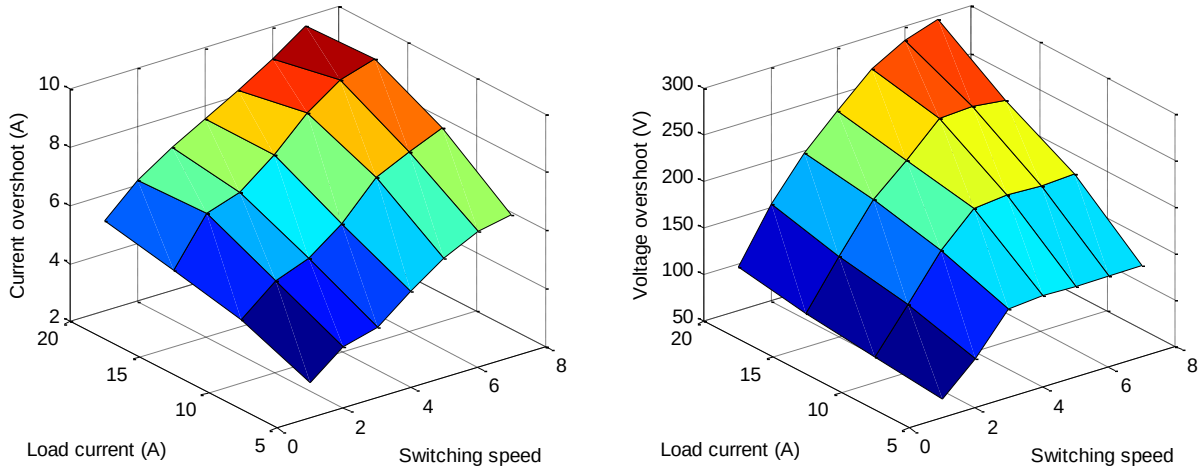


Figure 4-15: Overshoots for switched-resistor output stage: turn-on (left), turn-off (right)

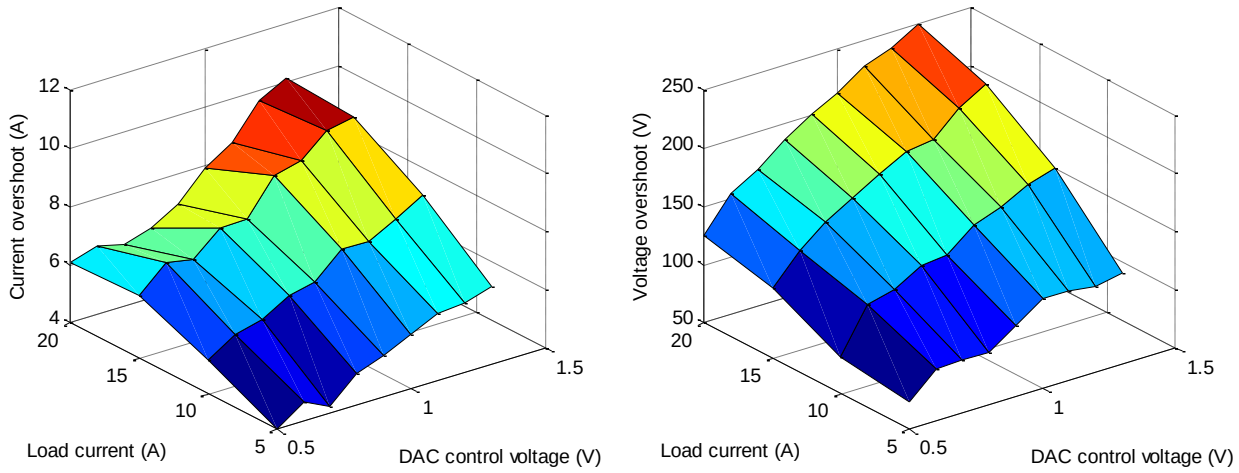


Figure 4-16: Overshoots for output stage with continuous current control: turn-on (left), turn-off (right)

It can be concluded that the best results for turn-on are obtained with switched-resistor output stage, while for turn-off the best results are obtained by continuous gate current control output stage. For all gate driver types, the following is true: varying switching speed during switching process usually leads to increase of switching losses.

Chapter 5:
Proposed Gate Driver

5.1. Switching loss reduction concept

In DC/AC converters, the sinusoidal waveform on the AC side generated by PWM is of a much higher frequency than the AC fundamental. A typical 2-level inverter leg in Fig. 5-1 will serve as an example to demonstrate the switching loss reduction concept. Consider a quarter-cycle of the AC fundamental, during which the load current increases from zero to the amplitude value. Because the current direction is away from the inverter leg, PWM pulses alternate through T1 and D2, while T2 and D1 are OFF.

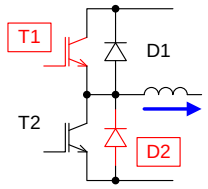


Figure 5-1: 2-level inverter leg used as example for waveforms in Figures 5-2 and 5-3

In this case, Fig. 3 left shows the current waveforms through the IGBT T1 and through the load for a conventional gate driver. The two inequalities limiting the overshoots are:

$$V_{DC} + V_{OS} \leq V_{MAX} \tag{5.1}$$

$$I_L + I_{rr} \leq I_{MAX} \tag{5.2}$$

The fixed turn-on speed in a conventional gate driver is set by the gate resistor, which is chosen based on the difference between the maximum load current and the maximum IGBT current allowed by its SOA. In some other implementations a fixed overshoot is achieved by controlling di/dt and dv/dt [11, 12, 14]. Thus, the limiting factor for current overshoot only occurs at maximum values of load current, and the SOA envelope is not fully utilized. Due to the fixed switching speed, the switching losses shown in Fig. 5-3 left for the conventional gate driver closely follow the sinusoidal pattern of the load current.

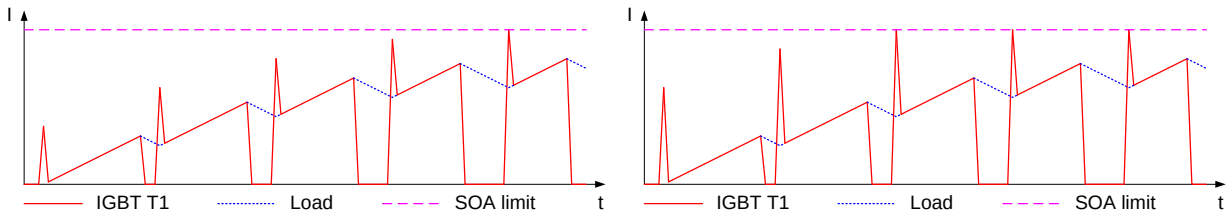


Figure 5-2: Current waveforms for inverter with: CGD (left), PGD (right)

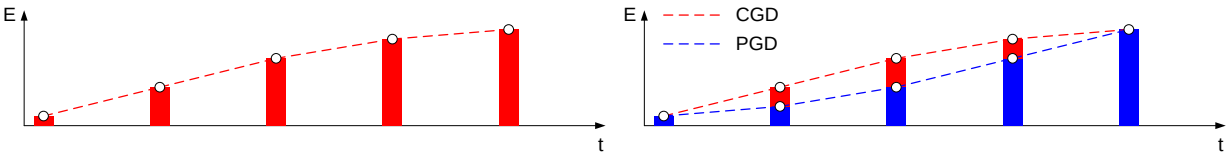


Figure 5-3: Turn-on losses for inverter with CGD (left), comparison to PGD (right)

The purpose of the proposed variable-speed gate driver is to track the SOA as shown in Fig. 5-2 right. Because all overshoots, except near the maximum load current, are increased by faster switching speeds, the corresponding switching losses are decreased, as shown in Fig. 5-3 right. The switching losses no longer follow the sinusoidal pattern but rather go below it, only with the maximum value being the same as for the conventional gate driver.

Typically in a real situation there will be more than 5 PWM cycles per quarter-cycle of the fundamental. In Fig. 5-2 right and in a real situation not all overshoots will reach the maximum value due to the limited range of switching speed increase comparing to the default speed. For turn-off the principle is the same, except it only turns out to be useful if the DC link voltage is not constant, typically in battery-powered applications. If the voltage is constant, a variable-speed turn-on circuit can be combined with a fixed-speed turn-off circuit for cost reduction.

5.2. Feedback control

5.2.1. Adaptive control based on statistical approach

Two types of gate driver stages (switched-resistor and with IGBT gate current control) have demonstrated the following overshoot functions:

$$I_{OS} \approx A_{ON} \cdot u_{ON} + B_{ON} \cdot I_L + C_{ON} \tag{5.3}$$

$$V_{OS} \approx A_{OFF} \cdot u_{OFF} + B_{OFF} \cdot I_L + C_{OFF} \tag{5.4}$$

where *u* is the input speed control signal in terms of control voltage for IGBT current control driver stage, or in terms of switched resistor combination index. Once the forward transfer function is known in terms of plane parameters A, B, C, the switching speed *u* can be found from:

$$u_{ON} = \left(I_{MAX} - I_L - B_{ON} \cdot I_L - C_{ON}\right) / A_{ON} \tag{5.5}$$

$$u_{OFF} = \left(V_{MAX} - V_{DC} - B_{OFF} \cdot I_L - C_{OFF}\right) / A_{OFF} \tag{5.6}$$

Because the inequalities (5.1) and (5.2) can be equalities or inequalities, the control inputs need to be limited between a tested range of switching speeds, i.e. the DSP needs to make sure the output will be within valid boundaries after computing values for *u*. But the overshoot is not known before the switching process has taken place, so the plane parameters A, B, C need to be estimated. Given a set of previous overshoot measurements (z), for which the control signal (x) and the load current (y) have also been saved, it is possible to run a linear regression calculation to determine the plane closest to all points (x, y, z). An example of an acquired set of points in circular buffer is shown in Fig. 5-4.

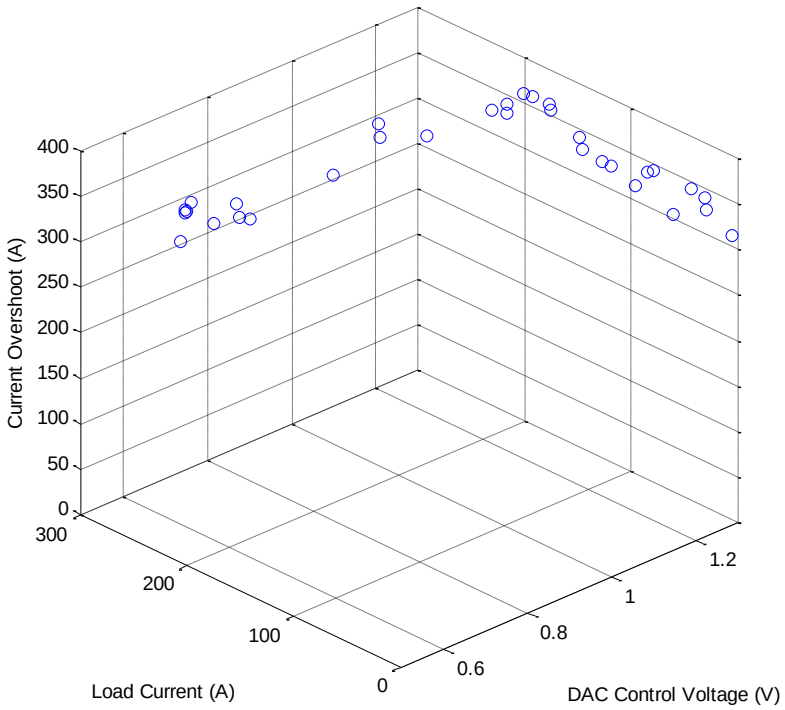


Figure 5-4: Example of circular buffer dump with previous switching data

In order to reconstruct the characteristic plane, a 2-D linear regression operation needs to be performed according to (5.7):

$$\begin{bmatrix} \sum x^2 & \sum xy & \sum x \\ \sum xy & \sum y^2 & \sum y \\ \sum x & \sum y & N \end{bmatrix} \begin{bmatrix} A \\ B \\ C \end{bmatrix} = \begin{bmatrix} \sum xz \\ \sum yz \\ \sum z \end{bmatrix} \tag{5.7}$$

where N is the number of acquired points and must be at least 3. The actual matrix inversion computations require first finding the determinant (5.8), before computing A, B, C (5.9). These coefficients need to be constantly updated, because they drift with temperature. Hence the attribution of this algorithm to the class of adaptive feedback control algorithms.

$$\det = 2\sum x \sum y \sum xy + N\left(\sum x^2 \sum y^2 - \left(\sum xy\right)^2\right) - \left(\sum x\right)^2 \sum y^2 - \left(\sum y\right)^2 \sum x^2 \tag{5.8}$$

$$\begin{bmatrix} A \\ B \\ C \end{bmatrix} = \begin{bmatrix} N\sum y^2 - \left(\sum y\right)^2 & \sum x \sum y - N\sum xy & \sum xy \sum y - \sum x \sum y^2 \\ \sum x \sum y - N\sum xy & N\sum x^2 - \left(\sum x\right)^2 & \sum xy \sum x - \sum y \sum x^2 \\ \sum xy \sum y - \sum x \sum y^2 & \sum xy \sum x - \sum y \sum x^2 & \sum x^2 \sum y^2 - \left(\sum xy\right)^2 \end{bmatrix} \begin{bmatrix} \sum xz \\ \sum yz \\ \sum z \end{bmatrix} / \det \tag{5.9}$$

5.2.2. Adaptive control theory

The proposed control technique can be graphically represented as shown in Fig. 5-5.

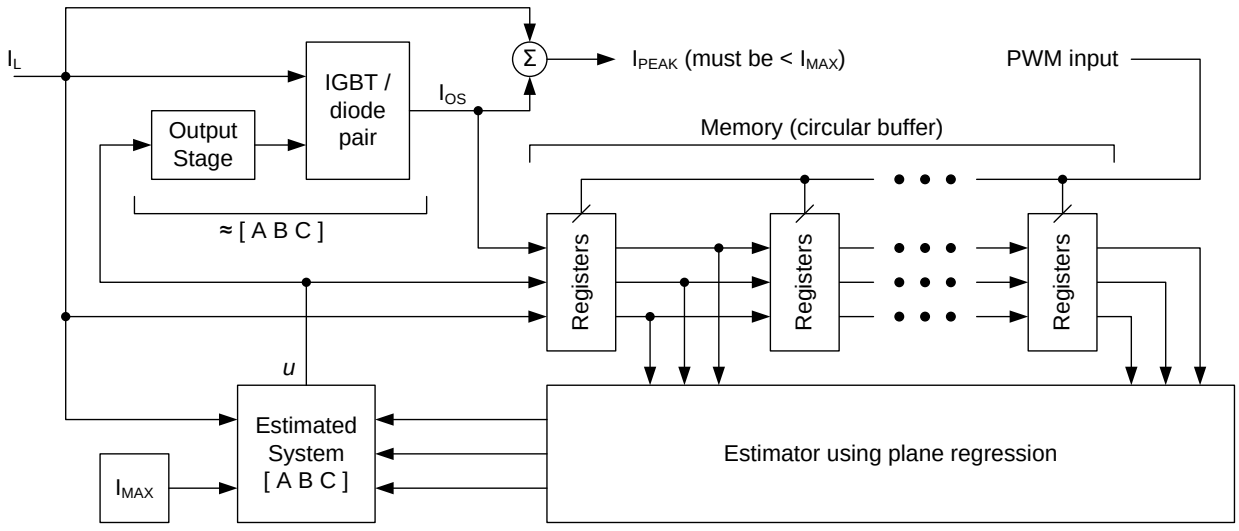


Figure 5-5: Graphical representation of feedback control core

The parameters A, B, C act as input weighting functions for both real and estimated systems [22]. The estimator in our case is the plane regression function, which can internally calculate and store errors between the real and estimated overshoot values. However, since the feedback is performed by reversing the estimated linear relationship to obtain the control signal *u*, the core of the control principle follows the inverse adaptive control techniques [23].

Stability of such systems depends on bound conditions of the real system itself, and on bounds imposed on certain variables used in feedback [24]. In our case, the bounds are only imposed on the control input *u*, and the real system is known to provide bounded output for all ranges of input signals and external factors such as temperature and variance of device manufacturing parameters. During performance testing of manufactured systems, additional bounds on plane parameters A, B, C can be introduced in software.

5.2.3. Algorithm timing

One of the requirements of the gate driver is to provide a quick response to input PWM signals. Comparing to the system controller, the gate driver is considered a "slave" device, and must be ready to accept PWM input signals at any time. The best way to achieve this on a microcontroller is to assign one interrupt to be triggered on positive PWM transitions, and another interrupt on negative ones. Also, quick response means that the latency between the PWM transition and the gate output signal must be small. Mathematically, a few operations are required to immediately compute *u*, as can be seen from (5.5) and (5.6). On most processors only division takes considerably more CPU cycles than other operations, which becomes the limiting factor for latency. In reality these calculations require V_{DC} and I_L to be known with good precision immediately before the gate pulse is fired. Measuring these analog signals requires ADC conversions, which may or may not be fast enough depending on the CPU. Because both V_{DC} and I_L are slowly-changing parameters compared to PWM timing, the ADC conversion may or may not be incorporated into the interrupt before the mathematical computation takes place. In case the ADC conversions are placed outside of interrupt, they have to be periodic with lower interrupt priority than PWM interrupts. In the next timing charts ADC conversions will be incorporated in the PWM interrupts for simplicity. The chart in Fig. 5-6 shows the default

behaviour of gate driver CPU, where "INTx" indicates times when the CPU is busy with switching speed calculations, and during "PROCESSING x" the CPU is busy computing linear coefficients A, B, C involving matrix inversion, storing and retrieving data points from a circular buffer, which amounts to significantly more calculations than finding the switching speed during a PWM interrupt. It is important to note that the overshoot value must be measured immediately after the PWM transition because of peak detector limitations.

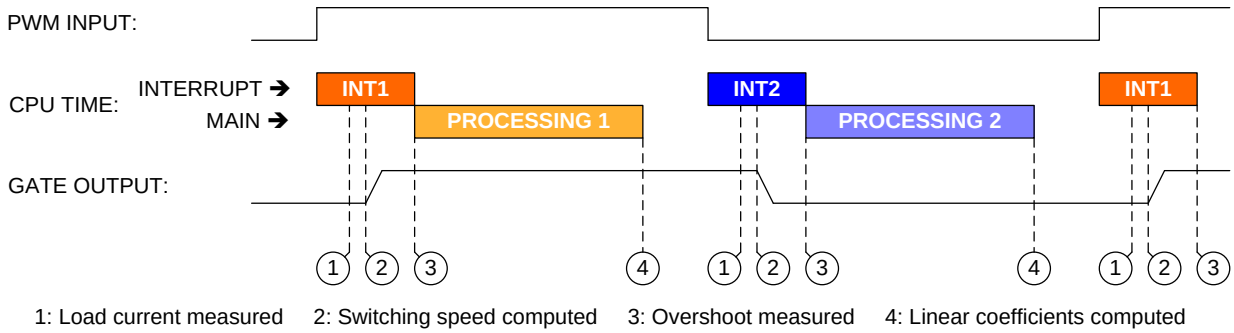


Figure 5-6: Gate driver CPU timing chart with widely-spaced PWM pulses

If the time between PWM pulses is large, the time spent on overshoot measurement does not affect the latency of the gate driver CPU. However, the following happens as PWM pulses become narrower (Fig. 5-7):

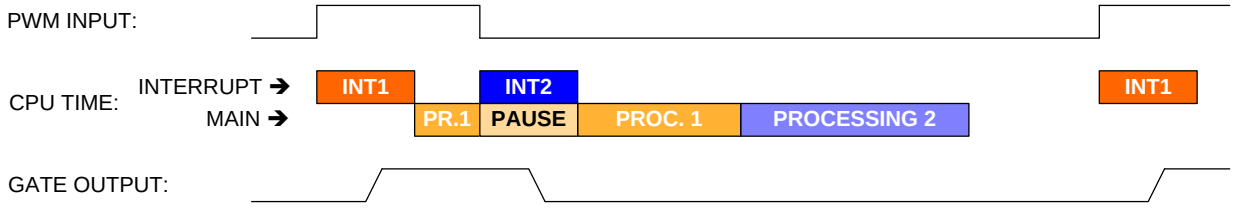


Figure 5-7: Gate driver CPU timing chart with narrow PWM pulses

Note that even though the CPU did not complete the processing for turn-on before the turn-off pulse has occurred, both turn-on and turn-off processing periods should complete before the next turn-on pulse, because the maximum PWM frequency sets the minimum time delay between signal transitions in the same direction. Therefore, the algorithm complexity and the CPU speed have to be estimated based on the maximum PWM frequency. The latency in

Fig. 5-7 is unaffected comparing to Fig. 5-6. Finally, if the PWM pulse width becomes less than the interrupt execution time, the timing chart becomes as shown in Fig. 5-8:

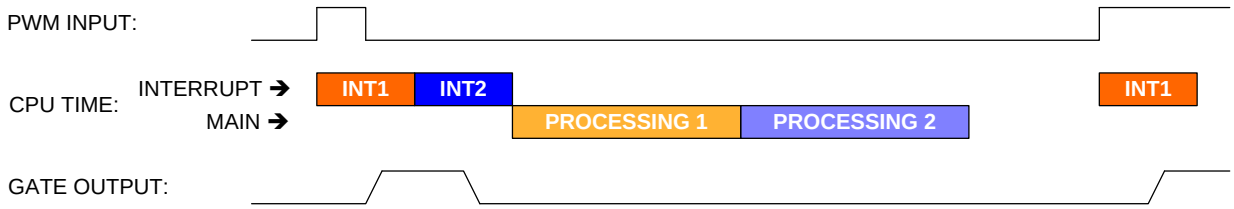


Figure 5-8: Gate driver CPU timing chart with PWM pulses narrower than interrupt execution time

The minimum pulse width the developed gate driver can generate is therefore equal to the CPU interrupt execution time, which at the bare minimum must contain the switching speed calculation and the overshoot sampling (beginning of ADC conversion). For CPUs operating around 40 MHz and above, this could be less than 1 µs. A CPU with hardware division capability is strongly recommended.

Equations (5.7) through (5.9) contain sums of functions of last points stored in the circular buffer. To avoid recomputing all terms in the equation "as is", the sums are stored separately from the buffer data. Before overwriting old data with new data, the old data is subtracted from the sums, and the new values are added to the sums. That way, the buffer size does not affect the computational complexity, i.e. the complexity is always O(1).

5.2.4. Algorithm improvement no. 1: avoiding matrix singularities

The buffer size on chip is usually very limited, and stores only the most recent points by default. In certain cases, the very effect of optimizing switching speed for given load current leads to linear correlation between all three parameters: input speed control signal, load current, and overshoot. In this situation, correlation is desirable in terms of performance, but creates a problem for further estimation of plane parameters A, B, C. An example of such data in the circular buffer is shown in Fig. 5-9, one switching transition before entering an almost singular condition.

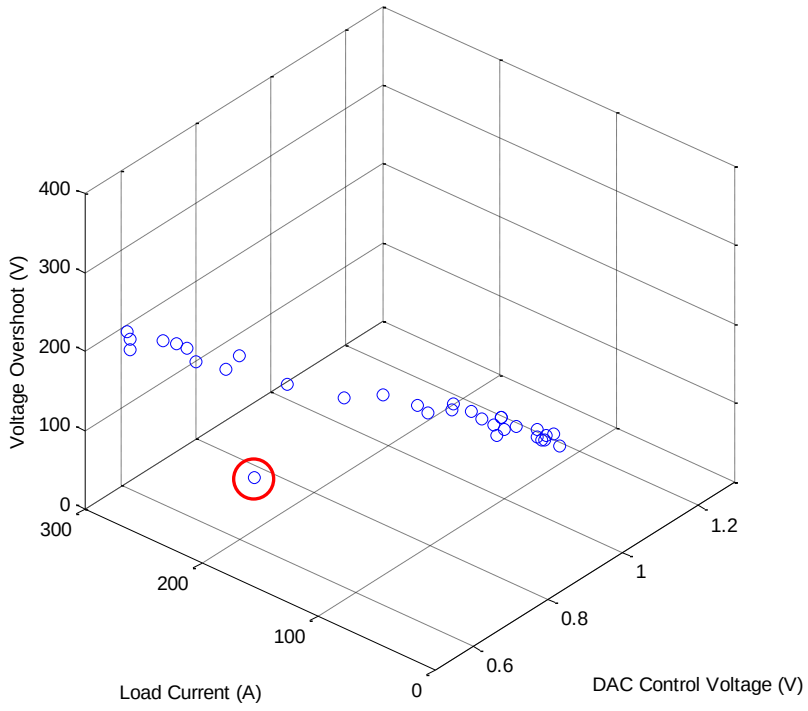


Figure 5-9: Example of circular buffer dump one switching transition before singularity

A singularity in this case means that if the data point circled in red is overwritten with data correlating with other points, the plane orientation becomes uncertain around the axis of correlation direction, effectively making it impossible to accurately estimate its three parameters A, B, C, leading to algorithm divergence and failure.

A workaround has been introduced into the algorithm to avoid circular buffer content leading to singular conditions. Before overwriting a data point, the algorithm checks if a new point in its place would cause a singular condition. If so, the same test is performed on the next point in the buffer, effectively trying to replace an old point in strong correlation with others, and leaving the critical point in the buffer (circled in red) by skipping it. The selection procedure is repeated until an old point is found, which can be successfully replaced by new data. There is also a limit on the maximum number of points to try to replace, after which the new data is simply discarded. This limit is based on microcontroller performance, because all computations for each of the turn-on and turn-off processes have to complete in half of PWM period in worst case scenario.

This workaround creates an undesirable side effect of failure of one or several data points to update fast enough to follow the converter temperature variations, leading to incorrect estimates of overshoots. In other words, one or a few data points could get stuck in place for a long time, without being updated. In order to keep them updated, single PWM pulses can be occasionally forced to the slowest switching speed, far from the optimal path in the buffer. The overall increase of switching losses will be insignificant, because such "probing" pulses need to be performed only once per at least 1000 pulses.

As for the criterion for determining if the buffer data represents a singular condition or not, the current algorithm implementation compares the matrix determinant (5.8) against a constant. It can be shown that the determinant is related to the average spread of data points in the 2-D plane of the two input variables: control input and load current. Also, the buffer size has effect on the uncertainty between the maximum and minimum possible spread areas. Large buffer size has a large uncertainty on the choice of determinant threshold constant for singularity checking. The current algorithm keeps 32 points in the buffer.

5.2.5. Algorithm improvement no. 2: adjusting for overshoot function nonlinearities

In practice, the actual relationship between overshoots, input signals, and load currents is not perfectly linear. For that reason, the statistical regression approach is also used to compute the standard deviation between measured overshoots and their computed values that lie on the regression plane set by parameters A, B, C. Upon switching speed calculation, a certain multiple of standard deviation is subtracted from the maximum programmed value of voltage or current, which provides a very flexible method of preventing overshoots from exceeding programmed maximum values at all times:

$$u_{ON} = \left(I_{MAX} - I_L - B_{ON} \cdot I_L - C_{ON} - K * STDEV_{ON}\right) / A_{ON} \quad (5.10)$$

$$u_{OFF} = \left(V_{MAX} - V_{DC} - B_{OFF} \cdot I_L - C_{OFF} - K * STDEV_{OFF}\right) / A_{OFF} \quad (5.11)$$

where K is the nonlinearity-related safety factor (2 in simulation), and STDEV for both turn-on and turn-off is found from:

$$STDEV = \sqrt{\frac{\sum \left(z - z_{REF}\right)^2}{N}} \tag{5.12}$$

The computation of the difference between z-coordinates requires the set of operations (5.13) for each data point:

$$z_{REF} = A \cdot x + B \cdot y + C \tag{5.13}$$

If they are performed as written by the mathematical equation, the complexity is O(N) due to buffer traversal. However, separate storage of buffer data sums allows reducing the complexity down to O(1) by expanding the STDEV expression:

$$\sqrt{\frac{\sum \left(z - Ax - By - C\right)^2}{N}} = \sqrt{\frac{\sum \left(z^2 + A^2x^2 + B^2y^2 + C^2 + 2\left(A\left(Bxy - xz\right) + B\left(Cy - yz\right) + C\left(Ax - z\right)\right)\right)}{N}} \tag{5.14}$$

The last implementation problem discussed here is the presence of the square root operation. Microcontrollers do not have hardware acceleration to perform them. Alternative ways need to be considered for their estimation, such as linear interpolation of lookup tables, resolution limiting, or iteration number limiting.

5.2.6. Algorithm startup after power-on reset and flowcharts

In order to have the circular buffer full of useful data, PWM pulses need to be performed at different switching speeds. But the buffer is empty after power-on reset, so the optimal switching speed cannot be calculated. Some initial spread of switching speeds is required to start filling the buffer with data that will not lead to a singular condition for regression plane calculation.

The proposed method uses a fixed "second" switching speed, which is typically higher than the default (slowest) speed by 15…30%. According to the example in Fig. 5-2 right, three first pulses can be safely performed at any switching speed within the driving capability of the output stage, because the load current is low enough. For each specific hardware realization, two important measurements have to be programmed into the microcontroller, one for turn-on and one for turn-off, both of which determine the highest load current for which the

overshoot will not exceed the SOA if switched at the second speed, for the entire range of DC link voltages and temperatures. Knowing these load currents, the actual value of the second speed can be adjusted. The matrix determinant (5.8) threshold also depends on the ratio between the default speed and the second speed, because a certain minimum spread is required to exit the singular condition in the circular buffer. If the microcontroller is abnormally reset in the middle of motor operation, the startup sequence can still handle the initial non-zero load current.

Having made all adjustments to the principle idea of the algorithm, the flowcharts of the three stages of operation can be presented. The stages are numbered from 0 to 2, where stages 0 and 1 are executed after power-on reset, and stage 2 is run in steady state. The flowcharts for all three stages are illustrated as completely independent for easier understanding, even though they have many repeating blocks. The actual code is organized to include repeating blocks only once, with conditions of execution depending on stage of operation, in order to reduce the code size.

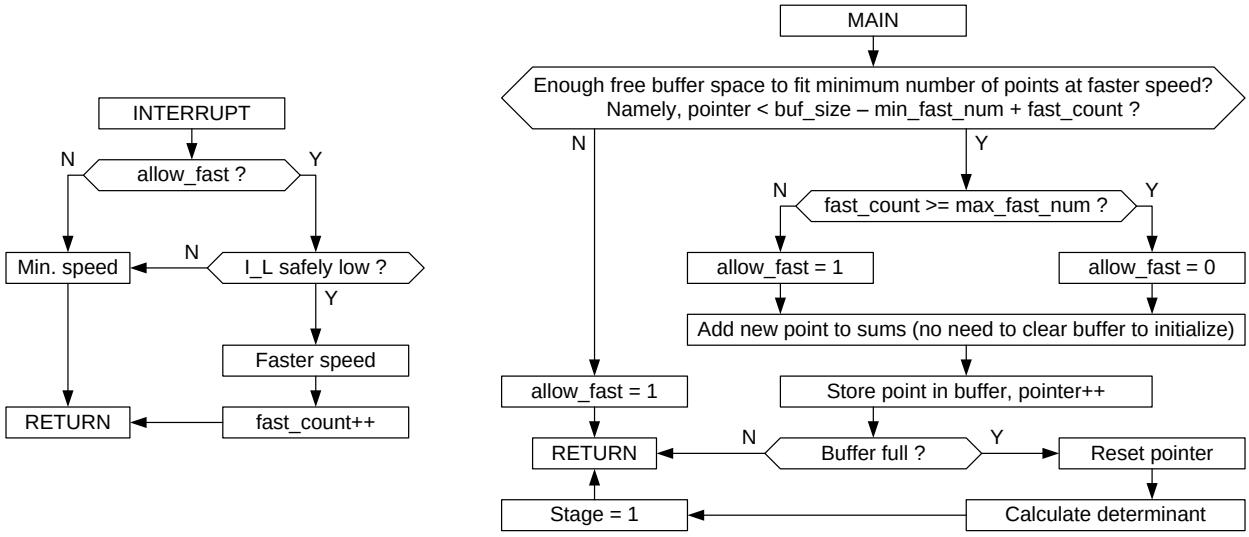


Figure 5-10: Operational flowcharts of stage 0 after power-on reset

The goal of stage 0 (Fig. 5-10) is to fill the buffer with data obtained using two fixed switching speeds close to the slow end of the range with the following restrictions: since faster pulses cannot be (yet) safely performed for any value of load current, they must be performed

when the current is lower than a programmed value, and the number of faster pulses must be at least sufficient to obtain enough initial spread in the next stage. The maximum number of faster pulses should be limited to N/3, because further increasing their number leads to decrease of spread because the number of slow pulses decreases.

The next stage 1 is necessary to perform all pulses at the slowest speed to obtain enough spread on the load current axis. Because the buffer is already full, the buffer and the cumulative sums are updated like in steady-state stage 2, but the matrix determinant is gradually brought to the required minimum by replacing points in the buffer. The interrupt routine is the same as in stage 0, and the main processing routine is shown in Fig. 5-11.

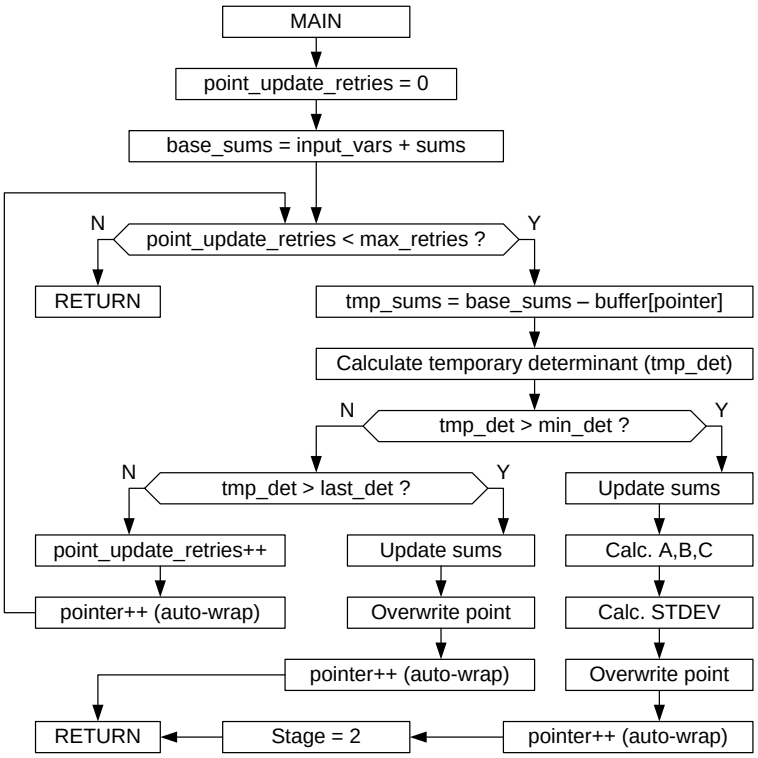


Figure 5-11: Operational flowchart of stage 1 after power-on reset (interrupt is the same as in Stage 0)

Finally, the steady-state stage 2 is the only stage where the switching speed is dynamically calculated, therefore it uses a different interrupt routine (Fig. 5-12). The main routine is very similar to stage 1, with the small exception of not performing the comparison

between the temporary determinant (tmp_det) and the determinant computed in the last cycle (last_det), and always assuming the result of that comparison is false (Fig. 5-11).

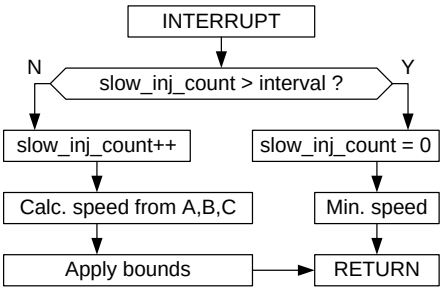


Figure 5-12: Operational flowchart of stage 2 interrupt after power-on reset

In the interrupt routine of stage 2 we can also find a condition that injects pulses at the slowest speed once per predefined repetition interval. They make sure the correlation between the two input variables will not lead to matrix singularity, and make sure all points in the buffer are kept updated.

Chapter 6:
Algorithm Validation and Results

6.1. Simulation procedures and test conditions

The algorithm has been implemented on MATLAB in form of code. All variable types are floating-point, so a few fixes were introduced to avoid bugs with integer comparison. The algorithm was tested using existing waveform data from full-scale simulations of the 54 kW motor [47] driven by the 650V 800A inverter [29]. Fig. 6-1 shows four points on the motor torque-speed envelope at which the simulations were conducted using SVPWM and DPWM2 [25] modulations. Additionally, SVPWM with overmodulation was tested for 40 Nm torque at 10000 rpm speed.

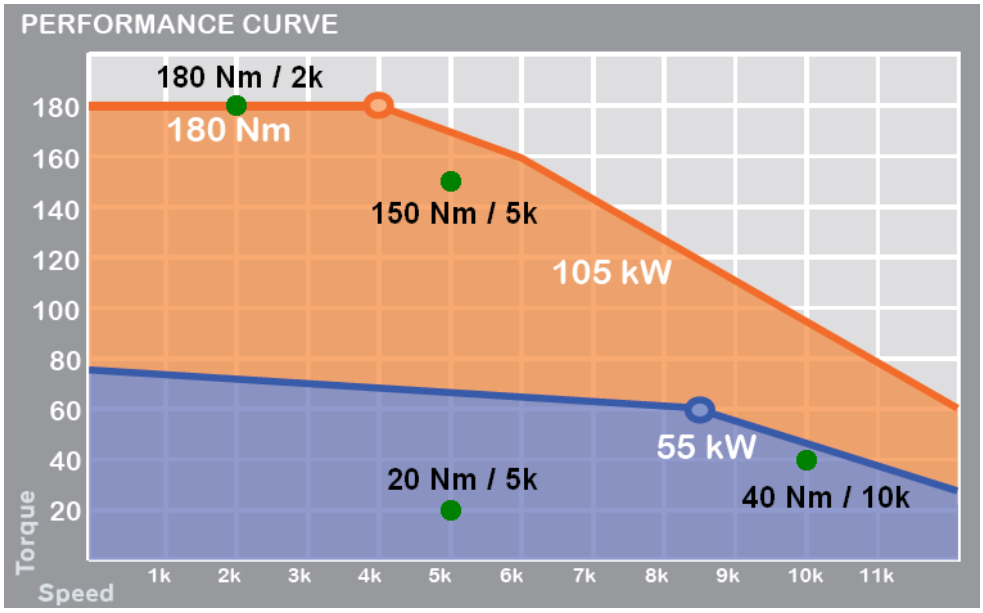


Figure 6-1: Points of gate driver algorithm performance and stability verification

For each modulation scheme mentioned above, two types of simulations were conducted. First, algorithm performance and stability were verified using switching waveform data for motor acceleration from rest to specified speeds. Second, switching and conduction losses were estimated for periods of steady-state motor operation only.

6.2. Algorithm performance and stability simulations

6.2.1. Overview

For both turn-on and turn-off processes, one set of performance graphs is shown for each modulation type (Fig. 6-2 through 6-7). Since gate drivers are "slave" devices, their algorithms operate on pulse by pulse basis, instead of equally spaced discrete time steps used in system controller simulations. The horizontal axis on simulation result graphs is in terms of PWM cycle number, so each step represents a time delay between two adjacent turn-on or turn-off commands received from the system controller. The vertical axis measurements are therefore sampled (strobed) at PWM signal transitions with uneven time distribution.

Figures 6-2 through 6-7 contain a section of time where the motor accelerates from rest to specified speed, and a section of steady-state operation at constant speed.

6.2.2. Turn-on performance

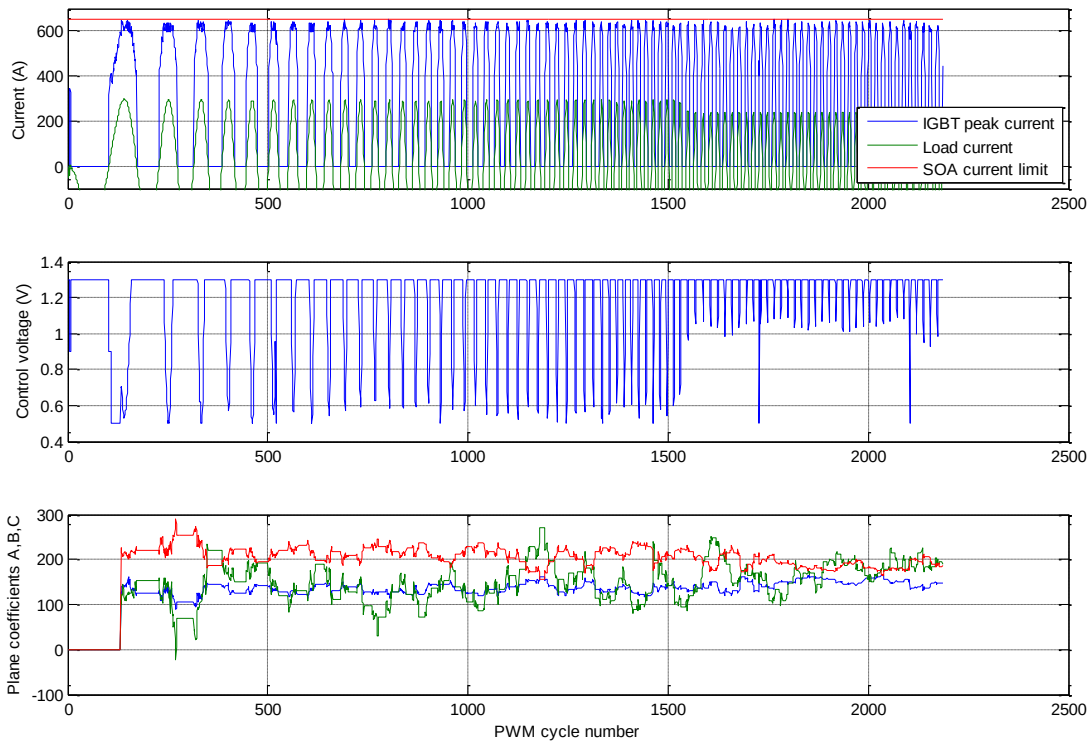


Figure 6-2: Performance turn-on test for SVPWM @ 150 Nm from rest to 5000 rpm

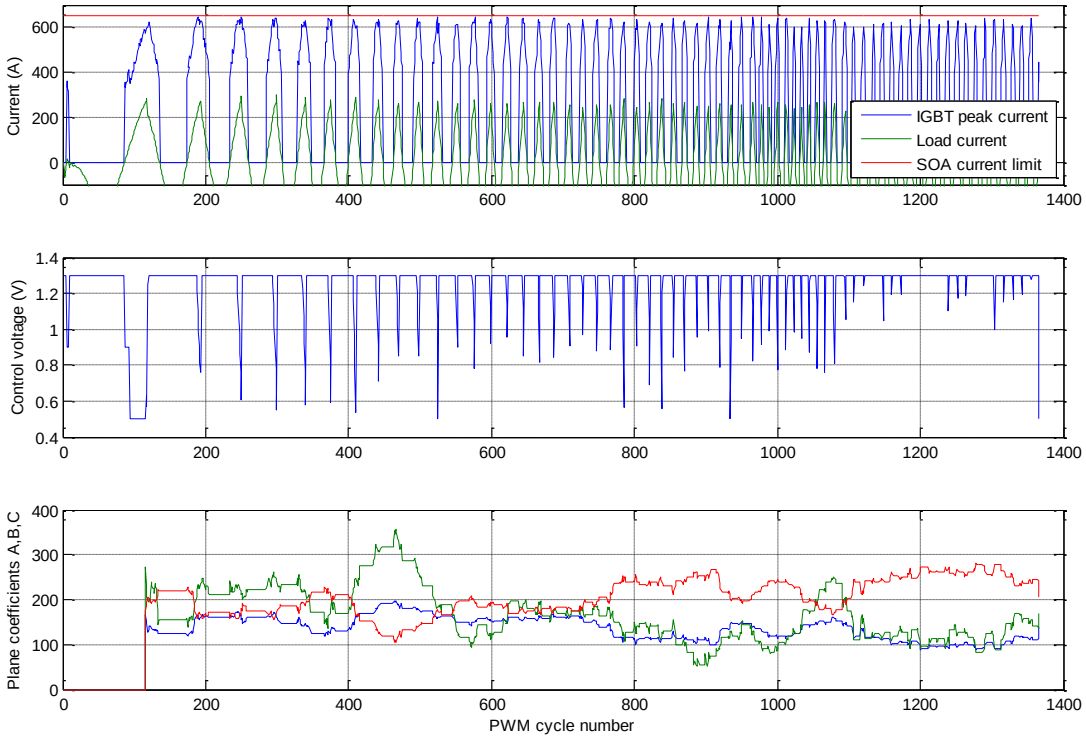


Figure 6-3: Performance turn-on test for DPWM2 @ 150 Nm from rest to 5000 rpm

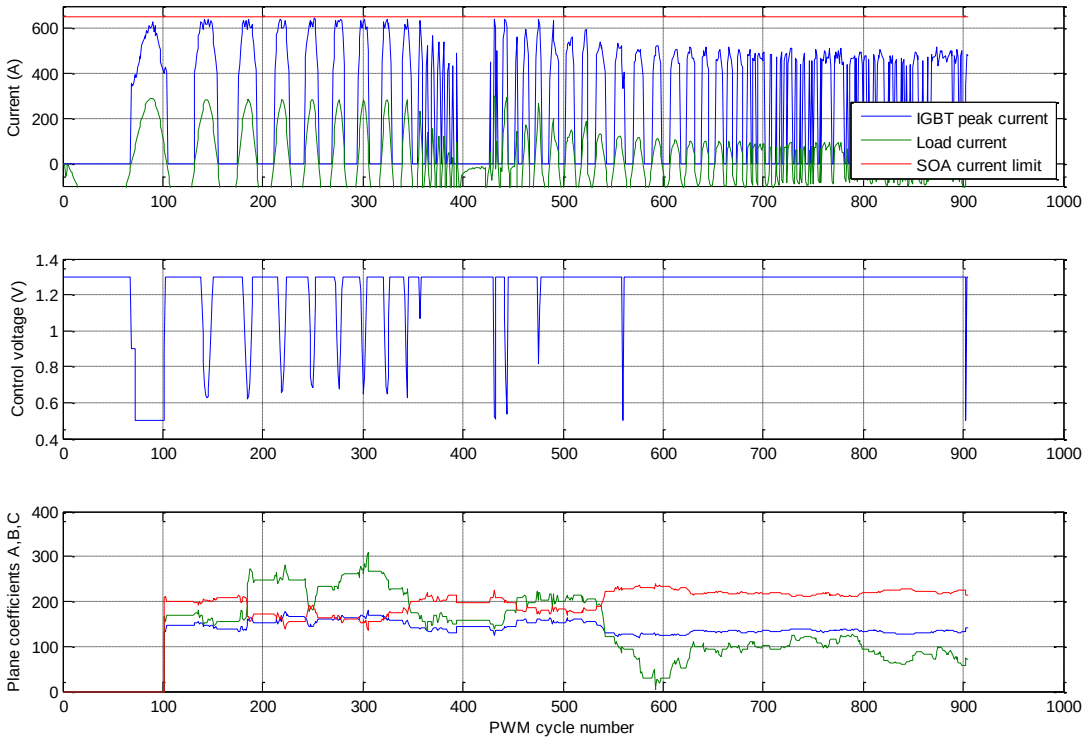


Figure 6-4: Performance turn-on test for SVPWM with overmodulation @ 40 Nm from rest to 10000 rpm

6.2.3. Turn-off performance

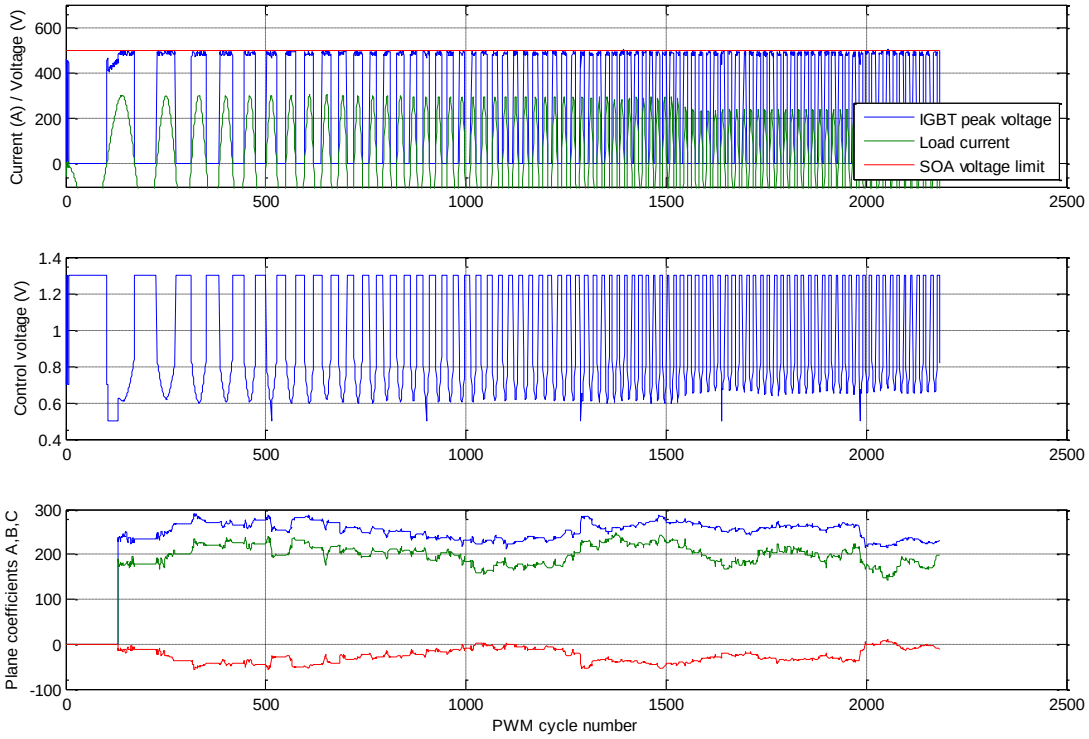


Figure 6-5: Performance turn-off test for SVPWM @ 150 Nm from rest to 5000 rpm

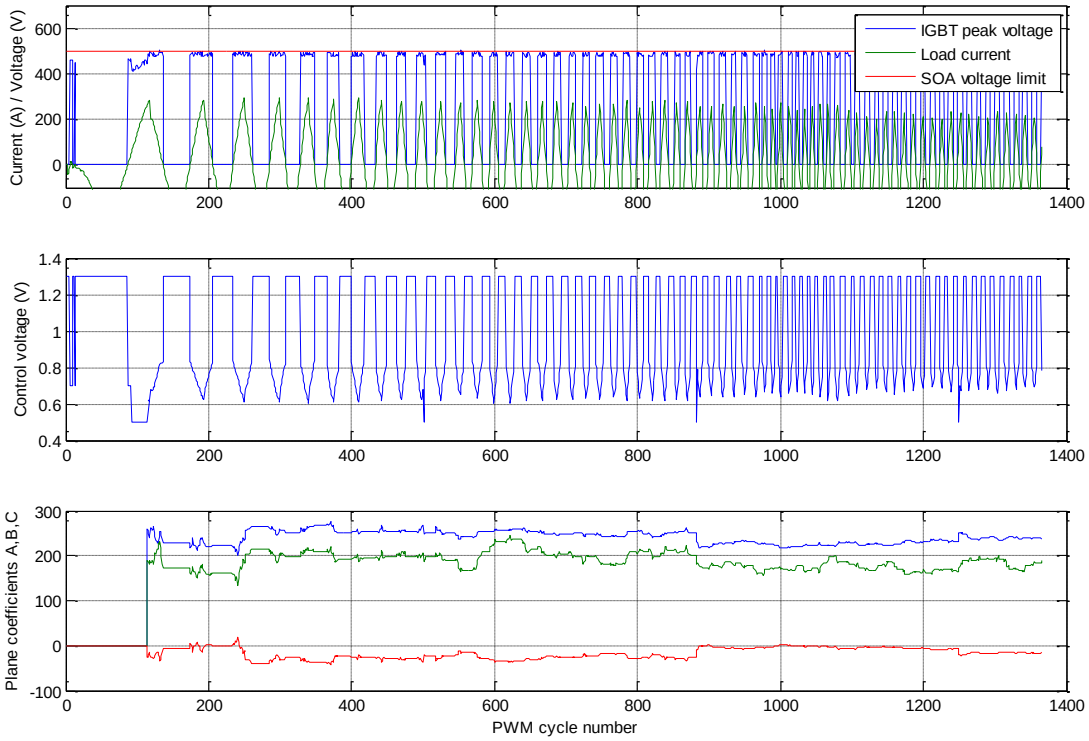


Figure 6-6: Performance turn-off test for DPWM2 @ 150 Nm from rest to 5000 rpm

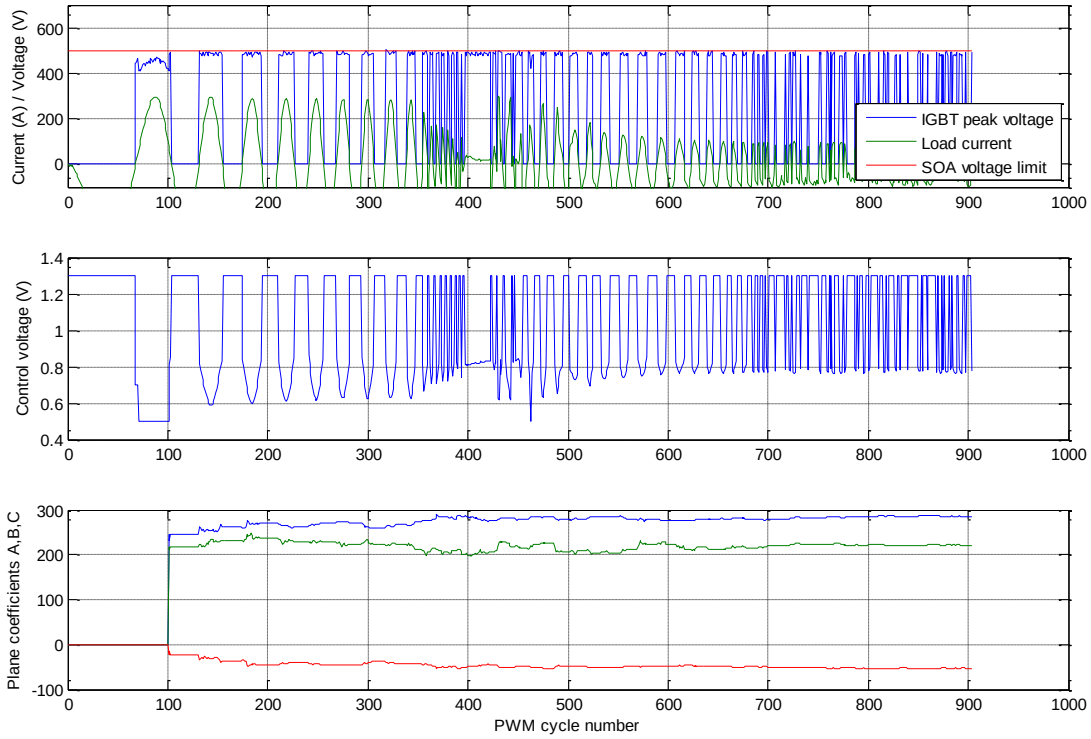


Figure 6-7: Performance turn-off test for SVPWM with overmodulation @ 40 Nm from rest to 10000 rpm

6.2.4. Performance and stability analysis

The top graph in each case shows the decrease of maximum load current at the beginning of steady-state operation. The middle graphs show how the optimal computed switching speed varies depending on the load current shown in the top graphs. During acceleration, where the maximum load current is high, the switching speed is brought down to default speed, as expected. In steady state the switching speed varies less and stays closer to maximum, because the load current is lower. Slow-speed probing pulses can also be observed at regular intervals in terms of PWM cycle count. For the purpose of demonstration, their repetition interval was reduced to 200 pulses. They are observed to repeat approximately every 400 pulses because the algorithm does not run when the load current is negative (flows through the freewheeling diode instead of IGBT), which happens for approximately half of the time. The switching speed does not have effect with negative load current, so it is kept at maximum in order to keep the control voltage continuous. The bottom graphs show the variation of estimated regression plane parameters A, B, C. Their variations provide a metric on algorithm stability. The least favorable PWM scheme for A, B, C parameter estimation is

SVPWM with overmodulation, because the system controller produces only one turn-on and one turn-off signal per load current fundamental cycle, causing a small spread of load currents stored in the circular buffer.

The programmed SOA current limit was chosen to be equal to the IGBT peak current for a conventional gate driver at maximum load current in the same motor drive application and at the junction temperature of 150°C. In that way, the variable-speed gate driver performance improvement is estimated with the condition of having the same maximum IGBT peak currents for both gate driver types.

6.3. Switching and conduction loss estimation

The loss estimation has been performed for steady-state part of simulation, spanning an integer number of several fundamental cycles. For turn-on, diode reverse-recovery losses were considered in addition to IGBT switching losses. The load current sensitivity functions for both IGBT and diode have been fitted to the datasheet curves using quadratic approximation. Since the datasheet provides IGBT and diode losses for effect of variable speed switching as functions of gate resistor only, the analog input voltage for gate current control has been mapped to equivalent resistor values, additionally considering the internal gate resistance.

Table 6-1: Turn-on and turn-off loss comparison between CGD and PGD

TEST PARAMETERS			TURN-ON LOSS (W)				TURN-OFF LOSS (W)			
MOD	TORQUE	RPM	P_{CGD}	P_{PGD}	%	DIFF	P_{CGD}	P_{PGD}	%	DIFF
DPWM2	150 Nm	5k	21.13	14.35	32.1	6.78	20.76	19.80	4.6	0.96
DPWM2	180 Nm	2k	24.28	16.86	30.6	7.42	23.19	22.22	4.2	0.97
DPWM2	20 Nm	5k	11.74	7.52	36.0	4.23	9.07	8.56	5.6	0.51
DPWM2	40 Nm	10k	37.32	25.03	33.0	12.30	26.22	24.88	5.1	1.34
SVPWM	150 Nm	5k	37.63	26.18	30.4	11.45	35.99	34.50	4.1	1.49
SVPWM	180 Nm	2k	42.85	32.54	24.1	10.31	40.97	39.49	3.6	1.48
SVPWM	20 Nm	5k	15.98	10.24	35.9	5.74	11.56	10.89	5.8	0.67
SVPWM	40 Nm	10k	45.19	30.22	33.1	14.97	31.81	30.18	5.1	1.64
SVM+OVM	40 Nm	10k	13.31	8.91	33.1	4.40	6.61	6.26	5.2	0.35

Tables 6-1 and 6-2 summarize the improvements introduced by the proposed gate driver in terms of turn-on, turn-off, total switching loss, and total converter loss (switching and conduction). The data provided is for one IGBT-diode pair, and needs to be multiplied by 6 to obtain total module losses. The columns "%" and "DIFF" quantitatively state the loss reduction in % and Watts, respectively. Figure 6-8 is equivalent to Table 6-2.

Table 6-2: Switching and conduction loss comparison between CGD and PGD

TEST PARAMETERS			SWITCHING LOSS (W)			COND. LOSS (W)	SW. + COND. LOSS (W)			
MOD	TORQUE	RPM	P_{CGD}	P_{PGD}	%		P_{CGD}	P_{PGD}	%	DIFF
DPWM2	150 Nm	5k	41.90	34.16	18.5	74.26	116.15	108.42	6.7	7.74
DPWM2	180 Nm	2k	47.47	39.08	17.7	95.94	143.41	135.02	5.9	8.39
DPWM2	20 Nm	5k	20.81	16.07	22.8	4.89	25.70	20.96	18.4	4.74
DPWM2	40 Nm	10k	63.54	49.91	21.5	27.12	90.67	77.03	15.0	13.63
SVPWM	150 Nm	5k	73.62	60.68	17.6	74.37	147.98	135.05	8.7	12.94
SVPWM	180 Nm	2k	83.82	72.03	14.1	95.74	179.56	167.77	6.6	11.79
SVPWM	20 Nm	5k	27.54	21.13	23.3	4.77	32.31	25.90	19.8	6.41
SVPWM	40 Nm	10k	77.00	60.40	21.6	28.02	105.02	88.42	15.8	16.61
SVM+OVM	40 Nm	10k	19.92	15.17	23.8	23.97	43.89	39.14	10.8	4.75

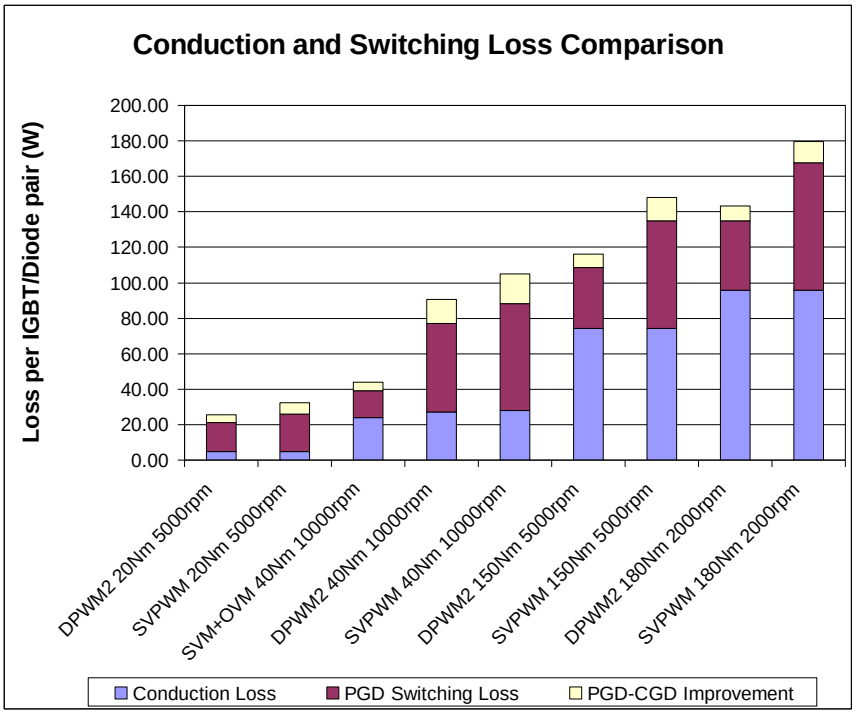


Figure 6-8: Graphical representation of loss comparison between CGD and PGD

Turn-on and turn-off loss comparisons between the conventional and the proposed gate drivers are demonstrated in Fig. 6-9 and 6-10.

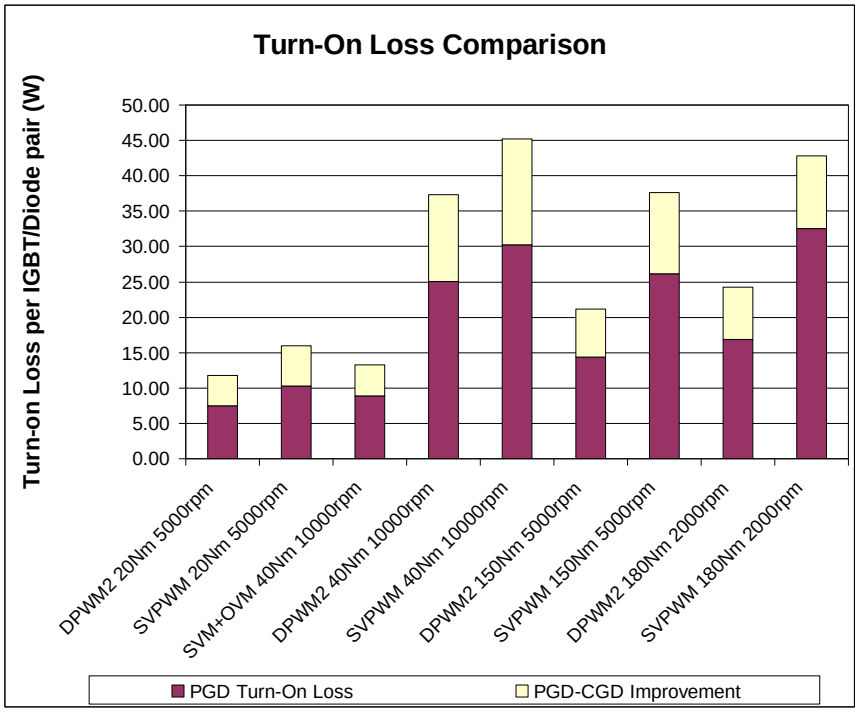


Figure 6-9: Turn-on loss comparison between CGD and PGD

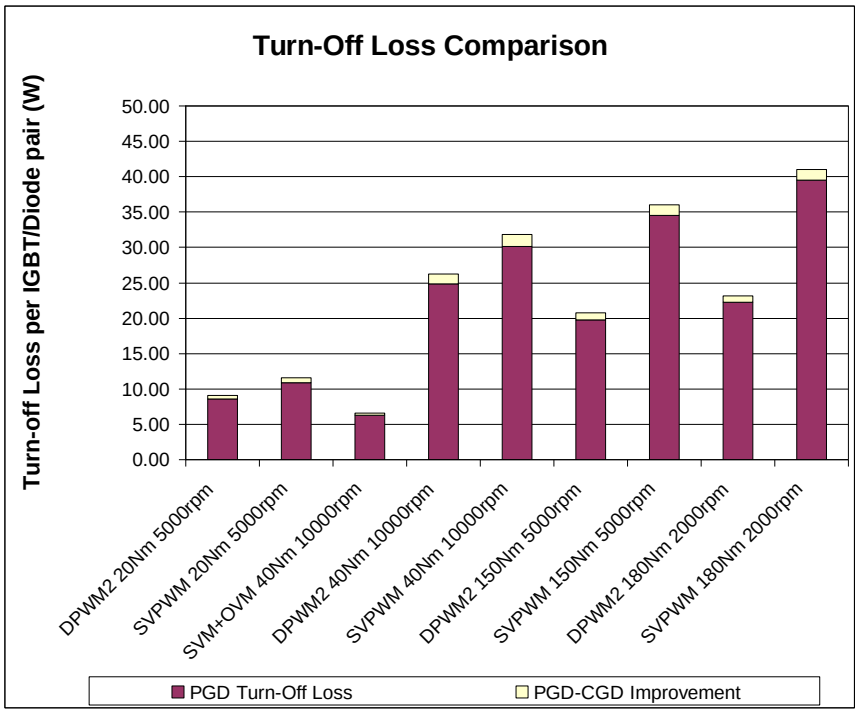


Figure 6-10: Turn-off loss comparison between CGD and PGD

6.4. Effects on EMI emissions

In order to see the impact of using the newly developed variable-speed gate driver on EMI, its generated EMI spectrum needs to be compared to a conventional fixed speed driver's EMI spectrum. EMI emissions in MHz range are closely related to di/dt and dv/dt across IGBTs [26]. Simulation results of the new gate driver's operation in closed loop reveal that di/dt is being varied much greater than dv/dt during one cycle of output AC load current fundamental frequency. Therefore, the spectrum of IGBT current waveforms will be compared. Time-domain IGBT current waveforms are presented for comparison in Fig. 6-11. The PWM sequence and the load current have been obtained from a simulation of the 54 kW motor [47] at 6000 rpm using DPWM2 modulation. The IGBT current overshoots were added later on top of the waveform, based on separate gate driver simulation results, after enhancing the resolution of time scale using spline interpolation.

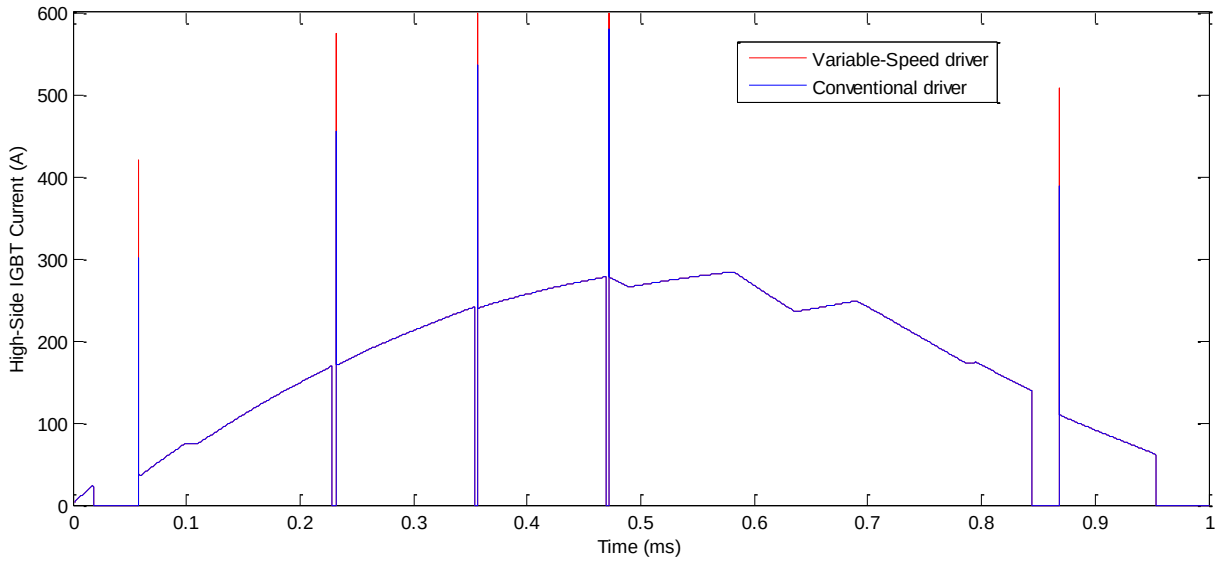


Figure 6-11: High-side IGBT current for half-cycle of load current

Since other half-cycles are similar, this is the minimum time frame required to perform FFT for spectrum analysis. Fig. 6-12 is the direct FFT of waveforms in Fig. 6-11, showing the difference between the two emitted spectra. It can be observed that the variable-speed IGBT

gate driver produces more EMI noise above approximately 5 MHz, but there is almost no change in spectrum below 5 MHz.

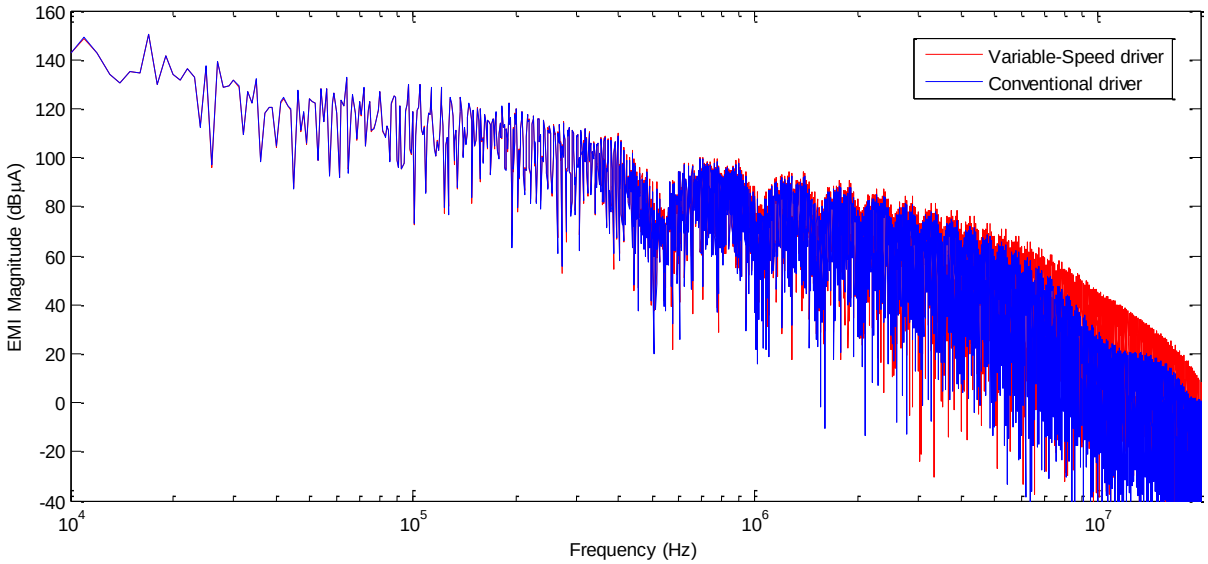


Figure 6-12: Generated EMI spectrum in high-side IGBT

Chapter 7:
Conclusion and Future Work

7.1. Summary

This thesis describes how multiple IGBT gate driving techniques proposed by literature have been tested and compared. Based on observations during testing, a new gate driver output stage circuit has been introduced, allowing continuous (analog) control over switching losses and overshoots of voltage and current. Following that, a new method of IGBT driving strategy has been introduced. This method maximizes the IGBT SOA utilization in order to reduce switching losses by using variable-speed gate driver output stages. An adaptive feedback control algorithm has been developed to set the switching speed of each PWM transition. The algorithm performance and stability have been verified through simulation on a 2-level 3-phase motor drive converter. Finally, loss reduction has been estimated, relative to conventional fixed-speed gate driver output stages.

7.2. Conclusion

Comparing switching losses of the proposed gate driver to the conventional one, the switching loss reduction is around 25% for most combinations of tested motor torque, speeds, and modulation schemes. As presented in the switching loss reduction concept, most of the effect is achieved for turn-on (20% reduction) with the rest 5% reduced for turn-off. Taking into account conduction losses, the overall converter loss reduction can vary approximately between 5% and 20%. An additional conclusion can be drawn regarding modulation scheme usage: because DPWM2 already takes care of preventing IGBTs from switching at high load currents, the proposed method has greater effect for SVPWM, where motor losses are generally lower.

This method only has effect in DC/AC conversion (in both ways), and can possibly be used in AC/AC matrix converters. In DC/DC conversion this method will not have much effect

with steady load, because it relies on load current or source voltage variation. Multilevel converters can also benefit from this method, in case the converter supports current measurement for every IGBT.

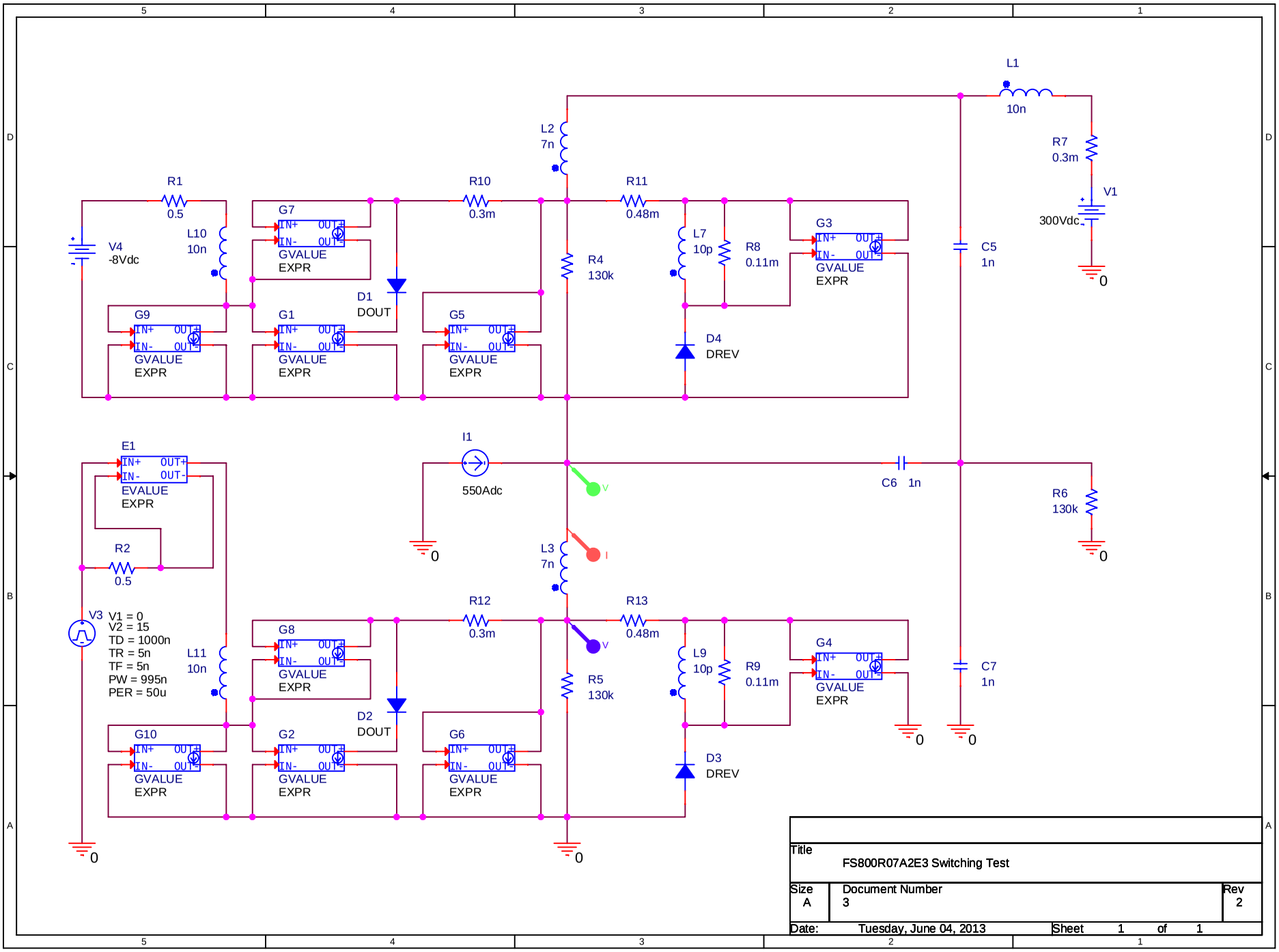
7.3. Future work

This research needs future work for real implementation. Gate driver output stages need to be scaled up or down depending on ratings of the IGBT device used in application. Voltage and current sensors also have to be designed for the scale of application. Even though the algorithm is written in a way close to real application, it still needs to be converted to a processor-compatible language (e.g. C), and the target processor needs to be selected to support the maximum PWM frequency. The algorithm might need to be optimized for speed of execution at the expense of calculation precision and/or program memory space required on the CPU. Protection schemes need to be integrated into the system, either into the algorithm, as a separate CPU interrupt, or as extra hardware logic after the CPU. The final verification of the concept is always a full-scale hardware test of the complete system, which can only be accomplished after all additional tasks above have been completed.

Appendix

Appendix A: PSpice component parameters and schematic

```
D1, D2     .MODEL DOUT D IS=3 N=7 RS=0 CJO=0

D3, D4     .MODEL DREV D IS=0.43 N=5.5 RS=0 CJO=0

G1, G2     IF(V(%IN+, %IN-) < 6, 0, IF(V(%OUT+, %OUT-) < (V(%IN+, %IN-) - 6) /
           1.7, 1.7 * 130 * ((V(%IN+, %IN-) - 6) * V(%OUT+, %OUT-) - 1.7 *
           V(%OUT+, %OUT-) * V(%OUT+, %OUT-) * 0.5), 130 * (V(%IN+, %IN-) - 6)
           * (V(%IN+, %IN-) - 6) * 0.5))

G3, G4     V(%IN+, %IN-)*9k

G5, G6     IF(V(%IN+, %IN-) < 0, 5.152962374n * DDT(V(%IN+, %IN-)),
           5.756140351n * DDT((V(%IN+, %IN-) + 0.35) ** 0.57))

G7, G8     IF(V(%IN+, %IN-) < 0, 5.152962374n * DDT(V(%IN+, %IN-)),
           5.756140351n * DDT((V(%IN+, %IN-) + 0.35) ** 0.57))

G9, G10    IF(V(%IN+, %IN-) < 8.5, 52n * DDT(V(%IN+, %IN-)), 150n *
           DDT(V(%IN+, %IN-)))

E1         IF(V(%IN+, %IN-) > 0, -V(%IN+, %IN-) * 2 * 3.3, -V(%IN+, %IN-) * 2
           * 6.2)
```



Title	FS800R07A2E3 Switching Test	
Size A	Document Number 3	Rev 2
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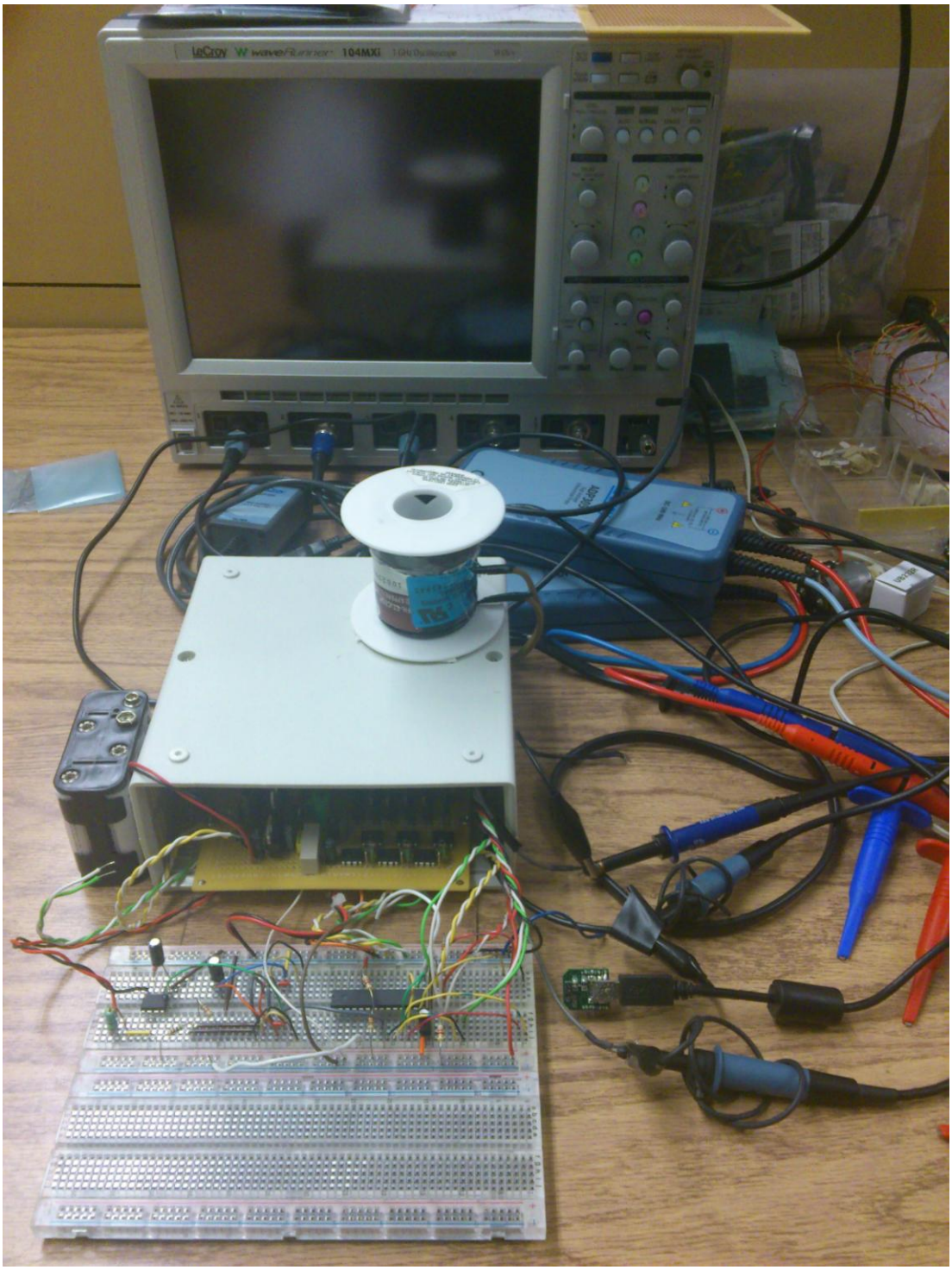
Appendix B: Hardware setup for double-pulse testing



Appendix C: List of publications

- A. Sokolov, D. Mascarella, and G. Joos, "Variable-Speed IGBT Gate Driver with Loss/Overshoot Balancing for Switching Loss Reduction," in *Energy Conversion Congress and Exposition, 2014 IEEE*, in press.
- A. Sokolov, D. Mascarella, and G. Joos, "Variable-Speed IGBT Gate Driver Control and Effects on Automotive Systems," in *Applied Power Electronics Conference and Exposition, 2015 IEEE*, pending.

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