A PROGRAMMABLE ANALOG GAUSSIAN NOISE GENERATOR FOR TEST APPLICATIONS

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Abstract

This thesis presents a robust programmable analog Gaussian noise generator suitable for mixed-signal test applications. Unlike conventional methods, noise generators employing a linear feedback shift register (LFSR) or resistor thermal noise amplification techniques, the user has full control over the characteristics of the Gaussian signal. Indeed, the frequency band, the mean, and the variance of the distribution are fully programmable over the voltage range within the supply rails. The method consists of digitally encoding the specified Gaussian signal in a random access memory (RAM), using pulse-density modulation, followed by filtering the output bit stream using an analog low-pass filter. It is demonstrated that the quality of the generated noise signal is independent of the quality of the filter used; hence, making the noise source highly robust. The output of the noise generator accurately models a real Gaussian signal, even at high sigma values; thus, making it a very effective and predictable dithering signal. Two applications of the proposed Gaussian noise source are demonstrated: histogram testing of analog-to-digital converters (ADCs) and high-resolution digitization. In addition, a high-voltage automotive test instrument that supports the high-resolution digitization process proposed is outlined.

Résumé

Ce mémoire présente un générateur de bruit Gaussien programmable pouvant servir au test de circuits à signaux mixtes. Contrairement aux méthodes conventionnelles (générateurs de bruit utilisant un registre à décalage rebouclé ou basé sur l'amplification du bruit thermique d'une résistance), les caractéristiques du signal Gaussien sont toutes contrôlables. En effet, la bande de fréquences, la moyenne et la variance de la distribution sont toutes programmables à l'intérieur de l'intervalle de la tension d'alimentation. La méthode consiste à encoder numériquement un signal Gaussien dans une mémoire vive, en utilisant la modulation sigma-delta, et filtrer la séquence de bits produite en utilisant un filtre passe-bas analogique. Il est démontré que la qualité du signal de bruit généré est indépendante de la qualité du filtre utilisé permettant ainsi à ce générateur d'être hautement robuste. La distribution du bruit produit se rapproche de façon très précise à celle d'un signal Gaussien idéale. Deux applications sont démontrées: le test par histogramme de convertisseurs analogiques-numériques et la conversion analogique-numérique à très haute résolution. De plus, un instrument de test à haut-voltage pour la prochaine génération d'automobiles utilisant le processus de digitalisation proposé est suggéré.

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CHAPTER 1

Introduction

It is known that testing is an important and essential phase in the manufacturing process of integrated circuits. In fact, the only way that manufacturers can deliver high quality chips in reasonable times is through an extensive testing process. However, the integration of mixed technologies (analog, digital, RF, MEMS) as well as third party IP cores in system-on-chip devices (SoC) causes a loss of test access and longer testing times [1]. In fact, testing this "new generation" of integrated circuits (ICs) can no longer be done efficiently with the current approaches, automated test equipment (ATE); therefore, new more efficient techniques must be used.

For purely digital cores, test access methodologies and design-for-test techniques, such as IEEE 1149.1 test wrappers [2], already exist and are heavily used. This is because in the digital domain, test patterns can be transported efficiently through the chip boundary. In contrast, the signals in analog cores tend to degrade rapidly when transported because analog devices are more affected by noise and distortion than their digital counterparts. As depicted in Figure 1.1, in a near future it is expected that the cost to produce a mixed-signal SoC will be dominated by the analog testing costs [1]. It is therefore obvious that if IC manufacturers want to remain competitive, they must find new cheaper ways to test the analog portion of mixed-signal devices.

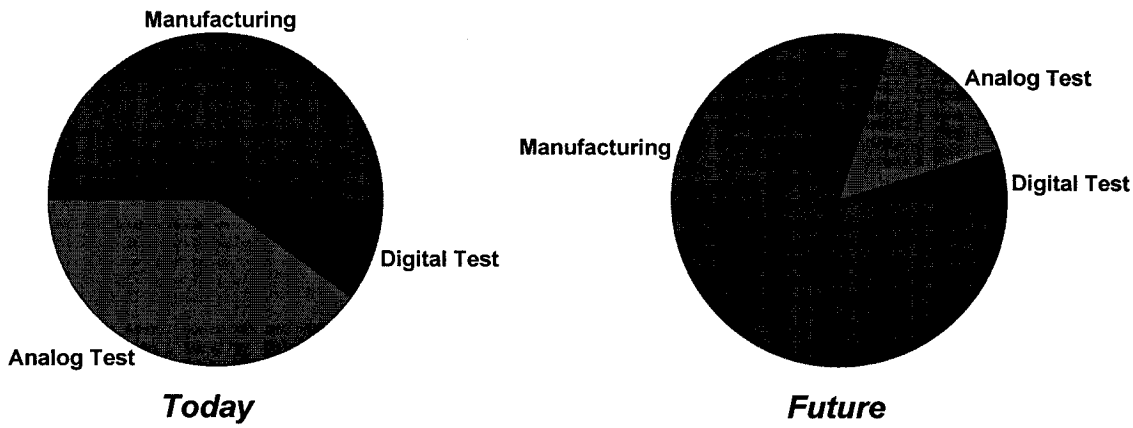

Figure 1.1: Cost to produce a mixed-signal SoC. Breakdown of relative manufacturing, analog test, and digital test costs for today and predicted future [1].

1.1 On-Chip Mixed-Signal Test

One solution to the above problem is the integration of easily accessible "on-chip testers". In [3], the integration of on-chip arbitrary waveform generators (AWG) and periodic waveform digitizers, basically what is needed for DSP-based testing, has been realized. In the testing industry, DSP techniques have proved to be very efficient. In fact, DSP based testing reduces test time and allows advanced signal manipulation (e.g. separation of signal components and interpolation between samples to obtain better time resolution). Consequently, most ATE machines are built such that DSP testing is supported [4]. The block diagram of these so-called "on-chip testers" is available in Figure 1.2. As shown, the test-core consists of a band-limited arbitrary waveform generator and a periodic waveform digitizer both synchronized with the same clock source. Traditionally, the test stimuli used in these test-cores have been sinusoidal signals. Another approach could be to use a white Gaussian signal as the test input. In fact, a Gaussian signal is relatively immune to noise as its presence will only increase

the standard deviation without altering the distribution (given that all the non-desired noise follows Gaussian statistics). Also, a white Gaussian signal has a flat magnitude spectrum which can allow the testing of a device under its entire band of operation using a single stimulus; hence, possibly reducing the cost of test.

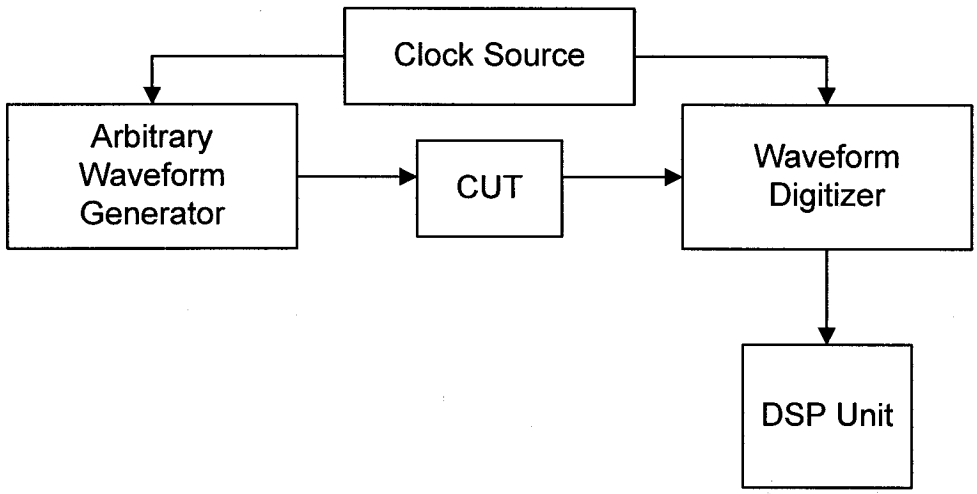

Figure 1.2: Block diagram of mixed-signal on-chip test system.

1.2 The use of a Gaussian Signal in Mixed-Signal Testing

Many physical phenomena in electronics can be modeled by a Gaussian distribution. This includes thermal noise in resistors, oscillations in power supplies, interference signals in transceivers, and jitter in clocks. This is mainly attributable to the Central Limit Theorem which states that even when individual random variables are not normally distributed, their sums and averages will tend to follow a normal distribution [5]. Being able to accurately model these effects is paramount when testing various electronic components. A random noise generator circuit has a wide variety of applications ranging from electronic testing and modeling to communication channel

emulation. For example, noise-like signals can be used to find the bit error rate in digital communication channels. In addition, in [6] it has been shown how histogram testing using a Gaussian noise stimulus is performed for video-rate analog-to-digital converters (ADCs). Typically analog Gaussian noise signals are generated either by low-pass filtering the output of a linear feedback shift register (LFSR) or by amplifying the thermal noise of a resistor. Both these methods do not allow the user to define the characteristics of the noise signal. The generated signal in the first method does not accurately follow a normal distribution and the second method is highly subject to process variations. Digital implementations of pseudo-random Gaussian signal sources employing techniques such as the Box-Muller method, described in [7], have successfully been realized in [8], [9], and [10]. However, converting those multi-bit digital signals to the analog world is not a trivial task as this would require very stringent digital-to-analog conversion specifications. In this thesis, a novel highly robust and programmable analog Gaussian noise source that accurately follows a normal distribution even at high standard deviation values is presented. A paper outlining the implementation of the proposed generator along with experimental results has been accepted for publication and will be available in [11].

1.3 Thesis Overview

This thesis documents our solution to the testing challenges described previously. The first chapter introduces the topic of this work and provides an overview of the objectives. The following chapter presents the background theory required for the understanding of this thesis. The basic properties of Gaussian random variables are outlined along with the principles of $\Sigma\Delta$ modulation and its use in signal generation for built-in-self-test (BIST) applications. Chapter 3 describes the current state of the art in Gaussian noise generation. The two methods described are: LFSR based noise generators and resistor thermal noise amplification techniques. The proposed programmable Gaussian noise generator is described in Chapter 4. A Matlab/Simulink implementation of the noise generator is presented with simulation examples investigating its robustness and required memory size. Also, a hardware implementation is demonstrated and experimental results are discussed. In Chapter 5, applications of the Gaussian noise source are demonstrated. The proposed applications are: ADC histogram testing and high-resolution digitization. Chapter 6 presents a fully integrated mixed-signal automotive test instrument for the 42 V powernet that uses the digitizer suggested in Chapter 5. Finally future directions of this work are suggested and conclusions are drawn in Chapter 7.

CHAPTER 2

Background Theory

2.1 Gaussian Distribution Background Theory

The Gaussian distribution is omnipresent in the world of electronics because the thermal noise in circuits accurately follows Gaussian statistics. The probability density function of a Gaussian signal is completely defined by its mean μ and standard deviation σ. A continuous random variable is said to have a normal distribution with parameters μ and σ if its corresponding pdf is

$$f(x;\mu,\sigma)=\frac{1}{\sqrt{2\pi}\sigma}e^{-(x-\mu)^2/(2\sigma)^2},\quad -\infty<x<\infty \quad [5]. \tag{2.1}$$

Referring to Figure 2.1, the probability that a random variable X will be less than a value 'a' is given by the cumulative distribution function F(a) defined as

$$F(a)=\int_{-\infty}^{a}\frac{1}{\sigma\sqrt{2\pi}}e^{\frac{-(x-\mu)^2}{2\sigma^2}}dx. \tag{2.2}$$

Note that in the case where the parameters μ and σ are equal to zero and one respectively, the normal distribution is known as a standard normal distribution. A random variable having a standard deviation is denoted as Z. Probabilities are often computed by "standardizing" the random variable X by subtracting μ from it and

dividing the result by σ. Doing so shifts the mean to zero and scales the standard deviation to one; hence, mapping X to Z. Often F(a) is written in terms of the standardized cumulative distribution Φ(z),

$$F(a) = \Phi(\frac{a-\mu}{\sigma}) = \Phi(z). \tag{2.3}$$

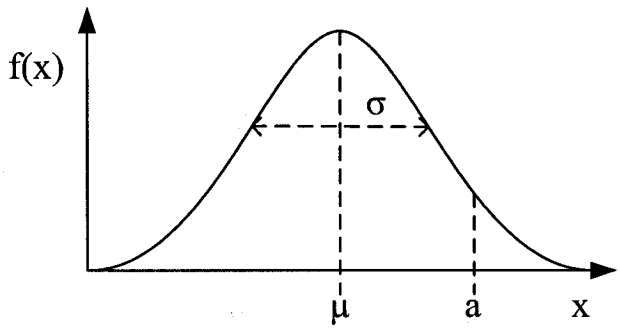

Figure 2.1: Probability density function of a Gaussian random variable.

2.2 ΣΔ Modulation Background Theory

The basic architecture of a first order ΣΔ modulator is depicted in Figure 2.2. ΣΔ modulators are basically oversampling analog-to-digital converters, meaning that the sampling rate of the signal is increased to the point where a low-resolution quantizer is enough for accurate digitization. The amount of oversampling is defined by the oversampling ratio

$$OSR = \frac{f_S}{2f_B}. \tag{2.4}$$

The digital output of the ΣΔ modulator corresponds to a pulse-density modulated version of the input signal.

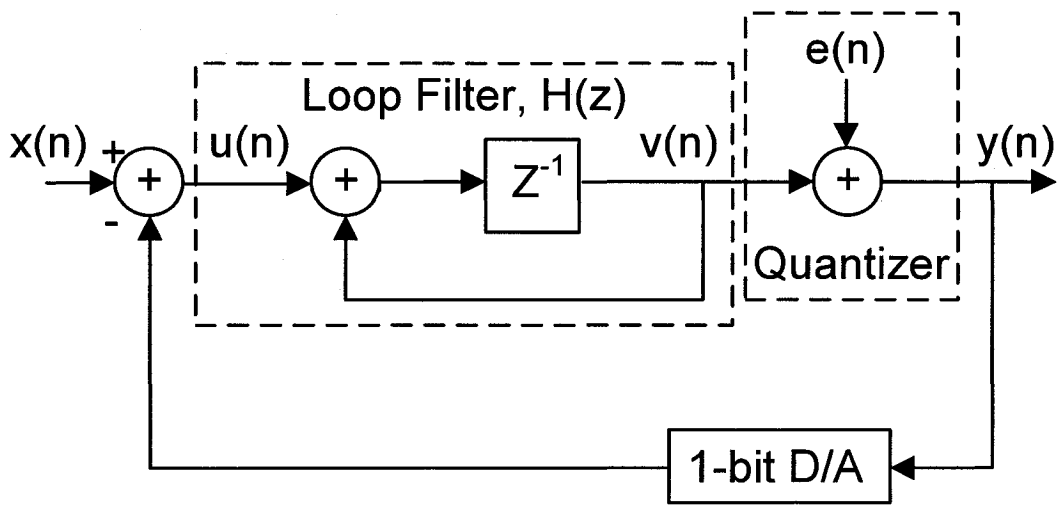

Figure 2.2: First order ΣΔ modulator architecture.

Referring back to Figure 2.2, the time domain difference equation mapping the input signal to the output signal is

$$y(n) = x(n-1) + [e(n) - e(n-1)], \tag{2.5}$$

where e(n) denotes the quantization noise of the quantizer. The frequency domain representation of (2.5) can easily be verified to equal

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1}) = STF(z)X(z) + NTF(z)E(z). \tag{2.6}$$

Note that Y(z) is composed of two transfer functions where the first one, z^{-1}, corresponds to the signal transfer function (STF) while the second, $(1-z^{-1})$, is the noise transfer function (NTF) [12]. As shown in Figure 2.3, the STF has a unity magnitude response while the magnitude response of the NTF starts at zero and increases to a value of two as it approaches $F_S/2$. This effect of pushing the quantization noise out of the bandwidth of interest is referred to as noise shaping and is a very powerful feature of ΣΔ modulators. Indeed, the high frequency quantization noise can be removed to recover the input signal by means of a simple low-pass filter connected to the output of the modulator.

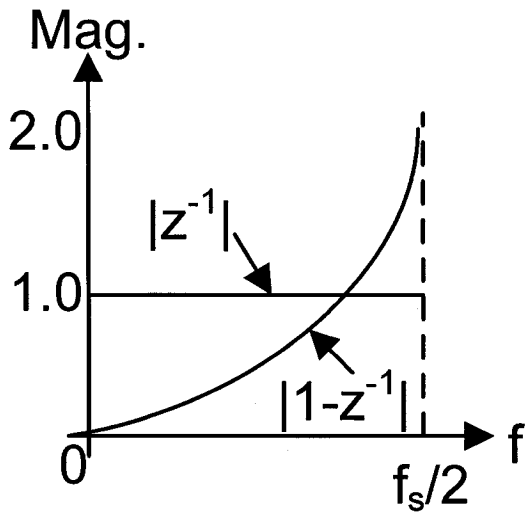

Figure 2.3: Signal and noise transfer function.

More generally, high order modulators can be implemented by utilizing more error history. For example, a second order modulator can be implemented by subtracting the previous two samples of the error signal to the current one. In many applications, such as analog signal generation for BIST, it is beneficial for the STF to always be equal to one. This is mainly because of stability issues associated with ΣΔ modulators embedded in oscillators. A topology that ensures a unity transfer function was first suggested in [13] and is often used for software generation of pulse-density modulated test stimulus for BIST applications. One can see from Figure 2.4 that for this topology the input signal feeds straight to the output and back to the filter input; however, it also feeds forward to the filter input with the opposite sign hence cancelling the signal feedback and resulting in a unity STF [14]. Note that here the NTF is equal to 1/(1+H(z)).

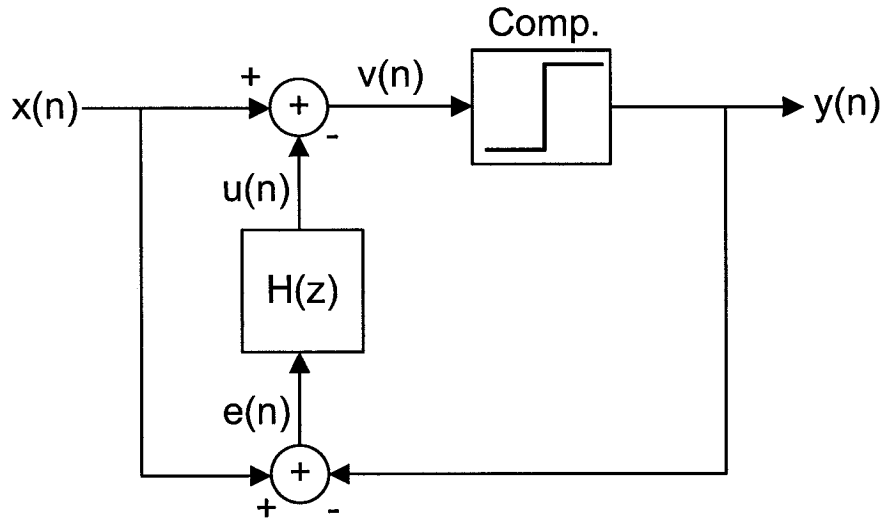

Figure 2.4: General delta-sigma modulator structure with unity signal transfer function.

2.3 Analog Signal Generation

Figure 2.5 shows the block diagram of an on-chip arbitrary waveform generator. In order to synthesize the analog test stimulus, a short sequence of digital bits is repeated as to approximate the output of a 1-bit ΣΔ modulator when driven by a periodic signal. As described in [15], the method consists of simulating a high-order noise-shaping modulator, as the one depicted above, and collecting a finite number of output samples. A periodic repetition of this sequence approximates the output of an infinite-duration ΣΔ oscillator (it is this sequence that is stored in the periodic bit stream generator of Figure 2.5). In order to obtain a periodic waveform, the output bit sequence must be periodic with a period of N/F_S, where N is the length of the sequence and F_S is the sampling frequency. Thus, the input signal to the ΣΔ modulator has to be harmonically related to the fundamental frequency of the bit sequence (i.e. Fs/N). Since

the approximate ΣΔ modulated output is forced to be periodic, it implies that the encoded signal contains only a finite number of frequencies [15]:

$$F_{out} = \frac{M}{N} F_S, \quad M = 0,1,2,..., N/2. \tag{2.7}$$

This characteristic of the bit-stream generator ensures sample coherence with the on-chip waveform digitizer. As described in [4], coherent sampling requires only a small number of samples for DSP-based testing, also in the situation of under-sampling digitizers, coherency allows test results to easily be tracked.

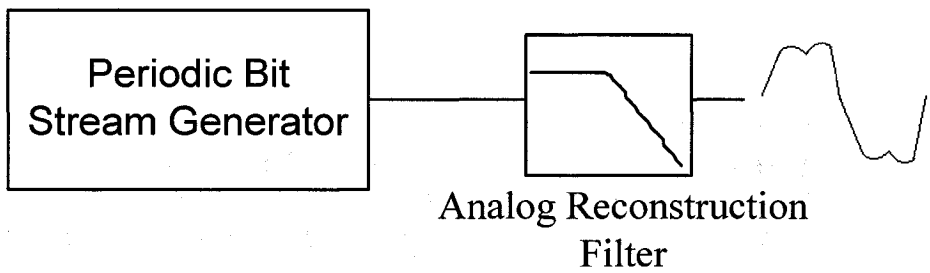

Figure 2.5: On-chip arbitrary waveform generator.

Figure 2.6 shows a typical spectrum of a periodically repeated sequence of a ΣΔ modulated bit stream. As a consequence of the noise shaping nature of pulse density modulation, as long as the encoded signal has a small enough bandwidth, it will have low distortion harmonics when filtered using a properly tuned low-pass filter.

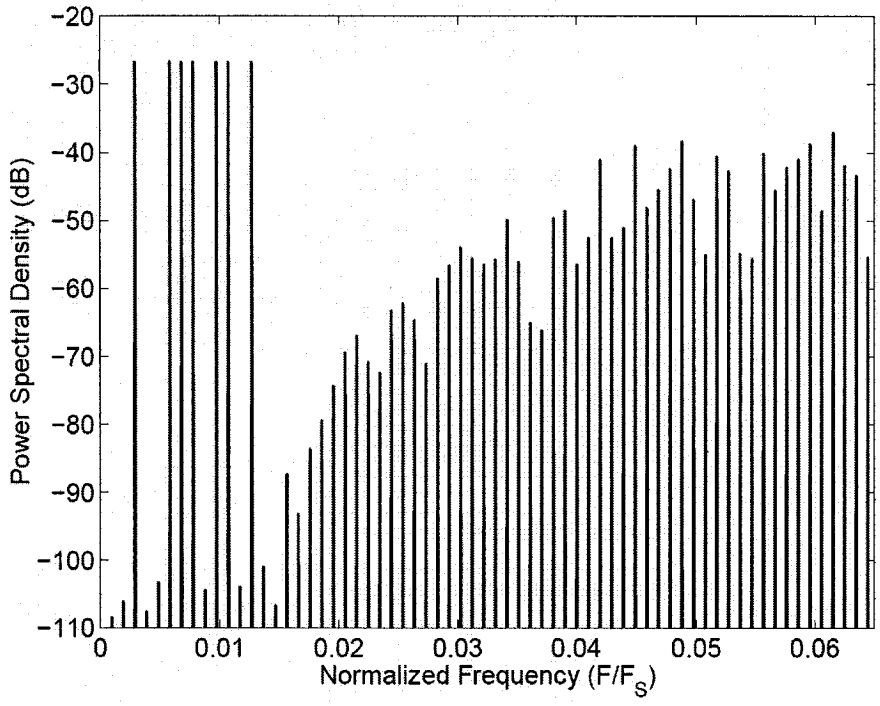

Figure 2.6: Typical spectrum of a periodically repeated finite-duration ΣΔ modulated bit stream encoding a multi-tone signal [16].

2.4 Summary

This chapter provided the basic background theory necessary for the comprehension of the principles of operation of the Gaussian noise source presented in this thesis. A review of the Gaussian distribution along with a description of its probability density function and cumulative distribution was discussed. In addition, the concept of ΣΔ modulation was introduced and its use in analog signal generation for BIST applications was outlined.

CHAPTER 3

State of the Art in Analog Gaussian Noise Generation

This chapter summarizes the traditional methods for analog Gaussian noise generation. In general, analog noise signals having a normal distribution are generated either by low-pass filtering the output of a linear feedback shift register or by amplifying the thermal noise of a large register.

3.1 LFSR-Based Noise Source

Linear feedback shift registers (LFSRs) are a very common way to generate a sequence of binary words. A carefully connected two-input exclusive-OR gate is the only hardware required to allow a shift register to output, by successive shifts, all of its possible non-zero values. The applications of LFSRs include: error-correcting codes, pseudorandom sequence generation for ranging and synchronization, test-pattern generation and signature analysis in VLSI circuits, and programming counters in simple computers. It has also been demonstrated in [17] that a LFSR produces a pseudo-random bit stream that can be used as a pseudo-noise source. To eliminate the DC offset of the LFSR and hence obtain a mean of 0 V, a DC level shifter that maps the high digital values to V_{DD} and low values to $-V_{DD}$ can be used. A simple RC low-pass filter

connected to the output of the level shifter is then used to generate the analog noise for the required frequency band.

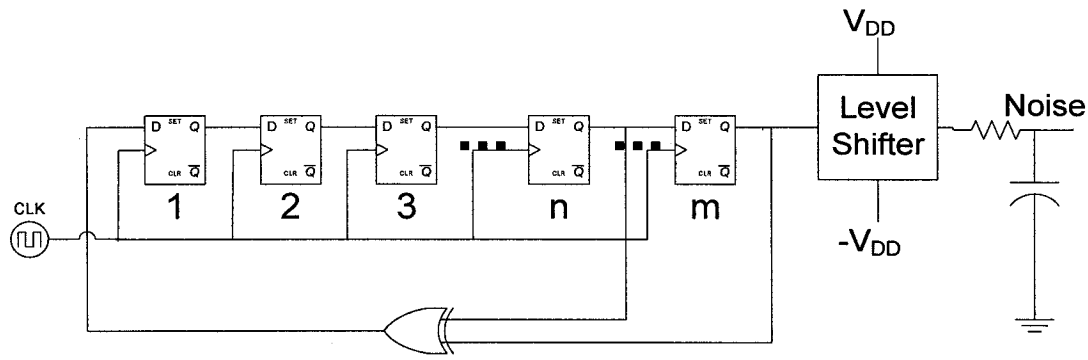

Figure 3.1: A pseudo-random noise source.

It has been demonstrated in [17] that the spectral density of the noise signal can be expressed as

$$S(f) = V_{DD}{}^2 \frac{2}{f_{clock}} \quad V^2/Hz, \quad f \le 0.2 f_{clk}. \tag{3.1}$$

In order to obtain the noise power, (3.1) must be multiplied by the equivalent noise bandwidth of the filter used. In the case where an RC low-pass filter is used then its equivalent noise bandwidth is

$$B = \frac{\pi}{2} f_{3dB}. \tag{3.2}$$

When (3.1) and (3.2) are combined together, after rearranging the terms the expression for the rms noise voltage becomes

$$V_{rms} = V_{DD}\left(\frac{\pi f_{3dB}}{f_{clock}}\right)^{1/2}. \tag{3.3}$$

For example, if V_{DD} is 1 V and the clock sampling frequency is 64 times greater than the 3 dB frequency of the analog filter, from (3.3) the rms noise voltage should equal 0.221 V. This case was simulated in Matlab with a 15-bit LFSR and the obtained rms noise was 0.219 V which is relatively close to the calculated value. However, as can be observed in Figure 3.2, the main disadvantage of this technique is that the generated noise signal does not have a "good" Gaussian distribution. Also, this method does not allow the user to program the desired mean and variance of the Gaussian noise signal.

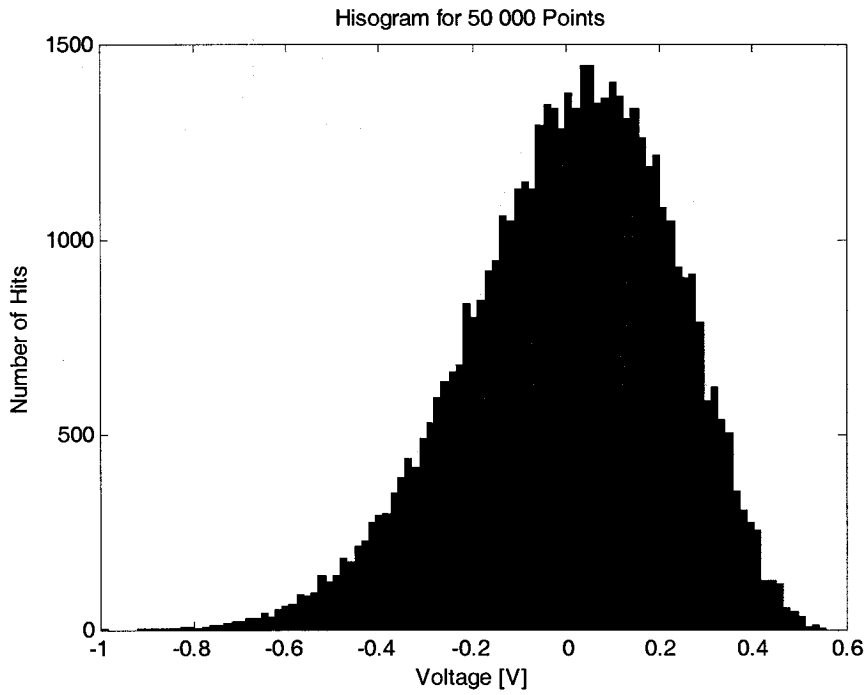

Figure 3.2: Histogram of noise signal for a 15-bit LFSR where V_{DD} = 1 V and f_{3dB}/f_{clk} = 1/64.

3.2 Resistor Thermal Noise Amplification Technique

In [18] and [19] a method to generate continuous-time Gaussian distributed noise by amplifying the thermal noise of a large input resistor using an operational amplifier in a high-gain closed-loop configuration has successfully been implemented. A basic scheme outlining this architecture is depicted in Figure 3.3. The large resistor R_S produces thermal noise that is then amplified. Note that the input capacitance C_{in} of the amplifier in conjunction with resistor R_S act as a low-pass filter that limits the noise bandwidth and power. In the case where a digital random sequence of bits is required, a comparator having its reference voltage set to the mean of the analog noise signal, analog ground, gives a random binary output sequence.

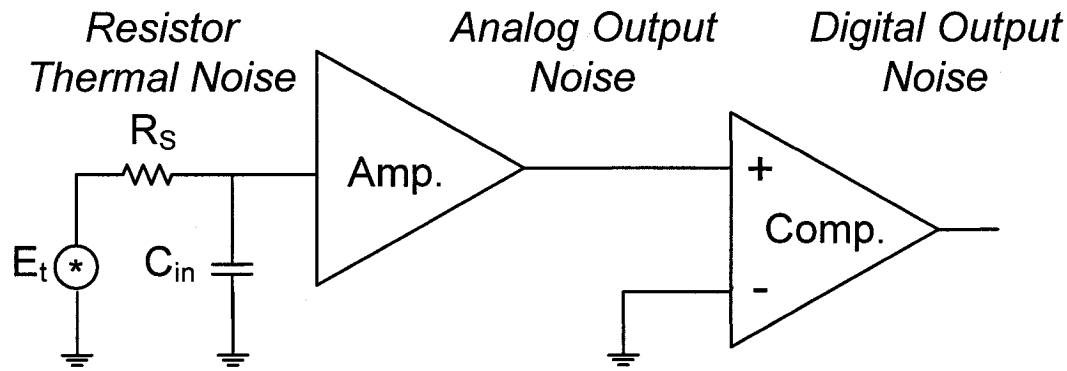

Figure 3.3: Topology of resistor thermal noise amplification method.

Although the random movement of electrons in a resistor produces a noise signal having an accurate Gaussian distribution, other effects such as 1/f noise will tend to affect the distribution. Indeed, it is believed that 1/f noise will affect the tails of the generated Gaussian signal if the noise bandwidth includes low frequencies. Furthermore, this implementation is highly subject to process variations as errors in the resistance, or in the gain and offset of the opamp will alter the mean and variance of the probability density function. As for the LFSR method, the user has no control over the distribution once the circuit is fabricated.

3.3 Summary

The two conventional methods used for analog Gaussian noise generation were presented in this chapter. The first method uses an LFSR to generate a pseudo-random bit sequence which is then converted to analog noise using a passive low-pass filter. However, the distribution of the generated analog signal is skewed and does not accurately follow a Gaussian distribution. The other method is based on the amplification of the thermal noise generated by a large resistor. Although thermal noise has a relatively good Gaussian distribution, the characteristics of the generated signal (mean, standard deviation, and frequency band) are heavily influenced by process variations. Furthermore, both these topologies do not allow the user to change the characteristics of the Gaussian signal once implemented.

CHAPTER 4

Proposed Programmable Gaussian Noise Source

4.1 Basic Description

Since there is currently no accurate and programmable analog Gaussian noise source available and although such a signal is often desired in some test applications (e.g. ADC histogram testing and multi-tone testing), a high-quality Gaussian noise source where the mean, standard deviation, bandwidth, and center frequency are user-defined is proposed. As depicted in Figure 4.1, the overall objective is to design a noise generator where all the characteristics of the Gaussian signal output would easily be adjustable through various "knobs".

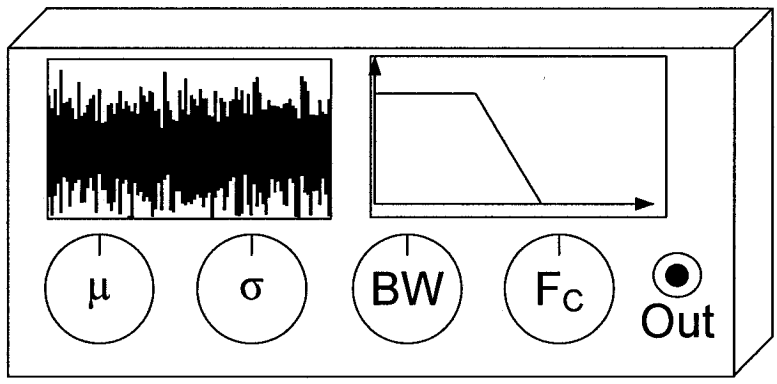

Figure 4.1: Gaussian noise source and its various knobs.

The proposed method to generate a high quality programmable Gaussian noise signal uses the concept of ΣΔ modulation and exploits its noise shaping characteristic. As described in section 2.3, to synthesize a periodic analog test stimulus (e.g. a sinusoid), a sequence of digital bits is repeated as to approximate the output of a 1-bit ΣΔ modulator and then filtered using an appropriate analog low-pass filter. Based on this approach, a method to generate a band-limited periodic signal having a Gaussian probability density function is presented. Recall that ΣΔ modulators require a sampling rate many times greater than the Nyquist rate of the signal being sampled. Therefore, in order to use the concept of ΣΔ modulation, the input signal to the modulator must have a finite bandwidth. Consequently, if we want to obtain pulse-density modulated bits representing a Gaussian noise signal, we must ensure that it is band-limited. One way to achieve this is to low-pass filter a white Gaussian noise signal and then apply it to the modulator.

The diagram shown in Figure 4.2 depicts the method to generate a noise signal having a Gaussian distribution. Note that all the components connected before the analog low-pass filter are only required to generate the bit pattern of the encoded Gaussian signal; thus, they can just be replaced by a memory block and do not have to be implemented in hardware. The process to generate the ΣΔ bits is as follows: first a white Gaussian noise source is connected to a digital low-pass filter (or band-pass depending on the application). Then, the output of the filter (band-limited Gaussian noise) is applied to a ΣΔ modulator. The output sequence of the modulator is collected

and corresponds to the bit stream of the pulse-density encoded noise signal. The pulse-density modulated signal is then applied to a low-pass filter to convert it to analog form.

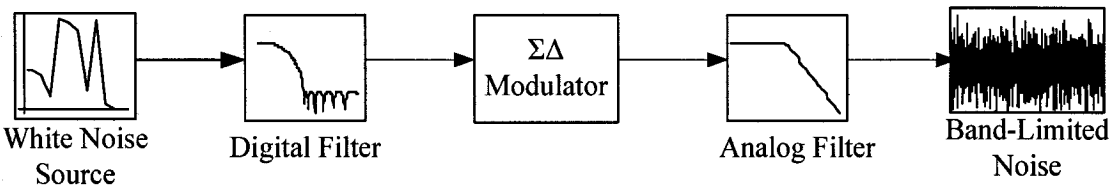

Figure 4.2: Band-limited Gaussian noise generator diagram.

4.2 Matlab Implementation

The ΣΔ Gaussian noise generator described above was implemented in Simulink. For the simulation, in order to comply with the 3.3 V hardware implementation described in the following section, the upper voltage level V_{DD} and lower voltage V_{SS} are set to 1.65 V and -1.65 V respectively. The value of the desired mean μ has initially been set to 0 V. Also, to ensure that the tails of the distribution are properly represented, the standard deviation is programmed to cover a range more than 5σ away from the mean in either direction before getting clipped by the supply rails. Indeed, the standard deviation is set to 0.30 V. Note that the white Gaussian noise source needs to have a higher σ to compensate for the energy lost when the signal is low-pass filtered.

The digital low-pass filter used to band-limit the Gaussian noise source is a Chebyshev type-2 digital filter of high order with a cutoff frequency of 1.95 kHz. Note

that since this filter will not be implemented in hardware, there are no constraints to its specifications. In this case, a Chebyshev Type 2 is used simply because such a filter has a flat magnitude response in the pass band.

The ΣΔ modulator used to digitally encode the band-limited Gaussian signal is a basic 2^{nd} order modulator having a sampling frequency of 500 kHz; thus, giving an oversampling ratio (OSR) equal to 128. Also note that the ΣΔ modulator does not have any constraints as its purpose is to simply generate the digital bits corresponding to the noise signal. The generated sequence of bits should map the high pulses to 1.65 V and the low pulses to -1.65 V to ensure that the mean of the Gaussian noise signal is 0 V.

The analog filter used to convert the digital bit sequence to an analog Gaussian noise source must be built in hardware; therefore, to investigate its robustness a first order low-pass filter is used in our simulations. As for the digital filter, the 3-dB cutoff frequency of the analog filter is also set to 1.95 kHz. Table 4.1 summarizes the parameters used for every component.

Table 4.1: Parameters used in Simulink implementation.

Block	Parameter	Value
White Noise Generator	μ	0 V
	σ	3.82 V
Digital Filter	Type	Chebyshev Type 2
	F_S	500 kHz
	F_{Pass}	1.95 kHz
ΣΔ Modulator	Order	2
	F_S	500 kHz
Analog Filter	Order	1
	F_{Pass}	1.95 kHz

4.2.1 Simulation Results and Quality Test

For the setup described above, 5 million points have been captured in Matlab. As suggested from the histogram plot in Figure 4.3, the probability density function seems to closely follow a Gaussian. However, simply looking at the histogram plot to see if the distribution accurately follows a Gaussian is difficult as the subtleties in the tails are not easy to observe. To further investigate the "goodness" of the distribution, the normal probability plot is used instead. This plot shows the cumulative probability versus the value of each point in the sample set. The scale of the y-axis is adjusted such that a perfect Gaussian data set would follow a straight line with the mean having a probability of 50 %. From Figure 4.4, it can be seen that when 5 million points are taken

the distribution follows a normal between -1.3 V to 1.3 V, which is 4.33σ away from the mean on either side. In the case where 10 million points are collected, the distribution is Gaussian up to about 5σ away; thus, it is expected that if an accurate distribution at high σ values is required, many samples must be collected.

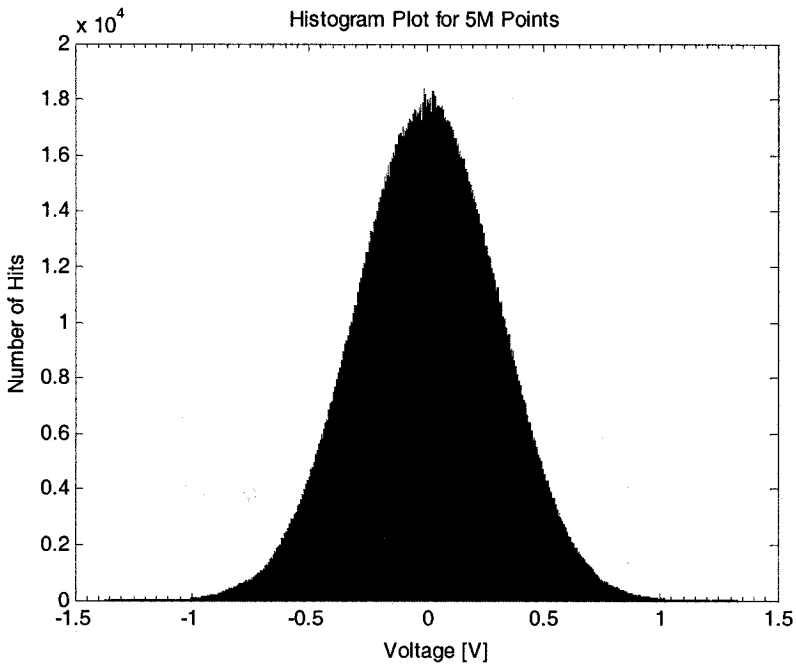

Figure 4.3: Histogram plot for 5M points and 1.95 kHz filter bandwidth.

Another commonly used metric to see how closely a given data set follows a Gaussian distribution is known as kurtosis. This method is a measure of whether the distribution of the data is peaked or flat relative to an ideal Gaussian distribution [20]. In other words, it indicates how outlier-prone a distribution is. Since the kurtosis of an ideal Gaussian distribution is 3, distributions that are more outlier-prone than a Gaussian have a kurtosis greater than 3; those who are less outlier-prone have a kurtosis less than 3. The kurtosis of a data set X is defined as

$$k = \frac{E(x-\mu)^4}{\sigma^4} \tag{4.1}$$

where μ is the mean of X, σ is its standard deviation, and E(t) is the expected value the quantity t. For the setup described in Table 4.1, a kurtosis of 2.98 is obtained which is a bit less than 3, the value for an ideal Gaussian distribution. This suggests that the distribution is slightly less outlier-prone or has shorter tails than a perfect Gaussian. However, this measure provides no information about where the given distribution starts failing to follow an ideal Gaussian distribution (up to how many standard deviations about the mean). Consequently, for the rest of this thesis the normal probability plot is used to investigate the quality of a given distribution as it gives a clearer visual interpretation.

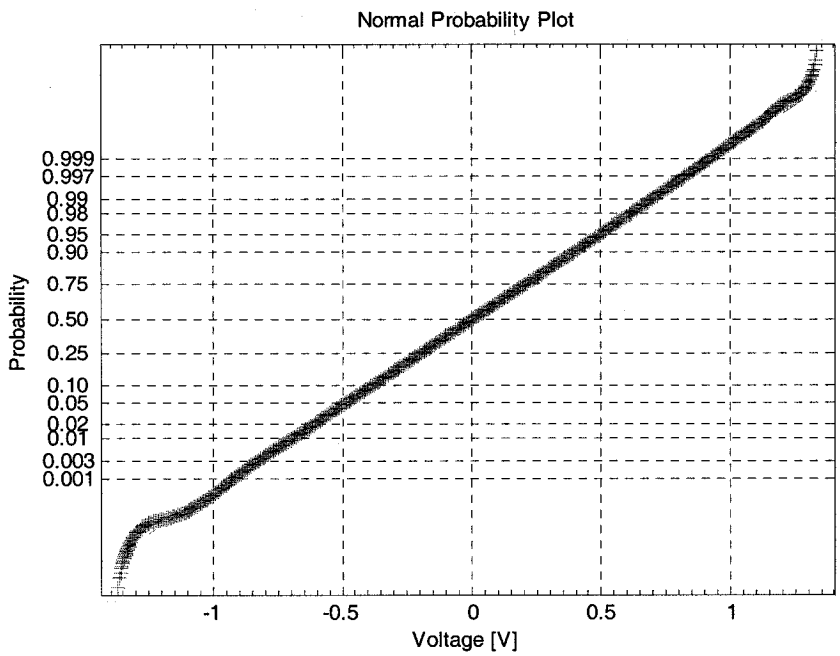

Figure 4.4: Normal probability plot for 5M points and 1.95 kHz filter bandwidth.

4.2.2 Analog Filter Robustness Test

In order to investigate the sensitivity of the noise generator to the analog filtering process, the distribution has been analyzed under different filter bandwidths. It has been observed that as the cutoff frequency is increased, the standard deviation σ also increases. This is no surprise as the wider the bandwidth the more quantization noise appears at the filter output. However, we observed that even though more quantization noise goes through, the quality of the Gaussian signal does not degrade proportionally to the increase in filter bandwidth. For example, it was noted that even if the bandwidth of the filter is five times the nominal, the distribution remains accurate up to around 4σ. In that case, the standard deviation σ increased to 0.36 V but the quality of the tails decreased since the distribution follows a Gaussian only up to 4.16σ on either side. As the filter bandwidth is further increased to ten times the nominal bandwidth, the distribution is relatively accurate up to around 3σ. This can be observed in Figure 4.5 which is a normalized normal probability plot for both cases: five times the nominal bandwidth and ten times the nominal bandwidth. Both normal probability plots were normalized to a Gaussian distribution having a mean μ equal to 0 V and standard deviation σ equal to 1 V in order to obtain a clearer visual interpretation.

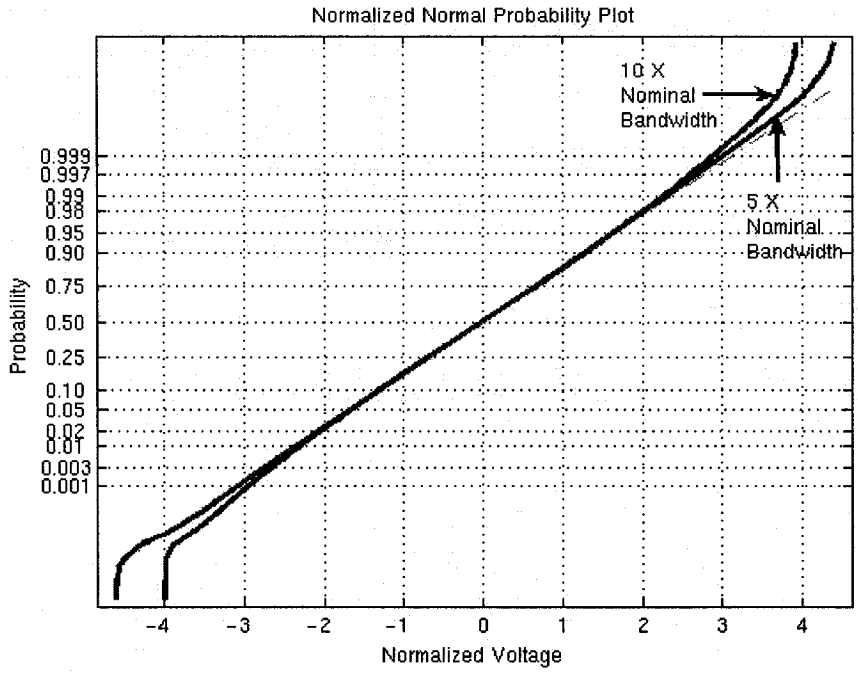

Figure 4.5: Normalized normal probability plot for an analog filter having 5 and 10 times the nominal bandwidth.

4.2.3 Single-Bit Versus Multi-Bit DAC Implementation

Generally speaking, it is advantageous to use ΣΔ modulation to encode band-limited signals because a greater signal-to-noise ratio can be achieved. In addition, ΣΔ modulation can also reduce the hardware costs as only a single bit DAC and filter are required to recover the encoded signal. In situations where a multi-bit DAC and memory are available, such as in common mixed-signal ATE, the same technique can be applied. However, depending on the OSR and number of collected modulated bits, the extra hardware cost of using a multi-bit DAC and memory is not always beneficial. In the case where a high OSR, say 128, and 1 million points are used, the generated Gaussian signal has a high quality even for small standard deviations. In fact, given that the standard deviation sigma is set to 0.15 V, the Gaussian signal is accurate up to about

3.2σ. On the other hand, when a smaller OSR is used and fewer points are collected the quality of the produced Gaussian signal slowly degrades for small standard deviations. For example, when the OSR is set to 32 and that 100 thousand points are collected, as depicted in Figure 4.6, under this scenario the distribution is accurate only up to about 2σ. When a 3-bit DAC is used instead, the quality of the achieved distribution improves to more than 3σ. In other words, it could be advantageous to use a multi-bit DAC to improve the quality of the Gaussian signal when a small standard deviation is required and that a small memory is available. In any other case, there are no real benefits of using a multi-bit DAC over a single-bit.

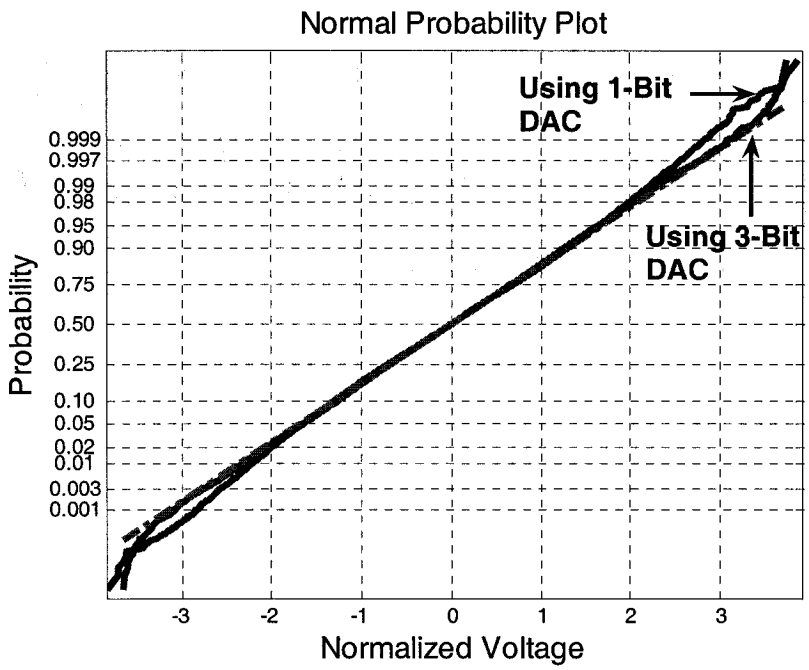

Figure 4.6: Normalized normal probability plot for a σ of 0.15 V, an OSR of 32 and 100 000 collected points. Two cases are shown: 1-bit and 3-bit DAC implementations.

4.2.4 OSR, Memory Size & Signal Quality Tradeoffs

In this section, it is demonstrated that the OSR and required number of points required to encode the Gaussian signal can be reduced at the expense of robustness and signal quality. Indeed, for a standard deviation σ of 0.3 V when the OSR is reduced to 32 and 100 thousand points are taken, the generated Gaussian signal is accurate up to about 4σ. However, if the analog low-pass filter bandwidth is doubled, the quality degrades to 2σ. As discussed above, reducing the OSR also decreases the quality of the Gaussian signal for small standard deviations. In many cases, it is not necessary to go as far as 4σ quality and hence the number of points and memory size can be reduced. In fact, a Gaussian signal has more than 95% of its values within 2σ about its mean. Under the same setup described in Table 4.1 but for an OSR of 32 and a modulator order of 4, 2σ quality can be achieved with only 2.5 thousand points; hence, making it attractive for BIST applications. Table 4.2 shows the required number of points for 2, 3 and 4σ quality.

Table 4.2: Quality of Gaussian signal depending on the number of points for an OSR of 32.

Number of Points	Quality in σ
100 000	4σ
15 000	3σ
2 500	2σ

4.3 Hardware Implementation and Experimental Results

In order to prove the operation of the proposed Gaussian noise generator, a hardware implementation using a field-programmable-gate-array (FPGA) is demonstrated. As mentioned earlier, all the components before the analog filter are only required to generate the pulse-density modulated bit stream representing the digitally encoded Gaussian signal. In other words, they can be replaced by a simple memory block such as a RAM. In this implementation, Matlab/Simulink is used to generate 1.45 megabits that are then used to initialize a RAM block on a Stratix DSP S80 FPGA. Note that 1.45 megabits are used because this is the largest allowable size for the memory initialization file; however, this only corresponds to 19% of the total memory resources of the FPGA [21]. The 3.3 V LVTTL output of the FPGA, which acts as a 1-bit DAC, is then low-pass filtered using a Krohn-Hite 3988 8th order frequency programmable filter box. As for the simulation setup described earlier, the bit sequence coming out of the FPGA is clocked at 500 kHz and the cutoff frequency of the analog filter is initially set to 1.95 kHz which results in an OSR of 128. The generated noise signal captured using an Agilent Infiniium 54830D scope is shown in Figure 12.

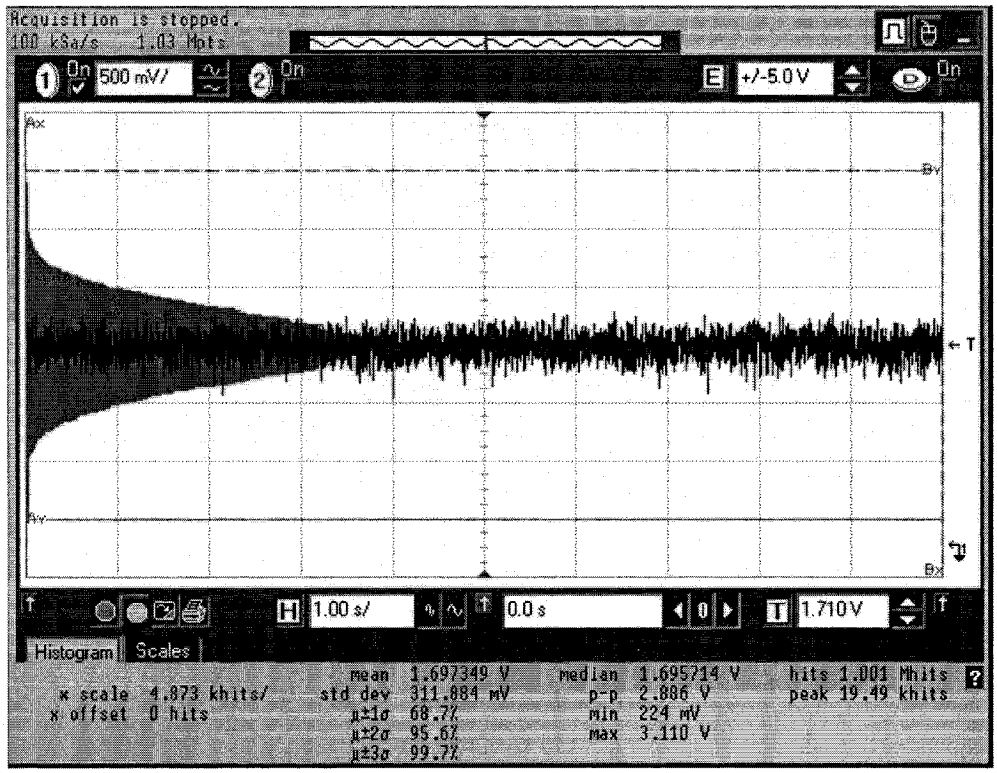

Figure 4.7: Captured generated Gaussian signal using Agilent Infiniium scope. Note that the vertically plotted histogram distribution is superimposed on the horizontally plotted time signal.

The mean and the standard deviation of the measured Gaussian noise signal do not exactly correspond to the programmed values. Indeed, the mean μ was programmed to be 1.65 V and the standard deviation σ to 0.3 V; however, the measured μ and σ are 1.70 V and 0.31 V respectively. This is attributable to the fact that the high and low voltage values of the DAC are not necessarily exactly 3.3 V and 0 V respectively. In fact, the measured high voltage level is 3.41 V whereas the low voltage level is 0 V. Thus, a simple calibration procedure where the exact high and low voltage levels of the 1-bit DAC are determined should always be performed.

A maximum of 1 million points can be captured using the Agilent Infiniium 54830D scope under its "High Resolution" acquisition mode [22]. As can be observed from the normal probability plot of the captured points in Figure 4.8, the tails of the distribution follow a Gaussian distribution up to 3.87σ away from the mean. As suggested from simulation, if the number of pulse-density modulated bits encoding the Gaussian noise signal is increased as well as the number of captured points, the quality of the tails of the probability density function should improve.

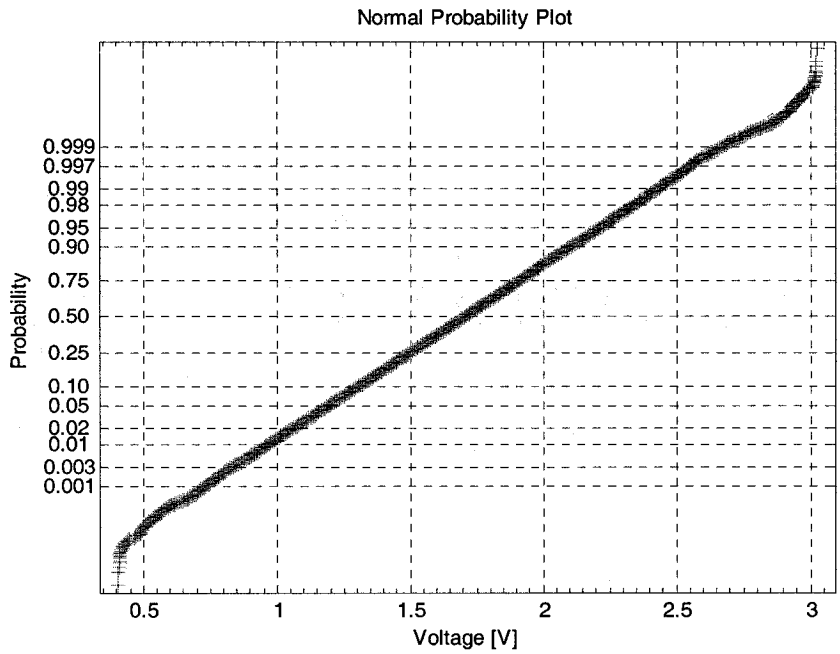

Figure 4.8: Experimental normal probability plot of captured signal when filter has a 1.95 kHz bandwidth.

The robustness of the noise generator was tested by varying the analog low-pass filter bandwidth. In the Matlab simulation example described previously, it was noted that when a first order analog filter is used, the quality of the distribution is relatively

insensitive up to around five times the nominal filter bandwidth. Since under this experimental setup the programmable analog filter used is 8^{th} order, it is expected that the Gaussian noise generation process would be tolerant to higher filter bandwidths as more quantization noise is filtered out by higher order filters. It was observed that when the filter bandwidth is increased by a factor of ten, resulting in a bandwidth of 19.5 kHz, the standard deviation σ increased to 0.32 V but the quality of the distribution is now valid up to 3.75σ away from the mean. Along with the noise-shaping nature of $\Sigma\Delta$ modulation, the insensitivity of the generator to the order and bandwidth of the filtering process can be explained by a dithering of the non-dominant quantization noise level for low enough filter bandwidths. Indeed, it was noticed that as the filter bandwidth is further increased, the quality of the distribution slowly degrades when compared to a Gaussian.

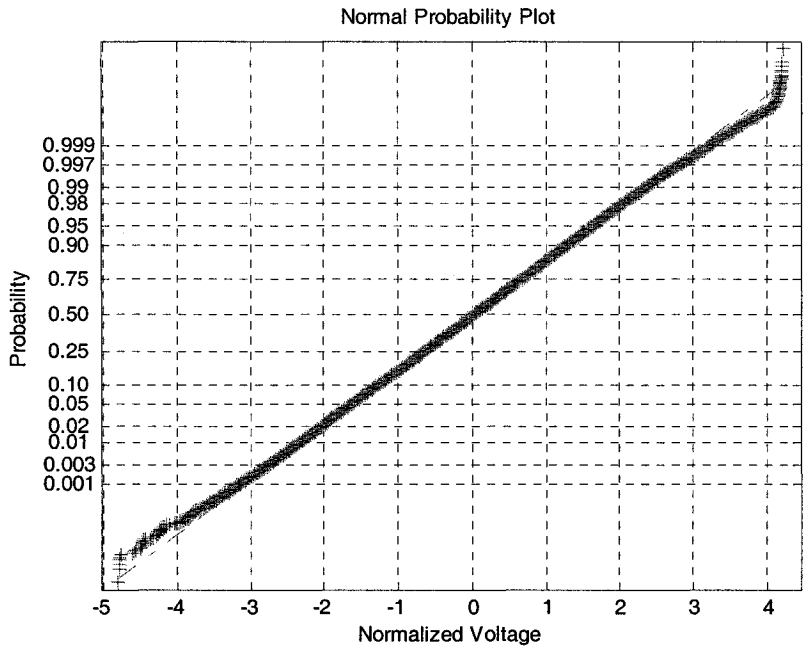

Figure 4.9: Experimental normalized normal probability plot of captured signal when filter has a bandwidth 10 times the nominal (19.5 kHz).

4.4 Summary

This chapter described the operation of the proposed Gaussian noise generator. Matlab simulations and a hardware implementation successfully proved its functioning. The method consists of encoding a specified Gaussian signal, using pulse-density modulation, into a RAM and then analog filtering the bit stream. It has been shown that the generated Gaussian signal can be very accurate (more than 5σ) when a large RAM is available. It was also demonstrated that the quality of the distribution has a weak dependence on the quality of the analog filter; hence, making the noise source extremely robust. Moreover, the possibility of only using 2.5 kilobits to encode a Gaussian signal having an accurate distribution up to 2σ suggests that the generator can be used in BIST applications.

CHAPTER 5

Gaussian Noise Source Applications

5.1 ADC Histogram Testing

Histogram testing is a technique where an ADC is excited using a signal having a known distribution and observing the resulting histogram at the ADC output [4]. The simplest way to perform a histogram test is using a linear ramp signal. This is due to the fact that a linear ramp has a uniform distribution; hence, all ADC output codes should ideally be "hit" an equal number of times. The number of occurrences of every code is directly mapped to the width of the code; thus, allowing differential nonlinearity (DNL) and integral nonlinearity (INL) calculations. Ramp tests are considered to be static tests, as the frequency of the ramp signal is usually quite low. To obtain dynamic differential linear error (DLE) and INL information, an input whose slope is on the order of the slew-rate of the device should be used instead. Also, generating a perfectly linear ramp is difficult and it is much easier to produce a pure sinusoidal waveform instead as spectral filtering is easily achievable with a passive filter. Referring to Figure 5.1, in sinusoidal histogram testing the distribution, or histogram, is pre-distorted to account for the non-uniform code density of a sinusoid. Consequently, any signal that has a known probability density function can be used for histogram testing as long as the test results are properly normalized.

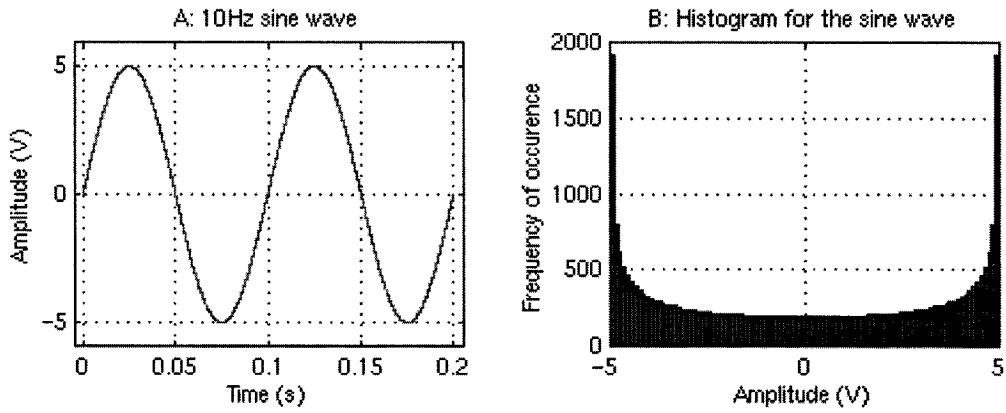

Figure 5.1: A sinusoid and its corresponding distribution.

Since a sinusoid is a deterministic signal, its pdf strongly depends on its magnitude and phase characteristics and any type of distortion or noise would affect its histogram. By being periodic, the sampling frequency must be carefully chosen to avoid redundancy in the sampled data. In addition, as depicted in Figure 5.1, a sine wave spends most of its time near the upper and lower peaks than the center. As a result, to achieve the desired test accuracy, many samples must be collected to ensure that there are enough code hits for the entire range of the ADC under test. On the other hand, a Gaussian noise signal is completely described by its first order statistics: its mean and variance. Also, any additional noise present in the test system will only add to the variance. Furthermore, an error in the variance of the noise test stimulus will only induce a gain error which can easily be accounted for if the gain of the converter is known beforehand [23]. Since the proposed noise source is programmable, the variance can be specifically chosen to have enough code hits in the mid-range of the ADC for the required accuracy.

In [6], histogram testing using a Gaussian signal generated by the amplification of the thermal noise of a resistor has been demonstrated. However, since the test signal used in this technique is purely random, this method is not amenable to a production testing environment. As a matter of fact, to obtain consistent reliable results within some confidence interval, many samples must be collected and averaged. In contrast, the Gaussian signal generated using the method proposed in this thesis is entirely predictable. In fact, the exact distribution of the test signal is exactly known and repeatable; consequently, the histogram test only needs to be executed once. An added benefit of using the test signal proposed is that it can be programmed for any frequency band within $F_S/2$. It could thus be used to investigate the behavior of the ADC for various frequency bands, something that cannot be achieved using traditional ramp or sinusoidal histogram testing.

A histogram test set-up using Matlab/Simulink has been realized. As depicted in Figure 5.2, the $\Sigma\Delta$ modulated bits encoding the Gaussian signal are stored in a circular memory and converted to analog form using a first order low-pass filter. Registers are used to capture the data at the output of the ADC. The number of samples in each output level is tabulated in order to determine its corresponding probability. The pulse-density encoded Gaussian stimulus is again generated by mapping the high bits to 1.65 V and the low bits to -1.65 V. The device under test is an 8-bit non-ideal ADC having a full-scale range of -0.6 V to 0.6 V. In order to make sure that all the ADC code levels are excited, the mean of the Gaussian test stimulus was set to 0 V and the standard deviation σ has been set to 0.3 V, which is 1/4th of the full scale range. More generally,

to ensure that the Gaussian signal covers the entire full-scale range of the ADC, the Gaussian signal should be programmed with parameters

$$\mu = \frac{V_{MAX} + V_{MIN}}{2}, \quad \sigma = \frac{V_{MAX} - V_{MIN}}{4}. \tag{5.1}$$

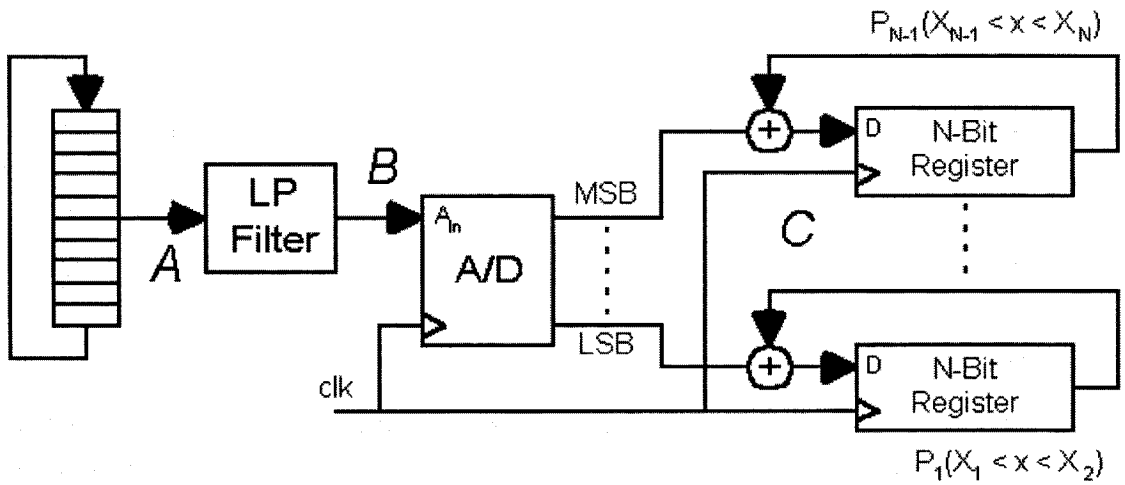

Figure 5.2: Histogram test set-up.

Figure 5.3 shows the obtained INL results for a Gaussian stimulus and the INL values obtained using an ideal ramp input (calculations were performed by acquiring 4 million points). Note that both INL plots are closely matched and the maximum difference is less than 0.04 LSB.

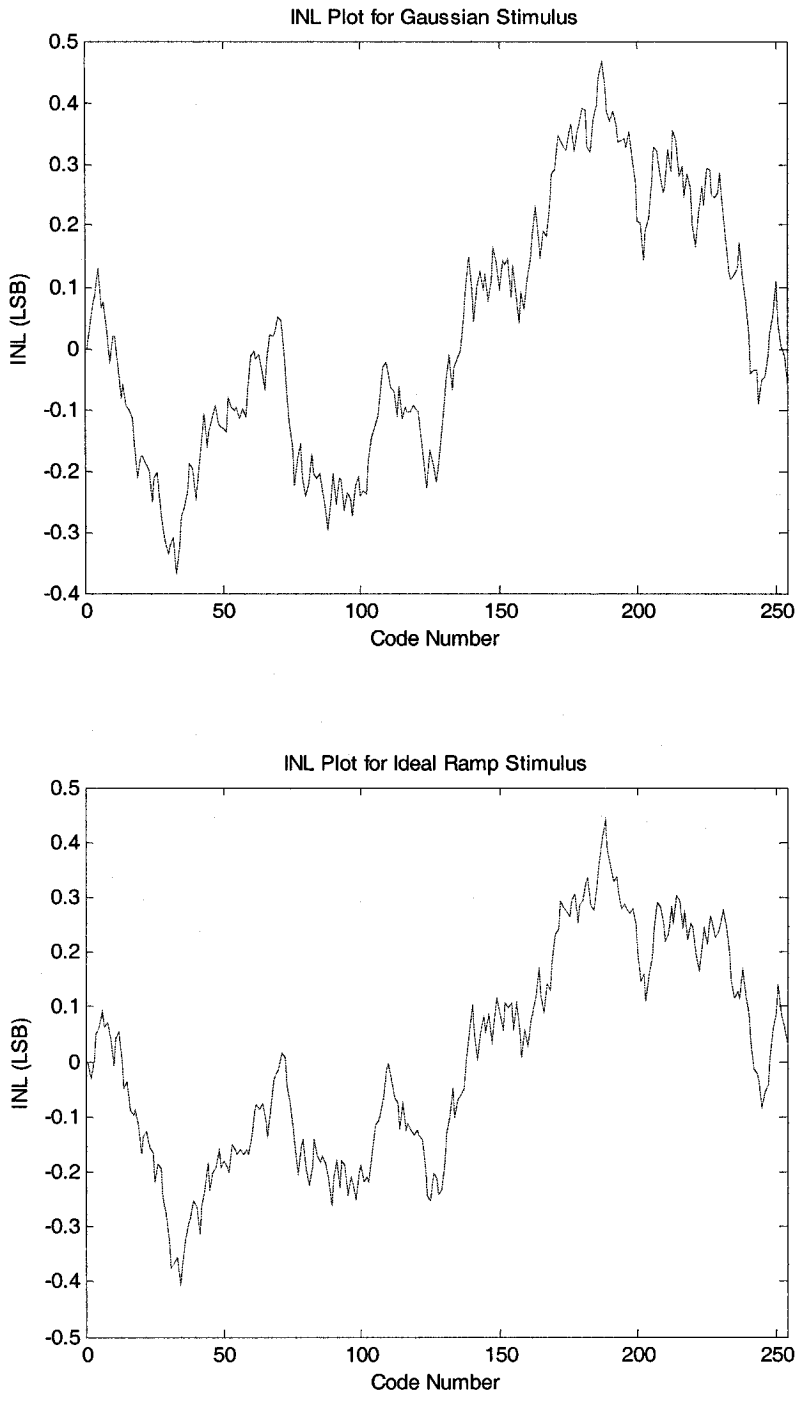

Figure 5.3: Top plot shows the INL results for a Gaussian input when 4M points are used. Bottom plot shows the real INL results for an ideal ramp.

5.2 High-Resolution Digitization Process

Another application of the Gaussian noise generator is as a high-quality predictable dithering signal for high-resolution digitization. The process consists of applying a Gaussian random signal with known mean and variance to one of the inputs of a comparator and connecting the other input to the unknown voltage to be digitized. After collecting enough comparator outputs to meet the required resolution, a probabilistic method is used to calculate the unknown voltage level. A Matlab/Simulink implementation of the proposed process showed that high accuracy can be obtained at the detriment of possibly longer test time when compared to conventional digitizers.

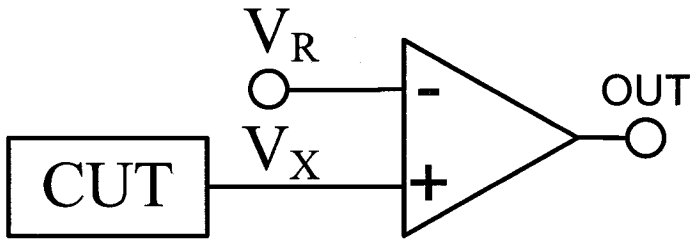

Figure 5.4: Comparator connections for probabilistic digitizer.

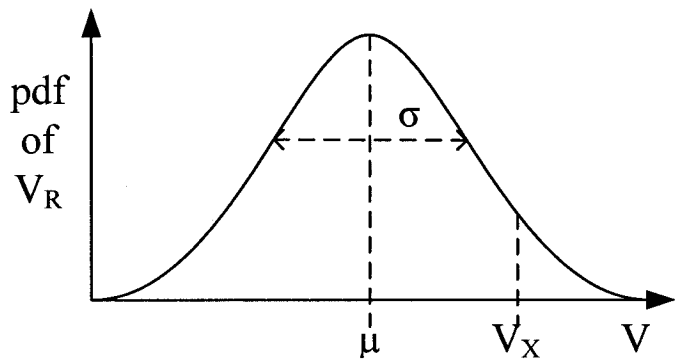

Figure 5.5: Gaussian reference signal.

Referring to Figures 5.4 and 5.5, the digitization process is outlined below. First a Gaussian reference noise signal with known mean μ and standard deviation σ is applied to V_R. Given an unknown voltage V_X, the number of times that $V_R < V_X$ is counted and divided by the total number of outputs to obtain the probability $P(V_R<V_X)$. Applying the inverse cumulative distribution function, Φ^{-1}, to the calculated probability provides an expression for the unknown voltage,

$$V_X = \sigma \times \Phi^{-1}(P) + \mu \,. \tag{5.2}$$

5.2.1 FPGA Implementation & DC Voltage Digitization Results

The overall implementation of the digitizer is depicted in Figure 5.6. As shown, the components to the left-hand side of the dashed line are used to digitally encode a Gaussian noise signal with a known probability density function. Thus, they can be replaced in hardware by a simple memory block. The proposed methodology has been successfully implemented on a FPGA and presented in [24]. The pulse-density encoded bit stream for the Gaussian signal was first generated using Matlab and then programmed as a RAM block on a FPGA. The first order analog reconstruction filter and comparator were built on a breadboard while the counting circuitry was also implemented on a FPGA.

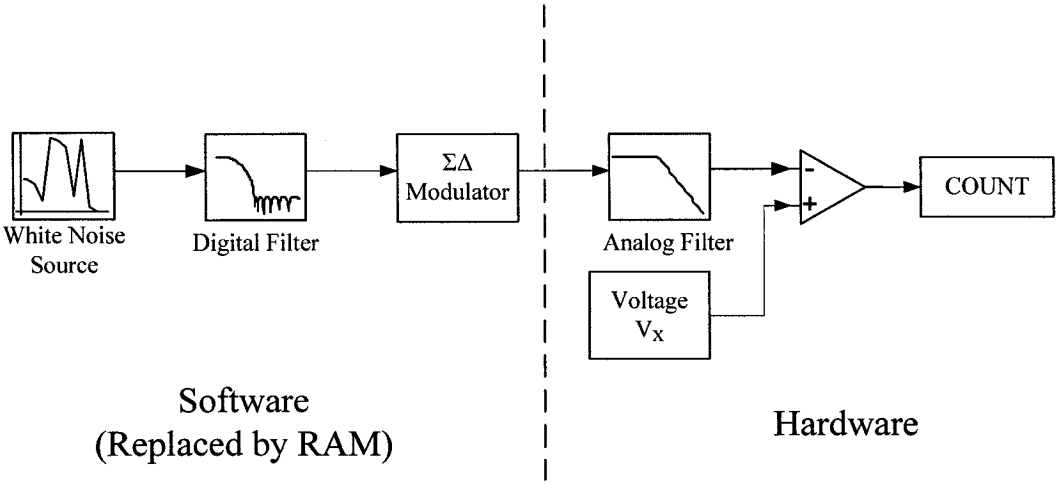

Figure 5.6: Digitizer architecture.

Under this experimental setup, the voltage range that has been digitized was limited to the common-mode range of the comparator used. Hence, as shown in Table 5.1, voltages between 0.35 V and 1.55 V have successfully been digitized with a resolution of a few millivolts (8.64 bits). The parameters of the Gaussian reference signal μ and σ have been set to 0.9 V and 0.3 V respectively. Note that 1 million comparisons were performed for every voltage level that was digitized. Consequently, a possibility to achieve greater resolutions is to increase the number of collected samples.

Table 5.1: DC digitization experimental results

Real [V]	Measured [V]
1.552	1.555
1.251	1.254
0.950	0.952
0.649	0.646
0.353	0.352

5.2.2 Matlab/Simulink Implementation for Time-Varying Inputs

The proposed methodology has been implemented in Matlab/Simulink for time-varying inputs. For this simulation, a sinusoid having a mean of 0 V and an amplitude of 1.35 V was digitized. In order to make sure that the entire sinusoid is covered within 3σ of its reference signal, the mean of the Gaussian source was set to 0 V and the standard deviation to 0.45 V. Coherent sampling was used where the total number of collected samples N is equal to 128 and the bin number M to 17. Note that 1 million comparisons were performed for every voltage level that was digitized. Consequently, the total test time is given by

$$Test\ Time = N_{Noise} \times T_{Comp} \times N_{Samples} \tag{5.3}$$

where N_{Noise} is the number of comparisons to the noise signal, T_{Comp} is the time necessary for every comparison, and $N_{Samples}$ is the number digitized samples. For example, if the comparator operates at 100 MHz, the total test time for this setup would

be 1.28 seconds. In addition, the digitized signal had a signal-to-noise-and-distortion ratio (SNDR) of 43.41 dB which gives about 7 bits of equivalent resolution. Figure 5.7 shows the power spectral density (PSD) plot of the digitized signal.

5.2.3 Voltage "Zooming" Technique to Increase Resolution

Since the characteristics of the dithering Gaussian signal are user-defined, the effective resolution can be further increased by repeating the same digitization process with a distribution that "zooms" more tightly around the voltage level being digitized. From above, a sinusoid ranging between [-1.35 V, 1.35 V] was digitized with a resolution of 7 bits. Subsequently, the Gaussian signal would be reprogrammed to have a mean μ equal to the previously digitized voltage and σ would be reset to about 5 LSBs (a σ of 0.1 V was used in this case). Therefore, the "zooming" procedure for every voltage level being digitized is as follows:

1. Reset the mean μ of the Gaussian noise signal to the current measured voltage value

2. Reset the standard deviation σ to focus around the current measured voltage (i.e. set it to 5 LSBs)

3. Repeat the aforementioned probabilistic digitization process.

As depicted in Figure 5.8, the noise floor of the PSD significantly decreases when the "zooming" technique is used. Indeed, the SNDR of the digitized signal increased to 84.17 dB which gives an equivalent resolution of nearly 14 bits. Note that

the "zooming" method can be applied iteratively to further increase the resolution. For the complete digitization process, the total test time found earlier needs to be multiplied by a "zooming" factor Z as follows:

$$Test\ Time = N_{Noise} \times T_{Comp} \times N_{Samples} \times Z\,. \tag{5.4}$$

In this case, where the "zooming" process is only applied once, the factor Z equals two and the total test time would simply double. To increase the frequency of the digitization process, methods to reduce the number of comparisons (noise points) required for every voltage sample digitized should be investigated to broaden the range of applications of this digitization process.

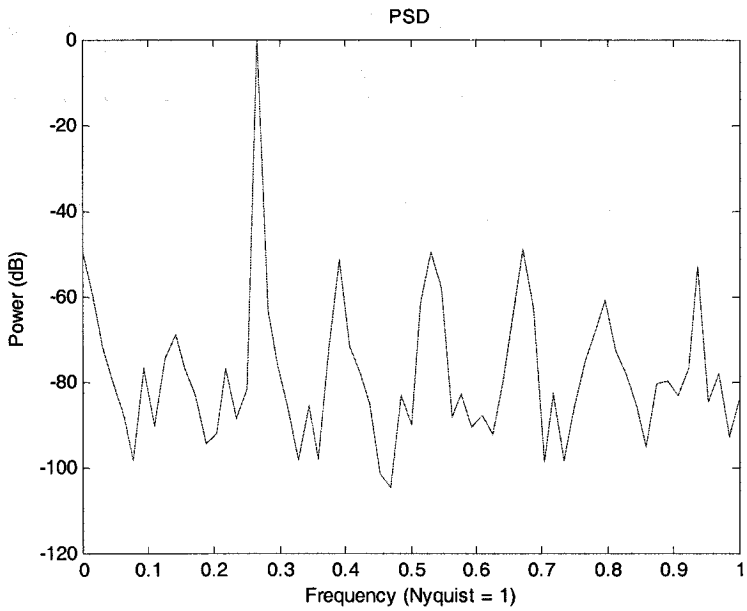

Figure 5.7: Power spectral density plot of the digitized signal using probabilistic digitization process without "zooming".

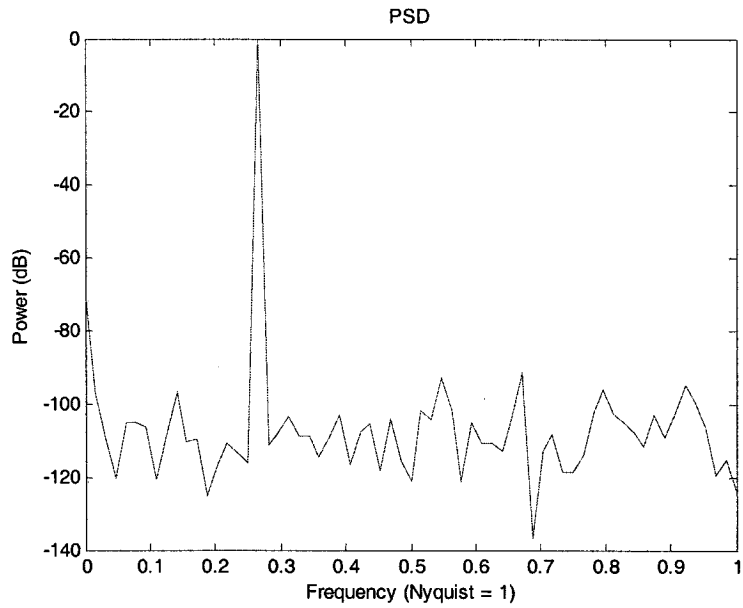

Figure 5.8: Power spectral density of the digitized signal when "zooming" technique is used to enhance the resolution.

5.3 Summary

This chapter has introduced two applications of the Gaussian noise generator. Firstly, it was demonstrated that ADC histogram testing can be accurately performed using the programmable Gaussian signal. In fact, simulation results showed that for an 8-bit ADC, INL results obtained using 4 million samples of a Gaussian signal closely match the results obtained using an ideal ramp (maximum difference being less than 0.04 LSB). Secondly, a high-resolution probabilistic digitization process (SNDR of nearly 14 bits was simulated) that also takes advantage of the programmability of the Gaussian noise signal was presented. In the following chapter, it is demonstrated that this probabilistic digitization process can be used in a high-voltage automotive test instrument.

CHAPTER 6

Automotive Test Instrument for 42 V Powernet

6.1 Introduction

One of the fields where the electronic revolution is having a great impact is the automotive industry. In fact, car manufacturers are currently rethinking the way the car is designed and the role of electronics in it. For example, modern vehicles are increasingly being equipped with advanced electronic systems to assist the driver in vehicle navigation (e.g. GPS systems) as well as to entertain the passengers (e.g. DVD players, internet access...). According to a recent statement from Daimler-Chrysler executives, more than 80% of innovation in the automotive industry will be in electronic components [25]. It is thus obvious that this is the new battlefield for electronic device manufacturers.

A major concern resulting from the increasing number of power hungry electronics in vehicles is the power delivery to these loads. The solution of choice to this problem is to use higher voltages since it permits the use of smaller connectors and hence reduces the wiring harness and the production costs. However, with this increase of power flowing in the vehicle, a more reliable and safer power distribution system is required. In fact, safety of the vehicle, its occupants, and service technicians is a

paramount priority with high power distribution systems. A power management and safety system employing "smart" connectors with embedded sensors and test instruments are currently being investigated.

In this chapter, a fully integrated mixed-signal high-voltage test instrument that can be implemented within these "smart" connectors is suggested. The test instrument incorporates the digitizer circuit described in Section 5.2. The following section describes a potential power management and safety system for the 42 V powernet. In Section 6.3, a test waveform generator suitable for the test instrument is suggested. Section 6.4 describes the digitizer proposed for the test instrument along with a Matlab implementation outlining its functioning. Finally, a brief summary is presented in Section 6.5.

6.2 42 V Power Management and Safety System

The transition to the 42 V power bus was first initiated by the MIT Consortium in 1994 after Mercedes-Benz realized that its new luxury model would be limited by insufficient power availability [26]. However, as pointed out earlier a major challenge in using a 42 V system is to ensure safe and reliable distribution to the various loads. For example, electrical arcing of connectors and relays when opened during current flow can cause non-reversible damage due to the large amount of heat generated by the electrical arc. A power management and safety system employing "smart" connectors that provides various functions to protect electrical loads as well as the vehicle's occupants and service technicians is currently being investigated by a group of

researchers from Auto21, a Canadian network of centres of excellence . As depicted in Figure 6.1, in order to monitor and safely manage the delivery of electrical power to the various components, smart connectors with on-board sensing and communication system are proposed.

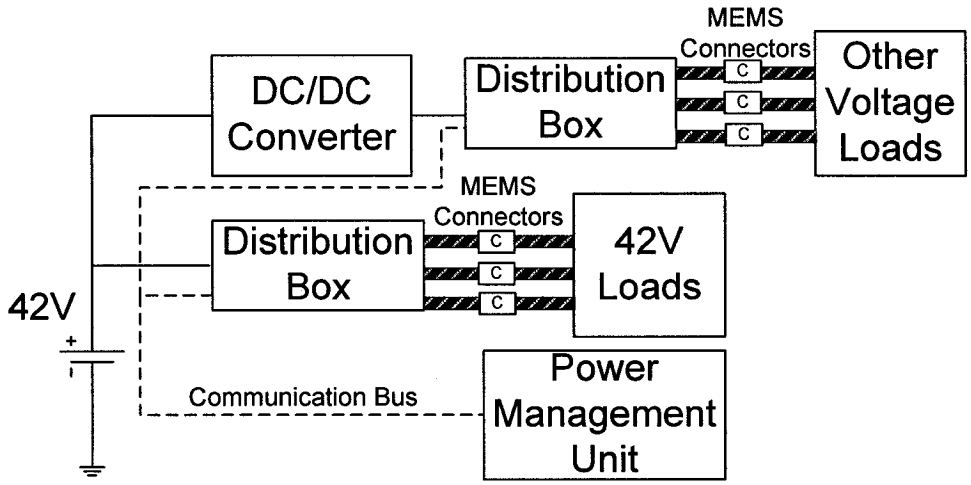

Figure 6.1: 42 V power distribution network

The test instrument suggested in this chapter would be incorporated right into the connector circuitry in order to test and detect any unusual loading conditions or device malfunctioning and to provide overload protection to the electrical loads. A power management unit (PMU) will monitor the power usage and automatically reduce or shut off power if any anomalous behavior is detected. Hence, the role of the proposed test instrument would be to provide diagnostic capability to the PMU.

6.3 Test Waveform Generator

In a vehicle, electronic components can suffer from many type of interferences. A critical aspect of line conducted interferences concerns the quality of voltage in the power distribution system. As specified in the ISO 7637 standard [27], "Road Vehicles - Electrical Disturbance by Conduction and Coupling", a very common type of test signal deals with voltage dips caused by the start of a big electrical drive (e.g. start-up of the engine). As depicted in Figure 6.2, this voltage dip should have no effect on the operation of electronic circuits in the vehicle. Hence, applying this type of signal to the various loads can allow easy and fast detection of malfunctioning devices.

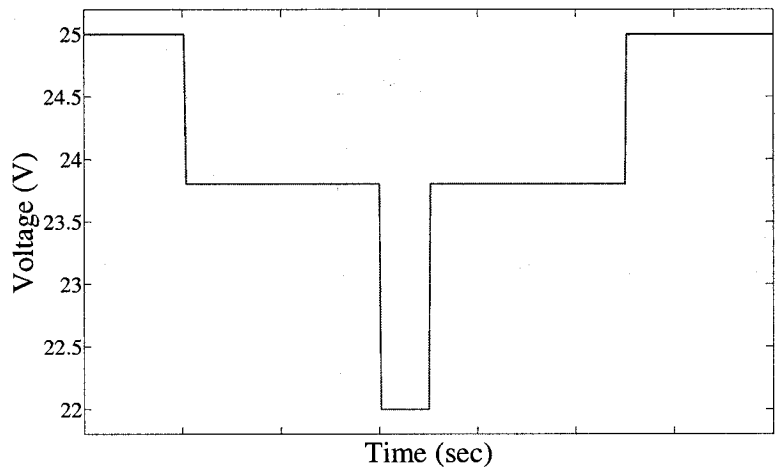

Figure 6.2: Voltage dip test signal for a 25 V load.

In Chapter 2, it has been shown that to synthesize a periodic analog test stimulus (e.g. a sinusoid), a short sequence of digital bits is repeated, as to approximate the output of a 1-bit ΣΔ modulator, and then filtered using an appropriate low-pass filter. Based on this approach, a method to generate a periodic test signal as the one above is

suggested. The test signal is generated by feeding the specified transient to a digital filter. Then, the output of the digital filter is applied to a 1-bit ΣΔ modulator and the output sequence is collected and stored in a RAM, as shown in Figure 6.3 . To recover the transient signal, the RAM's digital bit stream is applied to the input of a basic analog filter.

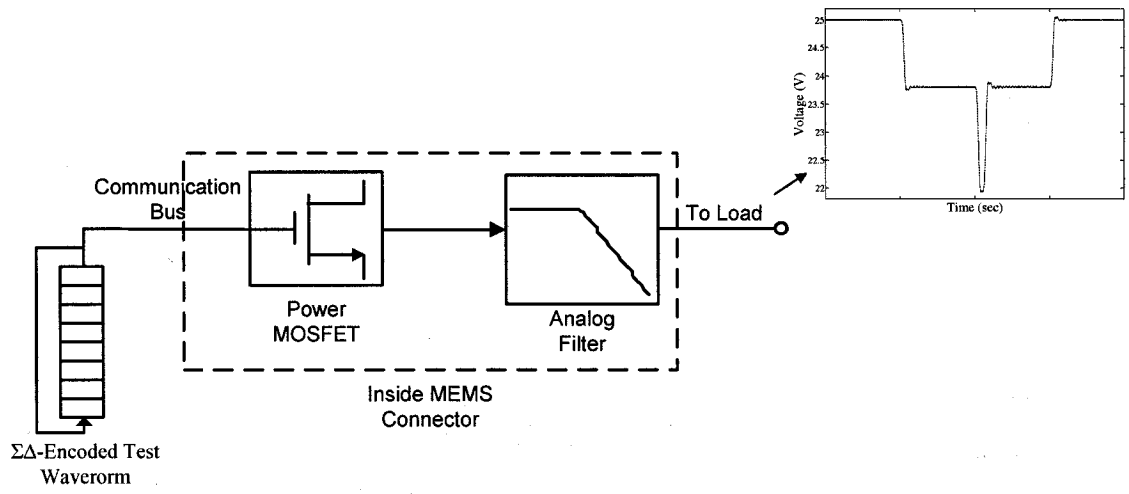

Figure 6.3: Proposed test waveform generator

6.4 Proposed Digitizer/Peak Detector Circuit

In this section, the architecture and operation of the proposed digitizer circuit for the test instrument is described and is supported with a Matlab implementation. One possibility would be to use a conventional Nyquist rate digitizer such as a flash-converter. However, since the objective is to consume as less space and power as possible, a traditional Nyquist rate converter cannot be used. Thus, an architecture supporting both the probabilistic digitization process discussed in Chapter 5 and the multi-pass algorithm described in [28] is presented.

6.4.1 Multi-Pass Digitization Algorithm

A single-comparator digitization process using a multi-pass algorithm was first presented in [28]. As depicted in Figure 6.4, the waveform digitizer consists of a comparator and a programmable reference voltage generator. Note that this architecture is constrained to digitize periodic signals. Indeed, multiple comparison passes over progressive periods must be performed. To generate the reference voltage levels, a repetitious sequence of ΣΔ modulated bits whose average equals the reference DC level are encoded and then filtered using a first-order low-pass filter.

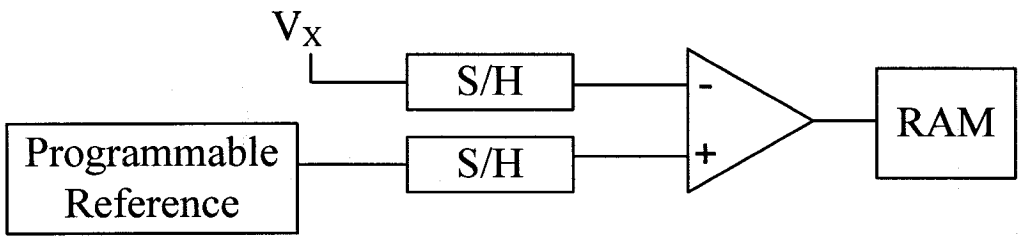

Figure 6.4: Multi-pass digitizer architecture.

Referring to Figure 6.5, the detailed digitization process occurs as follows. First, the programmable reference voltage generator is set to a voltage value to which all the samples, within a unit-test-period, of the unknown voltage signal V_X are compared and the results are stored in the output memory. Finally, the reference voltage level is set to the next value and the cycle repeats. Note that the maximum resolution achieved in [29] using this technique is 8 bits.

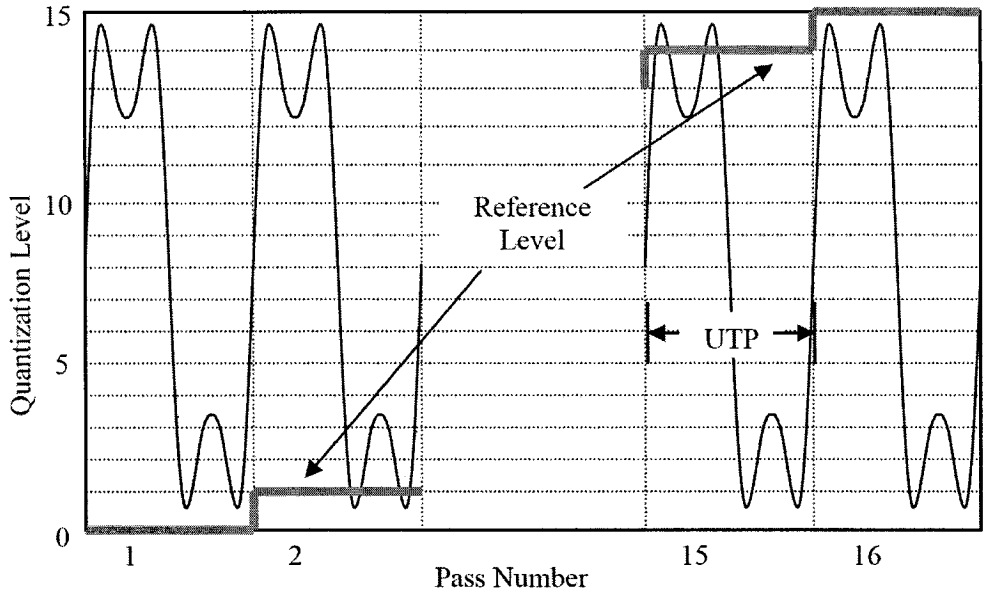

Figure 6.5: Digitization of periodic waveform [16].

6.4.2 Implementation of Proposed Digitizer/Peak Detector

The digitizer proposed for the test instrument supports both the probabilistic digitization process described in the previous chapter and the multi-pass process described above. As can be seen from Figure 6.6, a voltage divider is used to scale down the high voltage V_X ranging between [0, 42 V] to a value where low-voltage CMOS, 3.3 V or 5 V process, can be used. Scaling down the voltage V_X would result in a smaller capacitor in the sample/hold circuit of Figure 6.4. Another benefit is that the digitizer would consume considerably less power. In fact, not only would the comparator consume less power but the pulse-density reference voltages would be encoded using a smaller "V_{DD}" voltage. Scaling down the voltage V_X would also minimize crosstalk effects with other connectors during test mode.

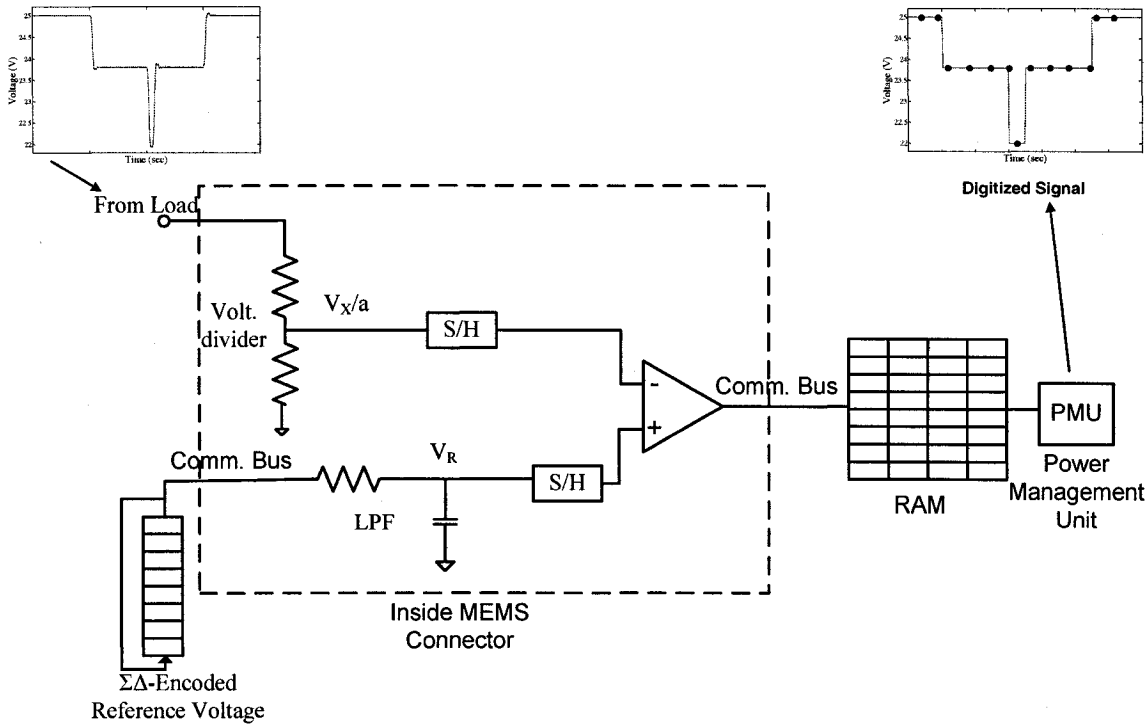

Figure 6.6: Digitizer/peak detector circuit

The main advantage of this architecture is its versatility. Indeed, the programmed reference voltage V_R can be programmed to support the following three test functions:

- Measure DC & AC signals with 8-bits resolution using the multi-pass algorithm.
- Enhance the resolution by using the probabilistic method.
- Peak detection by setting V_R to a max/min "tolerable" level.

The overall implementation of the test instrument within the MEMS connectors is shown below in Figure 6.7.

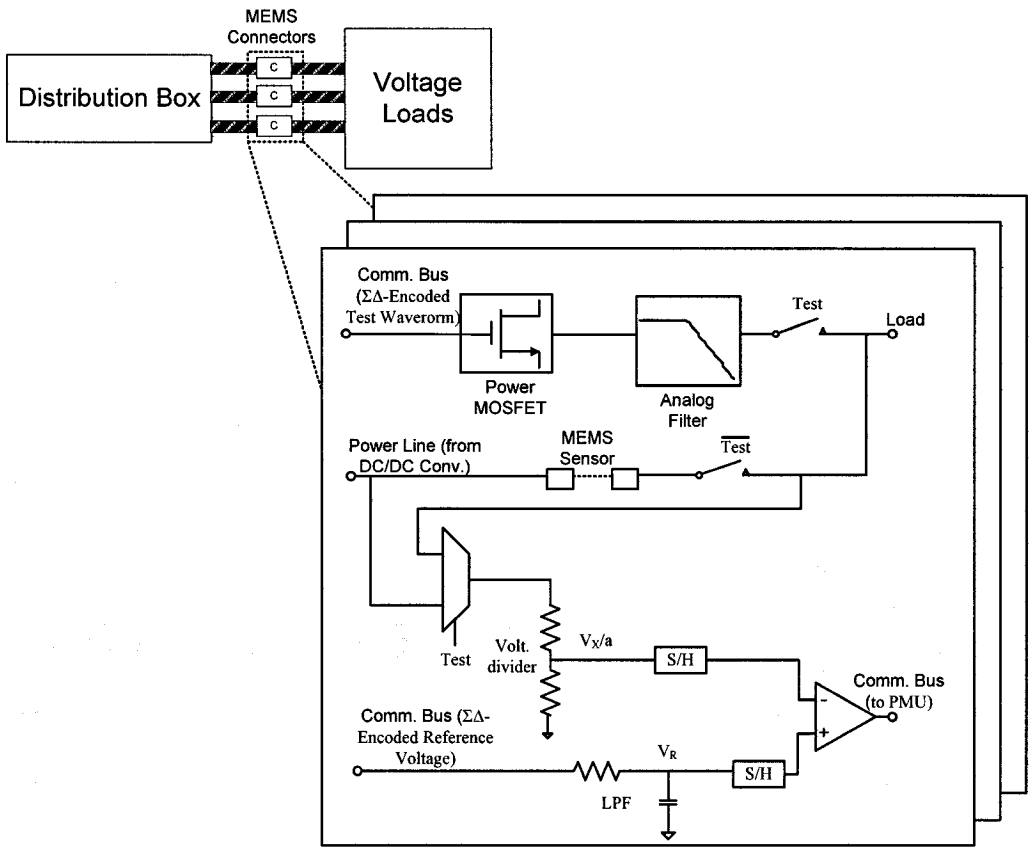

Figure 6.7: Test instrument inside MEMS connectors

6.4.3 Matlab/Simulink Simulations

In this section, the feasibility of the proposed digitization instrument is investigated and supported with Matlab simulations. The risks associated with the implementation of the proposed signal capture circuit are minimal since two of its test functions have already been successfully implemented for low voltage applications and the third one is just a simple peak detector circuit. Indeed, the multi-pass digitizer, first

suggested in [28], is a mature circuit and has been reused in the mixed-signal test-cores developed in [3] and [29]. On the other hand, the probabilistic digitization process is relatively novel but a board level implementation consisting of an FPGA and discrete components proved the correct functioning of the algorithm (Section 5.2). In order to further investigate the implementation of the proposed digitizer, a Matlab example showing how the probabilistic method can be used as a complement to the multi-pass algorithm to increase the effective quantization resolution is described below.

For the multi-pass digitizer to function correctly, it is imperative that the DC reference voltages be encoded and generated accurately. In the case where voltages between [0, 42 V] can be digitized with a resolution of 8 bits, maximum resolution achieved in [29], and that a voltage divider circuit that scales down the [0, 42 V] input to [0, 3.3 V] is used; then, reference voltages that cover the [0, 3.3 V] range must be generated with at least 8 bits of resolution. For example, if a voltage of 25 V is being digitized (corresponds to 1.964 V at the voltage divider output) and the reference voltage that caused the comparator output to switch from low to high is 1.977 V then this would give an equivalent resolution of 8 bits. However, if a higher effective digitization resolution is required then the probabilistic method can be used to "zoom" around the voltage being digitized. Referring to Figure 6.6, for this example, the encoded reference Gaussian signal mean μ is set to the 8-bit digitized voltage, 1.977 V in this case, and the standard deviation σ is set to 0.1 V. Using this technique, to ensure that the reference signal does not get clipped within 3σ of its distribution, voltages ranging between 0.3 V and 3.0 V have been digitized. Figure 6.8 shows the absolute

error of the digitized voltage versus the input voltage. As depicted, the maximum error is less than 0.3 mV which gives an equivalent effective resolution of more than 13 bits. Note that here again to achieve this resolution 1 million comparisons were performed for every voltage level digitized.

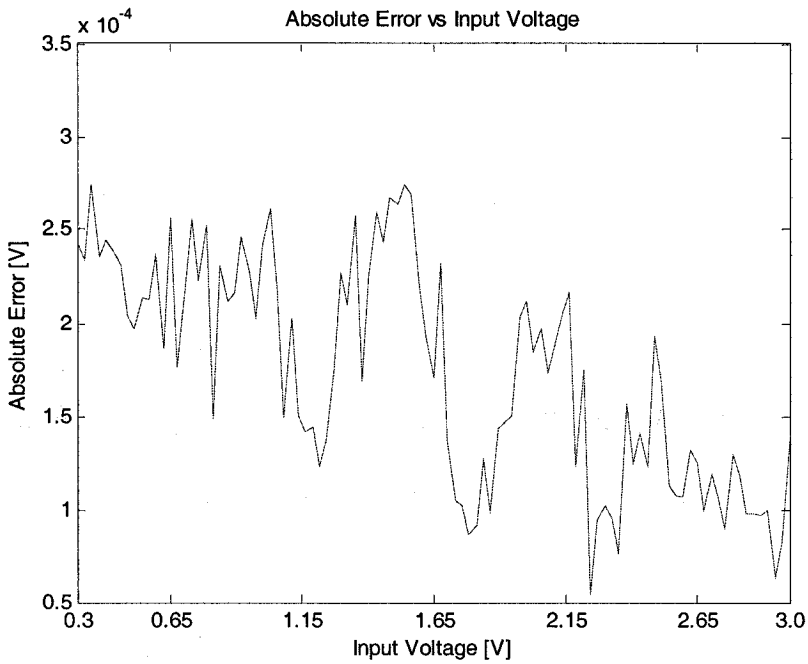

Figure 6.8: Absolute error vs input voltage level when "zooming" technique is used.

6.5 Summary

The simplicity, compactness, and digital interface of the instrument presented make it an attractive option for the target application. In fact, the test instrument could easily be implemented within the "smart" connectors that transmit electrical power to the various loads. In order to further reinforce and prove the operation of the design, an implementation of the test instrument on silicon can be realized in DALSA's high voltage CMOSP8G process. This technology combines both high voltage and low voltage operation on the same chip; hence, both the test waveform generator and digitization circuit can be incorporated on the same chip.

CHAPTER 7

Conclusion & Future Research

7.1 Conclusion

In conclusion, a robust programmable Gaussian noise generator has been presented. In contrast to traditional methods, the user has the freedom to set the distribution characteristics (i.e. frequency band, μ, and σ) as long as the signal is within the supply rails. The simplicity of the generation process as well as the high quality of the resulting distribution makes it a very effective and repeatable dithering solution applicable to mixed-signal/digital ATEs. The low sensitivity of the generator to the analog filtering process and the possibility of using only 2.5 kilobits to achieve 2σ quality, also makes it an attractive BIST solution. Two applications of the proposed Gaussian noise source were demonstrated: ADC histogram testing and high-resolution digitization. Subsequently, a high-voltage automotive test instrument that supports the proposed probabilistic digitization process was outlined for the next generation automobile.

7.2 Future Research

In this section, another envisioned possible application for the programmable Gaussian noise source is outlined. The main idea behind the proposed future application is to map the Gaussian noise source to the time domain. Indeed a jitter source that could possibly operate at high-frequency bands is proposed.

7.2.1 Programmable Jitter Source

In today's digital systems, phased-locked-loops (PLLs) are omnipresent building blocks. They realize essential functions such as clock distribution and clock recovery. They are thus present in large digital circuits such as microprocessors or mixed-signal circuits used in digital communication systems. When embedded in high-speed digital communication systems, PLLs have very stringent specifications. The challenge is thus to integrate an on-chip characterization scheme that involves two blocks: a stimulus source and a response capture circuit [30]. An important parameter of a PLL is its jitter transfer function which is defined as the ratio of output jitter to the applied input jitter as a function of frequency. Referring to Figure 7.1, the jitter transfer function is determined by applying a jittery clock to the input of the PLL and observing the output of the voltage-controlled oscillator (VCO) for different frequencies.

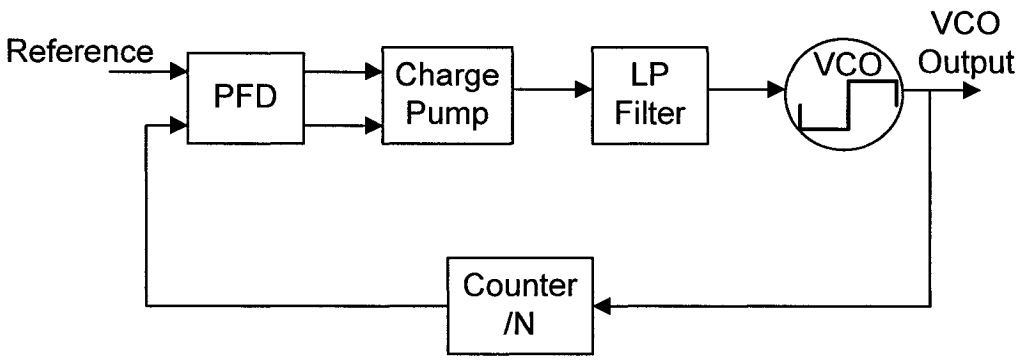

Figure 7.1: Digital phase locked loop functional block diagram.

A method to inject controlled temporal noise in a clock could be to pass a clean clock signal through a buffer which produces a delay that can be modulated by a controlling voltage. For example, the programmable Gaussian noise source described in this thesis can be used in conjunction with a voltage-controlled delay buffer to make a jittery clock source as shown in Figure 7.2. A circuit that could possibly achieve this function is depicted in Figure 7.3 [31]. Note that this circuit must be calibrated to determine the mapping between the applied control voltage and produced delay. As can be seen from Figure 7.4, for a 0.18-μm CMOS process the delay varies nonlinearly as the control voltage is swept from 0 V to 1.8 V. However, for inputs ranging between approximately 0.50 V and 0.65 V nearly linear delays varying from about 320 ps to 200 ps can be achieved [32]. Consequently, applying a Gaussian noise signal to the control voltage within the linear region will produce a delay also having a Gaussian distribution. In addition, since the Gaussian bias signal is programmable and generated in software, the delay buffer can even be used in the non-linear region if the transfer function between the delay and bias voltage is known beforehand. In fact, the Gaussian signal can be pre-distorted to account for any non-linearity.

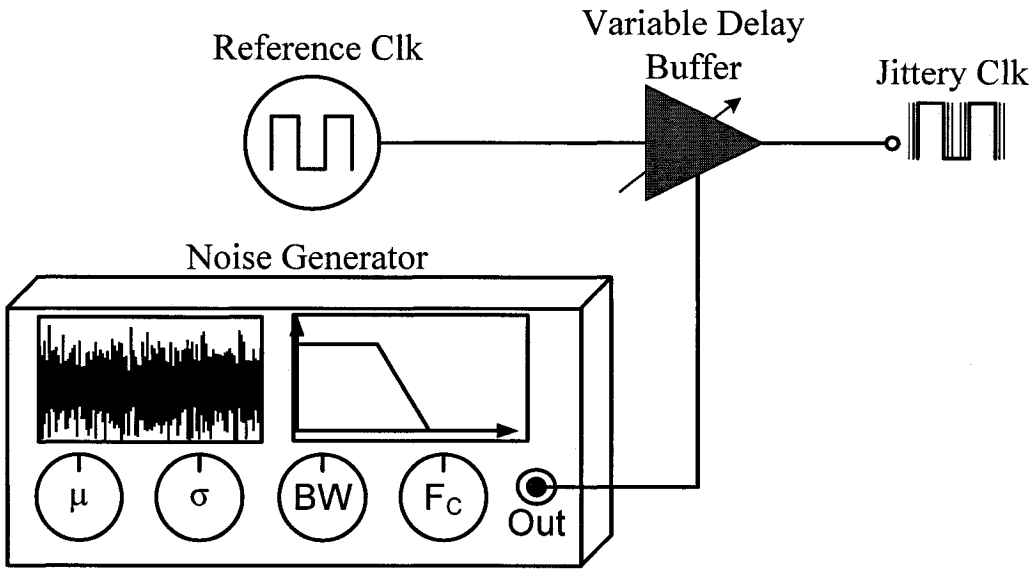

Figure 7.2: Proposed jittery clock source implementation.

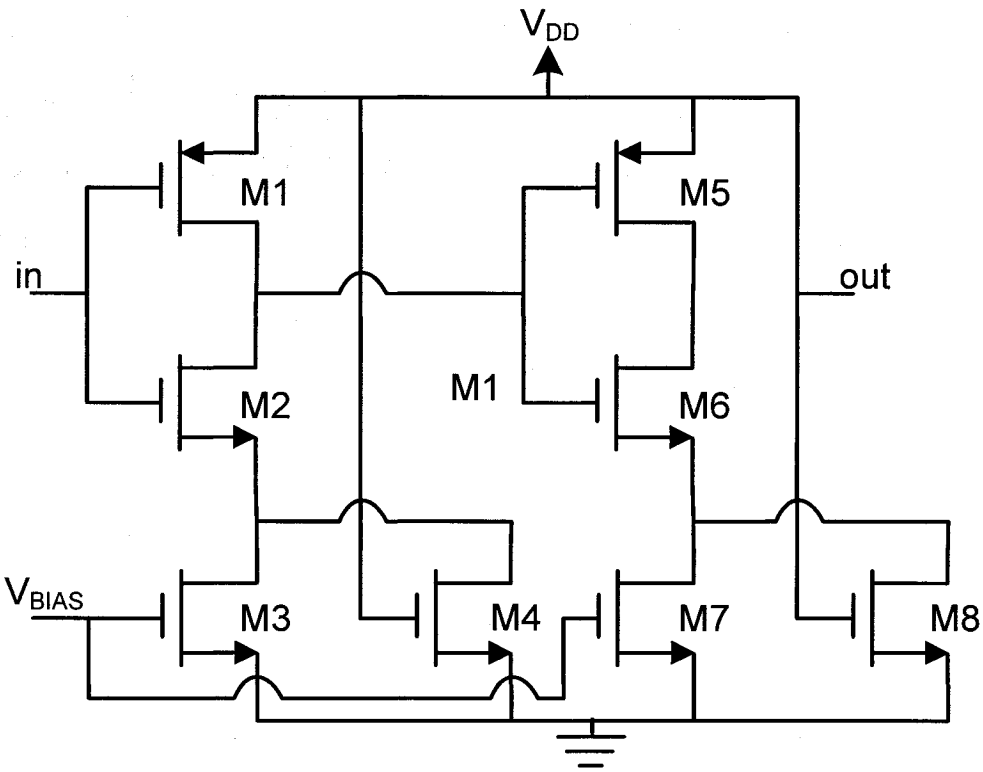

Figure 7.3: Circuit schematic for voltage-controlled delay buffer.

Table 7.1 Transistor sizes used for simulation of the voltage-controlled delay buffer as reported in [32].

Transistor	Width (μm)	Length (μm)
M_1/M_5	40	0.40
M_2/M_6	15	0.40
M_3/M_7	80	0.40
M_4/M_8	5	0.90

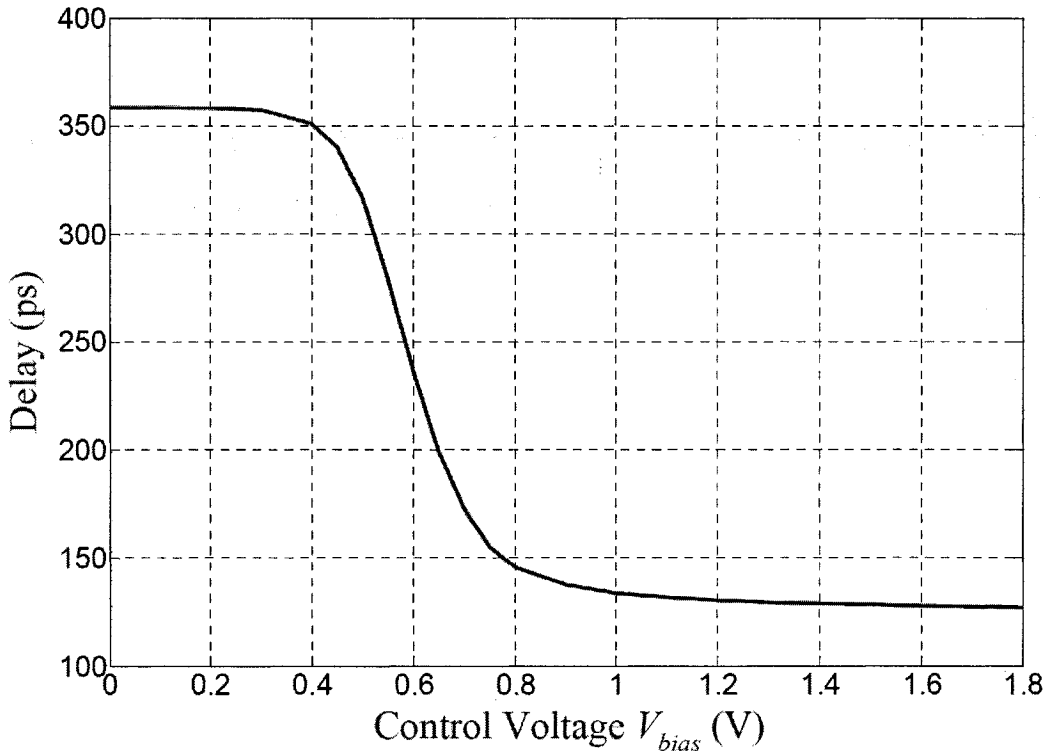

Figure 7.4: Simulated delay versus control voltage of voltage-controlled delay buffer [32].

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