Thin Film Transistors from II-IV Semiconductors on Polymer Substrates

By
Finlay MacNab.

Department Chemistry

McGill University
Montreal, Quebec

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Abstract

A chemical bath deposition technique has been used in the fabrication of thin film transistors (TFT), which have been deposited on a 200μm polymer substrate. This thesis documents the chemistry and microfabrication techniques used to create the TFTs. Because TFTs have not been fabricated on plastics in this manner before, insights gained from understanding the mechanical properties of the polymer, and how these interact with those of the inorganic components of the TFTs, were used to guide development of processes specifically suited to adapt the polymer to TFT fabrication.

Résumé

Un dépot par bain chimique a été employé pour la fabrication de transistors à couches minces (TFT). Ces derniers ont été déposés sur un substrat de polymère d'une épaisseur de 200 µm. Les techniques chimiques et de microfabrication utilisées pour créer des transistors à couches minces sont décrites dans cette thèse. Ces TFTs n'ont jamais été fabriqués sur des plastiques selon cette procédure. Le développement de procédés spécifiques à la fabrication de TFTs sur des polymères a été basé sur une meilleure compréhension de leurs propriétés mécaniques ainsi que de leurs intéractions avec les composants inorganiques.

Acknowledgements

I would like to acknowledge my supervisor Prof. Mark Andrews, my labmates at McGill, my co-workers at Silk Displays, and at Technologies Novimage. I would also like to express thanks to Prof. Ishiang Shih, J.P. Higgins, and Bell Fong for their help with this research.

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Chapter 1. Introduction

This thesis is concerned with the materials chemistry and fabrication of large area arrays of thin film transistors (TFT) on polymer substrates suitable for controlling pixel function in an active matrix liquid crystal display (LCD).

As anyone with a laptop computer can attest, LCDs are a ubiquitous technology viewed everyday by practically everyone in the developed world. Annually, billions of dollars are spent on LCD research and development and tens of billions of dollars are spent on the construction of high volume fabrication plants that produce millions of displays.

Currently, the TFT manufacturing industry has adopted well developed processes that use rigid glass, as opposed to polymer, substrates and physically deposited, lithographically patterned conducting and semiconducting film layers. As the demand grows for larger and larger TFT panels for use in LCD displays, the scale up of traditional fabrication techniques is becoming increasingly expensive and technically challenging.

A materials chemistry approach to the design and fabrication of TFT arrays promises to broaden the collection of processes and materials that can be utilized. Furthermore, a focused chemical approach may lead to advances that allow researchers to tailor the properties of materials that are currently used in the fabrication of semiconductor devices in ways that are impossible using more limited physical deposition techniques.

In this thesis, a combination of traditional TFT fabrication techniques and non-traditional chemical approaches are combined to build a quarter video graphics array (QVGA) TFT array on a polymer substrate. The creation of a II-VI

semiconductor thin film field effect transistor array on a polymer substrate presented here is a novel achievement.

The remainder of this chapter is devoted to the discussion of the materials and processes that were used in this research.

1.1 What is a TFT?

The components and mode of action of a thin film transistor are well known to electrical and semiconductor engineers[1]. A short description of the layer components and an active matrix TFT and an explanation of the mechanism of TFT function are therefore of interest.

Typical TFT arrays are composed of laminate layers of inorganic materials deposited on a rigid substrate (see figure 1.1). TFTs for use in displays are usually fabricated on specialty glass (e.g. Corning 1737 aluminosilicate subtrates). The transistor unit design utilized in this research project was adapted from the previous work of Ghan and Shih[1]. This TFT consists of an aluminum gate, an aluminum oxide dielectric layer, an SiO_2 passivation layer, a cadmium sulphide (CdS) semiconducting layer, and aluminum source and drain electrodes (figure 1.1).

The TFT array fabricated in this thesis is created by repeating transistors arranged in rows and columns. The gate electrode connects all the transistors in a given column, whereas the data lines connect the transistors in a given row

through the drain electrodes. The source electrodes of the transistors in the array are connected to the pixel electrodes (figure 1.2).

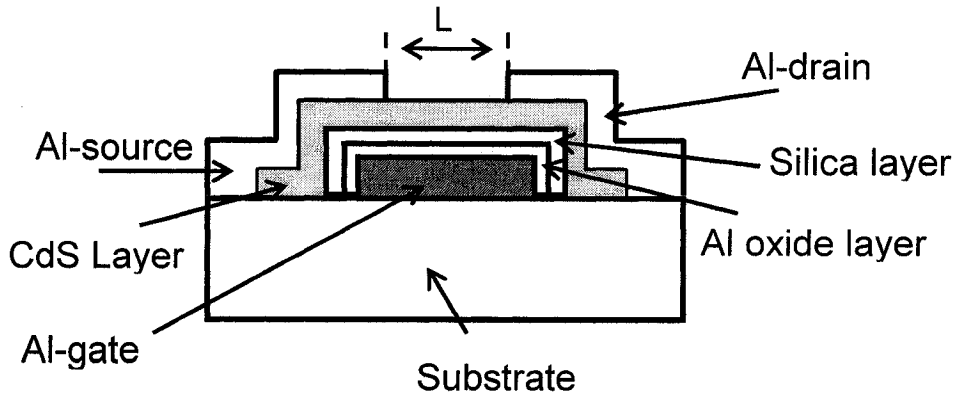


Figure 1.1 The component layers of a thin film transistor.

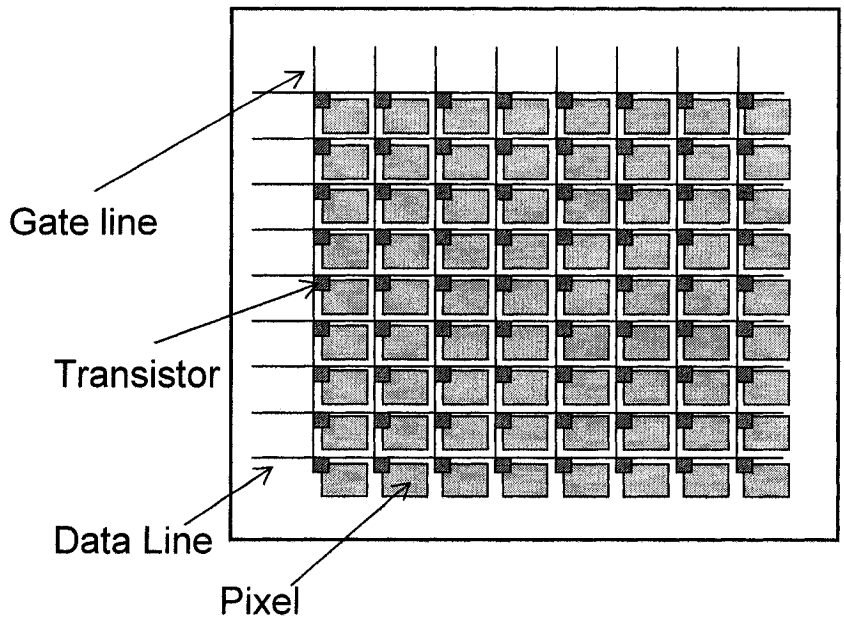


Figure 1.2 The TFT array structure.

An individual transistor in the array is addressed by applying a voltage to the gate and data lines that correspond to a given transistor position in the TFT matrix. Energizing the gate line of a transistor modulates the conductivity of the

semiconductor layer. Voltage applied to the data line then allows current to flow between the drain and source charging the pixel. Since the gate lines of all the other TFT units on the data are not under positive voltage bias their pixels electrodes remain isolated.

The mechanism of field effect transistor function: The mechanism of transistor current modulation is well studied[2,3,4]. Enhancement mode field effect transistors (FET) of the type presented here exploit the properties of semiconductors to modulate the current that flows between the source and drain electrodes under an applied gate voltage. For enhancement mode transistors, source-drain current will flow when the gate voltage is positive and above the threshold voltage.

The heart of a thin film FET is the semiconductor layer. Semiconductors are materials that have band gap energies between their filled valence bands and empty conduction bands that are intermediate between conductors and resistors. The band gap, E_g, of CdS deposited by chemical bath deposition (CBD) is approximately 2.4eV[5]. Most semiconducting devices utilize dopants that act as either electron acceptors with energies close to the valence band (p-type) or electron donors with energies near the conduction band (n-type). A feature of CdS films deposited by CBD under conditions that lead to non-stoichiometric inclusions of excess Cd^{2+} ions is that the sulphide lattice voids that result act as electron donors with a first ionization energy of ~0.6eV. CBD deposited CdS is an n-type semiconductor with low lying electron donor states.

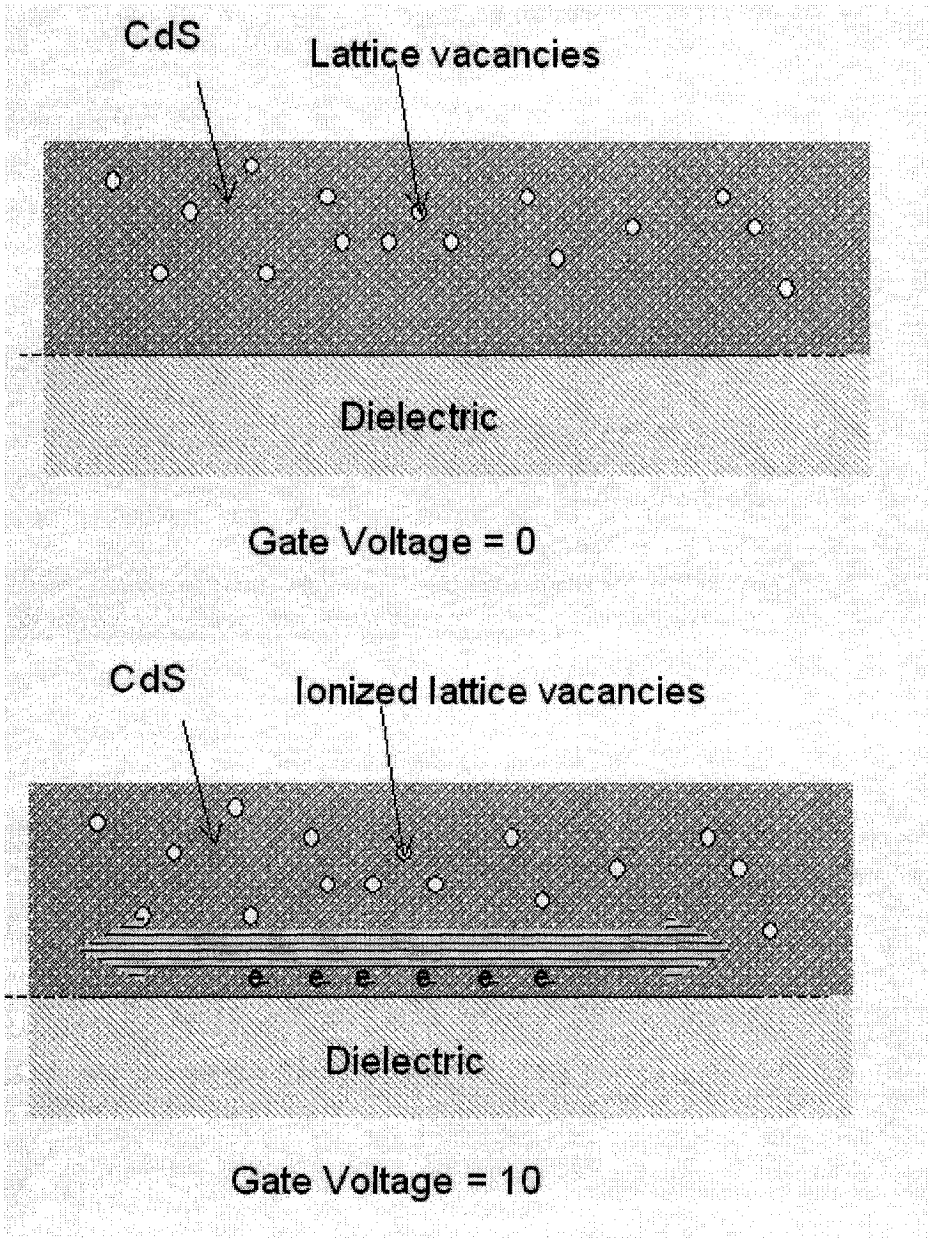


Figure 1.3 The semiconductor-dielectric interface with (bottom) and without (top) potential applied to the gate.

When a positive voltage is applied to the gate of FET, the electric field that results causes electrons to be promoted from the low lying donors in the CdS semiconductor to the conduction band. These electrons migrate to the semiconductor-dielectric interface and act as induced charge carriers allowing

current to flow between the drain and source under applied drain voltage (figure 1.3).

The current which flows along the interface depends upon the drift velocity of the induced electrons or mobility, μ, which is measured in cm^2/ Vs. The mobility of a semiconductor is dependent not only on the intrinsic properties of the material but on the morphology of the film. Lattice imperfections near the semiconductor-dielectric interface and the grain structure of the film greatly reduce the observed mobility of CdS. Pure, single crystal CdS exhibits a mobility of 250 cm^2/ Vs, the mobility of CBD deposited CdS is orders of magnitude lower at 0.2 ~ 2 cm^2/ Vs.

1.2 Materials and Processes Used in TFT Fabrication

In order to advance the science of microelectronics, a multidisciplinary approach may inject new ideas and expertise into already well developed fabrication processes and device designs. Though not traditionally the realm of chemists, TFT manufacture can benefit from advances in chemistry and chemical understanding.

The following subsections introduce the techniques and materials utilized in the conduct of this research. Section 1.2.1 introduces the technique of plasma surface roughening, which is used to improve the adhesion of film layers deposited on substrates. Section 1.2.2 describes DC magnetron sputtering of aluminium, the technique by which the TFT gate lines and data lines are

deposited. Section 1.2.3 is a short introduction to the science of SiO_2 deposition by plasma enhanced chemical vapour deposition (PECVD). PECVD was used to deposit the gate dielectric passivation layer, in order to protect the underlying aluminum oxide from dissolution in the high pH chemical bath solution. Section 1.2.3 deals with the electrochemical growth of the gate line dielectric by anodization of aluminum. This non-traditional technique benefits from not requiring a preceding lithographic pattering step. Finally section 1.2.4 presents a basic overview of photolithographic processes. Photolithography was used extensively in the micro-patterning of the deposited film layers.

1.2.1 Plasma Surface Roughening

Before discussing the process of plasma surface roughening, a short explanation of the science of plasmas is required to inform the discussion in this section and in section 1.2.2 and 1.2.3. Plasmas were first identified through the study of ionized gasses in high-current vacuum tubes[6]. Gradually, investigators realized that plasmas could not be described in the same way as regular gasses and today they have come to be regarded as a quasi-fourth state of matter.

Plasmas exhibit a collective behaviour under the influence of electromagnetic fields because they are composed of charged particles: electrons, and ions, as well as neutral particles. The vast majority of atoms in plasma are neutral; in glow discharge and arc plasmas (the type most useful for

thin film deposition and surface roughening) ionic densities range from 10^7 cm^{-3} to 10^{14} cm^{-3}.

Typically, plasmas of the Townsend discharge or glow discharge type, the kind of plasma produced in the instruments discussed in this thesis, are generated by charging two electrodes separated by a space containing a low-pressure gas. In the case of DC current, the mechanism of plasma generation is more easily understood with the aid of figure 1.4.

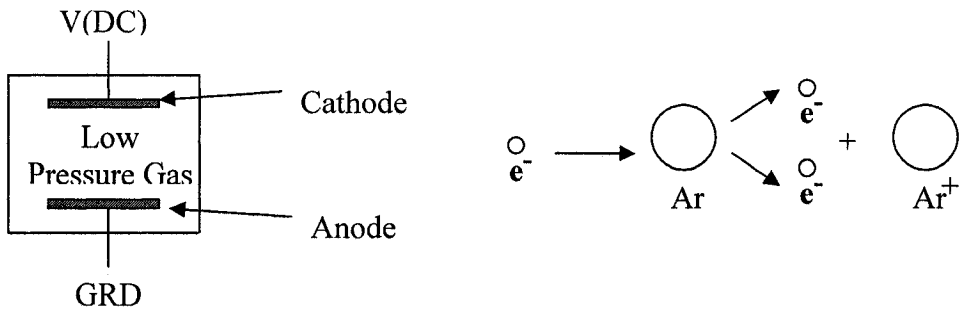


Figure 1.4 A schematic representation of an electrode pair and the ionization cascade for argon gas.

When DC voltage is applied to the cathode in a system like the one in the above figure, stray electrons are accelerated towards the anode by the resulting electric field. If the voltage and pressure are of an appropriate value the electron gains enough kinetic energy to ionize a neutral gas atom generating a second electron and a cation. The two electrons are both accelerated towards the cathode and in turn generate more electrons and cations. This process causes a cascade of ionization that generates the plasma. At the same time the generated

cations (argon ions in the above figure) are accelerated towards the cathode. The impact of the massive positive ions on the anode liberates more electrons, which then join in the cascade of ion generation. When the number of electons generated by collisions within the gas and by impact of cations on the cathode equals the number of electrons neutralized by de-excitation and by impact on the anode the plasma is in equilibrium and becomes self sustaining at a given applied voltage.

If the applied voltage is large the probability of secondary electron emission from collisions within the gas can become large enough that the current rises to infinity between the electrodes. This condition is known as breakdown. The breakdown voltage for various gasses is given by equation 1-1, known as Paschen's law,

$$V_B = \frac{APd}{\ln(Pd) + B} \qquad (1\text{-}1)$$

Here V_B is the breakdown voltage, A and B are constants specific to the low pressure gas used, P is the pressure of the system, and d is the distance between the electrodes. Figure 1.5 gives the Paschen curves for several different gasses. In practice, most plasmas used in microfabrication processes operate below the breakdown threshold.

The gas column of a glow discharge plasma along the axis between the electrodes is characterized by regions of glowing gas separated by regions without emission. Figure 1.6 depicts a simplified schematic of the inter-electrode

space. The region proximal to the cathode is called the Ashton dark space. In this region electrons are moving in the direction of the anode and cations are moving towards the cathode with high energy. The region is dark because none of the accelerating electrons is energetic enough to generate excitation collisions. Immediately above the Ashton dark space is the cathode glow. This luminous region is characterized by the neutralization of positive ions by de-excitation. The next region, the Cathode dark space, or Crooks dark space, contains

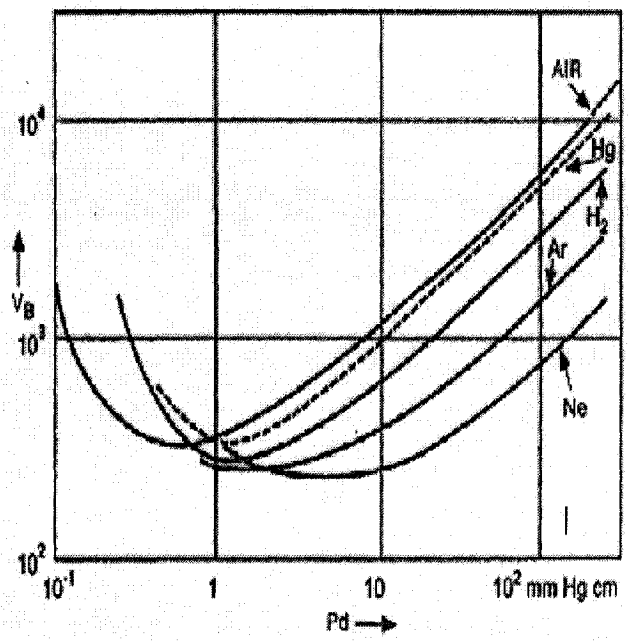


Figure 1.5 Paschen curves for various gasses (adapted from ref 7).

relatively few electrons with energies sufficient to generate ions and secondary electrons. This region is dark because of the low number of ionizing collisions. Closer to the anode is the negative glow region. Here the density of electrons with high energies increases to the point where the generation of secondary electrons and ions results in enough excitation and de-excitation interactions to

generate the characteristic violet glow. In sputtering instruments the substrates are generally placed within the negative glow region, and the Faraday darkspace and positive glow regions are obscured.

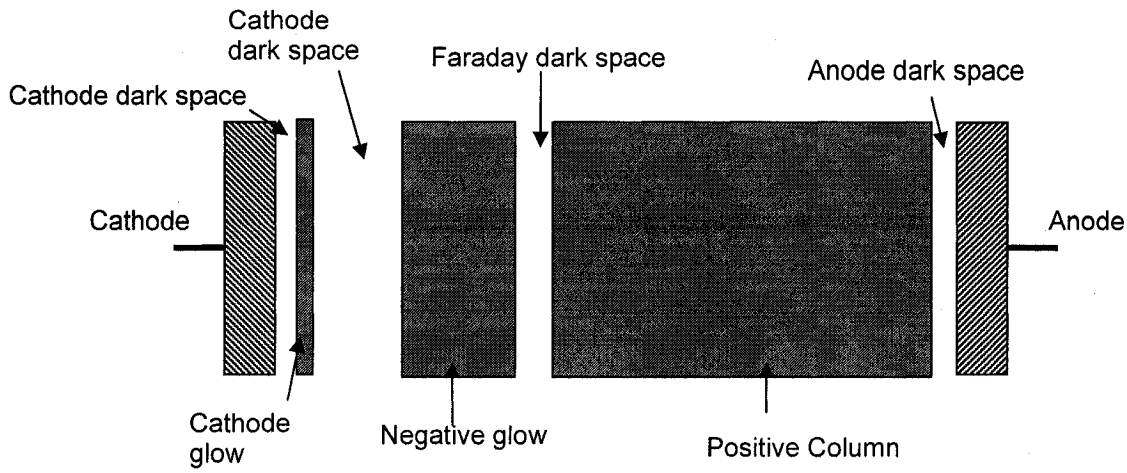


Figure 1.6 The structure of a DC glow discharge plasma (adapted from reference 9)

There are many other complex phenomena that occur inside glow discharge plasma of the type described above that are beyond the scope of this discussion but many fascinating and comprehensive books and reviews exist to broaden the interested reader's understanding[7,8,9,10,11]. Armed with a basic understanding of what characterizes glow discharge plasma, an examination of instrumental techniques of interest can be undertaken.

When a substrate is placed near the cathode in a glow discharge plasma system, the surface of the substrate is exposed to the high energy impact of accelerated ions. Surface treatments such as plasma cleaning, plasma etching,

and plasma roughening exploit the high energy ion flux at the cathode to modify the surfaces properties of substrates.

Plasma roughening of is a standard technique used to increase the adhesion of films deposited on the surface of polymer substrates. Ionic bombardment of polymer substrates can increase the adhesion of subsequent depositions by three mechanisms: organic removal[11], crosslinking via activated species of inert gasses[12] (CASING), and surface chemical restructuring[13].

Organic removal increases the adhesion of films to polymers by cleaning the substrate surface. Small organic molecules, such as monomers, mold release agents, and inhibitors left over from the polymerization process, and grease contamination from handling degrade the adhesion of films to the substrate surface. When exposed to oxygen plasma, which contains monatomic oxygen species (O^+ and O^-), surface hydrocarbons are readily oxidized forming CO_2 and H_2O. This process leaves a clean residue free substrate surface. Noble gas plasmas from argon and helium have also been shown to remove small organic molecules from the surface of substrates[14].

CASING is a widely used plasma treatment for polymer substrates. The impact of ions and vacuum ultraviolet radiation (VUV) on the surface of polymers can break C-H and C-C bonds generating radicals at the surface and near surface regions of the substrate. Reactive radical species can form crosslinks that densify the surface. Because of diffusion limitations within polymers, radical species can be long lived, enabling post plasma reactions.

Surface chemical restructuring is similar to CASING except that instead of intra-substrate crosslinking reactions the reactive groups generated within the substrate react with atmospheric gasses such as water or ammonia to functionalize the surface and greatly increase its surface energy. Experiments with PTFE reveal that a pre-treatment in helium plasma followed by ammonia exposure generates a barrier layer on the surface of the polymer with much improved surface functionalization and adhesion characteristics. Contact angle measurements on plasma treated PTFE films reveal the surface to be hydrophilic (20°) compared to untreated samples (107°)[15].

1.2.2 DC Magnetron Sputtering of Aluminum

A basic explanation of how glow discharge plasmas interact with cathode targets to produce the sputtering effect is presented below and is necessary to an understanding of the morphology of sputtered Al films and their interaction with polymer substrates.

Sputtering is a widely used thin film deposition technique. Popularized in the 1970's, today sputtering processes are ubiquitous in commercial microfabrication. There are many variants of sputtering instruments, such as DC, AC, and reactive, which are used to deposit metals, dielectric insulators and semiconductors. DC magnetron sputtering from planar targets is a variant of the DC family of sputtering instruments that has gained wide acceptance in industry because of its high metal deposition rates compared to traditional DC techniques.

DC magnetron sputtering instruments take advantage of the properties of glow discharge plasmas to deposit metal films by utilizing specially designed cathode targets. Aluminum targets like the one used in the fabrication of the TFT devices described in this thesis are of extremely high purity (99.99+%).

The basic design of a sputtering system can be understood as two electrodes separated by a space filled with low pressure gas (fig. 1.7). The cathode is replaced by a target composed of the material to be deposited in a film on the substrate, which is placed near the anode. Positively charged ions impacting the cathode eject target atoms which travel through the inter-electrode space and deposit on the target.

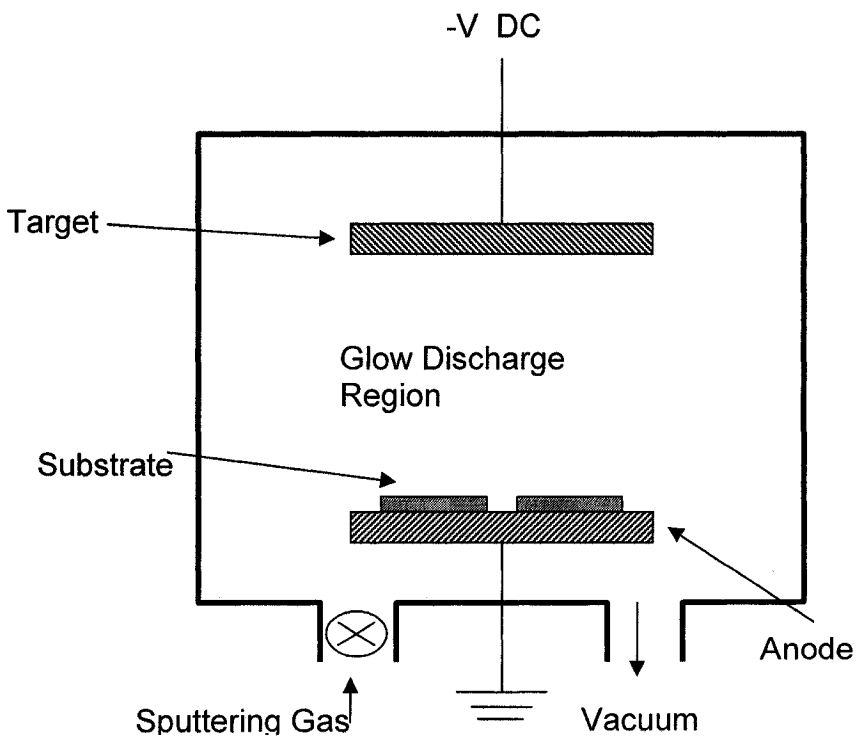


Figure 1.7 Schematic of a simplified DC sputtering system (adapted from reference 8).

The interaction of the incident ions with a cathode target in plasma instrumentation is complex. Figure 1.8 is a schematic representation of the some of those interactions. The type of collision which results between the ions accelerated by the electromagnetic field and the cathode depends strongly on the energy of the incident particle. The types of collisions most important to the understanding of sputtering are those that result in the ejection of an atom from the target into the inter-electrode space. Three types of collisions that result in sputtering in order of increasing incident ion energy have been identified: single knock-on, linear cascade, and spike type (figure 1.9).

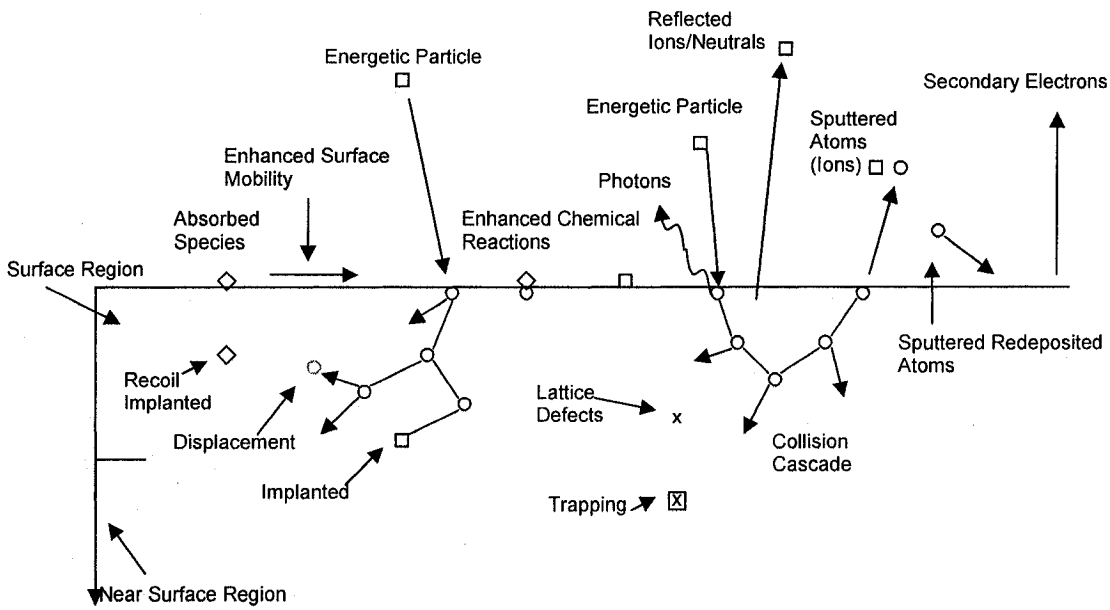


Figure 1.8 Depiction of energetic-particle bombardment effects on surfaces (adapted from ref 7)

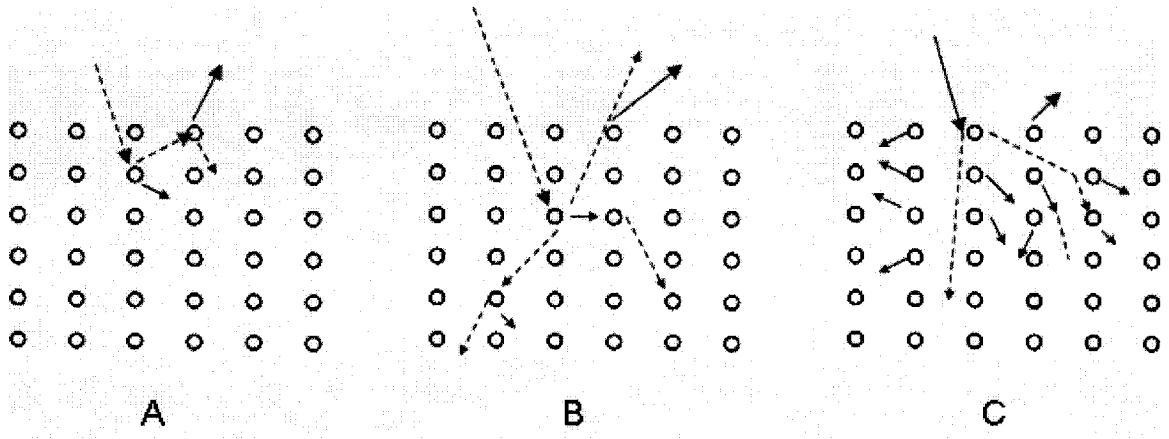


Figure 1.9 Ion impact in the the three sputtering energy ranges. A) Single knock –on, B) Linear Cascade, C) Spike Type (adapted from reference 7).

A description of linear cascade and spike type sputtering events will not be presented here, but many comprehensive discussions of these phenomena have been published[16,17]. Knock-on collisions are relatively low energy collisions that set the target atoms in motion. If enough energy is transferred to an atom in the target matrix to overcome the threshold energy, $E_{th,}$, it can be ejected from the target. The threshold energy is proportional to the binding energy, U_S, of atoms to the target surface which is typically assumed to be equal to the heat of vaporization of the target materal. Equations 1-2 and 1-3 give the relation between the threshold energy and the binding energy:

$$E_{th} = 4U_S \qquad 1\text{-}2$$

for $0.08 < M_1/M_2 > 1$, where M_1 is the mass of the incident ion and M_2 is the mass of the stationary target atom. If the mass of the incident ion is greater than the

mass of the target atom then the elastic collision results in less energy transfer and the threshold energy is given by:

$$E_{th} = \frac{U_S}{\gamma} \qquad 1\text{-}3$$

where $\gamma = \frac{4M_1M_2}{(M_1 + M_2)^2}\cos\theta$ the energy transfer function for collisions between particles of different masses. In the above relation θ is the angle of incidence of the two particles. Threshold energy values range from 5 to 40 eV depending on the nature of the target material and incident ion.

The sputter yield S is another important variable in sputtering. It is the ratio of the number of atoms ejected from the substrate per incident energetic particle. Table 1.1 gives a range of threshold values and sputtering yields for different sputtering materials and gasses.

Sputtering gas energy (KeV) ⟶	**He** (0.5)	**Ne** (0.5)	**Ar** (0.5)	**Ar** (1.0)	**Ar threshold voltage** (eV)
Ag	0.20	1.77	3.12	3.27	15
Al	0.16	0.73	1.05	1.0	13
Au	0.07	1.08	2.40	3.6	20
Cu	0.24	1.80	2.35	2.85	17
Ti	0.07	0.43	0.51	N/A	20

Table 1.1 Threshold sputtering energies and sputtering yields for different materials

DC magnetron sputtering instruments employ a modified cathode in order to increase the sputtering deposition rates relative to those for simple DC instruments. Currents in magnetron sputtering instruments are one or two orders

of magnitude higher and plasma gas pressures are much lower than for their non-magnetron counterparts. This effect is achieved through the placement of small permanent magnets behind the target in a "racetrack" type configuration (figure 1.10). The intense magnetic field generated above the target surface is parallel to the field at the edges and perpendicular to the electric field above the centre of the track. Electrons are confined inside the magnetic field because electrons emanating from the target are directed towards the centre of the track by the magnetic field normal the target surface and the perpendicular magnetic and electric fields in the centre region of the track confine the electrons and cause them cause them to be directed in a "hopping", cycloidal fashion along the axis of the field lines.

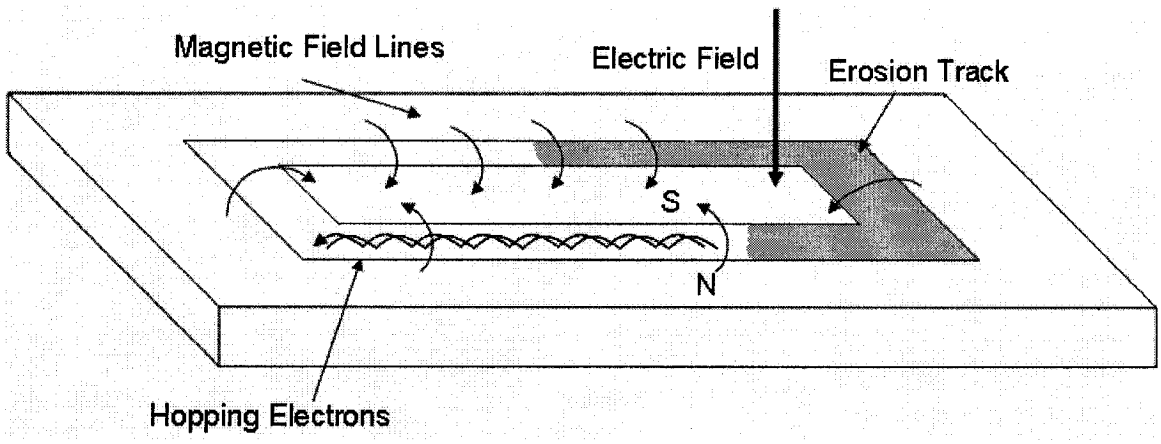


Figure 1.10 The cycloidal hopping of electrons at the surface of the cathode target (adapted from reference 9).

The high concentration of electrons in the region above the magnetic track cause the plasma generated there to be intensified allowing sputtering to be conducted at pressures and currents not possible for traditional DC sputtering.

The Deposition of Aluminum Films by Sputtering: The gate lines of TFT devices should be as flat as possible. Surface roughness at the gate dielectric-semiconductor interface results in transistor properties that vary across the surface of the array. Unfortunately, the deposition of low surface roughness aluminum films by sputtering is difficult for two reasons: the tendency of aluminum to form highly grainy films and the formation of hillocks and wiskers during subsequent annealing of the film.

The strong tendency of aluminum to form thin native oxide layers upon exposure to oxygen and water complicates the deposition of aluminum by sputtering. Oxidation of aluminum during the deposition can lead to the formation of large numbers of microscopic aluminum grains in the resulting film. At large film thickness (~1μm), the grainy structure result is an aluminum layer with a milky appearance and high surface roughness.

The grainy structure of sputtered aluminum films is a consequence of the high energy of the impacting aluminum atoms and the heat generated within the sputtering instrument by the glow discharge plasma. The energy of impacting aluminum atoms generated at the cathode that bombard the substrate during deposition is typically greater than 20eV. In contrast the energy of aluminum atoms deposited by thermal evaporation is only ~0.2eV. The impact aluminum atoms on the substrate is sufficiently energetic to break chemical bonds. This can result in the formation of small volatile fragments that can combine with the growing film and generate grain boundaries. Furthermore, the heating of

surfaces inside the vacuum chamber by exposure to plasma and radiation can liberate adsorbed water and oxygen which also reacts with the growing film. Water and oxygen in the vacuum chamber even at pressures as low as 10^{-7} torr also generate oxides and grain boundaries in deposited films[18].

Grainy aluminum films undergo structural changes during post deposition heat treatments that result in the formation of surface protrusions called hillocks and whiskers. Hillock and whisker formation further degrades the smoothness of the film surface and will consequently increase transistor variability. Hillocks and whiskers can also generate flaws such as deformations and cracks in overlying films that result in leakage currents, and open circuits. These undesirable surface features result when small aluminum grains with high surface energies re-order themselves during heating. Because the native oxide layer encapsulates the film surface it restricts the movement of the underlying metal during annealing. Flaws in the oxide coating at grain boundaries allow the metal underneath to extrude out in the case of a whisker or to deform thin regions of the native oxide layer into lumps in the case of hillocks[19].

1.2.3 Plasma Enhanced Chemical Vapour Deposition

Plasma enhanced chemical vapour deposition is a technique for depositing thin films. Commonly, materials such as oxides, nitrides, borides, or carbides are deposited, though aluminum, silicon and carbon films have also been demonstrated[20,21]. PECVD instruments enable the deposition of insulating

dielectrics and passivation layers at low temperatures and are therefore well suited to the task of depositing inorganic films on polymer substrates. PECVD was used in this project to deposit a passivating layer of SiO_2 on the surface of the gate line dielectric.

In the PECVD process glow-discharge plasmas initiate vapour phase chemical reactions and substrate surface reactions that enable film formation at low temperatures. Typically, PECVD instruments operate by RF plasma excitation of a carrier gas (e.g. Ar) and vapour phase reactants (e.g. SiH_4 and O_2) with frequencies in the MHz range. The generated glow discharge plasma is generally sustained under reduced pressures of between 50 mtorr and 5 torr, with positive ion and free electron densities of between 10^9 and 10^{11} /cm^2. Average electron densities range from 1 to 10 eV, a discharge energetic enough to excite gas molecules from the electronic ground state and decompose molecules into ions, atoms, molecular fragments, and free radicals.

The mechanism of film formation is complicated and not well understood. A description of the electron kinetics, plasma chemistry and surface reactions will not be presented here but several comprehensive reviews[20,21,22] have been published on the subject, including the work of Meeks et al. Meeks modeled the deposition of SiO_2 from silane and oxygen in an argon carrier gas, identifying 167 gas phase reactions and 96 surface reactions that affect film growth.

A schematic of a conventional PECVD reactor is presented in figure 1.11. Gasses are injected into the chamber and flow over the substrates before being evacuated by a mechanical pump. The substrates are placed on a rotating,

heated, aluminum plate that forms half of the RF coupled capacitor. The rate of film formation for common materials such as silicon nitride and silicon dioxide is on the order of 10^2Å/min.

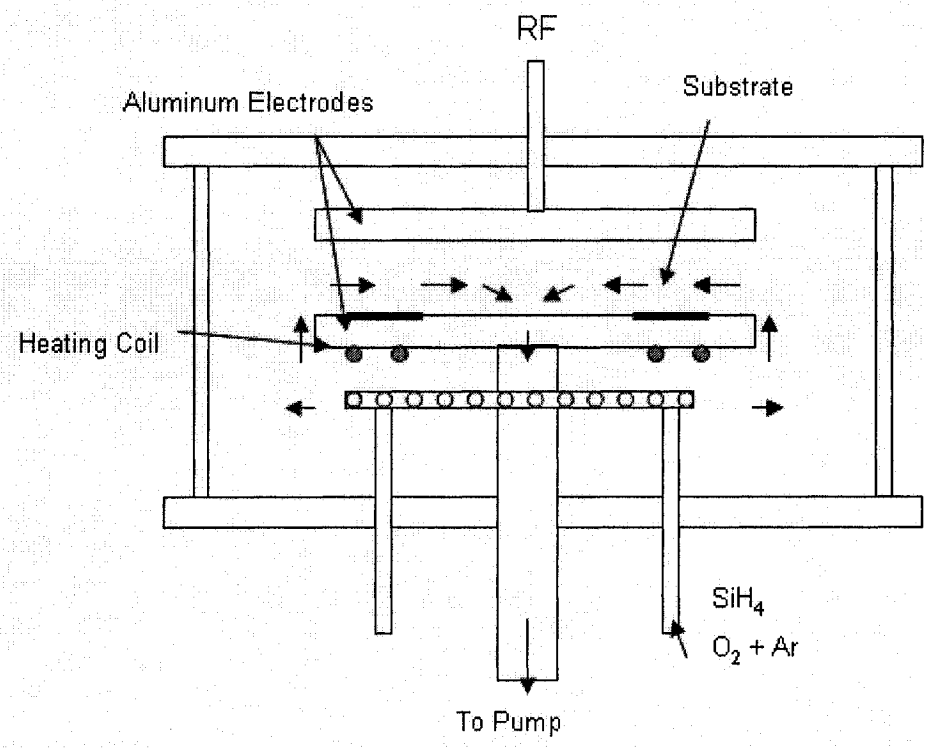


Figure 1.11 A schematic of a conventional PECVD instrument (adapted from reference 7).

1.2.3 Anodization

Anodization of aluminum is an electrochemical technique widely used in industry as a method of passivating the surface of aluminum parts against abrasion and to improve their appearance. Recently, it has been studied as a technique for generating dielectric layers for TFTs and as a method for

suppressing hillocks and wisker formation on micropatterned aluminum films

The technique employs an electrochemical bath in which the aluminum annode is paired with a platinum counter electrode in an electrolyte solution, often ethylene glycol based. (figure 1.12)

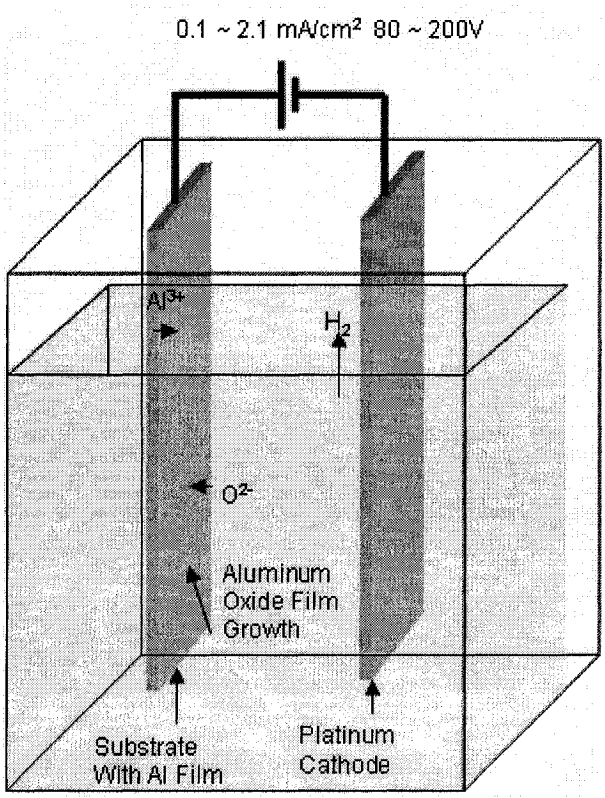


Figure 1.12 A Schematic representation of the anodization of aluminum.

The anodization reaction can be described by the following reactions, but the details of the aluminum oxide film are more complicated.

$$H_2O + 2e^- \rightarrow O^{2-} + H_2 \qquad 1\text{-}4$$

$$Al_{metal} \rightarrow Al^{3+} + 3e^- \qquad 1\text{-}5$$

$$2Al + 3H_2O \Leftrightarrow Al_2O_3 + 3H_2 \qquad 1\text{-}6$$

The mechanism of oxide formation is well studied[23] Of particular interest is the high field model description of anodic oxide layer growth. The model postulates that during film growth ions move through the layer by hopping from one interstitial site to the next. The activation energy, W, of lattice hopping increases with the distance between the lattice vacancies, therefore hopping occurs between the closest neighbour sites.

When no potential is applied across the electrodes, lattice hopping of ions may occur in any direction through the oxide lattice with equal ease and W is the same for hopping towards and away from the anode. Upon the application of a potential across the electrodes, the resultant electric field lowers the activation barrier for hopping in the direction supported by the field and raises it in the opposite direction. The directional diffusion of ions through the growing dielectric film under applied potential is the origin of the anodic current flow, the result of which is the growth of the oxide layer.

An equation to describe the rate of growth of aluminum oxide films by anodization can be derived by calculating the rate of ion movement within oxide layer and is given by:

$$\frac{dd}{dt} = \frac{M}{\rho_{ox} yF} i_0 \exp\beta\left(\frac{U - U_0}{d}\right) \qquad 1\text{-}7$$

where M is the oxide molecular weight, ρ_{ox} is the film density, y is the number of electrons needed to form one molecule of oxide, F is Faraday's constant, β is a constant which depends on the lattice hopping distance and symmetry of the

lattice hopping activation barrier, and U is the potential at a given value of d, the oxide thickness. Equation 1-7 can be solved numerically, figure 1.13 plots the oxide growth calculated for Al_2O_3. Significant deviations from the calculated growth profile have been reported[24]

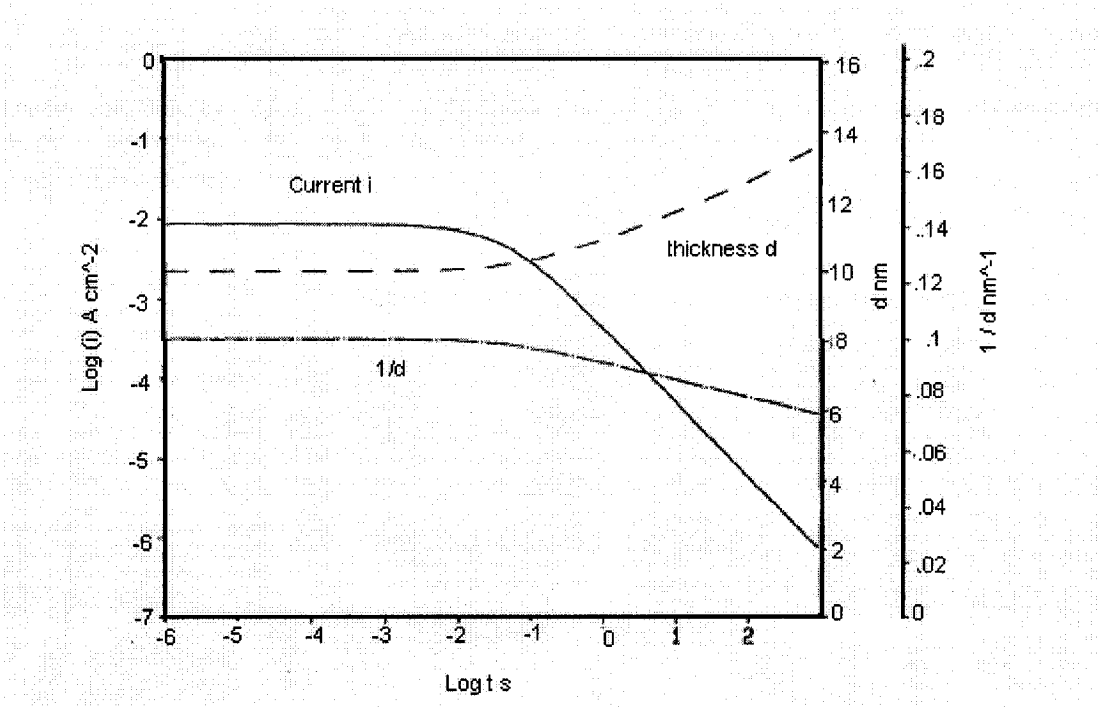


Figure 1.13 A logarithmic plot of current density i, oxide layer thinkness d and 1/d versus anodization time, using equation 1-7. Al metal where U=5 and E=8 MV/ cm (adapted from reference 23).

Early studies of the diffusion of ions through the dielectric postulated that oxygen ions were the charge carriers for oxide growth during anodization[25]. Later radioactive labelling experiments conducted by Chalk River Nuclear Laboratories confirmed that both anions and cations can be transported simultaneously. Today the transport of anions and cations during anodization is thoroughly understood and ratios of cation to anion transport have been calculated for Al

films between 0.2 and 0.5 depending on the applied field strength[26]. Figure 1.14 depicts the flow of charged species inside the growing dielectric film.

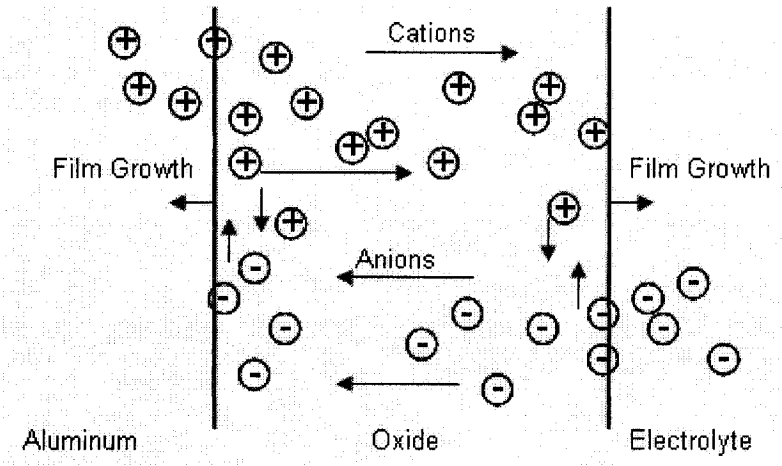


Figure 1.14 Schematic representation of oxide growth with a cation transport ratio of 0.5. The oxide grows at both interfaces (adapted from reference 23).

The morphology of aluminum oxide layers grown by anodization is varied[23] they can be extensively hydrated, amorphous, γ'-Al_2O_3 or γ-Al_2O_3[27].

The anodization technique employed in this thesis employs a buffered ethylene glycol/water/acid based electrolyte and a two stage anodization (TSA).

A two stage anodization involves a change in the current-voltage profile of the experiments from constant current to constant voltage (figure 1.15). This type of anodization has been shown to produce oxide layers of high density with low surface roughness compared to single stage constant current anodization, which results in large pores, and single stage constant voltage experiments, which results in dense films with high surface roughness[27].

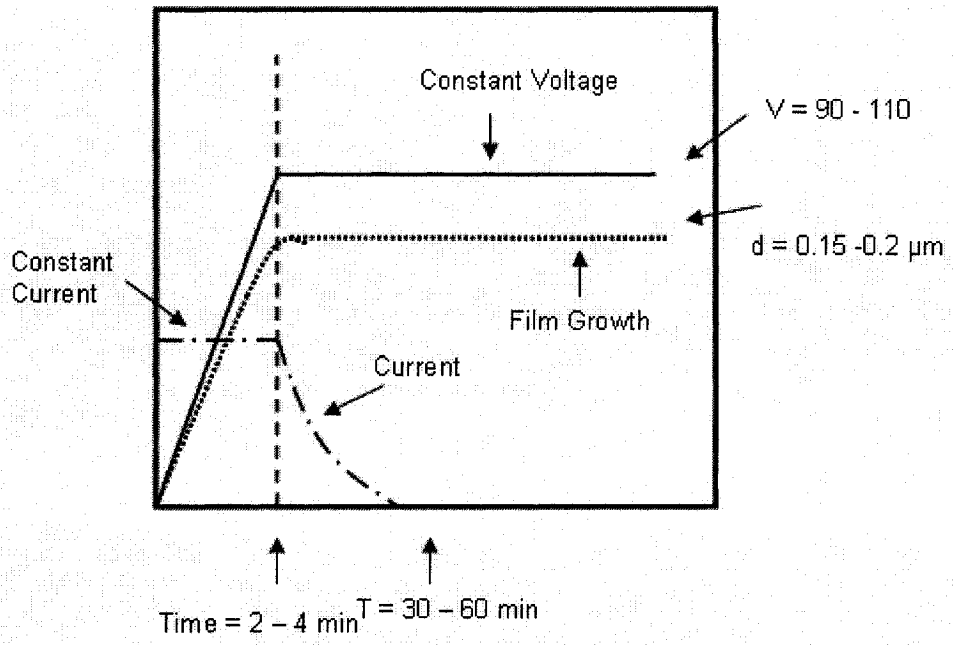


Figure 1.15 The current and thickness growth profile of an anodization experiment over time (adapted from reference 1).

Ethylene glycol based electrolyte TSA systems have been studied to determine the effect of electrolyte water content and pH on the quality of the resultant aluminum oxide film[28]. These studies found that a water content of between 20 and 40%, and a buffered pH of 6 led to dielectric layers with the highest breakdown voltage, lowest leakage current and slowest etch rate.

The influence of current density during the initial constant current stage of the TSA has been investigated[1]. Ghan and Shih showed that the highest breakdown voltages and lowest leakage currents for TSA films were achieved at current densities of between 1.1 and 1.3 mA/cm^2. They also found that annealing TSA films at 250°C for 2 hours under nitrogen reduced the leakage current of the dielectric by an order of magnitude relative to unannealed films. This observation is likely due to the dehydration of the oxide and the

crystallization of amorphous material into γ'-Al_2O_3, processes which are known to occur through heat treatment of anodized aluminum oxide[23].

1.2.4. Standard and Lift-off Photolithography

Photolithography is a micropatterning technique that is widely used in the fabrication of microelectronic and micro-electro-mechanical systems (MEMS) devices. Photo-patterning was used extensively in the conduct of our research to pattern the film layers into the layered structures that comprise the TFT array.

Two types of photolithography are relevant to the present discussion: standard lithography and lift-off lithography (figure 1.16). Standard lithography uses photosensitive polymer solutions to mask areas of an already deposited film layer so that exposed regions can be etched away. In lift-off lithography, the photosensitive material is patterned before deposition and a film layer is deposited onto the unmasked regions of the substrate. The lift-off process is completed by stripping the photoresist and overlying film, leaving the on substrate deposited material in place. Lift-off methods are useful when the substrate and structures that underlie the layer to be patterned are sensitive to wet-etch solutions.

Photolithography is simple in principle but difficult in practice. Careful consideration must be given to the type of technique selected and to the compatibility of the photoresist, developer, etchant, and stripper with the substrate and film components. Of the many lift-off layer techniques available

(e.g. negative resist[29], image reversal lift-off[30], pre-exposure developer treatment lift-off[31], bi-layer lift-off[32]) only a bi-layer liftoff process adapted from the work of Chang and Kempisty[33] was compatible with our fabrication process due to the sensitivity of the deposited layers to the wet etch techniques employed in this reseach.

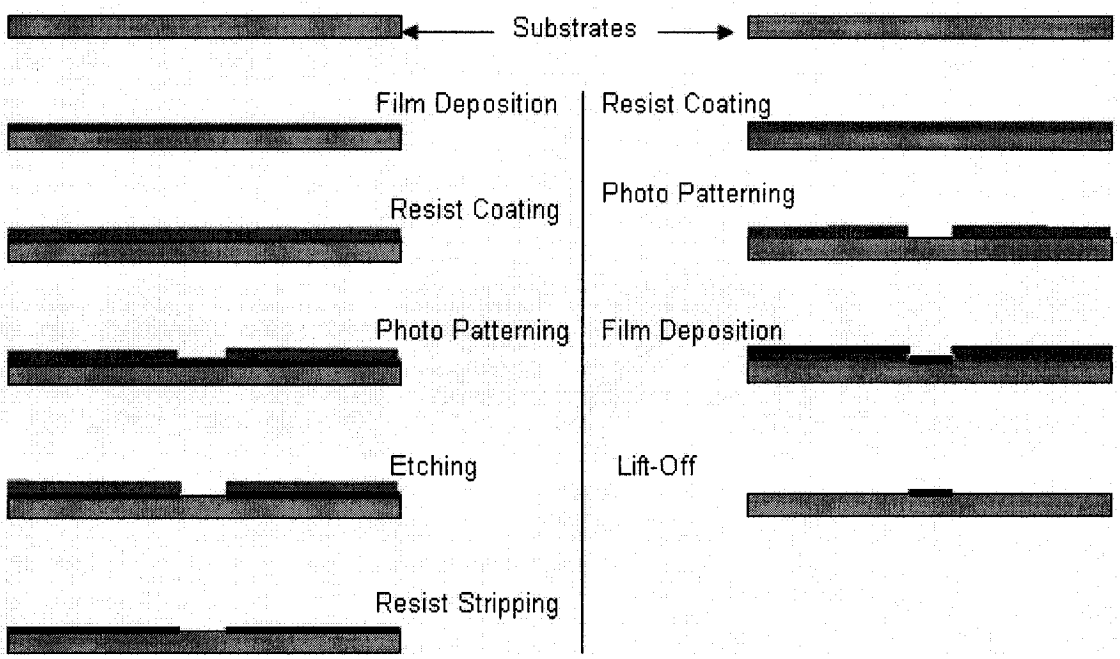


Figure 1.16 The process steps of standard and lift-off photolithography.

1.3 Substrates for TFT fabrication

TFTs have been fabricated on many different substrates, including glass[34], steel[35], and polymer substrates[36]. Careful consideration of the physical properties of a substrate material is required before a suitable candidate can be chosen. The present research calls for a transparent polymer substrate with the

following properties: good resistance to immersion in solvents such as water, acetone, and isopropanol, compatablility with photolithographic reagents such as developer and photoresist, the ability to sustain high temperature process condition without degrading, suitable surface properties that promote strong adhesion to overlying films, and mechanical properties that are compatible with those of the inorganic film layer (c.f. section 1.4).

	Arylite
Thermal	
Tg	325 °C
Decomposition temperature (at 5 wt% loss)	480 °C
CTE (-55 to 85 °C)	53
Flammability (UL94)	V-0
Optical	
%Transmission (400-700 nm)	90.4%
Refractive index (633 nm)	
base	1.64
coating	1.51
Retardation (100μm-thick film)	<10 nm
50% Cutoff wavelength	360 nm
Physical	
Young's modulus	2.9 GPa
Tensile strength	100 MPa
Elongation to break	17%
Specific gravity	1.22
Water absorption	0.4%
Electrical	
Volume resistivity (ohm.cm)	8.0×10^{16}
Surface resistivity (ohm/sq)	2.3×10^{17}
Dielectric constant (1 MHz)	3.4
Loss tangent (1 MHz)	9.0×10^{-3}

Table 1.2. Physical properties of Arylite. Chemical resistance: substrate resists all of the chemicals specified as follows: NMP, IPA, Acetone, Toluene, Methanol, Ethanol, THF, Ethylacetate, HMDS, H_2O, HCl-37%, H_2SO_4-98%, HNO_3-70%, H_3PO_4-85%, HBr-48%, CH_3COOH-glacial, $FeCl_3$, KH_2PO_4, H_2O_2-30%, sat. Na_2CO_3, sat. NaOH and sat. KOH.[37]

The commercially available amorphous engineering plastic, Arylite, manufactured by Ferrania Imaging Technologies of Italy, was found to possess the required material properties for successful, on-substrate fabrication of inorganic TFTs. The material properties of Arylite are summarized in Table 1.2[37]. The physical properties of Arylite, especially its Young's modulus, coefficient of thermal expansion, and rate of solvent uptake greatly effect the mechanical stress and strain that develop in the TFT-substrate couple during fabrication (c.f. section 1.4). Studies of solvent induced swelling and dimensional creep upon heating of Arylite[38] have shown that heat treatments can return Arylite substrates to their equilibrium dimensions after solvent immersion, and that dimensional creep in the polymer can be quenched out by extended heating at 300°C (figure 1.17).

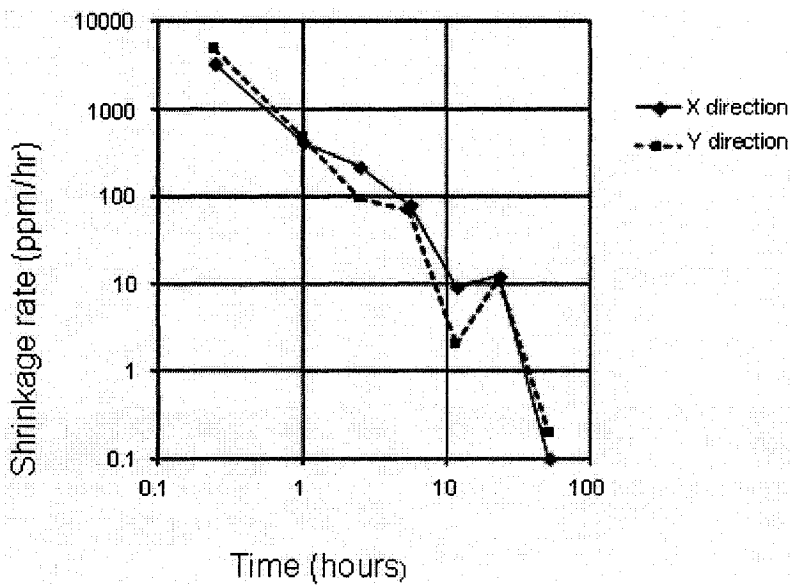
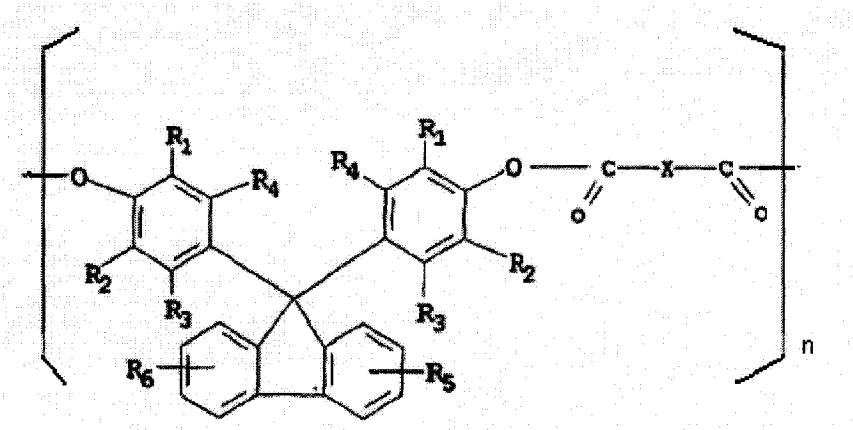


Figure 1.17 The dimensional creep of Arylite films upon heating to 300°C at under vacuum (from reference 38).

The exact structure of the Arylite polymer is unknown but patent data[39,40] suggests that it is polyaryl ester of the general formula:



1-7

where R_1 and R_2 independently represent an alkyl group, a halogen, an alkoxy group, an acyl group, a phenyl group or a nitrile group, R_3, R_4, R_5, and R_6 represent a hydrogen atom, an alkyl group, a halogen, an acyl group, a phenyl group, a nitro group, or a nitrile group and X represents a divalent hydrocarbon group having from 1 to 20 carbon atoms, or possibly a phenyl group.

The Arylite substrates used in the TFT fabrication process were 200μm thick and the top and bottom surfaces were received pre-coated with a 2μm thick "hardcoat". The hardcoat layer is a composite material composed of silica nano-particles and an unspecified acrylate polymer. Some researchers are working with similar composite coatings[41,42]. Interposing hardcoat between the bulk Arylite substrate and the inorganic film layer greatly affects the adhesion of film layers to the substrate (c.f. section 3.2)

1.4 The Mechanics of Thin Films on Flexible Substrates

One of the main difficulties that complicate the fabrication of inorganic TFT structures on the surface of flexible polymer substrates is the mismatch of physical properties between extensible organic materials and brittle inorganic materials. The tendency of polymer substrates to swell through the absorption of solvents, to expand upon heating as their flexible backbones and pendant groups sweep out larger and larger free volumes, and to exhibit hysteresis effects upon returning to initial environmental conditions, can destroy the mechanical integrity of inorganic films deposited on them.

These differences between substrate and film render standard TFT manufacturing practices extremely difficult or impossible. An understanding of mechanics of laminate film structures is essential to mitigating these difficulties and designing new approaches to manufacture that are better suited to flexible substrates.

The mismatch of physical properties between the rigid inorganic films that form the TFT structures presented in this manuscript and the compliant polymer substrate, upon which these structures are built, causes strain and generates stress in the film and substrate layers. The build up of forces within the layers can cause deformations and curvature of the substrate and, if they become too large, can damage transistors by causing cracking and delamination of the thin film structures.

The forces acting on the patterned substrate can be classified as either internal or external. External forces result from macroscopic mechanical bending or shaping and are not considered here. Internal forces are introduced by differential thermal expansion and contraction, and by dimensional changes that occur when the substrate absorbs solvents or releases them through evaporation. Internal forces are introduced into the TFTs and substrate during microlithographic processes such as photoresist deposition and patterning, metal film deposition, etching, developing, photoresist stripping, rinsing, and annealing.

The phenomena that result from the deposition and manipulation of multilayer films of dissimilar mechanical properties can be understood using the concepts of stress and strain. Stress, σ, is the force applied to an area. Strain, ε, is the response to that applied force. The relationship between stress and strain is given by the equation:

$$\sigma = Y\varepsilon \qquad 1\text{-}8$$

where Y is the experimentally determined elastic modulus of the material. A material with a low elastic modulus will exhibit deformation when small amounts of stress are applied, whereas a material with a high modulus will resist deformation and is typically hard and brittle. A material with an elastic modulus, will exhibit elongation with recovery, provided the elongation has not been taken to the break point. The values of stress and elastic modulus are espressed in units of pressure, and strain is usually expressed as a percentage. The elastic

moduli of materials like insulators, silicon, II-VI semiconductors, metals, and glass are between 50 and 250 GPa, whereas polymer substrates are more compliant, with an elastic modulus of ~5GPa.

Approximating the TFT structures on the substrate as a single film layer greatly simplifies the calculation of the stress-strain relationship, but still yields useful insights into the problems of stress management, accumulation and dissipation in multilayer structures.

Two types of film-substrate coupling are important to a discussion of the mechanics of TFT backplanes: the compliant film case and the compliant substrate case. Denoting the modulus and thickness of the substrate and deposited film layer by Y_s, d_s and Y_f, d_f respectively, if the product $Y_f d_f << Y_s d_s$ then the interaction is in the compliant film regime. In the case of $Y_f d_f \cong Y_s d_s$ the interaction is in the compliant substrate regime.

Because the modulus of glass substrates is large and the substrate thickness is much greater than the thickness of the deposited thin film layer, traditional TFT devices on glass substrates have compliant films. The substrate, therefore, dominates the mechanical response and the film complies with the substrate. There is little stress in the substrate and little curvature in the film-substrate couple.

TFT structures on polymer substrates have compliant substrates. The high modulus of the thin film structures and their resultant rigidity induces a complex mechanical response in polymer substrates of low modulus.

Mismatch Strain and Substrate Curvature: Mismatch strain, ε_o, is strain that is built into a film during its deposition or by some sort of treatment. Mismatch strain will induce a stress, σ_o, in the film. The mismatch strain is positive when the stress it induces is tensile. A variable thermal expansion mismatch strain, ε_{th}, is induced by changing the temperature, ΔT, of the film-substrate couple. The different thermal expansion coefficients of the substrate, α_s, and the overlying film, α_f, results in thermally induced strain upon heating or cooling. Differences in the moisture absorption characteristics of substrate and film layer give rise to the moisture absorption mismatch strain. The moisture absorption coefficient of expansion, β, is measured in ppm/ % relative humidity. The total mismatch strain, ε_{Mtot}, is given by:

$$\varepsilon_{Mtot} = \varepsilon_0 + (\alpha_f - \alpha_s)\Delta T - (\beta_f - \beta_s) \times \%RH \qquad 1\text{-}9$$

For a stiff substrate, the overlying film must conform to it (compliant film) and the biaxial stress will develop in the plane of the film. The stress experienced by the film is then:

$$\sigma_f = \varepsilon_{Mtot} Y_f^* \qquad 1\text{-}10$$

where Y_f^* is the biaxial elastic modulus of the film, $Y_f^* = Y_f/(1-\nu_f)$, and ν_f is the poisson ratio of the film. The stress, which is concentrated in the film layer will

cause the substrate to curve. For stiff substrates the radius of curvature is given by the Stoney equation:

$$R = \frac{Y_s^* d_s^{\,2}}{6\sigma_f d_f} \qquad 1\text{-}11$$

Because the biaxial elastic modulus of the stiff substrate is large, the radius of curvature is also large.

On compliant substrates the stress that results from mismatch is distributed between the stiff film and the compliant substrate. If the film-substrate couple is assumed to be flat, then the stresses of the film and subtrate layer are given by:

$$\sigma_f = \frac{\varepsilon_{Mtot} Y_f^*}{1 + Y_f^* d_f / Y_s^* d_s} \qquad 1\text{-}12$$

and

$$\sigma_s = -\sigma_f d_f / d_s \qquad 1\text{-}13$$

An examination of equation 1-13 reveals that, because $Y_f^* d_f \cong Y_s^* d_s$ the stress in the film on a compliant substrate is reduced by approximately a factor of 2 over the case for rigid films. It is also apparent from equation 1-14 that the stress in

the compliant substrate is much less than the stress in the film layer, as the thickness of the substrate is typically much greater than the thickness of the deposited TFT layers.

The assumption that the film-substrate couple is flat, though reasonable in the compliant film case (where the radius of curvature is extremely large), does not hold for compliant substrates. The radius of curvature for the compliant substrate case is given by:

$$R = \frac{\left(\bar{Y}_s d_s^{\,2} - \bar{Y}_f d_f^{\,2}\right)^2 + 4\bar{Y}_f \bar{Y}_s d_f d_s \left(d_f + d_s\right)^2}{6\varepsilon_{(1+\nu)} \bar{Y}_s d_f d_s \left(d_f + d_s\right)} \qquad \text{1-14}$$

where $\bar{Y} = Y/(1-\nu^2)$, the in-plane strain elastic modulus. Figure 1.18 plots the normalized radius of curvature, calculated using equation 1-14 for rigid substrates and compliant substrates. The radius of curvature for compliant substrates is displaced downwards relative to film-substrate coupling with similar Y values. An examination of the curves shows that the radius of curvature is largest when the film thickness is very small relative to the thickness or the substrate, or when the film thickness is somewhat larger than that of the substrate.

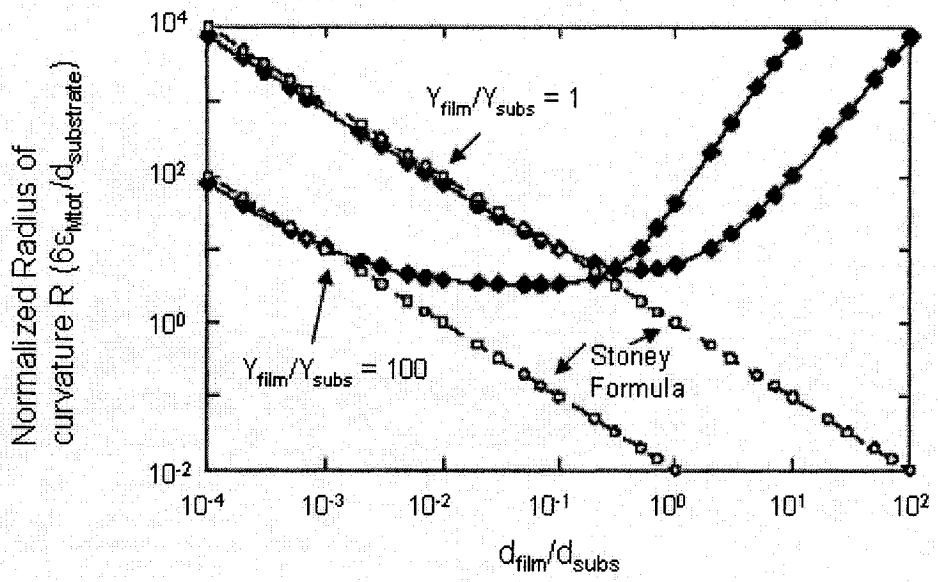


Figure 1.18 The normalized radium of curvature for rigid and compliant substrates for different film thicknesses (adapted from reference 43).

A better understanding of how stress distributions are altered when a substrate curves can be gained by first examining the case for a stiff substrate curved through the application of an external mechanical force. Because the top surface of the rigid substrate is in tension and the bottom surface is in compression (figure 1.19), there exists a region between the two extremes that has no strain, the neutral plane. Since rigid substrates have elastic moduli close to that of TFT materials the neutral plane occurs at the mid-surface of the laminate structure.

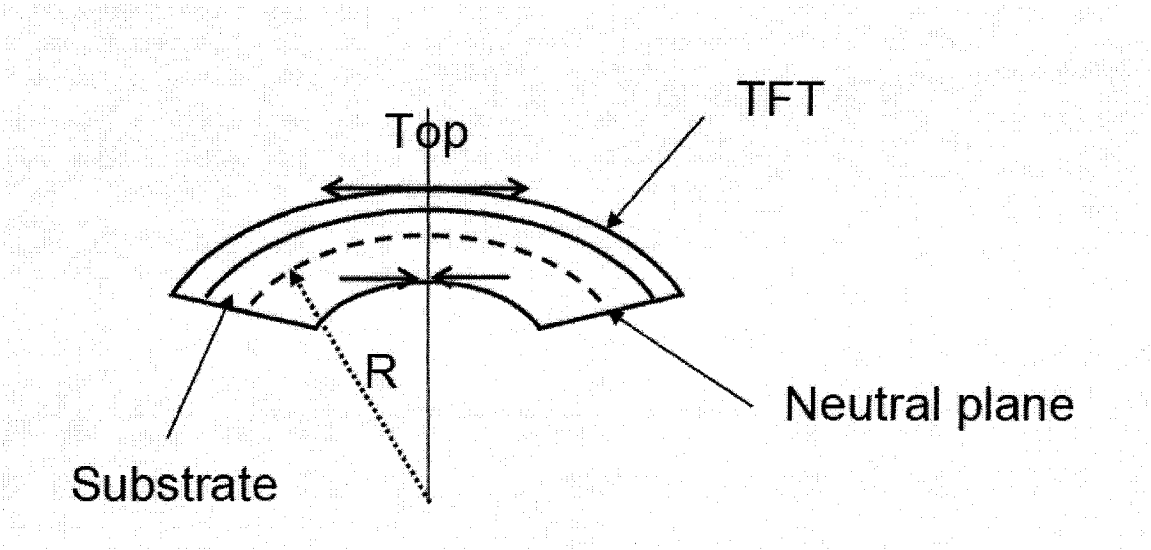


Figure 1.19 Tension and compression on a curved rigid substrate TFT array.

The strain at the top surface, ε_{top}, is given by:

$$\varepsilon_{top} = \left(d_f + d_s\right) / 2R \qquad 1\text{-}15$$

In the case of compliant substrates, the fact that $Y_s < Y_f$ means that the neutral plane of the curved laminate will shift towards the film surface and the strain at the top surface is reduced. The strain at the film surface for compliant substrates is given by:

$$\varepsilon_{top} = \left(\frac{\left(d_f + d_s\right)}{2R}\right) \frac{1 + 2\eta + \chi\eta^2}{(1+\eta)(1+\chi\eta)} \qquad 1\text{-}16$$

where $\eta = d_f / d_s$ and $\chi = Y_f + Y_s$. A comparison of normalized strain at the top surface of laminate structures with rigid and compliant substrates (figure 1.20) reveals that for a given R value and film/substrate thickness ratio the top surface strain can be reduced by a factor of 5.

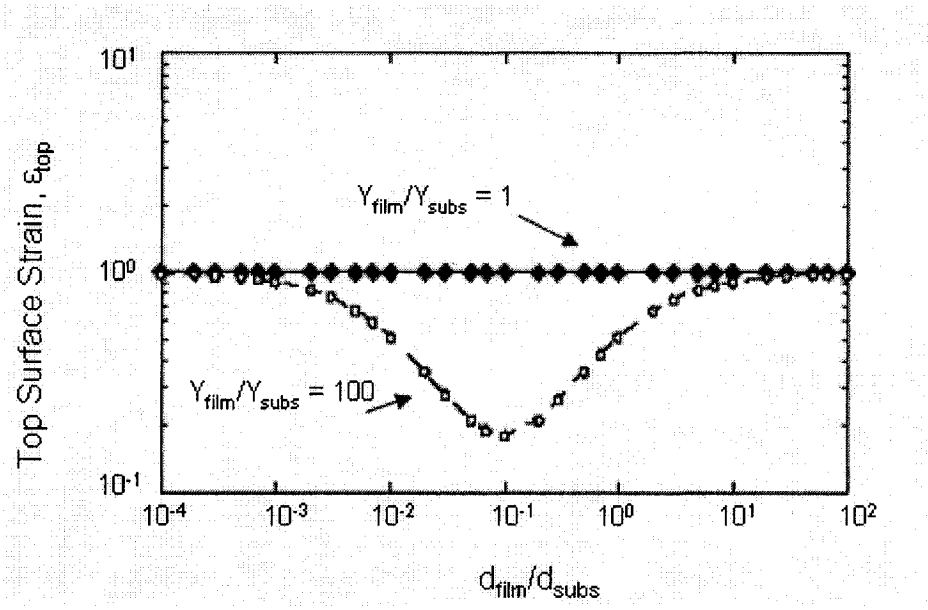


Figure 1.20 The strain at the top surface of a curved substrate-film couple for a given R value (adapted from reference 43).

Effects of Mechanical Strain on TFT Structures: Studies of mechanical strain on TFT have been conducted for amorphous silicon structures on polymer[43]. The experimenters noticed three regimes of strain influence TFT function. In the safe regime TFT function could be measured, though semiconductor mobility was observed to decrease under compression and increase under strain. In the definitive mechanical failure regime, the TFT ceased functioning and did not recover upon removal of the mechanically induced strain. The transition regime was the most interesting observation.

Strain in the transition regime resulted in loss of transistor function with recovery upon the removal of the compressive or tensile strain. It is also notable that the strain induced effects occurred more readily under tensile strain (figure 1.21)

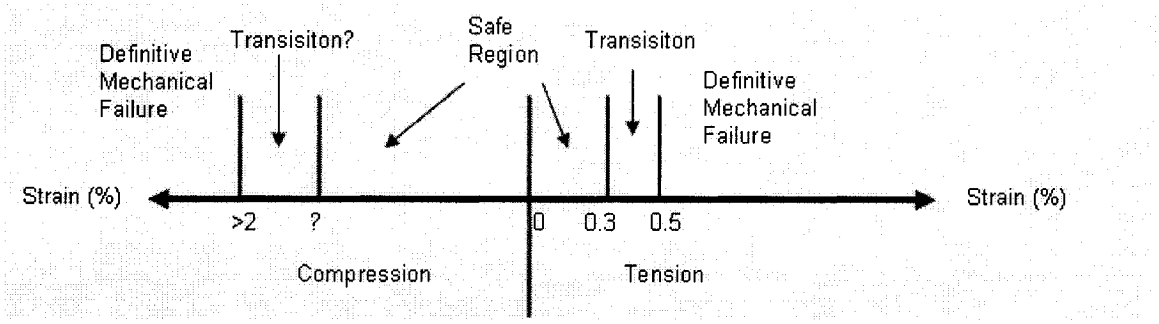


Figure 1.21 The three regimes of transistor function under strain (adapted from ref 43

The mechanism of TFT failure is different under compressive or tensile strain. Tension induces failure by crack propagation from pre-existing defects. Under compression, TFTs fail by delamination followed by buckling and fracture. Schematic representations of these failure mechanisms are presented in figure 1.22.

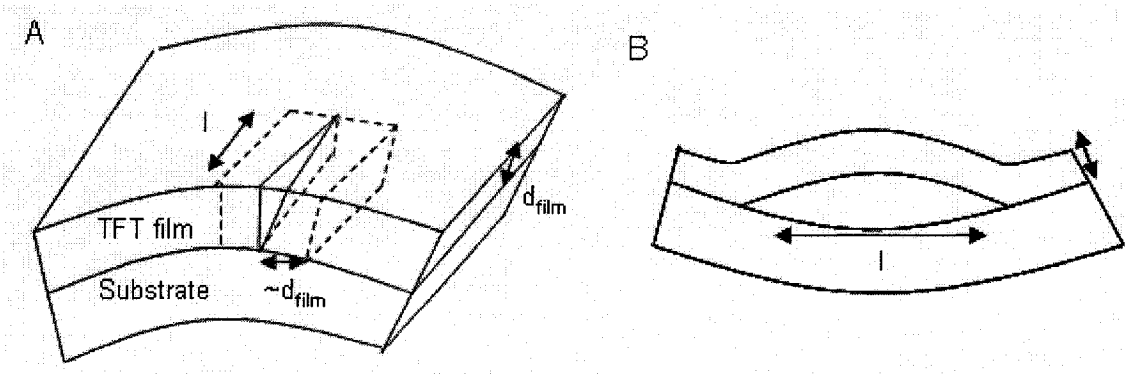


Figure 1.22 Failure mechanisms of rigid films under A) tension and B) compression

The control of stress in compliant substrate TFT laminates is much more difficult than for rigid substrates. Careful consideration of TFT design and substrate selection is critical to success. Mechanical effects observed on the compliant substrate TFTs produced over the course of this research are examined in Chapter 3.

1.5 Chemical Bath Deposition of II-VI Semiconductors

The deposition of semiconducting films at low temperatures by physical deposition methods, such as low pressure chemical vapour deposition (LPCVD), on polymer substrates is expensive and difficult. The low temperature deposition of semiconductor films from solution is an alternative strategy that benefits from low equipment costs, versatility, and simplicity. Chemical bath deposition was utilized in this research to deposit a CdS semiconducting film layer, the heart of the fabricated TFT structures. The chemistry of the deposition technique is presented below.

The technique of chemical bath deposition (CBD) has been known for over a century. Initially II-VI materials such as CdS were exploited for their vibrant colour for use in paints and pigments as well as for decorative films that highlighted the beautiful iridescence of deposited films. More recently, the semiconducting properties of CdS and CdSe have been investigated for use in

electronics and photovoltaic devices. This renewed interest has spurred work on illuminating the chemical mechanism of CBD deposition reactions.

Chemical bath deposition is a generic term given to the kinetically controlled deposition of solid films from solution, typically without changing the oxidation state of the metal deposited[44]. The driving force for the formation of metal chalcogenide films is the extremely low solubility product of their ionic components with the corresponding solid (eg K_{sp} CdS = $1x10^{-26}$)[45]. The details of the reaction are much more complicated as an investigation of the mechanism of deposition and the structure of the resulting films will show. An explanation of the role of solution complexation, nucleation, ion-by-ion versus cluster-by-cluster film growth, the morphology of grown films, the ionic strength of the deposition solution, substrate selection, autocatalysis of particle and film growth and the temperature dependence of the reaction are presented in this section.

The Mechanism of CBD deposition: The description presented here will focus on CBD deposition studies of CdS films from solutions containing a thiourea chalcogenide source and using an ammonia complexant, for which the body of research available is the greatest. The same principles can be extended to other systems that employ other metals (Zn, Sb, Pb, Cu, Co, Sn, Mo, and Ag), other chalcogenide sources (thioacetamide, thiosulphate, and allylthiourea for sulphides or selenourea and selenosulphate for selenides)[46,47,48,49] and other complexants (triethanolamine, citrate, tartrate, and diethylamine).

Four main aqueous reactions govern the solution phase behavior of CdS deposition in the thiourea/ammonia system.

$$NH_3 + H_2O \Leftrightarrow NH_4^+ + OH^- \quad \text{1-17}$$

$$Cd(NH_3)_4^{2+} \Leftrightarrow Cd^{2+} + 4NH_3 \quad \text{1-18}$$

$$S = C(NH_2)_2 + 2OH^- \rightarrow S^{2-} + H_2NC \equiv N + 2H_2O \quad \text{1-19}$$

$$Cd^{2+} + S^{2-} = CdS_{(s)} \quad \text{1-20}$$

The addition of ammonia to the deposition solution (equation 1-17) determines the pH of the solution. Since ammonia is the complexant in equation 1-18 and the source of hydroxide ions for the hydrolysis of thiourea (1-19), it is of critical importance to the CBD process. The concentration of complexant and cadmium ions determines the concentration of free metal ions in solution and the chalcogenide source concentration and pH determine the concentration of sulfide ions. When the concentration of sulphide and cadmium ions is high enough that the solubility product of CdS is exceeded the deposition begins.

The concentration of metal ions, chalcogenide sources, complexant and hydroxide ions determines the rate of CdS formation and whether the semiconductor forms as a film or as particles dispersed in reaction solution. The morphology of deposited films also depends highly on the initial reagent concentrations because these determine whether the film will grow by an ion-by-ion process, by the aggregation of colloidal particles from solution on the surface of the substrate, or by a combination of the two mechanisms.

Since the initial experiments conducted on CdS films[50], researchers have observed two types of film formation: dense, adherent, specularly reflecting films, or powdery, non-adherent films. An explanation of these observations has been

proposed. The arguments on a surface mediated deposition mechanism that results in ion-by-ion film growth[51,52,53,54] and is summarized by the following reactions.

$$Cd(NH_3)_4^{2+} + 2OH^- + site \Leftrightarrow [Cd(OH)_2]_{ads} + 4NH_3 \qquad 1\text{-}21$$

$$[Cd(OH)_2]_{ads} + S = C(NH_2)_2 \rightarrow [Cd(S = C(NH_2)_2)(OH)_2]^*_{ads} \qquad 1\text{-}22$$

$$[Cd(S = C(NH_2)_2)(OH)_2]^*_{ads} \rightarrow CdS + H_2NC \equiv N + 2H_2O + site \qquad 1\text{-}23$$

The key features of the above series of reactions are, the formation of an adsorbed surface complex $[Cd(OH)_2]_{ads}$, and the subsequent surface mediated decomposition of complexed thiourea to form CdS on the substrate. The involvement of cadmium hydroxide to the on-film deposition of CdS was first confirmed by radiochemical experiments[55]. Later experiments showed that the forming film catalyzes the on-film deposition reaction and that substrates precoated with PbSe exhibited film growth in CBD solution without $Cd(OH)_2$ precipitates[56].

CdS films will form on the substrate by the surface mediated ion-by-ion mechanism only in the presence of the $Cd(OH)_2$ complex. The formation of the hydroxide complex depends strongly on the concentrations of complexant, cadmium ions and hydroxide (pH) (figure 1.23). At a given Cd salt concentration, hydroxide complexes will be stable in the CBD solution above the hydroxide line in the figure (regions I and II). Conversely, $Cd(NH_3)_4$ complexes are only stable below the complex line. Because large amounts of solid $Cd(OH)_2$ precipitate can nucleate the formation of CdS in the bulk CBD solution as well as on the substrate surface, the quality of CdS films is higher when the deposition solution

is maintained in region I of the pH/complexant coordinate system, where the formation of the ammonia complex competes with the formation of metal hydroxide.

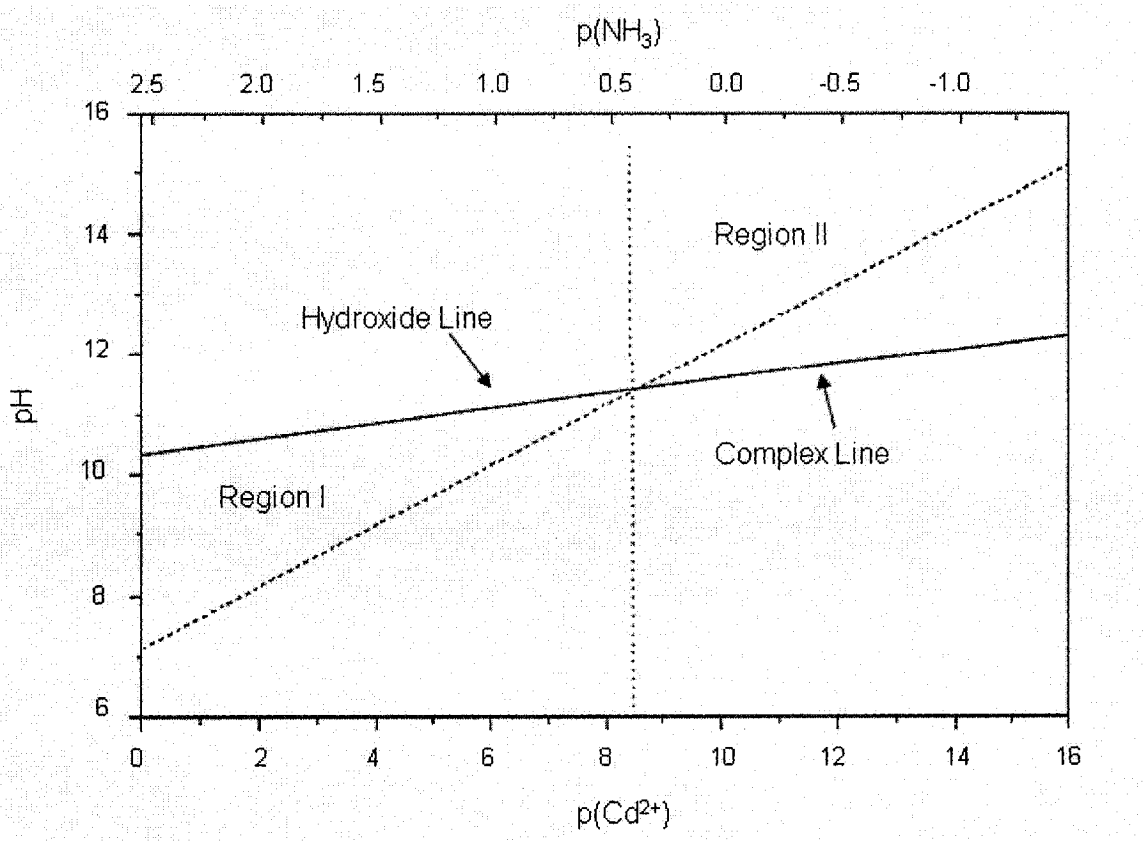


Figure 1.23 The complexant and pH regimes where $Cd(OH)_2$ will form. For $[Cd^{2+}] = 10^{-3}$ M and [Thiourea] = 10^{-2} M (adapted from ref 44).

Based on the information presented so far, the deposition of a dense, specularly reflecting film of CdS seems to be a simple matter of selecting the complexant and hydroxide concentrations necessary to promote ion-by-ion film growth, while suppressing the formation of solution phase crystals and

aggregates. Unfortunately, this is not the case. Gorer and Hodes have observed that as a deposition reaction proceeds the mechanism of film growth changes as the total concentration of metal ions in the solution phase decreases[57]. If precipitated metal ions are disregarded, the ratio of complexant to total metal ion concentration grows as the deposition proceeds. The result of this changing equilibrium is that the concentration of free metal ions (pCd^{+2}) does not remain constant but decreases as the metal chalcogenide solid forms. Figure 1.24 gives the calculated ratios of complexant to total metal concentration necessary to maintain a pCd^{+2} of 9. In practice this ratio is impossible to maintain throughout a deposition because the concentration of complexant is constant.

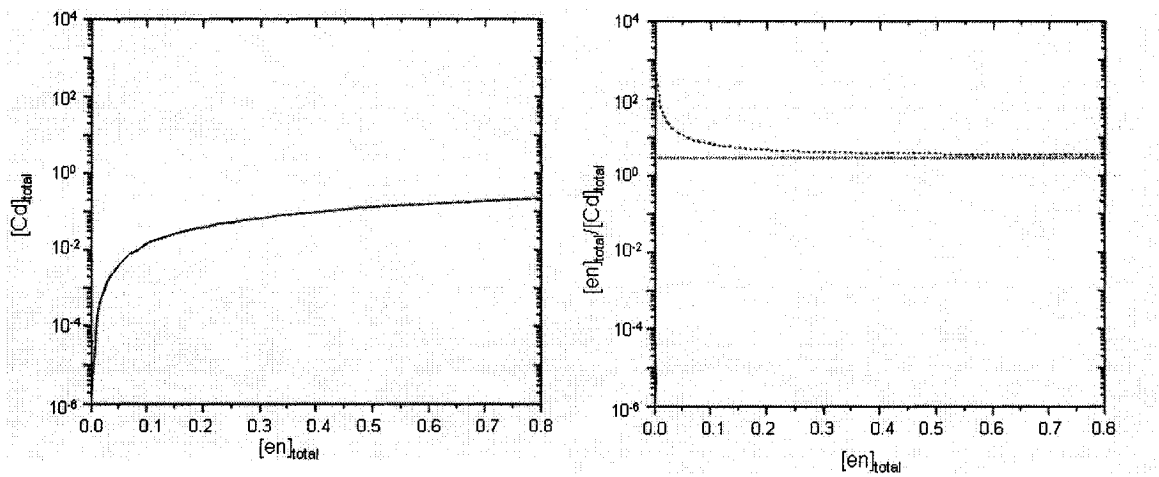


Figure 1.24 Equivalent solution contour plot: the total metal salt concentration vs the total ligand concentration at constant uncomplexed metal ion concentration. For pCd^{2+} = 9 at 50°C for nitrilotriacetate ligands (adaptded from ref 44).

As the concentration of free cadmium ions in the CBD solutions decreases the formation of CdS via ion-by-ion growth slows and the solution phase precipitation of CdS via hydroxide mediated decomposition of thiourea becomes

the dominant reaction. Generally grown as deposited films tend to be formed by a mixture of ion-by-ion growth and solution precipitate inclusions (figure 1.25).

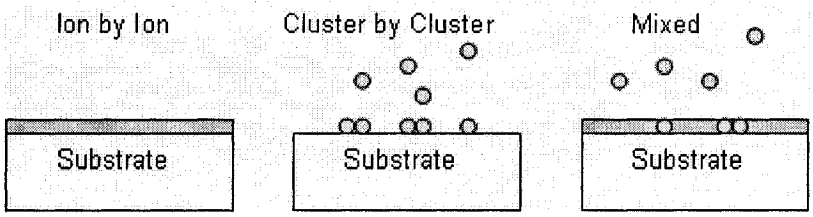


Figure 1.25 Three types of grown films.

Effect of Metal Salt Counterion Selection and the Addition of Ammonium Salts: Many CBD experiments introduce ammonium salts into the deposition solution as a buffer for ammonia in order to reduce the pH of the deposition bath while maintaining high complexant concentrations[1]. The addition of ammonium salts also appears to affect the deposition reaction in other ways.

Akintunde highlighted these effects in his research on the $CdSO_4$, $(NH_4)_2SO_4$, ammonia, thiourea system[57]. In a series of reactions maintained at pH 9.5, different concentration of ammonium salts were found to greatly influence the quality of the resultant CdS films. At low ammonium concentrations the reaction yielded large amounts of precipitate and non-adherent films. Higher ratios of ammonium salt to cadmium salt improved the quality of the deposited films and the induction period before film deposition began. At ten times excess salt concentration, the deposition lag time was 8 minutes and the resultant films were adherent, specularly reflecting, with a thickness of 120nm. Increasing the ammonium concentration to 15 and 20 times excess extended the film induction

time to 15 and 22 minutes respectively and generated films of approximately 100nm. The most interesting feature of this experiment is that for salt ratios of 10 or higher no CdS precipitate was observed suspended in the solution during the reaction.

The origin of this effect is the increased complexation of Cd^{+2} ions by ammonia. Because the cadmium ion in solution is sequestered by $Cd(NH_3)_4^{+2}$ complexation, it is not free react with sulphide ions generated by thermal decomposition of thiourea, meaning that film formation by the ion-by-ion mechanism is favored.

The excess complexant concentration also appears to affect the stoichiometry of the resulting films[58]. At high excess complexant concentrations, CBD deposited CdS films exhibit non-stoichiometric sulphide content (as much as 2% excess sulphur content). The exact mechanism of this effect is not known but is likely due to relative concentrations of free cadmium and sulphide ions.

The Morphology of CBD Deposited Films: The growth mechanism of CdS greatly affects the morphology of resultant films. The study of how different grain structures arise allows on to select deposition conditions that favour the formation of films with enhanced semiconductor properties (e.g. better stoichiometry, fewer charge carriers, and larger mobility).

Rieke and Bentjen[45] conducted an extensive series of experiments using X-ray photoelectron spectroscopy (XPS) and electron microscopy to track the growth of CdS films during CBD. Their results showed that film growth proceeds

in three phases. The first is the formation of a thin film of $Cd(OH)_2$ on the substrate surface. Interestingly, the hydroxide layer formed on the film at deposition pH is too low for the formation of bulk solution suspended cadmium hydroxide precipitates. The hydroxide layer formation phase of the deposition, which takes several minutes is followed by a very short CdS grain nucleation phase. Electron microscopy revealed a crystallite nucleation density of around 70 sites per square micron of substrate surface. After nucleation, the growth of CdS proceeded outward from the nucleation sites to form CdS islands. The growth rate appeared to be catalyzed by the growing film surface area. The experimenters observed a growth rate 2.8 times the diameter of the forming CdS islands that corresponded to a fractal surface growth area for substrate bound crystallites.

Lincot and Borges[51] investigated the impact of different concentrations of thiourea on the microstructure of CdS films. By using a combination of quartz crystal microbalance and capacitance measurements from a specially designed deposition apparatus, they were able to measure the growing films in situ. These experiments allowed the measurement of not only the amount of material deposited on the substrate but the point at which the nucleated sites coalesced from islands to a solid film layer (the point at which the capacitance and microbalance measurements agreed). They could also measure the growth of non-adherent powdery layers on top of the dense layer because the deposited mass as measured by the microbalance measurement diverged from the capacitance measurements in the later stages of deposition. Licot and Borges

found that a 2-fold excess of thiourea with respect to cadmium salt led to a short inductance, followed by a long coalescence period, indicating large grains and relatively few nucleation sites. A 10-fold excess of thiourea yielded a short inductance period, followed by a short coalescence time, indicating small grains in the growing film and a large number of nucleating sites.

The best results were achieved when allylthiourea was substituted for thiourea at 2 times excess concentration. The combined measurement results showed a large coalescence time, suggesting grains of around 140nm. The deposition measurements after coalescence of the nucleation islands showed very good agreement between the microbalance an capacitance measurements indicating an extended period of compact film growth. Figure 1.26 shows how the microstructure of grown films changes from dense to porous and finally powerdery as depositions proceed.

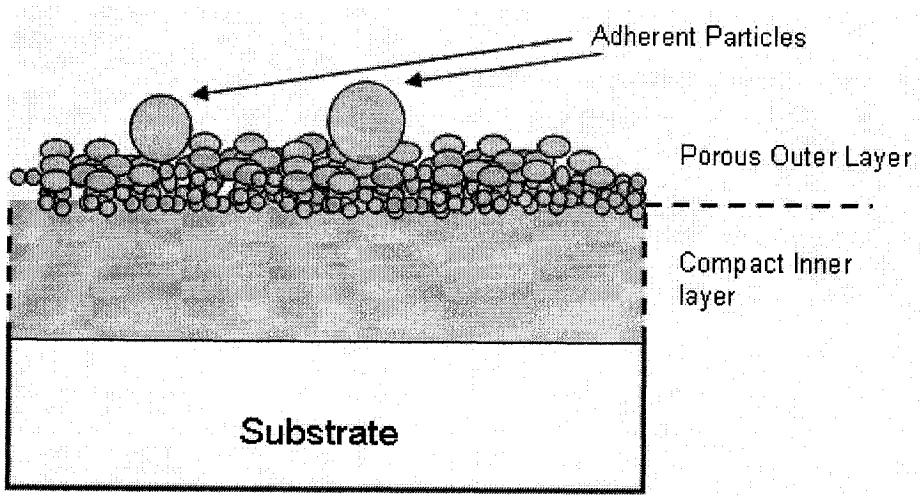


Figure 1.26 Schematic representation of the two phases of CdS films growth.

No inductance period was found for the growth of films on substrates pre-coated with a CdS layer and the films grew over the entire area of the substrate immediately without nucleation and coalescence, confirming the autocatalytic effect of the the CdS surface. Ghan and Shih exploited this effect by depositing their CdS layer in successive CBD immersions to produce thick dense films with minimal particulate inclusions.

Studies of the crystal structures of deposited CdS films[44] variously reveal hexagonal close packing, cubic, or mixture of the two. Stacking faults seem to be responsible for the change from hexagonal structure to cubic during depositions[59,60]. The number of stacking faults depends on the selected deposition conditions.

CdS films deposited by the ion-by-ion mechanism exhibit lattice orientation perpendicular to the substrate. Electron micrographs of dense films in cross section show grain structures that seem to form "towers" of oriented crystals. These features result because as the islands where nucleation originates coalesce, the grains continue to grow upward in a highly oriented fashion. Interestingly, visual evidence suggests that even after coalescence the grain boundaries between islands are maintained at the interface as the towers grow.

The Effect of Morphology and Film Composition on Semiconductor Properties of CdS: The semiconductor properties of monocrystaline CdS and CdSe are exceptional (e.g. the Hall effect mobility of bulk CdS is ~250 $cm^2/Vsec$ at room temperature and 10 times higher for CdSe)[61]. The fact that reported mobilities of these semiconductors when deposited by CBD are 100 to 1000

times lower than the theoretical maximum highlights the fact that managing the microcrystalline properties of CBD deposited CdS and CdSe is vital to the production of high quality transistors. Vast improvements in semiconductor properties may be possible through careful implementation of CBD process changes not explored by researchers to date because of their focus on the optoelectonic properties of CdS and CdSe films and their application to photovoltaic cells.

The problem of low mobility in microcrystalline CdS deposited by CBD is presented more fully in Chapter 3 along with a discussion of possible improvements to the deposition process.

References

1. Ghan, F.Y., *Ph.D. Thesis,* (McGill University, Montreal, Canada, 2001).

2. Neamen, Donald, *An Introduction to Semiconductor Devices*, (McGraw Hill, New York, 2006).

3. Banerjee, Sanjay, Streetman, B. G., *Solid State Electronic Devices*, 5th ed., (Prentice Hall, New Jersey, 2000).

4. Yang, E. S., *Microelectronic Devices*, (McGraw Hill, New York, 1988).

5. T. P. Niesen, M. R. de Guire, *Journal of Electroceramics*, **6**, 169-207 (2001).

6. I. Langmuir, Phys. Rev. **33**, 954 (1929).

7. Ohring, M., *The Material Science of Thin Films*, 2nd ed., (Academic Press, San Diego, CA, 2002).

8. Venables J. A., *Introduction to Surface and Thin Film Processes*, (Cambridge University Press, Cambridge, England 2000).

9. Elshabini-Riad, A. and Barlow III, F. D., *Thin Film Technology Handbook*, (McGraw Hill, USA1998).

10. Seshan, K., *Handbook of Thin Film Deposition: Processes and Technologies* 2nd Ed., (Noyes Publications, USA, 2002).

11. Wertheimer, Michael R., Martinu, Ludvik, Klemberg-Sapieha, Jolanta E., Czeremuszkin, Gregory, *Materials Engineering*, **14**(Adhesion Promotion Techniques), 139-173, (1999).

12. Park, Young-Bae, Rhee, Shi-Woo, Li, Xiaodong,Thomas J., *Physica Status Solidi A: Applications and Materials Science*, 13, **202**, 2448-2453, (2005).

13. Dasilva, W,. Entenberg, A, Kahn, B., Debies, T., Takacs, G. A., *Journal of Adhesion Science and Technology,* 5, **20**, 437-455, (2006).

14. Ryntz, Rose A., *Progress in Organic Coatings,* 1, **25**, 73-83. (1994).

15. Vandencasteele, N., Merche, D., Reniers, F., *Surface and Interface Analysis*, 4, **38**, 526-530. (2006).

16. Rohde, S. L., Muenz, W. D., *Adv. Surf. Coat.,* 92-126, (1991).

17. Sigmund, P., *Springer Series in Chemical Physics,* **36**, 2-7. (1984)

18. Knorr, David B., Tracy, Daniel P., Lu, Toh Ming., *Materials Research Society Symposium Proceedings*, **202**(Evol. Thin-Film Surf. Microstruct.), 199-204, (1991).

19. Chang, C. Y., Vook, R. W., *Thin Solid Films*, **228**, 205-209, (1993).

20. Klein, L.E., Kushner, M. J., *Crit. Rev. Solid State Mater. Sci.,* **16**, 1, (1989)

21. Hamaguchi, S., *IBM J Res. Develop.*, **43**, 199, (1999)

22. Meeks, E., Larson, R. S., et al., *J. Vac. Sci. Technol.*, **A16**, 544, (1998)

23. Lohrengel, M. M., *Materials Science and Engineering*, **R11**, 243-294, (1993).

24. Young, L., *Proc. R. Soc. London*, Set. A, **258**, 496, (1960).

25. Banter, J.C., *J. Electrochem. Soc.,* **114**, 508, (1967).

26. Diggle, J. W., Downie, T. C., Goulding, C. W., *Chem. Rev.,* **69**, 365, (1969).

27. Yakovleva, N. M., Yakovlev, A. N., Repnikova, E. A., Chupakhina, E. A., *Inorganic Materials*, **39**, 374–378, (2003).

28. Liang, C. W., et al., *Materials Chemistry and Physics,* **43**, 166-172, (1996).

29. Chang, Shih-Chia, Kempisty, Jeffrey M. *Lift -off methods for MEMS devices,* Materials Research Society Symposium Proceedings (2002)

30. Spak, Mark, Sagan, John, et al. *SPIE Conference on Advances in Resist Technology and Processing XVI*, **SPIE 3678**, (1989)

31. Martin, Brian, Odell, Andrew N., *Microelectronic Engineering*, **9**, 567-70, (1989).

32. Paraszczak, Jurij R., Stewart, Kevin J., *Microelectronic Engineering*, 11, 549-52, (1990).

33. Shih-Chia, Chang, Jeffrey M., Kempisty, *Mat. Res. Soc. Symp. Proc.*, **729**.

34. Voutsas, Apostolos T., Hatalis, Miltiadis K., *Applied Physics Letters*, **63**, 1546-8, (1993).

35. Theiss, S. D., Wagner, S., *Materials Research Society Symposium Proceedings*, **424**, 65-70, (1997).

36. Forbes, C. E., Gelbman, A., Turner, C., Gleskova, H., Wagner, S., *Digest of Technical Papers - Society for Information Display International Symposium,* **33**, 1200-1203, (2002).

37. Angiolini, Simone, Avidano, Mauro, Barlocco, Carlo, Bracco Roberto, *Euro. Displays*, conference, (2002).

38. Angiolini, Simone, Avidano, Mauro, *Proc SID*, (2001).

39. Angiolini, Simone, Avidano, Mauro, Barlocco, Carlo, Bracco Roberto, *U.S. Pat. Appl. Publ.*, 13p. (2004).

40. Angiolini, Simone, Avidano, Mauro, Barlocco, Carlo, Bracco Roberto, *Eur. Pat. Appl.*, 22p, (2002).

41. Costa, R. O. R., Lameiras, F. S., Vasconcelos, W. L., *Journal of Sol-Gel Science and Technology,* **27**, 343–354, (2003).

42. Soloukhina, Victor A., Posthumusa, Willem, et al., *Polymer*, **43**, 6169–6181, (2002).

43. Suo, Z., Wagner, S., Gleskova, H., Ma, E. Y., *Appl. Phys. Lett.*, **74**, 1177 (1999)

44. T. P. Niesen, M. R. de Guire, *Journal of Electroceramics*, **6**, 169-207 (2001).

45. Rieke, P. C., Bentjen, S. B., *Chem. Mater.*, **5**, 43 (1993).

46. Lokhande, C. D., *Mater. Chem. Phys.*, **27**, 1 (1991).

47. Grozdanov, I., *Semicond. Sci. Technol.*, **9**, 1234, (1994).

48. Nair, P. K., Nair, M. T. S., Garcia, V. M., et al., *Solar Energy Mater. Solar Cells*, **52**, 313, (1998).

49. Savadogo, O., *Solar Energy Mater. Solar Cells*, **52**, 361, (1998).

50. Mokrushin, S. G., Tkachev, Y. D., *Colloid J. USSR*, **23**, 366, (1961).

51. Lincot, A., Ortega-Borges, R., *J. Electrochem. Soc.*, **139**, 1880, (1992).

52. Lincot, A., Ortega-Borges, R., *J. Electrochem. Soc.*, **140**, 3464, (1993).

53. Dona, J. M., Herrero, J., *J. Electrochem. Soc.*, **139**, 2810, (1992).

54. Dona, J. M., Herrero, J., *J. Electrochem. Soc.*, **144**, 4081, (1997).

55. Kitaev, G. A., Uritskaya, A. A., *Inorg. Mater.*, **2**, 1334, (1966).

56. Fofanov, G. M., Kitaev, G. A., *Russ. J. Inorg. Chem.*, **14**, 322, (1969).

57. Akintude, J. A., *Phys. Stat. Sol.*, **173**, 363, (2000).

58. Rusu, M., Rumberg, A., Schuler, S., *Journal of Physics and Chemistry of Solids,* 64, 1849–1853, (2003).

59. Froment, M., Lincot, D., *Electrochim. Acta*, **40**, 1293, (1995).

60. M. Froment, M.C. Bernard, R. Cortes, B. Mokili, and D. Lincot, *J. Electrochem. Soc.*, **142**, 2642 (1995).

61. Ray, Brian, *II-VI Compounds,* (Pergamon Press, Oxford, New York, 1969)

Chapter 2. The TFT Fabrication Process:

This chapter describes the fabrication processes developed in this research project.

All processing was carried either in the McGill Nanotools Facility clean room or at the Silk Displays clean room facility. Sputtering, PECVD and roughening instruments were located in a class 1000 environment under ambient room light. Spin-coating, aligning, work at the acid bench (where the CBD, photoresist developing, acid etching and rinsing were conducted) and anodization was conducted in a class 100 environment under yellow lighting. The clean room temperature was maintained at a constant 25°C and the relative humidity at 45% +/- 5%.

A schematic of the target TFT structure is depicted below (figure 2.1). A description of the fabrication process for each layer follows.

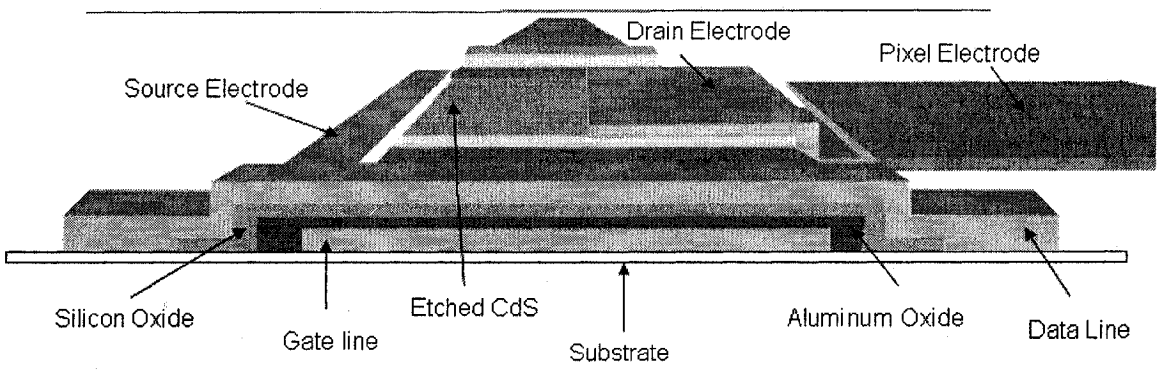


Figure 2.1 A schematic representation of a transistor unit of the TFT array.

2.1 Substrate Cleaning and Annealing

Arylite substrates were cut from rolls into 5"x5" squares and cleaned. The factory recommended cleaning method furnished by Ferrania calls for the sonication of the cut substrates in semiconductor grade propanol for 30 seconds, followed by a 30 second for rinse of the substrate. After rinsing the substrates may be dried under in a vacuum oven at 90°C and 1 millitorr for 8 hours[1].

Immediately prior to the gate line fabrication step the samples were plasma roughened to promote the adhesion of the deposited aluminum to the Arylite hard coat (c.f. section 1.3). The plasma roughening was conducted under an argon gas glow discharge plasma in an Semi Group PC5000A Reactive Ion Etcher (RIE) instrument.

2.2 Aluminium Gate Line Sputtering and Etching

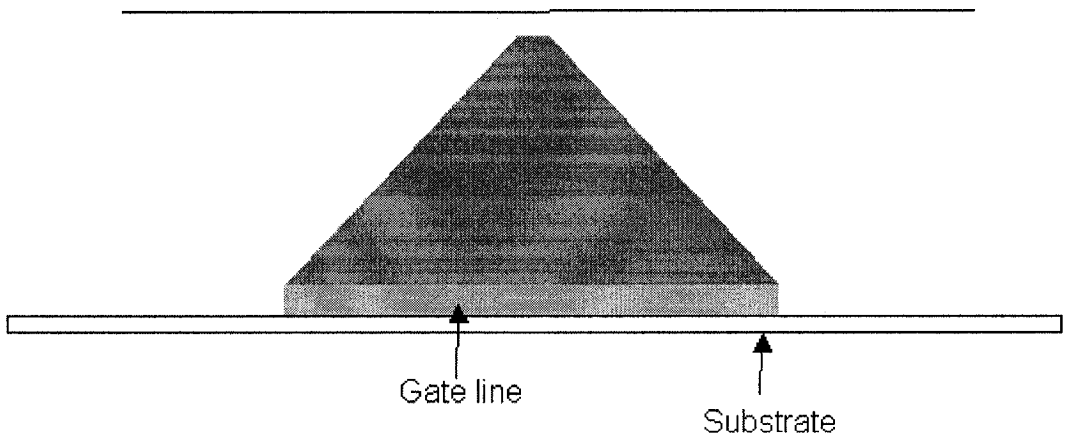


Figure 2.2 Schematic representation of the TFT gate lines (perspective drawing)

Immediately after the plasma roughening step, the Arylite substrates were transferred to the load lock of a Perkin Elmer 4419 sputtering instrument.

After transferring the substrates to the sputtering chamber the samples were allowed to degas under vacuum on the order of 2.5 $x10^{-7}$ torr. At this point aluminum deposition was conducted with an argon glow discharge plasma. The deposition power and gas pressures were experimentally determined to achieve mirror quality finish Al films. Deposition of aluminum by sputtering directly onto Arylite proved to be problematic. Because of the large kinetic energies of sputtered atoms (>20eV) compared to evaporation (~0.2eV), and the strong tendency of aluminum metal to oxidize (c.f. section 1.2.2), adventitious contaminants released from the substrate tended to generate large numbers of grain boundaries. In early experiments this led to films with very large surface roughness with a milky appearance. Therefore, great care was taken to achieve mirror finish quality of deposited aluminum films.

It was not possible to characterize the quality of the deposited aluminum films on Arylite by profilometry or four point probe conductance measurements, because the substrate was too soft to resist scratching by the probe tips. Instead, a glass slide was placed in the deposition instrument at the same time as the substrates, and was used to characterize the films. Thicknesses between 0.5 and 1μm were quantitatively reproduced. The thickness uniformity was +/- 10%. Aluminum conductance was typically ~ 3.5 $x10^{-6}\Omega cm$

The deposited aluminum films were patterned by photolithography and wet etched to form the TFT gate line structures. Photolithography used a Shipely 1827 positive resist.

Spin coating of flexible polymer substrates poses technical challenges, since most spin coaters and spin coater chucks are designed for use with rigid silicon wafer substrates. Several custom built chucks were designed and tested before resist layers of suitable thickness uniformity and minimal edge bead width were achieved.

The spin coating of the substrates was conducted at 3000rpm for 30 seconds followed by baking and exposure at ~180mJ/cm^2 under a Karl Suss MA56 contact mask aligner. Following developing the substrates were rinsed extensively; rinsing time was found to be more critical for Arylite substrates than for glass. After post baking, the substrates were wet-etched.

The etching of aluminum was initially conducted using Arch 16:1:1:2 commercial etchant at 45°C. Refinement of the technique eventually led to the development of an acetic acid free, "in house", mixture of acids that proved more effective and longer lasting.

2.3 Dielectric Growth by Anodization

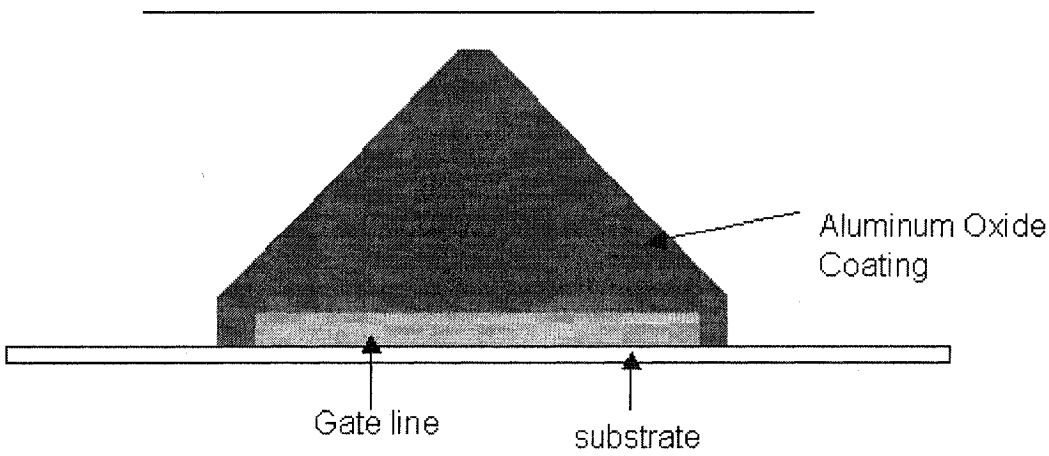


Figure 2.3 Schematic representation of the TFT after anodization (perspective)

After gate line formation, the substrates were anodized to produce the gate dielectric. As discussed in section 1.2.3 anodization results in the formation of a thick aluminum oxide layer on top of the gate lines by electrochemical oxidation.

The anodization procedure was adapted from earlier experiments[2]. The sample was connected to an electric circuit as the anode and a square platinum mesh was used as the counter electrode. Both electrodes were immersed in an electrolyte mixture of ethylene glycol and tartaric acid with a carefully controlled neutral pH.

Current and voltage were controlled manually during the experiment. Initially, the current was maintained at a constant 21mA and the voltage was

allowed to increase. The voltage was allowed to increase under constant current until to a value of 120V was reached. This stage of the anodization process determines the thickness of the dielectric layer. The sample was then held at constant voltage and current was allowed to decrease. Generally the anodization was considered complete when the current flowing between the electrodes fell to ~50μA. During the constant voltage stage of the anodization the aluminum oxide dielectric densifies.

After anodization the substrates must be annealed at high temperature to dehydrate the grown dielectric film and crystallize the amorphous material. After annealing, dielectric breakdown potentials were typically ~8MV/cm. Capaticance measurements revealed a dielectric constant of ~9 for the annealed anodized oxide. Leakage currents were on the order of 10^{-10} A.

2.4 SiO_2 Passivation of the Grown Dielectric

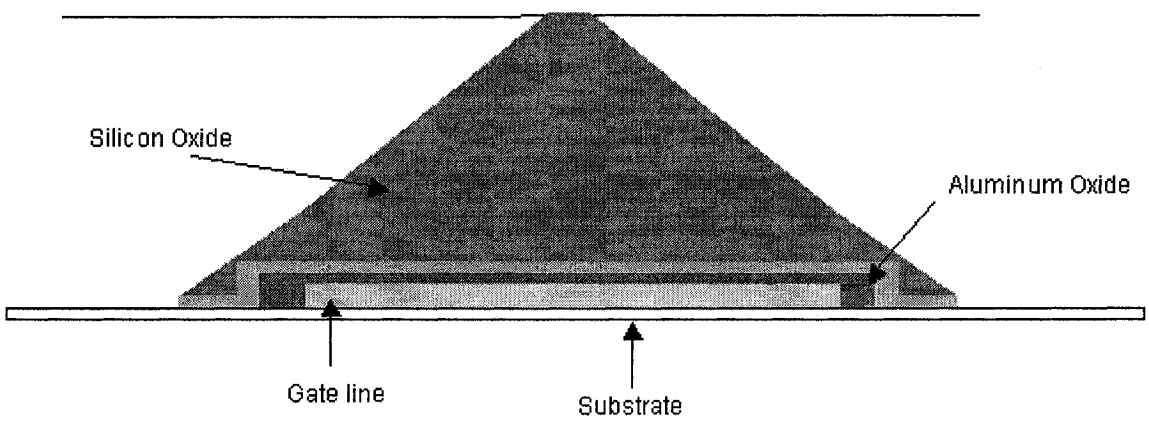


Figure 2.4 Schematic representation of the TFT after SiO_2 passivation (perscpective).

To protect the aluminum oxide dielectric from dissolution in the basic CBD reaction bath, the anodized gate lines were passivated with a layer of SiO_2. The deposition step was conducted using an Applied Materials Plasma II PECVD instrument.

Because the underlying gate structures and Arylite substrate were incompatible with standard wet etching techniques used for glass films, the substrate was patterned using a positive resist bilayer lift-off process prior to SiO_2 deposition.

The passivation layer was deposited using a mixture of silane and oxygen gasses at 50°C under nitrogen plasma. The deposition recipe was adapted from research conducted at Ecole Polytechnique under contract from Silk Displays.

The lift-off process was completed by immersion in acetone. The resultant passivation layer was adherent, dense and sharply defined. The thickness of the layer was 120nm as measured by profilometry.

2.5 Semiconductor Deposition by CBD

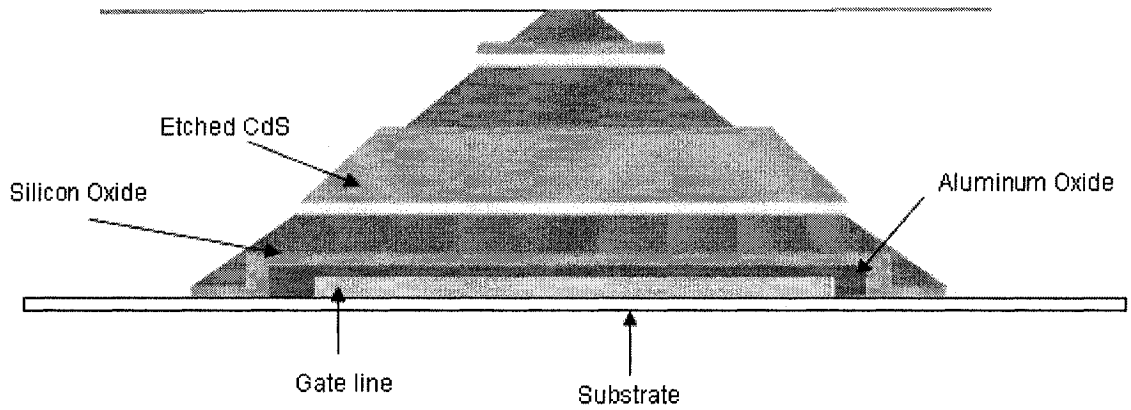


Figure 2.5 Schematic representation of the TFT after CBD deposition of CdS (perspective).

The chemical bath deposition of the CdS semicondutor layer was conducted using a procedure adapted from the work of Ghan and Shih[2]. Because most CBD experiments are conducted on small substrates such as glass slides, there has been no discussion of depositions over large areas in literature. Though an analysis of the CBD reaction would suggest that the process is infinitely scaleable, careful consideration of the experiment reveals this is not the case without careful adaptation

The formation of CdS films involves reactants in solution depositing on a surface or forming precipitate in solution. Thus the surface-to-volume ratio of the substrate relative to the deposition solution is very important to film quality, as CBD experiments on spacer separated glass slides suggest[3]. As the area of the substrate increases, the volume of the deposition solution increases dramatically.

This results in increased in-solution precipitation of CdS and films with greater particulate inclusions.

Two other problems become apparent upon attempting depositions with larger and larger substrates: temperature gradients within the deposition solution, and convection currents. The challenges unique to large area deposition required that we redesign our reaction vessels. One of several designs is depicted in figure 2.7.

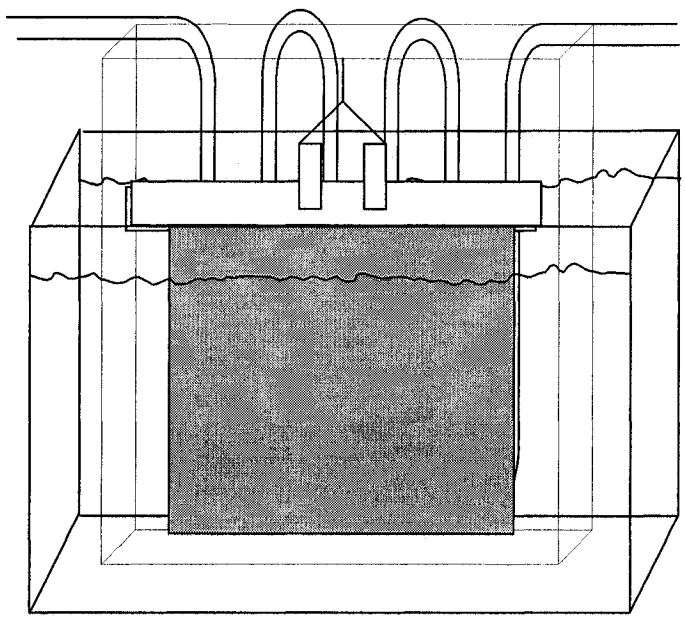


Figure 2.6 The vertical CBD apparatus with glass heating coils and circulating water pump.

The apparatus consisted of a large water bath with circulating pump, which was maintained at 70°C by a heater and circulating pump, a narrow rectangular deposition vessel, chosen to maximize the surface in contact with the

warm water bath, and a heating coil made of glass tubing in which 70°C water was circulated, the coil was suspended within the CBD solution.

The combination of a circulating large volume water bath and a heating coil successfully replicated the heating profile of the small area deposition apparatus used during process development. Unfortunately, the vertical deposition apparatus produces films with small, but unacceptable, quantities of solution phase grown precipitate particles adsorbed onto the the smooth film surface.

These adsorbed precipitates appear to be the result of convection currents within the CBD solution, which resulted from the natural circulation of the large volume of solution necessary to fill the vessel to the requisite level to submerge the substrate (750ml). In order to limit these deleterious convection currents within the solution, glass baffles were added to the apparatus. Glass baffles divide the reaction vessel into small separated areas and prevent the circulation of the CBD solution, it is the circulation of the solution which results in greater amounts of precipitate particles as previously observed in stirred small area deposition experiments. Deposition experiments with different configurations of glass baffles yeilded films with much lower non-adherent particle content.

After deposition, the CdS was variously left as a continuous layer or else etched everywhere but the channel region (as in figure 2.6). Etching was done in dilute HCl after masking the channel region by standard lithography.

2.6 Data Line Deposition

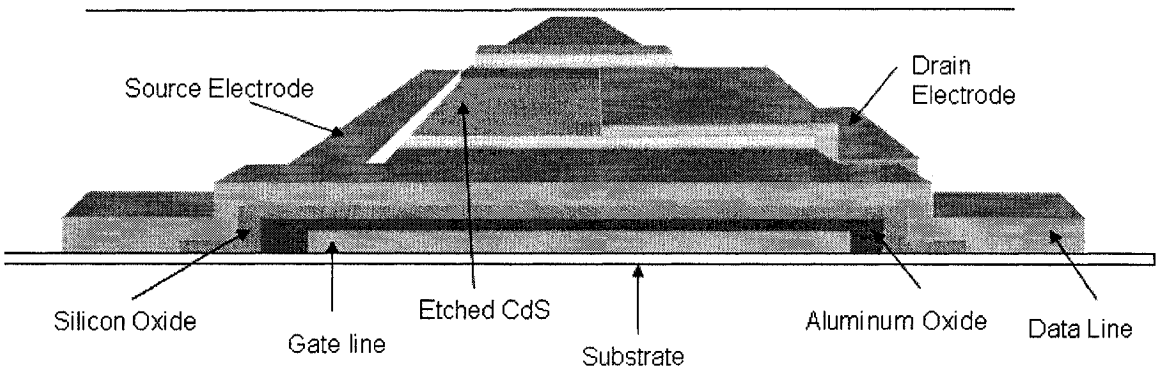


Figure 2.7 Schematic representation of the TFT after data line deposition (perspective).

The deposition of the data lines and source/drain contacts required a positive resist bilayer lift-off process, similar to the one employed for gate dielectric passivation.

After lift-off patterning, the subtrates were loaded into the sputtering instrument and the pressure in the deposition chamber was allowed to stabilize in the range of ~3 * 10^{-7} torr. Aluminum was then deposited under power and pressure conditions similar to those mentioned in section 2.2.

The lift-off process was completed by immersing the substrate in acetone. The resultant data lines were adherent, continuous and well defined. The thickness and conductivity of the deposited films were similar to those deposited in section 2.2

2.7 CdS Annealing

In order to increase the mobility, decrease the number of charge carriers and ensure good Ohmic contact of the data lines with the semiconductor layer, the substrate was annealed at elevated temperature. Previous investigators, using glass substrates, have achieved significant increases in semiconductor properties employing annealing temperatures of 400°C in an air[2]. Arylite substrates cannot sustain these temperature conditions without exceeding the T_g of the polymer; therefore, a lower annealing temperature was used (c.f. section 1.3).

2.8 Pixel Electrode Deposition

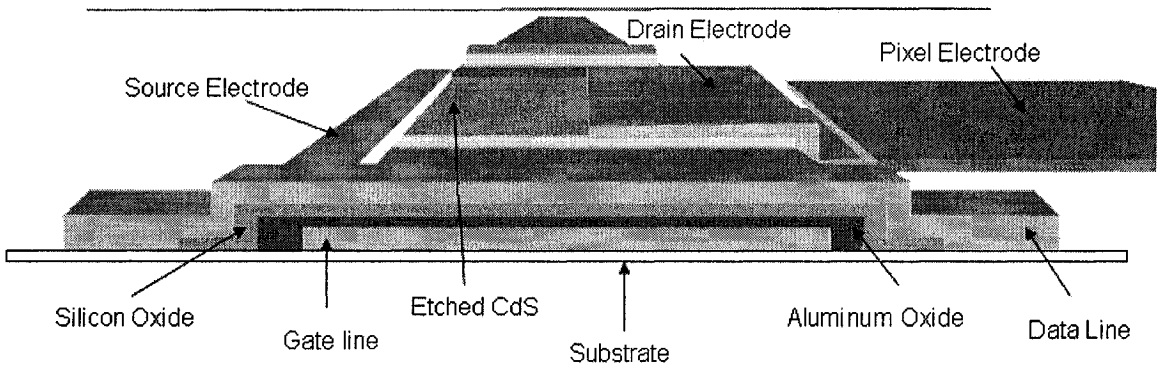


Figure 2.8 Schematic representation of the completed TFT (perspective).

Pixel electrode deposition also required the use of a positive resist bilayer lift-off patterning step. Initially, attempts were made to deposit sputtered ITO as

the transparent pixel conductor. ITO pixel deposition was complicated by the extremely narrow window of deposition conditions that give rise to conductive films of high transparency. As a result, the pixel electrode was fabricated from a 100nm thick layer of thermally evaporated gold. The layer was deposited with the equipment and expertise of Prof. Ishang Shih of the department of electrical engineering at McGill University.

After evaporation the extraneous lift off pattern was removed by immersing the substrate in acetone. The gold pixels were adherent, continuous and transparent. The thickness could not be determined directly but was inferred from previous testing and qualification of the thermal evaporation instrument performed in the electrical engineering department.

2.9 Transistor Testing

After the pixel deposition step the TFT array is complete. The transistors were characterized electrically on an HP4145A semiconductor parameter analyzer in collaboration with the electrical engineering department.

References

1. Angiolini, Simone, Avidano, Mauro, Barlocco, Carlo, Bracco Roberto, *Euro. Displays*, conference, (2002).

2. Ghan, F.Y., *Ph.D. Thesis,* (McGill University, Montreal, Canada, 2001).

3. Nair, P. K., Garcia, V. M., Gomez-Daza, O., Nair, M. T. S., *Semicond. Sci. Technol.*, **16,** 855–863, (2001).

Chapter 3. Results and Discussion

The TFT fabrication process resulted in functional arrays with greater than 50% transistor yield. Magnified images (figure 3.1) of the transistor-pixel unit cell show the following: the fabrication process does not significantly degrade the polymer substrate, and the mechanical stress generated in the TFT-substrate couple did not lead to catastrophic delaminations of the film layers. The current-voltage characteristics of the transistor units are presented in section 3.1. The challenges presented by the mechanical stresses that develop during processing are discussed in section 3.2. The chemistry of the CdS films and the relationship between process conditions and microcrystalline nanostructure is examined in section 3.3. Finally, the future possibilities of this research are investigated (section 3.4).

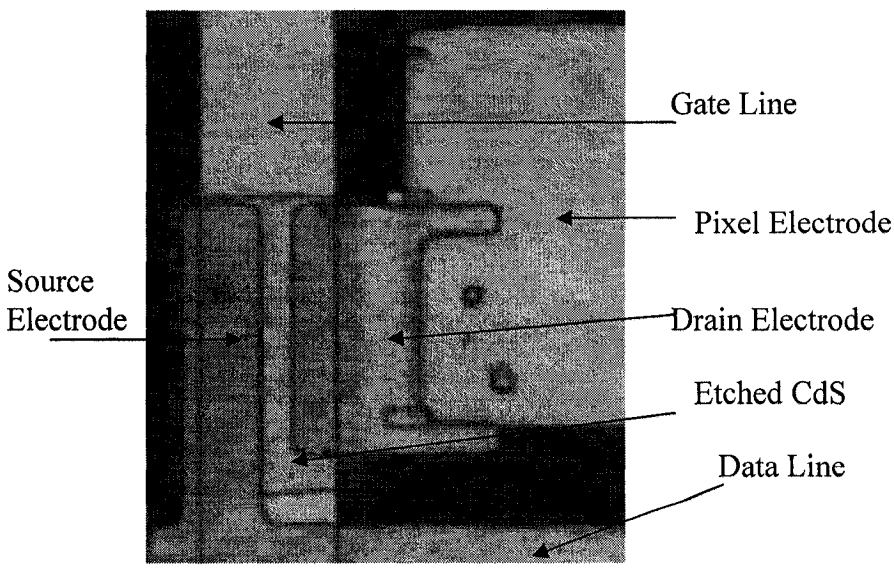


Figure 3.1 A microscope image of the transistor-pixel unit cell.

3.1 Measured Transistor Properties

The current between the drain and source was measured under different gate potentials. The resultant current-voltage profile of a representative transistor is presented in figure 3.2.

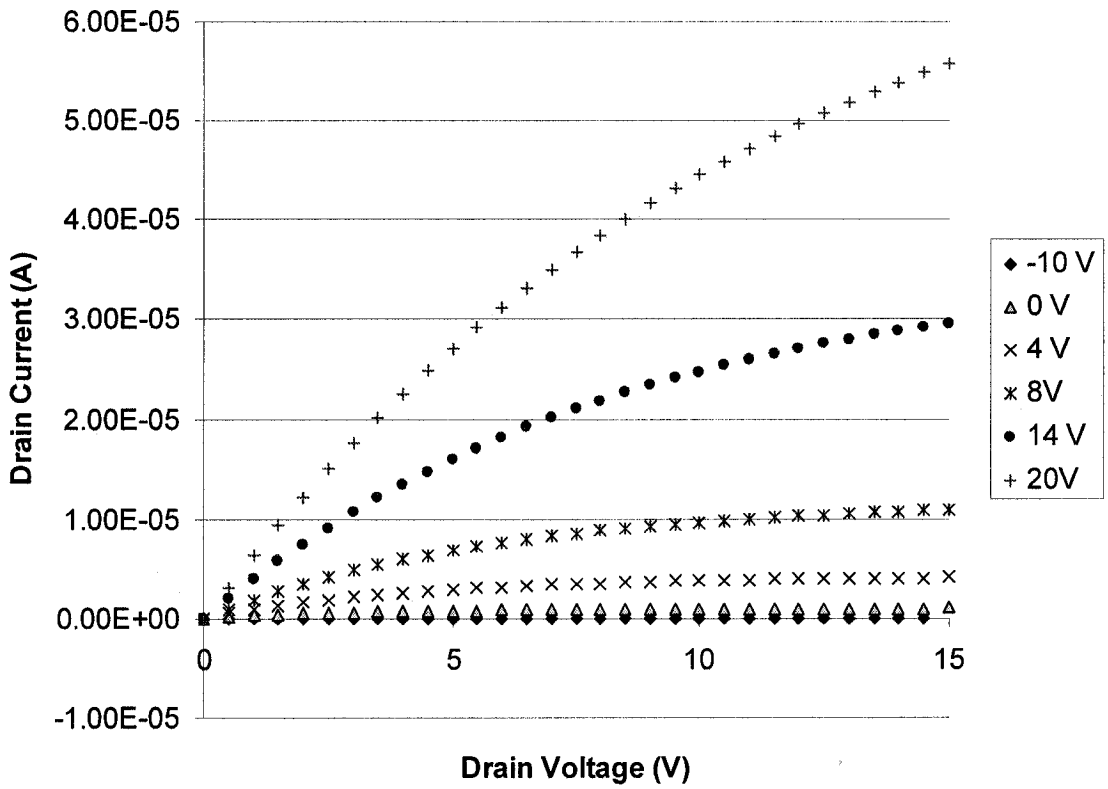


Figure 3.2 The I-V curve of a representative transistor at different gate line potentials.

By plotting the drain current, I_d, versus gate voltage, V_g, at constant data line potential, V_{ds}, the on off ratio of the transistors can be measured (figure 3.3). The on/off ratio is on the order of 10^5. Because the dielectric layer of the TFTs in

the fabricated arrays is thick relative to conventional transisitors, the current rise at the threshold voltage, V_{th}, is not sharp.

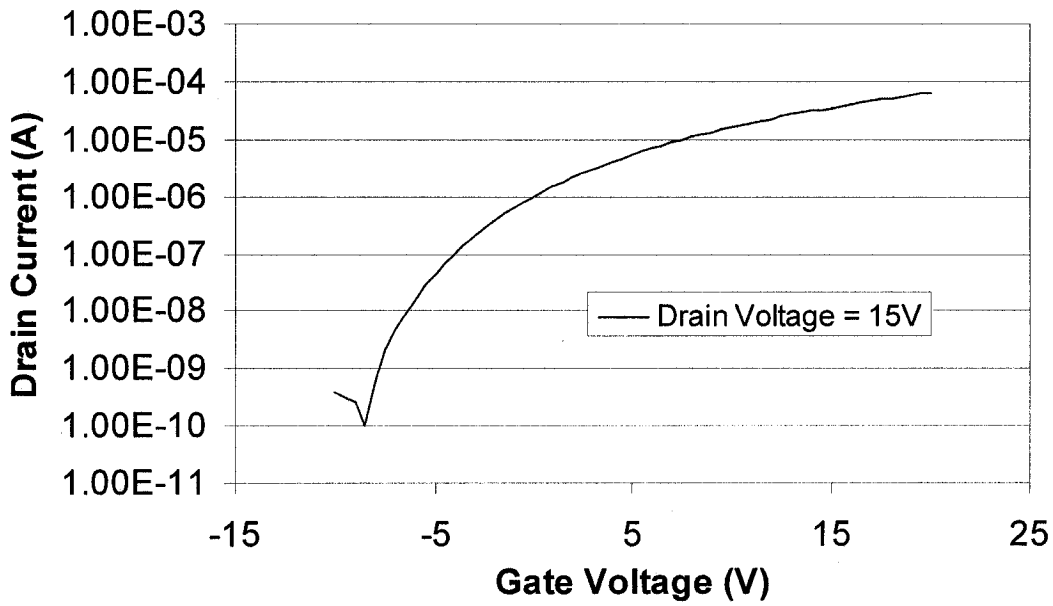


Figure 3.3 A plot of drain current vs gate voltage at constant drain voltage.

Other transistor properties can be calculated from the current modulation data. Using equation 3-1 we can calculate the mobility value of the semiconductor under conditions of current saturation, when $V_{ds} > (V_g - V_{th})$.

$$\mu_{eff} = \frac{2g_m{}^2 L}{WC_{ox}} \qquad 3\text{-}1$$

Where L is the channel length, distance between the source and drain electrodes, W is the width of the electrodes, C_{ox} is the capacitance of the

dielectric and, g_m is the transconductance, a measure of the electrical contact between the source and drain electrodes and the semiconductor.

The channel length and width, and the oxide capacitance values were measured with a probe station. The value of g_m, was obtained from a plot of $I_d^{1/2}$ vs V_g at constant V_d, when V_d is greater than the saturation voltage. The slope of the linear region of this plot is equal to the transconductance. By extrapolating the line to the intercept, the extrapolated threshold voltage can be determined (figure 3-4.

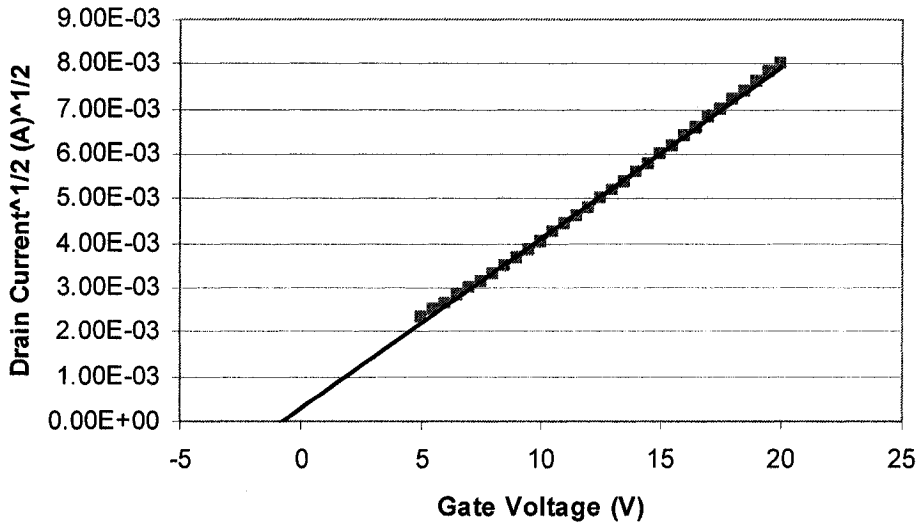


Figure 3.4 A plot of $I_d^{1/2}$ vs V_g, in the saturation region.

From the graph the mobility of the transistor was 0.34 cm^2/Vs and the threshold voltage was -0.75V. The negative threshold voltage is indicative of the presence of acceptor levels at the surface of the dielectric-semiconductor interface, which are known to depress the value of V_{th}[1]. Acceptor levels, or

surface traps result from lattice defects in the semiconductor and oxide in the region of the interface.

3.2 Mechanics of Compliant Substrates

The substrate-film couple fabricated in this experiment produces a compliant substrate laminate. The complex patterning of the film layers deposited on the Arylite surface make analysis of the stresses which are generated in the film and substrate during processing extremely difficult. The equations developed in section 1.4 cannot be applied to the TFT-substrate couple directly, but the insight they provide can be used as a guide to qualitative analysis of the stresses and strains that develop within the film and substrate during fabrication.

Table 3.1 presents the mechanical properties of the various materials which comprise the multi-layer film and the substrate. Unfortunately, the exact specifications of the acrylate-nanoparticulate SiO_2 hardcoat are unknown, though the T_g is reported to be below 180°C and similar materials are reported to have Young's moduli of ~6GPa[2].

An examination of table 3.1 reveals that the Young's moduli of the materials that make up the film layer are much larger than those of the substrate or the assumed value of the hardcoat. The coefficient of thermal expansion for the substrate is also very much larger than those of the constituents of the film layer. Thus the total mismatch strain experienced by the film upon heating will

be large (equation 1-9). Strain due to solvent absorption through immersion and moisture from the air are also large because the inorganic film materials are unaffected by solvent absorption, whereas the substrate is (section 1.3).

Material Property	**Arylite**	**SiO_2 by CVD**	**Al**	**Al_2O_3**	**Au**
Y	2.9 GPa	69 GPa	68 GPa	370 GPa	77.2GPa
Poisson Ratio	N/A	0.17	N/A	0.2	0.42
Tensile Strength	100 MPa	3.18 GPa	N/A	300MPa	120 MPa
CTE	55ppm /°C	< 1ppm/°C	24ppm/°C	7.4 ppm/°C	14.5 ppm/°C
Water Absorption	0.6-1.3% 80°C 2days	Low	Low	Low	Low

Table 3.2.1 Some material properties of the substrate and film layers.

The area of the substrate covered by each layer of film is also important to our interpretation of the stresses that develop in the process of device fabrication.

The area covered by the SiO_2 passivation layer is of particular interest (see figure 3.1). Because the passivation layer encapsulates the gate lines and acts as a rigid platform for the CdS and source and drain electrodes it may mitigate the stress experienced by the other film layers. This observation follows from the work of Bhattacharya[3], who found that stress in patterned films on polymer substrates was concentrated at the film edges. By using electron microscopy Bhattacharya was able to observe edge slipping of silicon nitride islands on polyimide substrates. The experiment suggested that since the slippage was confined to the edges of the material delaminations were

concentrated there and structures fabricated near the centre of the island suffered reduced stress induced defects.

Since the inorganic film layers of the fabricated TFT structures are not in direct contact with the Arylite polymer but instead rest on the surface of the hardcoat protective film, the properties of the hardcoat greatly affect the adhesion and stress experienced by the film layers at the substrate-film interface. Unfortunately, little is known about the composition of the proprietary hardcoat structure and composition, except that it is a composite of acrylate polymers and silica nano-particles with a T_g of less than 180°C. Investigations of similar systems reported in literature[4,5,6], suggest that the hardcoat is a core-shell latex composed of a silica core surrounded by an acrylate based shell.

As stated above, the reported young's moduli of hardcoat type materials (~6GPa) are larger than those of the Arylite substrate (2.9GPa). The larger elastic modulus of the hardcoat type materials causes them to suffer less deformation under stress than the bulk Arylite acting as a microscopic "expansion joint", improving the mechanical compatibility of the film-substrate couple.

Electron microscopy investigations of the morphology of core-shell silica nano-particulate polymer composites show the morphology of the surface of the film to be a rough "raspberry" aggregation of particles[7]. The microscopic morphology of the latex aggregates may improve the adhesion of the overlying film layers increasing effective area of the surface contact at the interface.

The structure hardcoat type material implies that surface roughening techniques may also be a particularly effective method for improving adhesion at

the substrate-film interface. If the roughening step ablates the polymer shell of surface latex particles sufficiently to expose the surface of the SiO_2 shell, then adhesion of inorganic over-layers will be stronger at those exposed surfaces. In this case the film layer would be anchored to the silica nano-particles which are implanted into the near surface region of the substrate itself.

The superior mechanical compatibility of hardcoated Arylite substrates with the TFT film layer over that of uncoated Arylite was observed when TFT fabrication was attempted on the bare substrate. Though the adhesion of the initial aluminum film layer was strong and the aluminum etching process was successful, the film layer completely delaminated after several minutes of anodization. This result was attributed to the progressive delamination of the gate line edges under the stress of the mechanical mismatch between the extremely rigid aluminum oxide film and the extensible Arylite substrate.

3.3 Chemical Bath Deposition of CdS

The deposition reaction was conducted in the ion-by-ion growth regime. Nevertheless, we observed that particles nucleated in solution for reasons discussed earlier. The CdS film, which was hard dense and specularly reflecting, was composed of film nucleated grains and small solution grown nanocrystals and crystal aggregates that were incorporated into the growing film.

Literature experiments report that CdS crystals incorporated from solution are of a much smaller size than on film grown grains, typically around 4nm[8].

Grains of on film nucleated CdS microcrystals can be as large as 140nm depending on the deposition conditions[9]. Films with incorporated solution grown grains have many more grain boundaries than films without. This can have a large influence on the transport properties of the CdS semiconductor. As the number of grain boundaries increases, the mobility of the charge carriers in the film decreases and the number of intrinsic charge carriers increases. These deleterious effects on the semiconducting properties of the film result from mismatch of the CdS lattice at the interface, the inclusion of microscopic voids, and non-stoichiometric film composition.

CBD deposited films are often non-stoichiometric by as much as 2%[10], the stoichiometric excess is determined by the relative concentrations of the free metal cations and chalcogenide anions. In this research the CBD conditions resulted in an excess Cd content in the CdS films. Presumably, much of the excess metal is located at the growing crystallite edges.

Annealing greatly improves the properties of the CdS by two mechanisms. Firstly, the high surface energies of the micro-crystalline grains allows adjacent particles to join into larger particles upon heating, reducing the number of grain boundaries in the film. Secondly, when the annealing is done under ambient atmosphere, oxygen in the air reacts with excess cadmium in the film to for CdO. The formation of CdO reduces the number of intrinsic charge carriers in the semiconductor[1].

The structure of the film at the dielectric interface also influences the properties of the transistor, since impurities and crystalline defects can result in

trapped charges and surface states at the interface. In the pH range of the deposition conditions utilized in this thesis, other researchers have observed an under layer of $Cd(OH)_2$ which remains un-reacted at the substrate interface[11] (ref). A lack of XPS data cannot confirm this result in these experiments, but cadmium hydroxide may be a source of trapped charges at the semiconductor-dielectric interface. Surface states resulting from the lattice mismatch between SiO_2 and CdS are also assumed to be present. Surface States and trapped charges act as scattering centres that lower the observed mobility of the transistor[1] (ghan). The experimentally determined values of the mobility (0.34 cm^2/Vs) and the negative threshold voltage (-0.75 V) indicate that there were many trapping states at the CdS-dielectric interface.

References

1 Ghan, F.Y., *Ph.D. Thesis,* (McGill University, Montreal, Canada, 2001).

2 Pu, Zhengcai, Mark, James E., *Chem. Mater.,* **9**, 2442-2447, (1997).

3 Sturm, J. C.; Hsu, P. I.; Gleskova, H.; Bhattacharya, R.; Wagner, S.. *International Journal of High Speed Electronics and Systems*, **16**, 365-374, (2006).

4 Qi, Dong-Ming, Bao, Yong-Zhong, Huang, Zhi-Ming, Weng, Zhi-Xue, *Journal of Applied Polymer Science*, **99**, 3425-3432, (2006).

5 Chen, Li, Chen, Su, Gu, Yuansong, *Polymer Preprints (American Chemical Society, Division of Polymer Chemistry)*, **46**, 806-807, (2005).

6 Oberdisse, Julian, *Macromolecules*, 35, 9441-9450, (2002).

7 Laruelle, G., Parvole, J., Francois, J., Billon, L., *Polymer*, **45,** 5013–5020, (2004).

8 T. P. Niesen, M. R. de Guire, *Journal of Electroceramics*, **6**, 169-207 (2001).

9 Rusu, M., Rumberg, A., Schuler, S., *Journal of Physics and Chemistry of Solids,* 64, 1849–1853, (2003).

10 Dona, J. M., Herrero, J., *J. Electrochem. Soc.*, **144**, 4081, (1997).

11 Rieke, P. C., Bentjen, S. B., *Chem. Mater.*, **5**, 43 (1993).

Chapter 4.0 Thesis Summary and Future Work

The two great challenges complicate the fabrication of inorganic TFT structures on the surface of flexible polymer substrates: developing deposition and patterning processes that do not degrade the substrate through overheating, and managing the mechanical incompatability of inorganic film layers with the underlying polymer.

The successful fabrication of a QVGA TFT array having >50% transistor yield and effective mobility values of up to 0.34 cm^2/Vs demonstrates that these challenges can be overcome, by the application of non-standard techniques such as anodization and chemical bath deposition, and by managing the mechanical stresses within the film-substrate couple.

The application of chemical principles to the study of microelectronic device fabrication is a promising avenue of investigation. The wide range of known chemistry applicable to the electronics industry is evident in the increasingly interdisciplinary nature of advanced semiconducting device manufacturing.

Future Work: Standard TFT fabrication processes and film deposition techniques have been studied and refined for decades. The practice of TFT manufacture on polymer substrates is in its infancy by comparison, and the possibilities for future research are vast. Future studies, which follow from the ideas presented in this manuscript, are presented below:

1. The CBD deposition process is a low temperature technique suitable for semiconductor film deposition on polymer substrates. Under the current conditions the mobilities of the CdS films are low. The observed dependence of film stoichiometry, grain size, and substrate-film interface properties on the concentration of CBD solution reactants suggests that films with much higher mobilities are possible. A comprehensive investigation of the CdS deposition reaction focusing on the role of the chalcogenide sources, cadmium complexants and substrate surface microstructure on the epitaxial growth of CBD depositied films is called for.
2. Improving the adhesion of deposited films on Arylite substrates would enhance the properties of the polymer film-substrate couple presented in this research and increase the array of accessible materials and micropatterned device designs. A comprehensive study of the surface modification of hardcoated Arylite by plasma roughening, employing the techniques of CASING and surface chemical restructuring could improve the properties of the substrate surface.
3. The material properties of Arylite are sufficient to achieve the present result, but the design of better compliant substrates would dramatically improve the performance of future flexible device fabrication. The surprising properties of the nano-particulate silica-acrylate composite hardcoat material suggest many exciting possibilities for research into

substrate design. Changing the materials used in the design of the core-shell latex particles is one example. If the silica particles were replaced with alumina particles, perhaps the young's modulus of the resultant composite would be improved because of alumina's greater rigidity. Using different polymer shell constituents could also be a valuable route of inquiry. If more thermally stable and rigid polymers were substituted for acrylate, the properties of the composite could improve dramatically. The polyaryl ester family of compounds could be a candidate shell polymer replacement.