IRON-GaAS SCHOTTKY CONTACT

FOR MESFET APPLICATIONS

Submitted by

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ABSTRACT

A novel technique for fabricating Schottky contacts on GaAs for device applications is presented. The technique consists of depositing iron by metalorganic chemical vapour deposition directly on similarly grown GaAs. In this project this metal-semiconductor contact is used in the making of diodes and field-effect transistors. Procedures for the processing of these iron-GaAs based devices, specially developed for the purpose as they are original and to the authors knowledge never previously attempted, are described. To demonstrate the usefulness of this contact, measurements and analysis including a study of Schottky barrier and interface properties has been performed. It has been found that iron-GaAs contacts can be used for good quality devices. Additionally, included in the project is the presentation of a low-cost custom-built MOCVD system which was used for iron deposition. A Hall effect system designed and built for the characterisation of the GaAs epilayers is also described.

SOMMAIRE

Une technique nouvelle, pour la réalisation de contacts Schottky sur l'AsGa, en vue d'application à des composants, est proposée. Il s'agit de déposer du fer par épitaxie métalorganique en phase vapeur sur une couche crystalline d'AsGa obtenue par la même technique. Dans ce projet, ce contact métal-semiconducteur est ultilisé pour la fabrication de diodes et de transistors à effet de champ. L'interface Fe/AsGa n'a jamais, à notre connaisance, été ni réalisée, ni étudiée. Les procédés développés pour la réalisation des composants correspondants sont donc originaux, et sont décrits dans ce travail. Pour montrer l'intérêt de cette interface, de mesures et des analyses incluant une étude des propriétés de la barrière de Schottky ont été realisées. Nous avons montré que l'interface Fe/AsGa peut être ultilisée pour la réalisation de composants de qualité. Nous présentons de plus un système MOVPE peu coûteux construit pour la déposition du fer, ainsi qu'un système d'acquisition de données construit pour les mesures d'effet Hall ayant servi à la caractérisation de l'AsGa.

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CHAPTER 1

INTRODUCTION

Currently, silicon is the dominant semiconductor used for device technology in industry. Until recently, this has been exclusive. Now, however, there is an increasing interest in other semiconductors offering superior performance characteristics. These are beginning to challenge the dominance of silicon. Among these newer materials are GaAs and InP, newly emerging II-VI compounds such as ZnSe, and some ternary compounds such as GaAlAs. Since silicon technology is very mature, these latter semiconductors are not successfully replacing silicon directly in most device application areas as the processing technology is not yet available. This reasoning applies most convincingly to VLSI (Very Large Scale Integration). Furthermore, the cost involved in switching over to different processes has made industry reluctant to do so. The newer materials are however, making inroads into areas where they have inherent physical advantages.

GaAs at present appears to be one of the strongest contenders. The higher mobility of GaAs and its direct band gap give it some undisputed advantages in operating speed and optical properties. The direct band gap of GaAs allows the fabrication of more efficient optoelectronic devices. The GaAs gap size is also advantageous as its optical output is

directly suited for optical waveguide use. Because of the higher mobility of GaAs, very high speed microwave field effect transistors, monolithic integrated circuits, and transit effect devices have been developed operating at frequencies above 100 GHz. Additionally, small and medium scale digital integrated circuits, offering ultra fast sub-nanosecond switching times are beginning to appear.

As mentioned before many of the techniques of GaAs device fabrication have not been perfected and are largely in the development stages. The fabrication of GaAs field effect transistors (FETs) remains an area under active development. One of the very important advantages of silicon is that its native surface oxide is a dielectric. The oxide permits the relatively easy and reliable fabrication of MOSFETs (Metal Oxide Semiconductor Field Effect Transistor). Unfortunately, GaAs does not form such an oxide and the MOS structure cannot be employed for field effect transistors. The problem of forming a good dielectric on GaAs is still being investigated using other materials. However, with all these problems a different approach to making GaAs FETs has been taken, notably the MESFET (MEtal Semiconductor Field Effect Transistor). Unlike the MOSFET, the MESFET's gate is a direct metal on semiconductor contact without any dielectric. The metal on semiconductor contact forms a rectifying Schottky diode.

The quest for the perfect contact material for Schottky junctions has yet to be accomplished. Metal-semiconductor

contacts using a wide variety of metals and semiconductors have been studied and their characteristics compiled[1]. Recently, there has been an increasing interest in refractory metals[2], silicides[3] and heterojunction[4,5] contacts for GaAs. In this report a novel technique for forming a metal-semiconductor contact is presented. The method involves the deposition of iron on GaAs by MOCVD (MetalOrganic Chemical Vapour Deposition). Although, the MOCVD of iron films have already been reported[6], the use of this method for placing iron on GaAs, especially for device applications, has not been attempted (to the author's knowledge). This deposition technique has an important technological advantage; the metal contact can be deposited immediately following the epitaxial growth of GaAs in the same reactor without having to break the vacuum. In this way a very high level of cleanliness can be ensured which is very critical in the formation of quality metal-semiconductor contacts. Additionally, due to the small lattice mismatch between GaAs and iron, a high quality interface might be expected.

A complete description of the original processes involved in the fabrication of an iron gate MESFET is described in this report. It will be demonstrated that this technique can indeed produce good quality Schottky diodes, which compares well with more conventional aluminium metallization procedures. Additionally, a custom built MOCVD system is presented, to which the author was a major contributor in both the design

and construction of the apparatus. This system includes a computer control unit which was fully developed and built by the author. A high performance Hall effect measurement system completely designed and built by the author is described. This work was already described in a previous publication[7] co-authored by other who helped in the conception of the experiment.

To summarise the thesis:

----- In chapter 2, an overview of metal-semiconductor junction theory is presented. This includes description of Schottky barrier formation and transport properties.

----- Chapter 3 describes the experimental apparatus and procedures used in the fabrication of the Schottky diodes and MESFETs. A complete presentation of the custom built MOCVD system is given, along with a summary of the growth conditions for both iron and GaAs. Furthermore, a Hall effect data acquisition system used for the characterization of GaAs is described.

----- Analysis of the results is presented in chapter 4, where the electrical properties of the iron-GaAs contact are shown. Additionally, data from the working MESFETs are given.

----- Concluding remarks that can be drawn from the experiments are presented in chapter 5.

CHAPTER 2

THEORY OF SCHOTTKY JUNCTIONS AND DEVICES.

2.1 Schottky Barrier Formation.

The formation of a barrier in a metal-semiconductor rectifying junction was first explained by Schottky on the basis of a highly idealized model. For greater practical usefulness Bardeen introduced an improvement which, further refined, led to the unified defect model. These are briefly described in the following sections.

2.1.1 The Original Schottky Theory.

The Schottky theory[8] of metal semiconductor contacts deals with a highly simplified case where there are no surface states present. This highly idealized model is quite erroneous when applied to practical device contacts. However, it does give an insight into the formation of Schottky barriers. In Fig. (2.1) we consider the energy band diagrams for a metal and a semiconductor. In this model a rectifying junction on n-type semiconductor is obtained if the work function of the metal, ϕ_m, is larger than that of the semiconductor, ϕ_s. The latter is directly related to the more meaningful electron affinity

quantity, X_s, as shown by

$$X_s = \phi_s - \xi \qquad (2.1)$$

where ξ is the energy difference between the Fermi level and the conduction band edge.

In Fig. (2.1)a the metal and semiconductor are separated by a large distance. If as in Fig. (2.1)b the materials are brought together, electrons flow from the semiconductor to the metal resulting in a build up of negative electric charge on the metal surface. This is due to the fact that when two materials of different work functions are placed in close proximity, the electrons from the lower work function will flow into the side of the higher, thus reducing free energy. As a result, the Fermi potentials of the two materials begin to align. By decreasing the separation further, there is an increasing negative charge build up on the metal surface due

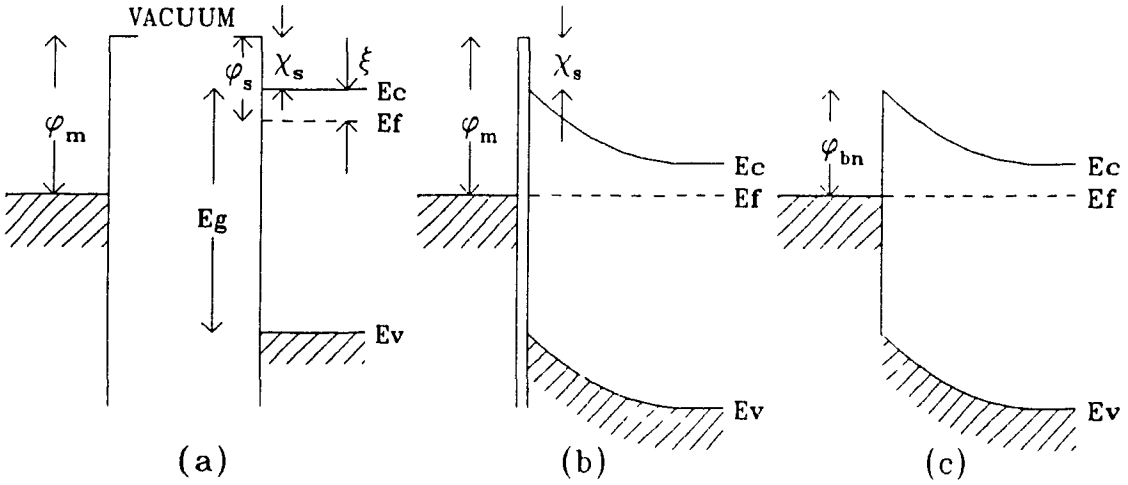

Fig. (2.1) The energy-band diagrams of a metal n-type semiconductor showing the formation of a Schottky barrier.

to conduction electrons. An equal and opposite charge thus develops in the semiconductor resulting from the depletion of mobile carriers. Fermi level alignment is complete when an electric potential difference, or contact potential, within the interface of the two materials is equal to the difference between the work functions, $q(\phi_m - \phi_s)$. In Fig. (2.1)c the separation is reduced to zero and the barrier is formed as shown. Hence, the barrier height, ϕ_b, is given by

$$\phi_b = \phi_m - X_s. \qquad (2.2)$$

The above is the basis of the well known Schottky barrier proposed by Schottky in 1938.

2.1.2 The Bardeen Approach[9].

As mentioned before, in practice the Schottky model fails, as the relationship between the barrier height and metal work function is not fulfilled. In fact, the barrier height appears to depend very little on the metal work function. Since at the surface of the semiconductor the crystal is discontinuous, a large density of surface states is present. These are allowed states with energies within the band gap of the semiconductor. If the density of states is sufficiently large, the charge transfer will be mainly to or from the surface states. This will result in the bulk of the semiconductor being effectively screened from the metal and,

hence, independent of the metal. Consequently ϕ_b has very small dependence on ϕ_m. In fact, there will be a charge transfer to the surface of the semiconductor, even without the metal present, resulting in band bending.

An important parameter is the position of the neutral level, ϕ_0, at the surface. This quantity represents the energy level to which the surface states must be filled in order to have charge neutrality satisfied at the surface. In a special case known as the Bardeen limit[8], ϕ_0 and the Fermi level in the semiconductor coincide. The resulting barrier height can then be easily found from the band diagram in Fig. (2.2), to be

$$\phi_b = E_g - \phi_0. \qquad (2.3)$$

This is the limiting case where the metal has no effect on the barrier. The Fermi level in this case is said to be pinned by the high density of surface states. In reality, however, the observed barrier height usually lies somewhere between the two extreme values given by Eqs. (2.2) and (2.3).

With an interfacial layer, which is the usual case with practical metal-semiconductor contacts, the barrier height has an additional dependence both on the thickness of the interfacial layer and the applied voltage. A detailed band diagram is shown in Fig. (2.2), including an interfacial layer of thickness δ. This layer is, however, assumed to be very thin and essentially transparent to electrons.

If we assume this system to have an acceptor density of surface states, D_s, the surface state charge density is then

given by

$$Q_{ss} = qD_s(\text{range of unfilled states below } \phi_0),$$

or quantitatively,

$$Q_{ss} = qD_s(\phi_b - E_g/q + \phi_0). \qquad (2.4)$$

From the band diagram it can be seen that the barrier height ϕ_b is given by

$$\phi_b = \phi_m - X_s - V_i. \qquad (2.5)$$

Where $V_i = E_i\delta$, is the potential drop across the interfacial layer. By applying Gauss's theorem across the layer, the electrical field, E_i, is determined, and hence, V_i becomes

$$V_i = \frac{\delta}{\epsilon_i}(Q_{ss} + \epsilon_s E_{max}). \qquad (2.6)$$

Where ϵ_s, ϵ_i and E_{max} are the semiconductor dielectric constant,

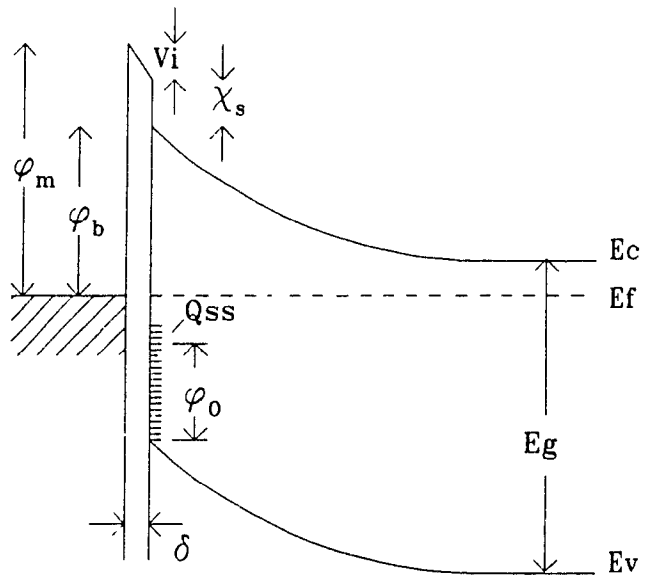

Fig. (2.2) Energy-band diagram of a metal n-type semiconductor contact with an interfacial layer of thickness δ.

interfacial layer dielectric constant, and the maximum electric field at the interface, respectively. By substituting Eq. (2.6) into Eq. (2.5), we obtain the following expression for the barrier height:

$$\phi_b = \beta(\phi_m - X_s) + (1 - \beta)(E_g - \phi_0) - \beta\delta\epsilon_s E_{max}/\epsilon_i \tag{2.7}$$

where

$$\beta = \epsilon_i/(\epsilon_i + q\delta D_s) \tag{2.8}$$

The flat band condition is obtained when the band bending is eliminated ($E_{max} = 0$) by an applied forward voltage. The flat band barrier height is then given by

$$\phi_{b0} = \beta(\phi_m - X_s) + (1 - \beta)(E_g - \phi_0). \tag{2.9}$$

And finally, a common form for ϕ_b

$$\phi_b = \phi_{bo} - \beta\delta\epsilon_s E_{max}/\epsilon_i. \tag{2.10}$$

2.1.3 The Unified Defect Model[10].

One of the most important experimental facts about metal-semiconductor contacts is that the barrier height varies very little with different metal work functions. Any model that attempts to describe accurately a barrier must take this fact into account. The Bardeen model fails in one important aspect; the model fails to give the source of the high density of surface states required to maintain metal independence. Recently, it has been found that the surface states are moved

out of the band gap region by electronic and lattice rearrangement at the surface, therefore reducing the density of states. The unified defect model (UDM) attempts to explain the Fermi level pinning effect by relating it not to surface states but rather to defect states. The defect states are assumed to be induced during the initial stages of the metal deposition. These native defects would be either anti-sites or vacancies, the energies of which control the pinned position of the Fermi level at the surface. As the pinning is a result of native defects it is independent of the contact material. Then using the same approach as taken for the Bardeen theory, the barrier height for the UDM theory is determined. The only difference is that the neutral level, ϕ_0, is now replaced by the pinning level, ϕ_1. Hence, without an interfacial layer the barrier height is given by

$$\phi_b = E_g - \phi_1. \qquad (2.11)$$

And, as before, the presence of an interfacial layer gives a barrier of the form

$$\phi_b = \phi_{b0} - \beta\delta\epsilon_s E_{max}/\epsilon_i. \qquad (2.12)$$

where ϕ_{b0} and β are given in Eqs. (2.9) and (2.8), respectively. In Eq. (2.8) ϕ_0 is, however, replaced by ϕ_1.

2.1.4 Effect of the Image Force on Barrier Height.[1]

It has been observed that the barrier height is voltage dependent. This dependence can be explained by the interfacial layer (as in Eqs. (2.10) and (2.12)) and by the effect of image forces. These image forces are the result of the electrostatic attraction of the electrons in the semiconductor to the surface of the metal. This attraction reduces the energy required to remove the electrons from the semiconductor, thus, in effect decreasing the barrier height (Fig. (2.3)). The reduction ϕ_b is calculated to be

$$\phi_b = \sqrt{qE_{max}/4\pi\epsilon_s} \qquad (2.13)$$

where E_{max} is the electric field at the interface resulting from the Schottky barrier. Furthermore, the position of the barrier peak, x_m, can be determined to be

$$x_m = \sqrt{q/16\pi\epsilon_s E_{max}}. \qquad (2.14)$$

The ranges of values that can be expected for ϕ_b and x_m are typically 0.01 to 0.1 V and 1 to 20 Å, respectively.

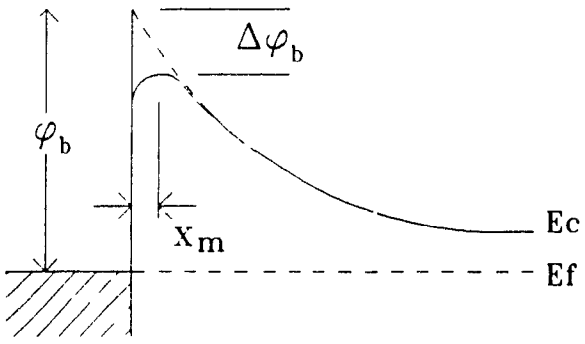

Fig. (2.3) The barrier lowering due to the image force of an metal n-type semiconductor contact.

2.2 Current Transport in Schottky Junctions.

In a Schottky junction there are four possible transport processes that occur under normal forward bias operation. For a metal n-type semiconductor these are shown schematically in Fig. (2.4) and are summarized below:

1) Emission of electrons over the barrier.
2) Quantum mechanical tunnelling through the barrier.
3) Recombination in the space charge region .
4) Recombination in the neutral region (hole injection).

Emission of the electrons over the barrier is by far the dominant process for moderately doped semiconductors at room temperatures. Currently there are two approaches of treating this case; the first is the thermionic emission theory and the second is the diffusion theory[8]. In the thermionic emission theory the current depends only on the barrier height, whereas in the diffusion theory the current depends on the flow of electrons

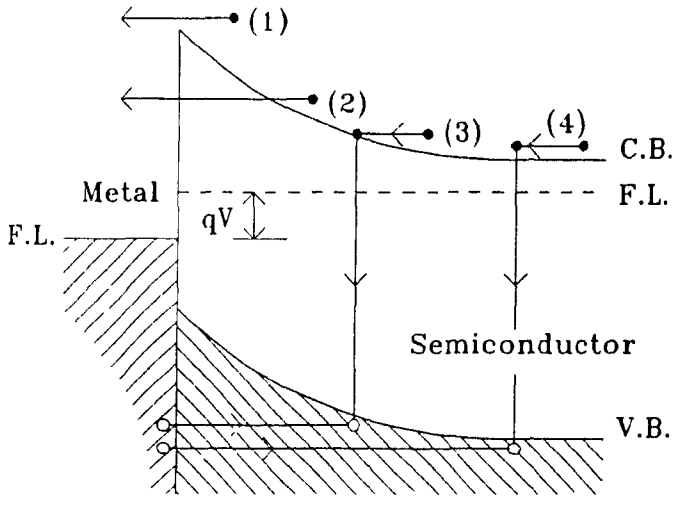

Fig. (2.4) The basic transport processes in a Schottky contact on n-type semiconductor in forward bias.

through the depletion region to the barrier. However, it has been demonstrated both theoretically and experimentally that thermionic emission is by far the most common transport process. For diffusion theory to apply, the mean free path of the carriers must be less than the depletion width, resulting in a continuously varying quasi-Fermi level. This condition is, however, rarely encountered in high mobility semiconductors such as Si, GaAs, etc.

In thermionic emission theory the current-voltage relationship was first proposed by Bethe[11]. The current density $J_{s->m}$ from the semiconductor to the metal is determined by calculating the number of electrons that have sufficient energy to overcome the barrier in the x direction (direction normal to the barrier plane). This can be represented by:

$$J_{s->m} = \int_{EF + q\phi b}^{\infty} qv_x \, dn \qquad (2.15)$$

where $E_F + q\phi_b$ is the energy required for the electrons to overcome the barrier, v_x is the carrier velocity in the x-direction and dn is the electron concentration within an incremental energy dE. The solving of this integral, as has been done in many texts[1], yields the following current-voltage expression:

$$J_{s->m} = A^*T^2\exp(-q\phi_b/kT)\exp(qV/kT) \qquad (2.16)$$

where A* is the effective Richardson constant for thermionic emission, T is the temperature of the lattice, and V is the applied bias voltage. Upon application of a reverse bias, the

electrons flow from the metal to the semiconductor and see a barrier of constant height. Consequently, the reverse current is constant for any reverse bias and is equal to the forward current density at zero bias (V = 0), and is given by

$$J_{m->s} = A^*T^2\exp(-q\phi_b/kT). \qquad (2.17)$$

By adding Eqs. (2.16) and (2.17) we obtain the total current density:

$$J = A^*T^2\exp(-q\phi_b/kT)\left[\exp(qV/kT) - 1\right] \qquad (2.18)$$

$$= J_0\left[\exp(qV/kT) - 1\right] \qquad (2.19)$$

where J_0 is the saturation current given by

$$J_0 = A^*T^2\exp(-q\phi_b/kT). \qquad (2.20)$$

When the doping level in the semiconductor is heavy or when the electric field is very high, tunnelling through the barrier becomes increasingly important. Tunnelling is the process (2) in Fig. (2.4). As, at lower temperatures, the contribution of thermionic emission decreases rapidly, tunnelling begins to dominate. The magnitude of the tunnelling current has been studied extensively by Padovani and Stratton[12]. They obtained the following general expression obtained to predict the current density:

$$J = J_T\exp(V/E') \qquad (2.21)$$

where E' is either E_{oo} or E_o depending on whether we have pure tunnelling (field emission) or tunnelling through a thinner part of the barrier at a higher energy by thermally excited electrons (thermionic field emission). J_T is a complex

function of T, E_{oo}, , ϕb and V. E_{oo} is given by

$$E_{oo} = h/4\pi(N_d/m^*\epsilon_s) \qquad (2.22)$$

where N_d is the donor density, m^* is the electron effective mass and ϵs is the semiconductor dielectric constant. E_o is given by

$$E_o = E_{oo}\coth(qE_{oo}/kT) \qquad (2.23)$$

By substituting Eqs. (2.22) or (2.23) into Eq. (2.21), it can be seen that pure field emission is predominant at lower temperatures. While, on the other hand, thermionic field emission becomes more significant at higher temperatures. When determining the importance of the tunnelling contribution to the total junction current the quantity E_{oo}/kT is considered. If $E_{oo} << kT/q$ then all tunnelling mechanism can be neglected.

The process (3) shown in the diagram (Fig. (2.4)), involves the recombination of carriers in the depletion region. From the Schockley, Read, Hall (SHR) expression for the recombination rate via localized states, maximum recombination occurs when the Fermi level in the depletion region of the semiconductor coincides with its intrinsic Fermi level[13]. The recombination rate is then given by

$$U_{max} = (n_i/2\tau_r)\exp(qV/2kT) \qquad (2.24)$$

where n_i is the intrinsic concentration and τ_r is the carrier lifetime in the depletion layer. If the depletion layer has a width d, the current density due to recombination is

$$J_r = qU_{max}d. \qquad (2.25)$$

Substituting Eq. (2.24) into Eq. (2.25) we obtain the complete

expression

$$J_r = (qn_i d/2\tau_r)\exp(qV/2kT). \qquad (2.26)$$

Recombination in the presence of dominating thermionic emission is most noticeable under any number of the following conditions; the carrier lifetime is very small, the barrier height is large, the temperature is low, the bias voltage is small, or d is large (i.e. N_d is small).

Recombination in the neutral region, or hole injection, is the fourth transport mechanism (see Fig. (2.4)). This process, which is dominant in pn junctions, is usually insignificant in Schottky contacts, typically less than 0.1% of the total current.

For a Schottky diode, to express the junction current in a general form we have the ideal diode equation[1]

$$J = J0(\exp(qV/\eta kT) - 1), \qquad (2.27)$$

where η is the ideality factor which is always greater than one, and J_0 is the saturation current. These two quantities are often used to characterize quality of the junction. The quality of the practical junction can be estimated by measuring its η value and comparing it to the theoretical value for the particular transport mechanism being considered. For thermionic emission, as it can be seen in Eq. (2.19), η should be 1. The greater the deviation from this value the poorer the junction. This deviation sometimes results from the presence of other transport processes present in the diode, such as recombination in the depletion layer and quantum

mechanical tunnelling through the barrier.

Recombination in the depletion region as seen in Eq. (2.26) gives ideally an η value of 2. Tunnelling, on the other hand, has a more complicated expression for η given by

$$\eta = qE'/kT \qquad (2.28)$$

where E' has been defined earlier.

The above summary of the theory forms the basis for the interpretation of the experimental results which will be presented in chapter 4.

CHAPTER 3

THE EXPERIMENTS AND THEIR RELATED APPARATUS

3.1. Metalorganic Chemical Vapour Deposition.

For the fabrication of the GaAs epilayers and the iron-GaAs Schottky contacts used in this work, the method of metalorganic chemical vapour deposition (MOCVD) was used. MOCVD is an epitaxial growth technique which was successfully demonstrated by Manaseveti in 1969[14].

MOCVD has many advantages over other epitaxial processes as it is simple, relatively easy to control and can be used for depositing a very wide range of materials.

In the following, we present the apparatus and deposition procedure both for GaAs and iron.

3.1.1. The MOCVD System.

In Fig. (3.1) a schematic diagram of a MOCVD system which we have designed and constructed is presented. One of the main features of the system is that it uses a small geometry reactor. The reactor consists of a vertically mounted quartz bell jar sitting on a stainless-steel base plate and sealed with an O-ring. The bell jar has a base diameter of about 5

cm and a height of approximately 20 cm. The small volume of this reactor allows for rapid exchanges of gases within. This is advantageous as a variety of newer MOCVD methods which require rapid gas changes can be used, such as atomic layer epitaxy[15,16] (ALE) and pulsed growth.

Located inside the bell jar, is a pedestal which holds and heats the wafer or substrate during deposition. This pedestal, which is made of graphite, has been shaped to accommodate standard 1 inch (2.5 cm) wafers. Furthermore, it has been designed so that the heating element can be inserted into its center. This heater consists of a small but powerful 650 watt quartz halogen projection lamp which can heat the

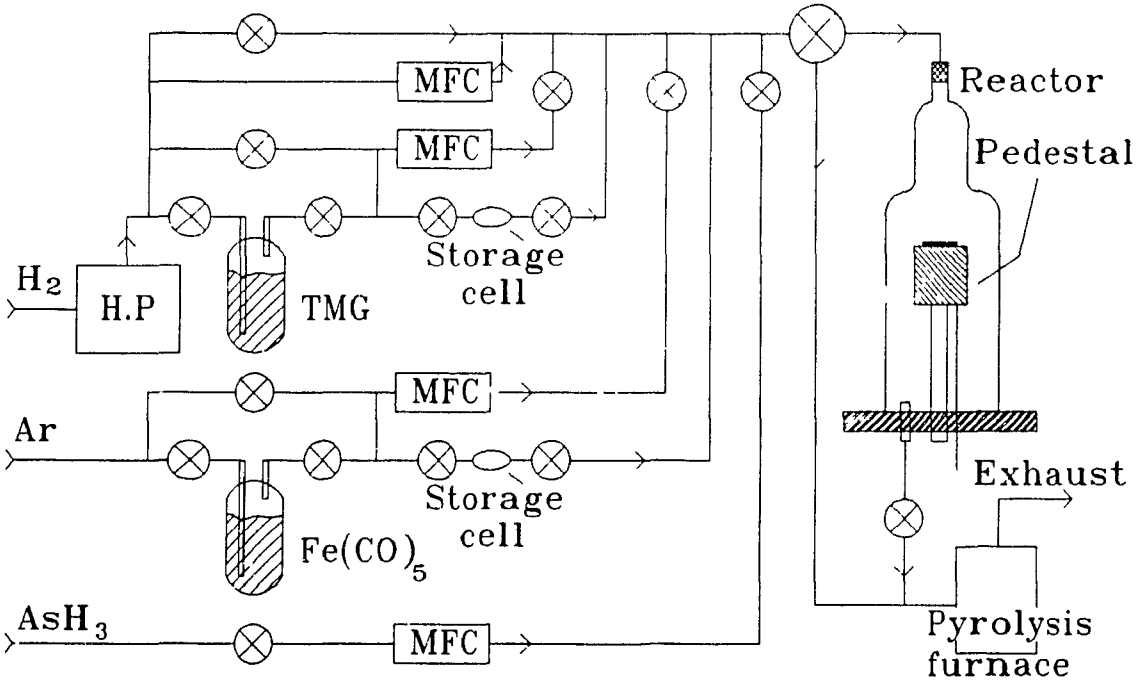

Fig. (3.1). The MOCVD system. (note: MFC - Mass flow controler, H.P - Hydrogen purifier)

pedestal up to a temperature of 950°C. Due to the small dimensions of the pedestal and the high power of the lamp, rapid heating and cooling are possible, reducing run time. The maximum temperature of 950°C can be reached within minutes. In order to obtain an accurate temperature reading of the pedestal a K-type thermocouple has been inserted into the base of the graphite.

The various gas species are injected through an opening at the top of the reactor bell jar. This helps to force the gases to spread uniformly over the surface of the wafer, resulting in improved uniformity of the epilayer.

The system has been designed so that two different metalorganics can be introduced simultaneously. The diagram shows trimethelgallium (TMG) and iron carbonyl ($Fe(CO)_5$) bubblers connected to the system. The flow rates of the metalorganics and the other gases are controlled by mass flow controllers. The flow controllers for the metalorganics and the arsine (99.999% pure) adjust the flow rate between 0 and 10 cc/min. The flow for the hydrogen can be varied between 0 and 1000 cc/min. Additionally, when growing by ALE or using a pulsed technique, the flow controllers can be bypassed and the storage cells shown in Fig. (3.1), can be used. These cells allow the user to inject a fixed amount (1 cc) into the reactor if the cell input and output valves are opened alternatingly. If the valves are opened simultaneously, the amount of metalorganic injected into the bell jar is

proportional to the duration of the open cycle of the valves.

The evacuation of the gases from the MOCVD system and the maintaining of a vacuum inside the bell jar is achieved through the use of a rotary pump. At the pump input there is a pyrolysis furnace which is used to breakdown any remnants of dangerous gases before evacuation. The pressure inside the bell jar maintained during deposition was generally about 2 torr. It is thus low pressure MOCVD.

3.1.2 The Control Unit.

The MOCVD system has been automated for simplified accurate and reproducible operation. This automation involves, among other things, the automatic control of valves, mass flow controllers and reactor temperature. A block diagram of the computer control unit is presented in Fig. (3.2). The unit is divided into two distinct sections; the main computer and the interface. In the interface section are all the circuits that actually operate the valves, mass flow controllers, etc. The circuit boards for this section are located in a separate card cage. Furthermore, the interface is built around its own custom designed bus. The main computer controls the interface linked by the interface controller.

The main computer is a standard configuration IBM PC compatible motherboard equipped with a 128K RAM. Furthermore,

one floppy disk drive has been included to store required program information and data.

Occupying one of the IBM PC slots is the MOCVD interface adaptor/controller. This controller provides the necessary buffering of the data and address busses. This card also includes the necessary address decoding, timing, and interface reset circuitry. A real-time clock circuit is also provided to interrupt the main computer at regular intervals of one second and serves to synchronize all control operations.

Video output is provided by a custom built video adaptor which is connected to the interface controller. The video

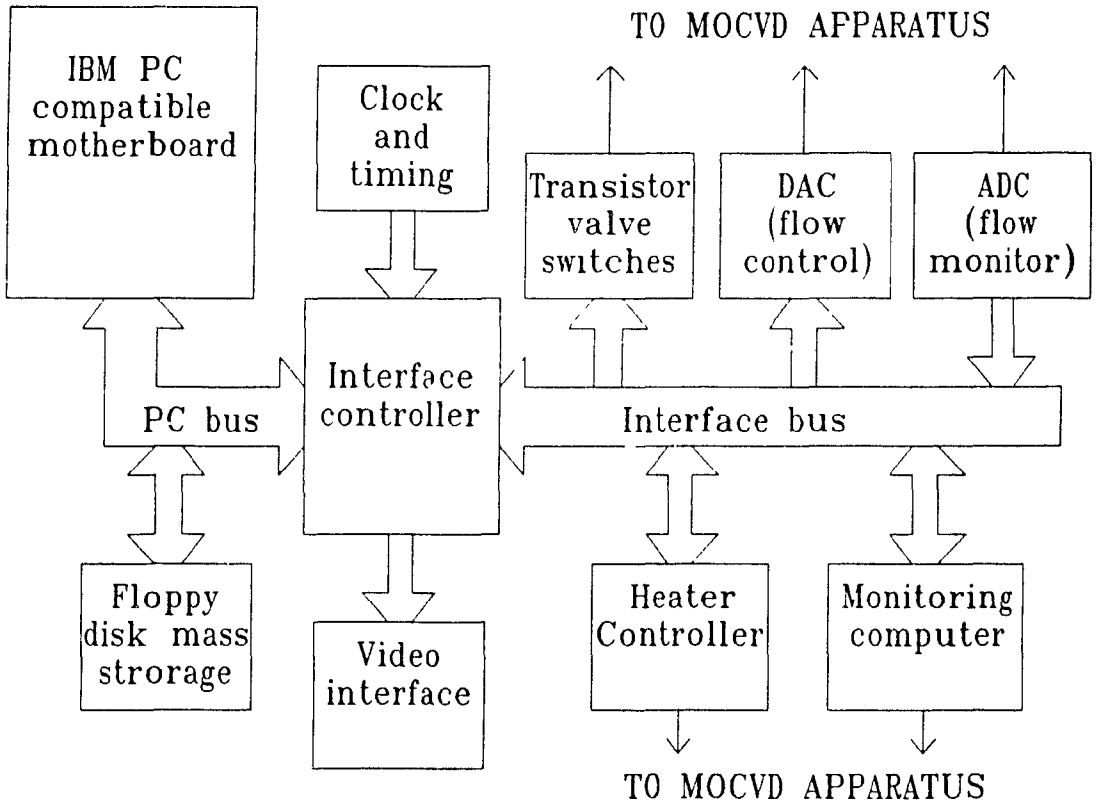

Fig. (3.2). A block diagram of the MOCVD system control unit.

circuit, based on the SNC2794[a] series integrated circuits, features the ability to have multiple pages of real-time status information which can be flipped through quickly with minimum CPU intervention. Additionally, it includes the hardware for flexible split screen operations.

As previously mentioned the interface has its own bus. This bus provides 8 bits of data, 10 bits of address, two wired 'or' interrupt lines, a reset line, and ten decoded enable lines; one for each interface card.

Among the cards built specifically for this system are a solid state valve driver board. This board was designed to switch up to 48 valves operating with a 24 volt supply. The drivers are MJE172[b] transistors that can switch a few hundred milliamperes to each valve without heatsinking, more than enough for the reliable switching of the valves.

A digital to analog board provides 9 analog voltages that are used to set the mass flow controllers. It uses DAC-08[c] 8-bit DAC's (digital to analog converter) coupled to op-amp buffers to give an output voltage of 0 to 5 volts. An 8-channel analog to digital converter board based on the ADC0808[d] 8-bit ADC (analog to digital converter) is used to

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[a]Signetics Inc., Sunnyvale, CA.

[b]Texas Instruments Inc., TX.

[c]Motorola Inc., AZ.

[d]Texas Instruments Inc., Dallas, TX.

monitor the flow rate signal of the mass flow controllers. The temperature controller board is used to control the pedestal heater. It works by reading the temperature with a thermocouple and then comparing it to the set point temperature. An output voltage signal, generated by a DAC-08 DAC, is then calculated using a proportional-differential-integral (PDI) algorithm. The temperature voltage is read by a 12-bit 8705CJ[a] ADC. The calculations are performed by an on board computer based on the 8052BA[b] microcomputer chip. This microcomputer has a built-in BASIC language interpreter. The PDI program is downloaded into the computer from the main computer upon power up. The programming task is greatly simplified as this BASIC includes floating point calculation capabilities. Since the output voltage is a low level signal that cannot directly power the heater, a triac based driver unit is used. This unit, which can control a 1 KW heater, synchronizes itself to the A.C. line, and is fired with a time delay from the zero crossing inversely proportional to the voltage from the controller. The larger the signal the larger the conduction angle and the power.

The monitoring computer is another 8052BA based unit which is used for monitoring the safety aspects of the system. This includes checking the bell jar pressure and cooling

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[a]Teledyne Semiconductor Inc.

[b]Intel Inc., Santa Clara, CA.

water, etc. The board is equipped with eight digital and analog inputs. If the board detects a faulty condition it interrupts the main computer which will then go through a shutdown procedure therefore reducing the risk of a dangerous situation.

The systems software has been written in C and assembly language. Assembly language was used to write some of the interface driver routines as well as all the hardware interrupt routines. On the other hand, C was used for the user interface and process control programs. The software is designed to provide manual control, using on screen menus, and automatic control through the use of sequence programs. By flipping through the video pages all system parameters can be monitored. A specially designed sequence programming language was also developed for easy use of the system's functions (see appendix A). The language is built on 14 instruction keywords. The keywords have been divided up into three groups:

1) Control; there are commands to turn on and off valves, set flow controllers, set temperature and give time delays.

2) Loop control; there are instructions to form loops so that repetitive operations can be performed.

3) Interrupt and exception handling; there are instructions that provide break control, and manual program interruption through the keyboard. This feature can be used

to stop the program while forcing it to follow a required closing sequence.

3.1.3 The MOCVD of GaAs.

The MOCVD of GaAs on semiinsulating GaAs substrate is based on the following chemical reaction involving a metalorganic of gallium , trimethylgallium (TMG), $Ga(CH_3)_3$, and arsine (AsH_3).

$$(CH_3)_3Ga + AsH_3 \Longleftrightarrow GaAs + 3CH_4$$

During growth the reacting species are deposited on the substrate surface through a carrier gas, namely hydrogen. The substrate is heated to a temperature of approximately 650°C. Once the temperature has been reached, and before the TMG and arsine are added, the sample is etched for a few minutes in pure H_2 to remove any native oxide. The typical TMG flow rate used is 5 cc/min. In order to obtain good control of the TMG, the bubbler is cooled, in a thermoelectric cooler, to -10°C. The arsine is also set at a flow of 5 cc/min. The carrier gas is typically set at about 1 ℓ/min. Using the above values a growth rate of about 3 μm/hour is obtained.

The purity of the epilayer depends very much on the quality of the chemicals, as well as the cleanliness of the system. Impurities in the GaAs epilayer give rise to a high background doping levels. This autodoping, unfortunately,

reduces the control and reproducibility of the epilayer. The GaAs substrate preparation is very critical as it affects dramatically the epilayer surface morphology. Considerable attention must be made to this step if good morphology is to be achieved. The first step of preparation involves a standard cleaning and degreasing procedure (see appendix B). Secondly, the wafers are polish etched in a solution of 3 H_2SO_4: 1 H_2O_2: 1 H_2O for about one minute. This etchant solution, as with most containing H_2O_2, tend to form bubbles on the surface of the sample. These bubbles can lead to non uniform etching and hence, introduce morphological defects on the sample. It was found that if the GaAs wafer is first soaked in pure H_2SO_4, wetting of the etchant solution is improved, and fewer bubbles are produced. After polishing, the samples are washed in deionized water and propanol. The cleaned samples are then immediately placed in the reactor to minimize contamination.

3.1.4. MOCVD of Iron on GaAs.

The MOCVD of iron on GaAs arises through the following pyrolytic reaction:

$$Fe(CO)_5 \Longleftrightarrow Fe + 5(CO)$$

where $Fe(CO)_5$ is a metalorganic of iron, namely iron carbonyl.

We found that iron could be deposited on GaAs in a large range of temperatures. By heating the substrate to between 100°C and 600°C, deposition was observed. One of the main problems with growing iron from $Fe(CO)_5$ is carbon contamination. Most of the work that went into developing the process, involved finding the growth conditions that minimized this contamination. Using a constant 5 cc/min flow of $Fe(CO)_5$ the manner that the iron grows varies significantly with temperature.

At higher temperatures (500-600°C), better surface morphology was obtained. However, the deposition rate tends to be slower and carbon contamination is more frequently observed. More rapid growth at elevated temperatures was achieved by using the pulsed technique. In the usual continuous flow method, the reaction appeared to occur above the wafer surface and most of the iron either deposited on the bell jar walls or was evacuated. By pulsing, a jet of chemicals is formed which reaches the surface and hence improves the deposition rate. Some success was obtained when growing iron at 500°C however, it was somewhat unpredictable

as occasionally it became somewhat contaminated with carbon. Unfortunately, this contamination makes further processing next to impossible as chemical etching of the iron is very difficult.

At about 300°C there appeared to be a transition in the growth mechanism of iron because at this temperature, the iron became very heavily contaminated with carbon and would occasionally go black. Generally, a yellow metal with severe morphological defects would appear. The growth rate did however increase significantly.

Below 300°C we obtained a better quality iron films. Unfortunately, the iron would not always deposit. The reaction appeared to be very catalytic in nature. Deposition generally happened in a very haphazard manner often emerging from a small area on the surface, perhaps a defect, and then spreading. However, occasionally this spreading was not observed at all. If and when growth starts however, it is very rapid. In fact, usually a minute or two of growth was sufficient. If left any longer, the layers became so thick that heavy flakes began to peel off from the strain.

As with growing GaAs, substrate surface preparation is critical. This applies especially to low temperature iron growth. First, a degreasing step is performed by washing the wafers in boiling trichloroethylene, boiling acetone and then deionized water. A final rinse in propanol also seemed to help in giving a spotless surface. Once the sample is loaded in the

reactor it is heated up to 600°C and flushed with hydrogen to clean up the surface. This step is carried out for 2 minutes to remove any native oxide that might be present. After this step is completed the system is set to the desired temperature for iron deposition When growing iron on GaAs epilayers any wet etching, commonly used to prepare the surface, is avoided as it could be damaging.

3.2 Schottky Device Fabrication.

3.2.1 Fe-GaAs Schottky Diodes.

The fabrication procedure begins with an n-type GaAs epilayer grown by MOCVD on which a film of iron is deposited by the same method. The GaAs epilayer is grown on a semiinsulating GaAs substrate, hence the diodes fabricated were of the planar type.

A diagram showing the steps involved in the fabrication procedure is given in Fig. (3.3). In Fig. (3.3)a, a GaAs sample with an iron layer on top is shown prior to any processing. At this stage, a full cleaning procedure is conducted (see appendix C). In Fig. (3.3)b, the iron in the area around the region where the Schottky contact is to be situated, is removed. This is achieved through the use of selective wet chemical etching. Selectivity is obtained by photolithography (see appendix B.2), which consists of placing photoresist on the wafer surface and then exposing it to suitable light through a photomask. The exposed photoresist is then removed by developing and windows opened for etching the iron. Many wet etchants dissolve iron. However, most etchants, including hydrogenchloride and hydrofluoric acid, severely undercut the photoresist. An etchant that proved reasonably successful is a sulphuric acid based solution (3 H_2SO_4: 1 H_2O_2: 1 H_2O). This etchant removes iron very quickly,

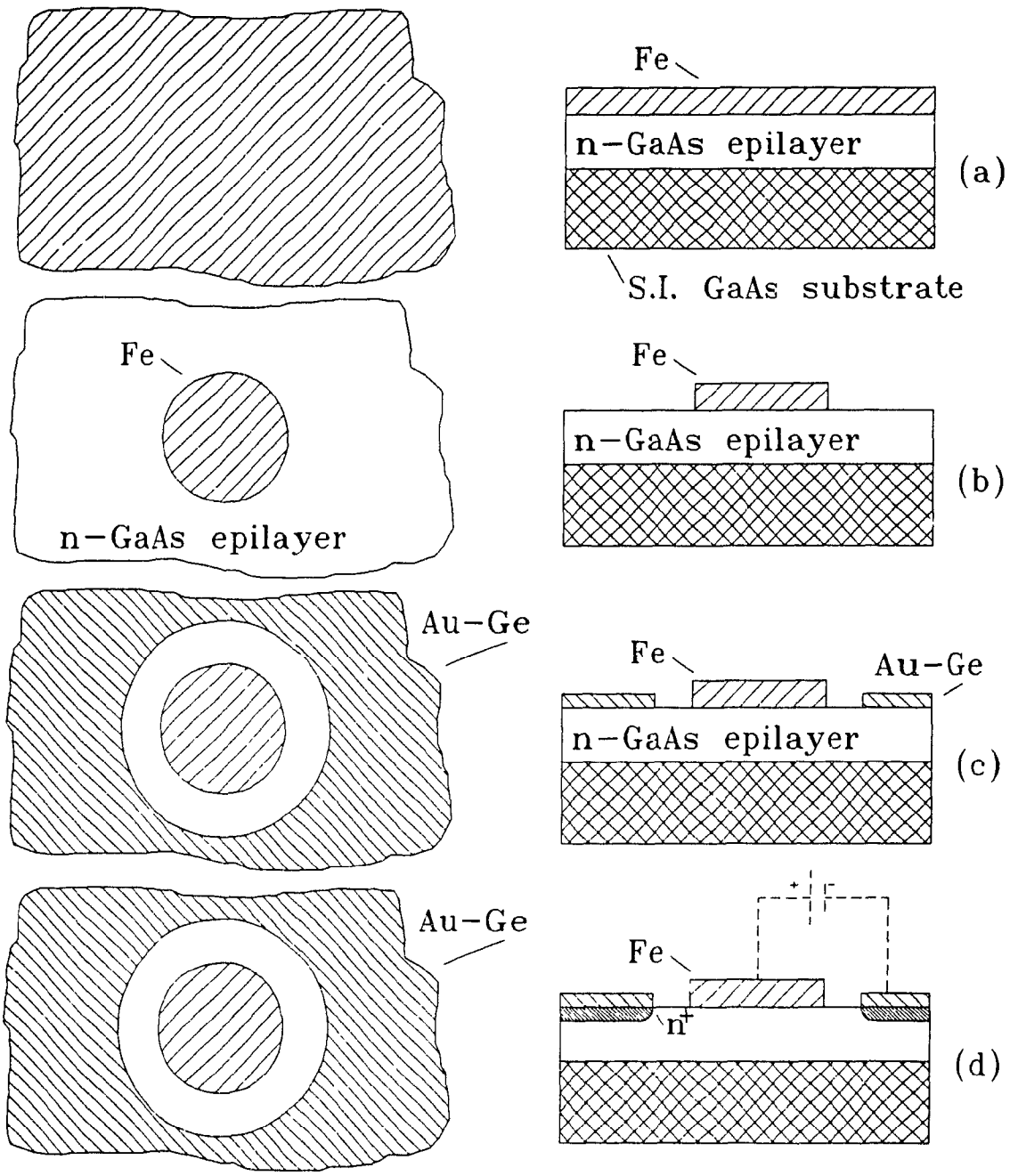

Fig. (3.3). The steps involved in the fabrication of iron-GaAs diodes.

typically taking less than 1 or 2 seconds to remove a layer of 0.1 μm thick. However, it also attacks GaAs, but fortunately at a slower rate (approx. 3 μm/min).

The next step involves the deposition of Au-Ge (gold-germanium) alloy to form the ohmic contacts as seen in Fig. (3.3)c. Selective deposition of Au-Ge is performed using the lift off technique (see appendix B.1). Lift-off is a photolithographic procedure where the photoresist pattern is established prior to metallization. After metallization is done the metal regions covering the photoresist are removed. The Au-Ge is deposited by thermal evaporation in a moderate vacuum of better than 10^{-5} torr.

The next step involves the alloying of the Au-Ge and the GaAs to create the heavily doped region in the semiconductor below the metal required for an ohmic contact, as shown in Fig. (3.3)d. The alloying takes place at a temperature of 450°C for 5 minutes in an inert atmosphere of nitrogen. The inert atmosphere helps to prevent oxidation of the Au-Ge. Fortunately, at this alloying temperature, iron diffuses only an insignificant amount into the GaAs. With this step, the diode fabrication is completed, as can be seen in Fig. (3.3)d.

The masks used for the iron-GaAs diodes give a Schottky contact diameter of 0.85 mm. The ohmic contact which covers the rest of the sample area, has its inner edge at a radius of 0.7 mm from the center of the diode.

3.2.2 Iron Gate GaAs MESFET Fabrication.

The dimensions of the MESFET are shown in Fig. (3.4). The gate length of the mask is 2 μm and the width is 50 μm. However, as it will later be seen, the gate length of 2 μm could not quite be achieved with iron, due to technological problems. The three masks used for the MESFET are shown in Fig. (3.5). These masks represent one set used in an 8 X 8 array of devices located on the photomask plate and eventually the wafer. A diagram, presenting the fabrication steps involved, is shown in Fig. (3.6).

Shown, Fig. (3.6)a, is the GaAs wafer, its surface covered with iron deposited by MOCVD. Prior to the isolation of the MESFET devices (which is the first fabrication step), the sample is cleaned and degreased (appendix C). The devices need to be isolated so that each MESFET can operate individually. This isolation is achieved through the use of the mesa geometry. This results in rectangular islands of active GaAs covered with a layer of iron, as can be seen in

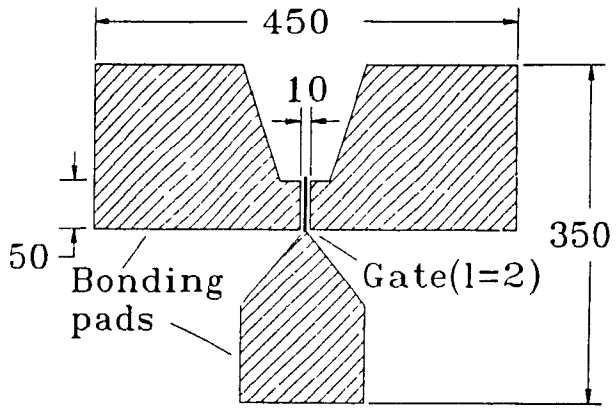

Fig. (3.4). A top view of the MESFET (dimensions are in microns).

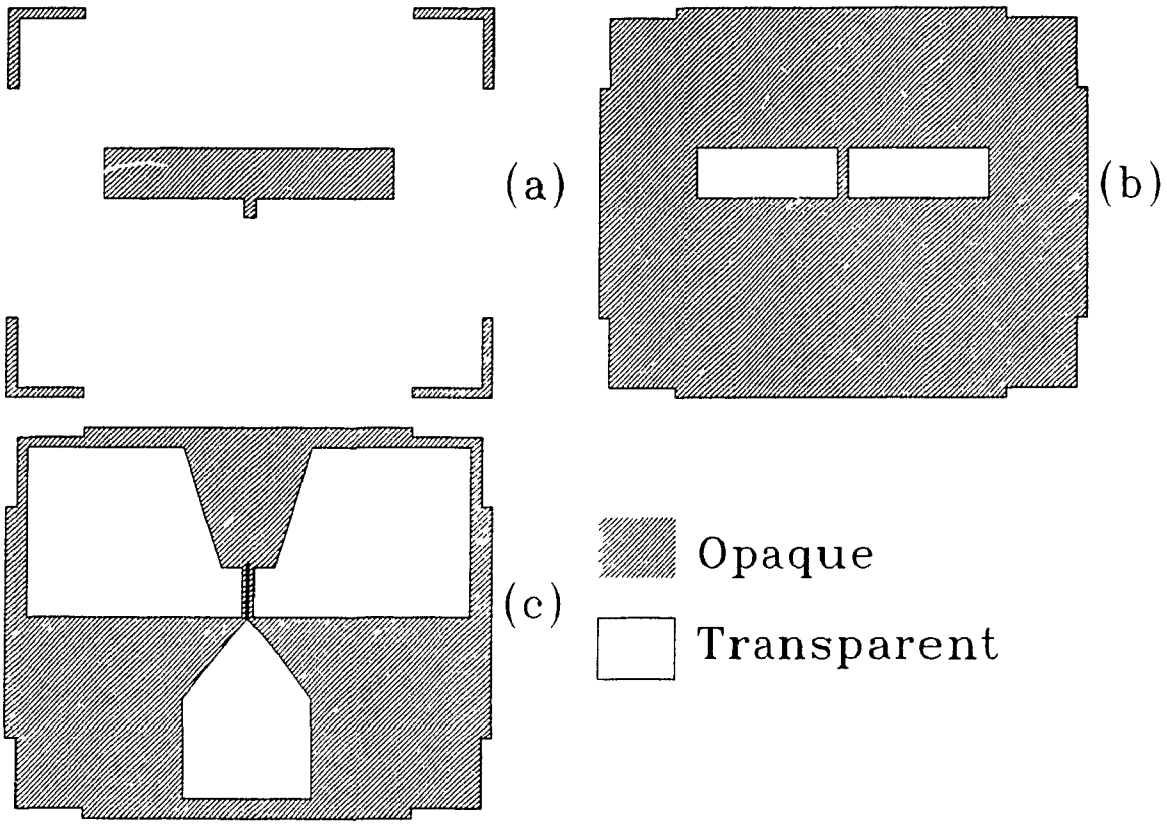

Fig. (3.5). The MESFET photomasks.

Fig. (3.6)b. The highly resistive semiinsulating substrate provides mechanical support for the devices while guarantying good electrical isolation from each other. The selective mesa etching is done by photolithography (appendix B.2), where mask (a) in Fig. (3.5) is used to define the regions. Using positive photoresist, the opaque region remains covered with photoresist and hence, will not be etched. The etchant solution used is sulphuric acid based (3 H_2SO_4: 1 H_2O_2: 1 H_2O) and etches both the iron and GaAs. The GaAs is typically etched at a rate of about 3 μm/min while the iron is attacked about twice as fast.

The next step involves the opening of windows in the iron layer (Fig. (3.6)c) in such a way that Au-Ge can be deposited directly onto the GaAs epilayer later on. This is required if ohmic contacts for the drain and source of the device are to be made. Using a similar procedure as in the previous step, selective etching is used to remove the unwanted (exposed) iron. The photolithography for the iron removal however, is done in such a way that the lift-off procedure (appendix B.1) can be used in the fabrication step that follows. The photoresist pattern is defined by mask (b) in Fig. (3.5). Under the opaque regions of the mask, photoresist remains protecting the iron while in the transparent areas, the iron layer is removed using the same etchant as used for device isolation. Even in the short time required for etching there is some photoresist undercutting and as a consequence the

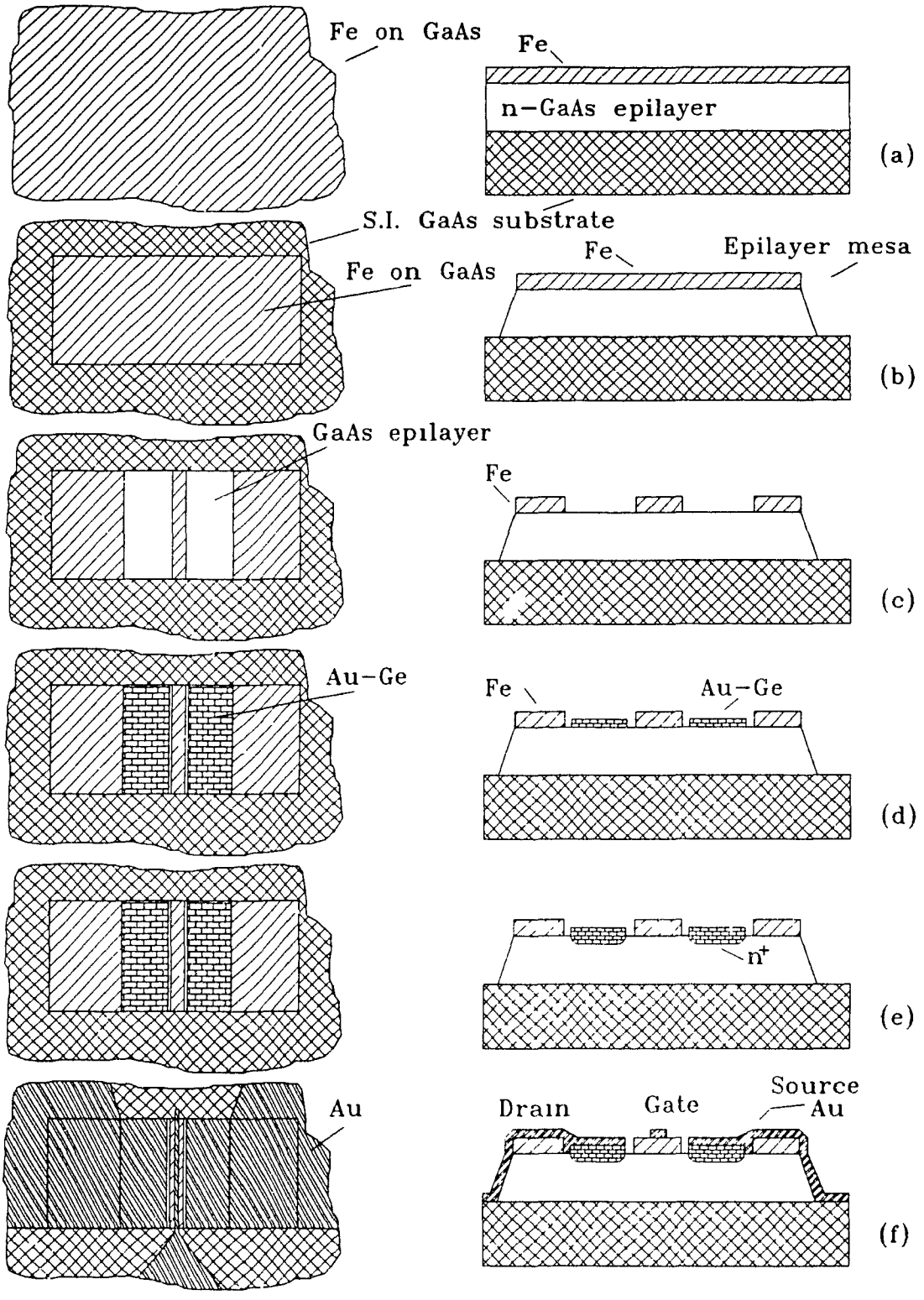

Fig. (3.6). A diagram showing the fabrication steps involved in the making of the iron gate MESFET. (Left side of page is the top view while the right side is the side view)

window in the iron layer is generally about a micron larger than the photoresist pattern.

This next step (Fig. (3.6)d) consists of applying the Au-Ge alloy with a thin overlay of nickel (Ni) eventually forming ohmic contacts. This metallization process is done by thermal evaporation. The selective deposition of Au-Ge/Ni is achieved by using the photoresist pattern that already exists from the previous step. With this lift-off procedure, Au-Ge/Ni remains in the areas where there in no photoresist which of course, corresponds to the regions where the windows in the iron have been opened in the previous step. As the Au-Ge/Ni pattern has the same dimensions as the photoresist pattern, the metal remains well inside the larger iron window, as can be seen in Fig. (3.6)d.

To complete the ohmic contacts, an alloying step follows, consisting of heating the sample at 450°C for 5 minutes in an inert atmosphere, namely nitrogen. This makes a heavily doped n^+ region below the metal. The nickel overlay serves to improve the wetting of the Au-Ge to the GaAs surface. Additionally, it helps to maintain sharp pattern edges during the heat treatment. The device after alloying is presented in Fig. (3.6)e.

The final procedure involves the fabrication of device bonding pads on the wafer. By using the lift-off technique gold is deposited selectively using thermal evaporation. Mask (c) in Fig. (3.5) is used to define the photoresist pattern.

As can be seen from the mask, gold in the gate region (2 μm line) overlays the iron. Initially, the gold was intended to be used as a mask for defining a 2 μm iron gate. Unfortunately, due to mask undercutting of the iron when wet etching, a two micron gate length was not possible to fabricate. This problem could possibly be remedied by the use of dry etching techniques although this was not attempted due to the unavailability of such equipment. The completed device where no iron etching in the gate region was performed is shown in Fig. (3.6)f. The resulting gate length is approximately 8 μm. The gold that overlays the ohmic contacts, form the drain and source connections.

3.3 Device Testing.

3.3.1 The Current-Voltage Apparatus.

The apparatus for performing current-voltage (I-V) measurements consists of a Wentworth Labs. probe station (PR0195 probes), a Hewlett-Packard model 4145A semiconductor parameter analyzer and an IBM PC microcomputer. The probe station allows the easy probing, using osmium probes, of device contacts as small as 50 μm^2 and thus, is used to make connections to the devices during testing. The probes themselves are then connected to the semiconductor parameter analyzer. This analyzer offers full computerized operation of I-V measurements. The voltage range over which the unit will scan can be programmed, as well as the scanning step. The voltage output of the unit can vary from -100 V to 100 V while currents, from -40 mA to 40 mA can be measured. For field effect transistor I-V data, an additional gate voltage can be set and varied automatically. The data collected by this unit are then transferred to an IBM PC which takes and stores the data on floppy disk for further analysis at a later time.

3.3.2 The Capacitance-Voltage Apparatus.

As in the I-V measurements, the probe station is used. A feature of the probe station which is important to note in this section, is that the probes are designed to have low capacitances and inductances. A Hewlett-Packard model 4274A, multi-frequency LCR meter is used to measure the capacitance. This unit has its own internal direct current (DC) bias voltage source that can be varied automatically. For capacitance-voltage (or C-V) measurements a small AC signal is superimposed on this DC bias voltage. With this apparatus, both the level and frequency of the AC signal can be varied. However, the frequency is not continuously variable and be can only adjusted to set values of 100 Hz, 200 Hz, 400 Hz, 1 KHz, 2 KHz, 4 KHz, 10 KHz, 20 KHz, 40 KHz and 100 KHz. The IBM PC controls the impedance analyzer and performs the required measurements. A measurement cycle proceeds as follows; the computer sets a bias voltage, obtains a capacitance value, measures the bias voltage and then stores the data. This control cycle is repeated with different biases until the desired range, has been covered. The bias voltage generated by the analyzer in not precisely known and it must therefore be measured externally during each cycle. The voltmeter that measures this bias voltage, is a Hewlett-Packard model 3468A multimeter which is also computer controlled.

3.4 Hall Effect Experiment.

A large part of the work for this thesis was devoted to the design of a novel high impedance and high resolution automated Hall effect system which is of general use in the characterization of semiconductors[17,28] and has been tested and used on the samples fabricated for this work.

3.4.1 The Data Acquisition Unit.

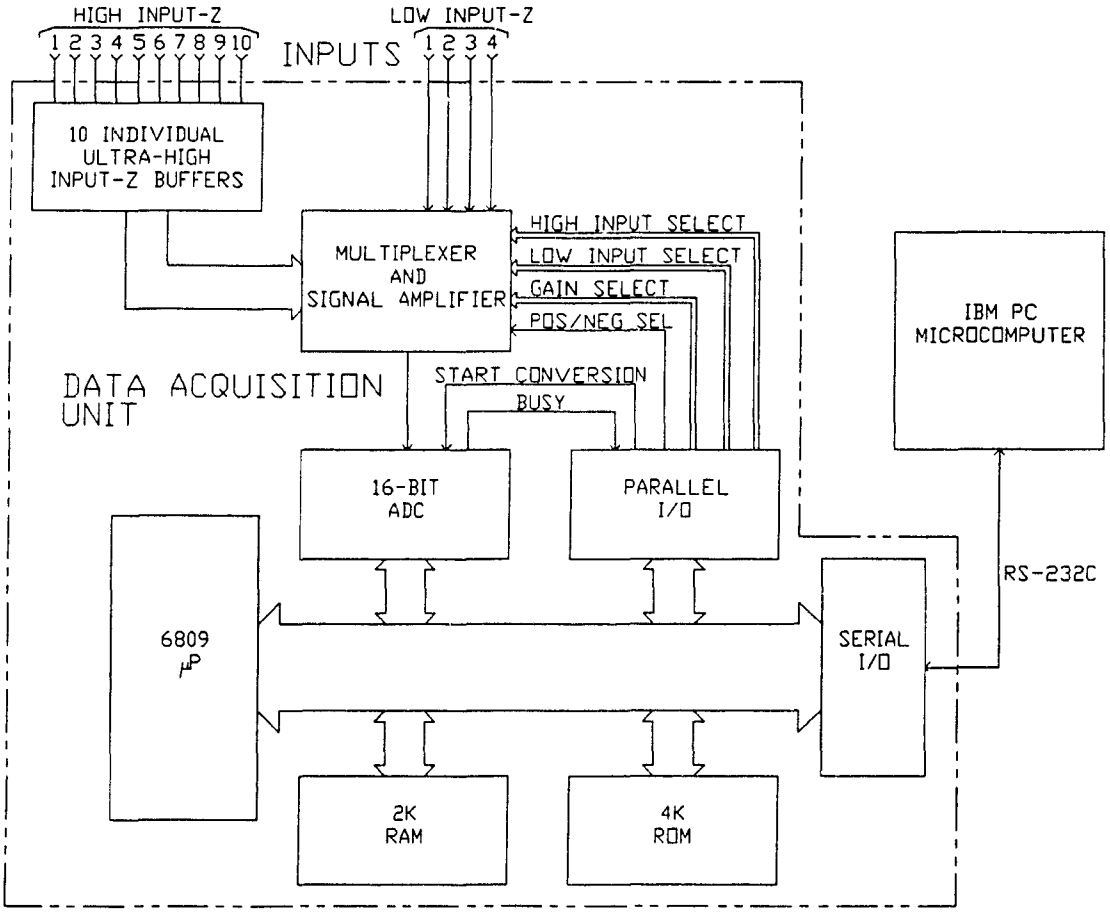

Fig. (3.7). A block diagram of the data-acquisition system.

A block diagram of the data acquisition unit is shown in Fig. (3.7). The system can be separated into four parts; the input buffering stage, the input multiplexing and amplification stage, the analog to digital conversion stage and the data processing computer stage which handles the analog to digital converter (ADC) data and communicates with an external microcomputer.

In order to obtain the very high input impedance required, a buffering stage is used, consisting of ten individual but identical buffer circuits. Each buffer is designed around an operational amplifier (op-amp) as shown in Fig. (3.8). An OPA111AM[a] op-amp was selected for this purpose[18]. It is a high performance FET input op-amp with the following specifications: More than 10^{13} Ω input impedance, 3 μV peak-to-peak (Vp-p) typical input noise and less than 1 pA input bias current. An input offset nulling circuit has been added to provide a trim range of 0.9 mV, which is more than

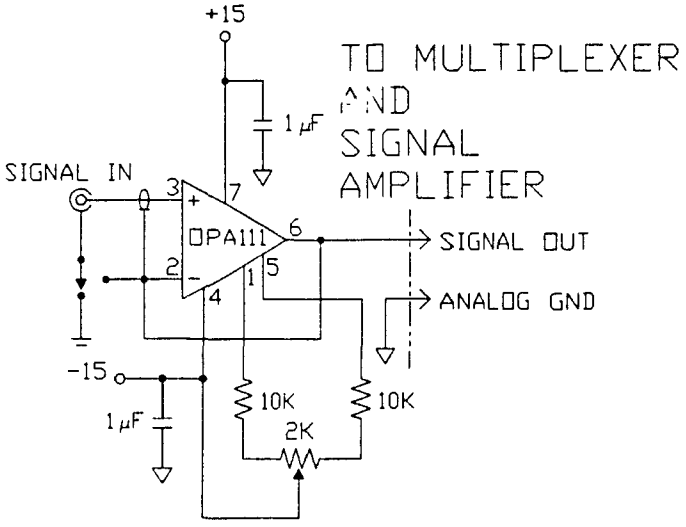

Fig. (3.8). Schematic diagram of a high impedance input buffer.

[a]Burr-Brown Corp., Tucson, AZ.

enough to compensate for the maximum specified offset of the op-amp. To achieve the low input current of the op-amp, the reduction of circuit board leakage is essential. The circuit board must be very well cleaned and sealed using a silicone coating. To further reduce leakage, the input is surrounded by a guard strip, connected to a low impedance source, kept at the same potential as the input. The op-amp output is used as the low impedance source. The potential drop across the leakage impedance will be almost zero, and will consequently give a near zero leakage current. The shields of the coaxial probe cables can be either connected to ground or be driven by the op-amp output, by using a jumper. Driving the shields improves the response time by reducing the charge stored in the cables.

The input multiplexing and amplifying stage consists of an instrumentation amplifier with two multiplexers for input selection as shown in Fig. (3.9). The two input multiplexers are connected in parallel so that measurements between any two of the fourteen inputs to this stage are possible as each multiplexer has its inputs addressed individually by the unit microcomputer. Ten of the inputs are connected to the high impedance input buffers and the other four are used for low

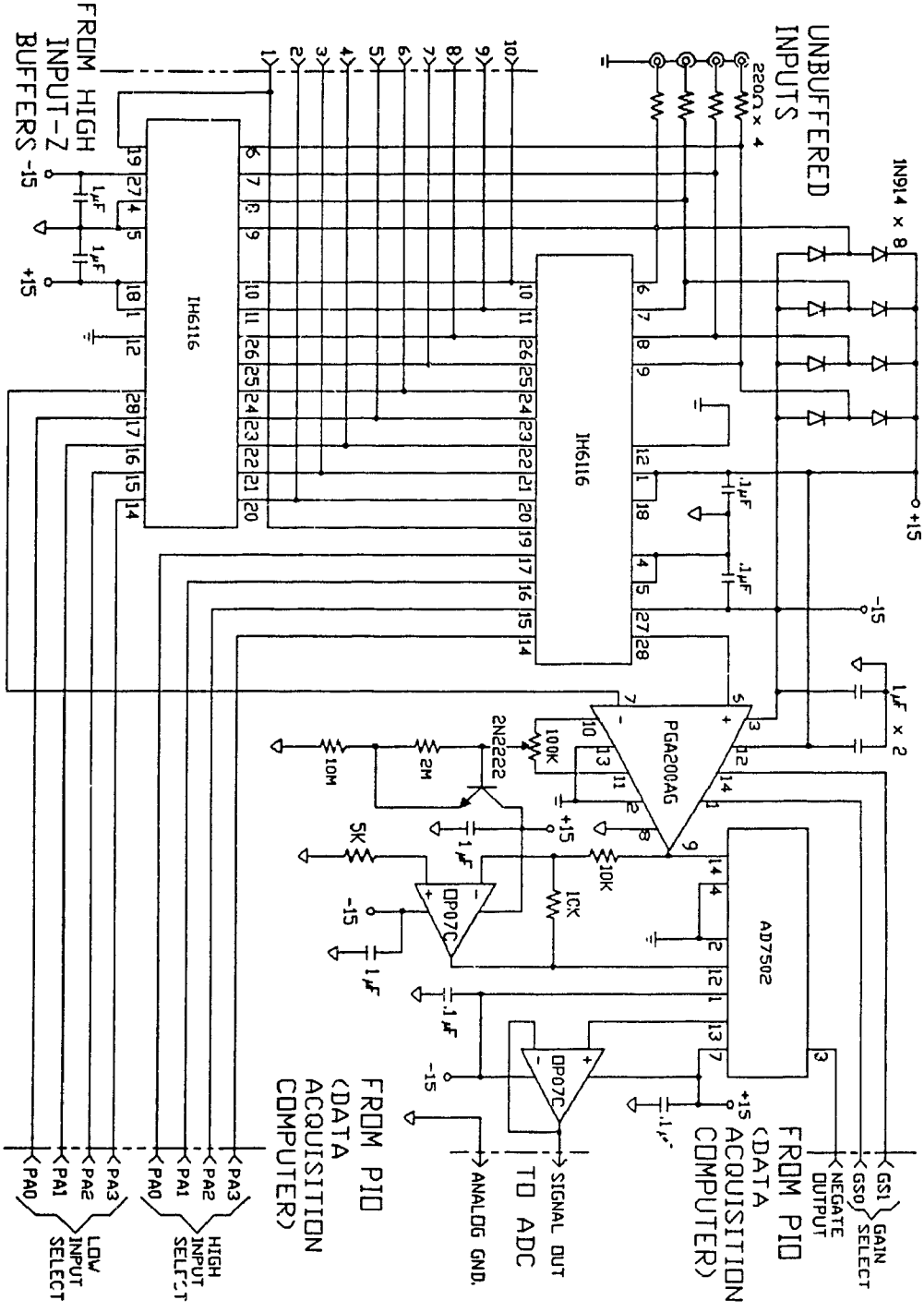

Fig. (3.9). Schematic diagram of the input multiplexer and amplifier.

impedance measurements. The multiplexers used are IH6116's[a]. Each of these is a 16 channel CMOS multiplexer. They introduce an insignificant error provided the source impedance is much lower than the instrumentation amplifier's input impedance (10^{10} Ω). This does not present a problem with the inputs connected to the buffers; however, when using the other inputs, the source impedance should be lower than 10^{6} Ω. This error is caused by the input current of the amplifier flowing through the on resistance (R_{on}) of the multiplexer. The four unbuffered inputs have an input protection circuit using 1N914 diodes and 220 Ω resistors. If the input voltage exceeds either the -15 or +15 V of the power supply lines, there is a path for the current through the resistors and the diodes to the supply lines protecting the multiplexers. The two unused multiplexer channels on each device are grounded on the circuit board and they can be used to ground reference any one of the other inputs. The signal amplifier uses a PGA200AG[b] which is a digitally programmable gain precision instrumentation amplifier. The unit microcomputer can program it to have any one of four voltage gain settings (1, 10, 100, or 1000). An input offset voltage trimming circuit for the instrumentation amplifier is included and it uses a 2N2222A transistor to improve temperature stability, as recommended

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[a]Intersil Inc., Cupertino, CA.

[b]Burr-Brown Corp., Tucson, AZ.

by the manufacturer4. The output of the instrumentation amplifier is then fed into a digital control signal. The AD7502[a] is a four channel differential CMOS multiplexer. In this design only two of the inputs are used. One of them is directly connected to the instrumentation amplifier output, and the other is connected to an OP-07C[b] op-amp inverter. This inverter negates the output of the instrumentation amplifier and hence, using the multiplexer, we can select either the true signal or the negated signal. The output of the multiplexer is connected to a noninverting op-amp (OP-07C) buffer which is necessary because the low impedance ADC load would create a substantial voltage drop in the signal as it passes through the multiplexer. Because of the very low noise and offset characteristics of the OP-07C op-amp, no external trimming circuits are needed.

The complete ADC circuit shown in Fig. (3.10), is based on an ADC71JG[c] ADC. This is a high resolution 16-bit ADC having a typical conversion time of about 60 μs. The ADC is set to accept an input voltage of 0-5 V. The digital data output of the ADC is interfaced to the unit microcomputer data bus through two 74LS374 latches. When the output of the ADC is ready (that is, when the conversion has been completed),

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[a]Analog Device, Inc., Norwood, MA.

[b]Precision Monolithics Inc., Santa Clara, CA.

[c]Burr-Brown Corp., Tuscon, AZ.

the data is latched automatically and the microprocessor is signalled. As the data is latched, the ADC can begin a new conversion cycle before the data is read, thereby improving acquisition speed. The logic support circuitry provides the transferring of 16-bit ADC data onto the 8-bit data bus, the controlling of the ADC, and the communication of necessary status information to the microprocessor.

When the ADC input voltage is negative, its digital output is zero. When the unit microcomputer receives a zero from the ADC, it assumes that the ADC's input is negative and automatically changes the polarity of the signal using the circuitry on the amplifier board. If after the change the computer still reads zero, the signal is considered to be zero; otherwise, the sign is changed and the ADC gives the absolute value of the voltage. This algorithm improves the resolution of the 16-bit ADC by including a sign bit, effectively giving 17-bit resolution over a -5 to +5 V range.

The unit microcomputer is based on the 2 MHz version of the 8-bit 6809[a] microprocessor. It is powerful although relatively easy to use, and has registers that can handle 16-bit data (to a limited extent), which is helpful when processing data from the ADC. The memory of the microcomputer consists of 2K RAM and 4K EPROM. The EPROM contains the operating software of the unit. A parallel I/O interface sends

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[a]Motorola, Inc., AZ.

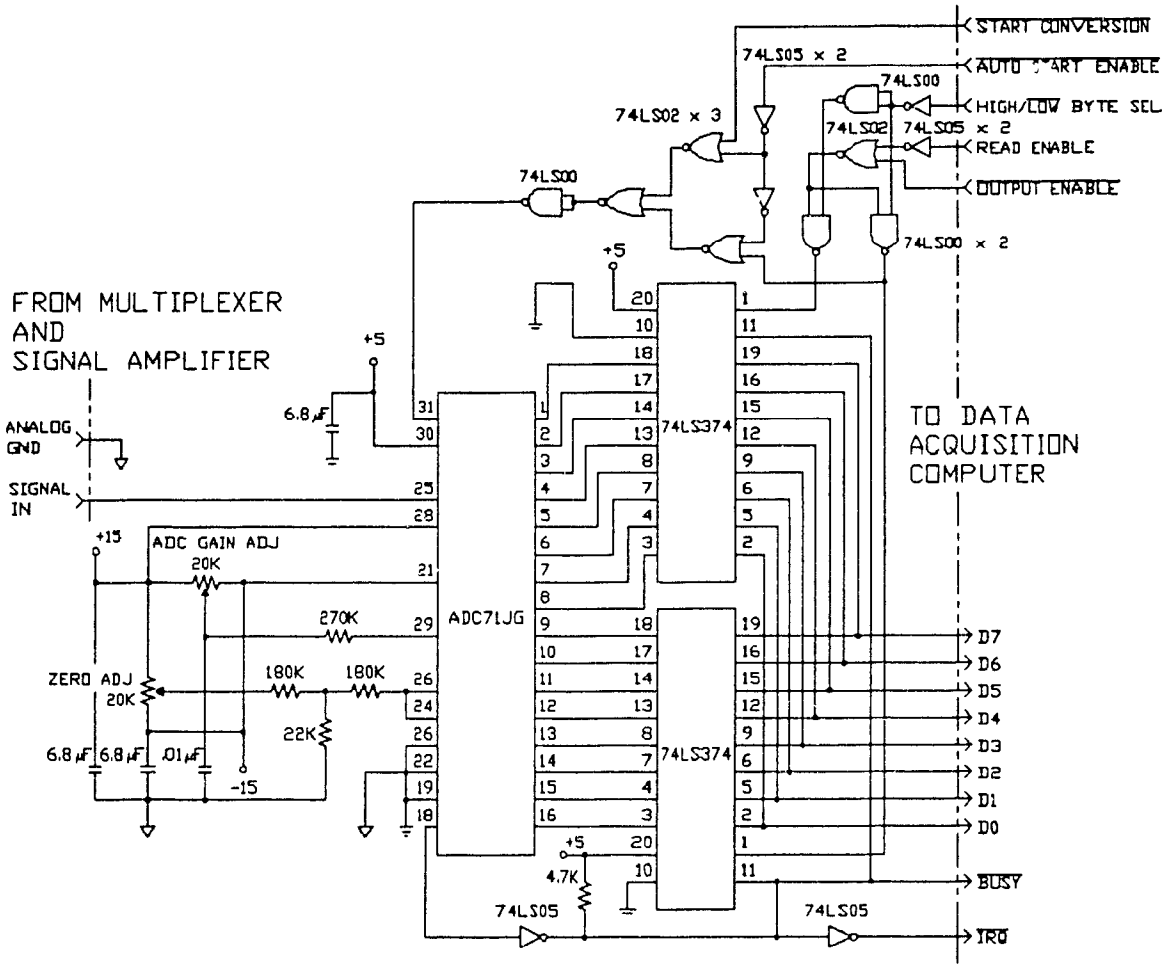


Fig. (3.10). Schematic diagram of the ADC.

and receives the necessary digital signals connected to the amplifier and ADC boards. A serial I/O interface is responsible for communications with an external computer via a standard RS-232C port.

Originally, we had many problems with large amounts of noise on the regulated voltage supplies. This was due to the digital circuit and was significant enough to affect the sensitive input stages. One of the primary sources of noise is the ADC, this being especially strong on the -15 V line. Hence, three different regulating sections have been added to the power supply. The sensitive buffer, multiplexer and amplifier section has its own set of regulators. The ADC and the microcomputer each have their own regulators. Noise transmission along the power supply lines also proved to be a very important noise problem. Breaking the voltage regulators in the power supply into three isolated regulator sections proved very beneficial.

The software for the unit microcomputer was developed in 6809 machine language to provide several functions and operation configurations to the user. Among them are the ability to measure, in a single acquisition cycle up to 16 different voltages within 1.5 ms using any combination of any two inputs of the unit. The system can also be programmed to do repeated measurements, within one cycle, on a given voltage so that an accurate average voltage value is obtained under noisy conditions. If the user so desires, the signal amplifier

gain can be set automatically, depending on the level of the input, to 1, 10, 100, or 1000 in order to obtain the highest possible resolution. Moreover, the maximum gain allowed for a given input voltage can be set by the user. A cycle is initiated by the external computer (PC) by sending a "start cycle" code, and terminated after all the data expected by the PC has been received. To improve efficiency, it is possible to send the start signal before the cycle has terminated, thereby allowing uninterrupted acquisition of data. By sending from the PC both a "start cycle on voltage" code and a voltage value to the unit, a cycle is initiated when this value corresponds, through an appropriate test, to an actual reading at a couple of inputs, selected as the control voltage. However, if the previous test is not satisfied, the unit returns the control voltage value alone to the PC, and the cycle is considered terminated. As the control voltage is always returned to the PC, real-time monitoring is possible. This procedure enables the unit to collect data as a function of selected input voltage.

The hardware of the data acquisition unit has been designed to provide a large amount of flexibility through appropriate software. For example, many inputs can be programmed into nearly any configuration, and the wide range of gains of the signal amplifier allows high impedance voltage readings over several orders of magnitude.

3.2.2 The Hall Effect Experimental Procedure and Apparatus.

Our high resistivity Hall effect measurement setup consists of:

1) a high isolation probe on which two samples can be mounted,
2) a dewar in which the probe can be placed to cool the samples to 1.4 K,
3) a magnet providing a field of 0 to 13 kG,
4) a complete automated data collection system using the data acquisition unit and an IBM PC as the external computer.

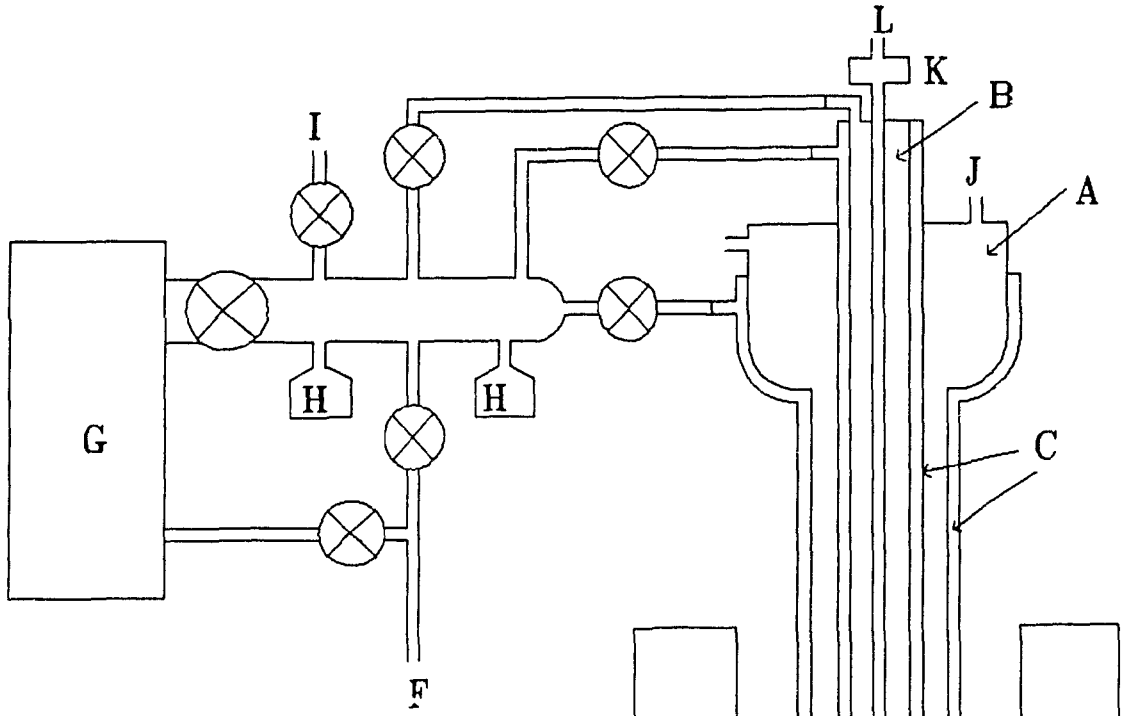
The probe consists of several hollow stainless-steel tubes leading into a copper end plate. To maintain the isolation required, the probe is wired with micro-miniature coaxial cables and the samples are mounted on alumina or sapphire wafers fixed to the end plate of the probe. To minimize the strain at low temperatures, the samples are glued only by one corner onto the wafers with GE varnish. Good thermal contact between the wafers and the end plate was obtained by using a mixture of vacuum grease and copper powder. Mounted near the samples on the end plate are a carbon glass temperature sensor and a resistive heater. Since the samples are first mounted on these wafers, a temperature gradient may exist between the

samples and the thermometer. To minimize this gradient, we let the temperature rise very slowly, in a natural way, from its lowest value. Above 20 K, moderate heating has little effect on the quality of the data.

The sample contacts are connected to the probe with very fine gold wires. These contacts are shaped in a standard bridge configuration[19], as can be seen in Fig. (3.12)a, for our automated high impedance measurements. Here, the Van der Pauw technique[20,21] has been discarded due to the fact that the large amount of switching of very low currents required would create too many large time delays for accurate high speed data acquisition.

The probe and the sample are inserted into a Dewar as shown in Fig. (3.10), Fig. (3.11). Liquid nitrogen is transferred into the outside cavity and liquid helium is transferred into the same cavity as the probe. This allows temperatures as low as 1.4 K by reducing the liquid helium vapour pressure. For temperatures above 77 K, the sample cavity is thermally isolated from the liquid nitrogen and the copper plate is heated to increase the temperature to more than 300 K.

Two current sources are used, namely KEITHLEY models 224 and 225, which can source down to 5 nA and .1 nA respectively. These provide the necessary excitation currents for each sample. The inputs of the data acquisition unit are op-amp inputs and, consequently, it is important that a path to



A - LN tank
B - Sample space cavity
C - Vacuum isolation
D - Sample holder
E - Electromagnet
F - Mechanical pump
G - Diffusion pump
H - Pressure gauges
I - Backfill port
J - LN fill port
K - Sample probe
L - LHe fill port
⊗ - Valves

Fig. (3.11). The Dewar setup.

ground be provided for the bias currents. This is achieved by connecting the low outputs of the current sources to the system ground inside the data acquisition unit. The system is set up to perform temperature dependent measurements, and hence the temperature sensor voltage is connected to two low impedance inputs which have been selected as the control inputs. Eight of the high impedance inputs are used by the four contacts on each of both samples.

Software for the IBM PC is written in compiled BASIC using assembly language subroutines in speed critical situations. The computer displays and stores in real time twelve different voltages and the temperature. In this case only eight of the voltages, four for each sample, are used. When the computer receives the temperature sensor voltage, it converts it to a temperature value (in Kelvin) by searching a calibration table. This calibration table was built with extreme precision, as any errors in it would propagate into the data. The system is capable of taking readings every .05 K, with .01 K precision at the lowest temperatures. Due to the characteristics of the temperature sensor, this precision decreases with increasing T.

The parameters required for an experiment include the start and the end temperatures, the temperature step at which readings will occur, and the current passing through each of the samples. During an experiment, all the data is stored directly in a disk file.

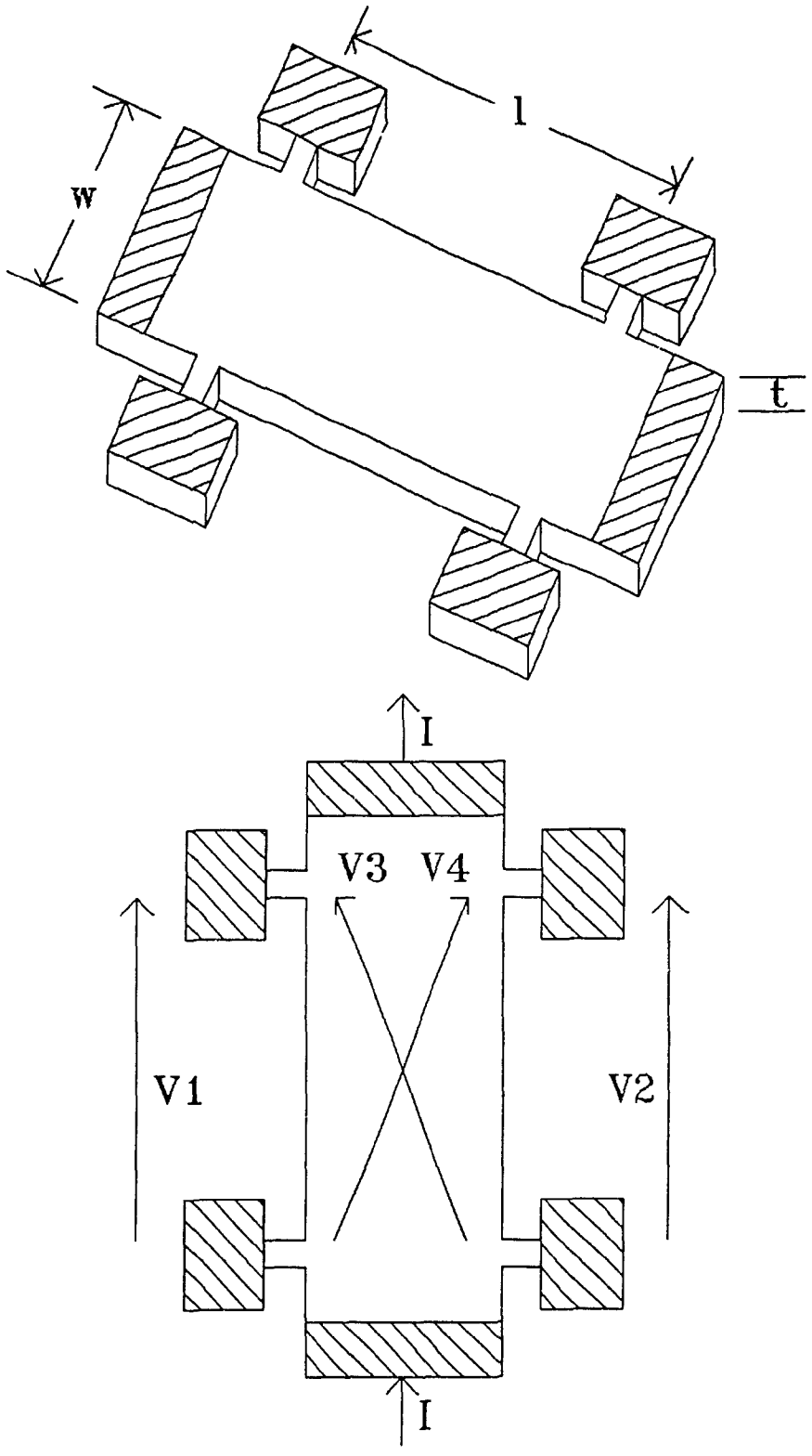


Fig. (3.12). The sample connections for bridge configuration Hall effect measurements.

The Hall effect measurements are performed in three temperature cycles; with no magnetic field, and with magnetic field applied in two antiparallel directions. The cycle without field is performed to determine the resistivity of the sample. The inversion of the B-field is used to reduce any errors that might be introduced by the earth's magnetic field or by alignment defects of the contacts. The Hall voltage, V_H, is determined in terms of the voltages of Fig. (3.12)b as

$$V_H = [V_4^+ - V_4^-]/2 = [V_3^+ - V_3^-]/2 \qquad (3.1)$$

where the superscripts indicate B-filed direction. In practice, the two differences in Eq. (3.1) are never exactly equal because of small defects of the sample geometry. If they differed too much, we concluded that the differences were due to non uniformity of the sample.

Measurements of V_X which is either V_1 or V_2 (or the average of the two) as well as V_H, knowing the excitation currents and sample geometries, allow direct extraction of the Hall data of interest (i.e. the mobility and the carrier concentration, typically).

3.2.4 System Test and Performance Results.

Each voltage was averaged over 128 readings. This averaging reduces the buffered input noise level of the system (3 μVp-p shields grounded and 4 μVp-p shields driven) while still permitting 4 acquisition cycles per second. The shields

were grounded for our experiments to take advantage of the lower noise level. The slower response time of the system does not affect the accuracy of the readings if the temperature, and hence the sample voltages, are varied slowly. The slow increase in temperature is necessary because errors caused by gradient effects between the sample and the holder can be important. The noise level of the unbuffered low impedance inputs is 1 μVp-p.

In order to determine the input impedance of the unit, a test sample of highly resistive semi-insulating GaAs was mounted on the probe. The resistance of the sample increases very rapidly with decreasing temperature. A constant current of 100 pA passing through the sample gave us the temperature dependent resistance data obtained in Fig. (3.13). Any deviation from the exponential behaviour would indicate the limit of the system. From the curve it can be concluded that a resistance above 2.5×10^{10} Ω can be accurately measured. The deviation seen above 2.5×10^{10} Ω was caused by the current source being unable to provide the set current, because the compliance voltage had reached its permissible limit. This limit is determined by the maximum common mode voltage that can be safely applied to the op-amp inputs without causing damage (12 V).

As evidence of the accuracy of the system, results obtained from Hall transport measurements on very high purity MOCVD grown GaAs samples are presented. The conductivity

behaviour of a highly compensated sample in a low temperature range is shown in Fig. (3.14). The resistance of this material reached over 10^8 Ω in this range. The straight portion of this curve is the much debated[22,23,24] but clearly evident $T^{-1/4}$ law hopping conductivity, which can only be observed with very accurate and low noise data. The slight discontinuities in the data result from the need to the change the excitation current through the sample, which is required to maintain low electric field conditions as the resistivity rapidly decreases as the temperature increases. They are originated by small nonlinearities in the contacts.

Fig. (3.15) shows the Hall mobility vs. T for another high purity GaAs sample. We point out that the Hall mobility is computed from three sets of data corresponding to the needed magnetic field configurations, and that errors are additive. The data is nevertheless excellent; this is also demonstrated by the corresponding free electron concentration shown in Fig. (3.16) as a function of T. The ability of the system to obtain such clean data is essential to study subtle scattering mechanisms which might be otherwise undetectable.

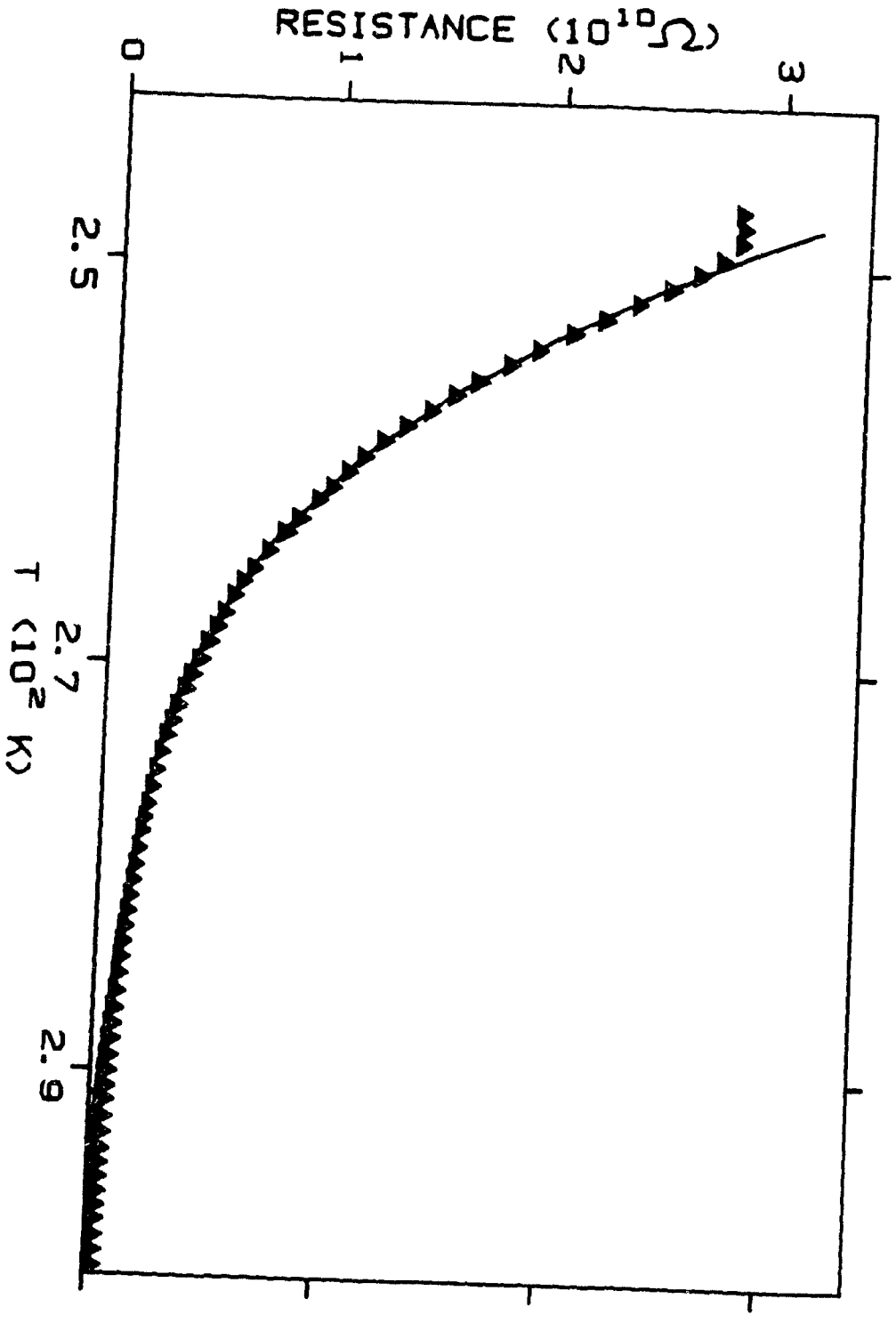


Fig. (3.13). Resistance of a GaAs substrate vs. temperature.

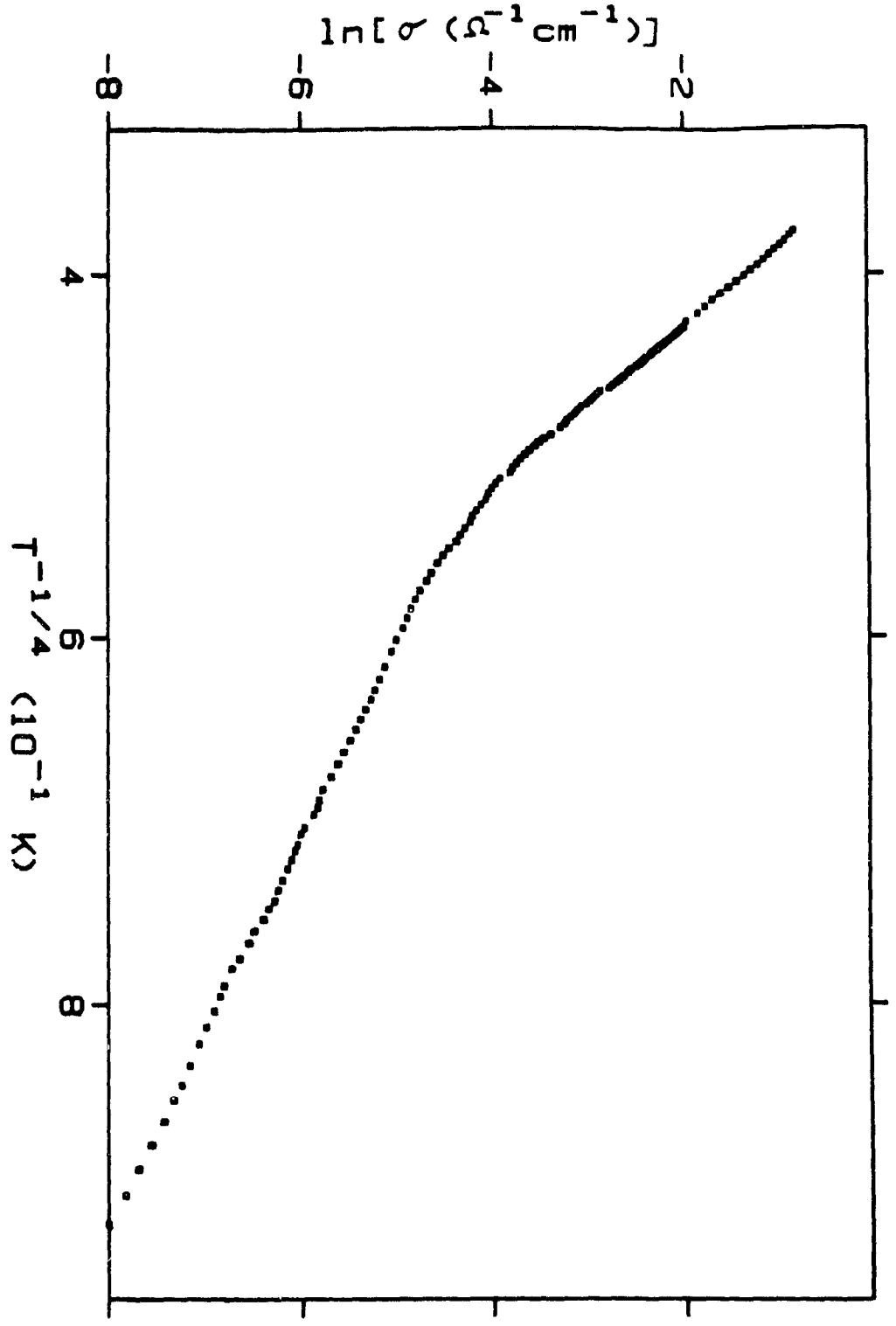


Fig. (3.14). Conductivity behaviour of high-purity n-GaAs at low temperatures.

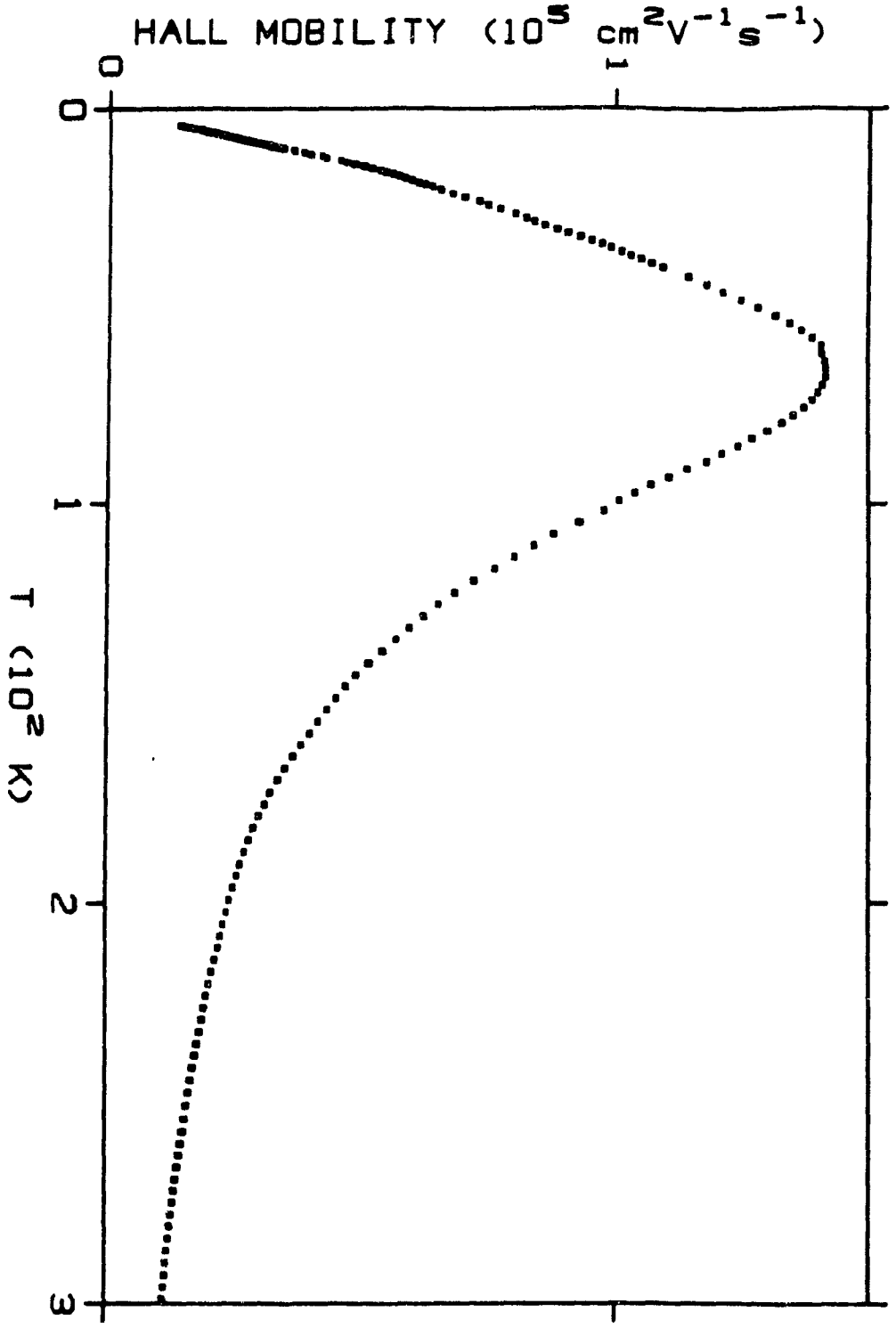


Fig. (3.15). Hall mobility of high-quality n-GaAs vs. temperature.

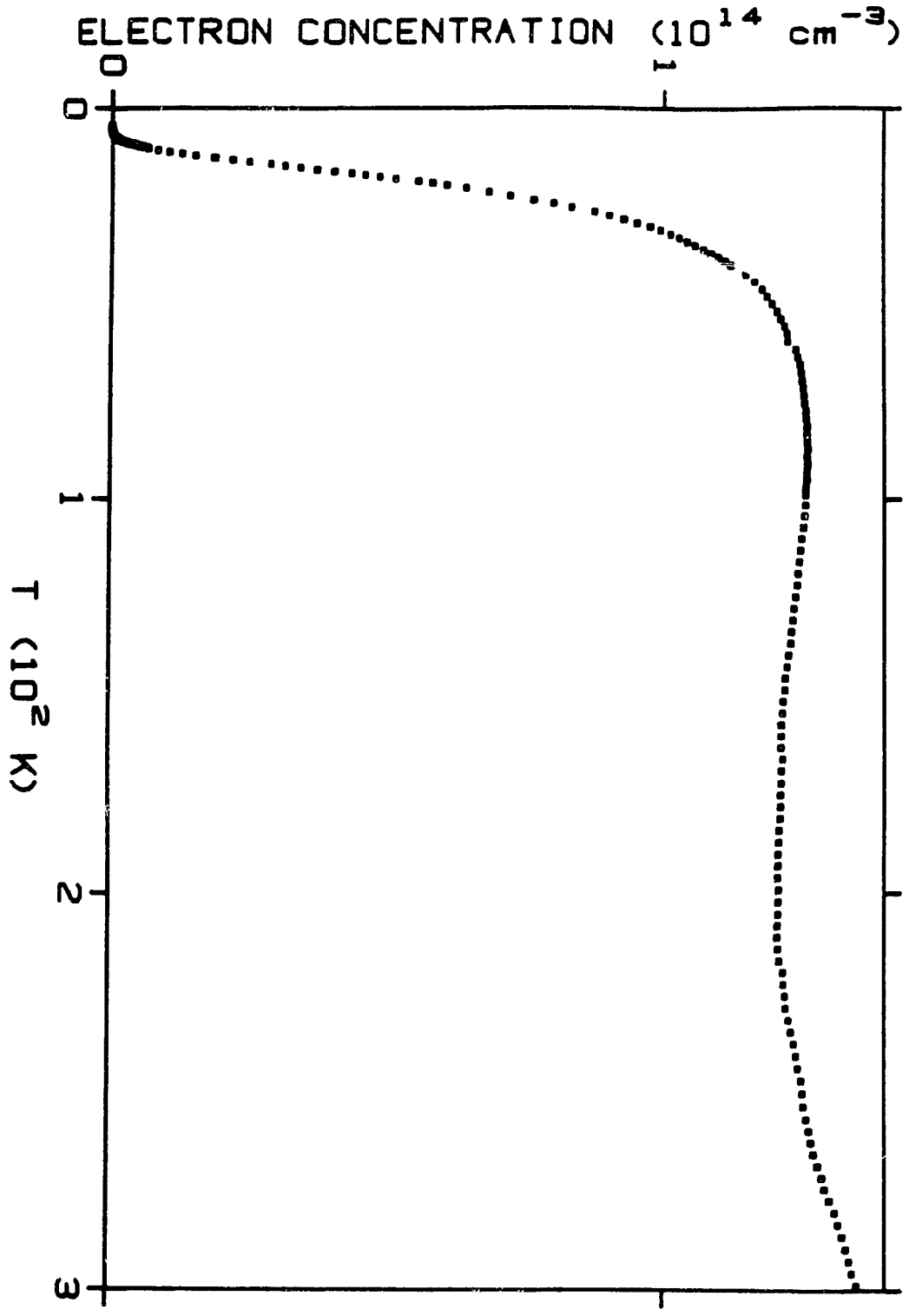


Fig. (3.16). Corresponding electron concentration vs. temperature.

CHAPTER 4

RESULTS AND ANALYSIS

A total of nine working devices are presented consisting of four Schottky diodes and five MESFETs. These devices have been made using the iron on GaAs contact; however one of each device type has been made with the more conventional aluminium on GaAs. The aluminium contact devices have been included for comparison purposes.

Due to the poor quality TMG available, the GaAs epilayers grown in our reactor tended to be somewhat

Table (4.1). List of working devices presented.

Device	Type	Epilayer Thickness (μm)	Diode area (cm^2)	Gate length (μm)	Gate Width (μm)
M6.2	Fe Diode	2	0.00535	------	------
M6.9	Fe Diode	2	0.0055	------	------
M6.10	Fe Diode	2	0.00535	------	------
MA6.1	Al Diode	2	0.003	------	------
MF6.36	Fe MESFET	2	--------	8-9	45
MF9.18	Fe MESFET	1.75	--------	8-9	45
MF9.21	Fe MESFET	1.75	--------	8-9	45
MF9.26	Fe MESFET	1.75	--------	8-9	45
MAF9.11	Al MESFET	1.75	--------	2-3	50

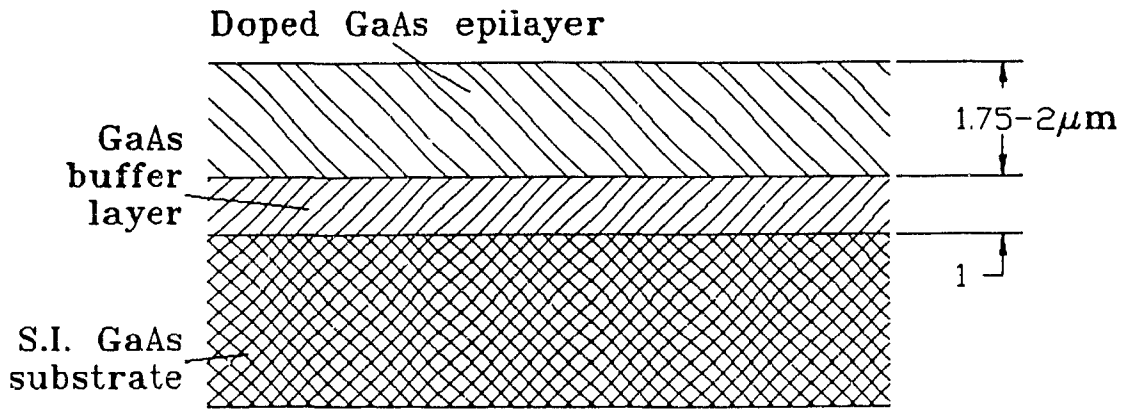


Fig. (4.1). A crossectional view of the epilayer structure.

contaminated and the background doping levels were mostly too high for device fabrication. As a result, the successful devices were fabricated on wafers prepared elsewhere[a]. Two different wafers were used (labelled M6 and M9). The difference between the two is the doping level and the active doped layer thickness (M9 is thinner but more heavily doped). The layer of the first wafer is 2 μm thick while that of the second is 1.75 μm thick. Both wafers include a 1μm undoped buffer layer as shown in a detail of the structure presented in Fig. (4.1).

The devices were prepared as described in chapter 3. The iron for each of the diodes (see Table (4.1)) was grown at 100°C for 5 minutes whereas the iron for the MESFETs was grown at 500°C for 35 minutes.

Due to the low lattice mismatch between iron and GaAs (1.2%) it was speculated that the iron deposited might be

[a]OMVPE Technologies, St. Laurent, Quebec.

crystalline. In Fig. (4.3) X-ray data is presented for iron grown at 100°C. The data was obtained in a powder diffractometer using a copper K-α X-ray source. The peak seen at about $2\theta = 45°$ is from (111) oriented iron. It is suggested from preliminary rocking-curve data that the iron grown at this temperature (100°C) is polycrystalline[25]. Iron grown on GaAs at higher temperatures might be more oriented although this has not been established yet.

4.1 Results from Capacitance-Voltage Measurements.

4.1.1 Schottky Barrier Height Analysis.

The barrier height can be determined by the use of capacitance-voltage measurements. For a one sided abrupt junction, the capacitance per unit area is given by

$$C = \epsilon_s/W \qquad (4.1)$$

where W is the depletion width found by solving Poisson's equation and ϵ_s is the dielectric constant of the semiconductor. Rewriting Eq. (4.1) including the expression for W we obtain

$$C = (q\epsilon_s N_B/2)^{1/2}(V_{bi} - V - kT/q)^{1/2} \qquad (4.2)$$

where V_{bi} is the built-in voltage equal to $\phi b - \xi$, given that ξ is the difference between the conduction band edge and the Fermi level in the semiconductor. Rearranging Eq. (4.2) we

obtain

$$1/C^2 = (2/q\epsilon_s N_B)(V_{bi} - V - kT/q) \qquad (4.3)$$

where N_B is the background doping level, replaced by N_d in n-type semiconductors. From Eq. (4.3) it can be seen that if a $1/C^2$ vs. V plot for large V values gives a straight line, the extrapolation of this line to the voltage axis ($1/C^2 = 0$) requires that at the intercept

$$V_{bi} - V_i - kT/q = 0 \qquad (4.4)$$

or

$$V_i = V_{bi} - kT/q \qquad (4.5)$$

where V_i is the voltage at the intercept. Substituting in the expression for V_{bi}, we obtain

$$V_i = \phi_b - \xi - kT/q. \qquad (4.6)$$

Therefore the barrier extracted from straight line $1/C^2$ vs. V plots can be found and is equal to

$$\phi_b = V_i + \xi + kT/q. \qquad (4.7)$$

For metal-semiconductor contacts, the above abrupt junction assumption applies. However, the properties of the metal contact must also be included in the formulation as they have important effects. If the Schottky diode has an interfacial layer, the capacitance is modified and an adjustment must be made to the barrier height expression in order to obtain an accurate result. Cowley proposed that if there is an interfacial layer (very common in practical devices), ϕ_b in Eq. (4.7) is replaced by $\phi_{b0}+\phi_1/4$[8], where $\phi_1 = 2\alpha^2 qNd/\epsilon_s$ and ϕ_{b0} is the flatband barrier height. In nearly

all cases however, $\phi_1 << \phi_{b0}$. This is because α, which is a function of interfacial layer thickness, is very small. Hence, rewriting Eq. (4.7) we have

$$\phi_{b0} = V_i + \xi + kT/q. \qquad (4.8)$$

This final equation can now be used to determine ϕ_{b0}, where V_i is the voltage intercept in the $1/C^2$ vs. V plot. ξ is calculated from the equation

$$\xi = (kT/q)\ln(N_c/N_d), \qquad (4.9)$$

N_c being the effective density of states in the conduction band, and kT/q is the thermal voltage. Table (4.2) lists the ϕ_{b0} values for the different devices.

Plots for $1/C^2$ vs. V of three iron contact devices are presented in Figs. (4.4), (4.5) and (4.6). In Fig. (4.7) the data from a more common aluminum on GaAs contact is shown.

The first thing that is noticed in the plots for the Fe-GaAs diodes is that the intercept on the voltage axis varies substantially with frequency. Commonly, shifting occurs due to carriers trapping inside the semiconductor. But here as this shifting is not seen in the Al-GaAs diode which has been made on the same wafer, it is assumed that the shifting is mostly related to the interface properties and not to the GaAs. It seems likely that this frequency dependence is introduced by the behaviour of the interface states. This apparent decrease in capacitance seems thus to be due to the fact that the population of the interface states does not vary rapidly enough for them to be in equilibrium with the metal.

Table (4.2). Data obtained from the C-V measurements.

Device	ϕ_{b0}(V)	V_{bi}(V)	(V)	$N_d(cm^{-3})$
M6.2	0.96	0.81	0.16	1.09×10^{15}
M6.9	0.93	0.77	0.15	1.17×10^{15}
M6.10	0.93	0.78	0.15	1.19×10^{15}
MA6.1	0.88	0.73	0.15	1.51×10^{15}

When the interfacial layer is not sufficiently thin, good communication between the metal and the interface states is not achieved and a longer time constant results due to the inability of electrons to follow the high frequency oscillations.

An additional shifting effect could also arise if there is a very thick interfacial layer, due to the fact that a capacitor between the metal and the semiconductor is formed. However, this situation is much more complicated and would result in non-linear $1/C^2$ vs. V plots. However, the plots show no noticeable non-linear effect.

In order to minimize barrier height error due to measurements, the low frequency measurements are used. A 1 KHz signal was found to be satisfactory since no detectible shift was observed in this frequency range.

The flatband barrier height (assuming the unified defect model, the most commonly used assumption for GaAs, see chapter

2) and a substantial interfacial layer and a density of states of 1.2 x 10^{14} $V^{-1}cm^{-2}$, is given by

$$\phi_{b0} \approx E_g/q - \phi_1 \qquad (4.10)$$

The values for level ϕ_1, obtained from the measured ϕ_{b0} values, range from 0.46 to 0.54 V. These values are comparable to those reported in the literature[1,26].

4.1.2. Carrier Distribution and Concentration.

C-V measurements can also be used to determine the carrier density and doping profile in the GaAs epilayer. Differentiating Eq. (4.3) with respect to voltage we obtain

$$\frac{d(1/C^2)}{dV} = \frac{2}{q\epsilon_s N_d} \qquad (4.11)$$

From this we can see that if a straight line is obtained from the $1/C^2$ vs. V plot the slope is equal to $2/q\epsilon_s N_d$. Hence the concentration can be obtained from the slope. This of course, assumes that the depletion approximation applies where the carrier density is negligible inside the depletion region and rises abruptly to the local background doping level at the edge of the depletion region.

In the linear region of the our plots the donor density was determined (using the 1 KHz measurement) for each of the Schottky devices and is presented in Table (4.2). Although the data presented is for devices fabricated on samples

obtained from the same wafer, the values indicate that there might be some nonuniformity of the GaAs over the area of the wafer.

Fig. (4.8) shows a $1/C^2$ plot where larger reverse biases were used. It can be seen that, as the reverse voltage is increased (i.e. the depletion width is increased), different slopes result, showing how the depletion edge passes through the GaAs active layer, the undoped buffer layer and the semiinsulating substrate. These regions are labelled A, B and C, respectively, in the plot.

4.2. Results from Current-Voltage Measurements.

4.2.1. Forward Bias Analysis.

From the forward bias data a measurement of the barrier height and an evaluation of the diode quality can be obtained. For moderately doped semiconductors the I-V characteristics are given by the thermionic emission current-voltage equation as described in chapter 2. For an ideal diode equation with an ideality factor η, the current voltage relation is given below

$$J = J_0\left[\exp(qV/\eta kT) - 1\right]. \qquad (4.12)$$

However, in a practical diode there are usually series and shunt resistances which cause a deviation from ideality. A model including these resistances is given in Fig. (4.2) and the diode equation becomes

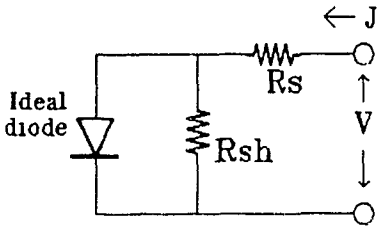


Fig. (4.2). The ideal diode with a series and a shunt resistance.

$$J_F = J_0\left[\exp(q(V - JR_s)/\eta kT) - 1\right] + (V - JR_s)/R_{sh} \qquad (4.13)$$

This equation which is nonlinear is solved numerically, using a simple bisection method for each voltage point. We obtain the values of the parameters J_0, R_s, R_{sh} and η by fitting the theoretcal J_F vs. V curve (Eq. (4.13)) to the experimental data.

The data for the diodes (M6.2, M6.9 and M6.10) are presented in Figs. (4.9), (4.10) and (4.11), respectively. A perfect fit of the theoretical J_F vs. V curve over the total range of variation of forward V was not possible. The fit was therefore optimized for lower values of V and deviation of the theoretical curve from the experimental points is ascribed to a voltage dependence of one or more of the parameters in Eq. (4.13). The field dependence of the Richardson constant A^* ($A^* \approx$ 144 under high electric field and $8.2 A/cm^2K^2$) and, hence, of the constant J_0, is well documented[1] and suffices to account

for the observed deviation. At high forward voltages the built-in electric field decreases sufficiently to be in the low field regime. As a consequence A^* decreases, hence, reducing J_0. The possibility of a reduction in forward current at higher voltages due to series resistance was dismissed as the resistance value to account for this large deviation was unreasonably high. In the MESFET gate I-V plot (Fig. (4.12)) this is relatively good however the characteristics show a poor diode. The η values for the diodes obtained are reasonable and compare well to those obtained by others using different metals. The empirical parameters obtained for each of the devices through curve fitting are presented in Table (4.3). A separate determination of R_s needed to be done by taking the slope of the I-V curve at high forward voltages (5 Volt).

From the J_0 values obtained, we can now determine the barrier height at zero bias. In chapter 2 the saturation

Table (4.3). The parameters obtained from the forward bias I-V plots for the Schottky contact devices.

Device	J_0 (A/cm^2)	η	R_s (Ω)	R_{sh} (Ω)	ϕ_b (V)
M6.2	2.0 x 10-10	1.28	4.4 x 103	5.6 x 109	0.99
M6.9	1.5 x 10-7	1.27	4.2 x 103	5.8 x 108	0.82
M6.10	6.5 x 10-7	1.28	4.3 x 103	1.1 x 108	0.79
MF9.18	7.0 x 10-7	5.3	1.0 x 103	1.4 x 1010	0.78

current J_0 was given by

$$J_0 = A^*T^2\exp(-q\phi_b/kT) \qquad (4.14)$$

Rearranging and solving for the barrier height we obtain

$$\phi_b = (kt/q)\ln(A^*T^2/J_0) \qquad (4.15)$$

Here all the parameters except A^* are known. As the value of ϕ_b is not very sensitive to the choice of A^*, the theoretical high field value of $A^* \approx 144$ A/cm^2K^2 is used in this calculation. The barrier heights obtained in this manner are shown in Table (4.3).

4.2.2. Reverse Bias Analysis.

Measuring reverse bias characteristics of metal-semiconductor contacts is informative as it provides yet another method of calculating Schottky barrier properties.

In this section, a reverse bias analysis is carried out to obtain a measure of the flatband barrier height (ϕ_{b0}) as well as a quantitative evaluation of the interfacial layer thickness (δ).

The total reverse current, J_R, is given by

$$J_R = J_{RT} + J_r + V/R_l. \qquad (4.16)$$

Here J_{RT} is the reverse bias thermionic emission current component, J_r is the recombination current contribution and V/R_l is a leakage current where R_l is a leakage resistance.

In relation to thermionic emission, there are two

important effects that lower the Schottky barrier; the first is due to image forces and the second arises from the interfacial layer. The sum of the two effects gives a total reduction of the barrier height given by the following

$$\Delta\phi = (qE_{max}/4\pi\epsilon_s)^{1/2} + \alpha E_{max} \qquad (4.17)$$

where

$$E_{max} = (2qN_d/\epsilon_s)^{1/2}(V + V_{bi} - kT/q)^{1/2} \qquad (4.18)$$

and

$$\alpha = \delta\epsilon_i/(\epsilon_i + q\delta D_s), \qquad (4.19)$$

where Ds is the density of surface states. The reverse current for a thermionic emission dominated system depends only on the barrier lowering and is given by

$$J_{RT} = A^*T^2\exp(-q\phi_{b0}/kT)\exp(q\Delta\phi/kT)$$
$$= J_{R0}\exp(q\Delta\phi/kT) \qquad (4.20)$$

The recombination in the reverse direction is given by

$$J_r = qn_i d/2\tau_r \qquad (4.21)$$

Substituting in d, which is the depletion width obtained from solving Poisson's equation, and rearranging we have:

Table (4.4). The reverse bias parameters for the Fe-GaAs Schottky contacts.

Device	J_{R0} (A/cm^2)	α (cm)	J_{r0} (A/cm^{2}V$^{1/2}$)	R_i (Ω)	ϕ_{b0} (V)
M6.2	3.5×10^{-11}	7.9×10^{-6}	0	7.1×10^{9}	1.03
M6.9	3.5×10^{-9}	4.4×10^{-6}	0	8.2×10^{8}	0.92
M6.10	3.6×10^{-9}	4.7×10^{-6}	3.7×10^{-7}	1.0×10^{8}	0.92
MF9.18	8.2×10^{-9}	2.5×10^{-6}	0	1.1×10^{8}	0.90

$$J_r = (qn_i\epsilon_s/2\tau_r N_d)(V_{bi}-V)^{1/2}$$
$$= J_{r0}(V_{bi} - V)^{1/2} \qquad (4.22)$$

The contribution of tunnelling in reverse bias was not included, as the GaAs in our samples is not sufficiently doped to expect this phenomenon at room temperature.

Fits of this total reverse current expression on the data were performed and the results are presented (Figs. (4.9), (4.10), (4.11) and (4.12)). The coefficients (J_{R0}, J_{r0}, α and R_l) obtained from the fits are presented in Table (4.4). The flatband barrier height is calculated from J_{R0} , the thermionic emission prefactor, for the devices. The resulting ϕ_{b0} values are also presented in Table (4.4).

4.3. Results from Hall Effect Measurements.

The Hall effect measurements were performed to determine the mobility and the carrier concentration of the GaAs active layer.

Using the experimental procedure described in chapter 3, the bridge contact configuration on a sample of each of the two wafers (M6 and M9) was used to obtain the V_X and V_H voltages. The Hall mobility was then calculated using the following expression

$$\mu_H = \frac{V_H}{V_X}\frac{1}{wB}, \qquad (cm^2V^{-1}s^{-1}) \qquad (3.3)$$

where B is the magnetic field in $Vscm^{-2}$, l is the sample length and w is the sample width. The corresponding carrier concentration in the conduction band, n_c, is given by

$$n_c = IB/V_H tq \quad (cm^{-3}) \qquad (3.4)$$

where I is the excitation current and t is the sample thickness. This concentration gives the doping level, N_d, to a good approximation.

Curves showing the Hall mobility and concentration for the two wafers (M6, M9) are presented in Figs.(4.13) and (4.14), respectively.

4.4. Results from MESFET Measurements.

The MESFET's I-V test results are presented in Figs. (4.15), (4.16), (4.17), (4.18) and (4.19). The first four plots are for the iron gate devices while the fifth is for the aluminum gate device.

The I-V plots for the iron gate devices show exceptionally high pinch-off voltages ($I_{ds} = 0$), much higher than the active layer requires for full depletion. This is believed to be due to the fact that the undoped buffer layer became more conductive during the heating procedure required for the iron growth. This heating of the wafer is likely to have caused the diffusion of dopant from the active layer into the buffer layer, resulting in a thicker (although less

uniform) active channel region for the device. In the I-V plots for the iron gate MESFETs, it is seen that the saturation current tends to display uncharacteristic behaviour at a certain gate voltage. This behaviour is believed to occur when the depletion region extends into the buffer layer. It is interesting to note that this effect is not observed in the I-V characteristic of the aluminium gate device. In this device no heating was required in the fabrication of the gate.

In Fig. (4.20) the transfer characteristics for each of the devices are also shown.

4.5. Comments on Results.

The results presented for the Schottky contacts were obtained using three methods of measurement; forward bias and reverse bias current-voltage measurements, and capacitance-voltage measurements. The barrier heights obtained from the three methods were found to be consistent. The flatband barrier heights deduced from the reverse bias I-V and C-V data are also consistent, within experimental errors. The zero bias barrier heights obtained from forward bias I-V measurements are lower than the flatband barrier heights as they would be expected to be as a result of barrier lowering effects. The results listed in Table (4.4) show that our values for α are generally larger than those expected in the literature[8] for

other GaAs Schottky devices. The large value of α reflects the observed barrier lowering of the order of 0.1 V at zero bias. According to Eq. (4.19) the obtained values for α result from a relatively thick interfacial layer. However, due to the fact that ϵ_i was not known, a numerical value for δ could not be obtained.

The carrier concentrations obtained from the Hall effect measurements are seen to be consistent with those of the C-V measurements. Furthermore, the Hall mobilities obtained are consistent with those reported in the literature for similar material[27].

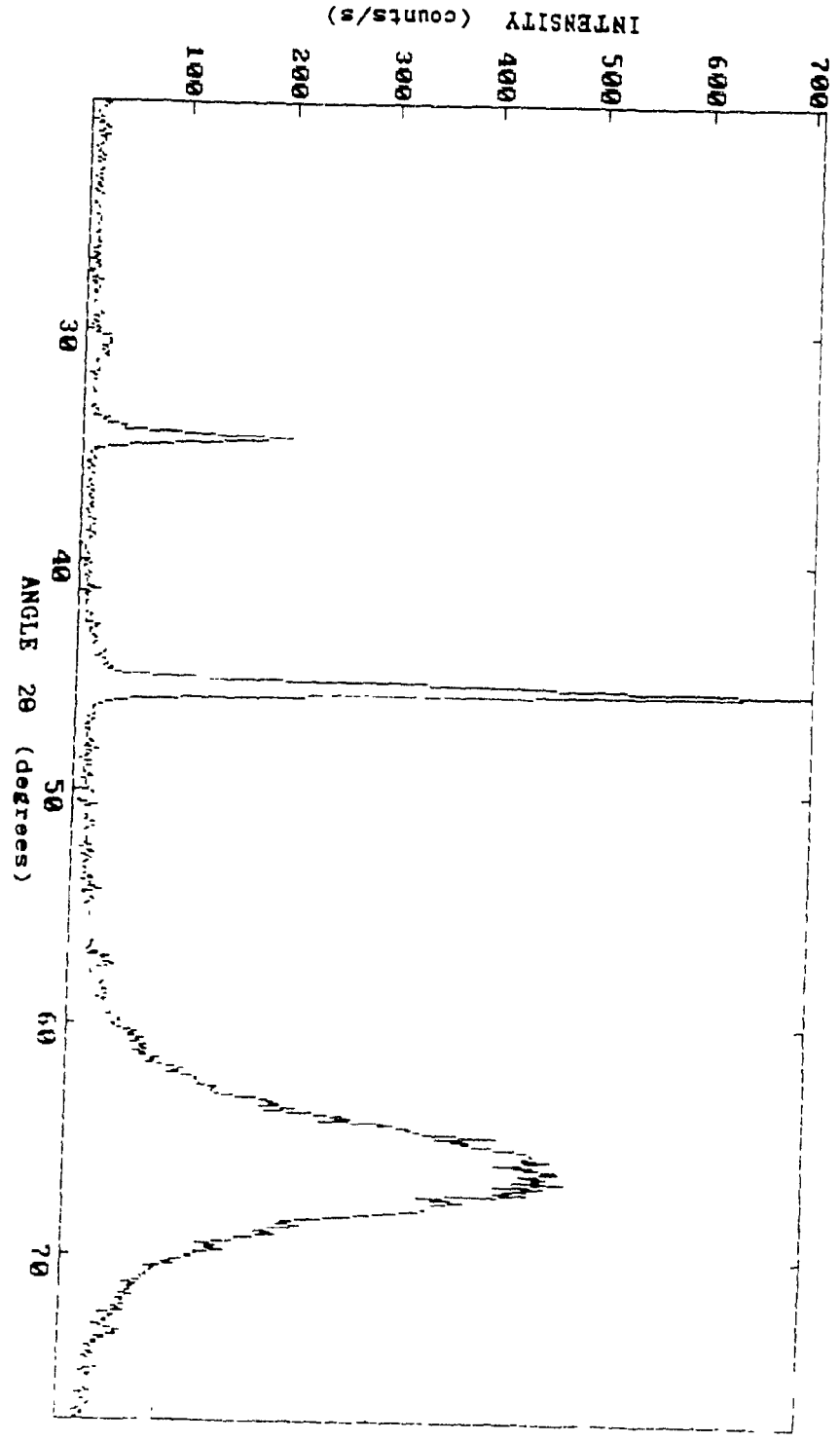


Fig. (4.3). X-ray data for iron grown on GaAs.

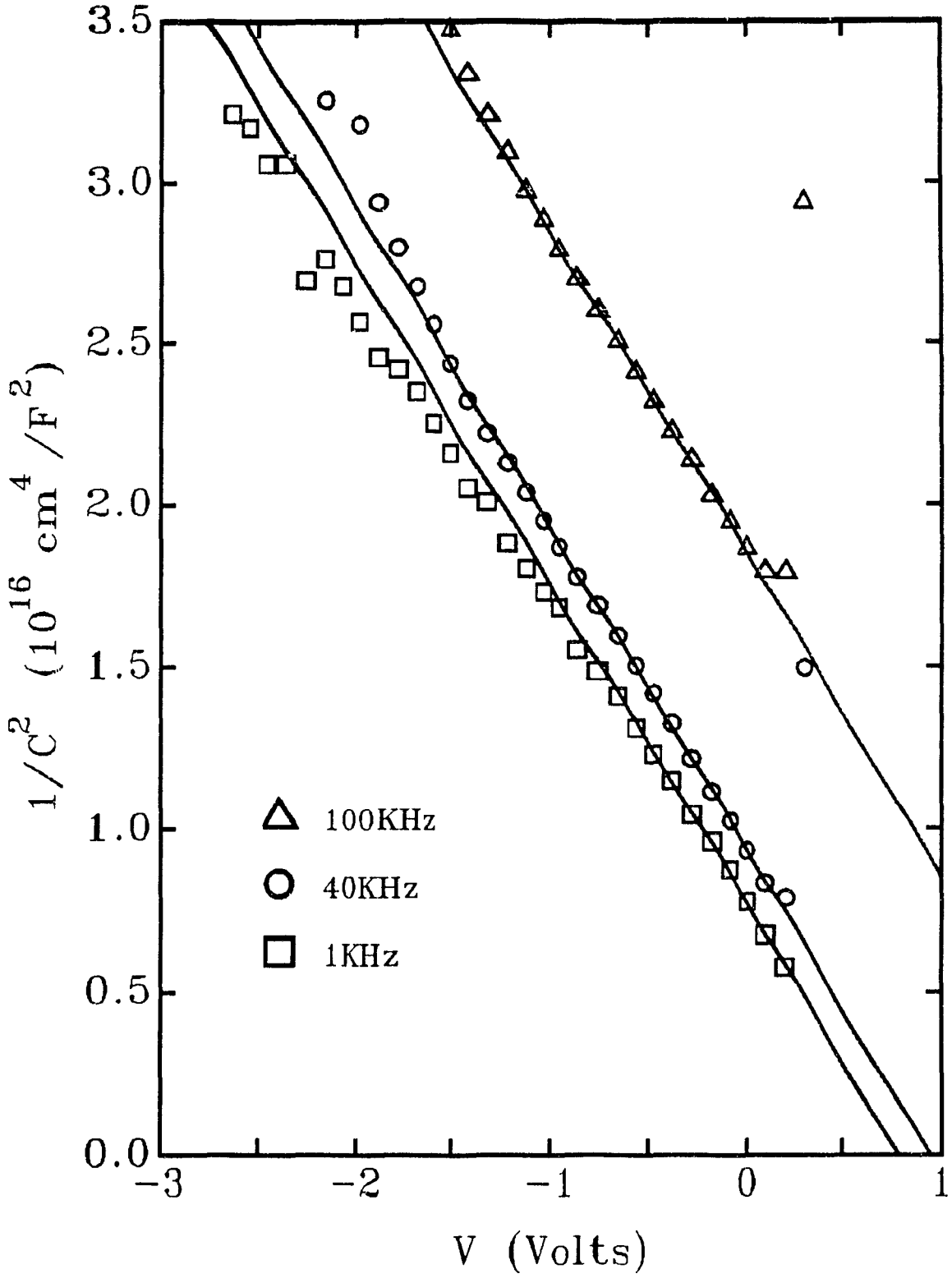


Fig. (4.4). $1/C^2$ vs. V plot for device M6.2.

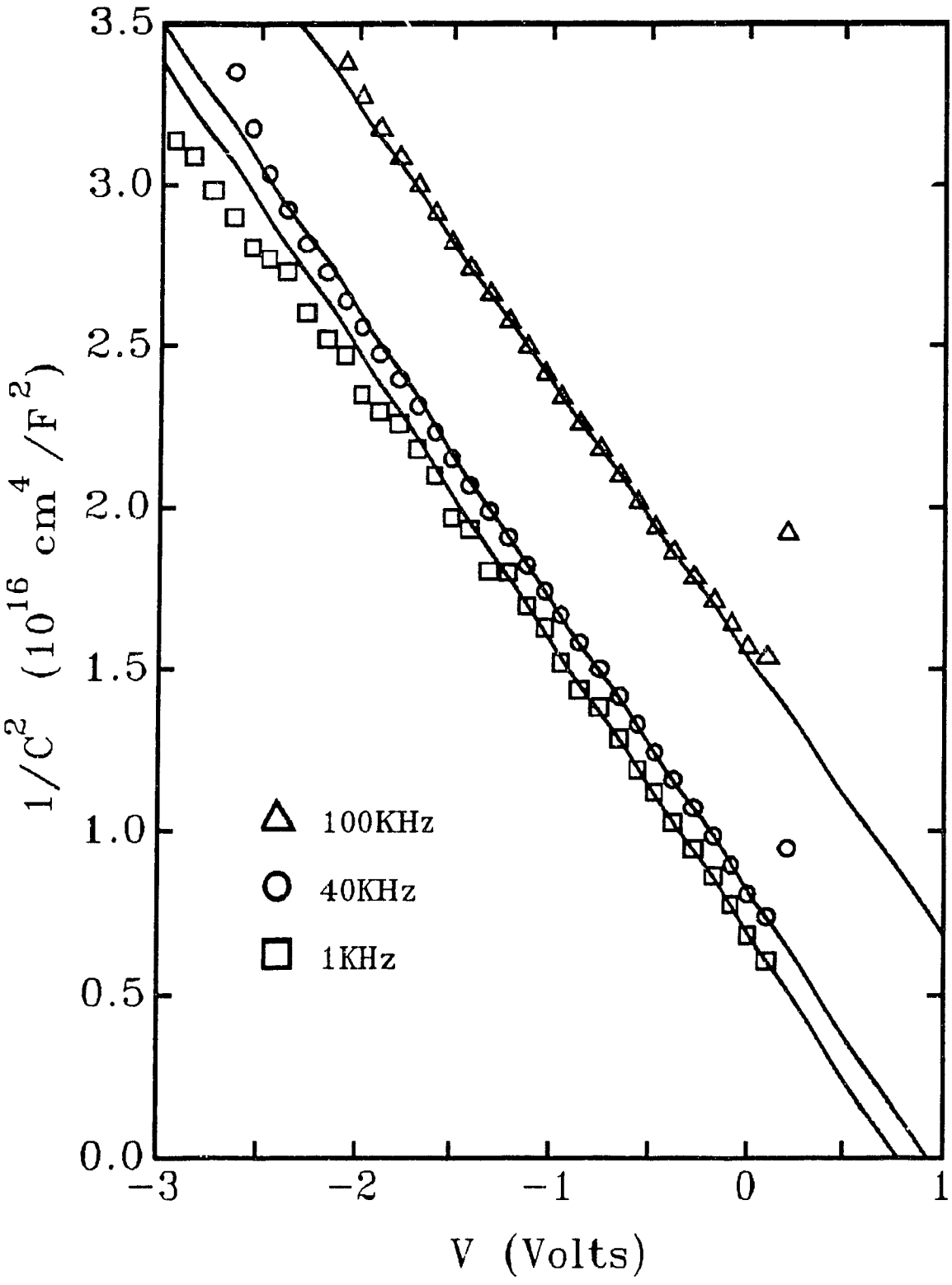


Fig. (4.5). $1/C^2$ vs. V plot for device M6.9.

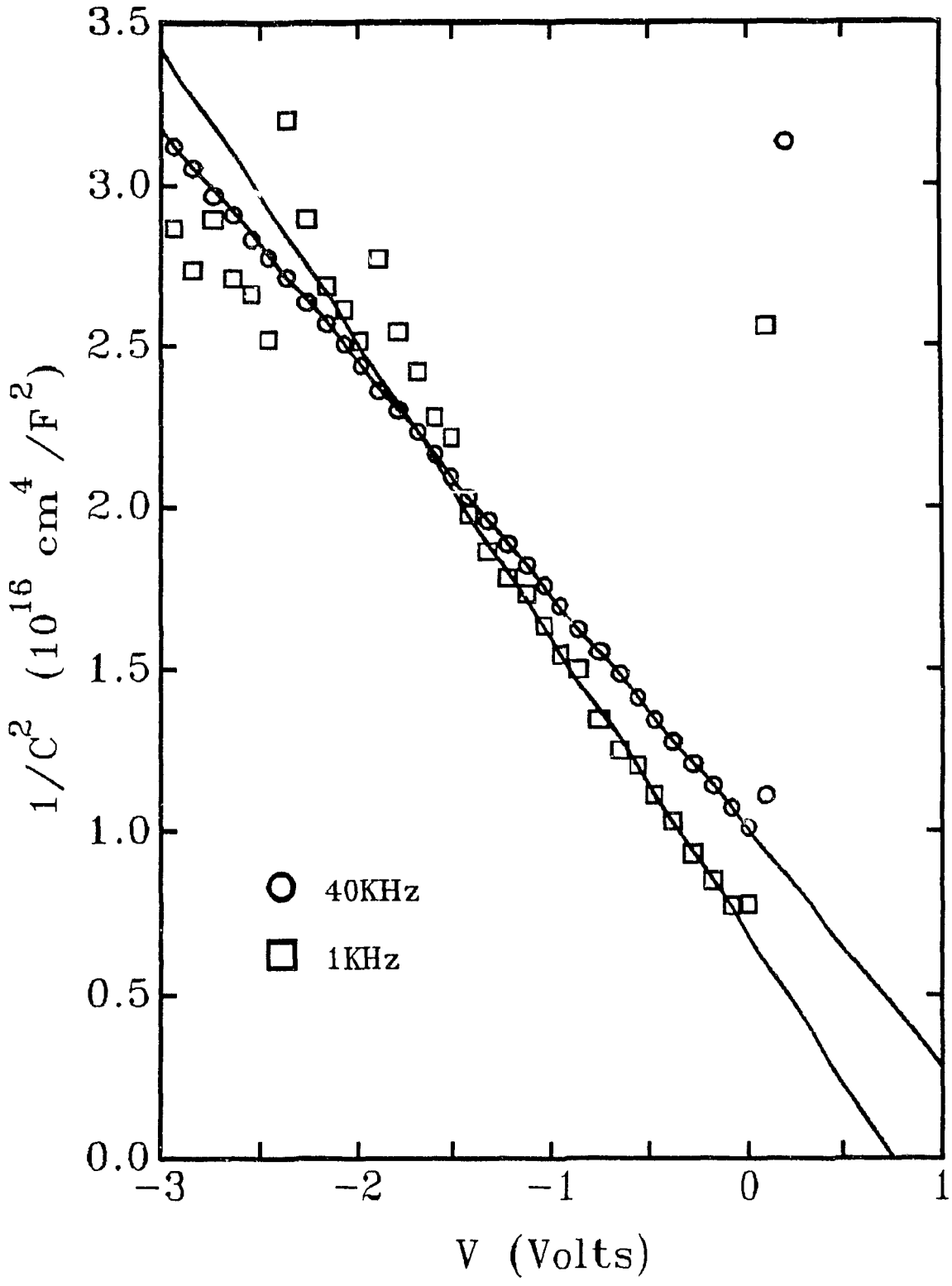


Fig. (4.6). $1/C^2$ vs. V plot for device M6.10.

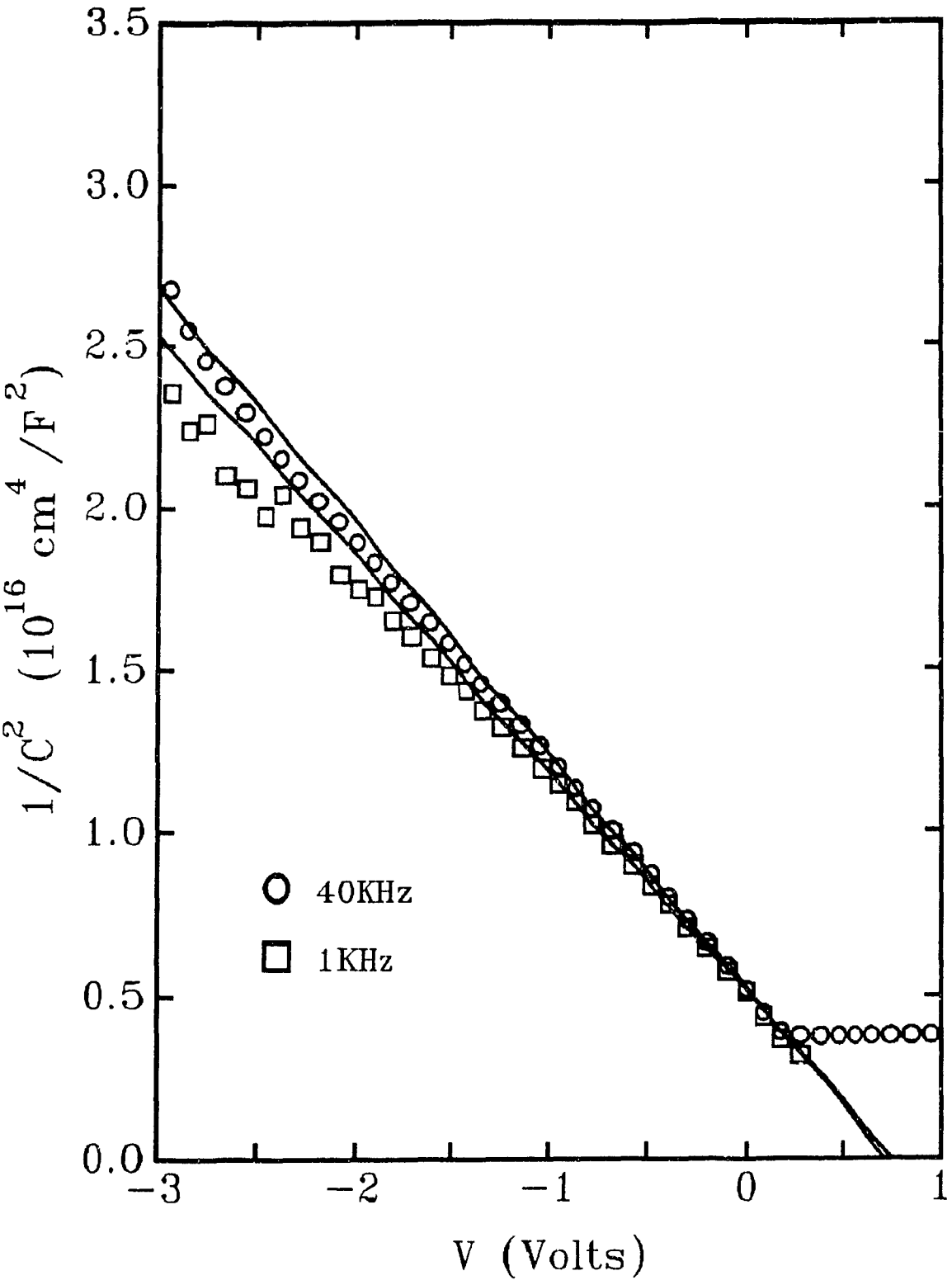


Fig. (4.7). $1/C^2$ vs. V plot for device MA6.1.

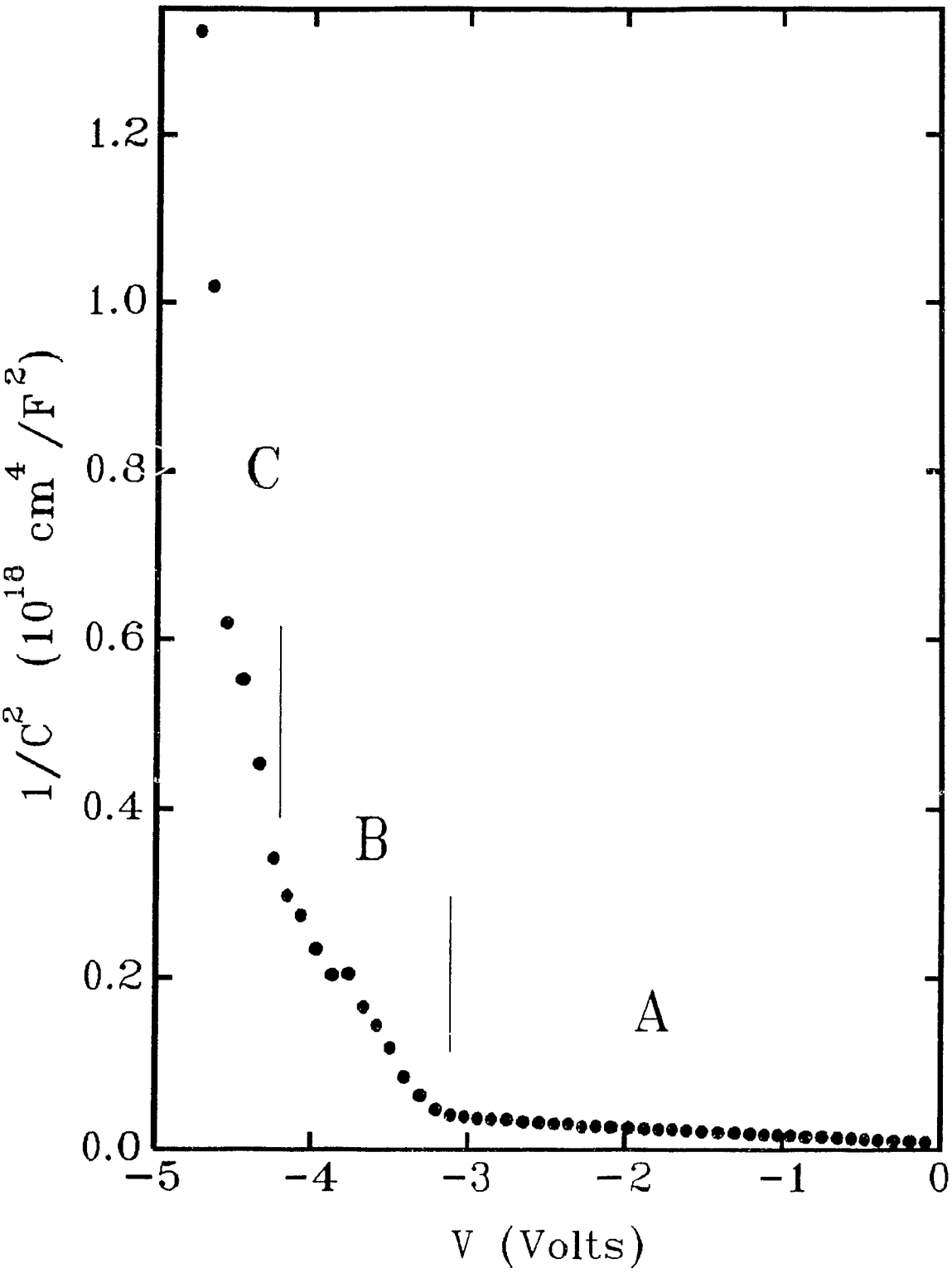


Fig. (4.8). 1/C2 vs. V plot showing the GaAs epilayer structure. The regions A, B and C show the active epilayer, the buffer layer and the substrate, respectively.

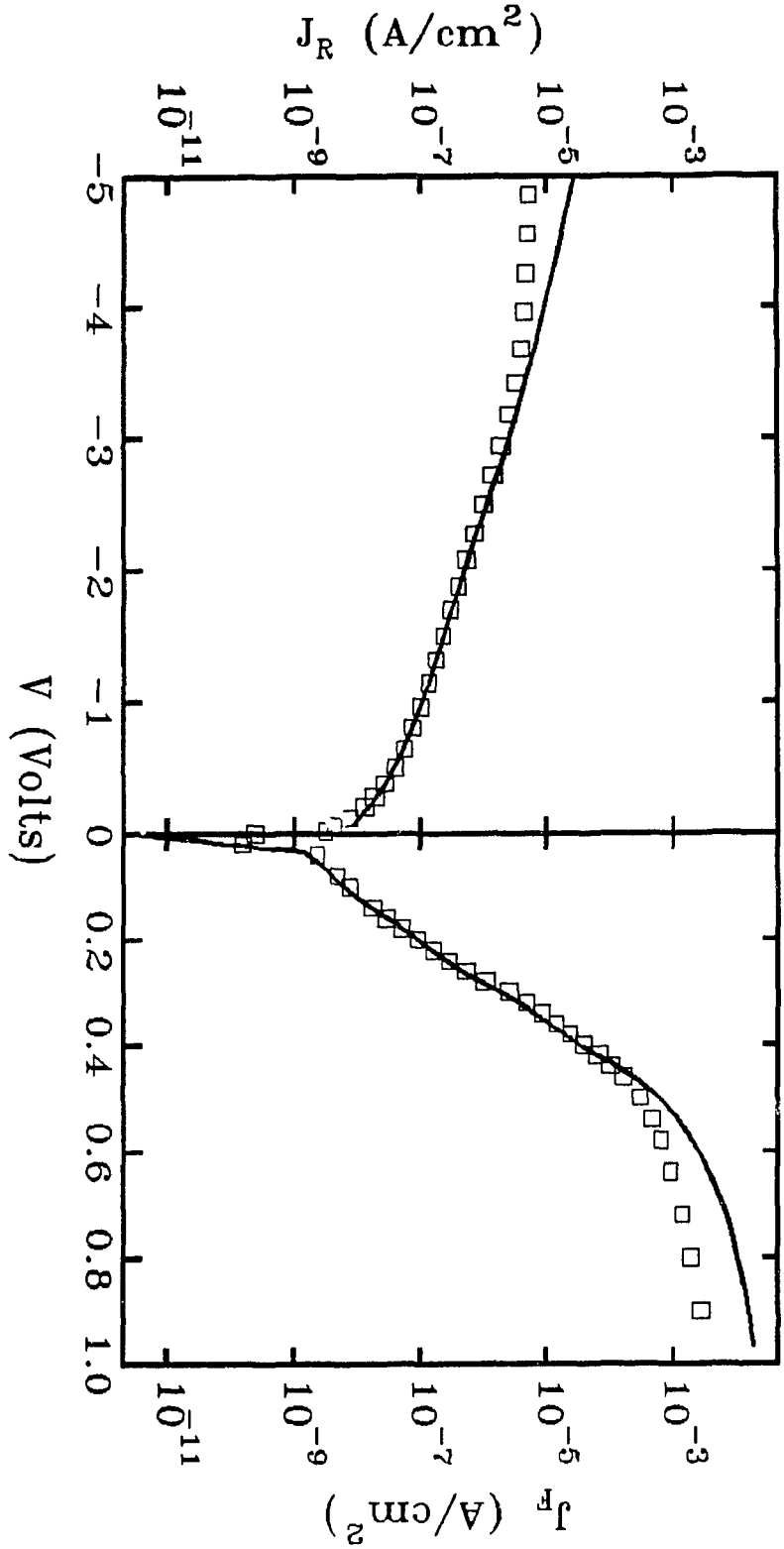


Fig. (4.9). I-V plot for device M6.2. The continuous line is the fit.

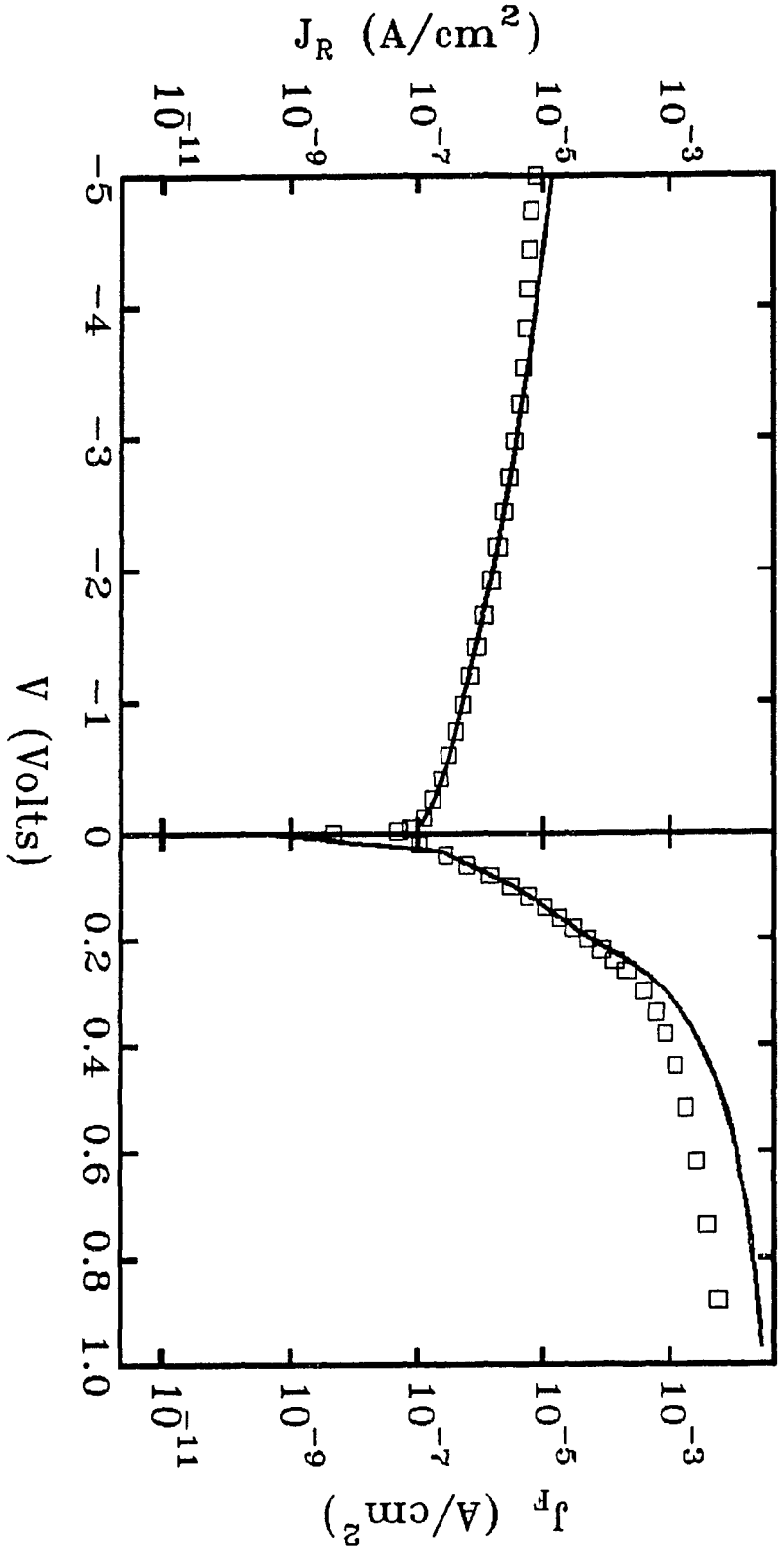


Fig. (4.10). I-V plot for device M6.9. The continuous line is the fit.

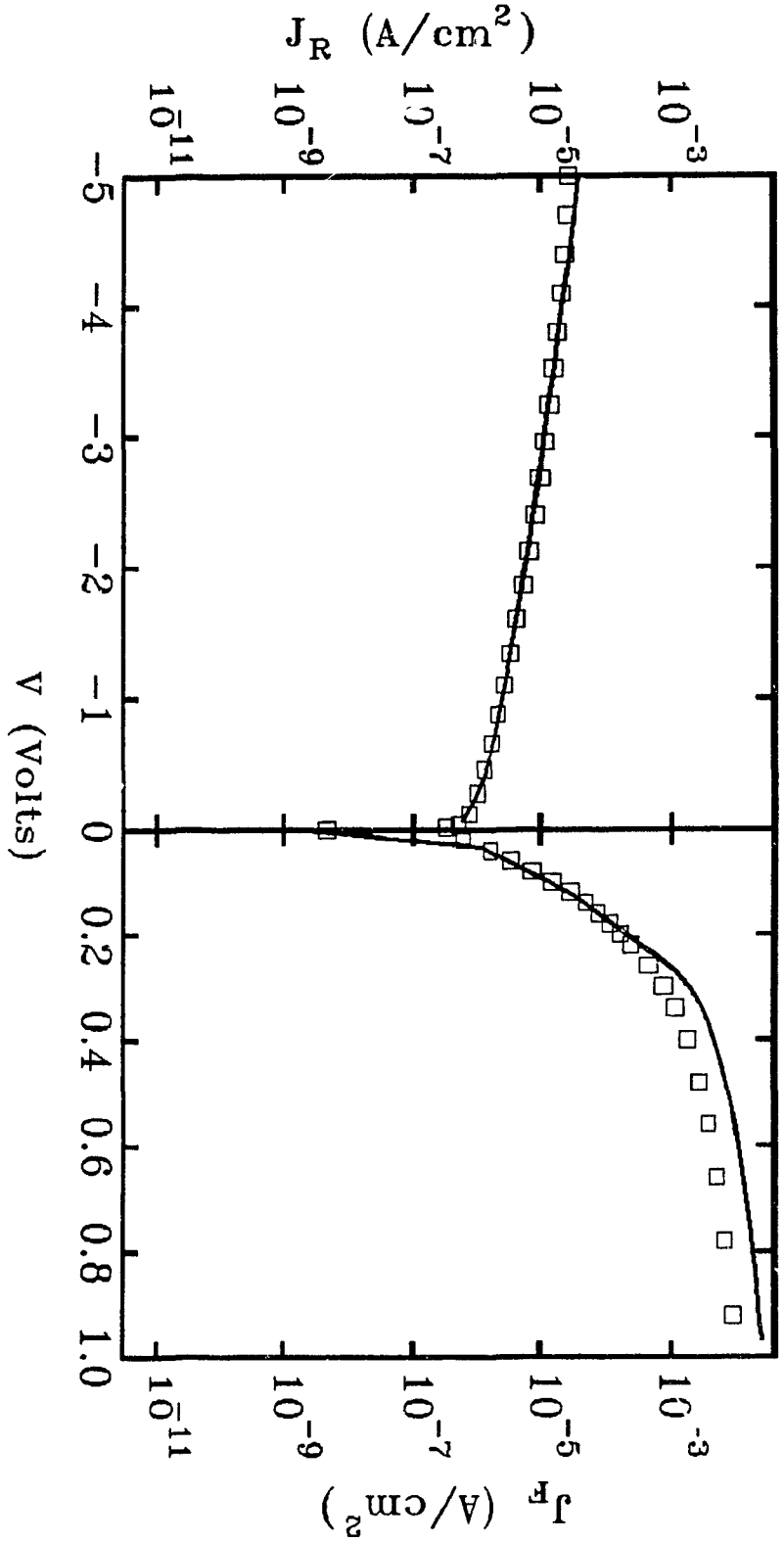


Fig. (4.11). I-V plot for device M6.10. The continuous line is the fit.

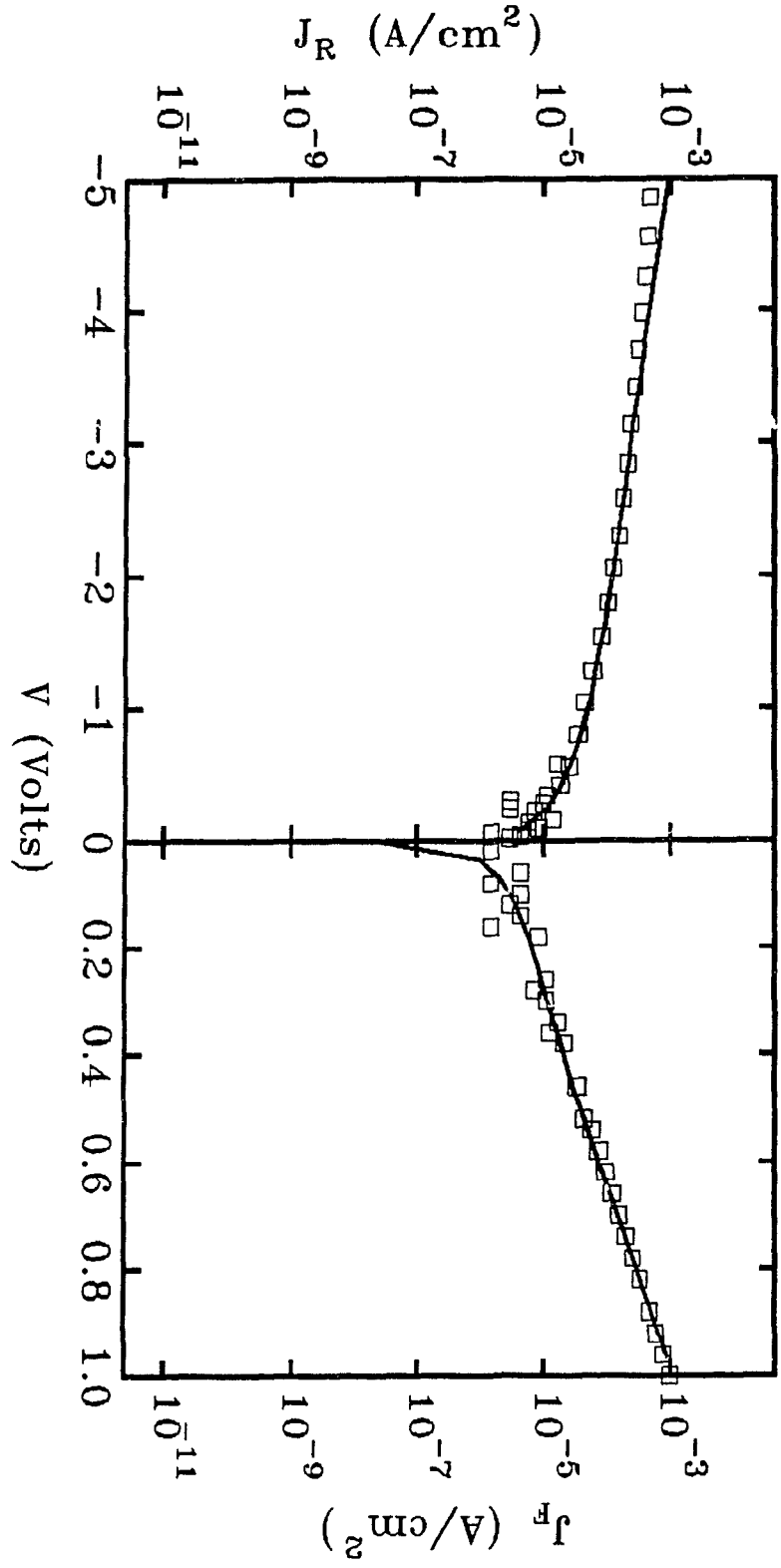


Fig. (4.12). I-V plot for device MF9.18. The continuous line is the fit.

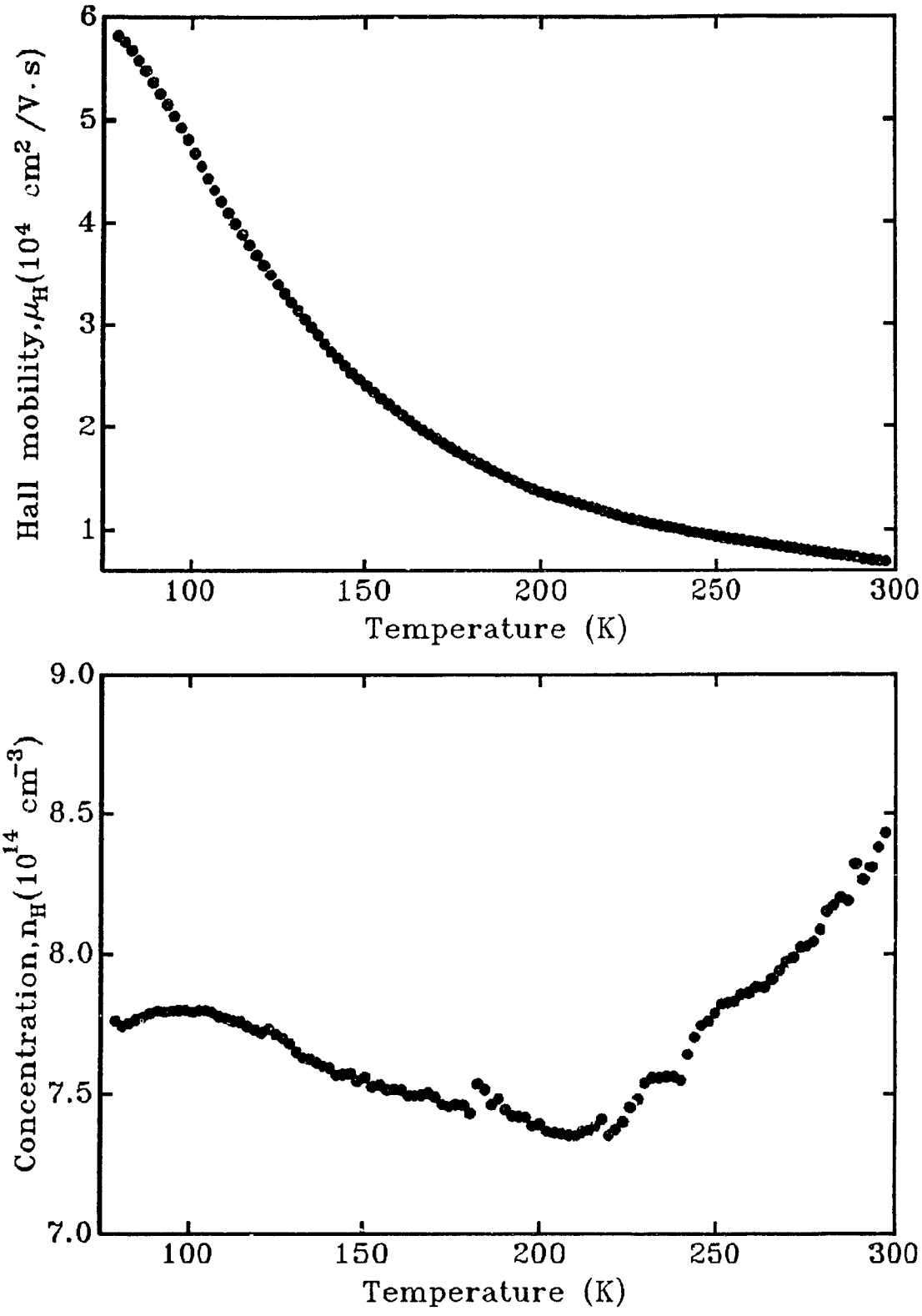


Fig. (4.13). Hall mobility and concentration for the M6 GaAs epilayer.

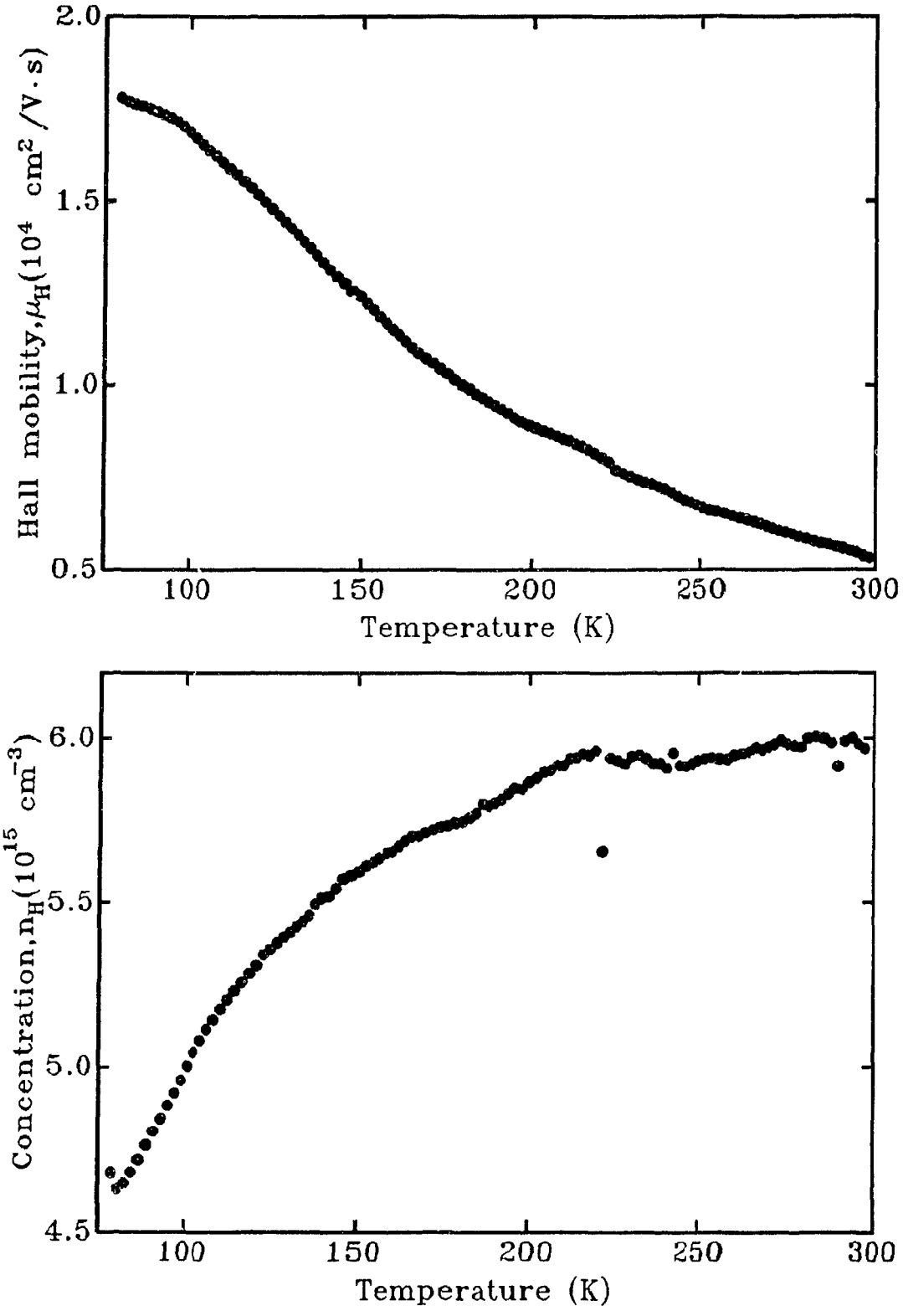


Fig. (4.14). Hall mobility and concentration for the M9 GaAs epilayer.

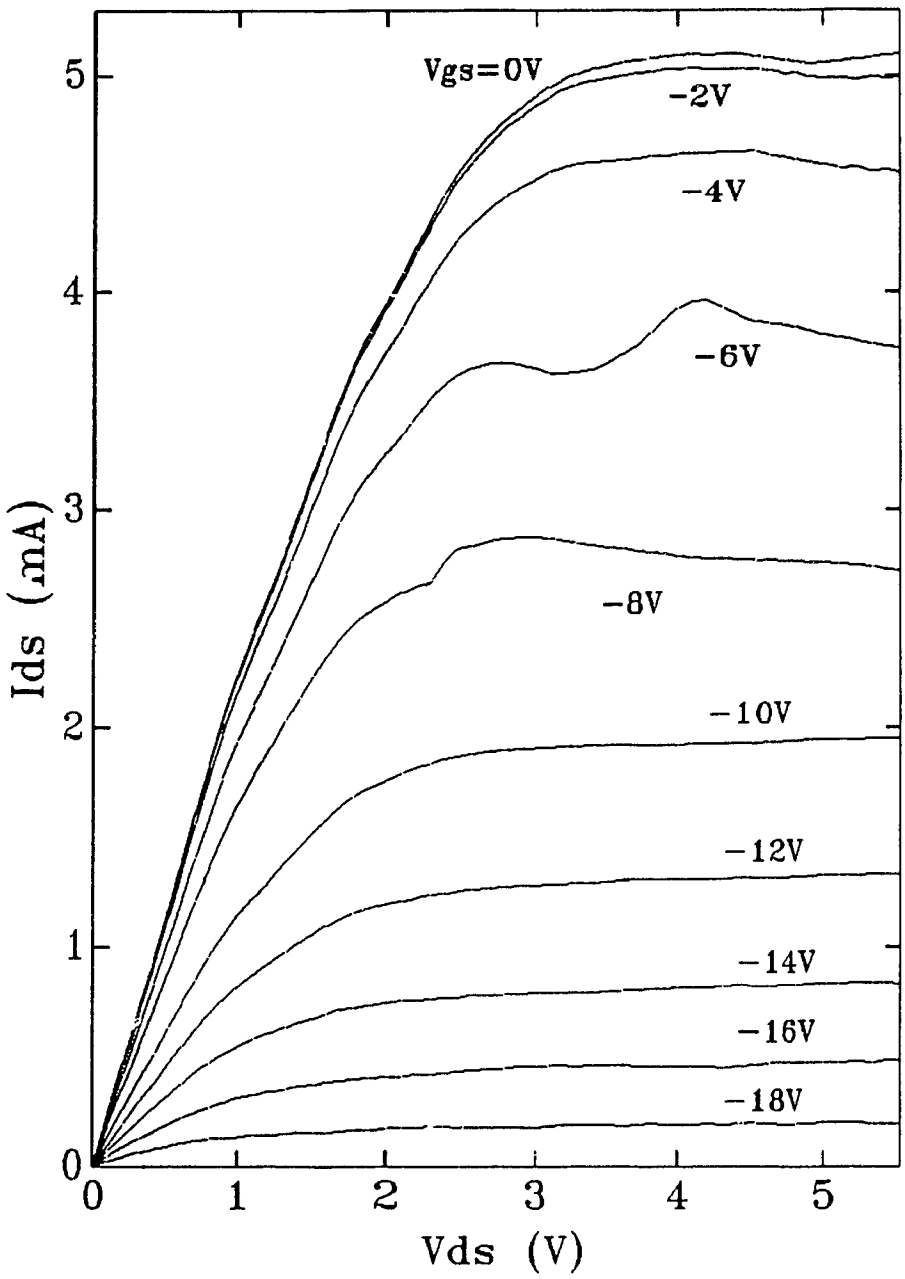


Fig. (4.15). The drain-source I-V data for the MF6.36 iron gate MESFET.

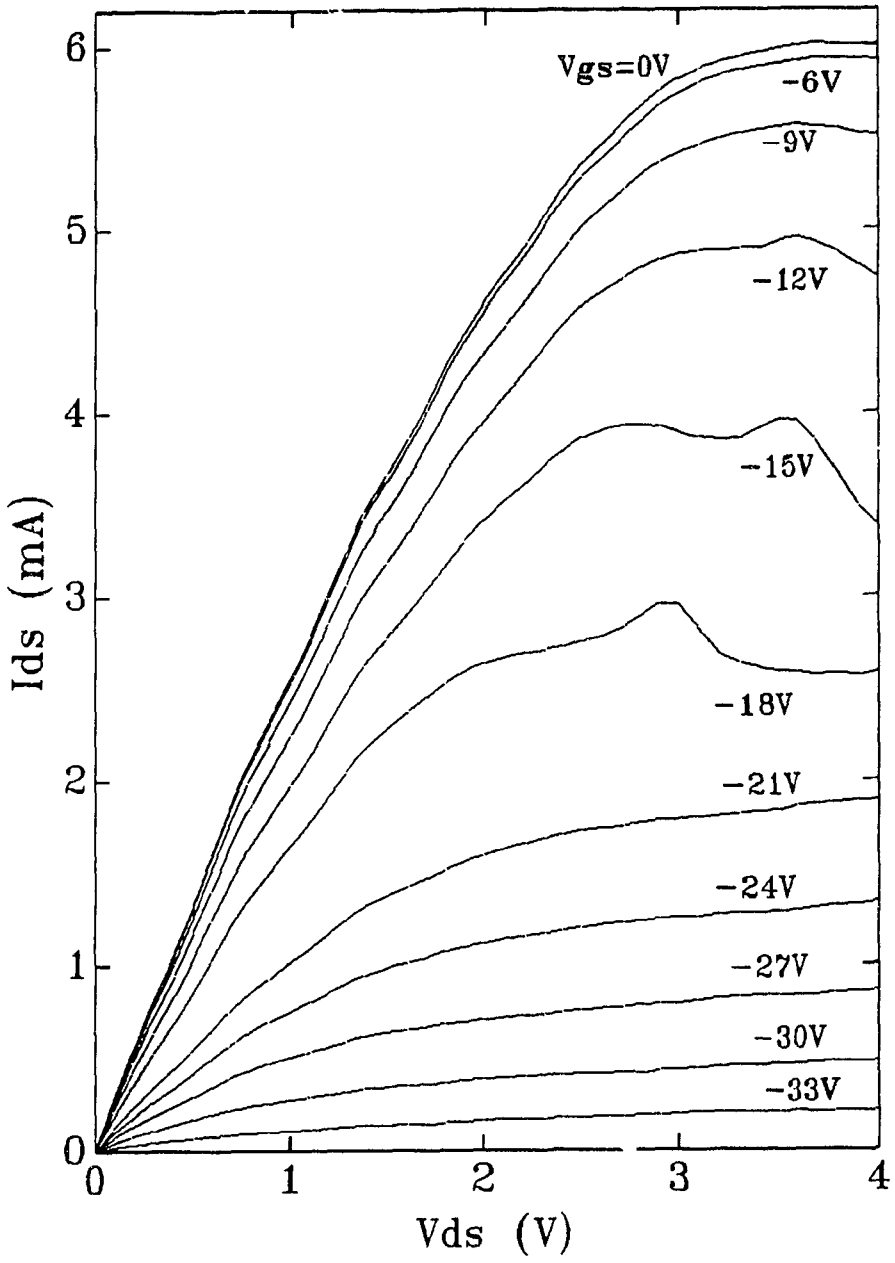


Fig. (4.16). The drain-source I-V data for the MF9.18 iron gate MESFET.

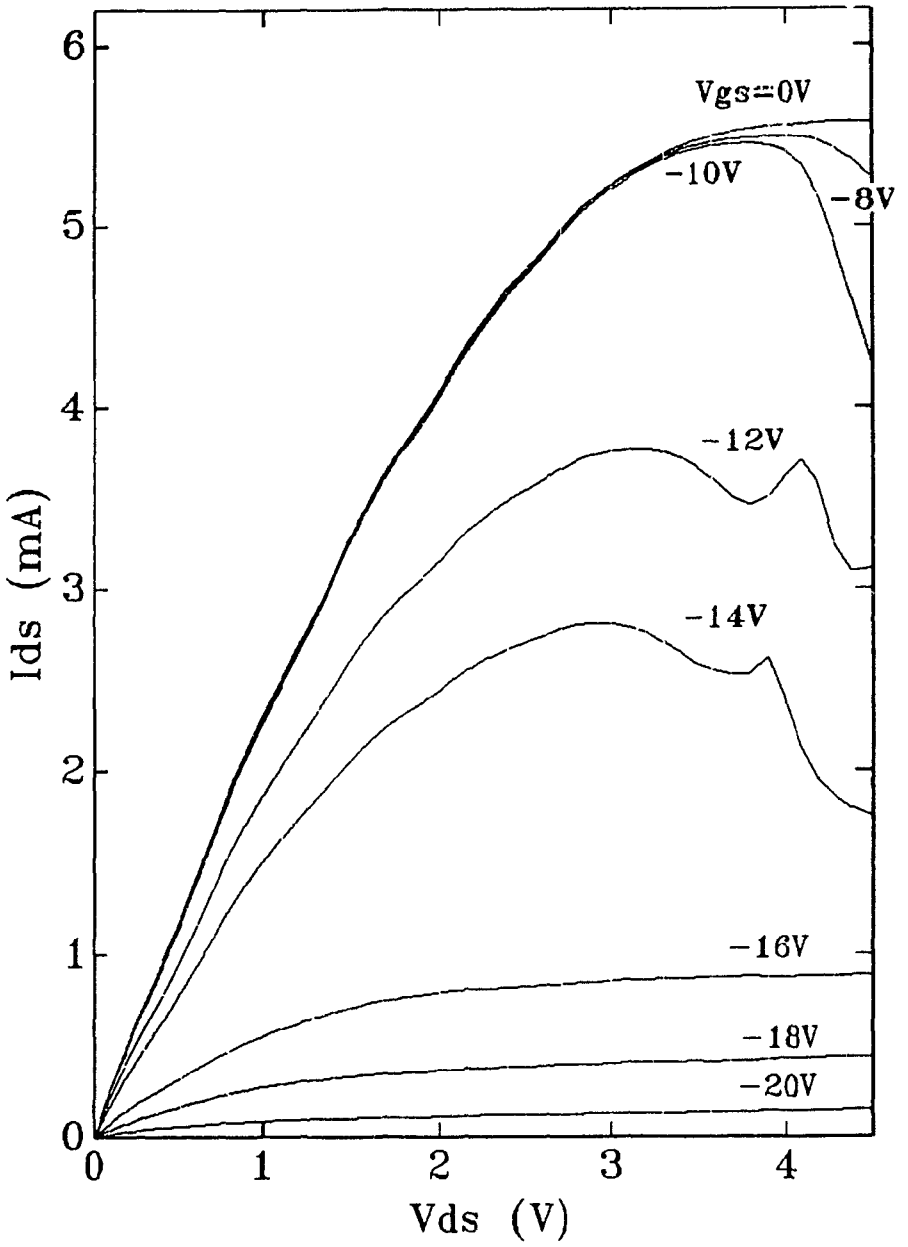


Fig. (4.17). The drain-source I-V data for the MF9.21 iron gate MESFET.

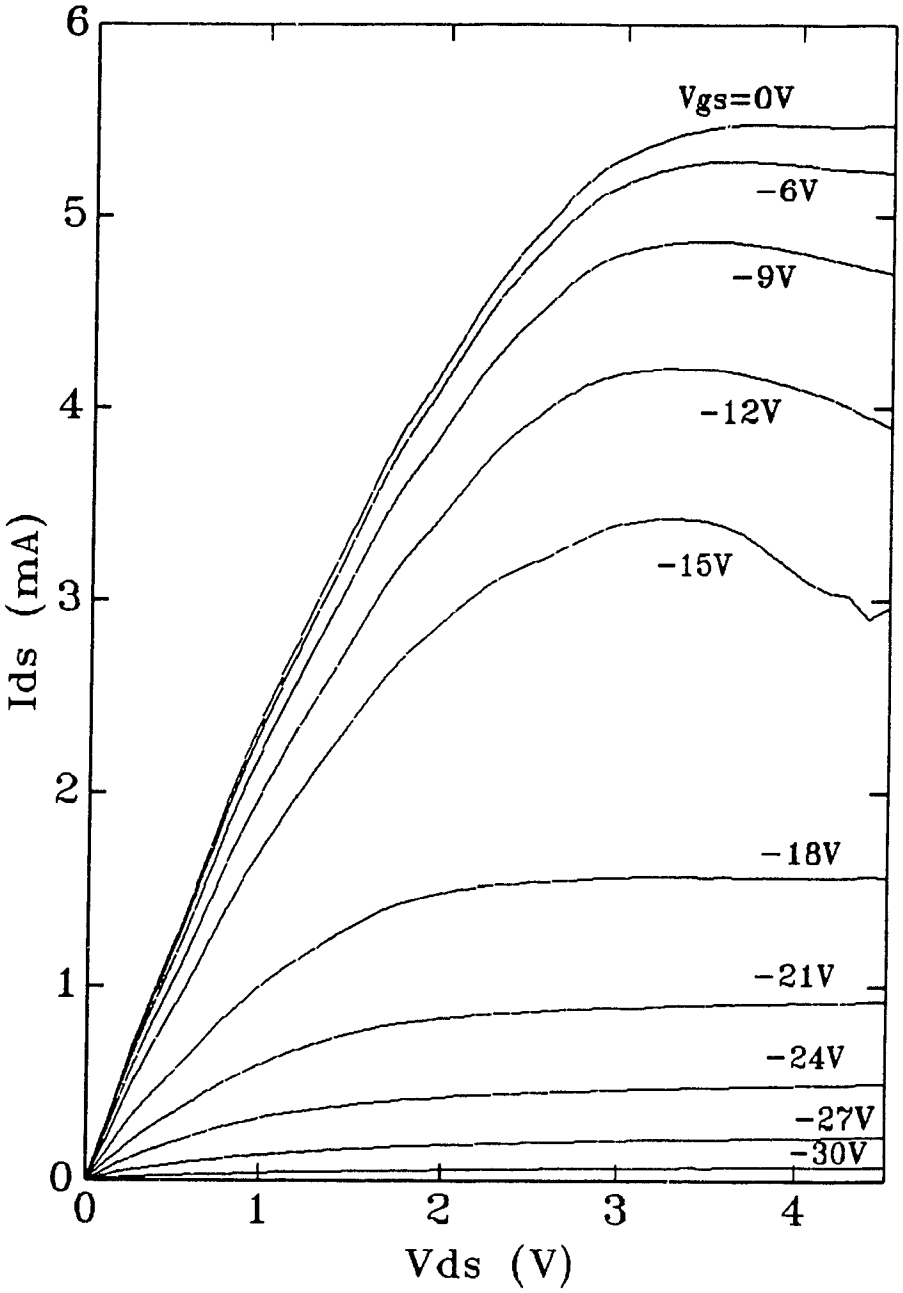


Fig. (4.18). The drain-source I-V data for the MF9.26 iron gate MESFET.

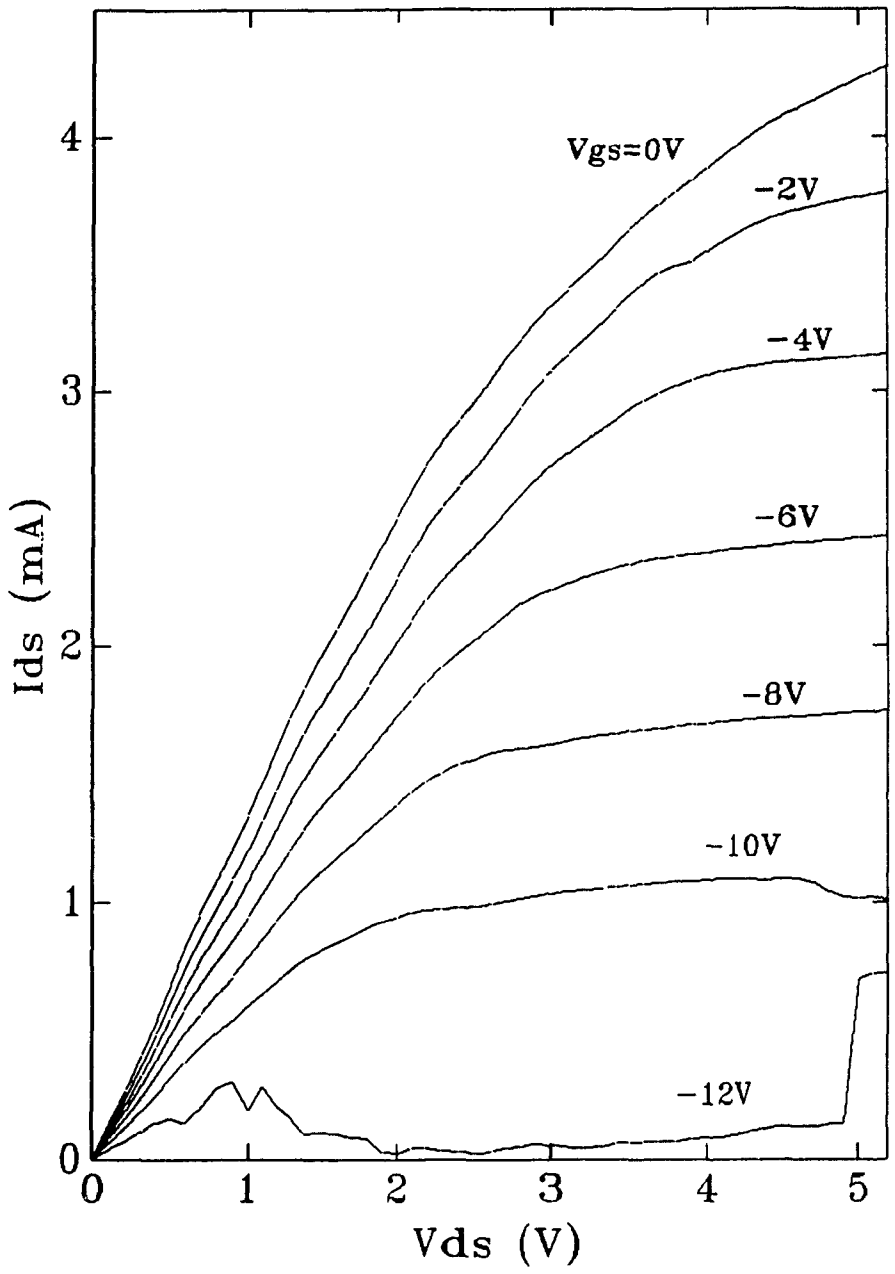


Fig. (4.19). The drain-source I-V data for the MAF9.11 aluminium gate MESFET.

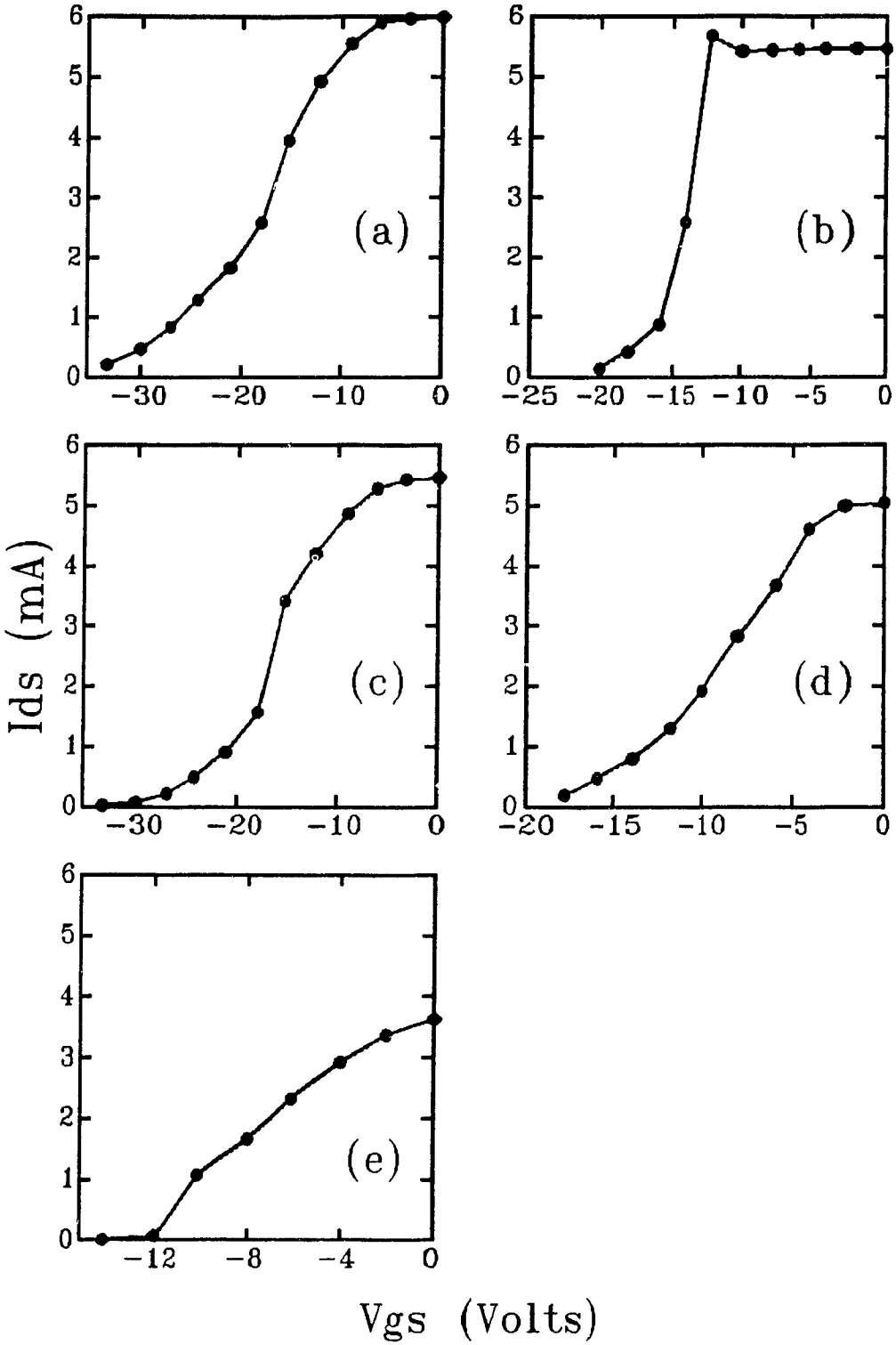


Fig. (4.20). The drain-source current versus gate voltage transfer characteristics for the MESFET devices fabricated: (a) MF9.18, (b) MF9.21, (c) MF9.26, (d) MF6.36 and (e) MAF9.11 (Al gate).

CHAPTER 5

CONCLUSIONS

The consistency of the results of our experiments with different samples or iron Schottky junctions on GaAs show that the iron MOCVD technology developed in this work is a viable method for the fabrication of GaAs diodes and MESFETs.

The Schottky barrier was consistently found to be about 0.8 V. However, the large barrier lowering effect, under reverse bias, which we attribute to a relatively thick interfacial layer, leads to an ideality factor of 1.27, which is somewhat high compared to the state of the art. One possible reason for this thick interfacial layer could be the carbon contamination in the deposited films which was considered in section 3.1.4. It is probable that this contamination problem could be palliated by the use of other iron based chemicals (metalorganics or others).

In the MESFETs fabricated by this novel technology, an interesting feature was the high reverse breakdown voltage. Additionally, the time dependent stability of the junction seems to be good as there was little or no change in the characteristics over a several week period. On the other hand, the presence of a thick interfacial layer may present problems for higher frequency applications, as suggested by the capacitance versus voltage characteristics.

Another problem encountered in the fabrication of the MESFETs remains the development of a satisfactory procedure for wet etching the iron film. Also as iron oxidises it would have to be overlaid by another protective material. Gold was used in our case.

A significant amount of this work concerns the development of a flexible MOCVD system and a versatile high impedance Hall effect measuring system. Both were shown to perform as planned.

APPENDICES

Appendix A. The Sequence Instruction Set.

The following is a list and description of the instruction keywords for MOCVD control unit sequence language.

1.BEEP

Causes the system to emit a audible beep.

2.BREAK

Usage: BREAK :label -- where label is the destination label. Upon pressing of the break key, if this statement has been executed, the program will jump to the destination label.

```
Example:  BREAK :END      ; initialize break.
                .         ; body of program.
                .
          END:            ; destination label.
          VALVE 10 OFF
```

3,4.DO and REPEAT

Usage: DO n -- where n is the number of iterations. This provides a do-repeat loop structure.

```
Example:  DO 15                ; turns valve 12 on, waits
               VALVE 12 ON     ; 10 seconds, and then turns
```

```
            WAIT 10          ; it off, 15 times.
            VALVE 12 OFF
        REPEAT
```

5.**FLOW**

Usage: FLOW n r -- where n in the flow controller number and r is the flow rate given as a percentage of the maximum. This is used to set the flow controllers.

6.**GOTO**

Usage: GOTO :label -- where label is the destination. Used to jump unconditionally to another point in the sequence.

```
Example:        GOTO :NEWL      ;bypass the section that
                                ;follows.
                    .
                    .
            :NEWL
```

7.**KEY**

Usage: KEY :label k -- label is the destination and k is the ASCII code of the interrupting key selected. This is similar to the BREAK instruction but allows the user to select the key.

8.**KLED**

Usage: KLED n state -- where n in the indicator light and

state is either ON or OFF.

This is used to turn a front panel status indicator light on or off.

9.**PAUSE**

Usage: This is used to pause the system until the user restarts it by pressing an appropriate break key.

10.**TEMP**

Usage: TEMP n t w -- where n is the heater number, t is the set temperature and w is either WAIT or NOWAIT. The w is used to tell the system to wait on not for the set temperature to be reached. This is used to set the heater controller.

11.**TIMER**

Usage: TIMER n s -- where n is the timer number and s is either ON or OFF. There are two on screen general purpose timers that can be turned on or off during execution of a sequence.

12.**VALVE**

Usage: VALVE n s -- where n id the valve number and s is either ON or OFF. This is used to control the valves in the system.

13.**WAIT**

Usage: WAIT t -- where t is a time in seconds. This is used to create a delay.

Appendix B. Photolithographic techniques.

B.1. The Photolithographic Lift-off Technique.

Selective metallization is used extensively in device fabrication. In Si technology this is mostly done by depositing metal over the surface of the wafer and etching away the unwanted regions. In GaAs, the problems are different; nearly all etchants that are used for metals, commonly used in GaAs technology, also etch GaAs. This makes wet etching unreliable and mostly unsuitable. This problem is avoided by using the lift-off method which involves no etching. The idea is to place photoresist selectively using photolithography before deposition of the metal. The metal that is then deposited over the photoresist, is removed along with the photoresist underneath it. This process has a complication however; the photoresist edge must be sharp, and

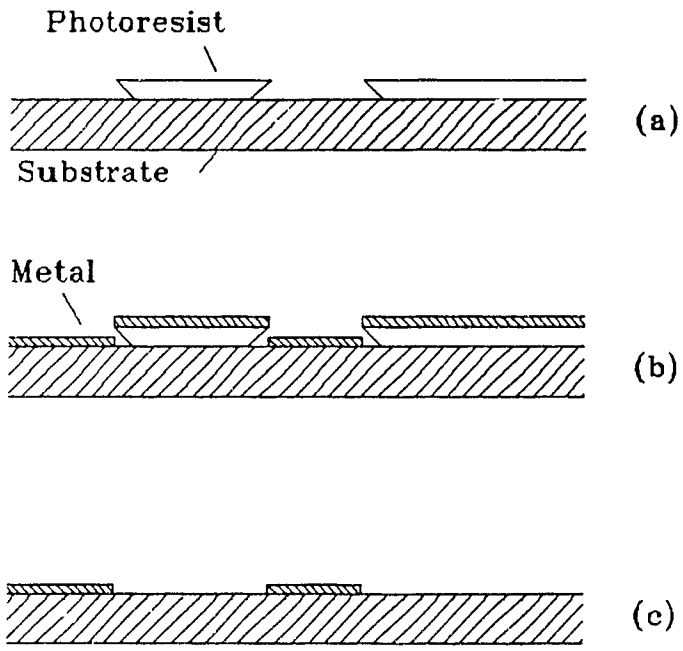


Fig. (B.1). The lift-off technique. (a) The applied photoresist. (b) After metallization. (c) After lift-off.

preferably undercutting, as seen in fig. (*b*.1). This type of edge can be achieved by soaking the photoresist prior to exposure, in chlorobenzene. Chlorobenzene has the effect of retarding the developing at the photoresist surface while letting the developing below the surface occurs at the normal rate. The procedure followed is summarized below.

---

1. Spin Shiply 1435J photoresist on wafer at 4000 rpm for 25 sec.
2. Prebake the photoresist at 90°C for 25 min.
3. Let wafer cool and then soak it in chlorobenzene for 5 min.
4. Spin dry the wafer immediately, and then let it dry in oven at 75°C for 2 min.
5. Expose to U.V. light in a mask aligner for 1.5 min. (Kaspar Inc. mask aligner).
6. Develop the photoresist in a developing solution (1 H2O: 1 Shiply MF-312 developer) for 50 sec. at 23°C.
7. Rinse the wafer in water.
8. Evaporate the metal desired.
9. Soak the wafer in acetone to lift off metal and wash away photoresist.
10. Rinse the wafer in water.

B.2. Photoresist for Standard Selective Wet Etching.

Photolithography for selective wet etching follows a standard procedure as given below.

---

1. Spin Shiply 1435J photoresist on wafer at 4000 rpm for 25 sec.
2. Prebake the photoresist at 90°C for 25 min.
3. Expose to U.V. light in a mask aligner for 50 sec. (Kaspar Inc. mask aligner).
4. Develop the photoresist in a developing solution (1 H2O: 1 Shiply MF-312 developer) for 1 min. at 23°C.
5. Rinse the wafer in water.
6. Postbake the photoresist at 120°C for 10 min.
7. Follow desired etching procedure.
8. Wash off the photoresist in acetone.
9. Rinse the wafer in water.

Appendix C. Sample cleaning and degreasing.

The standard procedure for cleaning and degreasing sample prior to processing is given below.

---

1. Place the sample in boiling trichloroethylene for 5 min.
2. Place the sample in boiling acetone for 5 min.
3. Rinse the wafer in propanol.
4. Rinse the wafer in deionized water of resistivity greater than $10^{15}\Omega$.

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