State Space Modelling of the Fuzz Face Guitar Pedal

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Abstract

Many of music's most beloved sounds and recordings were created using equipment now considered to be vintage. This vintage equipment is coveted by musicians and music enthusiasts for their perceived-superior sound quality. In the world of electric guitar pedals, few pedals are more revered than the Fuzz Face - a distortion pedal made famous by players like Jimi Hendrix. While sought after, the Fuzz face uses now-obsolete Germanium Bipolar Junction Transistors ("GBJTs"), which are failure-prone, fluctuate with temperature, and inconsistently manufactured.

To circumvent these issues, many researchers and industry engineers have focused their efforts on replicating the sound and behaviour of vintage audio circuits, like the fuzz face, using digital modelling techniques. These models are inherently low-cost, reproducible, and consistent. This field of research is referred to as Virtual Analog ("VA").

Within VA, there are several approaches to creating a digital model. One such technique is called "State space Modelling". It takes a very circuit-based approach, allowing each component within a circuit to be modelled individually, offering the designer a high degree of accuracy on a low-level. This technique lends itself well to circuits like the fuzz face, whose characteristics are largely determined by their two GBJTs.

A brief overview of the Bipolar Junction Transistor ("BJT"), its relevance to audio circuits, and some popular BJT macro-models are presented. A review of relevant VA research, with emphasis on state space modelling, is also given. The formation and simulation of an audio circuit's state space model is introduced in the context of a case study on the common-emitter amplifier, with considerations given to initial state conditions and the use of an iterative solver.

Finally, research on modelling the Fuzz Face circuit, and GBJTs, is presented. A scheme for measuring GBJTs using low-cost, general-use lab equipment is presented, followed by parameter optimization to match the behaviour of a BJT macro-model to the measured data. State space models of the Fuzz Face are then constructed using both the Ebers-Moll and Gummel-Poon models, and their behaviour is compared by examining their output waveforms, frequency spectra, computational cost, and audio quality.

Résumé

De nombreux sons et enregistrements musicaux ont été créé sur des équipements désormais considéré comme vintage. Ces équipements vénérables sont convoités par les musiciens et les passionnés de musique pour leur qualité sonore perçue comme supérieure. Parmi les pédales pour guitare électrique, peu sont plus révérées que la pédale Fuzz Face – une pédale de distorsion devenue célèbre grâce à des utilisateurs tels que Jimi Hendrix. Bien que recherché, La Fuzz Face utilise des transistors obsolètes de type bipolaires au Germanium (GBJT), enclins aux pannes, fluctuant avec la température, et de fabrication inégale.

Pour pallier ces problèmes, de nombreux chercheurs et ingénieurs ont concentré leurs efforts sur la simulation par modélisation numérique des sons et des comportements des circuits audio, tels que ceux de la Fuzz Face. Ces modèles sont par nature à faible coût, reproductibles et de qualité constante. Ce domaine de recherche est connu sous la dénomination d'analogues virtuels (AV).

Il y a plusieurs approches pour élaborer un modèle numérique selon l'approche AV. L'une d'entre elles, appelée "Modélisation en variables d'état (VE)" se fonde sur le circuit électronique lui-même, permettant à chacun de ces composants, linéaire ou non, d'être modélisé individuellement. Cela offre aux concepteurs un haut niveau de fidélité à un bas niveau électronique. Cette technique est appropriée à la modélisation de la pédale Fuzz Face, dont le comportement est hautement non-linéaire, en raison des caractéristiques de ces deux transistors GBJT. Un bref aperçu des transistors GBJT, de leur pertinence dans le cadre de l'audio, et de macro-modèles de GBJT est dressé. Suit un état de l'art de la recherche en AV, et notamment sur l'approche en (VE). Une étude de cas de modélisation en VE du circuit audio d'amplification à émetteur commun est ensuite présentée. Ce modèle prend en compte les conditions initiales et fait appel à un solveur itératif en raison de la non-linéarité des GBJT.

Finalement notre recherche sur la modélisation de la pédale Fuzz Face et des GBJT est présentée. Une stratégie de mesure des GBJT avec des équipements de laboratoire standard et à faible-coût est présentée puis mise en œuvre. Suit une procédure d'optimisation non-linéaire, qui estime les paramètres du macro-modèle de GBJT à partir de données mesurées. Les modèles en VE de la pédale Fuzz Face sont alors construits pour les modèles d'Ebers-Moll et de Gummel-Poon. Leur comportement est examiné en termes de formes d'ondes, de spectres, de coûts engendrés, et de qualité audio.

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List of Acronyms

AC	Alternating Current
ACME.jl	Analog Circuit Modeling and Emulation for Julia
BJT	Bipolar Junction Transistor
CBJ	Collector-Base Junction
CCCS	Current-Controlled Current Source
CCS	Constant Current Source
DAW	Digital Audio Workstation
DC	Direct Current
DE	Differential Evolution
DIY	Do-It-Yourself
DMM	Digital Multi-Meter
DUT	Device Under Test
EBJ	Emitter-Base Junction
EM	Ebers-Moll

FET	Field Effect Transistor
GBJT	Germanium Bipolar Junction Transistor
IC	Integrated Circuit
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LTI	Linear, Time-Invariant
MNA	Modified Nodal Analysis
NDK method	Nodal Discrete-Kirchhoff method
NSI	Non-Linear System Identification
ODE	Ordinary Differential Equation
OTA	Operation Transconductance Amplifier
PHS	Port-Hamiltonian Systems
PWM	Pulse-Width Modulation
RF	Radio Frequency
SGP	SPICE Gummel-Poon

SPICE	Simulation Program with Integrated Circuit Emphasis
STFT	Short-Time Fourier Transform
VA	Virtual Analog
VBIC	Vertical Bipolar Inter-Company
VCCS	Voltage-Controlled Current Source
VCVS	Voltage-Controlled Voltage Source
WDF	Wave Digital Filter

List of Notation

$\boldsymbol{X}$	Matrices are denoted by a bold, upper-case letter
$\boldsymbol{x}$	Vectors are denoted by a bold, lower-case letter
v_X	Total voltage at node X, with respect to the reference node (ground)
V_X	DC voltage at node X, with respect to the reference node (ground)
v_x	Signal voltage at node X, with respect to the reference node
v_{XY}	Total voltage difference between node Y and node X
V_{XY}	DC voltage difference between node Y and node X
v_{xy}	Signal voltage difference between node Y and node X
i_X	Total current flowing through element X
I_X	DC current flowing through element X
i_x	Signal current flowing through element X
i_{XY}	Total current flowing from node X to Y
I_{XY}	DC current flowing from node X to Y
i_{xy}	Signal current flowing from node X to Y

List of Symbols

k	Boltzmann constant
q	Charge of a single electron
V_{CC}	DC voltage from a power supply
V_{EE}	DC voltage from a power supply
V_t	Thermal voltage
I_S	Saturation current of the BJT
β	Current gain of the BJT
g_m	Transconductance of the BJT
r_π	The resistance of the emitter-base junction of the BJT in the hybrid-π small signal model
r_e	The resistance of the emitter-base junction of the BJT in the T small signal model
A_v	Voltage gain of an amplifier
i_f	Total forward current of the BJT
i_r	Total reverse current of the BJT
i_{CC}	Total dominant current-component of the BJT
β_f	Forward current gain of the BJT
β_r	Reverse current gain of the BJT
N_f	Forward nonideality factor of the BJT
N_r	Reverse nonideality factor of the BJT

V_{af}	Forward early voltage of the BJT
V_{ar}	Reverse early voltage of the BJT
I_{kf}	Forward knee current of the BJT
I_{kr}	Reverse knee current of the BJT
I_{SE}	Emitter leakage current coefficient
I_{SC}	Collector leakage current coefficient
N_E	Emitter leakage nonideality factor
N_C	Collector leakage nonideality factor
r_B	Base terminal resistance of the SGP BJT model
r_E	Emitter terminal resistance of the SGP BJT model
r_C	Collector terminal resistance of the SGP BJT model
C_{jE}	Emitter-base junction capacitance
C_{jC}	Collector-base junction capacitance
q_b	Charge at the base of the BJT
i_{GC}	Avalanche current of the BJT
I_D	Majority-carrier diffusion current of the *pn* junction
V_o	Junction built-in voltage, or barrier voltage of the *pn* junction

Chapter 1

Introduction

1.1 Context

Many of music's most beloved sounds and recordings were created using equipment now considered to be vintage. This vintage equipment is revered by musicians, sound engineers, and listeners alike for their perceived-superior and familiar sound quality. Despite its desirable tonal characteristics, vintage equipment is often bulky, failure-prone, inconsistently manufactured, difficult to transport, and to maintain. It is also inaccessible, expensive, and continues to become more scarce over time. In response to these shortcomings and barriers, many researchers and industry professionals have focused their efforts on developing methods of re-creating the sound and feel of this vintage equipment in a more robust, low-cost, portable solution that integrates seamlessly into a modern, computer-based music recording workflow.

These solutions are often realized in the form of computer software that utilizes digital modelling techniques to re-create the response of the original piece of equipment. These software alternatives are inherently portable, re-producible, maintenance-free, and, in some cases, have a sound quality that rivals that of their vintage counterparts. The digital modelling of analog audio gear, particularly electronic audio circuits, is referred to as Virtual Analog (VA), and it is a vibrant, ongoing field of research. Examples of vintage equipment that has been modelled by VA researchers in the literature include guitar pedals [1–24], vacuum tube-based guitar amplifiers [25–31], electronic components including operational amplifiers [32, 33] and transformers [34], guitar pickups [35], loudspeakers [36–40], electro-mechanical devices including tape machines [41, 42] and spring reverberators [43–46], and synthesizer modules [47–53]. Further examples can be found in these review papers [54–60].

In this thesis, we will focus on accurately modelling audio circuits that use Germanium Bipolar Junction Transistors (GBJTs). An “audio circuit” simply refers to an electronic circuit that was designed to process audio signals - be it a guitar, vocals, or an acoustic instrument recorded with a microphone. The GBJT [61] is a vintage, non-linear electronic component that has a rich history in audio circuit design, dating back as far as the 1960s. While they have been considered obsolete in most fields of engineering and electronics design for many decades, GBJTs remain sought-after by audio circuit designers - particularly guitar pedal designers, as they try to re-capture some of the magic of the classic equipment in which they were originally found. Perhaps the most famous audio circuit to use GBJTs is the Dallas Arbiter Fuzz Face. First introduced in the mid-1960’s, this fuzz-distortion circuit was one of the first guitar pedals ever produced and has become one of the most influential pedals in the history of the electric guitar [62]. It can be heard on countless records, including the works of Jimi Hendrix, David Gilmour of Pink Floyd, Eric Johnson, and Stevie Ray Vaughan, to name a few. The Fuzz face, and derivatives of it, continue to be used by a myriad of guitar players to this day.

In discussions of electronic circuits and in electronics education, it is common to use simplified, idealized component models, allowing most circuits to be analysed strictly as Linear, Time-Invariant (LTI) systems. However, all real-life electronic components exhibit some non-ideal, non-linear behaviour. Furthermore, it is often these non-idealities that give vintage musical equipment the warm, lo-fi sound that makes it so well-favoured amongst enthusiasts. Accurately modelling the non-linear behaviours of these electronic components is therefore fundamental for a large portion of VA research.

Circuits containing non-linear devices, like the Fuzz Face circuit which contains two GBJTs, encode differential algebraic equations for which no general, closed-form solution exists. Computational simulation of these circuits therefore requires the use of an iterative solver at each time step to find a numerical solution for a given input signal, system state, and point in time. Computational circuit simulation has been an active area of research since the late 1960s [63–65], and in many ways can be considered a complete field. A crucial mechanism of most generic circuit solvers such as Simulation Program with Integrated

Circuit Emphasis (SPICE), however, is a variable time-step mechanism that in and of itself hinders real-time simulation. Because of the necessity of real-time performance and interactive user control, the simulation of audio circuits poses a greater challenge than that of generic circuit simulation [66].

Because of its physical, circuit-based approach and familiarity to traditional circuit analysis/simulation, the state space formalism has been a popular choice for the simulation of audio circuits for many years. State space formalism simply refers to the numerical description of a physical system, allowing the system's future behaviour to be predicted given its current "state" and set of inputs [67]. They consist of a *state vector* that contains the current configuration of the system and a set of equations that describe how the system changes from one instance in time to the next. Given its generality, state space representations are used across a broad spectrum of engineering and scientific disciplines to numerically describe and simulate dynamic systems.

Some systems can be described with only a few numbers, or *state variables*, making the state vector, and the number of required equations, very small. Complex systems naturally require many more state variables, making the state space system far more complex and therefore more computationally expensive to simulate. The number of state variables required to describe an electronic circuit depends on the number of interconnections of components, or *nodes* in the circuit, and the properties of these components. This makes state space representation very practical for modelling relatively simple circuits with a small number of nodes as it enables each component to be modelled in great detail. This approach to modelling has been implemented successfully by VA researchers, e.g. [16–23, 31], with a notable advancement being described by Yeh et al. who proposed the Nodal Discrete-Kirchhoff method (NDK method) [68, 69]. This method provides a systematic approach to discretizing analog circuits in a manner very reminiscent of the well-known Modified Nodal Analysis [70] method. Advancements in model parameter optimization [22, 23], along with further improvements to the NDK method [71], have enabled state space models of analog circuits to become increasingly accurate and convenient for real-time simulation. Together, these advancements have enabled us to consider and conduct the proposed research.

1.2 Contributions

The original contributions of this thesis can be divided into three segments. First, we review the Bipolar Junction Transistor (BJT), it's significance in audio, and several popular BJT models used for circuit simulation. Next, a study of state space modelling, with a focus on the NDK method, is undertaken. Finally, research into the implications of constructing a state space model of the classic fuzz face guitar pedal are presented.

1.2.1 Applications of the BJT in Audio Circuits

The BJT is a fundamental electronic component, found throughout all disciplines of electronics design - including audio circuit design. An overview of the BJT is given, including an overview of their physical composition, historical significance in audio, and some common circuit configurations found in audio design. Following an introduction to the BJT, three popular macro models of the BJT are presented. These include the Ebers-Moll (EM) model, the SPICE Gummel-Poon (SGP) and the Vertical Bipolar Inter-Company (VBIC) model. The models are compared and contrasted, illustrating how the models become progressively more accurate, but also have progressively higher computational costs.

1.2.2 Simulating Audio Circuits using Non-linear State Space Representation

The NDK method is a systematic approach for deriving a non-linear state space system as a physical model for an electrical circuit [68, 69]. Its similarity to traditional circuit simulation and the elegance with which it handles non-linear elements make it ideal for modelling relatively simple circuits containing non-linear elements. Furthermore, techniques for simulation are well-described and contain many similarities to those used for Modified Nodal Analysis (MNA). As a primer, a state space model of a common-emitter amplifier circuit is derived using the NDK method. It is shown that simulation of a non-linear circuit requires the use of an iterative solver at each time step, and that the conditions of each state variable must be initialized carefully.

1.2.3 Modelling the Fuzz Face

Finally, a state space model of the Fuzz Face is created and evaluated. Several state space models are created using the various BJT macro-models, allowing them to be compared in context. Model parameters were extracted from measurements taken from four vintage Mullard/Phillips AC125 GBJTs, performed using only basic lab equipment and widely available analog electronics. This "bare-bones" equipment approach was adopted out of necessity in response to the COVID-19 pandemic, which restricted the ability to access more sophisticated lab equipment and techniques. These measurements were then fed through several optimization stages, allowing parameters for each model to be derived and matched to the measured data. During optimization, the traditional pedal-builder knowledge of "matched sets" is employed. In doing so, parameter optimization is performed in two passes, using data collected from only two of the transistors per optimization - one half of each matched set. The resultant sets of parameters are used for only one of the two transistors in the Fuzz Face. These models are then compared using their spectrum, waveforms, and with audio samples.

1.3 Structure of Thesis

The remainder of the thesis will be structured as follows. First, a review of relevant literature is presented in Chapter 2. Current trends relating to the BJT and its use in audio circuits, and trends in VA research with an emphasis on physical modelling for non-linear audio circuits containing GBJTs are presented. In Chapter 3, a case study is utilized to present concepts of the BJT and state space modelling in context. Chapter 4 presents a discussion on state space modelling of the Fuzz Face and the findings of the research carried out. Finally, Chapter 5 discusses future research directions and concludes.

In Appendix A, a table of standard resistor values is shown. In appendix B, we review some fundamental principles of electronic circuits, including some of the fundamental laws, filter basics, the *pn* junction, and the operational amplifier. Finally, in Appendix C, a more detailed overview of the BJT measurement setup is given, along with some general tips for performing measurements on BJTs.

Chapter 2

State of the Art

2.1 Introduction

In this section, we introduce topics and review literature related to the research carried out in this work. First, an overview of the Bipolar Junction Transistor (BJT) is given. A brief history of the BJT, its relevance to audio circuits, along with a review of several common BJT circuits is presented, followed by an overview of several BJT macro-models used for digital modelling. Some notable literature is also reviewed therein.

Next, a review of literature in the field of VA is presented. A distinction between the two main modelling paradigms, black-box and white-box modelling, is made. Several commonly used modelling techniques within these paradigms are then outlined, with emphasis given to recent advancements in the field and state space modelling, which is reviewed in greater detail.

2.2 The Bipolar Junction Transistor

Transistors are the fundamental building block of the modern information age in which we live and its impact on society cannot be understated. They are the foundation of countless technologies, ranging from simple analog guitar pedals to our modern-day, high-power computing systems. While the "transistor" refers to a broad family of electronic devices, we will only be discussing the BJT, with a focus on GBJTs, as they are the most widely used in audio circuits.

One would be forgiven for considering the field of analog circuit design and BJTs to be complete, certainly with respect to audio circuits. For the most part, they would be correct. The majority of researchers have shifted their focus to the digital domain, or have moved on from audio-frequency circuitry to more complex, higher-frequency applications. Further, pedal designers that still produce analog distortion and fuzz circuits will struggle to design a circuit that can truly be considered "novel" - the circuit will so often resemble that of a classic design.

One notable exception, however, is a fuzz pedal released in February 2021 by Benson Amps, simply called the "Germanium Fuzz" [72]. Perhaps the first notable innovation in fuzz pedals since their inception in the 1960s, this patent-applied-for design couples all-analog, dynamic temperature control with the classic Fuzz Face circuit. This alleviates many of the inconsistencies and challenges one faces when designing with GBJTs. Namely, the β or "gain factor" of a GBJT, which is very sensitive to ambient temperature, has significant influence on the Direct Current (DC) bias of the circuit. By controlling the temperature of the GBJTs inside the pedal, a consistent β, and therefore DC bias point, can be achieved despite the ambient temperature, insuring that the pedal will function and sound as intended, regardless of external conditions. Though the patent for this device has not been made public at the time of this work's completion, a copy of the patent application was obtained through personal communication with the inventor [73].

As the field of BJT research is otherwise complete, this section will serve more as an introduction to BJTs, rather than a literature review. All of the GBJTs used for this work were of type *pnp*, which is reflected in the notation of the equations and figures in the subsections to follow. It is of note that the difference between *pnp* and *npn* BJTs is that of notation, not of fundamental behaviour, and all information presented on *pnp* BJTs is equally valid for *npn* devices with some minor notation changes. Finally, the discussions in these subsections assume some basic knowledge of electronic circuits and *pn* junctions as a detailed introduction is beyond the scope of this work. As a primer, the reader is referred to appendix B or e.g. [74, 75].

2.2.1 Overview of the BJT

Until the late 1940s, circuits utilizing triode vacuum tubes were state-of-the-art for the amplification of electrical signals for applications such as radio broadcast and audio amplification. While tubes are still beloved by guitar players, they had several drawbacks from an engineering standpoint. As the name suggests, vacuum tubes requires the construction of a vacuum sealed inside a glass tube, they have an incandescent filament that represents wasted power, and require a warm-up time before they can begin function [76]. Invented by Bardeen, Brattain, and Shockley of Bell Telephone Laboratories, the first BJT, constructed of Germanium, was demonstrated in 1947 [61, 77]. The trio would later be awarded the Nobel Prize in Physics for the invention in 1956 [75]. The device was originally proposed as a compact, more efficient alternative to the triode vacuum tube that proceeded it, but the BJT has since proven useful in far more applications than the vacuum tube.

Like the vacuum tube, the BJT is a three-terminal device (hence the name "triode" tube). Three-terminal devices are advantageous for their ability to act as a "controlled source" - by varying the voltage/current between two of the terminals, you can accurately control the voltage/current at the third terminal. Depending on how it is connected within a particular circuit, the "controlled source" properties of a BJT can serve many electrical functions, including e.g. electronically-controlled switching, signal amplification, and constant-current sourcing/sinking. In audio circuits, BJTs are most commonly employed as signal amplifiers - examples of which are shown in section 2.2.3.

Simplified Physical Structure

"Semiconductors" are a group of elements (and compound elements), such as Silicon, Germanium, and Gallium Arsenide (GaAs), whose electrical characteristics lie somewhere between that of an insulator and conductors, such as copper and silver. The power of semiconductors, however, is that by purposefully embedding impurities, or "doping" regions of a semiconductor wafer, the electrical characteristics of the material can be predictably controlled. These doped regions are said to be either *n-type* or *p-type*, depending on the embedded element. A BJT is constructed from a wafer of semiconductor material with three "doped" regions: the emitter, base, and the collector. Each region is embedded with a metal electrode, with the terminals labelled E, B, and C, respectively.

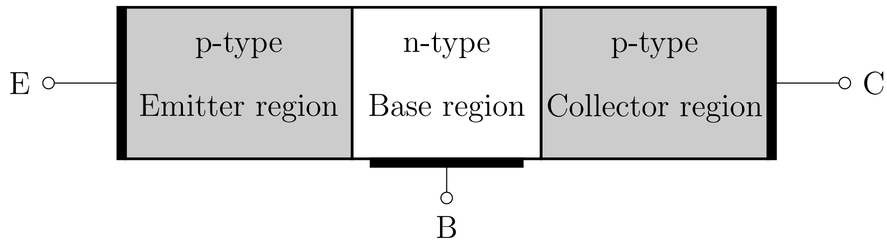


Fig. 2.1 Simplified internal structure of a *pnp* BJT.

Virtually all semiconductor atoms have four electrons in their valence shell, encouraging the formation of a crystal lattice structure through covalent bonds with four neighbouring atoms. Intrinsically, this leaves no free electrons to flow throughout the structure. Consider, then, implanting a "donor impurity atom" containing 5 electrons in its outer shell, such as phosphorus, into this lattice structure. Four of those electrons will form covalent bonds with the neighbouring atoms, but one electron remains loosely bound to the phosphorus atom, now free to flow through the structure. The structure now has a net-negative charge, so it is now said to be *n-type*. Conversely, if the structure were to be doped with an "acceptor impurity atom" containing just three electrons in its outer shell, such as Boron, it would form just 3 covalent bonds and leave an "empty position" for an excess electron to slot into. These vacant positions are also free to propagate through the structure like an electron, and are referred to as "holes". Holes are positively charged, however, so a structure with excess holes has a net-positive charge, making it *p-type* [78]. For an in-depth study of the implications of this phenomena within a BJT, the reader is referred to e.g. [75, 78].

"Conventional Current", which opposes electron flow, can therefore be conceptualized not only as the opposing flow of electrons, but also as the flow of holes. Moreover, since a hole and an electron have equal and opposite charges, they can recombine and "cancel out", leaving a net charge of zero when they come into contact.

A transistor of type *pnp* is shown in figure 2.1, which has a p-type emitter, n-type base, and p-type collector. Conversely, a BJT can also be of type *npn*, when the emitter and collector are n-type, and the base is p-type. The BJT consists simply of two *pn* junctions, the Emitter-Base Junction (EBJ), and the Collector-Base Junction (CBJ). The properties of *pn* junctions are introduced in appendix B, and explored in great detail in e.g. [61, 75]

Modes of Operation and Biasing

By applying either forward or reverse-bias conditions to the two junctions, the device will operate in one of three modes: The *active mode* is used if the BJT is to operate as an amplifier. Switching applications (e.g. logic circuits, relay control, etc.) utilize the *cut-off mode* and the *saturation mode*. As the name implies, in the cut-off mode no current flows because both junctions are reversed biased [75]. The bias conditions necessary to operate in each mode are summarized in table 2.1. Since audio circuits primarily employ BJTs as amplifiers, we will focus on the active mode.

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

Table 2.1 BJT Modes of Operation.

To operate in the active mode, two external DC voltages must be applied to the device, as shown in figure 2.2. The base-emitter voltage, V_{EB}, causes the p-type emitter to be at a higher potential than the n-type base, thus forward-biasing the EBJ. The collector-base voltage, $-V_{CB}$, causes the p-type collector to be at a lower potential than the n-type base, putting the CBJ into reverse bias.

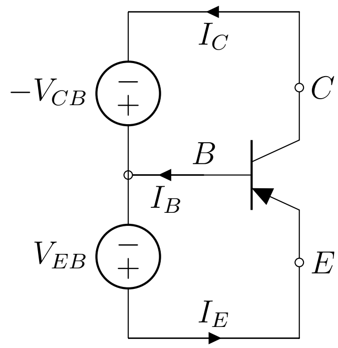


Fig. 2.2 A *pnp* BJT biased in the Active Region.

The forward bias on the EBJ will cause excess holes to flow "into" and across the emitter, forming a current I_E, towards the EBJ. As these holes cross the base, some of the holes will "recombine" with the excess electrons in the n-type base and neutralize. However, since the base is usually very thin and lightly doped with respect to the emitter [75], the vast majority of holes will reach the CBJ. Finally, since the CBJ is reverse-biased by $-V_{CB}$, and the collector is at a *negative* potential with respect to the base, these holes are swept across the CBJ and flow "out of" the collector, creating a collector current, I_C.

The current carried by the holes out of the collector current will be proportional to $e^{\frac{V_{EB}}{V_t}}$ [61], therefore:

$$I_C = I_S e^{\frac{V_{EB}}{V_t}} \tag{2.1}$$

where I_S is the *saturation current*, a parameter of the BJT that varies per component, and V_t is the *thermal voltage*, defined as:

$$V_t = \frac{kT}{q} \tag{2.2}$$

where k is the Boltzmann constant, T is the ambient temperature in Kelvin, and q is the charge of a single electron. At room temperature of 25 °C (298 K), $V_t \approx 25\,\mathrm{mV}$.

The base current has two components: electrons being injected into the emitter, and the electrons supplied by the external source, who replace the electrons lost by recombination with the flowing holes [75]. Both electron currents flow "into" the base, thus current is said to flow “out of” the base, and is proportional to the collector current, i.e:

$$I_B = \frac{I_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{\frac{V_{EB}}{V_t}} \tag{2.3}$$

where β is the *common-emitter current gain*, a transistor parameter to be explained in further detail in subsections to follow. Finally, since the current that leaves the transistor must equal the current flowing in, the emitter current can be expressed as:

$$I_E = I_B + I_C \tag{2.4}$$

By substituting equation 2.4 into 2.3, it follows that:

$$\begin{aligned} I_E &= \left(\frac{\beta+1}{\beta}\right) I_C \\ &= \left(\frac{\beta+1}{\beta}\right) I_S e^{\frac{V_{EB}}{V_t}} \end{aligned} \tag{2.5}$$

An important takeaway here is that the current flowing into the emitter and out of collector depends solely on the EBJ voltage, V_{EB}. The “controlled source” utility of a three terminal device has now been realized - the BJT in the active mode functions as a Voltage-Controlled Current Source (VCCS), where V_{EB} is the control voltage, and I_C is the output current. In practice, the EBJ will have a voltage drop of $V_{EB} \approx 0.6\,\mathrm{V}$, depending on the device (GBJTs typically have $V_{EB} \approx 0.2\,\mathrm{V}$). Like a diode, this voltage drop remains relatively constant, assuming that current limiting measures are in place. This property is explained further in appendix B. Concurrently, the collector voltage must not be allowed to rise to within more than 0.4 V or so of the base, otherwise the CBJ becomes forward biased, and the BJT enters the saturation region [75]. Further, this implies that the emitter-collector voltage, V_{EC}, should be greater than $V_{EB} + 0.4\,\mathrm{V}$.

2.2.2 BJT Small-Signal Model

For BJTs biased to operate in the active region, linear amplification can be achieved by keeping the input signal relatively small [75]. As such, the so-called “small signal model” of the BJT has been developed, which is frequently used when designing BJT amplifier circuits. While the assumption of linear operation seldom holds for most audio circuits, it remains a useful framework for understanding these circuits nonetheless.

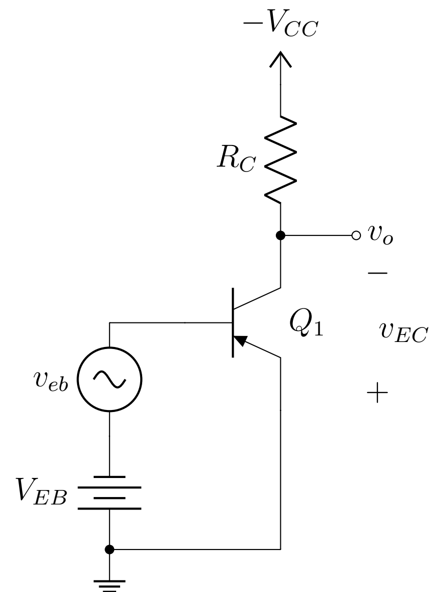


Fig. 2.3 A *pnp* BJT biased in the active region.

Consider the circuit of figure 2.3. The EBJ is forward-biased by the DC voltage source, V_{EB}, represented here as a battery, and the CBJ is reversed biased by connecting the collector to a negative power supply, $-V_{CC}$, through the resistor R_C. A time-varying input signal is represented by the voltage source v_{eb}. The DC bias point, i.e. when $v_{eb} = 0\,\mathrm{V}$, can then be expressed by the following relationships:

$$I_C = I_S e^{\frac{V_{EB}}{V_t}} \tag{2.6}$$

$$I_E = \left(\frac{\beta + 1}{\beta}\right) I_C \tag{2.7}$$

$$I_B = \frac{I_C}{\beta} \tag{2.8}$$

$$V_{EC} = I_C R_C - V_{CC} \tag{2.9}$$

The Collector Current and the Transconductance

When v_{eb} is non-zero, the *total* instantaneous collector current is:

$$\begin{aligned} i_C &= I_S e^{\frac{V_{EB}+v_{eb}}{V_t}} \\ &= I_S e^{\frac{V_{EB}}{V_t}} e^{\frac{v_{eb}}{V_t}} \end{aligned} \tag{2.10}$$

Substituting equation 2.6 yields:

$$i_C = I_C e^{\frac{v_{eb}}{V_t}} \tag{2.11}$$

Then, if $v_{eb} \ll V_t$, equation 2.11 can be approximated by ignoring the higher-order terms of the Taylor series expansion:

$$i_C \approx I_C \left(1 + \frac{v_{eb}}{V_t}\right) \tag{2.12}$$

recalling that $V_t \approx 25\,\mathrm{mV}$. It is here where we observe the conditions for which the small signal approximation is valid. For BJTs, the small signal approximation is valid for v_{eb} less than 5 mV to 10 mV at most [75]. The extent to which this assumption is valid relies on the particular device and application.

The total collector current in equation 2.12 can then be interpreted as the sum of the DC bias current, I_C, and the time-varying signal current, i_c, where:

$$i_c = \left(\frac{I_C}{V_t}\right) v_{eb} = g_m v_{eb} \tag{2.13}$$

Here, the *transconductance*, g_m, of the BJT is defined, which governs the relationship between the signal input voltage, v_{eb}, and signal output current, i_c:

$$g_m = \frac{I_C}{V_t} \tag{2.14}$$

It is observed that the transconductance is directly proportional to the DC collector current. Creating a constant, predictable bias current is therefore paramount in obtaining a predictable value of g_m. Some methods for establishing a predictable bias current will be outlined in the sections to follow, or see e.g. [75].

The Base Current and the Input Resistance at the Base

Applying the same analysis to the base current allows the input resistance presented by the EBJ to be determined. The total base current can be found by substituting equation 2.8 into 2.12:

$$\begin{aligned} i_B = \frac{i_C}{\beta} &= \frac{I_C}{\beta} + \left(\frac{1}{\beta}\right)\left(\frac{I_C}{V_t}\right) v_{eb} \\ &= I_B + \frac{i_c}{\beta} \\ &= I_B + i_b \end{aligned} \tag{2.15}$$

where the signal component of the base current, i_b, can be observed as a function of the input signal voltage, v_{eb}, and the transconductance by substituting equation 2.14:

$$i_b = \left(\frac{g_m}{\beta}\right) v_{eb} \tag{2.16}$$

The input resistance between base and emitter *looking into the base* is denoted as r_π, defined simply as the ratio of signal voltage to current, as per Ohm's law:

$$r_\pi \equiv \frac{v_{eb}}{i_b} \tag{2.17}$$

Re-arranging equation 2.16, substituting equation 2.14 for the transconductance, and substituting the DC base current from equation 2.8 allows r_π to be defined as a function of the DC base current:

$$r_\pi = \frac{\beta}{g_m} \tag{2.18a}$$

$$r_\pi = \frac{V_t}{(I_C/\beta)} \tag{2.18b}$$

$$r_\pi = \frac{V_t}{I_B} \tag{2.18c}$$

Note that the input resistance at the base is *inversely* proportional to the DC base current. Therefore, the input resistance will decrease as the base current is increased.

The Emitter Current and the Input Resistance at the Emitter

Applying a similar analysis to the emitter current allows the input resistance of the EBJ *looking into the emitter*, denoted by r_e, to be found:

$$r_e \equiv \frac{v_{eb}}{i_e} \tag{2.19}$$

$$r_e = \frac{V_t}{I_E} \tag{2.20}$$

Substituting equation 2.7 for I_E allows r_e to be expressed as a function of the transconductance:

$$r_e = \frac{\frac{\beta+1}{\beta}}{g_m} \approx \frac{1}{g_m} \tag{2.21}$$

Comparing the definitions of r_π and r_e it is observed that the are related by a factor of $\beta + 1$:

$$v_{eb} = i_b r_\pi = i_e r_e \tag{2.22}$$

$$r_\pi = \left(\frac{i_e}{i_b}\right) r_e \tag{2.23}$$

$$r_\pi = (\beta + 1) r_e \tag{2.24}$$

The Hybrid-π and T Model

Relationships have now been established linking the DC bias currents to the input resistance, current gain, and the transconductance, noting, of course, that these relationships are all linear approximations. Small signal representations of the BJT may now be constructed, as shown in figure 2.4. Both the hybrid-π and T models are shown. As the name suggests, the hybrid-π model uses the resistance r_π, while the T model uses r_e. Both are functionally identical, however the hybrid-π model is more commonly used as the input resistance looking into the base is often of greater interest to the designer.

The models shown in figures 2.4a and 2.4b represent the BJT as a transconductance amplifier, as derived in the previous sections. Figures 2.4c and 2.4d represent the BJT as a current amplifier. The equivalency between the two models is observed by re-arranging

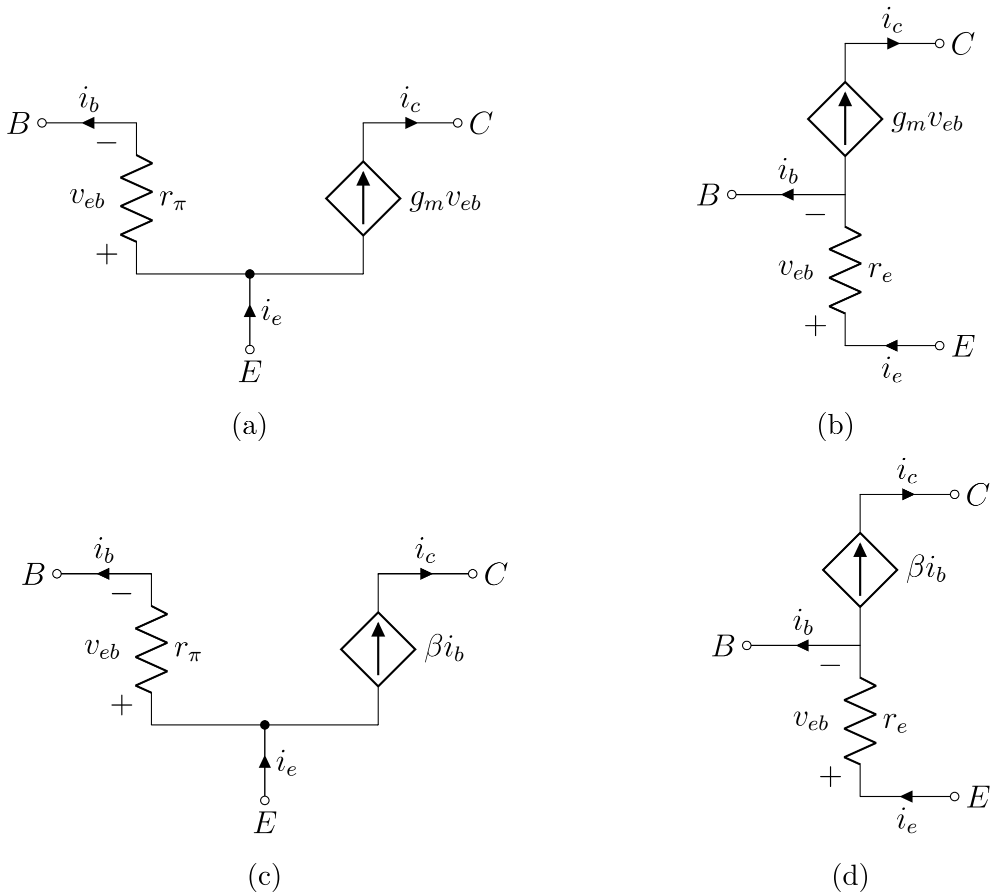


Fig. 2.4 Two variations on the hybrid-π and T models of small signal operation of the BJT. Figures (a) and (b) show the BJT as a transconductance amplifier, whereas figures (c) and (d) show the BJT as a current amplifier.

equation 2.16:

$$g_m v_{eb} = \beta i_b = (g_m r_\pi)\, i_b \tag{2.25}$$

These variations on the small signal models illustrate that the BJT can act as either a VCCS, or as a Current-Controlled Current Source (CCCS), depending on whether or not the input signal is a voltage source (as shown above), or a current source.

Voltage Gain

Finally, we consider the signal voltage gain of the BJT amplifier, denoted by A_v, which is defined as the ratio of the output and input signal voltages:

$$A_v \equiv \frac{v_{out}}{v_{in}} = \frac{v_{ec}}{v_{eb}} \tag{2.26}$$

Considering the emitter-collector voltage of figure 2.3, the following relationships can be derived by separating the total voltage, v_{EC}, into its DC and signal components:

$$\begin{aligned} v_{EC} &= V_{CC} - i_C R_C && (2.27)\\ &= V_{CC} - (I_C + i_c) R_C && (2.28)\\ &= (V_{CC} - I_C R_C) - i_c R_C && (2.29)\\ &= V_{EC} + v_{ec} && (2.30) \end{aligned}$$

Substituting equation 2.13, allows the signal portion of the emitter-collector voltage to be expressed as a function of the transconductance and the input voltage, v_{eb}:

$$\begin{aligned} v_{ec} &= -i_c R_C = -g_m v_{eb} R_C && (2.31)\\ &= -(g_m R_C) v_{eb} && (2.32) \end{aligned}$$

From there, the voltage gain can be expressed as a function of the transconductance by comparing with equation 2.26:

$$\begin{aligned} A_v &\equiv \frac{v_{out}}{v_{in}} = \frac{v_{ec}}{v_{eb}}\\ &= -g_m R_C = -\left(\frac{I_C}{V_t}\right) R_C \end{aligned} \tag{2.33}$$

The voltage gain, then, is proportional to the transconductance, and therefore the DC collector current, I_C, as shown by substituting g_m with equation 2.14. Producing a constant, predictable voltage gain is therefore dependent on producing a constant, predictable bias current.

2.2.3 Common Audio Circuits using BJTs

In this section, we will review some commonly-used BJT-based audio circuits. These circuits can all be analysed using the small signal model of the BJT from section 2.2.2, but detailed mathematical relationships of the circuits will be omitted here in favour of high-level, quantitative analysis. Some equations will be presented for context as required. Finally, it is of note that only *pnp* notation is shown, with the DC power supply $-V_{CC}$ being a *negative* potential with respect to ground. However, all of these circuits can be constructed with an *npn* BJT and a positive power supply.

The Common-Emitter Amplifier

The Common-Emitter Amplifier is by far the most widely-used of the BJT-based audio circuits. While it has several permutations, the defining features of all common-emitter amplifiers are that they use a single BJT with their emitter connected to ground, or the "common" voltage reference. The most widely-used form of the common emitter amplifier is shown in figure 2.5.

The resistive voltage divider of R_{B1} and R_{B2} is used to forward-bias the EBJ and establish a DC base current, I_B, at the BJT's base, which in turn induces a bias current from

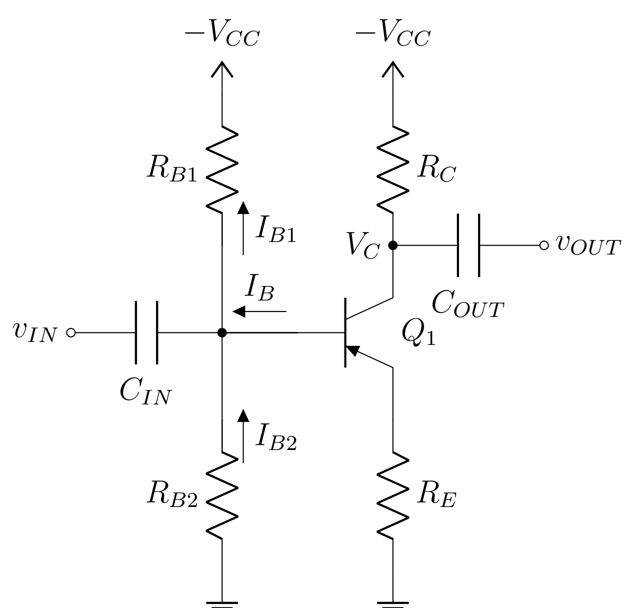


Fig. 2.5 A *pnp* BJT common-emitter amplifier.

emitter to the collector. The collector is tied to $-V_{CC}$ through the resistor, R_C, reverse-biasing the CBJ so that the BJT operates in its active region. The resistors R_C and R_E are specified to establish the collector bias point, V_C, and set the overall signal voltage gain of the circuit. Correctly biasing the collector, and therefore V_{EC}, is integral in maximizing the linear behaviour of the amplifier. Finally, the capacitors C_{IN} and C_{OUT} isolate the DC bias voltages from any additional circuitry connected to the input or the output.

A non-zero value for R_E establishes *emitter degeneration*, which mimics the effects of negative feedback [75]. This helps to stabilize the amplifier, increase it's linearity, and reduce the overall gain. As such, this is often referred to as "emitter feedback". The voltage gain of the circuit in this configuration can then be approximated as:

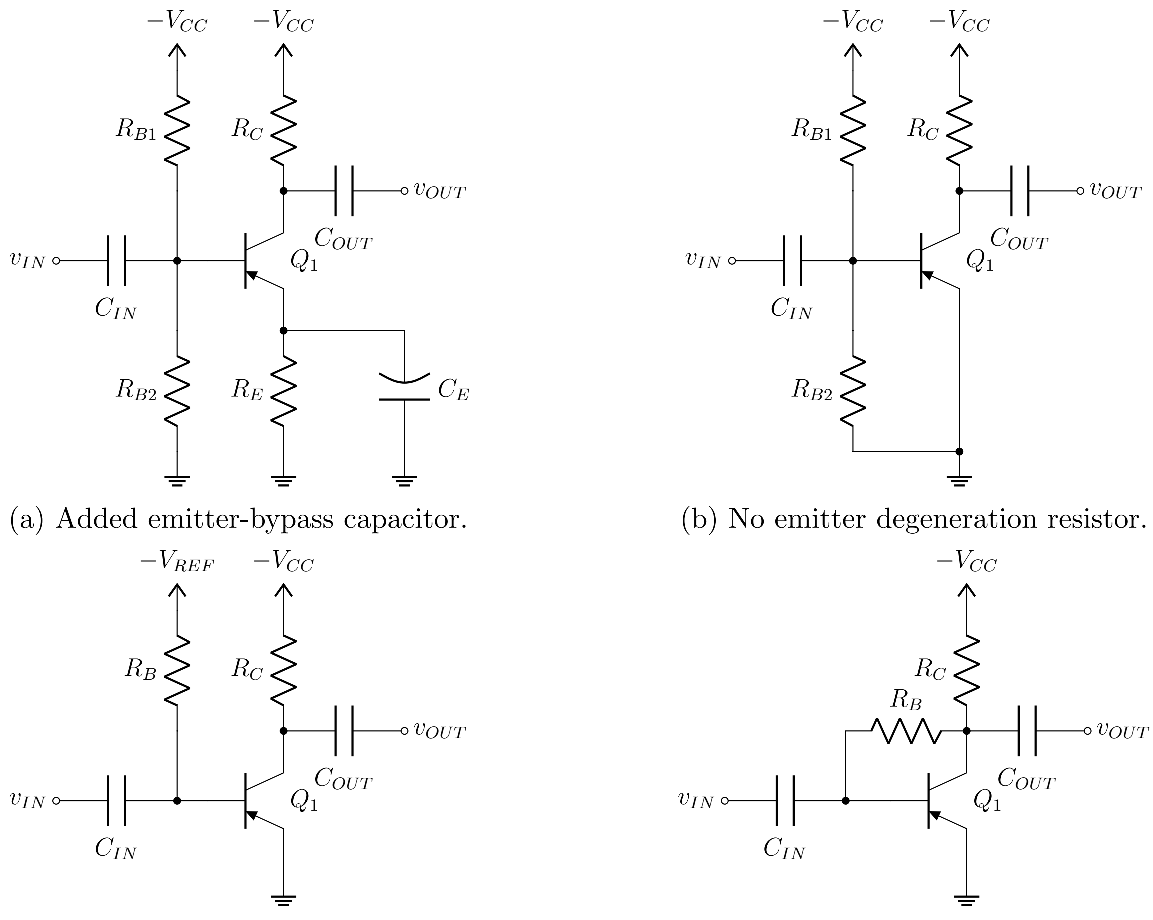
$$A_v = -\frac{R_C}{R_E + r_e} \approx -\frac{R_C}{R_E} \tag{2.34}$$

Since $r_e \ll R_E$, the voltage gain of the circuit can be approximated by simply omitting r_e. Note that the voltage gain is *negative* because the base voltage and collector voltage have an inverse relationship. This means that the output signal will be 180° out of phase from the input signal.

As noted above, several variations on the common-emitter amplifier are often found in audio circuits. These variations often involve a different biasing method, attempt to increase the overall voltage gain, or maximize linearity. Several variations on the common-emitter amplifier are shown in figure 2.6. To achieve a higher voltage gain, a bypass capacitor is often placed parallel[1], or "shunt" across the emitter resistor, R_E, as shown in figure 2.6a. Since a capacitor is effectively a short circuit at sufficiently high frequencies, this gives the input signal a direct path to ground, "bypassing" R_E without disturbing the DC bias network. With this signal-short to ground, the effective resistance is reduced to the internal emitter resistance, r_e, which is typically less than $10\,\Omega$ [75]. This provides a large increase in gain to the amplifier. The voltage gain can then be approximated as:

$$A_v = -\frac{R_C}{(R_E||Z_C) + r_e} \approx -\frac{R_C}{r_e} \tag{2.35}$$

[1]The notation $Z_1||Z_2$ is commonly used to denote two impedances in parallel



(a) Added emitter-bypass capacitor.

(b) No emitter degeneration resistor.

(c) "Fixed-base" biasing.

(d) "Collector-feedback" biasing.

Fig. 2.6 Variations on the common-emitter amplifier.

Alternatively, R_E may be omitted as a means of increasing the gain of the circuit. While this increases the gain by approximately the same amount as adding a bypass capacitor, it reduces the linearity of the circuit as well. Thankfully, though, that is often desirable in audio circuits. When the emitter resistor is omitted, it is common to use an alternative bias network. Some of these alternative bias networks are shown in figure 2.6.

The common-emitter amplifier can also be used to produce a *balanced* output from a *single-ended* input, as shown in figure 2.7. To do so, the emitter and collector resistor are set equal, i.e. $R_E = R_C = R$, with no bypass capacitor, as shown in equation 2.34. As per equation 2.34, this will make the voltage gain approximately unity. An output is then taken from both the collector and the emitter, whose signals are 180° out of phase from each other. Since the gain of the amplifier is unity, and the signal gain from the BJT's base to emitter is approximately unity anyway, the amplitude of the balanced output is approximately double that of the input signal's amplitude.

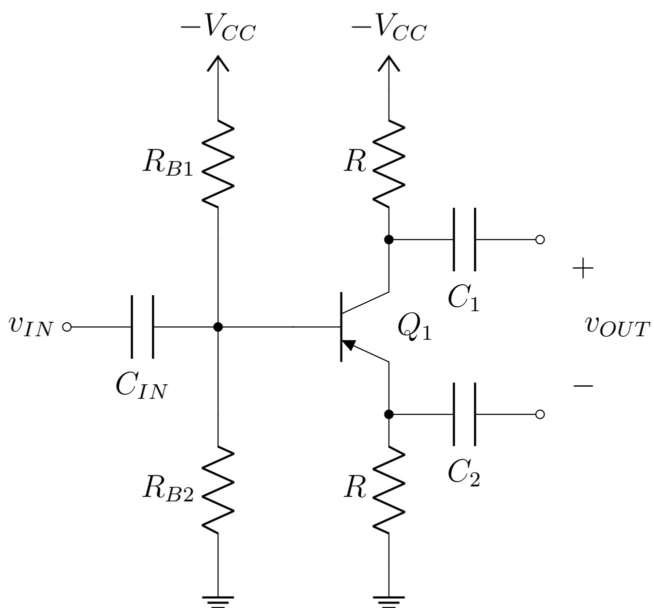


Fig. 2.7 Common-emitter amplifier that creates a balanced output.

The Emitter-Follower

The BJT emitter-follower is a unity-gain amplifier that "isolates" two stages of a circuitry from one another. It presents any circuitry at its input with a very large impedance, then feeds subsequent circuitry at its output with a very low output impedance. This type of circuit is often referred to as a "buffer", and they are widely used in applications where "loading" a circuit (connecting it to a low impedance load) will have adverse effects on its operation. A buffer mitigates the loading effects on the input side, and drives the subsequent load with a low output impedance. The BJT emitter-follower is shown in figure 2.8.

The base resistor, R_B is usually fairly large, around $1\,\mathrm{M}\Omega$, which both sets the signal input impedance of the circuit and biases the BJT's base at $-V_{REF}$ (typically $-V_{CC}/2$). R_E sets the emitter current of the BJT, and the capacitors C_{IN} and C_{OUT} AC couple the circuit, isolating the input/output from the DC bias voltages. A buffer circuit can often be found as the first stage and the last stage of a guitar pedal's circuit as it helps to reduce the transmission-line effects of long lengths of coaxial instrument cables, and to prevent the circuit from loading the guitar's pickups. Since a guitar pickup has a relatively high impedance (typically between 6 - 15 kΩ), the shunt capacitance of the cable can produce a significant roll-off in treble frequencies if not terminated with a high impedance - such is provided by an emitter-follower.

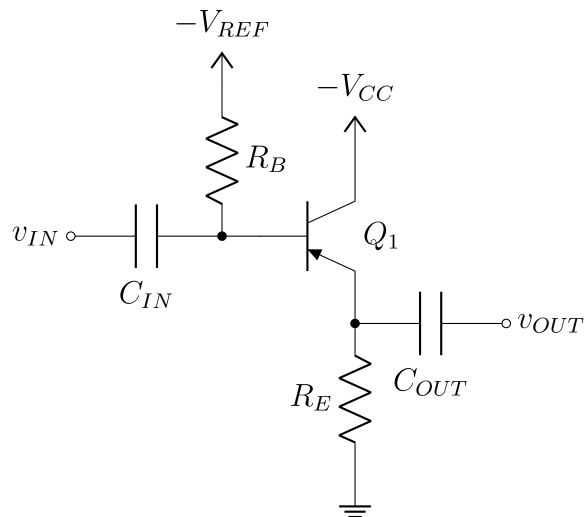


Fig. 2.8 The *pnp* BJT emitter-follower.

The Differential Amplifier

The differential amplifier ("diff amp") is another BJT-based circuit commonly used in audio applications. Utilizing a pair of BJTs whose emitters are coupled together, the circuit accepts a balanced input and produces an amplified, balanced output - though it can be configured for a single-ended input/output, and any combination therein. The diff amp typically has a much higher gain factor than that of the common-emitter amplifier, especially when coupled with an active load. The basic circuit is shown in figure 2.9.

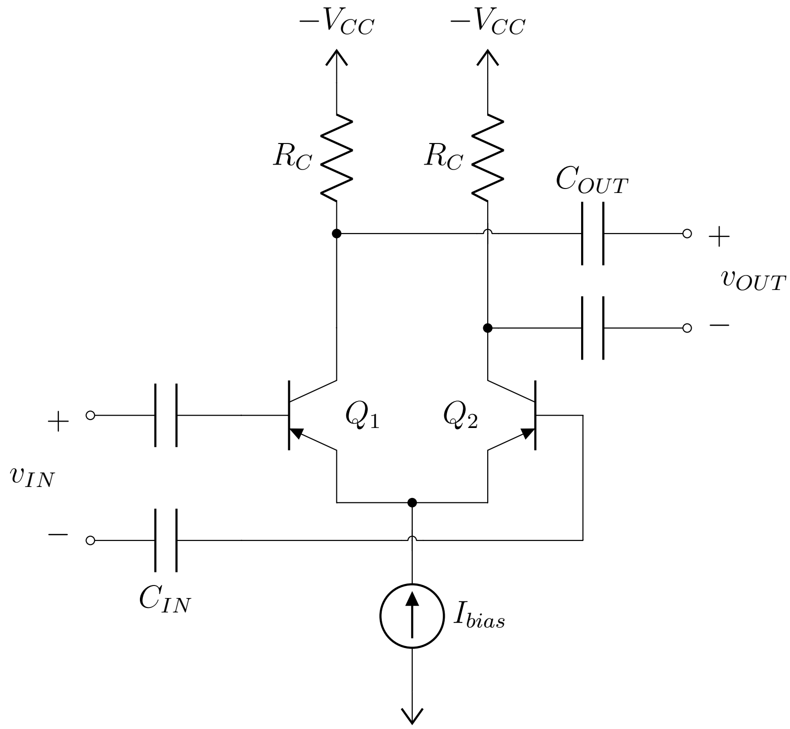


Fig. 2.9 The *pnp* BJT differential amplifier.

The basic function of the diff amp relies on Q_1 and Q_2 being *matched*, i.e. having the same gain factor β. The current source, I_{bias}, establishes a bias current in both BJTs. When $v_{IN} = 0$, it is implied that the base of both transistors are held to the same voltage. Both devices will therefore conduct an equal share of the bias current, i.e. $I_{bias}/2$. The voltage at each device's collector will also be equal, so the output voltage, v_{OUT} is also equal to 0. As the voltage at the two bases differs, i.e. $v_{IN} \neq 0$, so too will the output voltage. It can be said, then, that the diff amp responds to the *difference* between signals, while ignoring any common-mode portion of the input (such as DC bias) [75].

The diff amp can be found in many classic amplifiers designed by Marshall Products Ltd. (predominantly using vacuum tubes) [79], and variations of the diff amp are used in some octave fuzz pedals [80].

2.2.4 BJT Macro-Models for Computational Simulation

The Ebers-Moll Model

The first BJT model to experience widespread adaptation in computational circuit modelling and simulation, the EM model was first proposed in 1954 as a large signal model of the BJT [81]. The model was primarily designed to model the DC characteristics of the BJT when acting as a switch. Using just a handful of device parameters, it allows the open and closed impedance of the transistor and the switching time to be accurately predicted, and it provides a reasonably accurate model of the active region of the BJT [81]. The EM transistor model persists to this day in both engineering practice and education as it lends itself most readily to simple "rule of thumb calculations" [82].

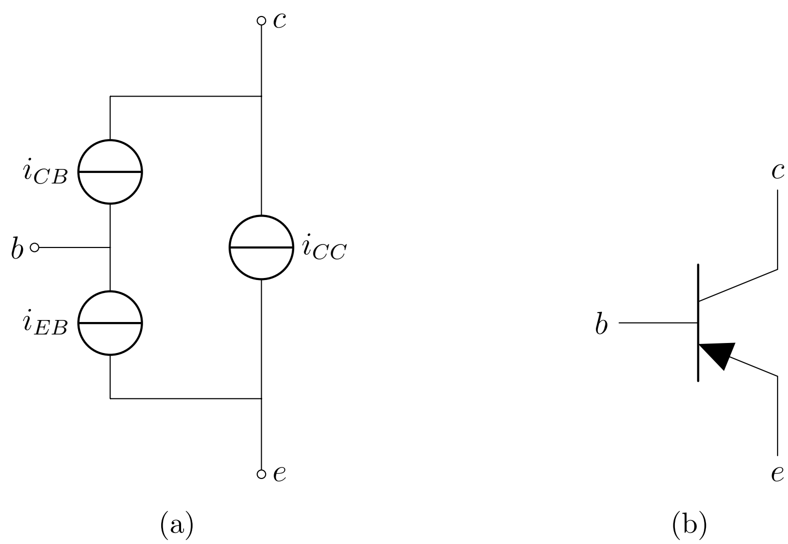


Fig. 2.10 The Internal Ebers-Moll model and the corresponding schematic symbol of a *pnp* BJT.

The EM representation of a *pnp* BJT and the corresponding schematic symbol are shown in figure 2.10. It can be understood as two back-to-back *pn* junction diodes with a common, dominant current component that couples the emitter to the collector. The inter-junction currents, i_{CB} and i_{EB}, and the dominant current component, i_{CC}, represent linear combinations of the forward and reverse currents, i_f and i_r. They are defined by the $i-v$ relationship of a Shockley *pn* junction diode [61], and are dependent upon the v_{EB}

and v_{CB}, respectively:

$$i_f = I_S\left(e^{\frac{v_{EB}}{N_f V_t}} - 1\right), \quad i_r = I_S\left(e^{\frac{v_{CB}}{N_r V_t}} - 1\right) \tag{2.36}$$

where N_f and N_r represent the forward and reverse ideality factors, respectively. The dominant current and the inter-junction currents are then defined as:

$$i_{CC} = i_f - i_r, \tag{2.37}$$

$$i_{EB} = \frac{1}{\beta_f} i_f, \quad i_{CB} = \frac{1}{\beta_r} i_r \tag{2.38}$$

where β_f and β_r are the forward and reverse common-emitter current gain, respectively. The current flowing through each terminal of the BJT can then be described as:

$$i_B = i_{EB} + i_{CB} \tag{2.39}$$

$$i_C = i_{CC} - i_{CB} \tag{2.40}$$

$$i_E = i_{CC} + i_{EB} = i_B + i_C \tag{2.41}$$

The remaining junction voltages can be found using Kirchhoff's current/voltage laws, i.e. $v_{EC} = v_{EB} - v_{CB}$. Therefore, only two non-linear equations and two non-linear variables need to be tracked and updated during each time step of simulation. This makes the model very efficient for real-time simulation in a state space model, as it typically requires few steps in an iterative solver to converge. As noted in [21], the equations can be further simplified into matrix form for use in a state space model:

$$\begin{pmatrix} i_B \\ i_C \end{pmatrix} = \boldsymbol{L} \begin{pmatrix} i_f \\ i_r \end{pmatrix} \tag{2.42}$$

where the matrix **L** is a square matrix of scalar values:

$$\boldsymbol{L} = I_S \begin{bmatrix} \frac{1}{\beta_f} & \frac{1}{\beta_r} \\ 1 & -\frac{\beta_r - 1}{\beta_r} \end{bmatrix} \tag{2.43}$$

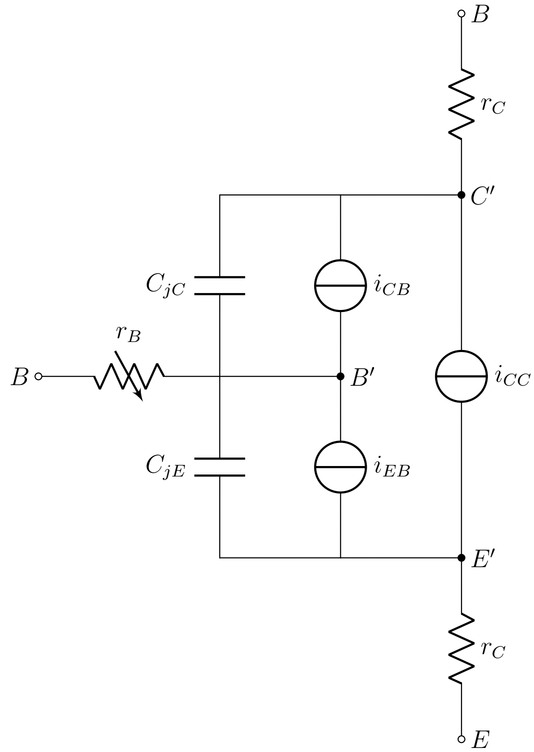


Fig. 2.11 The SGP BJT model.

The SPICE Gummel-Poon Model

The SPICE Gummel-Poon (SGP) model was first introduced in 1970 and was proposed as a compact, direct replacement to the EM model for use in computational simulation and analysis [83]. The SGP model incorporates the charge-control relation of the transistor [84], which introduces a relationship between the junction voltages, the collector current, and the total charge that enters through the base terminal. This relation, in conjunction with conventional charge-control theory [85] allows the SGP model to incorporate several BJT properties previously unrepresented in the EM model, while still maintaining a relatively low number of model parameters. These effects include collector-current-dependent output conductance (Early effect) [86], space-charge-layer generation and recombination (Sah-Noyce-Shockley effect) [87], conductivity modulation in the base (Webster effect) [88] and in the collector (Kirk effect) [89], and emitter crowding [90, 91].

As the SGP model was designed with backwards compatibility in mind, we begin by considering the EM model equations. The terminal currents, defined by equations (2.39), (2.40), and (2.41), respectively, hold for the SGP model. The forward and reverse currents (2.36), the dominant current component (2.37), and the inter-junction currents (2.38), however, are re-defined to include the aforementioned characteristics. The dominant current component is modified with an additional term, q_b, representing the charge at the base, to incorporate the Early effect and the Webster effect:

$$i_{CC} = \frac{1}{q_b}\left(i_f - i_r\right) \tag{2.44}$$

where q_b is as quadratic function of two terms, q_1 and q_2. The term q_1 represents the sum of zero-bias charge and the charge associated with the EBJ and CBJ capacitances. The second term represents the current-dependent charge associated with diffusion capacitances [83]. The former has the effect of creating a dependence of i_C on v_{EC}, and therefore the transistor's bias, while the latter introduces a roll-off in current gain at higher bias voltage values. It is defined below, along with its commonly-used approximation:

$$\begin{aligned} q_b &= \frac{q_1}{2} + \left[\left(\frac{q_1}{2}\right)^2 + q_2\right]^{\frac{1}{2}} = \frac{q_1}{2}\left(1 + \sqrt{1 + 4\frac{q_2}{q_1^2}}\right) \\ q_b &\approx \frac{q_1}{2}\left(1 + \sqrt{1 + 4q_2}\right) \end{aligned} \tag{2.45}$$

The two charge terms, q_1 and q_2, are defined as:

$$q_1 = 1 + q_e + q_c \approx \frac{1}{1 - \frac{v_{CB}}{V_{af}} - \frac{v_{EB}}{V_{ar}}} \tag{2.46}$$

$$q_2 = \frac{i_f}{I_{kf}} + \frac{i_r}{I_{kr}} \tag{2.47}$$

where V_{af} and V_{ar} represent the forward and reverse early voltages, respectively, and I_{kf} and I_{kr} represent the forward and reverse knee currents, respectively. Next, the inter-junction currents are re-defined to include a second exponential term, representing the leakage current:

$$i_{EB} = \frac{1}{\beta_f} i_f + I_{SE}\left(e^{\frac{v_{EB}}{N_E V_t}} - 1\right) \tag{2.48}$$

$$i_{CB} = \frac{1}{\beta_r} i_r + I_{SC}\left(e^{\frac{v_{CB}}{N_C V_t}} - 1\right) \tag{2.49}$$

The terms I_{SE} and I_{SC} represent the leakage current in the emitter and collector, respectively, while N_E and N_C represent the leakage nonideality factors of the emitter and collector, respectively. These re-defined terms comprise the internal structure of the SGP model, which is of the same form as the EM model (see figure 2.10). To complete the model, 5 external components are added. A resistor at each junction, the base resistor being variable, and a capacitor between the EBJ and CBJ to represent the space-charge and diffusion capacitance between the respective junctions [92]. The completed SGP model including external components is shown in figure 2.11. The base resistor is described as:

$$r_B = R_{BM} + 3\left(R_{B_o} - R_{BM}\right)\left(\frac{\tan(z) - z}{z \cdot \tan^2(z)}\right) \tag{2.50}$$

where

$$z = \frac{-1 + \sqrt{1 + (\frac{12}{\pi})^2 \cdot \frac{i_B}{I_{RB}}}}{\frac{12}{\pi^2} \cdot \sqrt{\frac{i_B}{I_{RB}}}} \tag{2.51}$$

and R_{B_o} is the zero-bias base resistance, R_{BM} is the minimum base resistance at high current, and I_{RB} is the base current at medium base resistance. The capacitance between the base and the i^{th} terminal is given by:

$$\begin{aligned} C_{ji} &= C_{Dji} + C_{Sji} \\ C_{ji} &= \frac{C_{ji0}}{\left(1 - \frac{V_{bi}}{Vji}\right)^{M_{ji}}} + \frac{T_m}{N_m V_t}\frac{I_S}{N_{q_b}} \exp\left(\frac{v_{iB}}{N_m V_t}\right) \end{aligned} \tag{2.52}$$

where M_{ji} is the exponential factor, C_{ji0} is the zero-bias capacitance, and V_{ji} is the built-in potential of the $j - i$ junction, T_m is the transit time and N_m is the nonideality factor for the $m^t h$ direction (forward for the EBJ, reverse for the CBJ).

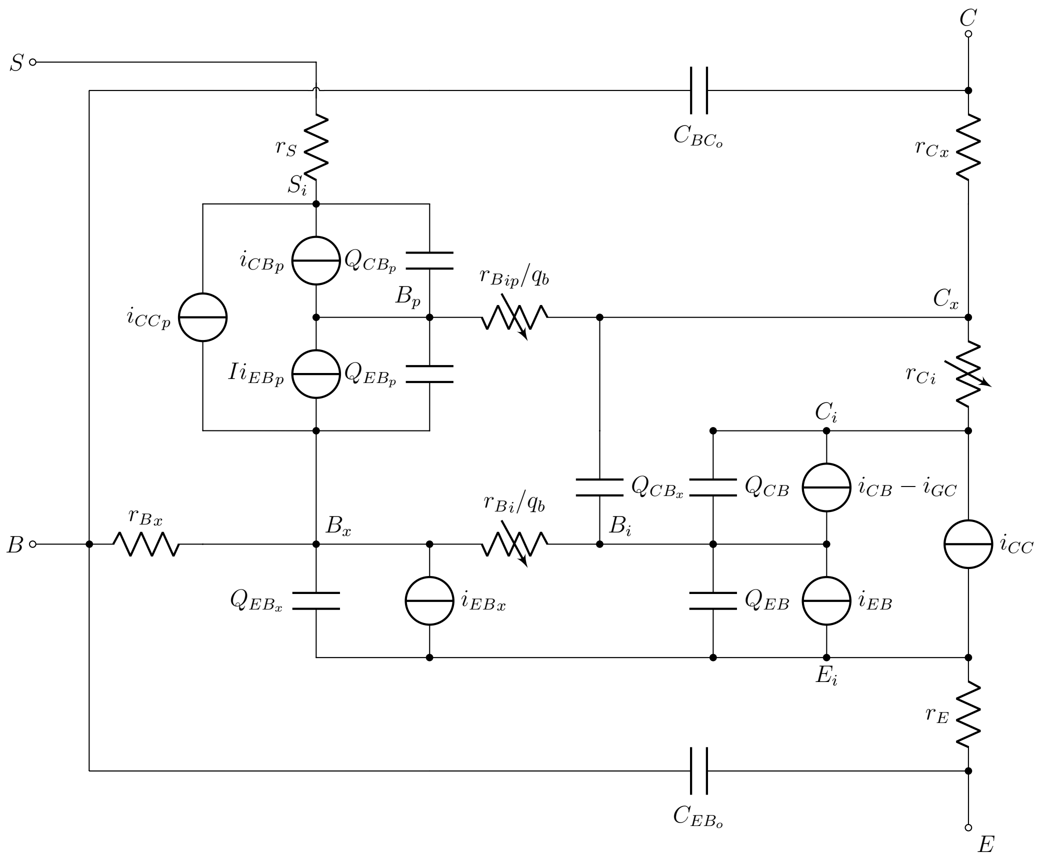
All of the additions to the EM model found in the SGP model allow it to more accurately represent the DC and AC characteristics of a BJT. The SGP model remains the default model used by circuit simulation software such as SPICE, and continues to be used as an accurate design aid by analog and Radio Frequency (RF) engineers.

The Vertical Bipolar Inter-Company BJT Model

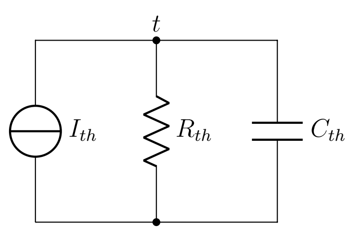
The VBIC model was introduced in 1995 [93] to address the shortcomings in the SGP model for use in modern Integrated Circuit (IC) design. Several updates contribute to the VBIC model's improved accuracy, including improved modelling of the early effect, quasi-saturation, substrate and oxide parasitics, avalanche multiplication [94], and temperature behaviour [93]. Like the SGP model, though, it was designed to be fully backwards compatible with its predecessor. By setting certain parameter values to zero or infinity, the VBIC model simplifies to the SGP model. This improvement in accuracy, however, comes at the expense of model complexity and computational cost of simulation. The full schematic of the VBIC model is shown in figure 2.12.

The most significant change in the VBIC model is the departure from the familiar three-terminal structure of the BJT in favour of a four-terminal device. This fourth terminal represents the device substrate (denoted by S). This terminal drives a parasitic transistor connected between the collector and base, which models the substrate losses. Two companion circuits are added to accompany the primary circuit which model the thermal and excess phase effects, respectively. Many more charge relationships have been added between the various junctions, a variable r_{Ci} is added in addition to the fixed collector resistor, r_{Cx}, a fixed base resistor is added to the variable base resistance, the avalanche current effect is embedded in the CBJ current source as $i_{CB} - i_{GC}$, and the base current is split between two current terms: i_{EBx} and i_{EB}. Finally, many of the mathematical relationships within these components have been updated to better describe the physical behaviour of the BJT.

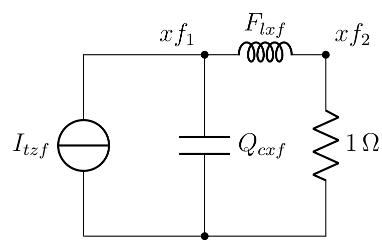
The number of equations and parameters involved with this model is large, and a detailed review of all of them is beyond the scope of this work. For a detailed explanation of all equations, parameters, and improvements made over the SGP model, the reader is referred to e.g. [92, 93, 95].



(a) Primary circuit.



(b) Thermal network.



(c) Excess phase network.

Fig. 2.12 Equivalent circuit of the VBIC BJT model.

Perhaps the most intriguing part of the VBIC model from the perspective of VA modelling is shown in figure 2.12b - the thermal network, which models the temperature-dependent effects of the BJT. While discussions about BJT circuits typically assume a constant ambient temperature, it is widely understood that ambient temperature, as well as self-heating effects, have a large impact on BJT circuit performance, particularly on its gain factor (and therefore bias currents).

2.2.5 Summary

In this section, an overview of the state of the art of BJTs as related to audio circuits was given. The history of the BJT was discussed, followed by its basic structure, modes of operation and bias, and the small signal model. Next, several BJT-based audio circuits were reviewed, followed by several BJT macro-models that are commonly used in computational simulations. These concepts will be integral in the discussions to follow in chapters 3 and 4.

2.3 Virtual Analog

As computing power has become increasingly inexpensive and plentiful, the demand of musicians, artists and producers for digitized versions of analog equipment and instruments has too increased. This demand can be partly attributed to our nostalgic tendency to re-create sounds from the past, and partly attributed to the increasing need for musical equipment to integrate well into the workflow of a modern Digital Audio Workstation (DAW).

The first example of a commercial product to implement the principles of VA was the NordLead Synthesizer, introduced by the Swedish company Clavia in 1994 [54]. It was the first synthesizer to implement the sound generation principles of an analog synthesizer using digital signal processing techniques, allowing the sound of the synthesizer to be enjoyed while avoiding all the downsides of analog synthesizers. Since then, VA research has flourished and continues to be a vibrant field of research to this day.

In [44], Parker identifies the three main goals that VA researchers are trying to accomplish. They are:

1. *Emulation* - to produce exact digital copies of particular analog systems.

2. *Artifact Reduction* - to produce digital sound processing or generation blocks which behave like their ideal continuous-time equivalents by reducing or eliminating the undesirable side-effects of digital signal processing.

3. *Analog Feel* - to produce techniques or structures that bring some of the above-mentioned artistically desirable qualities of the analog realm into digital systems without necessarily exactly reproducing a particular system. These qualities include unpredictability, drift and emergent behaviour, dynamic non-linear behaviour, etc.

This work will focus on accomplishing goals 1 and 3 - creating accurate digital models of analog systems with a "feel" that's authentic to the original. There are several general approaches to digitally modelling analog equipment that have been described in the VA literature across a wide range of systems and devices.

All of these approaches can be broadly categorized into two main paradigms, depending on the set of properties that the researcher sets out to recreate. These two categories are so-called "black-box modelling" and "white-box modelling", aptly named for the point of view they represent. Black-box modelling refers to methods that model perceptual variables and input-output measurements of the reference system. White-box modelling refers to methods that do the opposite - they use everything known about the system to model its physical properties. Also of note are so-called "grey-box" modelling techniques [7, 9, 25], which share many commonalities with black-box modelling techniques but assumptions are made about the basic structure of the reference system. Examples of black-box and white-box modelling techniques will be discussed in the sections to follow.

2.3.1 Black-Box Modelling

Black box modelling uses input-output measurements of a reference system to derive parameters or coefficients of a standard digital modelling structure - alleviating the need for specific knowledge of the reference system. This method is favourable for large, complex systems that would be too computationally expensive to model on the component or the physical level. Black box models tend to focus on the perceptual characteristics and the spectral domain properties of the system, rather than the time domain. Many methods have been described in the literature, including Dynamic Convolution [4, 96, 97], Block-Oriented models [1, 2, 5, 8, 48], and, more recently, the use of Neural Networks for model training [10, 26, 27, 98–101].

An LTI system can be completely characterised by it's impulse response, denoted as h. The output can then be found for any given input by convolving it with the impulse response in the time domain, or by multiplying them in the frequency domain

$$y(t) = (h * x)(t) = \int_{-\infty}^{+\infty} h(\tau)x(t-\tau)d\tau \tag{2.53a}$$

$$Y(\omega) = H(\omega)X(\omega) \tag{2.53b}$$

Non-linear systems, however, cannot be described in such a straightforward manner. As discovered by Vito Volterra in the 19th century through his work on the theory of analytic functionals [102], fully characterizing a non-linear system requires an infinite series of multi-dimensional impulse responses

$$y(t) = \sum_{m=0}^{+\infty} F_m[x](t) \tag{2.54}$$

where F_m are functionals (functions of functions) defined as

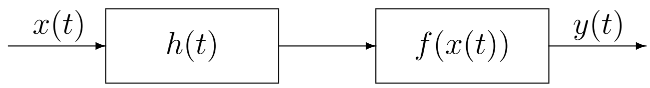
$$F_0[x](t) = h_0 \tag{2.55}$$

$$F_m[x](t) = \int_{\tau_1} \cdots \int_{\tau_m} h_m(\tau_1, \cdots, \tau_m) \prod_{n=1}^{m} x(t-\tau_n)d\tau_n \quad m > 0 \tag{2.56}$$

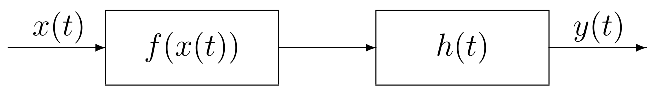
The function $h_m(\tau_1, \cdots, \tau_m)$ is the mth-order Volterra Kernel. This expansion is usually denoted as *Volterra Series* or *expansion* in the literature. It can be seen as a generalization of the description of an LTI system, or the introduction of memory to the Taylor expansion [103].

It follows, then, that a non-linear, time-variant reference system can be modelled by finding the Volterra series parameters that match the input-output behaviour of that system. Finding these parameters is referred to as Non-Linear System Identification (NSI), and is the basis of most black-box modelling research.

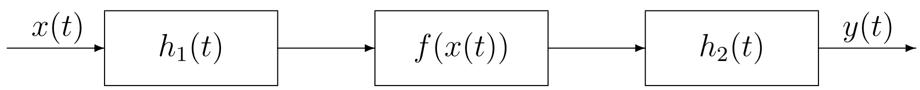
Models based directly on the Volterra series are not common in the literature, however. Not only would that require a prohibitive number of parameters to be found, but also because the multi-dimensional nature of the impulse responses has an exponentially increasing computational cost as kernels are added. Most NSI problems today can therefore be reduced to (1) selecting an appropriate discrete model of a truncated Volterra Series



(a) Weiner.



(b) Hammerstein.



(c) Weiner-Hammerstein.

Fig. 2.13 Common block-based model structures.

and (2) employing some model identification method to extract the Volterra kernels and other system parameters from the reference system [48, 103].

Block-Oriented Models

Several truncated versions of the Volterra series have been described in the literature, and successfully employed to create digital models of analog equipment. Collectively referred to as “block-based” or “block-oriented” models, these models consist of some combination of an LTI filter (linear memory blocks) and non-linear algebraic functions (memoryless non-linear blocks). Block-based non-linear system modelling has been ongoing since the 1950’s. Norbert Weiner was one of the first to study parameter estimation for the Volterra series for non-linear system modelling [104]. He approximated the Volterra series using an LTI filter cascaded with a memoryless non-linear block (figure 2.13a).

Other block-based models commonly used in VA research include the Hammerstein model, which swaps the LTI and non-linear block (figure 2.13b), and the Weiner-Hammerstein model which combines the two by using two LTI filters, one on either side of the non-linear block (figure 2.13c). Polynomial versions of the Weiner and Hammerstein models are also quite common, consisting of several parallel Weiner (or Hammerstein) models that are summed together. The non-linear blocks are typically powers of the input signal [103]. While these models are the most commonly used in VA research, others models, such as block-based models with feedback [105], have also been explored in the literature. A rigorous study of systems that can be accurately modelled using a finite Volterra series is given by Boyd and Chua in [106].

System Identification Methods

Once a suitable truncated Volterra series model has been chosen, the problem becomes estimating the number of kernels required and the kernel/system parameters. Traditionally, this is done by exciting the system with some known signal and recording the corresponding output. The input-output correspondence is then used to derive the kernel/system parameters. Excitation signals described in the literature include an impulse train [105], chirp [107], random signals [108], and correlation [105].

A promising method first proposed by Farina [107, 109] and studied in great depth by Novak and others [110–113], is the logarithmic swept-sine. This method excites and deconvolves the system with a logarithmically swept sinusoidal signal to extract higher-order impulse responses of each distortion order. This method alleviates the issue of estimating power and cross-spectral densities associated with correlation-based methods [103].

Neural Networks as Black-Box Models

In recent years, the concept of “neural networks” has infiltrated most areas of technology and has become a bit of a cliché. VA has proven to be no exception, with the emergence of several black-box models of audio circuitry supplemented by a neural network in the literature. The bulk of this research centres around distortion circuitry, namely vacuum tube amplifiers [26, 27, 100] and overdrive/distortion pedals for guitar [10, 98, 100], but applications to time-varying effects such as the phaser and tremolo [99, 101], and to synthesizer circuits [98] have also been described.

The concept of deep learning, neural networks, and machine learning are complex, active fields of research, and an in-depth overview exceeds the scope of this thesis. But essentially, a neural network is a computer algorithm with long-term memory that self-corrects over time, allowing it to become more precise. In order to initialize the model, a set of labelled training data is required. Usually this is a very difficult and time-consuming task, but because audio recording is so mature and readily available, training data for audio circuit modelling is relatively easy to collect [100].

In the context of black-box modelling, a neural network model stands in contrast to a truncated Volterra series model, whose system parameters are fixed and derived ahead of time. With a neural network, the system is adaptable and can modify itself based on the time-variance of the input signal.

2.3.2 White-Box Modelling

White box modelling refers to a paradigm in which everything that is known about the reference system is utilized when creating its digital model. For analog audio circuits, this includes the schematic of the circuit, the characteristics of each individual component, and even the context in which the circuit is used. Models created using such methods are derived directly from the physical properties of the reference system, so it is often referred to as "physical modelling". Physical models are often less abstract than black-box models and can often accommodate real-time control in an intuitive manner. Physical modelling techniques have been applied to a myriad of musical systems, including acoustic instruments [114–116], analog circuits [14, 18, 23, 29, 31, 117], and electromechanical devices [41–43, 118]. Several physical modelling techniques are outlined in the sub-sections to follow.

Port-Hamiltonian Systems

The Port-Hamiltonian approach offers a systematic framework for analysis, control and simulation of complex physical systems, for lumped-parameter as well as for distributed-parameter models [119]. Unlike other modelling methods, Port-Hamiltonian Systems (PHS) offer guaranteed stability and passivity when simulating non-linear circuits.

PHS are an extension of classical Hamiltonian systems. They model open dynamical systems made of energy storage components, dissipative components, and connection ports through which energy can flow. This leads to a state space representation of multi-physics systems structured according to energy flow, thus encoding the passivity property including non-linear cases [120]. Using an explicit or implicit numerical scheme, the continuous-time

PHS can be discretized into a digital model with guaranteed passivity and therefore stability. A recent publication explores the use of an ad hoc second-order numerical scheme that discretizes the Hamiltonian gradient and results in an accurate, guaranteed-passive digital simulation [121].

The implementation of PHS in the context VA is still relatively new. A handful of port-Hamiltonian models have been described by Falaize and their collaborators, including guitar effects pedals [11, 12], loudspeakers [38, 39, 122], parts of electro-mechanical pianos [120, 123], and most recently, individual electronic components such as the operational amplifier [32].

While PHS holds great promise for modelling both lumped and multi-physics systems, a systematic method for model derivation does not currently exist. Therefore, each system must be derived by hand, making PHS impractical for many applications.

Wave Digital Filters

Wave Digital Filters (WDFs) are another white-box modelling framework that has seen widespread adaptation amongst VA researchers in recent years. It is highly favoured for its inherent modularity, systematic procedure for model derivation, and its excellent numeric and energetic properties [124]. WDFs were developed out of the scattering formalism as applied to classical circuit theory [125]. This involves transforming Kirchhoff variables into wave variables, and the impedance matrices describing the interconnections between ports into a “scattering matrix”, also referred to as an “S-matrix”. The notation of wave variables is commonly used in microwave engineering to this day [126].

WDFs were first described in the literature by Fettweis in the late 1960s and 1970s as a means of translating analog filters to the digital domain [127]. They did not appear in the VA literature until 1987 [128] when Smith recognized their connection to digital waveguides [129] - a popular, well-described method for creating physical models of acoustic instruments. Since then, the use of WDF for the simulation of several acoustic instrument systems have been described in the literature, including the piano hammer [130, 131], the tone-hole [132], and the reed [133].

Representing a Lumped-element electrical circuit by a wave-digital structure requires a linear transformation from Kirchhoff variables to wave variables: the incident and reflected wave at each port. Many wave variable representations exist, but voltage, current, and power-normalized waves are the most common. From there, the components are digitized using an s-z mapping. While many can be used, the standard bilinear transform is still heavily favoured amongst VA researchers [134]. Critically, the energetic properties of a given reference circuit are preserved throughout the discretization. And, the topology of the reference circuit is always inherited by the digital filter structure [135].

Until recently, modelling non-linear audio circuits in the WDF formalism was very difficult and often times impractical. Over time, researchers developed methods for side-stepping these limitations. Meerkötter and Scholz were the first to attempt the problem, developing a method for simulating up to one non-linearity [136]. From there, researchers have been able to push that limitation by exploiting the topologies of the reference circuit [56, 137–139], introducing unit delays to the circuit [28, 117, 139, 140], simplifying non-linear devices [56, 141], and using global iteration techniques [142, 143]. Along with the development of these techniques, works have been published describing WDF models of electronic components including audio transformers [34], triodes, i.e. Field Effect Transistors (FETs) and vacuum tubes [28, 117, 139], diodes [33, 138], operational amplifiers [33, 144], and Operation Transconductance Amplifiers (OTAs) [145]. An overview of common non-linear components is given by Bogason in [135]. Simulations of entire circuits have also been described, including the bridged-T resonator [144, 146], the Fender Bassman amplifier [29, 30], and the Fairchild 670 limiter [147].

In [14], Werner proposed a generalized, systematic method that overcomes the aforementioned limitations, allowing arbitrary topologies with any number of non-linearities to be simulated. This method works by collecting all non-linear elements into a single vector that interfaces with the rest of the circuit using an R-type adaptor. The K method [116], table lookup, or a Newton-Raphson iterative solver [148] can then be used to resolve the relationship between the vector and the rest of the structure.

While this method is generalized and complete, it ultimately devolves into an approach that strongly resembles the state space modelling approach, while also requiring the transformation of the system from the wave domain to the Kirchhoff domain.

2.4 State Space Modelling

While state space formalism has its roots in modern control theory, it has been adapted for real-time audio circuit simulation by VA researchers. This modelling framework allows models of electrical circuits to be derived directly from circuit schematics, using the component models found in generic circuit simulators. In this section, a brief history of state space modelling in VA is given, followed by an overview of its fundamental principles. Finally, the NDK method is formally introduced, which, along with some notable extensions, enables a structured approach for deriving and solving the state variables of a non-linear system of Ordinary Differential Equations (ODEs) using numerical integration [68, 69]. This method, along with some extensions e.g. [18, 71], has been successfully deployed by VA researchers to derive and simulate state space models of vintage musical equipment and acoustic instruments.

2.4.1 History

The age of modern control theory was ushered in with the launching of the first Sputnik in 1957. This achievement of Soviet technology focused attention of scientists and engineers in general, and the automatic-control community in particular, eastward towards the USSR. In turning their attention to the Soviet Union, control system scientists and engineers discovered a different approach to control theory than the approach with which they were familiar. Differential equations replaced transfer functions for describing the dynamics of processes; stability was approached via the theory of Liapunov instead of the frequency-domain methods of Bode and Nyquist; optimization of system performance was studied by the special form of the calculus of variations developed by Pontryagin instead of by the Wiener-Hopf methods of an earlier era [149].

In the years to follow, this new so-called “state space” approach to control theory was adopted by western scientists and engineers for modelling dynamic systems, making a tremendous impact in countless fields of research, including, of course, the field of VA. State space modelling found its way into the VA literature in the early 90’s when Matignon and Depalle used state space formalism as a means of bridging physical models and signal modelling methods [114, 115]. Soon after, Borin proposed the "K method", a state space approach for modelling non-linear acoustic systems, so-called for its use of Kirchhoff variables which are more commonly used to describe electric circuits [116].

Following the advent of the K method, researchers began recognising the merits of state space formalism for the simulation of audio circuits. This realization was of particular interest to researchers looking to model guitar pedals and amplifiers, e.g., [17–19, 22, 23, 31]. The next notable advancement came from Yeh [13, 68] who proposed an extended version on the K method more specific to modelling audio circuits: the NDK method. Combined with extensions proposed by Holters [18, 71], the NDK method remains a popular choice for the construction and simulation of state space models of audio circuits.

2.4.2 Fundamental Principles

A state space model is a series of equations that describes the behaviour of a dynamic system based on the first-order derivative of the state equation, and the current system inputs. For a LTI system, the general expression is given as:

$$\begin{aligned} \dot{\boldsymbol{x}}(t) &= \boldsymbol{\mathfrak{A}}\boldsymbol{x}(t) + \boldsymbol{\mathfrak{B}}\boldsymbol{u}(t) \\ \boldsymbol{y}(t) &= \boldsymbol{\mathfrak{C}}\boldsymbol{x}(t) + \boldsymbol{\mathfrak{D}}\boldsymbol{u}(t) \end{aligned} \tag{2.57}$$

where $\boldsymbol{x}(t), \boldsymbol{u}(t), \boldsymbol{y}(t)$ represent the internal state, input, and output vector, respectively:

$$\boldsymbol{x}(t) = \begin{bmatrix} x_1(t) \\ \vdots \\ x_k(t) \end{bmatrix} \quad \boldsymbol{u}(t) = \begin{bmatrix} u_1(t) \\ \vdots \\ u_l(t) \end{bmatrix} \quad \boldsymbol{y}(t) = \begin{bmatrix} y_1(t) \\ \vdots \\ y_m(t) \end{bmatrix} \tag{2.58}$$

and $\dot{\boldsymbol{x}}(t)$ is the first-order time derivative of the state vector, $\frac{d}{dt}\boldsymbol{x}(t)$. $\boldsymbol{\mathfrak{A}}, \boldsymbol{\mathfrak{B}}, \boldsymbol{\mathfrak{C}}$, and $\boldsymbol{\mathfrak{D}}$ represent the system matrices, derived directly from the topology and the parameters of the system. It can be inferred that the matrix $\boldsymbol{\mathfrak{A}}$, called the "dynamics matrix", must be a square $k \times k$ matrix, since the vectors $\boldsymbol{x}(t)$ and $\dot{\boldsymbol{x}}(t)$ are necessarily of equal length. The matrix $\boldsymbol{\mathfrak{B}}$, called the "control matrix", need not be square. Since there are typically more state variables than system inputs, i.e. $k \gg l$, $\boldsymbol{\mathfrak{B}}$ tends to be a tall, thin matrix [149].

The system outputs tend to be quantities that can be *observed*, i.e. measured by means of a suitable sensor. Accordingly, the matrix $\boldsymbol{\mathfrak{C}}$ is called the "observation matrix" [149]. Finally, the presence of the matrix $\boldsymbol{\mathfrak{D}}$ indicates a direct connection between the input $\boldsymbol{u}(t)$ and the output $\boldsymbol{y}(t)$, earning it the name "direct link matrix" [115]. While there is no general reason for the $\boldsymbol{\mathfrak{D}}$ matrix to be absent in practical applications, it is absent in the overwhelming majority of applications [149]. This is not unexpected, as the input of the system is typically known or controlled, and therefore does not need to be "observed".

Upon deriving the system matrices, the system can be simulated simply by defining (or measuring) a set of initial conditions, driving the system with input vectors, and calculating the output vector using the system of equations.

In discrete-time, equation 2.57 can be expressed as:

$$\begin{aligned} \boldsymbol{x}[n+1] &= \boldsymbol{A}\boldsymbol{x}[n] + \boldsymbol{B}\boldsymbol{u}[n] \\ \boldsymbol{y}[n] &= \boldsymbol{C}\boldsymbol{x}[n] + \boldsymbol{D}\boldsymbol{u}[n] \end{aligned} \tag{2.59}$$

where the continuous time, t, is replaced by the discrete-time step, n, and the first order derivative, $\dot{\boldsymbol{x}}(t)$, is replaced by the state vector at the next time step.

While the above equations are valid for LTI systems, most physical system exhibit some non-linear behaviour. To incorporate such behaviour, equation 2.59 is extended to include a non-linear component:

$$\boldsymbol{x}[n+1] = \boldsymbol{A}\boldsymbol{x}[n] + \boldsymbol{B}\boldsymbol{u}[n] + \boldsymbol{C}\boldsymbol{i} \tag{2.60}$$

$$\boldsymbol{y}[n] = \boldsymbol{D}\boldsymbol{x}[n] + \boldsymbol{E}\boldsymbol{u}[n] + \boldsymbol{F}\boldsymbol{i} \tag{2.61}$$

$$\boldsymbol{v}[n] = \boldsymbol{G}\boldsymbol{x}[n] + \boldsymbol{H}\boldsymbol{u}[n] + \boldsymbol{K}\boldsymbol{i} \tag{2.62}$$

$$\boldsymbol{i} = \boldsymbol{f}(\boldsymbol{v}) \tag{2.63}$$

where $\boldsymbol{f}(\boldsymbol{v})$ is the non-linear vector function, and $\boldsymbol{v}[n]$ is a vector representing the non-linear state variables. The matrices $\boldsymbol{G}$, $\boldsymbol{H}$, and $\boldsymbol{K}$ define the linear combination of the state variables, input, and non-linear function, respectively, that contributes to the non-linear state variables. The symbols $\boldsymbol{i}$ and $\boldsymbol{v}$ are used deliberately, as many non-linear electronic components (including the BJT) are voltage-controlled current devices, having a non-linear mapping from control voltage to output current.

The steps involved in solving this system are more complex than that of the linear state space system. The process as defined in [18] is as follows for the current time step, n:

1. Calculate $\boldsymbol{p}[n] = \boldsymbol{G}\boldsymbol{x}[n] + \boldsymbol{H}\boldsymbol{u}[n]$
2. Numerically solve $\boldsymbol{p}[n] + \boldsymbol{K}\boldsymbol{i} - \boldsymbol{v}[n] = 0$ together with equation 2.63 to obtain $\boldsymbol{i}$, e.g., using the Newton-Raphson Method [148]
3. Compute the output with equation 2.61
4. Perform the state update with equation 2.60

No longer can a closed-form solution to the ODE simply be calculated by basic arithmetic - a numerical solution must be estimated using an iterative solver. The implications of such will be discussed in the chapters to follow.

2.4.3 The Nodal DK Method

The NDK method [68] is a systematic approach for deriving a state space model from an electric circuit that bares a strong resemblance to Modified Nodal Analysis (MNA) [70]. It starts by applying a discretization scheme to the energy storage elements (i.e. capacitors and inductors) in the circuit, turning the voltage across/current through these elements into the *state variables* of the system. Next, the so-called *incidence* and *admittance* matrices are derived by systematically analysing the nodal connections of each circuit element. Finally, these matrices are combined to realize the constant matrices of the non-linear state space system as defined in equations 2.60 - 2.62.

Modified Nodal Analysis

MNA was first described by Ho in [70] as a systematic way of deriving a circuit's equations for computer-aided analysis. This approach is still used by generic circuit solvers e.g. SPICE. For a circuit containing only linear elements and independent sources, its circuit equations are expressed by the system:

$$\boldsymbol{Y}\boldsymbol{v} = \boldsymbol{I} \tag{2.64}$$

where $\boldsymbol{Y}$ is the admittance matrix[2], $\boldsymbol{v}$ is a vector representing the voltages of the N nodes in the circuit, and $\boldsymbol{I}$ is also a vector of length N, containing a non-zero entry for any nodes with a current source attached to them. Each row of the system describes one node in the circuit, and solving the system for $\boldsymbol{v}$ allows the node voltages of the circuit to be found. The $\boldsymbol{Y}$ matrix is populated systematically by adding a "stamp" for each component from the corresponding entry on a list of rules, largely derived from Kirchhoff's Current Law (KCL). Each component also contributes a row to $\boldsymbol{v}$ and $\boldsymbol{I}$. Additional rows are also added for additional unknowns, i.e. the current flowing through a voltage source, which require an auxiliary equation to be solved.

Companion Circuits

This approach of populating a system matrix, with some extensions, is also taken by the NDK method to find the constant matrices of the non-linear state space model. To begin, the discretization scheme as outlined in [18] is applied to each capacitor and inductor in the circuit. Since no inductors are found in this work, only the capacitor is considered here. The $i - v$ relationship of a capacitor in the time domain is defined as:

$$i_C = C\frac{\mathrm{d}v_C}{\mathrm{d}t} \tag{2.65}$$

where the current through a capacitor is proportional to the time-derivative of its voltage. By applying the trapezoidal discretization scheme, the discrete-time approximation is found:

$$\frac{1}{2}(i_C[n] + i_C[n-1]) = \frac{C}{T_s}(v_C[n] - v_C[n-1]) \tag{2.66}$$

where T_s is the sampling interval. Solving for the current at time step n gives:

$$i_C[n] = \frac{2C}{T_s}(v_C[n] - v_C[n-1]) - i_C[n-1] \tag{2.67}$$

[2] Admittance is the inverse of electrical impedance, i.e. $Z = \frac{1}{Y}$

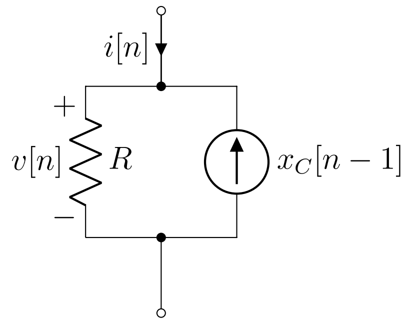


Fig. 2.14 Companion circuit for energy storage elements.

Note that the current at time step n is dependent upon the voltage and current from the previous time step. Holters then defines the canonical state, $x_C[n]$, as:

$$x_C[n] = i_C[n] + \frac{2C}{T_s} v_C[n] \tag{2.68}$$

Substituting the canonical state into equation 2.67 then yields:

$$x_C[n] - \frac{2C}{T_s} v_C[n] = \frac{2C}{T_s} v_C[n] - x_C[n-1] \tag{2.69}$$

leading to the final state update equation:

$$x_C[n] = 2\frac{2C}{T_s} v_C[n] - x_C[n-1] \tag{2.70}$$

By substituting the state update equation into equation 2.68, the current flowing through a capacitor is defined as a function of its voltage, and previous canonical state:

$$i_C[n] = \frac{2C}{T_s} v_c[n] - x_C[n-1] \tag{2.71}$$

This relationship allows every capacitor to be represented as a resistor and a current source, as shown in figure 2.14. The current source depends on the previous time-step, thereby holding the state information. The resistance is a function of the capacitance and the sampling interval, i.e. $R = T_s/2C$.

Deriving System Matrices

Having transformed each energy storage element into a resistor and current source, the system matrices can now be defined. Classical MNA is extended to include non-linear elements, and the circuit's equations are re-formatted slightly. The system matrices are defined by letting each row equal the KCL equation of a node in the circuit. The system is defined in [18] as follows, where $\boldsymbol{N_R}$, $\boldsymbol{N_x}$, $\boldsymbol{N_u}$, and $\boldsymbol{N_n}$ represent the incident matrices of the resistors, state elements, input sources, and non-linear elements, respectively:

$$(\boldsymbol{N_R^T Y_R N_R} + \boldsymbol{N_x^T Y_x N_x})\boldsymbol{v} + \boldsymbol{N_u^T i_u} = \boldsymbol{N_x^T x} + \boldsymbol{N_n^T i_n} \tag{2.72}$$

where the vector $\boldsymbol{v}$ again represents the unknown node voltages, $\boldsymbol{i_u}$ is a vector of unknown voltage source currents, $\boldsymbol{x}$ is the state vector, and $\boldsymbol{i_n}$ is currents of the non-linear elements. The matrices $\boldsymbol{G_R}$ and $\boldsymbol{G_x}$ are the aforementioned admittance matrices, containing the admittance of each resistor and storage element, respectively, along their major diagonal. For a circuit with M resistors and P capacitors, they are expressed as:

$$\boldsymbol{Y_R} = \mathrm{diag}(\frac{1}{R_1}, \frac{1}{R_2}, \ldots, \frac{1}{R_M}) \qquad \boldsymbol{Y_x} = \mathrm{diag}(\frac{2C_1}{T_s}, \frac{2C_2}{T_s}, \ldots, \frac{2C_P}{T_s}) \tag{2.73}$$

Each incidence matrix contains a row per element, and column per node in the circuit (excluding the reference "ground" node). There are at most two entries per element row that are non-zero: a 1 in the column of the node where the positive pole of the element is connected, and a -1 where the negative pole is connected. Connections to the reference node are omitted. Passive elements with no polarity may be placed at will, while polarized elements (i.e. voltage sources, non-linear elements) must be placed as per their directionality on the schematic.

By exploiting the known relationships between voltage sources and the node voltages, the system equation can be re-written as follows:

$$\boldsymbol{S}\begin{pmatrix}\boldsymbol{v}\\ \boldsymbol{i_u}\end{pmatrix} = \begin{pmatrix}\boldsymbol{N_x^T}\\ \boldsymbol{0}\end{pmatrix}\boldsymbol{x} + \begin{pmatrix}\boldsymbol{0}\\ \boldsymbol{I}\end{pmatrix}\boldsymbol{u} + \begin{pmatrix}\boldsymbol{N_n^T}\\ \boldsymbol{0}\end{pmatrix}\boldsymbol{i_n} \tag{2.74}$$

where $\boldsymbol{u}$ is the input source vector, the $\boldsymbol{0}$ and $\boldsymbol{I}$ matrices are sized by context, and $\boldsymbol{S}$ is the system matrix, which can be expressed as a combination of the incident and admittance matrices:

$$\boldsymbol{S} = \begin{pmatrix} \boldsymbol{N_R^T Y_R N_R} + \boldsymbol{N_x^T Y_x N_x} & \boldsymbol{N_u^T} \\ \boldsymbol{N_u} & \boldsymbol{0} \end{pmatrix} \tag{2.75}$$

By left-multiplying both sides by $\boldsymbol{S^{-1}}$, the node voltages of the system may be found. Further, by multiplying by their respective incident matrix, the voltages across the energy storage elements, the non-linear elements, and the output voltage, denoted by $\boldsymbol{v_x}$, $\boldsymbol{v_n}$ and $\boldsymbol{v_o}$, respectively, are obtained. $\boldsymbol{N_o}$ is a $1 \times N$ vector with a single non-zero entry at the output node:

$$\boldsymbol{v_x} = \begin{pmatrix} \boldsymbol{N_x} & \boldsymbol{0} \end{pmatrix} \boldsymbol{v_S} \tag{2.76}$$

$$\boldsymbol{v_n} = \begin{pmatrix} \boldsymbol{N_n} & \boldsymbol{0} \end{pmatrix} \boldsymbol{v_S} \tag{2.77}$$

$$\boldsymbol{v_o} = \begin{pmatrix} \boldsymbol{N_o} & \boldsymbol{0} \end{pmatrix} \boldsymbol{v_S} \tag{2.78}$$

where $\boldsymbol{v_S}$ is the column vector of the calculated node voltages, defined as:

$$\boldsymbol{v_S} = \boldsymbol{S}^{-1} \left(\begin{pmatrix} \boldsymbol{N_x^T} \\ \boldsymbol{0} \end{pmatrix} \boldsymbol{x} + \begin{pmatrix} \boldsymbol{0} \\ \boldsymbol{I} \end{pmatrix} \boldsymbol{u} + \begin{pmatrix} \boldsymbol{N_n^T} \\ \boldsymbol{0} \end{pmatrix} \boldsymbol{i_n} \right) \tag{2.79}$$

From here, the state space system defined by equations 2.60 - 2.63 may be formulated. First, the capacitor state update equation (eq 2.70) is re-written for the complete system[3]:

$$\boldsymbol{x}[n] = 2\boldsymbol{Y_x v_x}[n] - \boldsymbol{x}[n-1] \tag{2.80}$$

[3]For systems containing inductors, $\boldsymbol{Y_x v_x}[n]$ is left-multiplied by a matrix $\boldsymbol{Z}$, a diagonal matrix with a 1 for each capacitor and -1 for each inductor. For circuits with no inductors, $\boldsymbol{Z} = \boldsymbol{I}$, and may therefore be omitted, as here.

The system matrices $\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$ for the state update equation (2.60) are therefore:

$$\boldsymbol{A} = 2\boldsymbol{Y_x}\begin{pmatrix}\boldsymbol{N_x} & \boldsymbol{0}\end{pmatrix}\boldsymbol{S}^{-1}\begin{pmatrix}\boldsymbol{N_x} & \boldsymbol{0}\end{pmatrix}^T - \boldsymbol{I} \tag{2.81}$$

$$\boldsymbol{B} = 2\boldsymbol{Y_x}\begin{pmatrix}\boldsymbol{N_x} & \boldsymbol{0}\end{pmatrix}\boldsymbol{S}^{-1}\begin{pmatrix}\boldsymbol{0} & \boldsymbol{I}\end{pmatrix}^T \tag{2.82}$$

$$\boldsymbol{C} = 2\boldsymbol{Y_x}\begin{pmatrix}\boldsymbol{N_x} & \boldsymbol{0}\end{pmatrix}\boldsymbol{S}^{-1}\begin{pmatrix}\boldsymbol{N_n} & \boldsymbol{0}\end{pmatrix}^T \tag{2.83}$$

Similarly, the matrices $\boldsymbol{D}$, $\boldsymbol{E}$, and $\boldsymbol{F}$ are obtained for equation 2.61, which calculates the output voltage:

$$\boldsymbol{D} = \begin{pmatrix}\boldsymbol{N_o} & \boldsymbol{0}\end{pmatrix}\boldsymbol{S}^{-1}\begin{pmatrix}\boldsymbol{N_x} & \boldsymbol{0}\end{pmatrix}^T - \boldsymbol{I} \tag{2.84}$$

$$\boldsymbol{E} = \begin{pmatrix}\boldsymbol{N_o} & \boldsymbol{0}\end{pmatrix}\boldsymbol{S}^{-1}\begin{pmatrix}\boldsymbol{0} & \boldsymbol{I}\end{pmatrix}^T \tag{2.85}$$

$$\boldsymbol{F} = \begin{pmatrix}\boldsymbol{N_o} & \boldsymbol{0}\end{pmatrix}\boldsymbol{S}^{-1}\begin{pmatrix}\boldsymbol{N_n} & \boldsymbol{0}\end{pmatrix}^T \tag{2.86}$$

And finally, the remaining system matrices, $\boldsymbol{G}$, $\boldsymbol{H}$, and $\boldsymbol{K}$ from the non-linear state equation (2.62) are defined as:

$$\boldsymbol{G} = \begin{pmatrix}\boldsymbol{N_n} & \boldsymbol{0}\end{pmatrix}\boldsymbol{S}^{-1}\begin{pmatrix}\boldsymbol{N_x} & \boldsymbol{0}\end{pmatrix}^T - \boldsymbol{I} \tag{2.87}$$

$$\boldsymbol{H} = \begin{pmatrix}\boldsymbol{N_n} & \boldsymbol{0}\end{pmatrix}\boldsymbol{S}^{-1}\begin{pmatrix}\boldsymbol{0} & \boldsymbol{I}\end{pmatrix}^T \tag{2.88}$$

$$\boldsymbol{K} = \begin{pmatrix}\boldsymbol{N_n} & \boldsymbol{0}\end{pmatrix}\boldsymbol{S}^{-1}\begin{pmatrix}\boldsymbol{N_n} & \boldsymbol{0}\end{pmatrix}^T \tag{2.89}$$

The NDK method, then, is a generalized, systematic approach for obtaining the system matrices of the non-linear state space system for most electric circuits. In combination with equation 2.63, as defined by the non-linear elements of the circuit being modelled, the system may now be simulated.

2.4.4 Real-Time Simulation and Variable Parts

While obtaining the system matrices for a circuit is paramount for creating its state space model, other considerations must be taken into account in order to simulate it. One of the biggest advantages of white-box modelling approaches is the ease with which control parameters of the physical system being can be mapped to parameters of the model. Furthermore, it is often desirable that these parameters be controllable in real-time. The NDK method is reasonably compact at run-time, as the inverse of the system matrix, $\boldsymbol{S^{-1}}$ may be pre-computed ahead of time - assuming the system remains constant. To enable real-time control, though, this assumption does not hold, and recalculating the system matrices using a straight-forward approach would become computationally expensive.

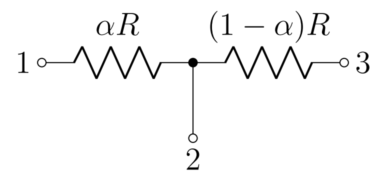


Fig. 2.15 Schematic of a potentiometer.

In [18], a method is proposed to more efficiently handle the modelling of variable parts, namely potentiometers, in a non-linear state space model. This is achieved by separating the system matrix into its static and variable parts, which requires just a small part of the matrix to be recalculated and inverted at each time step. A potentiometer forms a voltage divider with two variable resistors tied to a common node called the “wiper”. The resistance of each is a function of the rotational position, $\alpha \in [0, 1]$, of the potentiometer. As the pot is swept, one resistance increases while the other decreases by a common factor, as shown in figure 2.15.

To model potentiometers using the NDK method, the system matrix, $\boldsymbol{S}$, is re-defined as the sum of a static matrix, $\boldsymbol{S_o}$, and the variable component:

$$\boldsymbol{S} = \boldsymbol{S_o} + \begin{pmatrix} \boldsymbol{N_v} & \boldsymbol{0} \end{pmatrix}^T \boldsymbol{R_v^{-1}} \begin{pmatrix} \boldsymbol{N_v} & \boldsymbol{0} \end{pmatrix} \tag{2.90}$$

where $\boldsymbol{S_o}$ is simply the previous definition of $\boldsymbol{S}$ from equation 2.75, and $\boldsymbol{R_v}$ is a diagonal *impedance* (as opposed to admittance) matrix, i.e:

$$\boldsymbol{R_v} = \mathrm{diag}(\alpha R, (1-\alpha)R) \tag{2.91}$$

Defining the variable resistance this way avoids division by 0 when α equals 0 or 1. Then, by applying the Woodbury identity [150] to equation 2.90, the inverse of the system matrix is then re-defined as:

$$\boldsymbol{S^{-1}} = \boldsymbol{S_o^{-1}} - \boldsymbol{S_o^{-1}} \begin{pmatrix} \boldsymbol{N_v} & \boldsymbol{0} \end{pmatrix}^T (\boldsymbol{R_v} + \boldsymbol{Q})^{-1} \begin{pmatrix} \boldsymbol{N_v} & \boldsymbol{0} \end{pmatrix} \boldsymbol{S_o^{-1}} \tag{2.92}$$

We may then re-define the state space system matrices, (equations 2.81 - 2.89) using this re-defined system matrix. These re-defined system matrices require only the inversion of the relatively small matrix, $(\boldsymbol{R_v} + \boldsymbol{Q})$, at each time step, where $\boldsymbol{Q}$ is:

$$Q = \begin{pmatrix} \boldsymbol{N_v} & \boldsymbol{0} \end{pmatrix} \boldsymbol{S_o^{-1}} \begin{pmatrix} \boldsymbol{N_v} & \boldsymbol{0} \end{pmatrix}^T \tag{2.93}$$

For circuits containing a single potentiometer, $(\boldsymbol{R_v} + \boldsymbol{Q})$ is a 2×2 matrix, which is nearly-trivial to invert at each time step. For an overview of all the re-defined system matrices, the reader is referred to [18].

2.5 Summary

In this chapter, important concepts relevant to the research carried out in this work were reviewed. Namely, an introduction to the BJT was given, including some historical context and its basic operation, followed by a review of the small signal model, some commonly-used BJT audio circuits, and some popular BJT macro-models for computational simulation. Next, a review of the state of the art of VA modelling was presented. The two primary paradigms of VA modelling, black-box and white-box modelling were introduced, followed by a review of some modelling techniques and the literature therein. Particular emphasis was given to reviewing state space modelling, as that was the modelling method selected for this work. This introduction to both BJTs and VA modelling provides important context for the discussions to follow in chapter 3 and 4.

Chapter 3

Case Study: Modelling the Common-Emitter Amplifier

3.1 Introduction

To contextualize some of the principles discussed in the previous chapter, we will now embark on a case study of a BJT audio circuit. In this case study, we will design a common-emitter amplifier, then construct and simulate a state space model of the circuit. We begin by re-visiting the schematic of the common-emitter amplifier, before designing the bias network and specifying the capacitors to meet the design specifications. Next, we identify all of the nodes of the circuit, create individual component models using the NDK method, and derive the system matrices. From there, we derive the non-linear state space system of equations and discuss considerations for real-time simulation, including the choice of iterative solver, and its initialization at each time step.

3.2 Designing a Common-Emitter Amplifier

In this section, we will design a common-emitter amplifier[1]. Resources on BJT amplifier design are widely available, and so some design "rules of thumb" and design assumptions will be used here without reference.

[1] The general design procedure followed here derives from this tutorial.

Our design problem is presented as follows:

Design a common-emitter amplifier for maximum gain using a PNP BJT with $\beta = 100$ *for use with a* 9V *battery. The amplifier must be capable of driving a* 25kΩ *load, and the frequency response should be suitable for use with an electric guitar. Standard resistor and capacitor values should be used throughout.*

3.2.1 Establishing the DC Bias Point

To start, the resistors of the circuit must be specified to establish an appropriate DC bias point. Since capacitors do not allow DC current to flow through them, they are replaced by open circuits for these calculations. The isolated DC bias network is shown in figure 3.1.

First, the load requirements are addressed. Since the amplifier must be capable of driving a load of $R_L = 25\text{k}\Omega$, its output impedance must not exceed the load resistance. The output impedance of the amplifier is set by R_C, so $R_C = 22\text{k}\Omega$ is selected, since 22kΩ is a standard resistor value that meets the load requirements. For a list of standard resistor values, see appendix A.

Next, the saturation current, $I_{C_{(SAT)}}$, is calculated, which occurs when $V_{EC} = 0$. This, of course, is a scenario to be avoided, as the BJT must operate in the active region to function as an amplifier. It is desirable for the emitter resistor to have some voltage drop across it to establish emitter degeneration. Here a 1V drop will be used. The saturation current is then calculated as:

$$I_{C_{(SAT)}} = \frac{V_E - V_{CC}}{R_C} = \frac{-1\,\text{V} - (-9\,\text{V})}{22\,\text{k}\Omega} \approx 363.6\,\mu\text{A}$$

To ensure that the BJT operates in the active region, the collector current should not approach $I_{C_{(SAT)}}$ (saturation region), or drop to 0 (cut-off region). So, the collector bias current, I_C, is set as $I_{C_{(SAT)}}/2$, i.e.:

$$I_C = I_{C_{(SAT)}}/2 = 181.8\,\mu\text{A}$$

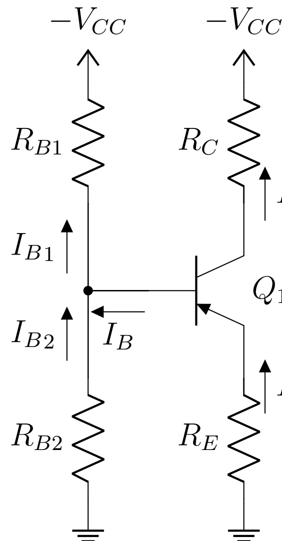


Fig. 3.1 The DC bias network of the common-emitter amplifier.

By using the relationship between emitter and collector current, the required emitter resistor is calculated as:

$$\begin{aligned} R_E = \frac{V_{R_E}}{I_E} &= \frac{V_E}{(\frac{\beta+1}{\beta})I_C} \\ &= \frac{0-(-1\,\mathrm{V})}{1.01 \times 181.8\,\mu\mathrm{A}} \\ &= 5446.09\,\Omega \end{aligned}$$

and $R_E = 5.1\mathrm{k}\Omega$ is selected as the closest standard resistor to the calculated value. Recall from section 2.2.1 that when the EBJ is forward-biased, $V_{EB} \approx 0.6\,\mathrm{V}$. Since the emitter voltage was set as $V_E = -1\,\mathrm{V}$, the base voltage is therefore:

$$V_B = V_E - V_{EB} = -1.6\,\mathrm{V}$$

Moreover, the base current can be calculated using the collector current and the β of the BJT:

$$I_B = \frac{I_C}{\beta} = \frac{181.8\,\mu\mathrm{A}}{100} = 1.818\,\mu\mathrm{A}$$

From there, the base resistors, R_{B1} and R_{B2} are specified. Ultimately, it is the base current, established by these two resistors, that sets the DC bias point of the amplifier. It is therefore imperative that the base current remains stable. To ensure stability for a wide range of input signal amplitudes, the current flowing through the base resistors must be large compared to the base current itself. This prevents the base current from loading down the resistors. Having $I_{B2} = 10 \times I_B$ is generally considered sufficient. R_{B2} can therefore be calculated as:

$$R_{B2} = \frac{0 - V_B}{10 \times I_B} = \frac{1.6\,\mathrm{V}}{18.18\,\mu\mathrm{A}}$$
$$= 88\,008\,\Omega$$

where $R_{B2} = 82\mathrm{k}\Omega$ is selected as the closest standard value. A smaller resistor than the calculated value is selected here, instead of the nearest larger resistor, as a higher current through the base resistors branch provides more stability. Using KCL, the current flowing through R_{B1} is observed as $11 \times I_B$. Therefore, R_{B1} is calculated as:

$$R_{B1} = \frac{V_B - V_{CC}}{11 \times I_B} = \frac{-1.6\,\mathrm{V} - (-9\,\mathrm{V})}{19.998\,\mu\mathrm{A}}$$
$$= 370\,037\,\Omega$$

And $R_{B1} = 360\,\mathrm{k}\Omega$ is selected as the closest standard-value resistor of lower value. All resistors in the circuit have now been specified. Since approximations were made in order to select standard resistor values, it is important to verify the design to ensure that acceptable biasing was achieved. First, the actual base voltage may be calculated:

$$V_B = \left(\frac{R_{B2}}{R_{B1} + R_{B2}}\right)(-V_{CC}) = -1.67\,\mathrm{V}$$

which is well within acceptable tolerance of the previously calculated value. Next, the emitter current and collector current are verified:

$$I_E = \frac{0 - (V_B + 0.6\,\mathrm{V})}{R_E} = \frac{1.07\,\mathrm{V}}{5.1\,\mathrm{k}\Omega}$$
$$= 209.8\,\mu\mathrm{A}$$
$$I_C = \left(\frac{\beta}{\beta + 1}\right) I_E = \frac{209.8\,\mu\mathrm{A}}{1.01}$$
$$= 207.7\,\mu\mathrm{A}$$

The collector voltage can then be verified:

$$\begin{aligned} V_C &= (I_C R_C) - V_{CC} = (207.7\,\mu\text{A} \times 22\,\text{k}\Omega) - 9\,\text{V} \\ &= -4.43\,\text{V} \end{aligned}$$

which is close to half of the supply voltage, so the actual bias point is acceptable. Biasing the collector to half the supply voltage gives the signal maximum head room in both directions, which helps to avoid "clipping" of the output waveform.

Input Resistance

To aid in the calculation of the capacitor values, the input resistance looking into the base is evaluated using the small signal representation. To do so, any voltage sources in the circuit are replaced by a short circuit, and any current sources with an open circuit[2]. The small signal model of the DC bias circuit can then be visualised using the hybrid-π model, as shown in figure 3.2.

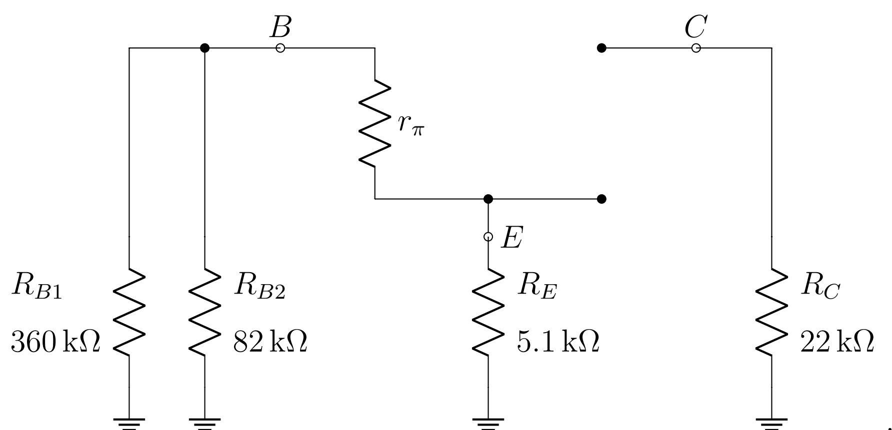


Fig. 3.2 Small signal model of the common-emitter amplifier's DC bias network. The DC voltage source is replaced by a short circuit, and the variable current source is replaced with an open circuit.

The transconductance and r_π of the circuit are calculated using the bias values found

[2]see appendix B for an explanation of this replacement

above, assuming $V_t = 25\,\text{mV}$:

$$g_m = \frac{I_C}{V_t} = 8.145\,\frac{\text{mA}}{\text{V}}$$
$$r_\pi = \frac{\beta}{g_m} = 12\,277\,\Omega$$

Then, the input resistance is calculated as:

$$\begin{aligned} R_{IN} &= (R_{B1}||R_{B2})\,||(r_\pi + R_E) \\ &= 13.79\,\text{k}\Omega \end{aligned}$$

The input resistance will be used in the following section to specify the input capacitor, determining the frequency response of the circuit.

3.2.2 Determining the Frequency Response

Having established the DC bias of the circuit, the input and output capacitors may now be specified. Furthermore, since the design specifies that the circuit have *maximum gain*, an emitter bypass capacitor will also be required, as shown in figure 2.6a. Since the amplifier is intended for use with a guitar, it should have a flat frequency response from approximately 100Hz - 10kHz. As such, the capacitor values will be tuned such that the circuit will not filter out these frequencies. For an introduction to basic filters in electronic circuits, see appendix B.

First, the input capacitor is specified. In conjunction with the input resistance, the input capacitor forms a *high-pass* filter. So, the 3 dB cut-off frequency of this filter should be around 100 Hz:

$$\begin{aligned} 2\pi f_{3\,\text{dB}} &= \frac{1}{R_{IN}C_{IN}} \\ 100\,\text{Hz} &= \frac{1}{2\pi(13.79\,\text{k}\Omega) \times C_{IN}} \\ C_{IN} &= 1.15 \times 10^{-7}\,\text{F} \end{aligned}$$

where $C_{IN} = 0.15\,\mu\text{F}$ is chosen as the closest standard value that is larger than the calculated value. The true cut-off frequency is therefore $f_{3\,\text{dB}} = 76.9\,\text{Hz}$. The output capacitor can be calculated in a similar manner using the load resistance, specified at 25kΩ:

$$
\begin{aligned}
100\,\mathrm{Hz} &= \frac{1}{2\pi(25\,\mathrm{k\Omega}) \times C_{out}} \\
C_{OUT} &= 6.37 \times 10^{-8}\ \mathrm{F}
\end{aligned}
$$

$C_{OUT} = 0.068\,\mu\mathrm{F}$ is taken as the nearest standard value. The emitter bypass capacitor also behaves as a high-pass filter. The general design rule is to specify the bypass capacitor such that its *reactance* is $R_E/10$ at the cut-off frequency. Therefore:

$$
\begin{aligned}
X_{C_E} &= \frac{1}{2\pi f_{3\,\mathrm{dB}} C_E} = R_E/10 \\
C_E &= \frac{1}{2\pi f_{3\,\mathrm{dB}}(R_E/10)} = \frac{1}{2\pi(100\,\mathrm{Hz})(5100/10)} \\
&= 3.12 \times 10^{-6}\ \mathrm{F}
\end{aligned}
$$

Rounding up to $C_E = 4.7\,\mu\mathrm{F}$ as the nearest standard value. Every component in the circuit has now been specified as per the design requirements. The final schematic with component values is shown in figure 3.3.

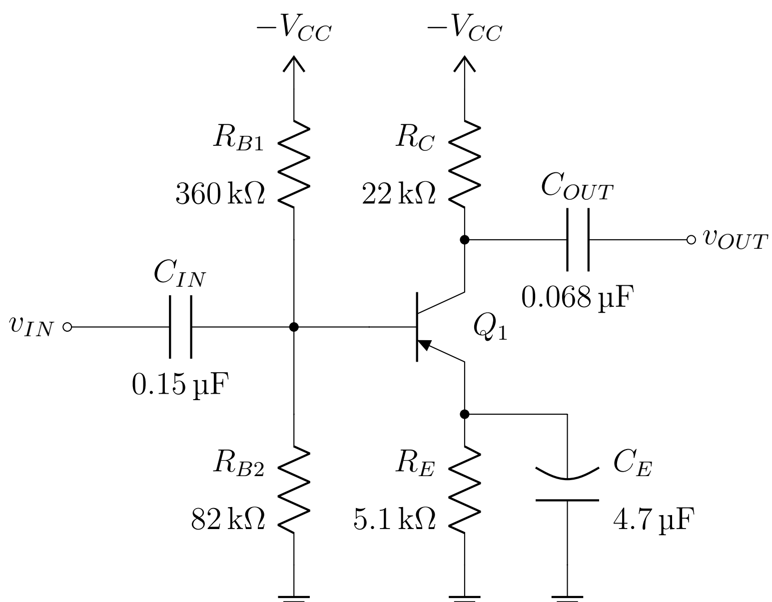


Fig. 3.3 Completed circuit of the common-emitter amplifier, shown with component values.

3.3 State Space Model Construction

Now that the schematic and the value of each component is finalized, it may be simulated by constructing a state space model of the circuit. To do so, each node of the circuit is labelled, and the incident and admittance matrices of the circuit are derived. This will enable the system matrices to be defined using the NDK method.

The nodes are numbered as shown in figure 3.4. The designed circuit is completed by the additions of a sinusoidal voltage source, v_{IN}, source resistor, R_S, load resistor, R_L, and DC voltage source, V_{CC}. The nodes are numbered such that the first two nodes are the voltage sources, and the last node is the output of the circuit. This is not a requirement, though it may help with organization when enumerating the nodes of a large circuit.

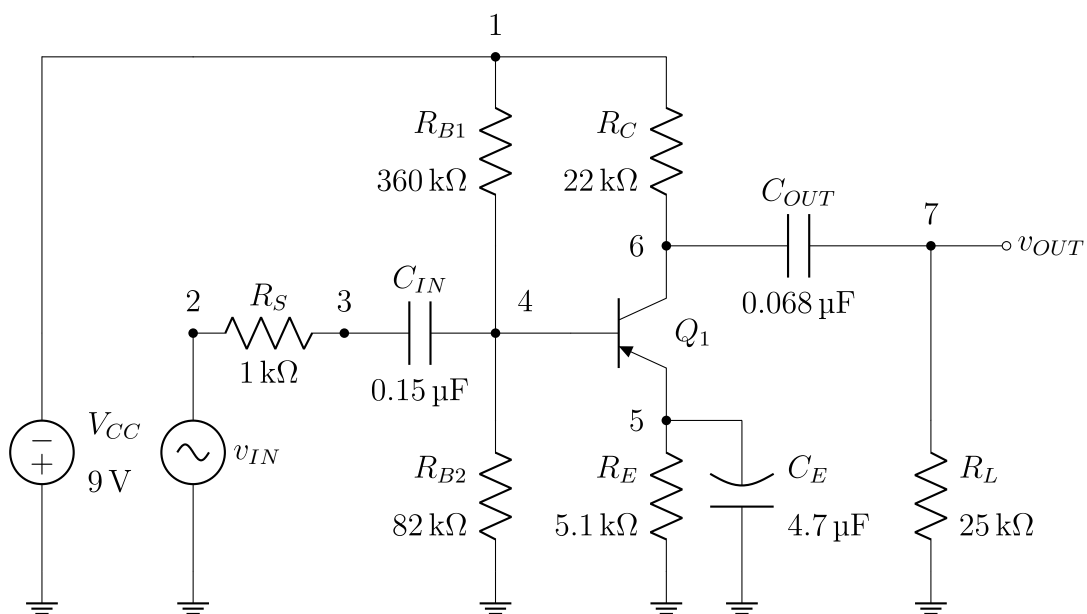


Fig. 3.4 Completed circuit of the common-emitter amplifier, shown with component values and labelled nodes.

3.3.1 Deriving System Matrices

First, the admittance matrices of the resistors and capacitors are calculated. They can be found using equation 2.73, defined as:

$$\boldsymbol{Y_R} = diag\left(\frac{1}{R_S}, \frac{1}{R_{B1}}, \frac{1}{R_{B2}}, \frac{1}{R_C}, \frac{1}{R_E}, \frac{1}{R_L}\right) \tag{3.1}$$

$$\boldsymbol{Y_x} = diag\left(\frac{2C_{IN}}{T_s}, \frac{2C_E}{T_s}, \frac{2C_{OUT}}{T_s}\right) \tag{3.2}$$

Next, the incident matrices, $\boldsymbol{N_R}$, $\boldsymbol{N_x}$, and $\boldsymbol{N_n}$ are found. Recall that each column of an incident matrix represents one node in the circuit (in this example, there are 7 nodes), and each row represents an element. A 1 or -1 is placed in the columns representing the nodes to which the element is connected. Further, the non-linear equations of the BJT must be considered. For this study, the EM model is used, which requires two non-linear equations to be solved at each time step, and two junction voltages to be monitored. Here, v_{EB} and v_{CB} are taken as the non-linear voltages. The incident matrices are therefore:

$$\boldsymbol{N_R} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.3}$$

$$\boldsymbol{N_x} = \begin{bmatrix} 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 \end{bmatrix} \tag{3.4}$$

$$\boldsymbol{N_n} = \begin{bmatrix} 0 & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & -1 & 0 \end{bmatrix} \tag{3.5}$$

Next, the two voltage inputs, V_{CC} and v_{IN}, are considered. To fully describe the circuit, it is noted that the node voltages to which the inputs are connected is already known at each time step, i.e.:

$$v_1 = V_{CC} \tag{3.6}$$

$$v_2 = v_{IN} \tag{3.7}$$

The input vector is therefore $\boldsymbol{u} = [V_{CC}\ v_{IN}]^T$. The incident matrix for the inputs, $\boldsymbol{N_u}$, can then be defined as:

$$\boldsymbol{N_u} = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.8}$$

Finally, the output incident matrix is defined, where node 7 is the output of the circuit:

$$\boldsymbol{N_o} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.9}$$

From there, the procedure as outlined in section 2.4.3 is followed to find the system matrix, $\boldsymbol{S}$, and derive the state space matrices $\boldsymbol{A}$ through $\boldsymbol{K}$. The calculated matrices are shown below. A state space model of the circuit has now been constructed, and the model can be simulated.

$$\boldsymbol{S} = \begin{bmatrix} 4.82\cdot10^{-5} & 0 & 0 & -2.78\cdot10^{-6} & 0 & -4.55\cdot10^{-5} & 0 & -1 & 0 \\ 0 & 0.001 & -0.001 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & -0.001 & 0.0539 & -0.0529 & 0 & 0 & 0 & 0 & 0 \\ -2.78\cdot10^{-6} & 0 & -0.0529 & 0.0529 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1.658 & 0 & 0 & 0 & 0 \\ -4.55\cdot10^{-5} & 0 & 0 & 0 & 0 & 0.0240 & -0.0239 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -0.0239 & 0.0240 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\boldsymbol{A} = \begin{bmatrix} 0.994 & 0 & 0 \\ 0 & 0.999 & 0 \\ 0 & 0 & 0.998 \end{bmatrix} \quad \boldsymbol{B} = \begin{bmatrix} 5.47\cdot10^{-6} & 2.95\cdot10^{-6} \\ 0 & 0 \\ -4.25\cdot10^{-6} & 0 \end{bmatrix} \quad \boldsymbol{C} = \begin{bmatrix} 1.969 & -1.969 \\ -1.999 & 0 \\ 0 & -0.9353 \end{bmatrix}$$

$$\boldsymbol{D} = \begin{bmatrix} 0 & 0 & -22.15 \end{bmatrix} \quad \boldsymbol{E} = \begin{bmatrix} -0.53 & 0 \end{bmatrix} \quad \boldsymbol{F} = \begin{bmatrix} 0 & -1.169\cdot10^{4} \end{bmatrix}$$

$$\boldsymbol{G} = \begin{bmatrix} 18.6125 & -0.603 & 0 \\ -18.6125 & 0 & -19.4941 \end{bmatrix} \quad \boldsymbol{H} = \begin{bmatrix} 0.0028 & -0.985 \\ 0.5295 & 0.985 \end{bmatrix}$$

$$\boldsymbol{K} = \begin{bmatrix} 1.0042\cdot10^{3} & -1.0036\cdot10^{3} \\ -1.0036\cdot10^{3} & 1.2715\cdot10^{4} \end{bmatrix}$$

3.4 Model Simulation

To simulate the state space model, the procedure outlined in section 2.4.2 is followed. The input signal is taken as a 480Hz, 10mV peak sine wave, sampled at a frequency of 48kHz.

Before simulating the model, there are some considerations to be made. Namely, an iterative solver, suitable for numerically solving the system at each time step must be chosen, and the initialization of the state variables at each time step must be considered.

3.4.1 Iterative Solvers

As mentioned in section 2.4.2, simulating a non-linear state space model requires the use of an iterative solver at each time step. Many solvers are described in the literature, e.g. [148, 151–153]. In general, the choice of algorithm may be considered a trade-off between robustness and computational cost. Naturally, algorithms that converge more reliably tend to have a higher computational cost.

Perhaps the most commonly used solver is the Newton-Raphson method ("Newton's method") [148], likely due to its ease of implementation. At a given time step, n, Newton's method, aims to find the optimal value of a vector, $\boldsymbol{v}$, and functions as follows:

$$\begin{aligned}
\boldsymbol{v_0} &= \text{initial guess} \\
\boldsymbol{g}[\boldsymbol{n}](\boldsymbol{v_m}) &= \boldsymbol{J}[\boldsymbol{n}](\boldsymbol{v_m})\boldsymbol{f}[\boldsymbol{n}](\boldsymbol{v_m}) \\
\boldsymbol{v_{m+1}} &= \boldsymbol{v_m} - \boldsymbol{g}[\boldsymbol{n}](\boldsymbol{v_m}), \quad m \in [0, 1, \ldots M-1] \qquad (3.10) \\
&\text{converges when:} \\
\boldsymbol{g}[\boldsymbol{n}](\boldsymbol{v_m}) &= \boldsymbol{0}
\end{aligned}$$

where $\boldsymbol{f}[\boldsymbol{n}](\boldsymbol{v_m})$ is the vector of non-linear functions at time step n, $\boldsymbol{J}[\boldsymbol{n}](\boldsymbol{v_m})$ is the Jacobian, and $\boldsymbol{v_m}$ is the proposed solution vector at iteration m, where M is the number of iterations required to converge on a solution. The solution vector is represented here as $\boldsymbol{v}$ deliberately, because in the case where the state space model represents an electric circuit, $\boldsymbol{v}$ is a vector of the node voltages of the schematic.

Ideally, the optimal solution is found when the residual function, $\boldsymbol{g}[\boldsymbol{n}](\boldsymbol{v_m})$, equals zero. In the interest of computational time, though, convergence is often accepted when the absolute value of the residual function is less than some tolerance, i.e.:

$$|\boldsymbol{g}[\boldsymbol{n}](\boldsymbol{x_m})| \leq \text{tol} \qquad (3.11)$$

where "tol" is some small, user-defined value, e.g. 10^{-12}. An example of Newton's method converging on a solution is shown in figure 3.5 where the y-axis is the residual function, and the x-axis is the iteration number, m.

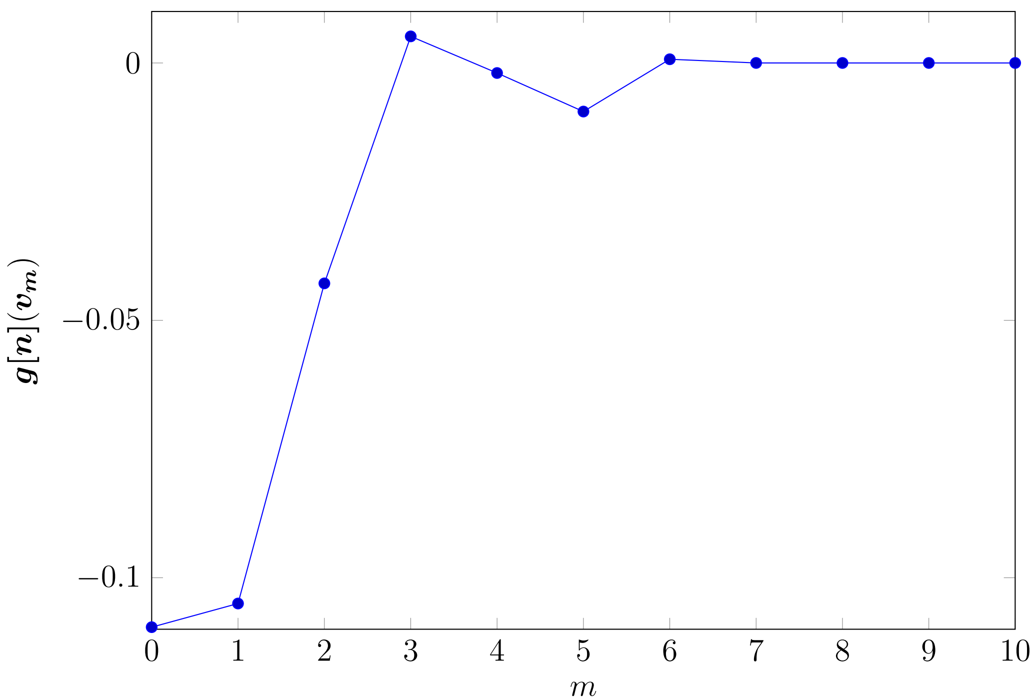


Fig. 3.5 Example of a convergent pattern of Newton's method with a good-quality initial guess.

Initializing the Iterative Solver

While it is relatively straight-forward in principle, Newton's method has some drawbacks. Its ability to converge is heavily reliant on the quality of the initial guess. Unfortunately, though, there is no generalized, systematic method for calculating a good initial guess for a given state space system - it must be inferred from the particular model. For some state space models, initializing the solver using the result from the previous time step may be sufficient, but for high-frequency inputs and non-linear systems, the previous result may not serve as a good initial guess. In [21], some methods for calculating a well-conditioned initial guess through analysis of the circuit are proposed, but they are not generalized methods.

As such, many iterative solvers [151, 152] are extensions to the basic Newton's method, whose aim is to alleviate the burden of well-initializing the solver by improving its robustness. Implementing a robust algorithm, however, may increase the computational cost of the simulation, making it unsuitable for real-time simulation.

3.5 Results

The model was constructed in the "Julia" programming language, a "flexible dynamic language, appropriate for scientific and numerical computing, with performance comparable to traditional statically-typed languages" [3]. Julia provides developers with many exceptional features, though it was primarily chosen for this work as it allowed use of the Analog Circuit Modeling and Emulation for Julia (ACME.jl)[4] library. A code package for Julia, ACME.jl provides a suite of functions and structures that enable the rapid creation and simulation of state space models of electronic circuits. The user simply provides information about the circuit, i.e. component values, parameters, and the schematic, and ACME.jl generates the state space model automatically using the technique described in [71], which differs slightly from the traditional NDK method. This package proved to be invaluable to the success of this work, as it alleviated much of the software development burden. However, identical results could be achieved using other programming languages, such as Matlab or Python.

The model was simulated for a full second with the aforementioned input signal using Newton's method as the iterative solver. The final two periods of the resultant output are shown alongside the input in figure 3.6. The small signal model assumption appears to have held - for an input signal with a 10mV peak, linear amplification is observed.

[3] `https://julialang.org/`
[4] `https://github.com/HSU-ANT/ACME.jl`

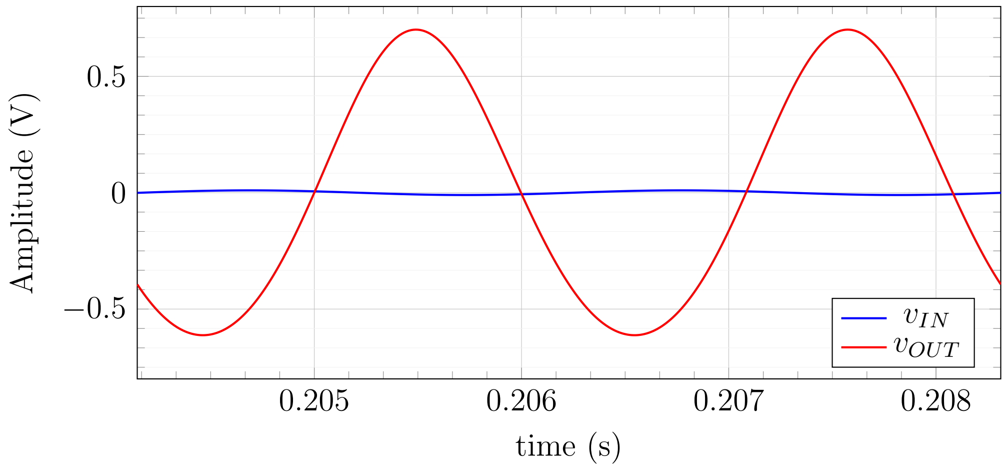


Fig. 3.6 Input and output of the simulated common-emitter amplifier.

To verify the gain factor of the simulation, the small signal model representation of the circuit is re-visited. While the voltage gain of the common-emitter amplifier is defined as R_C/r_e in equation 2.35, some additional considerations must be made here due to the additional components. Namely, the input resistance, R_{IN}, and the load resistor, R_L, must be taken into account. Incorporating these additional components into figure 3.2, the small signal model of the final schematic is shown in figure 3.7. It is assumed that the capacitors are sufficiently large to allow the 480Hz signal to flow through them unimpeded, so they are replaced by short circuits for this analysis.

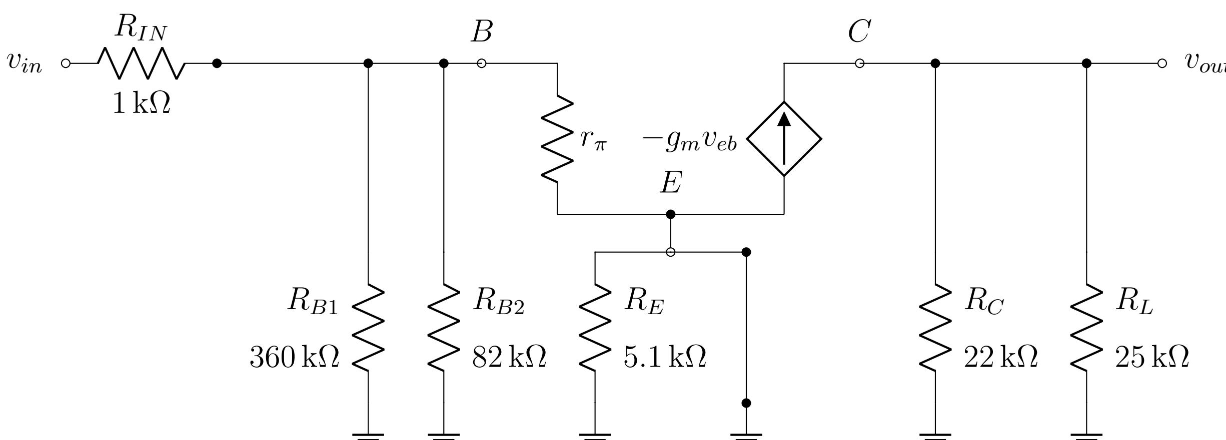


Fig. 3.7 Small signal model of the common-emitter amplifier, with capacitors replaced by short circuits.

From there, the emitter-base signal voltage can be expressed as a function of the input signal voltage by applying the voltage divide rule:

$$\begin{aligned} v_{eb} &= \left(\frac{R_{B1}||R_{B2}||r_\pi}{R_{B1}||R_{B2}||r_\pi + R_{IN}}\right) v_{in} \\ v_{eb} &\approx 0.9121 v_{in} \end{aligned}$$

Then, the output voltage can be expressed as a function of the input voltage:

$$\begin{aligned} v_{out} &= -g_m v_{eb} \left(R_C||R_L\right) \\ v_{out} &= -g_m \left(0.9121 v_{in}\right) \left(R_C||R_L\right) \\ A_v &\equiv \frac{v_{out}}{v_{in}} \approx -86.94 \end{aligned} \tag{3.12}$$

By examining figure 3.6, the maximum voltage of the output is observed as about 0.75 V. The maximum input voltage is 10 mV, so the calculated voltage gain is not observed. It is concluded, then, that the capacitors are not sufficiently large to be considered short circuits at 480 Hz. This is further supported by observing that the input and output are not quite 180° out of phase as expected. This phase difference causes a reduction in the observed gain factor. Noting that $-A_v = A_v \cos(180°)$, the phase difference can be calculated as:

$$\begin{aligned} A_v \cos(180 - \phi) &= \frac{0.75\,\mathrm{V}}{0.01\,\mathrm{V}} = 75 \\ 180 - \phi &= \cos^{-1}\left(\frac{75}{86.94}\right) \\ \phi &= 149.62° \end{aligned} \tag{3.13}$$

For the purposes of this case study, this performance is sufficient. However, if this phase difference was unacceptable, the capacitor values may be increased to compensate.

3.5.1 Summary

In this chapter, we embarked on a case study of the common-emitter amplifier circuit. The circuit was designed for a given specification using standard design practice and the concepts discussed in section 2.2.1. Next, a state space model of the circuit was derived using the NDK method. Finally, the model was simulated, using Newton's method as the iterative solver at each time step, with considerations given to the choice and initialization of the iterative solver. Finally, verification of design assumptions were performed by comparing the calculated voltage gain of the circuit and the observed gain of the model. The observed gain was slightly lower than expected, but the discrepancy was accounted for by analysing the phase difference between the input and output signals.

Chapter 4

State Space Modelling of the Fuzz Face

We now shift our focus to the primary study of this work: creating a state space model of the Fuzz Face guitar pedal. We begin by taking an in-depth look at the Fuzz Face schematic and discussing its defining characteristics. Next, we give an overview of BJT parameter extraction for both the EM and SGP models, including taking measurements from actual GBJTs, directly extracting parameters from the measurements, and parameter optimization. Finally, we compare three state space models of the fuzz face, created using the EM model, a DC SGP model, and an AC SGP model, respectively. The results of processing standard inputs with all three models is compared in both the time and frequency domain, followed by a comparison of their computational cost.

4.1 Introduction and Fuzz Face Overview

4.1.1 Schematic Overview

The schematic of the Fuzz Face is shown in figure 4.1. Elegant in its simplicity, the Fuzz Face consists of two tightly coupled GBJT amplification stages, with a negative feedback network and adjustable gain, or "fuzz" control. The guitar signal is fed into the base of Q_1 through the input capacitor, C_1. R_2 sets the bias current of Q_1, and the collector of Q_1 connects directly to the base of Q_2. R_3, R_4, and the fuzz control, R_f, set the bias current of Q_2, and negative feedback is established from the emitter of Q_2 to the base of

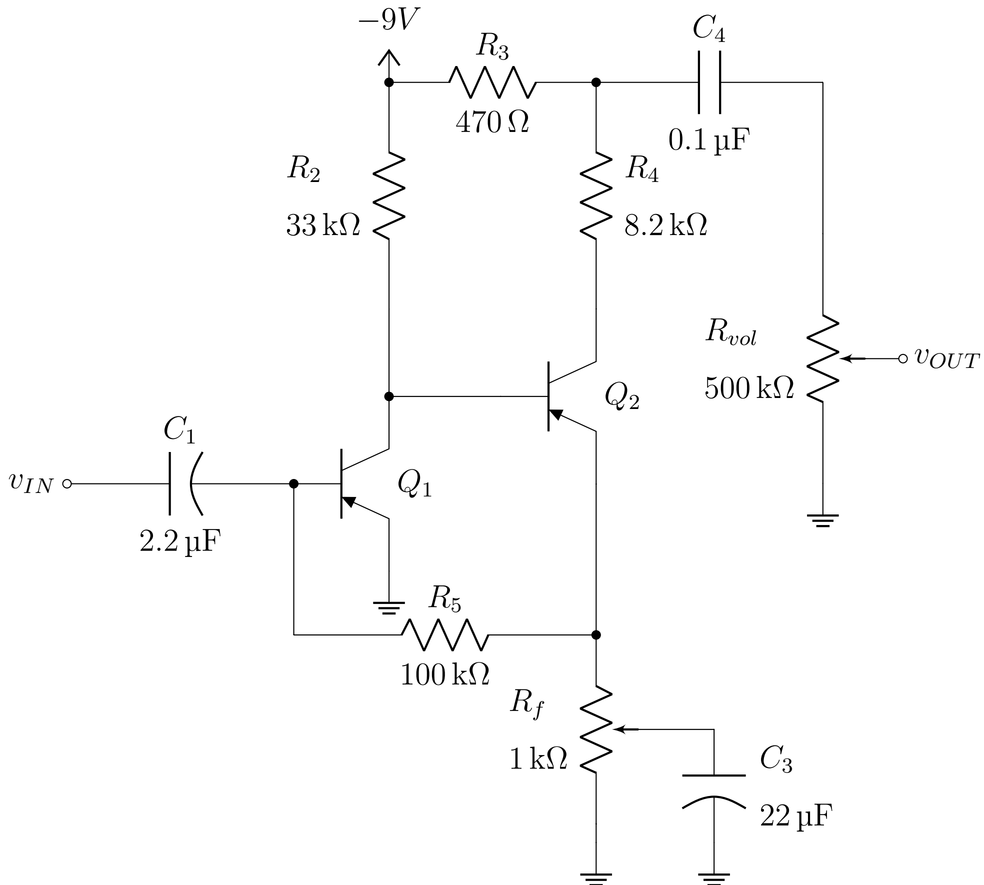


Fig. 4.1 Schematic of the Dallas Arbiter Fuzz Face.

Q_1 through R_5. Turning the fuzz control, R_f, clockwise gives the signal flowing through Q_2 an increasingly more direct path to ground through the bypass capacitor, C_3, which, as shown in section 2.2.3, increases the gain of the circuit. Turning up the fuzz control also has the effect of reducing the amount of negative feedback by providing a shunt path to ground, increasing the non-linearity of the circuit. The schematic shown in figure 4.1 is widely believed to be the "original" Dallas-Arbiter Schematic, though many permutations exist - several are outlined in [154, 155]. The original units used *pnp* GBJTs, and were powered by a 9 V battery with the positive terminal connected to ground.

4.1.2 Input Impedance

One of the more peculiar features of the Fuzz Face is its input impedance and, consequently, how it reacts to various guitars and their onboard controls. Through inspection of figure 4.1, the input impedance can be calculated as the input resistance looking into the base of Q_1 in parallel with R_5 and R_f, where the contribution of R_f is a function of the potentiometer's position, α. Letting $Z_a = R_5 + (1-\alpha)R_f$ allows the input impedance of the Fuzz Face to be expressed as:

$$\begin{aligned} Z_{in} &= r_\pi || Z_a \\ &= \frac{\beta}{g_m} || Z_a \end{aligned} \tag{4.1}$$

If we assume for a moment that Q_1 has $\beta = 70$, g_m can be estimated as:

$$g_m = \frac{I_C}{V_t} = \frac{\frac{(V_{CC} - V_{C_{Q_1}})}{R_2}}{V_t} \approx \frac{0.22\,\text{mA}}{25\,\text{mV}} = 0.0088 \tag{4.2}$$

the input impedance with the fuzz control set to maximum (i.e. $\alpha = 1$) follows as:

$$Z_{in} = \frac{70}{0.0088} || 100\,\text{k}\Omega \approx 7.37\,\text{k}\Omega \tag{4.3}$$

As mentioned in discussions of the emitter-follower circuit in section 2.2.3, it is generally recommended that the input impedance of a guitar pedal be $\geq 1\,\text{M}\Omega$ to prevent source loading between serially-connected devices, and to minimize transmission line losses in the instrument cables. The input impedance of the Fuzz Face, however, is several orders of magnitude lower than that. As such, the Fuzz Face presents a non-insignificant load to the guitar's pickups - which typically have a DC resistance of $6 - 15\,\text{k}\Omega$. This creates a voltage divider from source to the Fuzz Face's input which decreases signal amplitude, and induces a noticeable low-pass filter effect in the instrument cable, causing some high-end harmonics in the guitar's signal to be filtered out.

This non-ideal interaction, however, has become one of the defining characteristics of the Fuzz Face. It makes the circuit far more sensitive to the guitar's volume control than circuits with a "proper" input impedance, which allows players to use the onboard volume control of their guitar as a pseudo "distortion" control for the circuit. Rolling off the volume causes a decrease in distortion, allowing the player to fine-tune the amount of fuzz, and conversely, how clean the output will be. This gives the player access to nearly infinite shades of harmonic distortion, from clean through to full-on fuzz tones, simply by adjusting their volume.

4.1.3 Traditional Wisdom and the Fuzz Face

Like many artifacts and historical figures in the lineage of music, the Fuzz Face (and those who build them) is surrounded by a veil of folklore, mythology, and idiosyncrasies. One such phenomena is the idea of "matched sets" of GBJTs as they relate to the sound quality and "feel" of a particular Fuzz Face unit.

GBJTs, and consequently the Fuzz Face, were known to be inconsistently manufactured, with each unit sounding slightly different than the next. In the DIY pedal-building community, there is a consensus that the "best-sounding" Fuzz Faces contain a matched set of GBJTs, with Q_1 having a gain of $70 - 85$, and Q_2 having a gain of $110 - 130$. While this phenomena is treated as fact in the literature [154] and in several online articles [155–157], it is difficult to conclude whether or not Fuzz Faces with matched sets truly sound "better". However, given the widespread consensus, it was deemed necessary to incorporate this "traditional wisdom" into this work.

4.1.4 Summary

It is clear, then, that the Fuzz Face is a highly non-linear circuit whose behaviour is largely dictated by the GBJT pair of Q_1 and Q_2. It has very high signal gain, and produces rich, harmonic distortion - turning a sinusoidal input signal into a near square wave output. Furthermore, the low input impedance of the Fuzz Face allows it to interplay dynamically with the guitar's volume control, allowing the player to fine-tune the amount of distortion in real time. While the distortion characteristics can be influenced by changing the value of the three capacitors, the overall tonal characteristics and behaviour of the pedal are largely dependent on the two GBJTs. Modelling these GBJTs accurately is therefore paramount in creating an accurate model of the Fuzz Face.

4.2 Parameter Extraction

To create an accurate GBJT model, we begin by extracting the DC parameters of the EM and SGP models. Several sets of measurements were taken from actual GBJTs under various operating conditions, giving a concrete view of how they functioned under specific operating conditions. From those measurements, certain parameters of the models are extracted directly and used as a starting point for a non-linear parameter optimization procedure. A multi-stage approach is taken to optimizing the parameters, allowing the model's behaviour to be closely matched to that of the measured data.

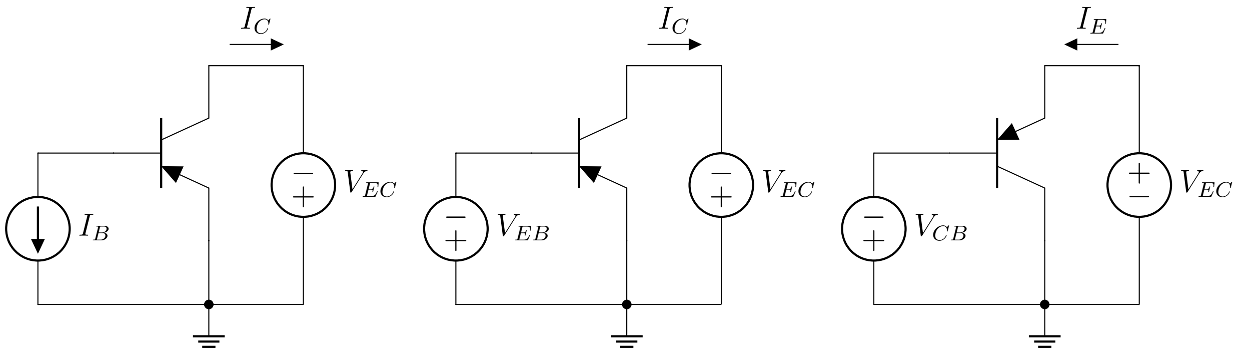
4.2.1 GBJT selection

The original Dallas Arbiter Fuzz Faces used several different GBJTs, likely due to availability and cost of components at the time. The two most-coveted GBJTs used in the Fuzz Face, though, are a pair of AC128 or NKT275 GBJTs. Obtaining these components has naturally become increasingly difficult and expensive over time. As such, a pair of vintage Mullard/Phillips AC125 GBJTs were measured instead as a comparable substitute. These GBJTs were procured as a "matched set", with Q_1 having $\beta \approx 70$, and Q_2 having $\beta \approx 125$ when measured with a component tester.

All measurements, parameter extractions, and optimization stages were therefore performed twice: once for each GBJT. This allowed two parameter sets to be derived, providing unique parameter sets for Q_1 and Q_2. Thus, the idea of the "matched set" was incorporated into this work.

4.2.2 Measurement Strategy

The measurement strategy used in this work is based on existing strategies, outlined in [23, 158, 159]. Three sets of measurements were captured for each GBJT, including the common-emitter output characteristics, and the so-called "gummel plots" in both the forward and reverse direction. Each measurement exposes specific behaviour of the device and allows the direct extraction of certain parameters. The high-level circuit used to record each measurement is shown in figure 4.2. The input current/voltage range(s) are listed in table 4.1.



(a) Common-emitter. (b) Forward gummel. (c) Reverse gummel.

Fig. 4.2 High-level circuits for GBJT measurement and parameter extraction.

The common-emitter characteristics are measured by fixing the base current, I_B at a constant current, sweeping V_{EC}, and measuring I_C. This is repeated for several values of I_B, giving multiple snapshots of the relationship between I_B, I_C, and V_{EC} in the Device Under Test (DUT). The resultant measurements are most often displayed as a family of I_C vs. V_{EC} plots, where each curve represents a different value of I_B.

The forward gummel plot is obtained by fixing V_{EC} to a positive bias, sweeping V_{EB}, and measuring both I_B and I_C. Similarly, the reverse gummel plot is obtained by fixing V_{EC} at a *negative* value while V_{CB} is swept and I_B and I_E are measured. This methodology is described in [158], where it is recommended that V_{EC} be biased between 2 V and half of the maximum value used for the common-emitter measurements. This creates a direct relationship between the common-emitter characteristics and the forward gummel plots for the same value of V_{EC}, such that the voltages/currents measured in both cases should be equal. This approach also biases the GBJT in the active region, providing confidence that the model will fit to all of the measurements. The gummel plots are best visualized by plotting both $log(I_B)$ and $log(I_C)$ (or $log(I_E)$ for the reverse case) against V_{EB} (or V_{CB})). Further, the DUT's current gain plot may also be visualized by plotting I_C/I_B (or I_E/I_B for the reverse case) against V_{EB} (or V_{CB})). Examples of the common-emitter and gummel plots can be found in figures 4.9 and 4.10 in section 4.4.2.

Measurement	Input	Range
Common Emitter	I_B	3 - 50µA
	V_{EC}	-5 - 5V
Forward gummel	V_{EB}	0 - 0.7V
	V_{EC}	2V
Reverse gummel	V_{CB}	0 - 0.7V
	V_{EC}	-2V

Table 4.1 Input ranges for each of the three measurement circuits.

4.3 Designing GBJT Measurement Circuitry

4.3.1 Introduction

The ultimate goal of this work was to re-implement the research presented in [23]. While the measurement strategy utilized by Holmes et al. is well-defined in [23] and elaborated further in their PhD thesis [160], their measurement strategy used a Keithley 2602B Source Measure Unit[1]. This unit provides an impressive amount of functionality. It can act as a constant voltage power supply from 100mV to 40V, a precision current source from 100nA to 10A, a Digital Multi-Meter (DMM), arbitrary waveform/pulse generator, and even an electronic load. It isn't surprising, then, that this piece of equipment makes short work of all the measurements required to extract all the BJT model parameters. All of this functionality comes with a hefty price tag, however - over sixteen thousand Canadian dollars (approx. $12,825 USD) at the time of this publication.

Under normal circumstances, it may have been possible to gain access to such a piece of equipment through the various support channels offered to students of McGill University. But, because of the COVID-19 pandemic that began in early 2020, many students were displaced from the university, had to move home to other parts of the world, and were forced to carry out their research remotely. This necessitated the development of another approach to complete the required measurements, as access to this piece of equipment would not be possible under the given circumstances. On the surface, this may not seem like a difficult task, but, it proved to be a significant challenge and quickly became one

[1] Keithley 2600B Series website

of the primary contributions of this work. After much experimentation and research, a minimum-cost solution for capturing the required measurements - consisting of only basic lab equipment and readily-available, inexpensive, analog electronics, was developed.

In this chapter, we will discuss the design of circuitry that, in conjunction with basic lab equipment, provides the functionality required to capture the aforementioned measurements. Namely, the design of a precision current source, a pulsed-DC voltage source, and instrumentation amplifiers as required, will be discussed. For further discussions on design choices made, including component choices and an in-depth analysis of the circuitry, see appendix C.

Self-Heating Considerations

When a BJT has a sufficiently high DC current flowing through it, its substrate begins to heat up slightly. This, in turn, increases the internal temperature of the device, lowering its internal resistance, and increasing the current draw of the BJT. This phenomena is aptly named BJT self-heating, and it becomes a significant factor in the device's operation when experiencing relatively high DC currents (10 - 50 mA or more). Self-heating has the propensity to obscure the accuracy of DC measurements of a BJT and, as mentioned in [158], can prevent the accurate extraction of macro-model parameters. It is therefore necessary to take these effects into account and mitigate them effectively during measurements. Self-heating mitigation strategies were implemented for each of the measurement schemes, and will be outlined in the sections to follow.

4.3.2 Designing a Precision Constant Current Source (Common-Emitter Measurements)

The first issue that one will likely encounter when attempting these measurements is the requirement of a Constant Current Source (CCS) to measure the common-emitter output of the BJT. Most run-of-the-mill bench-top power supplies are constant *voltage* sources - they maintain a constant voltage, and deliver as much current as needed (within reason) to the load. This stands in opposition to a CCS, which maintains a constant *current*, while allowing the voltage across it to vary per the load. Furthermore, a *variable* current source is required in this case, adding another layer of complexity to the problem.

What we desire, then, is to create a variable CCS powered by a voltage source, i.e., a VCCS. To do so, we will supplement the bench-top supply with some basic analog electronics. It is noted that there are *many* different ways to create a VCCS, and the solution presented here is just one such example.

Ideally, the voltage across a current source may vary infinitely in order to maintain the desired current output with changes in load. This implies that the ideal current source has an infinite output impedance. Any practical current source, however, will have some non-infinite output impedance, and a limit on how much the voltage across it is able to swing. In practice, this voltage swing is constrained by the DC supply used to power the circuitry[2]. To create a VCCS with a very high output impedance, two building-block circuit elements were used: an op amp-BJT current source and a cascode current mirror. The measurement setup is shown in figure 4.3, including the complete current source circuit, instrumentation, and the DUT.

The operation of the circuit is relatively straight forward. A constant reference voltage, V_{ref} is established by the resistor voltage divider of R_1 and R_2, which then connects to a unity-gain op amp buffer. The reference voltage is simply defined by the voltage divider rule, i.e.:

$$V_{ref} = -\left(\frac{R_2}{R_1 + R_2}\right) V_{CC} \tag{4.4}$$

The output of the op amp buffer connects to a potentiometer, R_3, whose wiper connects to the input of the op amp-BJT current source. This allows the input of the current source to be swept from 0V $\rightarrow V_{ref}$. Subsequently, this allows the output of the current source, I_{ref}, to be swept over the desired range. The output current as a function of the input voltage is simply:

$$I_{ref} = \frac{\alpha V_{ref}}{R_{sense}} \tag{4.5}$$

where αV_{ref} is the voltage at the wiper of R_3. The mapping from input voltage to output current can therefore be configured by setting R_{sense} to an appropriate value. Finally, the op amp-BJT current source is augmented by a cascode current mirror. This circuit functions similarly to a buffer, though it maintains the input *current* at its output, not voltage,

[2]Ideal and practical DC sources are discussed in appendix B.

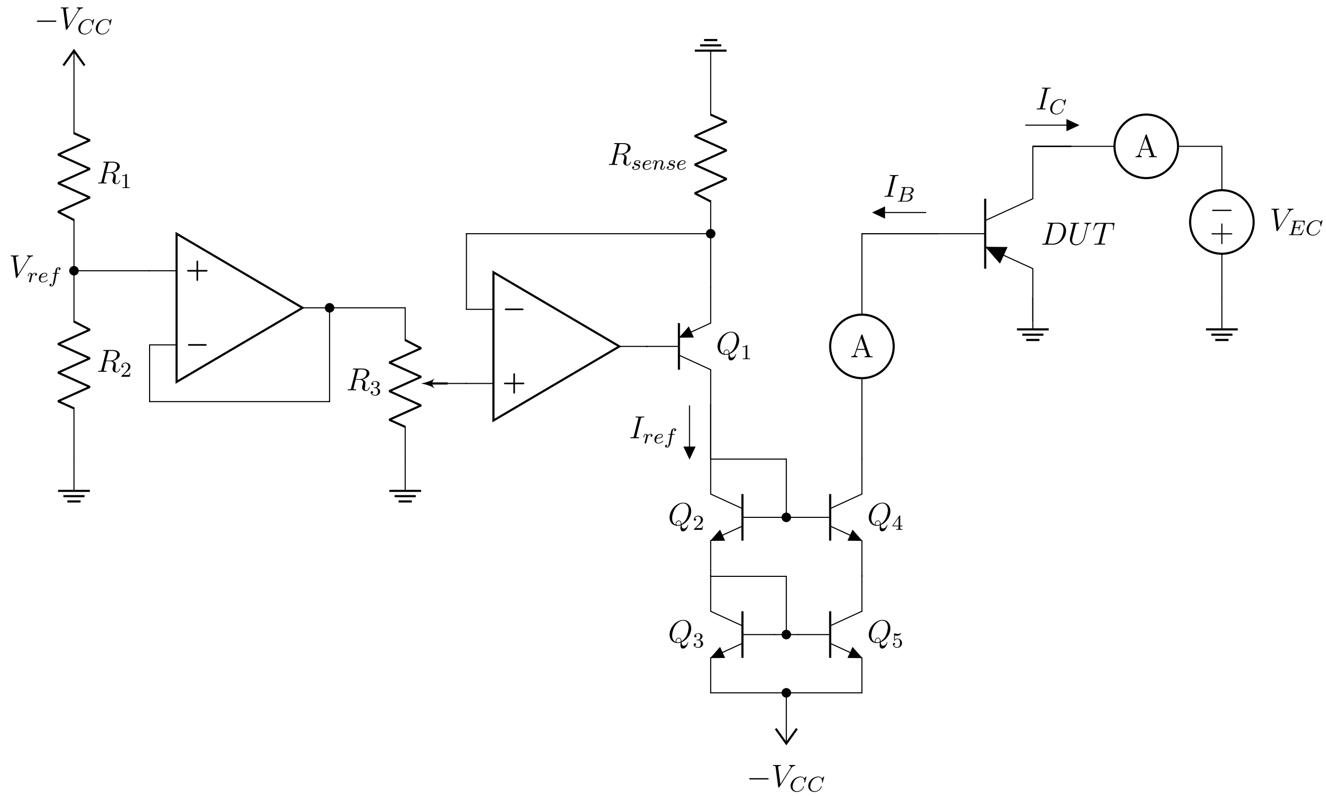


Fig. 4.3 Complete schematic of GBJT common-emitter measurement circuit. Ammeters connected to the base and collector of the DUT measure the base and collector current, respectively, while the voltage source V_{EC} is provided by a bench-top power supply.

and presents its load with a very high output impedance. The output of the cascode current mirror connects to the base of the DUT through a standard ammeter, allowing the input current to be measured and adjusted. For a more detailed explanation of the design and component choices made to create this circuit, see appendix C.

To mitigate the effects of self-heating during the collection of common-emitter measurements, the DUT was thermally coupled to a large heat sink with thermal paste, while two small computer fans circulated air across the device and the heat sink. This provided sufficient cooling to the device as to not obscure the measurements. The symptoms of self-heating in the common emitter measurements are identified in [158].

4.3.3 Designing a Pulsed-DC Voltage Source (Forward and Reverse Gummel Measurements)

While the combination of a heat sink and fans provided sufficient cooling in the common-emitter case, the same approach did not suffice for the gummel plots as the current draw was much higher - exceeding 1A at the high end of measurements. As such, a new approach was required, which motivated the development of a *pulsed-DC* voltage source. A pulsed-DC voltage source avoids self-heating by only applying voltage to the device in short intervals, alternated with periods of 0 V. This gives the device time to cool down between periods of applied voltage. Considering the time interval during which voltage is applied as "On", and the time interval where the voltage is 0 as "Off", the *duty cycle* may be defined as the percentage of the total time where the device is *on*, i.e.:

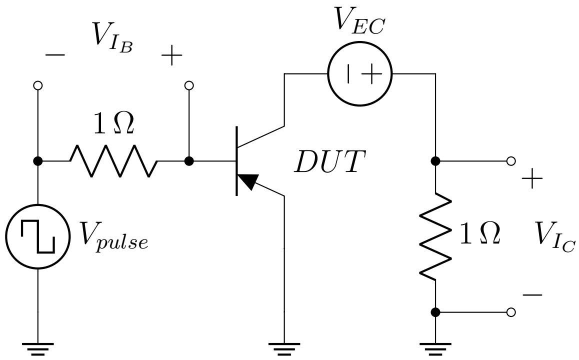
$$Duty\ Cycle(\%) = 100\% \times \frac{T_{ON}}{T_{ON} + T_{OFF}} = 100\% \times \frac{T_{ON}}{T} \tag{4.6}$$

where T is the period of the pulse. Note that true DC occurs when the duty cycle is 100%. Note also that a pulsed-DC signal is *periodic*, unlike a true DC signal, and the period can be observed as:

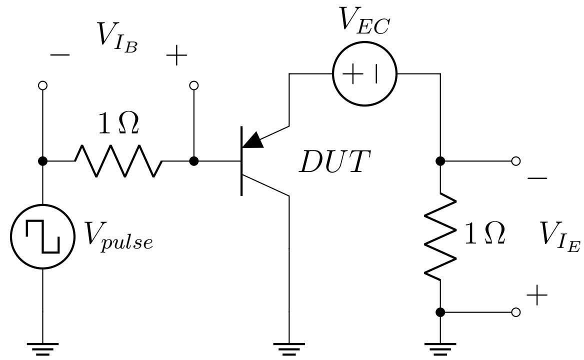
$$T = T_{ON} + T_{OFF} \tag{4.7}$$

Because a pulsed-DC voltage source produces a periodic signal, the base and collector (or emitter) currents can no longer be measured using the ammeter in a standard bench-top DMM. Instead, an oscilloscope and some 1Ω power resistors in series with the base and collector (or emitter) were used. The oscilloscope's probes were then connected across the two series resistors to observe their voltage waveform. Those readings are then converted to a current measurement using Ohm's Law. Because these voltages were so small for low currents, instrumentation amplifiers we used to amplify the waveforms before observing them on the oscilloscope.

Updated versions of figures 4.2b and 4.2c, reflecting the true measurement circuits, are shown in figure 4.4. V_{pulse} represents the pulsed-DC voltage source, while V_{EC} remains a standard DC voltage source - pulsing only the base is sufficient to turn the device on and off. The voltages V_{I_B}, V_{I_C} and V_{I_E} are connected to instrumentation amplifiers, whose output connects to an oscilloscope probe. Since the series resistors only have 1Ω of resistance, the current through the resistor simply equals its voltage drop, i.e. $I_B = V_{I_B}$. Note also that



(a) Forward gummel.



(b) Reverse gummel.

Fig. 4.4 Updated measurement circuits for the forward gummel (a) and reverse gummel (b) configurations.

the resistor used to measure the collector (or emitter) current is connected to the *low-side* of V_{CC}. This enables a single-ended instrumentation amplifier to be used, whereas the base current resistor requires a differential instrumentation amplifier. For more information on the instrumentation amplifiers used in this work, see appendix C.

The schematic of the pulsed-DC voltage source is shown in figure 4.5. The pulses are generated using a 555 timer configured as an astable multi vibrator[3]. R_2 is a variable resistor whose maximum value is equal to R_1. This allows the duty cycle to be varied from 0% to 50%. The output of the multi vibrator is connected to the resistor divider formed by R_3 and R_4, where R_4 is a potentiometer, which lowers the output voltage to the desired range as called for by the measurements. The wiper of the potentiometer connects to the non-inverting input of an op amp-BJT voltage source. This enables the circuit to maintain its output voltage level, even when the load draws a high current.

This simple, inexpensive voltage source enabled the measurement of GBJT behaviour at relatively high currents without the risk of overheating and damaging the device. As long as the duty cycle of V_{pulse} was kept sufficiently low, the self-heating effects were not observed. Experimentally, a duty cycle of 10% or less was found to be sufficient in avoiding self-heating.

[3] An introduction to the 555 timer can be found here

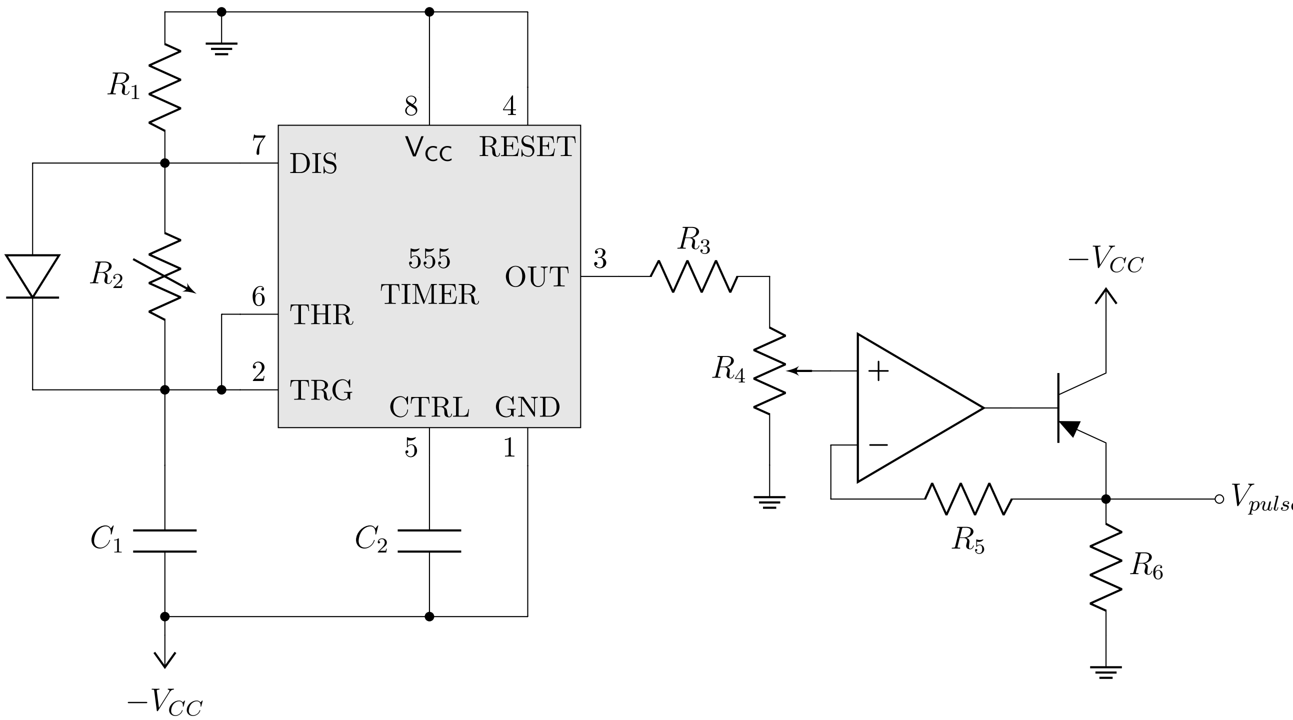


Fig. 4.5 A high-current, variable duty-cycle DC pulse generator using a 555 astable multi vibrator and an op amp-BJT voltage source.

It is of note that similar (if not more accurate) functionality can be achieved by feeding the op amp-BJT voltage source with the Pulse-Width Modulation (PWM) output of a micro-controller. However, the "all-analog" approach taken here seemed more fitting given the nature of this work. Furthermore, should more rigorous self-heating mitigation be required when measuring the common-emitter characteristics (as would be the case for higher base currents), this pulsed-DC voltage source may be modified to function as a pulsed-DC current source by replacing the op amp-BJT voltage source with a VCCS.

4.4 Macro-model Parameter Extraction

Having measurements from actual GBJTs, we will now extract the macro-model parameters that provide best fit to the measured data. To do so, we begin by extracting/estimating an initial parameter set directly from the measured data before processing the data with several stages of non-linear parameter optimization.

4.4.1 Direct Extraction

To provide good initial estimates for the optimization stages, several macro-model parameters may be extracted directly from the measured data. Some model simplifications are made to aid in the extraction, though this will not affect the accuracy of the final models - the majority of the extraction occurs during the optimization. It is paramount, however, that the optimization process be initialized closely to the final parameter space. This helps to avoid local minima, which may halt the optimization without providing best fit to the measured data.

Ebers-Moll Parameters

The EM parameters are extracted from the measured gummel plots. An exemplary forward gummel plot for the EM model is shown in figure 4.6, which illustrates the effects of the forward parameters, and the saturation current I_S.

The forward parameters were extracted first. To simplify this procedure, the opposing current term from equation 2.37, in this case i_r, is neglected. Since this assumption is only valid for $V_{CB} = 0$, as opposed to $V_{CB} < 0$, some error is introduced. This error is small, though, as $i_r \leq I_S$ when the CBJ is reverse-biased. Further, this error is later removed in the optimization process where no simplifications are made.

First, the thermal voltage is calculated by measuring the ambient temperature of the room in which measurements were taken. This, of course, assumes that appropriate self-heating mitigations are in place and the BJT remains at a constant temperature during measurements. Using the measured temperature in Kelvin, the thermal voltage is calculated using equation 2.2. At room temperature, $V_t \approx 25$mV. Next, the non-ideality factor, N_f, can be found by considering the gradient of the $log\,(I_C)$, as defined in equation 2.40. Neglecting the constant term from i_f, this can be expressed as:

$$\frac{\mathrm{d}log(I_C)}{\mathrm{d}V_{EB}} = \frac{1}{N_f V_t} \tag{4.8}$$

Rearranging this equation yields a value of N_f for a given value of V_{EB}. It is of note that the behaviour shown in figure 4.6 is linearized, and is not indicative of how measured data will appear. It is therefore important to choose a suitable extraction point. In [23], they

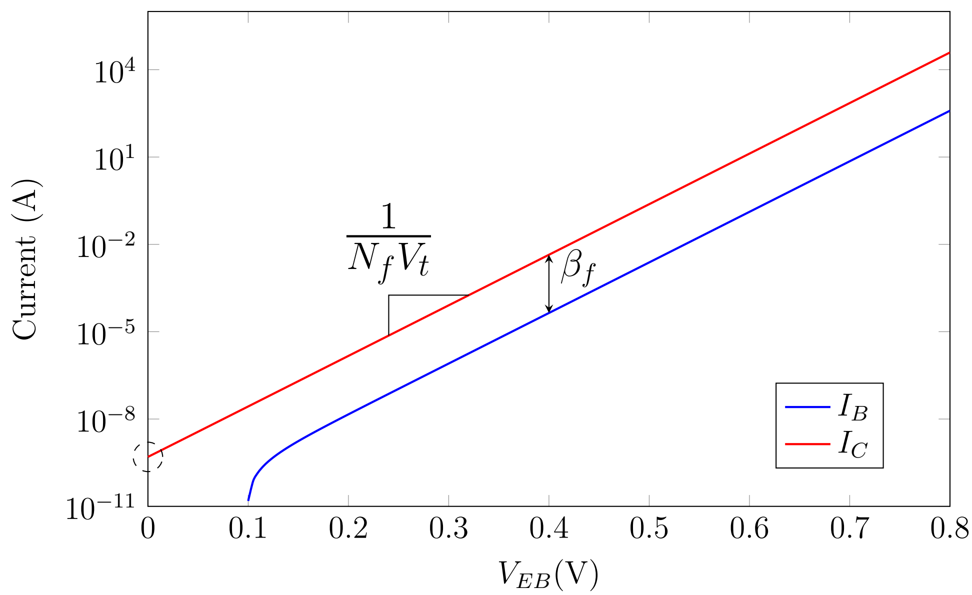


Fig. 4.6 Example forward gummel plot for the Ebers-Moll model, illustrating the relationships of the forward parameters. The currents are plotted logarithmically against linear voltage.

propose the first minimum of the absolute value of the second derivative of I_C as a suitable extraction point. A value for I_S can then be found by solving the simplified expression of I_C with constant term neglected, i.e.:

$$I_C = I_S \exp\left(\frac{V_{EB}}{N_f V_t}\right), \quad I_S = \exp\left(log(I_C) - \frac{V_{EB}}{N_f V_t}\right) \tag{4.9}$$

From this equation, it can be deduced that I_S is simply the y-intercept of the gummel plot, which is illustrated in figure 4.6.

Finally, the forward gain factor, β_f can be extracted by examining the relationship of I_C and I_B, i.e. the current gain. Equation 2.3 shows that $I_C = \beta_f I_B$ when the BJT is biased in the active region, as illustrated in figure 4.7. This relationship contradicts the linearized plot shown in figure 4.6, where β_f remains constant for all values of V_{EB}. As V_{EB} approaches zero, I_B decreases such that β_f increases rapidly. This region of the plot does not yield an accurate value of β_f, so values of β_f below the first local minima can be excluded [23]. The maximum of β_f beyond the local minima is then extracted as the initial parameter value, as shown in figure 4.7.

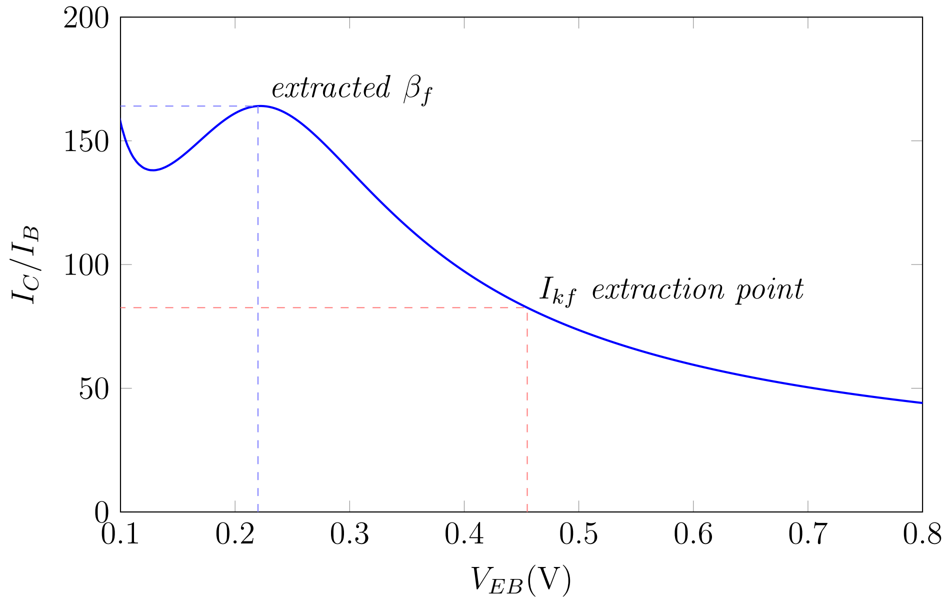


Fig. 4.7 Example plot showing a typical current gain gummel plot in the forward direction. A nominal value of the current gain is extracted from the maximum value. The knee current is extracted as the value of I_C where β_f falls to half of the maximum value.

The reverse parameters can be extracted for the reverse gummel plot following the same procedure as outlined above. Further, an initial estimate for I_S may be extracted from either plot. The extracted values of I_S should agree between the two plots, and so the value chosen is therefore arbitrary.

SPICE Gummel-Poon Parameters

To initialize the SGP model, the previously extracted values for e.g. I_S, β_f , and N_f are used, along with directly extracted estimates for the forward and reverse knee current and early voltage.

The knee currents are extracted from the current gain plots, shown in the forward direction in figure 4.7. The extracted values for I_{kf} and I_{kr} are taken as the value of I_C and I_E at which the current gain falls to half of its maximum value, respectively. If the current gain does not fall below half of its maximum value, the curve may be extrapolated.

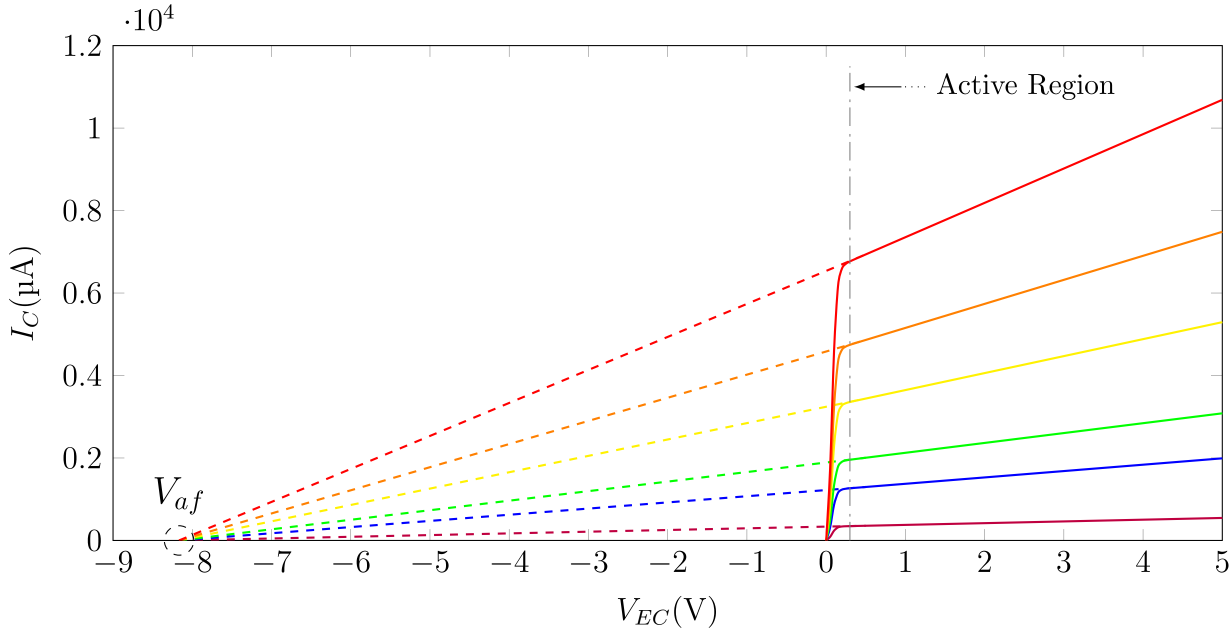


Fig. 4.8 Example of common-emitter plot, shown with lines tangent to the active regions of the plots. The x-intercept of these tangents is used to extract V_{af}.

Finally, initial values for the early voltages, V_{af} and V_{ar}, are extracted from the common-emitter plots. The early voltage is the x-intercept of the curves' tangents in the active region [75], as shown in figure 4.8. The extracted value will be negative in the forward direction, so V_{af} is taken as its magnitude. The procedure is then repeated for the reverse direction.

An extraction strategy was not implemented for the remaining parameters, i.e. the leakage currents and terminal resistances, as they can easily be initialized by manual tuning. The model data from similar works found in the literature, e.g. [23, 160], also served as starting points for the optimization, due to the similarity of the GBJTs in each work. Furthermore, the SGP model was simplified from the complete SGP model described in section 2.2.4 to aid with model implementation. The variable base resistor, r_B, and the non-linear capacitances, C_{jC} and C_{jE}, were replaced by fixed components, as modelling these components using current VA frameworks is non-trivial. The DC SGP model then consists of the simplified model with the capacitors omitted, while the AC SGP model includes the capacitances. Since fixed components were used, the capacitances were simply taken from the data sheet of a similar GBJTs, as the data sheet of the AC125 was unavailable.

4.4.2 Parameter Optimization

Having extracted and estimated an initial parameter set, non-linear optimization was then performed to closely match the model's behaviour to the measured data. To optimize the parameters of the EM model, a single optimization stage was used on a constrained range of the gummel plots. For the SGP model, a three-stage optimization strategy was used. The two intermediate optimization stages were performed on specific data sets, allowing smaller subsets of parameters to be optimized before the final, global optimization stage. This insured that the global optimization stage was well-initialized.

Parameter optimization is typically accomplished by applying a minimization algorithm to a so-called "objective function". An objective function compares measured data to a model with a parameter set, θ, such that the model's behaviour exactly matches the measured data when the objective function equals 0. The goal, then, is to find the parameter set, θ_{min}, that *minimizes* the objective function. For this work, an objective function was defined for each data set. They all conformed to the same basic structure, where the value is normalized with respect to the number of data points, and the value of each data point. The generalized objective function for a data set, D (i.e. forward gummel, reverse gummel, or common-emitter), was defined as:

$$R_D(\theta) = \frac{1}{N} \sum_{n=1}^{N} \left(\frac{y[n] - \hat{y}(\theta)[n])}{y[n]} \right)^2 \tag{4.10}$$

where N is the number of measured data points, $y[n]$ is the measured output for the input at point n, and $\hat{y}(\theta)[n]$ is the model output at point n, simulated with the parameter set, θ.

An optimization algorithm typically requires the user to provide either an *initial guess*, or *bounds* for each parameter, within which θ_{min} is expected to be found. Many optimization algorithms utilize the gradient and/or the hessian of the objective function and as such, they require the objective function be differentiable. One of the most important measures of an optimization algorithm is its ability to ignore the local minima of the objective function, finding instead the true, *global* minimum. Different algorithms handle local minima and discontinuous surfaces in a different manor, and many are described in the literature, e.g. [161–165].

Programs to perform parameter optimization were developed in Julia, where ACME.jl was used to construct models of each measurement scenario. One limitation of working with ACME.jl, though, is that its models and functions are written in such a way that their gradient cannot be calculated using the available methods in Julia. As such, gradient-free optimization algorithms were used.

Two optimization algorithms were chosen: Differential Evolution (DE) [166] from the BlackBoxOptim.jl package, and the Nelder-Mead Simplex method [162, 163] from the Optim.jl package. DE was chosen for the intermediate stages as it provides robust, gradient-free, bounded optimization. This ensured that the parameter sets it returned would serve as a suitable starting point for the next stage. Implementations of DE provided by BlackBoxOptim.jl include the classic DE algorithms as described in e.g. [161, 166], as well as radius-limited and adaptive-parameter versions. In general, the classic algorithms were favoured, but adaptive and/or radius-limited algorithms were used in instances where the classic algorithms did not reliably converge.

The Nelder-Mead simplex was used during the final optimization stage. Its ability to handle discontinuous surfaces enabled the use of an objective function that would return an infinite value if any of the supplied parameters were negative, preventing non-physical parameter sets. Extending equation 4.10, the objective function used with the Nelder-Mead Algorithm was:

$$R_D(\theta) = \begin{cases} \dfrac{1}{N}\displaystyle\sum_{n=1}^{N}\left(\dfrac{y[n]-\hat{y}(\theta)[n])}{y[n]}\right)^2 & \theta_p > 0 \ \forall \ p \in 1,2,\ldots,P \\ \infty & \theta_p \leq 0 \ any \ p \in 1,2,\ldots,P \end{cases} \tag{4.11}$$

Further, each optimization procedure was repeated twice - once for each GBJT in the matched set, producing two sets of parameters for both the EM and SGP model. The final parameter sets are summarized in table 4.4.

Model	Measurement	Input	Range
Ebers-Moll	Gummel plots	V_{EB}, V_{CB}	100mV - 200mV
Gummel-Poon	Current gain gummel plots	V_{EB}, V_{CB}	100mV - 600mV
	Gummel plots	V_{EB}, V_{CB}	100mV - 600mV
	Common-emitter	V_{EC}	-5V - 5V

Table 4.2 Optimization Ranges for each model and set of measurements. The current gain plots and gummel plots are both used in various optimization stages, so they are listed separately.

Ebers-Moll Parameter Optimization

For the EM model, a single optimization stage was performed against the gummel plots using a DE algorithm. As the EM model has a constant β, the input data needed to be limited to the low-current range of the gummel plots where the gradient of the collector (and emitter) current is constant. This reduced voltage range is shown in table 4.2.

SPICE Gummel-Poon Parameter Optimization

The optimization procedure for the SGP model compromised of three stages. After direct extraction, two bounded optimization stages were performed using DE, followed by a third, global optimization stage using the Nelder-Mead simplex.

No optimization	Measurements	Parameters
0. Direct Extraction	Forward and reverse gummel, common-emitter characteristics	I_S, β_f, β_r, N_f, N_r, I_{kf}, I_{kr}, V_{ar}, V_{ar}
Differential Evolution		
1. Optimize on Gain	Forward and reverse current-gain gummel plots	β_f β_r, I_{kf}, I_{kr}, I_{SE}, I_{SC}, N_E, N_C, r_B, r_E
2. Optimize on gummel	Forward and reverse gummel plots	I_{kf}, I_{kr}, r_B, r_E
Nelder-Mead Simplex		
3. Optimize on gummel and common-emitter characteristic	Forward and reverse gummel, common-emitter characteristics	*All parameters*

Table 4.3 Optimization strategy used to extract the DC parameters of the SGP model. The resultant parameters of each stage are used to initialize the following stage.

The first optimization stage was performed on the current gain gummel plots, i.e. I_C/I_B and I_E/I_B. The current gain plots have significantly reduced influence from I_S, V_{af}, V_{ar}, r_C, N_f and N_r, allowing them to be set as constant which reduced the number of dimensions of the optimization. The second stage, was performed on a subset of parameters from the first stage: I_{kf}, I_{kr}, r_B and r_E, against the gummel plots to further fine-tune their values. The final stage was initialized using the results from previous stages, and considered all parameters and all plots. A weighting was applied to the objective functions, making the objective value of the common-emitter characteristic $10\times$ higher than the gummel plots, i.e.:

$$R(\theta) = R_{FG}(\theta) + R_{RG}(\theta) + 10 \times R_{CE}(\theta) \tag{4.12}$$

The full extraction and optimization procedure is summarized in table 4.3, outlining the parameters included in each optimization stage - Parameters not shown were set as constant from the previous stage. The full list of extracted parameter values and optimization bounds is summarized in table 4.4. Further, simulated data using the extracted parameters is shown alongside the measured data for both Q_1 and Q_2 in figures 4.9 and 4.10, respectively.

Parameter		Extracted Values Q_1 EM	Q_1 GP	Q_2 EM	Q_2 GP	Optim. Bounds Lower	Upper	Initial Value
V_t	Thermal voltage	25 mV	25 mV	25 mV	25 mV	-	-	-
I_S	Saturation current	25.10 µA	10.33 µA	16.86 µA	15.84 µA	-	-	-
β_f	Forward current gain	69.59	130.76	99.21	180.34	40	300	-
β_r	Reverse current gain	16.14	16.13	14.03	13.95	3	20	-
N_f	Forward non-ideality factor	1.241	1.067	1.195	1.188	-	-	-
N_r	Reverse non-ideality factor	1.250	1.070	1.168	1.193	-	-	-
I_{kf}	Forward knee current	-	1.006A	-	1.62A	1µA	2A	-
I_{kr}	Reverse knee current	-	0.536A	-	0.289A	1µA	2A	-
V_{af}	Forward early voltage	-	30.22V	-	14.74V	-	-	-
V_{ar}	Reverse early voltage	-	42.07V	-	107.75V	-	-	-
I_{SE}	Emitter leakage current	-	0.324µA	-	0.503µA	100pA	1mA	$I_S/2$
I_{SC}	Collector leakage current	-	0.288µA	-	0.608µA	100pA	1mA	$I_S/2$
N_E	Emitter leakage coefficient	-	1.491	-	2.133	0.9	4	1
N_C	Collector leakage coefficient	-	2.118	-	2.059	0.9	4	1
r_B	Base resistance	-	3.775	-	1.917	1mΩ	250Ω	1 Ω
r_E	Emitter resistance	-	165.4mΩ	-	146.7mΩ	0.1nΩ	2Ω	10mΩ
r_C	Collector resistance	-	9.411mΩ	-	18.07mΩ	-	-	10mΩ
C_{jE}	Emitter-base capacitance	-	100pF	-	100pF	-	-	-
C_{jC}	Collector-base capacitance	-	100pF	-	100pF	-	-	-

Table 4.4 Summary of the extracted parameters for both models and both GBJTs. The optimization bounds and initial values are also shown.

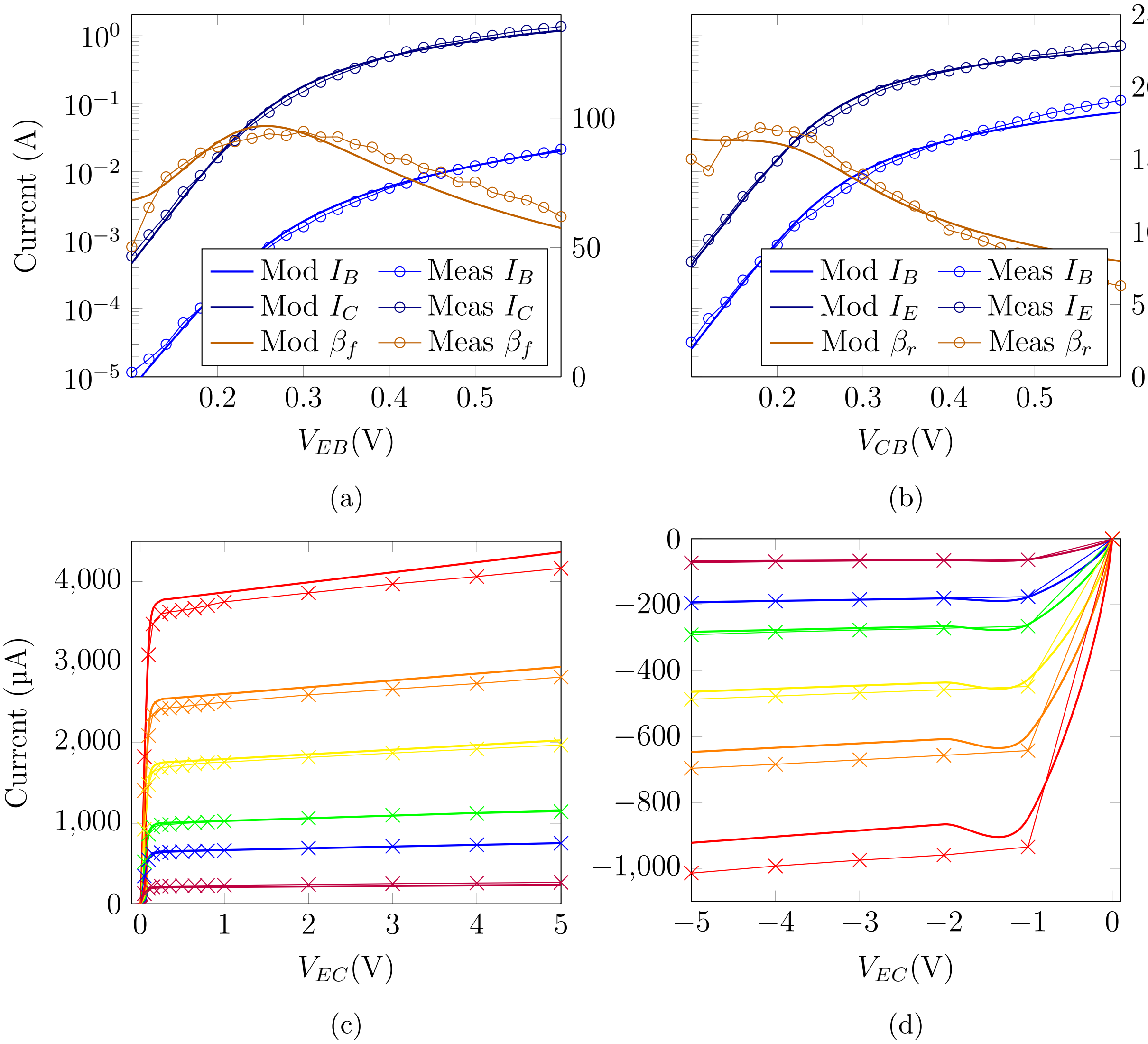


Fig. 4.9 Measured and simulated data for Q1. The simulated forward (a) and reverse (b) gummel plots, and the simulated forward (c) and reverse (d) common-emitter characteristics are shown alongside the measured data from which their GBJT parameters were extracted. From smallest to largest, the base currents of the common-emitter plots are 3 µA, 10 µA, 15 µA, 25 µA, 35 µA, 50 µA. Measured data points for the common-emitter plots are signified by an X. The gummel currents are plotted logarithmically (left y-axis), while the current gain is plotted linearly (right y-axis).

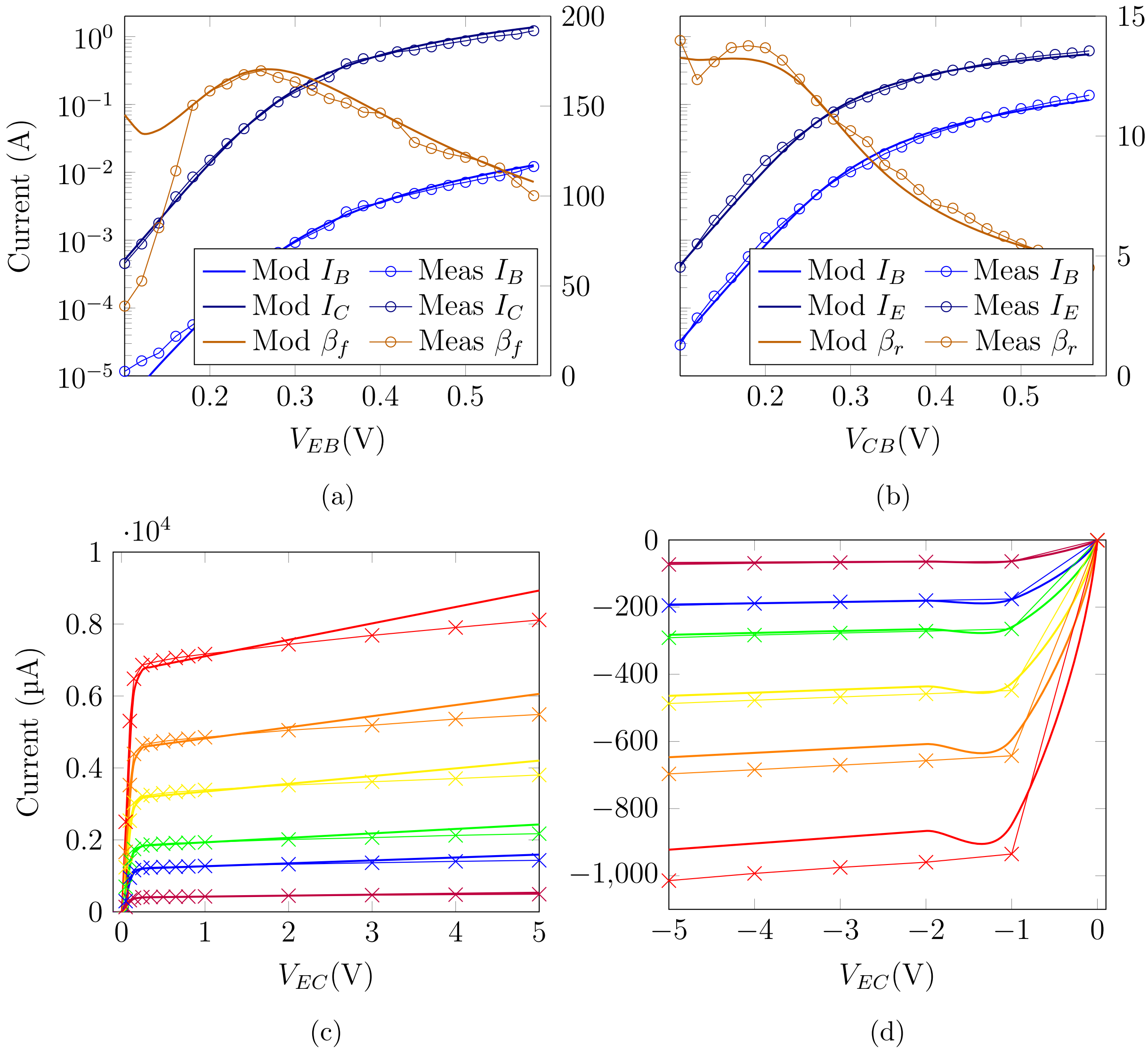


Fig. 4.10 Measured and simulated data for Q2. The simulated forward (a) and reverse (b) gummel plots, and the simulated forward (c) and reverse (d) common-emitter characteristics are shown alongside the measured data from which their GBJT parameters were extracted. From smallest to largest, the base currents of the common-emitter plots are 3 µA, 10 µA, 15 µA, 25 µA, 35 µA, 50 µA. Measured data points for the common-emitter plots are signified by an X. The gummel currents are plotted logarithmically (left y-axis), while the current gain is plotted linearly (right y-axis).

4.5 Results

Having extracted BJT macro-model parameters from the measured data, state space models of the Fuzz Face circuit were then constructed. In this section, the modelling and simulation procedure is presented, along with the subsequent results. Each model is compared using some objective measures including their waveform and spectra for several inputs and their computational cost, followed by an audio comparison.

4.5.1 Model Construction and Simulation

Three state space models of the Fuzz Face schematic, shown in figure 4.1, were constructed in Julia using the tools provided by ACME.jl. Models differed only by the BJT macro-model used: the first used the EM model, while the second and third used the DC SGP and AC SGP models, respectively. This allowed some standard inputs to be processed by each model and their outputs compared.

As mentioned previously, the GBJTs used in the original Fuzz Faces were known to be inconsistently manufactured, meaning their β values varied significantly. So, while the same resistor values were used in most original units (as shown in figure 4.1), the bias points, and therefore the sound characteristics, of each unit varied by some margin. Instead of utilizing the original values in the model, the bias resistors R_2, R_3, and R_4 were tuned to achieve desirable bias voltages as outlined in [156]. Furthermore, a $1\,\mathrm{k}\Omega$ input resistor was added in series with the input voltage source, and the -9V battery was modelled as an ideal DC voltage source. This updated schematic is shown in figure 4.11.

As we recall from section 2.4.2, the synthesis of a non-linear state space model requires the use of an iterative solver at each time step to find a numerical solution of the system's state variables. ACME.jl implements several such iterative solvers, including the classic Newton-Raphson method [148], a Newton Homotopy solver [152], and a k-d tree based caching solver [153]. By default, the three solvers are nested within each other to produce a very robust solver. As such, supplying the model with an accurate initial guess at each time step was not critical to ensure convergence. This robustness does come with a trade-off in computational cost, though the convenience was deemed worthy of the trade-off in cost. This would be especially true for larger circuits.

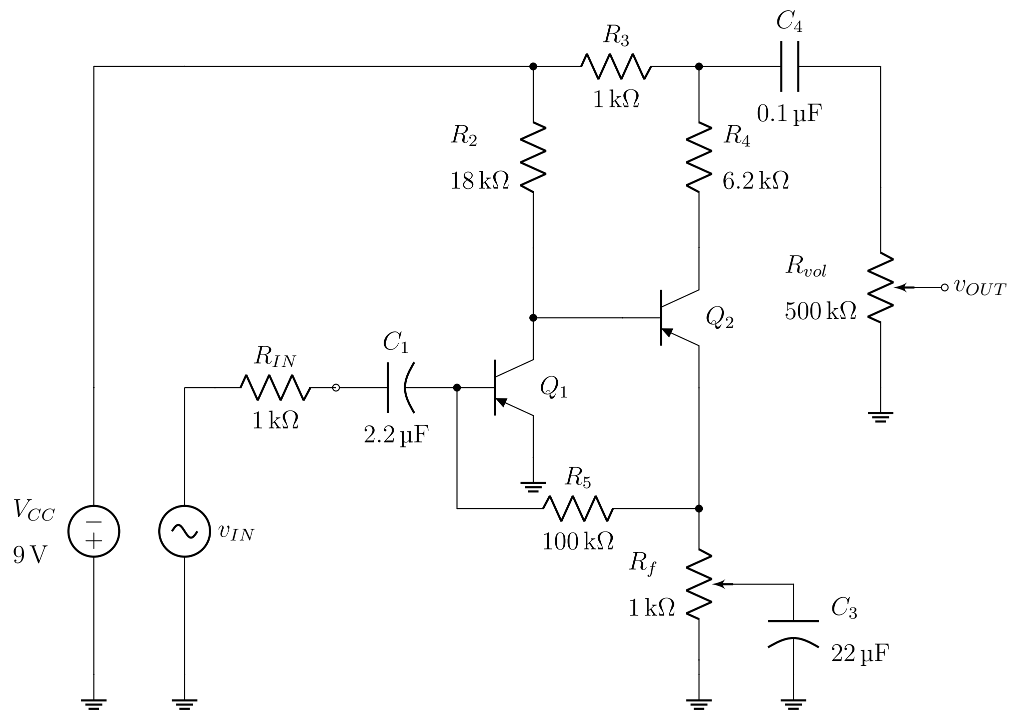


Fig. 4.11 Schematic of the Fuzz Face as modelled Julia using ACME.jl.

4.5.2 Waveform and Spectrum Comparison

Each model was simulated with a family of sinusoidal inputs of varying frequency and amplitude. This provided a good snapshot of the non-linear behaviour of each model, and how their responses changed to varying amplitudes and frequencies. To remove transient behaviour, the models run for several seconds and the end of the simulation was captured, as shown in figure 4.12. Furthermore, since the Fuzz Face creates harmonic distortion, it was important to compare the spectral output of each model for the various input signals. To capture each output spectrum, the Short-Time Fourier Transform (STFT) was taken with the parameters as shown in table 4.5. The final spectrum of each STFT was then extracted, as shown in figure 4.13. For all simulations, the fuzz and volume controls in the Fuzz Face were set to their maximum positions.

Parameter	Value
Window size	8192 samples
FFT size	8192 samples
Hop size	256 samples
Window	Hanning

Table 4.5 STFT parameters used to capture output spectra of each model for the various input signals.

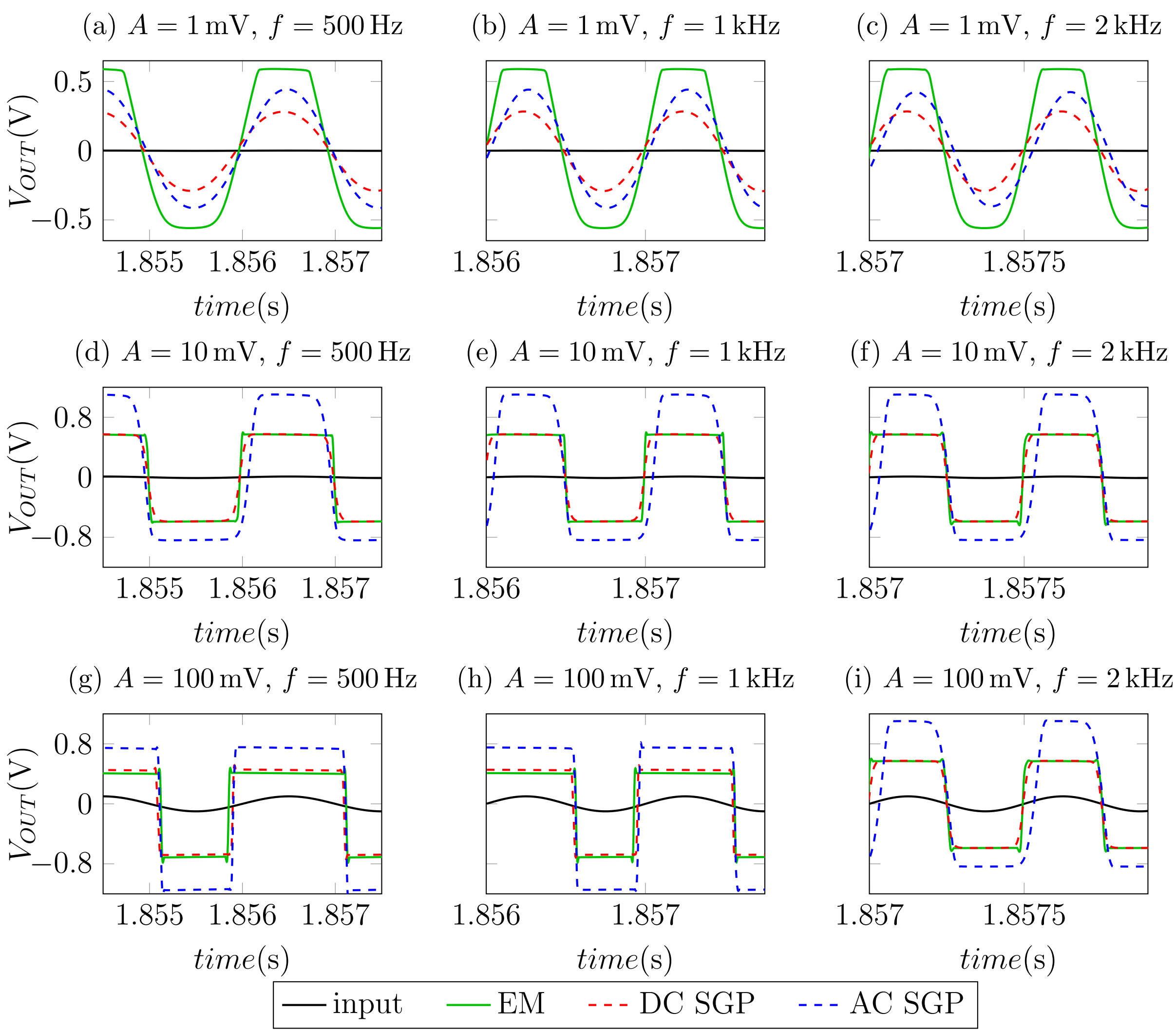


Fig. 4.12 Input and output waveforms produced by each model for the sinusoidal inputs of various amplitudes, A, and frequencies, f, as labelled.

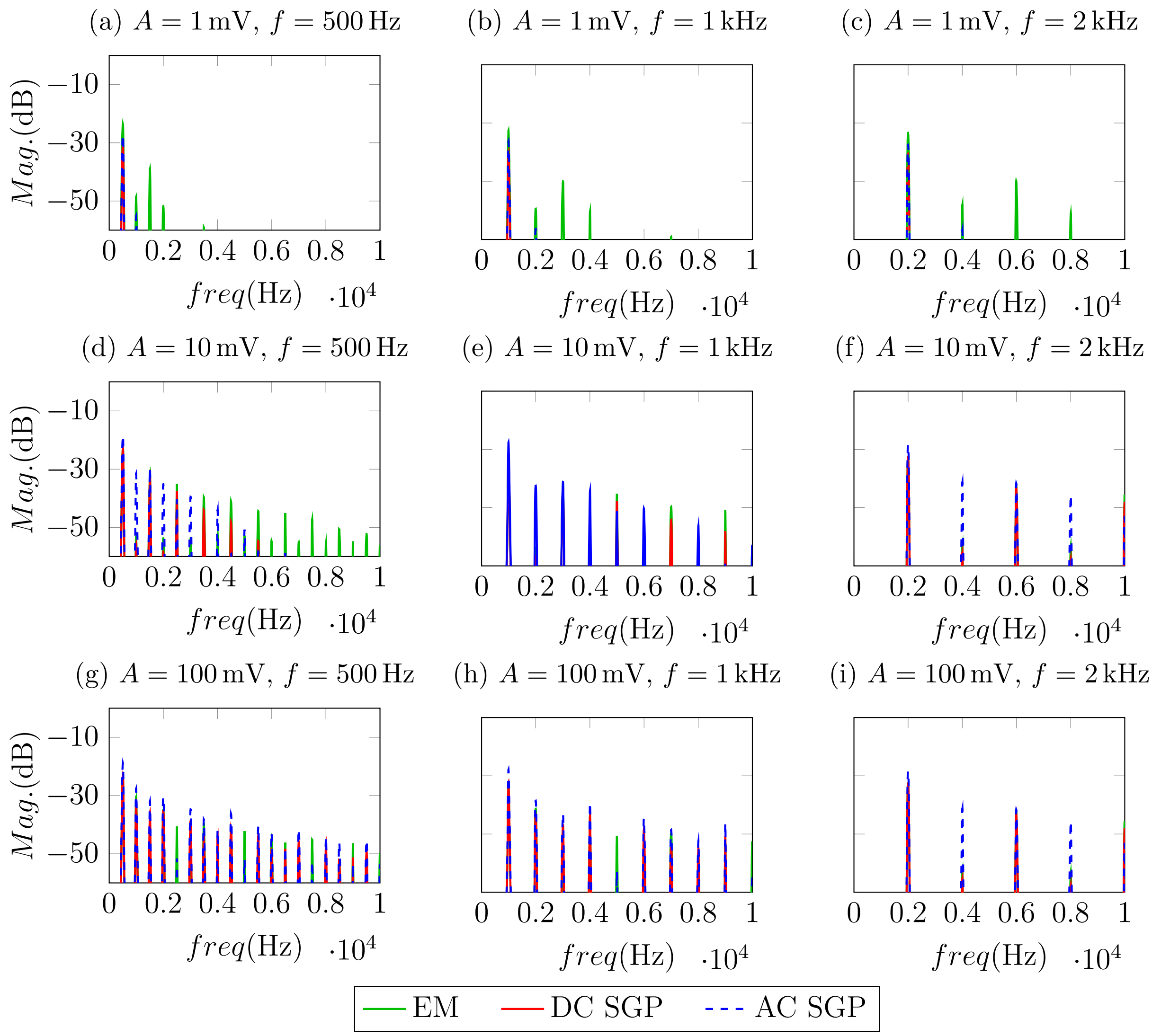


Fig. 4.13 Audio spectra produced by each model for the sinusoidal inputs of various amplitudes, A, and frequencies, f, as labelled.

4.5.3 Computational Cost

The computational cost of each model was evaluated by comparing the median and mean processing times when processing the sinusoidal inputs. Twelve inputs were processed in total, each having a different amplitude and/or frequency. A summary of the statistics is shown in table 4.6, where each value is normalized per second of input signal. The models were simulated in Julia, and tools from the BenchmarkTools.jl package was used to evaluate run times. The models were solved with the homotopy solver algorithm [152] provided in ACME.jl, which ensured that no caching of states or previous results took place.

As expected, the added DC complexity of the SGP model is more costly to simulate than the EM model. Interestingly, though, the incorporation of the additional AC effects in the AC SGP model did not require significantly more computational resources than the DC model.

Model	mean time/s (ms)	median time/s (ms)
EM	766ms	708ms
DC SGP	1030ms	970ms
AC SGP	1087ms	1025ms

Table 4.6 Mean and median processing times per second of input for each model.

4.5.4 Audio Examples

Finally, each model was used to process some audio files, allowing their sound quality to be subjectively compared. Two audio files of a guitar signal were recorded, and each processed by the models at varying levels of the fuzz control: first with the fuzz control set to its minimum setting (”no fuzz”), next with the fuzz control set to half (”half fuzz”), and finally with the fuzz control set to maximum (”full fuzz”). The audio samples are available on the author’s website[4].

[4] `https://www.bennettcustomaudio.com/thesis-material`

Chapter 5

Conclusion

5.1 Summary

In this thesis, the primary objective was to re-implement the BJT modelling techniques originally proposed by Holmes et al. in [23, 160]. The circumstances surrounding the COVID-19 pandemic, however, necessitated novel contributions in the way of BJT measurement techniques.

We began our study by reviewing the BJT, its relevance to audio circuits, and the macro-models commonly used for their computational simulation. Then, research trends in VA were reviewed, with particular emphasis given to state space modelling. We reviewed it's historical developments, fundamental principles, relevance to VA, and the NDK method, which provides a generalized, systematic approach to deriving state space models of electric circuits.

Next, we embarked on a case study to contextualize many of the concepts of the BJT and state space modelling as discussed in the previous chapter. A common-emitter amplifier was designed using basic principles and the small signal model to meet the design specifications as outlined. Then, a non-linear state space model of the final design was constructed using the NDK method. Considerations for the simulation of non-linear state space models were discussed, including the choice of an iterative solver, and initialization of the state variables at each time step. The design was then verified by comparing the voltage gain of the model to the calculated value. Discrepancies were justified by calculating the observed phase difference between input and output.

Finally, state space modelling of the Fuzz Face guitar pedal was investigated. We began by analysing the Fuzz Face schematic, and identified some of its defining characteristics - including objective characteristics and some derived from practical expertise. A pair of GBJTs were measured using a novel, low-cost solution, which provided measured data from which to extract macro-model parameters. This necessarily prompted a discussion on the self-heating effects of the BJT and how to mitigate these effects while taking measurements of these devices. The development of this measurement setup, necessitated by the COVID-19 pandemic, was very challenging and required a lot of experimentation and research.

Parameter extraction consisted of direct extraction from the measurements, followed by a three-stage non-linear optimization process, which closely-matched the behaviour of the macro-models to the measured data. Finally, three state space models of the Fuzz Face were constructed, using the EM, DC SGP, and AC SGP models, respectively, and were compared based on some objective measures, as well as their audio quality. The waveforms, spectra, and computational cost of each model was compared for a set of standard sinusoidal inputs, and their audio quality was compared by processing two different guitar signals at various levels of the "fuzz" control.

The results show that the increase in model complexity from EM to SGP does change the behaviour of the GBJTs. This was particularly prevalent for smaller input levels, where the EM model continued to distort quite heavily, while the SGP model did not. This seems to better suit the observed behaviour of the Fuzz Face, which is known to have reduced distortion as the volume knob of the guitar is turned down. This is further supported by observing their spectra, which shows that the EM model tends to produce more prominent high-order harmonics. Furthermore, the addition of the AC effects also changed the output significantly. While the increase in computational cost from EM to SGP was significant, incorporating AC effects did not come at comparatively as large a cost.

5.2 Recommendations for Future Work

Several topics discussed in this thesis could be extended, and subject to further development. Some possible extensions are noted below:

Measurement Accuracy A low-cost measurement setup was developed in this work that enabled the capture of the required measurements for SGP model parameter extraction. While it eloquently circumvented the self-heating effects of the BJT, it did lack some resolution compared to similar, higher-cost methods. Further development should aim to improve the resolution of this measurement setup.

Adjusting potentiometers with a single rotation is not precise, so setting precise input voltages/currents was difficult. A more accurate adjustment method is therefore recommended. Furthermore, measuring the output waveforms of the pulsed measurements with an oscilloscope and instrumentation amplifiers was very difficult, given the broad range of currents to be measured. The implementation of some sort of auto-scaling of measurements, or automated measurement capture, would reduce the range requirements, allowing smaller (and larger) base voltages to be measured, and in smaller increments.

Implementation of Pulsed Current Source The variable current source developed in this work was pure DC, and as such had strict limitations on the base current values that could be accurately measured for the common-emitter characteristics. It would be interesting to implement a pulsed current source, as outlined in appendix C, to allow larger base currents to be measured without fear of self-heating in the DUT. This would provide a more wholistic view of the device's behaviour.

BJT Model Complexity The SGP model studied in this thesis captures the behaviour of the BJT with good detail, but it is not comprehensive - there are many properties of the BJT not represented in the SGP model. The aforementioned VBIC model is yet to be explored in VA, and was omitted from this work due to its overwhelming complexity. It would be interesting, though, to explore a simplified version of the VBIC model that incorporates features such as the thermal sub-circuit, and more accurate modelling of the AC effects.

Comparison to Actual Hardware While we did not have the chance to do so in this work, future work should seek to verify the audio quality of the model by comparing it to analog hardware. The guitar and amplifier would need to be the same for objective comparison, so the use of an amplifier plugin and audio interface is recommended.

Plugin Development With some run-time optimization, the models developed in this work could be implemented into software plugins, allowing them to be used by musicians in real-time.

Appendix A

E24 Standard Resistor Series

E24	Nominal Values of Resistance						
1.0	1 Ω	10 Ω	100 Ω	1 kΩ	10 kΩ	100 kΩ	1 MΩ
1.1	1.1 Ω	11 Ω	110 Ω	1.1 kΩ	11 kΩ	110 kΩ	1.1 MΩ
1.2	1.2 Ω	12 Ω	120 Ω	1.2 kΩ	12 kΩ	120 kΩ	1.2 MΩ
1.3	1.3 Ω	13 Ω	130 Ω	1.3 kΩ	13 kΩ	130 kΩ	1.3 MΩ
1.5	1.5 Ω	15 Ω	150 Ω	1.5 kΩ	15 kΩ	150 kΩ	1.5 MΩ
1.6	1.6 Ω	16 Ω	160 Ω	1.6 kΩ	16 kΩ	160 kΩ	1.6 MΩ
1.8	1.8 Ω	16 Ω	180 Ω	1.8 kΩ	18 kΩ	180 kΩ	1.8 MΩ
2.0	2 Ω	20 Ω	200 Ω	2 kΩ	20 kΩ	200 kΩ	2 MΩ
2.2	2.2 Ω	22 Ω	220 Ω	2.2 kΩ	22 kΩ	220 kΩ	2.2 MΩ
2.4	2.4 Ω	24 Ω	240 Ω	2.4 kΩ	24 kΩ	240 kΩ	2.4 MΩ
2.7	2.7 Ω	27 Ω	270 Ω	2.7 kΩ	27 kΩ	270 kΩ	2.7 MΩ
3.0	3 Ω	30 Ω	300 Ω	3 kΩ	30 kΩ	300 kΩ	3 MΩ
3.3	3.3 Ω	33 Ω	330 Ω	3.3 kΩ	33 kΩ	330 kΩ	3.3 MΩ
3.6	3.6 Ω	36 Ω	360 Ω	3.6 kΩ	36 kΩ	360 kΩ	3.6 MΩ
3.9	3.9 Ω	39 Ω	390 Ω	3.9 kΩ	39 kΩ	390 kΩ	3.9 MΩ
4.3	4.3 Ω	43 Ω	430 Ω	4.3 kΩ	43 kΩ	430 kΩ	4.3 MΩ
4.7	4.7 Ω	47 Ω	470 Ω	4.7 kΩ	47 kΩ	470 kΩ	4.7 MΩ
5.1	5.1 Ω	51 Ω	510 Ω	5.1 kΩ	51 kΩ	510 kΩ	5.1 MΩ
5.6	5.6 Ω	56 Ω	560 Ω	5.6 kΩ	56 kΩ	560 kΩ	5.6 MΩ
6.2	6.2 Ω	62 Ω	620 Ω	6.2 kΩ	62 kΩ	620 kΩ	6.2 MΩ
6.8	6.8 Ω	68 Ω	680 Ω	6.8 kΩ	68 kΩ	680 kΩ	6.8 MΩ
7.5	7.5 Ω	75 Ω	750 Ω	7.5 kΩ	75 kΩ	750 kΩ	7.5 MΩ
8.2	8.2 Ω	82 Ω	820 Ω	8.2 kΩ	82 kΩ	820 kΩ	8.2 MΩ
9.1	9.1 Ω	91 Ω	910 Ω	9.1 kΩ	91 kΩ	910 kΩ	9.1 MΩ

Appendix B

Fundamental Principles of Electric Circuits

B.1 Introduction

In this chapter, we will examine some fundamentals of electronic circuits and electronic components, as relevant to this work. This is by no means a comprehensive introduction to electronic circuits, as that is beyond the scope of this work. For a full introduction to the topic, the reader is directed to e.g. [74, 75], or any of the available online tutorials[1].

B.2 Electric Circuit Basics

B.2.1 Fundamental Laws of Electricity

Ohm's Law

The most fundamental law of electricity, Ohm's Law, defines the relationship between the voltage across, and the current flowing through a circuit element. The ratio of voltage to

[1] A thorough, free online tutorial can be found here

current is then defined as the element's *resistance*:

$$\begin{aligned} V &= IR \\ I &= \frac{V}{R} \\ R &= \frac{V}{I} \end{aligned} \tag{B.1}$$

The higher the resistance, the less current will flow through the element for a given voltage potential. Conversely, lower resistances permit more current to flow for a given voltage.

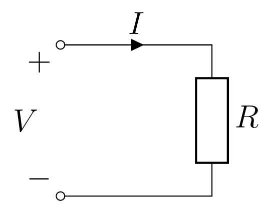


Fig. B.1 Relationship between the voltage across and current through a generic circuit element.

Kirchhoff's Circuit Laws

Kirchhoff's circuit laws offer some fundamental insight into how the currents and voltages within a circuit are distributed. Kirchhoff's Current Law (KCL) states that all current flowing into or out of a circuit node must sum to zero, i.e.:

$$\sum_{n=0}^{N} i_n = 0 \tag{B.2}$$

It is common notation to let currents flowing *into* a node to be positive, and currents flowing *out* of a node to be negative. This allows us the re-write equation B.2 as:

$$\begin{aligned} \sum i_{IN} - \sum i_{OUT} &= 0 \\ \sum i_{IN} &= \sum i_{OUT} \end{aligned} \tag{B.3}$$

Kirchhoff's Voltage Law (KVL) states that the voltage potential around any closed loop of an electric circuit must sum to 0, i.e.:

$$\sum_{k=0}^{K} V_k = 0 \tag{B.4}$$

When applying KCL to a circuit, it is common to consider voltage drops across source elements as *negative* and voltage drops across passive elements to be *positive*. In that case, a *drop* in voltage potential is considered to be positive. This implies that the voltage provided by source elements must equal the voltage drops across passive elements, i.e.:

$$\begin{aligned} -\sum V_{source} + \sum V_R &= 0 \\ \sum V_{source} &= \sum V_R \end{aligned} \tag{B.5}$$

Resistors in Series and Parallel

Resistors are said to be in *series* when they share a single node, as illustrated in figure B.2. As such, the same current flows through each resistor and the voltage drop across each resistor will be proportional to the resistance of each element.

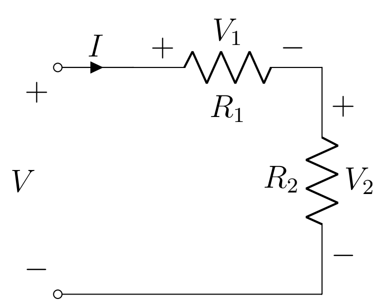


Fig. B.2 Two resistors in series.

From figure B.2, it is observed that:

$$\begin{aligned} V &= V_1 + V_2 \\ V &= IR_1 + IR_2 \\ I &= \frac{V}{R_1 + R_2} = \frac{V}{R_{tot}} \end{aligned} \tag{B.6}$$

Then, we may consider the voltage across R_2, defined as V_2, and express it as a proportion of the total voltage, V:

$$
\begin{aligned}
V_2 &= IR_2 \\
&= \left(\frac{V}{R_1 + R_2}\right) R_2 \\
&= \left(\frac{R_2}{R_1 + R_2}\right) V
\end{aligned} \tag{B.7}
$$

The ratio of the voltage across R_2 to the total voltage is thus equal to the quotient of R_2 and the total resistance. This property is known as the *voltage divide rule*, and it is fundamental to all electronic circuit analysis. It is valid for any number of resistances in series, and can be expressed more generally as:

$$
\begin{aligned}
\frac{V_n}{V} &\equiv \frac{R_n}{R_{tot}} \\
V_n &= \left(\frac{R_n}{R_{tot}}\right) V, \quad R_{tot} = R_1 + R_2 + \cdots + R_N
\end{aligned} \tag{B.8}
$$

A similar analysis may be performed for resistors in parallel. Circuit elements are said to be connected in *parallel* if both of their nodes are connected together, as shown in figure B.3. The voltage across each element will therefore be equal, and the current flowing through each resistor will be a fraction of the total current, I.

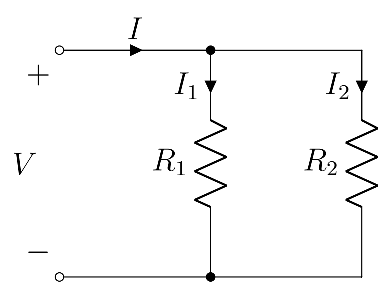


Fig. B.3 Two resistors in parallel.

From inspection of figure B.3, it is observed that:

$$
\begin{aligned}
I &= I_1 + I_2 \\
I &= \frac{V}{R_1} + \frac{V}{R_2} \\
I &= \left(\frac{1}{R_1} + \frac{1}{R_2}\right) V \\
V &= IR_{tot}, \quad \frac{1}{R_{tot}} = \left(\frac{1}{R_1} + \frac{1}{R_2}\right)
\end{aligned}
\tag{B.9}
$$

where R_{tot} is the total resistance of the circuit. Expanding R_{tot} yields:

$$
\begin{aligned}
\frac{1}{R_{tot}} &= \frac{1}{R_1} + \frac{1}{R_2} \cdot \left(\frac{R_1 R_2}{R_1 R_2}\right) \\
\frac{1}{R_{tot}} &= \frac{R_2}{R_1 R_2} + \frac{R_1}{R_1 R_2} = \frac{R_1 + R_2}{R_1 R_2} \\
R_{tot} &= \frac{R_1 R_2}{R_1 + R_2}
\end{aligned}
\tag{B.10}
$$

From there, the resistor currents may be found as a proportion of the total current, I:

$$
\begin{aligned}
I_1 &= \frac{V}{R_1} \\
I_1 &= \frac{IR_{tot}}{R_1} \\
I_1 &= \left(\frac{R_{tot}}{R_1}\right) I \\
I_1 &= \left(\frac{1}{R1}\right) \left(\frac{R_1 R_2}{R_1 + R_2}\right) I \\
I_1 &= \left(\frac{R_2}{R_1 + R_2}\right) I
\end{aligned}
\tag{B.11}
$$

The current through the resistor R_1 is therefore *inversely* proportional to its resistance, and proportional to R_{tot}. As such, a larger resistor will have a *smaller* fraction of the total current flowing through it, while a smaller resistor will have a *larger* fraction of the current flowing through it. This property is known as the *current divide rule*, and it can be expressed more generally for any number of resistors in parallel:

$$\begin{aligned} \frac{I_n}{I} &\equiv \frac{R_{tot}}{R_n} \\ I_n &= \left(\frac{R_{tot}}{R_n}\right) I, \quad \frac{1}{R_{tot}} = \left(\frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_N}\right) \end{aligned} \tag{B.12}$$

B.2.2 Filter Basics

Departing from the bounds of purely resistive circuits, we now formally introduce the capacitor, the idea of a complex *impedance*, and demonstrate how the capacitor's impedance is *frequency-dependent*.

First, the concept of *impedance* and *reactance* is formalized. Throughout this work, the terms resistance and impedance appear to be used interchangeably, though there is a fundamental difference: resistance is purely *real*, while impedance is *complex*. Impedance may be displayed in *cartesian form*, or *exponential form*, by applying Euler's identity:

$$\begin{aligned} Z &= R + jX \\ Z &= |Z|e^{j\theta} \end{aligned} \tag{B.13}$$

where Z represents impedance, R is the familiar resistance, X is *reactance*, and $j = \sqrt{-1}$. Furthermore, $|Z|$ and θ represent the *magnitude* and *phase*, respectively:

$$\begin{aligned} |Z| &= \sqrt{R^2 + X^2} \\ \cos\theta &= \frac{R}{|Z|} \\ \sin\theta &= \frac{X}{|Z|} \end{aligned} \tag{B.14}$$

The exponential form is often referred to as *phasor notation* in electrical engineering. The impedance of a circuit element is therefore a complex sum of its resistance and reactance. A full introduction to imaginary and complex numbers falls outside the scope of this work, but the primary implication of their presence here is that they represent the *frequency-dependent* component of an element's impedance. Furthermore, ohm's law may be re-defined for the complex domain as:

$$\begin{aligned} v &= iZ \\ i &= \frac{v}{Z} \\ Z &= \frac{v}{i} \end{aligned} \tag{B.15}$$

where v, i, and z are all complex values.

The Capacitor

A capacitor is an *energy storage* element, consisting of two parallel plates. The amount of energy, or "charge" stored in a capacitor is proportional to its capacitance and the voltage across it:

$$Q = CV \tag{B.16}$$

where Q is the charge in Coulombs, and C is the capacitance in Farads. Electric current is simply the flow of electric charge over time, so:

$$\frac{\mathrm{d}Q}{\mathrm{d}t} = i_C(t) = C\frac{\mathrm{d}v_C(t)}{\mathrm{d}t} \tag{B.17}$$

and conversely, the voltage across a capacitor is proportional to the integral of the current flowing through it:

$$v_C(t) = \frac{1}{C}\int_{-\infty}^{t} i_C(\tau)d\tau \tag{B.18}$$

To find the impedance of a capacitor, consider the case where the voltage across the capacitor is a sinusoidal function, i.e.:

$$v_C = \cos(\omega t + \phi) \tag{B.19}$$

v_C may be expressed in the *phasor notation* by applying Euler's identity once more, yielding:

$$v_C = e^{j(\omega t+\phi)} = e^{j\omega t}e^{j\phi} \tag{B.20}$$

where ω is the radial frequency, i.e. $\omega = 2\pi f$, and ϕ is an angle in radians. Substituting this expression for v_C into equation B.17 allows the capacitor's impedance to be found:

$$\begin{aligned} i_C &= C\frac{\mathrm{d}e^{j\omega t}e^{j\phi}}{\mathrm{d}t} = Cj\omega e^{j\omega t}e^{j\phi} \\ i_C &= j\omega C v_C \\ \frac{v_C}{i_C} &\equiv Z_C = \frac{1}{j\omega C} = \frac{-j}{2\pi f C} \end{aligned} \tag{B.21}$$

The impedance of a capacitor is purely reactive, and is inversely proportional to the radial frequency of the input voltage and its capacitance. Its impedance then, is frequency-dependent, and changes with the rate of change of the voltage across it.

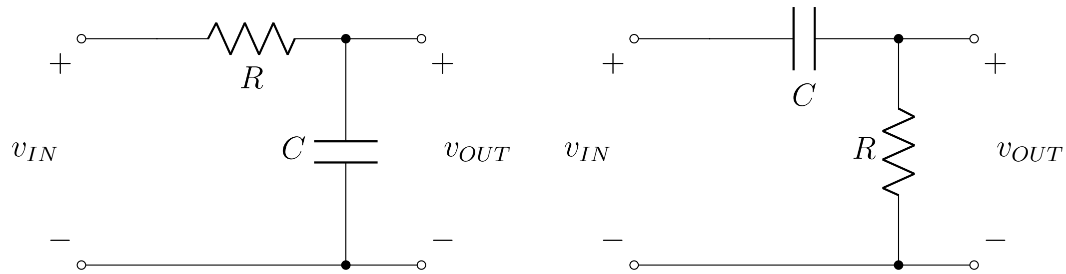
By appling the limit as f approaches zero, it is observed that the impedance of the capacitor will approach infinity. For DC voltages ($f = 0$), then, the capacitor behaves as an open circuit. As such, capacitors are frequently used to couple various stages of a circuit together, while keeping the various DC bias voltages isolated from one another.

Conversely, as f approaches infinity, the impedance of the capacitor approaches zero. Therefore, to high frequency signals, the capacitor appears as a short circuit. What constitutes a "high frequency" is dependent on the capacitance, and the context in which the capacitor is used.

In summary, capacitors do not pass DC voltages, and present a steadily decreasing impedance to AC signals as the signal's frequency increases. This allows the capacitor to be used as a *filter* - attenuating and removing unwanted frequencies from a signal, while readily allowing frequencies of interest to pass through.

RC Filters

The two most basic filter configurations, *low-pass* and *high-pass*, can be achieved using simply a resistor and a capacitor. Their schematics are shown in figure B.4.



(a) The RC low-pass filter.

(b) The RC high-pass filter.

Fig. B.4

Consider the voltage across the capacitor in figure B.4a, denoted by v_{OUT}. By applying the voltage divide rule, it's relation to the input voltage, v_{IN}, may be found:

$$\begin{aligned} v_{OUT} &= \left(\frac{Z_C}{R+Z_C}\right) v_{IN} \\ v_{OUT} &= \left(\frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}\right) v_{IN} \\ v_{OUT} &= \left(\frac{1}{1+j\omega RC}\right) v_{IN} \end{aligned} \tag{B.22}$$

Rearranging the equation and taking the magnitude of the complex impedance gives:

$$\frac{v_{OUT}}{v_{in}} = \frac{1}{\sqrt{1+(\omega RC)^2}} \tag{B.23}$$

Three cases can then be considered:

$\omega RC \ll 1$ The voltage divider formula can be approximated as 1, $v_{OUT} \approx v_{IN}$

$\omega RC = 1$ The amplitude is attenuated by $1/\sqrt{2}$, i.e. $v_{OUT} = (1/\sqrt{2})v_{IN}$. At this point, the signal's amplitude has been attenuated by 3 dB.

$\omega RC \gg 1$ The input is heavily attenuated. As the frequency ω is doubled (an “octave”), the signal's amplitude is attenuated by a further 6 dB.

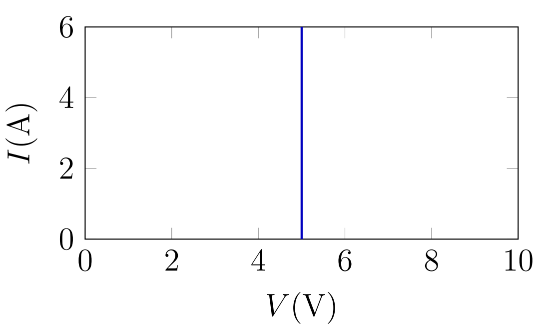
For lower frequencies, below $\omega RC = 1$, the signal will pass through unimpeded, hence the name *low-pass*. Signals whose frequency is beyond $\omega RC = 1$, however, are attenuated at a rate of -6dB per octave. This inflection point, then, represents the cut-off of frequencies that are passed, where attenuation begins. As such, it is referred to as the *cut-off frequency* of the filter, denoted as ω_o, and it can be designed by tuning the values of R and C, as shown in chapter 3:

$$\omega_o = \frac{1}{RC} \qquad f_o = \frac{1}{2\pi RC} \tag{B.24}$$

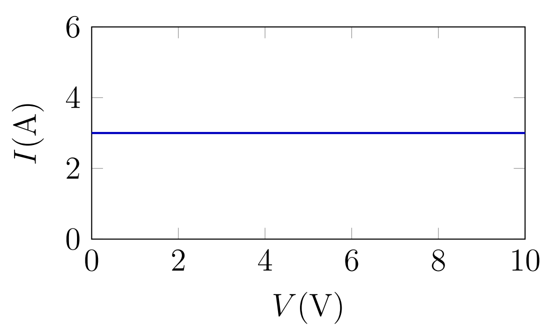
For the case of a high-pass filter, the definition of the cut-off frequency is the same, though the behaviour is reversed: frequencies below the cut-off are attenuated, while higher frequencies pass unattenuated.

B.2.3 The Ideal Voltage and Current Source

Throughout this work, voltage and current sources are assumed to be ideal. That is, their $I - V$ characteristics are as shown in figure B.5. For the case of the ideal voltage source, its output voltage remains constant regardless of the current flowing through it. Likewise, the ideal current source delivers a constant current, regardless of the voltage drop across it. This implies that an ideal voltage source has an impedance of 0, while the ideal current source has infinite impedance.



(a) Ideal voltage source.



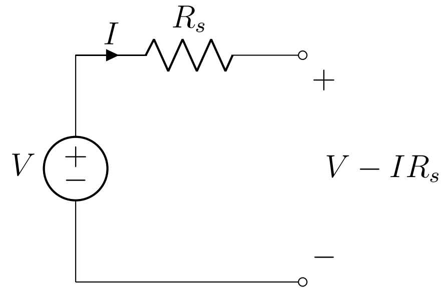
(b) Ideal current source.

Fig. B.5 $I - V$ characteristics of the ideal voltage and current source.

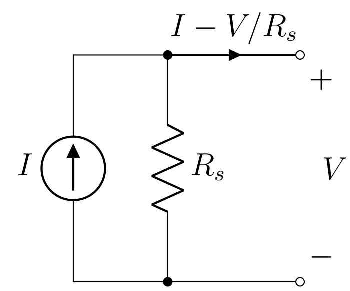
These assumptions are exploited during small-signal analyses, where voltage and current sources are replaced by a short circuit and open circuit, respectively, to simplify the analysis.

Practical Voltage and Current Sources

Of course, practical DC sources do not exhibit ideal behaviour. All practical voltage sources have some small series resistance, and all practical current sources have some large, finite parallel resistance across it. These practical representations are shown in figure B.6.



(a) A practical DC voltage source.



(b) A practical DC current source.

Fig. B.6 Schematics of the practical DC voltage and current sources.

B.3 The *pn* Junction and the Diode

In this section, a brief overview of the pn junction is given. An understanding of the pn junction is a prerequisite to understanding the BJT, as the BJT simply consists of two *pn* junctions. The diode is simply the implementation of a *pn* junction, and so they will naturally be discussed as well. This overview is not intended to be comprehensive. For a complete introduction, the reader is referred to chapters 3 and 4 of [75].

B.3.1 Physical Structure and Overview of the *pn* Junction

The simplified physical structure of the *pn* junction is shown in figure B.7. As the name implies, it consists of two regions of doped semiconductor material, one *p-type* and one *n-type*, with a metal contact connected to each. the *p-type* contact is the "Anode", and the *n-type* contact is the "Cathode".

A *p-type* region has an excess of free holes, i.e. positive charges, while *n-type* regions have an excess of negatively-charged particles (electrons). Because of this imbalance, some holes will diffuse across the junction to the *n* side, and conversely, some electrons will diffuse across to the *p* side. These two currents sum together to form the *diffusion current*,

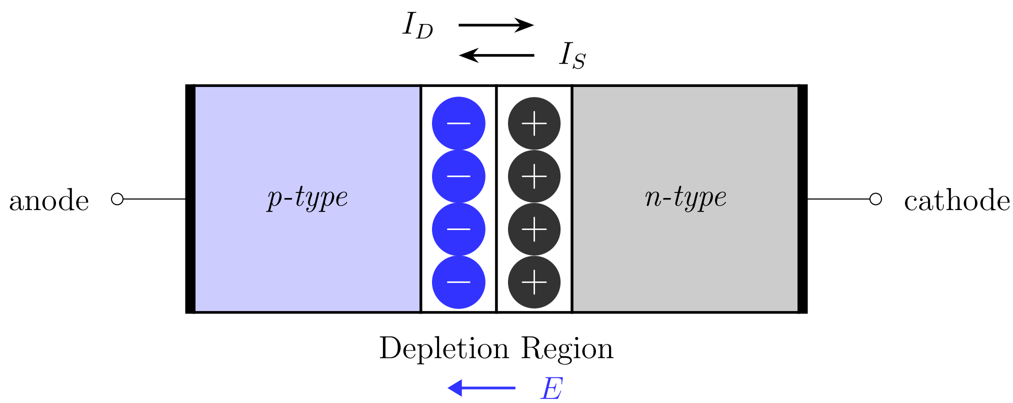


Fig. B.7 Simplified internal structure of a *pn* junction, shown with depletion region, diffusion current, I_D, minority carrier current, I_S, and barrier electric field, E.

I_D, which flows from the p side to the n side.

The diffused holes in the n side quickly recombine with free electrons, thus neutralizing both charges. Furthermore, some of the bound positive charges in the n side are no longer neutralized by the free electrons - this creates a small region close to the junction that is devoid of free electrons, and thus has a net *positive* charge. The reverse is true for the electrons flowing to the p side, which creates a small region of *negative* charge, close to the junction. This small region encompassing either side of the junction is referred to as the *depletion region*, as it has been depleted of free charges.

The charge of the depletion region establishes an electric field, E, as shown in figure B.7, across the junction from n to the p region - a potential difference has been established by the diffusing charges. This potential difference acts as a barrier that must be overcome by the holes in the p region in order to diffuse to the n region, and vice versa for electrons. The more charges that diffuse, the stronger the electric field becomes, and the more difficult it becomes for subsequent charges to diffuse. Eventually, an equilibrium is reached where very few free charges overcome the established electric field. A small current due to thermally-generated *minority carriers* (i.e. holes from n to p, and electrons from p to n) also exists across the junction, which oppose the majority-carrier diffusion, I_D. This minority-carrier diffusion current is denoted by I_S, and equilibrium is achieved when the two currents are equal:

$$I_D = I_S \tag{B.25}$$

I_S denotes the *saturation current*, found extensively throughout this work as a parameter of the BJT. Since these minority carriers are thermally generated, I_S is highly dependent on temperature, though independent of the strength of the electric field, E.

The potential difference established in the depletion region maintains this equilibrium between majority and minority carriers. It is referred to as the *barrier voltage*, or the *junction built-in voltage*, denoted by V_o. For *pn* junctions fabricated from silicon, V_o is typically 0.6 V to 0.9 V. For *pn* junctions fabricated from germanium, V_o is typically 0.2 V to 0.4 V.

The *pn* Junction in Reverse-Bias

Consider the case where the *pn* junction is reverse-biased by an external voltage, V. This puts the cathode at a positive potential with respect to the anode. Recall that the barrier voltage, V_o points from cathode to anode. Therefore, this applied voltage will *add* to the barrier voltage, increasing the effective barrier voltage to $(V_o + V)$, which will widen the depletion region. This makes it even more difficult for majority carriers to diffuse across the junction, and so I_D is reduced significantly. If the external voltage exceeds approximately 1 V, I_D is effectively reduced to 0, and only the very small, constant I_S current flows across the junction, from n region to p region.

The Forward-Bias Case

For the forward-bias case, the external voltage will *oppose* the barrier voltage, by applying a positive voltage potential from anode to cathode. This reduces the effective depletion region and encourages the diffusion of majority carriers across the junction. The current flowing from anode to cathode is therefore:

$$I = I_D - I_S \tag{B.26}$$

In the forward bias case, then, the *pn* junction can conduct a substantial current, comprised primarily of the diffusion of majority carriers. This current will increase *exponentially* with the external voltage, V, and is defined as:

$$I = I_S \left(e^{\frac{V}{V_t}} - 1 \right) \tag{B.27}$$

where V_t is the thermal voltage. This equation is the $i - v$ relationship of the junction diode, described by Shockley in [61], and first introduced in this work in equation 2.36.

When the external voltage V exceeds the barrier voltage, the depletion region shrinks almost completely, and charges are able to flow almost unimpeded. Beyond this point, the current flowing through the diode will rinse rapidly. However, since the barrier voltage has been overcome, the voltage drop across the pn junction remains almost constant. This property can be attributed to the almost constant voltage drop observed across a diode, or the EBJ of a BJT when it is forward-biased.

An analogy can be made between the pn junction and a one-way water valve. With pressure applied in the reverse direction, no water flows through the valve. But, with pressure applied in the forward direction, water is permitted to flow unobstructed. Such is the case for the pn junction: In the reverse bias direction, current cannot flow. In the forward bias direction, current is allowed to flow freely.

B.4 The Operational Amplifier

The operation amplifier ("op amp") is ubiquitous with analog electronics. Originally invented in the 1950s in Bell labs, it can be found in nearly every discipline throughout the world of electronics. An op amp is an example of an IC, meaning that its internal structure consists of many basic elements, including BJTs, resistors, and capacitors, all fabricated on a single wafer of semiconductor material.

Op amps were used extensively throughout this work in a variety of applications. In this section, it is formally introduced and its ideal characteristics are discussed. Then, some basic op amp configurations are reviewed, illustrating the effect of negative feedback on the op amp, and how that makes them so useful and flexible. For a comprehensive introduction to the op amp, the reader is referred to chapter 2 of [75].

B.4.1 The Ideal Op Amp

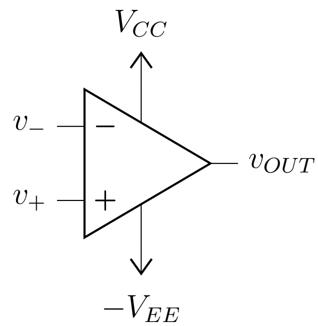


Fig. B.8 Circuit symbol of the ideal op amp.

The schematic symbol of the op amp is shown in figure B.8. It is powered by two DC voltages, V_{CC} and $-V_{EE}$. It has two signal inputs, the non-inverting input, v_+, and the inverting input, v_-. The output voltage, v_{OUT} is created by amplifying the *difference* between its two inputs by a *differential gain* factor, A, ignoring any components that are common to both inputs. This phenomena is referred to as *common-mode rejection.* The op amp, therefore, is a differential amplifier. The output voltage may then be expressed as:

$$v_{OUT} = A\,(v_+ - v_-) \tag{B.28}$$

For the ideal op amp, the differential gain factor (also called the "*open loop gain*") is infinite. Furthermore, the input resistance at the two input terminals is infinite, and the output resistance of the output terminal is zero. We may therefore consider the op amp to be an ideal Voltage-Controlled Voltage Source (VCVS), where the control voltage is the difference of the two inputs. Practically speaking, an infinite gain is not very useful - if the two inputs are not equal, the output will simply swing to $\pm\infty$. The op amp is almost never used alone, though. It is almost always used with the addition of *feedback.*

B.4.2 The Inverting Configuration

Consider the schematic shown in figure B.9. R_1 is connected between the input voltage source, v_{IN} and the inverting terminal, while R_2 is connected between the inverting terminal and the output. The non-inverting input is simply tied to ground. R_2, therefore, *closes* *the loop* around the amplifier, establishing what is known as *negative feedback*.

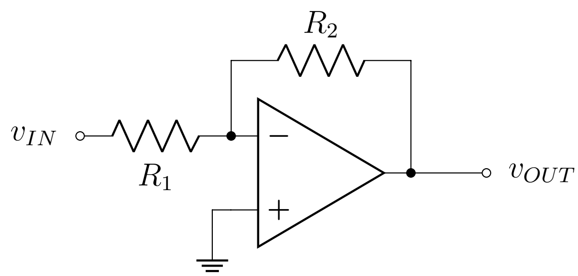


Fig. B.9 The inverting amplifier.

Negative feedback has the effect of reducing the gain, but increasing the linearity and stability of an amplifier. Therefore, it is assumed that a non-infinite output may be achieved by the addition of negative feedback. To investigate the effect of negative feedback on the op amp, the schematic of figure B.9 is analysed to find its *closed loop gain*, G, defined as:

$$G \equiv \frac{v_{OUT}}{v_{IN}} \tag{B.29}$$

Assuming that the circuit is producing a non-infinite output, equation B.28 can be rearranged to show that the voltage difference between the two input terminals approaches zero, i.e.:

$$\begin{aligned} v_+ - v_- &= \frac{v_{OUT}}{A} = 0 \\ v_+ &= v_- \end{aligned} \tag{B.30}$$

This phenomena is known as the *virtual short circuit* of the closed-loop op amp. And, since v_+ is connect to ground, a *virtual ground* is established at v_-. Having determined that $v_- = 0\,\mathrm{V}$, applying Ohm's law finds the current flowing through R_1:

$$\begin{aligned} i_1 &= \frac{v_{IN} - v_-}{R_1} = \frac{v_{IN} - 0}{R_1} \\ i_1 &= \frac{v_{IN}}{R_1} \end{aligned} \tag{B.31}$$

Since the input resistance of the ideal op amp is infinite, no current flows into the op amp's input terminals. Therefore, all of the current flowing through R_1 must flow through R_2. Apply Ohm's law to R_2 once again allows the relationship between v_{IN} and v_{OUT} to be determined:

$$\begin{aligned} i_1 &= -i_2 \\ \frac{v_{IN}}{R_1} &= \frac{0 - v_{OUT}}{R_2} = -\frac{v_{OUT}}{R_2} \\ \frac{v_{OUT}}{v_{IN}} &\equiv G = -\left(\frac{R_2}{R_1}\right) \end{aligned} \tag{B.32}$$

The closed loop gain, then, is simply the ratio of the two resistors. The minus sign indicates that the output signal is inverted from the input signal. Unlike the BJT, the closed-loop gain of the op amp depends entirely on external, passive components. This allows the behaviour of the amplifier to be controlled with high accuracy, and to do so repeat-ably. This also illustrates the effect of negative feedback - we began with a finite, uncontrollable gain, and created a stable, predictable gain.

B.4.3 The Non-Inverting Configuration

The non-inverting amplifier is shown in figure B.10. Here, the input and ground are effectively swapped from the previous example. The input signal is fed directly into the non-inverting input of the op amp, and R_1 connects the inverting input to ground.

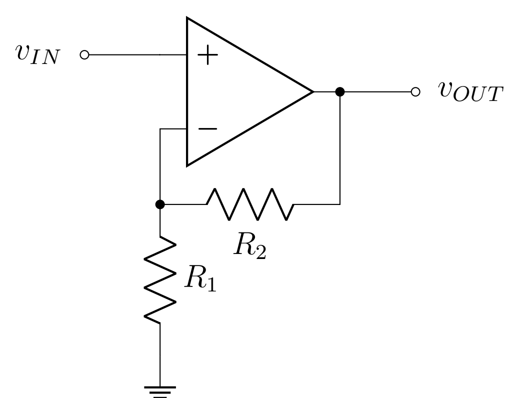


Fig. B.10 The non-inverting amplifier.

The circuit may be analysed in a similar fashion. Since negative feedback has been established, we know that $v_+ = v_-$. And, since no current flows into the op amp's input terminals, the output voltage can be found simply by applying the voltage divide rule for

R_1 and R_2:

$$\begin{aligned} v_- = v_{IN} &= \left(\frac{R_1}{R_1 + R_2}\right) v_{OUT} \\ \frac{v_{OUT}}{v_{IN}} \equiv G &= \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} \end{aligned} \tag{B.33}$$

The gain factor in this case is *positive*, indicating that the input and output are *in-phase* with one another. Furthermore, unlike the inverting case, the gain of the non-inverting amplifier cannot be less than one. As R_1 approaches infinity, i.e. an open circuit, the gain of the non-inverting amplifier becomes 1.

Input Resistance

For the non-inverting case, the input connects directly to the non-inverting input of the op amp. We recall that the input resistance of the op amp is near infinite, which implies that the input source experiences no loading from the op amp. As such, the non-inverting amplifier configured with a gain of 1 is commonly used as a *buffer*, similar to the emitter-follower discussed in section 2.2.3. The op amp buffer, however, has a near infinite input impedance, a true gain factor of 1, and a ideal output impedance of 0.

In the inverting case, the input resistance is simply equal to R_1, and as such, typically has a much lower input resistance.

Appendix C

Considerations for Performing GBJT Measurements

C.1 Introduction

In chapter 4, an overview of the two measurement setups designed for this work, a variable current source and a pulsed-DC voltage source, were introduced and discussed on a high level. In this appendix, we aim to further elaborate on the design process, component choices, and function of these two measurement setups.

In keeping with the general philosophy of this work, all of the measurements were captured using only a two-channel power supply, 2-3 Digital Multi-Meter (DMM), a two-channel oscilloscope, and the accompanying analog electronics, to be discussed in the sections to follow.

C.2 Designing a Precision Current Source

The final current source design as shown in section 4.3.2 consists of an op amp-BJT current source and a cascode current mirror. The complete circuit is shown in figure C.1 with specified component values and voltage rails.

The design of the circuit begins with a TL062 dual channel op-amp, IC_1, biased by one channel of the power supply with ground connected to its V_{CC} pin, and $-15\,\text{V}$ connected to the V_{EE} pin. A power supply voltage of $-15\,\mathrm{V}$ was chosen to ensure that the voltage across the current source would not be limited by the supply voltage. The TL062 was chosen because its common-mode input/output range includes the V_{CC} rail (ground in this case). This alleviated the need to power the op amp with a split power supply, i.e. $15\,\mathrm{V}$ and $-15\,\mathrm{V}$, leaving the other channel of the supply free to use as V_{EC}. Any op-amp with rail-to-rail input/output would suffice, assuming the power supply does not exceed its voltage limit.

The resistors R_1 and R_2 form the reference voltage, with the resistor values chosen to give $V_{ref} = -0.5\,\mathrm{V}$ - this was chosen somewhat arbitrarily, though it simplified the choice of the resistor R_{sense} in the next stage. That allows the input of the op amp-BJT current source to be swept from $-0.5\,\mathrm{V} - 0\,\mathrm{V}$. R_{sense} was specified as $10\,\mathrm{k\Omega}$, which gives the current source the desired output range of $0\,\mathrm{\mu A} - 50\,\mathrm{\mu A}$. For Q_1, a BC550C pnp BJT was used, while $Q_2 - Q_5$ were 2N3904 npn BJTs. The polarity of the BJTs was required to insure that currently flowed in the correct direction, though the choice of BJT is trivial - any small signal BJT will suffice. Likewise, the choice of a negative power supply, as opposed to a positive power supply, was necessary to facilitate proper current flow, and to ensure that the EBJ of the DUT was forward-biased.

The variable current source, shown in isolation in figure C.2a, is also referred to as a "transconductance amplifier" - a VCCS. It functions as follows: since negative feedback is established around the op amp, the op amp will adjust its output voltage to hold both its inputs to the same potential. In this case, the output of the op amp connected to the base, and the emitter of Q_1 is connected to the negative input, which puts EBJ in the feedback loop. This asserts that the EBJ will be forward-biased, while the emitter voltage is simultaneously controlled by the op amp's input. So, by setting the voltage at the non-inverting input using the potentiometer, we are also setting V_E of a forward-biased BJT, which induces a current flowing out of the collector.

Experimentally, it was discovered that the transconductance amplifier alone did not have a sufficiently high output impedance to reliably deliver current to the DUT. As such, it was necessary to increase the output impedance. To do so, a BJT current mirror was connected at the output of the transconductance amplifier. A current mirror is a two-terminal circuit that has the function of "copying" a reference current, I_{ref}, flowing into (or out of) its input terminal at its output terminal. They are commonly designed using

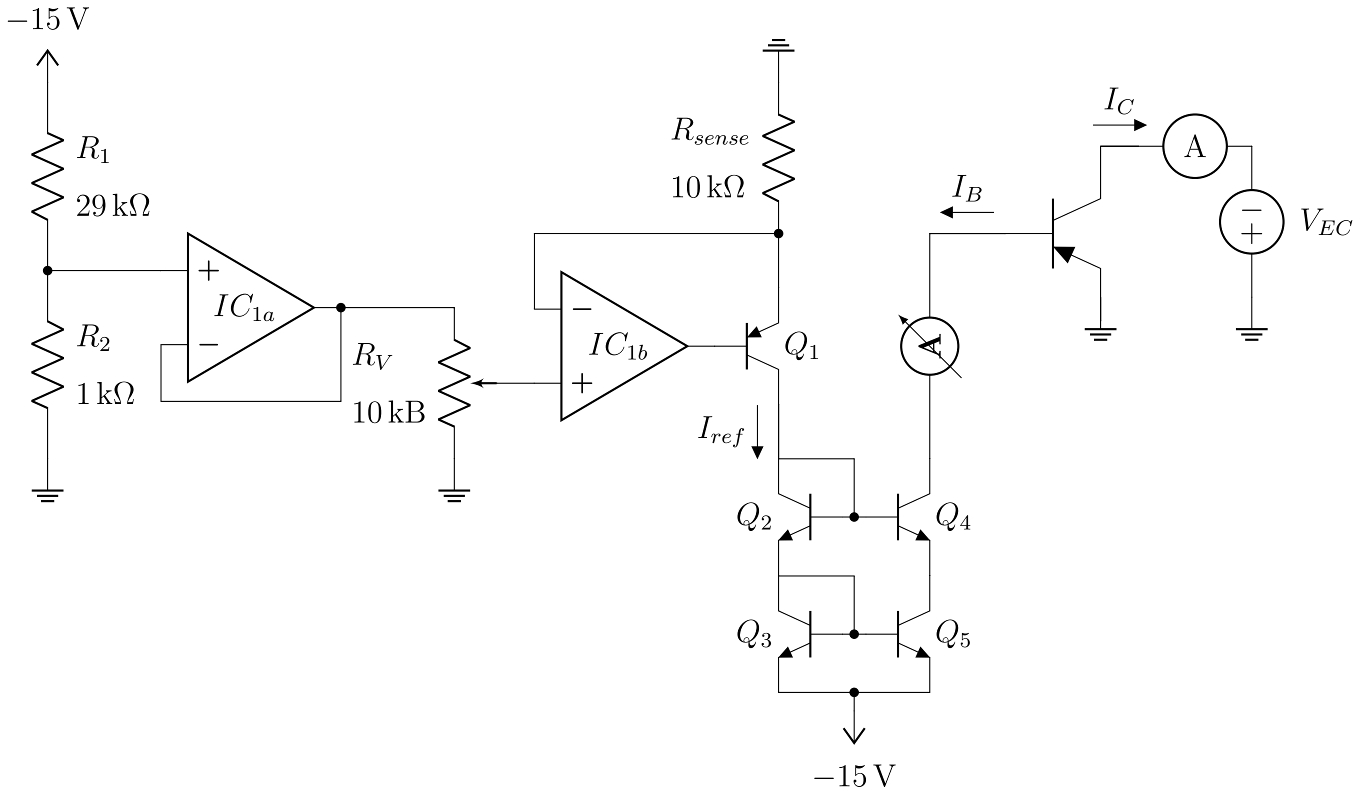
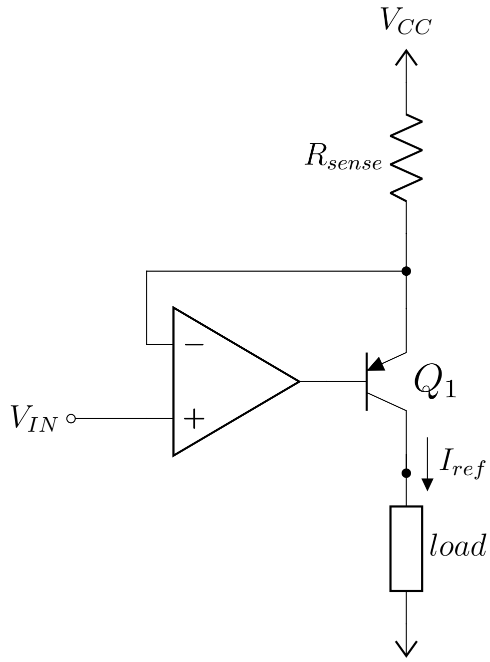


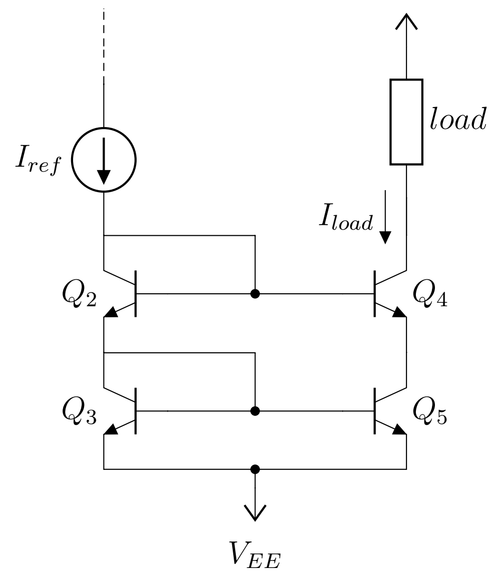
Fig. C.1 Complete schematic of GBJT common-emitter measurement setup.

BJTs or FETs, but BJTs were used here as is the focal point of this work. Critically, the current mirror presents its load with a very high output impedance, making it a very useful building block for designing current sources.

In its most basic form, a current mirror consists of a "diode-connected" input BJT with its base and collector connected by a short circuit, and an output BJT, such as the BJT pair of Q_3 and Q_5 in figure C.2b. The base and emitters of the pair are connected together, and their emitters are tied to a common voltage (−15 V in our case). The input BJT's collector functions as the input and accepts a reference current, I_{ref}, while the output BJT's collector becomes the output, and drives the load. The input BJT has the affect of fixing V_{eb} of the output BJT, which allows a constant output current to be maintained, neglecting any self-heating effects. In the ideal case, the current gain of the circuit is unity, i.e. $I_{load} = I_{ref}$ and the output impedance is very high, but of course there are a number of



(a) The Op Amp-BJT Constant Current Source.



(b) The BJT Cascode Current Mirror.

Fig. C.2 Building Block circuits found within the variable current source.

real-world imperfections that prevent the circuit from behaving ideally. Thankfully, there are many methods for improving the performance of a basic current mirror. One such method is the cascode current mirror, which was implemented here. The cascode current mirror adds an extra "stage" to the simple two-BJT current mirror, such as Q_2 and Q_4 in figure C.2b, which has the effect of correcting systemic current gain errors, and presenting an even higher output impedance to the load.

For optimal operation of a current mirror, the BJTs should be closely matched (i.e. similar β value) and thermally-coupled to ensure that they are all the same temperature. This is easily done within an IC where the BJTs are all constructed from the same substrate, which is typically how current mirrors are implemented. In this case, however, the performance was found to be adequate using discrete BJTs that were not matched, nor thermally coupled.

When combined, these two sub-circuits complete our variable current source, capable of precisely delivering a constant base current up to the required 50 µA with a relatively high input impedance.

DMM Measurement Considerations

To measure the base and collector currents for these measurements, the ammeter of a standard DMM was used. Many DMMs, including the ones used for this work, have an “auto range” feature, and when engaged, the DMM will automatically change its measurement range as the value being measured changes. While useful, it is worth considering how this feature works, and how it may affect the accuracy of the measurements.

Most ammeters function by placing a small resistor in-line with the two contacts and measuring the voltage across it. To limit the range of voltages that the DMM needs to be capable of reading, this resistor value changes for the various measurement ranges - as the current being measured increases, so too does the resistor. While capturing the common-emitter measurements, it was observed that the measured current values would change abruptly and significantly when the DMM switched from one range (and therefore resistor) to another. It is therefore recommended that the DMM's range be set manually such that it does not change.

If a single range does not encompass the full range of expected measurement values, it is advised that small resistors, e.g. 1Ω be placed in series with the DUT and the DMM instead be set to measure the voltage drop across it. This ensures that the series resistance remains constant, and the measurements remain as consistent as possible. Furthermore, the voltmeter in a DMM tends to be more accurate than the ammeter, so this technique is preferable from a precision point of view as well.

C.3 Designing a Pulsed-DC Voltage Source

Perhaps the most difficult part of collecting these series of GBJT measurements was mitigating the self-heating while measuring the gummel plots. This was handled eloquently using a pulse-DC voltage source, which limits the “on” time of the DUT, which prevented them from self-heating. In this section, the design of this circuit is outlined, including component choices, and a detailed explanation of each circuit block. Given the switching nature of the circuit, more stringent power supply filtering was required, which will also be discussed. Furthermore, the design of two instrumentation amplifiers is outlined, as they were required to facilitate the measurements.

C.3.1 Schematic Overview

The schematic of the pulsed-DC voltage source, as discussed in section 4.3.3, is shown in figure C.3, complete with component values and voltages. R_2 and R_4 are both 10 kΩ, linear-taper potentiometers.

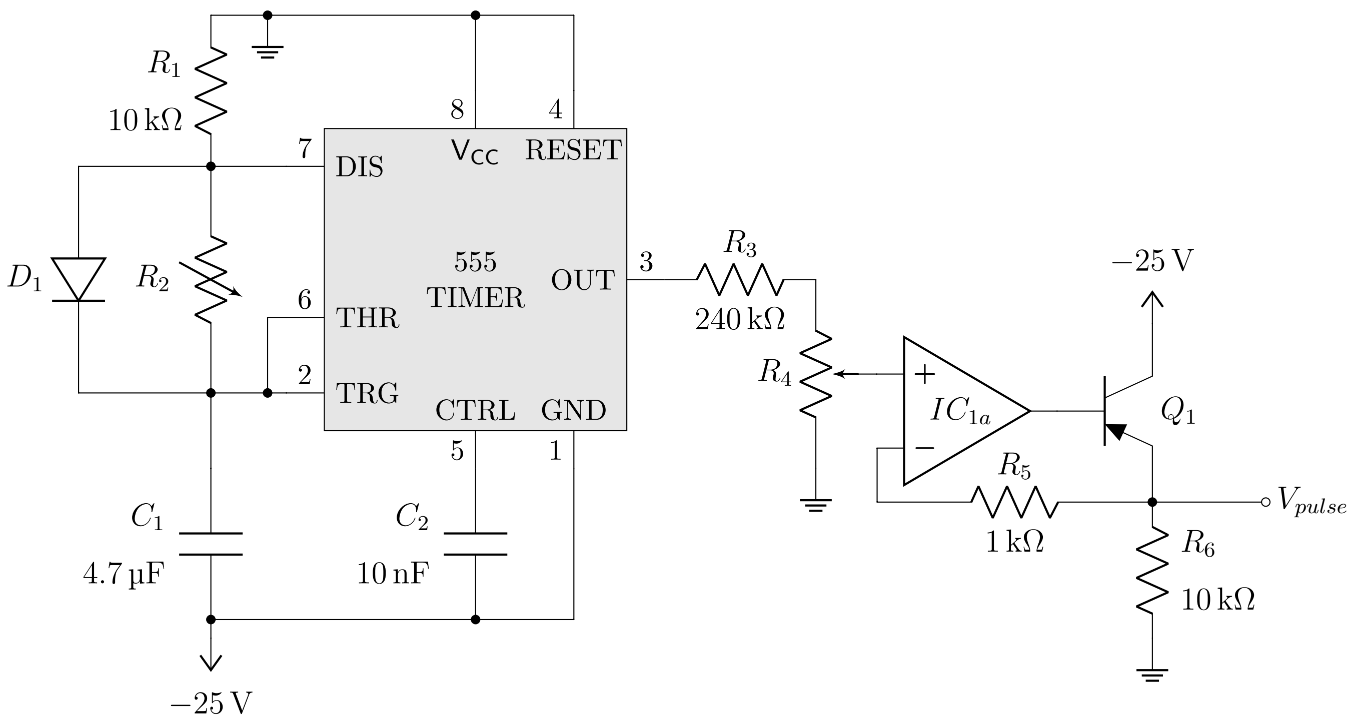


Fig. C.3 The pulsed-DC voltage source, shown with the component values used. R_2 and R_4 are both linear-taper 10 kΩ potentiometers.

The astable multi-vibrator was constructed using an LM555CN 555 timer. This design is very standard, found in the data sheet[1] of the IC. It creates a square wave at its output that swings between V_{CC} and GND. In our case, though, V_{CC} is connected to ground,

[1] LM555 datasheet

while the GND pin is connected to the $-25\,\mathrm{V}$ supply. Somewhat confusingly, this reverses what is considered the "on" and "off" portion of the waveform - during the "off" time, the circuit outputs $-25\,\mathrm{V}$, and during the "on" time it returns to ground. For continuity, the notation of the data sheet, where "on" refers to the output being at the V_{CC} pin, and "off" referring to the output being at the GND pin of the 555 timer, will be maintained.

If we exclude the diode D_1, the charge time of the traditional multi vibrator (and therefore the "on" and "off" times), can be calculated using the formulae found on the data sheet:

$$T_{ON} = 0.693(R_1 + R_2)C_1, \quad T_{OFF} = 0.693(R_2)C_1 \tag{C.1}$$

where the constant 0.693 comes from the data sheet. Since the capacitor charges through both resistors but discharges through just R_2, a duty cycle of less than 50% is not possible. Furthermore, it makes it difficult to vary the "on" or "off" time independently - changing either resistor will affect both the charge and discharge cycle. The added diode behaves as a short circuit during the charge cycle, essentially "bypassing" R_2. This allows the charge times to be instead calculated as:

$$T_{ON} = 0.693R_1C_1, \quad T_{OFF} = 0.693R_2C_1 \tag{C.2}$$

which allows T_{ON} and T_{OFF} to be varied independently, by adjusting R_1 or R_2, respectively. Furthermore, this allows a duty cycle of 50% for the case where $R_1 = R_2$, and duty cycles below 50% when $R_1 > R_2$. Therefore, by making R_2 adjustable, we can adjust the duty cycle between 0 and 50%. The choice of diode is trivial - any switching diode will do. In this case, a 1N4148 diode was used. With the values as specified in figure C.3, and assuming that R_2 is set to $1\,\mathrm{k}\Omega$, T_{ON}, and T_{OFF} can be calculated as:

$$T_{ON} = 0.693R_1C_1 = 0.693(10 \cdot 10^3)(4.7 \cdot 10^{-6}) = 32.57\,\mathrm{ms} \tag{C.3}$$

$$T_{OFF} = 0.693R_2C_1 = 0.693(1 \cdot 10^3)(4.7 \cdot 10^{-6}) = 3.257\,\mathrm{ms} \tag{C.4}$$

The waveform period and frequency are therefore:

$$T = T_{ON} + T_{OFF} = 35.827\,\mathrm{ms} \tag{C.5}$$

$$f = \frac{1}{T} = 27.90\,\mathrm{Hz} \tag{C.6}$$

This is a very low frequency - barely in the audible spectrum. A lower frequency value was favoured, though, as it avoided any switching time limitations of the DUT. The output of the multi vibrator is then voltage divided by R_3 and R_4, which allows the amplitude of the waveform to be adjusted from $0\,\mathrm{V} - 1\,\mathrm{V}$, which encompasses the desired range for the measurements.

The op amp-BJT voltage source can be analysed as an op amp buffer followed by an emitter-follower circuit. This may seem redundant, but the emitter-follower was necessary to insure that the voltage source could output the required current, as most op amps can only output $\approx 20\,\mathrm{mA}$. Furthermore, the op amp automatically biases the emitter-follower, and insures that the output voltage at the emitter is the same as the input voltage at the non-inverting input. This allows the circuit to be DC-coupled at its output, which was a necessity for this application. For Q_1, a D45H power BJT was used, as it is rated for very high currents. For the op amp, an LT1490 rail-to-rail op amp was used - to be discussed further in section C.3.2.

Power Supply Considerations

Because the pulsed-DC voltage source creates a square wave with very sharp transitions, and the current draw of the DUT is switching on and off quickly, a lot of noise is induced into the DC power supply. As such, it is paramount that the power supply rails be augmented with large coupling capacitors to smooth out those changes in current, and a smaller capacitor be placed across the rails of each IC. For this work, a $220\,\mathrm{\mu F}$ electrolytic capacitor was placed between each power supply input and ground, and a $100\,\mathrm{nF}$ ceramic capacitor was placed across the power rails of each IC, as physically close to the device as possible.

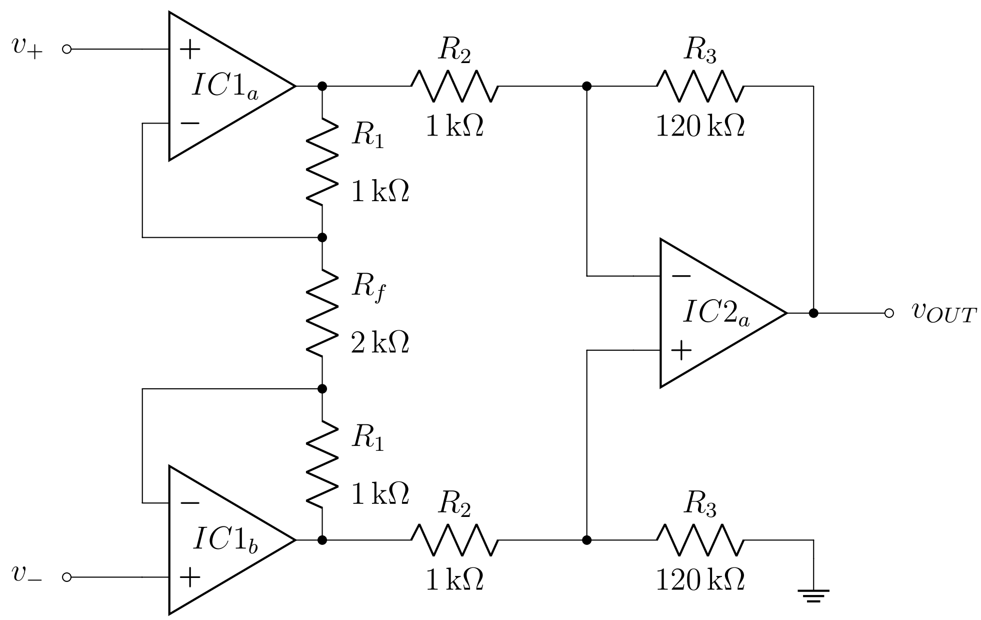


Fig. C.4 The classic instrumentation amplifier, used to measure a small, differential voltage. Resistor values shown as used in this work.

C.3.2 Instrumentation Amplifier Design

As mentioned in section 4.3.3, the use of an oscilloscope was necessary for these series of measurements as the the input voltage is now a periodic waveform. To facilitate the measurement of current, a $1\,\Omega$ resistor was placed in series with the base and the collector (or emitter) and the voltage drop across those resistors was measured, as shown in figure 4.4. The current is then calculated using ohm's law with the measured voltage and the measured resistance of the $1\,\Omega$ resistor. The challenge, however, is that the voltage drop across these resistors is immeasurably small for low currents. Further, the ground clip on an oscilloscope is tied to the ground prong on its power chord. Since neither node of the base resistor is connected to ground, measuring this voltage directly with the oscilloscope would disturb the circuit by shorting it to ground. As such, this voltage must be measured using a *differential* circuit. These small voltages, along with the necessity to measure a differential voltage, necessitated the use of an instrumentation amplifier.

An instrumentation amplifier is used to measure and amplify small voltages of interest, without disturbing the operation of the circuit. As such, they have a very high input impedance such that they do not load the circuit under test, and can measure differential voltages. The most classic instrumentation amplifier design, as shown in figure C.4, was used to measure the base current for the gummel plots. In essence, it consists of two non-inverting amplifiers, $IC1_a$ and $IC1_b$, coupled together by R_f, that then feed a differential amplifier, $IC2_a$. It measures and amplifies the difference between its two input voltages (connected across the base resistor), where its output voltage can be defined as:

$$v_{OUT} = A_{meas_B}(v_+ - v_-) \tag{C.7}$$

and the gain factor is defined as:

$$A_{meas_B} = \left(1 + \frac{2R_f}{R_1}\right)\left(\frac{R_3}{R_2}\right) \tag{C.8}$$

The output of this instrumentation amplifier was then measured by one of the oscilloscope probes. For the collector (and emitter) current, a *low-side*, inverting amplifier was used, since the series resistor is connected to ground and does not require a differential measurement. Further, due to the direction of the current flow, it was necessary that the amplifier be *inverting* such that the output voltage to be read was negative. The circuit is shown in figure C.5. The gain factor of this amplifier is simply the product of the two op amp gains, i.e.:

$$\begin{aligned} A_{meas_C} &= A_{IC1_a} A_{IC1_b} \\ A_{meas_C} &= \left(1 + \frac{R_5}{R_4}\right)\left(-\frac{R_7}{R_6}\right) \end{aligned} \tag{C.9}$$

The output of this amplifier was then measured using the second channel of the oscilloscope. Because these measurements cover such a large current range - from several µA up to 1A, tuning the gain factor of these amplifiers proposed a challenge. The gain must be high enough such that very small currents were measurable, but low enough that high currents did not exceed the voltage range of the amplifier. To provide maximum range for the measurement voltages, the power supply voltage was increased to $-25\,\mathrm{V}$ (as opposed to $-15\,\mathrm{V}$ used for the common-emitter measurements). From there, the gain factor of the instrumentation amplifiers was manually tuned such that the largest measured current would not produce a voltage that exceeded the voltage supply rail. The resistor values used for each amplifier, as shown in figure C.4 and C.5, can be used to calculate the gain factor

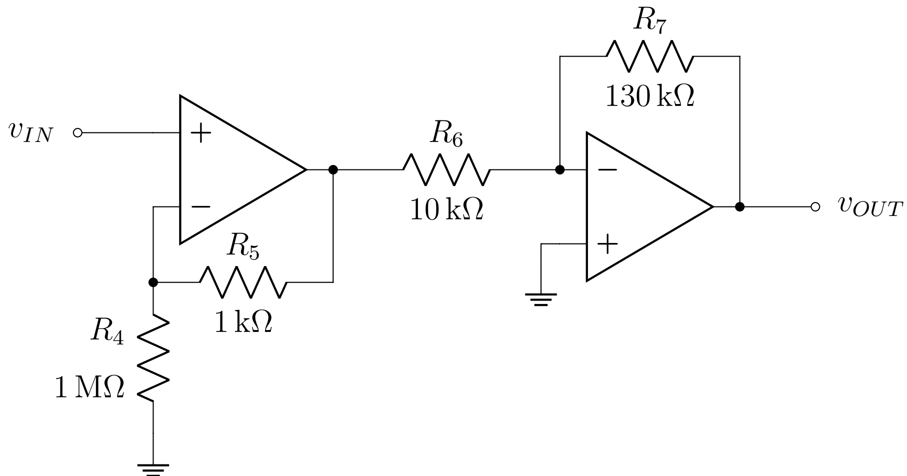


Fig. C.5 An inverting, single-ended instrumentation amplifier, used to measure a single-ended voltage.

of each amplifier:

$$A_{meas_B} = \left(1 + \frac{2R_f}{R_1}\right)\left(\frac{R_3}{R_2}\right) = 600 \tag{C.10}$$

$$A_{meas_C} = \left(1 + \frac{R_5}{R_4}\right)\left(-\frac{R_7}{R_6}\right) = 13.013 \tag{C.11}$$

where A_{meas_B} is the gain factor of the base current amplifier, and A_{meas_C} is the gain factor of the collector (and emitter) current amplifier. We note that the collector (and emitter) current amplifier has a much lower gain factor, as the current flowing through these terminals is much higher than the current out of the base. Like the op amp in the pulsed-DC voltage source, all of the op amps used for the instrumentation amplifiers were the LT1490[2]. This op amp was chosen because it is rated for rail-to-rail input/output, single supply operation up to 44 V, and, critically, has a very low input offset voltage and input bias current. Since the voltages being measured were so small (on the range of µV), the offset voltage of the op amp became non-trivial, and could skew the measurements. These op amps are more expensive than the TL062 used for the common-emitter measurements, but they are widely available.

[2] LT1490 data sheet

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