Design and Characterization of MEMS Micromirror Devices

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ABSTRACT

This thesis explores the design, implementation and characterization of MEMS micromirror devices for use in optical systems. Possible applications for these devices include areas such as adaptive optics, beam scanning, and optical switches. The devices were fabricated using a commercial MEMS foundry process, known as the Multi-User MEMS Processes (MUMPs) foundry service; the resulting prototypes were characterized using a phase-shifting Mirau interferometer, assembled specifically for this work. From these results, it was shown that the MUMPs process can be used to create satisfactory designs for rotational micromirrors with tilt angles in the range of 0-23 mrad and control voltages in the range of 0-30 V. In addition, the behaviour of these mirrors were shown to fall within 5% of the predicted values calculated by the theoretical models for the devices.

SOMMAIRE

L'objectif de cette thèse est d'étudier la conception, l'implémentation, ainsi que la caractérisation de micromiroirs de type MEMS. Leurs applications inclus plusieurs domaines, dont l'optique adaptive, le balayage optique, et les commutateurs optiques. Afin de fabriquer les miroirs, des designs ont été soumis au service MUMPs (Multi-User MEMS Processes) qui est un service de fabrication de type fonderie. Les miroirs fabriqués ont été caractérisés à l'aide d'un interféromètre Mirau qui a été construit spécifiquement pour cette thèse. Les résultats ont prouvé que le service MUMPs pourrait être employé pour fabriquer des miroirs avec des angles d'inclinaison de 0-23 mrad et des voltages de contrôle de 0-30 V. De plus, ces résultats ont confirmé les calculs prévus par le model théorique.

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1.0 INTRODUCTION

Recently, the design and fabrication of micro-electro-mechanical systems (MEMS) has received much attention. Some popular examples of commercial MEMS devices include pressure sensors for industrial applications, accelerometers for airbag deployment, and microfluidic chips for chemical assays. At the same time, much research has also been conducted on other MEMS devices such as optical micromirrors, which can be used in a number of applications, including adaptive optics, beam scanners, and optical switches. Of these three applications, however, optical switches are of especial interest to the MEMS community, due to their potential impact on the telecommunications industry.

Although several companies have already produced and marketed a number of MEMS micromirror devices, many of these devices have relied on the use of non-standard materials or on the use of non-standard processing techniques. As a result, the integration of these commercial mirror designs with standard CMOS circuitry has been challenging, and more work is needed in this area before these mirrors can be considered a commodity. On the other hand, the use of standard surface micromachining processes to create mirror devices out of polysilicon is one way of overcoming this limitation as it is a technique that lends itself well to the integration of microelectronics [1] [2]. As an added advantage, several commercial foundry services for MEMS devices are now available and these services can be used to prototype new designs at a reasonable cost [3] [4] [5]. Consequently, by using these prototyping services, new designs for MEMS devices can be created in short amounts of time and the designs modified to fit particular applications.

The goals of this thesis are three-fold: 1) To investigate the design and fabrication of customized mirror designs using standard foundry processes; 2) To characterize the experimental behaviour of the micromirrors fabricated; and 3) To identify the mirror designs that produced the best possible results in terms of both tilt angle and repeatability.

To accomplish this task, requests for manufacturing (RFMRs) were sent to the Canadian Microelectronics Corporation (CMC). CMC is a not-for-profit organization whose mandate is to provide its member universities with access to industrial microelectronic and microsystem technologies, such as CMOS foundry services and MEMS foundry services. Thus, through CMC, researchers in Canadian universities have the opportunity of creating their own MEMS designs and of having these designs fabricated using the Multi-User MEMS Processes (MUMPs) service developed at MCNC (formerly known as the Microelectronics Center of North Carolina); a process which is now administered by Cronos Integrated Microsystems, a spin-off company of MCNC. As a result of this opportunity, several MEMS designs were submitted for the March 2000 and the November 2000 fabrication deadlines. The devices chosen for implementation included designs with applications in both adaptive optics and beam scanning, as well as optical switching.

In June of 2000, the first set of MEMS prototypes were received from CMC. The devices were tested using a special interferometric setup developed specifically for this application, namely the testing of MEMS devices. Using this interferometer, the motion of any given device could be characterized quantitatively and its displacement plotted as a function of the input voltage or current. In addition, other characteristics such as the surface curvature and surface roughness of the mirror could also be determined.

From these results, it was shown that the MUMPs process can be used to create satisfactory designs for rotational micromirrors with tilt angles in the range of 0-23 mrad and control voltages in the range of 0-30 V. In addition, the behaviour of these mirrors were shown to fall within 5% of the predicted values calculated by the theoretical models for the devices.

The remainder of this thesis is divided into eight sections. Section 2.0 provides a short background on the history and applications of micro-electromechanical systems. Section 3.0 outlines some of the major activities and key players involved in the research of MEMS in Canada. Section 4.0 describes in greater detail the MUMPs process which was used for this work. Section 5.0 details the design process for the micromirrors studied in this thesis. Sections 6.0 and 7.0 describe the theoretical models and experimental setups used to characterize the behaviour of the devices. Section 8.0 presents the results obtained from this characterization procedure. Finally, Sections 9.0 and 10.0 summarize future directions and main conclusions from this work.

2.0 BACKGROUND

> *"I would like to describe a field, in which little has been done, but in which an enormous amount can be done in principle. (...) What I want to talk about is the problem of manipulating and controlling things on a small scale.*
>
> *(...) It is a staggeringly small world that is below. In the year 2000, when they look back at this age, they will wonder why it was not until the year 1960 that anybody began seriously to move in this direction."*
>
> *– Richard P. Feynman [6].*

2.1 A Brief History of MEMS

In 1959, Richard Feynman captured the imagination of many by asking one simple question: How can things be made smaller? For example, how can one write an entire encyclopedia on the head of a pin? How can one build a computer using wires that are only a hundred atoms in diameter? Better yet, how can one create a tiny mechanical surgeon, small enough to be swallowed by a patient? These were the types of problems posed by Feynman in his famous talk, "There's Plenty of Room at the Bottom" [6].

Although Feynman's area of expertise was in quantum physics and not in engineering nor the material sciences, Feynman was still an expert at thinking up new ideas and of creating new challenges for the scientific community. Indeed, many of the ideas put forth by Feynman in this early talk showed a great deal of foresight into the future of micro systems technology, both in the area of microelectronics and in the area of micromechanical systems [7].

By the end of the 1960's, the invention of the transistor had completely revolutionized the microelectronics industry, allowing for circuits that were much smaller than any of its predecessors. In addition, the creation of integrated circuits (ICs) allowed for a greater number of components to be squeezed in to the same amount of space. Large scale integration (LSI) soon became one of the hottest topics of the 1970's and continued to dominate throughout the 1980's with the invention of very large scale integration (VLSI) designs. Today, designers talk about ultra-large scale integration (ULSI) which has led to microelectronic circuits that are over a million times smaller and a million times faster than those that were available in Feynman's early years [8] [9].

However, aside from the advantages of speed and space, the reduced size of the silicon microchip also led to another important advantage: batch fabrication. Thousands of circuits could now be fabricated in a single batch, resulting in dramatic reductions in unit cost. By using batch fabrication, the cost of integrated circuits fell to near zero amounts, contributing greatly to the availability and affordability of consumer electronics today [10]. Fuelled by this demand, the microelectronics industry has continued to expand at a rapid rate, generating an extensive wealth of knowledge concerning the fabrication, operation and optimization of transistor devices. This in turn has led to vast improvements in process technology and in the CAD tools available for the design and synthesis of microelectronics.

By comparison, the history of micromachines has progressed at a much slower pace. In 1965, H.C. Nathanson and R.A. Wickstrom first reported the creation of a resonant gate transistor (RGT) using the same lithographic techniques used to create integrated circuits, with gold acting as the structural material and another metal acting as the sacrificial spacer material [11]. The advantage of the RGT was that it used electrostatic forces to vary the distance between the gate electrode and the substrate, thus allowing the quality factor, Q, of the circuit to be tuned dynamically. Still, despite the appeal of such an element, the RGT never gained much acceptance and was generally regarded as little more than a mechanical curiousity [12].

In the 1970's, a new technique for fabricating micromachines was developed. Instead of depositing additional layers of material using photolithography — a key technique for surface-micromachining processes, such as those described by Nathanson and Wickstrom — anisotropic etching was used to selectively remove material already present on the wafer [13]. Since this resulted in devices that were much taller than those produced by surface-micromachining alone, this new technique became essential for bulk-micromachining processes and enabled the creation of a number of other micromechanical devices. For example, thin silicon membranes were developed for use as pressure transducers in a variety of medical and industrial applications [14] [15] [16]. In addition, microscopic arrays of closely-packed holes were transformed into ink jet nozzles, a technology that is still in use today [17] [18]. Aside from these examples, bulk-micromachining techniques were also applied to other devices, such as field emitter arrays, electromechanical switches, and early versions of the integrated accelerometer [19]. Anisotropic etching also proved useful in creating precise V-grooves for the alignment of microscopic optical benches [20] [21].

Still, despite this wide range of applications, the field of micromechanics continued to struggle. In a world dominated by the use of silicon as an electrical material, few people were aware of its possibilities as a mechanical material. In 1982, K. E. Petersen wrote his classic paper, "Silicon as a Mechanical Material" [22] with the express purpose of addressing this gap. In addition to highlighting the many successes of the field to date, it also served as a primer for the electrical engineering community, summarizing many of the material properties and etching data required for the bulk micromachining of silicon.

At the same time in Germany, a new technique for micromachining other materials was developed. This technique was called LIGA, which is an acronym for the German words "lithographie", "galvanoformung" and "abformung" [23]. In essence, these three words refer to the three main steps in the LIGA process: lithography, electroplating, and molding. By using a synchrotron to produce powerful X-rays for the lithography process, thicker layers of resist could be patterned with greater accuracy; typical structures fabricated using LIGA range from 10 to 1000 μm in height, with lateral tolerances in the submicron range. This was a marked improvement over what anisotropic etching techniques could achieve, however the need for a synchrotron — generally a very expensive piece of equipment — has greatly restricted the use of LIGA in MEMS fabrication. Still, research in LIGA and other LIGA-like processes has continued to grow. In North America, one of the key research groups in this area has been the group formerly headed by H. Guckel at the University of Wisconsin-Madison (UW-Madison) [24].

Meanwhile, in 1983, researchers at the University of California, Berkeley (UC Berkeley) reported a new variant on an old technique. Using polysilicon as the structural material and silicon dioxide as the sacrificial material, R. T. Howe and R. S. Muller were able to fabricate singly-supported and doubly-supported beams — also known as cantilevers and bridges, respectively — using the planar surface micromachining techniques first described by H.C. Nathanson et. al. in 1965 [25]. These results were soon repeated by other researchers, most notably M. Mehregany, K. J. Gabriel and W. S. N. Trimmer at AT&T Bell Laboratories [26], who have all continued to work extensively in the field of micromechanics. By the end of the 1980's, the repertoire of micromachines had expanded to include other devices such as motors, gears, comb drives, inertial sensors, and even a pair of microtweezers.

In 1987, the first micromechanics workshop was held, entitled "Micro Robots and Teleoperators Workshop, An Investigation of Micromechanical Structures, Actuators and Sensors" [27], and in 1988 the name of this annual workshop was changed to read "MEMS Workshop". The acronym "MEMS" has since held and is now widely used throughout North America to denote the field of micro electro mechanical systems. In Europe, however, the acronym "MST" for micro systems technology is more commonly used and in Japan the term "micromachines" is preferred. The year 2001 marks the 14th edition of the International MEMS Workshop.

2.2 New Foundry Services for MEMS

The 1990's saw the establishment of two very important foundry services for surface micromachining in the United States. Building on the success of the accelerometer project at the Berkeley Sensors and Actuators Center (BSAC), researchers from Sandia National Laboratories, BSAC and Analog Devices, Inc. joined forces to create a new 3-axis MEMS accelerometer [29]. This joint collaboration led to the establishment of a new MEMS foundry service at Sandia National Laboratories in Albuquerque, New Mexico, and has since evolved in to a five-layer polysilicon surface micromachining process called "SUMMiT V", where SUMMiT is an acronym for Sandia Ultra-planar, Multi-level MEMS Technology [30]. Efforts to integrate this micromachining process directly with that for microelectronics has spurred the development of the "IMEMS", or integrated MEMS program. Both processes are now available through the Sandia Agile MEMS Prototyping, Layout tools, Education, and Services (SAMPLES) program [31].

At the same time, in 1993, the Advanced Research Projects Agency (ARPA) — now called the Defense Advanced Research Projects Agency (DARPA) — sponsored the development of a new low-cost MEMS process in North Carolina [32]. As a result of this sponsorship, MCNC (formerly the Microelectronic Corporation of North Carolina) was able to establish a multi-user MEMS processes service, better known by the acronym "MUMPs". Like the SUMMiT V process, the MUMPs service took advantage of the knowledge gained from the microelectronics industry to create a multi-layer surface micromachining process using polysilicon as the structural material. However, unlike the SUMMiT V process, the MUMPs service chose to use only three layers of polysilicon, as opposed to five. While this restriction greatly limits the complexity of the systems that can be achieved, this simplicity has also allowed for a higher turnaround rate and has kept production problems to a minimum. In the end, the MUMPs service has proven to be highly successful due to the accessibility of this prototyping service, particularly to research groups across North America. In 1999, the micromachining facility at MCNC was spun off to form a separate company called Cronos Integrated Microsystems and it is this company that continues to offer the MUMPs prototyping service to companies and other research organizations around the world [33].

3.0 MEMS ACTIVITY IN CANADA

3.1 Early pioneers in Canadian research

Although the idea of miniaturized microsystems first appeared forty years ago, it was not until the late 1980's that research in MEMS began to emerge in Canada [34]. Three of the researchers who helped pioneer this area of research are profiled below.

3.1.1 Dr. Meenakshinathan Parameswaran

When Dr. Meenakshinathan (Ash) Parameswaran first started his Ph.D. work in 1987, there was very little support available for MEMS-related research in Canada [35]. At the University of Alberta where he worked, facilities were limited to the usual collection of acids needed to etch printed circuits and clean silicon wafers [36]. However, to Parameswaran, they were all that was needed to devise a new way of micromachining silicon wafers using the limited resources available. Through the support of the Canadian Microelectronics Corporation (CMC), Parameswaran was able to send unusual circuit designs to Northern Telecom Canada (now called Nortel Networks) for fabrication. His idea was to use conventional CMOS fabrication processes to create a layered wafer that could then be post-processed using the acids he had on hand, creating a set of micromachines in the process. Working with the staff of the Alberta Microelectronics Corporation, a young spin-off company from the University of Alberta, Parameswaran was able to refine these ideas and to use them to create a set of microbridge structures. The results from so unconventional a process were remarkable. By 1990, Parameswaran had published several papers with his colleagues — G. McKinnon, Lj. Ristic, K. Chau, A. M. Robinson, and W. Allegretto, among others — outlining the use of this method to create other devices such as electrothermal actuators using commercial CMOS technology [37] [38]. Parameswaran's dream of creating working micromachines had been achieved.

Dr. Parameswaran is now a faculty member at Simon Fraser University (SFU), where he has continued to work on new MEMS technologies. In the early 1990's, Parameswaran enlisted the help of his new colleagues to create an "incandescent pixel", which could be used as a point source for thermal radiation [39]. This in turn led to the creation of a two-dimensional thermal image generator for use as a calibration aid in infrared applications, such as night vision systems and other navigational guidance systems. Ron Cheung, who was one of the key designers in this project, later took the technology with him to Optical E.T.C., Inc. in Huntsville, Alabama [40].

Recognizing the potential in the field of MEMS, SFU established the Institute for Micromachining and Microfabrication Research (IMMR) in 1992 [41]. Since then, the Institute has produced a number of interesting designs, including devices that can purify DNA and others that can replicate or "amplify" strands of DNA. In addition, thanks to funding from the B.C. Knowledge Development Fund and the Canadian Foundation for Innovation, students working at IMMR will soon have the option of fabricating their own prototypes using new equipment purchased by IMMR's microfabrication facilities, instead of relying solely on commercial foundry processes. Dr. Parameswaran is the current director of IMMR and continues to oversee a number of projects in the fields of photonics and biomedicine.

3.1.2 Dr. A.M. (Sandy) Robinson

Meanwhile, at the University of Alberta, Dr. A.M. (Sandy) Robinson has continued to work on the use of standard CMOS processes to fabricate MEMS devices. Since 1988, he has used these methods to manufacture a number of cantilever devices and has explored the use of these devices as sensors. Recent projects include the creation of magnetically actuated cantilevers and the development of a novel cantilever-in-cantilever design that can be used to monitor the deposition of thin films [42] [43].

Although much of the early work at the University of Alberta was done using the microfabrication facilities at the Alberta Microelectronics Corporation (AMC), in 1998 the AMC was privatized and its facilities placed off-limits to the university. However, through the generous support of organizations such as the Natural Sciences and Engineering Research Council (NSERC) and the Alberta Science Research Authority (ASRA), the University of Alberta was able to establish its own micro and nano fabrication facilities. Opened in March of 1999, the "MicroFab" has since been used by over 30 researchers from six departments within the university [44]. Some of the equipment available in this unique facility include a micro-embosser for fabricating micro-fluidic devices out of plastic, and equipment for deep silicon reactive ion etching (deep Si-RIE), a process which would yield LIGA-like structures with near vertical walls and high aspect ratios. Both pieces of equipment are currently the only ones of their kind available to universities in Canada.

Finally, in order to expand its current research capabilities, the MicroFab is planning to relocate its equipment to a new microfabrication facility, currently under construction. The move to the new building will more than double the amount of space currently available and will include new equipment for work in surface micromachining and other research in related material sciences. Work on the new facility is expected to be complete by September 2001.

3.1.3 Dr. D. Jed Harrison

At the same time, another professor from the University of Alberta has also been very active in the area of MEMS. Inspired by the work of his peers on tiny microsystems, chemistry professor Dr. D. Jed Harrison was one of the first to envision a miniaturized "lab-on-a-chip" which, despite its size, could still be used to perform the same types of reactions and analyses as a full-size laboratory [45]. To accomplish this goal, Harrison followed in the footsteps of his peers, relying on IC-fabrication technology to etch tiny networks of micropipes into substrates such as glass or silicon. From there, electric fields could be used to control the flow of fluids through the micropipes and non uniform electric fields could be used to manipulate individual particles contained within the fluids. The field of microfluidics was born [46].

Working at the University of Alberta, Harrison and his team of researchers soon expanded the capabilities of microfluidics to include ways of mixing and reacting reagents on-chip, as well as ways of using fluorescence and chemiluminescence to detect very small concentrations of a given molecule. Harrison's group was also the first to demonstrate a way of causing biological cells to rupture or "lyse" while on-chip. This, in turn, generated a number of new applications that could be explored; with these techniques, microfluidic chips could be used to perform single cell analyses and genetic analyses, as well as other biochemical measurements. Harrison's emphasis on using real biological samples to test microfluidic devices also helped to prove the ability of microfluidics to handle biochemical analyses in real life situations. Thanks to this work, by the end of the 1990's, the field of microfluidics had firmly established itself as an enabling technology for future generations of analytical instrumentation.

Today, Dr. Harrison is widely considered as a pioneer in the area of microfluidics. Under his leadership, a number of key microfluidic technologies were developed; in particular, his techniques for etching microchannels and other microstructures in to glass substrates was later transferred to the Alberta Microelectronics Corporation (now called Micralyne Inc.) which has continued to use this technology as the basis of their foundry service for microfluidic devices. Finally, in addition to his affiliation with Micralyne, Dr. Harrison also serves as a technical advisor to other lab-on-a-chip companies, such as Caliper Technologies Corporation, located in California.

3.2 Research Activities in Canada

Although the previous sections have concentrated mainly on the activities at the University of Alberta and at Simon Fraser University, a number of other Canadian universities have also been active in the field of MEMS [47]. Through the support of the Canadian Microelectronics Corporation (see Section 3.3), many of these universities have been able to fabricate both surface-micromachined and bulk-micromachined MEMS devices using either the MUMPs process from Cronos Microsystems Ltd, or the 1.5-μm CMOS technology from Mitel Corporation, respectively. In general, activities at these different universities can be divided according to the main applications for their area of research: biomedical, telecommunications, transportation, thermal imaging, and advances in material sciences and fabrication processes. The following is a sampling of some of the research activities currently in progress [34].

3.2.1 Biomedical Applications

By far, the most popular area of research is in the use of MEMS for biomedical applications. As mentioned previously, both the University of Alberta (U of A) and Simon

Fraser University (SFU) have been very active in this area, with researchers at U of A working on microfluidic devices and researchers at SFU developing items such as a DNA purification unit, a DNA amplification chamber, and even a "pressure-time" recorder to aid doctors in tracking the product of pressure and time, a necessary parameter in many medical applications. Several of the biomedical projects at SFU were done in collaboration with the Biotechnology Laboratory from the University of British Columbia.

Over at the University of Calgary, Dr. Karan Kaler has been working on dielectrophoresis as a way of manipulating cells. By applying a non-uniform electric field, neutral particles such as cells can be moved around due to the polarization effects that arise from this field. Since the rate of movement depends on certain dielectric properties of the cell, this technique can be used to separate different types of cells. This sorting capability is especially useful for work on DNA and cancer detection.

Meanwhile, researchers at the University of Windsor have been working on MEMS designs for the next generation of hearing aids. Under the leadership of Dr. Graham Jullien, the VLSI Research Group formed a partnership with IntelliSense Corporation in 1998; IntelliSense is a producer of software tools for computer-aided design. Since then, students have been able to use IntelliSense's "IntelliSuite" software for MEMS to design and simulate a number of devices related to aural communications. Examples of this include microphones, bandpass filters, microresonators, and speaker arrays.

Finally, researchers at the Ecole Polytechnique de Montreal have also been involved with a number of MEMS devices with biomedical applications. One of the more interesting applications, however, has been the design of a "pharmaceutical micro-dispenser", where micro-doses of medication can be released into the bloodstream at a controlled rate. This micro-dispenser is the subject of a patent by Drs. J. F. Currie, D. Ivanov, and A. Lecours [48].

3.2.2 Thermal Imaging

While Dr. Parameswaran's research groups at the U of A and SFU have produced MEMS devices for the production of thermal images, Dr. Richard Hornsey's group at the

University of Waterloo has produced devices for the detection of thermal images using tiny infrared sensors called microbolometers. In collaboration with CRESTech, an Ontario Centre of Excellence, Dr. Hornsey's group has worked on the design and characterization of hybrid CMOS-microbolometer sensors, formed by adding extra post-processing steps to standard CMOS designs. These sensors form the basis of the group's work on integrated detector systems.

In addition, work on microbolometers has also been performed by INO (l'Institut National d'Optique) located in Sainte-Foy, Quebec. Products developed include bolometric detector arrays, equipped with on-chip electronic circuitry. INO currently offers several foundry-type services for the fabrication of MEMS devices, however these services are intended more for the private sector.

3.2.3 Transportation

In the area of transportation, Dr. Ion Stiharu's group at the Concordia Centre for Advanced Vehicle Engineering (CONCAVE) at Concordia University has been working on incorporating MEMS devices into vehicles and traffic systems. Their goal is to develop an "intelligent transport system" (ITS) where sensors can tell cars what speed and distance to maintain, or warn heavy trucks when their loads have become unstable. Advances such as these are expected to influence the safety of future vehicles greatly, as well as ease the management of metropolitan traffic systems.

3.2.4 Telecommunications

Meanwhile, in the area of telecommunications, Carleton University has recently acquired the services of Dr. Niall Tait, formerly with the Alberta Microelectronics Corporation. Using the resources of Carleton University's Microelectronics Fabrication Laboratory, Dr. Tait has been working on new low-temperature MEMS processes for use in RF applications and optical interconnects. Examples of devices under development include low-voltage microswitches, suspended transmission lines, and micro-resonators.

In a similar vein, work by Dr. Andrew Kirk's group at McGill University has also concentrated on the creation of microswitches for use in optical interconnects and other telecommunications applications. In particular, the design and characterization of silicon micromirrors for optical switching has been investigated and forms the topic of this thesis.

3.2.5 Mechanical Test Structures

Over at DalTech-Dalhousie University (formed by the merger of Dalhousie University with the Technical University of Nova Scotia), students working under Dr. Ted Hubbard have participated in a number of MEMS projects, ranging from the design of ratcheting torsional micromotors to the design of compliant joint mechanisms. Dr. Hubbard has also been active in the creation of a java-based wet etch simulator and the creation of a test setup for the dynamic characterization of resonant micro-structures.

3.2.6 Material Sciences & Microfabrication

Last but not least, in addition to the applications listed above, a number of universities have also reported activity in the development of new materials and microfabrication techniques for MEMS devices.

At the University of Alberta, Professor Michael Brett has been specializing in thin film technology and has developed a new way of using "glancing angle deposition" (GLAD) to create thin porous films with micro-features on the nanometer scale. Research is currently underway to explore potential uses for these microstructures.

At Queen's University, the focus of Dr. Michael Sayer's group has been on the fabrication and characterization of thin films or coatings from ceramic materials such as piezoelectric composites. This work on piezoelectric materials has led to improvements in transducer technology and has allowed the development of an ultrasonic transducer array.

Finally, at Concordia University, Dr. Leslie Landsberger's area of specialty has been in the field of composite materials and structures. To this end, he has been actively involved in the study of anisotropic etching, with particular emphasis on its applications to sensor technology.

3.3 The Canadian Microelectronics Corporation

3.3.1 The Role of the Canadian Microelectronics Corporation (CMC)

Although many Canadian universities already have the ability to fabricate simple microelectronic devices, most universities do not have the resources to fund and maintain an industrial-class microfabrication facility. Consequently, researchers wishing to fabricate their own microelectronic designs have had to do so through a third party, such as the Canadian Microelectronics Corporation (CMC). Founded in 1984, CMC is a not-for-profit organization whose mandate is to provide its member universities with access to industrial microelectronic and microsystems technologies. In doing so, CMC hopes to foster world-class research in microelectronics and to ensure a steady source of well-trained graduates from universities across Canada [49] [50].

To achieve these goals, CMC currently provides its members with the following services:

- **Access to microfabrication technologies:** Through contracts with industry, CMC coordinates access to six different fabrication technologies, including the 0.18-μm CMOS technology from PMC-Sierra, the 1.5 μm CMOS technology from Mitel Corporation, and the MUMPs surface micromachining process from Cronos Integrated Microsystems.
- **Access to CAD tools:** To help researchers with their designs, CMC also negotiates special licensing agreements for CAD tools, such as the Cadence Design Framework II and the Synopsys synthesis tools.
- **Distribution of design kits:** Depending on the fabrication technology used, CMC may also provide a design kit with the CAD tools that it distributes. This design kit would include important items such as the layer mappings to be used during layout and the appropriate rule deck to be used with the design rule check (DRC) tool.
- **User training and support:** CMC also provides training and technical support for the CAD tools and fabrication technologies that it offers.

- **Equipment loans:** Finally, since an untested chip represents a waste of resources, CMC also provides its members with a pool of test equipment that can be borrowed as needed. Equipment available includes resources such as pulse generators, oscilloscopes, and network analyzers.

CMC is funded through contributions of money and resources from Canadian corporations, as well as a major grant from the Natural Sciences and Engineering Research Council (NSERC). Its current membership, as of May 2000, includes 42 universities and 25 industrial organizations.

3.3.2 The Can-MEMS Process

While CMC's involvement with MEMS dates back to Dr. Parameswaran and Dr. Robinson's earlier work with MEMS in 1987, it wasn't until 1994 that a full MEMS program was put into place in Canada. In 1994, CMC contracted researchers from the University of Alberta, Simon Fraser University, the Alberta Microelectronic Centre, and Ecole Polytechnique de Montreal to formally evaluate the prospect of using standard CMOS technologies to fabricate MEMS devices. However, since Northern Telecom no longer offered the 3-μm double-metal single-polysilicon process that had been popular with the MEMS community, researchers were asked to concentrate instead on the 1.5-μm double-metal double-polysilicon process offered by Mitel Corporation. This proved to be an interesting alternative.

In August of 1994, a one-day workshop was held at the University of Alberta to discuss the results of these activities and a prioritized list of post-processing steps was compiled. Based on these recommendations, 15 designs from various universities were received and processed using Mitel's 1.5-μm technology, along with selected post-processing steps. The initial results looked promising and summaries of these projects were later published in a report that appeared in September of 1995 [51].

Starting from 1996, CMC offered the new "Can-MEMS" process to all of its member universities. In addition to coordinating the initial designs to be submitted to the Mitel process, CMC also coordinated the post-processing steps by assigning these tasks to different research organizations with the appropriate equipment for the task. However, although this was feasible from a technical point of view, logistically the "Can-MEMS" process proved difficult to accomplish. Plagued by problems with service delivery, CMC was forced to withdraw the Can-MEMS process as an official service. Nevertheless, CMC continued to offer the use of Mitel's 1.5-μm CMOS process for MEMS devices, and work in this area has continued, with researchers such as Dr. A.M. Robinson (see Section 3.1.2) performing all their post-processing steps in-house.

3.3.3 Surface Micromachining through MUMPs

Although the Mitel process provided researchers with a way of doing bulk micromachining, researchers interested in surface-micromachining had to wait until 1999 for a similar process to be offered. In January of 1999, CMC added the MUMPs surface micromachining process to its list of supported technologies. In addition to complementing the Mitel service already being offered, the MUMPs process was also seen as a more accessible option for universities with little access to post-processing facilities since Cronos Integrated Microsystems also provides structural release services to its customers.

Thus, in CMC's first production run in March of 1999, six designs from four universities were fabricated. Designs ranged from thermal actuators and torsional motors to folding mirrors and capacitive pressure sensors. Since then, over 31 designs from six universities have been fabricated. Overall, the MUMPs process has proven to be very popular with researchers across Canada. Several universities, including McGill University, now rely on this service to prototype new designs for surface-micromachined MEMS devices.

4.0 MUMPS: MULTI-USER MEMS PROCESSES

As mentioned previously, the work presented in this thesis was fabricated using the Multi-User MEMS Processes or MUMPs foundry service, available from Cronos Integrated Microsystems, located in North Carolina, USA. Unlike the SUMMiT IV and SUMMiT V services available from Sandia National Laboratories, the MUMPs service is only a three-layer polysilicon process. Of these three layers, only the top two ("Poly1" and "Poly2") are releasable and can be used to form independent mechanical structures. The third layer, "Poly0", is fixed to the plane of the substrate and is usually used to create other elements such as wires and electrodes.

As a result of this reduction in complexity, only eight masks are needed for the MUMPs process, as opposed to 14 masks for SUMMiT V. These eight masks are used to pattern the three layers of polysilicon, along with four additional layers: the nitride layer, the metal layer, and the two layers of sacrificial oxide. A cross-sectional view of these seven layers, shown in the proper order, is illustrated in Figure 1. By specifying the desired layout for each of the eight masks appropriately, users can build a wide variety of devices using these seven layers.

TABLE 1: Summary of MUMPs Layers, Thicknesses, and Lithography Levels

Material Layer	Thickness (μm)	Lithography Level Name
Substrate	100 mm	—
Nitride	0.6	—
Poly0	0.5	POLY0 (HOLE0)
1st Oxide	2.0	DIMPLE ANCHOR1
Poly1	2.0	POLY1 (HOLE1)
2nd Oxide	0.75	POLY1_POLY2_VIA ANCHOR2
Poly2	1.5	POLY2 (HOLE2)
Metal	0.5	METAL (HOLEM)

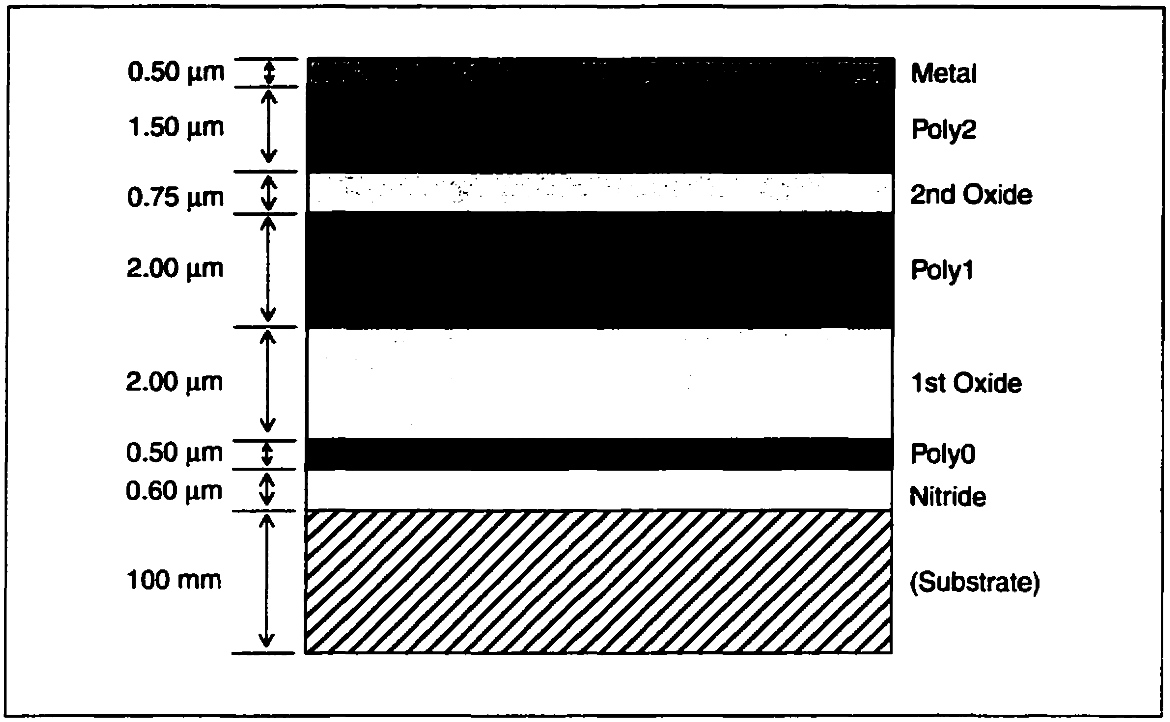


Figure 1. Physical Layers for the MUMPs Process.

To provide the reader with a better understanding of the MUMPs process, the fabrication steps for the MUMPs process are outlined below. For clarity, the name of the lithographic mask level is written using uppercase letters (e.g. POLY1, POLY2), whereas the name of the material layer itself is written using mixed capitals (e.g. Poly1, Poly2). To further aid the reader, Table 1 summarizes the names of each material layer and its corresponding mask levels. Finally, for additional details on any one step, the interested reader is referred to [52].

4.1 Process Description

The process begins with a silicon substrate:

- **Silicon substrate:** The surface of an n-type silicon wafer is heavily doped with phosphorus in order to reduce the effect of charge feedthrough. This is particularly important for the proper operation of electrostatic devices.

- **Nitride:** Next, a thin layer of silicon nitride is deposited on to the silicon substrate using LPCVD (low pressure chemical vapor deposition). The thickness of this layer is 600 nm. The nitride acts as an insulator and electrically isolates the substrate from the polysilicon structures to be built on top of this layer.
- **Poly0:** Next, a thin layer of polysilicon (Poly0) is deposited. The thickness of this layer is 500 nm. Poly0 is then patterned using photolithography, as follows:
  - First, Poly0 is coated with a layer of photoresist.
  - Next, the POLY0 and HOLE0 masks are combined to form a single lithographic mask for Poly0; the POLY0 mask is used to specify areas where the Poly0 layer is to be preserved, whereas the HOLE0 mask is used to specify areas (or "holes") where Poly0 is to be removed.
  - Using this combined mask, the photoresist is exposed to UV light and then developed. The photoresist that is left behind is used as an etch mask for the Poly0 layer.
  - Finally, the pattern in the etch mask is transferred into the Poly0 layer using Reactive Ion Etching (RIE); in this process, areas that are not protected by the photoresist layer are etched away, whereas areas that are protected by the photoresist are preserved. The photoresist is then stripped using a solvent, leaving behind only the patterned Poly0 layer.
- **1st Oxide:** Following this step, an oxide layer made of phosphosilicate glass (PSG) is deposited. The thickness of this layer is 2.0 μm. This layer forms the first sacrificial layer in the process and is used to create vertical gaps between the Poly0 and Poly1 layers.

  Note that unlike the SUMMiT V process, this oxide layer is not planarized before the next layer, Poly1, is deposited. This small detail often leads to the problem of "print-through", where the topography of a bottom layer adversely affects the topography of a higher layer, effectively allowing its features to print-through to the higher level. Consequently, this effect must be taken into account when designing MEMS devices for the MUMPs process.

However, before the Poly1 layer is deposited, the oxide layer must first be patterned using the DIMPLE and ANCHOR1 masks, as described below:

- **DIMPLE:** The DIMPLE mask is used to create small depressions in the 1st Oxide layer. These depressions have a nominal depth of 750 nm and are used to create "dimples" on the surface of Poly1. The main purpose of dimples is to help reduce problems with stiction and adhesion in the MEMS devices once they are released.
- **ANCHOR1:** The ANCHOR1 mask is used to mark the areas where the oxide layer is to be removed completely. This allows the user to create vertical supports or "anchors" perpendicular to the plane of the wafer that connect elements on the Poly1 layer to the surface of the substrate. Note that these anchors can either be connected to the substrate itself, which is electrically insulated, or to Poly0, which can be used to form an electrical connection to the anchored support.

- **Poly1:** Once the DIMPLE and ANCHOR1 masks have been used, a new layer of polysilicon (Poly1) is deposited on top of the oxide layer. The thickness of this layer is 2.0 μm. Poly1 is patterned using a slightly different lithographic process:
  - First, a very thin layer of PSG is deposited on top of Poly1; the thickness of this layer is 200 nm.
  - Next, the wafer is annealed. This is done for two reasons: one, so that the Poly1 layer may be doped with phosphorus from both its top and bottom surfaces; and two, so that the internal residual stresses of the Poly1 layer may be reduced by the annealing process.
  - Next, using the POLY1 and HOLE1 masks, the top layer of PSG is patterned photolithographically to form a "hard" etch mask, which is more resistant to the etching process than the photoresist mask alone. Consequently, by using both layers — that is, the photoresist and the PSG layer — as an etch mask, the proper transfer of the etch pattern into Poly1 is ensured.
  - Finally, the Poly1 layer is etched using RIE. The extra photoresist is stripped and the hard mask removed, leaving behind the patterned Poly1 layer.

- **2nd Oxide:** Next, a second layer of PSG (2nd Oxide) is deposited. The thickness of this layer is 0.75 μm. To reduce the residual stresses in the thin film, the oxide layer is annealed. Note that this layer, again, serves as a sacrificial layer and provides the user with a way of creating vertical gaps between the Poly1 and Poly2 layers. However, before the Poly2 layer is deposited, the 2nd Oxide is patterned using two new masks: POLY1_POLY2_VIA and ANCHOR2. These masks allow the user to create links between the Poly2 layer and the layers below it, for example the Poly1 layer or the substrate. The use of these masks is detailed as follows:
  - POLY1_POLY2_VIA: The POLY1_POLY2_VIA mask is used to mark the areas where the 2nd Oxide layer is to be removed completely, uncovering the Poly1 layer below. This allows for the creation of vertical links or "vias" connecting elements on the Poly2 layer with those on the Poly1 layer. Note that these elements will then be linked both mechanically and electrically.

    Another use for the POLY1_POLY2_VIA mask is to specify areas where a stacked "Poly1/Poly2" layer is desired. By removing the 2nd Oxide layer from large areas of Poly1, the Poly2 layer can then be deposited directly on top of the Poly1 layer. This "double" layer of polysilicon is then indistinguishable from a single layer of polysilicon 3.5 μm thick and can be patterned in the same way as the Poly2 layer.
  - ANCHOR2: As with the ANCHOR1 mask, the ANCHOR2 mask is also used to mark areas where the oxide layer is to be removed, so that vertical anchors to the substrate can be created. Note that for this connection to take hold, the areas indicated by ANCHOR2 must not overlap any non-oxide layers, such as Poly1, since both the 1st Oxide layer and the 2nd Oxide layer need to be removed from the surface of the substrate. Finally, as before, the anchors can either be connected to the substrate itself, which is electrically insulated, or to Poly0, which can be used to form an electrical connection to the anchor.

    NOTE: Although in theory the POLY1_POLY2_VIA and ANCHOR1 masks could be combined to achieve the same purpose, in general the use of the ANCHOR2 mask is preferred. The main advantage of this practice is that it eliminates the problem of alignment between the two masks and it also prevents the possibility of accidentally overetching the nitride layer on the substrate. Overetching of the nitride layer can cause structures to be shorted to the substrate, a scenario which is not usually desirable.

- **Poly2:** Once the 2nd Oxide is patterned, the third layer of polysilicon, Poly2, is deposited on the surface. The thickness of this layer is 1.5 μm and it is patterned using the same technique as for Poly1. This time, however, POLY2 and HOLE2 are combined to form the mask for the photolithographic step.
- **Metal:** Finally, the last layer to be deposited is the metal layer, which is often used for bond pads, low-resistance wiring, and as a highly reflective surface for optical components such as micromirrors. In order to improve the adhesion of the metal, the top surface is first coated with a very thin layer of chromium and a 0.5 μm layer of gold is then evaporated on to the surface of the wafer. The gold is patterned using the METAL and HOLEM masks; the patterning is done using lift-off.

At this point, the fabrication of the micro-structures is complete. The wafers are now ready for post-processing.

4.2 Post-Processing Steps

The three post-processing steps for the MUMPs service are dicing, sacrificial release, and critical drying. While the first step is always done at the foundry, the last two steps may either be done by the user at local facilities or by the foundry before the devices are shipped. The details for each step are described below:

- **Dicing:** After the completion of the fabrication process, the wafers are diced and the chips sorted. Since the chips still contain the unreleased micro-structures, the chips need to go through a structural release process before the devices can be tested.
- **HF Release:** The structures are released by immersing the chips in a bath of hydrofluoric acid (49% HF) for 2.0 to 2.5 minutes, with gentle agitation. This removes the sacrificial layers of oxide present on the devices. The chips are then rinsed by putting

them in a bath of deionized water for 5-10 minutes, followed by a bath of alcohol for another five minutes (see note below). The chips are then dried by baking them in an oven for at least 10-15 minutes.

NOTE: To reduce problems with stiction, the extra bath of alcohol is used to displace any water trapped in the structures. Due to the lower surface tension of alcohol, the surfaces in the structures will then be less likely to pull toward each other as the liquid evaporates.

- **Supercritical CO_2 Drying:** In order to further reduce the effect of stiction during the drying process, critical point drying in CO_2 can be used. Although this step is completely optional, it is usually recommended for chips containing intricate structures, as these structures would tend to collapse otherwise.

4.3 Packaging Options through CMC

All chips received from the MUMPs service through the Canadian Microelectronics Corporation (CMC) include both HF release and supercritical CO_2 drying. The final chips with the released micro-structures are delivered to participants either as loose dies in a "Gel-Pak" package, or mounted on to glass substrates, as desired. In addition, if the bond pads for the chip are arranged in a standard frame pattern, then participants can ask CMC to perform the wire-bonding and packaging required for their chips as well. However, since the facilities at McGill University include a manual wirebonding machine, all packaging for the MEMS chips presented in this thesis was done in-house.

The total delivery time for the chip, from date of submission to date of arrival, is typically 14-16 weeks.

5.0 DESIGN & IMPLEMENTATION

The goal of this thesis was to use the MUMPs process to prototype a number of designs for silicon micromirrors. However, although a consolidated element library (CaMEL, [53]) exists for many common elements such as bondpads, hinges, motors and comb drives, no standard layouts were available for silicon micromirrors. Thus, for the work in question, it was necessary to create all the corresponding mask layouts from scratch using standard CAD tools, in this case the Virtuoso layout editor, produced by Cadence Design Systems, San Jose, California.

In this section, the designs implemented using the MUMPs process are described in detail. Section 5.1 provides a review of some of the micromirror designs currently available in literature, which provided the inspiration for many of these final designs. Section 5.2 describes in greater detail the designs chosen for implementation on the first MEMS chip, "MEMS Test Chip" (MTC), whereas Section 5.3 outlines some of the changes included on the second MEMS chip, "McGill MEMS 2" (MM2). Finally, Section 5.4 summarizes the key aspects of each design and presents this information in the form of a table. Device modeling and details of the test results will be presented in Sections 6.0, 7.0 and 8.0.

5.1 Literature Review

Silicon micromirrors can be divided into two categories, depending on the type of motion of the mirror. Mirrors that can move up and down in the vertical direction are called "piston" mirrors, whereas mirrors that can rotate along an axis are called "torsion" or "tilt" mirrors. Piston mirrors are often used to modulate the phase of an incoming beam of light, whereas torsion mirrors are usually used to redirect beams of light. Both types of mirrors have been featured extensively in literature and have found a variety of applications in industry. Some of the more common applications for these designs are given below.

5.1.1 Beam Scanning

One of the first designs for a silicon torsional micromirror was developed by K. E. Petersen in 1980, using the same bulk-micromachining techniques used to form thin silicon membranes for sensor applications [54]. By selectively etching a layer of single-crystal silicon, the top surface of the mirror and its supporting axis could be created. This surface was then clamped to a glass substrate containing a shallow depression in which electrodes had been deposited, side by side. By applying a voltage to the control electrodes in sequence, the mirror could be made to oscillate at a given frequency; the result being a torsional mirror device capable of scanning beams of light at a resonant frequency of 15 kHz or more. Some of the advantages of this design over those made of glass or quartz are its relative ease of fabrication, the low amount of distortion experienced by the mirror surface, and the high fatigue strength inherent to single-crystal silicon. As a result, silicon torsional micromirrors have long been considered a plausible alternative to more conventional means of beam scanning, such as the use of electromagnetic and piezoelectric beam scanners.

Other approaches to silicon beam scanners have also been explored by other research groups, such as the MEMS groups at the University of California at Los Angeles (UCLA). Under the supervision of M. C. Wu, researchers at UCLA have used surface-micromachining processes to create a variety of micromirror devices using polysilicon. Examples of this work include vertical torsion mirrors that can be rotated out of the plane of the substrate [55], as well as a two-dimensional optical scanner that can be lifted several tens of microns above the substrate using a special micro-elevator self-assembly (MESA) system [56]. The latter design has also been implemented using single-crystal silicon, with good results [57].

5.1.2 Deformable Mirrors

Deformable mirrors are used in adaptive optics to modulate the spatial phase of an optical wavefront. For example, in an optical telescope, atmospheric turbulence may introduce unwanted aberrations in to the optical system. However, if one of the mirrors in the system is replaced with a deformable mirror, then the aberrations can be corrected for by deforming the surface of the mirror appropriately.

Deformable mirrors can be classified according to the type of reflective surface used. Mirrors with a continuous top surface are called "membrane" mirrors, whereas mirrors with a top surface divided into discrete sections are called "segmented" mirrors. Both types of mirrors can be fabricated using standard surface-micromachining processes. Some of the best examples of continuous membrane mirrors have been produced by R. Krishnamoorthy-Mali, T.G. Bifano, et. al. at Boston University [58] [59], using a customized MUMPs process, adjusted specifically for this application. In this mirror design, the thickness of the sacrificial layer was increased to produce a much larger gap between the control electrode and the top surface of the actuator membrane (see Figure 2). This allowed a much larger range of analog positions for the mirror before reaching the "pull-in" condition, where the electrostatic force overcomes the mechanical restoring force and the upper membrane is pulled in to its maximum position of deflection.

In addition, the top surface of the mirror was optimized using a unique layout strategy, designed to minimize the problem of print-through on the final device: instead of creating electrodes by specifying isolated sections of Poly0 that should be retained during the lithographic process, the electrodes were created by specifying thin lines in the Poly0 layer that should be removed during the lithographic process. This has the effect of delineating the edges of the electrodes by etching thin cuts in the Poly0 layer. The difference between the two approaches is illustrated in Figure 2. This layout strategy has been shown to increase the planarity of the upper surface considerably [60].

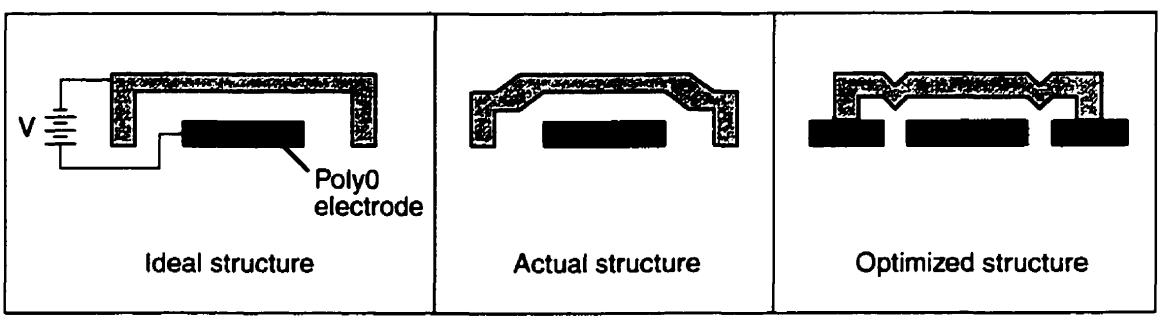


Figure 2. Cross-section of typical electrostatic actuator, showing print-through effect

On the other hand, much work on segmented mirrors has been done by M.A. Michalicek, D.E. Sene, W.D. Cowan, V.M. Bright, et. al. at the Air Force Institute of Technology [61] [62]. Their designs include both electrostatic and thermal actuation schemes for piston-like motion in the vertical direction. Since the motion of each mirror can be controlled independently of the motion of its neighbours, segmented mirror arrays have the advantage of a much simpler control algorithm than that for a continuous membrane device. However, due to the number of mirror devices needed to create the surface of the deformable mirror, fill-factor becomes an important issue for this type of application. Although the fill-factor can be increased by increasing the size of the individual mirrors, doing so would also increase the curvature experienced by each mirror, due to the residual stresses in the reflective metal layers. As this is not usually a desirable situation, other solutions to this problem have been found, including the use of a refractive lenslet array to focus the beams of light onto smaller portions of the segmented mirror array [63]. Recent developments in this area have also explored the use of solder bonds to align the lenslet array with the segmented micromirror array [64] and the use of flip-chip bonding [65].

5.1.3 Optical Switches

Another interesting application for MEMS micromirrors is in the area of optical switching. Some of the earliest work in this area was carried out by H. Toshiyoshi and H. Fujita at the University of Tokyo [66] [67]. Using a combination of surface-micromaching and bulk-micromachining techniques, Toshiyoshi and Fujita fabricated an array of torsional mirror devices that could be placed above a set of input and output fibers and used as a set of digital switches, as illustrated in Figure 3a. By rotating the appropriate mirror into the path of the input fiber, the incoming beam of light could then be deflected to the corresponding output fiber, forming a two-dimensional N x N switch.

This type of switch architecture has also been explored by other researchers, most notably J. E. Ford, V. A. Aksyuk, D. J. Bishop, and J. A. Walker at Bell Laboratories Lucent Technologies [68]; and L. Y. Lin, E. L. Goldstein, and R. W. Tkach at AT&T Labs-Research [69]. In both cases, the micromirror devices used were fabricated using the MUMPs foundry service, however in the latter work, mirrors are lifted out of the plane of

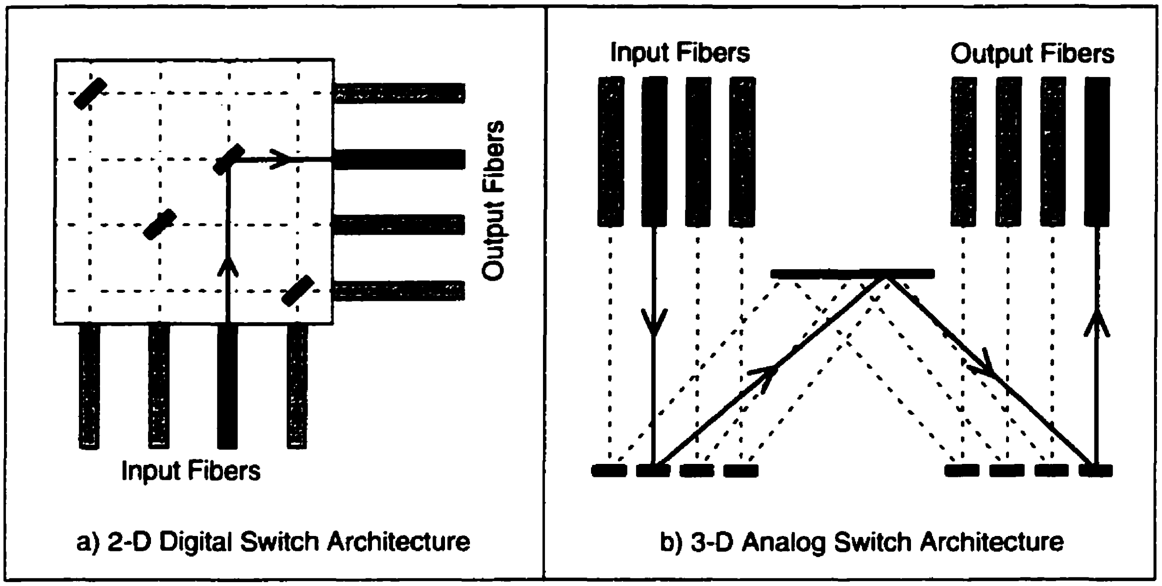


Figure 3. Common switch architectures for optical switching applications

the substrate through the use of scratch drive actuators. The final rotation angle of the mirror is then controlled through the precise positioning of these actuators; the measured switching time for this scheme was 560 μs. By comparison, the work by Ford et. al. utilized a more conventional, more planar approach to the mirror devices, using electrostatic forces to rotate the top surface of the mirror by $\pm 5^{\circ}$. The switching time for this scheme was clocked at 20 μs.

Although two-dimensional switching schemes are suitable for small sets of inputs and outputs, such as an 8 x 8 switch for use in a local area network (LAN), a different architecture is needed to handle larger numbers of inputs and outputs, such as those used in telecommunications applications [70]. One alternative to this scheme is to use two arrays of analog mirrors to create a three-dimensional N x N switch architecture, as shown in Figure 3b. By using analog mirrors instead of digital mirrors, the number of output positions can be adjusted dynamically, as needed. This in turn has a profound effect on the scalability of this architecture; the number of micromirrors needed for this architecture is 2N, as compared to N^2 for the two-dimensional switch.

This scheme is currently under development by a number of companies, including Agere Systems, a spin-off of Lucent Technologies; and Xros, a subsidiary of Nortel Networks.

5.1.4 Digital Projection Displays

Finally, perhaps one of the most successful examples of a commercial MEMS micromirror device has been the creation of the digital micromirror device (DMD) by Texas Instruments in Dallas, Texas, for use in digital projection displays [71]. As its name suggests, the DMD is an n-stable device, where n is the number of stable positions available for the top surface of the mirror. Typically, n is given a value of 2 or 3, depending on the intended application of the mirror. This bi- or tri-stability is created by careful choice of the mirror dimensions, as well as the biasing voltage used for the top surface of the mirror. By modifying these parameters, inflection points can be added or removed from the potential energy curve of the mirror, effectively changing the number of stable equilibrium points available for the mirror [72].

In terms of fabrication, the DMD is actually a three-layer device, with the micromechanics machined directly on top of the CMOS control circuitry. The top layer consists of the upper mirror surface, which is connected to the middle layer of the device by means of a central support post. This support post is connected to a yoke formed by the middle layer of the device, which rotates along a "hidden" torsion hinge; the hinge is so-named because it is located beneath the top surface of the mirror, hidden from view. Finally, the bottom layer of the device consists of the contacts for the address electrodes and for the biasing voltages needed for the top mirror surface. In addition, this layer also acts as an interface to the underlying CMOS technology.

This technology was used in the Digital Light Processing (DLP) Cinema Project which was used to screen movies at selected movie theatres around the world [73].

5.2 Designs Implemented on the McGill Test Chip (MTC)

The first MEMS chip for the Photonic Systems Group was submitted for fabrication on March 15, 2000. As its name suggests, the purpose of the "McGill Test Chip" (MTC) was to test a variety of different MEMS devices, including micromotors, thermal actuators, optical gratings, and micromirrors. To this end, the chip was subdivided into four quadrants, with each quadrant specializing in a different type of device: Quadrant 1 concentrated on micromirrors, which forms the focus of this thesis; Quadrant 2 on micromotors [74]; Quadrant 3 on optical gratings and optical systems [75]; and Quadrant 4 on thermal actuators and linear positioning systems [76]. Although the four quadrants were submitted to CMC as a single design, each quadrant was treated as a separate chip by the foundry and diced accordingly. As mentioned previously, all release steps for the dies — including supercritical $C0_2$ drying — were done at the foundry, before being shipped to CMC for final packaging and distribution. The final chips were received by the Photonic Systems Group from CMC on June 27, 2000.

The devices in Quadrant 1 can be divided into five families of designs: deformable membrane mirrors (DM), thermally-actuated mirrors (Th), electrostatically-actuated mirrors (E), and two types of electrostatic torsion mirrors (T) and (G). The details for each family of designs is given below.

5.2.1 Family I: Deformable Membrane Mirrors (DM)

This design is based on the deformable membrane mirrors developed at Boston University [58] [59]. In this design, the top surface of the mirror is positioned on top of an array of posts, where each post is connected to a separate electrostatic actuator. Thus, by applying voltages to certain actuators, the surface of the mirror can be manipulated into the shape desired. A general schematic of this design is shown in Figure 4.

Each electrostatic actuator is composed of two parts: an electrode which is fixed to the surface of the wafer, and a membrane which is suspended above the electrode by two vertical anchors. These two surfaces form the lower and upper plates of a parallel plate capacitor. When a potential difference is applied to the two plates, an electrostatic force is

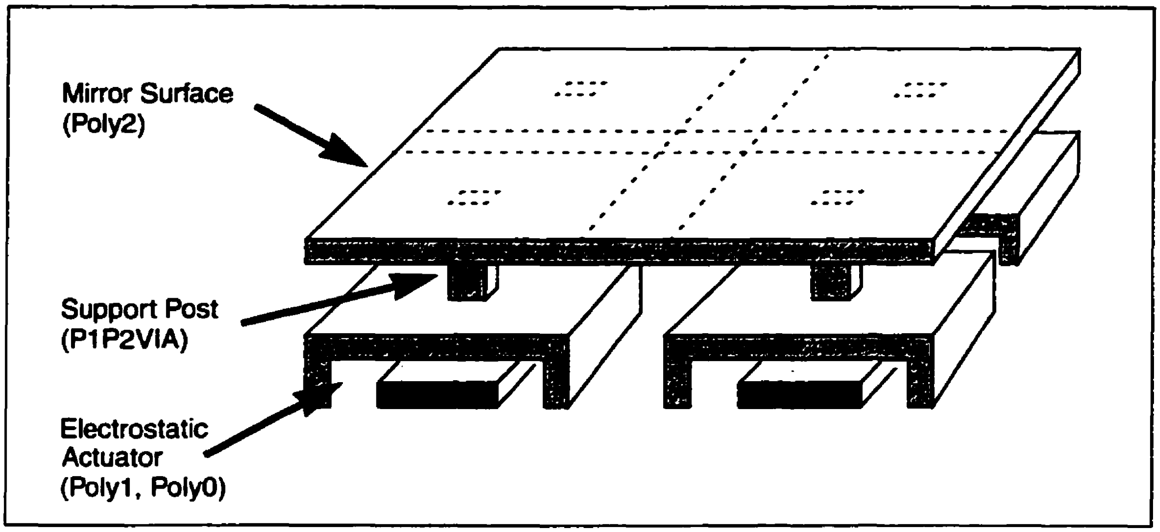


Figure 4. Schematic for deformable membrane mirror

generated. This draws the upper membrane (Poly1) down toward the lower electrode (Poly0), which in turn pulls down a post connected to the top surface of the mirror. The top surface of the mirror is made of Poly2.

While this design has been implemented successfully using customized MUMPs processes, the goal of this thesis was to implement designs using standard MUMPs processes. Thus, certain sacrifices had to be made to the original design. For example, the size of the gaps in the Poly0 layer had to be increased to 2.0 μm, since the minimum feature size allowed in standard MUMPs processes is 2.0 μm and not 1.5 μm. Etch holes also had to be added to the surface of the membranes so that the devices could be released properly; this is because the release of devices using back-etching is not a standard post-processing option for MUMPs. Finally, the use of standard MUMPs also implied that the oxide layer for the actuator gap could not be as large as 5.0 μm; instead, this gap could only be 2.0 μm thick. The major effect of these changes is expected to be a decrease in the surface quality of the mirror and a shorter range of motion for the underlying actuators; these three differences are summarized in Table 2.

TABLE 2: Summary of Changes Made to the Deformable Mirror (DM) Design

Property	Original Design	Modified Design	Expected Effect of Design Change
Minimum Feature Size	1.5 μm	2.0 μm	Less planar top surface. More problems with print-through.
Position of Etch Holes	Back surface	Front surface	Greater diffraction from mirror surface.
Thickness of Oxide1	5.0 μm	2.0 μm	Shorter working distance for actuators.

Finally, to improve the reflective properties of the mirror, a layer of metal was added to the surface of Poly2. For comparison, both mirrors with and without this top layer of metal were sent for fabrication. Figure 5 shows the corresponding mask layout for this design. A 3x3 array of microactuators was used. Each microactuator is approximately 210 μm by 230 μm and the total dimensions for the mirror are 675 μm by 675 μm.

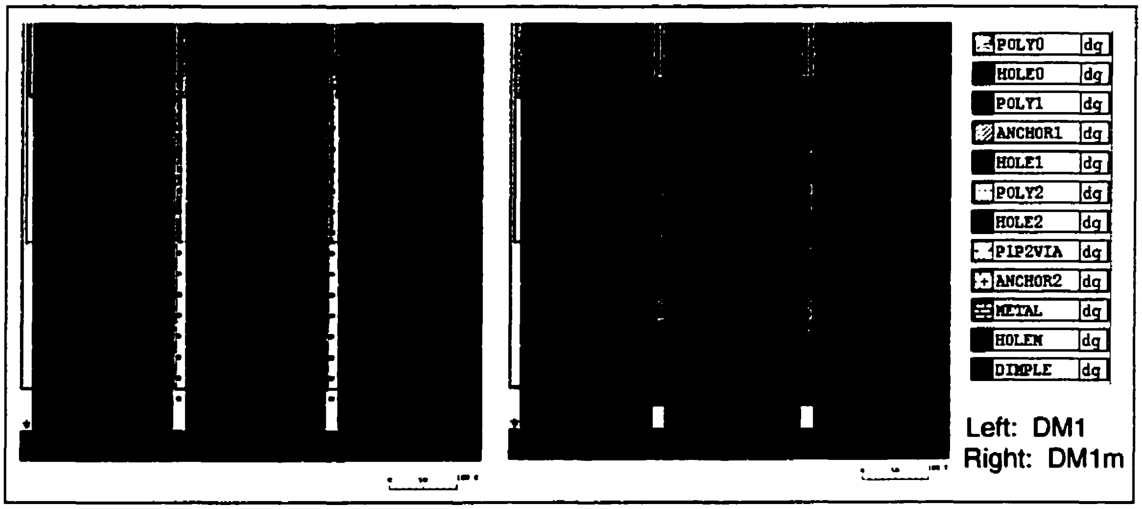


Figure 5. Mask layout for deformable membrane mirrors (Mirror DM)

5.2.2 Family II: Thermally Actuated Segmented Mirrors (Th)

A. Piston Mirrors

Another approach to adaptive optics is to use a segmented mirror array, such as the thermally actuated piston micromirror array developed by W.D. Cowan and V.M Bright at the Air Force Institute of Technology [77]. In this design, a circular mirror is suspended over the substrate by four thin arms, as shown in Figure 6. When a voltage is applied to the two sides of the device, a current is generated. This current causes the arms of the device to heat up and eventually expand, resulting in the motion of the central portion of the device. Due to the residual stresses of the deposited layers, the direction of motion for the device is usually down, toward the substrate.

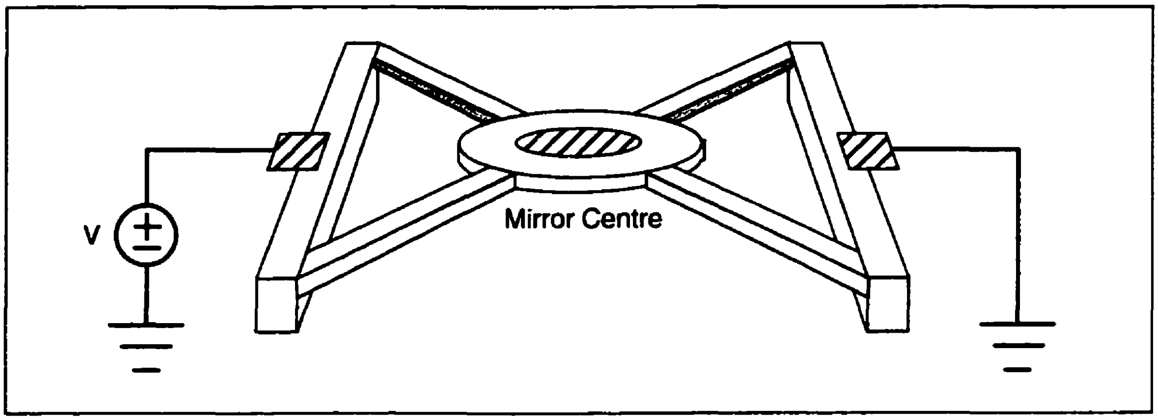


Figure 6. Schematic for thermally-actuated piston mirror

To implement this design, Poly1 was used to form the four resistive arms of the device. The central portion of the device was formed by stacking the Poly2 layer directly on top of the Poly1 layer; this was done to increase the mechanical rigidity of the mirror. Another alternative would have been to stack the Poly2 layer on top of the 2nd Oxide layer, so that the oxide layer would be sandwiched in-between the Poly1 and Poly2 layers, however this technique was not tried at this time. Finally, to increase the reflectivity of the mirror, a layer of metal was added to the top surface of the mirror. For comparison, both mirrors with and without this top layer of metal were sent for fabrication. Figure 7 shows the corresponding mask layouts for this design. The diameter of the central mirror is 60.0 μm. The length and width of each arm are 65.5 μm and 4.2 μm, respectively.

B. Tilting Mirrors

As an experiment, the piston mirror design was modified slightly to induce a tilting motion to the device. From Cowan and Bright's original work, it was shown that the thermal mirror device would translate smoothly in the vertical direction, without tilting, as long as the four arms of the device were designed to be perfectly symmetrical. Thus, to

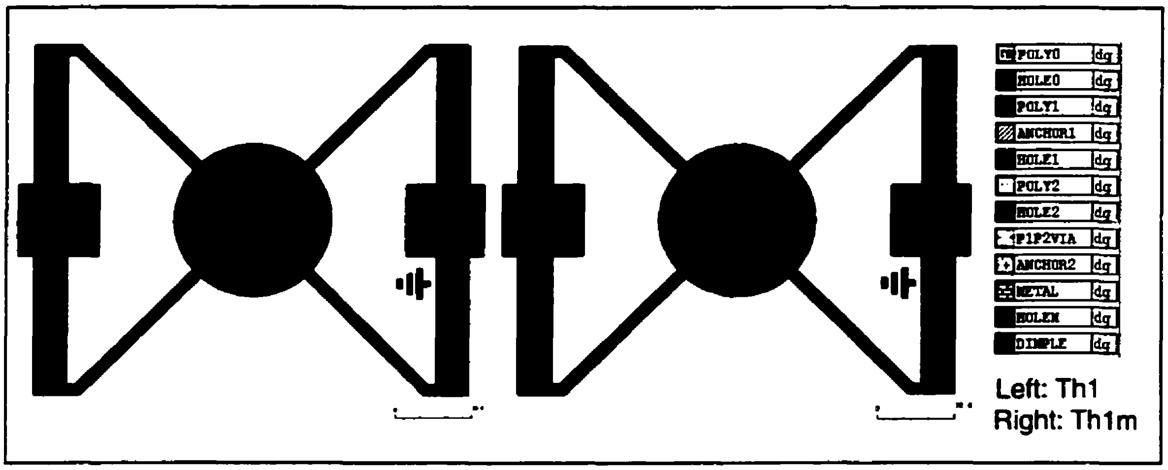


Figure 7. Mask layout for thermally actuated piston mirrors (Mirror Th1)

induce the mirror to tilt, the arms on the near side of the device were made thinner than those on the far side. As a result, when current passes through the device, the arms on the near side of the device are expected to heat up and expand faster than those on the far side, causing the mirror to tilt. The corresponding mask layouts for this design are shown in Figure 8. Again, the diameter of the central mirror is 60.0 μm and the length of all four arms is 65.5 μm. The width of the thin arms is 2.8 μm and the width of the thicker arms is 4.2 μm.

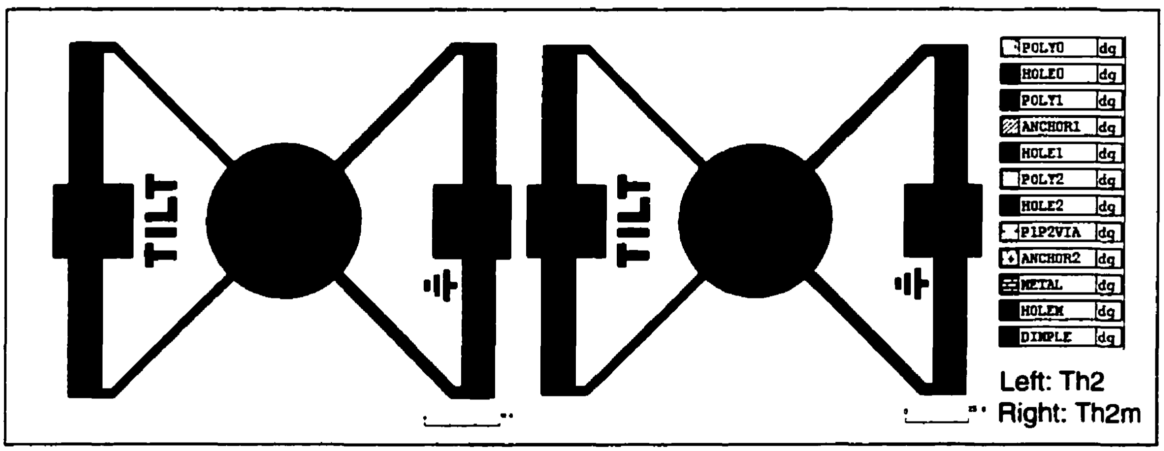


Figure 8. Mask layout for thermally actuated tilt mirrors (Mirror Th2)

5.2.3 Family III: Electrostatically Actuated Segmented Mirrors (E)

A. Piston Mirrors

This family of designs is based on the electrostatic flexure-beam micromirror device (FBMD) developed by M.A. Michalicek, D.E. Sene, and V.M Bright at the Air Force Institute of Technology [78]. Again, these designs were developed for use as a segmented deformable mirror array for use in adaptive optics. However, unlike the designs presented in the previous section, this device relies on electrostatic actuation, rather than thermal actuation. A general schematic for this device is shown in Figure 9.

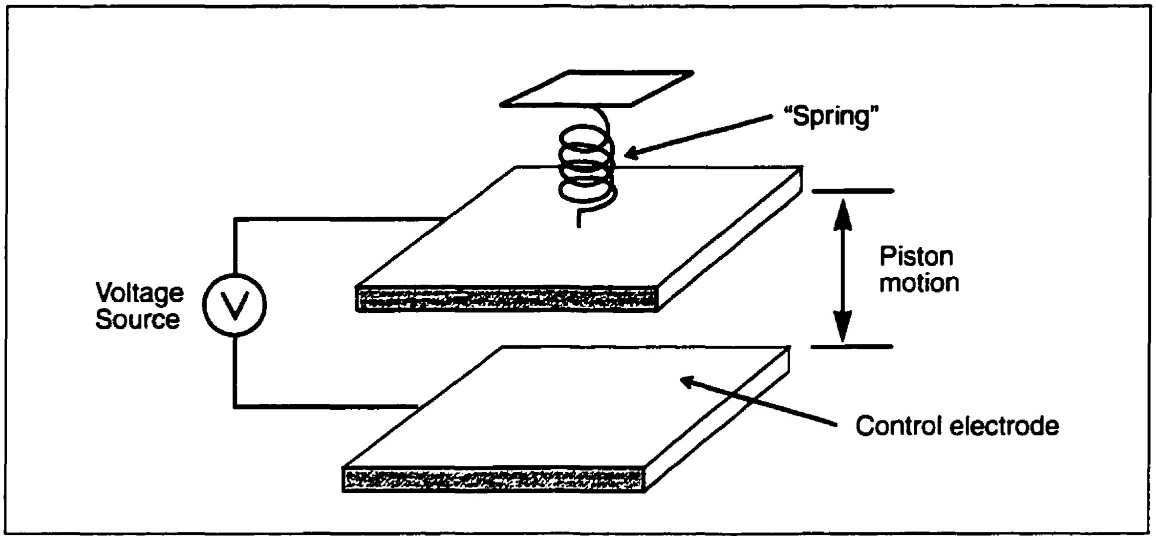


Figure 9. Schematic for electrostatically actuated piston mirror device

To operate this device, the top surface of the mirror is held at a fixed potential while a voltage signal is applied to the electrode below. The difference in potential between the two surfaces generates an electrostatic force causing the two surfaces to attract. However, since the lower electrode is already fixed to the substrate, it is the top surface of the mirror that moves down toward the bottom electrode, in a piston-like manner.

To implement this design, the flexures were created using Poly1 and the central portion of the mirror was created using a double layer of polysilicon, formed by stacking Poly2 directly on top of Poly1. In addition, to improve the surface quality of the mirror, the extra space around the control electrode was filled with Poly0 to form a ground plane, thus improving the overall planarity of the Poly0 layer. Note that this technique of using thin cuts to define the position of electrodes was also used for the design of the deformable membrane mirrors described earlier.

Finally, to increase the reflectivity of the mirror, a layer of metal was added to the top surface of the mirror. For comparison, both mirrors with and without this top layer of metal were sent for fabrication. Figure 10 shows the corresponding mask layout for this design. The overall dimensions of the mirror are 170 μm by 170 μm.

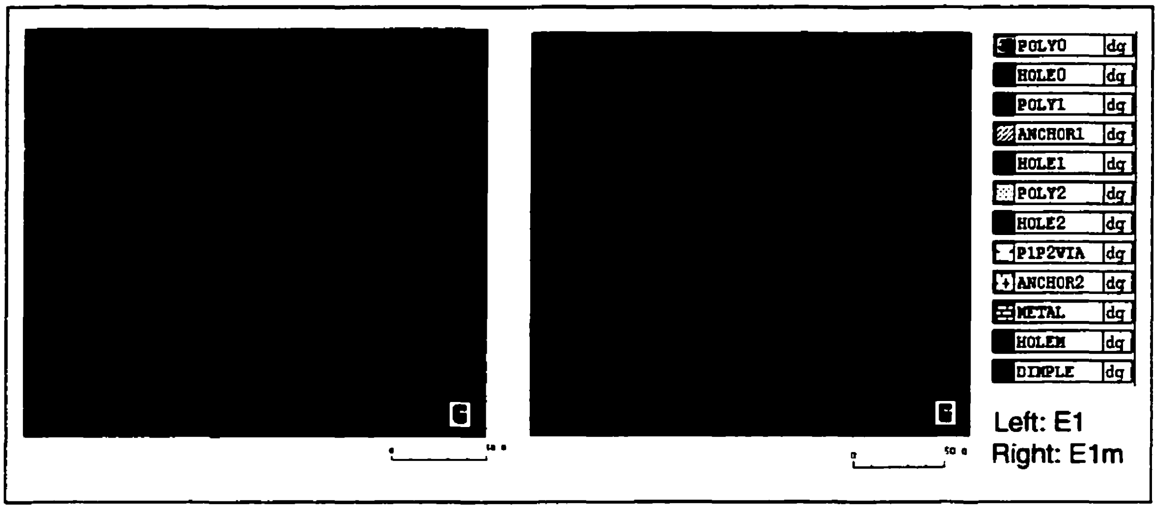


Figure 10. Mask layout for electrostatic piston mirrors (Mirror E1)

B. Digital Deflection Mirrors

An interesting variation to this design was also described by W.D. Cowan, et. al. in a recent paper on segmented mirrors for adaptive optics [61]. A general schematic of this design is shown in Figure 11. In this design, the area underneath the mirror is divided into four sections of equal area, with each section acting as a separate electrode. Since the deflection of the top surface is a function of both the area and the position of the control electrodes, the downward deflection of the mirror can be controlled by applying a constant voltage to each electrode in turn. Thus, by applying a fixed voltage to different combinations of the four electrodes, sixteen discrete levels of deflection can be obtained.

Finally, to implement this design, the electrode underneath the mirror was divided into four sections, as required. Two variants of this design were sent for fabrication. In the first variation, the etch holes for the top surface were spaced evenly, with certain etch

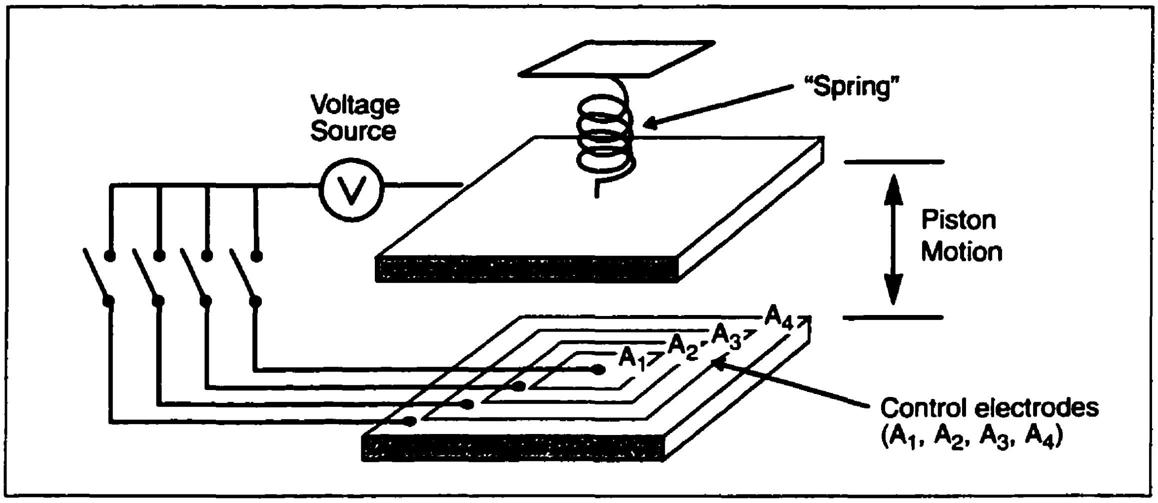


Figure 11. Schematic for digitally controlled electrostatic piston mirror

holes falling on top of the gaps between the electrodes defined in the Poly0 layer. As this was seen as a possible cause for manufacturing errors, a second design was also created. In this design, the etch holes were moved so that none of the holes would fall on top of any of the gaps. The corresponding mask layouts for both designs are shown in Figure 12. The overall dimensions for these designs are identical to those presented earlier: 170 µm by 170 µm. Neither mirror design was fabricated with a top layer of metal.

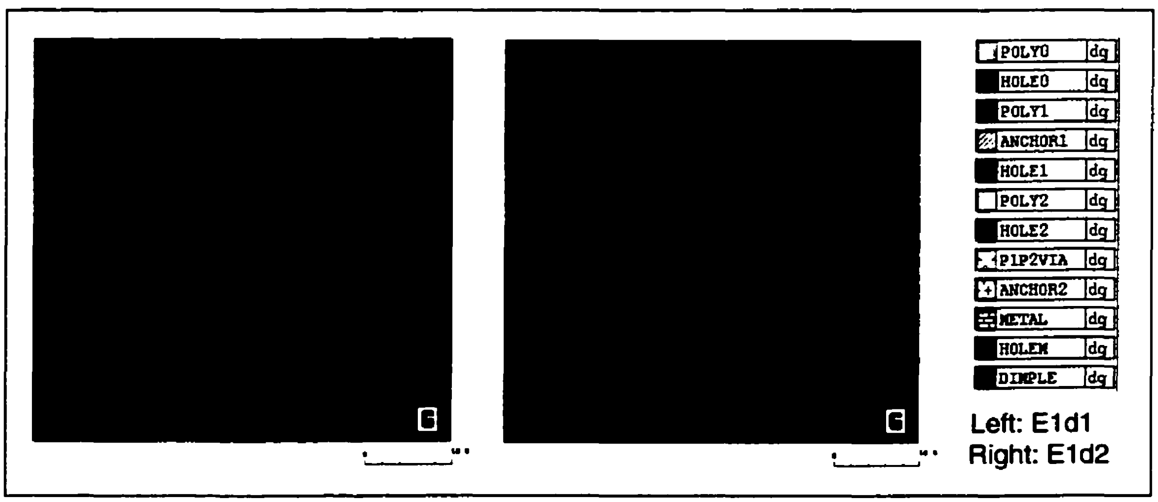


Figure 12. Mask layout for digitally controlled piston micromirrors (Mirror E1d)

C. Torsion Mirrors

As a third variation to this theme, the FBMD was also re-designed to work as a torsional mirror that would be able to rotate along a single axis. This was done by splitting the bottom electrode of the FBMD in to two separate electrodes and by removing the flexures on the upper and lower sides of the mirror. The resultant mirror would then be free to rotate along its horizontal axis. The corresponding mask layout for this device, Mirror E2, is shown in Figure 13. Both mirrors with and without a top layer of metal were sent out for fabrication.

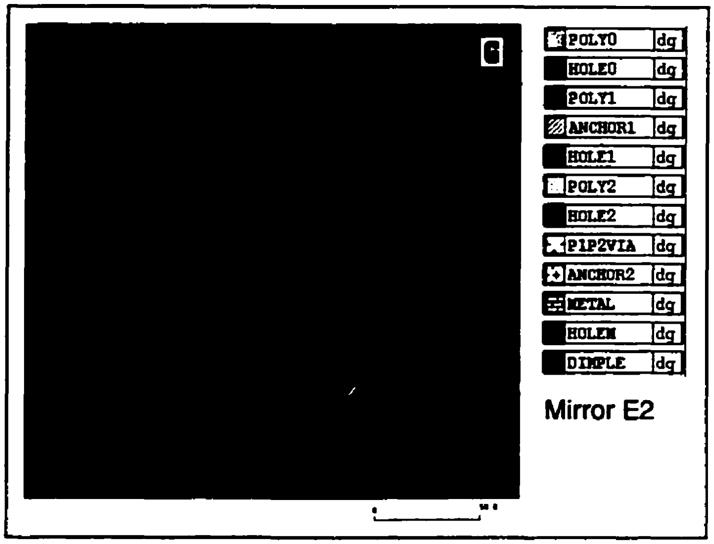


Figure 13. Mask layout for Mirror E2.

To operate this device, the top surface of the mirror is held at a fixed potential and a separate voltage is applied to one of the electrodes. A voltage applied to the upper electrode will cause the mirror to tilt toward the upper or "north" side of the device, whereas a voltage applied to the lower electrode will cause the mirror to tilt toward the lower or "south" side of the device. The two electrodes have been named north and south for clarity.

Finally, although this design is capable of tilting in the north and south directions, it is not capable of tilting along more than one axis. As a result, its use in beam-steering applications is very limited. This observation led to the creation of two additional families of designs, Families IV and V, which purport to address this issue.

5.2.4 Family IV: Electrostatic Torsion Mirror I (G)

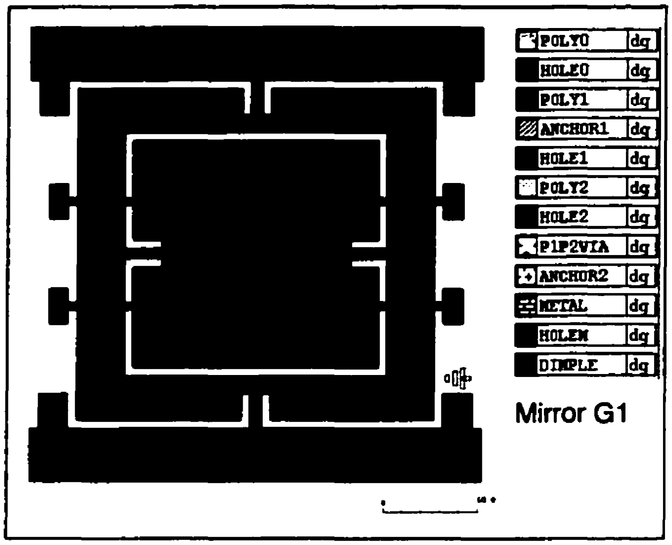


Figure 14. Mask layout for Mirror G.

This design was based on a prototype for a two-dimensional optical scanner developed by L. Fan and M.C. Wu at the University of California at Los Angeles [80]. A unique feature of this scanner was its use of a "micro-elevator" to elevate the surface of the mirror, thus allowing for larger rotation angles. However, since this would require a more complicated assembly process for the micromirror, this feature was excluded from the initial design. Instead, the idea of a gimbal-like suspension mechanism for the micromirror was retained. Using this "ring-within-a-ring" geometry, the new mirror would be able to rotate freely along two axes, instead of just one axis. The corresponding mask layout for this device, Mirror G, is shown in Figure 14.

To control the deflection of this device, the area underneath the mirror was divided into four quadrants to form four address electrodes, as suggested by the original design for the two-dimensional optical scanner. Thus, by applying control voltages to pairs of electrodes, the mirror can be made to rotate in all four directions; for clarity, these four directions are denoted north, south, east, and west. While the circuitry for this scheme may seem more complicated than that for other addressing schemes, it has the advantage of maximizing the area used by each pair of electrodes. This, in theory, should reduce the voltages required to operate this device.

Finally, unlike the previous mirror devices, no additional steps were taken to optimize the surface of this mirror. The top surface of this design was composed solely from Poly1 and no metal layers were added. The dimensions of the inner mirror surface are 130 μm by 130 μm and the overall dimensions of the device are 240 μm by 260 μm.

5.2.5 Family V: Electrostatic Torsion Mirror II (T)

Although the gimbal construction of the design for Mirror G was very appealing, the quadrant approach to the underlying electrodes seemed less ideal for the planarity of the mirror surface; due to problems with print-through, the top surface of Mirror G is expected to show indentations in the form of a cross. Thus, for this new family of designs, the positions of the electrodes were moved to the sides of the mirror, in order to create a smoother central region free from problems with print-through. In addition, to simplify the addressing scheme, the electrodes were redistributed so that each electrode would control the motion of the mirror in a single direction, as opposed to the double electrode scheme used for Family IV. The corresponding mask layout for this design, Mirror T, is shown in Figure 15.

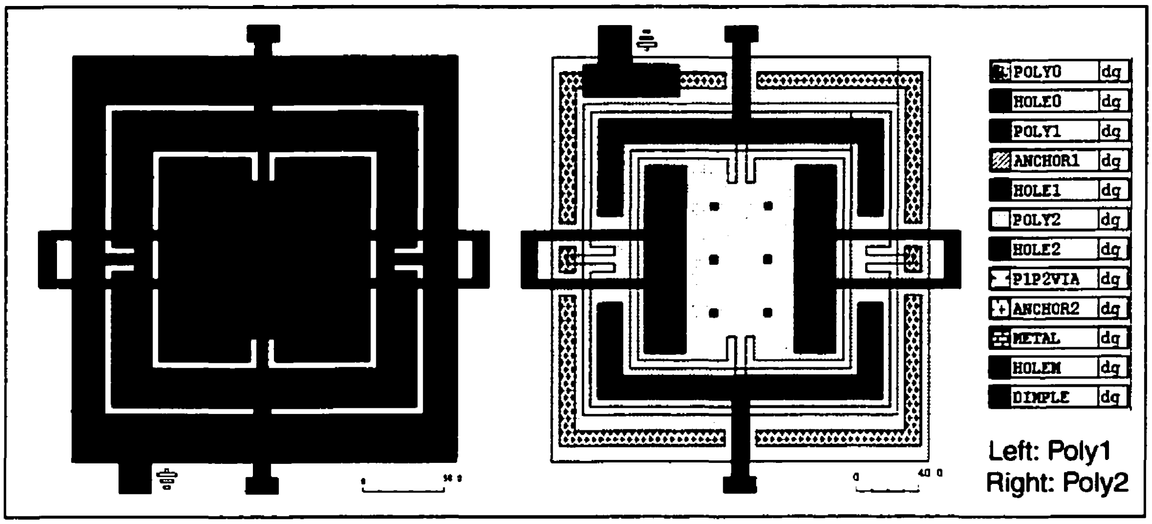


Figure 15. Mask layout for electrostatic torsion mirrors (Mirror T)

To maximize the mirror area free from print-through, the electrodes for the north and south terminals were moved off the central region of the mirror and hidden underneath the gimbal of the mirror. However, since the mirror surface and the gimbal are both held at the same potential, the mode of operation for these directions will still be the same: voltages applied to the electrodes below the gimbal will control rotation in the north and south directions; voltages applied to the electrodes below the mirror will control rotation in the east and west directions.

Another improvement to this design was the addition of anchored walls along all four sides of the mirror. This was done to create a barrier around the mirror that would prevent dust particles and other contaminants from entering the space beneath the mirror surface. Another change was made to the placement of the connecting wires for the electrodes. While the wiring for the north and south electrodes could be placed along the vertical axis of the mirror, the wiring for the east and west electrodes had to be moved, or else it would have run directly underneath the horizontal torsion springs for the gimbal (see Figure 15). Since this was seen as a possible source of complications, two wires per electrode were used instead, with each wire placed symmetrically about the horizontal axis of the mirror.

To test this design, two types of mirrors were sent for fabrication, the first using Poly1 as the top mirror surface and the second using Poly2 as the top mirror surface. Although the Poly1 design included dimples at the corners of the mirror in order to reduce problems with stiction, the Poly2 layer did not have a dimple layer available to it. Nevertheless, the Poly2 design is expected to have several advantages over that of Poly1, namely thinner torsion springs and greater rotation angles due to its added height from the substrate.

Finally, the overall dimensions for this mirror are the same as those for Mirror G. The length and width of the central area between the east and west electrodes is 100 μm by 70 μm.

5.3 Design Modifications for McGill MEMS 2 (MM2)

Based on the preliminary results of the McGill Test Chip, a second chip was sent for fabrication on November 22, 2000. Again, this chip was divided into four quadrants, with Quadrant 3 focusing on additional variations of the micromirror designs described in the previous sections. The details for these modifications are given below.

5.3.1 Modifications to Family II (Mirror Th)

Early tests on Mirror Th showed that these devices had a tendency to collapse toward the substrate. While this may have been caused by residual stresses in the polysilicon layer or problems with stiction during the release process, another possibility was that the four supporting arms may not have been strong enough to hold the weight of the central mirror. To rule out this possibility, three new designs were tried. In the first design, the thickness of the centre mirror was reduced to a single layer, thereby reducing the load supported by the arms of the device. The corresponding mask layout for this type of design is shown in Figure 16. The top layer of this particular device is composed of only Poly1. Other devices using a top layer of Poly2 and Poly2 with metal were also sent for fabrication.

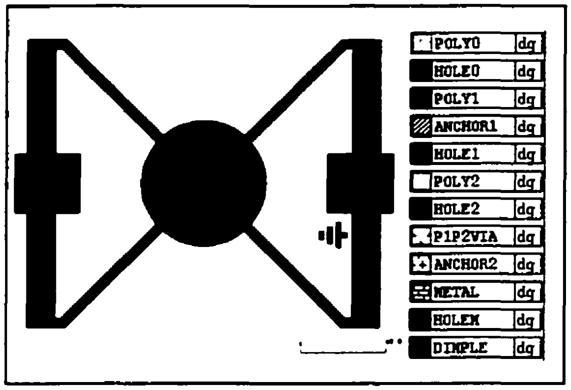


Figure 16. Mask layout for Th1_p1

In the second design, the length of the support arms were shortened by increasing the diameter of the central mirror. The corresponding mask layout for this design is shown in Figure 17. The length and width of the shortened arms are 50.2 μm and 4.2 μm. The diameter of the center mirror is 90.0 μm. Both mirrors with and without a top layer of metal were sent for fabrication.

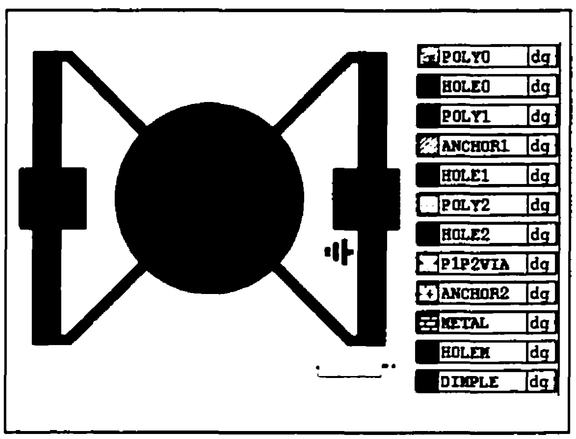


Figure 17. Mask layout for Th1_BIG

Finally, as a third variation, a circle of PolyO was included underneath the centre of the mirror as a "former", that is a layer influencing the topography and residual stresses of the upper layer in such a way that the legs of the mirror will tend to expand in the upward direction rather than in the downward direction. This technique was documented by Cowan and Bright and shown to work successfully for mirror geometries with low amounts of residual stress inherent in the original design [77]. The corresponding mask layout for this type of design is shown in Figure 18. A PolyO former was tried with both piston and tilt mirror devices.

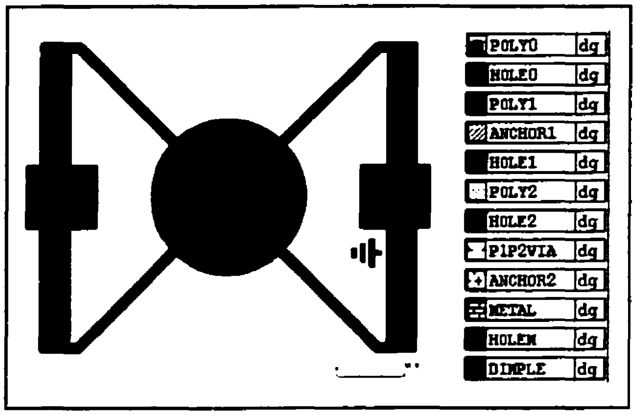


Figure 18. Mask layout for Th1_p0

5.3.2 Modifications to Family III (Mirror E).

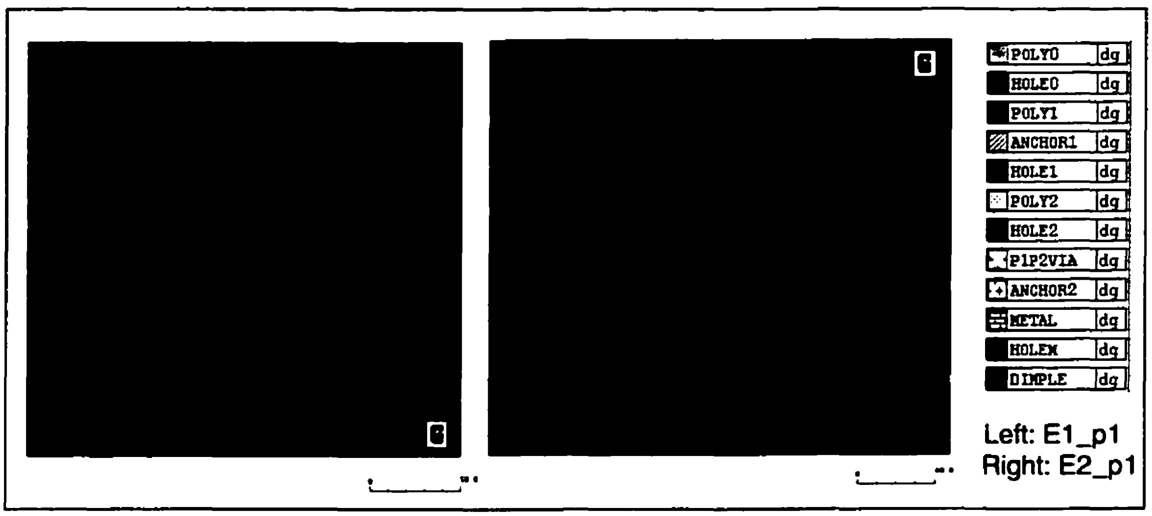


Figure 19. Modified mask layout for electrostatic piston & tilt mirrors (Mirror E1 & E2)

Two types of modifications were also explored for Mirror E. The goal of the first modification was to evaluate more rigorously the effect of thickness on the planarity and curvature of the top mirror surface. To accomplish this goal, two sets of devices were sent out for fabrication: devices with a top layer made out of a single thickness of polysilicon, namely Poly1, and devices with a top layer made out of a double thickness of polysilicon, namely Poly2 stacked on top of Poly1; the latter option being identical to the designs submitted for the first test chip. The corresponding mask layouts for the single thickness devices, both piston and tilt, are given in Figure 19.

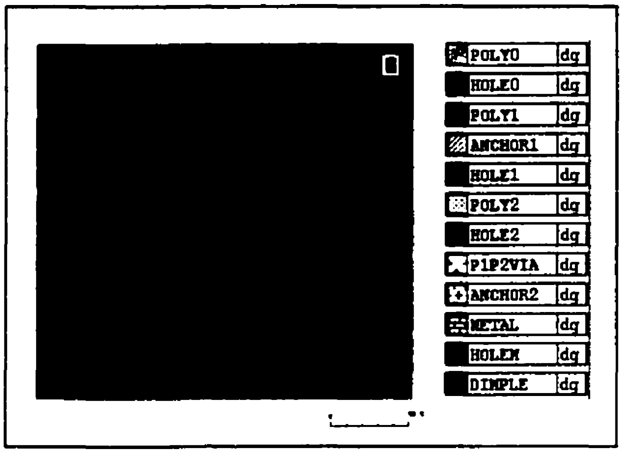


Figure 20. Mask layout for Mirror E2_h2

The goal of the second modification was to test the effect of using a different hinge structure to support the mirror surface and to determine how this change would affect the tilting motion of the device. Thus, instead of anchoring both hinges on opposite corners of the device, the hinges were anchored on the same side of the device. Figure 20 shows the corresponding mask layout for this design. For comparison, both mirrors with single and double thicknesses of polysilicon were sent for fabrication.

5.3.3 Modifications to Family V (Mirror T)

Finally, a number of variations were explored for the mirrors in Family V. For example, in order for this mirror to be used in an array with a grid spacing of 250 μm, the overall dimensions of Mirror T needed to be made slightly smaller. Thus, to accomplish this task, the walls surrounding Mirror T were reduced by several microns, yielding the space necessary to place extra control wires in-between the mirrors. The corresponding mask layout for this device is shown in Figure 21. The overall dimensions of the new mirror, excluding control electrodes, has been reduced to 222 μm by 224 μm.

To improve the surface quality of Mirror T, two additional designs were included for fabrication. In the first design, an extra section of Poly0 was added to the area between the east and west electrodes, located below the mirror surface. This was done in an effort to smooth out the topography of the Poly0 layer before the deposition of the upper mirror layers and is expected to reduce problems with print-through. Figure 21 shows the corresponding mask layout for this design.

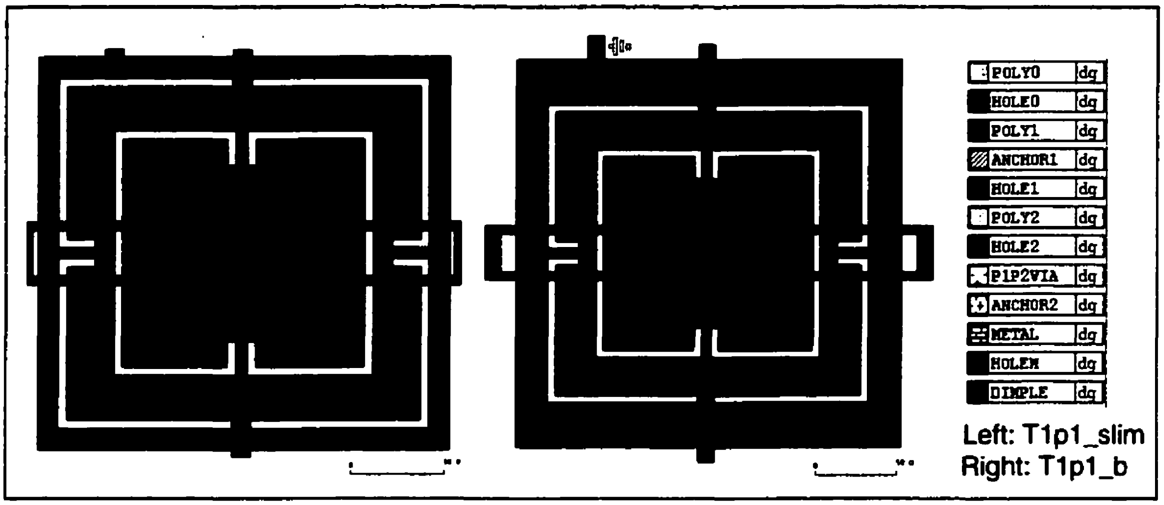


Figure 21. Modified mask layouts for 2-axis torsional mirror (Mirror T)

In the second design, a different approach was taken to improve the quality of the mirror surface. In order to reduce the residual stresses in the top layer of the mirror, the central portion of the mirror was reinforced using a double thickness of polysilicon; this is expected to reduce the amount of curvature observed in the top layer of the device. The corresponding mask layout for this design is shown in Figure 22.

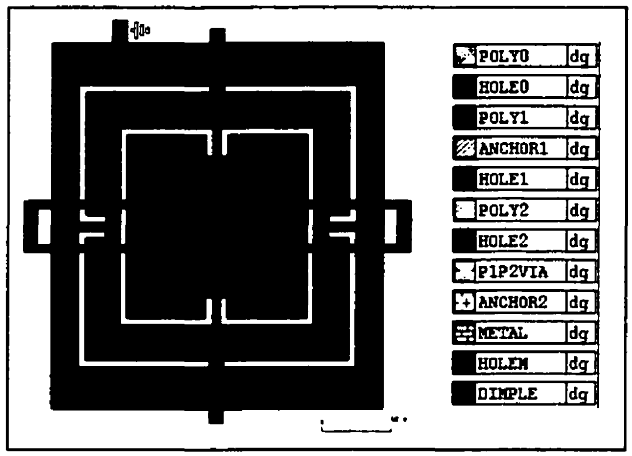


Figure 22. Mask layout for Mirror T1p12

Finally, since preliminary tests on the Poly2 version of Mirror T exposed a distinct problem with stiction, a second version of this design was created. In this design, the squared-off corners used for the electrodes in the original design were

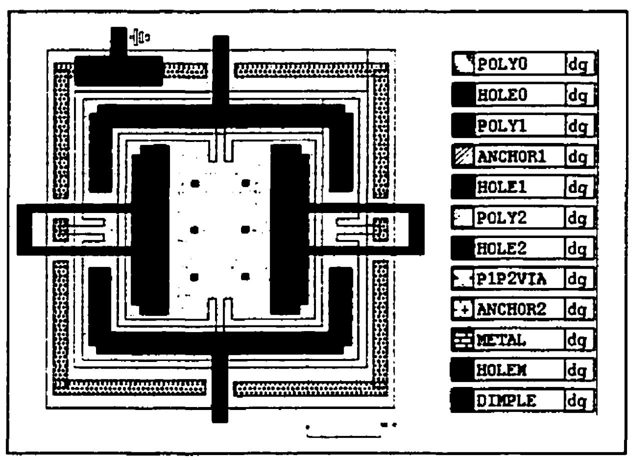


Figure 23. Mask layout for Mirror T1p2_b

replaced with the notched corners used for the electrodes in the Poly1 version of this design (see Figure 15 and Figure 23 for comparison). Thus, due to the conformal nature of the MUMPs process, the top layer of the mirror is expected to follow the shape of the notches, forming a set of "landing pads" in the process. These landing pads will then prevent the top surface of the mirror from coming too close to the bottom of the device and thus prevent it from adhering to the bottom surface of the device. The corresponding mask layout for this design is shown in Figure 23.

5.4 Summary

In this section, five different families of micromirror designs were presented. Families I, II, and III included designs for piston mirrors, which have applications in adaptive optics, whereas Families IV and V included designs for 2-axis torsional mirrors, which have applications in beam scanning and optical switches. In addition, Families II and III also included designs for 1-axis tilt mirrors; these designs may also be used as simple optical switches.

Table 3 summarizes the key points for each family of designs. In addition, this table also summarizes the naming scheme used for labelling the experimental results obtained from these devices. The term "P2/P1" is used to denote the stacked layer formed by depositing Poly2 directly on top of the Poly1 layer. The total number of devices fabricated per family for the McGill Test Chip was 30, 720, 540, 30, and 60 for Families I, II, III, IV, and V, respectively. For the second McGill MEMS chip, the total number of devices included for Families II, III, and V were 450, 420, and 180, respectively.

TABLE 3: Summary of Micromirror Designs by Family

Family (Prefix)	Suffix	Top Layer	Metal	Motion / Comments	MTC	MM2
I: Deformable membrane (DM)	1	Poly2		Deformable, piston driven	x	
	1m		x		x	
II: Thermal (Th)	1	P2/P1		Piston	x	x
	1m		x		x	x
	1_p0			Piston, with Poly0 former		x
	1m_p0		x			x
	1_BIG			Piston, with wider central mirror and shorter support arms.		x
	1_BIGm		x			x
	1_p1	Poly1		Piston, single thickness of polysilicon		x
	1_p2	Poly2				x
	1_p2m		x			x
	2	P2/P1		Tilt	x	x
	2m		x		x	
	2_p0			Tilt, with Poly0 former		x
III: Electrostatic (E)	1	P2/P1		Piston	x	x
	1m		x		x	x
	1d1			Piston, digital control scheme (etch hole patterns 1and 2)	x	
	1d2				x	
	1_p1	Poly1		Piston, single thickness of polysilicon		x
	2	P2/P1		Tilt	x	x
	2m		x		x	
	2_p1	Poly1		Tilt, single thickness of polysilicon		x
	2_h2	P2/P1		Tilt, second hinge structure, double & single thicknesses of polysilicon		x
	2_h2p1	Poly1				x
IV: Gimbal (G)	1	Poly1		Tilt	x	
V: Torsion (T)	1p1	Poly1		Tilt	x	x
	1p1_slim			Tilt, with thinner outer walls		x
	1p1_b			Tilt, with extra Poly0 layer		x
	1p12	P2/P1		Tilt, double thickness of polysilicon		x
	1p2	Poly2		Tilt	x	x
	1p2_b			Tilt, electrodes modified to prevent stiction		x

6.0 DEVICE MODELING

6.1 Overview

Despite the large variety of devices implemented in this project, two basic models can be used to describe the behaviour of these devices: the microbridge model and the electrostatic parallel-plate capacitor model. Using the first model, devices such as thermally-actuated micromirrors can be modeled by first dividing the structure into a set of smaller structures, called microbridges. These microbridges can then be used to model both the thermal and electrical behaviour of the device simultaneously.

On the other hand, the electromechanical behaviour of devices such as electrostatic micromirrors can be modeled using the electrostatic parallel-plate capacitor model, with the top mirror surface and bottom control electrode forming the upper and lower plates of the parallel plate capacitor. The flexures holding the top surface of the mirror can be modeled using the ideal spring model, where the restoring force or torque exerted on the mirror is directly proportional to the linear or angular displacement of the mirror. Consequently, devices in this category can be further divided into two groups depending on the type of motion and hence the type of spring constant used for the device: for mirrors operating in the piston mode, a linear spring constant is required; for mirrors operating in the torsion mode, a rotational spring constant is required. Table 4 lists the corresponding model used for each of the designs presented in Section 5.0. For simplicity, the designs from Section 5.0 are divided into seven categories, according to the family and type of motion of the device.

TABLE 4: Summary of Device Models by Family

Family (Prefix)	Suffix	Microbridge Model	Electrostatic Parallel-Plate Capacitor Model	
		Thermal+Elect.	Piston mode	Torsion mode
I: Deformable Membrane (DM)	all		x	
II: Thermal (Th)	1, 1m, 1_p0, 1m_p0, 1_BIG, 1_BIGm, 1_p1, 1_p2, 1_p2m	x		
	2, 2m, 2_p0	x		
III: Electrostatic (E)	1, 1m, 1_p1, 1d1, 1d2		x	
	2, 2m, 2_p1, 2_h2, 2_h2p1			x
IV: Gimbal (G)	all			x
V: Torsion (T)	all			x

Finally, while these models tend to work relatively well for simple devices, such as those presented in this thesis, it should be noted that a more accurate representation of these devices can be generated using more complicated analysis tools, such as those incorporating finite element analysis (FEA). In general, one of the major advantages of multiphysics FEA is its ability to combine both thermal, electrical, and mechanical analyses simultaneously. However, FEA is also a much more involved process, requiring large amounts of time and resources during both the setup and execution phases of the analysis. By comparison, analytical methods can be performed in relatively short amounts of time and thus provide a useful tool for understanding the basic behaviour of micromirror devices. Additional details for these analytical models are described in the sections below.

6.2 Microbridge Model for Thermally-Actuated Devices

To model the behaviour of thermally-actuated devices — that is, devices that move by thermal expansion when a current is applied to the device — devices must first be divided into a collection of microbridges. As the analysis involves both electrical and thermal considerations, each microbridge must be represented using two separate models: an electrical model and a thermal model [77]. For the electrical model, each microbridge is modeled as a resistor R_i whose resistance is a function of temperature. For the thermal model, each microbridge is represented using a combination of the following: the thermal conductance G_i of the microbridge, the thermal conductance G_{gas} of the media surrounding the microbridge, the thermal capacitance C_i of the microbridge, and finally the equivalent current source I_R for the microbridge, whose value is equal to the current generated in the resistance R_i of the electrical model [81]. The two models for the microbridge are shown below in Figure 24. These models can be used for both DC and AC analyses, however for AC signals that are faster than the thermal response of the device, a DC signal with the same average power as the AC signal should be used instead.

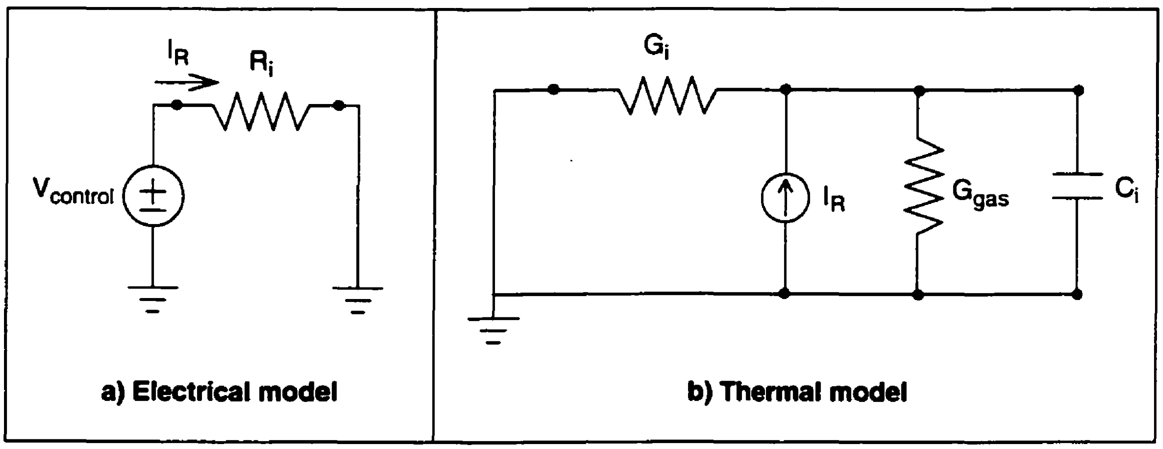


Figure 24. Electrical and thermal models for individual microbridge segments

Using SPICE simulation tools, the electrical and thermal models can be simulated simultaneously to determine the final temperature of each microbridge element. From this value, the total expansion of the microbridge can be calculated using the thermal coefficient of expansion for the material. As an example, the thermal coefficient of expansion for silicon ranges from about 2.6 x 10^{-6} K^{-1} at room temperature, to 4.2 x 10^{-6} K^{-1} at 1000 K [82]. Thus, the total change in length of the microbridge can be calculated and the final deflection of the microbridge, Δh, can be estimated using simple trigonometry, as shown in Figure 25.

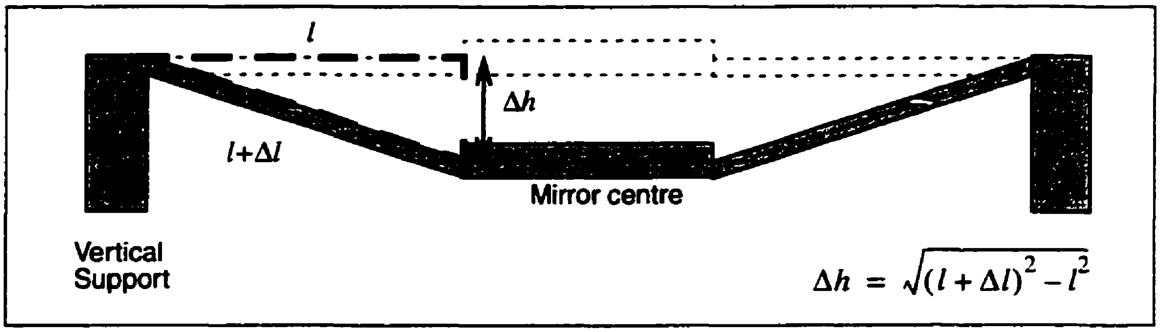


Figure 25. Cross-sectional view of Mirror Th, showing thermal expansion of microbridge

Finally, by cascading the different microbridges in sequence, a complete model for the whole device can be generated. For example, the complete model for the thermally actuated mirror "Th1" (see Section 5.2.2) can be modeled by dividing each of the legs into a series of ten or more microbridge segments; for accurate simulation results, a minimum of ten microbridge segments are required. Similarly, the effect of the central disk of the mirror can be modeled by dividing it into ten microbridge segments as well. The final model for this device is shown in Figure 26.

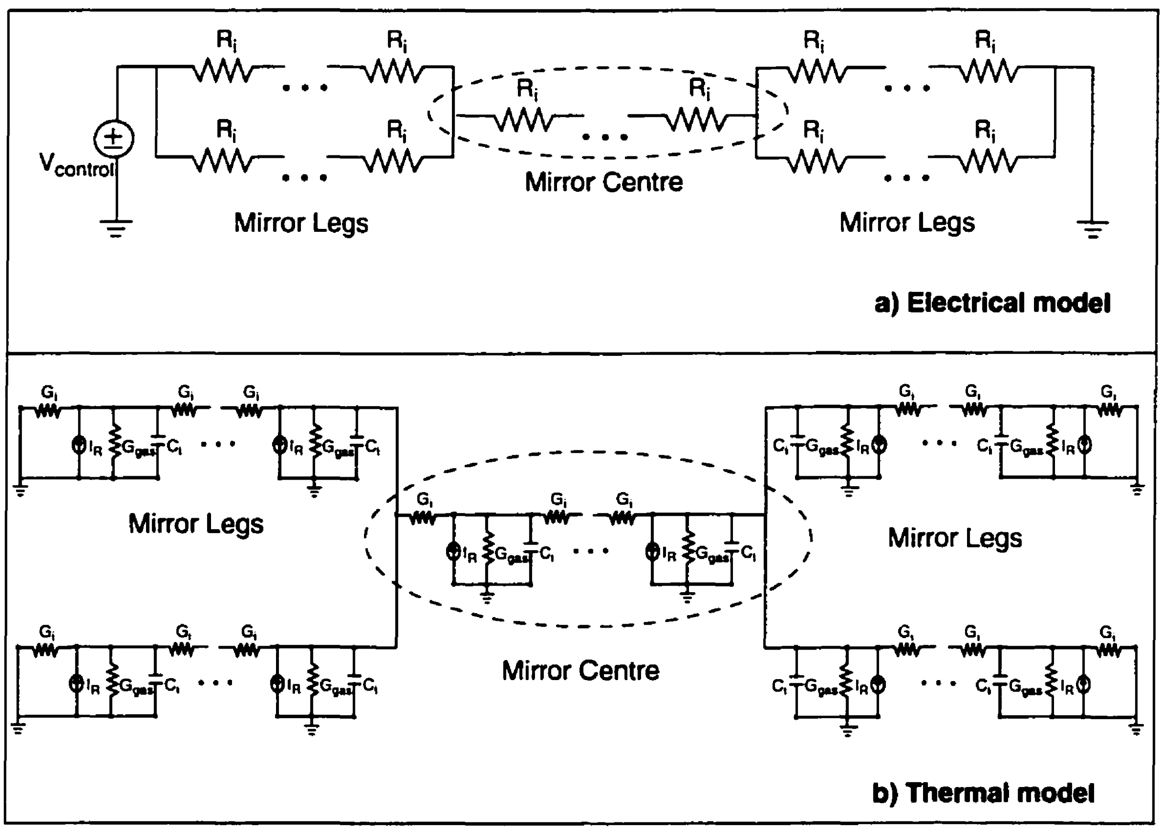


Figure 26. Complete electrical and thermal models for Mirror Th1 (Piston)

6.3 Electrostatic Capacitor Model for Electrostatic Mirrors

For electrostatically-actuated mirror devices, the electrostatic capacitor model can be used to determine the final position of the mirror as a function of the input voltage for the device. However, depending on the position of the electrodes and the position of the flexures used to support the mirror, the mirror can be actuated in one of two modes: the piston mode or the torsion mode. Since a different set of equations is needed to describe the motion of the mirror for each mode, the two cases are treated separately in the sections below.

6.3.1 Piston mode

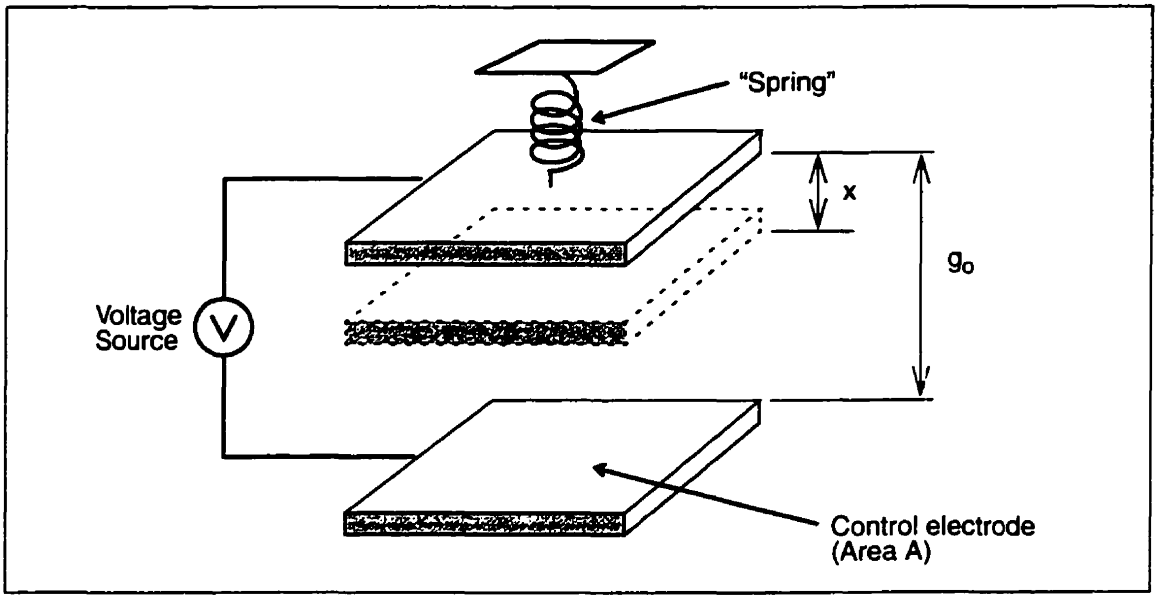


Figure 27. Schematic of electrostatic micromirror operating in the piston mode

Figure 27 shows a schematic of an electrostatic mirror operating in the piston mode, where V is the voltage applied across the two plates of the capacitive structure, g_0 is the initial distance of the air gap between the two plates, and x is the vertical displacement of the top mirror surface from its position at rest. Since the surface of the mirror is suspended directly above the electrode located on the surface of the substrate, this can be modeled using two parallel plates of infinite width. This simplification effectively ignores the contribution of any fringing effects that may occur, however a more complete analysis of this situation by M. A. Michalicek, D. E. Sene, and V. M. Bright [78] showed that the fractional loss in the electrostatic force due to fringing effects would be less than 1% for a mirror with a surface area of 50 μm^2 and less than 0.1% for a mirror with a surface area of 1000 μm^2; both values were calculated for separation distances in the range of 1.0 μm to 3.0 μm. In addition, due to the rigidity of the top surface, it can be safely assumed that this small variation in electrostatic force will not cause any non-uniform bending of the upper surface of the mirror. Thus, the electrostatic force F_{elect} created by the voltage V can be readily approximated by the following equation:

$$F_{elect} = \frac{\varepsilon_0 A V^2}{2(g_0 - x)^2} \tag{1}$$

where ε_0 is the permittivity of the air between the two plates and A is the area of the plate.

Although the electrostatic force generated causes the two surfaces to attract, the surface of the mirror is also suspended by a set of flexure springs, which exert a mechanical restoring force on the mirror. This restoring force can be modeled using Hooke's Law:

$$F_{mech} = Kx \tag{2}$$

where K is the spring constant for the particular mirror design. As a first approximation, the value of K can be estimated using the cross-sectional spring constant k_{cs} of the flexures:

$$k_{cs} = \frac{Ewt^3}{L^3} \tag{3}$$

where L, w, and t are the length, width, and thickness of a single flexure, and E is Young's modulus of elasticity for the flexure material, in this case polysilicon [79]. Thus for a device such as Mirror E1, which is supported by four flexure beams, the spring constant for the structure is given by

$$K_{E1} = 4k_{cs} = 4\left(\frac{Ewt^3}{L^3}\right) \tag{4}$$

Note, however, that this value can be further refined by introducing additional terms to account for the stress and torsion induced in the flexure. Details of these approximations can be found in the work published by M. A. Michalicek, et al. [78]

The final displacement of the mirror can be found by setting the equation for the electrostatic force (1) equal to that of the mechanical force (2), which yields the following relation:

$$V = (g_0 - x)\sqrt{\frac{2Kx}{\varepsilon_0 A}} \tag{5}$$

A typical graph for displacement versus voltage is shown in Figure 28; this graph was calculated using the design parameters for Mirror E1. The values for these parameters are summarized in Table 6.

TABLE 6: Parameters

	MIRROR E1
w	6.0 μm
t	2.0 μm
l	98.0 μm
A	23 104 μm^2
E	168 GPa
K	26.33 N/m

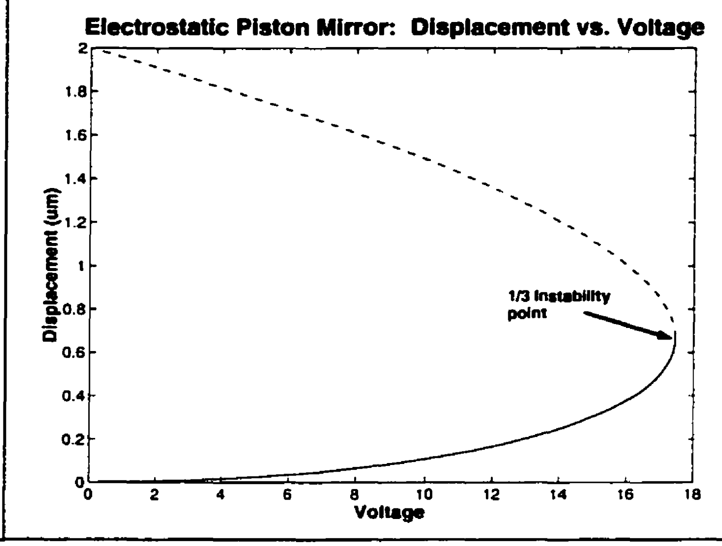


Figure 28. Graph of displacement versus voltage for Mirror E1

An interesting point on this graph is the so-called "1/3 instability point". This term is used to describe the point on the graph where the displacement of the top surface is almost equal to one-third the total distance of the air gap. At this point, the electrostatic force overcomes the mechanical restoring force supplied by the springs, causing the top surface of the mirror to be pulled down completely. Consequently, the corresponding voltage for this point is often described as the "pull-in" voltage or the "snap-to" voltage for the device. The theoretical pull-in voltage for Mirror E1 is 17.47 V.

6.3.2 Torsion mode

For the torsional mode of operation, the position of the electrode is shifted so that a potential difference across the two plates of the capacitor will create an electrostatic torque, causing the top surface of the mirror to rotate toward the bottom electrode. However, since the mirror is suspended by a set of flexure beams that act like torsional springs, a mechanical torque is also produced that counterbalances this movement. Thus, the final deflection angle of the mirror for a given voltage is determined by setting the equation for electrostatic torque equal to that for mechanical torque.

A. Electrostatic torque

Figure 29 shows a schematic of a generalized mirror design, where α is the angle between the two plates, a_1 is the distance between the axis of rotation and the nearest edge

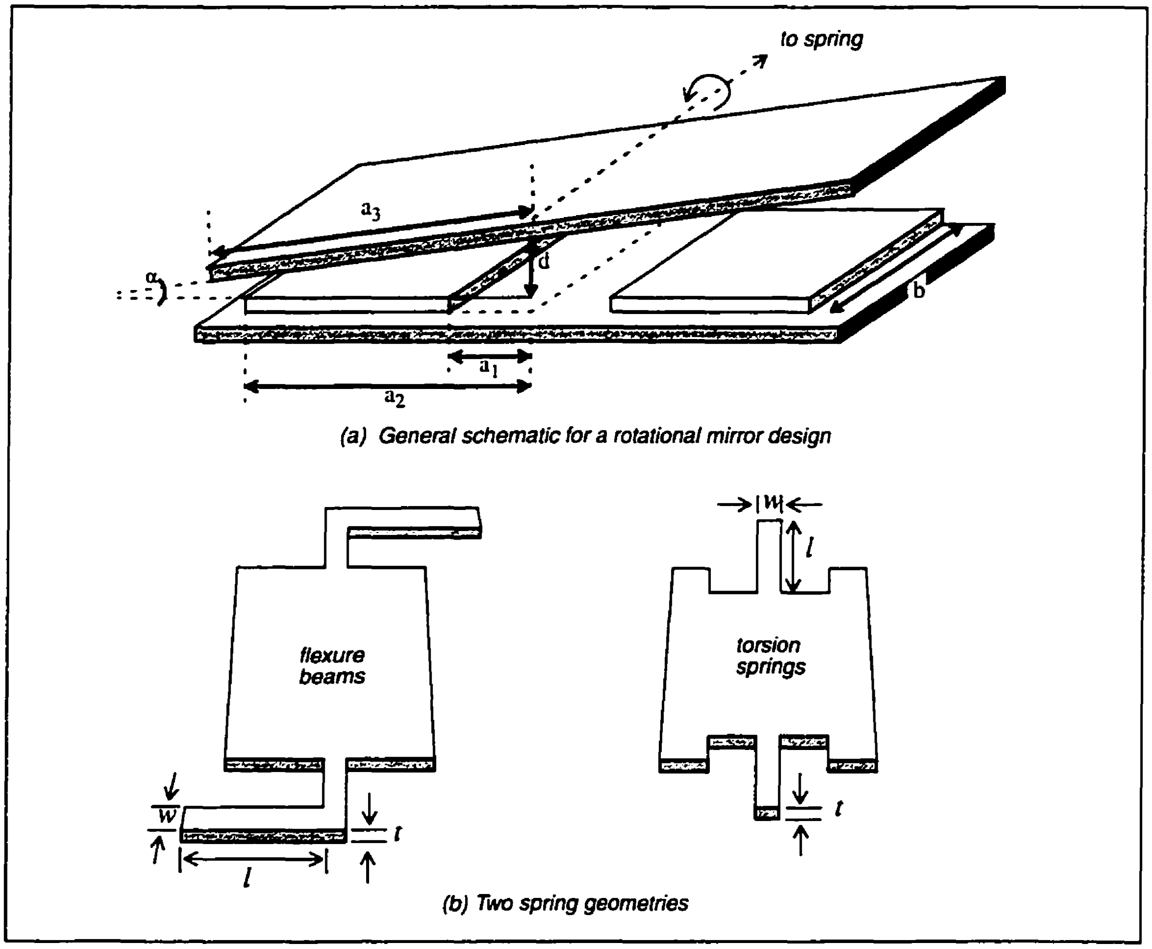


Figure 29. Schematics for a generalized rotational mirror design.

of the electrode, a_2 is the distance between the axis and the farthest edge of the electrode, a_3 is the distance between the axis and the edge of the mirror plate, b is the width of the electrode, and d is the distance between the mirror and the surface of the electrode, measured at the axis of rotation.

Using these variables, the small angle approximation for the electrostatic torque experienced by the mirror, expressed as a function of its angular position α, is given by the following equation, where V is the voltage applied to the electrode [83]:

$$M_{elect}(\alpha) = \frac{\varepsilon_o V^2 b}{2\alpha^2}\left[\frac{d}{d-a_2\alpha} - \frac{d}{d-a_1\alpha} + \ln\left(\frac{d-a_2\alpha}{d-a_1\alpha}\right)\right] \qquad (6)$$

As an example, the values for the device parameters a_1, a_2, a_3, b and d for three torsional mirror designs — namely Mirror E2, Mirror G, and Mirror T — are summarized in Table 7.

TABLE 7: Summary of Device Parameters for Three Torsional Mirror Designs

	Mirror E2	Mirror G	Mirror T	
	North / South	All Directions	East / West	North / South
a_1	21 µm	3.0 µm	35 µm	75 µm
a_2	76 µm	63 µm	60 µm	90 µm
a_3	85 µm	65 µm	65 µm	95 µm
b	152 µm	127 µm	122 µm	180 µm
d	2.0 µm	2.0 µm	2.0 µm	2.0 µm

B. Mechanical torque

The mechanical torque for the mirror as a function of the rotation angle, α, can be modeled as:

$$M_{mech} = K_\alpha \alpha \qquad (7)$$

where K_α is the spring constant for the structure.

For flexure beams of length l, width w, and thickness t (see Figure 29), K_α is equal to [83]:

$$K_\alpha = \frac{Ewt^3}{6l} \tag{8}$$

where E is the Young's modulus of elasticity for polysilicon and is in the range of 160-180 GPa for structures fabricated using the MUMPs process [84].

For torsional springs of length l, width w, and thickness t, K_α is given by the following equation [67]:

$$K_\alpha = 2 \times \frac{Gwt^3}{3l}\left[1 - \frac{192}{\pi^5} \cdot \frac{t}{w}\tanh\left(\frac{\pi w}{2t}\right)\right] \tag{9}$$

where G is the shear modulus for polysilicon. G is related to the Young's modulus by Poisson's ratio, ν:

$$G = \frac{E}{2(1+\nu)} \tag{10}$$

where $\nu = 0.28$ for polysilicon. Thus, for structures fabricated using the MUMPs process, G is in the range of 62.5 GPa to 70.3 GPa.

Table 8 shows a list of the design parameters used to calculate the theoretical value of K_α for the three torsional mirror designs described earlier. For each design, a combination of the flexure beam model and the torsion spring model was used. The numerical value listed in the table is for the value $E = 168$ GPa. Since, in practice, the value of E for thin films may vary significantly from structure to structure and from one fabrication run to another, this value may be used to calibrate the theoretical model and to ensure a good fit with the experimental data obtained [78].

TABLE 8: Summary of Design Parameters for Calculating K_α

	Mirror E2	Mirror G	Mirror T	
	North / South	All Directions	East / West	North / South
l	94 μm	30 μm	30 μm	30 μm
w	6.0 μm	5.0 μm	5.0 μm	5.0 μm
t	2.0 μm	2.0 μm	2.0 μm	2.0 μm
K_α	1.43×10^{-8} Nm	4.37×10^{-8} Nm	4.37×10^{-8} Nm	4.37×10^{-8} Nm

C. Pull-in voltage and normalized pull-in angle

As mentioned previously, the deflection angle of the mirror is given by setting the equation for electrostatic torque equal to that for mechanical torque. Using these equations, the resulting angle of the mirror for a given voltage V can be calculated using standard mathematical tools, such as MATLAB. A typical graph showing tilt angle versus voltage is given in Figure 30; this graph was calculated using the design parameters for Mirror T, when rotating in the east-west direction.

While for small angles of α the electrostatic torque can be balanced by the mechanical torque of the mirror, a critical angle exists where the electrostatic torque will overcome the mechanical torque exerted by the springs. This condition is called the "pull-in" condition and is marked on the graph in Figure 30.

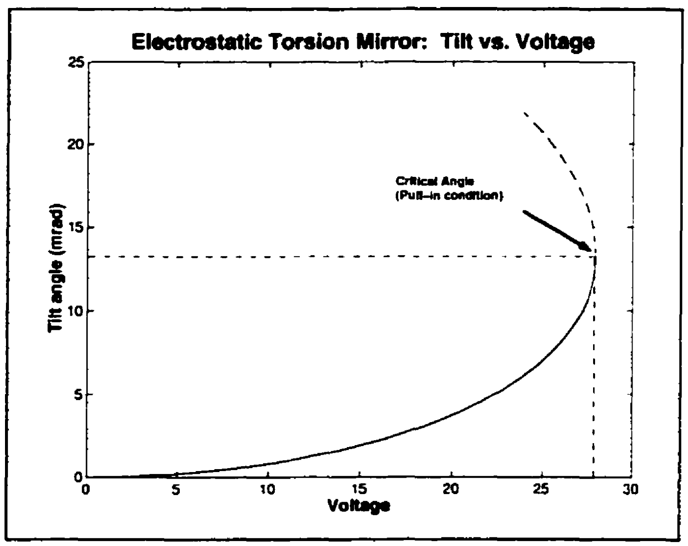


Figure 30. Graph of tilt vs. voltage (Mirror T, E/W)

The values for the critical angle and pull-in voltage for the device can be determined analytically using the methods outlined by O. Degani, et. al. [83] By normalizing the variables in equation (6) with respect to the distance a_3 — that is, the distance from the axis to the edge of the mirror — the electrostatic torque of the mirror can be rewritten as

$$M_{elect}(\alpha) = \frac{\varepsilon_o V^2 b}{2\alpha_{max}^2 \Theta^2} \cdot \left[\frac{1}{1-\beta\Theta} - \frac{1}{1-\gamma\Theta} + \ln\left(\frac{1-\beta\Theta}{1-\gamma\Theta}\right)\right] \tag{11}$$

where $\alpha_{max} = d/a_3$, $\beta = a_2/a_3$, $\gamma = a_1/a_3$, and $\Theta = \alpha/\alpha_{max}$ is the normalized angle for the mirror. Equation (11) can then be expanded into an infinite series and the solution for the critical angle, Θ_{pin}, can be approximated analytically using the following Nth order equation:

$$\sum_{n=0}^{N} (1-n)\left(\frac{n+1}{n+2}\right)(\beta^{n+2} - \gamma^{n+2})\Theta^n{}_{pin} = 0 \tag{12}$$

Good convergence for this solution can be obtained for N > 10.

Finally, the pull-in voltage for the mirror can be calculated using the following equation:

$$V_{pin}(\beta, \gamma) = \sqrt{\frac{2K_\alpha d^3}{\varepsilon_0 b a_3^3} \cdot f(\beta, \gamma)} \tag{13}$$

$$\text{where } f(\beta, \gamma) = \frac{\Theta^3{}_{pin}}{\left[\frac{1}{1-\beta\Theta_{pin}} - \frac{1}{1-\gamma\Theta_{pin}} + \ln\left(\frac{1-\beta\Theta_{pin}}{1-\gamma\Theta_{pin}}\right)\right]} \tag{14}$$

Table 9 shows the theoretical values for V_{pin} and Θ_{pin} corresponding to the three mirror designs. These values were calculated using the K_α values obtained earlier for E = 168 GPa.

TABLE 9: Theoretical Values for V_{pin} and Θ_{pin}

	Mirror E2	Mirror G	Mirror T	
	North / South	All Directions	East / West	North / South
V_{pin}	9.53 V	22.69 V	27.90 V	20.38 V
Θ_{pin}	0.4822	0.4541	0.4328	0.4297

7.0 CHARACTERIZATION

Several test procedures were developed to characterize the surface quality of the mirrors at rest as well as the active behaviour of these devices when actuated. This included the use of a static interferometer to inspect the devices visually for evidence of stiction or other surface defects, the use of a phase-shifting interferometer to generate surface profiles of the device, and the use of a monochromator to measure the reflectivity of the mirror surface across a broad range of wavelengths. The individual steps for this characterization process are described below.

7.1 Visual Inspection

Upon arrival, the chips are inspected visually for signs of debris or other defects that may have occurred during manufacturing. Examples of unwanted debris and surface abrasions are shown in Figure 31.

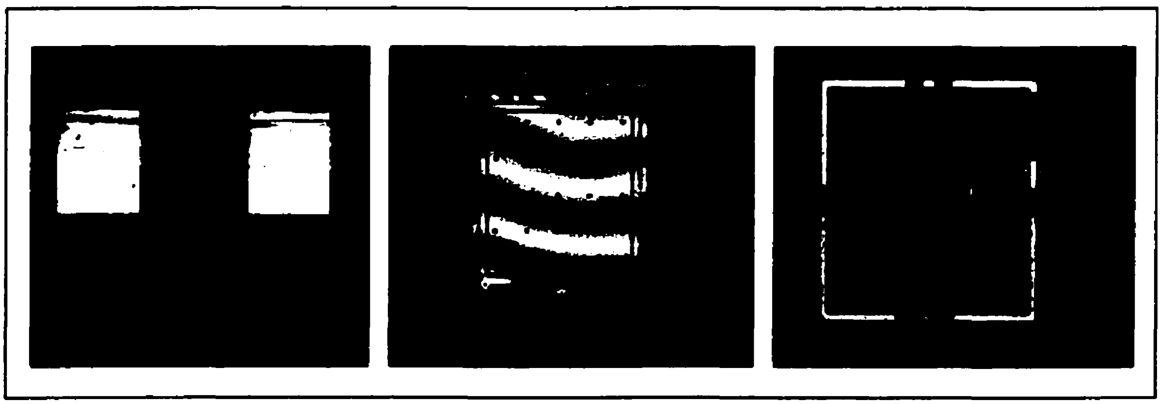


Figure 31. Devices showing signs of debris and other defects

Using an interferometer, the surfaces of the device are also examined for signs of stiction. This was accomplished by fitting a special interferometric objective onto an optical microscope, effectively transforming it into a compact Mirau interferometer; the layout of this interferometer is shown in Figure 32 and is very similar to that of a folded Michelson interferometer.

The interferometer is then lowered towards the surface of the device until the length of the test arm below the beamsplitter plate is almost exactly the same as that of thereference arm above the beamsplitter plate. At this point, light from the two arms will interfere constructively and destructively when recombined, causing a distinctive pattern of light and dark fringes to appear. By focusing on areas where the fringe pattern is very closely spaced, potential problems with stiction can be identified. For example, Figure 33a shows a structure with many closely spaced fringes on the supporting arms of the mirror. Since closely spaced fringes are an indication of a highly tilted surface, it can be assumed that the central portion of the mirror has been pulled down toward the substrate. This was later verified using a scanning electron micrograph (SEM), as shown in Figure 33b.

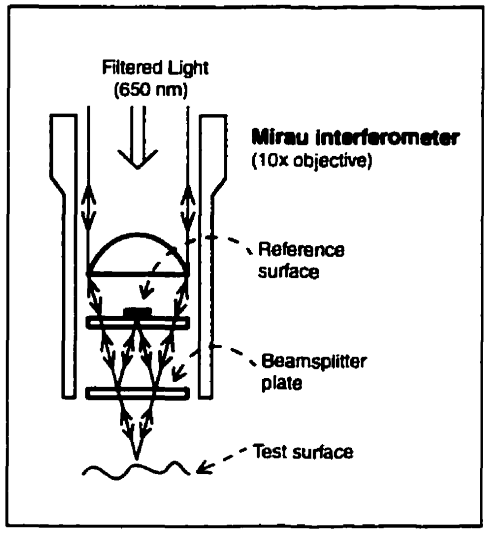
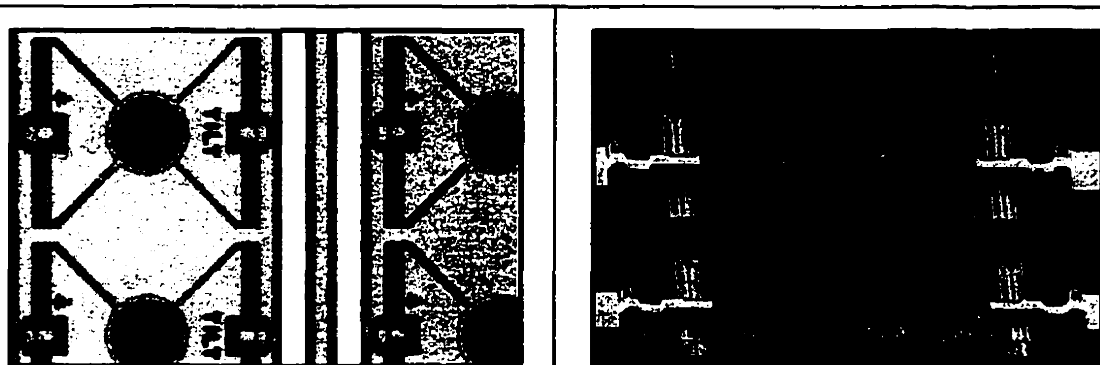


Figure 32. Mirau interferometer.



a) Fringe Image | **b) SEM Photo**

Figure 33. Results of visual inspection for thermally-actuated mirror devices.

7.2 Surface Roughness & Curvature Measurements

To evaluate the surface roughness and curvature of the mirror, the static Mirau interferometer described in Section 7.1 was transformed into a phase-shifting interferometer. This can be done by mounting the Mirau objective on to a piezoelectric transducer (PZT) which can shift the objective up and down in very small increments, thereby introducing small phase shifts in to the fringe pattern [85]. The schematic for this setup is shown in Figure 34.

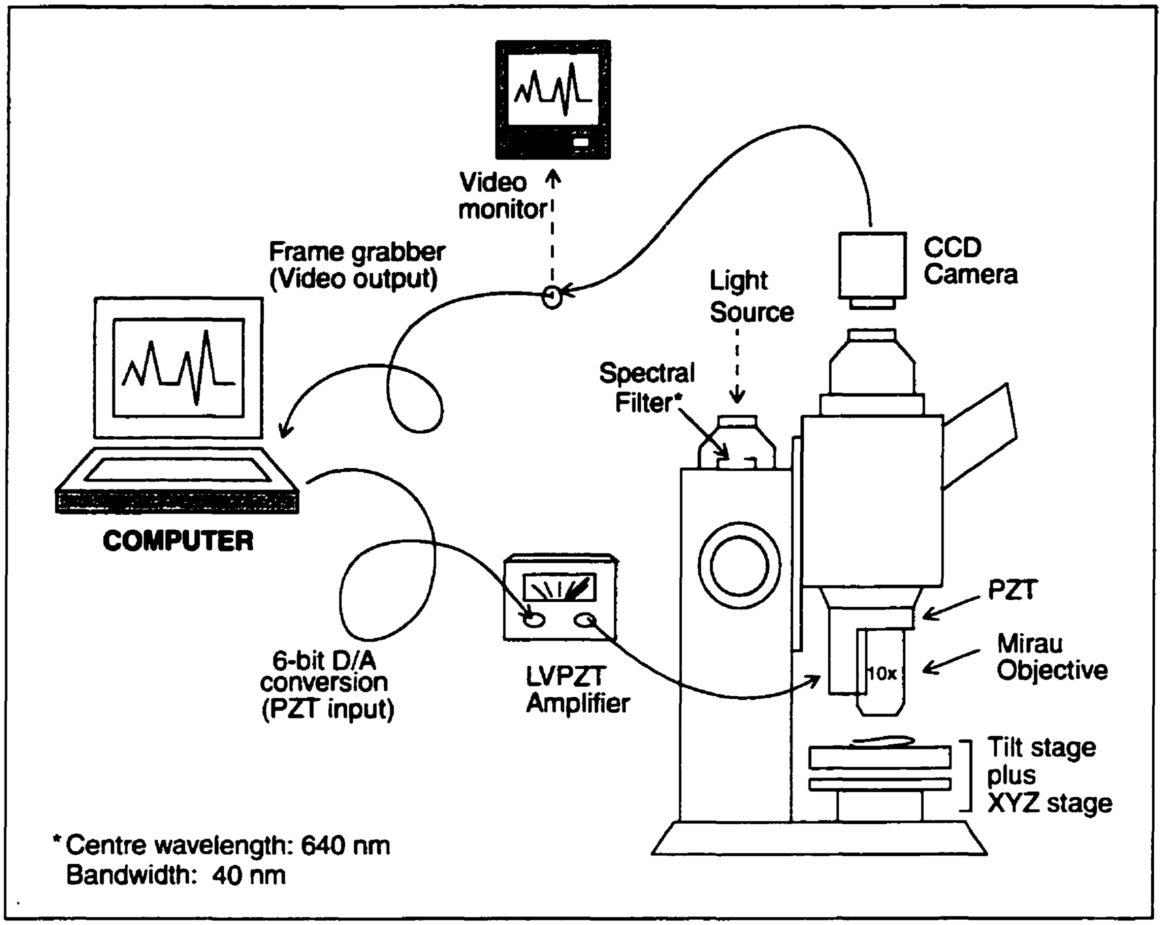


Figure 34. Setup for phase-shifting Mirau interferometer.

Again, by lowering the objective to exactly one working distance above the test surface, white light fringes can be observed, filtered, and captured using a CCD camera. Using the PZT, the path length of the test arm can be increased or decreased slightly to induce a small phase-shift in the fringe pattern. The resulting set of images can then be analyzed using phase-shifting algorithms, such as the five-bucket integration scheme [86], and the surface profile calculated from these results [87]. From this profile, the curvature of the mirror can also be calculated. In addition, statistics such as the peak-to-valley and rms values for the mirror surface can be used to provide an indication of the surface roughness of the device. All fringe acquisition and analysis procedures were coordinated using IntelliWave, a commercial interferometry software package produced by Engineering Synthesis Design, Tuscon, Arizona. The accuracy of the heights profiled was calibrated using a step-height standard purchased from VLSI Standards, San Jose, California.

Finally, if the surface profile were transferred to another program such as MATLAB — a mathematical tool produced by Mathworks in Natick, Massachusetts — other parameters for the surface roughness could also be calculated. This would include parameters such as the rms slope, summit density, autocorrelation function, and power spectral density for the surface [88]. However, since a full characterization of the surface roughness of the device was of lesser importance to the research interests of the Photonic Systems Group, these calculations were omitted from this investigation.

7.3 Reflectivity Measurements

The reflectivities of the different mirrors were measured using a separate setup located at the output of a monochromator. By using a monochromator, the reflectivity of the mirror at different wavelengths could be evaluated. This is especially useful for determining the influence of etalon effects on the reflectivity of the surface under test. The schematic for this setup is shown below in Figure 35. This setup was originally developed by M. Ayliffe for his Ph.D. work at McGill University [89].

Before entering the monochromator, the input light is broken up into a series of pulses by a rotating chopper, whose frequency is controlled by the DSP lock-in amplifier. Light entering the main arm of the setup is then focussed on to the sample through a series of lenses (L_1, L_2, objective lens). The spot size of the focussed beam is approximately 30 μm. The reflected light is then redirected to the output port (A) through the use of a beamsplitter. Two photodetectors are used to monitor the power of the reflected beam and the power of the incoming beam at point B. Since the power in these beams is on the order of picoAmperes, the output currents of the photodetectors are amplified using the lock-in amplifier, which locks in to the frequency of the light pulses generated by the chopper. This allows for a very accurate measurement of the output signal, with greater immunity to noise. To calibrate this setup, measurements are first taken using a reference mirror, which has a known reflectivity of greater than 99%. The output current for the test sample can then be compared to this value.

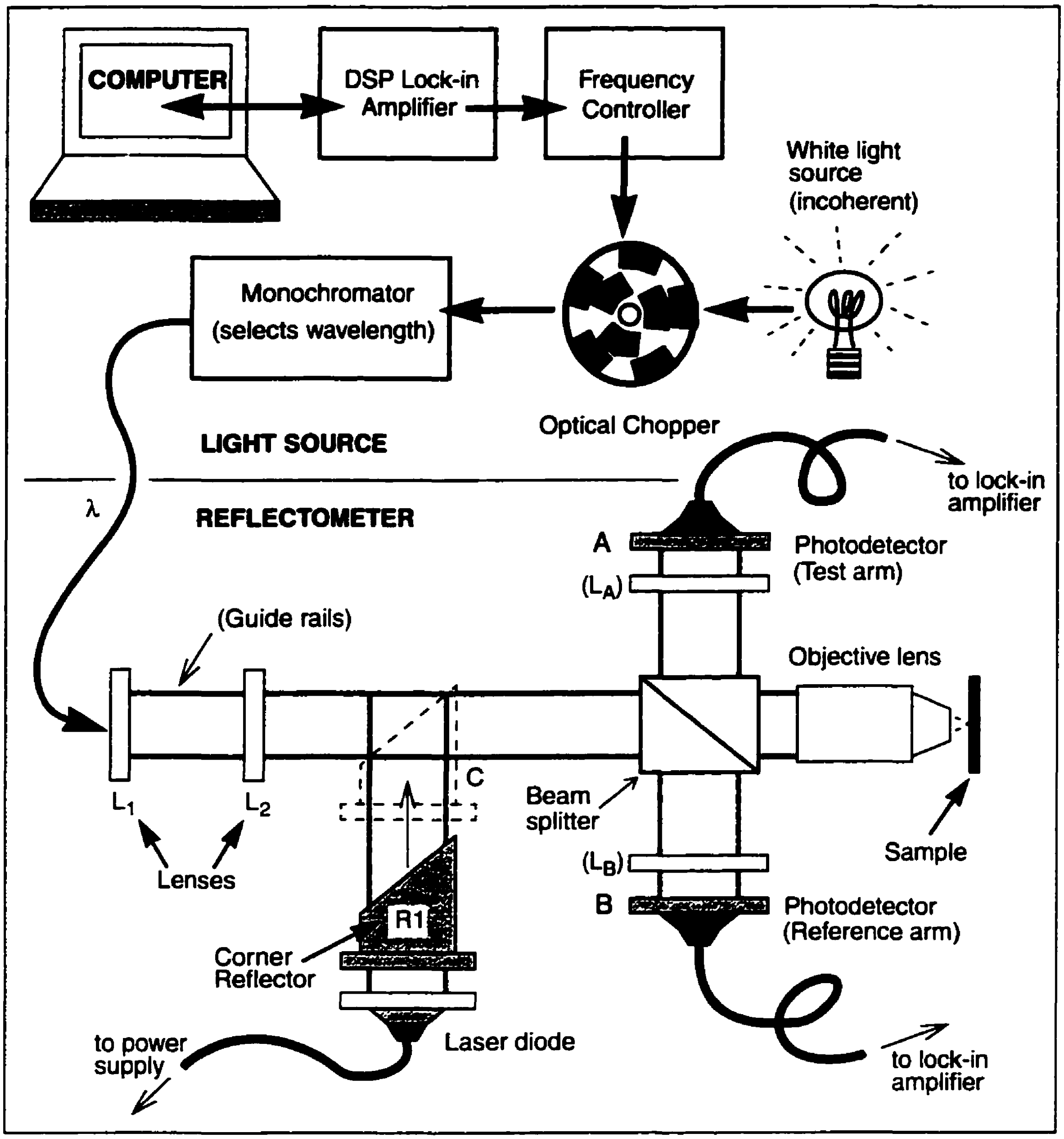
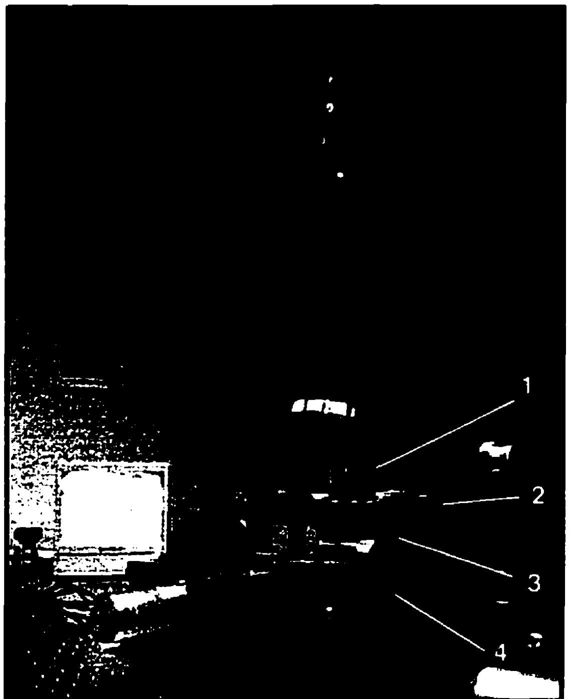


Figure 35. Experimental setup for reflectivity measurements

NOTE: In order to adjust the position of the spot on to the test surface accurately, the laser diode in the auxiliary arm (C) of the setup can be used. By replacing the photodetector at point A by a CCD camera, the image of the light reflected from the sample can be monitored visually. However, since the diameter of the spot illuminated by the monochromator is very small, a second light source is needed to illuminate the whole field of view. Thus, by moving the corner reflector (R1) into the path of the main test arm, light from the laser diode can be redirected toward the sample and used to illuminate the sample more fully. This allows for the proper positioning of the spot on to the surface under test.

7.4 Active Device Behaviour

Finally, to test the active behaviour of the device, the chips are either probed directly using a probing microscope or are wirebonded in to a printed circuit board, custom-made for this purpose [76] [90]. In both cases, the mechanical behaviour of the device can be characterized by examining the chip using the phase-shifting Mirau interferometer described in Section 7.2. To accomplish this, the chip carrier or the printed circuit board is first bolted to a tilt stage which, in turn, is bolted to the XYZ-platform of the optical microscope. The tilt stage is then used to manipulate the sample so that the device under test will lie perfectly flat with respect to the optics in the interferometer; this facilitates the analysis of the mirror surface. Figure 36 shows a picture of this setup.



1. PZT and Mirau objective. **2.** PCB board. **3.** Tilt stage. **4.** XYZ platform.

Figure 36. Setup to test active MEMS devices.

Voltages are brought on to the board through the use of ribbon cables, which are connected to the appropriate power supplies (not shown). As voltages are applied to the mirror device, the top surface of the mirror deforms itself accordingly. Thus, by capturing the fringe data generated as the voltage is varied, the mechanical behaviour of the device can be measured.

8.0 EXPERIMENTAL RESULTS

The completed chips for the MTC and MM2 fabrication runs were received from CMC on June 27, 2000, and March 6, 2001, respectively. Using the setups described in Section 7.0, the micromirror devices on these chips were tested. However, due to the large number of devices implemented, not all devices could be characterized in full detail. Thus while all devices were probed to check the behaviour of the devices when actuated, quantitative results were only collected for three of the seven mirror types: Mirror E2, Mirror G, and Mirror T. These three mirror designs were chosen based on the type of motion associated with the designs, namely rotational, which was judged to be of the most immediate benefit to the research interests of the Photonic Systems Group; the application envisioned being the area of optical switches for large-scale optical interconnects. The results of this analysis are discussed in Section 8.6. Sections 8.1 to 8.5 outline the preliminary results obtained for the five families of mirrors: Mirror DM, Mirrors Th1 and Th2, Mirrors E1 and E2, Mirror G, and Mirror T.

8.1 Results from Family I: Mirror DM

8.1.1 Visual Inspection

Figure 37 shows a scanning electron micrograph (SEM) of one of the metallized deformable membrane mirror devices fabricated on the McGill Test Chip (MTC). Due to the size of the mirror, only a close-up of the lower right-hand corner of the mirror is shown in this image. Three of the nine electrostatic actuators used for the mirror are clearly visible on the right-hand side; they are only partially covered by the mirror surface, which is the brighter surface extending to the left of the picture. The central post for one of the actuators can be seen as a square depression in the centre of the picture.

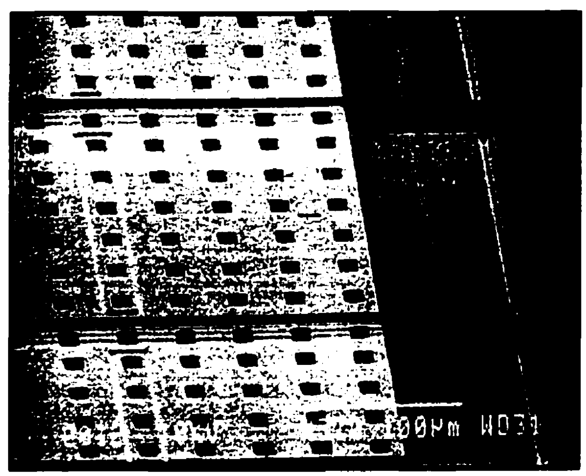


Figure 37. SEM Photo of Mirror DM

When viewed using the Mirau interferometer, the effect of residual stresses on the top surface of the mirror are apparent. Figure 38 shows images of the fringes captured using a CCD camera. Not surprisingly, the shape of the fringes show that the surface tends to dip periodically, coinciding with the location of the support posts below the mirror. The fringes also show that the surface has a tendency to roll off toward the edges of the mirror, which are unsupported. Thus, when using this device, the control scheme for the mirror would have to be adjusted, in order to account for these deformities

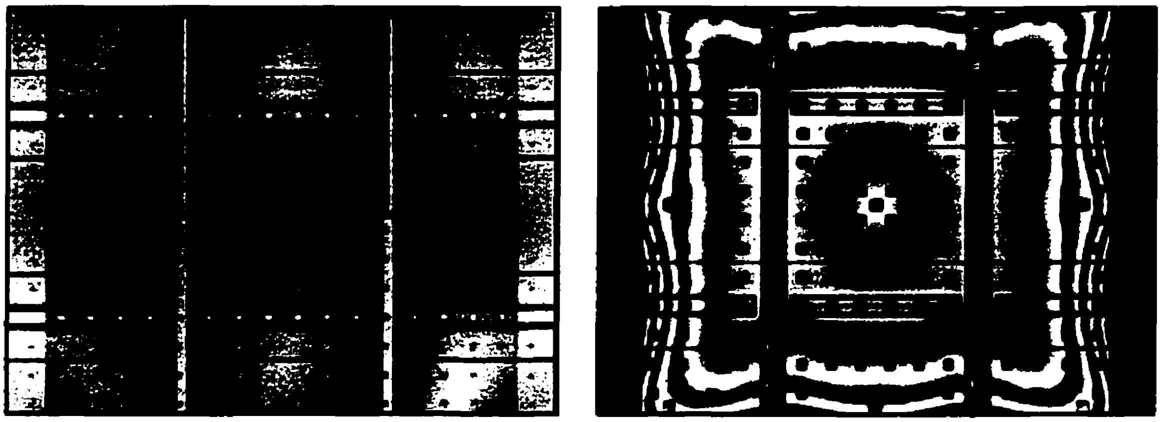
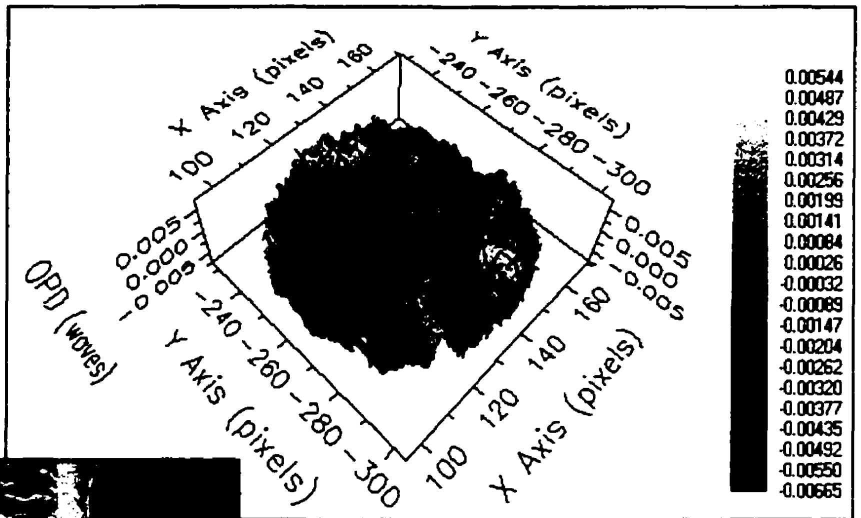


Figure 38. Static fringe images of Mirror DM. **Left:** Plain surface. **Right:** Metallized.

8.1.2 Surface Roughness

To evaluate the surface roughness of the mirror, the profile of the surface was measured using the phase-shifting Mirau interferometer described in Section 7.2. By examining a small enough section of the mirror, the tilt and curvature of the section could be eliminated and the surface roughness gauged by looking at the rms and peak-to-valley values for the surface. Figure 39a shows a close-up of the resulting profile. In this case, the rms roughness and peak-to-valley range for this section of the mirror were 0.544 nm and 3.87 nm, respectively. For comparison, Figure 39b shows a close-up of the metallized mirror surface, as seen using a scanning electron microscope.



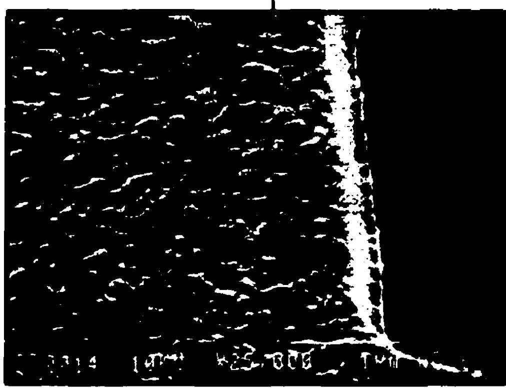


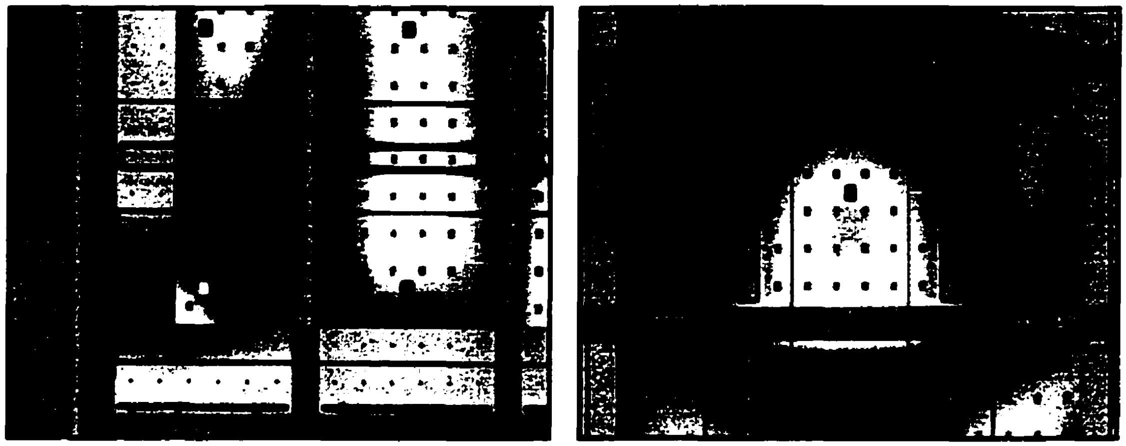
Figure 39. Surface profile of Mirror DM.

Top: Surface profile, showing closeup of top surface for Mirror DM.

Left: SEM photo, showing closeup of metallized surface, near an etch hole.

8.1.3 Active Behaviour

To test the active behaviour of the device, voltages in the range of 30 to 75 V were applied to the electrostatic actuators located beneath the surface of the mirror. Using the static Mirau interferometer, the effect of the actuators could be monitored by observing the change in fringe patterns on the mirror surface. As expected, applying voltages to the actuators caused small valleys to appear in the areas surrounding the posts for each actuator. Experimentally, it was determined that voltages in the range of 30-50 V are needed for the actuator to begin its deflection downward. Figure 40a shows a corner actuator that is in this early stage of deflection. At 60 V, the rate of deflection versus input voltage increases dramatically, with full deflection achieved at voltages in the range of 70-75 V. Finally, for voltages greater than 75 V, permanent deformities in the mirror surface are obtained; an example of this is shown in Figure 40b.



a) Corner: Deflection for 50 V   b) Centre: Permanent deformity after 75 V

Figure 40. Static fringe images of Mirror DM

8.2 Results from Family II: Mirrors Th1 and Th2

8.2.1 Visual Inspection of McGill Test Chip

The thermally-actuated micromirrors from the McGill Test Chip were first inspected visually using the static Mirau interferometer. Figure 41a shows an image of a typical fringe pattern generated by this setup. The presence of many dark and light fringes on the arms of the mirror suggests that the arms are highly tilted. This in turn suggests that the mirror has collapsed down toward the substrate, possibly due to problems with stiction or with residual stresses in the structure during the release process. To confirm this condition, the device was examined using a scanning electron microscope; Figure 41b shows an SEM photo of the device. As suspected, this photo clearly shows the bent nature of the mirror's arms, preventing it from proper operation.

8.2.2 Effect of Design Modifications from McGill MEMS 2

Since many of the thermal mirrors from the original MTC run showed signs of collapse, additional design modifications were trialed on the second test chip, McGill MEMS 2 (MM2). While certain problems with the manufacturing process were observed on this fabrication run (see Section 8.5.1), the mirrors from this family of designs appeared to be the least affected, possibly due to the small size of the mirror surface. Thus, the effective-

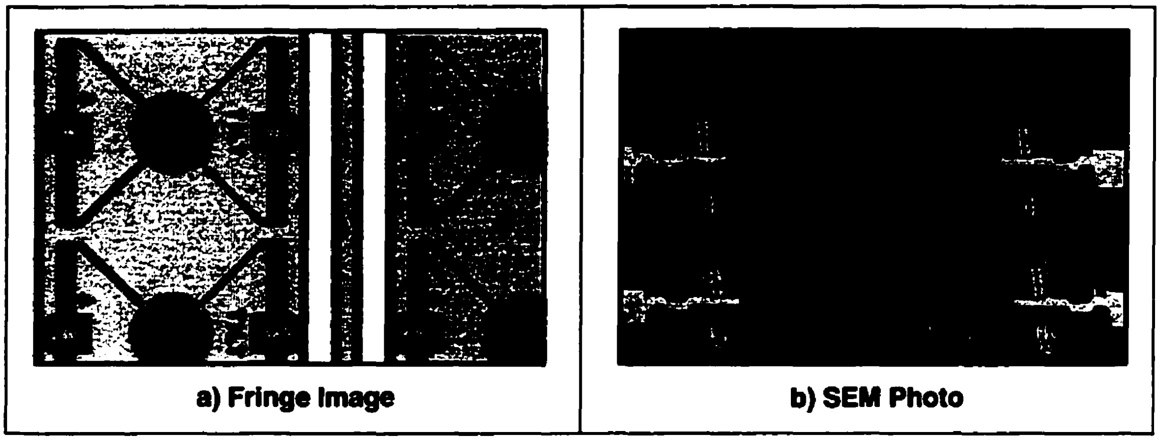


Figure 41. Results of visual inspection for thermally-actuated mirror devices.

ness of each design modification was evaluated by examining the yield obtained for each of the different design modifications.

By far, the best yield was observed for mirrors with shortened support arms — namely designs "Th1_BIG" and "Th1_BIGm" — with a yield of 100%. An SEM of the improved mirror device is shown in Figure 42. From this picture, the gap between the substrate and the top surface of the mirror is clearly visible. Thus, unlike the original design, the arms for this mirror design show little signs of buckling.

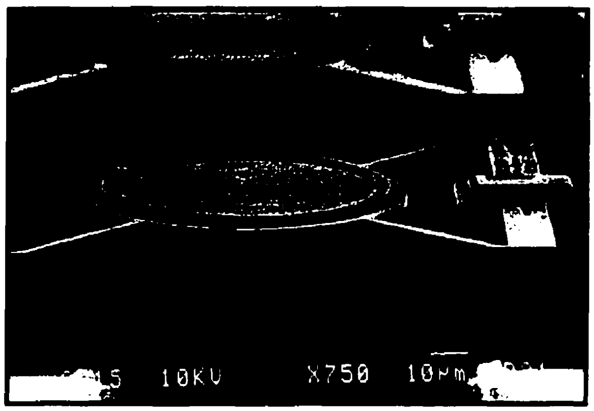


Figure 42. SEM Photo of Mirror Th1_BIG

Similarly, mirrors fabricated with a Poly0 former also showed a much better yield than its counterparts, with a combined yield of 97.8%. Although the reason for this is not entirely clear, it is possible that the Poly0 former influences the distribution of residual stresses in the polysilicon arms, making them less likely to curve downward when the structure is released. Consequently, in addition to the length of the support arms, the residual stresses in the mirror structure can also be seen to play an important role in the proper manufacturing of this design.

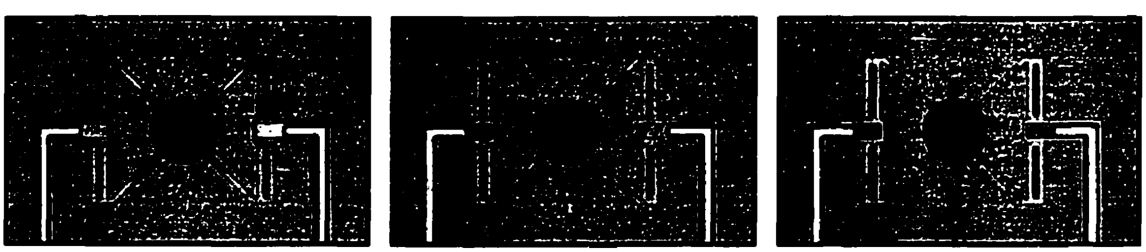
Finally, to complete this discussion, it should also be noted that designs composed of a single layer of polysilicon — either Poly1 or Poly2 — showed about the same yield or lower as those fabricated with a double thickness of polysilicon. The corresponding yields for the seven types of devices are summarized in Table 10.

TABLE 10: Summary of Device Yield for Family II

Device Name(s)	Description	Yield MM2
Th1, Th1m	Original piston mirror design	43.3%
Th1_p0, Th1m_p0	Piston mirror, with Poly0 former	100%
Th1_BIG, Th1_BIGm	Piston mirror, with wider central mirror and shorter support arms	100%
Th1_p1	Piston mirror, with single thickness (2.0 μm) of polysilicon	43.3%
Th1_p2, Th1_p2m	Piston mirror, with single thickness (1.5 μm) of polysilicon. Also: Gap increased to 2.75μm.	27.8%
Th2	Original tilt mirror design	33.3%
Th2_p0	Tilt mirror, with Poly0 former	93.3%

8.2.3 Active Behaviour

To test the active behaviour of this mirror, currents in the range of 0 to 8 mA were applied to the device. The vertical deflection of Mirror Th1 was estimated by counting the number of fringes that appeared on the arms supporting the central portion of the mirror. Figure 43 shows a sequence of some of the images taken during the testing of Mirror Th1_p1. This is a piston-type mirror, with a centre mirror composed of a single thickness of polysilicon, namely Poly1. The maximum deflection for this mirror was estimated to be 1.8 μm.



Current = 5.0 mA   Current = 6.0 mA   Current = 8.0 mA

Figure 43. Sequence of fringe images for Mirror Th1_p1 (Poly1, piston mirror)

8.3 Results from Family III: Mirrors E1 and E2

8.3.1 Visual Inspection of McGill Test Chip

Figure 44b shows an SEM of the electrostatically-actuated piston mirrors fabricated on the McGill Test Chip. While the mirror in the centre of the photo has a metallized surface, the mirror directly below it has a non-metallized surface; the difference in reflectivity between the two surfaces is clearly visible from this photo.

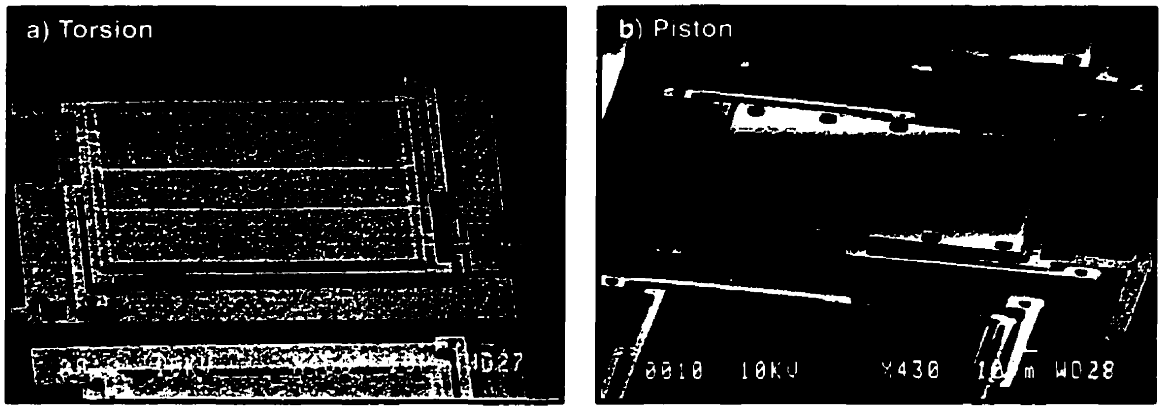


Figure 44. SEM photos for Mirror E2 (left) and Mirror E1 (right)

Aside from the difference in reflectivities between the two surfaces, another obvious difference was observed when the mirrors were viewed using the Mirau interferometer. Figure 45 shows the corresponding fringe patterns for the two types of mirrors. The image on the left corresponds to a mirror with a non-metallized surface, whereas the image on the right corresponds to one with a metallized surface. The presence of circular fringes in the image on the right clearly indicate the curved nature of the metallized sur-

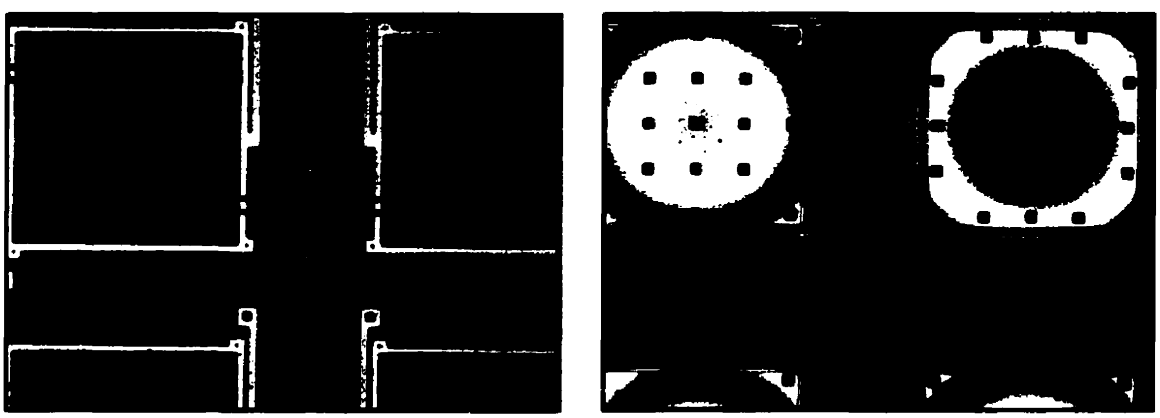


Figure 45. Static fringe images for Mirror E. **Left:** Non-metallized. **Right:** Metallized

face, as compared to the non-metallized surface. This is due to the extra stresses induced by the metal on top of the mirror surface. The curvature of the two types of mirrors is characterized in more detail in Section 8.3.3.

8.3.2 Visual Inspection of McGill MEMS 2

As explained in Section 5.3.2, a number of variations on Mirror E were trialed on the second test chip, McGill MEMS 2. In particular, a number of mirrors with only a single thickness of polysilicon as its top surface were included on this chip. However, due to the decrease in rigidity of the upper surface, many of these single-thickness devices came back malformed. Figure 46 shows a sample of the fringe images captured from these devices.

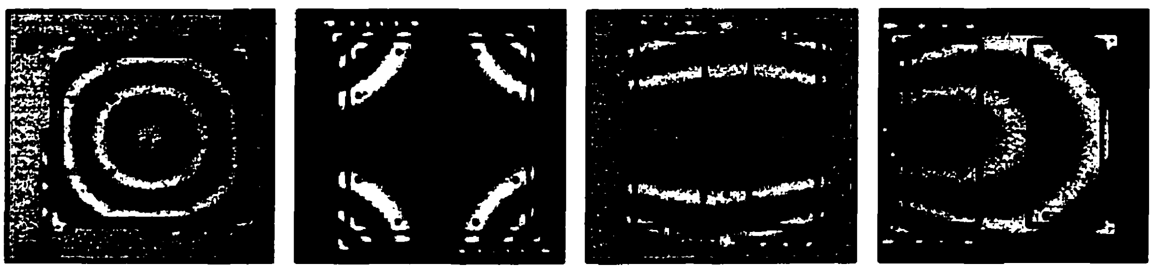


Figure 46. Typical malformations observed for single-thickness devices from Family III

Finally, although a number of malformations were also observed for the double-thickness structures, the total number of malformations for the double-thickness devices was still considerably lower than that for the single-thickness devices. As a comparison, the production yield for the different design variations are summarized in Table 11 below.

TABLE 11: Summary of Device Yield for Family III

Device Name(s)	Description	Yield MM2
E1	Original piston mirror design	73.3%
E1_p1	Piston mirror, with single thickness of polysilicon	35.0%
E2	Original tilt mirror design	85.0%
E2_p1	Tilt mirror, with single thickness of polysilicon	43.3%

TABLE 11: Summary of Device Yield for Family III (Continued)

Device Name(s)	Description	Yield MM2
E2_h2	Tilt mirror, with modified hinge structure	90.0%
E2_h2p1	Tilt mirror, with modified hinge structure and single thickness of polysilicon	43.3%

8.3.3 Surface Reflectivity and Curvature

The reflectivity of the mirror surface was measured using the setup described in Section 7.3. For a wavelength of 850 nm, the reflectivity of the non-metallized mirror was measured to be 53%, whereas the reflectivity of the metallized mirror was 91%. Thus, as expected, the reflectivity of the mirror surface was greatly improved by the addition of the metal layer.

However, this improvement came at the cost of another important consideration: curvature. Due to the lack of annealing steps after the deposition of the metal layer, the amount of residual stresses in the metallized surface was much higher than that of the non-metallized surface alone. As a result, when the metallized structure was released, the surface of the mirror sagged downward to a much greater degree than that of the non-metallized surface. Figure 47 shows the corresponding surface profiles for the two torsional mirrors, Mirror E2 and Mirror E2m. From these profiles, the corresponding sag for the

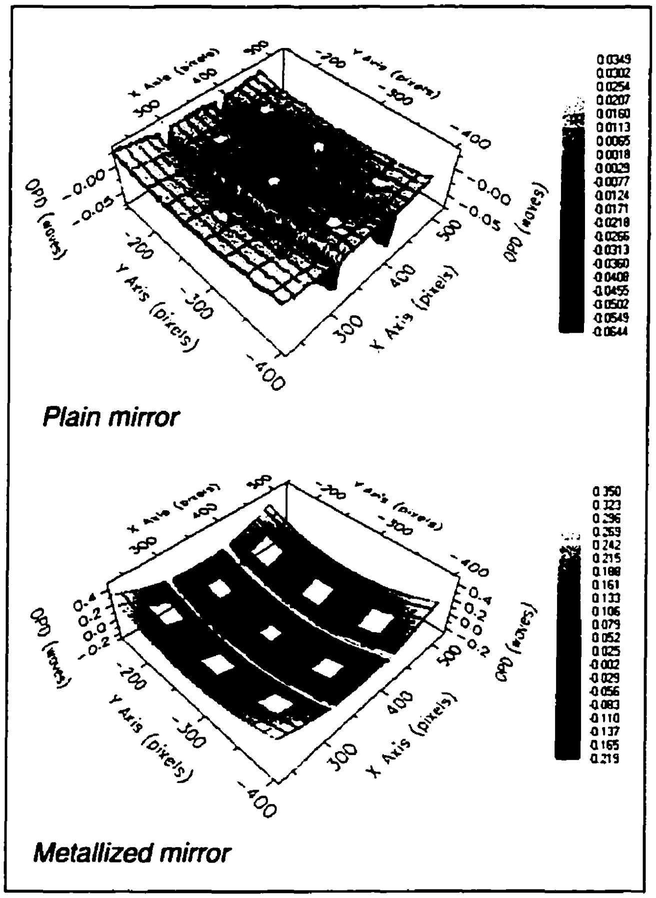


Figure 47. Surface profiles for Mirrors E2 & E2m

metallized surface was measured to be 0.37 μm, whereas the sag for the non-metallized mirror was measured to be merely 0.065 μm.

8.3.4 Active Behaviour

A. Piston mirror

To test the active behaviour of Mirror E1, voltages in the range of 0 to 20 V were applied to the device. As with the thermally-actuated piston mirror, the vertical deflection of the mirror was estimated by counting the number of fringes that appeared on the flexures supporting the mirror. Figure 48 shows a sequence of the images taken during the testing of Mirror E1_p1, which is a piston mirror with a top surface composed of a single thickness of polysilicon, namely Poly1. The maximum deflection of this mirror was estimated to be approximately 1.1 μm for a voltage of 15.0 V.

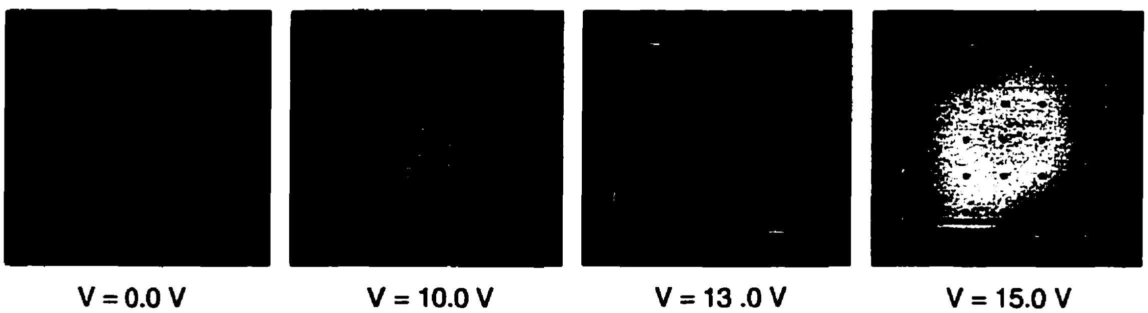


Figure 48. Sequence of fringe images captured for Mirror E1_p1 (Poly1, piston mirror)

B. Torsion mirror

On the other hand, the pull-in voltages for the torsional mirror design, Mirror E2, were found to vary from 8 V to 17 V, which is similar to the theoretical value calculated in Section 6.3. Figure 49 shows a sampling of the fringe images captured using the CCD camera. The top sequence corresponds to the motion of a plain mirror, without a top layer of metal, whereas the bottom sequence corresponds to the motion of a metallized mirror. Both mirrors are rotating toward the south terminal, located at the bottom of the images.

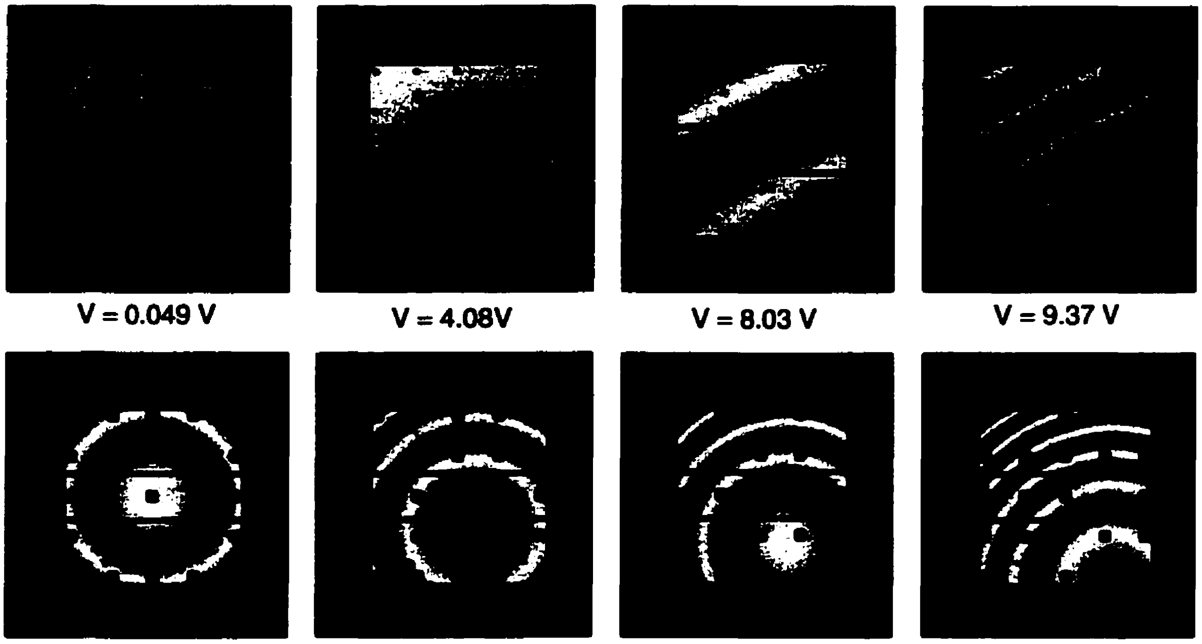


Figure 49. Sequence of fringe images for Mirror E2. **Top:** Plain. **Bottom:** Metallized.

From these images, an important observation can be made. Since the surface of the mirror was first nulled — that is, the tilt component was removed from the initial image of the mirror at rest — the direction of the fringes in later images indicates the direction in which the mirror is tilting. In this case, the fringe images clearly show that the mirror is tilting diagonally toward the bottom right corner of the mirror, instead of tilting uniformly toward the south terminal.

The most likely cause of this asymmetry lies in the asymmetry of the two hinges supporting the mirror surface: Although the two hinges are physically identical, one is positioned with its anchor to the lower left, whereas the other is positioned with its anchor to the upper right. As a result, tilting the mirror in a certain direction will cause one hinge to bend forward smoothly, whereas the second hinge will be forced to twist back upon itself to comply with the motion of the mirror. Since it is much easier for a flexure to bend forward than it is for it to twist backward, the spring constant for the former will be much lower than the latter. Consequently, when actuated, the mirror will have a tendency to tilt toward the flexure with the lower spring constant, as was observed experimentally.

To confirm this hypothesis, tests were performed on the modified hinge design included on the second chip, McGill MEMS 2 (see Section 5.3.2). Figure 50 shows a sequence of the fringe images captured for this design. As these images clearly show, the modified spring structure allows the mirror to tilt evenly in a single direction, in this case south. The pull-in voltage for the south terminal was approximately 7.0 V, whereas the pull-in voltage for the north terminal was closer to 6.2 V. Again, this difference in pull-in voltages emphasizes the difference in the two spring constants for the flexures when excited using the two different types of motion.

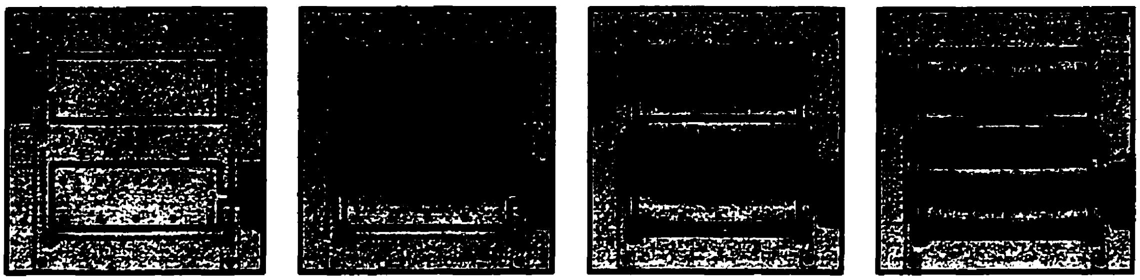


Figure 50. Sequence of fringe images captured for Mirror E2, with modified springs

On the other hand, a large variation in pull-in voltages was also observed for the mirrors on the McGill Test Chip. The pull-in voltage for the upper electrode varied from 15-17 V for mirrors with and without a top layer of metal, whereas the pull-in voltage for the lower electrode varied from 8-10 V for the same set of mirrors. This time, however, the cause of the asymmetry was traced back to asymmetries in the wiring of the control electrodes, caused by the presence of debris bridging certain parts of the electrical path; this situation is illustrated in Figure 51 and was confirmed by the presence of a small leakage current observed during testing. With the debris creating a closed circuit for the voltage supply, the whole circuit acts as a simple voltage divider. Consequently, depending on the resistance of the debris, only a fixed fraction of the voltage supplied by the source will be transmitted to the terminals of the mirror. Thus,

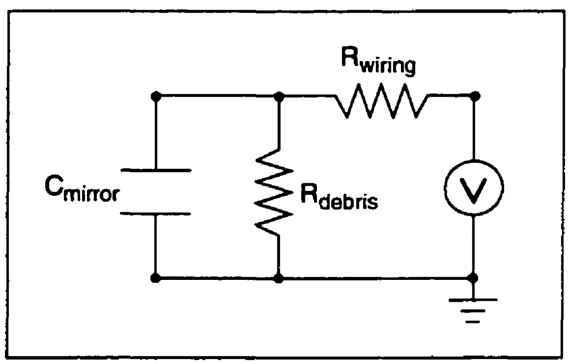


Figure 51. Effect of debris on Mirror E2

the amount of voltage needed from the source to satisfy the pull-in condition will vary according to this fixed fraction, however the voltage seen by the mirror will remain the same.

Figure 52 shows the characteristic voltage curves for the two mirrors. The graphs on the left show the tilt of the mirrors as a function of the source voltage, V_s. However, in order to better compare the voltage characteristics for the north and south directions simultaneously, the graphs have been replotted on the right as a function of the normalized voltage, V_{norm}; this eliminates the effect of the voltage divider described earlier. As expected, the two normalized curves for the north and south directions lie directly on top of each other; this was expected due to the radial symmetry of the mirror design.

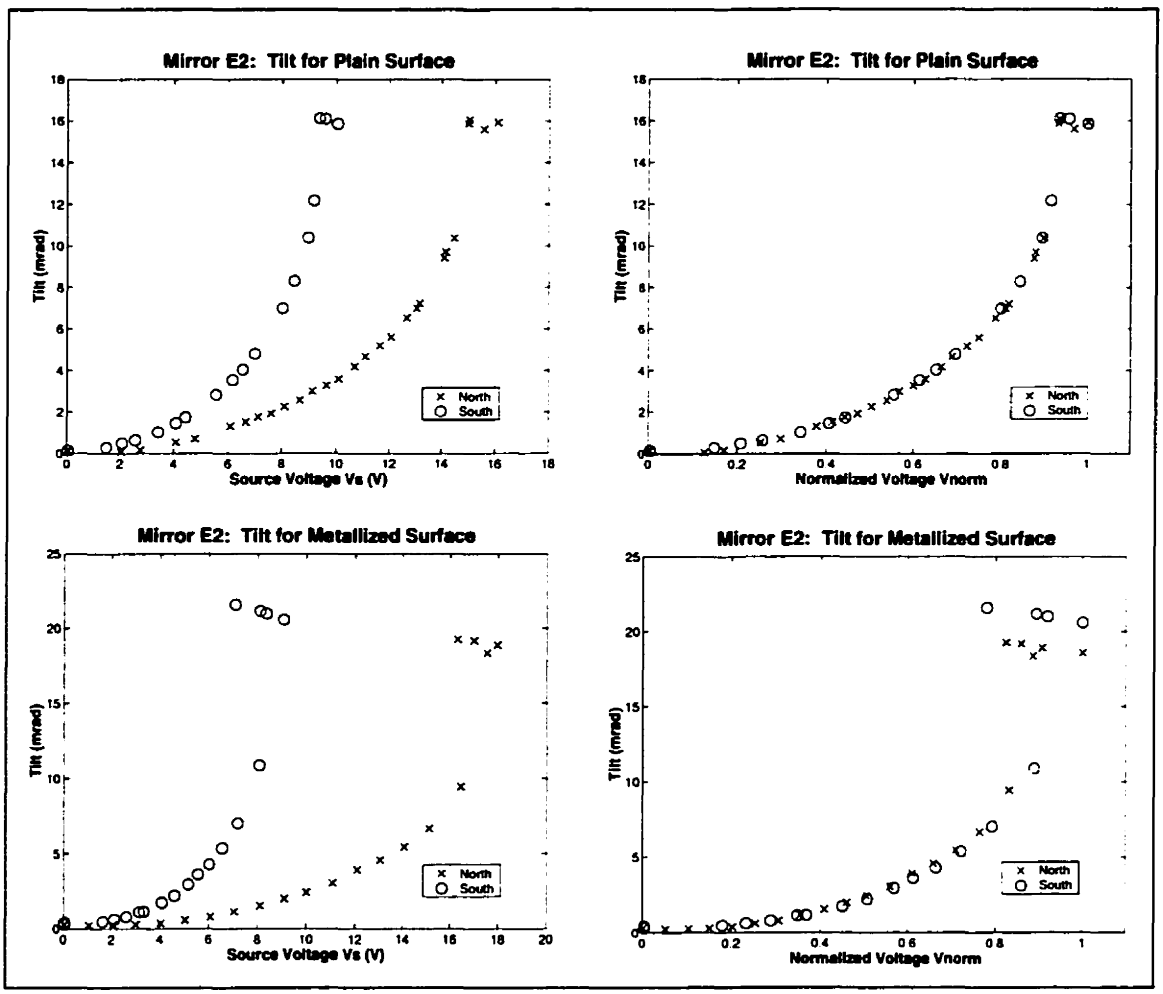


Figure 52. Voltage characteristics for Mirror E2.

In addition, Figure 52 also highlights another interesting disparity: although the characteristic curve for the non-metallized mirror is very smooth and shows little signs of hysteresis, the voltage characteristic for the metallized mirror is more abrupt and displays greater signs of hysteresis. One possible explanation for this disparity is the increase in curvature of the metallized surface versus that of the non-metallized mirror. As a result of this curvature, more of the top mirror surface will be at a lower vertical height than expected, thus increasing the electrostatic torque experienced by the mirror surface. Consequently, the critical angle for the mirror — that is, the angle where the electrostatic torque overcomes the mechanical torque for the mirror — is reached at a slightly lower voltage. By the same reasoning, the release voltage for the mirror is also affected and this in turn explains the lower voltages required to return the mirror to its initial position on the voltage characteristic.

Finally, from the results of this analysis, it is clear that this design would be very effective as an analog mirror for deflections in the range of 0-16 mrads, however its use as a digital mirror would be limited. The voltages required to control this mirror's deflection would be in the range of 0-10 V.

8.4 Results from Family IV: Mirror G

8.4.1 Visual Inspection

Figure 53 shows an SEM photo of Mirror G. As expected, a large cross-like indentation can be seen in the centre of the mirror surface; this is due to problems with print-through. However, by comparing the surface of this mirror with that of Mirror E2 (see Figure 44), it is clear that the width of the gap in between the electrodes can play a significant role in improving the planarity of the top surface. Thus, one way of reducing the prominence of the surface indentations would be to

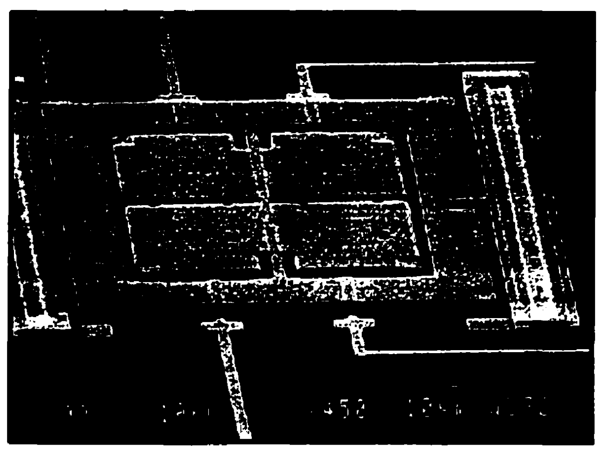


Figure 53. SEM photo of Mirror G

reduce the spacing of the electrodes beneath the surface of the mirror to its minimum value, namely 2.0 μm, instead of using the larger value of 5.0 μm.

8.4.2 Active Behaviour

To test the active behaviour of this mirror, voltages in the range of 0 to 27 V were applied to the device. The pull-in voltages for Mirror G varied from 21.8 V for motion in the axial direction, to 26.3 V for motion on the diagonal. Motion on the diagonal was created by applying a voltage to only one electrode, as opposed to a pair of electrodes. Figure 54 shows a sampling of the images taken using the CCD camera. The top sequence corresponds to motion in the east direction. The bottom sequence corresponds to motion in the south-east direction.

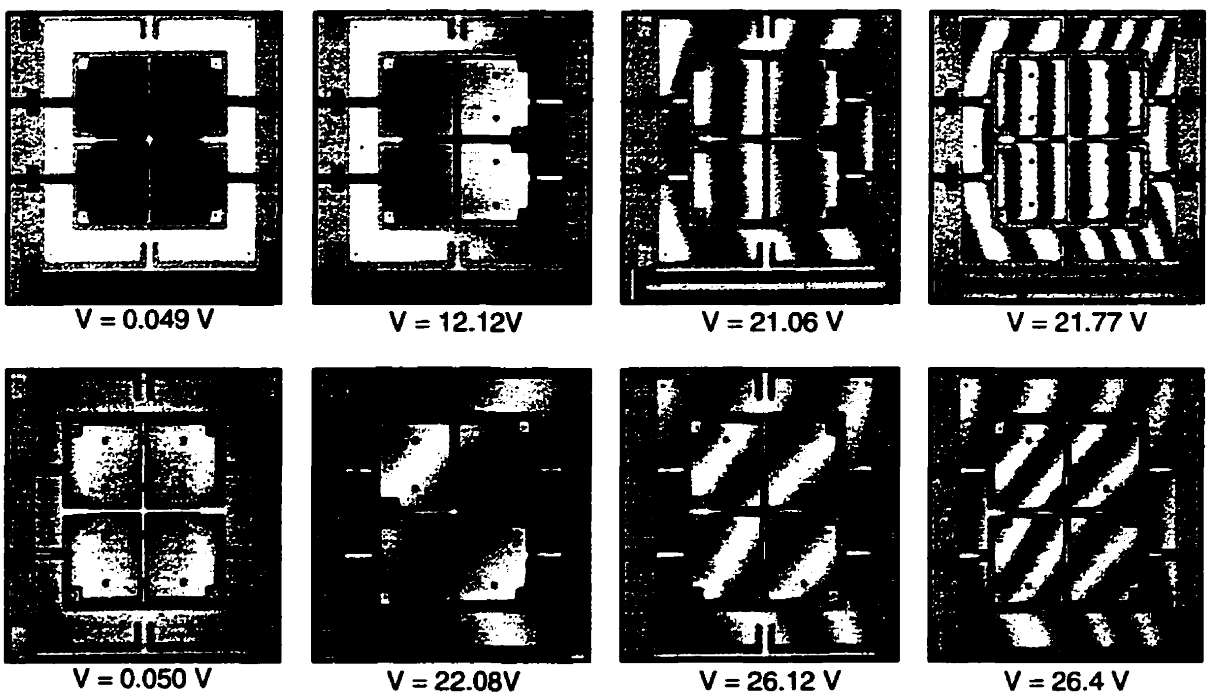


Figure 54. Sequence of fringe images for Mirror G. **Top:** Axial tilt. **Bottom:** Diagonal tilt.

The voltage characteristics for this mirror are displayed in Figure 55. From these graphs, it can be seen that the critical angle of operation for this mirror is approximately 12 mrads. For angles below this value, the mirror can be operated in the analog regime. Past this value, however, the electrostatic torque of the mirror will overcome the mechanical torque of the springs and the pull-in condition will occur. Due to the slight curvature of the mirror surface, the tilt of the mirror at pull-in ranges from 19.2 mrad to 23.2 mrad, depending on the section of the mirror under examination. After reaching the pull-in condition, the voltage would then have to be lowered by 5-10 V in order to return the mirror to the analog regime of operation. This asymmetry is due to hysteresis, which is caused by the temporary adhesion of the mirror surface to the substrate when it reaches the pull-in condition.

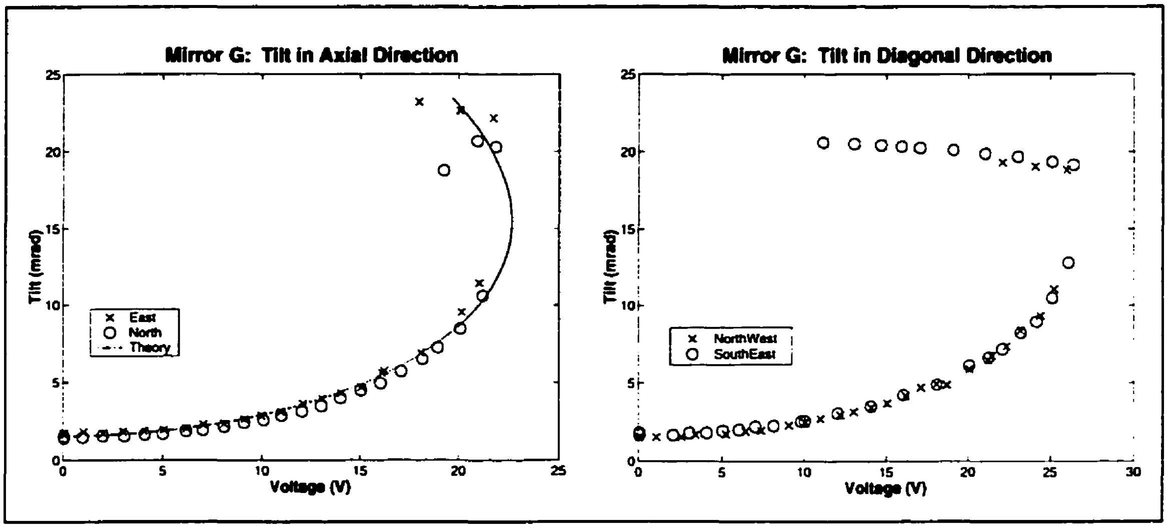


Figure 55. Voltage characteristics for Mirror G.

On the other hand, for digital operation, the mirror would require voltages in the range of 25-30 V to ensure that the pull-in condition was met for all directions of operation, including the four diagonals. Similarly, to ensure the release of the mirror, the voltage would have to be lowered to at least 10 V, although for most directions a drop of 5 V from the pull-in value would suffice. This range of values is probably due to small physical defects, such as a rough edge on the electrode catching the surface of the mirror, or the presence of small particles underneath the surface of the mirror. Nevertheless, in general, the behaviour of this mirror in all eight directions was deemed highly repeatable.

The calibrated values of E needed to fit the experimental data to the theoretical models of Section 6.0 are 163 GPa and 160 GPa for the north-south and east-west directions, respectively. These values correspond to spring constants, K_α, of 4.25×10^{-8} Nm and 4.15×10^{-8} Nm, respectively, which represent percent differences of 2.7% and 5.0%.

8.5 Results from Family V: Mirror T

8.5.1 Visual Inspection of McGill Test Chip & McGill MEMS 2

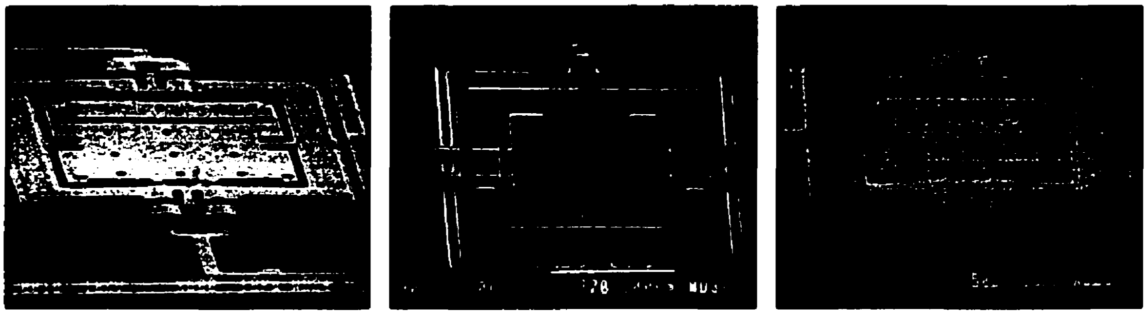


Figure 56. SEM photos of Mirror T. **Left to Right:** Poly1, Poly2, and Poly2 modified.

Figure 56 shows a series of SEM photographs for Mirror T taken from both the McGill Test Chip and the second chip, McGill MEMS 2. As expected, the modifications to the electrode geometry have greatly improved the topography of the surface in the central region of the mirror. This in turn has facilitated the use of this mirror by other students in the Photonic Systems Group for optical setups in the lab [91].

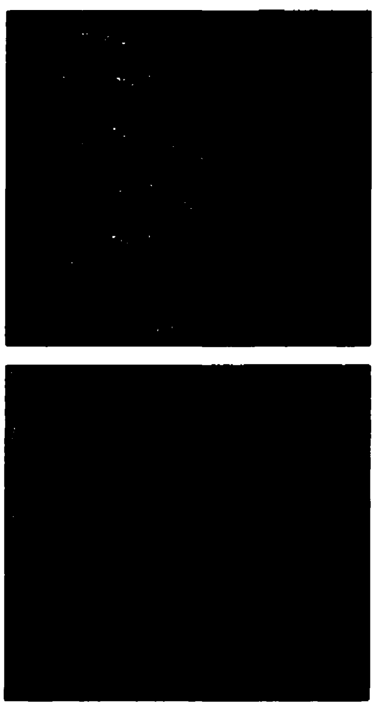


Figure 57. Examples of production flaws for Family V, taken from McGill Test Chip

However, when viewed using the Mirau interferometer, a number of manufacturing problems become apparent. For the McGill Test Chip, a visual inspection of all the devices received revealed that four of the 28 devices fabricated from the Poly1 layer were malformed, and six of the 28 devices fabricated from Poly2 were also malformed. Examples of these malformations, as seen by the Mirau interferometer, are shown in Figure 57. Nevertheless, the overall yield for these designs remained high, at 85.7% and 78.6% for the Poly1 and Poly2 type devices, respectively.

On the other hand, a much higher number of malformations were observed for the devices fabricated on the second chip, McGill MEMS 2. Out of the

201 devices fabricated from the original Poly1 design for Mirror T — that is, Mirror T1p1 — only 45 mirrors were properly formed; this corresponds to a yield of only 22.4%. Similarly, the yield for the Poly2 version of the mirror, Mirror T1p2, was only 6.7%. These numbers are in strong contrast with those obtained for the previous test chip. Figure 58 shows a sample of the fringe patterns captured from this set of faulty mirror devices.

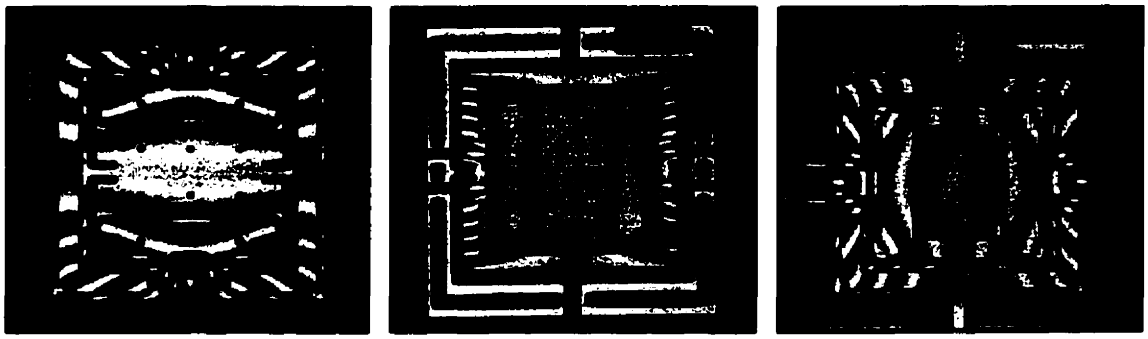


Figure 58. Examples of production flaws for Family V, taken from McGill MEMS 2

From these fringes, it is clear that the majority of the mirrors suffer from the same type of deformity, namely one in which the centre region of the mirror is pulled down in to contact with the substrate. Consequently, the most likely cause of this malformation is problems with stiction during the release process. Alternatively, storing the devices in an environment with a high level of humidity may also produce a similar pattern of collapse for this structure. Both possibilities are currently under investigation so as to prevent future re-occurrences of this problem.

Finally, although most variations of Mirror T yielded poor results, slightly better yields were obtained for two types of mirrors: mirrors with an extra layer of Poly0 beneath the surface of the mirror, and mirrors with a stacked layer of Poly1 and Poly2 on its upper surface. The yields for these devices were 53.3% and 80.0%, respectively. Although the reasons for this improvement in yield are not entirely clear, the latter is probably due to the increase in rigidity of the upper surface, making it less likely to sag, whereas the former may be due to a decrease in the residual stresses of the upper surface, caused by the increase in planarity of the surface topography. The corresponding yield for the different design variations are summarized in Table 12.

TABLE 12: Summary of Device Yield for Family V

Device Name	Description	Yield MTC	Yield MM2
T1p1	Original torsional mirror design for Poly1	85.7%	22.4%
T1p1_slim	Poly1 mirror, with thinner outer walls	—	33.3%
T1p1_b	Poly1 mirror, with extra Poly0 layer	—	53.3%
T1p12	Based on Poly1 mirror, with double thickness of Poly1/Poly2 in centre region.	—	80.0%
T1p2	Original torsional mirror design for Poly2	78.6%	6.7%
T1p2_b	Poly2 mirror, with electrodes modified to prevent stiction	—	11.1%

8.5.2 Surface Reflectivity

The reflectivity of the mirror surface was measured using the setup described in Section 7.3. For a wavelength of 850 nm, the reflectivity of the Poly1 mirror (Mirror T1p1) was measured to be 59.7%. This value, however, was found to vary significantly with the wavelength of the input beam. Figure 59 shows the graph of reflectivity versus input wavelength for Mirror T1p1.

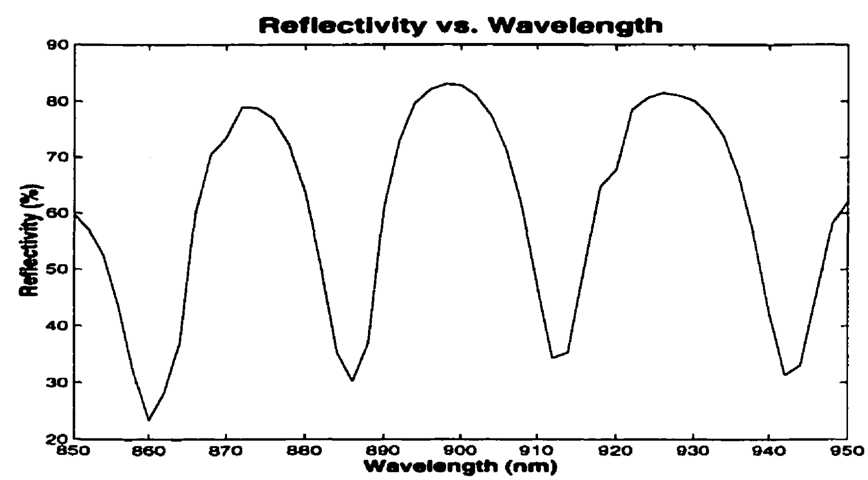


Figure 59. Graph of reflectivity versus wavelength for Mirror T1p1

From the comb-like structure of the graph, it is clear that the surface of the mirror is behaving as an etalon. However, since the period of the comb is only 26.0 nm, the optical path length of the equivalent etalon must be 13.0 nm, which is much smaller than the optical thickness of the polysilicon layers. Thus, this data would seem to imply the existence of a very thin layer — possibly an oxide layer — on top of the polysilicon surface of the mirror. More work is needed, however, to confirm the nature and thickness of this upper layer.

8.5.3 Active Behaviour

To test the active behaviour of these mirrors, voltages in the range of 0 to 30 V were applied to the devices. Unfortunately, during the test procedure for the McGill Test Chip, a new design flaw was observed with the mirrors designed using Poly2. Due to the lack of dimples in the Poly2 layer, mirrors manufactured from this layer experienced problems with stiction during the pull-in condition. More specifically, mirrors that succumbed to the pull-in voltage of the address electrode could not be returned to their initial position, even after the address voltage had been fully removed. In an effort to overcome this difficulty, a new design was trialed on McGill MEMS 2 (see Section 5.3.3). In this design, the corners of the electrodes were notched to form small landing pads for the top surface of the mirror. Unfortunately, when tested, these notches proved to be too shallow for the task and were consequently ineffective at preventing the charge stiction problems from reoccurring with this mirror. Thus, a complete mechanical characterization of both Poly2 designs was not possible and has been postponed for future work. Some possible improvements currently under investigation include the use of the DIMPLE mask to create larger indentations in the Poly2 layer, as well as the creation of grounded landing pads underneath the edges of the mirror, to reduce charge sticking effect.

By contrast, the mirrors designed using Poly1 did not experience any fatal problems with stiction during the pull-in condition. Figure 60 shows a sampling of the fringe images captured from the McGill Test Chip. The voltage characteristic for these mirrors are shown in Figure 61. The average pull-in voltages for the north and south directions are 20.4 V and 20.5 V, respectively. The average pull-in voltage for the east and west directions are 28.7 V and 28.2 V, respectively. The deflection of these mirrors at pull-in varied from 22.26 mrad to 22.62 mrad for all four cardinal directions. Deflection along the diagonal was not tested with this design.

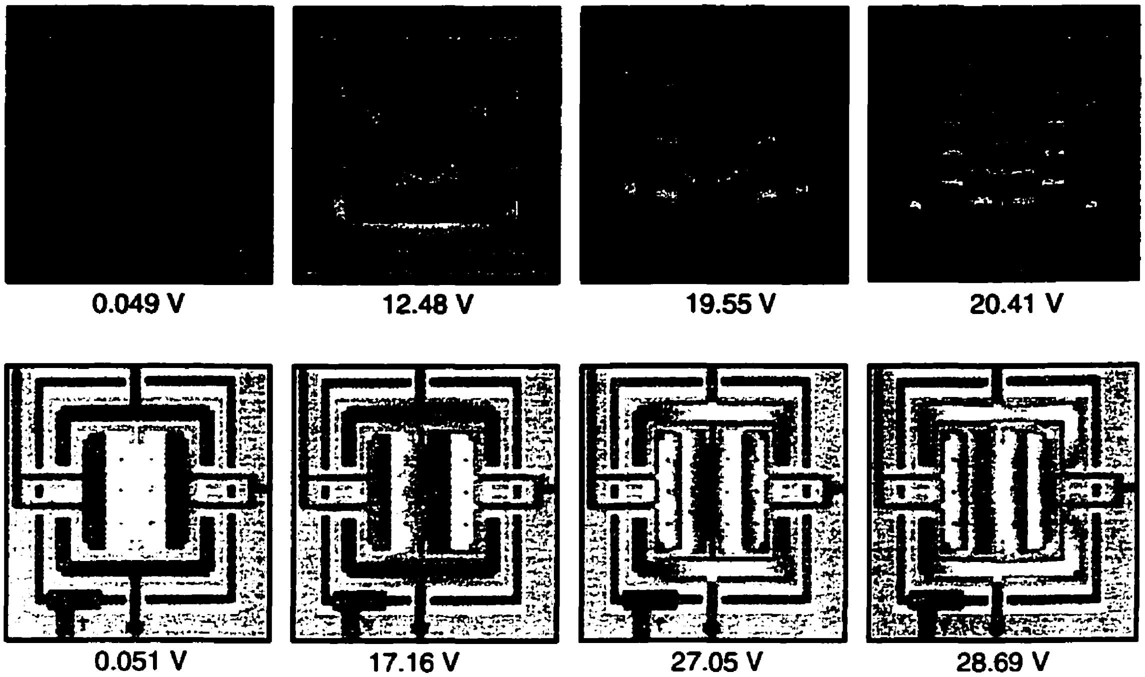


Figure 60. Sequence of fringe images for Mirror T. **Top:** North. **Bottom:** East.

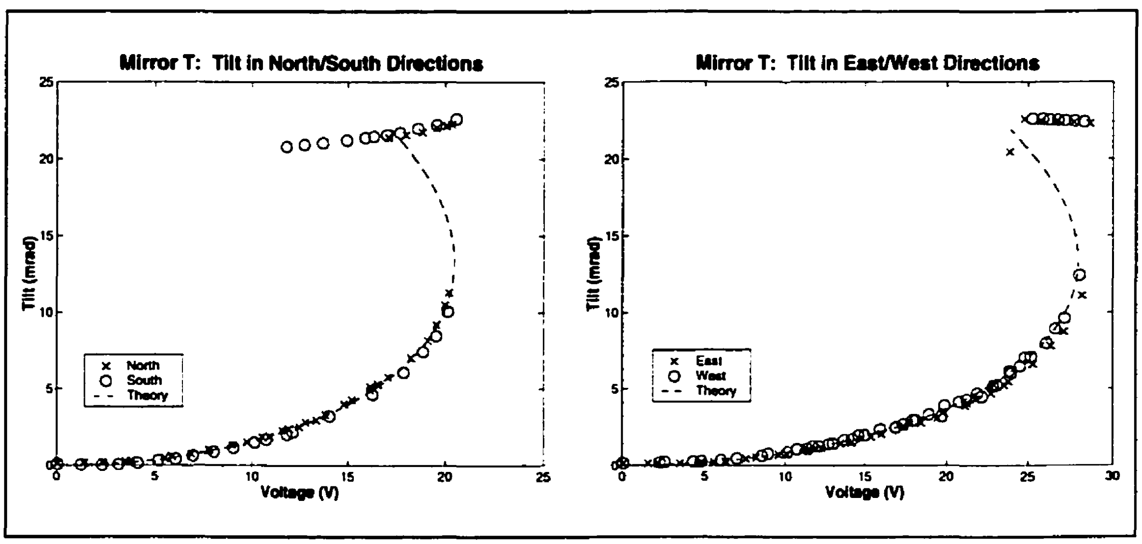


Figure 61. Voltage characteristics for Mirror T (Poly1).

As with Mirror G, the critical angle for this mirror was measured to be approximately 12 mrads. Thus, for angles less than 12 mrad, this design could be used as an analog mirror. Past this point, however, the mirror will pull in to its maximum deflection angle, at which point the voltage would need to be reduced by 5-10 V in order for the mirror to return to its initial position. Thus, for digital operation, an "on" voltage of 20-30 V and an "off" voltage of 0-10 V would be required.

Finally, the calibrated values of E needed to fit the experimental data to the theoretical models of Section 6.0 are 169 GPa and 164 GPa for the north-south and east-west directions, respectively. The corresponding spring constants, K_α, are 4.40 x 10^{-8} Nm and 4.26 x 10^{-8} Nm, which represent percent differences of 0.68% and 2.5%, respectively, from the values calculated in Section 6.3

8.6 Analysis of Results

8.6.1 Analysis of Device Yields

In general, the much lower yields for the designs on the second McGill MEMS chip, as compared to those for precisely the same design on the first McGill Test chip, are an indication of the higher number of production problems that must have occurred during the second fabrication process. Still, by comparing the device yields on the second chip for the different types of modifications trialed within each family of designs, important observations can be made about the type of design features that may produce the best possible yield, in spite of any production problems that may occur. In particular, from the results of Families II, III, and V, the following rules were compiled:

1) Double-thickness devices work better than single-thickness devices. This is because the top layer is much stiffer, creating surfaces that are much flatter and less susceptible to sagging. This increase in rigidity also helps prevent the mirror from collapsing during the structural release process.

2) Metal can be used to increase the reflectivity of the mirror surface, however this will also increase the curvature of the surface due to the higher levels of residual stress present in the metal layer. One possible solution to this problem, suggested in litera-

ture, is the use of a stacked Poly1-Oxide2-Poly2 structure; that is, a structure with a layer of oxide trapped in-between the two layers of polysilicon [92]. This structure is said to reduce the curvature of the upper surface due to the opposing stresses in the oxide layer versus those of the metal layer.

3) To increase the planarity of the upper surface, "dummy" sections of Poly0 can be used to fill in the gaps between the electrode geometries. Aside from flattening the topography of the upper layer, this technique also reduces the amount of residual stresses present due to the conformal dips and bends in the top surface as the layer is deposited. This in turn helps prevent the mirror from collapsing during the structural release process.

4) From the thermal devices of Family III: Shorter arms support loads better than longer arms. Thus, to reduce the possibility of structures collapsing during the release process, shorter arms should be used. However, from equations (8) and (9) in Section 6.3, it should be noted that shorter arms also have higher spring constants, when used with an electrostatic device; thus higher voltages would also be needed to actuate electrostatic devices with shorter support arms.

5) Finally, also from the results of Family III, Poly0 can be used to influence the stresses of an upper layer, making it less likely to curve downward when released. This bit of information may prove useful for future designs; one hypothesis is that the placement of polygons on the DIMPLE mask layer may be used to achieve a similar effect.

Thus, by following these five guidelines, the device yield for future sets of micromirror designs may be improved.

8.6.2 Active Behaviour: Rotational Mirror Designs

Table 13 summarizes the key results observed for the three rotational mirror designs: Mirror E2, Mirror G, and Mirror T, from Families III, IV, and V, respectively. The results are divided according to the two regimes of operation, namely analog and digital.

TABLE 13: Summary of Active Behaviour for Mirrors E2, G, and T

	MOTION	ANALOG	DIGITAL OPERATION		
DESIGN NAME	Tilt Direction(s)	Tilt Range (mrad)	Maximum Tilt (mrad)	Pull-in Voltage (V)	Release Voltage (V)
Mirror E2	N, S	0-16	16.0	—	—
Mirror G	N, S, E, W, NE, SE, NW, SW	0-12	20-23	22-26	16-21
Mirror T	N, S, E, W	0-12	22.4	20-29	16-23

From this table, Mirror E2 would appear to have the best analog response of the three mirrors, with tilt angles in the range of 0-16 mrad. On the other hand, Mirrors G and T can be used to tilt along several axes, with controllable tilt angles in the range of 0-12 mrad. Practically speaking, however, a safety margin would need to be added to this tilt range, in order to avoid meeting the pull-in condition for these mirrors accidentally. Thus, an analog tilt range of 0-10 mrad would be more realistic.

On the other hand, in terms of digital operation, both Mirrors G and T share very similar responses, with pull-in voltages in the 20-30 V range and release voltages in the 16-23 V range. The maximum tilt for both designs ranged from 20 to 23 mrad, depending on the direction of motion. Although both mirrors could, in theory, be tilted in eight discrete directions — namely, four axial and four diagonal — the control scheme for Mirror G would be much simpler than that for Mirror T. However, if the surface quality of the two mirrors is considered, it is clear that Mirror T would be the design better suited to applications in optical switching due to its larger central area free from print-through; this is in strong contrast with the upper surface for Mirror G, which displays distinct indentations across both central axes of the mirror. Thus, for this reason, Mirror T has been the design most favoured for further experiments in subsequent setups for optical switching applications [90] [91].

8.6.3 Device Modeling: Mirrors G and T

Finally, the key modeling results obtained from Mirror G and Mirror T are summarized in Tables 14 and 15 below. Since the model developed in Section 6.3 only applies to mirrors rotating in the axial direction, the results from Mirror E2 and Mirror G for motion in the diagonal direction have been excluded.

TABLE 14: Summary of Modeling Results for Mirrors G, and T (Part1)

	Modulus of Elasticity E		Torsional Spring Constant K_α		
Design Name (Direction)	**Typical (GPa)**	**Measured (GPa)**	**Model (Nm)** (E = 168 GPa)	**Measured (Nm)**	**% diff**
Mirror G (N/S)	160-180	163	4.37×10^{-8}	4.25×10^{-8}	2.7%
Mirror G (E/W)		160		4.15×10^{-8}	5.0%
Mirror T (N/S)	160-180	169	4.37×10^{-8}	4.40×10^{-8}	0.69%
Mirror T (E/W)		164		4.26×10^{-8}	2.5%

TABLE 15: Summary of Modeling Results for Mirrors G, and T (Part2)

	Modeled Values (E = 168 GPa)			Measured Values			
Design (Dir.)	Θ_{pin}	α_{pin} (mrad)	V_{pin} (V)	Θ_{pin}	α_{pin} (mrad)	V_{pin} (V)	% diff for V_{pin}
Mirror G (N/S)	0.4541	14.0	22.69	~0.39	~12	21.90	3.48%
Mirror G (E/W)						21.77	4.05%
Mirror T (N/S)	0.4297	13.2	20.38	~0.39	~12	20.45	0.34%
Mirror T (E/W)	0.4328	13.3	27.92			28.45	1.90%

From these tables, it is clear that the experimental values measured for Mirrors G and T match very well with the values predicted by the model presented in Section 6.3. Although the values for Mirror T seem to fit the theoretical model better than those for Mirror G, the reason for this improvement is not clear. One possible reason for this difference may be the increase in surface area for the electrodes in the design of Mirror G. This in turn may cause the top surface of the mirror to translate slightly in the z-direction, causing a small change in the value of the air gap, d. Since the behaviour of the mirror is highly sensitive to the value of d, this may account for the slight variation in the behaviour observed. Further refinements to the theoretical model would be needed to confirm this hypothesis.

9.0 FUTURE WORK

Future work for this project can be divided into three main areas: the collection of data for additional mirror devices, the development of new characterization techniques for oscillating MEMS devices, and the addition of new design modifications. The three categories are described in detail below.

9.1 Characterization of Additional Mirror Devices

Although this thesis involved the design and fabrication of five families of mirror designs, time constraints permitted the quantitative characterization of only three of these designs. Consequently, one area of future work for this project is the collection of additional data from the remaining families of mirror designs. This would include the deformable membrane mirrors of Family I, the thermally-actuated mirrors of Family II, the electrostatic piston mirrors of Family III, and the additional mirror variations fabricated for Families III, IV, and V. From this data, additional information on the behaviour of different mirror designs could be compiled and the designs adapted for use in future MEMS applications.

9.2 Dynamic Characterization of Oscillating Devices

A second focus for future work is in the area of device characterization. Although several test setups were assembled to characterize the static behaviour of a MEMS device, none were developed to characterize the dynamic behaviour of a MEMS device, that is the response of a device to an oscillating input signal. Thus, a new setup would be needed to measure both the frequency of oscillation of a device and the magnitude of the device's displacement simultaneously. Other parameters, such as the resonant frequency of the device, could also be measured. With this information, new designs for optical scanners could be developed and the designs customized to fit a variety of beam scanning applications.

9.3 Additional Design Modifications

Finally, a third area of interest for future work is the development of additional design modifications to help accomplish a number of the following goals: 1) To minimize problems with stiction during the release process; 2) To increase the planarity of the top mirror surface; 3) To minimize charge sticking effects during the operation of the device; 4) To reduce the range of operating voltages needed to control the device; and 5) To increase the range of tilt angles possible for the device.

As described previously (see Sections 5.0 and 8.0), a number of these goals could be accomplished in a variety of ways. Of especial note are the following suggestions: the use of "dummy" sections of Poly0 to planarize the topography of the Poly0 layer; the reduction of gaps between electrodes on the Poly0 layer to 2.0 μm — that is, the minimum possible value — instead of 5.0 μm; the use of the DIMPLE layer to form deeper indentations in the Poly2 layer; and the use of an elevator-like structure to raise the surface of the mirror high above the surface of the substrate. These suggestions — as well as those mentioned in other sections of this thesis — would all be worthy of further investigation.

10.0 CONCLUSIONS

In this thesis, five sets of designs for MEMS micromirror devices were prototyped using the MUMPs foundry service. These families of designs were chosen specifically to explore a number of different design parameters, including type of motion, actuation scheme, and layers used for the upper surface of the mirror. In addition, these designs were also chosen to fit a variety of different applications, such as adaptive optics, beam scanning, and optical switching.

The prototypes received were tested with the help of a phase-shifting Mirau interferometer, assembled specifically for the task. Although most designs seemed to work as expected, some manufacturing problems were observed with specific types of devices, such as those in Families II and III. These observations were used to develop a set of guidelines outlining possible design strategies that could be used to improve the production yield of future designs. Examples of these guidelines include the use of double-thickness layers of polysilicon instead of single thickness layers, as well as the use of Poly0 to increase the planarity of the upper mirror surface.

Further tests were performed on three of the rotational mirror designs, namely Mirrors E2, G, and T. From these tests, it was shown that all three designs could be used as analog mirrors for tilt angles in the range of 0-10 mrad, however Mirror E2 exhibited the best analog behaviour of the three mirrors, with tilt angles in the range of 0-16 mrad. On the other hand, Mirrors G and T could also be used as digital mirrors, with full deflection angles in the range of 20-23 mrad. The control voltages for these mirrors ranged from 0-10 V for Mirror E2, 0-26 V for Mirror G, and 0-29 V for Mirror T. The results of Mirrors G and T were shown to fall within 5.0% of the values predicted by the theoretical model presented in Section 6.0.

Finally, although both Mirror T and Mirror G can be used to control the direction of a beam of light along two separate axes, Mirror T was shown to have a distinct advantage over Mirror G due to its larger central area free from print-through. As a result, it is this mirror design that has been chosen for further tests by the Photonic Systems Group for applications in optical switching.

Future work on this project is expected to focus on three main areas: the collection of quantitative data for the remainder of the mirror designs not yet characterized, the development of new design modifications to improve the operation of these devices, and the development of new test setups for the dynamic characterization of oscillating MEMS devices.

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