Analysis and Design of a Gated Envelope Feedback Technique for Automatic Hardware Reconfiguration of RFIC Power Amplifiers, with Full On-Chip Implementation in Gallium Arsenide Heterojunction Bipolar Transistor Technology

by

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DEDICATION

À ma mère, Renée, en remerciement
pour son dévouement pour notre famille

ABSTRACT

In this doctoral dissertation, the author presents the theoretical foundation, the analysis and design of analog and RF circuits, the chip level implementation, and the experimental validation pertaining to a new radio frequency integrated circuit (RFIC) power amplifier (PA) architecture that is intended for wireless portable transceivers.

A method called Gated Envelope Feedback is proposed to allow the automatic hardware reconfiguration of a stand-alone RFIC PA in multiple states for power efficiency improvement purposes. The method uses self-operating and fully integrated circuitry comprising RF power detection, switching and sequential logic, and RF envelope feedback in conjunction with a hardware gating function for triggering and activating current reduction mechanisms as a function of the transmitted RF power level. Because of the critical role that RFIC PA components occupy in modern wireless transceivers, and given the major impact that these components have on the overall RF performances and energy consumption in wireless transceivers, very significant benefits stem from the underlying innovations.

The method has been validated through the successful design of a 1.88GHz CDMA RFIC PA with automatic hardware reconfiguration capability, using an industry renowned state-of-the-art GaAs HBT semi-conductor process developed and owned by Skyworks Solutions, Inc., USA. The circuit techniques that have enabled the successful and full on-chip embodiment of the technique are analyzed in details. The IC implementation is discussed, and experimental results showing significant current reduction upon automatic hardware reconfiguration, gain regulation performances, and compliance with the stringent linearity requirements for CDMA transmission demonstrate that the gated envelope

feedback method is a viable and promising approach to automatic hardware reconfiguration of RFIC PA's for current reduction purposes. Moreover, in regard to on-chip integration of advanced PA control functions, it is demonstrated that the method is better positioning GaAs HBT technologies, which are known to offer very competitive RF performances but inherently have limited integration capabilities.

Finally, an analytical approach for the evaluation of inter-modulation distortion (IMD) in envelope feedback architectures is introduced, and the proposed design equations and methodology for IMD analysis may prove very helpful for theoretical analyses, for simulation tasks, and for experimental work.

ABRÉGÉ

Dans cette thèse de doctorat, l'auteur présente les fondements théoriques, l'analyse de circuits analogiques et hyperfréquences, la réalisation de circuits microélectroniques, et les vérifications expérimentales se rattachant à une nouvelle architecture d'amplificateur de puissance intégré RFIC fonctionnant aux hyperfréquences, et dédié aux transmetteurs pour communications sans fil.

Une méthode intitulée Rétroaction d'Enveloppe Conditionnée est proposée afin de rendre possible la reconfiguration automatique d'un amplificateur de puissance RFIC en conditions hardware multiples, dans le but d'améliorer son efficacité énergétique. Cette méthode utilise des circuits entièrement intégrés sur puce et fonctionnant de façon autonome, permettant de déclencher et d'appliquer des mécanismes de réduction de courant dépendamment du niveau de la puissance transmise.
Étant donné le rôle critique qu'occupe un amplificateur de puissance RFIC dans un transmetteur-récepteur pour communications sans fil, ainsi que l'impact important de ses caractéristiques sur les performances électriques et sur la consommation d'énergie, des avantages considérables découlent des concepts innovateurs qui s'y rattachent.

Cette méthode a été validée à travers la conception d'un amplificateur de puissance RFIC à reconfiguration hardware automatique pour transmetteurs CDMA et fonctionnant à 1.88 GHz, en utilisant l'un des procédés de semi-conducteur GaAs HBT appartenant à Skyworks Solutions, Inc., États Unis.

Les techniques de circuits qui ont permis la réalisation complète et réussie de ce système sur puce sont analysées en détails. Les résultats expérimentaux qui sont présentés démontrent la possibilité d'une diminution importante de la consommation de courant suite à la

reconfiguration automatique des circuits, ainsi qu'une compensation automatique du gain avec un taux de régulation attrayant, tout en respectant les normes sévères qui concernent le niveau de distorsion dans les signaux hyperfréquences émis.

Les résultats de ce travail de recherche permettent de mieux positionner la technologie GaAs HBT en ce qui a trait à l'intégration sur puce de fonctions complexes pour le contrôle des amplificateurs de puissance RFIC.

Finalement, une méthode pour l'évaluation de la distorsion dans un amplificateur hyperfréquence utilisant la rétroaction d'enveloppe est introduite dans cette thèse. Les équations qui sont proposées peuvent s'appliquer à des analyses théoriques, à des problèmes de simulation, et à des travaux pratiques.

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INTRODUCTION - Front-end RFIC power amplifiers for wireless transceivers

Generalities: wireless transceivers and their applications

Wireless communication systems occupy critical functions in today's societies, and are likely to play an even more important role in the future. One only has to think of the numerous wireless applications that modern societies have come to depend on extensively to realize how much these technologies are part of our daily lives, and to be able to gauge their impact on our way of life in social and economical terms. While a broad and expanding array of wireless communication applications exists and others are emerging [1]-[3], the more commonly known ones, such as mobile telephony for personal communication, wireless LANs (Local Area Networks) for data communication, GPS navigators, wireless sensors, RF medical equipment, and RF identifier devices (RFID), just to name a few, may be cited to highlight the practicality and diversity that wireless systems provide.

Mobile telephony is the largest segment in wireless applications today. Its phenomenal expansion in the last few decades has led to the 1.8 billion strong worldwide subscriber population by the end of the year 2007 [4], creating a historical and unprecedented growth in the electronic business sector. This vast communication coverage is enabled by various transmission protocols for radio links and networks, using different modulation schemes for conditioning the electric signals in the wireless transceiver units before being transmitted through the air. Among the most widely used transmission standards today are CDMA, W_CDMA, GSM, UMTS and EDGE [3], [5].

Regardless of the transmission protocol used, an important feature in any wireless and portable communication equipment is that it has to be supplied with batteries. This implies that the total ***current consumption*** of the equipment has to be reduced as much as possible in all operating conditions, in order to maximize its power efficiency, and thus improve the power supply autonomy of the transceiver equipment through longer battery life-time.

1.1 The critical role and key technological aspects of front-end RFIC power amplifiers in modern wireless transmitter architectures

The analog and RF processing of information through a typical transmitter path within a modern wireless transceiver is depicted in Fig. 1.1.1, and may be used to refer to the well known super-heterodyne digital modulation transmitter architecture [5]-[7].

The original binary information is split into two low-pass filtered multilevel digital streams called the I/Q base-band signals, before being applied as modulating signals to the I/Q orthogonal modulator, which delivers the modulated intermediate frequency (IF) carrier at its output, typically within a 200MHz range. This IF signal is applied to the input of a variable gain amplifier (VGA) circuit, which is used to adjust the overall transmitter chain gain, and an RF mixer circuit is used to up-convert the modulated IF signal to the desired transmit carrier frequency, through a frequency mixing process between the RF local oscillator non-modulated signal and the modulated IF signal. The resulting modulated RF carrier is filtered at the output of the up-converter mixer, before being applied to the input of the RF integrated circuit (RFIC) power amplifier (PA) component located in the front-end section near the antenna. While it depends on the specific transmitter design, the power level at the input of the RFIC PA in a mobile transceiver used in cellular telephony is typically below 6dBm (4 mW).

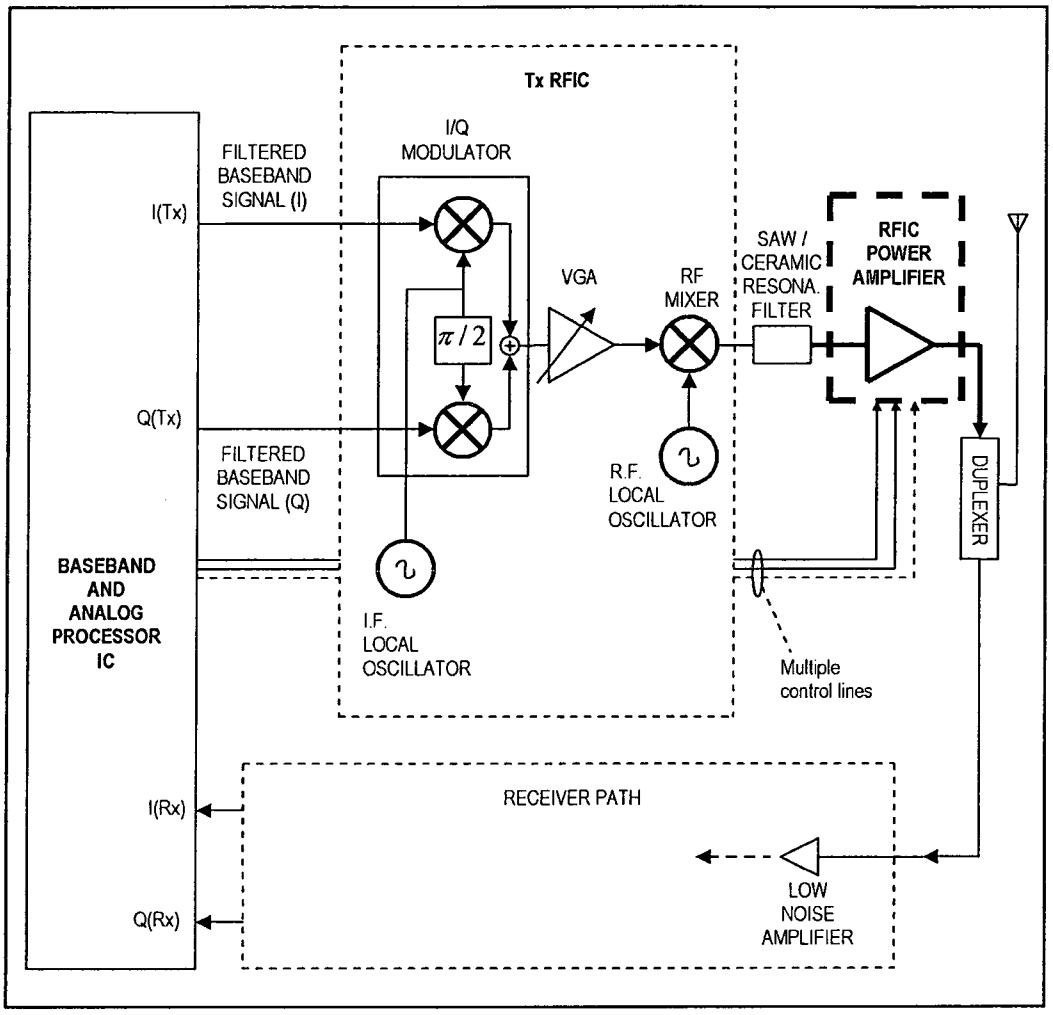

Figure 1.1.1: Block diagram of the transmitter path in a typical modern super-heterodyne wireless transceiver employing orthogonal modulation.

Thus, the primary role of the RFIC PA is to raise the power level of this modulated RF carrier signal at levels that are typically in the range of 24dBm (0.25 W) to 34.8dBm (3 W) for cellular phones. The output power level specified for the PA accounts for the losses through the duplexer and other front-end components, in order to meet the transmitted power requirements as per the regulated standards and transmission protocol. Therefore, the PA must deliver the large current signal to the antenna while maintaining the original modulation characteristics with the highest

possible fidelity, i.e. with minimum distortion. Because of the high current intensities in the PA circuitry, this high fidelity amplification process (referred to also as high ***linearity*** amplification) is one of the major design challenges in modern wireless transceivers.

This power amplification process also translates into high energy consumption. For example, in cellular phones as much as 50% of the total power supplied by the batteries to the entire transceiver is typically consumed in the PA component alone [5]. This justifies the need in some existing transmitter architectures for some form of ***circuit reconfiguration*** of the PA block with the use of ***multiple control lines*** (Fig. 1.1.1), for the purpose of adapting the mode of operation of the PA and scaling down its current consumption when the operating conditions allow it. The notion of circuit reconfiguration with the use of multiple control lines will be referenced and discussed in more detail in later sections.

The high power amplification process also contributes to other difficult design challenges, such as electronic noise that tends to increase with the current intensity; the generation of disruptive interference signals in the receiver path of the transceiver through conduction and air coupling; and the need for thermal dissipation.

All of the above considerations make the PA component a critical element in modern wireless transceivers, and are among the driving forces behind intensive research efforts in the field of RFIC power amplifiers.

1.1.1. Gain and phase variations in the modulation schemes

For the purpose of highlighting the modulation characteristics that influence the most the design of wireless transceivers circuitry, and in particular the power amplifier stage that delivers the large modulated RF carrier signal to the antenna, the modulation standards may be grouped

into two distinct categories: constant envelope modulation, and non-constant envelope modulation.

Constant envelope modulation

With modulation standards such as GSM and UMTS, the information conveyed through the communication channel is contained only in the phase variations of the RF carrier signal, and thus the amplitude of the RF carrier signal is independent of the digital information stream, but adjusted only through the VGA circuit (Fig. 1.1.1). Hence, it is common practice to refer to this type of modulation standard as a constant envelope modulation, underlying a constant peak-to-peak amplitude of the RF signal as a function of time, for a given constant average transmitted power level.

Non-constant envelope modulation

In contrast, for modulation standards such as CDMA and W-CDMA, the information is contained in both the amplitude and the phase variations of the RF carrier signal. Hence, due to the dependence of the carrier amplitude on time and information, and making use of a symbolic representation of the amplitude variations as an envelope that delimitates the peak-to-peak amplitude of the RF carrier signal in time, it is common practice to refer to this type of modulation standard as a non-constant envelope modulation.

1.1.2. Power added efficiency

The characteristic desired from an RFIC PA in regard to current consumption is generally measured by the power added efficiency (PAE) metric.

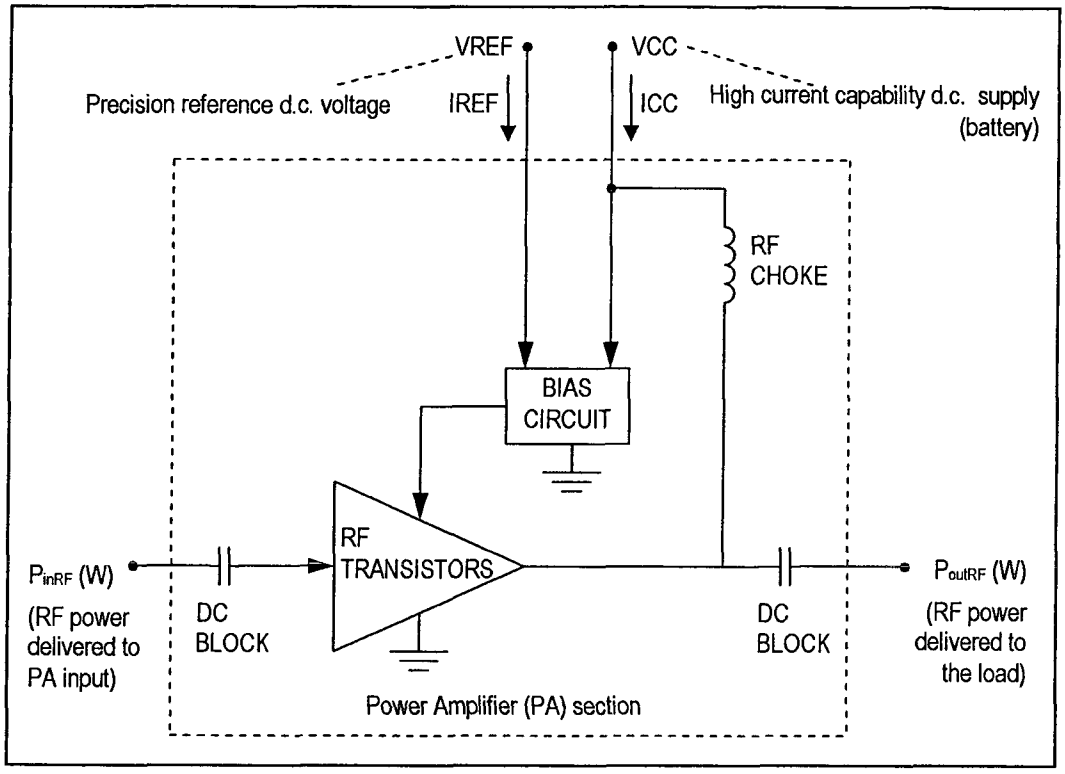

Figure 1.1.2: Block diagram of a typical RF power amplifier section.

From Fig. 1.1.2, the efficiency of the amplifier section in converting the total d.c. power (P_{DC}) supplied by all d.c. sources (as an example, 2 d.c. sources are shown in Fig. 1.1.2: VREF and VCC) into an RF output power (P_{outRF}) delivered to the load (usually including a duplexer followed by the antenna) may be expressed as an ***output efficiency*** in a percentage value as

$$\text{Output Efficiency: } \eta(\%) = \left(\frac{P_{outRF}}{P_{DC}}\right) \cdot 100 \qquad (1.1.1)$$

and when taking into account (i.e. subtracting) the RF power delivered to its input (P_{inRF}), the ***power added efficiency*** (PAE) is expressed by

$$PAE = \left(\frac{P_{outRF} - P_{inRF}}{P_{DC}} \right) \cdot 100 \qquad (1.1.2)$$

In the example shown, the total d.c. power is equal to ($VREF \cdot IREF + VCC \cdot ICC$) in Watts, and thus the above expressions translate a low d.c. current consumption (i.e. low $IREF$ and ICC values) into high power efficiencies.

1.1.3 The trade-off between efficiency and linearity

Based on conventional high efficiency amplifier design techniques [8], the power efficiency of a transistor based RF amplifier may be improved by shaping the high intensity RF current flowing through the transistor and the voltage waveforms across the transistor device terminals with specific time dependant relationships. The rationale is that ideally no power is dissipated by the transistor when the current flowing into it is nil, even if a non-zero voltage is applied across its terminals. Hence, by shaping the waveforms for maximizing the time spent with a zero amplitude RF current (i.e. with minimum conduction time), the power dissipated in the transistor is minimized, and consequently the overall PAE is maximized. With a sine wave input signal excitation of frequency ω, the conduction time may be referred to by the corresponding conduction angle θ, and commonly used also to categorize the operating condition of the PA in different classes, namely class A, class B, class AB and class C. A simplified representation of this concept is illustrated in Fig. 1.1.3, showing a bipolar transistor that is biased using a base-emitter (V_{BE}) voltage in a controlled fashion that allows adjusting the conduction angle θ of the collector current $I_C(\omega t)$ (with θ representing the total conduction angle within one angular period 2π), while maintaining the same peak collector current value (i.e. the maximum intensity $I_{\max}$).

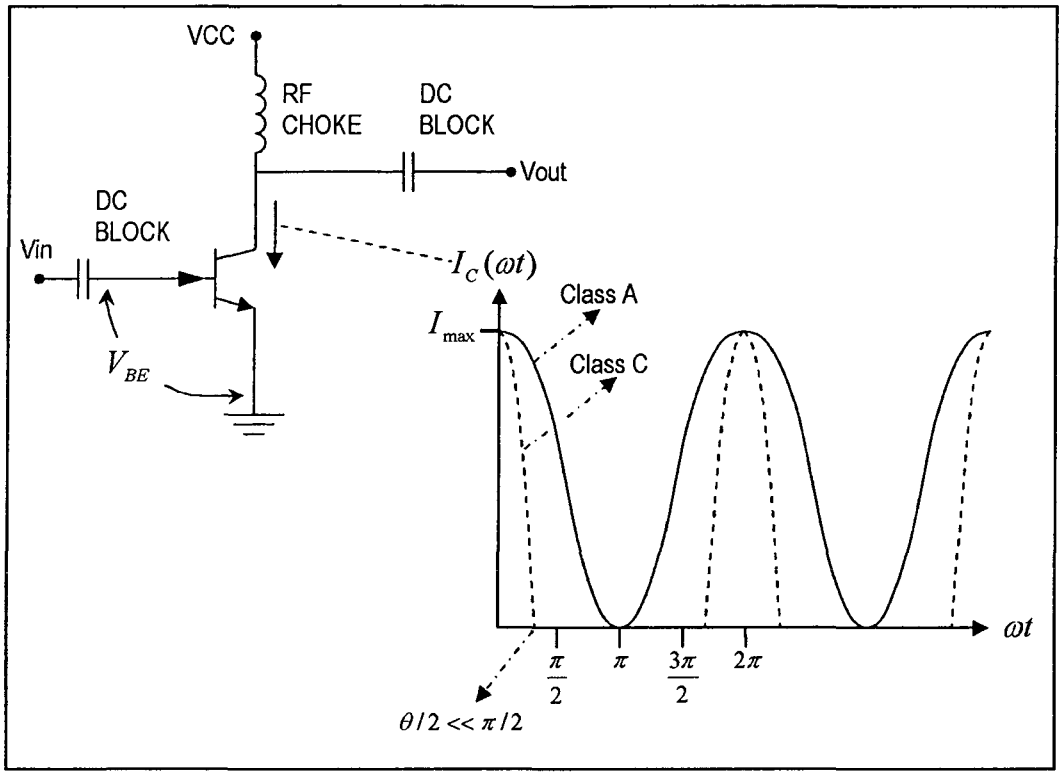

Figure 1.1.3: Representation of an RF transistor biased and driven with a sine wave excitation for different collector current conduction angles.

The current waveform showing a 2π total conduction angle within one period corresponds to a class A operation, by definition. The one showing a total conduction angle that is well below π (i.e. with a cut-off angle $\theta/2$ well below $\pi/2$) corresponds to a class C operation, and the case of a total conduction angle $\theta = \pi$ (not shown) would correspond to a class B operation. The average current value I_{DC} and the amplitude I_1 of the fundamental frequency component (i.e. the frequency of the input excitation sine wave) of these even function current waveforms as functions of the conduction angle θ may be derived through Fourier analysis and expressed by [8]

$$I_{DC} = \left(\frac{I_{\max}}{2\pi}\right)\left(\frac{2\sin(\theta/2) - \theta\cos(\theta/2)}{1-\cos(\theta/2)}\right) \quad (1.1.3)$$

$$I_1 = \left(\frac{I_{\max}}{2\pi}\right)\left(\frac{\theta - \sin(\theta)}{1-\cos(\theta/2)}\right) \quad (1.1.4)$$

and all the current harmonic content (i.e. the 2nd, 3rd, 4th,... harmonics) may be derived following the same approach.

Using similar formulations of the current harmonic content and the definition of power efficiency in eq. (1.1.1), and assuming that only the fundamental current component expressed by eq. (1.1.4) contributes to the useful and desired signal power P_{outRF} delivered to the output load in Fig. 1.1.2, then the well known "trade-off between efficiency and linearity" may be represented graphically in a simplified form that relates the power efficiency to the harmonic distortion, as shown in Fig. 1.1.4 [8]. The current amplitudes of the d.c. component, the fundamental component and the 2nd harmonic component as a function of the conduction angle are shown, with their values normalized to the maximum intensity current value $I_{\max}$. The corresponding output efficiency is also shown. It can be seen from these curves that the efficiency may be increased by reducing the current conduction angle from the class A condition to the class C condition, which results in a reduction of the average current component (I_{DC}), and which is a fundamental conventional approach for improving the efficiency of power amplifiers at high power levels. However, this also increases the amplitude of the second harmonic current ($I_{harmonic\_2}$), which is a simplified representation of the fact that more generally, distortion (hence a degradation of the linearity due to a nonlinear amplification process) is inevitably introduced when the amplifier is operated in the low conduction angle (i.e. high efficiency) amplification mode.

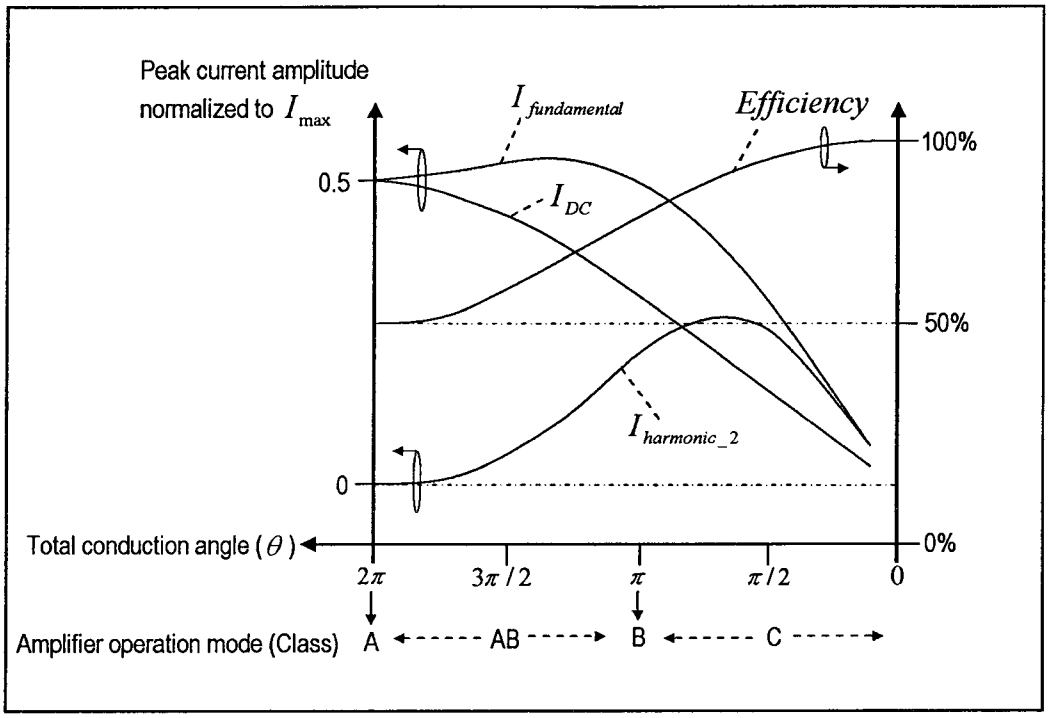

Figure 1.1.4: Normalized current amplitudes of the average current and the current harmonic content, and the output efficiency as a function of the total conduction angle (from [8]).

This has major implications in the design of wireless transceivers [5]-[7]. The undesired output harmonic components that are generated in the case of a pure sine wave input excitation as discussed above may be more easily filtered out, given the wide frequency spacing between the wanted RF carrier signal and the second harmonic. In contrast, the undesired output frequency components that may be generated through a nonlinear amplification mode in the case of an input excitation consisting of multiple sine waves at different frequencies may be much more difficult or sometimes impossible to eliminate practically with the use of filters, when these undesired output frequency components are very close to the desired fundamental frequency carrier signal.

An analytical study of these unwanted distortion signal components that are close to the carrier signal (usually referred to as inter-modulation distortion (IMD) products) with a multiple sine wave input excitation (multi-tone excitation) may be carried out using well established formulations (e.g. [5], [6], [8]) for IMD analysis. Such analyses may allow taking into consideration various types of nonlinear mechanisms that generate distortion in an amplifier besides the conduction angle, such as gain compression, supply voltage clipping, transistor saturation effects, and nonlinear transistor device parameters. And by extension, analytical multi-tone distortion formulations may also be used to predict with some level of accuracy the amount of distortion generated in the case of modulated input excitation signals (e.g. [9], [10]), thus taking into account the effects of the envelope amplitude functions of non-constant modulation schemes (e.g. CDMA and W-CDMA), which are more complex than what is associated with a multi-tone sine wave excitation.

1.1.4. Efficiency improvement in the upper range of the transmitted power levels

The approach described above for trading off linearity performances for increased efficiency yields more significant results in the upper range of the transmitted power levels, where the adjustment of the conduction angle may be more precisely achieved. The large RF current and voltage amplitudes, compared to the values of design parameters such as the minimum transistor quiescent current required in order to meet the desired gain objective, or compared to a bipolar transistor's collector-emitter saturation voltage (VCE_{sat}), allow for relatively precise and repeatable adjustments.

The trade-off between linearity and efficiency at high power levels may also be very significantly improved with the use of various types of linearization techniques in conjunction with a high efficiency mode of

operation such as class AB or class B. Some of these linearization techniques may be grouped according to the different approaches they use, including (but not limited to): (i) multi-harmonic source and load impedance matching techniques (e.g. [11]-[15]), where source and load impedances at the fundamental and harmonic frequencies are optimized in order to shape the current and voltage waveforms across the transistor terminals in the time domain to ensure minimum power dissipation in the transistor; (ii) dynamic load adaptation (e.g. [16]-[18]), where the power transfer to the load is maximized across a given power range through a dynamic adjustment of the load impedance level; (iii) hardware based pre-distortion techniques (e.g. [19]-[21]) that make use of nonlinear analog and RF circuits to drive the PA input with distortion characteristics that tend to oppose and ideally cancel the distortion generated by the PA itself; (iv) digital signal processing (DSP) based pre-distortion techniques (e.g. [22]-[26]), where the pre-distortion principle described above is implemented in DSP algorithms and applied at the base-band signal level (i.e. the I-Q signals in Fig. 1.1.1), and generally function of look-up tables that contain characterization data describing the typical nonlinear behaviour of the PA in different operating conditions; (v) Envelope Feedback techniques (e.g. [27]-[28]) that use analog, RF and hybrid circuits to compensate for distortion in the instantaneous amplitude or phase of the output modulated signal as a function of the input envelope signal, through a feedback correction process.

While the above techniques have demonstrated significant improvement in the efficiency-linearity trade-off in the upper range of the output power level, it is worth noting that they require a considerable amount of additional circuitry, and may also rely on extensive characterization data of the PA for their successful implementation. And, as a matter of fact, extensive additional circuitry may have a significant negative impact on the current consumption at low power levels, where the biasing current

required for this circuitry becomes comparable to the quiescent current of the PA itself. Moreover, the additional circuitry required may not always be suitable for integration on a single integrated circuit die.

1.1.5. The importance of current reduction at low to mid-range transmitted power levels

While an improvement in power efficiency in the upper range of the output power level of a PA translates into significant current reduction (given the high currents in the upper range), ***improving the efficiency at low to mid-range power levels has also a major impact on the overall average current consumption*** of the transceiver equipment, and thus on the battery life-time. This is better understood by considering, as an example, the graph in Fig. 1.1.5 which represents the transmitted power occurrence probability for a CDMA mobile phone [5] and the associated average current that is typically drawn by the power amplifier section.

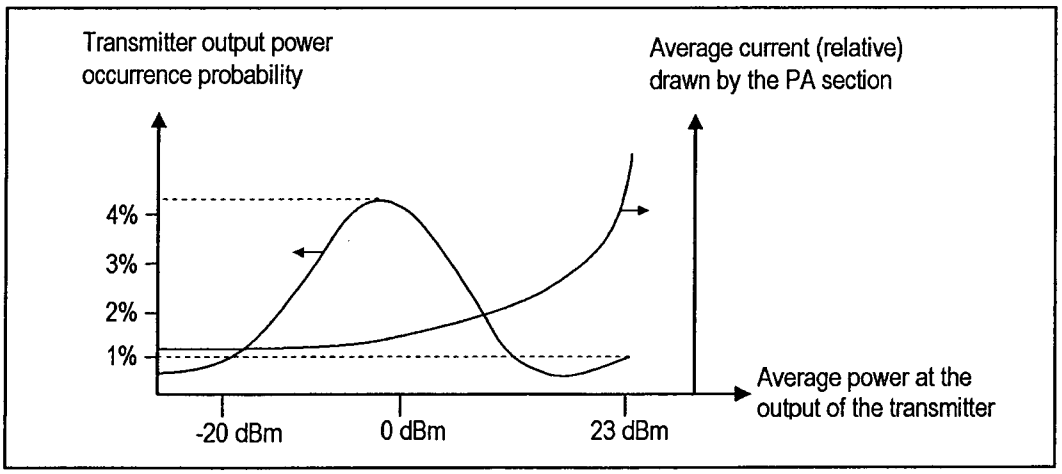

Figure 1.1.5: Probability distribution for the PA output power in a CDMA mobile phone and the typical associated average current consumption on a relative scale (from [5]).

It can be seen from this figure that for a CDMA mobile transceiver there is a high probability of transmitting at the low to mid-range power levels (i.e.

below ~20dBm), and thus in general the ***current reduction techniques for RFIC PA's in the lower range of output power have a major impact on the average current drawn from the battery***.

1.2 GaAs HBT technology for linear RFIC PA applications

A few semi-conductor technologies have been demonstrated to be applicable with various degrees of RF performance competitiveness for RFIC PA designs that are intended for mobile wireless transceivers. Among those technologies, Silicon (Si) and Silicon-Germanium (SiGe) BiCMOS processes have been demonstrated in the recent years to offer improved performances in efficiency and linearity, as well as in other aspects that are important in PA design, such as RF power gain, robustness and low voltage operation [29]-[35].

On the other hand, Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) technologies have been demonstrated to offer outstanding RF performance in the PCS frequency band in particular (i.e. in the vicinity of the 1.8GHz to 1.9GHz range), and thus to be very competitive for RFIC PA applications that require an optimum trade-off between efficiency and linearity [36]-[40] at those frequencies. This explains why these technologies have dominated for more than a decade, and continue to dominate, the linear RFIC PA market, besides its very strong presence in the nonlinear RFIC PA market (such as for GSM transceivers) as well. The efficiency-linearity trade-off is of particular importance for power amplifiers used in transceivers that employ non-constant envelope modulation schemes, such as in CDMA and W-CDMA transceivers. The linearity dependence on envelope amplitude variations may be better understood through an IMD analysis, by verifying that the IMD products generated through a nonlinear amplification mode and which fall on frequencies that are closer to the carrier signal (referred to as the 3^{rd} order IMD products because of their direct mathematical relationship with 3^{rd} order polynomial terms that are function of the excitation frequencies) are

closely dependent on the peak-to-average power ratio related to the envelope variation of the carrier signal [5]-[6], [8].

However, the GaAs HBT processes offer significantly less circuit integration capabilities when compared to Si or SiGe BiCMOS [36]. This may become a considerable disadvantage for future RFIC PA applications that might require the integration of increasingly complex functions on the same IC die. Nevertheless, advanced circuit techniques such as those pursued in this thesis could lead to GaAs HBT technology superiority for linear RFIC PA applications.

1.3 The rationale and objectives of this research work

With the rapid technological advancements in modern wireless communication systems, there is a need for research on the subject of high performance and highly integrated RFIC PA's that can address the very challenging system performance requirements, in particular in regard to efficiency and linearity. Many emerging technologies and applications in wireless telecommunication are significantly affected by the PA performance, including those for mobile telephony and wireless LANs.

The motivations behind this research work were the following:

to explore and propose new transmitter concepts, new RFIC PA architectures, engineering concepts and RF circuit techniques that would contribute to improve the performances of the RF transmitter front-end sections in wireless transceivers, with focus on investigating RFIC PA architectures that offer increased autonomy and functionalities in this critical component, flexibility in their application, higher on-chip circuit integration, ease of implementation, and cost and size effectiveness.

More specifically, because of the major impact RFIC PA's have on the overall current drawn from the batteries of wireless transceivers, the power efficiency management and linearity performance trade-offs were key aspects in defining the research objectives, and because of the need for better positioning GaAs HBT technologies for the increasingly needed complex PA functions, contribution toward single-chip integration in this semi-conductor technology was set as a priority research effort.

1.4 Thesis outline

In Chapter 2 of this thesis, the scope and specific research objectives will be presented in detailed technical terms that relate directly to the innovations sought through this work for front-end RFIC PA architectures and performances. The theoretical foundations pertaining to the new concepts and techniques introduced will also be presented. Design equations that facilitate IMD analysis in an envelope feedback amplifier are introduced, together with a design and test methodology.

In Chapter 3, the design that was used to validate the new RFIC PA architecture introduced and investigated will be presented with detailed system and circuit analysis.

In Chapter 4, the practical integrated circuit (IC) implementation and the experimental results that allowed the validation of the proposed concepts and techniques will be presented.

Conclusions and suggestions for new research topics are summarized in Chapter 5.

1.5 Contributions to research from this work

The contributions to research from this work may be referred to at different levels: (i) at the RF systems design level; (ii) at the RF systems analysis level; (iii) at the RFIC power amplifier techniques level; (iv) at the RF transmitter front-end architecture design level, and (v) at the GaAs HBT IC circuit integration level.

(i) RF systems design

The ***Gated Envelope Feedback*** concept is introduced and validated. This method uses a hardware ***gating function*** in conjunction with envelope feedback in order to restrict the necessity for optimum envelope feedback performances to a narrow power dynamic range only. The concept is applicable and relevant for RF power amplifier design in IC technologies, as well as in discrete components technologies.

(ii) RF systems analysis

Design equations for closed loop multi-tone IMD analysis of envelope feedback RF amplifier architectures are introduced, and a ***design and test methodology*** which is based on these design equations is proposed. The design equations and the proposed methodology are intended for use as an alternative or complementary approach to computer based circuit simulation. The formulations that are derived are based on a behavioural model of an RF envelope feedback amplifier, and are based on using a 3-tone, 5^{th} order IMD analysis which facilitates:

- the theoretical analyses during the design of RF envelope feedback amplifier systems
- piece-wise simulations that are localized in the power domain, and that may be particularly helpful in avoiding simulation convergence problems
- the estimation of IMD and gain performance requirements for the circuit blocks in the error signal path of an envelope feedback amplifier in open loop conditions, as a function of the overall desired closed loop IMD performances and system parameters.

(iii) RFIC Power amplifier techniques

A functional and ***full on-chip*** implementation of an envelope feedback based RF power amplifier is demonstrated, with evidence of the feasibility for single-chip integration.

(iv) RF transmitter front-end architecture design

The following RF transmitter front-end architecture features are rendered possible thanks to the gated envelope feedback PA concept:

- ***a versatile and automatic RFIC PA hardware reconfiguration scheme*** that allows a wireless transmitter front-end reconfiguration into ***multiple states*** (theoretically into an unlimited number of hardware states) for current reduction and efficiency improvement purposes (and that could be used possibly for other purposes) at low to mid-range transmitted power levels, thus requiring the use of a ***single control line*** and the ***minimum of synchronisation*** with the other RF, analog, and digital IC's in the transmitter
- ***automatic reduction of the gain perturbations*** that occur upon hardware reconfiguration
- ***only three (3) measurement points for calibration at room temperature*** to compensate for gain perturbations upon hardware reconfiguration.

(v) Gallium Arsenide (GaAs) IC circuit integration

The concept and circuit techniques proposed and validated in this research work are ***better positioning GaAs technologies*** for single-chip integration of advanced PA control functions aimed at current reduction (efficiency improvement), for future stand-alone PA's.

1.6 Publication

N. G. Constantin, P. J. Zampardi[1], and M. N. El-Gamal, "A Gated Envelope Feedback Technique for Automatic Hardware Conditioning of RFIC PA's at Low Power Levels," the *IEEE Microwave Theory and Techniques Symposium*, pp. 139-142, June 2007.

Note: the above paper was accepted for presentation in the long lecture category, and also in the finalists' presentations for the "best student paper" competition, at the 2007 IEEE MTT International Microwave Symposium (MTT-IMS) held in Honolulu, Hawaii, USA in June 2007. The paper was ranked in the 4th place (tied), and was awarded an honourable mention certificate by the IEEE MTT-S society.

[1] Skyworks Solutions, Inc., USA.

CHAPTER 2

Scope of research, objectives and theoretical foundation

This chapter presents the motivations behind this work, the scope of research, the specific research objectives, the theoretical foundations used, and the new concepts and techniques that have been introduced and investigated. Also, design equations are derived for IMD analyses that can be used for analytical and experimental work.

Section 2.1

A review of the techniques proposed for current reduction in RFIC power amplifiers at low power levels

This section serves as a brief review of the techniques that have been proposed in the literature for current reduction at low power levels, and highlights the drawbacks and limitations associated with these techniques.

2.1.1 On the efficiency and linearity improvement methods using digital signal processing techniques and advanced hardware architectures

Various methods have been proposed for improving the power added efficiency and linearity of microwave amplifiers. Some techniques (e.g. [41]-[42]) utilize digital signal processing (DSP) algorithms to improve the trade-offs between efficiency and linearity, for example through adaptive pre-distortion of the RF signal itself, or through feedback based error corrections at the base-band signal frequency. While these techniques have been demonstrated to be particularly flexible and useful at the upper range of power levels and up to the maximum power levels in very high power amplifiers, they require, on the other hand, complex circuitry that would not be applicable to stand-alone single-chip RFIC PA implementations.

2.1.2 Proven current reduction techniques at low and mid-range power levels

Because of the high probability for certain mobile communication equipment of transmitting at low and mid-range power levels (i.e. typically below 20dBm) [43]-[44], and consequently due to the high impact on the overall current consumption of the transmitter at these levels, some techniques have been proposed for reducing the current consumption as a function of power level. These techniques focus mainly on various types of

hardware reconfiguration within the PA circuitry at different power levels, in order to drastically reduce the overall bias current. The deactivation of sections of the amplifier's RF transistor arrays together with their corresponding biasing circuitry, the reconfiguration of the RF transistor arrays and the adjustment of the output matching circuit are typical means of achieving this goal.

Transistor array reconfiguration

In [43], it is demonstrated that the separation of a power amplifier output stage transistor array into groups and sub-groups of different sizes as a means for dynamic current biasing, and the reconfiguration of the sub-groups into a current reuse topology as a means for voltage dynamic biasing, allows achieving very significant reductions in the overall current consumption. The concept is validated in a CDMA RFIC PA design using the high integration capability of a SiGe BiCMOS technology. The switching and reconfiguration of the different sections require NFET transistor circuits that are designed for optimizing power gain and minimizing the compression of the amplifier. Upon activation of the hardware reconfiguration, gain deviations as high as 1.8dB are reported. Such gain deviations have to be compensated for in order to comply with the regulations for CDMA transmissions. This important aspect will be further detailed in later sections.

Note also that with Doherty amplifiers [8], [17], which employ a load-modulation scheme in conjunction with transistor array reconfiguration as a function of power for efficiency improvement, significant gain variations may be encountered, besides the requirement for special impedance matching circuitry that may not be integrated on an IC.

Transistor array switching and bias switching

In [45]-[46], it is demonstrated that with the use of external digital control signals, different sections in the RF transistor arrays of an RFIC power

amplifier and their corresponding biasing circuits may be turned OFF in a discrete step fashion at predetermined power thresholds. At low power levels, turning OFF these sections results in very significant current reduction. The use of external digital control signals and simple bipolar transistor logic circuits allows the implementation of this technique in a single-chip GaAs HBT power amplifier. While no gain deviation figures were given in [45], the data provided on the bias current scaling upon activation of the different hardware states suggests important gain deviations associated with the current scaling. This is in agreement with the output power discontinuities reported in the power versus bias control data, and with the reference in the article to large gain expansions versus bias current at low power levels. Large gain deviations are reported also in [46].

Output impedance matching control

In [45] and [47]-[48], current reduction as a result of improving power added efficiency at low power levels is reported. The underlying concept is that, for a given low power level at the output of the power amplifier, the adjustment of an ideally lossless impedance matching network for the purpose of increasing the load impedance presented at the output of the amplifier will also translate into a decrease in the RF current amplitude passed by the RF transistor, and thus translates into a power efficiency improvement. The proper output matching reconfiguration allows the scaling down of the quiescent biasing current of the RF transistor without introducing any current clipping or transistor saturation [8]. Such scaling of the bias current as a function of the load tuning inevitably introduces significant gain deviations, because of the sensitivity of the amplifier's gain with respect to the current intensity at low power levels.

Dynamic biasing

In [49], the dynamic adjustment of the biasing current of RF transistors in a power amplifier chain in a continuous fashion, as a function of the average power of the RF signal at the input, is shown to allow significant reduction in the current consumption at low power levels. A 1dB maximum gain variation design objective over the full usable power dynamic range is achieved by trading-off the corresponding boundary conditions on the bias current range. While this approach mitigates the gain deviation issue, the technique uses relatively complex circuitry, including precision detector circuits, and thus relies necessarily on the high integration capabilities of Bi-CMOS semi-conductor technologies. Moreover, since this approach uses a forward compensation scheme for the adjustment of the bias current as a function of power, important gain deviations would still be introduced if it were used together with some hardware reconfiguration technique, such as the switching of the output matching circuit at different power levels.

2.1.3 Drawbacks and limitations with the state of the art techniques proposed for current reduction at low power levels

While the above state of the art techniques for current reduction at low power levels have shown significant improvements in power efficiency, drawbacks and limitations may be pointed out in regard to their practical implementation and the overall transmitter performance.

Number of control lines

With techniques that depend on the activation of digital control signals from outside the power amplifier in order to perform a reconfiguration of the hardware (e.g. [43], [45]), the number of control lines increases with the number of programmable states. This has negative implications in regard to (i) the integration level and size of the power amplifier module, (ii) to noise coupling issues, (iii) to the hardware requirements imposed on

interfacing with other integrated circuits in the chip set that form the transceiver system (see Fig. 1.1.1), and (iv) in regard to the hardware requirements imposed on the test jigs used for testing the amplifier module.

Requirement for synchronization

Besides the issue of number of control lines, the requirement for the activation of external control lines imposes more burden on the transceiver's software for managing the necessary synchronization associated with the reconfiguring of the hardware.

Calibration requirements

With the techniques presented in [43], [45]-[48], large gain deviations are inevitably introduced upon activation of the hardware reconfiguration mechanisms, and have to be compensated for in order to comply with system requirements in terms of continuity in the signal transmission, and in terms of the quality of the transmission, defined by performance criteria such as power level increments, distortion related spectral regrowth (Adjacent Channel Power - ACP) in the frequency domain, waveform quality (Rho), and error vector magnitude (EVM) measured from the transmitted RF signal [50]. The gain deviations in the techniques proposed so far for RF transistor array reconfiguration or switching may be as important as 1.8dB, as reported in [43], and are not necessarily consistent from one device to another, given the very nonlinear dependence of the gain on the current intensity and temperature. Hence, the use of a typical-behaviour look-up table embedded in each transceiver unit, and containing gain correction factors that are representative of a sample population of power amplifier devices, may not always be sufficient to compensate for these nonlinear gain perturbations in an accurate enough and consistent fashion. Consequently, stringent and time consuming calibration steps may be required both in the development phase and in

the production phase of wireless communication equipment utilizing power amplifier devices that are reconfigured with these techniques for current reduction purposes.

Restrictions in regard to the semi-conductor technology

The technique presented in [49] and validated with a 0.5um Bi-CMOS design may not be suitable for implementation in a cost and die size efficient way in GaAs technologies, due to the inherent low integration capability of these technologies [36]. In particular, the use of precision RF power detectors, such as the patented voltage squarer circuits reported in [49], may be prohibitive with a bipolar transistor only GaAs HBT process, and given also the large base to emitter voltage (~1.35V at room temperature) that are typical of GaAs HBT technologies, which would not allow a low voltage mode of operation.

Section 2.2

Scope and specific research objectives in this work

This section presents the scope and the specific objectives targeted in this research work.

2.2.1 The need for novel power amplifier architectures that better address the demands of wireless communication systems

In order to respond to the fast technological evolution toward the emerging wireless communication protocols and systems, the trends in the research and development of front-end RF modules are driven mainly by the need for transmission with multi-band and multi-mode operation, by the expectations for RF front-end modules to have an impact with better overall transceiver performances in terms of current consumption, and by the need for greater on-chip integration for size reduction, for more added functionalities that are aimed at versatility and power efficiency improvement, for cost and size reduction as well as for ease of implementation by the manufacturers of wireless equipment [51]-[52].

Power amplifiers being major constituents of RF front-end modules, the general scope of this research work was to investigate novel RFIC PA architectures that address the above mentioned general needs. The main contributions sought were in terms of innovation with respect to amplifier architecture and on-chip hardware functionalities, with focus on the overall power efficiency performance improvement through current reduction at low power levels, on-chip circuit integration in GaAs HBT technologies, increased overall performances of transceivers, as well as cost and size effectiveness.

Moreover, the fast expanding CDMA and W-CDMA technologies are driving the need for more complex and integrated RF front-end modules

(e.g [53]-[54]). Accordingly, the efforts in this research work were directed towards future CDMA and WCDMA applications.

2.2.2 Specific research objectives

The following research objectives were pursued in the course of this research work:

(1) To propose a novel stand-alone RFIC power amplifier architecture that provides ***increased autonomy*** in regard to optimizing power efficiency as a function of the transmitted power level, allowing ***automatic reconfiguration*** into ***multiple hardware states*** for the purpose of drastically ***reducing the current consumption at low power levels*** (hence for significantly improving the amplifier's overall power efficiency), with the use of a ***single external control line***, minimum hardware interface requirements and minimum synchronization from outside the power amplifier module.

(2) To propose a power amplifier architecture intended for automatic reconfiguration for ***various types of hardware conditioning***, while performing ***automatic compensation against the perturbations in the RF signal transmission*** and ***compliance with the CDMA standard specifications***, namely in terms of ***continuity*** and ***quality*** of the transmission.

The features listed in (1) and (2) above are referred to in the RFIC PA and transmitter chip-set illustration shown in Fig. 2.2.1, which highlights the typical RFIC PA hardware flexibility and automatic reconfiguration capability sought in the course of this research work. The multiple types of hardware states that were taken into consideration for efficiency improvement during the investigations are represented by the switching ON and OFF of sections in the RF driver stage (DR2) and in the RF power stage (PS3, PS4), the switching of the power supply feed to different supply voltages, and the switching of the output node of the amplifier (RF_OUT) to different impedance matching networks. All these types of

hardware conditioning schemes introduce severe gain perturbations that have to be compensated for.

(3) To propose IC solutions that minimize the calibration requirements, for simplification of test procedures, for costs reduction and for ease of implementation.

(4) To propose and validate circuit techniques that allow achieving the goals in the research objectives (1), (2), and (3) in an embodiment that demonstrates the ***feasibility of a single-chip GaAs HBT integration*** with the ***smallest possible die size***, in order to better position this technology in terms of integration and added functionalities for power amplifier applications.

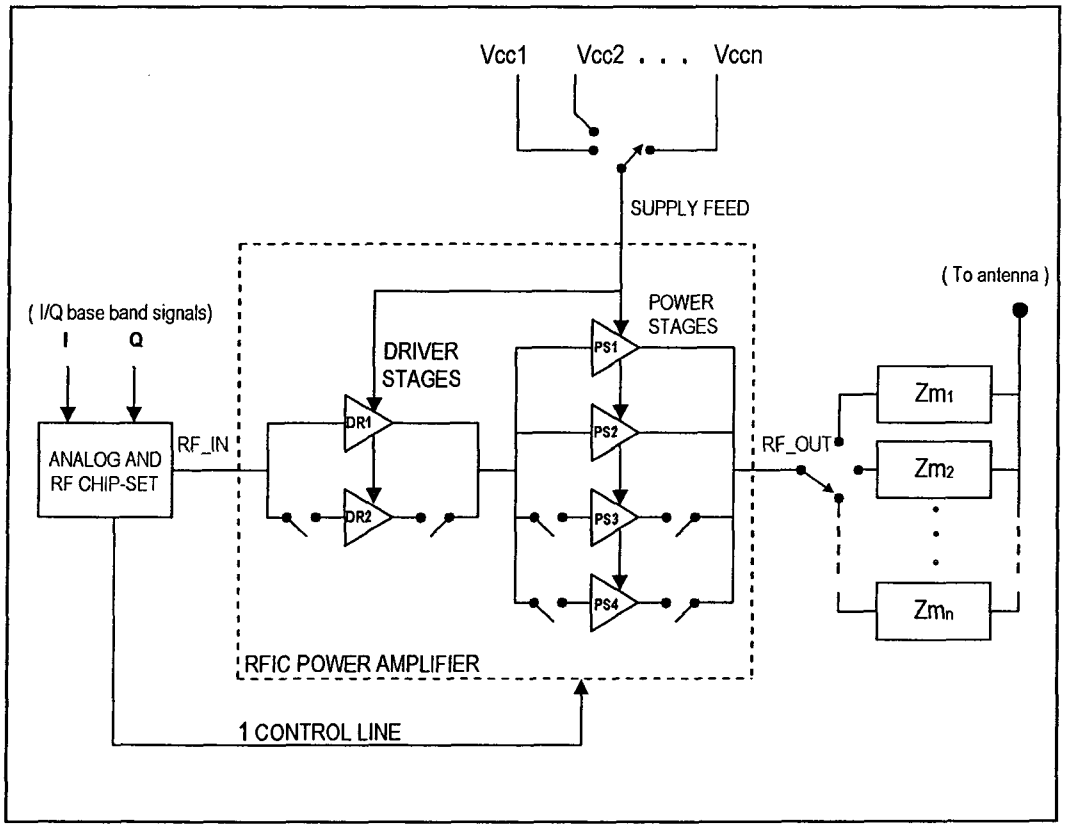

Figure 2.2.1: Illustration of an RFIC power amplifier architecture, which describes the hardware flexibility and automatic reconfiguration capabilities addressed during the course of this research work.

Section 2.3

A new approach to hardware reconfiguration of RFIC power amplifiers

In order to meet the specific research objectives presented in section 2.2, there was a need to develop a novel approach to RFIC PA hardware reconfiguration. The following sections present the key aspects that differentiate the power amplifier architecture introduced in this work and intended for current reduction through hardware reconfiguration, with respect to the techniques that have been reported in the literature.

2.3.1 Increased PA autonomy

As detailed in section 2.1, the techniques that have been reported to date in the literature for hardware reconfiguration of RFIC power amplifiers rely exclusively on the activation of external control signals. It was discussed that the drawbacks of this approach include more control lines as the number of states increases, increased hardware interfacing requirements, and the need for synchronization from outside the power amplifier. In contrast, the power amplifier architecture proposed in this work allows for ***increased power amplifier autonomy*** in regard to the management of the hardware reconfiguration as a function of power level. The appropriate functionalities required for this purpose, such as RF power detection, analog signal processing and sequential logic, are embedded together in a feedback mechanism (i.e. adjustments on the input, based on the observation of the output) within the power amplifier on-chip circuitry in order to provide ***automatic*** hardware reconfiguration in ***multiple*** states, and with the use of a ***single external control line***.

2.3.2 Increased PA adaptability through feedback

The techniques reported to date for PA hardware reconfiguration rely entirely on the characterization of the transistor devices and circuits, as well as calibration procedures, to enable hardware reconfiguration with a

forward (open loop) compensation scheme against perturbations. These techniques use typical-behaviour look-up tables as a means to estimate the necessary correction needed to compensate against the nonlinear and temperature dependant gain variations that occur upon activation of the hardware reconfiguration. In contrast, the architecture proposed in this work makes use of the inherent ***adaptability of a feedback structure*** (closed loop architecture) to ***automatically*** cancel large, nonlinear and temperature dependant gain perturbations that occur under most of the conditions where hardware reconfiguration takes place, thus requiring ***minimum characterization and calibration***.

2.3.3 Architecture to suit the low integration capability of GaAs technologies

While the most recent techniques proposed for hardware conditioning [43], [49] tend to rely on the high integration capabilities of Si BiCMOS and SiGe BiCMOS technologies, the architecture introduced in this work is aimed at making use of high performance but simple enough circuit structures to suit the low integration capabilities of GaAs technologies, thus better positioning these technologies in the implementation of complex on-chip circuitry for power efficiency improvement.

2.3.4 Technological challenges and pertinence to RF System-On-Chip integration

The implementation of the proposed architecture in a single-chip GaAs HBT solution poses major challenges, besides the circuit integration limitations that are inherent to this technology. In addition to this, the need for implementing a full on-chip feedback architecture to provide the adaptability sought in the processing of a non-constant envelope signal at microwave frequencies (such as a PCS band CDMA signal) imposes difficult goals. This is particularly challenging in regard to meeting the linearity requirements for this type of modulation, considering the large

dynamic range in the CDMA envelope variation that delimits the peak-to-peak amplitude of the signal. As detailed in [8] on this specific issue, regardless of the semi-conductor technology used, it is particularly challenging to implement an on-chip feedback mechanism that processes a modulated RF signal over its entire dynamic range with good enough feedback performances in order not to generate excessive AM-PM distortion to an extent that outweighs the intended goals, that is, in this work, the automation and adaptability features of feedback.

Concurrently, it is to be noted that no full on-chip implementation of a power amplifier that uses an envelope feedback structure to process any complex waveform such as CDMA has ever been reported in the literature. Hence, the RFIC PA architecture introduced in this research work addresses technological challenges that are at the heart of RF System-On-Chip (S.O.C.) integration.

Section 2.4
Some system level considerations pertaining to regulations on RF transmissions for CDMA2000 wireless equipment

This section describes system level specifications pertaining to regulations on RF transmissions for mobile CDMA transceivers, which have direct implications on the performance objectives in the development of a CDMA RFIC power amplifier. Only limited specifications are listed in this section, as a guideline for the validation of the PA architecture and circuit techniques that are introduced to meet the research objectives.

2.4.1 Linearity metrics

A CDMA transceiver has to comply with challenging linearity performance criteria that are defined with specific measurement test set-ups and conditions [50], and that may be related to the linearity performance requirements of its front-end RFIC power amplifier as a stand-alone component. The basic linearity requirements for CDMA2000-1X mobile handsets are listed below, as a reference for linearity design goals in an envelope feedback amplifier system.

Adjacent channel power rejection (ACPR)

Relative to the total CDMA information channel power contained in the 1.2288MHz bandwidth (i.e. given in dBc relative to the channel power), the adjacent channel power rejection (ACPR) metric defines the maximum acceptable level of power transmitted in an upper or lower frequency band, as a result of distortion in the transmitter path, or noise and spurious signals being amplified. The CDMA2000-1X ACPR specification is -42dBc/30KHz in the upper or lower frequency range defined by an offset of 885KHz to 1.98MHz from the center of the information channel.

Waveform quality (ρ)

The waveform quality factor (ρ) is a scalar metric that is defined with a specific formulation [50] and that gives a measure of the distortion in a CDMA modulated signal. It represents a correlation figure of merit between the complex CDMA signal (hence function of amplitude and phase) that is transmitted and an ideal distortion free transmitted CDMA signal. A ρ factor of 1 corresponds to an ideal distortion free transmitted signal. For CDMA mobile handsets, ρ needs to be greater or equal to 0.944.

Error vector magnitude (EVM)

A third linearity metric used for the transmission of modulated signals is the error vector magnitude (EVM) [5]. It gives a measure of the distortion in terms of the modulation accuracy of the amplified modulated signal, by relating the complex instantaneous CDMA information (i.e. the phasor quantity that represents the CDMA modulation) of the amplified signal to that of an ideal distortion free transmitted CDMA signal. Hence, the EVM metric is a percentage value that relates to the mean square error between samples of the actual CDMA phasor quantity of the amplified signal and samples from the ideal signal, normalized to the average power of the ideal signal. The specified value (typically below 5%) at the level of the amplifier component may vary slightly, based on the manufacturer's specification standards.

2.4.2 Transient metrics

The power level at the output of the power amplifier in a mobile CDMA transmitter is continuously adjusted based on information sent through the communication link between the mobile transmitter and a base station [6]-[7], [50], and must comply with transient and precision metrics [50] that are

defined with specific measurement test set-ups and conditions [50]. Some of these metrics are referred to below.

Power control step response

The CDMA transmitter must be able to perform a 20dB power increase following a rate of change that is contained within upper and lower limits. Only the minimum rate of change needs to be validated in this work, since the compliance with the upper limit is necessarily achievable (with the use of slew rate reduction techniques in the transmitter) when the lower limit can be met. The minimum rate of change requirement is of exponential form [50] with a maximum gradient that is approximately 5dB per 10ms.

Incremental step precision

The CDMA transmitter must be able to perform power incremental steps of 1dB with a precision of +/- 0.5dB.

Section 2.5
Envelope feedback and its practical implementation

This section serves as a review of the envelope feedback concept [8] and presents some key aspects of its practical implementation, for the purpose of defining the technological challenges in implementing this technique in an on-chip environment.

2.5.1 Gain pre-distortion as a building block of envelope feedback

Figure 2.5.1 illustrates the notion of pre-distorting the complex gain of a power amplifier as a means for linearization, thus for canceling any distortion in the amplitude and phase of the RF signal at the output of the amplifier. Expressions that are similar to those presented in [55] will be used to highlight the limitations of envelope pre-distortion and to derive some design guidelines.

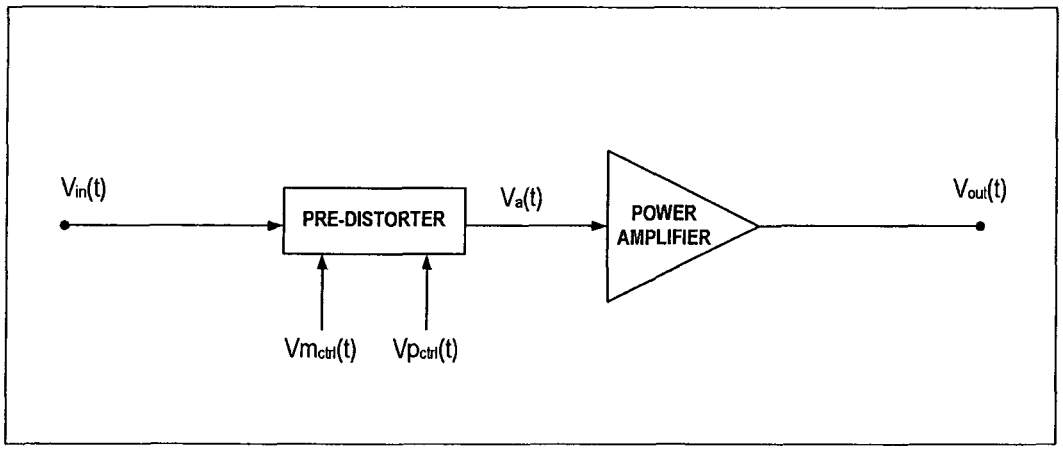

Figure 2.5.1: Block diagram illustrating the pre-distortion of an amplifier.

The RF power amplifier block in Fig. 2.5.1 is preceded by a low power variable gain and variable phase pre-distorter element, which may be adjusted with the control signals $Vm_{ctrl}(t)$ and $Vp_{ctrl}(t)$ in order to vary the

amplitude of the signal $V_a(t)$ applied to the input of the power amplifier as well as its phase, respectively. Ideally, the cascaded gain and phase of the overall chain may be kept constant if the control signals provide the information required for the cancellation of any perturbation.

Considering an excitation by an RF carrier signal of frequency w_c and whose amplitude is modulated by a function $A(t)$, the signal applied to the input of the system may be represented in the exponential form by:

$$V_{in}(t) = A(t)e^{j(w_c(t)+\phi(t))}. \quad (2.5.1)$$

$A(t)$ is a time domain function that only describes the amplitude variation of the input excitation, while $\phi(t)$ defines only its phase variation as a function of time. The pre-distorter element is assumed to have a nonlinear complex gain defined by a function $P\{V_{in}(t)\}$ that transforms $V_{in}(t)$ into a driving signal $V_a(t)$ to the input of the power amplifier element. This transformation is represented by a dependence on the control voltages $Vm_{ctrl}(t)$ and $Vp_{ctrl}(t)$, that are assumed to be function of only the amplitude $A(t)$ of the input signal $V_{in}(t)$, and following a relationship that guarantees the cancellation of any gain or phase distortion in the output signal $V_{out}(t)$.

Accordingly,

$$V_a(t) = P\{A(t)\}\left(A(t)e^{j(w_c(t)+\phi(t))}\right) \quad (2.5.2)$$

with $P\{A(t)\}$ defining a complex gain. Thus, the time dependant scalar quantity $|P\{A(t)\}A(t)|$ may be used to define the amplitude variation of $V_a(t)$.

The nonlinearities of the RF power amplifier may be represented by a complex function $G[V_a(t)]$ that multiplies the low level driving signal $V_a(t)$. This nonlinear transformation is assumed to introduce amplitude and phase distortion in the output signal $V_{out}(t)$, but only as a function of the amplitude of $V_a(t)$. Thus:

$$G[V_a(t)] = G\left[|P\{A(t)\}A(t)|\right] = G\left[|P\{A(t)\}|A(t)\right].$$

Hence, the transformation of the signal from the input to the output of the cascaded chain may be represented as follows:

$$V_{out}(t) = G[V_a(t)]V_a(t),$$

which, after substitution, yields:

$$V_{out}(t) = G\left[|P\{A(t)\}A(t)|\right] P\{A(t)\}\, A(t)\, e^{j(w_c(t)+\phi(t))}$$

and thus

$$V_{out}(t) = P\{A(t)\}\, G\left[|P\{A(t)\}\, A(t)|\,\right] V_{in}(t) \qquad (2.5.3)$$

Assuming a perfect cancellation of the gain and phase distortion introduced through the cascaded chain implies that the ratio between the input and output amplitudes is equal to some constant C, and the phase shift from the input to the output is nil, such that:

$$|P\{A(t)\}| = \frac{C}{\left|\left(G\left[|P\{A(t)\}\, A(t)|\,\right]\right)\right|} \qquad (2.5.4)$$

and

$$\arg\left(P\{A(t)\}\right)+\arg\left(G\left[\left|P\{A(t)\}A(t)\right|\right]\right)=0 \qquad (2.5.5)$$

Limitations in AM-AM pre-distortion

Equation (2.5.4) sets the condition for amplitude distortion cancellation, but at the same time shows the limitation of the pre-distortion technique as a linearization method. Considering the case where the power amplifier is brought into gain compression as a result of a large and increasing input amplitude $|V_a(t)|$, it is therefore assumed that in response to this increasing value the power amplifier element experiences a gain decrease, implying a negative rate of change of the gain term $\left|\left(G\left[\left|P\{A(t)\}A(t)\right|\right]\right)\right|$ with respect to $|V_a(t)|$. The inverse proportionality of eq. (2.5.4) shows that the pre-distorter gain term $|P\{A(t)|$ has to expand, i.e. with a positive rate of change, as $|A(t)|$ increases, in order to counter the amplifier's gain compression. However, the need for an expansion of $|P\{A(t)|$ is rendered even more severe by the fact that the negative rate of change of the amplifier gain, associated with the term $\left|\left(G\left[\left|P\{A(t)\}A(t)\right|\right]\right)\right|$, is itself intensified by its dependence on the expanding quantity $|P\{A(t)|$. This translates into severe requirements for a low power pre-distorter element in an RFIC embodiment, in terms of output power driving capability and power control dynamic range. The above described implicit relation and its implication on the output power dynamic range requirements for the pre-distorter, together with the amplifier's inevitable deep compression and power saturation characteristics [8] that come into play as $|V_a(t)|$ further increases,

constitute an inherent limitation in the effectiveness of the pre-distortion technique as an amplitude to amplitude (AM-AM) linearization method.

Limitations in AM-PM performances

When operating the power amplifier at power levels that result in a moderate gain compression, hence well below the amplifier's saturation level, the phase distortion behavior generally poses no significant added complexity in the design of a hardware based phase pre-distorter. At moderate gain compression levels of the amplifier, the phase deviation that is introduced in the carrier signal at the output of a power amplifier as a result of its amplitude-to-phase (AM-PM) distortion generally follows a nonlinear variation with respect to $|V_a(t)|$, which may be characterized and predicted with good repeatability. As $|V_a(t)|$ increases as a result of an increase of $A(t)$ and drives the power amplifier into compression up to some moderate level, the phase of the RF carrier signal experiences a monotonous negative rate of change (e.g. [56]) or a monotonous positive rate of change (e.g. [22]), depending on the nonlinearity characteristics. However, when the amplifier is forced into deeper compression toward saturation, the rate of change in its phase distortion generally experiences a reversal at some power level [8], which would have to be taken into consideration in the design and would complicate significantly the design of the phase pre-distorter hardware.

Design guidelines for an AM-AM only RFIC pre-distortion circuit embodiment

Assuming that only moderate compression levels of the power amplifier block are considered, the above relationships point to the following guidelines to allow using an AM-AM only pre-distortion function as a building block for envelope feedback with good linearity performances, in an RFIC embodiment with the highest possible power efficiency:

(i) the power dynamic range covered through gain expansion at the output of the pre-distorter as well as its power saturation level must be maximized because of their big impact on the extent to which the power amplifier's gain compression may be cancelled. At the same time, the total current consumption must be kept to a minimum, for power efficiency reasons. This requires careful trade-offs in the choice of the driver stage (DR1 and DR2 in Fig. 2.2.1) device size.

(ii) since envelope feedback with a correction of the amplitude distortion only is considered in this work (given the goal of compensating only for gain deviations upon hardware reconfiguration), then for the envelope feedback implementation to comply with linearity requirements, the power amplifier's AM-PM distortion effects must be negligible compared to the AM-AM distortion effects. This imposes constraints on the power stage device size (PS1 to PS4 in Fig. 2.2.1) that may be deactivated by the automatic reconfiguration mechanism, and subjected to envelope feedback. Here also careful trade-offs are required, between deactivating the largest possible device size for maximum current reduction, and maintaining the minimum device size that guarantees no excessive gain compression or phase deviation.

2.5.2 Linear envelope feedback analysis

Figure 2.5.2 illustrates a small signal model of the envelope signal path through the main building blocks that are typically used in an envelope feedback amplifier system. The RF signal propagating through the system is dynamically conditioned through a gain control circuit acting as a pre-distorter element, as part of an envelope feedback mechanism. Hence, the envelope information V_a available at the input of the power amplifier ideally includes the pre-distorted information required to compensate for

the amplitude distortion introduced by the power amplifier, and is dynamically adjusted through the gain control element.

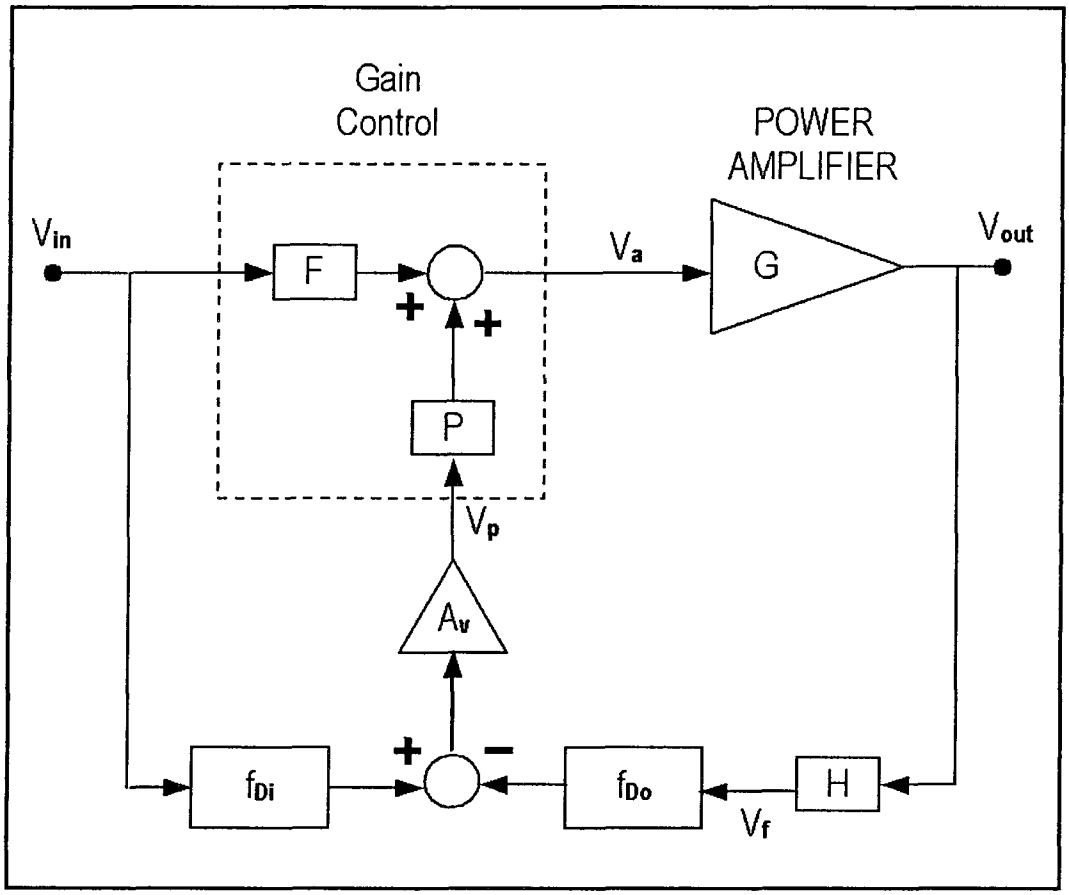

Figure 2.5.2: Small signal representation of the envelope signal path in an envelope feedback amplifier system.

The different signals and blocks may be defined as follows:

V_{in}: a time dependant envelope information that defines the amplitude variation of the RF signal that is applied at the input of the feedback power amplifier system

V_a: the time dependant envelope information that defines the amplitude variation of the RF signal present at the input of the power amplifier element

V_{out}: the time dependant envelope information that defines the amplitude variation of the RF signal delivered at the output of the power amplifier system

G: the gain function that relates the envelope information V_a to the envelope information V_{out}

V_p: the a.c. component of the feedback information used to dynamically adjust the gain control circuit

F: the forward gain function that relates a variation of V_{in} to the corresponding variation of V_a, when V_p is zero

P: the gain control slope factor that relates the rate of change of V_a with respect to V_p, for a given constant value of V_{in} (for the purpose of the small signal analysis in this section, P will be considered as a constant, but will be reexamined as a nonlinear function in the context of distortion analysis in a later chapter)

f_{Di}: the input RF detector's RF to analog conversion gain function, which translates V_{in} into an analog signal at the non-inverting input of the feedback comparator as a reference measure of V_{in}

H: the gain function associated with the attenuation of the envelope information in the reverse path

V_f: the time dependant envelope information that defines the feedback sample of the output envelope information V_{out}, i.e. V_{out} multiplied by H

f_{Do}: the output RF detector's RF to analog conversion gain function, which translates V_f into an analog signal at the inverting input of the feedback comparator as a feedback measure of V_{out}

A_v : the analog amplifier gain function that scales up the envelope feedback error information to V_p

Considering small variations of V_{in}, V_a, V_f and V_p at any given input RF power level, and by using the approximation that all gain and attenuation functions are linear in the vicinity of these small envelope variations, the block diagram depicted in Figure 2.5.2 may be analyzed as a linear feedback system in the Laplace domain [57]. In this case, the above definitions may be transposed into frequency domain relationships of signals and transfer functions, with the Laplace variable $s = j\omega$, as follows:

$$V_a(s) = F(s)V_{in}(s) + P(s)V_p(s)$$

and

$$V_{out}(s) = G(s)\left[F(s)V_{in}(s) + A_v(s)P(s)\left(f_{Di}(s)V_{in}(s) - f_{Do}(s)H(s)V_{out}(s)\right)\right], \quad (2.5.6)$$

which may be re-written as

$$V_{out}(s) = F(s)G(s)V_{in}(s) + \left(A_v(s)P(s)G(s)\right)\left(f_{Di}(s)V_{in}(s) - f_{Do}(s)H(s)V_{out}(s)\right) \quad (2.5.7)$$

Accordingly, the input to output envelope transfer function in the frequency domain may be represented as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{F(s)G(s)}{\left(1 + A_v(s)P(s)G(s)f_{Do}(s)H(s)\right)} + \frac{A_v(s)P(s)G(s)f_{Di}(s)}{\left(1 + A_v(s)P(s)G(s)f_{Do}(s)H(s)\right)} \tag{2.5.8}$$

For conditions where the open loop gain amplitude $\left|A_v(s)P(s)G(s)f_{Do}(s)H(s)\right|$ is much greater than unity, eq. (2.5.8) may be simplified to:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{F(s)}{A_v(s)P(s)f_{Do}(s)H(s)} + \left(\frac{f_{Di}(s)}{f_{Do}(s)}\right)\left(\frac{1}{H(s)}\right) \tag{2.5.9}$$

Ideally, the analog amplifier is designed to provide a gain $\left|A_v(s)\right|$ that contributes the most to the overall open loop gain and is high enough for the feedback system to yield a good precision. This ensures that $\left|A_v(s)P(s)f_{Do}(s)H(s)\right|$ is far greater than $\left|F(s)\right|$, and thus has the equivalent effect of canceling any nonlinearity that may be introduced in the signal path through the forward conversion gain $\left|F(s)\right|$ of the gain control element. Under these conditions, the envelope feedback analysis may be simplified to the following transfer function:

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{f_{Di}(s)}{f_{Do}(s)}\right)\left(\frac{1}{H(s)}\right) \tag{2.5.10}$$

The use of a passive attenuator with a non-variable transfer function $\left|H(s)\right|$ in the feedback path would ideally ensure consistency in the system's

transfer function, i.e. to the extent of what is achievable with the reciprocal of $|H(s)|$.

While the frequency dependency in the above signal and transfer function definitions relates to the spectrum of the envelope information, the phase distortion introduced in the envelope information as a result of the phase shifts experienced by the RF carrier signal through the forward and feedback paths have not been taken into consideration. This is justified by the fact, that in an IC circuit implementation of envelope feedback for the processing of CDMA or WCDMA signals (i.e. using base-band signals limited to several MHz), the carrier propagation time delays normally involved are very small compared to the period of the highest frequency component in the envelope information channel or in its adjacent channels.

However, eq. (2.5.10) shows the importance of using precise and linear RF detectors in envelope feedback applications that require the processing of the envelope information over large power dynamic ranges. From one implementation to another, any variation of performance in one or both detectors, and that can be measured as a variation of the ratio $\left(\frac{f_{Di}(s)}{f_{Do}(s)}\right)$, will be reflected as a variation of the system's transfer function characteristics in the same proportion. ***This partly justifies the hardware complexity associated with the envelope feedback implementations that have been proposed to date*** in the literature (e.g. [58]-[59]), and which are ***prohibitive for on-chip GaAs HBT integration*** as in the scope of this work.

Section 2.6
Introducing a Gated Envelope Feedback technique for automatic hardware reconfiguration of RFIC PA's

This section presents a new concept as well as the new RFIC power amplifier architecture introduced in this work.

2.6.1 Problem statement and motivations

The research objectives set in section 2.2 in relation to the hardware reconfiguration of RFIC PA's for current reduction has led, in section 2.3, to identifying and specifying the need for a novel on-chip approach that provides increased autonomy, adaptability and suitability for integration in GaAs technology. It was postulated that the use of a feedback approach would enable such features.

However, the analysis carried out in section 2.5 points to limitations that are inherent to envelope feedback, and helps understand the reasons behind the complexity of the hardware associated with the envelope feedback architectures that have been proposed in the literature for large power dynamic range applications. These embodiments rely on the extensive use of discrete analog and RF components, as well as hybrid distributed structures (e.g. [27]-[28], [58]-[59]), and hence are not suitable for the on-chip implementation goals of this work. The analysis also partly justifies the fact that there has been no published evidence demonstrating the feasibility of single-chip envelope feedback embodiments.

In this work, a new concept related to RFIC PA hardware reconfiguration for current reduction is introduced to meet all the research objectives set in section 2.2. For this purpose, a novel embodiment of envelope feedback is also introduced, and is demonstrated to be suitable for on-chip implementations in GaAs HBT technologies, while being applicable to Bi-CMOS technologies as well. This approach addresses the specific needs pertaining to RFIC PA automatic hardware reconfiguration for current

reduction purposes, as well as the necessity to meet the technological imperatives related to the limitations that are inherent to envelope feedback, and that were analyzed in section 2.5.

2.6.2 Hardware reconfiguration at stepped thresholds within a limited power range

A hardware reconfiguration mechanism intended for current reduction purposes and operating in a stepped fashion at a few discrete power thresholds remains quasi optimally exploited, even if activated only within some limited mid-level power range. This is based on the fact that too many discrete steps between the low-range power levels and the maximum power level would result in considerably more hardware complexity, as pointed out in [43], and the fact that additional circuitry that consumes extra current for the activation of hardware reconfiguration mechanisms at very low power levels does not yield significant efficiency improvement, given the low current consumption and the low probability for the PA of operating at those power levels (see Fig. 1.1.5). Hence, it is possible to define a narrower window within the amplifier's full operating input power range, where it is beneficial to perform hardware reconfiguration, while allowing an almost optimal overall current reduction. The exact span of this window may be optimized through simulation or experimental characterization.

On the basis of this assumption, and in regard to hardware reconfiguration, the technological requirements that normally stem from the inherent envelope feedback limitations (as discussed in section 2.5) may be drastically simplified through a form of windowing of the feedback operation itself within a narrow power dynamic range, thereby restricting the optimum feedback design imperatives to this limited power range only.

2.6.3 Gated Envelope Feedback

Within the scope of achieving all the research goals and minimizing the technological imperatives associated with envelope feedback, a technique that uses a hardware gating function in conjunction with envelope feedback (*Gated Envelope Feedback*) has been investigated.

The method employs an on-chip hardware gating function to condition the envelope feedback operation and, with the help of signal level detection and asynchronous logic, it enables the self-reconfiguration of an RFIC PA hardware in an automatic fashion. It is demonstrated in this research work that the gating function allows for a simplified envelope feedback embodiment as a gain regulation mechanism, requiring the feedback to be effective only across a narrow input power dynamic range, and resulting in drastically simplified PA circuitry and control. In contrast with more complex envelope feedback applications that operate across large power dynamic ranges (e.g. [27], [58]), the gating concept introduced here and the design implementation presented provide ***a clearly defined approach towards integrating a fully functional envelope feedback implementation on a single chip***.

Figure 2.6.1 illustrates the concept of gating an envelope feedback operation on a gain versus input power (P_{in}) curve. To facilitate the description of the concept, a continuous wave (CW) excitation is assumed first. The gating mechanism requires the activation of on-chip circuitry from outside the PA through a single external control line, called the GATE control.

Gating OFF state

In the upper range of P_{in}, the external GATE control signal is kept at logic OFF, which corresponds to a first hardware condition where all the envelope feedback circuit blocks are electrically disabled, with their biasing paths to ground opened and their biasing sections shut off.

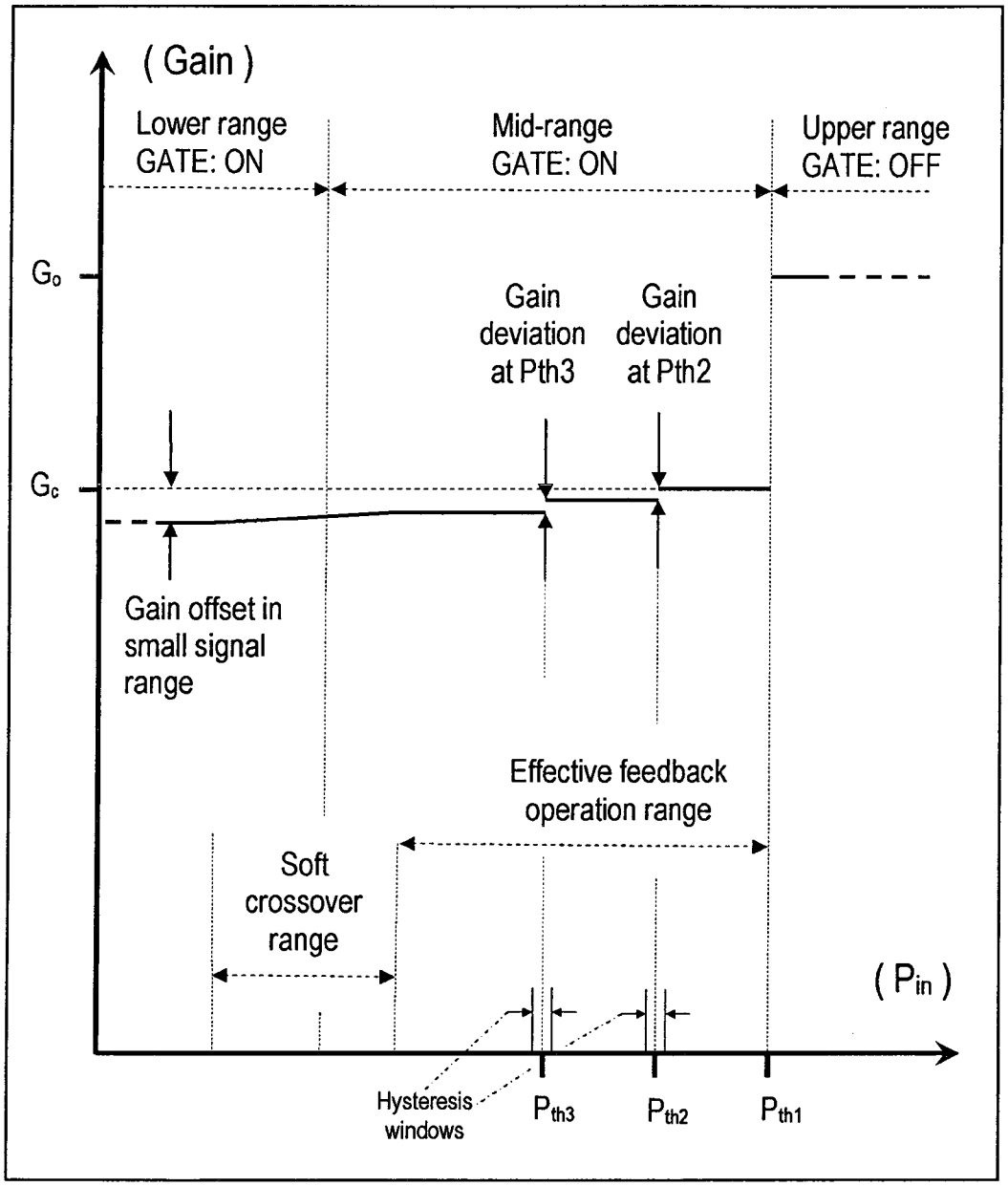

Figure 2.6.1: The gated envelope feedback concept illustrated on a gain versus average input power curve.

Thus, in this first hardware condition, no envelope feedback is applied to the amplifier, and its gain is G_o, i.e. the gain traditionally specified for the

operation of a power amplifier at the higher power range and up to the maximum output power specified.

Gating ON state with automatic switching

As P_{in} decreases and reaches a P_{th1} threshold which is appropriate for hardware reconfiguration, the GATE signal is turned ON, thus physically enabling all the envelope feedback circuitry. In this second hardware condition, the gain of the amplifier system under the feedback dynamics will be automatically set to a value G_c that is typically lower than G_o, and ideally not dependant on temperature, as per the closed loop feedback characteristics. A gain reduction at the mid-range and lower power levels is usually desirable, as it often reduces the level of noise at the output of a transmitter [5]. The detection of the P_{th1} threshold may be achieved with simple hardware circuitry, and with an easy to achieve tolerance in the order of plus or minus 2 dB, thanks to the adaptability that is inherent to feedback. The activation of the GATE signal at P_{th1} is also used to reconfigure parts of the PA's on-chip and off-chip hardware such as biasing and variable impedance matching networks, for the purpose of reducing current.

As P_{in} further decreases and crosses P_{th2}, ***on-chip circuitry*** this time performs ***automatic hardware reconfiguration***. With the help of signal conditioning and sequential logic within the PA chip, the P_{th2} threshold is detected, and a hysteresis comparator ***automatically*** sets a third hardware condition, with a section of the amplifier's output stage (e.g. PS3 and PS4 in Fig. 2.2.1) shut off completely to reduce current consumption. The gain deviation associated with turning off RF transistors is cancelled through the envelope feedback, and the gain is maintained at about G_c. Similarly, the crossing of P_{in} below P_{th3} is detected by the on-chip circuitry, and another hysteresis comparator automatically sets a fourth hardware

condition, with a section of the amplifier's driver stage (e.g. DR2 in Fig. 2.2.1) now shut off completely, and the gain still maintained at about G_c.

Effective feedback operation range and crossover range

The nonlinear gains of the detectors with respect to the power of the input RF signal, as well as the gains of the rest of the feedback loop circuit blocks, are designed to provide a response in power that is tailored to a specific desired sensitivity profile. Thus, as P_{in} continues to decrease, the overall loop gain decays ***in a controlled fashion***, resulting in an optimum transition in the feedback dynamics, defined as a "soft crossover range", from closed loop operation in the mid-range, towards an ***effectively*** open loop mode (i.e with no feedback loop gain) in the lower range. Therefore, this transition acts as ***gating OFF*** the envelope feedback, although the GATE signal is left at the logic ON level. Hence, the gating ON condition is effectively applied to the envelope feedback between P_{th1} and the upper edge of the soft crossover range, and is defined as the "effective feedback operation range".

Optimizing the soft crossover profile and its range as functions of power is critical to meeting the linearity requirements when the system is used for amplifying envelope varying signals (e.g. CDMA). At small signals, the gain offset can be minimized through direct control of the gain of the PA, using the upper voltage levels of the GATE control signal, above the logic ON threshold.

With envelope varying excitations, all threshold levels discussed above would apply to the average RF input power (P_{in_ave}). Thus, the GATE signal is enabled when P_{in_ave} is below the P_{th1} threshold.

Calibration requirements

Gain variations over temperature are automatically cancelled within the effective feedback operation range. Outside this range, where no hardware reconfiguration takes place, typical-behavior look-up tables with

temperature dependant gain correction factors that are measured from a small sample population of the amplifier system are sufficient to compensate against gain variations due to temperature. Hence, assuming the typical temperature dependant gain correction factors are obtained from the developers of the RFIC amplifier component, the method introduced in this work allows the developers of the transmitter to reduce the transmitter gain compensation scheme to only 3 measurement points at room temperature, which correspond to the small signal range, the effective feedback operation range, and the upper range defined in Fig. 2.6.1.

Multi-state conditioning capability with a single control line

While only 3 hardware conditions below P_{th1} are considered here, the method allows for automatic switching between an unlimited number of hardware conditions within the effective feedback operation range with the use of a single control line (i.e. the GATE signal). Furthermore, while the nature of the hardware reconfiguration in this work is driven by the needs for current reduction, the gated envelope feedback principle is applicable as well for automatic hardware reconfiguration and automatic cancellation of gain deviations in implementations that serve different purposes, as long as the reconfiguration mechanisms are triggered within the effective feedback operation range.

2.6.4 Block diagram description

Fig. 2.6.2 illustrates the block diagram of the gated envelope feedback technique that has been investigated and implemented during the course of this work, for the purpose of validating this technique in an amplifier system as a means for automatic hardware conditioning. The signal paths for the processing of the envelope information throughout the envelope feedback system are highlighted in thicker lines.

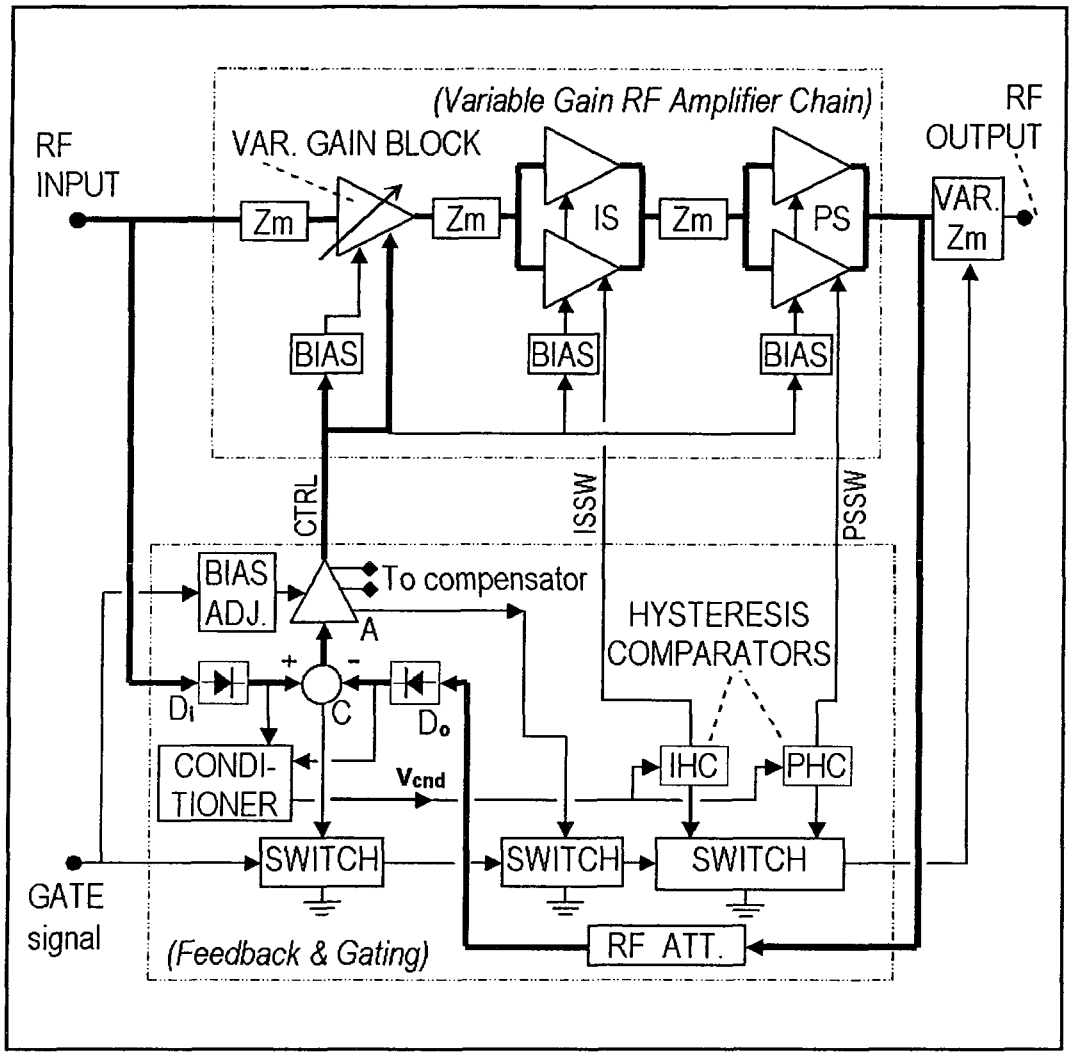

Figure 2.6.2: Block diagram of a gated envelope feedback implementation.

The diagram shows the partitioning of the amplifier system on two GaAs HBT integrated circuit dies. The first die is used for the implementation of a Variable Gain RF Amplifier Chain, and the second die is used as a Feedback and Gating Controller. This partitioning has been used to facilitate the investigation of different sections of the amplifier system.

Variable gain RF amplifier chain IC

The RF amplifier chain is built-up with a cascade of amplifier stages, impedance matching networks and bias sections. The first amplifier stage

(VAR. GAIN BLOCK) is designed to be controlled as the primary variable gain block in the amplifier chain. This is achieved essentially through the control of an electronic attenuator within this amplifier stage, as well as through the control of its biasing current, as functions of the feedback control signal (CTRL).

The second amplifier stage, called the Intermediate Stage (IS), is built-up with two amplifier sections in parallel, with independent bias feeds. Upon activation of the intermediate stage reconfiguration, one of these two sections may be shut off completely by reducing its bias feed current to zero.

The third amplifier stage, called the Power Stage (PS), is built-up also with two amplifier sections in parallel and with independent bias feeds as well. Upon activation of the power stage reconfiguration, one of these two sections may be shut off by reducing its bias feed current to zero. The output impedance of PS is matched with an off-chip variable impedance matching circuit (VAR Zm), which has been implemented in the form of a computer controlled passive Load-Pull tuner for these investigations.

Besides the control of the first stage, some amount of gain variation is achieved through the adjustment of the bias current intensities of the IS and PS stages, as functions of the CTRL feedback control signal. The input impedances of the three amplifier stages are optimally matched to their respective sourcing impedances with the help of LC on-chip impedance matching networks (Zm).

Feedback and gating controller IC

The Feedback and Gating controller is built-up with RF envelope detectors (D_i and D_o), an RF attenuator network (RF ATT.), an envelope signal error comparator (C), an analog amplifier (A) whose output d.c. voltage may be adjusted with the external GATE control signal through a biasing adjustment circuit (BIAS ADJ.), an analog conditioning circuit (CONDITIONER), hysteresis comparator circuits (IHC and PHC), and

switch circuits (SWITCH) that are activated by the GATE signal and placed in bias paths between the circuit blocks C, A, IHC and PHC and the ground of the amplifier system.

The GATE signal uses 0V as logic OFF, 1.5V and above as logic ON, and between 1.8V to 2.8V is used as a gain control for the RF amplifier chain through the adjustment of the output d.c. voltage of the analog amplifier (A).

Open loop operation

When the GATE signal is at logic OFF, all switch circuits are opened, thereby shutting off the circuit blocks C, A, IHC and PHC and forcing them in the hardware state where they do not draw any current. In this state, the feedback control signal CTRL and the hardware reconfiguration signals ISSW and PSSW are automatically pulled down to logic low, in order to allow the variable gain block of the RF amplifier chain to operate with the maximum of gain, and allow all RF sections in both the intermediate stage and the power stage to operate with full quiescent current, hence with maximum gain. The GATE signal at logic low also forces the output variable matching circuit (VAR Zm) to provide optimum large signal loading for power, gain, efficiency and linearity performances.

This condition corresponds to the GATE OFF state illustrated in Figure 2.6.1, and is intended for the open loop mode of operation of the power amplifier system in the upper power range, that is when the input average RF power is above the P_{th1} level illustrated in the same figure.

Feedback operation

When the GATE signal is at logic ON, the electronic switches in Fig. 2.6.2 sink the bias currents of the circuit blocks C, A, IHC and PHC, allowing these circuit blocks to be functional, and hence enabling the envelope feedback and gating mode of operation. The input RF envelope detector D_i provides a measure of the envelope amplitude of the RF signal that is

applied to the input of the amplifier system. The analog signal at the output of D_i is applied to the non-inverting input of the envelope error comparator C, as the reference envelope information within the feedback system.

The RF signal delivered at the output of the power stage is first attenuated by the RF attenuator network. After attenuation, the amplitude of its envelope is detected by the output RF envelope detector D_o. The analog signal delivered by D_o is applied to the inverting input of comparator C, as the feedback envelope information within the closed loop control system.

The analog signal at the output of comparator C, resulting from the comparison between the reference and feedback envelope information, is amplified through the analog amplifier A, and then used as the feedback control signal for the dynamic adjustment of the gain of the Variable Gain RF Amplifier Chain. The above signal flow description corresponds to a closed loop feedback structure that conditions the envelope amplitude of the RF signal at the output of the amplifier system as a function of the envelope amplitude of the RF signal that is applied to the input of the amplifier system. In an ideal feedback operation mode, the envelope amplitude at the output is linearly magnified with respect to the envelope amplitude at the input.

Activation of the gating ON condition

The synchronous activation of the gating ON condition is accomplished by switching the GATE signal level from logic OFF to logic ON, thereby enabling the envelope feedback circuitry and operation with the help of the SWITCH circuits shown in Figure 2.6.2. Only an estimate of the input average RF power (P_{in_ave}) from outside the power amplifier system is required to determine when this power crosses below the P_{th1} threshold, which corresponds to the power level where it becomes appropriate for synchronously enabling the hardware reconfiguration mechanism. Due to the adaptability feature of the feedback system, this threshold may vary

within a range of approximately plus or minus 2dB, thereby relaxing significantly the precision required on the external power detection for the decision making in activating the GATE signal.

The GATE signal is used also to trigger the reconfiguration of the variable output matching circuit (VAR. Zm) in order to provide optimum loading for power, gain, efficiency and linearity performances - this time as a function of the impedance matching requirements that are proper to the operation of the amplifier at mid-range power levels.

Automatic hardware reconfiguration

The reference envelope signal delivered by D_i is also applied to the CONDITIONER circuit, which acts as a buffering circuit, and at the same time scales this analog signal to voltage levels on the V_{cnd} conditioned signal line (Fig. 2.6.2) that are appropriate for optimum operation of the hysteresis comparators.

When the GATE signal is at logic high, and thus enables the operation of the hysteresis comparators IHC and PHC, which also include RC integrator circuits, each one of the ISSW and PSSW switching signals is allowed independently to toggle when the average of the V_{cnd} signal crosses ***above*** or ***below*** two different narrow voltage ranges. Each one of these two voltage ranges corresponds to a hysteresis power window of about 2dB at the input of the amplifier system, and the two hysteresis power windows are centered across the P_{in_ave} thresholds corresponding to the P_{th2} and P_{th3} levels (Fig. 2.6.1). The time constants of the integrators together with the use of the hysteresis windows prevent the hardware reconfiguration from being triggered continuously by amplitude variations or noise in the reference envelope signal.

When P_{in_ave} crosses below the P_{th2} hysteresis window, the PSSW signal is automatically set to logic high in order to shut off half of the RF transistor array in the power stage PS, through the deactivation of the corresponding bias circuit. Inversely, when P_{in_ave} crosses above the P_{th2}

hysteresis window, the PSSW signal is automatically set to logic low in order to restore the full usage of the RF transistor array in the power stage. In the same fashion, the ISSW signal is automatically set to logic high when P_{in_ave} crosses below the P_{th3} hysteresis window, and to logic low when P_{in_ave} crosses above the P_{th3} hysteresis window, which correspond to the conditions where half of the RF transistor array in the intermediate stage is shut off, and the condition where the full array is operational, respectively.

2.6.5 Design specifics for an embodiment in GaAs HBT technology

A full on-chip embodiment of the envelope feedback architecture of Fig. 2.6.2 in a GaAs HBT technology requires necessarily careful trade-offs between circuit complexity and performance, because of the low integration capabilities of this technology, which implies design requirements that have to be taken into consideration early on.

In particular, for the validation of the envelope feedback technique in this work, the RF detectors D_i and D_o have been designed as single stage NPN transistor amplifiers that are biased in deep class AB [8] (as will be discussed in details in a later section), with the filtered collector envelope voltage used as a measure of the RF envelope power. Such a simple detector structure, which does not include any form of logarithmic scaling, provides necessarily a low sensitivity in the conversion gain at low RF power levels, as well as an abrupt variation of the detected signal at higher power levels. This translates into ***a narrow usable dynamic range*** of the envelope power to be measured. Moreover, such a detector has a ***strongly nonlinear*** RF to analog conversion gain, and its low sensitivity at low power levels drastically reduces the feedback open loop gain.

The design imperatives in regard to the above RF detector performance limitations may be deduced from the envelope feedback transfer functions formulated in section 2.5.

Gain variations with power

From eq. (2.5.8) through eq. (2.5.10), it may be seen that an open loop gain term $|A_v(s)P(s)G(s)f_{Do}(s)H(s)|$ that is significantly reduced with a decreasing power level, as a consequence of a decreasing detector sensitivity, will result in a potentially drastic change in the overall transfer function of the amplifier system.

Starting from the condition where the detectors are driven with a high level RF signal and assuming that $|f_{Do}(s)|$ is high enough to maintain a large loop gain, the amplifier system presents the gain transfer function that reflects the ***effective feedback operation range*** design optimization referred to in Fig. 2.6.1, according to

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{f_{Di}(s)}{f_{Do}(s)}\right)\left(\frac{1}{H(s)}\right)$$

As the power decreases and $|A_v(s)P(s)G(s)f_{Do}(s)H(s)|$ is significantly reduced, the gain transfer function is subject to the ***crossover range*** referred to in Fig. 2.6.1, where the forward conversion gain $F(s)$ becomes influential, as defined by the first term of eq. (2.5.9).

When the open loop gain term $|A_v(s)P(s)G(s)f_{Do}(s)H(s)|$ and $|f_{Di}(s)|$ in eq. (2.5.8) are zeroed by the lack of sensitivity in the detectors, the resulting gain in the ***small signal range*** becomes

$$\frac{V_{out}(s)}{V_{in}(s)} = F(s)G(s) \qquad (2.6.1)$$

Hence, the gain variation of the amplifier in scalar terms across the three ranges is bounded by the highest maximum and the lowest minimum reachable with expressions (2.5.9), (2.5.10) and (2.6.1).

Nonlinearity introduced by the RF power detectors

Besides the amount of gain variation with power, the profile and rate of change of the detectors' conversion gains also have a predominant effect within the ***crossover range***. According to the term

$$\frac{F(s)G(s)}{1+A_v(s)P(s)G(s)f_{Do}(s)H(s)}$$

in eq. (2.5.8), any nonlinear variation in the conversion gain $f_{Do}(s)$ as a function of power within the crossover range will be reflected in the amplifier's gain. The symmetry between the detectors' conversion gains also has important implications. The term

$$\left(\frac{f_{Di}(s)}{f_{Do}(s)}\right)$$

in eq. (2.5.10) indicates that in the upper region of the crossover range, if the nonlinear conversion gains $f_{Di}(s)$ and $f_{Do}(s)$ vary in a symmetrical fashion so that their ratio remains constant, then their nonlinearities are not reflected in the gain transfer function of the amplifier. This is not the case, however, when the quantity $|A_v(s)P(s)G(s)f_{Do}(s)H(s)|$ in eq. (2.5.8) approaches unity in the lower region of the crossover range, since ***even identical nonlinear variations in the two detectors will introduce nonlinearities*** in the amplifier's transfer function.

Design guidelines for optimally flat gain response over power

In order to maintain an optimally flat gain response over power in a gated envelope feedback amplifier, hence a linear response across the effective feedback operation range, the crossover range, and the small signal

range, the following design guidelines may be deduced from the above analysis.

(i) Appropriate circuitry is required to adjust the gain at low power, in order to obtain a minimum of small signal gain deviation (Fig. 2.6.1); this implies adjusting $|F(s)G(s)|$ between the boundary values defined by eq. (2.5.9) and (2.5.10), i.e. a small signal gain tuning range that covers at least

$$|F(s)G(s)| = \left| \frac{F(s)}{A_v(s)P(s)f_{Do}(s)H(s)} + \left(\frac{f_{Di}(s)}{f_{Do}(s)}\right)\left(\frac{1}{H(s)}\right) \right| \qquad (2.6.2)$$

and

$$|F(s)G(s)| = \left| \left(\frac{f_{Di}(s)}{f_{Do}(s)}\right)\left(\frac{1}{H(s)}\right) \right|, \qquad (2.6.3)$$

which have to be evaluated across the full usable input power range and under all load, temperature and other operating conditions.

(ii) The influence of the nonlinear conversion gains of the RF detectors on the amplifier's transfer function must be minimized by keeping the ratio of their conversion gains as a function of frequency and power as constant as possible, which means that the input and output detector circuits have to be matched in performance as much as possible.

(iii) Besides how well matched the detector circuits are, the profiles of their conversion gains must present the lowest rate of change with respect to power within the crossover range in particular, in order to introduce the minimum of nonlinearity at the output.

Section 2.7

Multi-tone IMD analysis of an envelope feedback system

This section introduces a design equations based approach for IMD analysis in an envelope feedback amplifier system, as a function of system parameters, a multi-tone input excitation, and the overall inter-modulation product levels desired at the output of the closed loop amplifier system. The need for such design equations is first highlighted. Basic formulations of the Volterra series for linearity analysis are then briefly reviewed for the purpose of highlighting the difficulty in applying this otherwise robust and very general small signal analytical tool with such a complex nonlinear system as a gated envelope feedback system, and thus to show the pertinence of deriving simpler design equations that are ***conditional*** to known and quantifiable restrictions and assumptions. The proposed design equations will be used in IMD analyses in later sections.

2.7.1 The need for simulation independent linearity analysis methods

The importance of carefully optimizing the conversion gain profile and range of the nonlinear RF envelope detectors, thereby inducing a soft crossover range that acts as an automatic gating off mechanism in a gated envelope feedback system, was discussed in section 2.6. The feedback dynamics across both the soft crossover range and the effective feedback operation range was analyzed with a small signal transfer function approach in regard to the minimization of the amount of nonlinear effects that are reflected at the output of the amplifier and that originate from the envelope detectors. This is critical for compliance with linearity requirements when amplifying modulated signals (e.g. CDMA). It was also discussed that the RF envelope detector topologies that would be suitable for single-chip integration in GaAs HBT technology would potentially present strongly nonlinear characteristics. In the light of the above, the design of the gating function circuitry for a gated envelope feedback

implementation clearly should benefit from a computer aided approach that makes use of optimization algorithms within a circuit simulation environment, and function of a modulated input excitation.

However, there is also a need for an approach allowing the study of the nonlinear effects in the feedback system in an analytical form, and ***independently from the optimization algorithms of a circuit simulation tool***.

The pertinence of design equations in the design and simulation phases

The use of a design equations based approach, independently from optimization through simulation, to determine distortion characteristics throughout the envelope feedback system provides valuable insight to the designer. Although the actual linearity performance of the amplifier system will be function of the envelope variations that are proper to the modulated signal used, linearity analysis based on a multi-tone excitation, for example, remains a valuable approach because it allows more easily identifying trends and nonlinear relationships with analytical formulations. Design equations may also prove helpful in circumventing convergence problems that may be encountered during simulation, as these equations may be used to develop behavioral models that allow avoiding simulation with sections of the system where strongly nonlinear analog or digital circuits impose severe constraints on the harmonic balance convergence process. In the course of the simulation of the gated envelope feedback embodiment illustrated in Fig. 2.6.2, severe convergence problems were encountered and were attributed to the switching off of sections in the RF transistor arrays and to the operation of the hysteresis comparators.

The pertinence of design equations in an experimental environment

The use of design equations may also be of particular interest as a circuit characterization, a design adjustment and an experimental optimization tool outside the circuit simulation environment. One rationale in support of this statement is the difficulty the designer is likely to face while trying to perform a design validation on each feedback loop building block while the complete system is in closed loop operation. With an envelope error signal amplitude in the order of only a few millivolts, the difficulty is heightened by the probing of the RF and envelope feedback signals for characterization purposes. RF noise induced through the probing interface and, as a result, interaction between the RF noise injected and the analog circuits may steer the operation conditions away from the simulated conditions and possibly induce instability, and thus may prevent accurate characterization.

Moreover, simulation may not always allow predicting to what degree the performance matching of the RF detectors, as one of the critical design aspects discussed in section 2.6.5, may be achieved. Also, the effects from an imbalance between the two detector circuits or between the two error comparator inputs, as a result of layout sensitive considerations such as asymmetrical RF coupling through the substrate, may not always be modeled accurately. Hence, simulation may not always allow predicting the actual level of inter-modulation that is ***added*** in the error signal path (i.e. between the envelope detectors' outputs and the CTRL control line in Fig. 2.6.2), as a result of a lack of performance matching in the envelope detection paths.

For all of the above practical reasons, design equations that facilitate the linearity performance validation of each individual circuit block ***separately*** through experimental characterization as well as their design adjustment in an ***open loop*** condition, but as a function of the overall ***closed loop*** linearity performance goals may then become a very useful complementary approach to simulation.

2.7.2 The use of the Volterra series and power series for the analysis of weakly nonlinear systems

The application of the Volterra series and power series to the analysis of weakly nonlinear systems [60]-[61] is briefly reviewed in this subsection, based on the formulations provided in [60], but with emphasis here on highlighting the difficulty of defining the nonlinear transfer functions in a complex system such as a gated envelope feedback embodiment.

Systems with inseparable linear reactive elements and memoryless nonlinear elements

The general case of a weakly nonlinear system containing two inseparable groups of elements: (i) resistive nonlinear elements (i.e. having voltage and current relationships that do not depend on time dependent initial conditions), and (ii) reactive nonlinear elements (i.e. with memory effects due to electric charge storage or magnetic flux storage), is represented in Fig. 2.7.1.

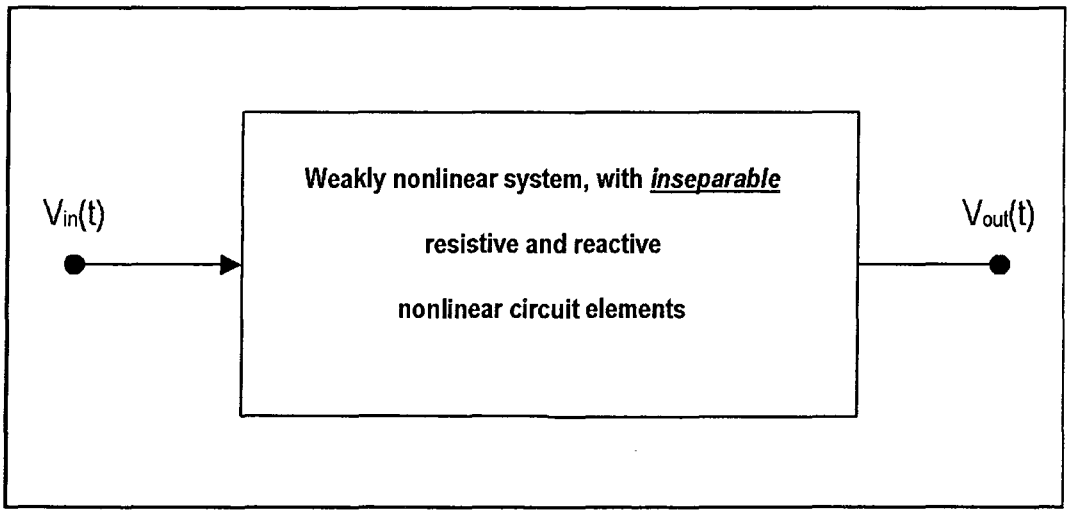

Figure 2.7.1: Weakly nonlinear system with inseparable resistive and reactive elements.

It is assumed that no d.c. component is present at the input and at the output of the system, and that the input signal $V_{in}(t)$ is a multi-tone signal made up of a quantity Q of sinusoidal signals at frequencies $\omega_1, \omega_2, ...\omega_q$ that are non-commensurate (i.e. the ratio between any two of them yields a number that is not rational), which guarantees that any mixing product at the output of the system derived from these tones will be at a distinct frequency. Using Euler formula: $e^{j\theta} = \cos\theta + j\sin\theta$, a sinusoidal signal may be represented by a sum of complex exponential functions, and accordingly the input multi-tone signal may be represented by

$$V_{in}(t) = \frac{1}{2}\sum_{\substack{q=-Q \\ q\neq 0}}^{Q} V_{in\_q}(t)\, e^{(j\omega_q t)} \qquad (2.7.1)$$

with $\omega_{-q} = -\omega_q$, and $V_{in\_(-q)} = V^*_{in\_(q)}$ (i.e. the complex conjugate).

It may then be shown through the Fourier transforms of multi-dimensional convolution functions [61] that the response at the output of the nonlinear system to a small-signal input excitation is in the form of

$$V_{out}(t) = \sum_{n=1}^{N} \frac{1}{2^n} \sum_{\substack{q1=-Q \\ q1\neq 0}}^{Q} \sum_{\substack{q2=-Q \\ q2\neq 0}}^{Q} ..... \sum_{\substack{qn=-Q \\ qn\neq 0}}^{Q} V_{in\_q1}(t) V_{in\_q2}(t) ..... \\ ... V_{in\_qn}(t) \cdot H_n(\omega_{q1}, \omega_{q2}, ..., \omega_{qn}) \cdot e^{[j(\omega_{q1}+\omega_{q2}+.....+\omega_{qn})t)]} \qquad (2.7.2)$$

with $H_n(\omega_{-q}) = H_n^*(\omega_q)$, and N being the highest order required to represent the nonlinear response of the system with the desired precision. The term $H_n(\omega_{q1}, \omega_{q2}, ..., \omega_{qn})$ represents an n^{th} ***order nonlinear transfer function***, with n being an element of the set $\{1,2,.....,N\}$. A

particular case is the first order of this transfer function, which yields distinct linear functions that depend on the excitation frequency, that is $H_1(\omega_1)$, $H_1(\omega_2)$,....., $H_1(\omega_n)$ individually and distinctively defined at the frequencies ω_1 , ω_2 ,....., ω_n , respectively, in conformity with the superposition theorem that is proper to any linear transfer function. For any given order n superior than one, the corresponding n^{th} order transfer function represented by $H_n(\omega_{q1},\omega_{q2},.....,\omega_{qn})$ defines a series of $(2Q)^n$ complex gain terms that are associated with the $(2Q)^n$ mixing product frequencies. These gain terms may be grouped in complex conjugate pairs, which may individually be associated with a real time waveform in the output signal at a particular mixing frequency. Some of these frequencies are harmonics of the input tones, and the others may be related to algebraic combinations of the input excitation frequencies.

Any n^{th} order transfer function $H_n(\omega_{q1},\omega_{q2},.....,\omega_{qn})$ is made up of a combination of linear and nonlinear lower order transfer functions, which themselves are combinations of even lower order functions, and so forth. For example, with a two-tone excitation (i.e. $Q=2$), the 2^{nd} order transfer function represented by the expression $H_2(\omega_1,\omega_2)$ is a combination of $H_1(\omega_1)$ and $H_1(\omega_2)$. In general, any n^{th} order nonlinear function represented by $H_n(\omega_{q1},\omega_{q2},.....,\omega_{qn})$ may not necessarily be simplified to a simple product of terms that individually depend on a single and distinct frequency (i.e., for example, in the above 2^{nd} order case, the term $H_2(\omega_1,\omega_2)$ may not necessarily be reduced to the product of the distinct transfer functions $H_1(\omega_1)\cdot H_1(\omega_2)$). Hence, in general, the key to the applicability of the Volterra series is the feasibility of determining a single-function nonlinear expression $H_n(\omega_{q1},\omega_{q2},.....,\omega_{qn})$ for every transfer function of order n higher than the 1^{st} order.

Systems with separable linear reactive elements and memoryless nonlinear elements

Fig. 2.7.2 illustrates the case of a weakly nonlinear system in which the circuit elements may be separated into two cascaded blocks: a linear network including all reactive elements of the system, followed by a ***quasi-static*** (i.e. whose nonlinear elements are described by nonlinear functions that change instantaneously with their voltage or current control variables) and ***memoryless*** (i.e. that does not contain any charge or flux storage element) nonlinear network.

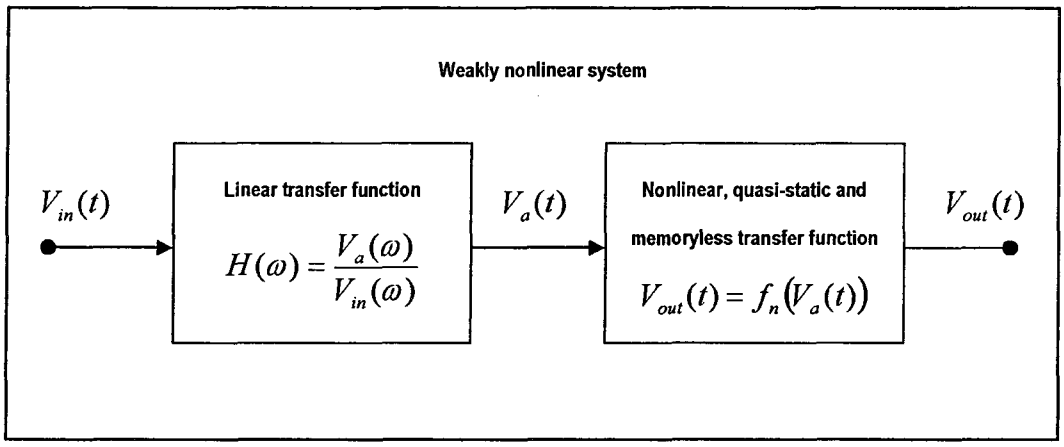

Figure 2.7.2: Representation of a weakly nonlinear system as a circuit block with all reactive elements of the system, followed by a circuit block containing quasi-static and memoryless nonlinear elements only.

As in the case of any weakly nonlinear, quasi-static, and memoryless network, the nonlinear transfer function $f_n(V_a(t))$ may be represented by a ***power series*** of the form [60]:

$$f_n(V_a(t)) = \sum_{n=1}^{N} a_n V_a^n(t) = a_1 V_a(t) + a_2 V_a^2(t) + ... + a_N V_a^N(t) \qquad (2.7.3)$$

where N is the highest degree required in eq. (2.7.3) to represent $f_n(V_a(t))$ with the desired precision.

Considering the same multi-tone input excitation represented by eq. (2.7.1), it may be shown [61] by applying eq. (2.7.1) to the linear transfer function representing the linear part of Fig. 2.7.2, and then substituting the result in eq. (2.7.3), that the output response is in the form

$$V_{out}(t) = \sum_{n=1}^{N} \frac{a_n}{2^n} \sum_{\substack{q1=-Q \\ q1\neq 0}}^{Q} \sum_{\substack{q2=-Q \\ q2\neq 0}}^{Q} ..... \sum_{\substack{qn=-Q \\ qn\neq 0}}^{Q} V_{in\_q1}(t)V_{in\_q2}(t)..... \quad (2.7.4)$$
$$...V_{in\_qn}(t)\cdot H(\omega_{q1})\cdot H(\omega_{q2})\cdot(.....)\cdot H(\omega_{qn})\cdot e^{[j(\omega_{q1}+\omega_{q2}+.....+\omega_{qn})t)]}$$

By comparing eq. (2.7.2) and eq. (2.7.4), it may be deduced that the ***power series*** formulation of eq. (2.7.4) is a particular case of the generalized ***Volterra series*** of eq. (2.7.2), i.e. with the n^{th} order nonlinear function $H_n(\omega_{q1},\omega_{q2},.....,\omega_{qn})$ from eq. (2.7.2) replaced by a product of linear transfer functions of the form $a_n\cdot H(\omega_{q1})\cdot H(\omega_{q2})\cdot(.....)\cdot H(\omega_{qn})$, and a_n being the n^{th} order polynomial coefficient associated with $f_n(V_a(t))$ as per eq. (2.7.3).

Discussion on the general application of the Volterra and power series

From the above formulations, the main difficulty in using the Volterra series for determining the response of a weakly nonlinear system to a multi-tone excitation is to obtain the series of $(2Q)^n$ complex gain terms represented by $H_n(\omega_{q1},\omega_{q2},.....,\omega_{qn})$ in eq. (2.7.2). Each n^{th} order nonlinear transfer function in the frequency domain may theoretically be obtained [60]-[61] through the Fourier transform of the n^{th} order *nonlinear*

impulse response $h_n(\tau_1,\tau_2,...,\tau_n)$ in the multidimensional convolution function of the form

$$
\begin{aligned}
&V_{out}(t) = \\
&\int_{-\infty}^{\infty} h_1(\tau_1)V_{in}(t-\tau_1)d\tau_1 \\
&+ \int\int_{-\infty}^{\infty} h_2(\tau_1,\tau_2)V_{in}(t-\tau_1)V_{in}(t-\tau_2)d\tau_1 d\tau_2 \\
&\cdot \\
&\cdot \\
&\cdot \\
&+ \int\int...\int_{-\infty}^{\infty} h_n(\tau_1,\tau_2,...,\tau_n)V_{in}(t-\tau_1)V_{in}(t-\tau_2)...V_{in}(t-\tau_n)d\tau_1 d\tau_2...d\tau_n
\end{aligned}
\qquad (2.7.5)
$$

As a foundation of the Volterra series, eq. (2.7.5) is an extension of the 1^{st} order convolution integral (which is the first integral in eq. (2.7.5)) that is applicable to linear systems, and applied to nonlinear systems under the assumption that the input excitation is small enough and that the system's nonlinearities are weak enough to guarantee the convergence of the series. It is used to relate the input excitation $V_{in}(t)$ and any of the n^{th} order nonlinear impulse response $h_n(\tau_1,\tau_2,...,\tau_n)$ to the resultant n^{th} order time domain output response $V_{out\_n}(t)$, or to find the total output response $V_{out}(t)$ function of any given order n considered to represent the system, as expressed by the complete series in eq. (2.7.5).

Hence, an analytical approach for determining the response of the system represented by Fig. 2.7.1 to a multi-tone excitation based on the Volterra series is rendered difficult mainly due to the necessity of defining the nonlinear transfer function $H_n(\omega_{q1},\omega_{q2},.....,\omega_{qn})$ in eq. (2.7.2), which may be subject to not only very elaborate mathematical manipulations that

become practically unhelpful as the order n increases even moderately, but also subject to the condition that an analytical representation of the system is available. Furthermore, the requirement for non-commensurate frequencies to define the input excitation may render simulation tasks using Volterra series based behavioural models time consuming, because of the inconvenience of choosing the frequencies, and possibly the difficulty associated with the non-periodic time-waveforms.

When the nonlinear system may be reduced to the representation of Fig. 2.7.2, the process of determining an n^{th} order nonlinear response (i.e. the solution from eq. (2.7.4) with any specific value n) is more accessible in that the dependence of each linear function $H(\omega_{qn})$ in eq. (2.7.4) on frequency is distinct at the specific frequency ω_{qn} considered, and the complete n^{th} order response is built up with products of these linear functions. However, this still requires that the analytical representation of the linear block of Fig. 2.7.2 be available, or alternatively be found by experimentation. Also, the polynomial coefficients a_n still need to be determined from an analytical model of the memoryless nonlinear elements of the system, unless they may alternatively be determined through experimentation. The latter case would imply that an experimental characterization of $V_{out}(t)$ as a function of $V_a(t)$ is practically feasible, which poses the potentially very difficult to meet necessity that the nonlinear memoryless circuit elements be physically separated from the linear block, as per the representation of the system in Fig. 2.7.2.

Discussion on the application to an envelope feedback system

Based on the above observations, the more efficient way to obtain an accurate model of a moderately complex but weakly nonlinear circuit structure with analytical formulations would be to obtain first its equivalent representation as depicted in Fig. 2.7.2. This is achievable only with circuit

structures containing well defined nonlinear models, such as circuits employing only few transistors and that are biased in conditions where their model elements are accurately predictable, or at least where the model topologies are accurately defined. In the latter case, the focus of the analysis could be at least on observing trends in the performance versus structural elements, rather than actual performance values. However, even this would be clearly unfeasible in practical terms in the case of such a complex system as a gated envelope feedback system. The separation of all elements that contribute to memory effects from the rest of the active nonlinear elements in a system like the one represented in Fig. 2.6.2, even by considering only the circuit blocks in the envelope feedback paths, would be so laborious that it would render the approach unhelpful, compared to what may be achieved by simulation.

The above observations on the application of the Volterra series point to the pertinence of making use of design equations that allow the designer to carry out ***simplified analyses*** based on ***known and quantifiable approximations***. This should enable easier and quicker ***estimates*** of the linearity performances achievable in an envelope feedback system based on known system parameters, on the excitation conditions, and on the desired linearity performances at the output of the system, and therefore could be used efficiently as a truly helpful equations based complementary approach to simulation.

This rationale can be used as a prelude to the introduction of simplified multi-tone excitation based design equations for the IMD analysis of envelope feedback RF amplifier systems in the following sections.

2.7.3 Introducing a behavioural model and a design equations based methodology for estimating the IMD performance requirements in the error signal path of an envelope feedback amplifier system

In [58], expressions are provided (equations (2) to (7)) to describe a two-tone signal within an envelope feedback amplifier in a form that is limited only to the symbolic representation of the squaring and cubing of the excitation envelope signal, but not as a function of the resulting two-tone and IMD product levels and their distinct frequencies. Also, these expressions are only representative of the hypothetical condition wherein the feedback correction process has not started, and thus do not express a closed loop steady-state solution.

Also, while a two-tone input excitation is commonly used for inter-modulation analysis (e.g. [8], [58], [60], [61], [62], [63]), it may not always suit linearity analyses that require limited envelope variations that modulate large input carrier signals. In the case of the gated envelope feedback in particular, because of the critical gain alignment requirements between the small signal range, the crossover range and the feedback operation range (Fig. 2.6.1), there may be an interest for a linearity analysis that is localized in the power domain, i.e. which allows evaluating the distortion in the envelope signal when it sweeps across a given narrow span anywhere along these three power ranges. This may allow one, for example, to distinguish the nonlinear effects introduced by the RF envelope detectors in the upper region of the crossover range, from those introduced in the lower region, as discussed in section 2.6.5.

For these reasons, the IMD analysis presented here is based on a behavioral model of an envelope feedback system using a three-tone input excitation that is equivalent to an AM modulated signal, in order to facilitate the consideration of various peak-to-average ratios of the envelope signal when analyzing the gating function, together with the convenience of a symmetrical frequency spectrum as well as envelope

amplitudes that can be parameterized as input variables. This allows considering envelope variations ranging from the case of zero peak-to-peak amplitude (i.e. the case of a zero AM modulation percentage), to the case of a 6dB peak-to-average ratio and total collapse of the envelope (i.e. the case of a 100% AM modulation). Hence it is more suitable for analyses that are localized in the power domain and based on the assumption of small peak-to-average variations, compared to the fixed envelope variation of an equal-amplitude two-tone analysis.
Moreover, the design equations that are derived are aimed at solving a closed loop steady-state response to a three-tone excitation, hence for determining the IMD levels at any node within a typical envelope feedback amplifier architecture, subject to some approximations.

Behavioural model for IMD analysis of an envelope feedback system

Fig. 2.7.3 will be used as a behavioral model representing the envelope signal path that is highlighted in the gated envelope feedback architecture of Fig. 2.6.2 (excluding all switched control circuitry) with some simplifications that will be justified in the following sections. The frequency content of the three-tone input excitation (i.e. ω_c, $\omega_c \pm \omega_x$), as well as that of the output three-tone signal and some of the associated IMD products (i.e. ω_c, $\omega_c \pm \omega_x$, $\omega_c \pm 2\omega_x$, $\omega_c \pm 3\omega_x$, and $\omega_c \pm 4\omega_x$), are illustrated with frequency domain spectrum that are centered at the RF carrier frequency ω_c. The frequency content of the down-converted envelope error signal (V_e) is illustrated with a single side-band frequency domain spectrum that is centered at 0 rad/s. This behavioral model, together with the design equations that will be derived and the proposed methodology for the estimation of IMD performance requirements in the error signal path (which includes the envelope detectors, the error comparator, and the analog error amplifier shown in Fig. 2.6.2) are governed by some assumptions and approximations, which are described next.

Memoryless and quasi-static behaviour assumption

The use of a three-tone excitation with limited frequency spacing ensures that a memoryless and quasi-static assumption [60] can be made. The associated condition is that the highest order mixing product considered in the envelope signal path (i.e. the $4\omega_x$ mixing product in the frequency spectrum of the error signal V_e in Fig. 2.7.3) be small enough compared to any cutoff frequency in the amplifier system's open loop envelope frequency response, so that the phase shifts may be neglected.

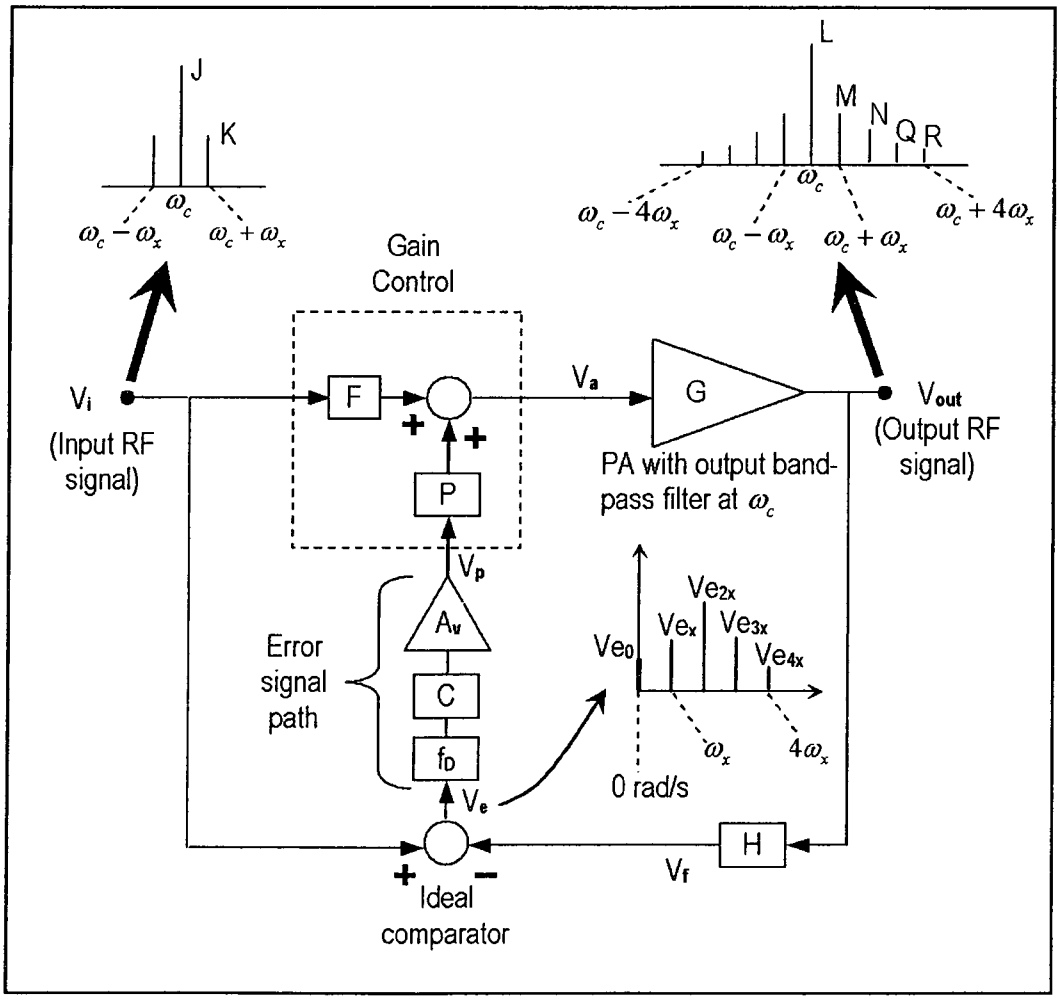

Figure 2.7.3: Block diagram representing a behavioural model for multi-tone IMD analysis of an envelope feedback based RF amplifier.

Approximation for the gain control function

The design equations and proposed methodology for IMD analysis are also subjected to the condition that the variable gain function of the RF amplifier chain (Fig. 2.6.2) may be approximated with a gain control element (Fig. 2.7.3) which has a gain or attenuation factor F at its input and a gain control sensitivity P, followed by a PA amplifier block (G in Fig. 2.7.3) that is defined with a power series and that has an ideal band-pass filter centered at the carrier frequency ω_c at its output. Note that, typically, the output signal V_{out} in Fig. 2.7.3 corresponds to the node between the output RF transistor array in the RF amplifier block and the output matching network (not shown). Hence, the frequency selective loading effect of the output matching network provides the band-pass filtering function.

The approximation for the gain control element may be justified with the help of Fig. 2.7.4, which represents, in (a), a variable gain RF amplifier chain, the envelope amplitude V_{ae} of the RF signal V_a at its input, the envelope amplitude V_{oe} of the RF signal V_{out} at its output, and the gain control signal V_p.

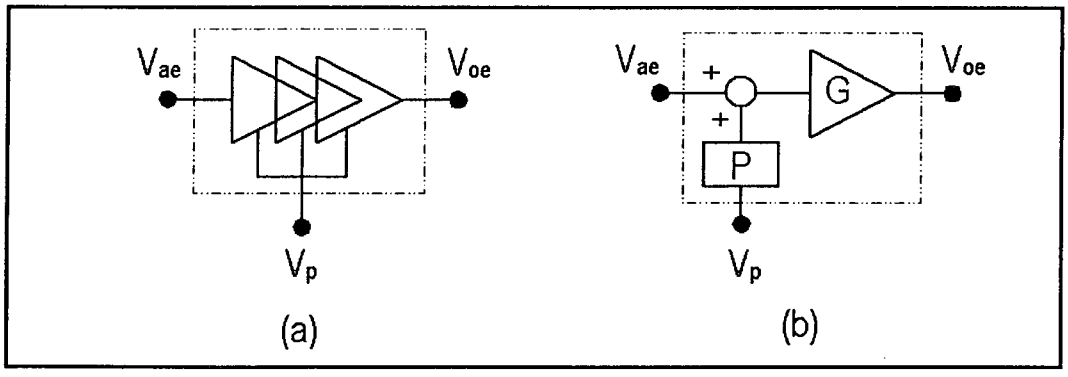

Figure 2.7.4: A variable gain amplifier chain in (a), with a gain control signal V_p, and an approximate model in (b), assuming small variations in V_{ae} and V_p.

We consider a *small* adjustment of V_p in Fig. 2.7.4 (a), which translates into a small variation in V_{oe}, for any given amplitude V_{ae} within some range. Given a memoryless AM-AM model (represented by G in Fig. 2.7.4 (b)) that allows closely approximating the relation between V_{ae} and V_{oe} *after* the gain adjustment, then the small variation in V_{oe} as a result of the small gain adjustment may be referred at the input with a small change in V_{ae}, defined by an incremental quantity ΔV_{ae} that depends on V_p and a gain control parameter P, as illustrated in Fig. 5 (b).
The limitations from this approximation may be understood with the help of Fig. 2.7.5.

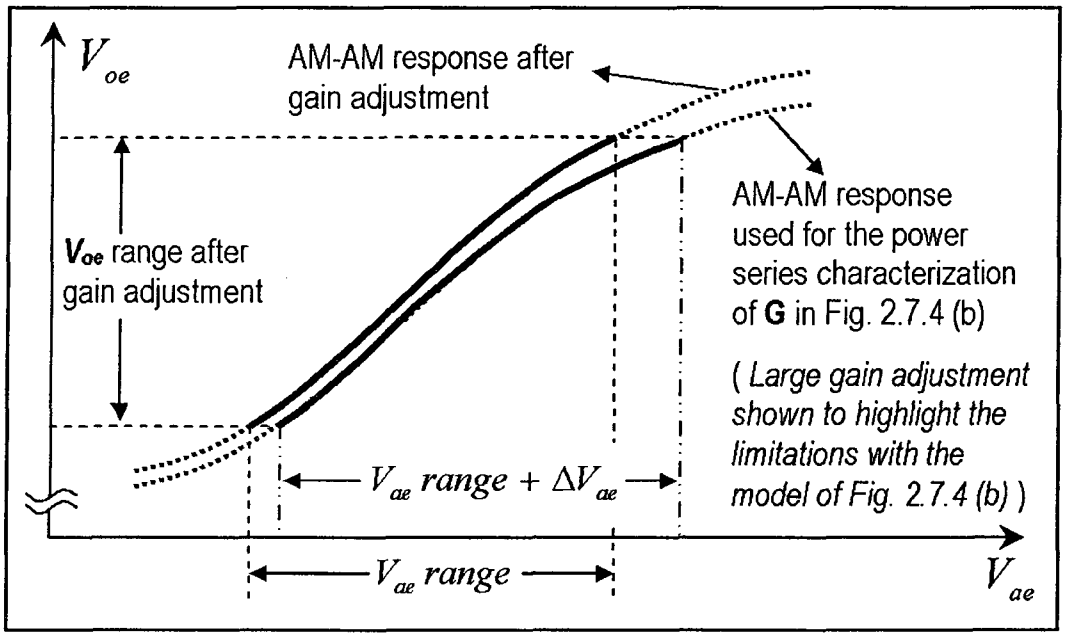

Figure 2.7.5: AM-AM curves illustrating the limitations of the model in Fig. 2.7.4 (b).

The bottom curve represents the AM-AM response used for the characterization of G with a power series, and at a given quiescent condition on V_p. The top curve represents the AM-AM response after a

small change in the gain as a result of a small increment in V_p, which translates into a change in the V_{oe} range, for the same V_{ae} range considered at the input. It can be seen from Fig. 2.7.5 that as the change in the gain is increased, the representation of the V_{oe} signal (associated with the solid line segment on the top curve) with the solid line segment on the AM-AM curve which is used to define G becomes less accurate. Therefore, this approximation is conditional to operating conditions where the d.c. value of the control signal V_p is very close to the quiescent value of V_p used for the power series characterization of G, to small a.c. amplitudes of V_p, and to limited excursions in V_{ae}.

This approximation of the effects of a small gain adjustment through feedback in the amplifier chain allows drastically simplifying the formulation of the design equations. Accordingly, the envelope amplitude V_{ae} of the signal V_a at the output of the gain control element is considered as being built up with a quantity which is proportional to the input envelope signal (i.e. $F \cdot V_{ie}$) added to an incremental amplitude adjustment quantity ΔV_{ae} that is introduced through the feedback operation, as represented by the summation symbol in Fig. 2.7.3. Moreover, this incremental amplitude adjustment is approximated as being a linear function of the control signal V_p only, in a proportion defined by a constant gain control parameter P (i.e. $\Delta V_{ae} = P \cdot V_p$).

Therefore, the behavioral model and the proposed design equations are applicable under the conditions where the representation of the effects of a small gain variation by $\Delta V_{ae} = P \cdot V_p$ yields an acceptable error in the calculation of the IMD levels, and in the context of estimating the IMD performance requirements for the circuit blocks in the error signal path.

The uncertainty related to these approximations is dependent on the particular amplifier circuit characteristics and the specific operating conditions. A case study based on the RF amplifier chain that was designed in the course of this work will be presented in section 3.4.3, and an insight into the uncertainty related to these approximations will be provided through a numerical example, demonstrating that it yields acceptable error margins in the context of this type of analysis.

The a priori assumptions made in the proposed methodology

As can be understood from the observations made in section 2.7.2 in regard to the difficulty of modeling an envelope feedback system for distortion analysis, the availability of design equations for the estimation of IMD levels along the circuit blocks in the feedback error signal path in open loop conditions would be very pertinent for the theoretical or experimental validation of the linearity performances associated with these circuit blocks. This rationale stands even if the validation is in the form of a comparative study with conservative safeguards. And, in the proposed methodology, this translates into the bench-marking of the actual multi-tone, small envelope amplitude IMD levels that can be measured (or simulated) at the output of each one of these circuit blocks separately in *open loop* conditions and with specific multi-tone excitation, against the *best achievable closed loop* IMD levels that may be computed as *bench-marking figures* with the design equations and function of the same multi-tone excitation conditions that are applied to these circuit blocks during the measurements (or simulation), but with some *a priori* idealized assumptions made for the closed loop operation, and which are known and quantifiable.

It is assumed a priori, in the proposed methodology, that the two envelope detectors are identical (i.e. with performances that are perfectly matched), which allows equating their RF to analog conversion gains, i.e.

$$f_{Di} = f_{Do} = f_D \qquad (2.7.6).$$

Also, it is assumed a priori that no distortion is ***added*** by the circuit blocks along the error signal path. This allows regrouping their low frequency gains, i.e. the conversion gain f_D of the envelope detectors, the envelope comparator gain C, and the analog error amplifier gain A_v, as cascaded linear blocks following an ideal comparator, as shown in Fig. 2.7.3, and with a combined low frequency gain:

$$E = f_D \cdot C \cdot A_v \qquad (2.7.7)$$

These a priori assumptions imply also that the calculated bench-marking IMD levels at the output of any of the three circuit blocks in the error signal path may be modeled as IMD product levels that are referred to the output of the ideal comparator, and then scaled up by the low frequency gain factors of the circuit blocks that are in between.

Test criterion sought for the circuit blocks in the error signal path

The worst case linearity requirements for the RF envelope detectors, the error comparator, and the error amplifier should be dictated by the maximum acceptable level for the IMD products that are added in the error signal path as a result of the nonlinear transfer functions of these circuit blocks. Hence, as a test criterion for circuit analysis or experimental investigations with the proposed methodology, the actual multi-tone IMD levels that can be simulated or measured along the error signal path in open loop conditions would ***ideally*** have to be lower, by some design margin, than the bench-marking IMD levels that may be computed with the help of the proposed design equations under the above defined a priori assumptions. Essentially, these bench-marking IMD levels are

representative of the ideal case scenario where there is no inter-modulation distortion generated within the circuit blocks in the error signal path, but only inter-modulation products that stem from the nonlinear amplification of the RF amplifier block alone (i.e. G in Fig. 2.7.3) and transformed by the linear small signal feedback loop characteristics. Compliance with such a worst case test criterion would ensure that the circuit blocks in the error signal path do not degrade the amplifier's overall linearity performance that is theoretically ***achievable*** with the set of small signal feedback loop parameters considered. The design margin depends on the safeguard value sought to guarantee this worst case design criterion. **Alternatively**, departure from the ideal case performance by a *known* error margin still allows setting design goals for performance improvement.

Degree of nonlinearity for the PA block

Given the memoryless, quasi-static, and weakly nonlinear assumptions, the RF power amplifier block (G in Fig. 2.7.3) will be analyzed with power series to relate the input signal $V_a(t)$ to the output signal $V_{out}(t)$, that is:

$$V_{out}(t) = a_1 V_a(t) + a_2 V_a{}^2(t) + a_3 V_a{}^3(t) + a_4 V_a{}^4(t) + a_5 V_a{}^5(t) + \ldots \quad (2.7.8)$$

with a_n being scalar coefficients. While it is common to analyze the IMD characteristics of weakly nonlinear systems with 3rd degree power series (e.g. [5], [8], [58], [60], [61], [63], just to name few), the analysis of the distortion introduced by hardware reconfiguration schemes, which implies gain deviations upon the switching on or off of RF transistor arrays, requires higher degree polynomial representations of the RF amplifier chain for enhanced accuracy. The proposed formulations will be based on a 5th degree power series representation of the gain G of the RF power

amplifier block, and its output multi-tone frequency components limited to $(\omega_c \pm 4\omega_x)$ as depicted in Fig. 2.7.3, for conciseness. However, the proposed methodology may be extended to formulations using higher degree polynomials and a broader multi-tone representation.

2.7.4 Derivation of the design equations

An expression of the form $V_{ae}(t)\cos(\omega_c t)$ is used to represent the RF signal applied to the input of the power amplifier block of Fig. 2.7.3, with $V_{ae}(t)$ describing the multi-tone envelope information. Assuming an ideal band-pass filter at the output of the amplifier to pass only the useful envelope information that is centered around the fundamental carrier frequency ω_c, it may be shown through the substitution of $V_a(t)$ by $V_{ae}(t)\cos(\omega_c t)$ in eq. (2.7.8) and the expansion of this polynomial with a fifth degree representation, that the signal at the output of the amplifier system is in the form:

$$V_{out}(t) = \left(a_1 V_{ae}(t) + \left(\frac{3}{4}\right)a_3 {V_{ae}}^3(t) + \left(\frac{5}{8}\right)a_5 {V_{ae}}^5(t)\right)\cos\omega_c t \,. \qquad (2.7.9)$$

With the scalar parameters J and K representing the amplitudes in the frequency spectrum of the three-tone input signal as shown in Fig. 2.7.3, this input signal may be formulated as

$$V_i(t) = \left(J + 2K\cos(\omega_x t)\right)\cos(\omega_c t) \qquad (2.7.10)$$

and thus the input envelope information may be expressed as

$$V_{ie}(t) = J + 2K\cos(\omega_x t)\,. \qquad (2.7.11)$$

In the same way, the band limited envelope information associated with the frequency spectrum of V_{out} as depicted in Fig. 2.7.3 may be formulated with the scalar amplitude parameters L, M, N, Q, and R, as

$$V_{oe}(t) = L + 2M\cos(\omega_x t) + 2N\cos(2\omega_x t) + 2Q\cos(3\omega_x t) + 2R\cos(4\omega_x t) \quad (2.7.12)$$

The assumptions made for the behavioral model in section 2.7.3 allow expressing the instantaneous envelope signal $V_{ae}(t)$ as well as the envelope error information $V_{ee}(t)$ at the output of the ideal comparator in terms of scalar products of $V_{ie}(t)$ and of $V_{oe}(t)$, i.e. using the scalar low frequency gains H, E, P and F as follows:

$$V_{ae}(t) = FV_{ie}(t) + EPV_{ee}(t) \text{ , and} \quad (2.7.13)$$

$$V_{ee}(t) = V_{ie}(t) - HV_{oe}(t) \quad (2.7.14)$$

with E being the low frequency cascaded gain defined by eq. (2.7.7). Hence eq. (2.7.13) may be expanded to

$$V_{ae}(t) = FV_{ie}(t) + EPV_{ie}(t) - EPHV_{oe}(t). \quad (2.7.15)$$

Substituting eq. (2.7.11), (2.7.12) and (2.7.14) into eq. (2.7.13) yields the following general expression, that defines the envelope information applied to the input of the power amplifier block, assuming a three-tone AM input signal, a fifth order polynomial representation of the amplifier block, and a memoryless behavior:

$$V_{ae}(t) = U + V\cos(\omega_x t) + W\cos(2\omega_x t) + X\cos(3\omega_x t) + Y\cos(4\omega_x t) \quad (2.7.16)$$

with

$$U = FJ + EP(J - HL) \qquad (2.7.17)$$

$$V = 2(FK + EPK - EPHM) \qquad (2.7.18)$$

$$W = -2EPHN \qquad (2.7.19)$$

$$X = -2EPHQ \qquad (2.7.20)$$

$$Y = -2EPHR \qquad (2.7.21)$$

and E being the low frequency gain product $(f_D \cdot C \cdot A_v)$.

The band limited multi-tone envelope information $V_{oe}(t)$ was defined in eq. (2.7.12), and the non-linear processing of $V_{ae}(t)$ by the power amplifier block according to a fifth degree polynomial power series was formulated with eq. (2.7.9). Accordingly, solving for the closed loop, band limited inter-modulation products present at the output of the amplifier system of Fig. 2.7.3 (and thereafter at any node in the system) under the assumption made above requires equating the envelope expressions from the two solutions, i.e.:

$$\begin{aligned} &L + 2M\cos(\omega_x t) + 2N\cos(2\omega_x t) + 2Q\cos(3\omega_x t) \\ &+ 2R\cos(4\omega_x t) = \\ &a_1 V_{ae}(t) + \left(\frac{3}{4}\right) a_3 {V_{ae}}^3(t) + \left(\frac{5}{8}\right) a_5 {V_{ae}}^5(t) \end{aligned} \qquad (2.7.22)$$

with $V_{ae}(t)$ defined in eq. (2.7.16)-(2.7.21).

After expansion of the right hand side terms in eq. (2.7.22), solving for only the constant term and the $\cos(\omega_x)$, $\cos(2\omega_x)$, $\cos(3\omega_x)$, and $\cos(4\omega_x)$ terms allows determining the frequency components L, M, N, Q and R

in the amplifier system's output envelope spectrum, as a function of the scalar parameters J, K of the multi-tone driving signal, and the system parameters a_1, a_3, a_5, F, E, P and H.

Alternatively, the excitation levels J and K and the system parameters that would be required in order to meet some *desired* closed loop inter-modulation performance goals at the output of the amplifier system may be determined. Any such analytical approach would consist of solving a system of 5 nonlinear equations and a certain number of unknowns among the above 14 parameters. The resulting system of equations is given by:

$$\begin{aligned} V_{oe(L)} - L &= 0 \\ V_{oe(M)} - 2M &= 0 \\ V_{oe(N)} - 2N &= 0 \\ V_{oe(Q)} - 2Q &= 0 \\ V_{oe(R)} - 2R &= 0 \end{aligned} \qquad (2.7.23)$$

with the five terms $V_{oe(L)}$, $V_{oe(M)}$, $V_{oe(N)}$, $V_{oe(Q)}$ and $V_{oe(R)}$ defining the envelope amplitudes associated with the center frequency ω_c and with the ω_x, $2\omega_x$, $3\omega_x$ and $4\omega_x$ related mixing products, respectively, which are depicted at the output of the amplifier system in Fig. 2.7.3. The general form of these terms as functions of U, V, W, X, and Y (eq. (2.7.17) to (2.7.21)) are obtained through the substitution of eq. (2.7.16) into eq. (2.7.22), and then the complete expansion of the power series in the resulting equation, followed by the selection and regrouping of terms that are function of the d.c. component and the frequencies $\omega_x, 2\omega_x, 3\omega_x$ and $4\omega_x$:

$V_{oe(L)}$ =

a_1U

$+(3/4)a_3U^3$

$+(3/16)a_3(6VXY+6VWX+3W^2Y+6UW^2+6UX^2+6UY^2+6UV^2+3V^2W)$

$+(5/8)a_5U^5$

$+(25/128)a_5(V^4Y+6UV^4+12V^2WX^2+48U^2VXY+12V^3XY+24VW^2XY$

$+16U^3W^2+16U^3Y^2+16U^3X^2+6UX^4+6UW^4+6UY^4+12VWX^3+12W^2X^2Y$

$+4W^4Y+12VW^3X+24UV^2WY+6WX^2Y^2+12V^3WX+4V^4W+12VX^3Y$

$+12VXY^3+24UV^2W^2+6V^2X^2Y+24U^2V^2W+12V^2WY^2+24VWXY^2$

$+24UWX^2Y+16U^3V^2+6V^2W^3+48UVWXY+24UV^2X^2+24UV^2Y^2+24UVW^2X$

$+24U^2W^2Y+24UX^2Y^2+24UW^2X^2+24UW^2Y^2+8UV^3X+12V^2W^2Y+6W^2Y^3$

$+2W^3X^2+48U^2VWX)$

$V_{oe(M)}$ =

a_1V

$+ (9/16)a_3(V^3+4UVW+4UWX+2VWY+2WXY+4UXY+4VU^2+W^2X$

$+V^2X+2VW^2+2VX^2+2VY^2)$

$+(25/128)a_5(2V^5+24UWX^3+48UWXY^2+48V^2WXY+48UVWX^2+24UW^3X$

$+48VWX^2Y+24U^2V^3+24UX^3Y+16VW^3Y+18W^2XY^2+12WX^3Y+5V^4X$

$+24UVX^2Y+32U^3WX+72UV^2WX+24U^2W^2X+48U^2WXY+16V^3WY$

$+24VW^2Y^2+16U^4V+32U^3VW+48UW^2XY+48U^2VX^2+72UV^2XY+24U^2V^2X$

$+48U^2VWY+16W^3XY+6V^2X^3+32U^3XY+8UV^3Y+48U^2VW^2+6VY^4$

$+32UV^3W+48UVWY^2+48U^2VY^2+12V^2XY^2+12VWY^3+30VW^2X^2$

$+30V^2W^2X+24UXY^3+24UVW^3+30VX^2Y^2+4W^4X+12V^3Y^2+12V^3X^2$

$+14V^3W^2+6VW^4+48UVW^2Y+6W^2X^3+12WXY^3+6VX^4+2X^3Y^2)$

$V_{oe(N)}$ =

a_1W
$+(9/16)a_3(W^3+4U^2W+4UVX+4UWY+2VXY+2VWX+2UV^2+2V^2W+2WX^2+2WY^2+X^2Y+V^2Y)$
$+(25/128)a_5(2W^5+30V^2WX^2+48VW^2XY+24V^2WY^2+24UV^3X+12V^2W^3$
$+16U^3V^2+8UV^4+6WX^4+24U^2W^3+12VX^3Y+24UV^2X^2+24UV^2Y^2$
$+36VWXY^2+48UVXY^2+20V^3WX+16VW^3X+6X^2Y^3+72UVW^2X+24WX^2Y^2$
$+4V^4Y+48U^2VWX+32U^3VX+48U^2WX^2+24UVX^3+36UV^2W^2+48U^2WY^2$
$+24V^2X^2Y+24U^2X^2Y+48UV^2WY+24U^2V^2Y+16U^4W+12UW^2X^2+32U^3WY$
$+6WY^4+7V^4W+24UWY^3+96UVWXY+12UX^2Y^2+12VXY^3+4X^4Y+12W^3X^2$
$+14W^3Y^2+48U^2V^2W+48U^2VXY+48UWX^2Y+12VWX^3+18W^2X^2Y$
$+24V^2W^2Y+16V^3XY+32UW^3Y+6V^2Y^3)$

$V_{oe(Q)}$ =

a_1X
$+(3/16)a_3(V^3+12U^2X+6VWY+12UVW+12UVY+6WXY+6V^2X+3VW^2+6W^2X+6XY^2+3X^3)$
$+(25/128)a_5(V^5+12V^2X^3+24U^2X^3+48UVW^2Y+48U^2V^2X+48UW^2XY$
$+36VWX^2Y+8U^2V^3+2X^5+30V^2XY^2+8UW^3X+48U^2XY^2+18VW^2Y^2$
$+18VW^2X^2+12W^3XY+4VW^4+6V^4X+72UVX^2Y+48V^2WXY+48U^2WXY$
$+16V^3WY+72UVWX^2+32U^3VW+24U^2VW^2+24UVW^3+24UV^2XY$
$+16WX^3Y+30V^2W^2X+48UV^2WX+32U^3VY+6XY^4+16U^4X+48U^2VWY$
$+24UVY^3+12W^2X^3+48UVWY^2+6VX^2Y^2+48U^2W^2X+16VW^3Y+12VWY^3$
$+24UV^3W+24W^2XY^2+12X^3Y^2+24UWXY^2+6W^4X+4V^3Y^2+6V^3X^2$
$+10V^3W^2+24UV^3Y+12WXY^3)$

$V_{oe(R)}$ =

a_1Y
$+(9/16)a_3(Y^3+4U^2Y+4UVX+2VWX+2X^2Y+2V^2Y+V^2W+WX^2+2UW^2$
$+2W^2Y)$
$+(25/128)a_5(2Y^5+48U^2V^2Y+2UV^4+16U^3W^2+6X^4Y+24U^2WX^2+36VWXY^2$
$+24UWX^2Y+36VW^2XY+96UVWXY+4WX^4+24UV^3X+16VW^3X$
$+24U^2V^2W+16V^3WX+24UW^2X^2+12V^2Y^3+12W^2Y^3+48U^2VWX+18WX^2Y^2$
$+32U^3VX+24UVX^3+8V^3XY+24UV^2W^2+24W^2X^2Y+18V^2WY^2+48UV^2WY$
$+48U^2W^2Y+4VX^3Y+16U^4Y+30V^2X^2Y+24V^2W^2Y+48UVW^2X+7W^4Y$
$+8UW^4+24V^2WX^2+72UVXY^2+48U^2X^2Y+36UW^2Y^2+24U^2Y^3+8V^2W^3$
$+12UV^2X^2+12X^2Y^3+4V^4W+6V^4Y+6W^3X^2+12VWX^3)$

The correctness of these terms as solutions to the expansion of the right hand side polynomial of eq. (2.7.22) may be verified by subtracting the quantity

$$V_{oe(L)} + V_{oe(M)}\cos(\omega_x t) + V_{oe(N)}\cos(2\omega_x t) + V_{oe(Q)}\cos(3\omega_x t) + V_{oe(R)}\cos(4\omega_x t)$$

from this same polynomial (with $V_{ae}(t)$ expanded through eq. (2.7.16)) and observing that the result does not contain any term of frequency inferior to $5\omega_x$. Once these terms are compiled in any analysis, simulation or test software tool, the task of solving for the bench-marking IMD product levels (as per the test criterion defined in section 2.7.3) at any node of the envelope feedback system of Fig. 2.7.3 is simply reduced to the following steps.

Summary of design equations for IMD calculation function of the multi-tone amplitudes and system parameters, and under the a priori assumptions

With the system of equations defined by eq. (2.7.23) solved, and thus with J, K, L, M, N, Q and R known as input variables to this system of equations *or* any of them obtained as solutions, then the general expression for the bench-marking IMD multi-tone envelope information at the output of the power amplifier (under the idealized a priori assumptions described in section 2.7.3), may be readily obtained using eq. (2.7.12), which is repeated here for convenience:

$$V_{oe}(t) = L + 2M\cos(\omega_x t) + 2N\cos(2\omega_x t) + 2Q\cos(3\omega_x t) + 2R\cos(4\omega_x t)$$

From eq. (2.7.11), (2.7.12), (2.7.14) the general expression representing the bench-marking IMD multi-tone envelope information at the output of the ideal comparator of Fig. 2.7.3 may be expressed as:

$$V_{ee}(t) = (J - HL) + 2(K - HM)\cos(\omega_x t) - 2HN\cos(2\omega_x t) - 2HQ\cos(3\omega_x t) - 2HR\cos(4\omega_x t) \quad . \quad (2.7.24)$$

And, from eq. (2.7.13), the general expression representing the envelope signal at the input of the RF power amplifier block of Fig. 2.7.3 (under the bench-marking a priori conditions) may be expressed as:

$$V_{ae}(t) = J(F + EP) - EPHL + \left(2K(F + EP) - 2EPHM\right)\cos(\omega_x t) - 2EPHN\cos(2\omega_x t) - 2EPHQ\cos(3\omega_x t) - 2EPHR\cos(4\omega_x t) \quad . \quad (2.7.25)$$

CHAPTER 3

Design of a Gated Envelope Feedback RFIC PA with automatic hardware reconfiguration in GaAs HBT technology

This chapter describes in detail the circuit techniques that have enabled a successful and full on-chip embodiment of a GaAs HBT RFIC power amplifier with automatic hardware reconfiguration capabilities for current reduction purposes. The design is based on an amplifier architecture that uses the gated envelope feedback technique with the goal of demonstrating the viability of the proposed technique, and using circuit techniques that offer optimum trade-offs between electrical performances and on-chip integration, with a clear path toward single-chip integration in GaAs HBT technology. The design equations and the methodology that were proposed in sections 2.7.3 and 2.7.4 will be used for IMD analysis.

The targeted functional and performance specifications for this design are summarized in Table 3.0.1. These specifications were set to demonstrate the advantages that stem from the gated envelope feedback technique in the context of hardware reconfiguration for current reduction as postulated in section 2.2, i.e. mainly in regard to increased autonomy in the PA module to allow multiple hardware states with the minimum of interfacing with the external components, automatic compensation against gain perturbations and gain regulation across a significantly large power range, compliance with some of the key specifications for CDMA applications, and the suitability for full on-chip integration in GaAs HBT technology with minimum chip area.

Table 3.0.1: Targeted functional and performance specifications.

Functional specifications	
Number of hardware states	4
Number of control lines	1
Features for hardware reconfiguration within the envelope feedback gating power range	Fully self-reconfigurable
Calibration requirements	Minimum of points over power
Performance specifications	
Output power range (P_{out} range) for the envelope feedback gating function	0 dBm to 15 dBm
Power gain within the feedback gating range	15 dB (min.)
Return loss	-15 dB or less
Frequency of operation	PCS band (1.85 GHz - 1.91 GHz)
Total current consumption at P_{out} = 15 dBm	150 mA max. (3.4V: PAE = 6%)
Current reduction in the full hardware reconfiguration state (P_{out} = 12 dBm and lower)	50% or higher
Power added efficiency at P_{out} = 12 dBm	4% or higher
Gain deviation upon hardware reconfiguration	0.15 dB or less
Gain variation across the small signal and feedback gating power range	1 dB or less
Output envelope slew rate with a CW step input	5 dB/10ms min.
ACPR below P_{out} = 12 dBm with CDMA2000 input	-42 dBc max.
Error vector magnitude below P_{out} = 12 dBm	less than 5%
Rho factor below P_{out} = 12 dBm	higher than 0.944

Section 3.1

Brief description of Skyworks Solutions' 4th generation GaAs HBT semiconductor technology

3.1.1 Skyworks Solutions' 4th generation GaAs HBT process

The semiconductor technology that was used for the RFIC power amplifier design in this work is the HBT4 fourth generation GaAs HBT process developed, owned and commercialized by Skyworks Solutions, Inc., U.S.A., and intended for high volume production of RFIC power amplifiers. This process offers high frequency NPN devices as well as RF passive components, including varactor diodes, base-collector diodes, metal-insulator-metal (MIM) capacitors, thin film resistors, base layer resistors, and inductors. It also offers the possibility of using through-wafer via (TWV) interconnects, and allows the routing between devices using two metal layers (M1 & M2), with M2 specifically processed for the routing of the high current signals and grounding in power amplifier designs.

Multiple epitaxial materials are supported in Skyworks' GaAs HBT process family for different applications, and the Skyworks' P401 material HBT4 process was used in this work, since this specific process was engineered for power amplifier applications that need to comply with linearity requirements, such as in CDMA and W-CDMA transmission, while providing highly competitive performances for other important power amplifier parameters such as power efficiency, RF power gain and robustness.

The electrical specifications of some of the standard library components from the P401 material HBT4 process are summarized in Appendix I (with permission from Skyworks Solutions, Inc.).

Section 3.2
RF amplifier chain IC

In this section, the design of the variable gain RF amplifier chain of Fig. 2.6.2 and simulation results are presented.

3.2.1 RF amplifier chain architecture

Fig. 3.2.1 shows a detailed block diagram of the 3-stage RF amplifier chain that was implemented on a GaAs HBT IC, as well as the supply and main control signals.

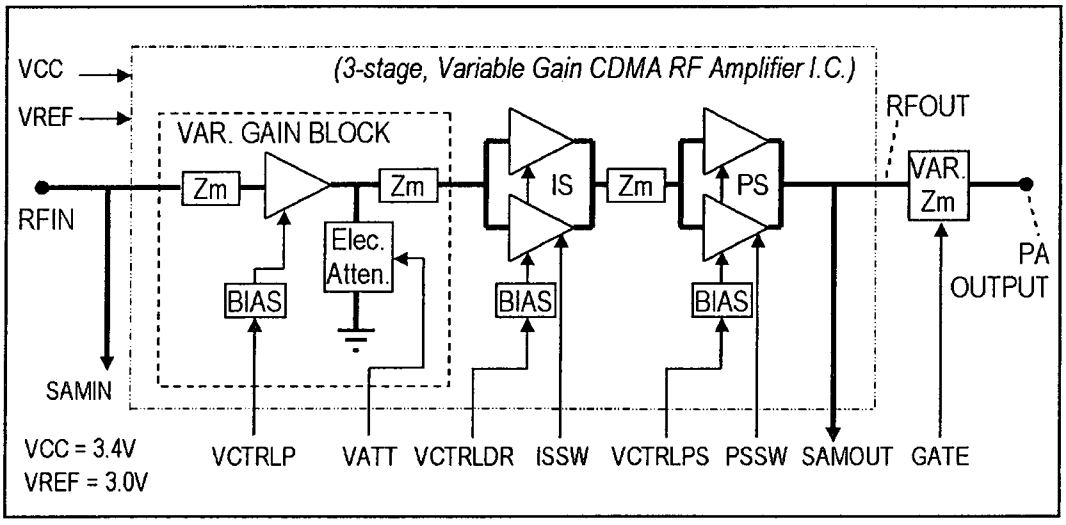

Figure 3.2.1 Block diagram of the RF amplifier chain.

The thick lines represent the RF signal paths. All elements shown have been integrated on a single GaAs HBT IC, except the output variable impedance matching network (VAR. Zm), which normally is implemented off-chip in a power amplifier module using discrete components, in order to minimize the losses. For simulation purposes in this work, a fixed output multi-harmonic impedance matching circuit was used and optimized for large signal conditions, as will be described in a later section. For the

experimental part of this work, the variable impedance matching network was embedded within the test setup as a computer controlled passive load-pull synthesizer.

3.2.2 Variable gain stage

Fig. 3.2.2 shows the schematic of the variable gain block.

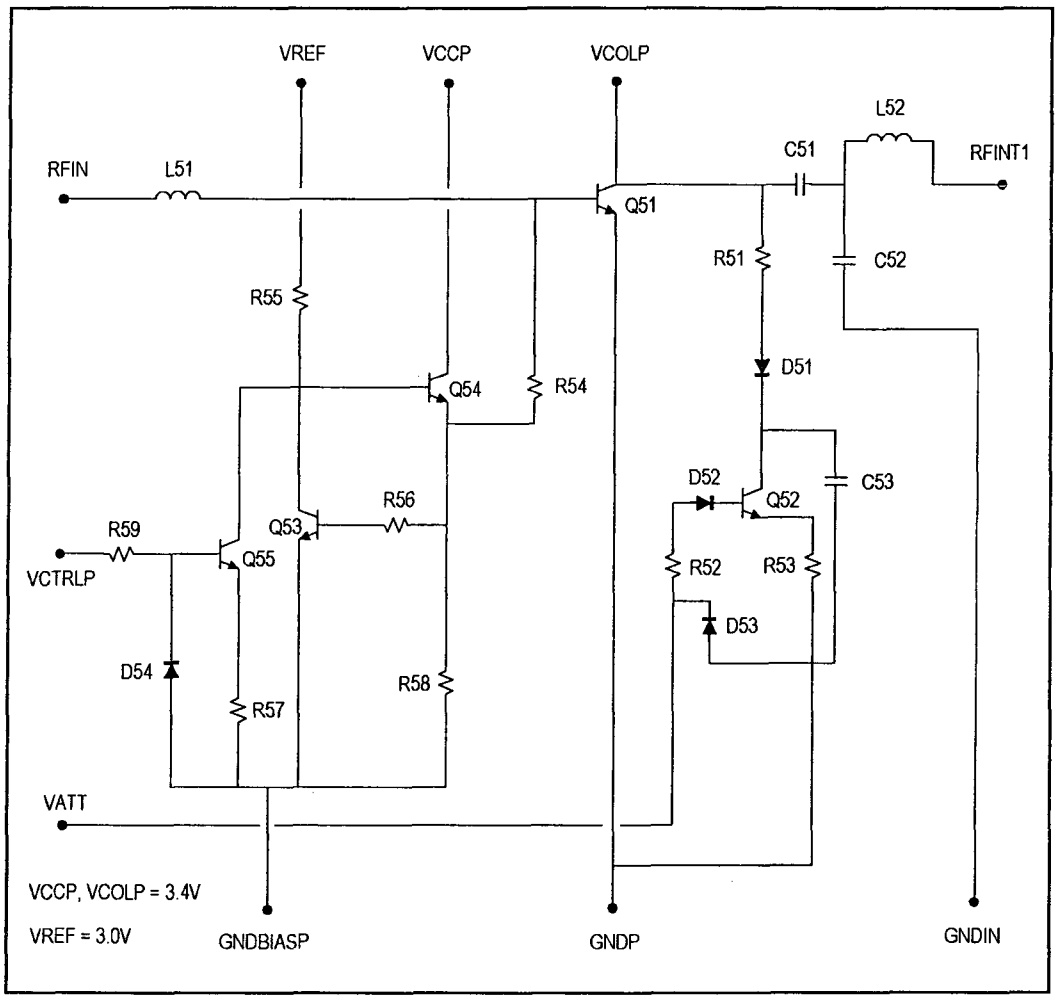

Figure 3.2.2: Schematic of the variable gain block.

The role of this first stage as a pre-amplifier (VAR. GAIN BLOCK in Fig. 3.2.1) is to provide a variable gain function in the forward path of the

envelope feedback system. This topology has been chosen as a good compromise between simplicity for on-chip integration in pure GaAs HBT technology, and a maximized gain dynamic range performance as a function of the amplified error signal that is applied to the VCTRLP, VATT, VCTRLDR, and VCTRLPS control lines in Fig. 3.2.1 (see also Fig. 2.6.2).

Circuit description

The size of the RF pre-amplifier transistor (Q51) has been optimized by simulation following the design guideline (i) in section 2.5.1, since this amplifier stage acts also as a pre-distorter element in the RF amplifier chain. This pre-amplifier transistor is biased with the help of an electronically adjustable current mirror biasing circuit, which is built up with Q53, Q54, R55, R56, R58 and R54. The collector current of the reference transistor Q53 is set by the difference between the reference voltage VREF and the sum of the two V_{BE} voltages of Q53 and Q54, and also by the value of R55. The collector quiescent current of Q51 is higher than that of Q53 in a proportion that is set by the resistor values and transistor sizes in the current mirror circuit.

The RF pre-amplifier is matched at its input for adequate return loss with a series inductor (L51). An on-chip impedance matching circuit (C51, C52 and L52) at its output ensures an optimum power transfer at 1.88GHz between this stage and the following stage (i.e. stage IS in Fig. 3.2.1). The gain of the RF pre-amplifier may be varied primarily through the control of an adjustable shunt load at its output, and used a variable electronic attenuator. This attenuator is built up with R51, Q52, R53, C53, and the base-collector diode D51, and is controlled by the VATT signal. The role of R52 and D52 is to set the tuning voltage threshold where VATT is allowed to bias Q52. When VATT is at a low voltage, Q52 and the diode D51 are not biased. In this condition, the impedance seen from the collector of Q51

and looking into R51 is high (~ 900 Ohms), which allows for maximum power transfer to the output (RFINT1).

When VATT is increased and reaches the tuning threshold which is set primarily by the sum of the turn on voltage of the Schottky diode D52 and the VBE_{ON} of Q52, the collector current of Q52 increases proportionally with VATT, and the resistance offered by D51 is significantly reduced as VATT increases. Thus, the impedance seen from the collector of Q51 and looking into the small resistor R51 may be reduced by increasing VATT, which has the effect of mismatching the impedance at the collector of Q51, hence reducing the gain of the amplifier chain. R51 is used to control the level of impedance mismatch, and R53 is required to adjust the current intensity in Q52 and provide temperature stability within the electronic attenuator circuitry. In order to provide a low impedance RF path to ground, C53 is used to bypass Q52 and R53.

The gain control dynamic range of the RF pre-amplifier is further improved by simultaneously adjusting the bias current of Q51 through the current mirror, as a function of the level of VCTRLP. This is accomplished by deviating part of the reference current that circulates through R55 into the current control branch that includes Q55. R59 and R57 are used to adjust the range of this current control, while D54 limits any reverse V_{BE} biasing of Q55.

Simulated dynamic range performance

The simulated gain control achievable with the 3-stage RF amplifier chain, when using the variable gain block of Fig. 3.2.2, is shown in Fig. 3.2.3. The main contribution for the dynamic range comes from the variable gain block. For this simulation, sections of the RF transistor arrays in the intermediate stage and in the power stage (IS and PS in Fig. 3.2.1) have been turned OFF to emulate the conditions set through automatic hardware reconfiguration at input power levels lower than P_{th3} in Fig. 2.6.1. This is the worst case scenario in regard to ensuring that the dynamic

range in the gain control is high enough to maintain good gain regulation through feedback.

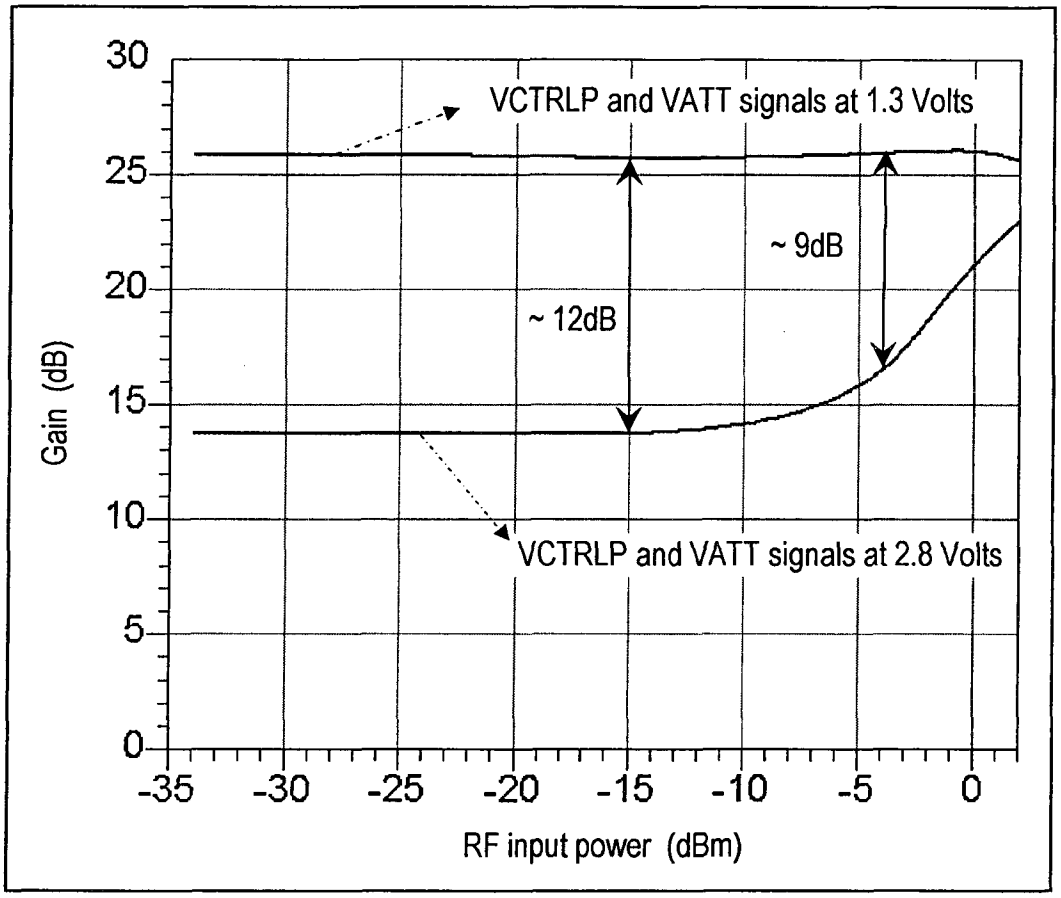

Figure 3.2.3: Simulated gain control dynamic range of the 3-stage amplifier chain (Fig. 3.2.1) with the use of the variable gain stage shown in Fig. 3.2.2.

The gain of the RF amplifier chain as a function of the input power is shown for the case where the VCTRLP signal (which is connected to the VCTRLDR and the VCTRLPS signals, as represented by Fig. 2.6.2 and Fig. 3.2.1) and the VATT signal are both set at 1.3 Volts for maximum gain, and the case where they are both set at 2.8 Volts for minimum gain.

It can be seen that at the low and mid-range input power levels (below -10dBm) a dynamic range of ~12dB or better may easily be achieved. As the input power increases, the asymmetrical pulsed RF current that flows into Q52 and R53 causes the average collector voltage of Q52 to rise, which in turn tends to reduce the biasing of D51. Hence, the effectiveness of the electronic attenuator is reduced as the power increases, and consequently the gain control dynamic range is reduced as well. Nevertheless, sufficient dynamic range (e.g. 9dB at -4dBm and 3dB at 2dBm) may be achieved with this circuit topology in order to ensure proper envelope feedback operation.

3.2.3 Intermediate stage

The schematic of the intermediate stage is shown in Fig. 3.2.4.

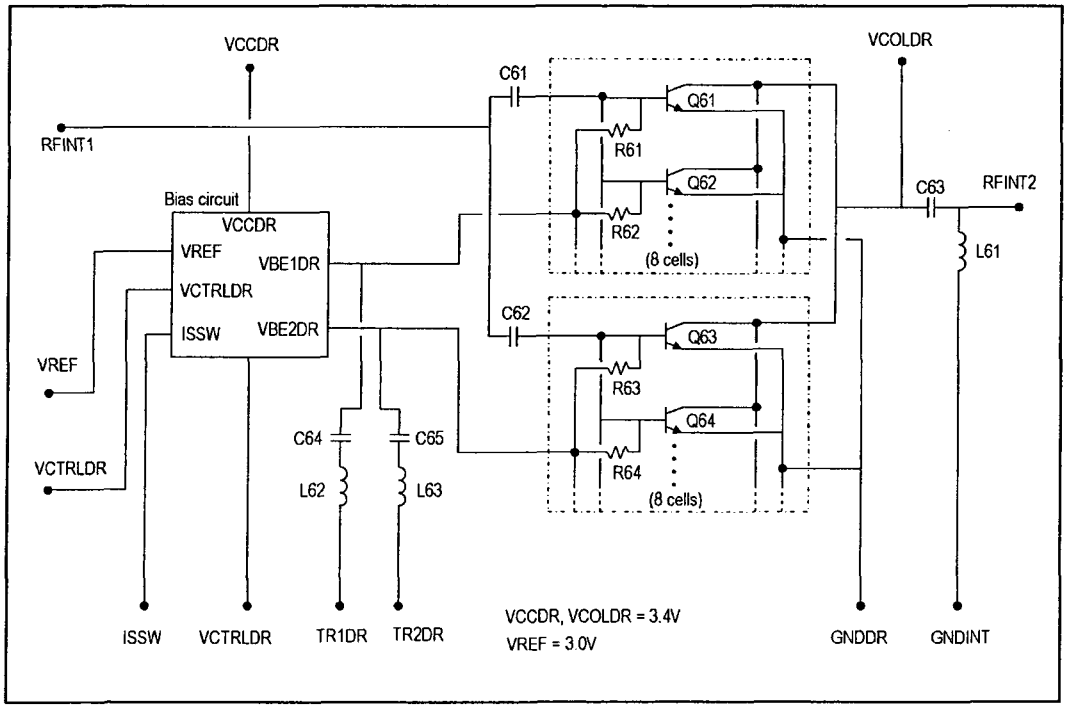

Figure 3.2.4: Schematic of the intermediate stage.

RF section

The intermediate RF amplifier section is split into two arrays, one array containing 8 paralleled transistors including Q61 and Q62, and a second array of 8 transistors including Q63 and Q64. The second array may be shut off upon hardware reconfiguration, and the ratio between the sizes of these two arrays has been determined by simulation, following the design guideline (i) in section 2.5.1. The inputs of these two arrays are isolated in d.c. with the help of C61 and C62. Their outputs are combined and matched to the input of the power stage (PS in Fig. 3.2.1) for optimum power transfer through the matching elements C63 and L61.

These two RF transistor arrays are biased separately and function of the voltages VBE1DR and VBE2DR delivered at the output of the bias circuit. These bias voltages are filtered with the help of notch filters (C64,L62 and C65,L63) that are centered at 1.88GHz.

Bias circuit

The bias circuit for the intermediate stage is shown in Fig. 3.2.5. It uses two current mirror circuits to control the two RF transistor arrays of Fig. 3.2.4 separately, by setting the proper voltages VBE1DR and VBE2DR. A first current mirror is built with Q71, Q72, Q73, Q74, R71, R72, R73, R74 and R75.

The total reference current circulating through the collectors of reference transistors Q71 and Q72 is set by the difference between the reference voltage VREF and the sum of the two V_{BE} voltages of Q71 and Q73, and also by the value of R71. The total collector current circulating in the first RF transistor array that includes Q61 and Q62 in Fig. 3.2.4 is higher than the reference current in a proportion that is set by the resistor values and transistor sizes in the current mirror.

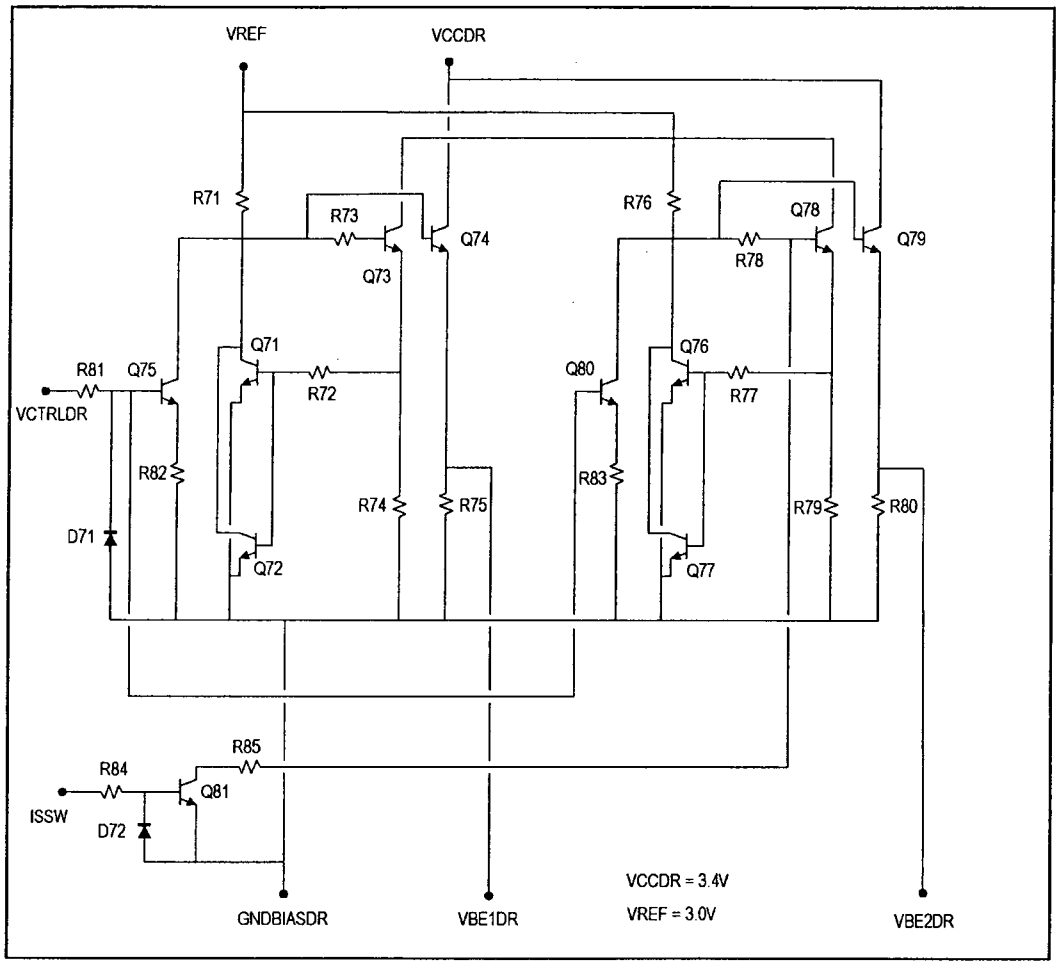

Figure 3.2.5: Schematic of the bias circuit for the intermediate stage.

The second current mirror is built with Q76, Q77, Q78, Q79, R76, R77, R78, R79 and R80, and operates in the same fashion as the first current mirror circuit. However, its output voltage VBE2DR may be lowered to near zero Volts when Q81 is forced into saturation as a result of applying a logic high condition to the ISSW signal. The saturation of Q81 has the effect of turning OFF transistor Q79 by lowering its base voltage, and this mechanism is used to shut OFF completely the RF transistor array that includes Q63 and Q64 in Fig. 3.2.4, for current reduction purposes. When the ISSW signal is at logic low to enable both RF transistor arrays in Fig. 3.2.4, their bias currents may be controlled symmetrically by

simultaneously varying their corresponding reference currents in the current mirror circuits. This is accomplished by deviating part of the current circulating through R71 and R76 into Q75 and Q80, respectively, through the increase of the VCTRLDR signal. An increase in the bias current of each RF transistor results in an increase in the gain, since the trans-conductance of the transistor increases with the bias current [8], [63]. Hence, this bias current modulation scheme is used to improve the dynamic range of the RF amplifier chain. Diodes D71 and D72 are used to limit any negative voltage applied to the bases of Q75, Q80, and Q81.

3.2.4 Power stage

The schematic of the power stage is shown in Fig. 3.2.6.

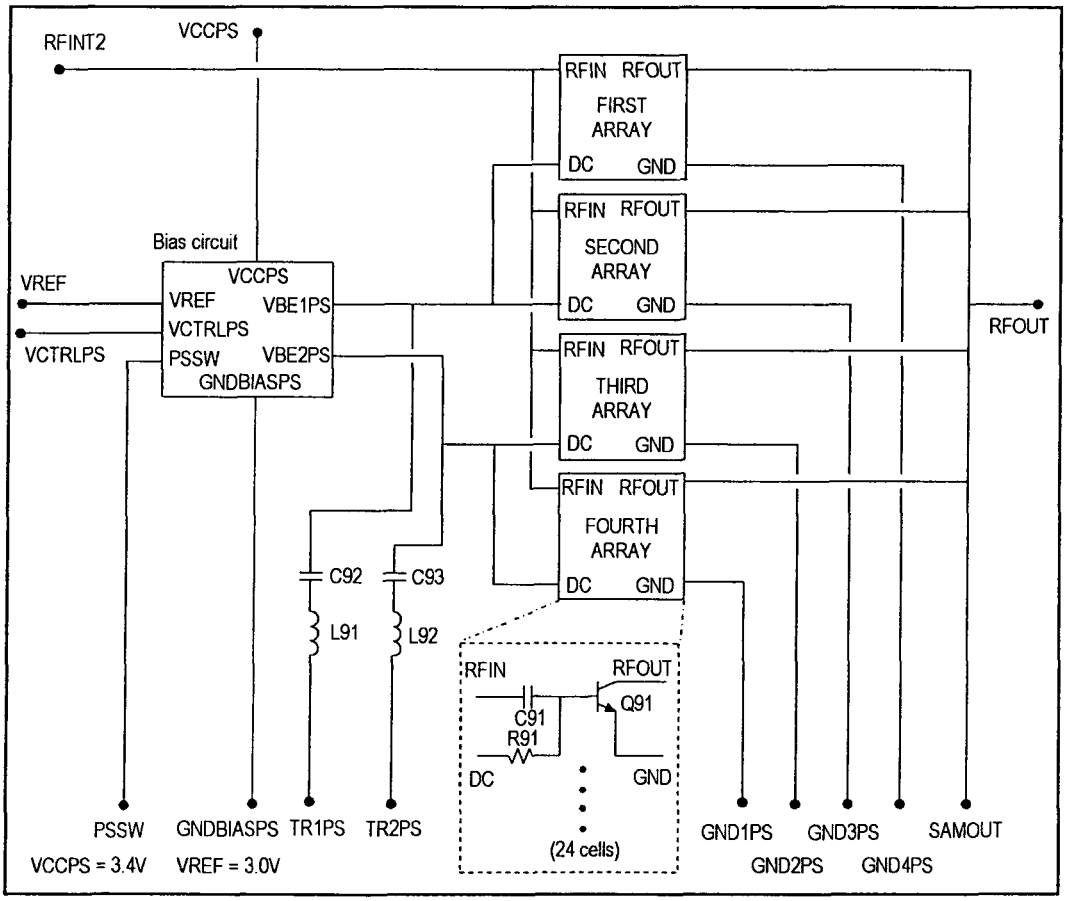

Figure 3.2.6: Schematic of the power stage.

RF section

Similar to the structure of the intermediate stage (Fig. 3.2.4) the power stage is built up with arrays of paralleled cells. Four arrays are used, each one containing 24 cells in parallel. An example of a single cell structure is shown in Fig. 3.2.6 inside the dotted lines, with a bias resistor (R91), a capacitor (C91) used as a d.c. block, and an RF transistor (Q91).

In each one of the four arrays, the 24 cells are connected in parallel, i.e. with the nodes bearing identical names tied together. The four arrays are split into two groups, with the first and second arrays connected in parallel, and the third and fourth arrays connected in parallel as well. The ratio between the sizes of these two groups has been determined by simulation following the design guideline (ii) in section 2.5.1. While the RF signal RFINT2 is applied simultaneously to all the RF inputs (RFIN pin in each array), these two groups of arrays are biased separately with the two d.c. signals (VBE1PS and VBE2PS) delivered by the bias circuit block. These bias voltages are filtered with the help of notch filters (C92, L91 and C93, L92) that are centered at 1.88GHz. With this bias distribution, the third and fourth arrays may be completely shut off when VBE2DR is lowered to near zero Volts, for current reduction purposes.

The RF outputs of the four arrays are tied together at the RFOUT node for the purpose of combining their RF power. As in the case of the intermediate stage, the bias current of the RF transistors in the four arrays of the power stage are controlled through the bias circuit block to improve the dynamic range of the RF amplifier chain.

Bias circuit

As shown in Fig. 3.2.7, the current mirror based bias circuit structure used for the power stage is identical to that of the intermediate stage, and their principle of operation is exactly the same. The VCTRLPS signal is used to vary the quiescent current of the power stage by adjusting the reference currents symmetrically in both current mirror circuit blocks, and a logic

high condition on the PSSW signal is used to switch off completely the third and fourth RF transistor arrays in the power stage for current reduction purposes, by lowering VBE2PS to near zero Volts.

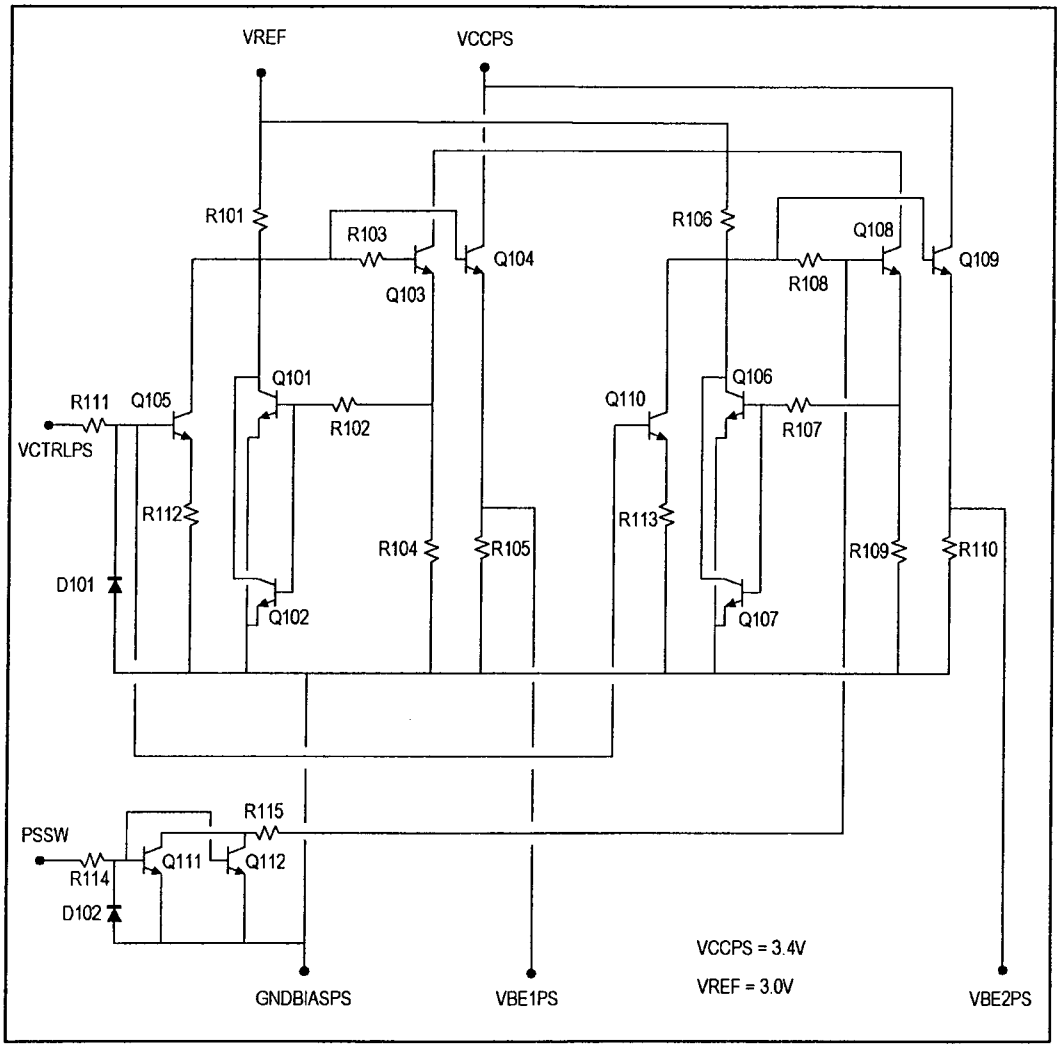

Figure 3.2.7: Schematic of the bias circuit for the power stage.

3.2.5 Output multi-harmonic impedance matching network

Fig. 3.2.8 shows the schematic of the output multi-harmonic impedance matching network that was used for the simulation of the RF amplifier. In

addition to inductors and capacitors, micro-strip transmission lines are used as matching elements.

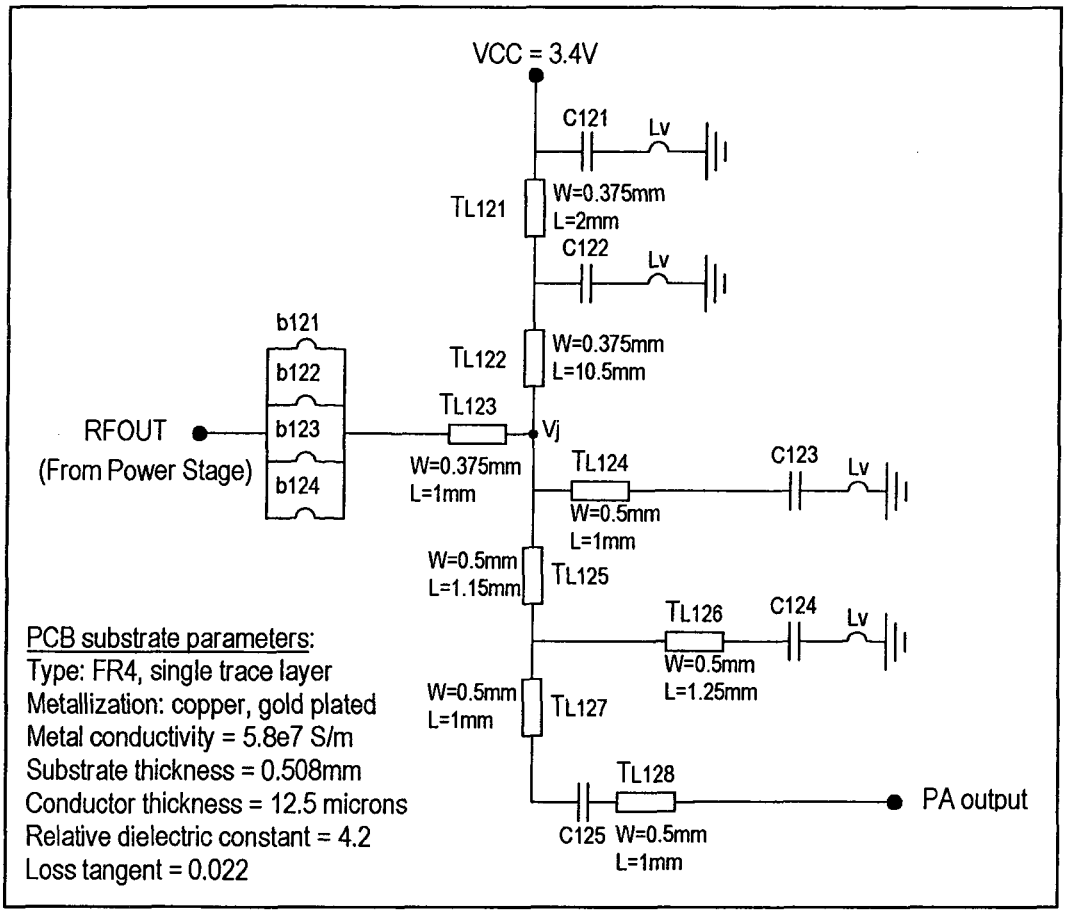

Figure 3.2.8: Schematic of the output multi-harmonic impedance matching network used for simulation, together with the PCB substrate parameters.

Each line contributes to the flexibility of having phase adjustments in the reflection coefficient while maintaining its modulus constant [64] along the line. The matching network is designed for implementation with surface-mount inductors and capacitors on an FR4 type printed circuit board (PCB), with the substrate parameters given in Fig. 3.2.8. The primary role of the matching network is to transform the 50 Ohm output termination that

the amplifier is designed to drive into a multi-harmonic impedance that is presented as a load to the output of the power stage block (Fig. 3.2.6) at the RFOUT node.

The use of a multi-harmonic loading at the fundamental frequency 1.88GHz and the harmonic at 3.76GHz is to ensure the best trade-off between efficiency and linearity when the amplifier is driven into large signal operation [8]. This impedance transformation is accomplished with the transmission line segments TL123 through TL128, capacitors C123, C124 and C125, as well as the bond wires b121, b122, b123 and b124. The equivalent inductive reactance (Lv) of the PCB's plated through holes (PTH) are also included in the design. The transmission line segments TL121 and TL122, as well as capacitors C121 and C122 are used as a bias feed to pass the d.c. current that is sunk by the RF transistor arrays of the power amplifier stage through the RFOUT node, while isolating the d.c. supply line (VCC) from the RF signal by presenting a high impedance at the junction node V_J, looking into TL122.

The secondary role of this matching network is to provide the necessary impedances at the output of the power stage (i.e. at the RFOUT node) in order to guarantee RF stability in the operation of the amplifier chain. Based on the stability circles design techniques [64], the design for stability is achieved through computerized optimizations that solve simultaneously for stable output load conditions over a broad frequency range, while providing optimum gain at the transmission frequency of 1.88GHz.

3.2.6 IC embodiment of the RF amplifier chain

The schematic in Fig. 3.2.9 illustrates the IC embodiment of the above described RF amplifier chain in a single GaAs HBT IC that is directly bonded on the same single layer PCB used for the output matching network, and thus with the same substrate parameters as in Fig. 3.2.8.

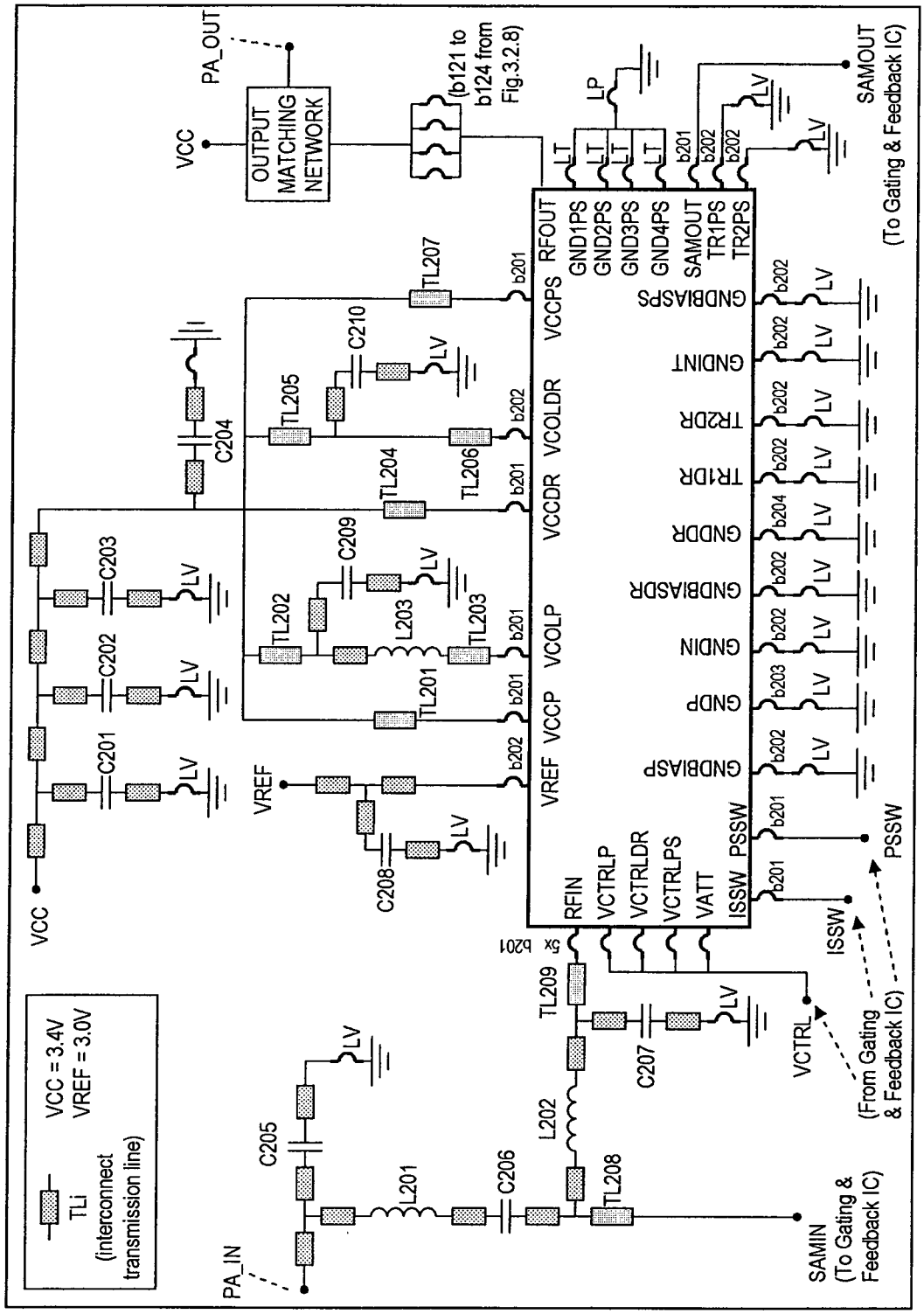

Figure 3.2.9 IC embodiment of the RF amplifier chain. The GaAs HBT IC is directly bonded on the same PCB represented by Fig. 3.2.8.

Micro-strip transmission lines (TL201 to TL207) and decoupling capacitors (C201 to C204, C209, C210) are used in the power supply network for stability reasons, as per the simulation results. An off-chip input matching network built with L,C components (L201, L202, C205, C206, C207) provides facilities for the adjustment of the input impedance of the PA system (PA_IN node) in either case where a load is present at node SAMIN or not. The effects of interconnect tracks on the PCB are modeled with transmission line segments (TLi), and the inductive reactances of bond wires (b_n), of the through wafer vias of the IC (LT), and of the PCB vias (Lv and Lp) are also taken into consideration for adequate treatment of the signal integrity.

Using the schematic of Fig. 3.2.9, the complete amplifier chain has been optimized through numerous iterations between small signal simulation and large signal simulation, in order to find the best trade-off between the small-signal gain, stability, large signal gain and minimum gain compression at large signal for linearity, and with the minimum of current consumption for best power efficiency.

3.2.7 Amplifier chain simulated performances

Small signal performance

The simulated performances obtained after optimization for gain and stability in a small signal regime with all the RF transistor arrays fully functional are shown in Fig. 3.2.10. These results indicate that a small signal gain of ~27dB and an input return loss of -16dB are achievable when the VCTRLP, VATT, VCTRLDR and VCTRLPS gain control signals (shown in Fig. 3.2.1) are set for maximum gain (i.e. at 1.3V), together with good stability performances over a broad frequency range. As per their definitions in the ADS(TM) (Advanced Design System) simulation tool, for μ_{in} and μ_{out} values greater than zero, these two metrics represent the

difference between the reflection coefficient $|\Gamma| = 0$ on the center of a Smith chart and the smallest reflection coefficient magnitude associated with the input stability or output stability circles. Accordingly, μ is a measure of the smallest distance between a point on a stability circle and the center of the Smith chart. Hence μ_{in} greater than 1 indicates that the input stability circle is outside the radius $|\Gamma| = 1$ on a Smith chart, and μ_{out} greater than 1 indicates that the output stability circle is outside the radius $|\Gamma| = 1$, which are sufficient conditions to demonstrate unconditional stability in regard to passive source and load impedances [64].

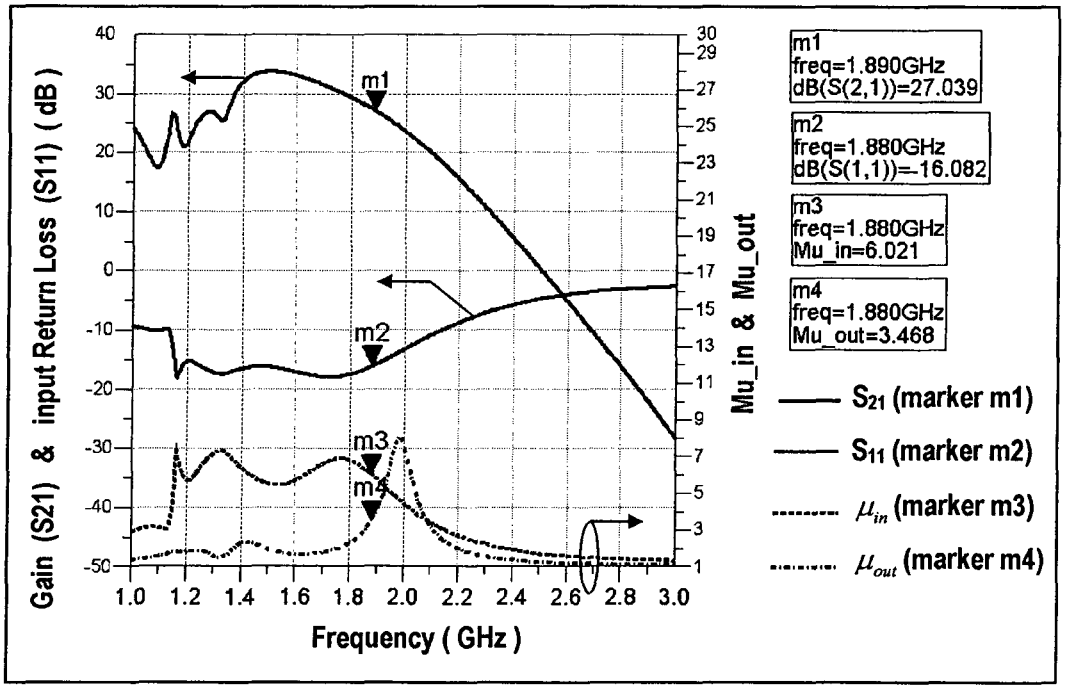

Figure 3.2.10: Simulated small signal gain, return loss, and stability conditions (μ is labelled as "Mu" on the right axis).

The simulated stability circles that are closer to the $|\Gamma| = 1$ condition are also plotted on the Smith chart of Fig. 3.2.11.

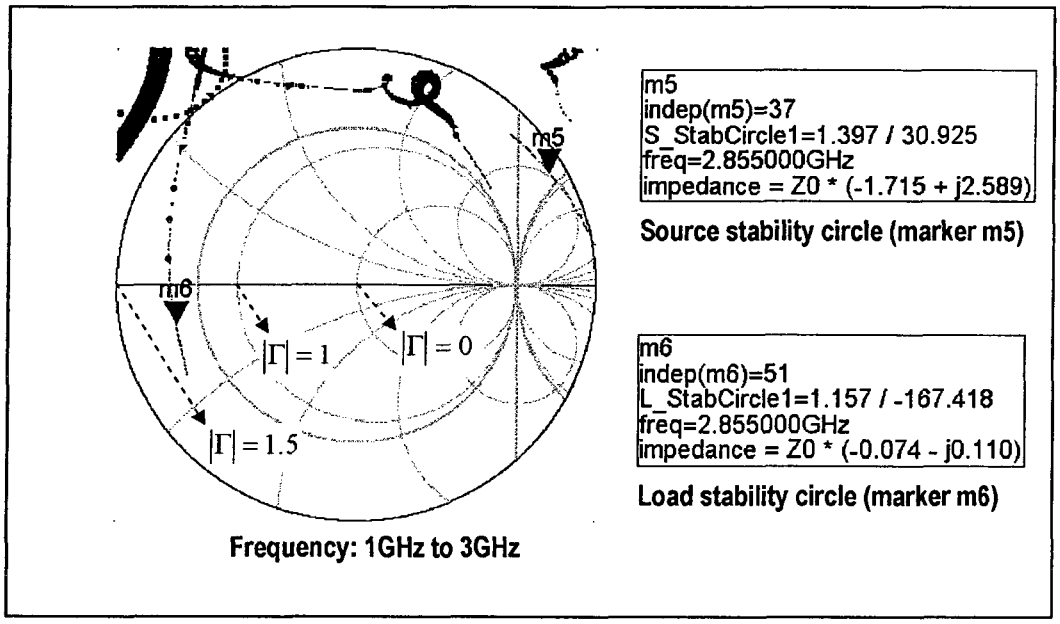

Figure 3.2.11: Smith chart showing the simulated source and load stability circles.

Large signal performance

The simulated large signal gain and total supply current as a function of the output power level are shown in Fig. 3.2.12, for a first condition (i.e. ISSW & PSSW at logic low) where all RF transistor arrays are fully functional, and a second condition (i.e. ISSW & PSSW at logic high) where hardware reconfiguration is performed to shut off half of the intermediate stage RF transistor periphery and half of the power stage RF transistor periphery, for current reduction purposes. In both cases, the maximum gain is enabled (i.e. with VCTRLP, VATT, VCTRLDR, and VCTRLPS in Fig. 3.2.1 set at 1.3V). It can be seen that a significant current reduction may be achieved at low and intermediate power levels upon hardware reconfiguration. At ~0dBm output power, this corresponds to a reduction from ~145mA to 86mA, with an associated gain reduction of ~2dB.

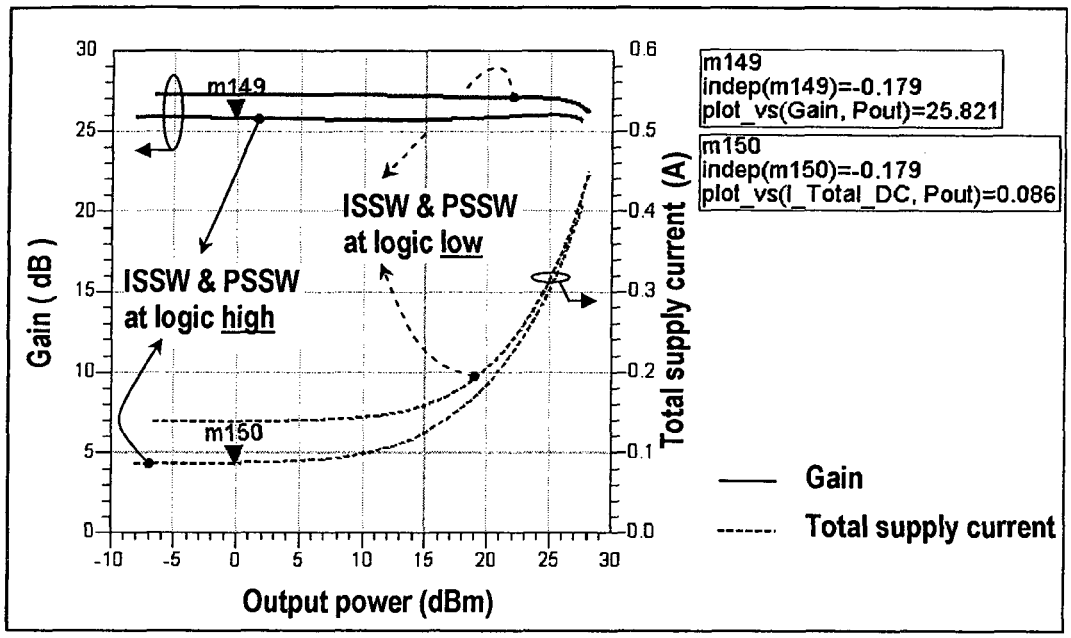

Figure 3.2.12: Simulated large signal gain and total supply current as functions of the output power. With ISSW and PSSW at logic high, half of the transistor arrays in the intermediate and power stages are shut off.

ACPR performance with CDMA2000 modulation

Fig. 3.2.13 shows the simulated ACPR performance of the 3-stage RF amplifier chain with a CDMA2000 excitation applied to its input and adjusted for a total output power of ~20dBm, and with half of the intermediate stage and half of the power stage shut off for current reduction purposes, i.e. with the ISSW and PSSW signals at logic high. Also, the maximum gain was enabled by setting VCTRLP, VATT, VCTRLDR, and VCTRLPS (Fig. 3.2.1) at 1.3V.

The worst case -55.1dBc output ACPR performance shown for the lower adjacent channel (ACPR_Vout(1) in Fig. 3.2.13) is well within the -42dBc standard specification for CDMA2000 transmission (see section 2.4.1). This demonstrates an adequate choice of the RF device sizes (as per the design guidelines of section 2.5.1) in both the intermediate and power stages for the condition where the hardware has been reconfigured for

current reduction, thus allowing amplification of the CDMA2000 signal without excessive AM-AM or AM-PM distortion, which ensures compliance with the linearity requirements with ample margin.

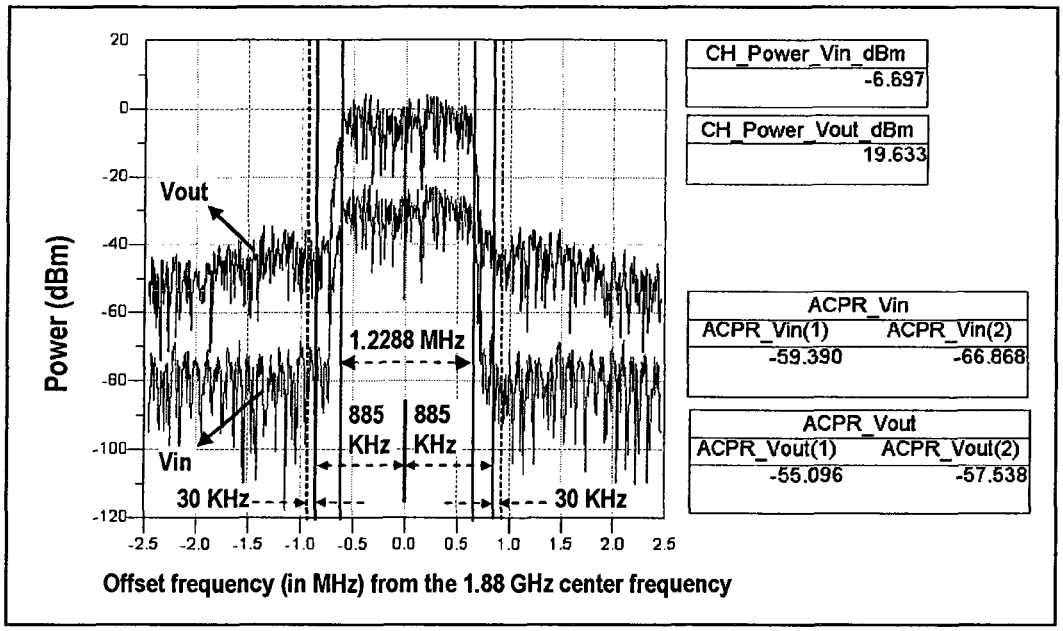

Figure 3.2.13: Simulated Adjacent Channel Power Rejection (ACPR) performance at the input (V_{in}) and at the output (V_{out}) of the RF amplifier chain with a CDMA2000 input excitation, and with half of the intermediate stage and half of the power stage switched off (i.e. ISSW & PSSW at logic high) for current reduction purposes.

Section 3.3
The gating and feedback controller IC

In this section, the design of the gating, envelope feedback and hardware reconfiguration circuitry, as well as simulation results are presented.

3.3.1 Block diagram of the gating and feedback circuitry, and the automatic reconfiguration circuitry

Figure 3.3.1 is a detailed block diagram of the on-chip gating, envelope feedback and hardware reconfiguration control circuitry, showing also the RF and envelope signal paths in thick lines, the different supply and control signals, as well as the ground separation (7 ground signals: GND_) between the circuit sections, which is important for crosstalk reduction and signal integrity considerations.

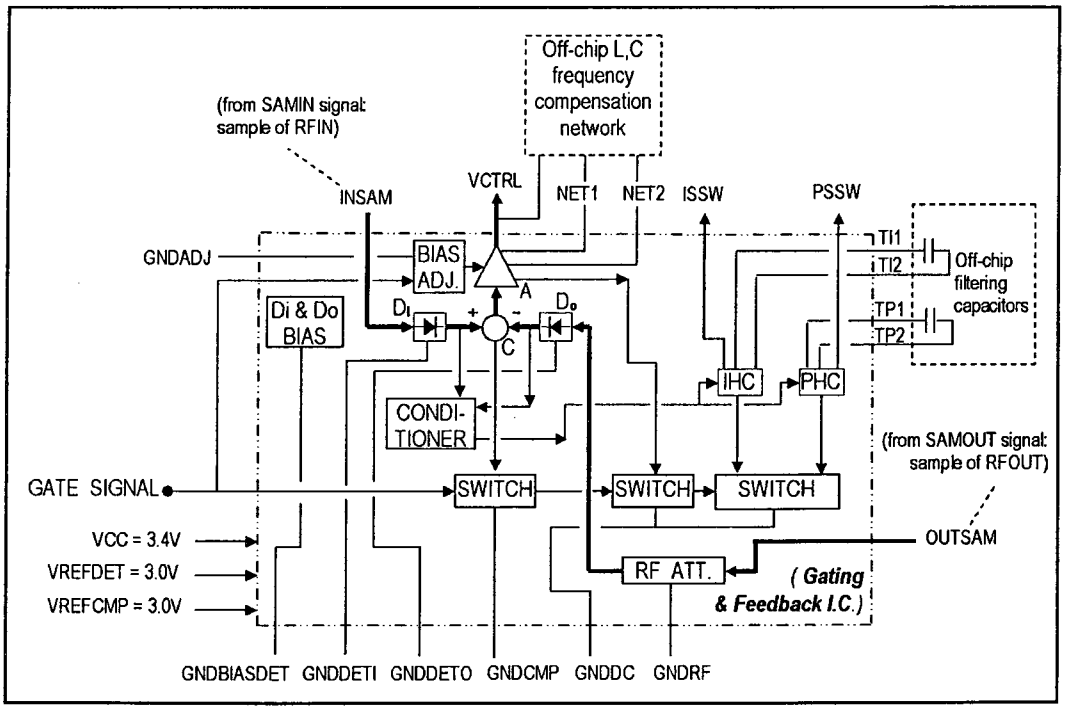

Figure 3.3.1: Block diagram of the gating, envelope feedback and hardware reconfiguration control circuitry.

3.3.2 Envelope detector and envelope comparator circuits

Fig. 3.3.2 shows the schematics of the input and output RF envelope detectors and the envelope error comparator that were implemented on this second GaAs HBT IC, as part of the gating function and feedback circuitry.

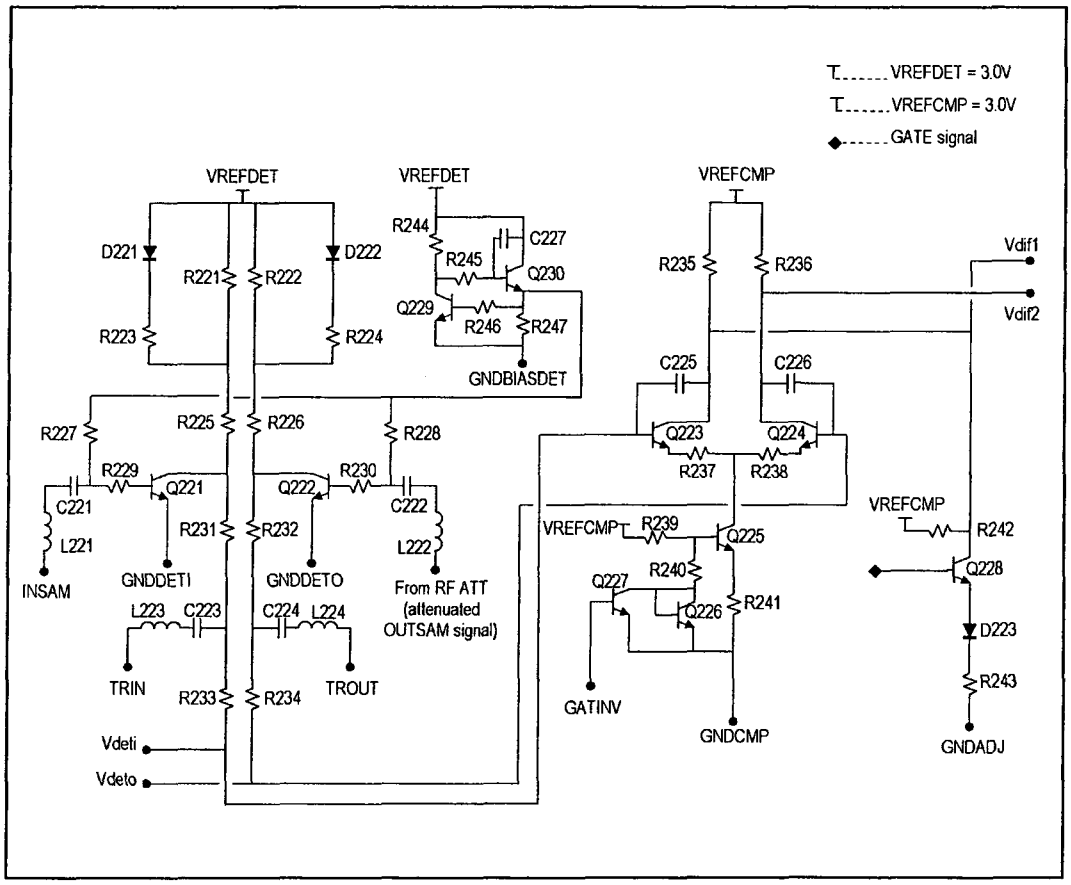

Figure 3.3.2: Schematic of the RF envelope detectors with their separate bias circuit, the envelope comparator, and the d.c. offset adjustment circuitry.

This RF envelope detector circuit topology has been chosen over the more sophisticated on-chip detector topologies that have been proposed (e.g. [49]) in order to allow the use of a minimum of on-chip cells and a compact layout, which facilitates their integration in GaAs HBT

technologies, and to guarantee as closely matched performances as possible, using as much symmetry as possible in the layout. Their nonlinear RF to analog conversion gain characteristics across the effective feedback operation range, the crossover range, and the small signal range have been optimized as per the design guidelines (ii) and (iii) discussed in section 2.6.5.

Circuit description

Each one of the detectors is built with a single NPN transistor (Q221 and Q222) biased at a low quiescent current through a resistor in the RF path at the base (R229 and R230), and a resistor in the bias path (R227 and R228). A series LC network is used at the base (L221,C221 and L222,C222) for impedance matching at 1.88GHz, and at the same time to act as a d.c. block. As the RF power that is applied to the input of the amplifier system (PA_IN in Fig. 3.2.9) increases, the average collector current varies from its quiescent condition until it reaches a maximum current value that corresponds to the maximum peak input RF power, in conformity with the self-biasing mechanism that is typical of transistors biased in a class AB [8]. The resulting envelope voltage signals at the collectors of Q221 and Q222 are applied to the envelope error comparator circuit after being filtered by the RC networks (R231, C223 and R232, C224) and by the notch filters (C223, L223 and C224, L224) that are designed for maximum rejection of the RF signal components.

As part of the optimization of the gating function, the RF to analog conversion gain profiles of the detectors are shaped with the help of resistors and diodes in the collector circuits of Q221 and Q222. At input RF power levels that are below ~ -12dBm, the collector currents are low and the diodes D221 and D222 are turned OFF. The conversion gains are then optimized for maximum sensitivity but without excessive rate of change as per the design guideline (iii) discussed in section 2.6.5, through careful adjustment of the quiescent currents for Q221 and Q222, and

proper selection of the values for R221 and R222. Beyond some collector current intensity, the voltages across R221 and R222 become high enough to turn ON D221 and D222, which results in a nonlinear compensation effect as a function of power.

Nonlinear compensation

The benefits gained from the nonlinear compensation network may be seen in Fig. 3.3.3, where the simulated envelope voltage at the collector of Q221 and the overall closed loop gain of the amplifier system (Fig 2.6.2) are shown as functions of the power applied to the input of the amplifier system (PA_IN in Fig. 3.2.9), for a first case where the collector circuitry is purely resistive, hence linear, and a second case where the above described nonlinear compensation mechanism is implemented.

In the first case, the high conversion gain at RF input power levels of -12dBm and above causes the detected envelope signal to drop too rapidly over the power axis, resulting in gain compression in the feedback loop, and eventually a collapse of the closed loop gain at -4dBm and above.

In the second case, the nonlinear compensation effect using diodes D221 and D222 is self-triggered at ~ -12dBm, and maintains an adequate feedback operation beyond +2dBm. It may be deduced from the RF power axis of Fig. 3.3.3 that for the same detected voltage swing from 2.75V to 1.9V, the input RF power dynamic range applicable to the detectors is improved by 8.5dB, thanks to this compensation scheme. This implies an 8.5dB increase of the effective feedback operation range, i.e. an increase of a power range where automatic hardware reconfiguration is applicable (Fig. 2.6.1).

While some of the nonlinear effects that result from this compensation are reflected at the output of the amplifier, the associated gain deviation is kept to a minimum, as can be seen in Fig. 3.3.3 (i.e. ~0.3dB peak-to-peak between -20dBm and -5dBm), by allowing the diodes to turn ON or OFF only within the effective feedback operation range (which corresponds

approximately to power levels between -15dBm and +2dBm), thus taking advantage of the benefits brought by the matched performances of the detectors, as analyzed in section 2.6.5, referring to the transfer function expressed by eq. (2.5.10). Allowing the diodes to switch outside this range, where the loop gain is significantly lower, may result in much larger gain perturbations and severely degraded linearity performances, because of the nonlinear gain variations that may be associated with the terms $F(s)$ and $f_{Do}(s)$, and which would affect the closed loop gain, as represented in the first term of eq. (2.5.9).

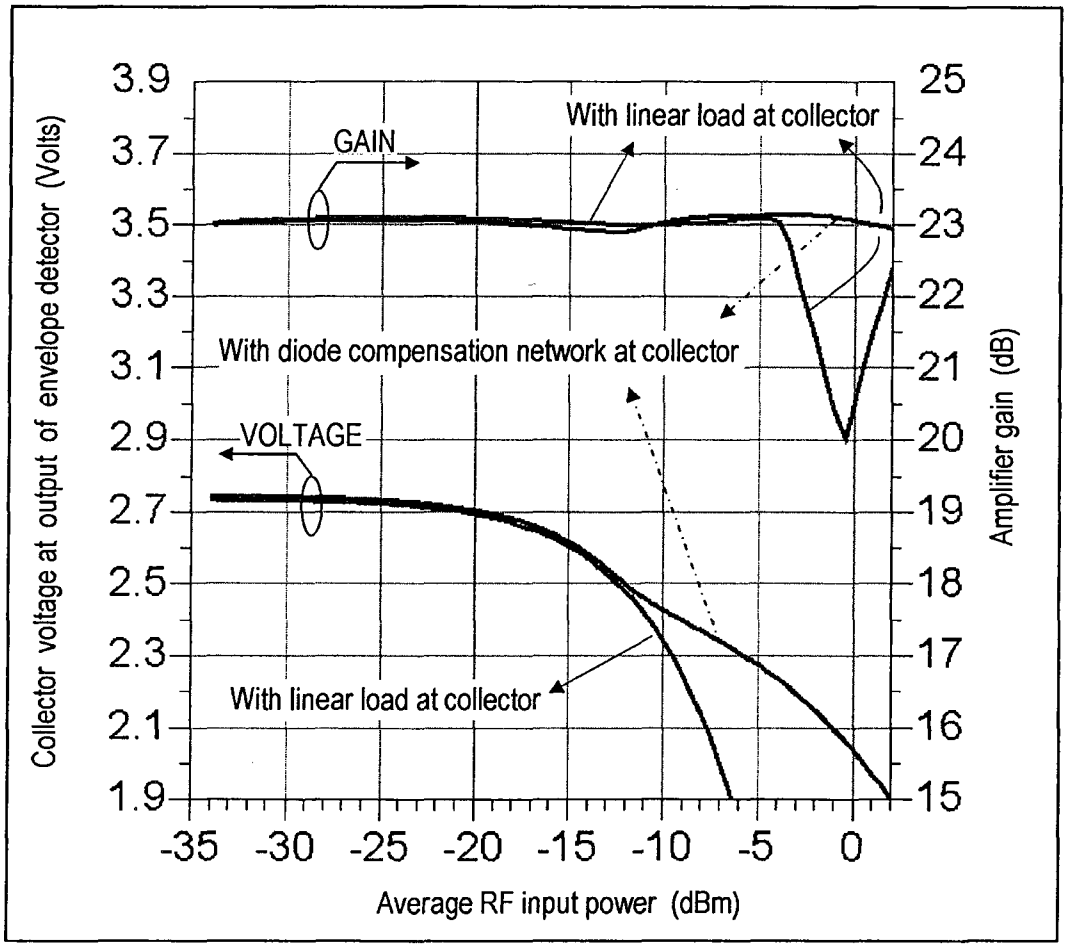

Figure 3.3.3 The simulated dynamic range of the envelope detector and the gain of the amplifier system, versus the average input power.

Error comparator circuitry

The error comparator uses a pair of transistors in a differential configuration (Q223, Q224) and desensitized against RF coupling with the use of capacitors between the base and the collector of each transistor (C225, C226). The comparator is biased with a temperature compensated current source (including Q225, Q226), which is shut OFF for minimum current consumption with the help of transistor Q227 when the envelope feedback circuitry is disabled, i.e. with the GATINV signal (the inverse of the GATE signal) at logic high.

DC offset adjustment for small signal gain control

The d.c. offset voltage between V_{dif1} and V_{dif2} at the output of the error comparator is used to adjust the average value of the VCTRL signal in Fig. 3.3.1 (i.e. CTRL in Fig. 2.6.2), and thus to optimize the small signal gain offset (Fig. 2.6.1) as per the design guideline (i) discussed in section 2.6.5. The offset voltage control is achieved by sinking part of the current circulating through R242 into Q228. When the envelope feedback is enabled (i.e. GATE at logic high) the upper voltage range of the GATE signal (1.8V to 2.8V) is used for this fine tuning adjustment. The VBE voltage drop of Q228 and the voltage across D223 set the threshold for enabling this adjustment, while the value of R243 determines the range of the adjustment. The temperature dependence of this adjustment may be predicted consistently with the use of correction factors in a look-up table.

3.3.3 The error amplifier and the phase compensator

Fig. 3.3.4 shows the schematics of the error amplifier, which includes a phase compensation circuit.

Circuit topology for optimum rejection of noise and perturbations

The error amplifier includes two differential stages (built with Q251, Q252 and Q257,Q258) which are biased with temperature compensated current

sources (using Q253 and Q259), and which are limited in their frequency responses with the use of capacitors (C251, C252 and C253, C254) between the base and the collector of each transistor, for improved immunity against RF coupling and for noise reduction.

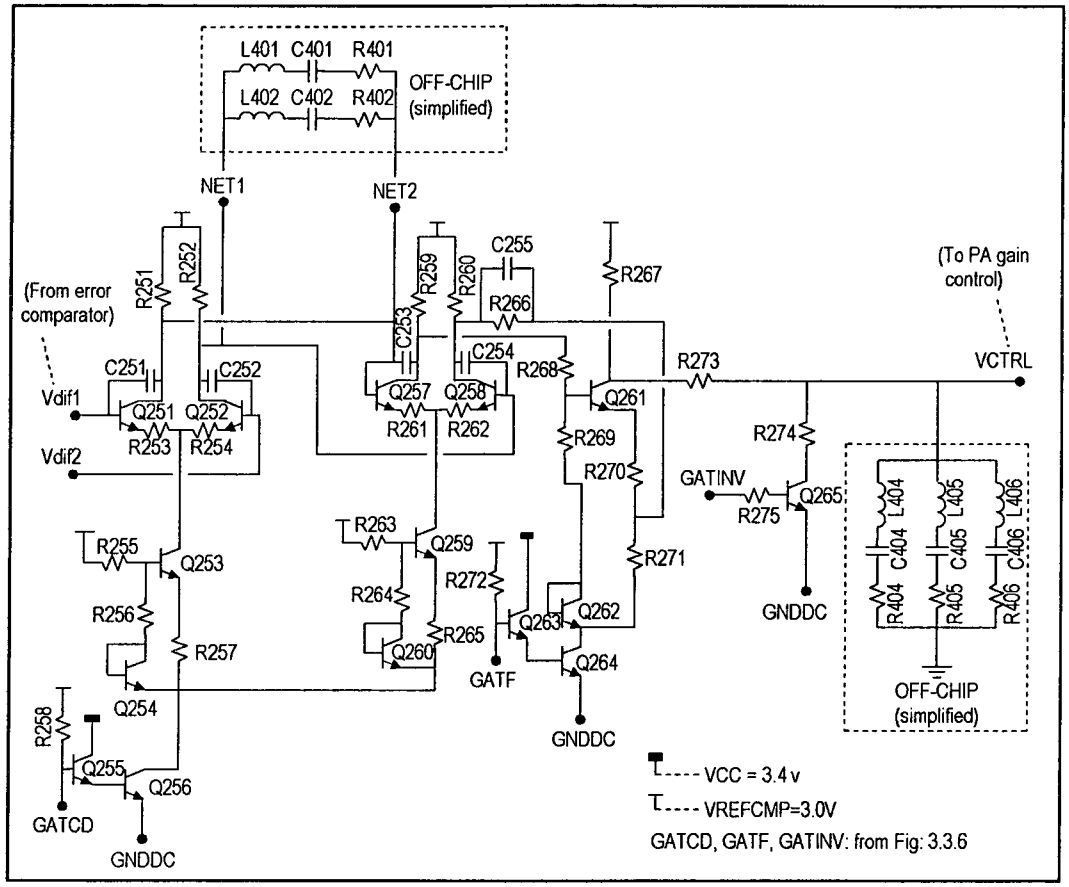

Figure 3.3.4: Schematic of the error amplifier.

These two stages are followed by a temperature compensated single-ended output amplifier stage (built with Q261) that delivers the common mode gain control signal VCTRL for the feedback operation. All stages are biased through NPN switches (Q256 and Q264) biased in a Darlington configuration (Q255, Q256 and Q263, Q264) and that operate in saturated mode when the GATCD and GATF signals (which are buffered signals derived from the external GATE control signal for fan-out considerations)

are at logic high. Hence, the error amplifier may be completely shut off when the envelope feedback is disabled, i.e. with the GATE signal at logic low.

The differential structure of the amplifier improves immunity to noise and reduces the effects from voltage perturbations across the NPN switches and which fluctuate with the RF power level, due to the inevitable interaction between the RF signals and the analog circuits in an on-chip embodiment.

LC resonators at the output of the first differential stage and at the output of the error amplifier are used as notch filters and phase compensators in order to provide the appropriate gain and phase margins in the open loop envelope frequency response, for stability and optimum transient performances that have to comply with the metrics given in section 2.4.2 for CDMA2000 transmission. Since these resonators are tuned at relatively low frequencies (~8 MHz to 100 MHz), the inductors may be placed outside the amplifier module without any significant impact on the resonance frequencies, provided that the lengths of the additional interconnect traces on the printed circuit board are kept short.

Design for optimum gain regulation

The role of the error amplifier is to provide enough gain in the feedback loop for precision. The performance criteria which was used is a maximum steady-state gain deviation of ~ 0.15dB upon the reconfiguration of the intermediate stage (IS) and the power stage (PS) shown in Fig. 3.2.1 (i.e. at the P_{th2} and P_{th3} thresholds shown in Fig. 2.6.1). This compares favorably with the 0.5dB precision specification that relates to the incremental power control steps requirements for CDMA2000 mobile terminals [50]. A simplified system level simulation set-up was used for the simulation of the envelope feedback architecture shown in Fig. 2.6.2, in order to estimate the loop gain which is required to achieve this steady-state error performance. The results indicated that for input power levels

that are within the effective feedback operation range, and in the condition where ISSW and PSSW are at logic high (Fig. 3.2.12), this goal can be met with an overall 36dB feedback loop gain in static conditions (i.e. the quantity $|A_v(s)P(s)G(s)f_{Do}(s)H(s)|$ from Fig. 2.5.2 evaluated at $s = j\omega = 0$, and with the gain of the comparator included in $A_v(s)$), which translates into a 35.7dB gain in the analog error amplifier.

Simulated open loop envelope frequency response

Fig. 3.3.5 shows the simulated open loop gain and phase response of the envelope feedback system, as well as the phase response required in the analog error amplifier alone in order to achieve the stability and transient performance goals.

It can be seen from these results that the 36dB static gain objective is met, and the ***open loop*** 3dB cutoff frequency is in the vicinity of 1.23MHz. Thus, under closed loop operation where the closed loop gain will be set to significantly lower than 36dB, the 3dB cutoff frequency of the amplifier system will be significantly higher than the CDMA2000 1.2288 MHz channel bandwidth. At the 0dB crossing on the open loop gain curve, the phase margin is 38 degrees (the phase itself being equal to -142 degrees), and at the -180 degrees crossing on the open loop phase curve, the gain margin is 16dB (i.e. an actual gain of -16dB). These stability metrics were simulated with an average input power level of -2dBm, which is in the upper region of the effective feedback operation range. Since the gain and phase margins increase as the input power level decreases, due to the gain decay in the feedback loop with a decreasing power, the stability improves as the input power level decreases across the effective feedback operation down to the small signal range.

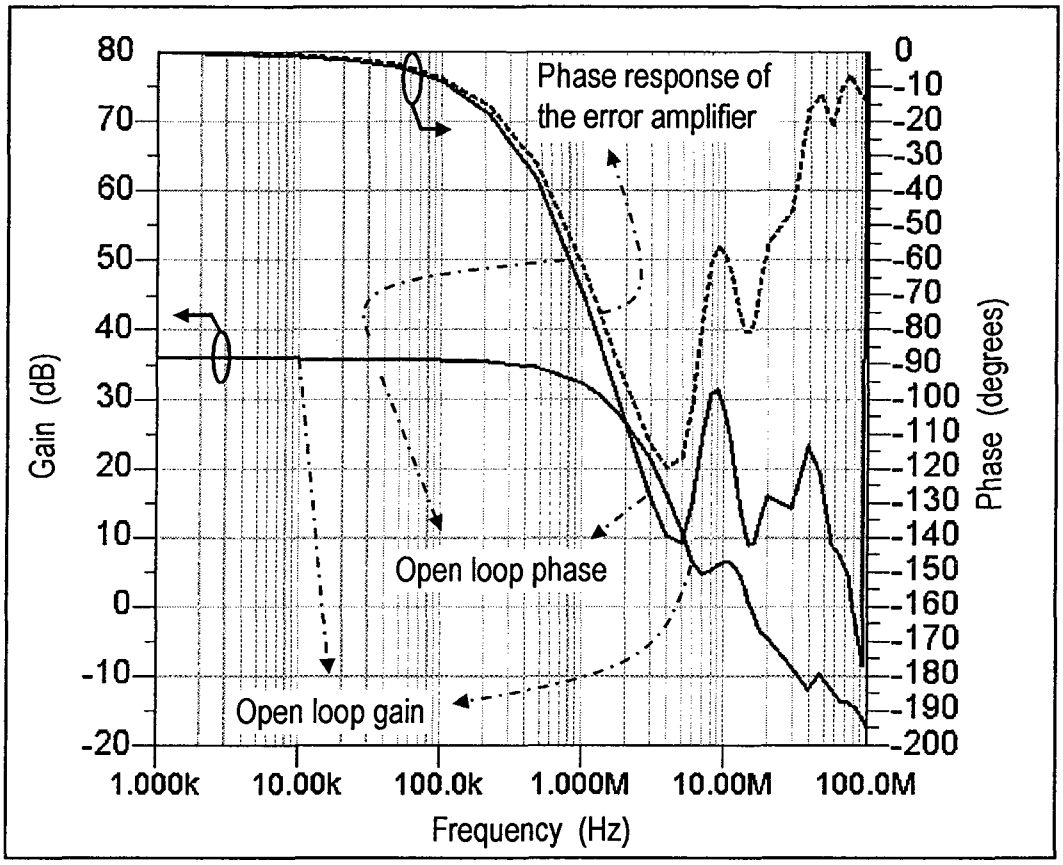

Figure 3.3.5: Simulated open loop envelope gain and phase response of the amplifier system in the condition where ISSW and PSSW are at logic high (see also Fig. 3.2.12). The phase response that is required in the analog error amplifier to achieve the stability and transient performance goals is also shown.

3.3.4 Envelope signal conditioner and hysteresis comparator circuits

Fig. 3.3.6 shows the circuit topology introduced in this work for the implementation of the envelope signal conditioning function and the two hysteresis comparators (IHC and PHC in Fig. 3.3.1), as well as the logic circuitry for the buffering of the GATE signal for fan-out considerations. To the best of the author's knowledge, a circuit topology that allows implementing these key functions using as few components and in a bipolar transistor only technology has not been proposed in the literature.

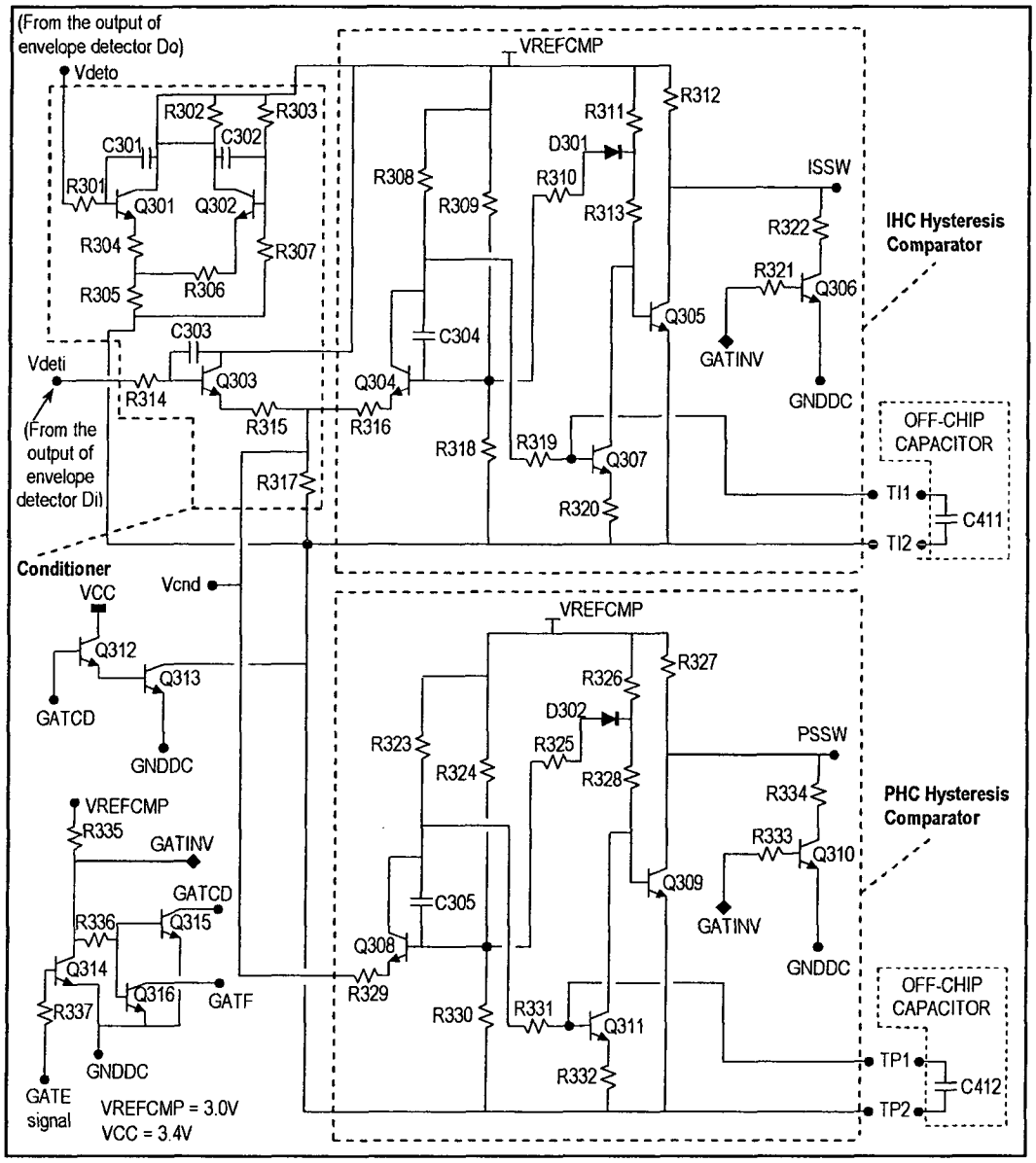

Figure 3.3.6: Schematics of the envelope signal conditioner, the two hysteresis comparators, and the GATE signal buffering.

Circuit topology

The role of the conditioner circuit is to act as a buffer for the envelope signal V_{deti} generated by the input envelope detector (Fig. 3.3.2), and at the same time to adjust the average value and range of this signal to levels that are compatible in terms of amplitude and optimum in terms of

signal to noise ratio for the operation of the hysteresis comparators. The buffering is accomplished by transistor Q303, which is biased in an emitter-follower configuration in order to present a high input impedance, when seen from the output of the input RF envelope detector D_i (Fig. 3.3.1). R315 and R317 provide the necessary level shift to the envelope signal generated by D_i, so that the resulting signal (V_{cnd} in Fig. 3.3.6) is conditioned for triggering the hysteresis comparators at the right thresholds. These thresholds correspond to the average RF input power levels that are appropriate for automatic reconfiguration.

The circuit section that is built-up with Q301, Q302, R301 to R307, C301 and C302 is connected to the V_{deto} signal for the purpose of maintaining an impedance load that is as close as possible to the load on the V_{deti} signal, in order to minimize the perturbations and the d.c. offset between the inputs of the error comparator.

The same type of hysteresis comparator circuit is used to activate the hardware reconfiguration of both the intermediate and power stages via signals ISSW and PSSW, respectively, and hence V_{cnd} is applied to the inputs of both comparators simultaneously through R316 and R329.

Switching circuit logic

The conditioner circuit and the two hysteresis comparators are enabled and their bias currents sunk through switch Q313 when the GATE signal is at logic high (i.e. with GATCD high). These circuit sections are disabled when Q313 is switched OFF with the GATE signal at logic low, and in this condition the control signals ISSW and PSSW are pulled down with the help of Q306 and Q310, which are forced into saturation by the inverted GATE signal (i.e. GATINV). The GATCD and GATF signals are also used to disable the error amplifier by switching OFF Q256 and Q264 in Fig. 3.3.4.

Hysteresis function

With the conditioner and hysteresis circuits enabled (GATE at logic high) to allow automatic hardware reconfiguration, and with the envelope of the RF signal at the input of the amplifier system at a high level, the voltage V_{deti} at the output of the input RF detector is low (see also Fig. 3.3.2 and Fig. 3.3.3), and Q303 is turned OFF. Thus Q304 is biased, and its low collector voltage maintains Q307 in the OFF condition. Since Q306 is OFF when the GATE signal is high, then Q307 in the OFF condition also allows Q305 to be biased in a saturated mode, which forces the output activation signal (ISSW) to be low, and which corresponds to the hardware state where no RF transistor is deactivated in the intermediate stage. In this condition, diode D301 is turned OFF and the voltage at the emitter of Q304 is set primarily by the voltage divider resistors R309 and R318.

Figure 3.3.7 shows simulation results that were used to optimize the hysteresis function, and are also used here in conjunction with Fig. 3.3.6 to further describe its operation. It shows a sine wave that represents the envelope signal V_{deti} (Fig. 3.3.6) delivered at the output of the input detector (D_i in Fig. 3.3.1), the V_{cnd} signal at the output of the conditioner circuit, and the activation signal (ISSW) at the output of the IHC hysteresis comparator of Fig. 3.3.6. At this point a slow sweep time is used to avoid delays in the waveform, and to render the filtering effect of the off-chip capacitor C411 negligible, for clarity.

As the average input RF power decreases and becomes low enough for the activation of the hardware reconfiguration mechanism, the envelope signal voltage at the output of D_i is high enough to bias Q303, and V_{cnd} is raised above a first threshold voltage value (T_H in Fig. 3.3.7). At the crossing of T_H, the emitter voltage of Q304 is high enough to turn this transistor OFF, which allows Q307 to be turned ON and Q305 to be turned OFF. This forces ISSW to toggle at a high level, which corresponds to the

hardware state where half of the RF transistor array in the intermediate stage of the RF amplifier chain is deactivated, for current reduction.

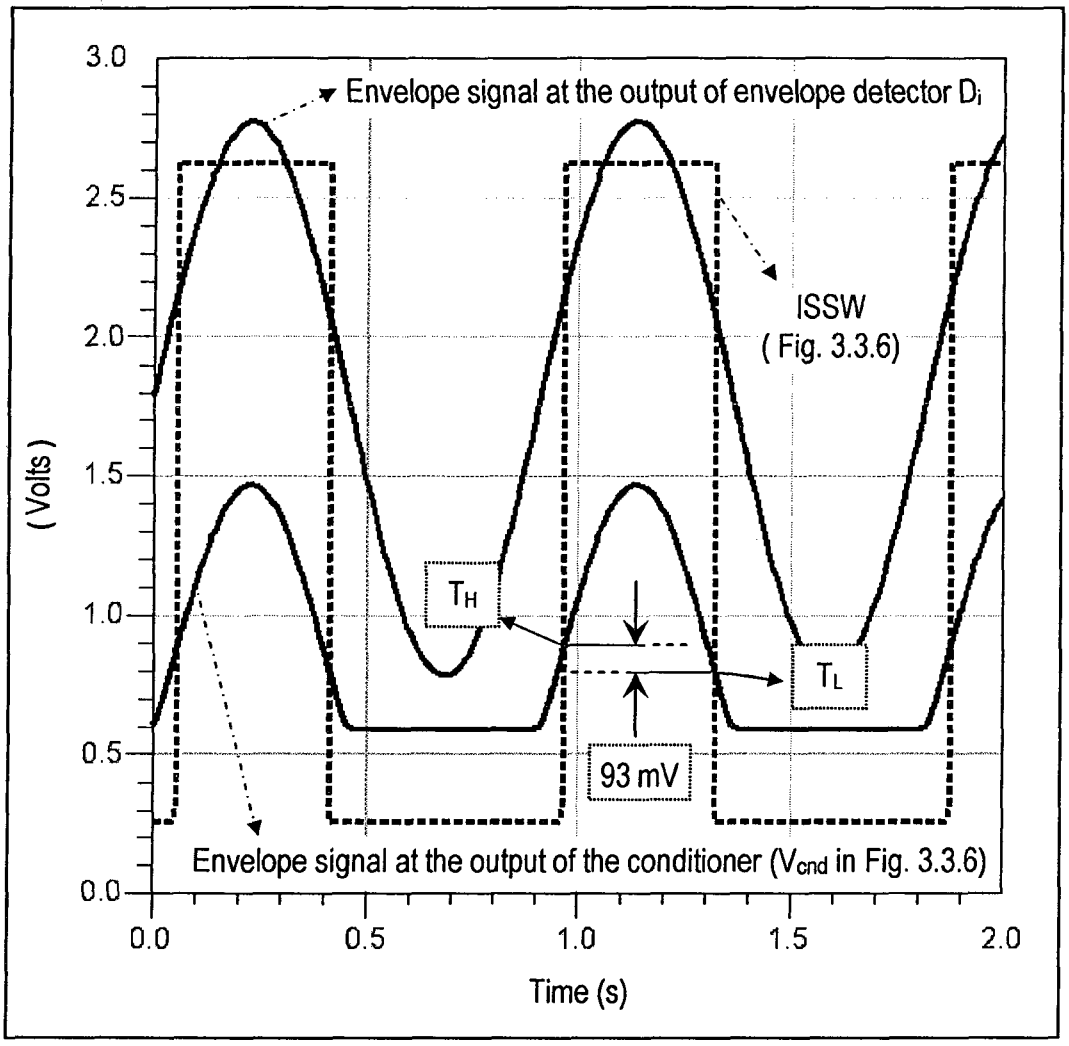

Figure 3.3.7: Simulation results showing the signal conditioning of the envelope signal and the output activation signal of one of the hysteresis comparators (IHC), for automatic hardware reconfiguration.

The saturation of Q307 also allows D301 to be turned ON, with its bias current sunk via R313, and consequently the base voltage of Q304 is lowered. Thus, as the input RF power increases again, which corresponds to the negative slope region of the V_{cnd} signal in Fig. 3.3.7, the lowered

base voltage value requires V_{cnd} to reach a lower threshold voltage value (T_L in Fig. 3.3.7) in order to enable the biasing of Q304 again. The difference between these two threshold voltage values has been set to ~93mV in this design implementation, and defines a hysteresis window of approximately 2dB in the RF power domain, for the toggling of the ISSW activation signal in the hardware reconfiguration mechanism.

Hysteresis window and time constant adjustment

The off-chip capacitor C411 is used as a filtering capacitor, and it has the equivalent effect of restricting the toggling of ISSW with the above described hysteresis feature as a function of variations of the input ***average*** RF power only. The width of the hysteresis window (which is function of the difference between T_H and T_L, i.e. 93mV in this design) and the time response dictated by C411 need to be set properly in order to ensure that the reconfiguration mechanism is not triggered by the instantaneous envelope power of the input RF signal or noise spikes, but instead by the average level of the envelope signal. The amplifier system still needs to offer a fast enough reaction to changes in the average power in order to comply with the open loop or closed loop power control steps requirements for CDMA transmission (see section 2.4.2). The on-chip capacitors C303 and C304 are used to reduce the frequency responses of Q303 and Q304, as a means of desensitizing the conditioner and the comparator against RF perturbations.

The operation of the PHC hysteresis comparator is identical to that of the IHC comparator, with the exception that the thresholds are adjusted for the activation of the PSSW control signal at different average input power levels.

3.3.5 The RF attenuator circuit

The RF attenuator circuit shown in the block diagram of Fig. 3.3.1 is built up with 3 on-chip resistors in a pi network configuration, and their values

(180 Ohms for each one of the shunt resistors and 30 Ohms for the series resistor) have been optimized through simulation to achieve the desired closed loop envelope feedback gain.

3.3.6 IC embodiment of the gating and feedback circuitry, and the hardware reconfiguration control circuitry

The schematic in Fig. 3.3.8 illustrates the I.C. embodiment of the above described gating circuitry, feedback circuitry and hardware reconfiguration control circuitry in a single GaAs HBT IC that is directly bonded on the same single layer PCB of Fig. 3.2.8.

The effects of interconnect tracks on the PCB are modeled with micro-strip transmission line segments (TLi), and the inductive reactances of bond wires (b_n), of the through wafer vias of the IC (LT), and of the PCB vias (Lv and Lp) are also taken into consideration.

This IC is connected to the RF amplifier chain IC (Fig. 3.2.9) via their common signal nodes SAMIN (for the sampling of the input RF signal), VCTRL, ISSW, PSSW, and SAMOUT (for the sampling of the output RF signal) to form the complete gated envelope feedback RFIC PA system.

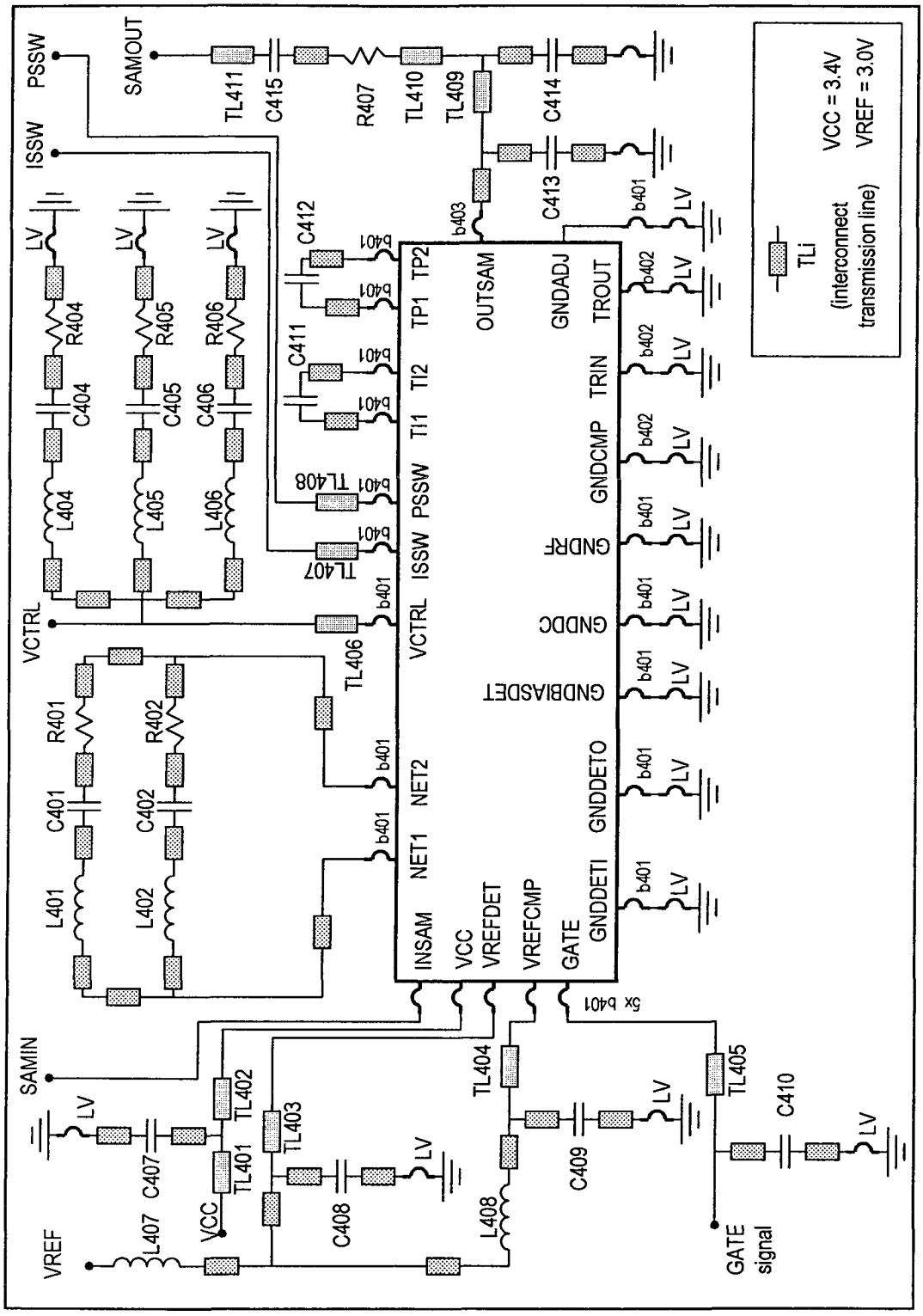

Figure 3.3.8 IC embodiment of the gating, envelope feedback and hardware reconfiguration control circuitry.

Section 3.4

Simulation results for closed loop operation and IMD analysis based on the proposed design equations

This section presents the simulated closed loop performances of the complete gated envelope feedback RFIC PA described by the schematics of Fig. 3.2.9 and Fig. 3.3.8. The design equations that were introduced in section 2.7.4 are used for IMD analysis, following the methodology that was discussed in section 2.7.3. The IMD performances of the envelope detectors are validated in the context of this design. Also, an example is provided to demonstrate how the design equations and the proposed methodology may be applied at the architecture level for the optimization of the IMD and gain performances of the envelope detector and the other circuit blocks in the error signal path of a gated envelope feedback amplifier.

3.4.1 Gain, output power, and input return loss performances

Fig. 3.4.1 shows the simulated gain, output power and input impedance matching performances versus the power applied to the input of the amplifier system (PA_IN in Fig. 3.2.9) in the condition where half of the RF transistor arrays in the intermediate and the power stages are shut off. Despite the gain perturbation due to the triggering of the nonlinear compensation network in the envelope detector circuitry (Fig. 3.3.2) at ~ -12dBm, a reasonable gain flatness is maintained across a 35dB dynamic range, together with a return loss of better than -15dB. This indicates a good optimization of the gating function and the envelope feedback operation across the small signal range, the soft crossover range and the effective feedback operation range.

3.4.2 ACPR performance with a CDMA2000-1X excitation

Fig. 3.4.2 shows the simulated output ACPR performance (V_{out} curve) with a -7dBm CDMA2000-1X excitation applied at the input (V_{in} curve), which yields an average output power of 16dBm. Half of the intermediate stage and half of the power stage are shut off for current reduction purposes, i.e. with the ISSW and PSSW signals at logic high. With -7dBm of average input power, the instantaneous CDMA envelope power sweeps across the small signal range, the soft crossover range and the effective feedback operation range. The worst case -49.1dBc ACPR performance shown for the lower adjacent channel (ACPR_Vout(1)) is well within the -42dBc standard specification for CDMA2000 transmission (see section 2.4.1).

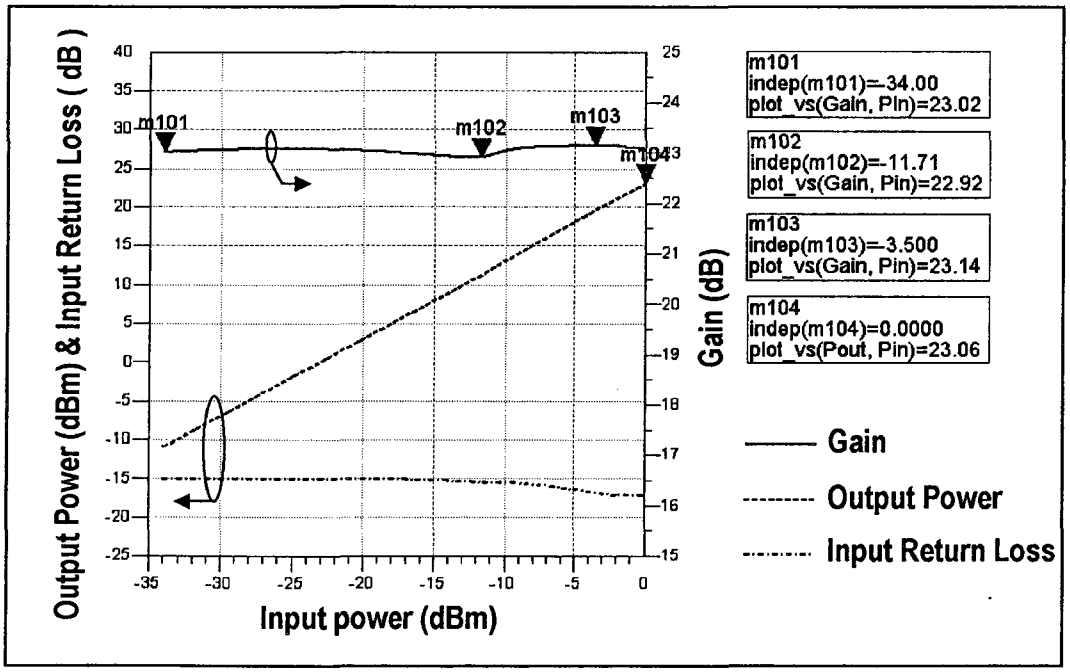

Figure 3.4.1: Simulated gain, output power and return loss performance of the amplifier system in closed loop operation as a function of the input power.

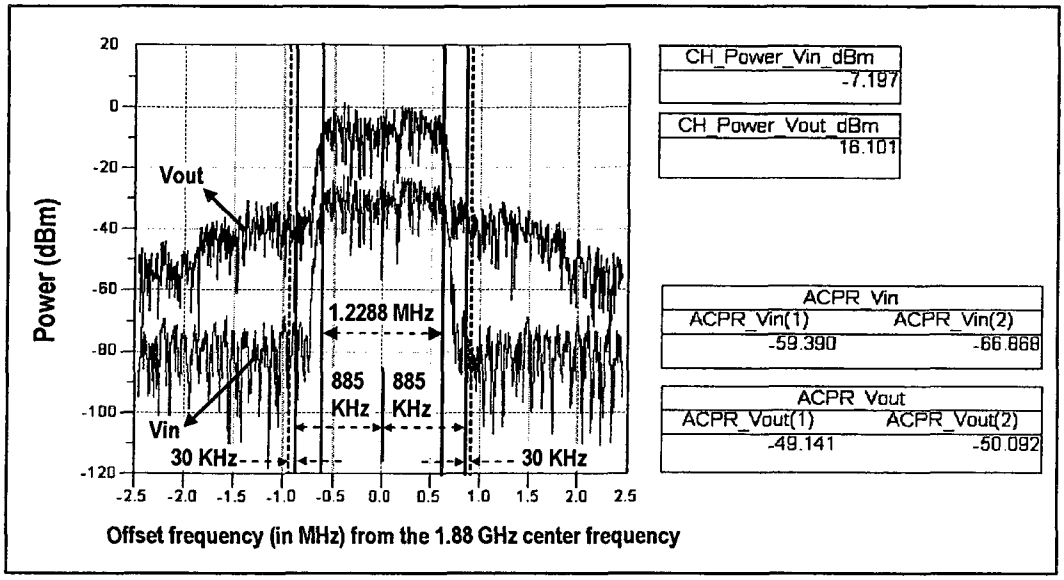

Figure 3.4.2: Simulated linearity performance (V_{out}) in closed loop operation with a CDMA2000-1X input excitation.

3.4.3 Analysis of localized linearity performances of the RF envelope detectors.

The design equations introduced in section 2.7.4 are used in this section, and the methodology that was proposed in section 2.7.3 is used for estimating the linearity performance and design requirements associated with the envelope detector circuitry and the other circuit sections in the error signal path (shown in Fig. 2.7.3), in specific excitation conditions, and as stand-alone circuit blocks. The detector circuitry presented in Fig. 3.3.2, and whose nonlinear conversion gain profile is shown in Fig. 3.3.3, will be evaluated as a separate circuit block in open loop conditions, with the terminals that are connected to inductors L221 and L222 (Fig. 3.3.2) used as the inputs, and the terminals V_{deti} and V_{deto} (Fig. 3.3.2) as the outputs. In conformity with the test criterion described in section 2.7.3, the detectors' linearity performance will be bench-marked against the AM-AM distortion levels that would be expected when referred to the output of the ideal comparator of the system representation of Fig. 2.7.3 in an ideal

case situation, i.e. assuming these distortion levels were function only of the nonlinearities of the power amplifier block (G in Fig. 2.7.3) and the small signal feedback loop parameters, and assuming no distortion is added in the error signal path. The gain and distortion characteristics associated with the RF amplifier chain of Fig. 3.2.1 in the static condition where the ISSW and PSSW signals are at logic high (see also Fig. 3.2.12) will be used in this analysis to represent the power amplifier block of Fig. 2.7.3 with typical amplifier characteristics. The small signal envelope feedback parameters associated with the design presented in section 3.3 will also be used for this analysis.

It is worth noting here that in the proposed design methodology, the use of the design equations allows avoiding a full simulation run on the entire gated envelope feedback system for such linearity analyses, within the scope of evaluating performance figures or deriving architecture level specifications for the detectors, the other circuit blocks in the error signal path, and the feedback loop parameters. The pertinence of this stems from the need for equation based analyses as discussed in section 2.7.1.

Localized nonlinearity effect introduced by the envelope detector compensation circuitry

This analysis is localized in the power domain, i.e. for a limited input power sweep chosen in this case in the vicinity of the input power threshold (i.e. ~ -12dBm when referred to PA_IN in Fig. 3.2.9) where the self-triggering of the nonlinear diode compensation network in the detector circuitry (Fig. 3.3.2) occurs. As shown in Fig. 3.4.1, the self-triggering mechanism at this power threshold introduces nonlinearities that cause a noticeable perturbation in the closed loop gain, and thus represents a pertinent case example for investigations using a localized distortion analysis. Within this scope, and under the memoryless assumptions discussed in section 2.7.3, this analysis will allow estimating the amount of linearity degradation introduced through the envelope detectors in the

vicinity of this power threshold, and accordingly will allow estimating the possible range of linearity performance improvement in the envelope detector circuitry, when referenced to the optimum linearity performance that could ultimately be achieved, given the small signal feedback loop parameters at this power level. This type of analysis is useful also as a basis for estimating how much performance relaxation in the feedback loop parameters could be envisaged at the specific power level considered.

Approximation for the gain control element

The variable gain characteristics of the RF amplifier chain shown in Fig. 2.6.2 may be reasonably well approximated with the use of the equivalent gain control representation of Fig. 2.7.3 when the excitation signal has limited envelope variations. For this purpose, the envelope of the RF_INPUT signal in Fig. 2.6.2 is associated with the envelope V_{ie} of the input signal V_i in Fig. 2.7.3, the envelope signal at the output of the power stage (PS) is associated with the envelope V_{oe} of the output signal V_{out}, and the a.c. component of the $CTRL$ signal line is associated with the a.c. signal V_p. As detailed in the behavioral model description in section 2.7.3, the characteristics of the RF amplifier chain will be represented by a gain function G that is defined with a power series, and its variable gain characteristics approximated with the help of a gain control element (as shown in Fig. 2.7.3) whose output envelope signal (V_{ae}) is considered to be adjusted dynamically through feedback as a linear function of the control signal V_p only, and in a proportion that is defined by the gain control parameter P. This parameter may be approximated in different ways that yield different degrees of accuracy.

For the purpose of this analysis, the simple method chosen for the approximation of P can be justified with the following observations.

Simulation performed on the RF amplifier chain alone shows that, for a given constant envelope amplitude V_{ieo} of the signal V_i, a small variation of the signal V_p yields an almost proportional variation in the envelope signal gain $G(V_p)$ defined as $\frac{V_{oe}(V_p)}{V_{ieo}}$, and in a static condition $G(V_p)$ has a value G_{Vp0} that corresponds to $V_p = 0$, $V_{ie} = V_{ieo}$. In addition, with V_p kept constant, the gain $\frac{V_{oe}}{V_{ie}}$ varies only moderately when the amplitude excursions in V_{ie} are limited to a small range in the vicinity of a given average value of V_{ie}. This tends to support the rationale of approximating the effect of a small incremental adjustment of the gain through feedback with an incremental adjustment of V_{ae} that is a function of V_p only (i.e. $\Delta V_{ae} = P \cdot V_p$), for the purpose of simplifying the formulations.

From the above observations, the following approximation can be made assuming small variations in V_p:

$$V_{oe}(V_p, V_{ie}) \cong G(V_p) \cdot V_{ie}\Big|_{V_{ie} = V_{ieo}} \qquad (3.4.1)$$

with

$$G(V_p) = m \cdot V_p + G_{Vp0} \qquad (3.4.2)$$

and with m being a constant that reflects the approximation made for the V_p to $G(V_p)$ proportionality. Hence, substituting (3.4.2) into (3.4.1) yields the expression:

$$V_{oe}(V_p, V_{ie}) = m \cdot V_p \cdot V_{ie} + G_{Vp0} \cdot V_{ie}\Big|_{V_{ie}=V_{ieo}}, \qquad (3.4.3)$$

which translates a small variation in the gain defined by eq. (3.4.2) into a small output voltage variation as a function of V_p.

Assuming F in Fig. 2.7.3 is equal to 1, the following boundary consideration and derivatives apply, and are useful for the estimation of P in Fig. 2.7.3 through simulation or measurements on the RF amplifier chain, being given that the signal V_a does not exist physically in the circuit:

$$\lim V_p \to 0 : \; V_{ae}(V_p, V_{ie})\Big|_{\substack{F=1 \\ V_{ie}=V_{ieo}}} = \frac{V_{oe}(V_p, V_{ie})}{G_{Vp0}}\Bigg|_{\substack{F=1 \\ V_{ie}=V_{ieo}}} \qquad (3.4.4)$$

and thus:

$$P = \frac{\partial V_{ae}(V_p, V_{ie})}{\partial V_p}\Bigg|_{\substack{F=1 \\ V_{ie}=V_{ieo}}} = \frac{1}{G_{Vp0}} \cdot \frac{\partial V_{oe}(V_p, V_{ie})}{\partial V_p}\Bigg|_{\substack{F=1 \\ V_{ie}=V_{ieo}}} = \frac{1}{G_{Vp0}} \cdot m \cdot V_{ieo}\Big|_{F=1}. \qquad (3.4.5)$$

The dependence of P on V_{ieo} in eq. (3.4.5) indicates that despite the boundary consideration $V_p \to 0$ for the estimation of the gain control parameter P in Fig. 2.7.3, the representation of the effects of a small gain increment in the amplifier chain with the small incremental quantity $\Delta V_{ae} = P \cdot V_p$ will yield an increasing error as the amplitude excursions in V_{ie} departs from V_{ieo}, as a result of the modulation of the input signal.

Nonetheless, because of the drastic simplifications it brings to the formulations, a constant gain control parameter P and a dependence of ΔV_{ae} on V_p only will be assumed in this analysis, and the uncertainty due

to the dependency of P on V_{ie} will be mitigated through the limitation of the peak-to-average ratio of the envelope signal V_{ie}. Some more insight into this uncertainty will be provided in the context of this analysis, and it will be shown that this approach yields error margins that are quite acceptable.

Hence, the above rationale justifies the approximation of the gain control parameter P defined by eq. (3.4.5) through simulation or measurements using small increments ΔV_p in the control signal V_p, and with the RF signal V_i set at a constant amplitude corresponding to the average input power of interest at the RF_INPUT signal node in Fig. 2.6.2. Thus, P may be approximated with

$$P \cong \frac{1}{G_{Vp0}} \cdot \left. \frac{\Delta V_{oe}}{\Delta V_p} \right|_{V_{ie}=constant,\ F=1} . \qquad (3.4.6)$$

Accordingly, an RF-envelope simulation performed on the RF amplifier chain with a -12dBm input carrier signal at 1.88GHz (applied to PA_IN in Fig. 3.2.9) and a small modulation of the gain control voltage V_p (VCTRL in Fig. 3.2.9) at 1KHz allows the extraction of the envelope gain along the amplifier chain (between SAMIN and SAMOUT in Fig. 3.2.9) at 1.88GHz, and thus allows estimating a gain control parameter P equal to 0.045 for input power levels that are in the vicinity of the -12dBm threshold.

Small signal open loop parameters

The small signal envelope feedback loop parameters associated with the design described in sections 3.2 and 3.3 are also used in this analysis. Simulation sessions performed on the gated envelope feedback amplifier system in open loop conditions, and using a -12dBm carrier signal at 1.88GHz with small envelope variations at low frequencies, allow determining the small signal gains in the envelope frequency response

through the envelope detector, the comparator, the error amplifier, the RF amplifier chain, and the feedback path. These values will be summarized in Table 3.4.1 below.

The overall low frequency loop gain drops to ~42 at this input power level (from ~63 in the condition associated with Fig. 3.3.5, i.e. with -2dBm of input power). The envelope amplitude to detected voltage conversion gain (i.e. f_D in Fig. 2.7.3) is equal to 2.466 (i.e. 7.84dB). The comparator and analog error amplifier voltage gains (C and A_v in Fig. 2.7.3) are equal to 6.187 and 61.31, respectively. Hence, the low frequency gain product E (i.e. $(f_D C A_v)$) used in the definition of eq. (2.7.17) to (2.7.21) is ~935. The reverse path attenuation (i.e. H in Fig. 2.7.3) is 0.124, and since no voltage attenuation or amplification element precedes the input of the power amplifier block, the forward conversion gain (F in Fig. 2.7.3) may be set to 1.

Power series representation of the amplifier block

Fig. 3.4.3 shows the voltage gain and phase responses that will be used to represent the AM-AM and AM-PM relationships between the signal applied to the input of the amplifier block (V_a in Fig. 2.7.3) and the output signal (V_{out} in Fig. 2.7.3). These data were obtained through simulation performed on the RF amplifier chain described in Fig. 3.2.1 alone (see also Fig. 3.2.9), assuming a fixed output load and fixed bias conditions, in the hardware state where half of the intermediate stage RF transistor periphery and half of the power stage RF transistor periphery were shut off (i.e. the condition with ISSW & PSSW at logic high as shown in Fig. 3.2.12), and considering the RFIN and SAMOUT terminals (Fig. 3.2.1) as the input and the output, respectively. A continuous wave input excitation with stepped amplitudes at 1.88GHz was used to generate the steady-state gain and phase response at this frequency for each amplitude step, over a range that corresponds to the input signal amplitude range shown

in Fig. 3.4.3. The band-pass output matching network used for simulation (Fig. 3.2.8) rejects the harmonics at the SAMOUT terminal by 12dBc at $2\omega_c$, 20dBc at $3\omega_c$ and even more at $4\omega_c$ and above. Therefore, it will be assumed, as a realistic approximation which is appropriate in this type of analysis, that the gain shown in Fig. 3.4.3 corresponds to the 1.88GHz centered band-limited AM-AM nonlinear response described by equation (2.7.9).

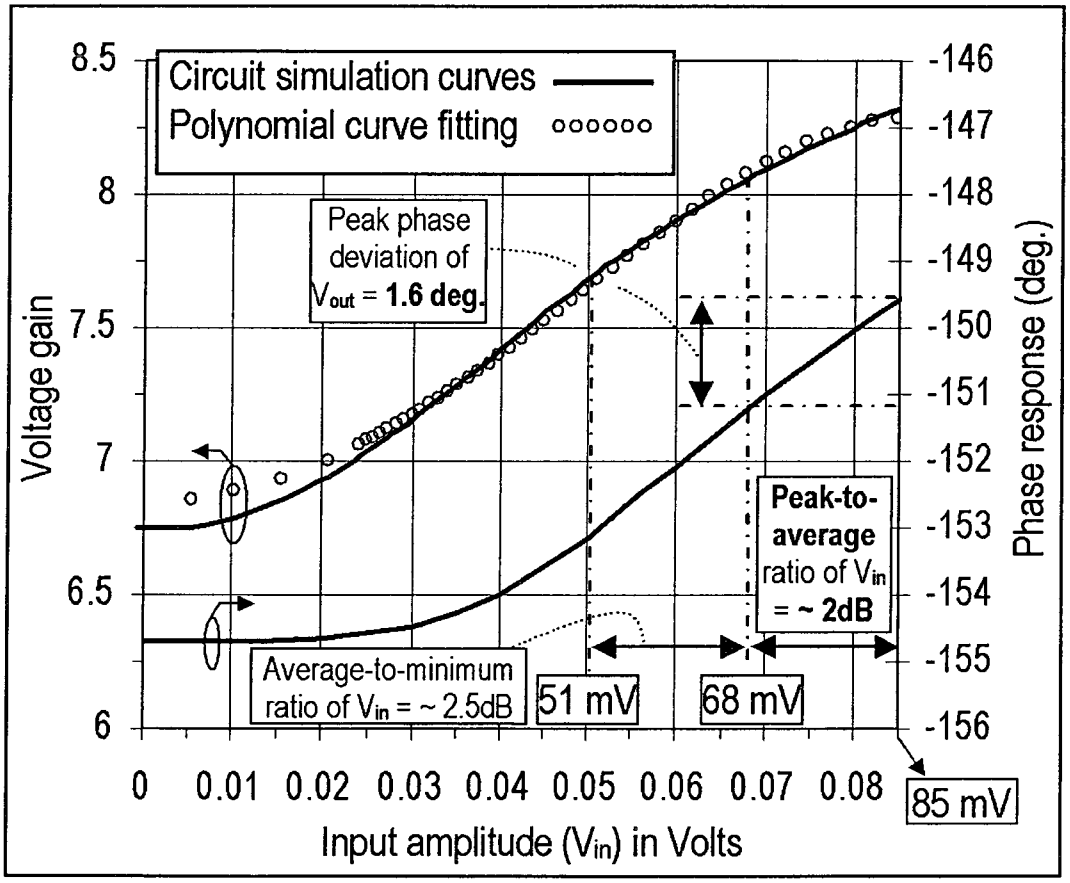

Figure 3.4.3: Simulation results for the amplifier block's band-limited input to output gain and phase relationship, together with a 5th degree polynomial curve fitting based on the coefficients a_1, a_3', and a_5'.

Using a mathematical curve fitting tool (MATLAB$^{(TM)}$), a fifth degree power series was extracted to describe with sufficient accuracy the corresponding memoryless input to output voltage relationship, that is with the scalar polynomial coefficients a_1 = 6.8436, a_3' = (3/4)a_3 = 388.5, and a_5' = (5/8)a_5 = -26187, in order to define the $V_{ae}(t)$ to $V_{out}(t)$ relationship with eq. (2.7.9). Coordinates that are solutions to the polynomial curve fitting with a_1, a_3', and a_5' are plotted on Fig. 3.4.3 to demonstrate a satisfactory match to the simulated response. The coefficients a_1, a_3, and a_5, which are necessary for solving the system of equations (2.7.23), are reported in Table 3.4.1. The nonlinear response of the RF amplifier chain translates into a significant gain variation (~ 6.75 to ~ 8.3) as a function of the amplitude of the input signal, and a moderate phase variation (-154.5 to -149.5 degrees) may also be observed.

Table 3.4.1: Input variables to the system of equations (2.7.23) for the calculation of the amplitudes L, M, N, Q, and R of the mixing products at the output of the amplifier system of Fig. 2.7.3, as well as the envelope error signal components Ve_0, Ve_x, Ve_{2x}, Ve_{3x} and Ve_{4x}.

J(mV)	K(mV)	F	P	E	H	a_1	a_3	a_5
68	8.5	1	0.045	935	0.124	6.8436	518	-41899

Calculation of AM-AM closed loop bench-marking distortion levels from the solutions to the system of nonlinear equations (2.7.23)

With the voltage transformation through the input impedance matching network (including C205, C206 and L201 in Fig. 3.2.9) taken into consideration, simulation allows determining that a continuous wave input power of -12dBm translates into an input signal (V_i in Fig. 2.7.3) amplitude of 68mV. Accordingly, the input variable J that defines $V_i(t)$ in eq. (2.7.10) may be set to 68mV. The envelope variation of this signal will be

limited to a maximum peak-to-average ratio of ~ 2dB (i.e. a ratio of 1.25, corresponding to 85mV over 68mV) and an associated average-to-minimum ratio of ~2.5dB, as an example of a localized nonlinearity analysis with parameterized envelope peak-to-average ratio. Accordingly, the variable K in eq. (2.7.10) may be set to 8.5mV.

Table 3.4.1 summarizes the above defined input variables to the system of equations (2.7.23) for determining the inter-modulation products.

Table 3.4.2: Amplitudes of the mixing products L, M, N, Q, and R at the output of the amplifier system, and of the mixing products Ve_0, Ve_x, Ve_{2x}, Ve_{3x}, and Ve_{4x} of the error signal at the output of the ideal comparator of Fig. 2.7.3.

V_{out} Tones	L	M	N	Q	R
Amplitude (mV)	548.4	68.8	-5.5e-3	-6.9e-3	-691e-6
Amplitude (dBmV)	54.8	36.8	-45.1	-43.2	-63.2
(dBc) relative to L	0	-18	-99.9	-98	-118
V_e Tones	Ve_0	Ve_x	Ve_{2x}	Ve_{3x}	Ve_{4x}
Amplitude (mV)	-1.45e-3	-52.5e-3	1.37e-3	1.71e-3	171e-6
Amplitude (dBmV)	-56.8	-25.6	**-57.2**	-55.3	-75.3
(dBc) relative to Ve_x	-31.2	0	-31.6	-29.7	-49.7

Solving the system of nonlinear equations (2.7.23) with the input variables of Table 3.4.1 yields the solutions for the combined fundamental and AM-AM inter-modulation distortion amplitudes L, M, N, Q, and R associated with the band-limited output spectrum of the envelope

information at the output of the closed loop amplifier system as defined in eq. (2.7.12), and which may be related to the amplitudes of the tones of the envelope error information spectrum (Ve_0, Ve_x, Ve_{2x}, Ve_{3x} and Ve_{4x}) at the output of the ideal comparator of Fig. 2.7.3 using eq. (2.7.24). These solutions are summarized in Table 3.4.2.

Verification of the convergence for computation with MATLAB(TM)

The solutions to the system of equations (2.7.23) and which are reported in Table 3.4.2 were obtained through computation with the use of the "*fsolve*" function in MATLAB(TM) sequentially and manually, while verifying the convergence toward valid solutions through the procedures that follow, and which could be implemented in a software algorithm:

(i) Residual error: for each set of solutions obtained with the "*fsolve*" function, the precision of the solutions was validated by verifying that the outputted Jacobian matrix, which is related to the residual errors in the solutions for the zeros of a multivariable nonlinear system [60], contains only values that are negligible compared to the corresponding variable solution.

(ii) Continuity: the computation was run in multiple sessions for swept values of the input excitation amplitudes J, K in small incremental steps, from J=1mV, K=0.5mV to J=68mV, K=8.5mV, and it was verified that there is no discontinuity in the variations of the L, M, N, Q, and R output mixing products over the entire swept amplitude range.

(iii) Range of the input amplitude for the polynomial function: equation (2.7.25) was used to verify that, with the conditions set in Table 3.4.1, the peak amplitude of the signal $V_{ae}(t)$ at the input of the amplifier block does not exceed the maximum input voltage value (i.e. 85mV in this case) which is applicable to the polynomial representation of the system (as shown in Fig. 3.4.3 for this analysis case).

(iv) Initial conditions for the "*fsolve*" function in MATLAB(TM): for each computation with a small incremental amplitude step in J and K, the

initial conditions that were set for solving the system of nonlinear equations were the approximate solutions that can be anticipated, based on the trigonometric relationships that govern the rate of change of a given mixing product at the output of a weakly nonlinear system as a function of the degree of the polynomial expression, and which relates the input excitation tones to this particular mixing product, similar to case examples provided in [60]. Note, however, that these initial conditions are rough estimates that can only be anticipated for small incremental steps in the excitation amplitudes, and starting from a valid solution.
The following relationships were used to estimate the initial conditions.

The variations in the output tones levels L and M as a function of J and K are close to a linear relationship because of the feedback operation.
Given the typically large difference (as exemplified in Table 3.4.2) between L, M and the IMD levels N, Q, and R (defined in Fig. 2.7.3), it is reasonable to make the approximation that the predominant contribution to the IMD product level N in this weakly nonlinear system comes from a 3rd order response to the excitation tones J (at ω_c) and K (at $\omega_c + \omega_x$), i.e. a response with an amplitude term in the form $a \cdot J^1 \cdot K^2$ (with a being a constant) and which implies a first degree amplitude dependency on J and a second degree amplitude dependency on K. Accordingly, it can be anticipated that a small increase in J (with K kept constant) will result in an increase of N with the same ratio, whereas a small increase in K (with J constant) will result in an increase of N with the square of the ratio.
In the same way, the variation of Q as a function of small changes in the amplitude of K may be anticipated by approximation. The predominant contributions to the IMD product level Q come from a 3rd order response to the two excitation tones of equal amplitudes K (at $\omega_c - \omega_x$ and $\omega_c + \omega_x$), and a 5th order response to the excitation tones J (at ω_c) and

K (at $\omega_c + \omega_x$). These two contributions are unequal, but they are both dependent on a third degree function of K when J is kept constant. Accordingly, the variation of Q may be anticipated by approximation with a cubic dependency on the rate of change in the amplitude variation of K.

(v) Robustness: for every solution obtained and that was assumed to be valid, the computation was rerun with various sets of initial conditions that were different, but that remained in the vicinity of the initial solutions, and in each case the convergence toward the same initial solutions was verified.

Validation of the results through simulation with an envelope signal path model

The block diagram of Fig. 3.4.4 may be used in a simulation set-up to validate the results that were obtained from the system of equations (2.7.23) and reported in Table 3.4.2.

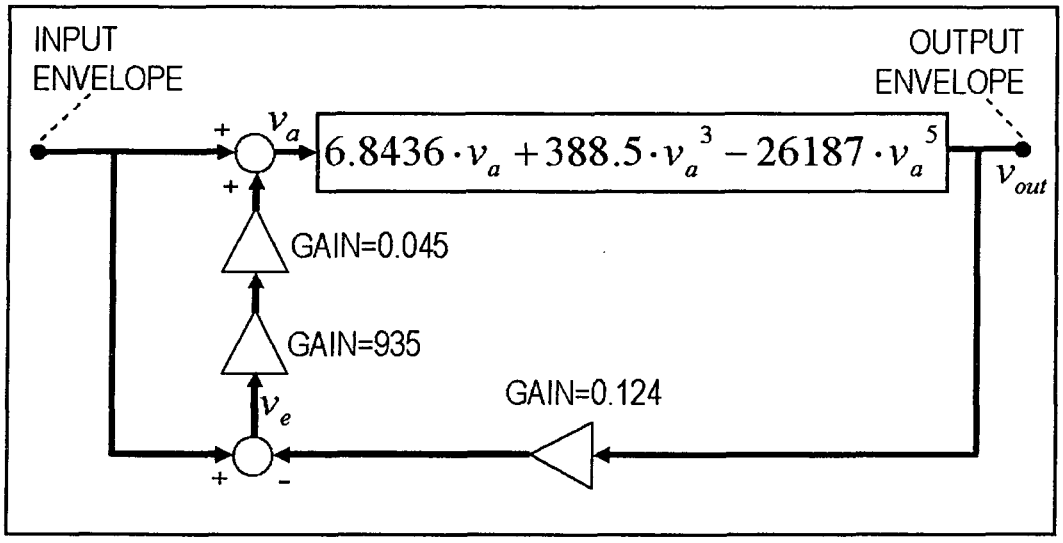

Figure 3.4.4: Block diagram used for simulation and validation of the computed solutions reported in Table 3.4.2.

The polynomial function that represents the V_a to V_{out} transfer function describes the band-limited nonlinear gain response shown in Fig. 3.4.3, and thus is function of the coefficients a_1 = 6.8436, a_3' = (3/4)a_3 = 388.5, and a_5' = (5/8)a_5 = -26187. Using an input envelope signal defined as $(J + 2 \cdot K \cdot \cos(2\pi f t))$, with J =68mV, K =8.5mV, and f being an arbitrary frequency, and with the harmonic content in the analysis limited to $4\omega_x$ and below, simulation shows that the frequency spectrum of V_e and V_{out} are the same as the computed solutions (Table 3.4.2).

Note that V_{e0} in Table 3.4.2 multiplied by E (Table 3.4.1) represents a d.c. offset that is generated through feedback as a gain compensation mechanism, and added to the gain control signal V_p in Fig. 2.7.3. It was also discussed in section 2.7.3 that the approximation for the gain control element in Fig. 2.7.3 is based on the assumption of small deviations in the gain control signal V_p from the condition used for the AM-AM characterization. The $V_{e0} \cdot E$ d.c. offset value may be used to determine a new quiescent condition in the gain control signal for the extraction of a new AM-AM response of the RF amplifier chain (as represented in Fig. 3.4.3) and the associated polynomial coefficients. Therefore, an iterative process that consists of solving the system of equations (2.7.23), determining new quiescent conditions for V_p based on the $V_{e0} \cdot E$ offset, extracting new AM-AM polynomial coefficients, and solving (2.7.23) again, until V_{e0} is minimized, will ensure a minimum of error in the IMD bench-marking levels.

The calculated d.c. offset due to V_{e0} from Table 3.4.2 (i.e. -1.45uV times 935 = -1.36mV) is very small compared to the 1.3V to 2.8V tuning range of V_p (which corresponds to VCTRLP in Fig. 3.2.3), and the a.c. amplitude of V_p (i.e. ~ $V_{ex} \cdot E$) is small. Therefore, the approximation made for the gain control element in Fig. 2.7.3 is applicable in this analysis.

Solutions for different excitation amplitudes and gain parameters in the feedback path

The simulation set-up of Fig. 3.4.4 may also be used to validate the computed solutions reported in Table 3.4.3.

Table 3.4.3: Results from computation using equations (2.7.23) and from the simulation set-up of Fig. 3.4.4, for F=1, P=0.045, E=935, J=50mV, K=6.25mV, and for two values of H corresponding to a gain adjustment of the amplifier system by ~ +2dB or ~ -2dB.

H=0.100	**L (dBmV)**	**M (dBmV)**	**N (dBmV)**	**Q (dBmV)**	**R (dBmV)**	**N-L (dB)**
	53.9	35.9	-41.2	-46.2	-70.9	-95.1
	Ve_0 (mV)	**Ve_x (mV)**	**Ve_{2x} (mV)**	**Ve_{3x} (mV)**	**Ve_{4x} (mV)**	**Ve_{2x} (dBmV)**
	0.294	21.5e-3	-1.75e-3	978e-6	57.1e-6	**-55.2**
H=0.158	**L (dBmV)**	**M (dBmV)**	**N (dBmV)**	**Q (dBmV)**	**R (dBmV)**	**N-L (dB)**
	50.0	32.0	-39.2	-66.1	-93.6	-89.2
	Ve_0 (mV)	**Ve_x (mV)**	**Ve_{2x} (mV)**	**Ve_{3x} (mV)**	**Ve_{4x} (mV)**	**Ve_{2x} (dBmV)**
	-0.180	-74.7e-3	-3.49-3	156e-6	6.64e-6	**-49.2**

These results were computed (using eq. (2.7.23)) with two other sets of conditions, that is with F, P, and E unchanged (i.e. the same as in Table 3.4.1), but with the excitation tones adjusted to J=50mV, K=6.25mV, and the feedback attenuation adjusted from 0.124 to two other values: H=0.100 and H=0.158, which corresponds to adjusting the closed loop gain of the amplifier system by ~ +2dB and ~ -2dB, respectively. The results reported in Table 3.4.3 are identical when computed with both

methods, which validates the correctness of the proposed design equations in predicting the band-limited envelope signal response, given the above excitation conditions and values of H, and the F, P, E values and AM-AM polynomial coefficients of Table 3.4.1.

However, the case with the 2dB gain increase yields a $V_{eo} \cdot E$ d.c. offset of +275mV (i.e. 0.294 times 935), and the case with the 2dB gain decrease yields and offset of -168mV (i.e. -0.180 times 935). These offset values are part the numerical solutions that allow satisfying the system of equations (2.7.23) and the above gain conditions, assuming the fixed AM-AM response of Fig. 3.4.3 to represent G in Fig. 2.7.3. Such significant offset values suggest that the error introduced through the modeling of the gain function as in Fig. 2.7.4 (b) may be considerable. In order to solve for IMD bench-marking figures with the minimum of error, the AM-AM response of the RF amplifier chain would have to be extracted with different quiescent conditions on the VCTRL gain control signal (Fig. 2.6.2) for both cases of Table 3.4.3, based on the corresponding $V_{eo} \cdot E$ offset values and through an iterative process that tends to minimize V_{e0}.

Pertinence of analyzing the Ve_{2x} IMD level at the frequency $2\omega_x$ in the error signal path, and the output distortion at $\omega_c \pm 2\omega_x$

Considering the $(\omega_c - \omega_x)$ to $(\omega_c + \omega_x)$ frequency range in the input signal of Fig. 2.7.3 as the information channel processed by the amplifier system, then any distortion added by the detector circuitry at $2\omega_x$ (which corresponds to the down-converted $(\omega_c - 2\omega_x)$ and $(\omega_c + 2\omega_x)$ output frequency components) will translate into distortion added at the center of an adjacent channel, i.e. between $(\omega_c - \omega_x)$ and $(\omega_c - 3\omega_x)$, or between $(\omega_c + \omega_x)$ and $(\omega_c + 3\omega_x)$. Hence, the evaluation of the $2\omega_x$ IMD product through this multi-tone linearity analysis indicates ***trends that are relevant as well for the study of the adjacent channel power rejection***

(ACPR) performance proper to this system under a digitally modulated excitation (e.g. CDMA).

Estimation of the output AM-PM distortion level at $\omega_c \pm 2\omega_x$

Since in principle the envelope feedback does not accomplish any correction on the phase deviation in the output signal, the AM-PM distortion level generated at the output of the amplifier system may be estimated by calculating the sidebands that correspond to the phase modulation introduced through the RF amplifier chain alone. The trigonometric series representation of the frequency spectrum associated with a phase modulated signal of carrier frequency ω_c and modulating frequency ω_x is given by [65]:

$$f(t) = A\sum_{n=-\infty}^{\infty} J_n(\beta)\cos(\omega_c + n\omega_x)t \qquad (3.4.7)$$

where A is the amplitude of the non-modulated carrier signal, J_n is the Bessel coefficient of n^{th} order, and β is the modulation index, which is equal to the peak phase deviation in radians. In this distortion analysis, the $\omega_c + 2\omega_x$ and $\omega_c - 2\omega_x$ inter-modulation products of concern correspond to $n = 2$, $n = -2$, and from Fig. 3.4.3, it may be deduced that the peak phase deviation associated with the multi-tone excitation used in this analysis is 1.6 degrees, i.e. 0.0279 radian. For a very small modulation index as in this case, the 1st and 2nd order Bessel coefficients may be very closely approximated [65] with:

$$J_1(\beta) = -J_{-1}(\beta) = \frac{\beta}{2}\left(1 - \frac{\beta^2}{8}\right) \qquad (3.4.8)$$

and

$$J_2(\beta) = J_{-2}(\beta) = \frac{\beta^2}{8}\left(1 - \frac{\beta^2}{12}\right), \quad (3.4.9)$$

respectively.

Thus, using $\beta = 0.0279$ in eq. (3.4.9), the output sidebands at $\omega_c + 2\omega_x$ and $\omega_c - 2\omega_x$ due to AM-PM conversion through the RF amplifier chain may be estimated at -80.2dBc relative to the carrier signal at ω_c at the output of the amplifier system (L in Table 3.4.2), i.e. at an amplitude of -25.4dBmV. Despite its phase modulation origin, this AM-PM side-band level will be used in a later section as a reference figure in equivalent amplitude terms (i.e. by considering its power level as an hypothetical AM-AM side-band that can be associated with N in the output spectrum of Fig. 2.7.3) for the purpose only of bench-marking the detectors' IMD performances.

Validation of the design methodology through a comparison between the calculated Ve_{2x} IMD levels and simulation results using the actual RF amplifier chain circuitry

Fig. 3.4.5 shows the block diagram that was used in a simulation set-up for a comparison with the calculated solutions that were reported in Table 3.4.2. In contrast with the set-up of Fig. 3.4.4, the simulation set-up this time includes the complete RF amplifier chain circuitry described in section 3.2 (Fig. 3.2.1 to Fig. 3.2.9), at the same bias and loading conditions as those which were used for simulating the gain response shown in Fig. 3.4.3, and using an AM modulated RF carrier signal at 1.88GHz as input excitation, with J =68mV, K =8.5mV and with a modulating frequency of 1KHz. The impedance loading conditions at the SAMIN and SAMOUT nodes when looking into the RF terminals of the

Feedback & Gating I.C. (Fig. 3.2.1 and Fig. 3.3.1) are emulated with the help of the dummy loads LOAD1 and LOAD2. Ideal AM demodulators are used to extract the input and output envelope information. An ideal shunt band-pass filter centered at ω_c = 1.88GHz may be connected or disconnected from the output of the RF amplifier chain for the purpose of evaluating the effects of the out-of-band signals and loading conditions. When connected, the load seen by the RF amplifier chain at ω_c = 1.88GHz is unaffected and the phase shift perturbation at ω_c = 1.88GHz in the output signal V_{out} is negligible, while all harmonic signal voltages on the V_{out} node are nearly zeroed.

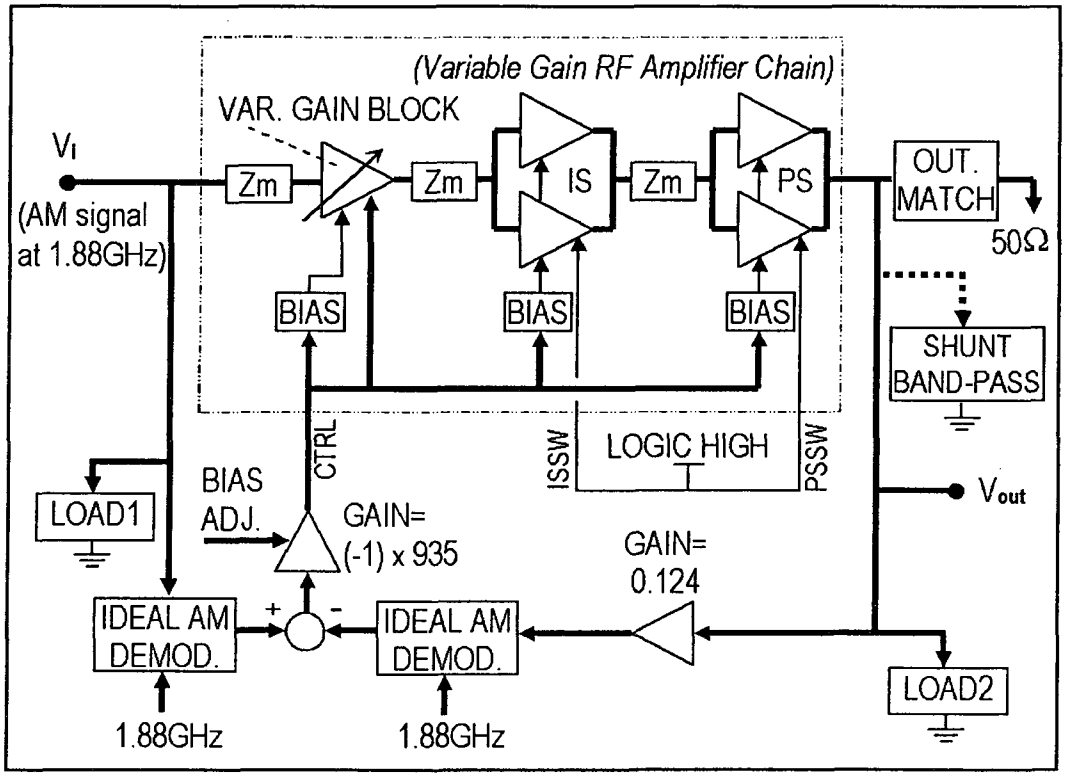

Figure 3.4.5: Simulation set-up using the complete RF amplifier IC circuitry for the validation of the IMD product solutions obtained from the design equations and which were reported in Table 3.4.2.

Table 3.4.4 allows comparing the solutions for the amplitudes of mixing products obtained from the design equations (copied from Table 3.4.2), with those obtained from the simulation set-up of Fig. 3.4.5 for two cases: with the ideal shunt band-pass filter disconnected, and with the filter connected.

Table 3.4.4: Comparison between the solutions to the input variables and system conditions set in Table 3.4.1, and obtained from the design equations (2.7.23) and from the simulation set-up of Fig. 3.4.5.

Solutions from equations (2.7.23)					**Estimated (Fig. 3.4.3)**	
IMD Tones	**L**	**M**	**N**	**Ve_{2x}**	**Phase deviation**	**Level (dBmV) at $\omega_c \pm 2\omega_x$**
(dBmV)	54.8	36.8	-45.1	**-57.2**	1.6 deg. peak	-25.4
Solutions from simulation with the RF amplifier chain circuitry						
IMD Tones	**L**	**M**	**N**	**Ve_{2x}**	**Phase deviation**	**Level (dBmV) at $\omega_c \pm 2\omega_x$**
(dBmV) **No filter**	54.8	36.7	-50.8	**-62.9**	2.0 deg. peak	-21.5
(dBmV) **With filter**	54.9	36.7	-44.2	**-56.3**	1.2 deg. peak	-30.3

In the first case, a difference of ~ 5.7dB in the N and Ve_{2x} components is observed between the solutions from the design equations and the solutions from simulation. This difference may be attributed to the combined effects of all approximations made, including the effects due to the IMD products falling on $\omega_c \pm 2\omega_x$ and that stem from the mixing

between the out-of-band tones that are centered across the harmonic frequencies. From the earlier discussion on the power series representation, these harmonics are as high as -12dBc at $2\omega_c$ and -20dBc at $3\omega_c$. Hence, the non-ideal filtering of harmonics may affect significantly the output $\omega_c \pm 2\omega_x$ IMD products, which are reinserted in the feedback loop and nonlinearly processed, and as a function also of the nonlinearities that affect the RF signal components at the collector of the RF transistors in the output stage (PS).

In the second case, the difference between the calculated and simulated results is reduced to 0.9dB. This is an expected result, since the shunt band-pass filter limits the voltage at the V_{out} node to only the envelope information that is centered at ω_c=1.88GHz (i.e. with no harmonics), which is a condition that conforms with the band-limitation assumption made when solving the system of equations (2.7.23). The residual 0.9dB difference may be attributed to the approximation that is inherent to the polynomial function and the approximation made in modeling the gain control element. Therefore, it also indicates that the approximation made with eq. (3.4.6) yields an error that is quite acceptable.

In both cases, the simulated phase deviation due to AM-PM conversion is slightly different to the 1.6 degree estimate from Fig. 3.4.3, which is justified by the fact that the phase curve shown in Fig. 3.4.3 relates to variations in the input signal amplitude only, and at fixed bias condition, whereas the simulated AM-PM conversion accounts for the effects of a feedback conditioning of the RF amplifier chain through the control of the electronic attenuator and the dynamic biasing of each stage.

Bench-marking of the detectors' linearity performance against the calculated IMD levels in the error signal path

The detector circuits linearity performances will now be bench-marked against the calculated Ve_{2x} performances that are reported in Table 3.4.2

and that are function of the conditions shown in Table 3.4.1. A simulation performed on the two detector branches as a stand-alone circuit block in open loop conditions was carried out to evaluate the added inter-modulation levels in the differential signal at their outputs at the frequency $2\omega_x$. The same biasing and impedance loading conditions that were used for the simulation associated with the compensated envelope detector response of Fig. 3.3.3 were applied.

The simulation was performed with different values of a parameter α, which is a scaling factor applied simultaneously to all resistor values in the nonlinear compensation network of the collector circuit in the input envelope detector branch (Fig. 3.3.2), and used for the purpose of this analysis as a simple metric to measure some level of hardware mismatch between the two detector circuits (note that the Monte Carlo type analyses tools in the ADS(TM) simulation environment could also be used for a more detailed evaluation of hardware mismatch effects).

The same input multi-tone excitation considered for solving the system of equations in this analysis was applied to the input detector during the simulation, i.e. J at the frequency ω_c kept constant at 68 mV and K at the frequencies $(\omega_c - \omega_x)$ and $(\omega_c + \omega_x)$ kept constant at 8.5 mV (see Table 3.4.1). The frequency spacing ω_x was set to 1 KHz for near-zero phase shifts in the envelope frequency response, and thus to ensure conformity with the memoryless assumption. While the solutions from the design equations would allow, in a more general case, considering a multi-tone signal comprising also the frequency components $(\omega_c + 3\omega_x)$, $(\omega_c - 3\omega_x)$, $(\omega_c + 4\omega_x)$ and $(\omega_c - 4\omega_x)$ as an excitation for the output envelope detector, the very low levels of the tones Q and R that were calculated in this particular analysis case allow simplifying the simulation set-up by using excitation tones at frequencies ω_c, $(\omega_c - \omega_x)$, and

$(\omega_c + \omega_x)$ only, with their amplitudes obtained for the corresponding frequencies through the solutions of Table 3.4.2 (i.e. L = 548.4 mV and M = 68.8 mV) and multiplied by 0.124 in order to take into consideration the attenuation H in Fig. 2.7.3.

It is worth recalling here that with these excitation conditions at the inputs of the envelope detectors, and with the use of ideal envelope detectors and an ideal comparator, there would be no mixing product at the frequency $2\omega_x$ in the differential signal at the output of the comparator in the equivalent system representation of Fig. 2.7.3.

The simulated inter-modulation product that is added at $2\omega_x$ by the nonlinear envelope detector circuits presented in Fig. 3.3.2 in open loop conditions, as a function of the mismatch parameter α over a +/-2% span, and with the above input driving conditions, is shown in Fig. 3.4.6. These simulated results have been scaled down by 7.84dB (i.e. the value of f_D obtained from the small signal open loop parameters) in order to account for the conversion gain of the detectors and allow a direct comparison with the closed loop Ve_{2x} = -57.2 dBmV quantity that was calculated and reported in Table 3.4.2 (also shown in Fig. 3.4.6), thus allowing a comparison of performance levels referred to the output of the ideal comparator in the equivalent system representation of Fig. 2.7.3.

For the purpose of this analysis, it is assumed that the -25.4dBmV AM-PM side-band level that was estimated from Fig. 3.4.3 with the help of eq. (3.4.9) does not actually contribute to the detected voltage at the frequency $2\omega_x$ at the output of the detector, but will be used, however, as a reference limit value for the bench-marking of the detectors' IMD performance and the envelope feedback AM-AM distortion reduction capability. Accordingly, assuming hypothetical AM-AM inter-modulation products of equal amplitudes at the frequencies $(\omega_c - 2\omega_x)$ and $(\omega_c + 2\omega_x)$ (i.e. tones associated with N in Fig. 2.7.3), and that would be at the level

of the estimated AM-PM product (i.e. -25.4 dBmV), such AM-AM components would translate into an error signal of amplitude -37.5 dBmV at $2\omega_x$, due to the $2H$ scaling factor in eq. (2.7.24). This bench-marking reference value is also shown in Fig. 3.4.6.

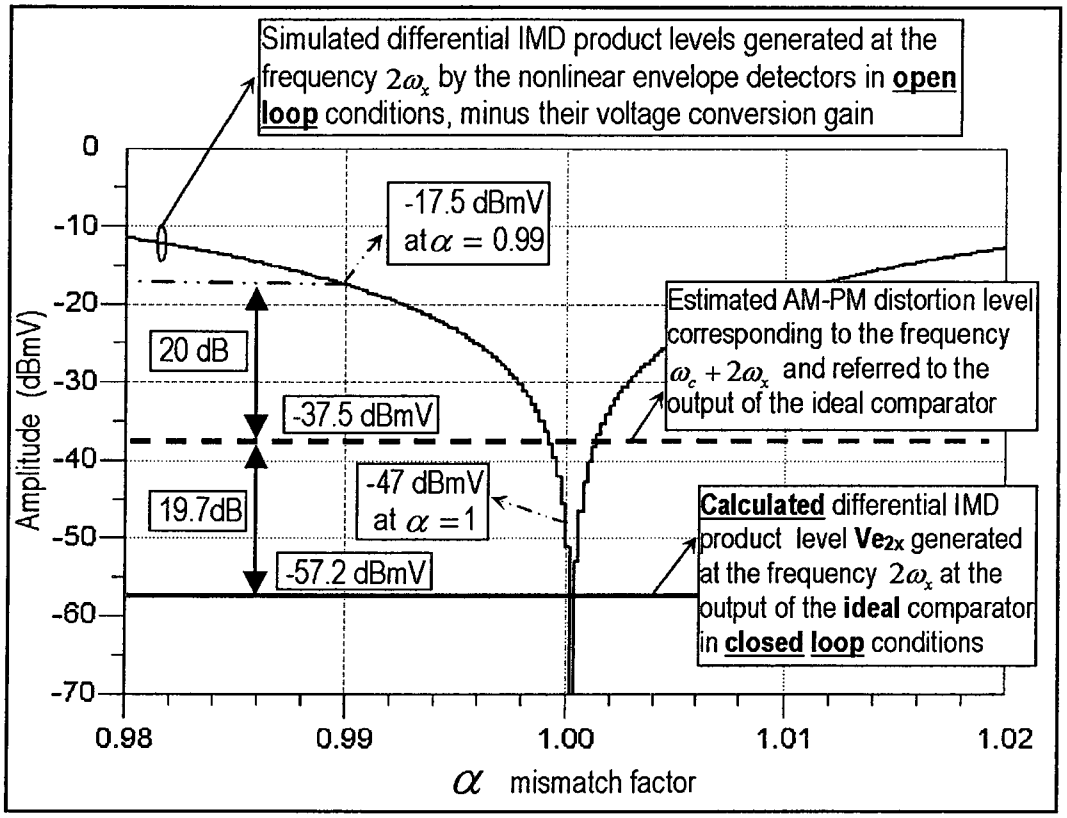

Figure 3.4.6: Simulated amplitude of the $2\omega_x$ frequency component in the differential signal generated by the envelope detectors in open loop conditions, referred to the output of the ideal comparator of Fig. 2.7.3 (i.e. reduced by the 7.84dB detector conversion gain), and function of a mismatch factor α to emulate a resistor value mismatch between the two detector circuits. A perfect match corresponds to α = 1. No $\omega_c + 2\omega_x$ or $\omega_c - 2\omega_x$ frequency component is applied at the detector inputs.

A first observation that can be made from Fig. 3.4.6 is that the general trend expected from the design guidelines of section 2.6.5 can be seen from these results. As the hardware mismatch between the two detectors increases (i.e. for α values that are lower or higher than the theoretically perfect match condition of α=1) the nonlinearity of the detectors have an increased effect, and consequently the added inter-modulation at $2\omega_x$ increases.

However, the ***actual*** optimum linearity condition simulated is seen to be at an α value slightly higher than 1. This can be explained by the fact that a slight mismatch between the detectors may introduce the equivalent of a distortion cancellation effect at $2\omega_x$ in the differential signal at the output of the detectors. When the detectors are perfectly matched, the $2\omega_x$ inter-modulation mixing products at the output of the two detectors are different, since they originate from the identical nonlinear processing of two different input excitations (i.e. J, K on one side, and L, M multiplied by 0.124 on the other), and thus a certain amplitude of the $2\omega_x$ component will result from their differential combination. In contrast, slightly different nonlinear processing of these same two separate excitation signals may result, in some particular condition, in $2\omega_x$ inter-modulation mixing products that approach each other, and consequently producing a differential quantity that tends to vanish. As will be seen in another analysis case in a later section, as the loop gain decreases, this distortion cancellation effect may occur at α values that are significantly different than the ideal case α=1.

Neglecting the possible benefits from the distortion cancellation effects, this linearity analysis allows deducing that even when the detectors are perfectly matched (i.e. with α = 1) in conformity with the design guidelines discussed in section 2.6.5, the nonlinearity they introduce in the vicinity of the -12dBm average input power threshold (where the compensation mechanism is activated) significantly impacts the AM-AM linearity

performances of the amplifier system, since the level of the $2\omega_x$ mixing product that they generate, when referred to the output of the ideal comparator (i.e. -47dBmV), is at a significantly higher level than the calculated $2\omega_x$ error signal level (-57.2dBmV).

It is worthwhile noting however, as far as the AM-AM only distortion is concerned, that since the average input power level considered in this analysis (-12dBm) lies well within the effective feedback operation range (Fig. 2.6.1) where the open loop gain is maximized, this calculated -57.2dBmV ideal case value for the $2\omega_x$ differential error signal corresponds to $\omega_c + 2\omega_x$ and $\omega_c - 2\omega_x$ output mixing products (N in Table 3.4.2) that are as low as -99.9dBc relative to the level of the center frequency component (L in Table 3.4.2). Therefore, this is a bench-marking against the lowest $\omega_c + 2\omega_x$ and $\omega_c - 2\omega_x$ output AM-AM mixing products level that could theoretically be achieved (assuming no distortion added in the error signal path) with the small signal feedback parameters used in Table 3.4.1, which correspond to the optimum feedback operation condition. Whereas the ***actual*** design specification value that needs to be met for the $2\omega_x$ differential error signal at the output of the detectors in a practical implementation would have to be the value that corresponds to the maximum ***allowable*** $\omega_c + 2\omega_x$ and $\omega_c - 2\omega_x$ output AM-AM mixing products level at the output of the amplifier system. This may imply a significant relaxation of the performance specification with respect to the -57.2dBmV bench-marking value. Hence, while it can be deduced from Fig. 3.4.6 that the detectors' nonlinearity under the excitation conditions specified above has a significant impact on the amplifier system's overall multi-tone linearity performance, it does not invalidate the design. In fact, the simulated ACPR performance shown in Fig. 3.4.2 with an input average power of -7dBm tends to validate this detector design as suitable for meeting linearity performances with a CDMA2000 excitation.

Design trade-offs based on the solutions to the design equations

The curves shown in Fig. 3.4.6, and which were derived starting from solutions to the system of equations (2.7.23), are very useful in a design cycle, as they provide reference values in making design trade-offs at the system level design for the specific input excitation considered. The analysis below is intended as an example of how this could be carried out, although these design trade-offs were not practically implemented in the PA design that was evaluated in the course of this work.

First, since the estimated AM-PM distortion level referred to the output of the ideal comparator (-37.5dBmV) as a bench-marking reference value corresponds to the largely dominant output distortion level, it may be deduced that the small signal envelope feedback parameters could be traded-off to the extent where the closed loop Ve_{2x} AM-AM distortion that originates from the RF amplifier chain would increase and reach just below this -37.5dBmV bench-mark level with a given margin, which means a possible relaxation of the open loop envelope feedback gain requirement that would yield a Ve_{2x} increase of 19.7dB (see Fig. 3.4.6) minus the design margin. This rationale applies only in regard to the AM-AM distortion performance at $\omega_c \pm 2\omega_x$, (not in regard to the feedback precision performance at ω_c and $\omega_c \pm \omega_x$) and is bound to the excitation being considered in this analysis. Nevertheless, it indicates trends and provides estimations that would translate into some amount of gain reduction in the error signal path as the average input power level is reduced to -12dBm, which is very desirable for minimizing the amount of noise injected in the RF amplifier chain through its gain control.

While the AM-AM performance trade-off range in this case (i.e. 19.7dB) appears to be large, it is however heavily dependant on the peak-to-average ratio considered in the analysis. Therefore, in general, the targeted Ve_{2x} AM-AM distortion level should account for the fact that the

excitation used in this type of analysis is a three-tone signal with a peak-to-average ratio that is limited to a specific value (e.g. 2dB in this case), besides the uncertainty from the weak nonlinearity in the gain control element.

Second, the curves in Fig. 3.4.6 allow estimating the possible range of improvement for the linearity of the detectors, which would contribute directly to an improvement in the output AM-AM distortion. For the purpose of clarifying this design optimization possibility, it will be assumed first that the small signal envelope feedback parameters have been traded-off to the extent where the closed loop Ve_{2x} AM-AM distortion level has increased from -57.2dBmV to the -37.5dBmV AM-PM related bench-mark value referred to above. No design margin with respect to the AM-PM related value is included in this case, since the corresponding output AM-PM distortion level at $\omega_c \pm 2\omega_x$ which was calculated above was found to be as low as -80.2dBc relative to the output carrier signal at ω_c, and thus it is assumed that despite the low peak-to-average value considered in this analysis (i.e. 2dB), an output AM-AM IMD performance that would be close to -80.2dBc would be a sufficient linearity performance requirement.

It will be assumed also, as an approximation, that the simulated $2\omega_x$ IMD curve shown in Fig. 3.4.6 remains practically unchanged despite this trade-off in the small signal parameters. Note, however, that this simulated $2\omega_x$ IMD curve is in fact dependent on the small signal feedback parameters, since the differential $2\omega_x$ IMD level at the output of the detectors depends on the two sets of multi-tone excitation at their inputs, which implies that the detectors' $2\omega_x$ IMD performance would normally have to be simulated for every set of feedback loop parameters considered.

Given the above assumptions, and considering the case where the detectors are perfectly matched (i.e. with $\alpha = 1$), their nonlinearities would have no impact on the overall output $\omega_c + 2\omega_x$ and $\omega_c - 2\omega_x$ AM-AM mixing products level, since the distortion level they generate (-47dBmV as shown in Fig. 3.4.6) would be 9.5dB below the Ve_{2x} bench-marking value of -37.5dBmV. However, a more sound design approach would be to take into consideration the effects of hardware mismatch between the detectors. Considering, for example, a mismatch that would be equivalent to $\alpha = 0.99$ as shown in Fig. 3.4.6, the detectors' linearity performance would have to be improved by 20dB.

An insight into the uncertainty due to the dependency of P on V_i

Though the exact distortion contribution that stems from the dependency of the gain control parameter P on the variations of the input envelope amplitude V_{ie} in the gain control model of Fig. 2.7.3 relates to a complex inter-modulation process, it is insightful in the analysis to visualize this dependency of P on V_{ie} as a modulation of the feedback loop gain. The gain control parameter P does not vary in the same proportion as an increase or decrease of V_{ieo} in eq. (3.4.5), since m and G_{Vp0} are also dependent on V_{ieo}. However, to gain an insight into the uncertainty due to the variations in V_{ie}, the IMD bench-marking levels may be estimated with P values that reflect a proportionality with respect to the two extreme values of the input envelope amplitude. Simulation shows that for a weakly nonlinear amplifier response as represented in Fig. 3.4.3, such an estimate is conservative.

This may be carried out by solving the system of equations (2.7.23), after substituting P in Table 3.4.1 by values that reflect the proportionality associated with the maximum excursions in V_{ie} with respect to its average

value, that is by setting $P=\left(0.045\cdot\frac{51mV}{68mV}\right)$ and $P=\left(0.045\cdot\frac{85mV}{68mV}\right)$. The corresponding Ve_{2x} bench-marking values obtained from eq. (2.7.23) and (2.7.24) are then found to be -54.8dBmV and -59.2dBmV, respectively. Comparing these values with the -57.2dBmV value from Table 3.4.2 gives an indication (considering the variations of +2.4dB or -2dB) that the uncertainty introduced by the approximation made in the modelling of the gain control element (with eq. (3.4.6)) does not significantly impair the 20dB design criterion derived above for the detectors linearity improvement.

Conclusion from the analysis

Under the memoryless assumptions made in section 2.7.3, and function of the approximations made in the behavioural model of Fig. 2.7.3, the use of the design equations has allowed determining that the detectors' nonlinearities have a significant impact on the amplifier system's overall multi-tone linearity performance in the vicinity of the -12dBm power threshold for the diode compensation mechanism. However, the actual output IMD levels are low enough that the effects due to the detectors' AM-AM nonlinearity at this power level do not invalidate the design in this gated envelope feedback implementation.

In order to meet an -80.2dBc output IMD level at $\omega_c+2\omega_x$ and $\omega_c-2\omega_x$ (which represents the performance limitation dictated by the AM-PM conversion through the RF amplifier chain only) under the condition of a three-tone input excitation with J = 68mV and K = 8.5mV, the small signal feedback loop parameters may be relaxed (in terms of loop gain reduction) to the extent where the AM-AM IMD level at the frequency $2\omega_x$ at the output of the comparator in the behavioural model is increased from -57.2dBmV to -37.5dBmV.

The multi-tone amplitude solutions obtained from the design equations have also been used to determine the excitation levels in a simulation

performed on the detector circuitry alone, and under a condition where the excitation level is in the vicinity of the power threshold for the self-triggering of the diode compensation mechanism. This has allowed determining (with some approximation) that the linearity improvement that would be required in the detector circuitry in order to meet the -80.2dBc output AM-AM IMD performance (assuming a detector hardware mismatch corresponding to α=0.99), can be quantified by a reduction of the detector's IMD product at $2\omega_x$ by 20dB under these same input excitation conditions.

Such architecture level design metrics, which are derived from the proposed design equations, can be used to optimize the circuit blocks in the error signal path separately from the rest of the gated envelope feedback system.

3.4.4 Gating design example using the design equations: distortion analysis of dynamic hardware reconfiguration - with no hysteresis function - within the soft crossover range

In this application example, the design equations are used to evaluate the feasibility of performing ***dynamic hardware reconfiguration*** (i.e. switching on and off RF transistors without the use of any hysteresis function) within the soft crossover range, where the envelope feedback loop gain is drastically reduced, for power efficiency improvement purposes. With this approach, the hardware reconfiguration mechanism is allowed to be activated ***continuously*** in a dynamic fashion and dependent on the varying ***instantaneous*** input envelope amplitude.

This contrasts heavily with the hardware reconfiguration scheme that was practically implemented in this work, where the hardware reconfiguration mechanism is allowed to be activated in the upper region of the effective feedback operation range (where the feedback loop is optimized for maximum gain), only as a function of the average power level and

conditioned by hysteresis windows, as depicted in Fig. 2.6.1 and described in section 2.6.4.

The potential benefit from dynamic hardware reconfiguration (with no hysteresis functions) is the elimination of the hysteresis comparators and their replacement by simpler activation circuits, which should translate into significant die size reduction and current reduction. However, the linearity performance with this type of reconfiguration may potentially be worse.

The goal of the analysis is to determine what degradation in the linearity performance may be attributed to the dynamic hardware reconfiguration within the soft crossover range, the requirements on the loop gain to meet a specific output AM-AM related IMD performance, and the requirements on linearity performances from the detectors for compliance with the desired output IMD performance. Hence, the possibility for architecture level design optimization based on the proposed design equations is demonstrated through this analysis.

Hardware reconfiguration scheme

Fig. 3.4.7 illustrates an example of the RF amplifier chain's gain shaping versus input signal amplitude that may result from this type of hardware reconfiguration. The top solid curve represents the band-limited gain of the RF amplifier chain for an input signal amplitude ranging from 0mV to 30mV, in the case where no additional hardware reconfiguration is performed besides the existing hardware state associated with ISSW and PSSW at logic high as shown in Fig. 3.2.12. Hence, the top solid curve corresponds to the lower portion of the same gain curve shown in Fig. 3.4.3.

The bottom solid curve represents the gain variation resulting from the dynamic hardware reconfiguration scheme investigated in this analysis, and which implies the deactivation of sections of the RF transistor arrays

in the power stage or in the intermediate stage as a function of the instantaneous input envelope signal, and performed gradually over a first 4dB input signal amplitude range (i.e. from ~24mV down to ~15mV) and a second 4dB range (i.e. from ~15mV down to ~9mV). The gain deviation envisaged with this scheme would result in a 0.25dB gain reduction, which suggests the possibility for switching off a significant portion of the RF transistor periphery.

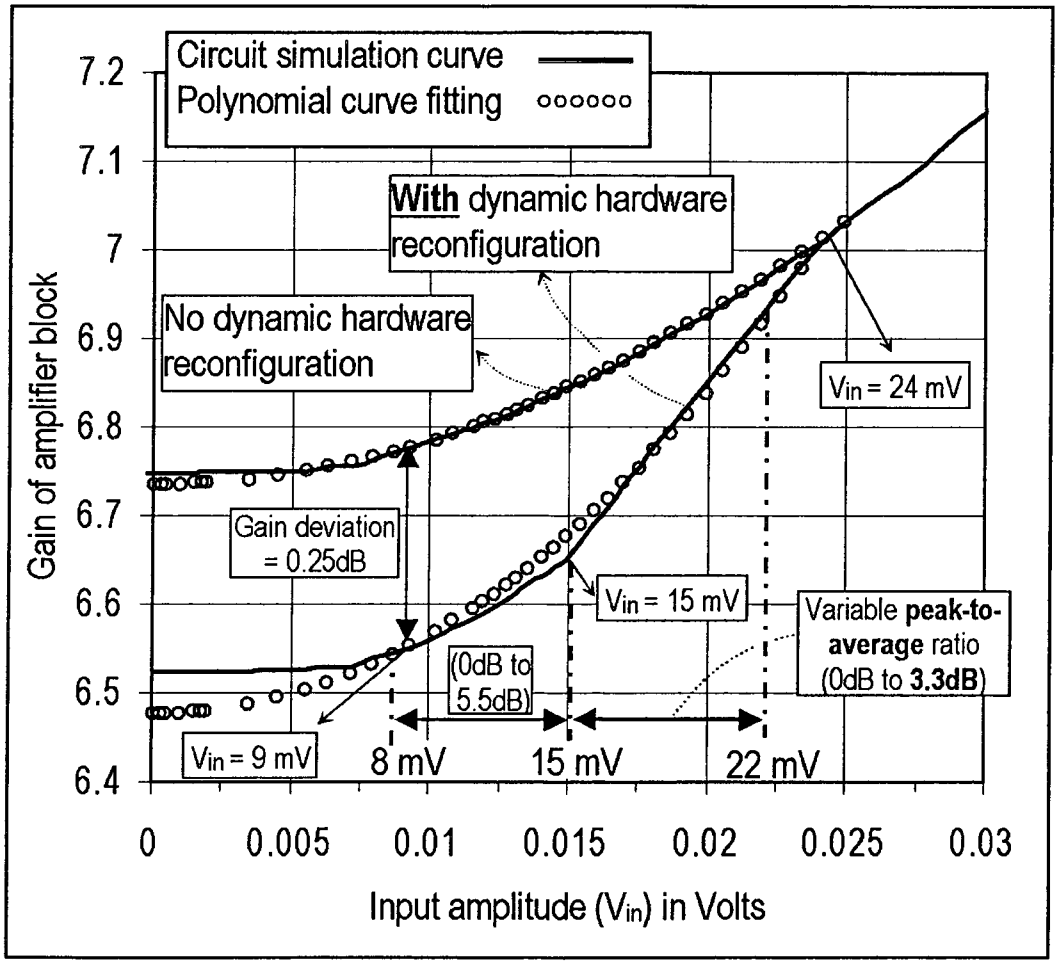

Figure 3.4.7: Band-limited gain profile associated with the proposed dynamic hardware reconfiguration scheme (bottom solid curve) within the soft crossover range, and with no hysteresis function.

Using MATLAB(TM), a fifth degree power series was extracted to describe with sufficient accuracy the memoryless input to output voltage relationship associated with both curves, that is with a first set of scalar polynomial coefficients a_1 = 6.7345, a_3' =(3/4)a_3 = 493.23, and a_5' = (5/8)a_5 = -23020 associated to the band-limited gain profile with no hardware reconfiguration, and a second set of scalar polynomial coefficients $a_1 = 6.4759$, a_3' =(3/4)a_3 = 874.63, and $a_5' = (5/8) \cdot a_5 = 90456$ associated with the band-limited gain profile with hardware reconfiguration.

Coordinates that are solutions to the polynomial curve fittings for these two cases are plotted on Fig. 3.4.7. The two sets of polynomial coefficients (a_1, a_3, and a_5) that relate to the $V_{ae}(t)$ to $V_{out}(t)$ relationship in eq. (2.7.9) for both cases are reported in Table 3.4.5.

The distortion analysis will be performed with a variable peak-to-average ratio of the input envelope signal, ranging from 0dB to 3.3dB, i.e with an input amplitude J equal to 15mV for the carrier signal at ω_c, and a modulating signal of amplitude K varying from zero to 3.5mV. This also translates into an average-to-minimum ratio of 5.5dB.

Small signal envelope feedback parameters

The small signal envelope feedback loop parameters of the design described in sections 3.2 and 3.3 are again used in this analysis, and have been determined through simulation in the same way as described in the previous analysis, but this time with the 1.88GHz input signal having an amplitude of 15mV (V_i in Fig. 2.7.3). This corresponds to an input power of -25dBm (PA_IN in Fig. 3.2.9), and the low sensitivity of the detectors at this power level (see Fig. 3.3.3) indicates an operation in the lower region of the soft crossover range.

The overall loop gain at this power level drops to ~10 (from ~42 in the previous distortion analysis case with -12dBm of input power). The envelope amplitude to detected voltage conversion gain (i.e. f_D in Fig.

2.7.3) is equal to 1.529 (i.e. 3.69dB). The comparator and analog error amplifier voltage gains (C and A_v in Fig. 2.7.3) are equal to 6.187 and 64.12, respectively. Hence, the low frequency gain product E (i.e. $(f_D C A_v)$) used in the definition of eq. (2.7.17) to (2.7.21) is ~607. As in the previous analysis case, the reverse path attenuation (H in Fig. 2.7.3) is 0.124, and the forward gain (F in Fig. 2.7.3) may be set to 1.

RF simulation performed on the amplifier block alone with a continuous wave input excitation at 1.88GHz, a constant input power of -25dBm, and with small variations of the gain control voltage (V_p in Fig. 2.7.3), allows determining (with the use of equation (3.4.6)) a gain control parameter P equal to 0.0195. The above parameters are summarized in Table 3.4.5.

Table 3.4.5: Input variables to the system of equations (2.7.23) for determining the amplitudes L, M, N, Q, and R of the mixing products at the output of the amplifier system of Fig. 2.7.3, for the two cases of Fig. 3.4.7, i.e. case (i): with no dynamic hardware reconfiguration, and case (ii): with dynamic hardware reconfiguration.

	J(mV)	K(mV)	F	P	E	H	a_1	a_3	a_5
(i)	15	0 to 3.5	1	0.0195	607	0.124	6.7345	657.7	-36832
(ii)	15	0 to 3.5	1	0.0195	607	0.124	6.4759	1166	144730

Calculated AM-AM closed loop distortion, and simulated detector linearity performance in open loop

With the parameters from Table 3.4.5 for case (i) (no dynamic hardware reconfiguration) and case (ii) (with dynamic hardware reconfiguration) as

input variables, the amplitudes L, M, N, Q, and R of the multi-tone output signal depicted in the closed loop configuration of Fig. 2.7.3 have been calculated separately for both cases using the system of equations (2.7.23), and the corresponding multi-tone amplitudes Ve_0, Ve_x, Ve_{2x}, Ve_{3x}, and Ve_{4x} of the error signal at the output of the ideal comparator of Fig. 2.7.3 have been calculated using eq. (2.7.24). The solutions for the output mixing product level N (at $\omega_c + 2\omega_x$) in dBc relative to the carrier amplitude of L, as well as the amplitude of the corresponding error signal component Ve_{2x} (at $2\omega_x$) in dBmV as a function of a variable envelope peak-to-average voltage ratio in the input signal (i.e. function of the constant amplitude J and the variable amplitude K, following the relation $20 \cdot \log\left(\frac{J+2K}{J}\right)$) are shown in Fig. 3.4.8. The case with no hardware reconfiguration corresponds to the dashed curves, and the case with hardware reconfiguration corresponds to the solid curves.

Output AM-PM distortion level

As can be seen in Fig. 3.4.3, the phase variation through the RF amplifier chain for envelope variations ranging from 15mV to 25mV is very small (i.e. ~0.2 degrees), and using eq. (3.4.9) it may be deduced that the level of the associated output sidebands at $\omega_c + 2\omega_x$ and $\omega_c - 2\omega_x$ due to AM-PM conversion in both cases of Fig. 3.4.7 are low enough that they may be neglected in this analysis.

Comparison with the detectors' linearity performance

The differential error signal at the output of the detector circuitry as a separate circuit block in open loop has been simulated in the condition where the two detector branches are perfectly matched (i.e. $\alpha = 1$) and as a function of the peak-to-average value of the input signal, using the three-tone component values J and K from Table 3.4.5 as excitation

amplitudes for the input detector. The output multi-tone component values L and M that were calculated with the system of equations (2.7.23) for the case where dynamic hardware reconfiguration is assumed (i.e. case (ii) in Table 3.4.5) were used as excitation amplitudes for the output detector (the solutions for Q and R are much lower than M, and thus again were not used, though the proposed design equations and design methodology would allow extending the analysis to their inclusion in the simulation).

The simulated amplitude Ve_{2x} of the $2\omega_x$ inter-modulation product (for case (ii)) minus the detector's 3.69dB conversion gain is represented in Fig. 3.4.8 by the solid curve that is drawn over a narrower peak-to-average span.

The results shown in Fig. 3.4.8 also demonstrate how the use of the design equations may be very helpful in a design cycle at the architecture level for making performance trade-offs.

First, they allow estimating the AM-AM distortion levels that may be expected from the nonlinearity of the RF amplifier chain and the envelope feedback parameters when the amplifier system is operated in the lower region of the soft crossover range without any dynamic hardware reconfiguration, and as a function of the peak-to-average envelope voltage ratio. The level N at $\omega_c \pm 2\omega_x$ reaches -71.5dBc with a peak-to-average ratio of 3.3dB.

Second, they allow determining the degradation that may be expected in the AM-AM linearity performance when the dynamic hardware reconfiguration scheme represented in Fig. 3.4.7 is considered, assuming no distortion is added in the error signal path. As shown in Fig. 3.4.8, for a peak-to-average ratio of 3.3dB, this linearity degradation translates into a 5.8dB increase in the IMD product level at the frequencies $\omega_c + 2\omega_x$ and $\omega_c - 2\omega_x$, thus reaching -65.7dBc relative to the carrier signal at ω_c. The

corresponding IMD product level at $2\omega_x$ in the error signal path is calculated using eq. (2.7.24) and found to be at -36.2dBmV.

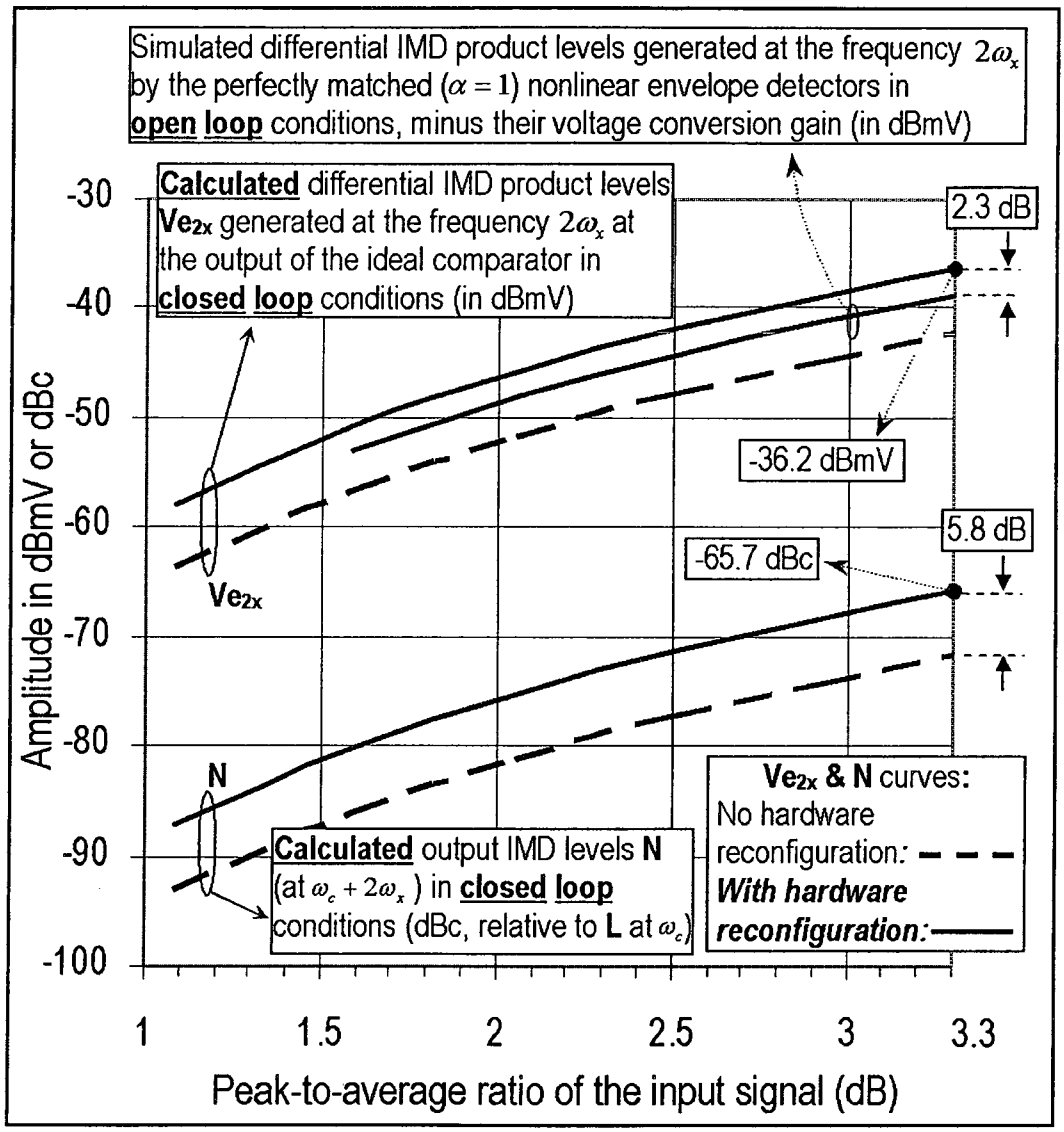

Figure 3.4.8: Calculated solutions for the amplitude of the output mixing product N and the amplitude Ve_{2x} in the error signal for the two cases of Table. 3.4.5, function of the peak-to-average envelope voltage ratio of the input signal.

Third, it may be deduced from these curves that with the excitation signal considered, the distortion characteristics of the detector circuitry in perfectly matched conditions (i.e. assuming α =1) would have no significant impact on the overall linearity performance of the amplifier system, since the IMD product added at $2\omega_x$ by the detectors would be at ~ 2.3dB lower than the calculated bench-marking values (and precisely 2.3dB lower than -36.2dBmV in the 3.3dB peak-to-average condition), when referred to the output of the ideal comparator (Fig. 2.7.3).

The solutions for case (ii) in Table 3.4.5 (including dynamic reconfiguration) with a 3.3dB peak-to-average envelope voltage ratio in the input signal are summarized in Table 3.4.6. Note that the $V_{eo} \cdot E$ d.c. offset (i.e. 0.207mV times 607 = 126mV) on the gain control signal V_p (Fig. 2.7.3) is considered small enough for the purpose of this analysis.

Table 3.4.6: Solutions to the system of equations (2.7.23) with the parameters of case (ii) in Table 3.4.5 (with dynamic hardware reconfiguration) as input variables, and for an envelope peak-to-average voltage ratio of 3.3dB (i.e. J = 15mV, $K = 3.5$mV).

V_{out} Tones	**L**	**M**	**N**	**Q**	**R**
Amplitude (mV)	119.3	28	62.2e-3	2.4e-3	-326e-6
Amplitude (dBmV)	41.5	29	-24.1	-52.4	-69.7
(dBc) relative to L	0	-12.6	**-65.7**	-93.9	-111.3
V_e Tones	**Ve_0**	**Ve_x**	**Ve_{2x}**	**Ve_{3x}**	**Ve_{4x}**
Amplitude (mV)	0.207	0.052	-15.4e-3	-595e-6	81e-6
Amplitude (dBmV)	-13.7	-25.7	**-36.2**	-64.5	-81.9
(dBc) relative to Ve_0	0	-12	-22.5	-50.8	-68.2

IMD performance optimization and design requirements for the detectors' linearity performance and the analog amplifier gain

The design equations will now be used to optimize the system parameters in the case where dynamic hardware reconfiguration is performed, as a function of some desired output IMD performance, and accordingly to determine the design requirements for the detectors and the analog amplifier.

The analog error amplifier gain was initially optimized for gain regulation upon hardware reconfiguration within the effective feedback operation range (section 3.3.3), which translated into a gain E of 935 in the error signal path within the effective feedback operation range (Table 3.4.1), and a gain E equal to 607 in the soft crossover range (Table 3.4.5).

However, further decreasing the gain in the error signal path would reduce the amount of noise applied to the gain control input of the RF amplifier chain (CTRL in Fig 2.6.2), and thus would reduce the noise level at the output of the PA at low power levels. Accordingly, it will be assumed that the analog amplifier gain (A_v) needs to be reduced in an adaptive fashion, but only within the input power range where the dynamic hardware reconfiguration is activated, and to the extent where the input excitation levels J =15mV and K =3.5mV (which corresponds to the envelope voltage peak-to-average ratio of 3.3dB in Fig. 3.4.8) yields an output IMD level N at the frequencies $\omega_c \pm 2\omega_x$ that is increased from -65.7dBc to some maximum level, as per the design goals.

Approximate IMD design goal

A three-tone IMD performance expressed in voltage ratios, and which is also function of the limited envelope peak-to-average voltage ratio of an AM signal, may not be directly computed from the ACPR performance metric of a digitally modulated signal such as CDMA. The ACPR metric is defined in terms of power density ratios and is generally function of a high peak-to-average power ratio (e.g. 5.4dB peak-to-average power ratio in

the case of CDMA2000_1x, based on a 99% amplitude cumulative density function [5]). Alternatively, analytical approaches similar to what is proposed in [9], [10] could be used to estimate a multi-tone IMD design goal as a function of ACPR design objectives. Also, experimental characterization may be performed to correlate the ACPR performance of a nonlinear system with its corresponding multi-tone IMD performance when operated at the same average output power level.

For the purpose of setting a design goal that serves as a numerical example in this analysis, a simulated three-tone IMD performance goal that reflects an acceptable degree of linearity performance with a conservative design margin will be used. Simulation performed on the RF amplifier chain alone (i.e. without feedback and without dynamic hardware reconfiguration) with a 3.3dB peak-to-average envelope voltage ratio in the three-tone input excitation (J = 15mV, K = 3.5mV) shows $\omega_c \pm 2\omega_x$ AM-AM IMD levels of -55dBc relative to the carrier signal at the output. The 10.7dB difference between this figure and the calculated -65.7dBc IMD level reported in Table 3.4.6 for case (ii) (i.e. with dynamic hardware reconfiguration) points to the linearization capability of the envelope feedback system within the soft crossover range when provided with a gain of 607 in the error signal path, and demonstrates that this linearization capability largely overcomes the linearity degradation induced through the dynamic reconfiguration. However, simulation performed on the RF amplifier chain alone in the same conditions but with a CDMA2000_1x input excitation also demonstrates that the ACPR performance complies with standard requirements with ample design margin. Therefore, on the basis of this AM-AM IMD and ACPR comparison, the -55dBc IMD performance will be used in this analysis as a figure of merit that would be indicative of an acceptable degree of linearity in the presence of dynamic hardware reconfiguration as well, thus justifying a 10.7dB IMD linearity performance relaxation as a trade-off to

allow a gain reduction in the error signal path, at power levels that correspond to the soft crossover range.

Solving for the minimum value of A_v

The N = -55dBc design goal is a quantity that is relative to the amplitude L. Due to the nonlinear behaviour of the system, L and N do not vary in the same proportion when the loop gain is changed, and the adjustment required in the analog amplifier gain A_v is not a linear function of the above mentioned 10.7dB increase in N. One way of converging toward the exact required analog amplifier gain A_v with the minimum of transformation in the design equations (2.7.23) is to obtain, in a **first step**, a very close estimate of L and an approximate value A_v by assuming a linear adjustment of N (i.e. using the estimated value N as an input variable, besides the input variables J and K) and obtaining L and A_v as solutions, and in a **second step** to solve for the exact value of A_v, this time by using, as input variables, the accurate amplitude N of the output IMD design goal as well as J and K.

In the **first step**, it may be deduced from Table 3.4.6 that a linear increase of N by 10.7dB would result in an amplitude N = 213 μV (i.e. 3.428 x 62.2 μV). A hypothetical linear adjustment on A_v would result in a proportional decrease of the small signal gain E (i.e. $(f_D C A_v)$) in the error signal path by 10.7dB. Using the same input variables shown in case (ii) of Table 3.4.5 (with K set to 3.5mV), but with E set as an unknown variable and with N set as a known input variable equal to the estimated value 213 μV, then the system of equations (2.7.23) may be solved, and the solutions of L and E determined as 114.9mV and 126, respectively. As expected, this adjustment on the gain (i.e. from 607 in Table 3.4.5,

down to 126) corresponds to a decrease (~ -13.7dB) that differs from the 10.7dB mentioned above, because of the nonlinearities involved.

In the **second step**, the exact value of A_v is determined by solving for E with the system of equations (2.7.23), using the same input variables as in the first step, but this time with L=114.9mV added as a known input, and also this time with the input variable N set to the exact desired design goal of -55dBc relative to 114.9mV, which is equal to 204 μV. The solution for E is found to be 134.5, that is a decrease (from 607 in Table 3.4.5) by a factor of 4.514. This allows determining the minimum requirement for the analog amplifier gain A_v (E being proportional to A_v), that is the original value A_v = 64.12 divided by 4.514, which yields A_v = 14.2.

This two step approach for solving eq. (2.7.23) while using an output inter-modulation distortion level set as an input variable to the system of equations increasingly facilitates the application of eq. (2.7.23) and becomes increasingly helpful in avoiding convergence problems with MATLAB (TM) as the nonlinearity of the system becomes more important, or when solving eq. (2.7.23) with one (or more than one) higher order output IMD level design goal as part of the input variables.

Solving for the IMD performance with the optimized analog amplifier gain

With A_v now set to 14.2 (i.e. E = 134.5) and all other input parameters set as in case (ii) of Table 3.4.5 (i.e. for the dynamic hardware reconfiguration scheme represented by Fig. 3.4.7), the system of equations (2.7.23) was used to calculate the amplitudes L, M, N, Q, and R of the multi-tone output frequency spectrum depicted in the equivalent closed loop configuration of Fig. 2.7.3 as a function of the peak-to-average ratio.

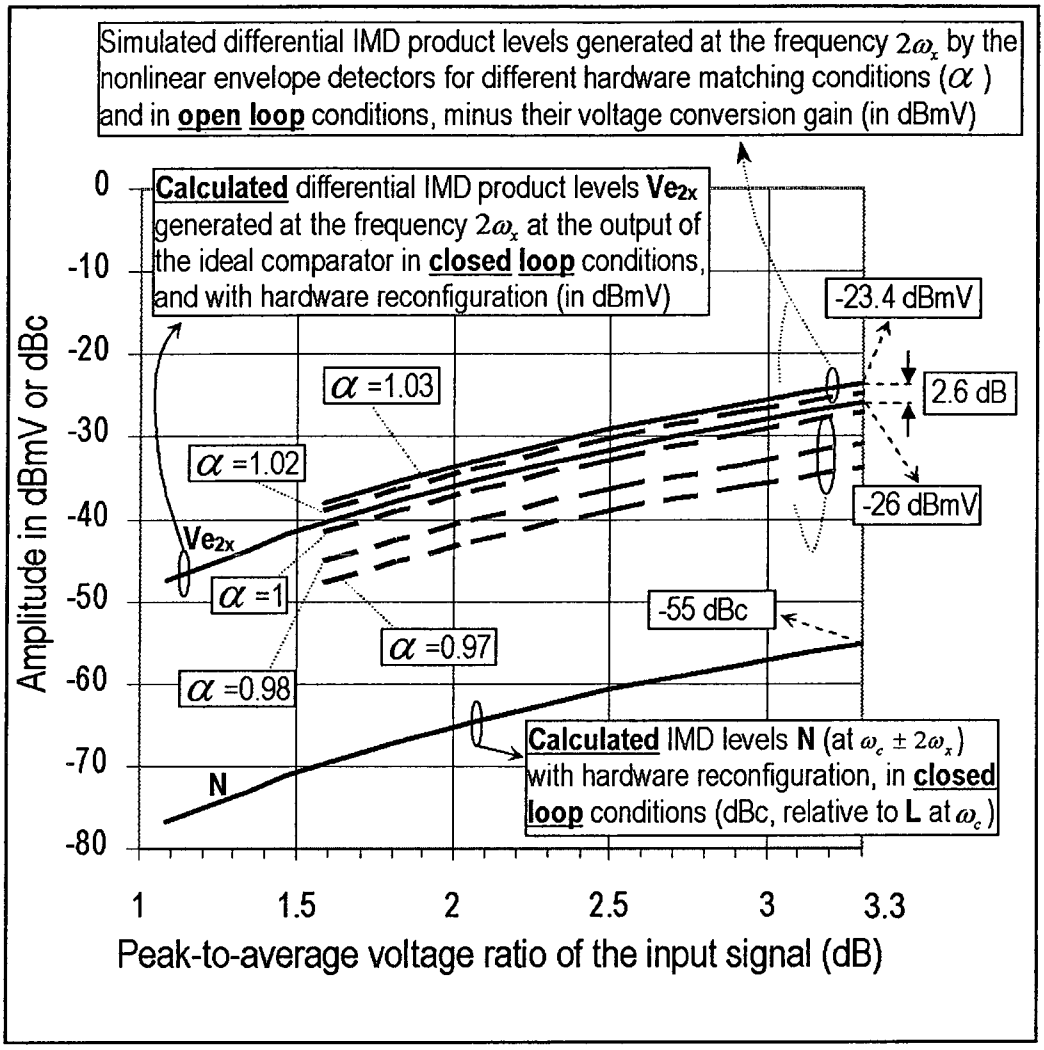

Figure 3.4.9: Solutions for the closed loop output mixing product level N at the frequency $\omega_c \pm 2\omega_x$ and the amplitude of the corresponding error signal component Ve_{2x} at the frequency $2\omega_x$ after optimization of the analog amplifier's gain A_v. The open loop detectors' IMD performance at $2\omega_x$ for different hardware matching conditions (α values) is also shown.

The corresponding multi-tone amplitudes Ve_0, Ve_x, Ve_{2x}, Ve_{3x}, and Ve_{4x} of the error signal at the output of the ideal comparator of Fig. 2.7.3 have been calculated using eq. (2.7.24). The solutions for the output mixing

product level N (at the frequency $\omega_c \pm 2\omega_x$) in dBc relative to the carrier amplitude of L, as well as the amplitude of the corresponding error signal component Ve_{2x} (at the frequency $2\omega_x$) in dBmV as a function of a variable peak-to-average envelope voltage ratio in the input signal are shown in Fig. 3.4.9.

It can be seen that the desired output performance N = -55dBc for a peak-to-average ratio of 3.3dB is met, and the corresponding error signal component Ve_{2x} is at -26dBmV.

Linearity performance requirements for the envelope detectors

Each set of solutions obtained from the system of equations (2.7.23) for every peak-to-average ratio considered in Fig. 3.4.9 was used to define the input excitation signals in the simulation of the open loop Ve_{2x} IMD product level generated by the envelope detectors at the frequency $2\omega_x$. The simulation was run for different values of the hardware mismatch factor α, and the results (scaled down by the detectors' 3.69dB conversion gain) are also reported in Fig. 3.4.9 to allow a direct comparison with the previously calculated closed loop Ve_{2x} performance, and which is function only of the nonlinearities due to the dynamic hardware reconfiguration and the envelope feedback parameters.

It may be deduced from these curves that in the case of a perfect hardware match between the detector branches (i.e. with $\alpha = 1$), the distortion level that would be added by the detectors in the error signal path at a peak-to-average ratio of 3.3dB is ~1dB lower than the calculated closed loop Ve_{2x} bench-mark performance value of -26dBmV, and thus would have limited impact on the output IMD performances. However, this added distortion increases to 2.6dB above the calculated Ve_{2x} bench-mark

value with $\alpha = 1.03$, which represents a condition where the detector's nonlinearities would impact the output IMD performances. Using $\alpha = 1.03$ as a design parameter is a reasonably conservative measure, since the hardware mismatch assumption made represents the very stringent scenario where all resistors in the collector circuitry of the input detector have their values scaled simultaneously by the factor α. A careful and symmetrical I.C. layout of the detector circuitry is likely to allow for hardware matching characteristics that do not exceed these boundaries in equivalent terms.

Furthermore, a sound design goal in this application example would be to set the requirements for the linearity of the detectors so as to improve their open loop Ve_{2x} IMD performance to a level that is ~6dB (used here as a design margin example) lower than the closed loop -26dBmV bench-mark value shown in Fig. 3.4.9. Accordingly, the IMD linearity performance of the detectors would have to be improved by ~ 8.6dB.

It may be seen also from Fig. 3.4.9 that the distortion cancellation effect that was discussed in section 3.4.3 (and also evident in Fig. 3.4.6) occur at α values that are significantly different from 1, that is for α lower than 0.97 in this case example. The explanation resides in the increased difference between the two sets of multi-tone excitation signals at the inputs of the two detector branches as the feedback loop gain is decreased, since the distortion in the feedback path (node V_f in Fig. 2.7.3) is then more important. This results in an increased asymmetry between the two multi-tone excitation patterns, which translates into the requirement for an increased asymmetry in the hardware of the detector branches in order to reach the condition for maximum distortion cancellation.

The uncertainty due to the approximation in the gain control function

Here also it is insightful to estimate the effects, on the IMD bench-marking values, that are due to the dependency of the gain control parameter P on the envelope amplitude V_{ie} of the input signal at the two extreme conditions. After substitution of P (from case (ii) in Table 3.4.5) by $\left(0.0195 \cdot \frac{8mV}{15mV}\right)$ and with E maintained at 134.5, solving the system of equations (2.7.23) and using eq. (2.7.24) yields an IMD product level Ve_{2x} = -22.9dBmV.

In the same way, substituting P by $\left(0.0195 \cdot \frac{22mV}{15mV}\right)$ yields Ve_{2x} = -28.2dBmV.

Comparing these values with Ve_{2x} for a 3.3dB peak-to-average ratio in Fig. 3.4.9 shows a variation of +3.1dB or -2.2dB with respect to the Ve_{2x} = -26dBmV level, which corresponds to the N = -55dBc design goal. These differences stem from conservative estimates that are associated with the extreme values of the envelope signal, and thus are indicative of a very moderate uncertainty when put into the context of the 8.6dB linearity improvement design goal derived above. Therefore, it may be deduced that this approach for distortion analysis and for deriving design goals may be relied upon despite the approximation in the modelling of the gain control element of Fig. 2.7.3.

Conclusion from the analysis

The above analysis allows concluding that with J =15mV and K =3.5mV in the excitation signal, the activation of the dynamic hardware reconfiguration within the soft crossover range introduces a 5.8dB increase in the output AM-AM IMD level at $\omega_c \pm 2\omega_x$, assuming the error signal path is distortion free.

With the same excitation signal, an output AM-AM IMD performance of -55dBc at $\omega_c \pm 2\omega_x$ can be achieved with a gain of 134.5 in the error signal path (which allows a relaxation in the analog amplifier gain A_v from 64.12 to a minimum of 14.2) and with the envelope detectors' linearity performance improved by 8.6dB to yield an IMD product Ve_{2x} = -32dBmV. These design adjustments may be performed through circuit simulation on the detector circuitry and the analog amplifier, and independently from the rest of the gated envelope feedback system.

3.4.5 Discussion on the use of the design equations

The two previous localized linearity analyses exemplify a design methodology where the architecture level optimization of circuit blocks in the error signal path in open loop conditions and separately from the rest of the envelope feedback architecture may be greatly facilitated by the use of a similar comparative study, based on the application of the proposed design equations. Similar localized analyses performed at different and carefully chosen power levels and peak-to-average envelope voltage ratios are likely to help significantly in the design cycle of a gated envelope feedback system at architecture level and during simulation.

The same methodology may be applied in an experimental environment, where the IMD analyses are carried out using exclusively experimental characterized data as input variables, and the IMD performance bench-marking carried out through direct measurements on the circuit blocks in the error signal path in open loop conditions. This would be totally independent of the circuit simulation environment, which is likely to help very significantly in the design convergence process.

Extension to analyses with higher degree polynomials

Extending the design equations to a higher degree polynomial representation of the nonlinearities of the RF amplifier chain (G in Fig.

2.7.3) would render the proposed design methodology even more valuable. This would not only enhance the precision of the numerical results, but would allow greater flexibility and application possibilities. As an example, with a 9^{th} degree polynomial representation of the RF amplifier chain in the same hardware state shown in Fig. 3.2.12 with ISSW and PSSW at logic high, the AM-AM distortion that would be introduced through additional hardware reconfiguration in a dynamic fashion (no hysteresis) and with the gain profile shown in Fig. 3.4.10 could be analyzed. The dotted curve corresponds to the case without additional dynamic hardware reconfiguration, and thus corresponds to the same gain characteristics as that shown in Fig. 3.4.3, but represented over a broader range of input signal amplitude. The solid curve shows the gain profile that may be associated with a dynamic hardware reconfiguration in the lower region of the effective feedback operation range (Fig. 2.6.1), i.e. the switching on and off of sections in the RF transistor arrays as a function of the instantaneous input envelope amplitude, at power levels where the envelope feedback parameters are non-optimal. The nonlinearity introduced with this scheme is likely to be more severe than in the case analyzed in section 3.4.4, since the 4dB activation range is shifted at higher voltage swing amplitudes (i.e. between 50mV and 80mV), and the gain deviation that is introduced is larger (i.e. 0.5dB instead of 0.25dB), which is also representative of the switching off of larger sections in the RF transistor arrays, thus allowing for greater efficiency improvement. The polynomial curve fitting shown in Fig. 3.4.10 indicates that a 9^{th} degree representation of the nonlinearities would be sufficient for an IMD analysis with a peak-to-average ratio higher than 3.3dB.

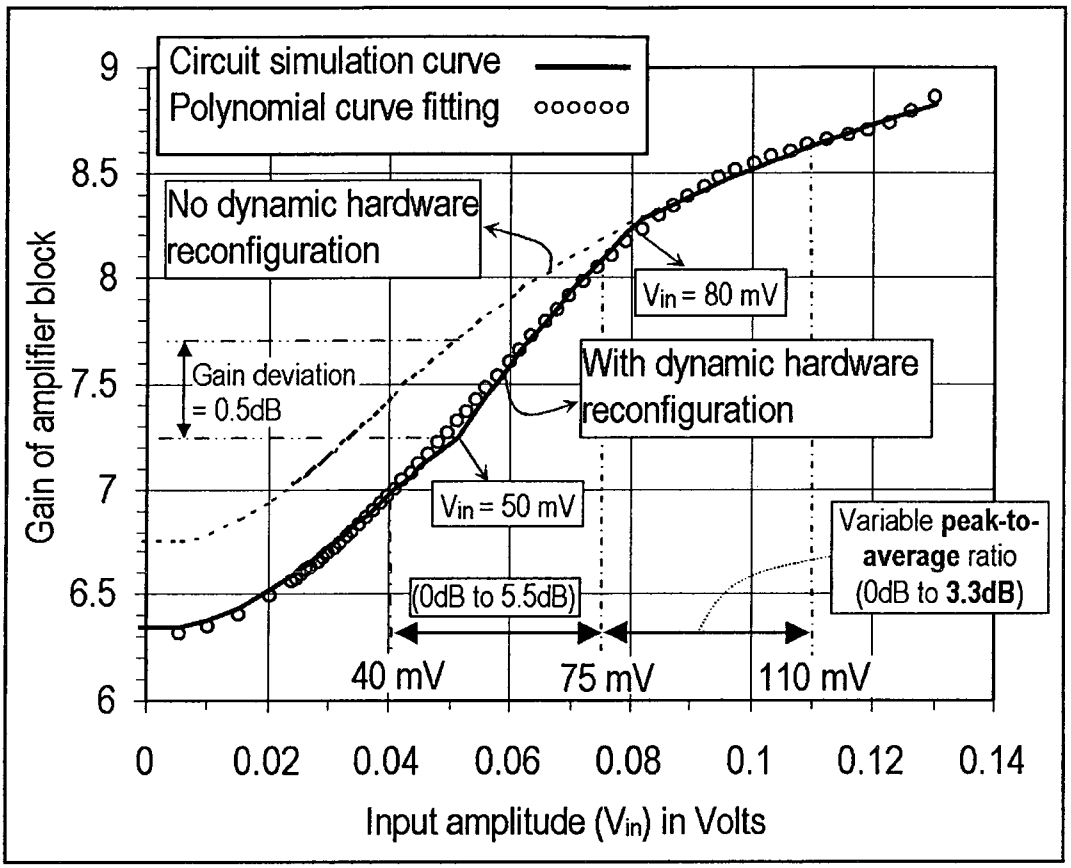

Figure 3.4.10: Example of a band-limited gain profile associated with a dynamic hardware reconfiguration scheme - without hysteresis - and that would require a 9th degree polynomial function representation.

Synthesis of the gain profile in a dynamic hardware reconfiguration, function of linearity performances

An example of increased flexibility brought by a higher degree polynomial representation is the possibility of using the system of equations (2.7.23) to solve simultaneously for the narrowest activation range, the maximum gain deviation, and the smallest loop gain that would allow meeting some given output inter-modulation distortion requirements. In this application, the solutions to the system of equations would be the coefficients of a polynomial function that defines the gain profile associated with the dynamic hardware reconfiguration. Some of the amplitudes L, M, N, Q,

and R of the multi-tone output signal would be input variables, as conditions on the output IMD performances. The complete system of equations to be solved would be the system of equations (2.7.23) augmented by a few gain requirements (using eq. (2.7.9)) that define the gain profile of the reconfiguration scheme, based on a similar representation to that shown in Fig. 3.4.10 (e.g. a range of values that limits the gain at V_{in} = 0mV; a range of values that limits the gain deviation at V_{in} = 50mV; the desired gain at the triggering point V_{in} = 80mV; and the gain associated with a few V_{in} values above 80mV).

Such an analysis based on the design equations would allow defining architecture level design requirements before defining the circuit topologies used for the gating function and reconfiguration mechanism, and would allow estimating the required performances of the circuit blocks in the envelope feedback loop prior to defining their circuit structures.

In an experimental environment, it would significantly facilitate the adjustment of the hardware gating function in open loop conditions, starting from small signal open loop parameters and the desired closed loop IMD performance.

Chapter 4

IC implementation and experimental results

In this chapter, the chip layout partitioning of the gated envelope feedback RFIC PA design in a dual GaAs HBT IC solution and their implementation on the test board is shown. The experimental results that are provided demonstrate the viability of the gated envelope feedback concept and the circuit techniques that are introduced in this work. The RF performances of the power amplifier system in terms of gain, gain regulation, ACPR, waveform quality, and transient characteristics, as well as current reduction upon automatic hardware reconfiguration are presented.

Section 4.1
IC Layout partitioning in GaAs HBT technology and implementation on the test board

4.1.1 GaAs HBT die for the 3-stage CDMA RF amplifier chain

Figure 4.1.1 is a photograph showing the partitioning of the GaAs HBT IC for the 1.88GHz CDMA three-stage amplifier chain represented in Fig. 3.2.1. Excluding the area used for the test signals and the redundant electrostatic discharge (ESD) protection and bond pads, the effective die area used is 1.07 mm^2.

4.1.2 GaAs HBT die for the gating, feedback and automatic reconfiguration control circuits

Figure 4.1.2 is a photograph showing the partitioning of the GaAs HBT IC for the gating, feedback and automatic reconfiguration control circuits represented in Fig. 3.3.1. Excluding the area used for the test signals and the redundant electrostatic discharge (ESD) protection and bond pads, the effective die area used is 0.328 mm^2.

4.1.3 Implementation on the printed circuit test board

Figure 4.1.3 shows a photograph of the two GaAs HBT dies directly wire bonded on the printed circuit test board, which provides facilities for various tests, including on-board full 2-port scattering (S) parameter calibration for the de-embedded measurements of RF parameters and the envelope feedback loop response.

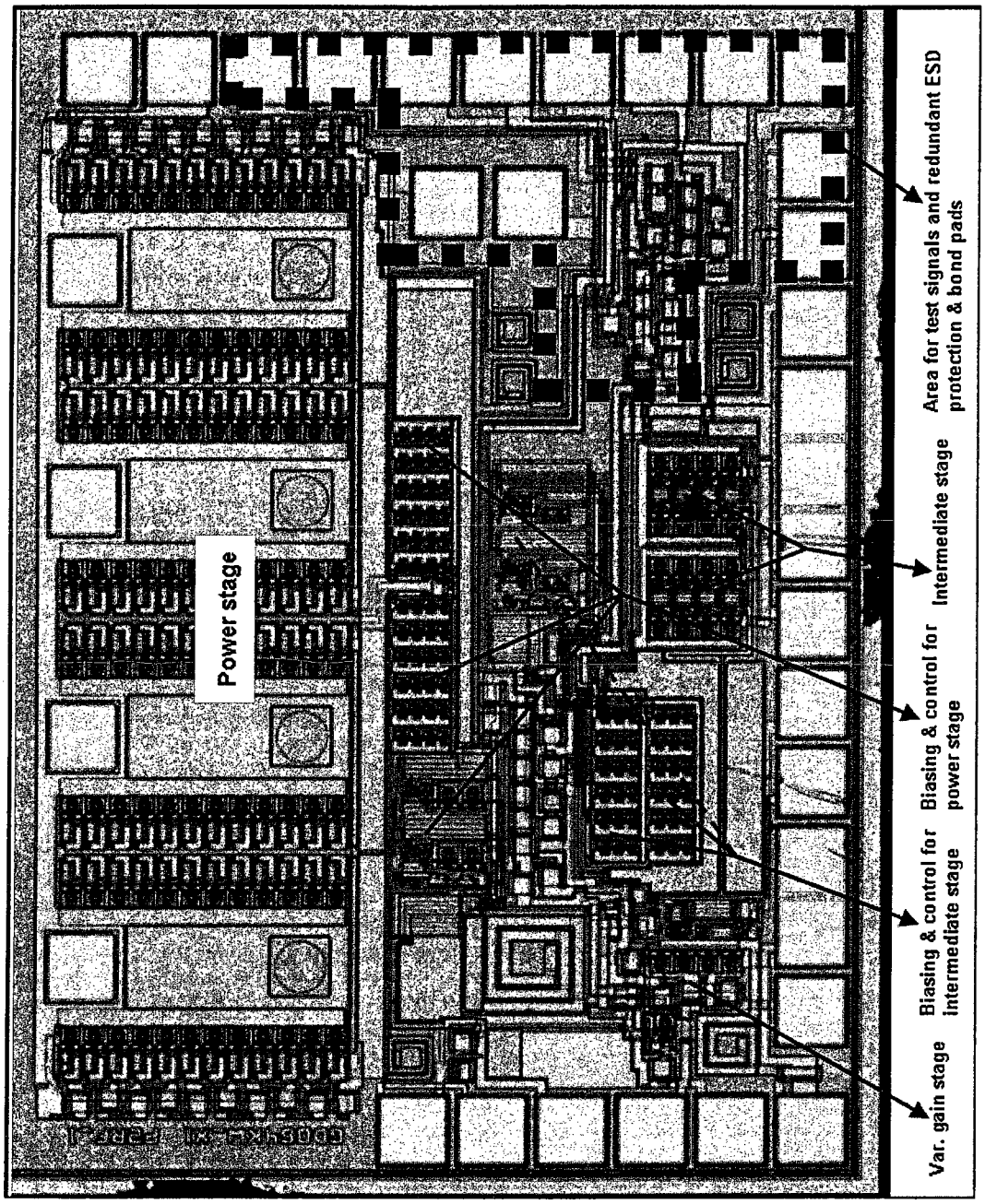

Figure 4.1.1: Photograph of the GaAs HBT chip for the 1.88 GHz CDMA three-stage RF amplifier chain represented in Fig. 3.2.1 (Skyworks Solutions' HBT4-P401 4th generation GaAs HBT process).

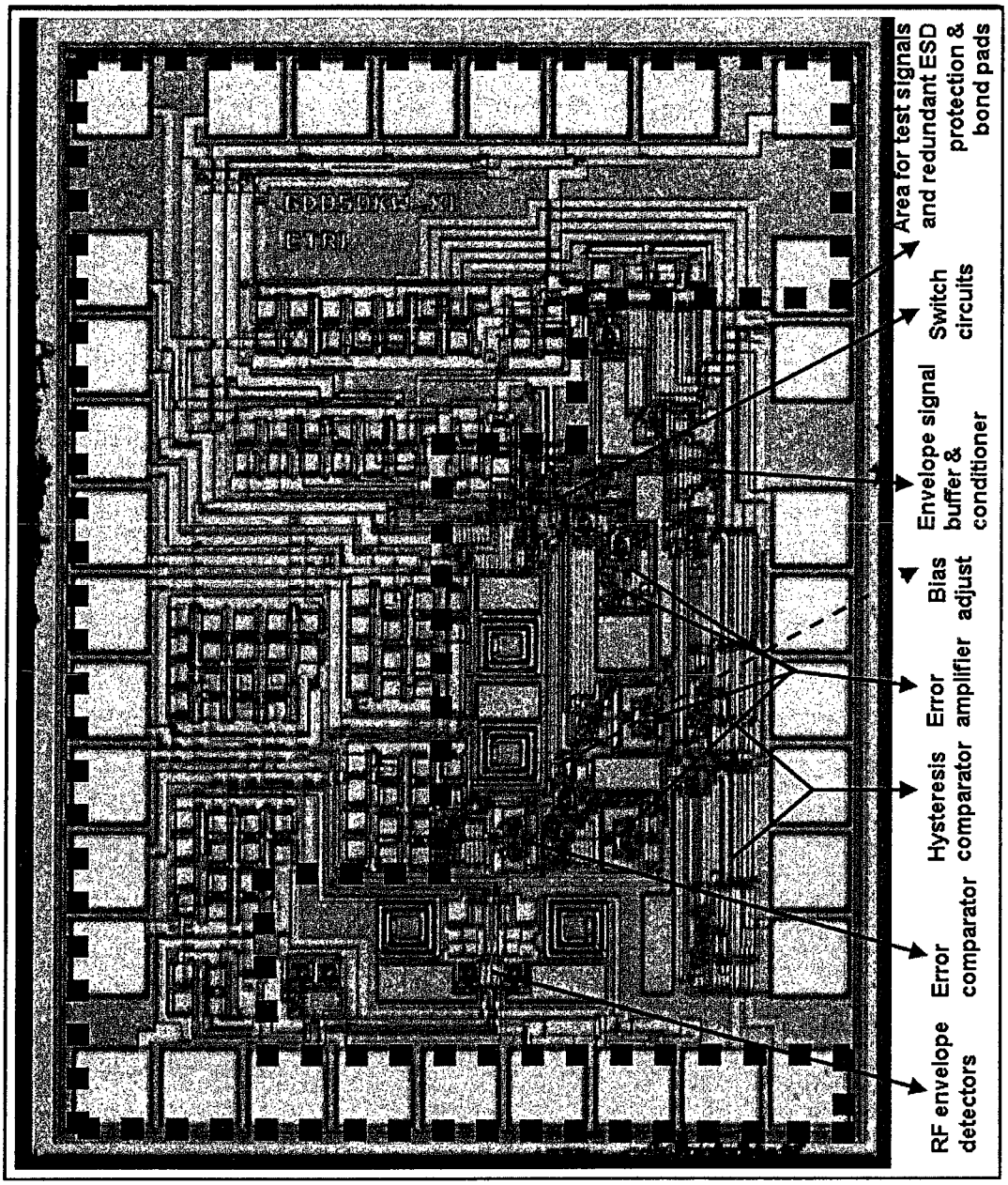

Figure 4.1.2: Photograph of the GaAs HBT chip for the gating, feedback and automatic reconfiguration control circuits represented in Fig. 3.3.1 (Skyworks Solutions' HBT4-P401 4th generation GaAs HBT process).

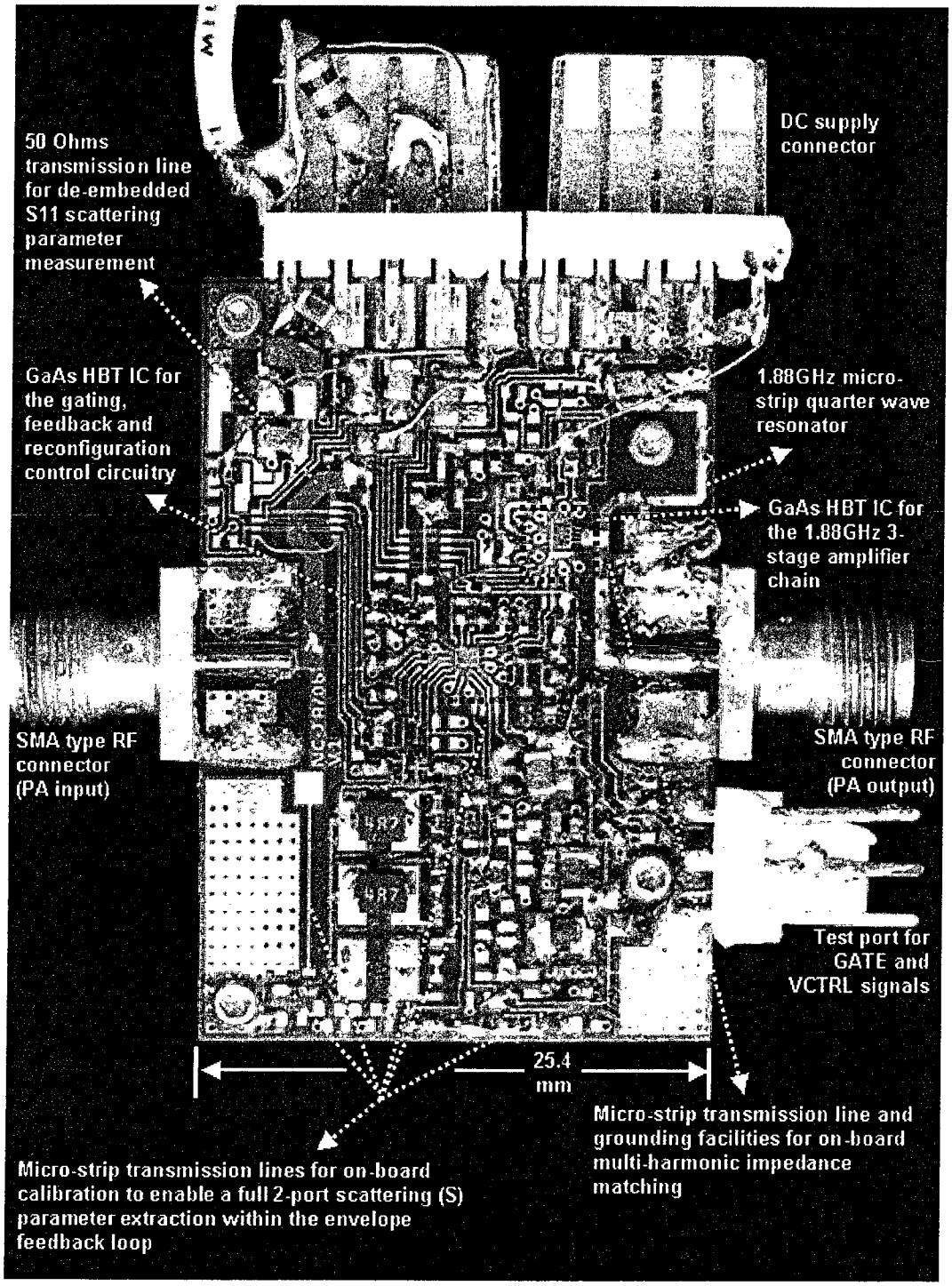

Figure 4.1.3: Photograph of the printed circuit board (PCB) with micro-strip based RF structures and test facilities for de-embedded RF measurements.

Section 4.2
Experimental results

4.2.1 Gain deviation upon hardware reconfiguration

To demonstrate that automatic hardware reconfiguration is indeed performed by the stand-alone PA, and to evaluate the typical gain deviations which are normally involved upon hardware reconfiguration in the RF transistor arrays, the gain of the amplifier system was measured with a continuous wave excitation (CW) in the condition where the GATE signal was ON, thus enabling the hardware reconfiguration circuitry, while the feedback was manually disabled. This was achieved by disconnecting the VCTRL signal of Fig. 3.3.1, and setting the control signals VCTRLP, VATT, VCTRLDR, and VCTRLPS shown in Fig. 3.2.1 to 0 Volt.

For these measurements, the PA's output impedance was adjusted through the control of the load-pull synthesizer (i.e. VAR. Zm in Fig. 3.2.1) in order to obtain an optimum performance trade-off within the effective feedback operation range (Fig. 2.6.1), i.e. the maximum of RF power gain with a stable operation, and the minimum of current consumption, for input power levels lower than ~0 dBm. In a gated envelope feedback embodiment which would include an on-board variable output multi-harmonic matching network, this impedance adjustment could be performed electronically with the use of the GATE signal, as illustrated in Fig. 3.2.1.

Figure 4.2.1 shows the gain variations when the hardware conditioning is automatically performed at the input power levels of -3.5 dBm and -0.3dBm, which can be associated with the hardware reconfiguration thresholds shown in Fig. 2.6.1. Large gain deviations of ~1.36dB are observed.

Gain deviations of up to 1.8dB upon the reconfiguration of an amplifier's RF transistor array were reported in [43].

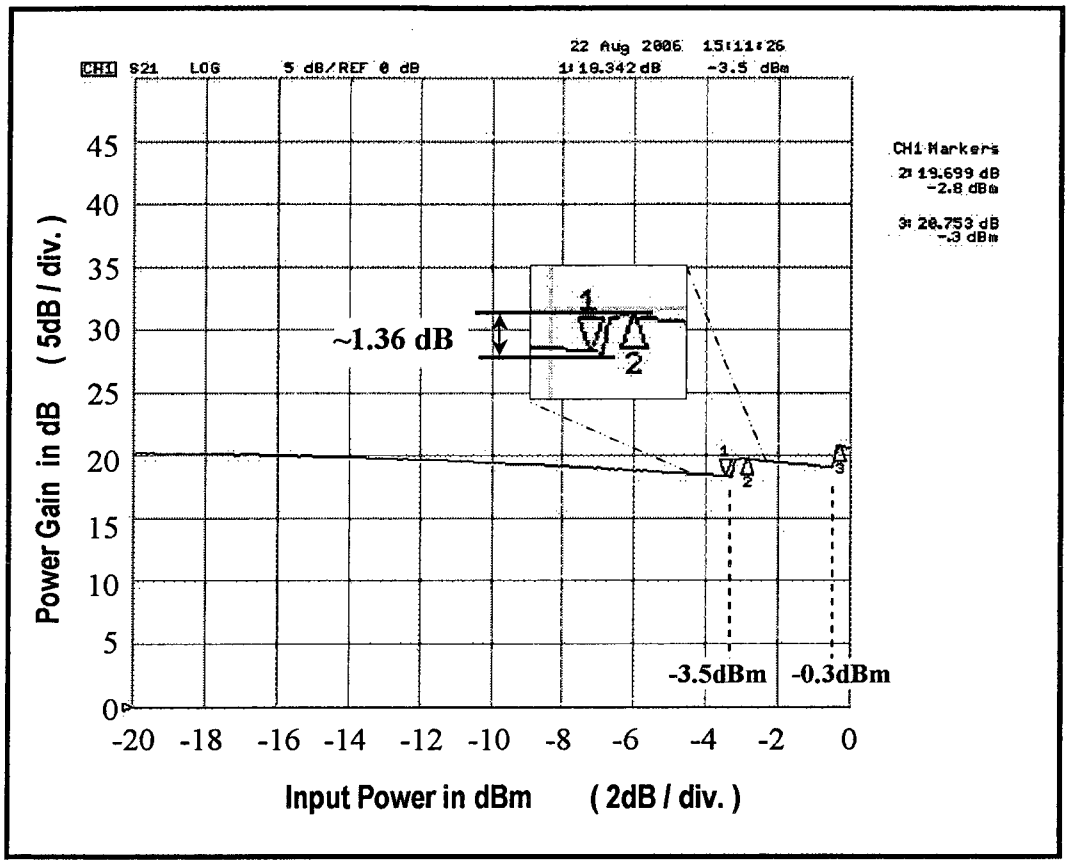

Figure 4.2.1: CW amplifier gain (S_{21}) versus the input power, measured on a vector network analyzer (VNA), with the GATE signal ON and the envelope feedback operation manually disabled.

4.2.2 Gain regulation upon automatic hardware reconfiguration

Figure 4.2.2 shows the gain regulation and return loss performances of the amplifier system beyond the -3.5dBm threshold when the gated envelope feedback is enabled. It can be seen that at ~ -3.5dBm where automatic reconfiguration occurs, there is a very significant reduction in the gain deviation, i.e. from ~1.36dB (Fig. 4.2.1) to ~0.27dB, which demonstrates the automatic gain compensation capability of the system. Between -20dBm and -2dBm of input power, the gain variation remains under ~1dB, which demonstrates the proper operation of the envelope feedback within the effective feedback operation range, as well as an

optimum performance of the gating function across the small signal range and the soft crossover range. This 1dB gain variation, with a peaking at about -10dBm, reflects the closed loop gain transformation through equations (2.6.3), (2.5.9), and (2.5.10) (in this order), as the input power is swept across the small signal range, the soft crossover range, and the effective feedback operation range. Moreover, the input impedance of the amplifier system remains very well matched, with a return loss kept below -23.4dB across the full power dynamic range.

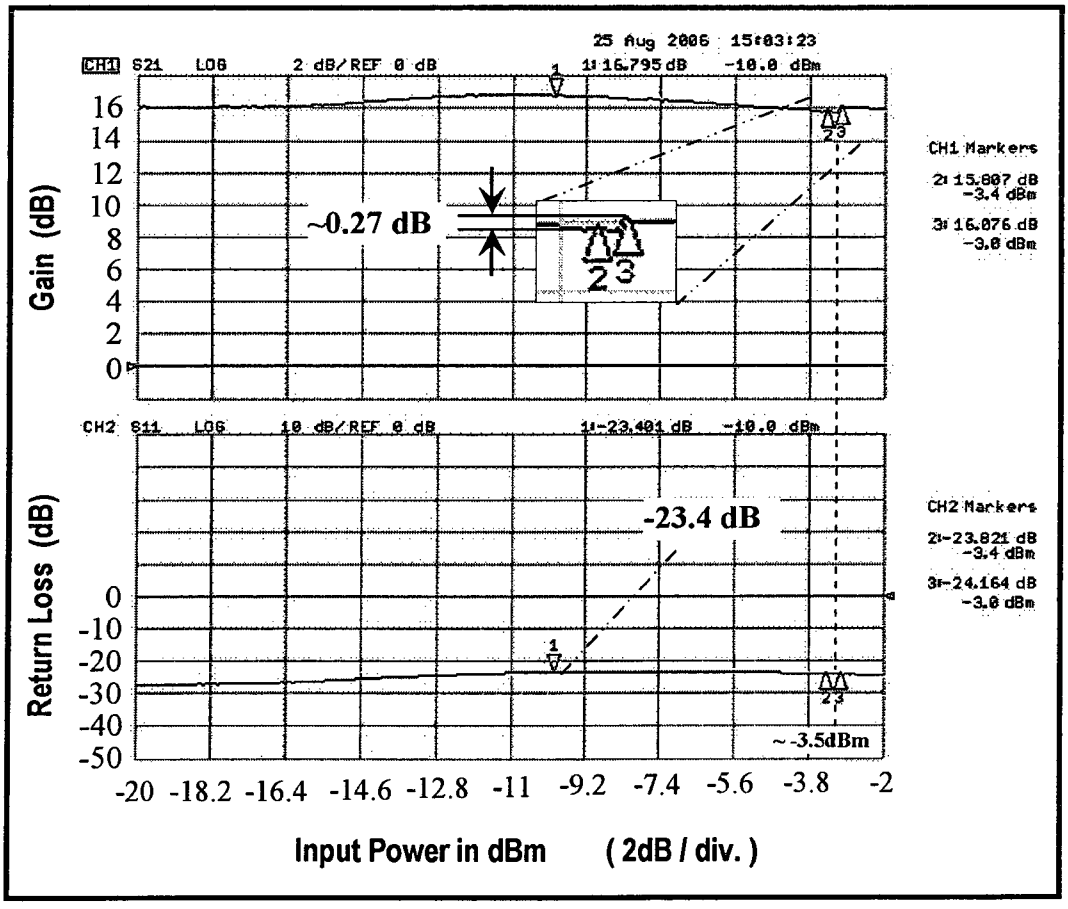

Figure 4.2.2: CW amplifier gain (S_{21}) and return loss versus input power, measured on a vector network analyzer (VNA), with the GATE signal ON and the automatic hardware conditioning and envelope feedback enabled.

4.2.3 Current reduction

Fig. 4.2.3 shows the total current consumption as a function of the output power with a CW input excitation in two cases. In the first case, no hardware reconfiguration is performed and the envelope feedback mechanism is disabled, and in the second case hardware reconfiguration is allowed to take place and the envelope feedback circuitry is enabled.

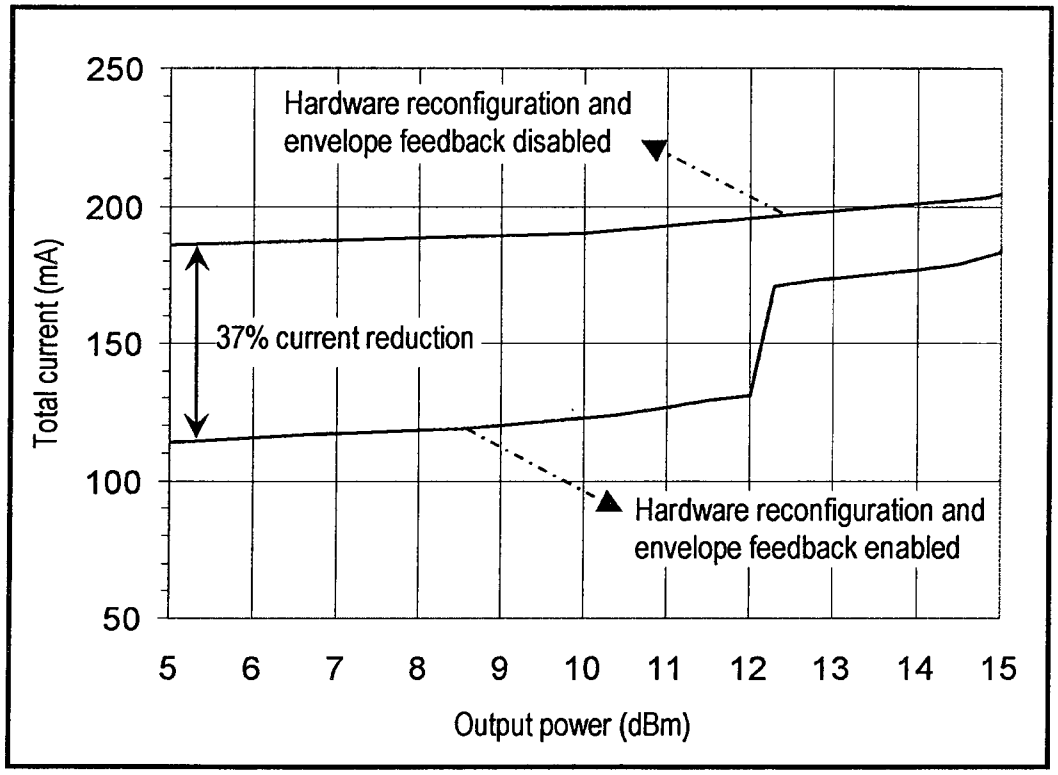

Figure 4.2.3: Total current versus the output power with a CW excitation in the case where hardware reconfiguration and envelope feedback is disabled, and in the case where both are enabled.

These curves demonstrate a significant reduction in the total current consumption as a result of automatic hardware reconfiguration. The sharp current variation occurs due to the switching of half of the RF transistor array in the power stage when the output power crosses a 12dBm

threshold, which also corresponds to the -3.5dBm input power threshold of Fig. 4.2.2. At ~5dBm of output power, an overall ***37% current reduction*** is observed, as a result of automatic hardware reconfiguration.

4.2.4 ACPR performance with CDMA2000-1X modulation for an average input power within the effective feedback operation range

Fig. 4.2.4 shows the measured ACPR performance with a CDMA2000-1X excitation at an average input power of -4.5dBm.

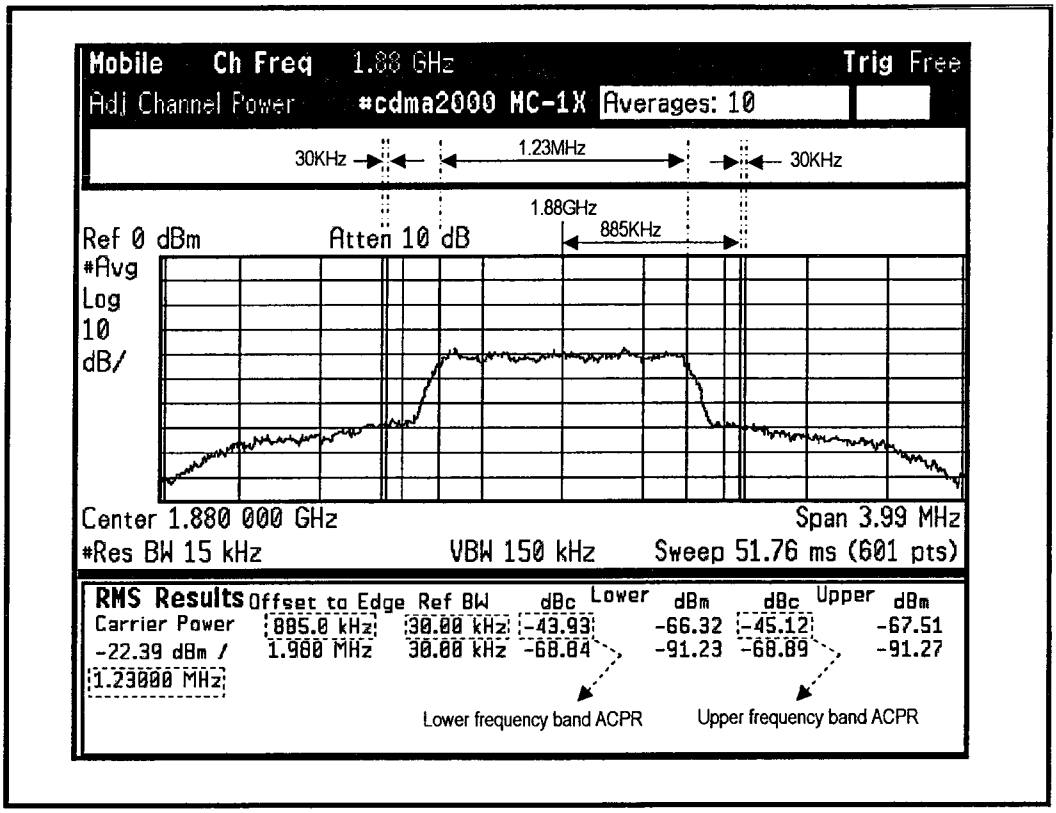

Figure 4.2.4: Adjacent channel power rejection (ACPR) measured on a spectrum analyzer, with an average input power of -4.5dBm.

In these conditions, hardware reconfiguration has been performed automatically, and thus half of the RF transistor arrays in the intermediate

stage and the power stage have been automatically switched off. The -44dBc worst case performance for the lower adjacent channel complies with the -42dBc linearity specification for CDMA transmission.

4.2.5 ACPR and gain regulation versus power

Measured with a CDMA2000-1X input excitation at different average power levels, the gain and the worst case output ACPR performance at 885 KHz offset versus the average output power are shown in Fig. 4.2.5.

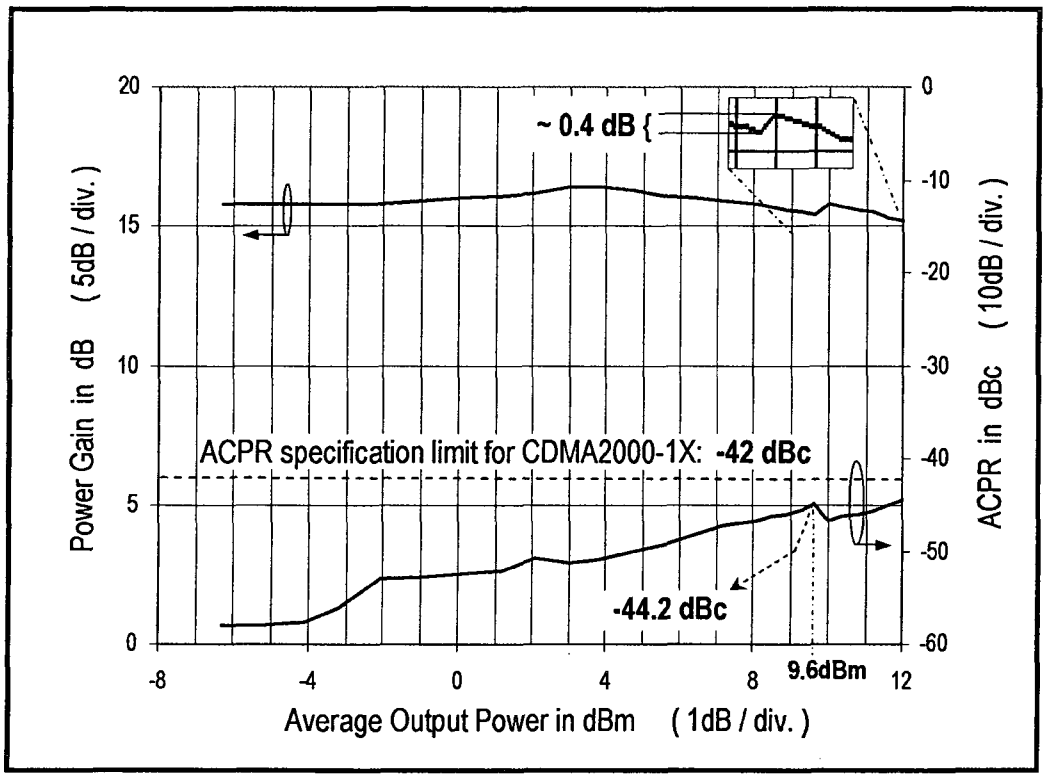

Figure 4.2.5: Measured gain and ACPR performance, showing good gain regulation and compliance with the CDMA2000-1X linearity specifications.

The feedback and soft crossover dynamics shape the instantaneous envelope power of the RF signal. For average output power levels that are in the vicinity of ~4dBm and above, the instantaneous envelope power

effectively sweeps across the small signal range, the soft crossover range, and the effective feedback operation range. These measurements demonstrate that the -42dBc ACPR specification for CDMA2000-1X can be met across the full power range shown in Fig. 4.2.5, and a gain deviation that is reduced to ~0.4dB can be observed at 9.6dBm output power, where automatic hardware reconfiguration occurs.

4.2.6 Waveform quality versus power

Fig. 4.2.6 provides further evidence that the gating function implemented through this design allows meeting the CDMA2000 linearity requirements, despite the fact that the feedback dynamics are dependant on the strongly nonlinear envelope detector response across the crossover range and the effective feedback operation range.

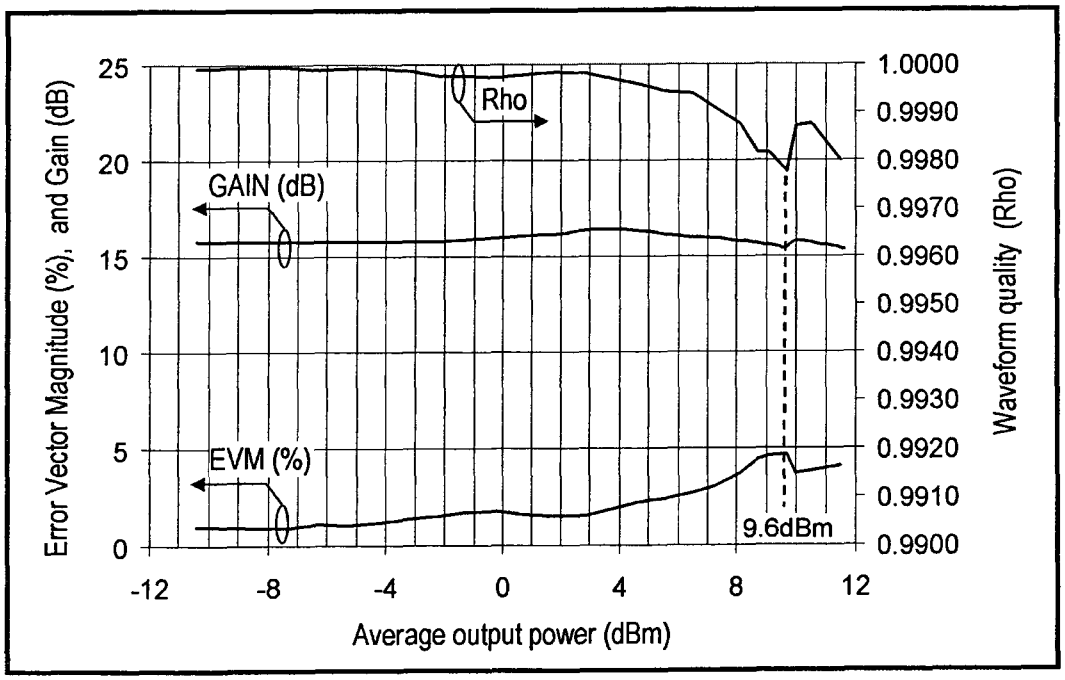

Figure 4.2.6: Measured EVM and Rho (ρ) linearity performances.

The measured waveform quality (Rho) and the error vector magnitude (EVM) performances shown are function of the average power at the output of the amplifier, with a CDMA2000-1X (RVS_RC1_FCH_9.6Kbps) modulated excitation applied at its input.

The waveform quality (Rho) remains well above the 0.944 standard specification limit (see section 2.4.1) and, in the vicinity of the 9.6dBm reconfiguration threshold, the error vector magnitude (EVM) reaches a maximum of 4.7%, which is slightly below the 5% maximum specification typically targeted [66] for a stand-alone amplifier used for the amplification of CDMA2000 signals in mobile transceivers.

4.2.7 Stability and transient performances

The transient response of the closed loop amplifier to an input step excitation is shown in Fig: 4.2.7, for both a continuous wave (CW) signal and a CDMA2000-1X signal. In both cases, the amplitude of the step is adjusted to obtain an average output power of ~9dBm (i.e. below the 9.6dBm threshold shown in Fig. 4.2.5 and Fig. 4.2.6), thus maintaining a section of the RF transistor array in both the intermediate and the power stages turned OFF, and ensuring that the instantaneous envelope power sweeps across the soft crossover range and the effective feedback operation range. The peak of the envelope with CDMA excitation exceeds the 9.6dBm threshold, while linearity is met at this average output power level (as presented in Fig. 4.2.5 and Fig. 4.2.6). This demonstrates the effectiveness of the hysteresis functions and the filtering capacitors C411 and C412 in Fig. 3.3.6 in preventing the automatic reconfiguration mechanism from being triggered by the envelope of the CDMA signal. Still, the response of the amplifier is fast enough (50.24dB/267ns) to comply with the minimum requirement for CDMA transmitters (see section 2.4.2, and the transient response masks in [50]). The optimally flat response seen with the CW measurement case demonstrates a very

stable envelope feedback operation and an optimum transient performance.

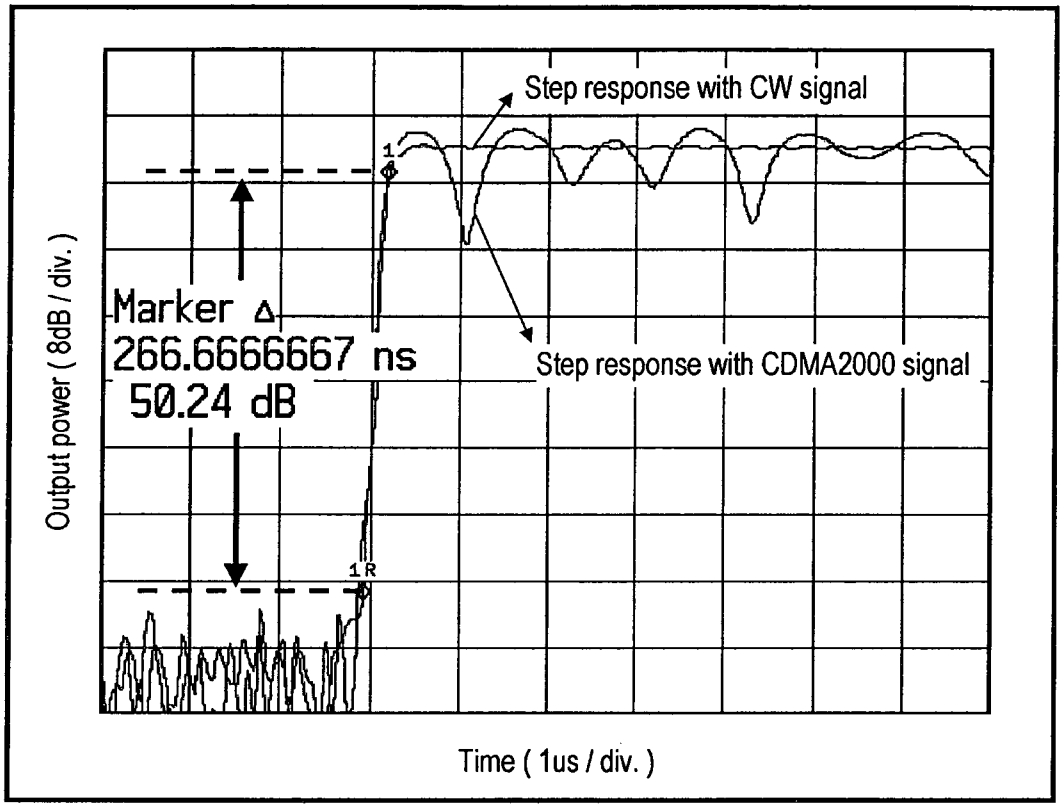

Figure 4.2.7: Measured transient response of the amplifier within the operating range of the gating function (CW and CDMA2000-1X modulation).

4.2.8 Discussion on the experimental results

The experimental data provided above, which demonstrate good performances in regard to some key specifications typically sought for RFIC PA's, are sufficient to validate the gated envelope feedback technique as a promising method for full on-chip automatic hardware reconfiguration, for current reduction purposes. Some discrepancies between the simulated results and the measured results are discussed

below, as a guideline for future development work aimed at refining the performances when employing this technique.

Power gain

While a very stable envelope feedback operation was demonstrated, some RF instability behavior (between ~ 1GHz to 1.5GHz) was observed, and was circumvented by intentionally lowering the gain of the RF amplifier chain and the closed loop feedback gain (set by the RF attenuator in Fig. 3.3.1), and also by trading-off the output impedance matching conditions for improved stability, through the control of the load-pull synthesizer (i.e. VAR_Zm in Fig. 2.6.2). This explains the difference between the measured small signal closed loop gain of ~ 16dB (Fig. 4.2.2) and the simulated small signal closed loop gain of ~ 23dB (Fig. 3.4.1), as well as the difference between the measured small signal open loop gain of ~ 20dB (Fig. 4.2.1) and the simulated small signal open loop gain of ~ 27dB (Fig. 3.2.10).

The full gain of the RF amplifier chain with stable operation may be restored through another design cycle at the IC level and at the PCB level, with the focus on improving the amplifier's stability performance at ~ 1GHz to 1.5GHz with a better modeling of the unwanted RF feedback coupling mechanisms at these frequencies, while maintaining the same gain at 1.88GHz. The use of an active load-pull synthesizer (instead of the passive load-pull synthesizer used in this work) as a computer controlled variable output matching would help considerably in stabilizing the amplifier system under test, since the out-of-band impedances presented by this type of load-pull synthesizer are typically closer to the requirements for stable operating conditions. The quality of the assembly work on the PCB, the routing of the transmission lines, and the location of the surface mount components would be of critical importance also to achieve a high gain with stable operation.

Gain regulation

Based on simulation, the difference between the measured gain deviation with a CW excitation (i.e. 0.27dB as shown in Fig. 4.2.2) and the 0.15dB gain regulation design goal (from section 3.3.3), and also the difference between the CW excitation case and the CDMA excitation case (i.e. 0.27dB versus 0.4dB as shown in Fig. 4.2.5), may be attributed to a lack of on-chip desensitization against asymmetrical current pulling effects on the inputs of the error comparator. These currents are sunk through the V_{deti} and V_{deto} signal lines in the conditioner circuit shown in Fig. 3.3.6, and are dependent on the hysteresis comparators and the switches. Hence, these current pulling effects vary with the envelope of the RF signal and the different hardware states of the PA, which explains a dependency on the type of envelope modulation in the excitation signal. Better immunity against these current pulling effects could be achieved with circuit techniques that provide an increased symmetry in the nonlinear impedance variations on the V_{deti} and V_{deto} signal lines as a function of the envelope variations and the hardware states.

Current reduction and power added efficiency

The 75mA current consumption specification in Table 3.0.1 (i.e. based on a 50% reduction through automatic hardware reconfiguration) and the associated 4% PAE specification that were adopted in this design for an output power of 12 dBm are reasonable, given the scope of demonstrating primarily the feasibility of the gated envelope feedback technique. However, the 4% PAE performance targeted in this design was not met. From Fig. 4.2.3, and using equation (1.1.2), it may be deduced that the measured PAE at 12 dBm output power is 3.3%. This lower efficiency is not primarily attributed to the circuitry employed in the gated envelope feedback architecture, but rather to the fact that the biasing current of the RF transistors had to be intentionally increased during the experimentation, in order to overcome an early compression in the

amplifier's gain response. This has limited the current reduction to 37% (Fig. 4.2.3) in the full hardware reconfiguration state, and negatively impacted the PAE performance. Without this design problem, one can expect a significantly higher current reduction and improved PAE performance with the proposed technique.

Furthermore, while higher PAE figures at comparable power levels have been reported in other work (e.g. 7% PAE at 12 dBm was reported in [43], Fig. 22), the PAE results obtained in this work and the targeted specifications listed in Table 3.0.1 do not represent a performance limitation that is inherent to the gated envelope feedback technique. In fact, simulation shows that the deactivation of larger sections in the RF transistor arrays upon automatic hardware reconfiguration, together with the use of gated envelope feedback circuitry that consume less current would allow obtaining PAE results that are significantly higher and which would compare very favorably with the figures reported in [43].

Adjustment of the power thresholds

The open loop measurement in Fig. 4.2.1 demonstrates that the automatic hardware reconfiguration circuitry is functional at both power thresholds (i.e. at an input power of -3.5dBm and -0.3dBm).

The closed loop measurements in Fig. 4.2.2, Fig. 4.2.3, Fig. 4.2.5, and Fig. 4.2.6 show the activation of the hardware reconfiguration at one power threshold only, which is sufficient to demonstrate the automatic gain compensation and automatic current reduction capabilities of the gated envelope feedback technique, as well as compliance with the linearity specifications.

Because of the effects of RF signals interacting with the analog and control circuitry, the feedback operation is perturbed in the vicinity of the upper threshold (-0.3dBm), which results in degraded closed loop performances at this power level, and which are not relevant in evaluating the potential of the proposed technique. Hence, the closed loop

performances upon automatic hardware reconfiguration are shown for the lower threshold only.

In order to demonstrate a maximum of current reduction upon hardware reconfiguration, the circuits were adjusted in order to enable the automatic reconfiguration of the power stage at the lower threshold, which corresponds to -3.5dBm in Fig. 4.2.1 and Fig. 4.2.2, 12dBm in Fig. 4.2.3, and 9.6dBm in Fig. 4.2.5 and Fig. 4.2.6. The automatic reconfiguration of the driver stage was set at the upper threshold, which corresponds to -0.3dBm in Fig. 4.2.1.

Difference in the power thresholds between the CW modulation case and the CDMA modulation case

The difference between the 12dBm threshold of Fig. 4.2.3 in the CW excitation case and the 9.6dBm threshold of Fig. 4.2.5 in the CDMA excitation case is justified mainly by two aspects. The triggering thresholds of the hysteresis comparators (T_H and T_L in Fig. 3.3.7) are dependant on the envelope variations, because this circuitry is not fully desensitized against the effects due to RF perturbations, such as the rectification of RF signals in base-emitter junctions, which may result in shifts in the threshold values. The RF carrier fundamental and the harmonics present at the output of the input envelope detector (i.e. at the collector of Q221 in Fig. 3.3.2) are not totally rejected by R231, C223 and L223, and, as can be deduced from Fig. 3.3.3, a shift of only 100mV in the voltage thresholds of the comparator can translate into as much as 3dB of power offset.

Also, while C411 and C412 in Fig. 3.3.6 are effective in their filtering roles to prevent a toggling of the hardware reconfiguration mechanism by the envelope of the input RF signal, their asymmetrical charge and discharge time constants may still influence the toggling thresholds of the hysteresis comparators, depending on the envelope amplitude.

Note also that the ACPR performance in Fig. 4.2.4 was measured with slightly different measurement settings that affected only the power thresholds. However, it was verified that with -4.5dBm of input power, hardware reconfiguration had been performed automatically on both the intermediate and the power stages, even though Fig. 4.2.5 indicates an input power threshold of ~ -6dBm.

The importance of on-chip isolation design techniques

The gain regulation, the RF-to-analog perturbation, as well as the power threshold shift issues described above, and to some extent also the RF instability encountered, relate to the need for robust on-chip isolation design methodologies to minimize the undesired effects that stem from the interaction between a modulated, high intensity RF signal and highly nonlinear analog circuits on the same die (e.g. the biasing circuits, the conditioner circuit, and the hysteresis comparators). This is an important design issue, as it constitutes one of the major challenges that are at the heart of any RF system-on-chip integration.

Extensive simulation has been carried out to address this issue during the design phase. This has allowed demonstrating in a conclusive way, within the scope of this research work, that the use of the gated envelope feedback technique enables a very significant reduction in the gain deviation upon automatic hardware reconfiguration.

Because of the difficulty to predict accurately these undesired nonlinear effects, the optimization of the on-chip isolation mechanisms for improved performances in a commercial application of the technique would likely benefit from a modular design approach during an intermediate design phase. The critical sections that can be defined as sensitive to RF and analog interaction (e.g. the conditioner circuit and the hysteresis comparators), and which are likely to introduce significant perturbations in the neighboring circuitry (e.g. the envelope error comparator) could be

implemented, during the intermediate design phase, as separate circuit blocks with the appropriate test facilities that allow accurate experimental characterization, for the purpose of comparing the simulated results with the measured results. The design adjustments in the final design cycle would then be function of circuit behavioral parameters that reflect a more accurate description of these undesired effects, and this would help significantly in the design convergence toward achieving better on-chip isolation.

Chapter 5

CONCLUSION & FUTURE WORK

5.1 Summary

The results obtained through this work allow concluding that the research objectives defined in section 2.2.2 of this thesis were met, and that contributions were made to research in the field of RFIC power amplifiers for wireless communications through the concepts and techniques that were demonstrated.

A new approach to the hardware reconfiguration of RFIC PA's for current reduction purposes has been proposed. It is based on the gated envelope feedback technique that was introduced in this work. This approach offers key advantages and a promising potential in terms of performances, in regard to the RFIC PA's and the RF front-end sections found in modern wireless transceivers.

Demonstrated multi-state hardware reconfiguration capability, increased RFIC PA autonomy, and flexibility

In contrast with the techniques that have been reported for RFIC PA hardware reconfiguration prior to this work (e.g. [43], [45], [48]), the hardware reconfiguration method introduced in this work allows ideally for automatic switching between an unlimited number of hardware states within a predetermined power range, with the use of a single external control line.

It was demonstrated that upon the self-reconfiguration of on-chip biasing and RF circuitry, the associated gain deviations are significantly reduced in a fully automatic fashion.

As a result of these automation features, the requirements for synchronization between the PA and the other components in the RF

front-end section of the transceiver are reduced, and the gain calibration requirements are also significantly reduced, i.e. to 3 measurement points at room temperature only.

Moreover, this approach to hardware reconfiguration offers flexibility in its application, as various types of hardware reconfiguration schemes that introduce gain perturbations are likely to benefit from the underlying self-conditioning concept. The reconfiguration of RF transistor array topologies (e.g. [43]), the deactivation of RF transistor arrays (e.g. [45]), the paralleling of low power and high power amplifier blocks in a switched fashion (e.g. [67]), and the load modulation techniques (e.g. [17]), may be cited as examples.

Envelope feedback gating, hardware reconfiguration circuitry, and design guidelines

The RFIC PA architecture that was proposed in this work includes on-chip signal detection and sequential logic for the automatic triggering of the hardware reconfiguration, and uses the gated envelope feedback technique to achieve the automatic gain compensation.

It was demonstrated that the use of a hardware gating function in conjunction with envelope feedback enables a fully functional on-chip embodiment of envelope feedback as a means to regulate the gain. With the use of the gating function, the requirements for optimum envelope feedback operation is restricted to only the power range where gain perturbations may occur, which results in a drastic simplification of the circuitry, compared to other envelope feedback embodiments that have been proposed (e.g. [27]-[28], [58]-[59]).

Design guidelines for an optimum embodiment of the gating function were derived, namely in terms of shaping the nonlinear gain profiles of the RF envelope detectors as a function of power and designing for the maximum of performance matching between them, in order to ensure minimum distortion at the output of the amplifier system.

Demonstrated suitability for GaAs HBT technologies

The gated envelope feedback technique method was validated in a full GaAs HBT on-chip implementation, thereby demonstrating that this technique is better positioning GaAs RFIC PA's in terms of integrating complex control functions for current reduction at low power levels. The circuit techniques that stem from the simplification brought by the gating function and that suit GaAs HBT technologies have been described and analyzed, and successfully implemented in a dual IC design totaling a die area of only 1.4mm^2, demonstrating a clear path toward single-chip integration in this technology, as well as the cost and size effectiveness associated with this approach for RFIC PA hardware reconfiguration.

Demonstrated functionality and performances

The experimental results on gain, current reduction, linearity, and transient response, which were obtained from the 1.88GHz CDMA RFIC PA design that was presented in this work, allow concluding that the gated envelope feedback technique is a viable and promising approach to self-operating hardware reconfiguration for current reduction (hence for efficiency improvement) as a function of power, and suitable for CDMA applications. Measurements on the gain regulation upon hardware reconfiguration have demonstrated a reduction in the gain deviation from 1.36dB to 0.27dB with a CW input excitation, which is indicative of a promising potential, given the 1dB power incremental step and +/- 0.5dB precision requirements for CDMA mobile transmitters.

A gain regulation of 0.4dB upon hardware reconfiguration with a CDMA input excitation was demonstrated, and technical grounds were provided to justify that the automatic gain compensation that is achievable with this hardware reconfiguration technique in both the CW and the CDMA cases may be improved with better on-chip circuit isolation techniques.

At low power levels, a 37% reduction in the total current consumption upon automatic hardware reconfiguration was demonstrated, which

supports the viability of proposed approach for power efficiency improvement.

It was also verified that despite the strongly nonlinear RF envelope detector response that form part of the gating function, the careful optimization of the design as per the design guidelines that were derived allow obtaining full compliance with the linearity requirements for CDMA2000 wireless transceivers. An ACPR performance that is within the -42dBc standard specification, a waveform quality factor (Rho) which is well above the 0.944 minimum specification value, and an error vector magnitude (EVM) that is below the 5% figure of merit typically sought for stand-alone CDMA RFIC PA's in the industry were demonstrated with the gated envelope feedback PA implementation reported in this work.

The measured performances with both a CW and CDMA2000 excitation also demonstrated the possibility of achieving optimum transient responses with a very stable operation, even when operating at a power level where the instantaneous envelope of the modulated signal crosses the automatic hardware reconfiguration thresholds. Yet, the measured time response (~ 50dB/267ns) complies with the transient response masks that define the minimum requirements for CDMA2000 wireless transceivers.

Design equations and a methodology for IMD analysis

A methodology based on design equations for estimating the inter-modulation distortion (IMD) performance requirements of circuit blocks within the error signal path of an envelope feedback amplifier was introduced, and supported with numerical examples that relate to the nonlinearities in the RF power amplifier chain and the RF envelope detectors that were practically implemented in the course of this work. It was also demonstrated how these design equations may be used at the system level in investigating the IMD performances related to the gain switching profiles associated with hardware reconfiguration.

The proposed design equations are valid under the assumption of a quasi-static and memoryless response of the amplifier system. They may be used as an IMD analysis tool in the form of a system of nonlinear equations to calculate the IMD levels at any node within a typical envelope feedback amplifier architecture, with the help of a mathematical computation software such as MATLAB(TM). The equations are based on a three-tone excitation and a 5^{th} order power series representation of the nonlinearities in the RF amplifier chain, and allow the parameterization of the input variables to the system of equations in terms of the following: the peak-to-average envelope voltage ratio of the excitation signal, the input multi-tone levels, the desired output IMD levels, the small signal feedback loop gain, and the coefficients of the power series. They may also be extended to higher order power series representations for enhanced precision and increased flexibility in their application.

These readily applicable formulations may facilitate IMD analyses during the design phase of envelope feedback amplifiers, and may be used with behavioral models to simplify simulation tasks, possibly as a means for circumventing convergence problems during simulation. The proposed design equations and methodology are likely to be particularly helpful during the experimental development phase of an envelope feedback amplifier, as they may be used independently of the circuit simulation environment to facilitate the experimental validation and optimization of the IMD performances of circuit blocks in the error signal path in open loop conditions, using exclusively the design goals and the system parameters that may be obtained from the practical circuit implementation.

5.2 Topics for future research

As an extension to the concepts presented in this thesis and the results obtained through this work, some of the research topics that may be explored are listed below.

Circuit techniques for better on-chip isolation

The gain regulation performances (0.27dB with CW excitation and 0.4dB with CDMA2000 excitation) were limited partly by the effects of perturbations in the form of current pulling on the error comparator, which points to the possibility for improved performances with better on-chip isolation techniques. Problems of this nature are at the heart of RF system-on-chip (S.O.C.) integration, and thus research on RF circuit techniques that enable better on-chip immunization against RF perturbations through conduction and substrate coupling would be very relevant to the improvement of the gated envelope feedback technique, as well as for other RFIC applications.

Integration in GaAs BiFET technology

The validation of the gated envelope feedback technique was carried out with Skyworks Solutions' 4th generation GaAs HBT semi-conductor process, which is an NPN bipolar transistor only process. While GaAs BiFET technologies, which allow the use of both FET and HBT transistor devices on the same GaAs IC, have been proposed for LSI high-speed digital applications for over a decade [68]-[69], only recently that the GaAs BiFET processes have been demonstrated to offer potential for RFIC PA applications, with greatly enhanced integration capabilities, while maintaining the outstanding RF performances of GaAs technologies [70]-[71]. However, there is still a need to further demonstrate and exploit the full potential of this technology for the integration of complex PA functions. Hence, investigating the possibility of higher systems and circuits integration with a GaAs BiFET process for the implementation of more complex PA control functions for power efficiency and linearity management would be very relevant for the emerging wireless technologies.

Application of the gating function to feedback in other areas

The concept of using a hardware gating function in conjunction with feedback was introduced in this work as a means for restricting the requirements for optimum envelope feedback operation only to the power range where gain perturbations may occur in an RFIC PA application. It would be relevant to investigate whether and how the same feedback gating concept could be applied to other applications that rely on feedback, for the purpose of simplifying circuit structures and enabling higher on-chip integration.

Envelope feedback IMD analysis and characterization

The general formulations introduced in this work for IMD analysis applied to envelope feedback architectures, with a 5^{th} degree representation of the nonlinearities in the power amplifier block and a 3-tone input excitation, allow evaluating the IMD requirements for circuit blocks in the error signal path as a function of system parameters and the closed loop output IMD performance goals. Integrated design, characterization and simulation methods (e.g. [72]-[73]) have been demonstrated to improve the design and development cycles. It would be very relevant to the area of computer aided design (CAD) techniques for microwave systems to investigate how these formulations may be incorporated in behavioral model-based algorithms for more efficient power amplifier design methodologies. Their use as part of alternative strategies for avoiding convergence problems during simulation may be of particular interest.

Moreover, investigations on how to incorporate these formulations into automated test systems would be very relevant to techniques for circuit characterization and automated testing methodologies.

Appendix I

Some electrical specifications for the active and passive devices in Skyworks' HBT4-P401 GaAs HBT library

(Printed with permission from Skyworks Solutions, Inc., USA)

Parameter	Specification
D.C. current gain (Beta) @ 0.1mA/μm^2	115
V_{BE} @ 0.1mA/μm^2	1.34V
B_{vebo} @ Je = 100nA/μm^2	9.3V
B_{vcbo} @ Ic = 200 nA	27V
B_{vceo} @ Jc = 0.5 $\mu A / \mu m^2$	14.8V
Schottky turn-on @ J = 20 $\mu A / \mu m^2$	0.688V
BC diode turn-on @ J = 10 $\mu A / \mu m^2$	1.222V
BE turn-on @ J = 20 $\mu A / \mu m^2$	1.265V
F_T @ 0.25mA / μm^2, V_{CE} = 1.5V	46.9 GHz
MIM capacitor	0.93 fF/μm^2
TaN Resistor	50 Ohms/sq.

Appendix II

Components values

Transistor and diode values define the areas (in μm^2) associated with the transistor Emitter area and the diode Base Contact Via area. Resistor values are in Ohms. Capacitor values are in pF. Inductor values are in nH, with quality factors (Q) at 1.88GHz. Via inductance (LV) values are in nH. All bond wires are simulated with the Philips/TU_Delft ADS(TM) models; all bond wire dimensions are in μm, and the bond wire values define the spacing (in μm) between two adjacent wires.

Variable gain block (Fig. 3.2.2)

Ref. ID	Q51	Q52	D51,D53	D52	R51	R52	R53	C53
Value	236	59	400	32	25	1K	100	6
Cell name or description	qrh2s	qrh2s	dbc	ds	TaN	TaN	TaN	MIM

Intermediate stage (Fig. 3.2.4)

Ref. ID	Q61,Q62, Q63,Q64	C64,C65	L62,L63
Value	59	3.6	0.75
Cell name or description	qrh2s	MIM	Q=4

Power stage (Fig. 3.2.6)

Ref. ID	Q91	C92,C93	L91,L92
Value	59	3.6	0.75
Cell name or description	qrh2s	MIM	Q=4

Output matching network (Fig. 3.2.8)

Ref. ID	b121 to b124	C121	C122	C123	C124	C125	LV
Value	200	100	9	2.2	1.5	3.3	0.3
Cell name or description	Rw=12.5 Gap=2500 Start=600 MaxH=900 Tilt=800 Stretch=800 StopH=500	SMT	SMT	SMT	SMT	SMT	

RF envelope detectors (Fig. 3.3.2)

Ref. ID	Q221, Q222	D221, D222	R221, R222	R223, R224	R225, R226	R231, R232	L223, L224	C223, C224
Value	59	400	1200	70	60	400	2	2.2
Cell name or description	qrh2s	ds	TaN	TaN	TaN	TaN	Q=4	MIM

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