# Low-loss passive serial-to-WDM interface for energy-efficient optical interconnects

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# Abstract

The increasing number of computational servers in the data centers is imposing tighter constraints on the networking infrastructure. Conventional dense electronic integration introduces large RC delay, latency, jitter and leads to high power consumption, that increases the operational cost of the data center network. Optical interconnects can address some of the challenges to improve the power efficiency, bandwidth capacity and scalability of the physical layer in the data center network. Therefore, scalable power efficient optical interconnect network becomes necessary to leverage the bandwidth capacity of current electronic switches or opto-electronic components. Novel optical interconnect technology can enhance the network capacity by harnessing the feasibility of simultaneous processing of optical signal in the wavelength and time domains.

Interconnect with discrete optical components such as vertical-cavity surface-emitting lasers (VCSELs); multimode fibers; and off-chip photodetector-based receiver modules have already been deployed. However, to further increase the scalability, reliability and operational flexibility of interconnects, hybrid or monolithically integrated optical and electronic components are necessary. Therefore, extensive research to design and characterize the optical components on photonic integrated circuits (PICs) is going on to build the optical interconnects that will meet the ever increasing bandwidth demand.

Propagation loss of the integrated optical waveguide is one of the key challenges to design optical components that requires large time delay to implement functionalities such as buffering, time division multiplexing. For example, conventional InP and silicon waveguides exhibit 1.5 dB/cm and 2.5 dB/cm propagation loss, respectively. InP or silicon waveguide based optical buffers will suffer from more than 100 dB loss to implement just $\sim$10 ns time delay. Therefore it is important to investigate the possibility of using a low-loss integrated

waveguides to build photonic circuit that requires long optical buffers.

In this thesis, we present two photonic components designed on a low-loss $Si_3N_4$ waveguide platform : a thermally tunable 1 × 4 channel wavelength demultiplexer and a four channel passive wavelength-striped mapping (PWSM) device. We have also proposed an optical time sampling based photoreceiver and a ring-based 25 Gb/s DAC-less reverse biased PAM-4 modulator. The latter two devices are designed on the silicon photonics platform. The design and characterization result of these two devices are presented briefly in this thesis.

The thermally tunable 1 × 4 channel optical demultiplexer is designed using an ultra low-loss $Si_3N_4$ (propagation loss ∼3.1 dB/m) waveguide. The demultiplexer has three 2 × 2 Mach-Zehnder interferometers (MZI), where each of the MZIs contains two 2 × 2 general-interference-based multimode interference (MMI) couplers. The MMI couplers exhibit -3.3 dB to -3.7 dB power division ratios over a 50 nm wavelength range from 1530 nm to 1580 nm. The Chromium (Cr) heaters placed on the delay arms of the MZI filters enable thermal tuning to control the optical phase shift in the MZI delay arms. This facilitates achieving moderately low crosstalk (14.5 dB) between the adjacent channels after optical filtering. The optical insertion loss of the demultiplexer per channel is between 1.5 dB to 2.2 dB over 1550 nm to 1565 nm wavelength range. Error free performance (bit error rate (BER) of $10^{-12}$) is obtained for all the four 40 Gb/sec data rate channels. The optical demultiplexer is an important toolbox towards building photonic integrated circuits with complex optical signal processing functionalities in the low-loss $Si_3N_4$ waveguide platform.

Next, we present the four channel optical PWSM device, which passively time compresses/expands serial packets through optical wavelength multiplexing/demultiplexing. The PWSM device, which has a 1 × 4 channel optical wavelength demultiplexer with integrated optical delay lines, is also designed in the low-loss $Si_3N_4$ waveguide platform.

The PWSM device multiplexes/demultiplexes four wavelength division multiplexed (WDM) channels and offsets in time the adjacent channels to optically serialize/de-serialize the data packets. In this demonstration, a 64 ns long data packet is formed at the output of the device by combining four 16 ns data segments of the packet in the time domain. Incremental optical insertion losses between the adjacent channels is 9.7 dB due to the integrated passive optical delay waveguides. We have measured a bit error rate (BER) performance below $1 \times 10^{-9}$ for the 64 ns serial data packet regenerated by the PWSM device for a received optical power of -6.7 dBm.

In addition to these two components, a novel photoreceiver architecture enabling parallel processing of a high-speed optical signal in the electronic domain is demonstrated using SiGe photodetectors. This allows the electronics to operate at a significantly lower frequency than the optical signal and hence reduces power consumption and the impact of parasitic capacitance. The photoreceiver performs optical time sampling with four integrated SiGe photodetectors connected in series by waveguide delay lines. Four variations of the optical time sampling receiver are designed and demonstrated which differ by the data rate (10 Gb/s and 20 Gb/s) and silicon delay waveguide loss (2.5 dB/cm and 0.2 dB/cm). The BER performance of the photodetectors in the receiver was measured individually and reached a performance below $1 \times 10^{-10}$ at an input optical power between 4.8 and 6.3 dBm through an off-chip 50 $\Omega$ load at the output. After O/E conversion, the electrical signal (one segment of $2^{15} - 1$ PRBS data) from each of the photodetector is processed without errors at a quarter of the bit rate, leading to an overall more power efficient receiver front-end.

## Sommaire

Le nombre croissant de serveurs informatiques dans les centres de données impose des contraintes plus strictes sur l'infrastructure de réseau. L'intégration électronique dense conventionnelle présente un grand retard de RC, une latence, une fluctuation dans le temps et requiert une forte consommation d'énergie, ce qui augmente les coûts d'exploitations du réseau des centres de données. Les interconnexions optiques peuvent répondre à certains des défis pour améliorer l'efficacité énergétique, la capacité de la bande passante et l'évolutivité de la couche physique du réseaux des centres de données. Par conséquent, la puissance évolutive efficace des réseaux d'interconnexion optiques devient nécessaire pour tirer parti de la capacité de la bande passante de commutateurs électroniques actuels ou des composants optolectroniques. La technologie novatrice d'interconnexion optique selon l'invention peut améliorer la capacité du réseau en mettant à profit la possibilité d'un traitement simultané du signal optique dans la longueur d'onde et en matière de temps.

L'interconnexion avec les composants optiques discrets tels que le laser à émission de surface de commande et à cavité verticale (LÉSCV), les fibres multimodes et les modules hors puce photodétecteurs à base de récepteurs ont déjà été déployés. Toutefois, pour augmenter davantage l'évolutivité, la fiabilité et la flexibilité opérationnelle de l'interconnexion, les composants optiques et électroniques intégrés hybrides ou monolithiques sont nécessaires. Par conséquent, des recherches approfondies pour concevoir et caractériser les composants optiques sur circuit intégré photonique (CIP) est en cours pour construire l'interconnexion optique qui répondra à la demande croissante de bande passante.

L'affaiblissement de propagation du guide d'onde optique intégré est l'un des principaux défis pour concevoir le composant optique qui nécessitent un grand délai à mettre en œuvre des fonctionnalités telles que le tamponnage et le multiplexage temporelle. Par exemple, les

guides d'ondes en InP et de silicium conventionnels présentent 1.5 dB/cm et 2.5 dB/cm un affaiblissement de propagation respectivement. Les tampons optiques à base InP sur guide d'ondes en silicium souffriront une perte de plus de 100 dB pour mettre en œuvre seulement ∼10 ns de délai. Par conséquent, il est important d'étudier la possibilité d'utiliser des guides d'ondes intégrés à faible perte pour construire un circuit photonique qui requièrent de longs tampons optiques.

Dans cette thèse, nous présentons deux composants photoniques conçus sur la plateforme à faible perte de guide d'ondes $Si_3N_4$: un démultiplexeur en longueur d'onde de $1 \times 4$ canaux thermiquement accordable et un dispositif à quatre canaux de cartographie de longueur d'onde à rayures passives (CLP).

Le démultiplexeur optique de $1 \times 4$ canaux thermiquement accordable est conçu en utilisant une faible perte de guide d'ondes $Si_3N_4$ (perte de propagation ∼3.1 dB/m). Le démultiplexeur a trois $2 \times 2$ interféromètres de Mach-Zehnder (MZI), où chacun des MZI contient deux coupleurs interférences multimodes (IMM) à base de deux $2 \times 2$ à interférence générale. Les coupleurs MMI présentent des rapports de division de puissance de –3.3 dB à –3.7 dB sur une gamme de longueur d'onde de 50 nm de 1530 nm à 1580 nm. Les appareils de chauffage à base de chrome (Cr) placés sur les bras de délai des filtres de MZI permettent le réglage thermique pour commander le décalage de phase optique dans les bras de délai MZI. Cela facilite la réalisation modérément faible de couplage (14.5 dB) entre les canaux adjacents après le filtrage optique. La perte d'insertion optique du démultiplexeur par canal est entre 1.5 dB et 2.2 dB sur la gamme de longueurs d'onde de 1550 nm à 1565 nm. Un fonctionnement sans erreur (taux d'erreur binaire, BER, de $10^{-12}$) est obtenu pour tous les quatre canaux à un débit binaire de 40 Gb/s. Le démultiplexeur optique est un composant important pour la construction de circuits intégrés photoniques avec fonctionnalités complexes de traitement de signal optique dans la faible perte plateforme

de guide d'ondes $Si_3N_4$.

Ensuite, nous présentons le dispositif à quatre canaux optiques de cartographie de longueur d'onde à rayures passives (CLP), qui comprime/décomprime passivement le temps des paquets en série par le multiplexage/démultiplexage de longueur d'onde optique. Le dispositif CLP, qui présente un démultiplexeur optique de canal $1 \times 4$ de longueurs d'onde intégrés avec des lignes à délais optiques, est également réalisé sous la plateforme de guide d'ondes à faible perte $Si_3N_4$. Le dispositif CLP multiplexe/démultiplexe quatre canaux WDM et ajuste le délai des canaux adjacents en sérialisant/désérialisant optiquement les paquets de données. Dans cette démonstration, un paquet de données long de 64 ns est formé à la sortie du dispositif en combinant quatre segments de données de 16 ns du paquet dans le domaine temporel. La perte graduelle d'insertion optique entre les canaux adjacents est de 9.8 dB due aux guides d'ondes intégrés à retard optiques passifs. Nous avons mesuré des performance de taux d'erreur binaire inférieur à $1 \times 10^{-9}$ pour le paquet de données en série régénéré de 64 ns par le dispositif CLP pour une puissance optique reçue de – 6.7 dBm.

En plus de ces deux composants, une nouvelle architecture de photorécepteur permettant le traitement parallèle dans le domaine électronique d'un signal optique à grande vitesse est démontrée en utilisant les photodétecteurs SiGe. Cela permet à l'électronique de fonctionner à une fréquence nettement inférieure à celle du signal optique et donc de réduire la consommation d'énergie et l'impact des parasites. Le photorécepteur optique effectue un échantillonnage temporel avec quatre photodétecteurs SiGe intégrés connectés en série par des lignes à délai. Quatre variantes du récepteur d'échantillonnage temporel optique sont conçues et démontrées qui diffèrent par le débit de données (10 Gb/s et 20 Gb/s) et une perte de guide d'ondes (2.5 dB/cm et 0.2 dB/cm). La performances de taux d'erreur binaire des photodétecteurs dans le récepteur a été mesurée individuellement, et a atteint un rendement inférieur à $1 \times 10^{-10}$ à une puissance optique d'entrée entre 4.8 et 6.3 dBm

par l'intermédiaire d'une résistance de charge hors puce de 50 Ω à la sortie. Après la conversion O/E, le signal électrique (un segment de données PRBS de $2^{15} - 1$) de chacun des photodétecteurs est traité sans erreur à un quart du débit binaire, menant à un récepteur plus efficace en puissance.

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## Contributions of the Author

The work presented in this thesis has been published in four journal papers and two conference papers. Three patent applications are a result of the research work presented in this thesis.

**Patent application related to this thesis:**

[1] O. Liboiron-Ladouceur, **M. S. Hai**, P. G. Raponi, N. Andriolli, I. Cerutti, and P. Castoldi, "Methods and Devices for Space-Time Multi-Plane Optical Networks," US 13/913,652, issued July 22, 2016.

O. Liboiron-Ladouceur: Proposed the idea. Supervised the work. She wrote, edited and reviewed the manuscript.

M. S. Hai: Simulated the theoretical model of the PWSM circuit presented in the paper and wrote part of the manuscript.

[2] M. Ménard, O. Liboiron-Ladouceur, and **M. S. Hai**, "High-speed Silicon Photonic Photoreceivers Based on Optical Time Sampling," US 15/248,582, August 26, 2016.

M. Ménard: Proposed the idea. He supervised the work and wrote, edited and reviewed the manuscript.

O. Liboiron-Ladouceur: She supervised the work. She wrote, edited and reviewed the manuscript.

M. S. Hai: He proposed the idea of the low-loss version of the device and the electrical model to reconstruct original data offline. He simulated and experimentally characterized the optical receiver. He wrote the manuscript.

[3] O. Liboiron-Ladouceur, **M. S. Hai**, and M. Moayedi, "Methods and Devices for Photonic M-ARY Pulse Amplitude Modulation," US 14/879,361, Apr. 14, 2016.

O. Liboiron-Ladouceur: She supervised the work. She wrote, edited and reviewed the manuscript.

M. S. Hai: He proposed the idea, simulated the inter-coupling ring modulator and electrical characteristics of the p-n diode, and drew the layout. He experimentally characterized the optical modulator. He wrote the manuscript.

Monireh Moayedi Pour Fard: She simulated the p-n diode phase shifter of the ring modulator and drew the layout. She experimentally characterized the RF response of the electrodes. She wrote the manuscript.

**Patent application not directly related to this thesis:**

[1] O. Liboiron-Ladouceur, **M. S. Hai**, M. Moayedi, C. Zhang, M.N. Sakib, "Methods and Systems for Board Level Photonic bridges," US 14/955,142, June 2, 2016.

**Peer reviewed journal articles related to this thesis:**

[1] **M. S. Hai** and O. Liboiron-Ladouceur, "Low-Loss Passive $Si_3N_4$ Serial-to-WDM Interface for Energy-Efficient Optical Interconnects," *Journal of Lightwave Technology*, in press (2016).

M. S. Hai: Proposed the idea. He drew the layout. He simulated and experimentally characterized the PWSM devices. He wrote the manuscript.

O. Liboiron-Ladouceur: Proposed the idea. She supervised the work. She wrote, edited

and reviewed the manuscript.

[2] **M. S. Hai**, A. Leinse, T. Veenstra, O. Liboiron-Ladouceur, "A Thermally Tunable 1 × 4 Channel Wavelength Demultiplexer Designed on a Low-Loss $Si_3N_4$ Waveguide Platform," *Photonics*, vol. 2, no. 4, pp. 1065–1080, Oct. 2015.

M. S. Hai: Proposed the idea. He drew the layout. He simulated and experimentally characterized the optical demultiplexer. He wrote the manuscript.

A. Leinse, and T. Veenstra: They reviewed the layout of the design and gave useful suggestions about mask design.

O. Liboiron-Ladouceur: Proposed the idea. She supervised the work. She wrote, edited and reviewed the manuscript.

[3] **M. S. Hai**, M. Ménard, O. Liboiron-Ladouceur, "Integrated Optical Deserialiser Time Sampling Based SiGe Photoreceiver," *Optics Express*, vol. 23, no. 25, pp. 31736–31754, Nov. 2015.

M. S. Hai: He proposed the idea of the low-loss version of the device and the electrical model to reconstruct original data offline. He drew the layout. He simulated and experimentally characterized the optical receiver. He wrote the manuscript.

M. Ménard: Proposed the idea. He supervised the work and wrote, edited and reviewed the manuscript.

O. Liboiron-Ladouceur: She supervised the work. She wrote, edited and reviewed the manuscript.

[4] O. Liboiron-Ladouceur, P.G. Raponi, N. Andriolli, I. Cerutti, **M. S. Hai**, and P. Castoldi, "A Scalable Space-Time Multi-Plane Optical Interconnection Network using Energy Efficient Enabling Technologies," *OSA/IEEE Journal of Optical Communication and Networking*, vol. 3, no. 8, Aug. 2011.

O. Liboiron-Ladouceur: Proposed the idea. Supervised the work. She wrote, edited

and reviewed the manuscript.

M. S. Hai: Simulated the theoretical model of the PWSM circuit presented in the paper and wrote part of the manuscript.

**Peer reviewed conference papers related to this thesis:**

[1] **M. S. Hai**, M. Ménard, O. Liboiron-Ladouceur, "A 20 Gb/s SiGe Photoreceiver Based on Optical Time Sampling," in *Proc.* $41^{st}$ *European Conference and Exhibition on Optical Communication (ECOC)*, Sept. 29 2015, paper Tu.1.3.5.

[2] **M. S. Hai** and O. Liboiron-Ladouceur, "Low-loss $Si_3N_4$ Wavelength-striped Multiplexer," in *proc. IEEE Optical Interconnects Conference (OI)*, San Diego, CA, Apr. 2015, paper TuP.16.

**Peer reviewed journal articles not directly related to this thesis:**

[1] **M. S. Hai**, M. Moayedi, and O. Liboiron-Ladouceur, "A Ring-based 25 Gb/s DAC-less PAM-4 Modulator ," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 22, no. 6, pp. 1–8, Nov. 2016.

[2] **M. S. Hai**, M. N. Sakib, and O. Liboiron-Ladouceur, "Monolithic 1 × 2 MMI Based 25 Gb/s SOI DPSK Demodulator Integrated with SiGe Photodetector," *IEEE photonic technology letters*, vol. 27, no. 6, pp. 565–568, Mar. 15, 2015.

[3] B. Banan, **M. S. Hai**, P. Berini, and O. Liboiron-Ladouceur, "Simultaneous High-capacity Optical and Microwave Data Transmission Over Metal Waveguides," *Optics Express*, vol. 23, no. 11, pp. 14135–14147, May 2015.

[4] M. N. Sakib, **M. S. Hai**, and O. Liboiron-Ladouceur, "A Silicon Photonic Integrated

Packaged Coherent Receiver Front-End For Soft-Decision Decoding," *J. Lightwave Technol.*, vol. 32, no. 24, pp. 4151–4156, Dec. 2014.

[5] **M. S. Hai**, M. N. Sakib, and O. Liboiron-Ladouceur, "A 16 GHz Silicon-based Monolithic Balanced Photodetector with On-chip Capacitors for 25 Gbaud Front-end Receivers," *Optics Express*, vol. 21, no. 26, pp. 32680–32689, Dec. 2013.

[6] B. Banan, **M. S. Hai**, E. Lisicka-Skrzek, P. Berini, O. Liboiron-Ladouceur, "Multichannel Transmission Through a Gold Strip Plasmonic Waveguide Embedded in Cytop," *IEEE Photonics Journal*, vol. 5, no. 5, p. 2201811, June 2013.

[7] **M. S. Hai** and O. Liboiron-Ladouceur, "Design of a 50-Gb/s SOI-Based DPSK Demodulator for Dense Photonic Integration," *IEEE Photon. Technol. Lett*, vol. 34, no. 19, pp. 1749–1752, Oct. 2012.

**Peer reviewed conference papers not directly related to this thesis:**

[1] **M. S. Hai**, M. Moayedi, O. Liboiron-Ladouceur, "A Low-voltage PAM-4 SOI Ring-based Modulator," in *Proc. IEEE Photonics Conference (IPC)*, pp. 194–195, paper TuB3.3, Oct. 2014.

[2] **M. S. Hai**, P. Liao, M. Mirshafiei and O. Liboiron-ladouceur, "MZI-based Non-blocking SOI Switches," in *Proc. Asia Communications and Photonics Conference*, paper ATh3A.147, Nov. 2014.

[3] L. R. Chen, R. Adams, R. Ashrafi, J. Wang, M. Rezagholipour Dizaji, **M. S. Hai**, and O. Liboiron-Ladouceur, "Photonic Integrated Circuits for Microwave Photonics Applications," in *Proc. International Topical Meeting on Microwave Photonics/Asia-Pacific Microwave Photonics Conference*, pp. 32–35, Oct. 2014.

[4] **M. S. Hai**, M.N. Sakib, O. Liboiron-Ladouceur, "A Compact Silicon-on-Insulator Op-

tical Hybrid for Low Loss Integration with Balanced Photodetectors," in *Proc.* $39^{th}$ *European Conference and Exhibition on Optical Communication (ECOC)*, paper We.2.B.2, Sept. 2013.

[5] **M. S. Hai** and O. Liboiron-Ladouceur, "Robust and Compact 45 Gb/s MMI-based SOI DPSK Demodulator for On-chip Optical IO Layer," in *Proc. Conference on Lasers and Electro-Optics (CLEO)*, paper JTu4A.28, June 2013.

[6] B. Banan, **M. S. Hai**, E. Lisicka-Skrzek, P. Berini, and O. Liboiron-Ladouceur, "49 Gb/s Optical Transmission through Long-Range Plasmon Polariton Waveguide," in *Proc. IEEE Photonics Conference*, paper TuI3, Oct. 2012.

[7] M. N. Sakib, **M. S. Hai** and O. Liboiron-Ladouceur, "A Monolithic Optical Front-end for Soft-decision LDPC Decoders," in *Proc. SPIE Photonics North*, vol. 8412, Oct. 2012.

[8] O. Liboiron-Ladouceur, M. N. Sakib, M. Sowailem, **M. S. Hai**, R. Varano, and D. Rolston, "Optically Interconnected High-performance Servers," in *Proc. SPIE Photonics North*, vol. 8412, Oct. 2012.

# Contents

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# List of Acronyms

| | |
|---|---|
| ADC | Analogue to digital converter |
| AWG | Arrayed waveguide gratings |
| BER | Bit error rate |
| BPD | Balanced photodetector |
| CMOS | Complementary metal oxide semiconductor |
| CMRR | Common mode rejection ratio |
| CW | Continuous wave |
| DAC | Digital to analog converter |
| DBR | Distributed Bragg reflector |
| DCA | Digital communication analyzer |
| DFB | Distributed feedback laser |
| DOM | Dynamic offset modulation |
| DRC | Design rule check |
| DSP | Digital signal processing |
| DUT | Device under test |
| EDFA | Erbium doped fiber amplifier |
| EO | Electro-optic |
| FDL | Fiber delay line |

| | |
|---|---|
| FDTD | Finite difference time domain |
| FEC | Forward error correction |
| FIR | Finite impulse response |
| FSR | Free spectral range |
| GC | Grating coupler |
| GVD | Group velocity dispersion |
| IMDD | Intensity-modulated/direct-detection |
| ISI | Inter symbol interference |
| LA | Limiting amplifier |
| LSB | Least significant bit |
| LSI | Large-scale integration |
| MIM | Metal insulator metal |
| MMF | Multimode fiber |
| MMI | Multimode interference coupler |
| MSB | Most significant bit |
| MUX | Multiplexer |
| MZI | Mach-Zehnder interferometer |
| MZM | Mach-Zehnder modulator |
| NF | Noise figure |
| NIC | Network interface card |
| NoC | Network on Chip |
| NRZ | Non-return-to-zero |
| ODL | Optical delay line |
| OOK | On-off keying |

| | |
|---|---|
| OSA | Optical spectrum analyzer |
| OSNR | Optical signal-to-noise ratio |
| PAM | Pulse amplitude modulation |
| PC | Polarization controller |
| PCB | Printed circuit board |
| PD | Photodetector |
| PECVD | Plasma enhanced chemical vapor deposition |
| PIC | Photonic integrated circuit |
| PPG | Pulse pattern generator |
| PRBS | Pseudorandom binary sequence |
| PWSM | Passive wavelength-striped mapping |
| QAM | Quadrature amplitude modulation |
| RF | Radio frequency |
| RZ | Return-to-zero |
| SerDes | Serializer-deserializer |
| SiGe | Germanium on Silicon |
| SiP | Silicon photonics |
| Si-TWPDA | Si-Ge traveling wave PD array |
| SOA | Semiconductor optical amplifier |
| SOI | Silicon on insulator |
| SMF | Single mode fiber |
| STIA | Space-time interconnection architecture |
| TDM | Time division multiplexing |
| TIA | Trans-impedance amplifier |

| | |
|---|---|
| TOR | Top-of-rack |
| VCSEL | Vertical-cavity surface-emitting laser |
| VOA | Variable optical attenuator |
| WDM | Wavelength division multiplexing |
| WS | Wavelength-striped |

# Chapter 1

# Introduction

## 1.1 Optical interconnect for short-reach data communication

Optical fiber-based lightwave systems are commercially used in the long-haul communication link which operates over bit rates exceeding Tb/s scale. In a research laboratory, for example, transmission of 96 $\times$ 100 Gb/s PDM-RZ-QPSK channels over 10,610 km path was demonstrated [1]. However, the recent boom in the number of Internet service applications and cloud computing imposes higher bandwidth demand on long-haul networks as well as on short-reach networks between server boards, servers to switch (2 m) and switch connections between the buildings (2 km) [2]. The increasing number of servers in the data centers also puts tight constraints on the networking infrastructure. To scale the short-reach interconnects beyond 10 Gb/s or 100 Gb/s, traditional electrical I/Os (input/output) for such high bandwidth would require complex circuits for SerDes, equalization, and noise cancellation, due to their large RC delay, latency and jitter. Therefore, short-reach interconnect is becoming a bottleneck for next-generation communication links between the computer servers or data centers.

The inherent bandwidth limitation of electronic interconnects can be overcome by using optical components in the interconnects. It is already demonstrated that communication between the servers through exchange of specific time length data packets is benefited by the optical interconnect which offers large bandwidth, low-loss and low crosstalk [3–7]. However, traditional silica fibers cannot be used to build compact PIC, as they exhibit high propagation losses with low bending radius (at large bending radius, propagation loss of the single mode silica fiber is as low as 0.2 dB/km). Bulk-fiber-based components are not suitable for short-reach optical I/O. On the other hand, application of low-loss passive PICs in optical interconnects can also reduce power consumption in the network. Therefore, to evolve optics from long-haul communication to short-reach interconnects between the data center servers, innovation in compact PIC and optical packaging is necessary [2].

InP based PICs have been deployed commercially and those PICs have been part of the roadmap in terms of the increasing number of photonic components integrated on a chip. For example, Infinera Inc. has demonstrated InP based PIC with more than 1,700 photonic components on the same chip [8]. InP based PICs have shown an exponential increase in the number of components integrated on the chip for the last two decades, Fig. 1.1 [9]. Availability of the on-chip laser source facilitates the growth of InP based PIC market. Silicon photonics based PICs are also investigated due to the high yield, low production cost and their potential to increase the component density on-chip. However, silicon is an indirect band gap material and therefore efficient on-chip silicon laser is unavailable. Heterogeneous integration of III-V lasers on silicon is complex and costly, which is slowing down the commercial deployment of silicon photonics based PICs. Although reliable and cost effective electrically pumped continuous-wave InAs/GaAs quantum dot laser directly grown on silicon substrate has recently been demonstrated in [10].

InP has better optical properties compared to silicon, however, silicon photonics has

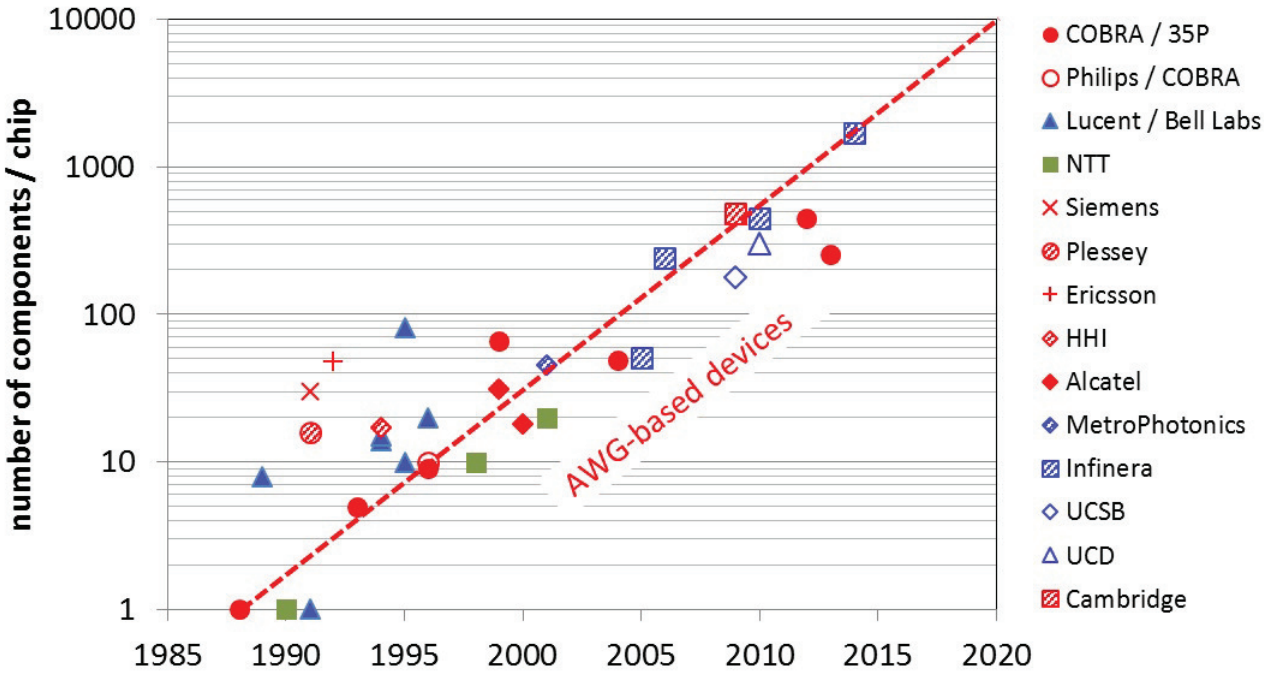



**Fig. 1.1** Increase in the number of photonic components on a single InP chip over the years [9].

some other advantages that InP waveguide platform does not offer. For example, InP has larger temperature dependent linear expansion coefficient compared to silicon ($5\times10^{-6}$ $K^{-1}$ vs $2.5\times10^{-6}$ $K^{-1}$ at $30^0$C). In addition to this, mechanical properties of silicon is much better than InP, allowing larger wafers in silicon photonics platform (300 mm in silicon vs 75 mm in InP) [11]. InP modulators are more temperature sensitive compared to silicon modulators. The quantum-confined Stark effect based InP modulators are inherently temperature sensitive due to the band edge movement with temperature. On the other hand, in silicon photonics based modulators optical phase shift is achieved through the change in the effective index of the waveguide by electrical carrier injection or depletion, which is a less temperature dependent phenomenon. Table 1.1 shows (taken from [11]) the pros

and cons of InP and silicon photonics based PICs. This table demonstrates that both technologies should be investigated to meet the specific types of demands (*i.e.*, on-chip laser, bandwidth, cost, yield, reliability) for short reach interconnects or long haul optical network components.

**Table 1.1** The pros and cons of InP and silicon photonics waveguide platform [11]

| InP | Si |
|---|---|
| Expensive material | Cheap material |
| • In is scarce | • 27% mass Earth's crust is Si |
| Medium yield | High yield |
| • W.g. material from epitaxy | • W.g. material from original boule |
| Small footprint | Extremely small footprint |
| • High index contrast in 1D | • High index contrast in 2D |
| Native laser | No native laser |
| Poor native oxide | Excellent native oxide |
| Low dark current | Medium dark current |
| Small wafers (75 mm typ.) | Large wafers (300 mm typ.) |
| • 75 mm typical | • 300 mm typical |
| • Brittle material | • Strong material |
| Modulator temperature sensitive | Modulator temperature insensitive |
| • Band edge moves with temperature | • Carrier density not v. temp. dep. |

## 1.2 Review of short-reach optical interconnect technologies

Short-reach optical communication links are generally required in the intra-data center network for connecting the boards and racks between the large capacity computational servers or nodes. In a large data center network, as the traffic scales, meeting the bandwidth demand for the intra-data center network becomes more critical compared to the long-haul communication network, as most of the data route within the same data center network. For example, Cisco Systems, Inc. forecasted that, by 2019, 83% of the data center traffic data will come from cloud services and applications, and 73% of the data center traffic will come from or route within the data center [12]. Therefore short-reach optical links are necessary to scale the bandwidth capacity of the data center networks. The required length of the short-reach interconnect in data centers at present typically ranges from 2 km to 40 km.

Multimode fiber-based short-reach links employing directly modulated VCSEL are deployed commercially. In multimode fiber-based optical links, discrete optical components such as VCSEL, optical filter, photodetectors (PD) are used. Fig. 1.2 shows an illustration of the optical interconnect system for board-to-board and rack-to-rack communication [13]. As illustrated in the figure, the electrical circuit boards are built in a rack and connected to the backplane. The backplane contains both the multimode optical fibers and electrical wires. Two important optical components on the boards are VCSELs and photodetectors for electrical-to-optical (E/O) and optical-to-electrical (O/E) conversion, respectively. The electrical wires are used to transmit the high speed ($\sim$5 Gb/s to $\sim$20 Gb/s) electrical signal for modulating the VCSELs and receiving the photodetected signals. Short length electrical wires are used between the large-scale integration (LSI) electronic chips to prevent signal distortion. Finally, the boards and racks are connected by the multimode fibers.

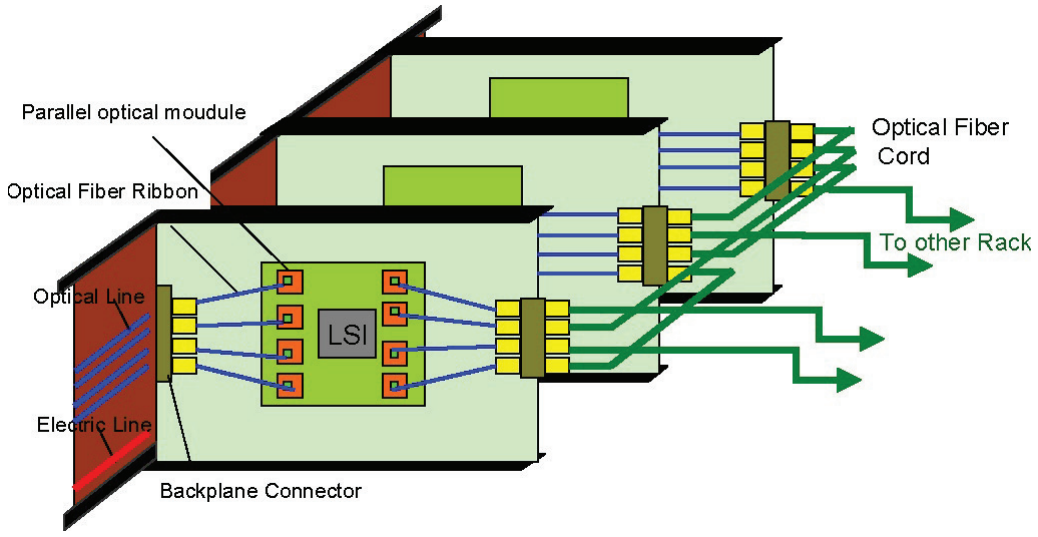



**Fig. 1.2** Optical interconnect between board-to-board and rack-to-rack modules of computational servers [13].

VCSELs and PD-array-based short-reach optical interconnects have been demonstrated with aggregated bandwidth from 240 Gb/s (20 × 12 channels) [14,15] to 480 Gb/s (10 × 48 channels) [16, 17]. VCSEL based optical links are cheaper compared to the PIC-based links, as the latter generally require complex off-chip or on-chip integration of the laser on the PIC. However, VCSELs over the multimode fiber (MMF) link has low bandwidth-distance product of 2 GHz-km due to the modal and chromatic dispersion in the MMFs. This limits the length of the VCSEL-MMF based short-reach optical links to 100 m in a 25 Gb/s link [11]. Therefore, several optical waveguide technologies such as InP, silicon photonics, $Si_3N_4$ are being investigated to build different components of the short-reach optical interconnect network. The goal is to externally modulate the CW signal generated from the laser by using an InP or silicon photonics based modulator. The modulated signal can be transmitted by a single mode (SM) fiber over the distance required in the short-reach optical interconnect, *i.e.* from 2 km to 40 km.

Silicon photonic based 100 Gb/s coherent transceivers have been demonstrated in ref. [18] by Acacia Communications, NJ, USA, where eight modulators and eight photodetectors are designed on the same chip along with the passive components such as phase-shifter, multimode interference coupler, and polarization beam splitter/rotator. The chip was characterized using an off-chip laser source, which generates the CW signal. On the other hand, a 40 channel $\times$ 57 Gb/s InP-based coherent transceiver is demonstrated by Infinera [8]. The monolithically integrated chip has 40 tunable distributed feedback (DFB) lasers along with the modulators, variable optical attenuators and optical multiplexers. While coherent transceivers are more suitable for long-haul optical networks, direct-modulation-based transceivers have also been demonstrated on both the silicon photonics and InP platforms for short-reach applications. For example, Luxtera demonstrated a 4 channel $\times$ 26 Gb/s optical transceiver, with integrated silicon Mach-Zehnder modulators (MZM) and SiGe photodetectors on the same chip in ref. [19]. The chip contains a DFB laser, a lens, an optical isolator, and a turning mirror in a small hermetic assembly on top of the PIC, Fig. 1.3. The electronic IC (containing the modulator driver, transimpedance amplifiers) is wire bonded to the photonic chip.

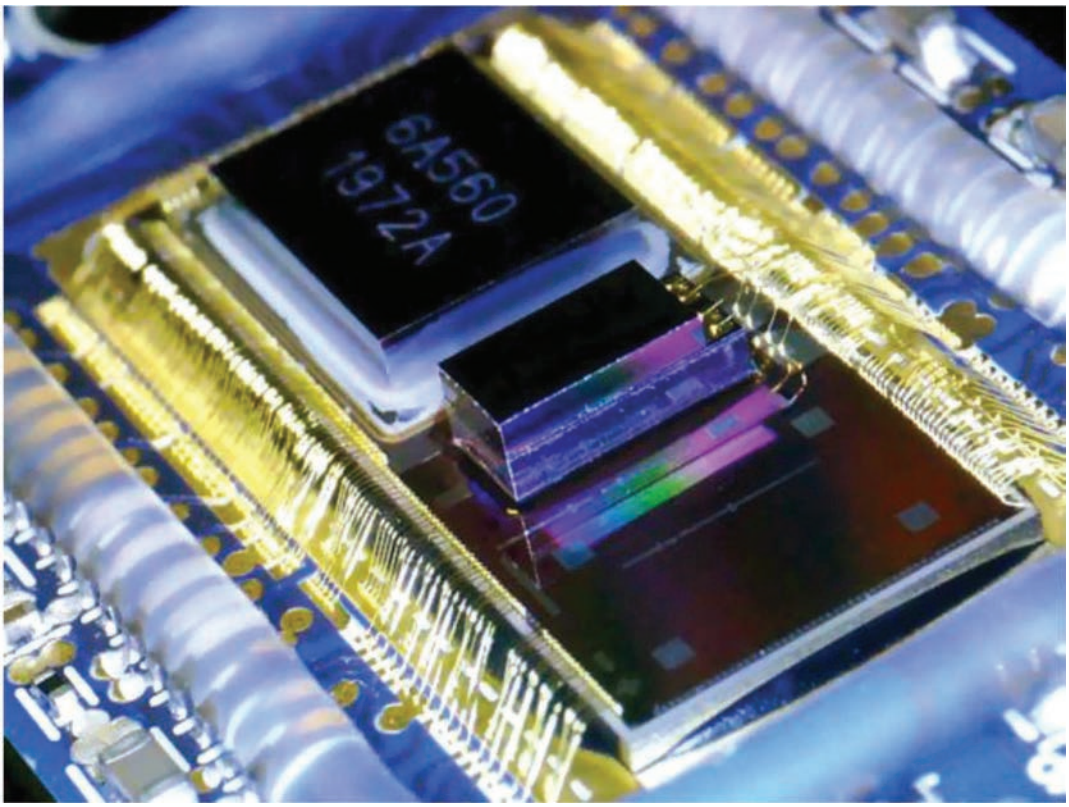



**Fig. 1.3** A silicon photonic chip containing 4 × 26 Gbps transceiver is wire bonded to the electronic IC. The CW laser is flip-chip bonded to the photonic IC [19].

In ref. [20], an eight-channel monolithically integrated multiwavelength transmitter is demonstrated by the photonic integration group of Eindhoven University of Technology (TU/e), Eindhoven, The Netherlands, where an array of eight distributed Bragg reflector (DBR) laser is integrated with the MZMs, Fig. 1.4. The modulation data rate per MZM is 12.5 Gb/s. In [20], the modulated optical signals from the MZM's are multiplexed using the arrayed waveguide grating (AWG) multiplexer.

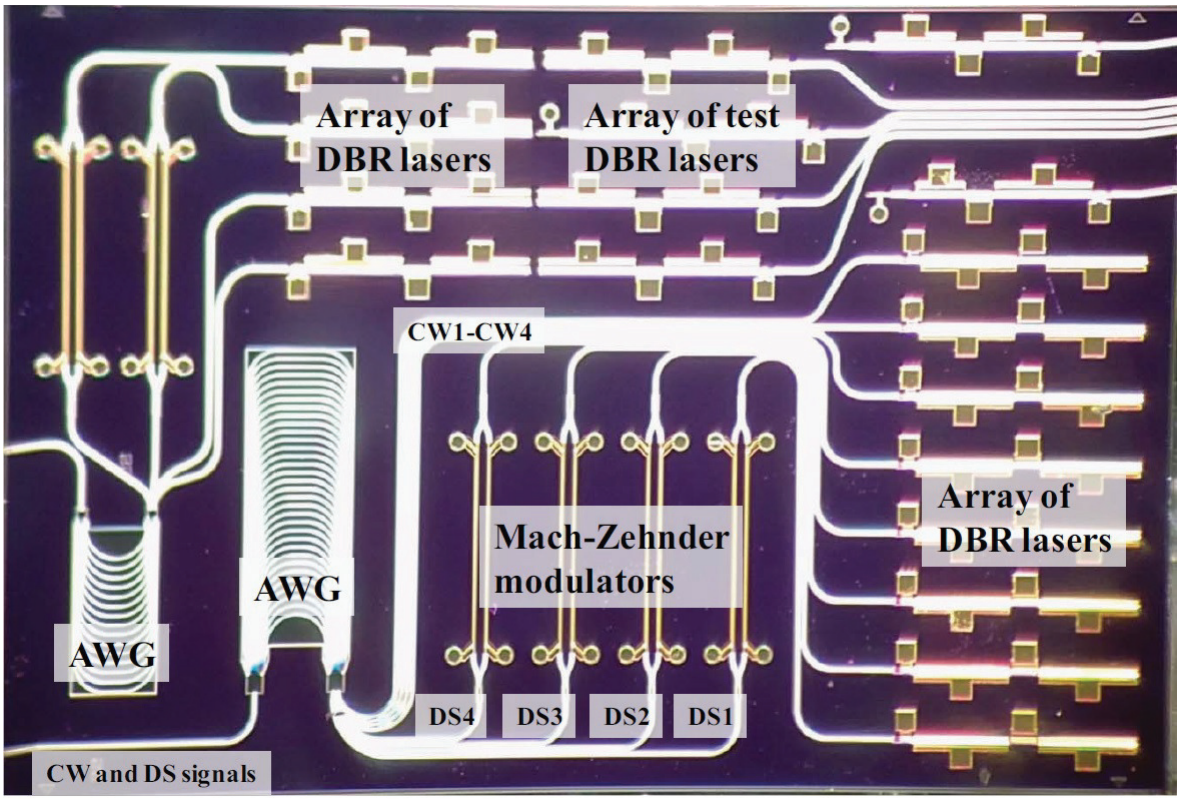



**Fig. 1.4** Photograph of the 4 mm × 6 mm area InP circuit with modulators, lasers, and AWGs [20].

The requirement of having a low propagation loss waveguide is another important criterion to build short-reach optical interconnects with complex signal processing functionalities. Typical InP and SOI waveguides exhibit reasonable propagation losses of 0.5∼1.5 dB/cm [21] and 2∼3.5 dB/cm [22, 23], respectively, at a low bending radius (as low as 10 $\mu$m for SOI waveguides), which justifies their application in building compact photonic components. Hybrid integration of InP photonic components on SOI waveguides (silicon photonics) has also been demonstrated [24]. The hybrid integration of these two types of photonic components promises the availability of compact photonic I/O for next

generation servers and data centers. Besides the advancement in photonic integration technology, several promising all-optical packet-routing schemes have been proposed [25, 26] (although not deployed yet), which require an optical buffer circuit to avoid packet congestion and contention. Buffering of optical packets requires memory or storage, which is easily achievable in electronics through memory devices such as RAM, but difficult to achieve in PICs. The propagation loss of both InP and silicon waveguides limits their applications in designing long optical time delays, which is an important requirement in some optical switching and buffering circuits. Material absorption and side-surface scattering loss are the main contributors to the propagation loss in the InP and silicon waveguides, respectively.

Recently, ultra low-loss $Si_3N_4$ waveguides have been demonstrated that exhibit propagation loss from 3 dB/m [27] to as low as 0.1 dB/m [28]. Propagation loss is reduced to 0.1 dB/m in $Si_3N_4$ waveguide by increasing the bending radius ($\sim$10 mm) and by using thermally grown silicon dioxide layer as a wafer-bonded top cladding structure. Detailed method to design the low propagation loss $Si_3N_4$ waveguide is presented in [27]. In a relatively high index contrast $Si_3N_4$ waveguide, where the core waveguide and silica cladding have refractive index of 1.99 and 1.45, respectively, sidewall scattering is the primary contributor to the overall waveguide propagation loss. To reduce the sidewall scattering loss a high-aspect-ratio core waveguide geometry is used, where the width of the waveguide is made larger than the thickness of the waveguide. For example, in this work, the cross section geometry of the $Si_3N_4$ waveguide is 72 nm $\times$ 2.8 $\mu$m. In a high-aspect-ratio core waveguide, optical mode is more confined to the top/bottom surface of the waveguide compared to the sidewalls. As for planar waveguides, roughness in the top/bottom surface is much less compared to the sidewalls, higher mode confinement in the top/bottom surface of the waveguide results into low propagation loss. Fig. 1.5 shows the propagation of visible

red light through a 1 m long $Si_3N_4$ waveguide, demonstrated in [28]. The ultra low-loss $Si_3N_4$ waveguide can be used to design PICs with complex optical signal processing capabilities, *i.e.*, AWGs, optical gyroscopes, optical buffers and as demonstrated in this thesis, PWSM devices with long optical delay lines or optical buffers.

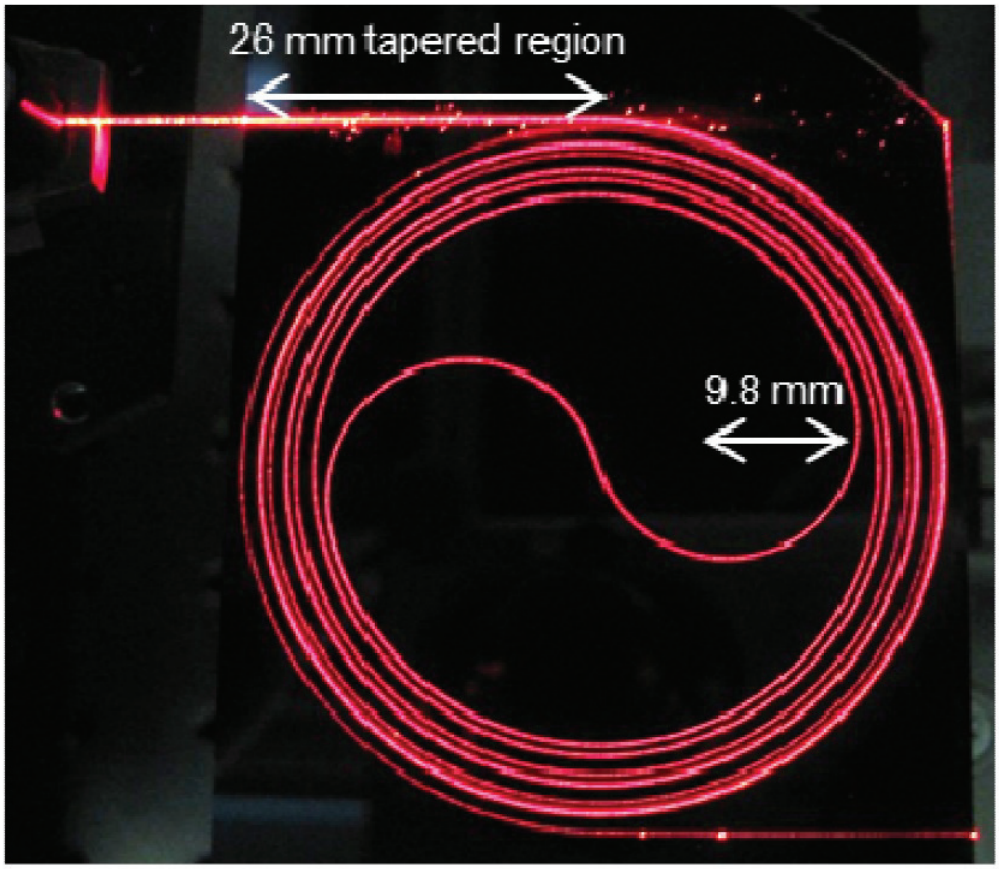



**Fig. 1.5** Visible red light propagation in a 1 m long $Si_3N_4$ waveguide with plasma-enhanced chemical vapor deposition (PECVD) oxide top cladding [28].

On the low-loss $Si_3N_4$ waveguide platform, integration of active lasers, modulators or photodetectors have not been demonstrated so far. The silicon photonics platform, on the other hand, with its compatibility with CMOS electronic fabrication process, offers

low-cost integration of photonic components on SOI platform with high yield. Integration of a laser [10], modulator, and photodetector [29] on the silicon waveguide have already been demonstrated. Silicon-based waveguide technology (both silicon and $Si_3N_4$ waveguide) promises complex and high-density integration of passive devices such as filters, optical buffers, polarization beam splitters on the same substrate [30]. Therefore, in a heterogeneous integration platform, silicon waveguides can be used for integrating active components and compact waveguide routing. On the other hand, $Si_3N_4$ waveguides can be used in the PIC sections where low-loss optical delay lines are required. Integration of a silicon photonics waveguide with the low-loss $Si_3N_4$ waveguide platform has been demonstrated in ref. [31], which paves the way for integrating a hybrid silicon laser and silicon photodetectors with the ultra low-loss $Si_3N_4$ waveguide. In ref. [31], before integrating the silicon layer, the $Si_3N_4$ waveguides are annealed at $> 1050^0$C. Next, the silicon waveguide on the SOI substrate is transferred to the top of the low-loss $Si_3N_4$ waveguide via oxide-to-oxide bonding. Fig. 1.6 shows the schematic view of the silicon-$Si_3N_4$ waveguide integration platform [31].

## 1.3 Recent progress in the PIC based optical components

In this thesis, we investigate the design method of two PICs that implements on-chip optical buffering and optical time sampling for increasing the bandwidth capacity of short-reach optical interconnects. Essentially the two most important photonic modules on a PIC are modulators (for E/O conversion) and photodetectors (for O/E conversion). However, recent progress in the PIC-based technologies motivates researchers to implement optical modules with more on-chip functionality, such as a traveling wave modulator [32, 33], a PAM-16 modulator [34], a coherent optical transmitter-receiver [35], an optical gyroscope [36], an

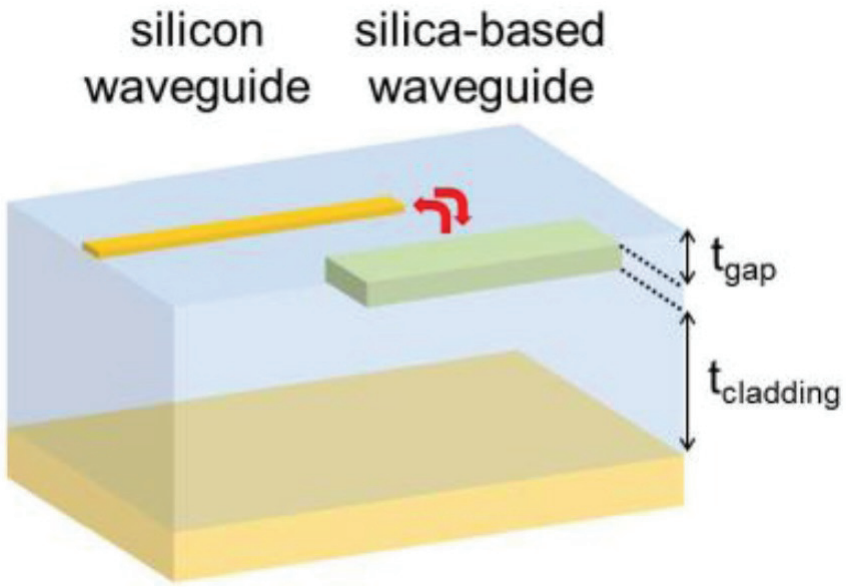



**Fig. 1.6** Schematic view of the silicon and low-loss $Si_3N_4$ waveguide integration platform [31].

AWG [37], a traveling wave photodetector [38], and a self-equalizing photodetector [39]. Progress in the PIC-based technology includes waveguides with low bending radius and active implant layers (*i.e.*, silicon waveguides) and with ultra-low propagation loss (*i.e.*, $Si_3N_4$ waveguides). Therefore, researchers in the field of photonics are investigating the possibility of transferring some of the power hungry signal processing functionality of an interconnect from the electronic domain to the optical domain. Next, we give examples of three recent works where PICs with such functionalities have been demonstrated.

### 1.3.1 Pulse amplitude modulation (PAM) in silicon photonics

An intensity-modulated / direct-detection (IM/DD) based optical communication link is a promising low-cost solution to build a 100 Gb/s/$\lambda$ data rate interconnect within data centers [40]. To further enhance the capacity of the optical interconnect, advanced modulation-

format-based MZM on a silicon photonic platform offers the possibility of designing power efficient, low-cost and integrated IM/DD networks. In ref. [34], for example, the first 20 Gb/s PAM-4 and PAM-16 silicon photonic modulators were proposed, where a multilevel optical modulated signal is generated using the segmented electrode based MZM. Fig. 1.7(a) and Fig. 1.7(b) shows the structure of the segmented electrode modulator and the generated PAM-4/PAM-16 eye diagrams, respectively [34]. Each arm of the MZM contains varying length electrode segments such that when driven by a different RF driving signal of equal amplitude, a multilevel optical modulated signal (PAM-4 for two segment and PAM-16 for four segment electrode) is generated at the output of the modulator. The segmented photonic modulator eliminates the need for an electronic digital-to-analog converter (DAC), from the optical interconnect, which simplifies the design and reduces the operational cost of the transmitter. For example, a 3 bit DAC with a 3.2 V output swing consumes 2 W of electrical power [41]. On the other hand, the segmented electrode based quadrature amplitude modulation (QAM-16) MZM transmitter with the electronic driver circuit demonstrated in [42] consumes 1 W of power. Fabrication of the $p$ and $n$-doped implant regions on the silicon waveguide facilitates designing segmented electrode based MZMs.

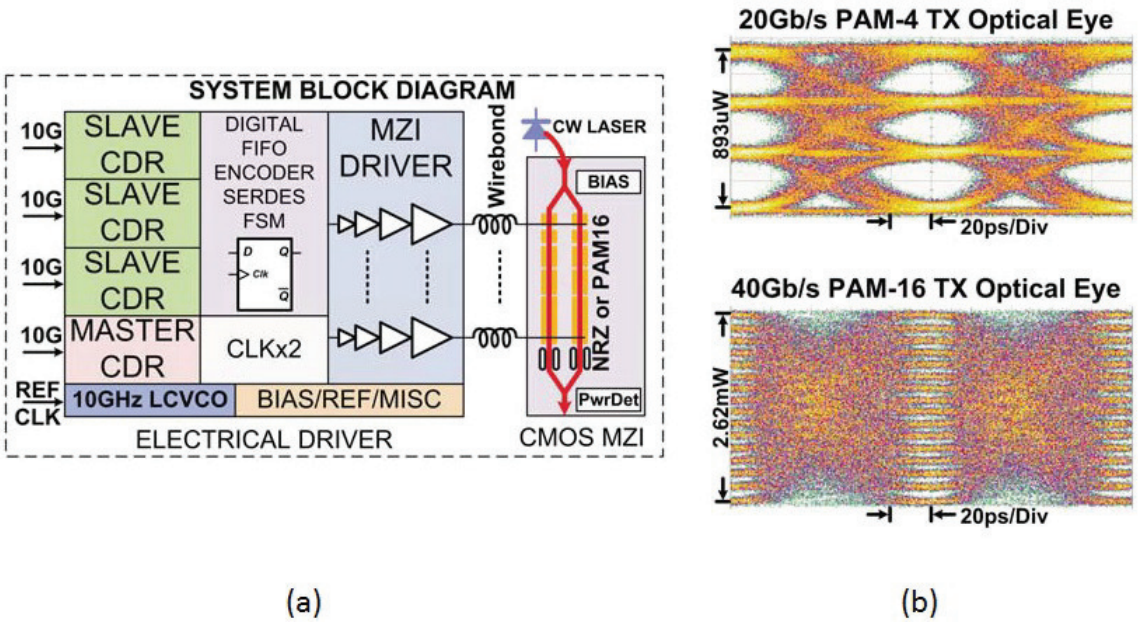



**Fig. 1.7** (a) Schematic of the segmented modulator and the test circuit, (b) generated PAM-4 and PAM-16 optical eye diagram [34].

### 1.3.2 Traveling wave photodetectors in silicon photonics

An integrated photodetector is another important photonic module for short-reach optical interconnects. High bandwidth and linear photodetectors are required in an interconnect to design the photoreceivers with low BER performance. To increase the bandwidth of the photodetector, designers keep the length of the active absorption region of the photodetector small with the aim to decrease the capacitance and carrier transit time of the photodetector. However, a small-sized photodetector has low optical power handling capability, which saturates the photocurrent at high optical power and thus reduces the linearity of the photodetector. To break this bandwidth-linearity trade-off of the photodetector, a traveling-wave-based photodetector array has been proposed and designed on both InP

and silicon photonics platforms [38, 43]. In a traveling-wave photodetector array, incoming optical signal power is equally distributed to four or more paths by using the directional or MMI couplers and the optical signal is converted to an electrical signal using a PD array and a traveling wave electrode, Fig. 1.8 [38]. Optical delay lines are used in a complementary way to offset the phase delay mismatch of the traveling wave electrode. Indeed, the availability of the compact waveguide routing and traveling wave electrode on PIC, facilitates incorporating this phase matching feature in the photodetector array. This example demonstrates another case where the conventional O/E conversion process in the photoreceiver circuit can be enhanced by using the present state-of-art PIC technology.

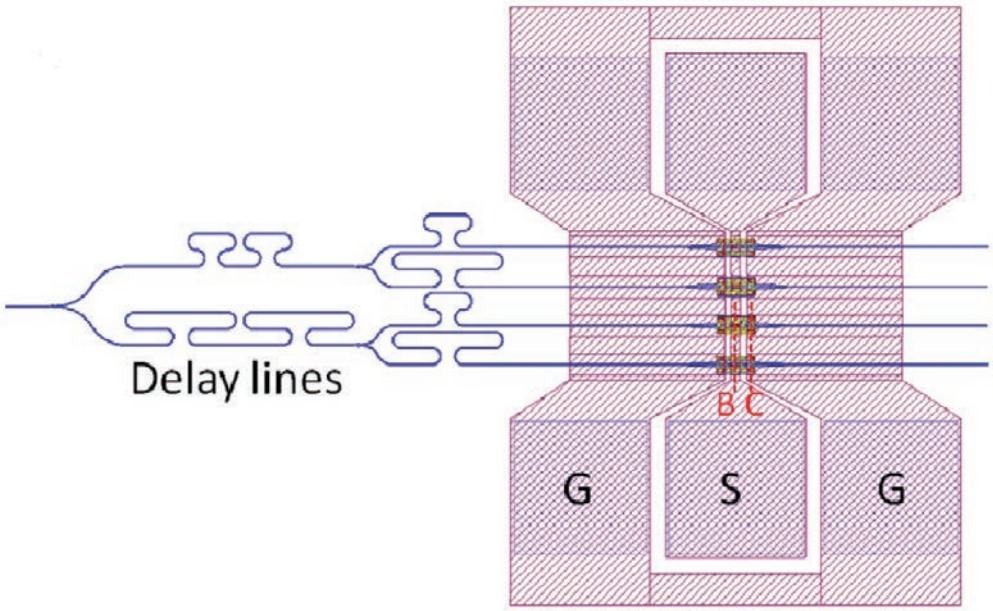



**Fig. 1.8** Layout of the 4-channel traveling wave PD array, where the power of the incoming optical signal is distributed to four paths using MMI splitter. Optical delay lines were used in complement to offset the electrical phase delay in the traveling wave electrode. GSG: ground-signal-ground pads [38].

### 1.3.3 Low-loss $Si_3N_4$ waveguide integrated with III-V photodetectors

Ultra low-loss $Si_3N_4$ waveguides have been demonstrated in [27, 28, 44]. Availability of the $Si_3N_4$ waveguide on PIC paves the way to monolithic integration of low-loss photonic components with III-V active components, such as photodetectors [45]. In [45], a 0.85 dB insertion loss AWG is integrated with eight photodetectors, Fig. 1.9. The $Si_3N_4$ waveguides were fabricated on the silicon substrate and the III-V wafer was wafer-bonded to the silicon layer. The photodetectors were designed on the III-V wafer. This heterogeneous integration technology opens the possibility of designing more complex PICs where, optical buffering can be performed by the passive low-loss $Si_3N_4$ waveguides and O/E or E/O conversion process can be done using the active silicon or III-V components.

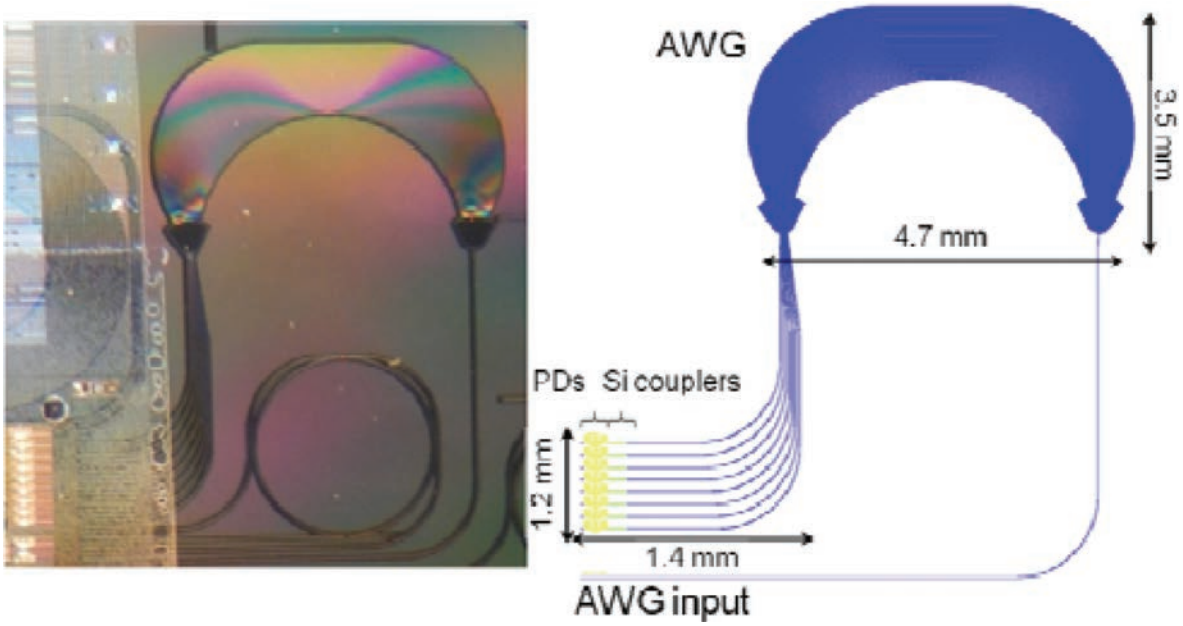



**Fig. 1.9** Schematic and layout of the AWG integrated with the III-V photodetectors [45].

## 1.4 Background on wavelength-striped techniques in optical interconnections

The recent Internet traffic growth demands important data processing capabilities in the modern data centers hosting large number of computational servers. Hence, the type of interconnection network between the servers is a major concern to meet the increasing network traffic. Optical interconnection between servers can enhance network scalability and data processing by exploiting space, time, and wavelength domains [46]. To further address the scalability challenge, server throughput incremental techniques have been implemented based on dynamically changing data traffic patterns between interconnected servers [47,48]. To fully exploit the optical domain parallelism and tremendous bandwidth, electrical data must be aggregated. However, high-speed electronic serial-to-parallel and parallel-to-serial data conversion in the time domain becomes more complex to design and more power demanding as capacity increases. For example, recently demonstrated 56 Gb/s PAM-4 transceiver based serializer-deserializer (SerDes) designed in the 40 nm CMOS technology node dissipates 710 mW electrical power (transmitter: 290 mW and receiver: 420 mW, [49]). On the other hand, a comparatively low bandwidth 25 Gb/s PAM-4 transmitter dissipates 101.8 mW [50] and 22 Gb/s PAM-4 receiver dissipates 228 mW power [51]. Indeed, scalable processing capacity and interconnectivity between the servers has an important impact on the overall power consumption of modern computational platforms where serializing and de-serializing data constitutes an increased portion of the overall operating cost [52].

Optical wavelength-striping has been shown to be a technique to overcome some of the scalability and power consumption limitations [53–60]. Similar to a WDM communication link, in the wavelength-striping method, information bits of a channel are encoded onto

the optical wavelength channels. Therefore, optical domain parallelism is maintained as in a WDM link, by multiplexing different wavelength channels. However, in contrast to the traditional WDM method, in the wavelength-striping approach, different data segments of a single channel are spread across multiple wavelengths.

A novel PWSM process was demonstrated by Liboiron-Ladouceur *et al.* in [61], where the serial data stream of a packet is encoded onto multiple WDM channels. The PWSM process requires one modulator for all the four or eight WDM channels in the system, and thus decouples the static power dissipation in the interconnect from bandwidth utilization. A theoretical model of the integrated PWSM device on a low-loss waveguide platform has been proposed and characterized in [46]. An integrated PWSM device replaces the bulk fiber-based delay lines required to implement the fixed time delay between the adjacent WDM channels [61]. A compact PWSM device integrated with the thermal heaters is necessary for the reliable and robust application of PWSM process in the optical interconnect. In this work, we have designed the MZI filter based four channel PWSM device on the low-loss $Si_3N_4$ platform.

## 1.5 Recent progress in the integrated photoreceiver technology

In optical communication links, a photodetector (PD) is a key building block in the receiver front-end. Moreover, in most commercial photoreceivers a transimpedance amplifier (TIA) is required to amplify the received electrical bits as well as to convert the photocurrent into a voltage.

Germanium-based photodetectors on a Silicon-on-Insulator (SOI) substrate are promising candidates toward silicon photonic integration because of their high bandwidth (31 GHz, [62]) and possible low cost integration with electronics [63,64]. However, due to the low responsivity

of the SiGe photodetector (0.7 to 1 A/W), the peak to peak voltage at the output of the photodetector is limited 10 to 20 mV, assuming 50 Ω termination. The low peak to peak voltage at the output of the SiGe PD degrades sensitivity of the overall photoreceiver. Therefore, a TIA is generally used before the limiting amplifier (LA) stage of the photoreceiver to increase the voltage amplitude swing. For example, in [63] a $1\times10^{-12}$ BER sensitivity of -11.9 dBm and -7.3 dBm are achieved at 10 Gb/s and 28 Gb/s data rate, respectively, where a SiGe PD is wirebonded to the TIA-LA circuit, Fig. 1.10. At optical input power of -11.9 dBm and -7.3 dBm, generated photocurrent from the PD is 65 $\mu$A and 186 $\mu$A, respectively. Using a 150 Ω transimpedance gain of the TIA, the peak to peak input electrical signal swing to the LA stage was increased to 10 $mV_{pp}$ (at 10 Gb/s) and 28 $mV_{pp}$ (at 28 Gb/s). As the data rate of the input optical signal is further increased to 40 Gb/s, the peak to peak electrical signal voltage is increased to 150 mV by degrading the BER sensitivity of the photoreceiver to -0.6 dBm. Therefore, the required peak to peak voltage from the PD and TIA combination varies from 10 mV to 150 mV as the data rate increased from 10 Gb/sec to 40 Gb/sec.

As described in the previous section, to achieve higher data rate such as 28 Gb/s or 40 Gb/s, a large gain-bandwidth TIA is required which increases the power consumption and design complexity of the photoreceiver. Also one important limitation in photoreceivers is the bandwidth mismatch between the PD and the electronic TIA circuit. For example, whereas the bandwidth of Ge-on-SOI PD can be extended with inductive gain up to 60 GHz [65], a suitable TIA with such bandwidth remains challenging. While the low bandwidth of the TIAs helps remove some high frequency noise, if it is too low it causes intersymbol interference (ISI), which severely degrades the BER performance of the receiver. In [66], a TIA less photoreceiver is demonstrated where a photodetector emulator of responsivity 1 A/W (similar to a SiGe photdetector) is wire bonded to the post processing electrical

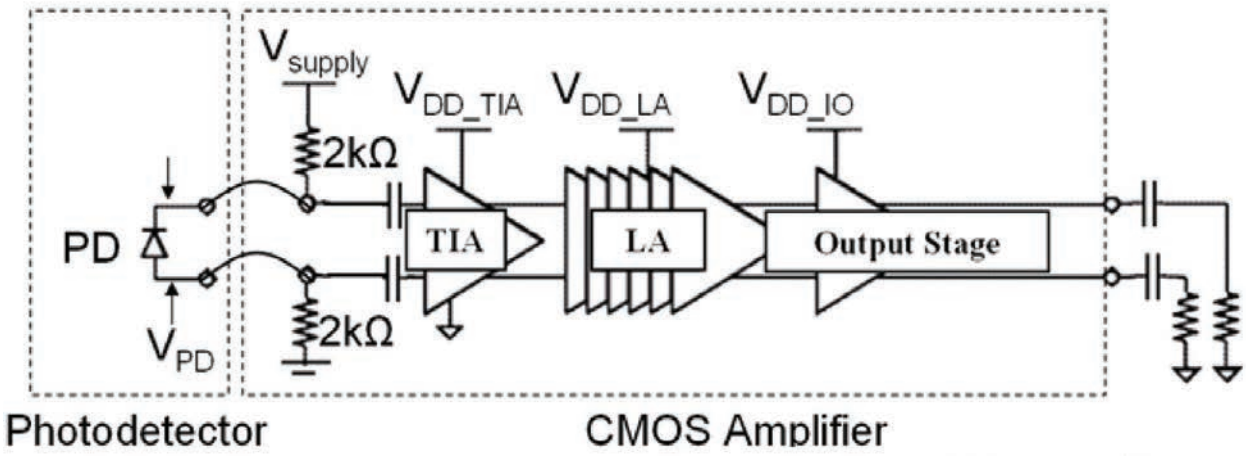



**Fig. 1.10** Schematic of the CMOS receiver amplifer consisting of a trans-impedance amplifier (TIA) followed by a six-stage limiting amplifier (LA) and a current-mode logic output stage (OS) buffer [63].

circuit. The voltage sensitivity of the TIA less electronic receiver is only 13 mV at 20 Gb/s and 17 mV at 24 Gb/sec. The voltage sensitivity of the electronic circuit is improved due to the integrating electrical front-end where the input time constant (RC) is set much larger than the one bit period. The voltage across the PD resistance is generated by integrating the photocurrent by the passive RC circuit. The integrated received bits are then resolved using a low bandwidth double sampling circuit. The photoreceiver achieved an optical sensitivity of -4.7 dBm at 24 Gb/s.

Another interesting application is enabling the high power handling capability in Ge-on-SOI PDs while maintaining their linearity [38], as mentioned in section 1.3.2. Indeed in [38], optical waveguide delay lines are used to balance the electrical phase delay of the electrode to design a Si-Ge traveling-wave PD array (Si-TWPDA). Four PDs are used to design a parallel-fed traveling-wave photodetector array, which increases the power handing capability as well as the linearity of the photoreceiver (optical input saturation power of 160 mW with a 65 mA output photocurrent). These demonstrate the benefits of developing new

design methods either electronically or optically to overcome the responsivity-bandwidth trade-off of photoreceivers.

We demonstrate a novel time sampling based SiGe photoreceiver in this thesis, by leveraging the benefit of having compact, low-loss delay waveguides in SOI technology. The photoreceiver paves the way to integrate high speed photodetectors with low bandwidth post-electronic circuits.

## 1.6 Thesis scope

In this thesis, we have designed two PICs in $Si_3N_4$ and silicon photonics waveguide technology. The passive wavelength-striping mapping method is demonstrated on a $Si_3N_4$ waveguide based PIC. On the other hand, directional couplers, delay waveguides and SiGe photodetectors designed on a silicon photonics platform are utilized to implement the optical deserialiser time sampling based photoreceiver.

The novel PWSM method is demonstrated in [61], where a single data packet is spread across multiple wavelength channels for efficient broadcasting of a channel to multiple destination nodes. In this approach, serial-to-parallel conversion of a data packet is required to compress the data packet in time domain. In the serial-to-parallel conversion process, continuous segments of the data packet share a same time slot over four or eight different wavelength division multiplexing (WDM) channels. At the receiver-end, the parallel-to-serial conversion or time expansion is performed to reconstruct the whole data packet in time domain. As bandwidth of a traditional WDM optical front-end is much higher compared to an electronic interface, implementing the serial-to-parallel and parallel-to-serial process in optical domain simplifies the design and increases the bandwidth capacity of the interface. The PWSM method demonstrated in [61], has been achieved using the

discrete fiber-based components. In this thesis, to the best of our knowledge, for the first time, a compact and integrated PWSM interface on PIC is proposed and experimentally demonstrated.

In addition to this, we have demonstrated an optical time sampling based photoreceiver that consists of a 1 × 4 PD array in a series architecture. We show that by using the correlation property between the four PD channels, it is possible to electronically process the photodetected signals at a quarter of the data rate to recover the original signal.

Following is a list of the goals set in this thesis:

- Explaining the passive wavelength-striping concept for designing a serial-to-WDM optical interface.
- Developing an integrated PWSM interface on the low-loss $Si_3N_4$ waveguide platform.
- Integration of the thermal heaters on the PWSM interface to tune the optical demultiplexer section of the circuit.
- Designing a novel photoreceiver architecture enabling parallel processing in the electronic domain of a high-speed optical signal such that the post-processing electronic circuit operates at a lower data rate.
- Proposing the theoretical model of the electronic circuit to process the data captured from the parallel photodetector array in offline and to recover the original input bit stream.

## 1.7 Key contributions

The key contributions of this thesis are manifested by the design and characterization of the two novel PICs and their photonic component modules. The original contributions and

findings of this thesis are as followed:

- Design and characterization of the 3 dB 2 × 2 MMI couplers on the low-loss $Si_3N_4$ platform (in chapter 3).
- Experimental demonstration of the Cr heater integrated Mach-Zehnder interferometer on the low-loss $Si_3N_4$ platform (in chapter 3).
- The FDTD simulation to calculate the effective and group refractive index of the 72 nm × 2.8 $\mu$m cross-section $Si_3N_4$ waveguide. The simulation value of the group index is later verified by the experimentally measured value (in chapter 3).
- Design and characterization of the Chrome-based (Cr) heaters on the delay arms of the MZI's to tune the phase delay of the optical signal by $\pi/2$ (in chapter 3 and 4).
- Designing the thermally tunable 1 × 4 channel optical demultiplexer on the $Si_3N_4$ platform (in chapter 3).
- Designing the four channel optical PWSM device on the $Si_3N_4$ platform (in chapter 4).
- Experimental demonstration of forming a 64 ns long data packet by combining four 16 ns long segments of the data packet in time domain using the PWSM interface (in chapter 4).
- Design and characterization of four variations of the optical time sampling receiver using SiGe photodetectors (in chapter 5).
- Explaining the concept of optical time-sampling data recovery principle (in chapter 5).

## 1.8 Overview of the Thesis

In this research work, we have used different waveguide technologies to design PICs for short-reach interconnect system. The principal objective of the research work is to demonstrate the performance result of the four channel PWSM circuit designed on low-loss $Si_3N_4$ waveguide platform.

We have organized the thesis as followed: in chapter 2, we present the theory and background of the wavelength-striped mapping method. Motivation behind designing the PWSM device on low-loss $Si_3N_4$ waveguide platform is explained. Next, we describe the optical time sampling method using four SiGe photodetectors in an array structure. Two demonstrations of the electronic and optical front-ends augmenting the performance of the overall photoreceiver circuit is explained in this chapter.

In chapter 3, we present the analysis and experimental result of a thermally tunable $1 \times 4$ channel MZI based wavelength demultiplexer. We describe the structure and properties of the low-loss 72 nm $\times$ 2.8 $\mu$m cross-section area $Si_3N_4$ waveguide. The group index of the $Si_3N_4$ was experimentally measured.

In chapter 4, detailed design method of the four channel PWSM PIC is presented. Using the PWSM device, we have experimentally demonstrated WDM-to-serial conversion of the four 16 ns long data packets to construct one 64 ns long data packet.

Chapter 5 contains the design method and characterization result of the time sampling based optical deserializer using the SiGe photoreceiver. A TIA-less electronic front-end model of the optical receiver is also proposed in chapter 5, to demonstrate offline processing of the 20 Gb/sec photodetected signal in a low bandwidth electronic circuit.

In chapter 6, we have described performance result of a 16 GHz balanced photodetector and a 25 Gb/sec PAM-4 ring modulator, both were designed on the silicon photonics

platform. The methodologies to design these two devices are not directly related to this thesis. We have included the results in this chapter to list our involvement in other projects in parallel with this research work.

In chapter 7, we include possible future research directions to improve the performance of the two PICs presented here. We have discussed the result and contribution of the work presented in this thesis in chapter 8.

# Chapter 2

# Background and Motivation

In this chapter, we describe the theory of a conventional wavelength-striping method. We then explain a novel PWSM process proposed in [61], in the context of the work presented in this thesis. We will explain the motivation behind designing the PWSM circuit using low-loss $Si_3N_4$ waveguides and integrated thermal heaters. Finally, we describe the time sampling method, where silicon delay waveguides and directional couplers are used to enhance the performance of the overall photoreceiver architecture.

## 2.1 Theory

### 2.1.1 Optical wavelength-striped method

In the wavelength-striping approach, payload segments are encoded onto different wavelength channels. In a WDM link, one wavelength is dedicated for the entire payload data or information channel, whereas in the wavelength-striped based network parallel payload segments of a data packet are used to modulate different wavelength channels [59, 67, 68]. Therefore, wavelength-striping is suitable for high speed parallel interconnects to provide

high bandwidth link to a single host. Similar to a conventional WDM link, wavelength-striping approach also avoids serial-to-parallel or parallel-to-serial conversion of the data channels in the electrical domain. Fig. 2.1 shows a model of the basic wavelength-striped based network. In this model, it is assumed that the parallel payload segments of a data packet share the same time slot, which is common in a parallel data bus network. Therefore, each segment of the payload electrical data modulates an optical wavelength channel using an E/O modulator. Note that for an experimental demonstration, the parallel payload are generated by the same generator and electrically [59] or optically [58, 60] decorrelated to ensure different data are modulated on different segments. The optically modulated payload segments are multiplexed using the optical wavelength multiplexer (*i.e.*, AWG) to form the wavelength-striped packets. At the receiver-end parallel payload segments are optically demultiplexed by an AWG. Each of the individual payload segments are converted to electrical signal using photodetectors.

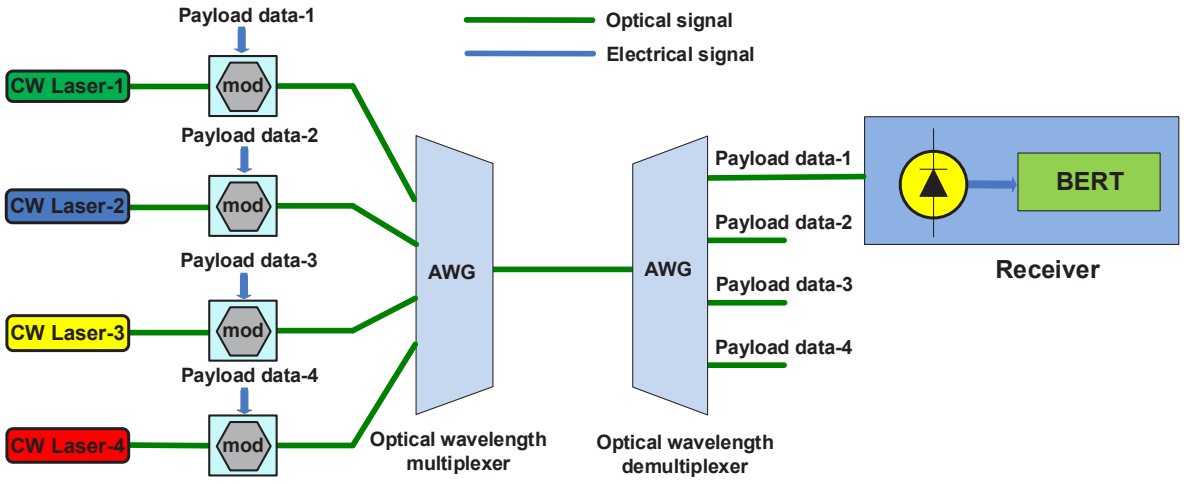



**Fig. 2.1** Simplified schematic diagram of the experimental testbed model of a wavelength-striped network. BERT: BER tester.

### 2.1.2 Passive wavelength-striped mapping (PWSM)

A novel PWSM process is proposed in [61], where, one serial stream of the data packet modulates multiple wavelength channels by using only one modulator. In [61], it was shown that, it is possible to convert a serial packet stream to a parallel stream by the PWSM technique. The proposed technique requires simultaneous optical filtering and delaying each time segment of the serial data packet with respect to its adjacent channel by a pre-determined amount of time using the optical buffer delay lines. For practical purpose, an integrated approach becomes essential for highly paralleled optical interconnects with the increased off-chip bandwidth density requirement in data communication.

In a conventional WDM or wavelength-striped optical interconnect, each wavelength of light is modulated using one optical modulator. The optical modulator is driven by the electrical data stream. At the transmitter node, the modulated optical wavelength channels are multiplexed using an optical multiplexer (MUX) before transmission. In the PWSM process demonstrated in [61], one modulator was used to modulate all wavelength channels (for example, $N = 8$ wavelength channels in Fig. 2.2) with the same electrical data stream. An optical filter is used after the modulator to separate all eight channels and then with different length fiber delay lines (FDL), each of the channels is delayed by a fixed amount of time with respect to its adjacent channels. The fixed time delay depends on the number of channels ($N$) and the data packet size ($T$ ns). The delayed wavelength channels are then multiplexed and gated at an appropriate time to form the WDM packet, which contains the time compressed data packet on all the $N = 8$ channels. The gating can be done using a SOA.

There is an idle time equal to $(N-1)T/N$ ns between two adjacent WDM packets. This idle time between two WDM packets can be interleaved by $(N-1)$ different WDM

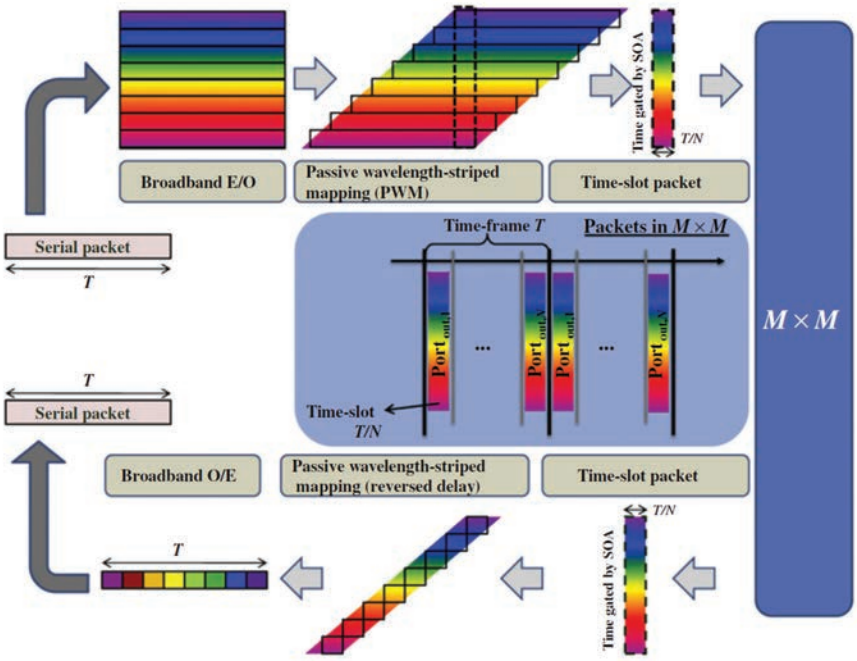



**Fig. 2.2** Time compressed WDM packets in the passive wavelength-striped mapping process [46].

packets by time division multiplexing. The $(N-1)$ WDM packets are generated using a similar mechanism from other PWSM circuits. At the receiver, the data packet can be recovered all-optically, first by gating, then by demultiplexing and delaying each wavelength with respect to its adjacent wavelength in a complementary way to that performed at the transmitter. After this the $N$ channels are optically multiplexed at the receiver to form the original data packet, as shown in Fig. 2.3.

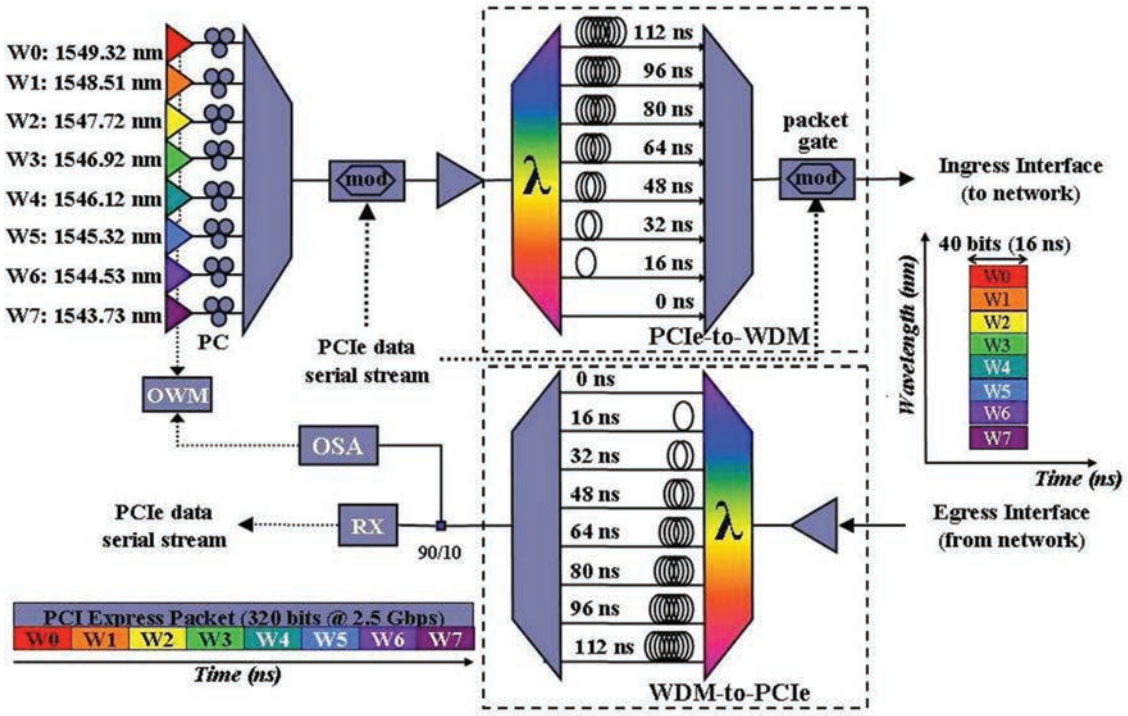



**Fig. 2.3** Detailed schematic of the all-optical PWSM experimental demonstration [61].

### 2.1.3 Energy-efficient PWSM method

In [61], it is shown that by exploiting PWSM process, the scalability of an optical interconnect can be increased. In addition to this, due to the use of one modulator per PWSM circuit, where one modulator modulates multiple number ($N$) of wavelength channels, static power dissipation significantly reduces in the interconnect. To prove this concept, we compare power dissipation of the conventional wavelength-striped (WS)-based and the PWSM-based network, where each of the systems has a four-channel WS-based transmitter, as shown in Fig. 2.4.

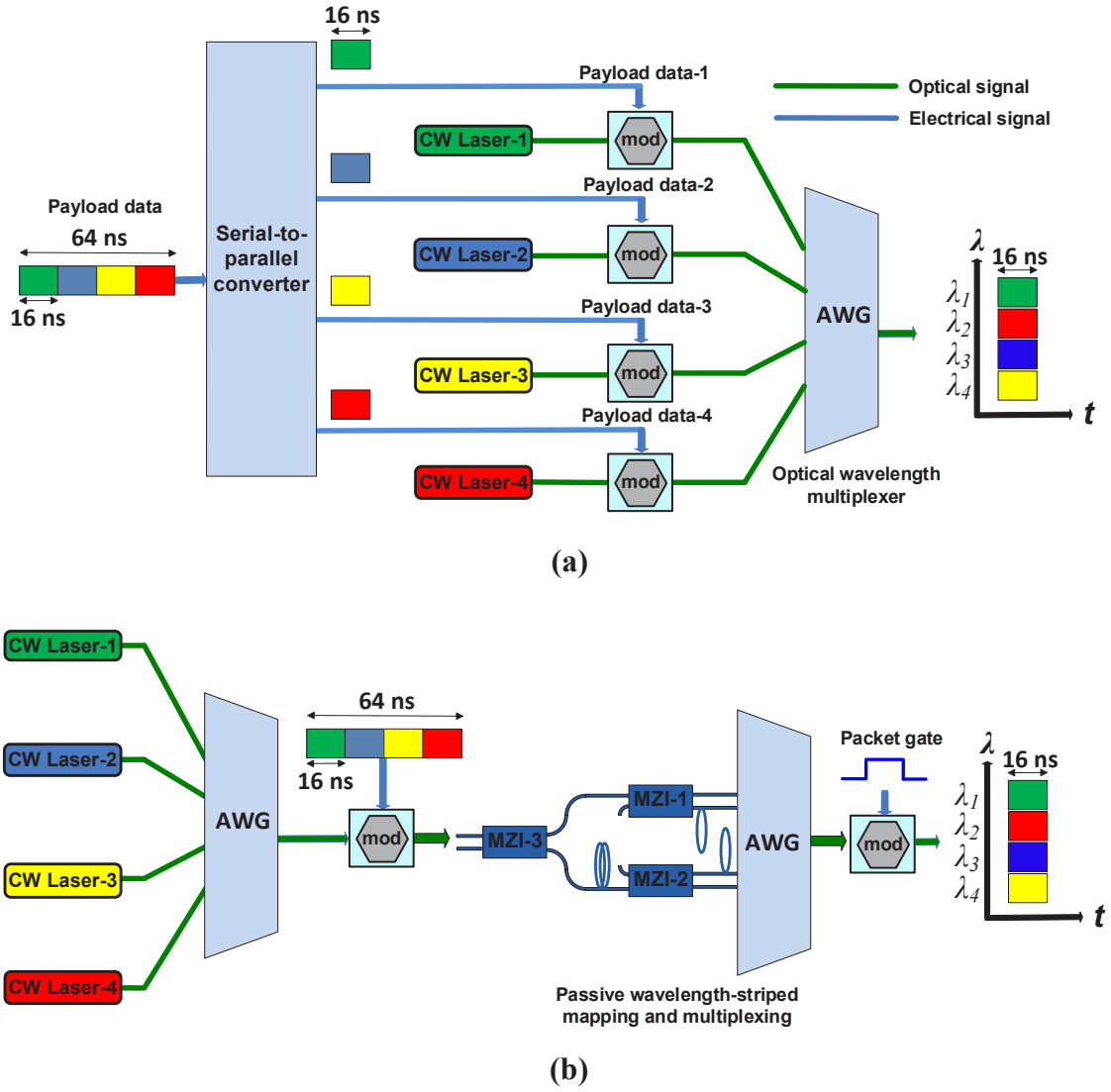



**Fig. 2.4** Simplified schematic diagram of transmitter section of the four-channel (a) conventional WS network, (b) PWSM network. AWG: arrayed waveguide grating.

Fig. 2.4 (a) shows the simplified schematic of a WS network, where a 64 ns serial data packet is partitioned or striped into four 16 ns long packets using an electronic serial-to-

parallel converter circuit. Four optical modulators or E/O components are utilized to map the four data packets to four wavelength channels. Therefore, in the WS process, power dissipation linearly increases with the number of wavelength channels limiting the scalability of the WS-based network. For example, the commercial SHF 803P optical modulator driver consumes 5 W of power (9 volt supply, 0.55 A current) [69]. This is the static power consumption of the electronic driver circuit meaning that this power will be consumed per modulator driver even when the input electrical driving signal or the data packets are set to null or zero. With the improvement of the low driving voltage optical modulator, the power consumption in the electronic driving circuit will be reduced (*i.e.*, the modulator driver in [70] consumes 0.437 W power from a 5 volt supply). However, even with the improvement in technology scaling 0.437 W is moderately high power, therefore, the static power consumed by the E/O modulator drivers is a bottleneck in increasing the scalability of the one-to-one E/O mapping based WS network. In addition to this bandwidth-coupled power dissipation, high-speed and power-consuming electronic circuits would be required for converting the bit sequence of the serial packet into parallel streams. For example, the aforementioned (in section 1.4) 56 Gb/s PAM-4 transceiver based serializer-deserializer (SerDes) designed in the 40 nm CMOS technology node dissipates 710 mW electrical power (transmitter: 290 mW and receiver: 420 mW, [49]). In a PWSM system, on the other hand, the full 64 ns long serial data stream is directly mapped onto four optical wavelengths by simultaneously modulating all the wavelengths using a single optical modulator, as shown in Fig. 2.4 (b). Therefore, the static power dissipated by the electronic driver module of the network is reduced to $1/4^{\text{th}}$ of that of the conventional WS network in this particular example. The dynamic power consumption remains same due to the requirement of 64 ns long E/O mapping of the data packet in both cases. However, with the improvements offered by CMOS technology scaling, the overall dynamic power dissipation remains rel-

atively constant while the static power dissipation arising from leakage currents becomes the dominant power consuming source. In addition to this, the PWSM network has the possibility of further reducing the power consumption of the network, as the serial data packet is partitioned to parallel streams in the optical domain utilizing passive MZI based filters and optical delay lines (Fig. 2.4 (b)).

An experimental 73.5% reduction in the static power dissipation is achieved in the eight-channel PWSM device demonstrated in [61], without considering power consumed by the optical power amplifying sources (*i.e.*, erbium doped fiber amplifiers (EDFA), semiconductor optical amplifiers) and the modulator gating the packet (Fig. 2.4 (b)). In chapter 4, it will be shown that EDFA or SOAs are required to compensate the insertion loss of the passive PWSM device having longer delay lines. However, in future, the PWSM device can be designed with further low-loss $Si_3N_4$ waveguides (*i.e.*, 3.2 dB/m in this work vs 0.5 dB/m or 0.1 dB/m in [28]) leading to the energy efficient integrated PWSM device.

### 2.1.4 Time sampling based photodetection

In this section, we introduce the background of time sampling based photodetection theory leading to design of the novel SiGe photodetector presented in this thesis. Time sampling based photodetection leads to the design of an ultra low power and scalable bandwidth photoreceiver. This method facilitates the integration of the high speed O/E photodetectors with the low speed electronic front-end [66, 71]. In time sampling based photoreceivers, total capacitance ($C_P$) of the photodetector and the electronic frond-end ($C_{in}$) is used to integrate the PD generated photocurrent ($I_{PD}$). The model of the RC front-end proposed in [66] is shown in Fig. 2.5. In Fig. 2.5, the PD capacitance ($C_P$) and the resistance ($R$) are shown. The voltage across ($V_{PD}$) the PD resistance is generated by integrating the photocurrent.

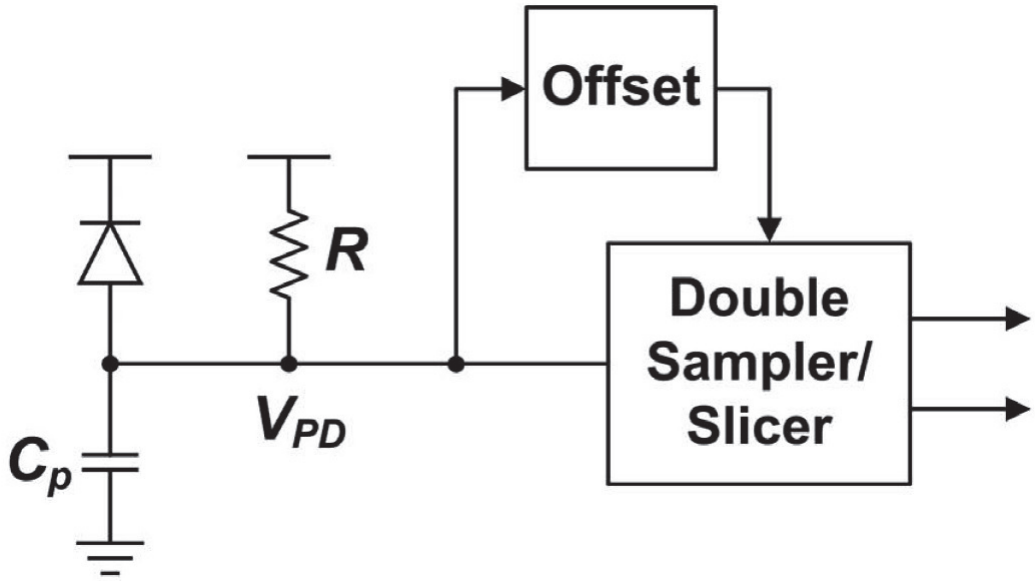



**Fig. 2.5** Model of the double time sampling based RC electronic front-end [66].

The PD voltage ($V_{PD}$) is sampled by a double sampling module. The double sampling module samples $V_{PD}$ at the end of two consecutive bit times ($V_{n-1}$ and $V_n$). In [66], dynamic offset modulation (DOM) is used to increase the voltage difference ($\Delta V_n$) for weak ones/zeros and to decreases it for strong ones/zeros. The DOM module is shown in Fig. 2.5 before the double sampling module. If one bit duration of the incoming signal is ($T$), then the sampled voltages in the electronic front-end at $n$ and $n-1$ sampling intervals can be related as shown in equation 2.1 [72]:

$$V_n = V_{n-1} + \frac{I_{PD}.T}{C_P + C_{in}} \tag{2.1}$$

The original bit sequence $V_n$ can be recovered by comparing the voltage difference ($\Delta V_n$) between $V_n$ and $V_{n-1}$ (*i.e.*, if $\Delta V_n < 0$, then $V_n = 0$, and if $\Delta V_n > 0$, then $V_n = 1$ ). It

is shown in [66] that, the application of time sampling method eliminates the need of TIA from the receiver circuit, and an analog electronic front-end of $RC$ bandwidth 290 MHz can be used to capture a 24 Gb/s photodetected signal with $1 \times 10^{-12}$ BER at –4.7 dBm optical sensitivity. It is shown in [71] that a low bandwidth TIA can further enhance the sensitivity of the receiver with the minimum power overhead. The challenges to design the electronic front-end to implement the time sampling method are: sampling and storing the analog voltage, voltage comparison at the original bit rate, subtracting the average input current to generate bipolar voltage and generating the phase matched clock signals [72]. These challenges are addressed by designing the analog RC front-end and the post-processing electronic circuits using the present state-of-art CMOS technology [66, 71, 72].

In our contribution, we propose a novel time sampling based photoreceiver, where some of the challenges in designing the electronic front-end have been transferred to the optical front-end. At the optical front-end, before the photodetection stage, the power of the incoming modulated optical signal is distributed to four channels. The optical data in each channel are delayed with respect to the adjacent channel by one bit duration, as shown in Fig. 2.6. The one bit delay between the adjacent channels has been implemented by using integrated delay waveguides.

To uniformly distribute the optical power across the four channels, coupling ratios of the power splitters were varied to compensate for the delay waveguide loss. Therefore, each of the four PDs generates consecutive one bit delayed version of the same data stream. Averaging each channel's response over four bit intervals using the PD capacitance and the input capacitance of the electronic front-end, a five-level distinct symbol can be generated from each of the PD channels. We have shown that by comparing the sampled voltage or symbols at every four bit intervals, the original bit stream can be recovered. The TIA-less photoreceiver requires a low-bandwidth analog front-end and a digital circuit which

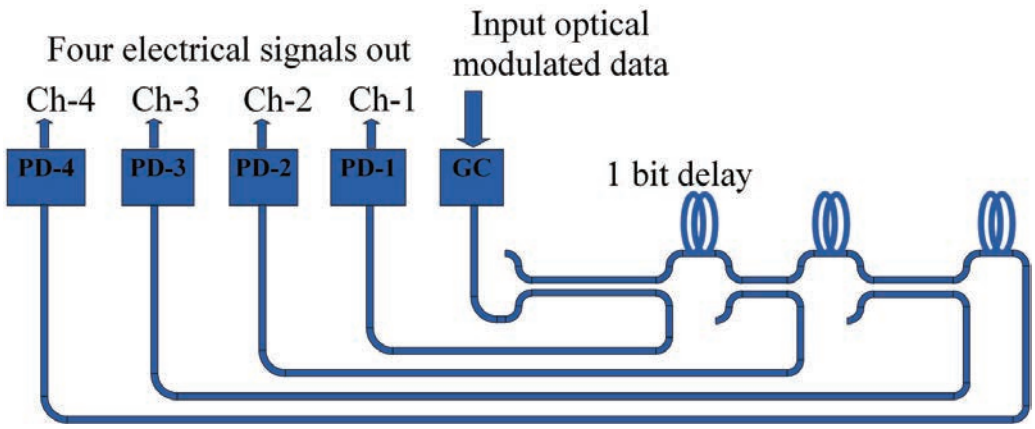



**Fig. 2.6** Schematic of the optical front-end of the time sampling photoreceiver architecture.

operates at $1/4^{th}$ of the original data rate. Detailed methodology to regenerate the original bit stream using the time sampling based photoreceiver is described in chapter 5.

## 2.2 Motivation

In section 2.1, we have presented the theory of wavelength-striped multiplexing, PWSM and time sampling based photodetection methods. In this section, we will discuss the challenges to design the PWSM device on the conventional InP or silicon photonics waveguide based PIC platform. We find that the ultra low-loss $Si_3N_4$ waveguide is a suitable PIC platform to design the long optical delay waveguides required for the PWSM device. We will also present the motivation behind designing the time sampling based photodetectors on SiGe platform.

### 2.2.1 PWSM on PIC

The basic function of a PWSM process is to filter each wavelength channel and then delayed the adjacent channels in time. The challenge and price to pay for performing the mapping in the optical domain is the power loss due to the longer propagation associated with the delay process. The power-efficient implementation has been experimentally demonstrated with fiber-based components in [61]. The PWSM circuit was built with fiber-based components, where the wavelength-striped process was achieved using passive optical components such as filters and FDLs. While fiber-based implementation is viable due to the low-loss silica fibers, it becomes impractical and bulky when considering delays as long as the serial packet length (e.g., delaying by 2048 bits at 50 Gb/s requires 8 m of silica fiber). In [46], for example, we proposed an analytical model of the PWSM circuit, where an optical serial packet stream is converted to a parallel stream to increase the bandwidth scalability of the optical interconnect networks. The theoretical model of the PWSM circuit is built by considering the propagation loss typically exhibited in the low-loss silica based waveguides. Therefore, it is important to use a low-loss integrated waveguide technology to build the PWSM circuit on PIC.

Propagation losses of the 80 nm $\times$ 2.8 $\mu$m cross-section area $Si_3N_4$ waveguides first reported in [44] were measured to be 8 dB/m (0.5 mm bend radius), and as low as 3 dB/m for larger bends (2 mm bend radius). Large bending radius is required in the low-loss $Si_3N_4$ waveguide to reduce the mode-mismatch loss in the bending regions. Therefore, in the PIC applications, where compact waveguide routing is required, high index contrast waveguides, such as SOI waveguides are preferable to $Si_3N_4$ waveguides. Standard SOI waveguides (220 nm $\times$ 500 nm cross-section area) with propagation losses of $\sim$2.5 dB/cm have been demonstrated with bending radius as low as 7 $\mu$m [73]. However, to design the

optical buffer circuits using long length delay waveguides (*i.e.*, in the range of meters to introduce several $ns$ time delay [46, 74]), SOI waveguides are not suitable. For example, to design the 12.86 ns delay line demonstrated in [74], a ∼0.92 m long 220 nm × 500 nm cross-section SOI waveguide will exhibit around ∼230 dB loss.

In this work, low-loss $Si_3N_4$ waveguides are investigated to build integrated long optical buffers. Using a wafer-bonded silica-on-silicon planar waveguide platform, propagation losses as low as 0.1 dB/m are reported in [28], where the waveguide thickness is set to 40 nm and the waveguide width varies from 3 $\mu$m to 14 $\mu$m. The low trending propagation loss of $Si_3N_4$ waveguides suggests that these waveguides can be used to build all optical packet routing PICs where long optical delay lines or low-loss optical buffer circuits are required [75].

### 2.2.2 Time sampling based photodetector on SiGe platform

From the theory of the time sampling based photodetectors presented in section 2.1.4, it is evident that directional couplers, optical delay lines and photodetectors need to be integrated on the same platform to design the photoreceiver. All of these components have been experimentally demonstrated on silicon photonics technology. For example, directional couplers with varying coupling ratios have been characterized in [73]. Low-loss ridge-based silicon waveguides with only 0.026 dB/cm propagation loss is demonstrated in [23]. Ge on Si (SiGe) photodetector is a mature component, demonstrated in several works, such as in [62, 76, 77]. Also, in [63] a SiGe PD is wire bonded to a 90 nm CMOS TIA for post amplification of the photodetected signal. Integration of the SiGe photodetector with the electronic circuit is important to further process the photodetected signal in analog (for amplification) and digital (for post processing) domain. Therefore in this work, we have chosen the silicon photonics technology to design the time sampling based photoreceiver by

optimizing the design parameters of the directional couplers, optical delay lines and SiGe photodetectors.

## 2.3 Summary

In this chapter, we reviewed the theory of wavelength-striped and passive wavelength-striped mapping method. In the wavelength-striped method, payload segments of the data packet are encoded onto a unique optical wavelength. In the PWSM method, one serial stream of the data packet modulates multiple wavelength channels using only one modulator. The PWSM method offers the advantage of using one modulator regardless of the number of wavelengths used in the network. Therefore, this method decouples the static power dissipated by the E/O modulators from the aggregated bandwidth capacity of the network. The PWSM device is built using the passive optical fiber-based multiplexer and delay lines, which leads to reducing the power consumption of the device. In this work, we have proposed to design the PWSM device using integrated $Si_3N_4$ waveguide based technology.

We have also discussed the time sampling based photodetection method to recover a high data rate photodetected signal using a low bandwidth TIA-less electronic front-end. We proposed a novel approach in this work, where the delay lines and power couplers are implemented in the optical front-end, which facilitates to integrate/average the optical signal energy using the PD and electronic front-end capacitance.

# Chapter 3

# A Thermally Tunable 1 × 4 Channel Wavelength Demultiplexer

Optical interconnection between servers within a data center can enhance the data processing capacity of the network by exploiting space, time, and wavelength domains [46, 59, 78]. An important challenge is to design PIC with complex optical signal processing functionalities such that many of the data processing tasks can be transferred from the electrical to the optical domain. PICs using low-loss optical waveguide on $Si_3N_4$ [27] platform technology is a promising solution to implement some complex optical functionalities on-chip such as generating large optical time delay (*i.e.*, by using optical buffers [74]) or to build high quality factor resonators [79].

The PWSM circuit implements simultaneous optical filtering and delays each time segment of the data with respect to its adjacent channel by a specific amount of time using optical buffers or long optical delay waveguides. To design an integrated version of the PWSM circuit, low-loss $Si_3N_4$ waveguides can be used to build its key building blocks (*i.e.*, a demultiplexer to filter the optical channels and the long delay lines to implement the

time delay between the adjacent channels). A low-loss AWG demultiplexer using $Si_3N_4$ waveguide platform is proposed in [37]. An AWG based demultiplexer on $Si_3N_4$ waveguide platform presented in [37] (<0.5 dB insertion loss and 40 dB crosstalk) demonstrates better performance than the MZI filter based optical demultiplexers. However, in [46] we find that the AWG approach to build the demultiplexer in a PWSM circuit incurs overall greater loss and increases the footprint of the PWSM device due to the individual time delay requirements for each of the channels after the AWG. MZI based demultiplexers can solve this problem by simultaneous filtering and delaying the optical channels with respect to their adjacent channels. In addition to this, the optical signal processing circuit requires a MZI based lattice filter architecture such that filter parameters can be tuned (electro-optically or thermo-optically) to generate tunable optical signals [80]. Therefore, a MZI based thermally tunable wavelength demultiplexer is an important device which adds more functionalities or tunability in the low-loss $Si_3N_4$ delay waveguide based components. For the applications where large optical time delays are required in addition to the wavelength filtering, the AWG based multiplexer and MZI filter based demultiplexer can be used together to build the complete PIC on chip [46].

In this chapter, we present the analysis and experimental result of a thermally tunable 1 × 4 channel MZI based wavelength demultiplexer designed using a 2.8 $\mu$m × 72 nm cross-section area $Si_3N_4$ waveguide. The waveguide has a $SiO_2$ substrate and a PECVD $SiO_2$ upper cladding, where the thickness of both layers is 15 $\mu$m. The demultiplexer is fabricated using the TriPleX photonic platform [81] from LioniX BV. Performance result of the general interference based 2 × 2 MMI couplers used to build the MZ interferometers shows a 3 dB uniform power division ratio over 50 nm wavelength range from 1530 nm to 1580 nm. After filtering by the demultiplexer, we have measured 1 × $10^{-12}$ BER for all of the four 40 Gb/s data rate channels at a 10 Gb/s rate. The results presented in this

chapter are published in [82].

## 3.1 Design of the 1 × 4 channel wavelength demultiplexer

In this section, we first describe the structure and properties of the low-loss 2.8 $\mu$m × 72 nm cross-section area $Si_3N_4$ waveguide. Next we present the simulation method and result used to design the MMI couplers and the overall MZI based demultiplexer.

### 3.1.1 Low-loss $Si_3N_4$ waveguide

The low-loss single strip geometry $Si_3N_4$ waveguide from the TriPleX photonic platform [81] was chosen to design the photonic components presented in this chapter. The waveguide fabrication process is similar to the methods reported in [27]. The width and height of the waveguide were chosen such that minimum propagation loss is achieved at the bending radius equal to or more than 4 mm. The cross-section area of the waveguide is shown in Fig. 3.1(a). Fig. 3.1(b) shows the TE mode profile of the optical waveguide obtained from 2D finite-difference time- domain (FDTD) simulation using the Lumerical software.

We calculate the effective index ($n_{eff}$) and group index ($n_g$) of the waveguide using the 2D FDTD method over the wavelength range from 1530 nm to 1580 nm. Fig. 3.2(a) and Fig. 3.2(b) shows that the effective index and group index of the waveguide varies by $\triangle\, n_{eff} = -0.0015$ and $\triangle n_g = -0.006$, respectively, over the wavelength range from 1530 nm to 1580 nm. The change in both the effective index and in the group index of the waveguide with respect to the wavelength results into a wavelength dependency in the transmission response of the demultiplexer, which will be discussed in section 3.2.2.

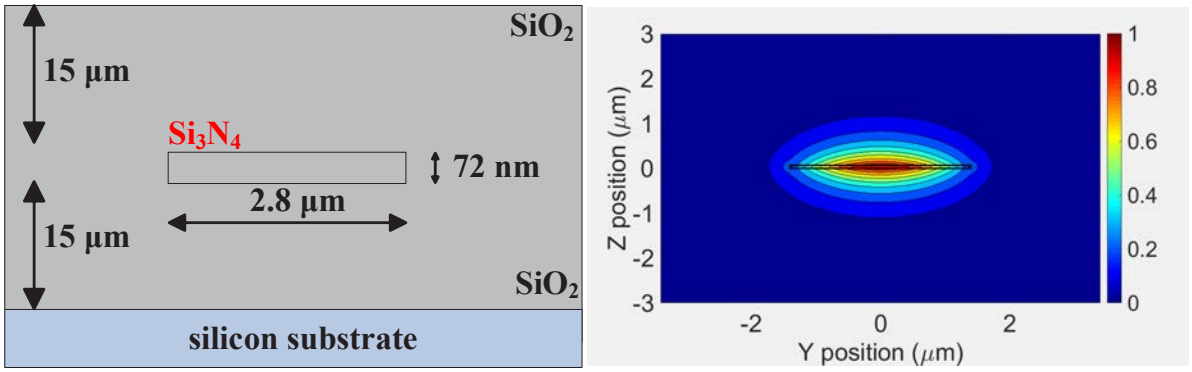



**Fig. 3.1** (a) Cross-section (not to scale) of the single stripe geometry $Si_3N_4$ waveguide, (b) Simulated TE mode profile (in linear scale) at 1550 nm wavelength, where the 72 nm thick $Si_3N_4$ waveguide is superimposed (drawn to scale).

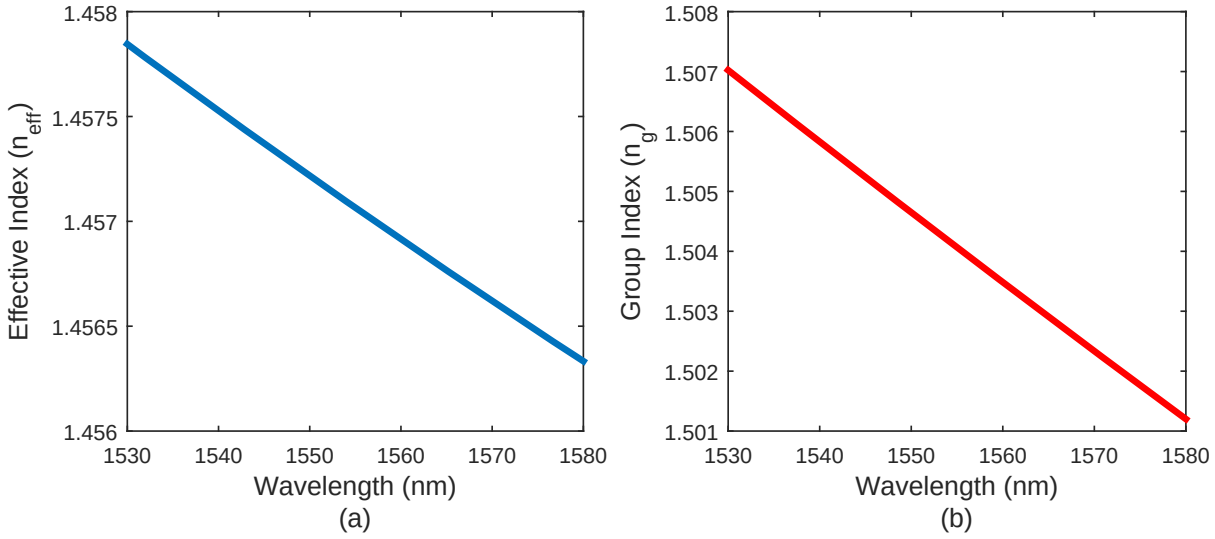



**Fig. 3.2** Variation in the (a) effective index ($n_{eff}$) and (b) group index ($n_g$) of the $Si_3N_4$ waveguide from the wavelength range from 1530 nm to 1580 nm.

### 3.1.2 Design of the 2 × 2 MMI coupler

The general interference based 2 × 2 MMI couplers were used to build the MZ interferometers of the demultiplexer. It is necessary to perform numerical simulations to accurately estimate the core waveguide length of a MMI coupler for a given core waveguide width [83].

In this work, we use FDTD simulation from Lumerical software to estimate the core MMI waveguide length '$L_{MMI}$'. Fig. 3.3(a) shows the waveguide geometries of the 2 × 2 MMI coupler designed in this work. The core waveguide width ($W_{MMI}$ = 30 $\mu$m) is chosen to make the lateral separation between the two input or the two output waveguides large enough ($L_{lat}$ = 10 $\mu$m) such that no inter-coupling occurs between the two side-by-side input (I/P) waveguides. The access waveguide width ($W_a$) is increased to 5 $\mu$m to minimize the mode mismatch loss at MMI core waveguide input and output edges [83]. A 200 $\mu$m long taper waveguide is designed to lower optical loss transition from the 5 $\mu$m wide waveguide to the 2.8 $\mu$m wide waveguide. Fig. 3.3(b) shows the electric field distribution (in linear scale) in a 2D plane of the MMI coupler for a MMI core waveguide length of $L_{MMI} \sim 1860\mu m$ at 1550 nm wavelength.

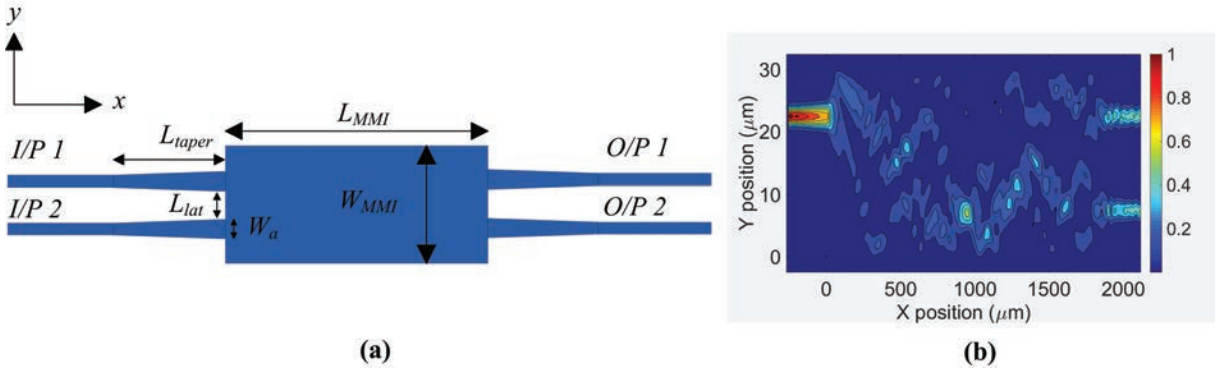



**Fig. 3.3** (a) Schematic of the 2 × 2 MMI coupler with taper waveguide length, $L_{taper}$ = 200 $\mu$m and access waveguide width, $W_a$ = 5 $\mu$m and (b) the electric field distribution in a 2D plane of the MMI coupler at 1550 nm wavelength.

To determine the effect of the variation in the MMI coupler length on the insertion loss and the power coupling between the two output (O/P) ports of the MMI coupler, we have simulated three MMI structures with different core waveguide lengths, while keeping the core waveguide width fixed to $W_{MMI}$ = 30 $\mu$m. Table 3.1 shows that at 1550 nm

wavelength, MMI coupler with the core waveguide length '$L_{MMI} \sim 1860\ \mu m$' exhibits minimum insertion loss per O/P waveguide (∼0.3 dB).

**Table 3.1** Simulation values of the power coupled to the two O/P waveguides of the MMI coupler

| $L_{MMI}(\mu m)$ | Percentage of the input power coupled to the two $o/p$ waveguides | | Input power coupled to the two $o/p$ waveguides ($dB$) | |
|---|---|---|---|---|
| | $O/P-1$ | $O/P-2$ | $O/P-1$ | $O/P-2$ |
| 1850 | 42% | 40% | –3.76 | –3.97 |
| **1860** | **47.1%** | **46.5%** | **–3.27%** | **–3.32** |
| 1870 | 43% | 42.5% | –3.66 | –3.71 |

### 3.1.3 MZI based 1 × 4 channel wavelength demultiplexer

Fig. 3.4 shows the schematic of the proposed demultiplexer architecture. The demultiplexer is designed to filter four 40 Gb/s data rate channels, where the wavelength separation between the adjacent channels is 3.2 nm. Therefore, in the demultiplexer structure shown in Fig. 3.4, each of the four output channels is designed to have 4 × 3.2 nm = 12.8 nm free spectral range (FSR) in its corresponding optical spectrum. The detailed design method of the MZI based optical demultiplexer/filter can be found in [84,85]. In addition to the extra delay lengths ($L_1$, $L_2$ and $L_3$) each of the MZI filters contains two equal length s-shaped bend waveguides (= 25.13 mm long), with a bending radius of 4 mm. As shown in Fig. 3.4, on top of these bend waveguides, 12 mm long heaters are situated for thermal heating. To achieve 12.8 nm FSR at the four output channels (*ch-1*, *ch-2*, *ch-3* and *ch-4*) of the demultiplexer, the first MZI (MZI with the extra delay waveguide length, $L_1$) is designed to have 6.4 nm FSR at its two output channels ($A_1$ and $A_2$), where the wavelength separation between the two channels is 3.2 nm. We have set the delay length, $L_1 = 249.5\ \mu$m in the first MZI to obtain FSR = 6.4 nm at its output channels ($A_1$ and $A_2$). Eqn. 3.1 is used to

estimate the value of $L_1$,

$$L_1 = \frac{\lambda^2}{FSR \times n_g} \tag{3.1}$$

where, the group index, $n_g = 1.505$ at $\lambda = 1550$ nm wavelength (from Fig. 3.2(b)).

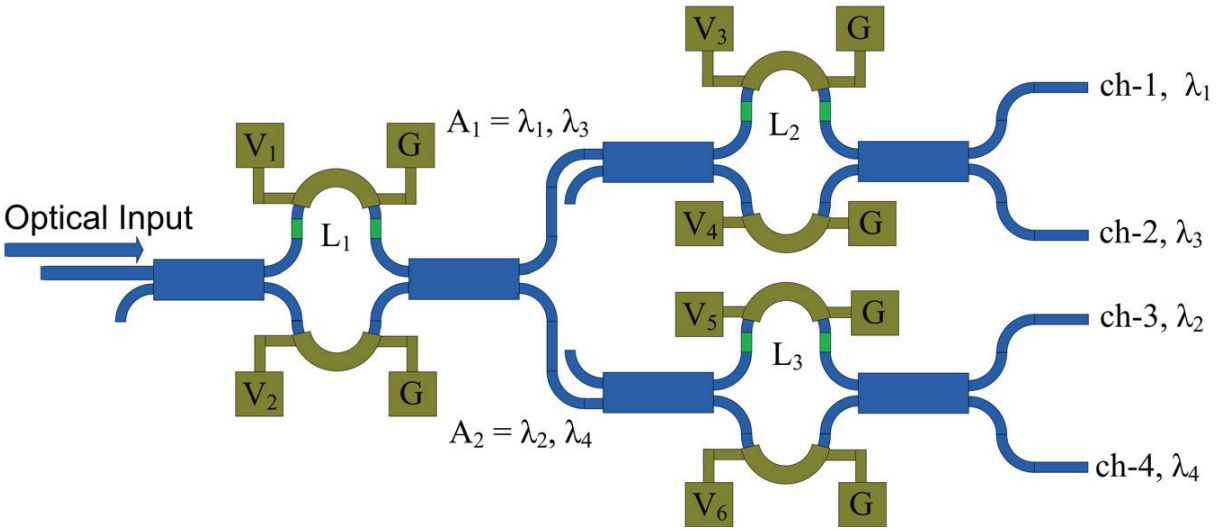



**Fig. 3.4** Schematic of the 1 × 4 channel wavelength demultiplexer architecture with the integrated Cr heater on the delay arms of the MZI (not to scale). $V_1$ to $V_6$: electrical pad to apply the DC voltages for thermal tuning, G: Ground pad, $L_1$ to $L_3$: Delay waveguide lengths (in green color).

The values of the delay waveguide lengths, $L_2 = 124.7\ \mu\text{m} + L_\pi/2$ and $L_3 = 124.7\ \mu$m, are chosen such that the corresponding MZI's containing these delay lines have an FSR = 12.8 nm. Note that, an extra delay length, $L_\pi/2 = 0.257\ \mu$m, is added to $L_2$ in the second MZI, to induce a phase shift of $\pi/2$ in the optical signal of the corresponding delay arm. This extra $\pi/2$ phase shift is necessary to obtain the required wavelength separation of 3.2 nm and low crosstalk between the output channels *ch-1* and *ch-2*. Fig. 3.5(a) presents the simulation result of the overlapped optical transmission response of the four channels (*ch-1*, *ch-2*, *ch-3* and *ch-4*) of the demultiplexer, where a ∼15 dB crosstalk between the channels is obtained. We find that it is important to implement thermal tunability in the

delay arms of the MZIs to ensure low crosstalk as well as the required channel separation between the output channels. As an example, a 100 nm length offset error is added in the simulation to all the three delay arms ($L_1$ to $L_3$) of the demultiplexer to assess the impact of fabrication error on the demultiplexer. From Fig. 3.5(b), it is seen that this error results into an important degradation in the crosstalk performance of the demultiplexer (from 15 dB to 8 dB). The 100 nm length offset error induces 0.19 $\pi$ of phase error. It will be shown in section 3.2 that the thermal heaters designed in this work, can compensate up to 0.5$\pi$ of phase shift error at the expense of 150 mW (25 V, 6 mA) electrical power consumption. We have also investigated the effect of waveguide width variation on the phase shift between the two long delay arms (25.13 mm) of each MZI filter. As an example, we include a 2 nm width variation on the two delay arms (*i.e.*, 2.8 $\mu$m and 2.802 $\mu$m wide) of each of the three MZI filters in the demultiplexer. From a similar mode simulation method described in section 3.1, we find that for a 2.802 $\mu$m waveguide width, the group index increases by $\triangle n_g = 1.55\times10^{-5}$ at 1550 nm wavelength. The change in group index induces $\pi/2$ phase mismatch between the two 25.13 mm long delay waveguides which can be compensated by the thermal heaters. However, if the waveguide width variation is more than 2 nm over 25.13 mm long waveguide, the thermal heaters designed in this work cannot compensate for the phase error. However, the MZI delay waveguides are placed in proximity, and it is unlikely that two waveguides maintain such width difference over the 25.13 mm length. In fact, two delay waveguides in proximity are more likely to have the same width offset, which would induce near zero phase shift in the demultiplexer compensable by the thermal heaters.

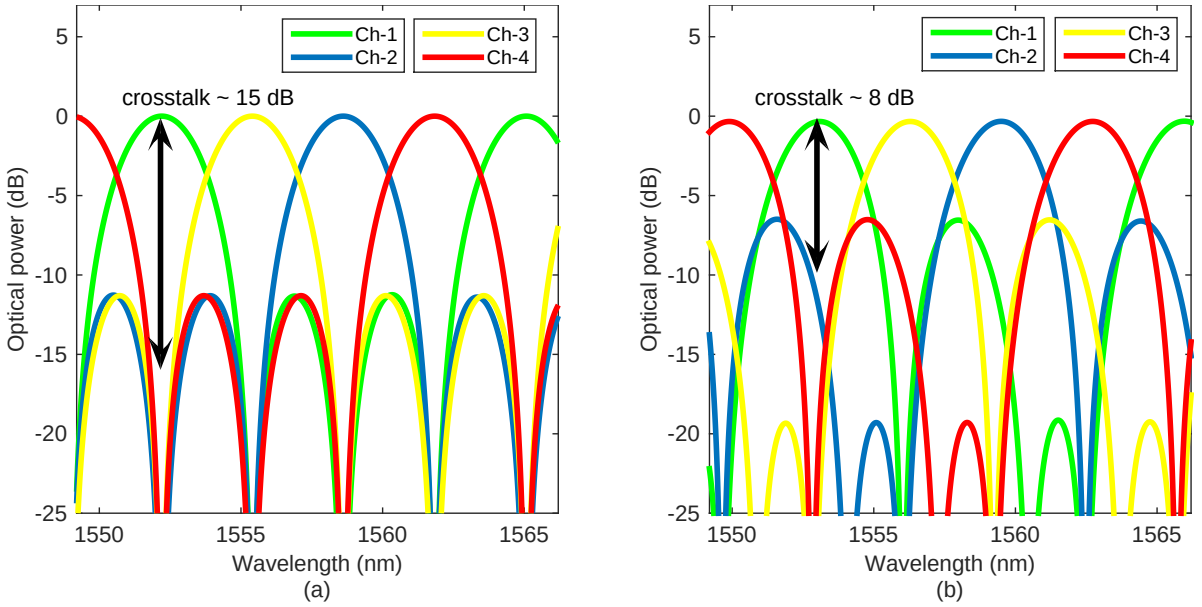



**Fig. 3.5** Simulation result of the (a) overlapped transmission responses of the four optical output channels, (b) overlapped transmission responses of the four optical output channels in the presence of a delay length mismatch error 100 nm.

Thermal heaters were integrated on top of the MZI delay waveguides for tuning the phase of the optical signal upto $\pi/2$. As mentioned in the paragraph above, we have added an extra delay length of $L_\pi/2 = 0.257$ $\mu$m to passively achieve the $\pi/2$ phase shift. Despite this delay, thermal heaters make the design of the demultiplexer more robust against fabrication variations. The electrical contact pads on the heaters were 2 mm × 0.5 mm in dimension with pitch = 1 mm (Fig. 3.6(a)). The large separation between the contact pads will simplify and lower the cost of wire bonding to the chip. However, in this work we have applied electrical voltage to the heaters using external DC probes. We have used proprietary data from LioniX BV to keep the separation between the thermal heaters from 8 mm to 16 mm, to avoid thermal crosstalk (Fig. 3.6(b)).

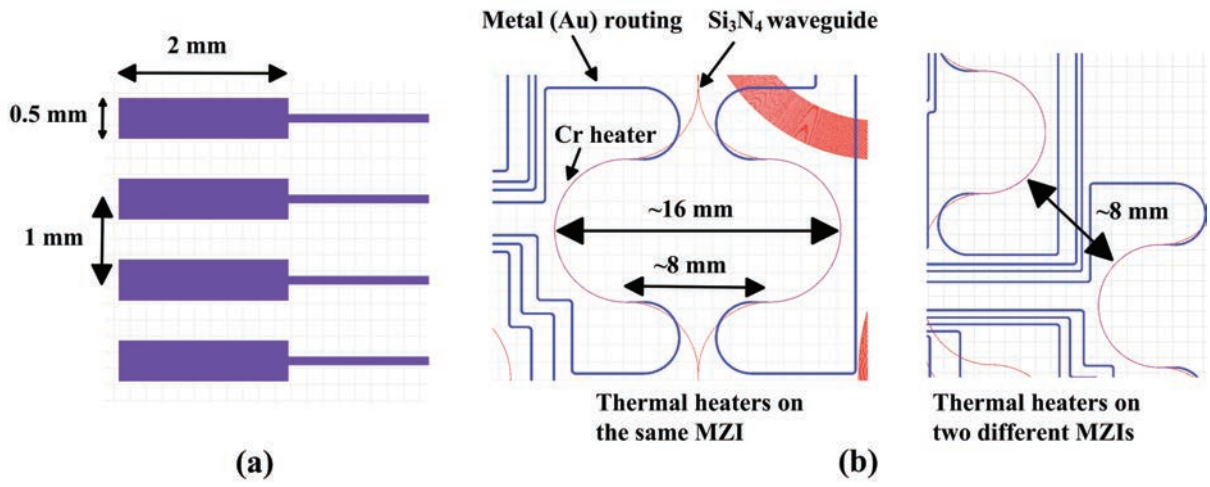



**Fig. 3.6** (a) Dimension and vertical separation between the electrical contact pads, (b) Layout of the thermal heaters, minimum distance is kept to 8 mm to avoid thermal crosstalk.

## 3.2 Experiment setup and results

To determine the performance result of the 1 × 4 channel wavelength demultiplexer, first, we have measured the transmission responses of the different passive test devices which were designed on the same chip. The test devices include a 10 cm long $Si_3N_4$ waveguide having nine bends of 4 mm bending radius, a spiral shaped 1.5 m long delay waveguide and three test structures for MMI couplers with different core waveguide lengths. The 1.5 m long test delay waveguide has a 4 mm bending radius at the center and routing regions (Fig. 3.7). Several 10 cm long test structures were designed next to each of the test components. The transmission response of these test devices allowed us to determine the propagation loss of the $Si_3N_4$ waveguide and the insertion loss of the MMI couplers. These test results also facilitate assessing the insertion loss of each channel of the demultiplexer. Then, we proceed to measure the BER performance of the demultiplexer.

Fig. 3.7 shows the experimental setup used to measure the transmission response of the passive components. A CW signal from a laser with an optical power of 10 dBm is

connected to a polarization controller (PC) and tuned over the wavelength range from 1530 nm to 1580 nm. At the output of the PC, the measured optical power is around ∼8.8 dBm. The polarized CW optical signal is applied to the input edge coupler (I/P) of the test device. The output optical power is measured for each of the test components and their corresponding 10 cm long test waveguide. The optical power transmitted through the 10 cm long test $Si_3N_4$ waveguide is used to normalize the output power of the other test devices such as the MMI couplers and wavelength demultiplexer to find their corresponding insertion loss. The distance between the i/o waveguide edges of the test components and the 10 cm long test waveguide at the polished facet is kept to 60 $\mu$m. This minimizes the error in measuring the test component's insertion loss due to the variation in fiber to chip coupling loss.

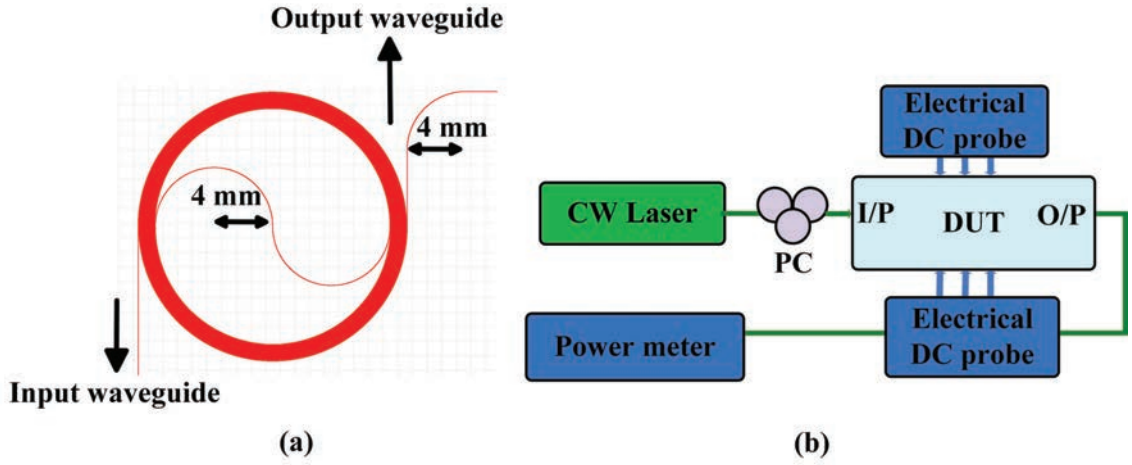



**Fig. 3.7** (a) Layout of the 1.5 m long spiral waveguide, (b) Experimental setup to measure the transmission responses of the different test devices, (10 cm long waveguide, 1.5 m long spiral waveguide and the 1 × 4 channel wavelength demultiplexer).

Fig. 3.8 shows the normalized optical transmission response of the ∼10 cm long straight waveguide and ∼1.5 m long spiral delay waveguide. The optical coupling to the chip was implemented using two cleaved fibers at the input and output edge of the chip. From

this figure it is seen that the total edge coupling in and out loss is around 9.8 dB at the wavelength of 1550 nm, considering the propagation loss in the 10 cm long $Si_3N_4$ waveguide is negligible compared to the edge coupling loss. The measured coupling loss variation over all the 10 cm long waveguides is less than 1 dB. From Fig. 3.8, it is also seen that the 1.5 m long spiral delay waveguide suffers an extra 4.6 dB optical loss compared to the 10 cm long $Si_3N_4$ waveguide. From this result, we measured an approximate 3.1 dB/m propagation loss for the 72 nm thick $Si_3N_4$ waveguide, where the total fiber to chip coupling loss is assumed to be 9.8 dB.

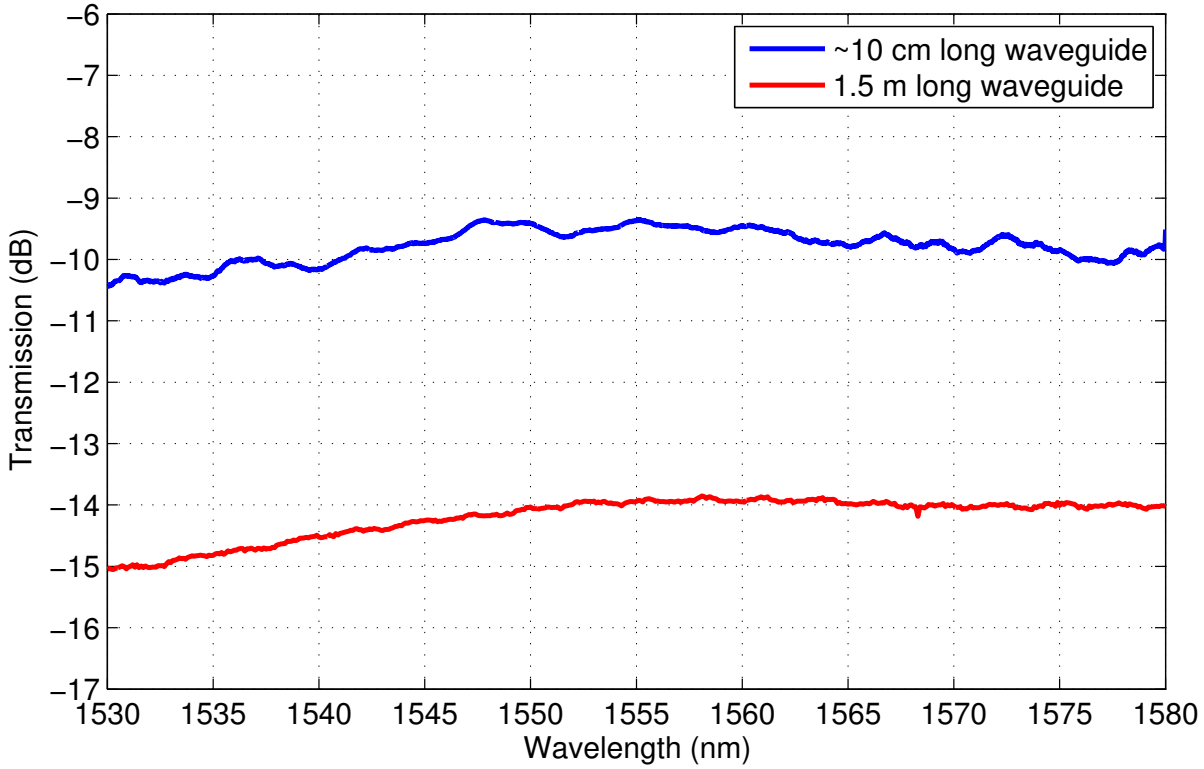



**Fig. 3.8** Normalized optical transmission response of the 10 cm and 1.5 m long $Si_3N_4$ waveguide.

We have experimentally determined the group index of the 72 nm thick $Si_3N_4$ waveguide using the transmission response of a test MZI. The length difference between the two arms

of the MZI is 4.4 mm (the two MZI arms are 12.26 mm and 16.66 mm in length). In addition to this, a ∼12 mm long and 20 $\mu$m wide heater was placed on top of the longer arm of the MZI filter to find the $P_\pi$(input power required at the heater to achieve $\pi$ phase shift in the CW signal) of the heater. All the heaters in the 1 × 4 channel wavelength demultiplexer have similar geometry. It should be mentioned that the test MZI structure is similar to the MZI filters of the 1 × 4 channel wavelength demultiplexer shown in Fig 3.4. However, as mentioned in section 3.1.3, the extra delay lengths in the MZI filters of the 1 × 4 channel wavelength demultiplexer is much smaller (*i.e.*, $L_1 = 249.5$ $\mu$m, $L_2 = 124.96$ $\mu$m and $L_3 = 124.7$ $\mu$m) compared to the extra delay length (4.4 mm) of the test MZI filter. Therefore, in the test MZI filter we expect to have smaller FSR, which will facilitate the experimental measurement of the group index of the waveguide within a small wavelength range. In both the test MZI and demultiplexer, $P_\pi$ of the heaters will be similar, as the heaters have same length (∼12 mm) in all the MZI filters presented in this chapter. Fig 3.9(a) shows the zoomed optical transmission response of the test MZI structure, where the input CW signal from the laser with an optical power of 10 dBm is tuned over the wavelength range from 1547 nm to 1552 nm. We found that at a heater bias voltage of 25 V (6 mA), the optical transmission response of the filter shifts in wavelength by an amount equal to $1/4^{th}$ of its FSR (0.09 nm). Therefore, the measured resistance and $P_\pi/2$ is 4.17 kΩ and 150 mW, respectively, for the MZI delay arms heater. From this result, the approximate value of $P_\pi$ can be interpolated to be 300 mW. Next, we used the method provided in [86] to measure group index ($n_g$) of the waveguide from the transmission response of the MZI. In this method, the measured FSR at different wavelengths is used to calculate the group index. Fig. 3.9(b) shows the simulated and experimental value of the group index at wavelength near 1550 nm. From this figure, it is clear that the experimental value of the group index is within ∼0.001 error limit from the simulation value. We calculated that within this

error limit of the group index, the FSR of the filter would change by only ∼0.003 nm. As the wavelength separation between the adjacent channels of the filter is 3.2 nm, this FSR variation due to this group index variation does not affect the filter performance.

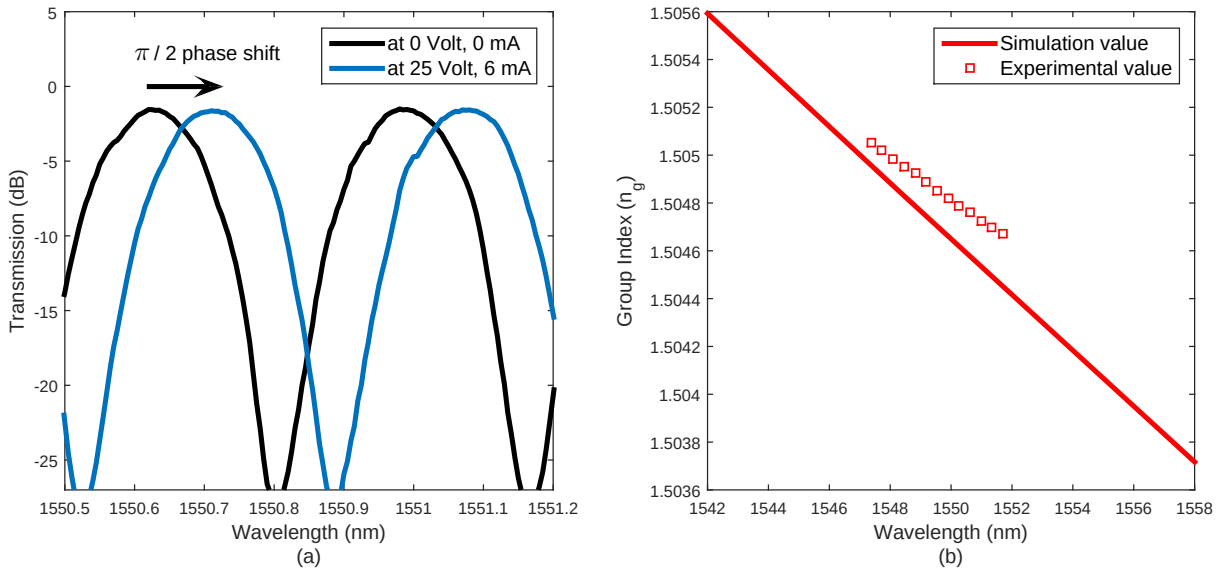



**Fig. 3.9** (a) Optical transmission response of the test MZI filter at two different bias voltages to the heater, (b) Measured and calculated group index of the 72 nm thick $Si_3N_4$ waveguide.

### 3.2.1 Power splitting ratio in the $Si_3N_4$ waveguide based MMI couplers

We assess the power splitting ratio in the two output arms of the MMI couplers. Three test MMI couplers were designed such that all the MMI couplers have the same core waveguide width ($W_{MMI}$) of 30 $\mu$m. The core waveguide lengths ($L_{MMI}$) of the three MMI couplers are varied from the first beat length (∼1860 $\mu$m found from simulation, section 3.1.2). Fig. 3.10 shows the normalized output transmission response of the MMI couplers. From this figure, it is seen that optical power splitting ratio within 0.3 dB power range is obtained for all the MMI couplers at both ports. The MMI coupler with $L_{MMI}$ = 1860 $\mu$m core waveguide length exhibits 0.4 dB loss per output channel at 1550 nm wavelength. The optical loss

per channel increases to 0.8 dB and 1 dB for the MMI couplers with ±10 $\mu$m variation from the simulated optimum core waveguide length. The 0.4 dB to 1 dB insertion loss for the MMI coupler is still high, considering the low-loss $Si_3N_4$ platform used to design the devices. This suggests that in the future runs the MMI coupler should be designed more carefully by considering both the simulation and experimental result obtained from this run.

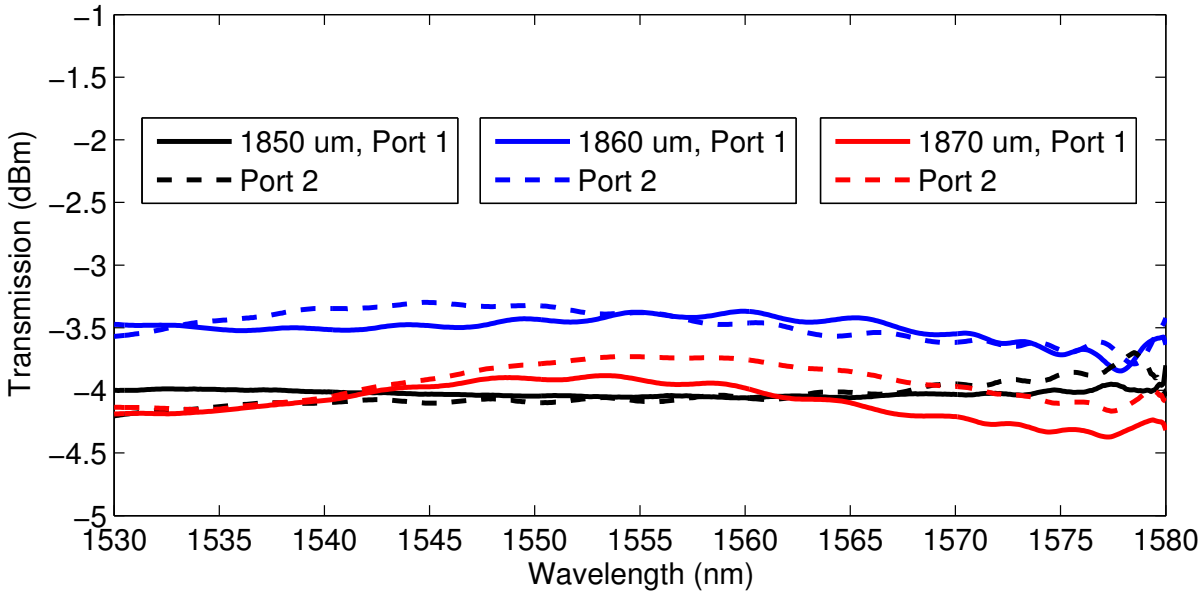



**Fig. 3.10** Normalized output transmission response at the two output ports of the MMI couplers.

### 3.2.2 Transmission response of the four channel wavelength demultiplexer

To determine the insertion loss and crosstalk between the adjacent channels of the 1 × 4 channel demultiplexer, we have used a similar setup as in Fig. 3.7(b). The optical phase shift in the the delay arms of the MZI interferometers was thermally tuned. We have applied a set of DC voltages to implement thermal heating in the corresponding delay arms. The thermal heating occurs from the electrical power loss in the resistive load of the heater. Fig. 3.11 shows the optical transmission response of each of the four channels of the demultiplexer. The applied DC voltages in the thermal heaters of the delay arms were $V_2 = 1.5$ V (0.32 mA), $V_3 = 4$ V (0.9 mA) and $V_5 = 2.5$ V (0.55 mA). All the voltages were applied simultaneously to the heaters to minimize the crosstalk between the channels. Each of the heaters has separate signal and ground contact pads, therefore no electrical cross-talk was observed due to simultaneous biasing. From this figure it is seen that the side lobe suppression ratio for $ch-1$, $ch-2$, $ch-3$ and $ch-4$ are 12 dB, 12.8 dB, 12.6 dB and 11.2 dB, respectively from 1530 nm to 1580 nm wavelength range. The FSR from 1550 nm to 1580 nm wavelength range for $ch-1$, $ch-2$, $ch-3$ and $ch-4$ are 12.85 nm, 12.9 nm, 12.85 dB and 12.9 nm, respectively.

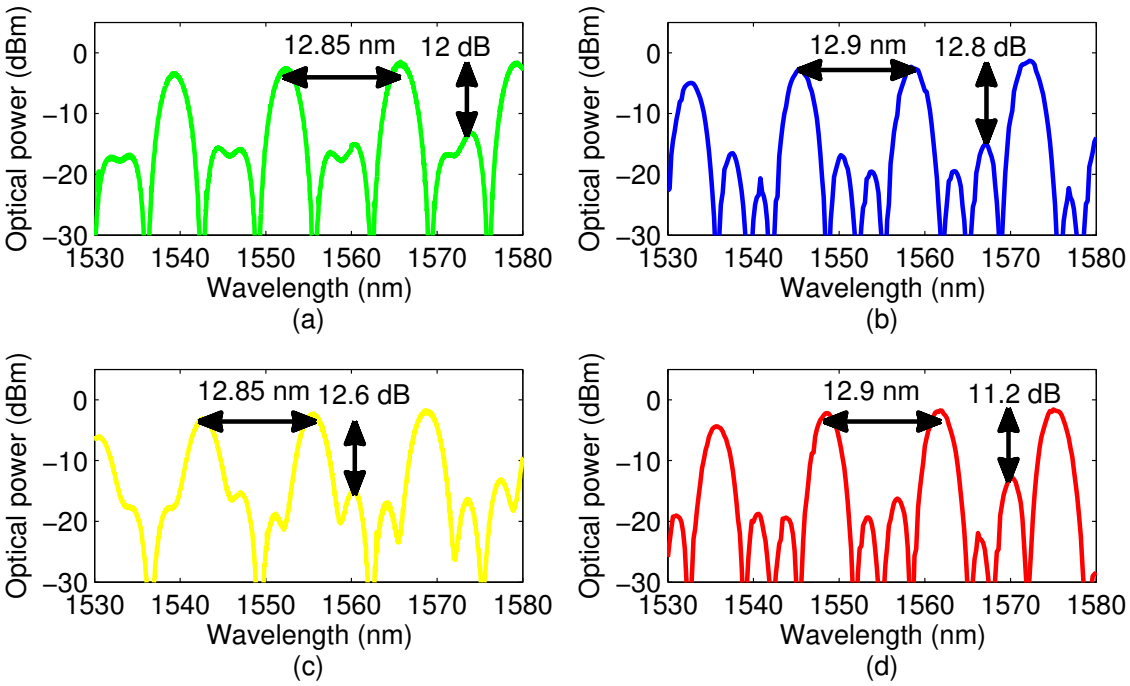



**Fig. 3.11** Normalized transmission response of the four optical output channels (a) $ch-1$, (b) $ch-2$, (c) $ch-3$ and (d) $ch-4$.

Fig. 3.12(a) shows the overlapped transmission responses of all four channels of the demultiplexer. In the transmission response from wavelength range 1550 nm to 1565 nm (Fig. 3.12(b)), we measured that the transmission peaks of $ch-1$, $ch-2$, $ch-3$ and $ch-4$ are at 1552 nm, 1558.45 nm, 1555.3 nm and 1561.6 nm. Therefore, the wavelength separation between $ch-1$ and $ch-3$ is 3.1 nm, between $ch-2$ and $ch-3$ is 3.15 nm, and between $ch-2$ and $ch-4$ is 3.15 nm. The FSR and wavelength separation between two channels is within the 0.1 nm range of the simulation result presented in Section 3.1.3. The FSR and wavelength separation between two channels match the simulation result presented in section 3.1.3. We used the results of Fig. 3.12(b) to set the four CW laser signals at the wavelength range from 1552 nm to 1561.6 nm to demonstrate WDM operation in section 3.2.3.

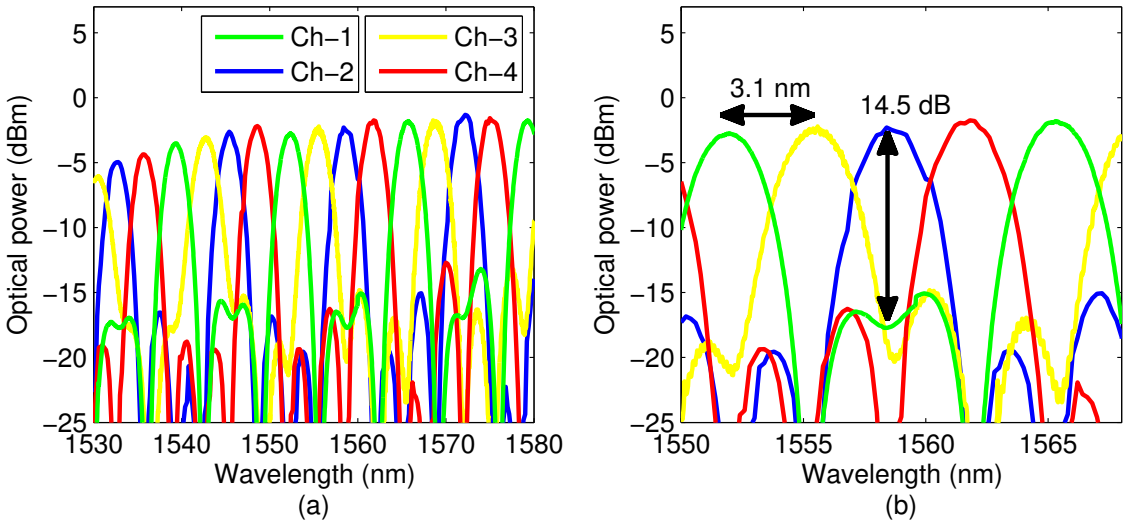



**Fig. 3.12** (a) Overlapped transmission response of the four optical output channels, (b) zoomed view of the optical response shows 14.5 dB crosstalk for $ch-2$.

### 3.2.3 160 Gb/s wavelength division multiplexing operation

Fig. 3.13 shows the experimental setup that was used to record the eye diagrams and to evaluate the BER performance of the four WDM channels. To demonstrate the WDM operation, four laser sources emitting CW light at wavelengths of 1552 nm, 1555.2 nm, 1558.4 nm and 1561.6 nm are set with an optical power of 10 dBm/channel. The wavelengths of the CW signal are chosen such that they are aligned with the transmission power peaks of the four channel optical demultiplexer (Fig. 3.12(b)).

Polarization controllers (PC-1 to PC-4) were inserted at each of the CW channel paths to maximize the extinction ratio of the modulated signal from the polarization sensitive electro-optic $LiNbO_3$ modulator. Prior to the external optical modulator, the four CW signals were multiplexed onto a single fiber using a 4:1 optical power coupler. The 4:1 optical power coupler has an insertion loss of around 6.4 dB. We measured around 9.5 dBm total optical power from the output of the 4:1 optical coupler. The optically multiplexed four

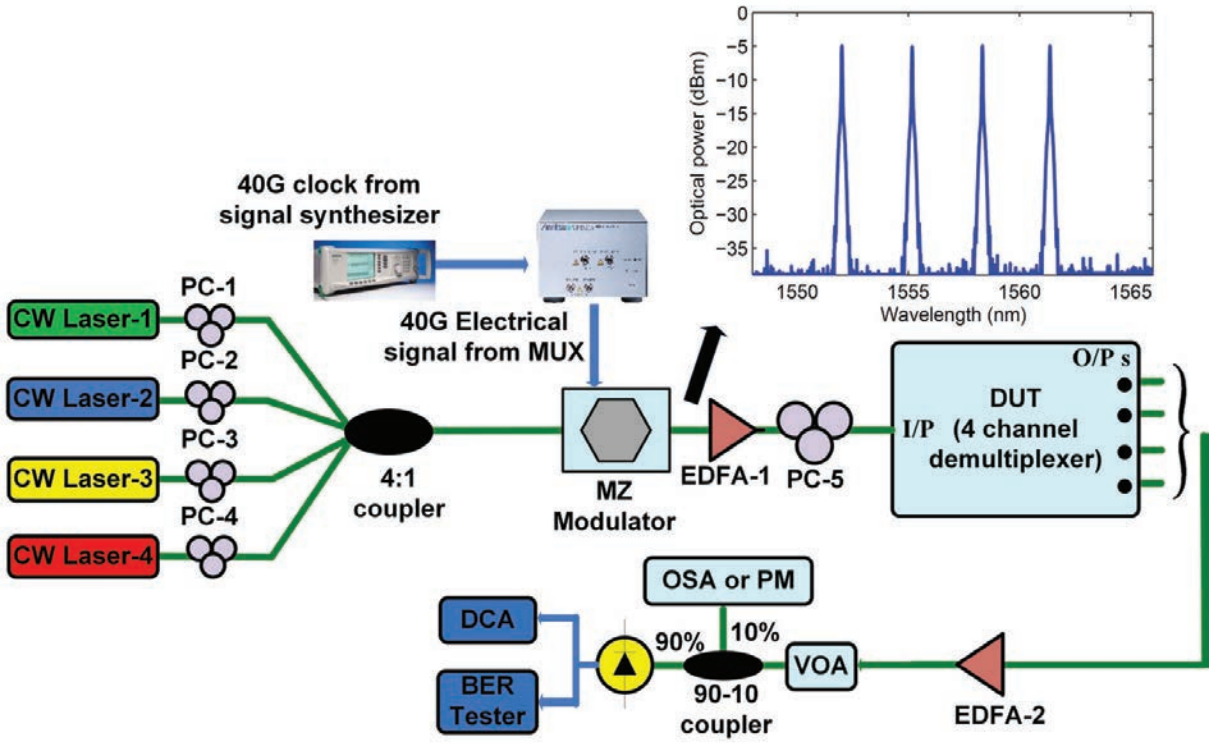



**Fig. 3.13** Experimental setup to capture eye diagrams and to evaluate BER performance of the optical demultiplexer. EDFA: Erbium doped fiber amplifier, PM: power meter, OSA: Optical spectrum analyzer, DCA: digital communication analyzer. Inset shows the optical spectrum of the four modulated channels.

CW channels were given as input to the commercial $LiNbO_3$ modulator. The modulator has a measured insertion loss of 7 dB. The optical modulator was driven by a 40 Gb/s non-return to zero (NRZ) on-off keying (OOK) electrical data generated from four 10 Gb/s pulse pattern generators (PPG). The four 10 Gb/s data generated from the PPGs were time multiplexed by the electrical MUX to create the 40 Gb/s data. The electrical signal is a PRBS data with a bit pattern of length $2^{31} - 1$.

To compensate the insertion loss of the optical modulator and the device under test, two EDFAs (EDFA-1 and EDFA-2) with 5 dB noise figure were used before and after the chip. A polarization controller (PC-5) is used before the chip to control the polarization state of the

input signal to the polarization sensitive $Si_3N_4$ waveguide. A variable optical attenuator (VOA) was used to control the received optical power by the commercial photodetector such that BER performance of the demultiplexer can be evaluated in terms of the average received power. A 90/10 optical coupler was used after the VOA to measure the amount of received power by the photodetector and to record the optical spectrum of the output signals. Fig. 3.14 shows the recorded eye diagrams from the DCA for each of the four channels of the demultiplexer.

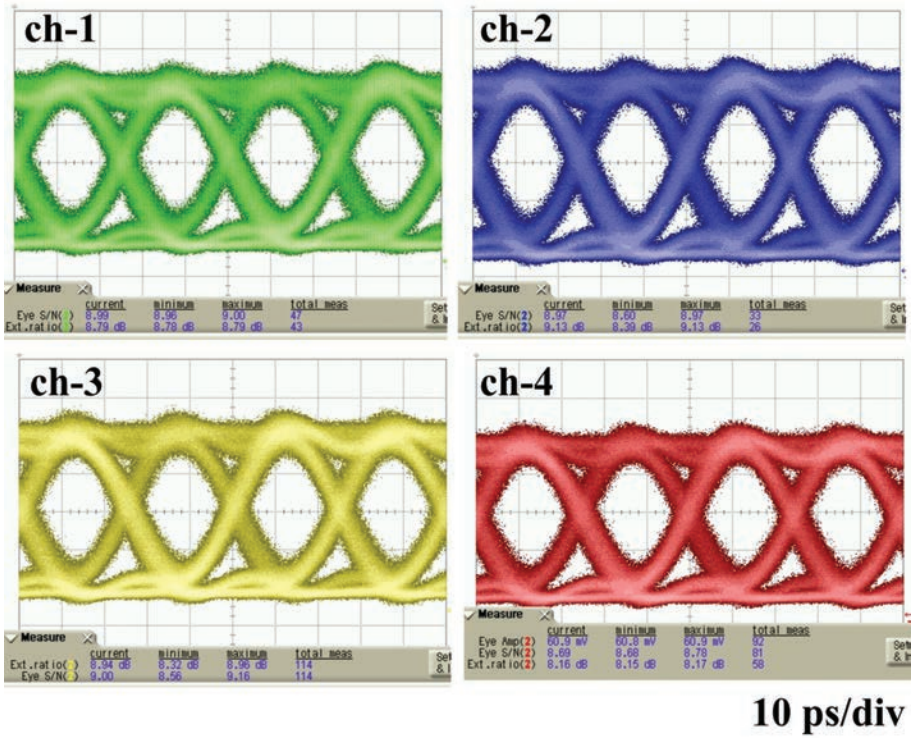



**Fig. 3.14** 40 Gb/s electrical eye diagrams obtained for the four channels at the output of the demultiplexer.

To measure the BER of all four channels, we used an electrical demultiplexer after the commercial photodetector to electronically demultiplex each of the 40 Gb/s channel to a 10 Gb/s channel. The 10 Gb/s data rate signal was used to measure the BER performance of each channel using a BER tester (Anritsu MU181040A-002). Fig. 3.15 shows that an average received power of -2.5 dBm is required at the photodetector input to achieve $1 \times 10^{-12}$ BER for all four channels. It should be mentioned that the BER performance result does not include errors due to the crosstalk between channels, as all the channels were modulated with same PRBS data. In the case of the back-to-back link, only one CW signal source is modulated without using the 4:1 optical coupler, where the device under test is replaced by an optical attenuator set to the insertion loss of the $Si_3N_4$ demultiplexer (approximately 11.1 dB). The power penalty of 1 to 1.5 dB for *ch-1* to *ch-4* is attributed to the different optical gain setting in the two EDFAs for the back-to-back case.

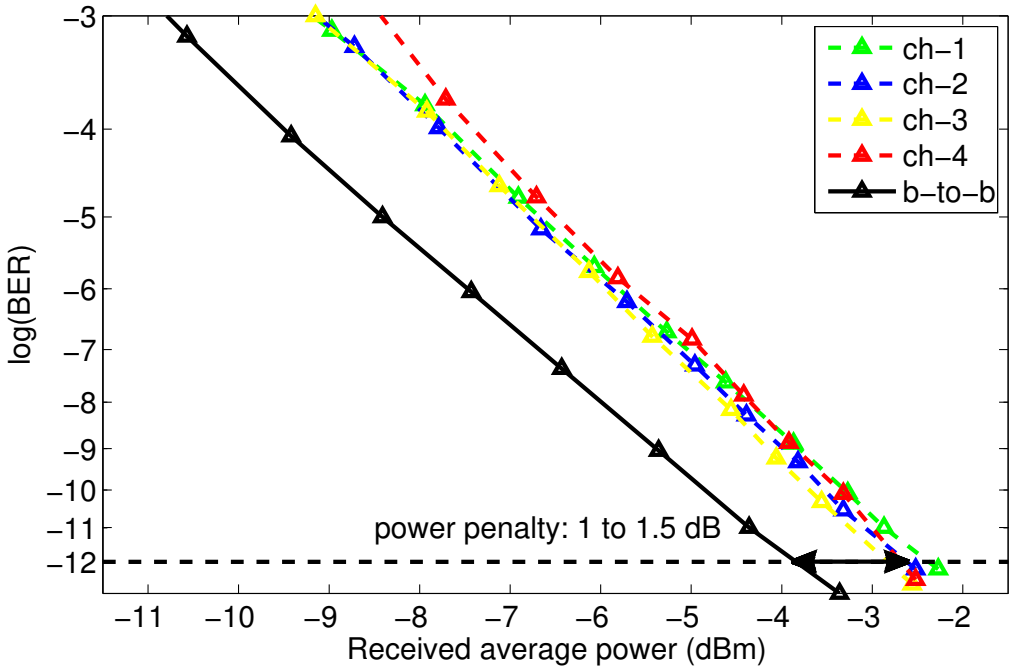



**Fig. 3.15** Measured BER as a function of the average optical power at the input of the photodetector for the back-to-back and four output channels of the demultiplexer.

## 3.3 Summary

The performance results of the 1 × 4 channel optical demultiplexer circuit reported in this chapter suggests that complex optical signal processing functionalities can be added to the $Si_3N_4$ waveguide based components (*i.e.*, phase shifting by thermal tuning, integrating optical buffers) such that more advantages from this ultra low-loss PIC technology can be harnessed. Low-loss AWG based demultiplexer on $Si_3N_4$ waveguide platform presented in [37] shows better performance than the 1 × 4 channel optical demultiplexer presented in this work. However, as explained above, for the applications where large optical time

delays are required as optical buffers in addition to the wavelength filtering, the AWG based MUX and MZI filter based demultiplexer can be used together to build the complete PIC on chip [46]. Using the integrated thermal tuners, the optical phase shift in the MZI delay arms can be controlled, which promises the scalability of the proposed demultiplexer architecture from four to eight channels by decreasing the adjacent channels'separation. In this chapter, we have designed the PIC using 3.1 dB/m propagation loss $Si_3N_4$ waveguides with PECVD top cladding. However, by changing the waveguide cross-section of $Si_3N_4$ waveguides (50 nm × 6.5 $\mu$m) and by increasing the minimum bend radius to 9.8 mm with the PECVD top cladding, lower propagation losses (*i.e.*, 0.5 dB/m in [28]) than a 3.1 dB/m loss are demonstrated. Therefore, in future designs, the losses of some application specific PICs (*i.e.*, that includes long optical buffer waveguides with MZI based demultiplexers [46]) can be reduced by using the $Si_3N_4$ waveguides demonstrated in [28].

# Chapter 4

# Passive Wavelength-Striped Mapping (PWSM) on the $Si_3N_4$ Waveguide

## 4.1 Introduction

In this chapter, we proposed an integrated PWSM device designed using low-loss $Si_3N_4$ waveguides [27]. In chapter 2, section 2.2, we have discussed that the ultra low-loss $Si_3N_4$ waveguide is a suitable PIC platform to design the long optical delay waveguides required in the PWSM device. The proposed PWSM technique requires simultaneous optical filtering and delaying each time segment of the serial data packet with respect to its adjacent channel by a pre-determined amount of time using optical buffer delay lines. In data center applications, the discrete fiber-based PWSM device needs to be integrated on a PIC to be used in the intra-card and inter-card schedulers proposed in [46, 87]. The card schedulers on the network interface cards (NIC) facilitate designing modular multiple rack-based optical interconnects, where they receive electrical data from the serial packet generators or microprocessors [88]. The E/O modules are also placed on the NIC

along with the PWSM device [46]. The PWSM PIC can be an important building block of the wavelength–striped based intra-card and inter-card schedulers, which are typically located in the top-of-rack (TOR) switches. Therefore, for practical purpose, an integrated approach becomes essential for highly paralleled optical interconnects with increased off-chip bandwidth density requirement in data communication. In this chapter, an integrated PWSM device is designed using low-loss $Si_3N_4$ waveguides [27].

The integrated optical PWSM circuit performs wavelength filtering of four channels and optically delays each channel from its adjacent channel by 16 ns. The insertion loss between the adjacent channels varies due to the integrated optical delay lines, with measured relative insertion loss of 0 dB, 9.7 dB, 19.1 dB and 28.7 dB in $ch-1$, $ch-2$, $ch-4$ and $ch-3$, respectively, with respect to $ch-1$. The optical demultiplexer section of the PWSM device is designed with a FSR of 12.8 nm and 3.2±0.1 nm wavelength separation between adjacent channels. The maximum crosstalk measured is 15.2 dB. A complete demonstration of the PWSM serial-to-WDM and WDM-to-serial process requires two PWSM devices with complementary optical delay lines. In such system, the serial-to-WDM process of the PWSM device is used for time-compression of the data packet at the transmitter side while the WDM-to-serial process of another PWSM device is used for time-expansion of the data packet at the receiver end. In this work, we design the later stage where the concept is experimentally demonstrated. The WDM-to-serial PWSM device reconstructs a 64 ns long data packet from four 16 ns data packets. The BER performance of the aggregated 64 ns packet is below $1\times10^{-9}$ for a received optical power of -6.7 dBm. The PWSM device exhibits a 2.3 dB power penalty. The results presented in this chapter are published in [89].

## 4.2 Passive wavelength-striped multiplexer design

The PWSM PIC requires an optical demultiplexer with integrated low-loss optical delay lines. $Si_3N_4$ waveguide based low-loss optical delay lines delay the optical channels with respect to the adjacent channel for a specific amount of time. In this design, multiple of 16 ns are used for a WDM-to-serial process on a 64 ns long payload serial packet. $Si_3N_4$ waveguides with a cross-sectional area of 2.8 $\mu$m $\times$ 72 nm is used for lower loss properties necessary for the four optical delay lines of 0 m, 3.1896 m, 6.3809 m and 9.5662 m. The detailed characterization of this waveguide structure is presented in chapter 3, with measured 3.1 dB/m propagation loss and group index ($n_g$) of 1.505 in the 1550 nm wavelength region.

In a conventional WDM based optical interconnect link, each wavelength is modulated using an optical modulator driven by the electrical serial data stream of the transmitter. The modulated optical wavelength channels are then multiplexed using an optical MUX before transmission. This process requires one modulator per wavelength challenging the scalability of the optical interconnect link due to strongly coupled power consumption to the increasing number of modulators and electronic circuitry. In our proposed wavelength-striped data transmission process, the same data packet is simultaneously encoded on all WDM channels using one modulator. By time scaling the data packets from all the transmitters, the overall interconnect capacity can be scaled up [46]. A novel PWSM process enabling such process was initially demonstrated experimentally in [61], where one modulator was used to modulate eight wavelength channels with the same electrical data stream. The wavelength-striped process was implemented using discrete fiber-based off-chip delay lines and optical wavelength demultiplexer/multiplexer. However, time delaying the data packets with fiber delay lines required long fiber lengths, which becomes impractical

to implement as packet length increases in time. We first proposed the theoretical model of an integrated PWSM device with low loss delay waveguides in [46]. Fig. 4.1 shows the schematic diagram of the PWSM PIC with four channels. In Fig. 4.1, the outputs (*ch-1*, *ch-2*, *ch-3* and *ch-4*) are the results of the PWSM circuit filtering each of the wavelengths and simultaneously time delaying the wavelength channels *ch-1* ($\lambda_1$), *ch-2* ($\lambda_3$), *ch-3* ($\lambda_2$) and *ch-4* ($\lambda_4$) by 0 ns, 16 ns, 48 ns and 32 ns, respectively.

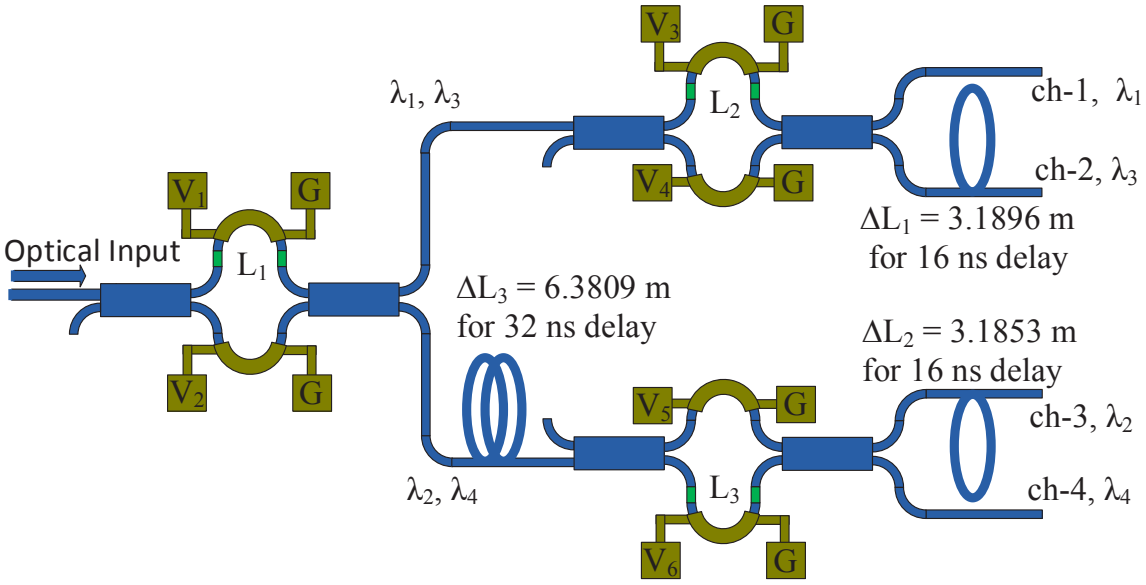



**Fig. 4.1** Schematic of the four channel PWSM multiplexer architecture with the integrated Cr heater on the delay arms of the MZI(not to scale). $V_1$ to $V_6$: electrical pads to apply the DC voltages for thermal tuning, G: ground pads, $L_1$ to $L_3$: integrated delay waveguide lengths (in green color).

In this section, we present the working principle of the integrated PWSM device. Next, we describe the design method of the long delay waveguides and their integration with the four channel optical demultiplexer.

### 4.2.1 Working principle of the PWSM device

Full functionality of the PWSM process is described in chapter 2 section 2.1.2, which requires two PWSM devices with complementary delay waveguides. In [61], eight WDM channels were modulated simultaneously with the same 2.5 Gb/s payload of 128 ns. The first PWSM device was used to apply 16 ns delay between each of the eight channels. The output of the first PWSM device was then gated to form the eight channels packet of 16 ns, such that the entire 128 ns long serial data packet was converted to a compressed 16 ns long WDM parallel packet. To recover the 128 ns long serial data packet from the 16 ns long parallel data packet, another PWSM device was used in [61] where the optical delay lines were oriented in a complementary manner. The complementary-oriented waveguide delay lines in the two PWSM devices also remove the optical power non-uniformity among the channels. This is achieved by applying increasing and decreasing order of time delays to the channels in the two PWSM devices. For example, the first channel (*ch-1*) in the PWSM device shown in Fig. 4.1 has no time delay waveguides in its optical path, whereas in the second PWSM device of the receiver node (not shown in Fig. 4.1), a 64 ns time delay is applied to *ch-1*.

In this chapter, to explain the working principle of the PWSM device, we focus on one PWSM device and demonstrate how a 64 ns long data packet can be regenerated from four 16 ns data packets encoded on four distinct WDM channels. The same PWSM device can be used to demonstrate the full passive wavelength-striped process described in [61]. The working principal of the proposed device is shown in Fig. 4.2, where four WDM channels are simultaneously modulated with the same 64 ns long data packet using one modulator (not shown in Fig. 4.2). However only the first 16 ns of the packet segment contains information bits, where in the next 48 ns, the information bits are set to zero. The PWSM device filters

the four WDM channels and time delay the adjacent channels by 16 ns. At the output of the device, a 64 ns long packet is formed over the four channels which can then be optically multiplexed and detected by an optical broadband receiver. It should be mentioned that, in this demonstration, each 16 ns segment contains the same data, whereas in [61] each of the 16 ns segments contains distinct data packet.

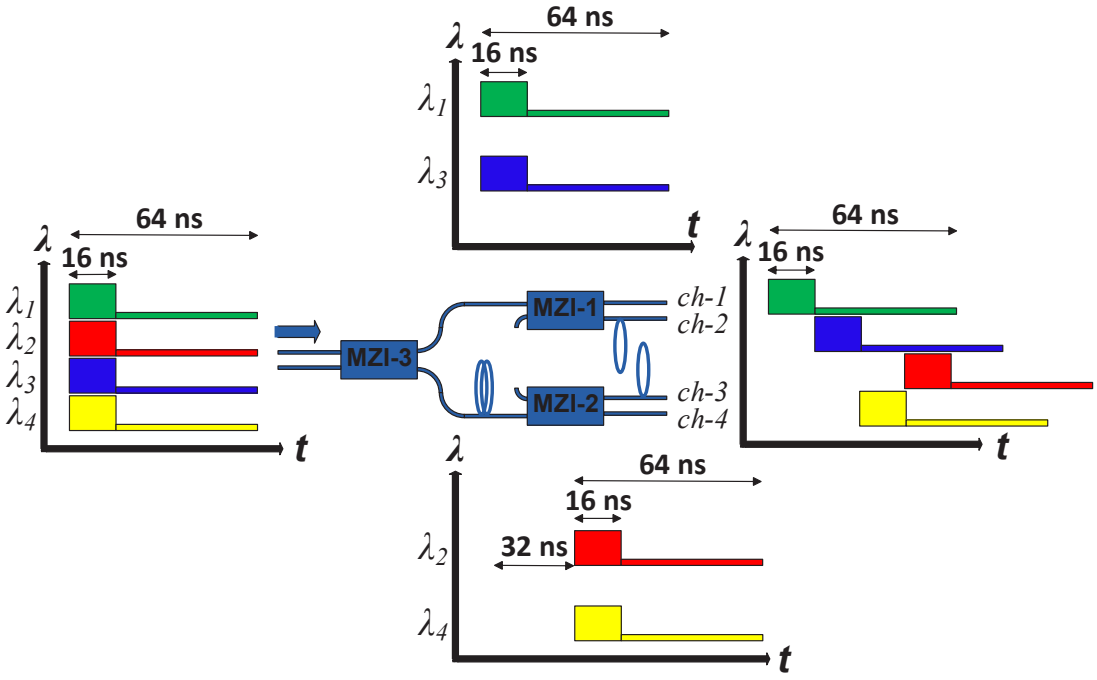



**Fig. 4.2** Working principle of the proposed PWSM device. Four WDM channels ($\lambda_1$, $\lambda_2$, $\lambda_3$ and $\lambda_4$) containing the same data are filtered to four wavelength channels and delayed with respect to the adjacent channels by 16 ns.

The optical demultiplexer section of the PWSM device has a channel separation of 400 GHz or 3.2 nm such that passive wavelength-striped process can be applied to 25 Gb/s or 50 Gb/s modulated data channels. While data rate and modulation format transparent, the current constraint of the demonstrated device is that the total packet length must be

kept to 64 ns. Different delay lines need to be used for a different packet length and/or a different number of WDM channels. At higher data rate, the total number of bits per wavelength obviously increases proportionally. For example at 25 Gb/s and 50 Gb/s data rate 1600 bits or 3200 bits can be allocated per packet, respectively, for serial to parallel or parallel to serial conversion.

The data rate of the wavelength-striped channels in the proposed device is set to 25 Gb/sec based on the 100 G Ethernet standard. In a network with four pairs of PWSM devices in the transmitter and receiver nodes, 100 G aggregated bandwidth can be achieved by the 4 × 25 Gb/sec WDM channels with time division multiplexing (TDM) interleaving [61]. At present short reach interconnect distance from the server to switches is ∼2 m [2]. Therefore, the proposed PIC is suitable for used within the NICs between the serial packet generators.

### 4.2.2 Design of the long delay waveguides

The PWSM circuit demonstrated in this work, consists of MZI based filters incorporated with relatively long optical delay lines ($\Delta L_1$, $\Delta L_2$, and $\Delta L_3$ in Fig. 4.1), where the longest delay line is 9.5662 m for $ch-3$ to implement 48 ns time delay. In the long length delay waveguides, the time delay mismatch between the wavelength channels due to the dispersion effect needs to be taken into consideration. We have calculated the group velocity dispersion (GVD) of the 220 nm × 2.8 $\mu$m cross-section $Si_3N_4$ waveguide from the group index ($n_g$) of the waveguide, by using the following equation:

$$D = \frac{1}{c_0}\frac{dn_g}{d\lambda}, \text{ where } c_0 \text{ is the velocity of light} \tag{4.1}$$

Fig. 4.3(a) and (b) shows the FDTD simulation results of the group index and GVD

of the waveguide over the wavelength range from 1530 nm to 1580 nm. The dispersion length of the waveguide for 25 Gb/sec data rate signal can be estimated from the following equation [90]:

$$L_D = \frac{2\pi c_0 T_0^2}{\lambda^2 |D|} \tag{4.2}$$

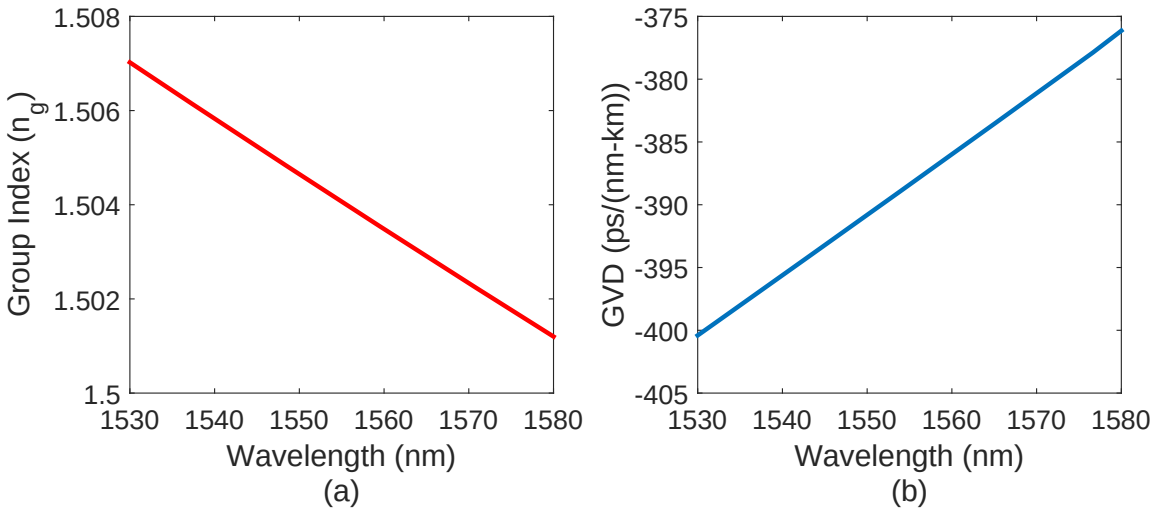



**Fig. 4.3** Variation in the (a) group index ($n_g$) and (b) group velocity dispersion (GVD) of the 220 nm × 2.8 $\mu$m cross-section $Si_3N_4$ waveguide for the wavelength range from 1530 m to 1580 m.

In equation 4.2, $D$ is the GVD parameter of the waveguide and $T_0$ represents the half–width of a Gaussian pulse at $1/e$ intensity point. We assume $T_0 = 10$ ps ($T_0 \leq T_B/2\sqrt{2}$, calculated from [90]) for the 25 Gb/sec data rate signal (one bit time duration, $T_B = 40$ ps). The calculated value of the dispersion length for 25 Gb/sec data rate signal is $L_D = 200.7$ m, assuming $D = -391$ ps/(nm-km) at 1550 nm wavelength from Fig. 4.3(b). The longest delay line in the PWSM device is 9.5662 m (calculated in the next paragraph), which is approximately 20 times less than the dispersion length. Therefore, at 25 Gb/sec data rate, the output optical waveform from the PWSM device will not suffer distortion due to the

dispersion effect.

To compensate the time delay mismatch between the four WDM channels due to dispersion, the required lengths of the delay lines are then determined by solving the following set of equations,

$$\Delta L_1 = \frac{c_0 \times T_3}{n_{g3}} \tag{4.3}$$

$$\Delta L_2 + \Delta L_3 = \frac{c_0 \times T_2}{n_{g2}} \tag{4.4}$$

$$\Delta L_3 = \frac{c_0 \times T_4}{n_{g4}} \tag{4.5}$$

Table 4.1 shows values of the input parameters (time delay, $T$ and group index, $n_g$) in equations (4.3), (4.4), and (4.5). The group index of the waveguide at each of the wavelengths is obtained from Fig. 4.3(a). Table 4.1 also shows the calculated delay waveguide lengths.

**Table 4.1** Delay waveguide length in the PWSM device

| Channel and wavelength | Time Delay (ns) | Group index | Delay Length (m) |
|---|---|---|---|
| 1. ch-2, $\lambda_3$ | $T_3 = 16$ | $n_{g3} = 1.5049$ | $\Delta L_1 = 3.1896$ |
| 2. ch-3, $\lambda_2$ | $T_2 = 48$ | $n_{g2} = 1.5053$ | $\Delta L_2 + \Delta L_3 = 9.5662$ |
| 3. ch-4, $\lambda_4$ | $T_4 = 32$ | $n_{g4} = 1.5045$ | $\Delta L_3 = 6.3809$ |

From Table 4.1, it is seen that to achieve a time delay of approximately 16 ns between adjacent channels, the length of the delay waveguides needs to be accurate within 0.1 mm or 100 $\mu$m. We estimate about 0.5 ps time delay mismatch for 100 $\mu$m waveguide length offset from the designed length. Therefore, considering the target data rate of 25 Gb/s (one

bit duration = 40 ps), we set the length of the waveguide to be accurate up to 100 $\mu$m. Achieving this length accuracy in the discrete fiber delay lines based PWSM device is challenging. However, in the $Si_3N_4$ waveguide based integration technology 100 $\mu$m length accuracy is achievable, considering the width of the waveguide is 2.8 $\mu$m.

### 4.2.3 Integration of the delay waveguides with the 4-channel demultiplexer

The optical demultiplexer without the integrated delay lines has been designed and characterized in chapter 3. The four-channel device consists of three 2×2 MZI based filters to demultiplex four 40 Gb/s WDM channels. A spiral-shaped 1.5 m long delay waveguide test structure is also characterized in chapter 3 to determine the waveguide propagation loss. In this work, three spiral-shaped long delay waveguides ($\Delta L_1$, $\Delta L_2$, and $\Delta L_3$) are monolithically integrated with the four-channel optical demultiplexer to design the PWSM device. The length of the optical delay waveguides are set to time delaying the 25 Gb/sec data rate channels in the multiples of 16 ns. On the other hand, the optical path delay lengths in the MZIs ($L_1$, $L_2$ and $L_3$) are designed to achieve a channel spacing of 3.2 nm (or 400 GHz) at the output of the PWSM device. $MZI_1$ requires a $\pi/2$ phase delay for effective filtering of channels $\lambda_1$ and $\lambda_3$, which is achieved by adding an extra delay length of 0.257 $\mu$m for this $\pi/2$ delay. To effectively tune the phase delay to $\pi/2$, we include a 12 mm long Cr heater ($V_1$ to $V_6$) on top of each of the MZI delay arms. The Cr heaters are monolithically integrated with the $Si_3N_4$ waveguide based PWSM device. The MZIs are designed using two 2×2 MMI-based couplers to achieve the optical broadband 3 dB coupling required for filtering in this proposed wavelength-striping technique. Fig. 4.4 shows the layout of one segment of the PWSM device containing the longest delay waveguide ($\Delta L_3$ = 6.3809 m) and one of the MZI filters.

The area of the PWSM device on the PIC is 4.2 cm × 4.7 cm. The input/output waveg-

uides of the device are routed beyond this region to the edge of the chip to accommodate other test devices. The on-chip area of the longest delay waveguide ($\Delta L_3 = 6.3809$ m) is 2.3 cm × 2.3 cm. The whole PIC (area: 7 cm × 7 cm) also includes test devices such as a four-channel optical demultiplexer, MMI couplers, MZI filters, bent and straight waveguides.

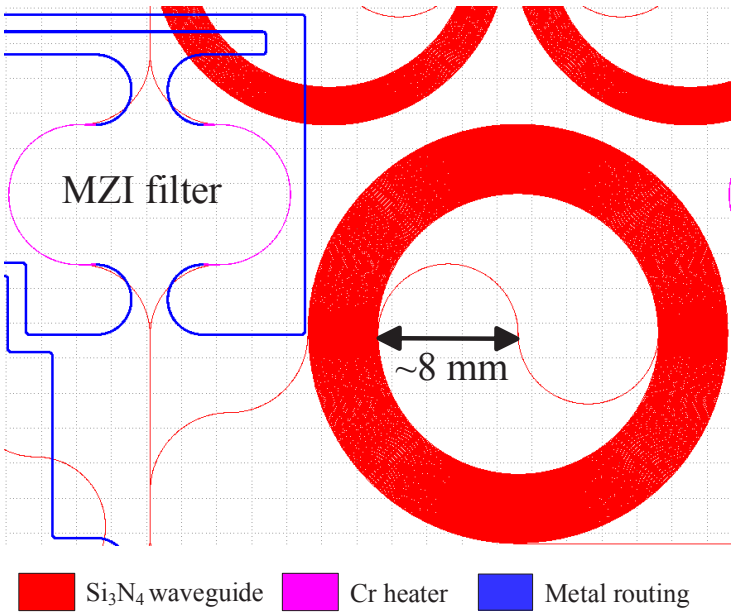



**Fig. 4.4** Layout of the longest optical delay waveguide, $\Delta L_3 = 6.3809$ m, connected to one of the MZI filters of the PWSM circuit.

## 4.3 Experiment setup and results

To characterize the PWSM device, we first determine the optical transmission response of the four wavelength channels. Next, the time delays between the adjacent channels is evaluated using a modulated optical waveform. The experimental results obtained are utilized to form a 64 ns long data packet from the four 16 ns long data segments. We also determine the BER and power penalty of the 64 ns long data packet generated by the

PWSM device.

### 4.3.1 Optical transmission response of the PWSM device

Fig. 4.5(a) shows the experimental setup to characterize the transmission response of the PWSM device (device under test, DUT) and to determine the insertion loss of each of the four channels of the PWSM device which are critical in this proposed system. In Fig. 4.5(b), the actual photograph of the PIC along with the fiber array and DC electrical probe has been shown. The optical phase shift in the delay arms of the MZI is thermally tuned to reduce crosstalk between the channels by applying a set of DC voltages for thermal heating in the corresponding delay arms. The thermal heating occurs from the electrical power loss in the resistive load of the heater. The applied DC voltages in the thermal heaters of the delay arms were $V_2 = 1.5$ V (0.31 mA), $V_3 = 4.1$ V (0.95 mA) and $V_6 = 2.4$ V (0.55 mA). The total electrical power consumption of the PWSM device from the thermal heaters is 5.68 mW. The wavelength of a CW laser source is swept from 1525 nm to 1575 nm with a constant optical power at 12 dBm. A polarization controller is used at the input of the PWSM chip to reduce the polarization dependent loss in the $Si_3N_4$ waveguide. The optical output power from each of the four output channels of the PWSM circuit ($ch-1$, $ch-2$, $ch-3$ and $ch-4$) is recorded separately.

Fig. 4.6 shows the optical transmission response of each of the four channels of the PWSM device normalized to the optical output power of a reference straight $Si_3N_4$ waveguide. From this figure, the side lobe suppression ratio for *ch-1*, *ch-2*, *ch-3* and *ch-4* are 14 dB, 17 dB, 14 dB and 16 dB, respectively, for a 50 nm wavelength range from 1525 nm to 1575 nm. The FSR range for *ch-1*, *ch-2*, *ch-3* and *ch-4* are 12.75 nm, 12.8 nm, 12.8 nm and 12.75 nm, respectively. The optical insertion loss in the first channel (*ch-1*) is 1.7 dB at 1553.5 nm. From this figure, it can be seen that there is an insertion loss difference of

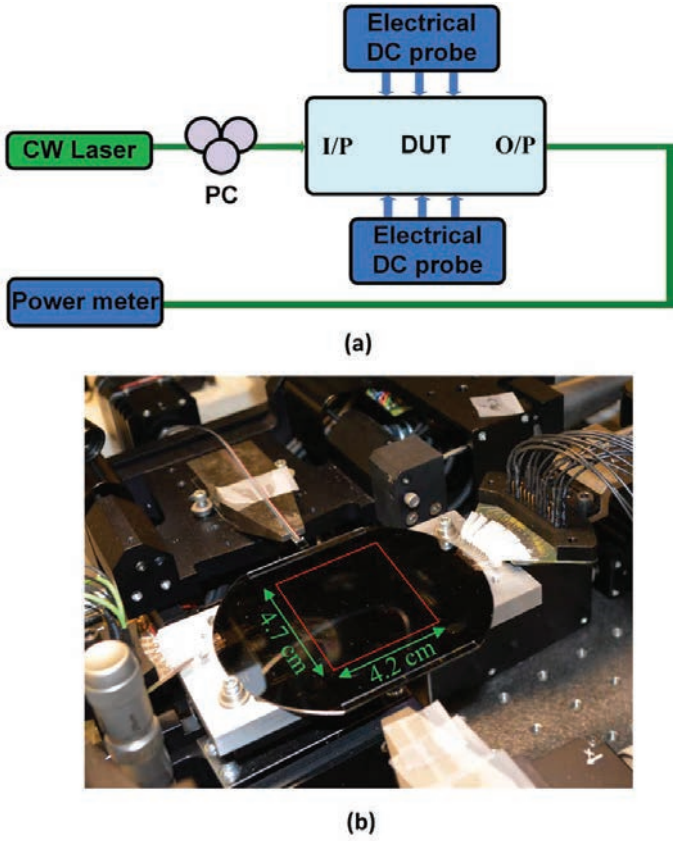



**Fig. 4.5** (a) Experimental setup to measure the transmission responses of the four channel PWSM device, (b) Photograph of the test setup with the PIC, fiber array and DC electrical probes. The area and location of the PWSM device on PIC is highlighted by the red rectangle.

approximately 9.7 dB between two adjacent channels. This is the incremental loss for an optical delay of 16 ns corresponding to 3.1 dB/m propagation loss in the delays. The insertion loss is 11.4 dB for the second channel (*ch-2*), 20.8 dB for the fourth channel (*ch-4*), and 30.4 dB for the third channel (*ch-3*).

Fig. 4.7 illustrates the overall optical transmission response of the PWSM device by overlapping the response of each channel removing the additional insertion loss from corresponding delay lines. A narrow spectral response is shown in Fig. 4.7(b) from 1539 nm to 1553 nm with the transmission peaks of *ch-1*, *ch-2*, *ch-3* and *ch-4* found at 1541.1 nm,

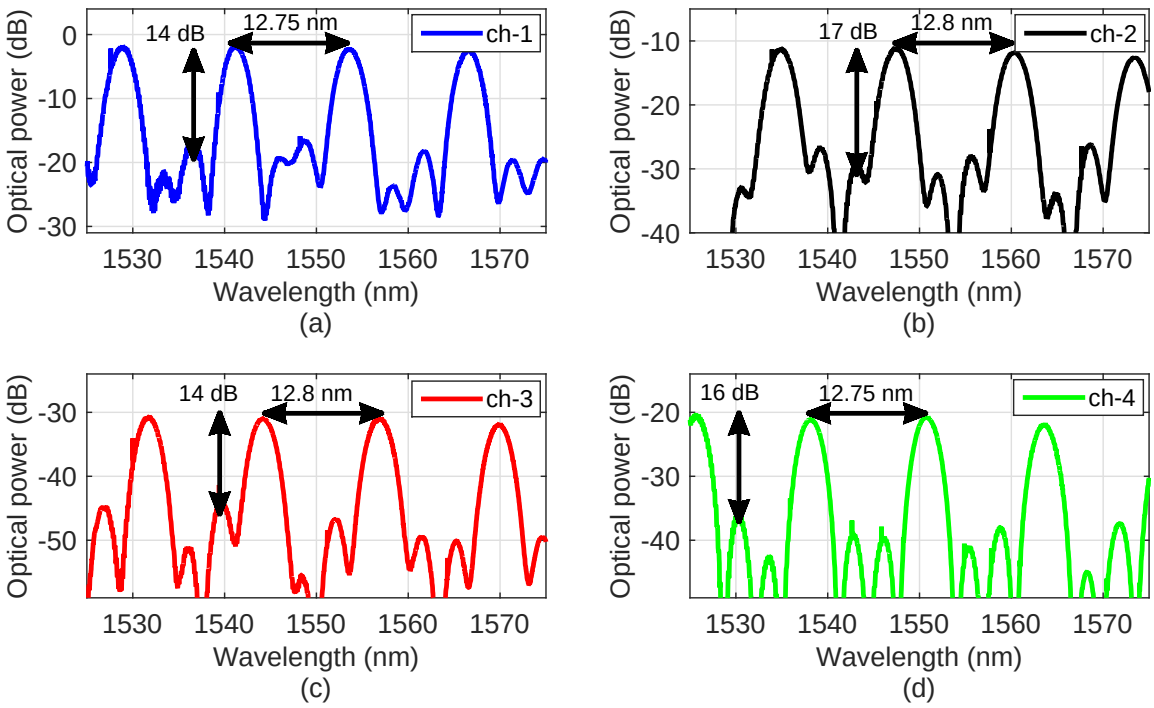



**Fig. 4.6** Normalized transmission response of the four optical output channels (a) *ch-1*, (b) *ch-2*, (c) *ch-3* and (d) *ch-4*.

1547.45 nm, 1544.3 nm and 1550.7 nm, respectively. This confirms a wavelength separation of 3.2 nm between *ch-1* and *ch-3*, 3.25 nm between *ch-2* and *ch-4*, and 3.15 nm between *ch-2* and *ch-3*. The FSR and wavelength separation between two channels is within the 0.1 nm range of the simulation result. We used the results of Fig. 4.7(b) to set wavelength of the four CW lasers within a wavelength range from 1541.1 nm to 1550.7 nm to demonstrate the proposed PWSM operation.

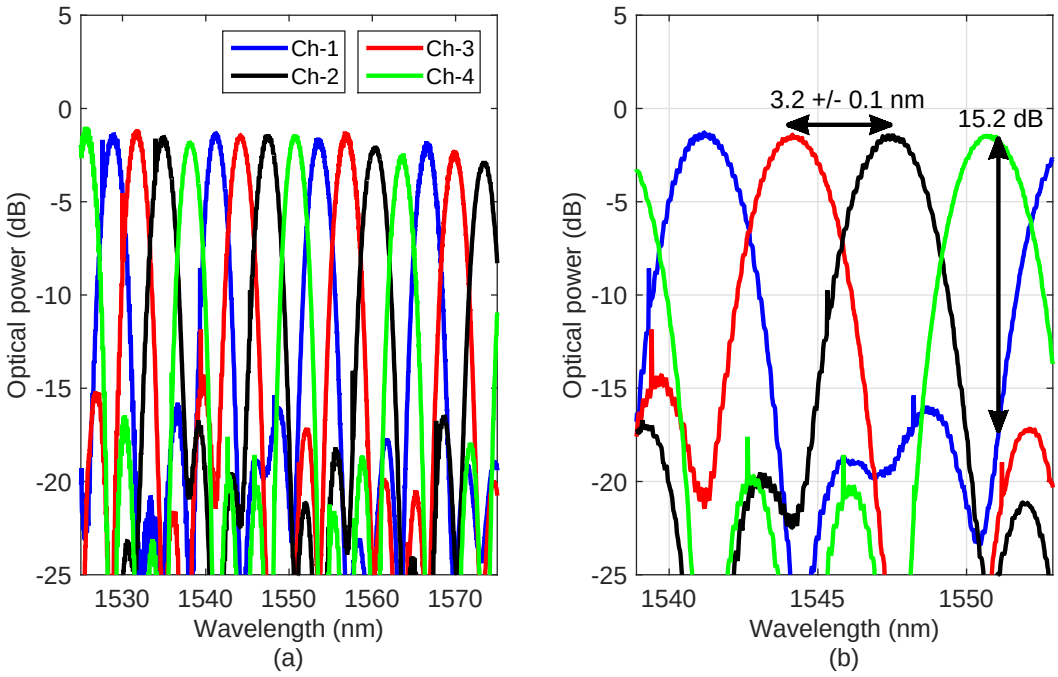



**Fig. 4.7** (a) Overlapped transmission response of the four optical output channels. (b) Zoomed view of the optical response shows 15.2 dB crosstalk for *ch-4*.

### 4.3.2 Time delay between adjacent channels

The operation of the PWSM process is demonstrated by constructing a 200 byte long serial packet (1,600 bits) from four 50 byte long packets (400 bits). Full serialization and deserialization of the whole 200 byte long packet requires simultaneous operation of two different PWSM photonic circuits, where each of the PWSM circuit performs wavelength to time delay mapping in a complementary manner. As one version of the PWSM circuit was designed, the 50-byte long four WDM packets to a 200-byte long serial packet conversion process is demonstrated in this paper. To demonstrate the concept, each of the four WDM channels is modulated by a 200 byte long electrical signal, where the first 50 byte contain data and the remaining 150 byte are set to zero. The first 50 byte or 400 bits contain three sets of $2^7 - 1$ PRBS bits and nineteen trailing zeros. The last 1200 bits of each data

packets are set to zero. The PWSM circuit receives the four WDM channels, where each of the WDM channel contains 50 byte long data at the same time segment. At the output of the PWSM circuit, four WDM channels are simultaneously filtered, time delayed and multiplexed to form a 200 byte long data packet.

In Fig. 4.8, the experiment set up used to check the time delay between the adjacent WDM channels is shown. Four laser sources emitting CW light at wavelengths of 1541.1 nm, 1544.3 nm, 1547.45 nm, and 1550.7 nm are set with an optical power of 12 dBm per channel. The wavelengths of the CW signal are chosen such that they are aligned with the transmission power peaks of the four channel optical demultiplexer section of the PWSM (Fig. 4.7(b)). The channels are multiplexed onto a single fiber with a 4:1 multiplexer and modulated simultaneously with a 33 GHz bandwidth lithium niobate amplitude modulator at 25 Gb/s. The optical multiplexer has a 6.2 dB insertion loss. The extinction ratio of the optical modulator is approximately 14 dB. The extinction ratio of the polarization sensitive modulator is maximized for each individual wavelength by using polarization controllers prior to the 4:1 multiplexer. In this demonstration, the modulator is driven by an amplified bit sequence, representing one 200 byte long packet, generated at 25 Gb/s by a programmable pattern generator. The simultaneously modulated optical wavelengths are amplified by an EDFA (EDFA-1) and launched into the demultiplexing input port of the PWSM device. The optical output signal from each of the four optical output ports of the PWSM circuit are coupled to a single mode fiber one at a time. A second EDFA (EDFA-2) is used before the photodetector to compensate for the insertion loss of the PWSM circuit. As each of the channels has different optical loss due to the different delay lengths, the optical power amplification in the two EDFAs is set accordingly.

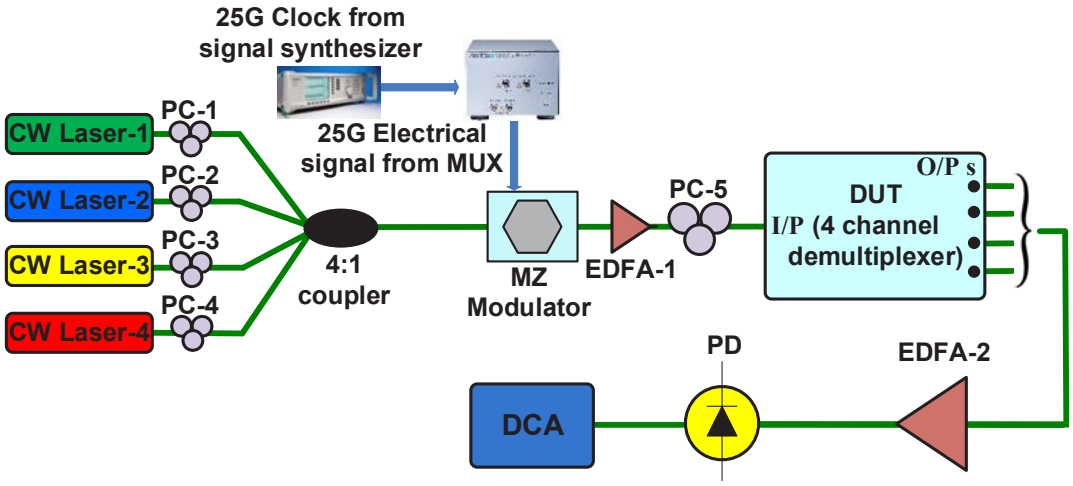
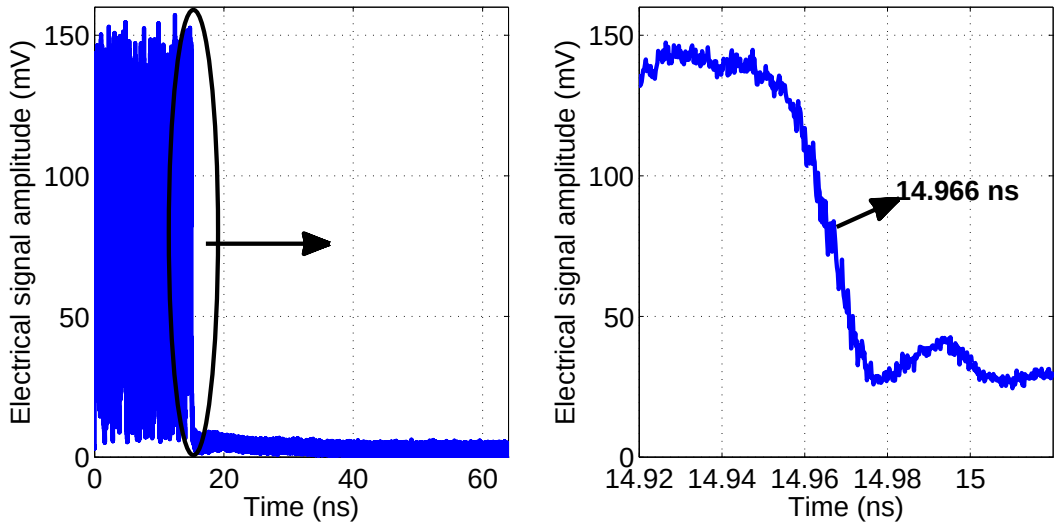
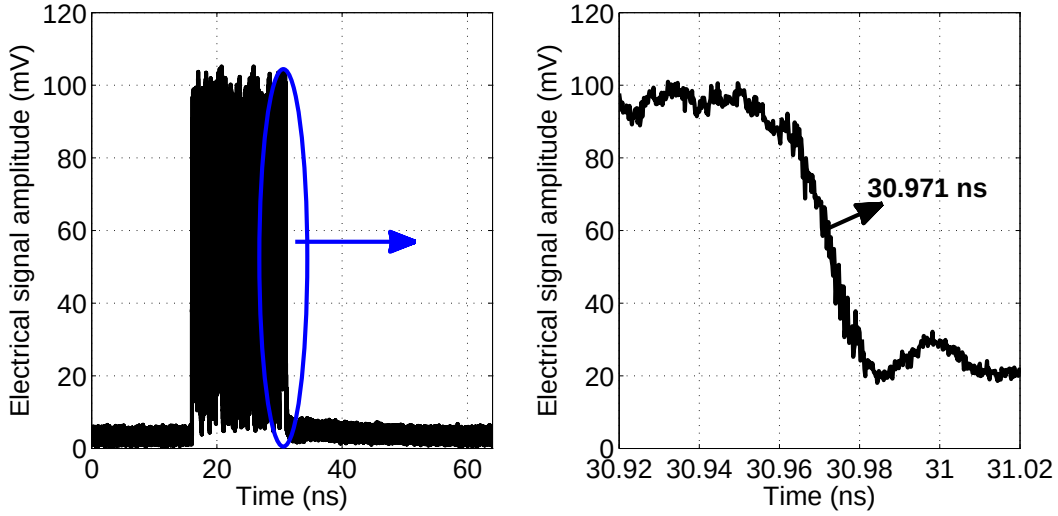



**Fig. 4.8** Experimental setup to capture pattern locked data for each of the four channels separately. EDFA: Erbium doped fiber amplifier, PC: polarization controller, VOA: variable optical attenuator, PD: photodetector, DCA: digital communication analyzer.

Fig. 4.9(a) to (d) shows the pattern locked data (one set of 1600 bits captured from 86100D Infiniium DCA) for each of the output channels (*ch-1* to *ch-4*), and the corresponding time delay between the adjacent channels. To accurately measure the time delay between channels, the last bits transition of each of the received signal is shown at the right. The measured time delay between adjacent channels is within 16.010 ns ± 5 ps. Thus, the time delay offset between the adjacent channels is accurate within ±5 ps (or ±0.125UI at 25 Gb/s).


Electrical signal amplitude (mV)
Time (ns)
14.966 ns

(a)


Electrical signal amplitude (mV)
Time (ns)
30.971 ns

(b)

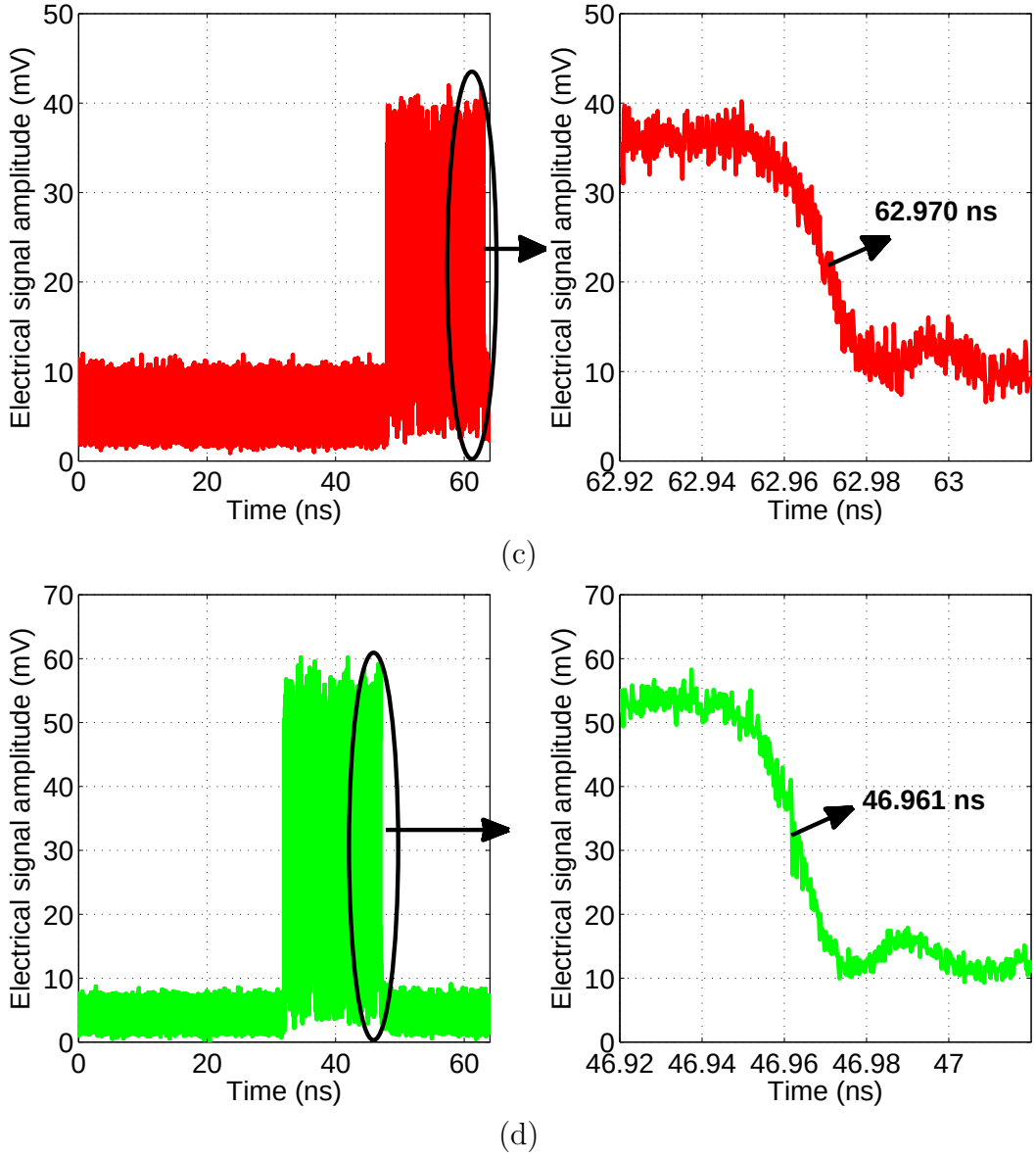



**Fig. 4.9** 64 ns (200 byte) long patterned locked data and the corresponding time delay for (a) *ch-1*, (b) *ch-2*, (c) *ch-3* and (d) *ch-4*.

### 4.3.3 Parallel-to-serial conversion validation

In this section, we present the experimental method of parallel-to-serialization of the four data segments using the PWSM device. The reconstructed 200 byte serial data should

be 64 ns long where each of the channels bit information is contained within each of the 16 ns long block. Fig. 4.10 shows the experiment set up to validate the 200 byte long data packet from the four 50 byte long data packets. In this setup, an additional 4:1 optical coupler is inserted after the first EDFA (EDFA-1). The 4:1 optical coupler divides equally the optical power of the signal to its four optical port. As such, each of the four optical output port of the coupler carries all four WDM signals. The PWSM chip is designed to demultiplex a single WDM channel from each of its four input ports, and then multiplex the four channels at its output port. The delay lines inside the PWSM circuit subsequently add 16 ns delay between the adjacent channels. A fiber array with 250 $\mu$m pitch is used to simultaneously couple the four signals to the four input ports of the PWSM device. VOAs are used to attenuate the optical power of the channels suffering less optical loss compared to the other wavelength channels, *i.e.*, *ch-1* suffers 9.7 dB less loss than *ch-2* inside the PWSM device. Using the VOA, the optical power of the WDM channels is adjusted up to a certain limit such that the whole packet formed by the PWSM chip can be amplified using the second EDFA (EDFA-2). Polarization controllers are used before each channels of the PWSM chip. External optical delay lines (ODL) are used to compensate time delay mismatch occurred due to the small fiber length difference in the VOA, PC and fiber arrays of the adjacent channels. To compensate for the insertion loss of the DUT, a second (EDFA-2) with 5 dB noise figure is used after the chip. A VOA is used to control the received optical power by the commercial photodetector to measure BER performance of the PWSM device in terms of the average received power at the photodetector. A 90/10 optical coupler and a power meter is used after the VOA to measure the average received power. As discussed in section 4.2.1, in a complete PWSM based network [61], two PWSM devices in the transmitter and receiver nodes would remove the optical power non–uniformity due to the complementary oriented optical delay waveguides. In such a

scenario, the optical power coupler used after the EDFA-1 in Fig. 4.10 would be replaced by a wavelength multiplexer integrated on the PWSM device. An AWG based optical multiplexer demonstrated using the similar $Si_3N_4$ waveguide based platform in [37] can be integrated with the PWSM circuit for this purpose.

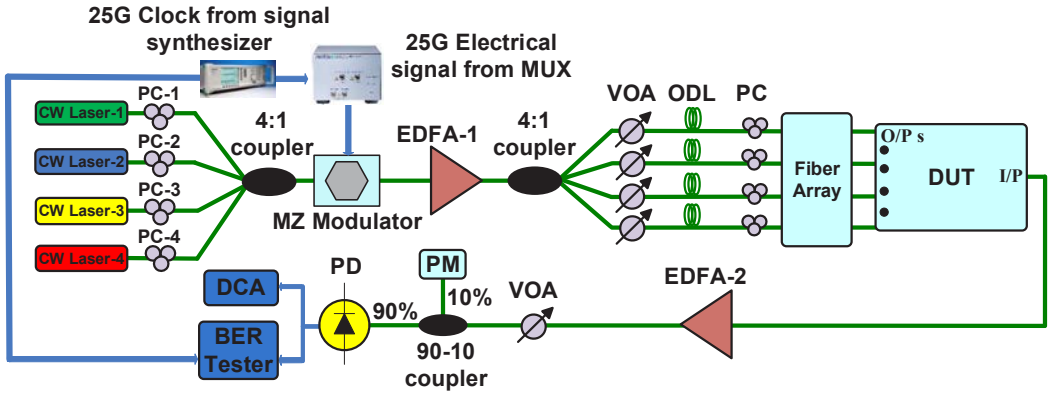



**Fig. 4.10** Experimental setup to reconstruct the 64 ns long packet and to evaluate the BER performance of the PWSM device. PC: polarization controller, EDFA: Erbium doped fiber amplifier, VOA: variable optical attenuator, PM: power meter, PD: photodetector, DCA: digital communication analyzer.

Fig. 4.11 shows the recorded patterned locked electrical data packet from the DCA. The 64 ns long data packet contains four 16 ns block of data from the four WDM optical channels. The electrical peak to peak voltage swing varies at every 16 ns time duration as each of the four channels suffers different optical loss in the PWSM device. However, as mentioned in the above paragraph, the peak to peak voltage difference between the packet segments were reduced by using a separate optical attenuation for each channel.

The bit error rate of the constructed packet is measured after the photodetector. Since the transmitted data from the PPG and received data are different (Fig. 4.9 and Fig. 4.11), the expected 200 bit long data pattern is loaded onto the BER tester, which contains four repeated blocks of the transmitted bit patterns from the PPG. Both the PPG and BER tester are synchronized to the same clock signal from a clock synthesizer module such that

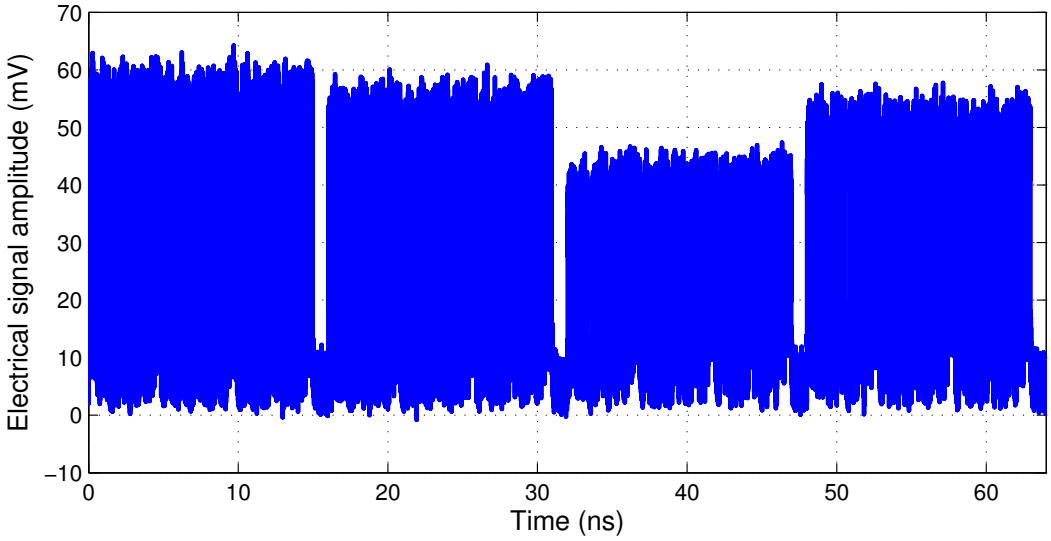



**Fig. 4.11** Aggregated reconstructed 64 ns long packet at the output of the PWSM device from four wavelengths ($\lambda_1$ to $\lambda_4$) each carrying a 16 ns long segment of the data.

the BER tester is synchronized to the PPG. Fig. 4.12 shows the BER of the received packet with respect to the average received power at the photodetector. The BER of the photonic link with the PWSM device is compared with a back to back case, where the whole 64 ns packet (four segments of 16 ns data) is used to modulate the first wavelength channel only. From the BER result in Fig. 4.12, a 2.3 dB power penalty is observed for the PWSM interface. The power penalty can be attributed to the uneven peak to peak voltage, time delay mismatch and varying extinction ratio of the four wavelength channels across the full 64 ns packet generated from the PWSM device (as shown in Fig. 4.11).

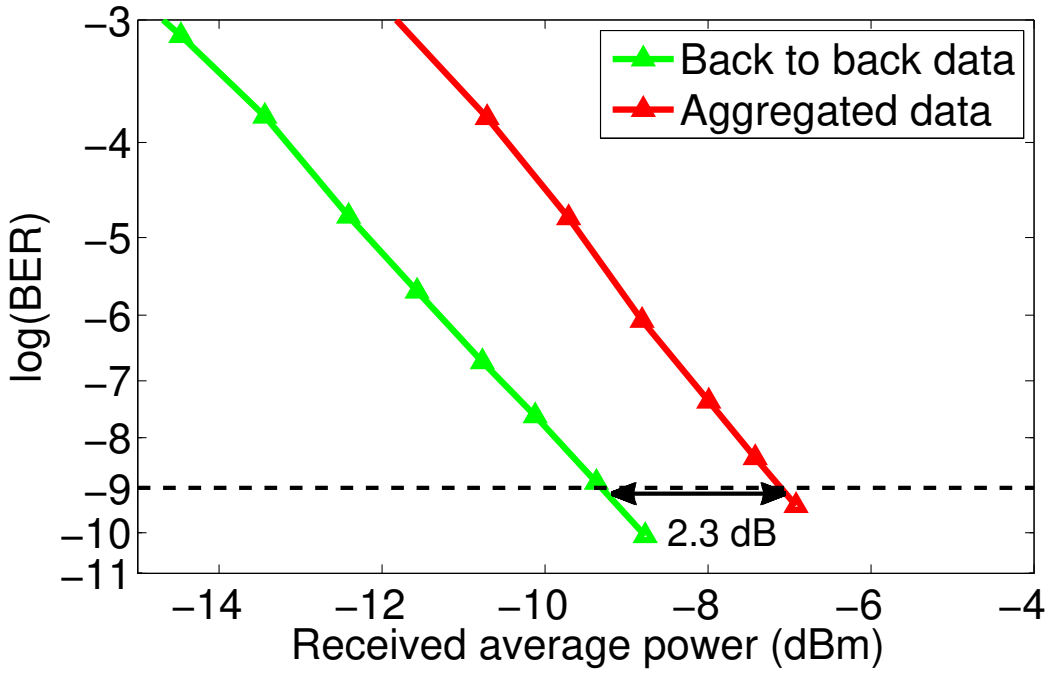



**Fig. 4.12** Measured BER and power penalty of the 64 ns aggregated packet generated from the PWSM output with respect to the back to back generated single 64 ns long data.

## 4.4 Discussion

A four channel PWSM device is designed in this work using the low-loss $Si_3N_4$ waveguide and a 64 ns long data packet is constructed from four 16 ns long packets.

In the experimental setups, a PC is used before the PWSM chip to reduce the polarization dependent loss of the $Si_3N_4$ waveguide, inherently polarization sensitive due to its high aspect ratio in the cross-section area. The high aspect ratio cross-section area is necessary to achieve low propagation loss in the waveguide [27]. Recently, in [91], a polarization insensitive $Si_3N_4$ waveguide is demonstrated by decreasing the aspect ratio of the cross-section area (1.2 $\mu$m $\times$ 170 nm) and by using double strip taper waveguide as the edge couplers. However, the waveguide demonstrated in [91] has a relatively higher propagation loss (9.5 dB/m in [92]) compared to the single strip waveguide used in this work.

The AWG based filters on the low-loss $Si_3N_4$ waveguide platform proposed in [37], has lower crosstalk (30 dB) compared to crosstalk of the demultiplexer (15.2 dB) demonstrated in this work. However, the MZI based demultiplexer allows simultaneous filtering and time delaying of the optical channels with respect to their adjacent channels, which is important for the proposed wavelength-striped mapping device demonstrated in this work. For example, the integrated delay line ($\Delta L_3$) in the PWSM device (Fig. 4.1) is utilized to delay both $ch-3$ and $ch-4$ by 32 ns, which reduces the footprint area of the PWSM device. In an AWG filter based PWSM device, on the other hand, two separate time delay blocks of 32 ns and 48 ns would be required for $ch-3$ and $ch-4$ increasing the footprint of the PWSM device. Another approach to decrease the crosstalk is to use a cascaded or lattice MZI based filter architecture, which improves the crosstalk between channels to approximately 20 dB in high index contrast silicon waveguide based demultiplexers [93]. In this work, we have not implemented the lattice architecture based demultiplexer so to minimize the footprint of the circuit. However, in the future designs, lattice-based MZI demultiplexer should be considered to reduce the crosstalk between the channels.

In the experimental setup, EDFAs are used to compensate for the insertion loss of the delay waveguides. In practical applications such as in data centers, SOA can be integrated within the PWSM device to provide the necessary optical amplification. A flip–chip process integration of SOAs onto silica–based waveguides has been demonstrated in [94] leading the path to the feasibility of a hybrid integration of the SOAs within the $Si_3N_4$ waveguide based PICs. Another approach is to eliminate the need of optical amplification by reducing the insertion loss of the delay waveguides. For example, utilizing the 0.5 dB propagation loss $Si_3N_4$ waveguide demonstrated in [28], the insertion loss of the longest delay waveguide in this work can be reduced to 4.8 dB. However, integration of SOAs will still be necessary for the scalability of this approach, *i.e.*, to increase the number of channels from four to

eight.

In [87], a theoretical model of the eight-channel PWSM device based space-time interconnection architecture (STIA) is shown to be more energy efficient than the 10 Gb/sec 48 port Ethernet switch [95]. An eight-channel STIA's power budget includes power consumption by an eight-channel laser array, one modulator driver, one receiver and two SOAs. The two SOAs at the transmitter and receiver links are required to gate the wavelength-striped WDM packets generated by the PWSM device. However, the model of the PWSM device in the STIA is designed with the 0.5 dB/m propagation loss $Si_3N_4$ waveguides [87]. Therefore, no additional SOAs were needed to compensate the optical power mismatch among the channels. The integrated PWSM device proposed in this work requires off-chip EDFAs to compensate the optical power mismatch among the channels, which increases the power budget of the experimental setup. The proof of concept of forming a 64 ns long data packet demonstrated in this work will be helpful to design the PWSM device with 0.5 dB/m propagation loss $Si_3N_4$ waveguides in future.

In this work, the delay lengths of the PWSM device are designed to form a fixed length data packet for 25 Gb/s data rate channels which limits the flexibility of the network in the need of dynamic resource allocation or change in the data rate and traffic patterns. However, the PWSM device itself draws only 5.68 mW power, which is low compared to the active elements such as lasers, modulator drivers, receivers and SOAs. A detailed analysis on the power budget of the PWSM device based STIA switches compared to the Ethernet switches is presented in [46, 87]. At lower traffic or lower level of network utilization, energy consuming active devices such as SOAs in the STIA switch remain in the idle mode, increasing the energy efficiency of the network. At higher traffic levels, the energy consumed by the PWSM device remains constant, and the energy consumed by the SOAs increase linearly with server utilization. Therefore at the expense of network flexibility the STIA

based optical switches offer energy efficient and scalable network architecture.

## 4.5 Summary

The performance results of the four channel PWSM circuit reported in this chapter suggests that some of the electronic serialization and parallelization of data packet can be done passively and efficiently in the optical domain. Integrated optical delay lines on low loss $Si_3N_4$ waveguide platform facilitates the serializing/deserializing of long length packet on PIC (*i.e.*, 320 bits long packet in [61] vs 1600 bits long packet in this work).

From the experimental result presented in this chapter we find that 9.7 dB loss difference exists between the adjacent optical channels due to the 3.1 dB/m loss in the delay waveguides which can be compensated through optical amplification. This incremental loss difference between the adjacent channels limits the scalability of the PWSM process in terms of number of channels. However, in [28] ~0.5 dB/m propagation loss in the $Si_3N_4$ waveguide has been demonstrated by changing the waveguide cross-section (6.5 $\mu$m $\times$ 50 nm) and by increasing the minimum bend radius to 9.8 mm with the PECVD top cladding. The $Si_3N_4$ waveguide based PWSM device proposed in this work is designed adopting a similar fabrication technology used to design a 6.5 $\mu$m $\times$ 50 nm cross-section area waveguide exhibiting 0.5 dB/m propagation loss in [28]. Hence, the propagation loss of the integrated delay waveguides can be further reduced by changing the waveguide cross-section geometry and by increasing the bending radius. Such approach would lead to a loss difference between two adjacent channels drastically reduced by more than a factor of six. In other words, the loss of the 16 ns optical delay lines would only be 1.5 dB making the proposed interface a practical solution for optical passive serial–to–WDM and WDM–to–serial process.

# Chapter 5

# Optical Deserialiser Time Sampling Based SiGe Photoreceiver

## 5.1 Introduction

The advent of standardized silicon photonic (SiP) process has made the fabrication of complex optical systems more practical and affordable. Therefore, new paradigms and architectures can be explored to optimize optoelectronic devices. For instance, it is now possible to perform on-chip processing in the optical domain to ease the performance requirements on electrical processing and hence reduce the cost and/or the power consumption of electronic circuits in telecommunication networks [96, 97]. Based on this concept, we implemented a photoreceiver or optical front-end that performs optical time sampling to reduce the operating speed of its electronics components. The optical sampling allows to reduce the electronic processing speed by enabling parallel processing of the optical bit stream and results in a deserialization of the data directly at the optoelectronic interface.

In this chapter, we present a photoreceiver that consists of a 1 $\times$ 4 time sampling

PD array in a series architecture. The power of the incoming optical signal is uniformly distributed to four PDs using directional couplers. The optical bit stream is delayed in increments of one bit period prior to each of the last three PDs using optical passive waveguide-based delays. To compensate for the incremental loss of the waveguides, directional couplers with different coupling ratios are used, such that each of the PD receives an equal amount of optical power. As such, each PD generates the same electrical bit streams but the four PDs are delayed with respect to each other. A similar approach can be found in a silicon photonics based optical equalizer demonstrated in [39], where MZI based power splitters were thermally tuned to divide the optical power of the incoming signal and to set the coefficients of the equalizer or the finite impulse response (FIR) filter. The Si-Ge traveling-wave PD array (Si-TWPDA) demonstrated in [38], also optically divides the power of the incoming signal onto four channels, and, as mentioned in the above paragraph, it uses optical waveguide delay lines to balance the electrical phase delay of the electrode. However, in [38] the required delay length of the waveguides were small (in the multiples of 0.25 $\mu$m), therefore no power compensation was required to balance the delay waveguide loss. In this work, we present an analysis on the design of the coupling ratio of directional couplers such that equal power is obtained at the four photodetectors without thermal tuning when taking into account the loss from the incremental delay lines. We also show that low-loss SOI waveguides decreases variation in the required coupling ratio of the directional couplers with respect to change in the waveguide loss. This increases the tolerances on the coupling ratio of the directional couplers over variation in waveguide loss.

Next, we show that by using the correlation property between the four PD channels, it is possible to electronically process the photodetected signals at a quarter of the data rate to recover the original signal. This scheme simplifies the post processing electronic circuit design and reduces the dynamic power consumption of the electronic circuit by lowering

the sampling rate of the received signal. The speed reduction factor is proportional to the number of PDs, which is only limited by the losses in the delay lines and the increased optical power splitting. Moreover, the overall insertion loss of the photoreceiver depends on the length of the optical delay waveguides, which is proportional to the duration of one bit. For example, for a 10 Gb/s photoreceiver the duration of a one bit delay is 100 ps, whereas for a 20 Gb/s photoreceiver this delay is 50 ps. Therefore, the overall insertion loss in a 10 Gb/s sampling photoreceiver will be higher compared to a 20 Gb/s sampling photoreceiver because the latter requires shorter delay waveguides. As such, we designed four variations of the optical time sampling front-end: 1) 10 Gb/s and 20 Gb/s optical time sampling front-end with typical 220 nm × 500 nm cross-section SOI waveguides (∼2.5-3 dB/cm propagation loss) and 2) 10 Gb/s and 20 Gb/s optical time sampling front-end with lower propagation loss (∼0.2 dB/cm) SOI waveguides. For all four photoreceivers we have measured BER below $10^{-10}$ for each of the four PD channels. We also propose a post-electronic front-end model to recover the original input bit stream at a quarter of the data rate. Using offline processing in MATLAB, the original $2^{15} - 1$ PRBS input data is recovered for all of the four devices. The results presented in this chapter are published in [98].

## 5.2 Design of the 1 × 4 sampling photodetector architecture

Fig. 5.1 shows the schematic of the proposed architecture for the 20 Gb/s data rate optical front end. The layout and the number of components are the same for the four devices. A 20 Gb/s optical NRZ signal is received as the input to the grating coupler (GC). The energy of the optical signal is uniformly distributed over four output channels (*Ch-1* to *Ch-4*) through three directional couplers (*DC-1* to *DC-3*). To implement the one bit time delay

of 50 ps, a ∼3.6 mm long silicon waveguide delay line is added between adjacent channels. The power coupling ratio of each directional coupler is adjusted by varying its coupling length ($L_1$, $L_2$ and $L_3$) to compensate for the optical propagation loss in the delay lines. As mentioned in the above section, lower speed implementations (*e.g.*, 10 Gb/s) require longer delay lines (∼7.2 mm at 10 Gb/s), and hence, suffer higher propagation losses. Fig. 5.1 also shows the Ge-on-SOI PD schematic with its capacitance ($C_{PD}$) and series resistance ($R_{PD}$), as well as its on-chip biasing capacitor ($C_G$). The biasing capacitor facilitates the application of an on-chip DC reverse bias voltage, simplifying the test circuit [99]. The PD has an 8 $\mu$m × 20 $\mu$m surface area and a 500 nm thick Ge-layer over a 19 $\mu$m × 24 $\mu$m SOI passive waveguide area. The biasing capacitors for all the four PDs have a 470 $\mu$m × 700 $\mu$m surface area. Each PD exhibits a bandwidth of ∼25 GHz with a reversed bias voltage of 4 V and a responsivity of ∼0.7 A/W. From the I-V characteristic of the PD, the measured dark current is approximately 1.5 $\mu$A with a reverse bias voltage of 4 V. By fitting the forward bias region of the I-V curve to a linear model at 0.8 volt, we estimated the PD resistance ($R_{PD}$) to be approximately 110 Ω. Detailed characterization of the PD with an on-chip capacitor can be found in [100].

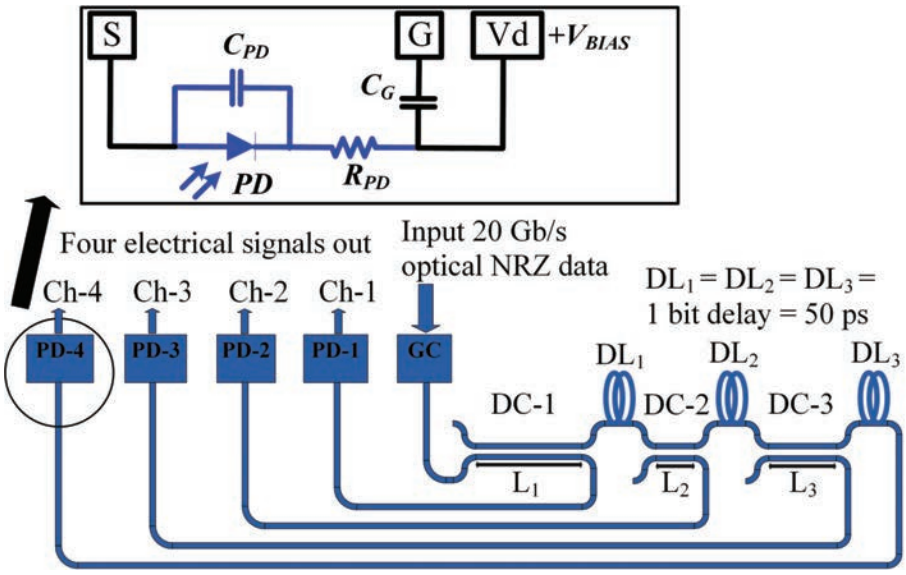



**Fig. 5.1** Schematic of the sampling PD architecture for 20 Gb/s data rate, inset shows the detailed schematic of the PD layout. GC: grating coupler, DC: directional coupler, G: ground pad, S: signal pad. Different coupling lengths ($L_1$, $L_2$ and $L_3$) are used in the directional couplers to maintain uniform power distribution among all the four PD channels.

### 5.2.1 Design method for the delay waveguides

To implement one bit delay using a typical single mode 220 nm × 500 nm cross-section SOI waveguide, we designed the delay lines in compact rectangular spirals to reduce the footprint. The minimum bend radius of the delay lines is 20 $\mu$m. Simulations and experimental results suggest that with a 20 $\mu$m bend radius, the mode mismatch loss is reduced below 0.015 dB [73] in a 220 nm × 500 nm cross-section SOI waveguide. In another variation, to reduce the propagation loss in the delay lines, we choose a 220 nm × 3 $\mu$m cross-section area ridge based SOI waveguide with a 90 nm slab. The low-loss SOI waveguides have higher bending losses due to their ridge-based structure; therefore where bends are required, we used the 220 nm × 500 nm cross-section SOI waveguide with a 10 $\mu$m bend radius. The two types of waveguides are connected by a 200 $\mu$m long taper such that only

the fundamental mode is excited in the 220 nm × 3 $\mu$m multimode SOI waveguides [23]. Fig. 5.2 shows the delay waveguide structure and their geometry (not to scale).

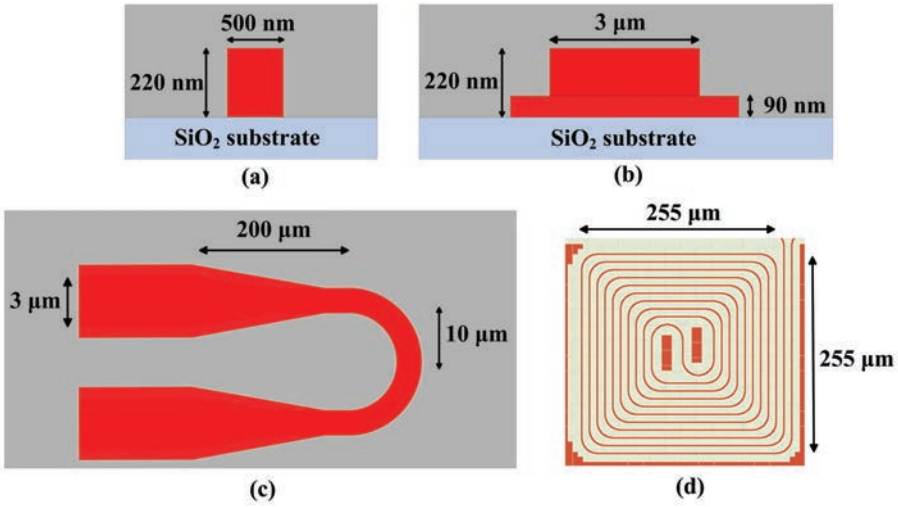



**Fig. 5.2** Schematic of the (a) typical 220 nm × 500 nm cross-section and (b) 220 nm × 3 $\mu$m cross-section low-loss SOI waveguide, (c) low-loss SOI waveguide at the routing/bending region (top view), (d) actual layout of the rectangular shaped ~7.2 mm long delay line with the typical 220 nm × 500 nm cross-section SOI waveguide for the 10 Gb/s optical front-end.

We performed 2D FDTD simulation to determine the group index of both types of SOI waveguides in the wavelength range from 1500 nm to 1600 nm (Fig. 5.3). Fig. 5.3 shows that the group indices for wavelengths around 1550 nm for the 220 nm × 500 nm and the 220 nm × 3 $\mu$m cross-section SOI waveguides are approximately 4.18 and 3.71, respectively. We used these values for the group indices to calculate the length of the delay waveguides to produce one bit delays in both types of the devices.

The length of the delay waveguides and the loss per channel for the four different optical front-ends reported here are summarized in Table 5.1 of section 5.2.2.

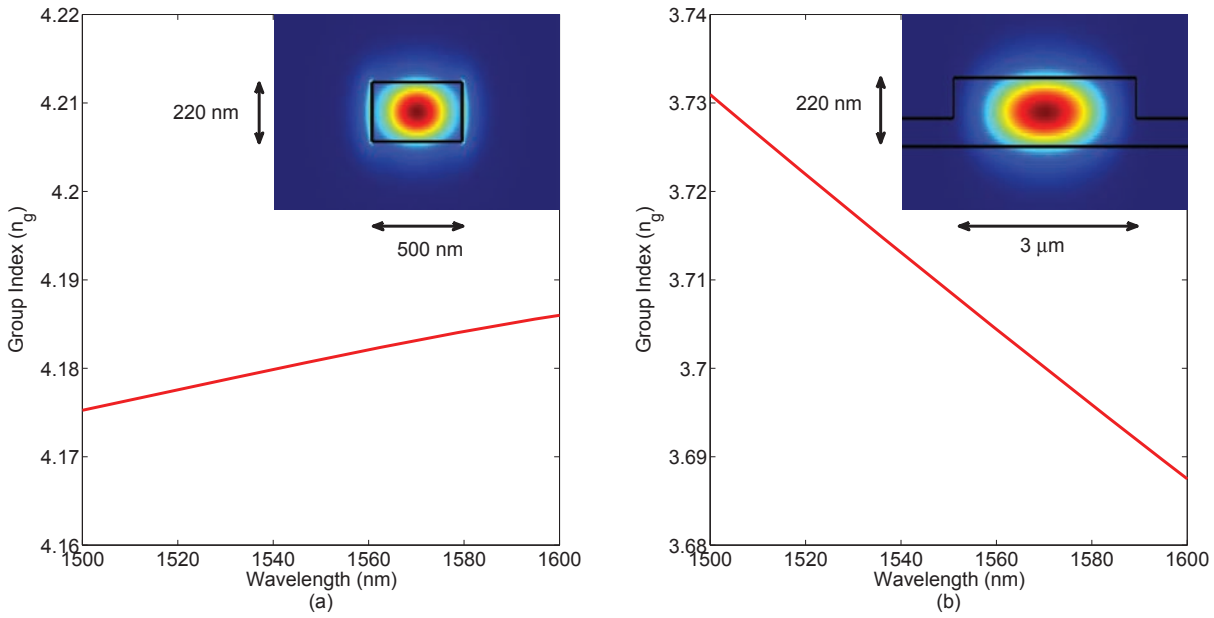



**Fig. 5.3** Variation of the group index as a function of wavelength over the range from 1500 nm to 1600 nm for the (a) typical 220 nm × 500 nm cross-section and (b) 220 nm × 3 $\mu$m cross-section low-loss SOI waveguide, inset: shape of the fundamental mode inside each of the waveguide cross-section area.

### 5.2.2 Design of the 1 × 4 optical splitter with simultaneous 1 bit optical delay

Three directional couplers with different coupling ratios compensate the loss exhibited by the delay waveguides as well as uniformly distribute the optical power over four PD channels in each sampling photoreceivers (Fig. 5.4). In the following, we will demonstrate how the losses of the delay lines impact the tolerance on the coupling ratio required to implement the receiver functionality.

Fig. 5.4 shows the three directional couplers with their cross ($r_1$, $r_2$, and $r_3$) and through (1-$r_1$, 1-$r_2$, and 1-$r_3$) power coupling ratios.

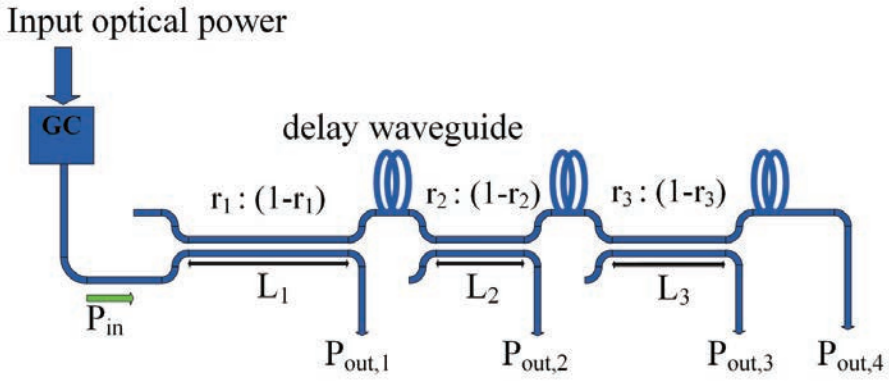



**Fig. 5.4** Schematic of the passive section of the time sampling photoreceivers with the directional couplers.

To achieve uniform optical power distribution (*i.e.*, $P_{out,1} = P_{out,2} = P_{out,3} = P_{out,4}$), it is necessary that the power coupling ratios of the directional coupler are as follow (Eq. 5.1), where '$L$' denotes the total propagation loss coefficient in a delay waveguide.

$$\begin{aligned} r_1 &= 1 - \frac{1}{1 + \frac{1}{L} + \frac{1}{L^2}(1 + \frac{1}{L})} \\ r_2 &= \frac{1}{1 + \frac{1}{L}(1 + \frac{1}{L})} \\ r_3 &= \frac{1}{1 + \frac{1}{L}} \end{aligned} \tag{5.1}$$

In Eq. 5.1, the total propagation loss coefficient in the delay waveguide can be calculated as: $L = 10^{\frac{-loss \times l}{10}}$, where $loss$ = 2 to 3 dB/cm for the 220 nm × 500 nm cross-section SOI waveguide [73] and $loss$ = 0.1 to 0.2 dB/cm for the low-loss 220 nm × 3 $\mu$m cross-section SOI waveguide, and $l$ is the length of the delay waveguide in cm. In [23], the reported propagation loss is 0.026 dB/cm for a 300 nm × 3 $\mu$m cross-section SOI waveguide. We measured higher propagation loss in the 220 nm × 3 $\mu$m cross-section SOI waveguide (0.17 dB/cm). These higher propagation losses might be caused by the tapers added to transition to narrower waveguides before and after the bends, the propagation in the narrow

bended waveguides, and the different waveguide thickness (220 nm here vs 300 nm in [23]). Fig. 5.5 shows the variation in the power coupling ratio ($r$) for different values of propagation losses in the typical 220 nm $\times$ 500 nm cross-section SOI waveguide. A different slope is observed for the coupling ratio $r_1$ because the optical power is coupled from the bottom arm of the directional coupler, whereas in the other two directional couplers ($r_2$ and $r_3$) the optical power is launched from the upper arm (Fig. 5.4). In all three directional couplers, the power coupling ratios are calculated such that uniform power distribution is achieved in both the 10 Gb/s and 20 Gb/s time sampling photoreceivers. As expected, due to the use of longer delay line in the 10 Gb/s sampling photoreceiver, the variations of the cross-coupling ratio across the couplers are larger to account for the higher propagation losses. Thus, it is important to consider the propagation losses when designing the power coupling ratio of the directional couplers. Moreover, the performance of the technology used to implement the receiver must be taken into account since in SOI waveguides, loss is affected by scattering caused by the sidewall roughness, which is a parameter dependent on the fabrication process. For this work, we choose the coupling ratio parameters assuming a waveguide propagation loss of 2.5 dB/cm for the typical 220 nm $\times$ 500 nm cross-section SOI waveguide fabricated through IME-A*STAR in Singapore.

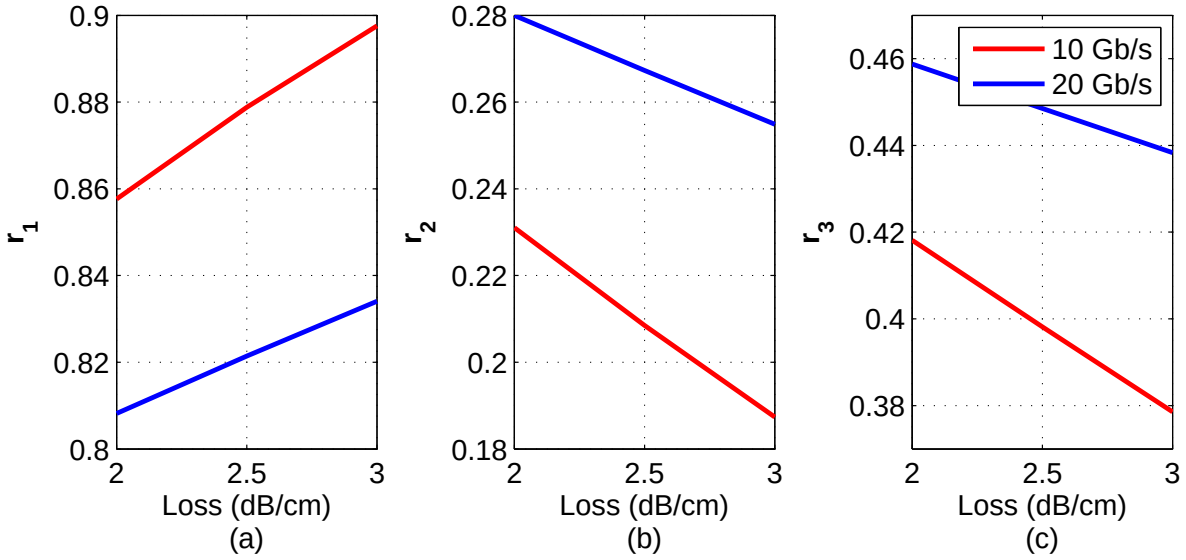



**Fig. 5.5** Variation in the required cross-coupling ratio for different propagation losses in 220 nm × 500 nm cross-section SOI delay waveguide for directional coupler 1 ($r_1$), 2 ($r_2$) and 3 ($r_3$), respectively.

In the photoreceivers with the low-loss SOI waveguides, the changes in the required cross coupling ratio becomes less sensitive to variations in propagation losses, as shown in Fig. 5.6. Therefore, sampling photoreceivers with low-loss waveguides are more robust to fabrication process variations. Here, the optical power is launched from the top input arm in the three directional couplers thus all the slopes are the same. In addition to the propagation losses, we consider the bending losses and the tapered waveguide losses during the directional coupler optimization. Thus, we assumed a 0.2 dB/cm propagation loss in the one bit delay waveguides with the wider cross-section.

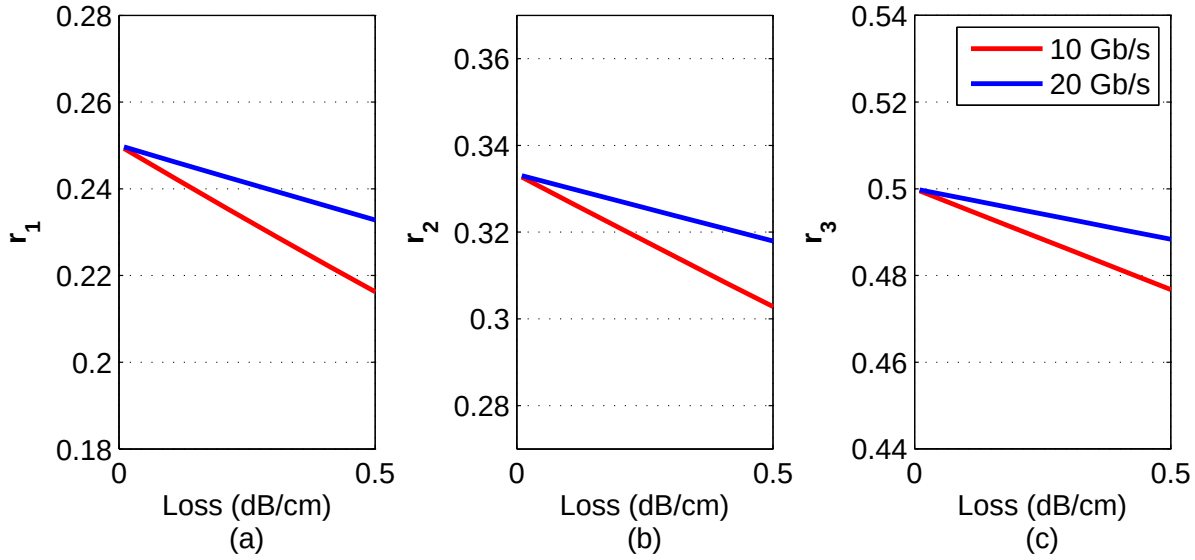



**Fig. 5.6** Variation in the required cross-coupling ratio for different propagation losses in 220 nm $\times$ 3 $\mu$m cross-section SOI delay waveguide for directional coupler 1 ($r_1$), 2 ($r_2$) and 3 ($r_3$), respectively.

We determine the theoretical propagation losses per channel and the power coupling ratios of the directional couplers (Fig. 5.5 and 5.6) using Eq. 5.1. Table 5.1 lists the length of the delay waveguides and the estimated propagation losses per channel for the four sampling photoreceivers presented in this chapter.

We use a 90 nm slab loaded ridge based SOI waveguide to implement the directional couplers. In all the directional couplers, the gap between the two waveguides in the coupling region is fixed to 200 nm and the bending radius at the beginning and the end is set to 20 $\mu$m. The method used to design the slab loaded ridge waveguide based directional couplers is detailed in [73]. Table 5.2 lists the coupling lengths of the directional couplers for all the sampling photoreceivers presented in this chapter.

**Table 5.1** Projected loss in the photoreceivers

| Component | Length of one bit delay waveguide | Loss per channel |
|---|---|---|
| 1. 10 Gb/s optical front-end with 220 nm × 500 nm cross-section SOI waveguide | 7.2 mm | 9.2 dB |
| 2. 20 Gb/s optical front-end with 220 nm × 500 nm cross-section SOI waveguide | 3.6 mm | 7.5 dB |
| 3. 10 Gb/s optical front-end with 220 nm × 3 $\mu$m cross-section SOI waveguide | 8.2 mm | 6.3 dB |
| 4. 20 Gb/s optical front-end with 220 nm × 3 $\mu$m cross-section SOI waveguide | 4.1 mm | 6.1 dB |

**Table 5.2** Directional coupler geometries in different time sampling photoreceivers

| Component | $L_1$ | $L_2$ | $L_3$ |
|---|---|---|---|
| 1. 10 Gb/s optical front-end with 220 nm × 500 nm cross-section SOI waveguide | 7 $\mu$m | 0.11 $\mu$m | 2.04 $\mu$m |
| 2. 20 Gb/s optical front-end with 220 nm × 500 nm cross-section SOI waveguide | 6.25 $\mu$m | 0.75 $\mu$m | 2.52 $\mu$m |
| 3. 10 Gb/s optical front-end with 220 nm × 3 $\mu$m cross-section SOI waveguide | 0.52 $\mu$m | 1.34 $\mu$m | 2.97 $\mu$m |
| 4. 20 Gb/s optical front-end with 220 nm × 3 $\mu$m cross-section SOI waveguide | 0.54 $\mu$m | 1.37 $\mu$m | 3 $\mu$m |

## 5.3 Time-sampling photoreceiver data recovery principle

From the optical front-end of the time sampling photoreceiver, four optical signals are converted into electrical signals. Due to the one bit delay lines, the four electrical signals from the PD channels are delayed from each other by one bit. After the O/E conversion, the voltage of each of the four electrical signals accumulates over every period of four bits through a capacitive load ($C_{LOAD}$) in the electronic circuit front-end model (Fig. 5.7(a)). The voltage signal accumulation process in the capacitive load ($C_{LOAD}$) is presented in detail in section 5.3.1 below. After each period of four bits, the accumulated signal at

point 'A' is sampled at $1/4^{\text{th}}$ of the data rate and processed by an analogue-to-digital converter (ADC). The load capacitor ($C_{LOAD}$) voltage is then reset to zero. To overcome the challenge of a high-speed reset, two capacitive loads ($C_{LOAD}$) operate in switched capacitor mode, [101, 102] such that over every period of four bits, one of the capacitors accumulates charges while the other one is discharged though a switch (SW). The process is shown in Fig. 5.7(a). When $C_{LOAD,1}$ accumulates charge, switches labelled $SW1$, $\overline{SW1}$, $SW2$ and $\overline{SW2}$ are in off (open), on (close), on (close) and off (open) states, respectively. In this switching state, $C_{LOAD,2}$ is discharged through $SW2$. Over the next four bits duration, opposite switching conditions occur (*i.e.*, $SW1$, $\overline{SW1}$, $SW2$ and $\overline{SW2}$ are in on (close), off (open), off (open) and on (close) states, respectively). In this configuration, $C_{LOAD,2}$ accumulates charges and $C_{LOAD,1}$ is discharged through $SW1$. The four streams of symbols are digitally processed at $1/4^{\text{th}}$ of the data rate to generate the original input bit stream. Depending on the sequence and value of the four bits, each sampled symbol can be normalized to one of five possible levels (*i.e.* 0, 0.25, 0.5, 0.75, 1). A 3 bit ADC can be used to pass the 5 level symbols generated from each of the PD channels simultaneously to the digital signal processing (DSP) blocks, *i.e.*, to an adder-subtractor. Indeed, the five possible levels for symbol represent a 5-level polybinary sequence [103] that is generated at the receiver end in this work, whereas the transmitted signal is still OOK data. In optical transmission networks using polybinary coding, polybinary symbols are generated either at the transmitter or receiver end, but in both cases the post-processing electronic circuit (*i.e.*, ADC and DSP blocks) at the receiver needs to operate at the original bit rate. The post-processing electronic circuit cannot operate at the reduced symbol rate because each polybinary symbol essentially carries only one bit of information [103]. In [104], 10 Gb/s 5-level polybinary format optical signal transmission is experimentally demonstrated, where the polybinary symbols were captured using a 13 GHz digital sampling scope. In

our work, the simultaneous generation of four symbols at the receiver allows the ADC and post-processing DSP blocks to operate at only $1/4^{\text{th}}$ of the data rate.

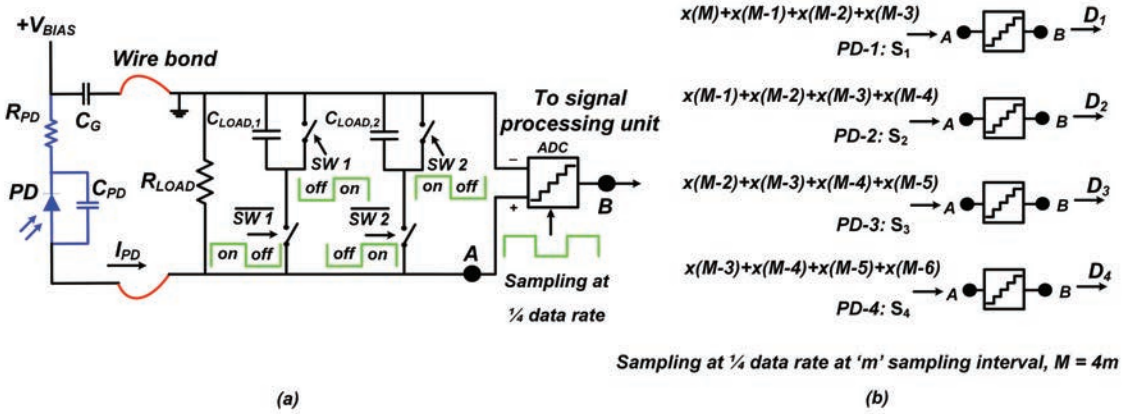



**Fig. 5.7** (a). Proposed front-end of one of the four PD with post electronic circuit model. (b) Average value of 4 bits is sampled by four samplers at $1/4^{\text{th}}$ data rate and sent to the ADC and DSP blocks for post processing.

The following algorithm is implemented to recover the original bit stream. At every sample point '$m$', which is taken over $1/4^{\text{th}}$ of the data rate, each PD channel generates a 3 bits sequence with a voltage corresponding to one of the five possible normalized levels mentioned above, representing the accumulated received power over that interval. The symbols from each PD channel are aggregated into a data segment that is then processed by solving four linear equations using simple adder-subtractor blocks. Eq. 5.2 shows the general expression of the accumulated photodetected signal from each of the four PDs at '$m$' sampling interval, where $x(M-i)$ is the voltage build-up across $C_{LOAD}$ for every input bits (or photocurrent '$I$'), '$i$' is the bit sequence and '$M$' is '$4m$'.

$$D_s = \sum_{i=s-1}^{s+2} x(M-i) \tag{5.2}$$

From Fig. 5.7(b) it is seen that the four symbol data segment ($D_1$, $D_2$, $D_3$ and $D_4$ generated from the four PDs, $s = 1,\ 2,\ 3,$ and 4, respectively) in Eq. (2) contains information

about 7 consecutive unknown input bits from $x(M)$ to $x(M-6)$. However, at the first sampling point when $m = 1$ (or $M = 4$), three of the 7 input bits ($x(0)$, $x(-1)$, and $x(-2)$) are equal to zero. These three zero bits actually come from the idle time segments in the $2^{nd}$, $3^{rd}$ and $4^{th}$ PDs for the first four input bits due to the one bit delay lines following the $1^{st}$ PD implemented in the optical front-end, which sets the initial condition of this algorithm. Therefore, from the first sampling point ($m = 1$ or $M = 4$), it is possible to deduct the initial four unknown input bits from the four symbol segment or four equations. Now, in the subsequent iterations, the three extra input bits are known from the previous iteration, and thus four new unknown input values can be found. In a digital signal processing circuit, these operations will require three adder blocks and six subtractor blocks (see Fig. 5.8).

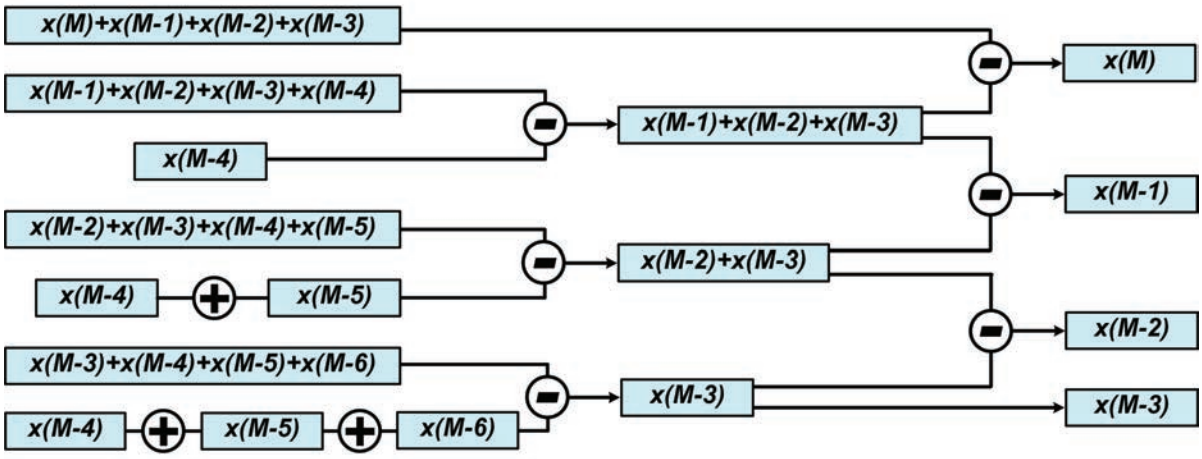



**Fig. 5.8** Block diagram of the digital signal processing method to recover the original input bit stream from the sampled signal.

From Fig. 5.8, it is seen that if an error occurs in the bits of the previous symbol (*i.e.*, in *x(M-4)*, $x(M-5)$ or $x(M-6)$), then the error will propagate in all subsequent bits. To prevent this, the original electrical input bits ($a(M)$) at the transmitter should be precoded into the binary sequence ($x(M)$) using the same algorithm developed for polybinary signal transmission networks [103, 104]:

$$x(M) = a(M) \oplus x(M-1) \oplus x(M-2) \oplus x(M-3) \tag{5.3}$$

After the 5 level symbols generated from ADC, the original input bit streams can be recovered using modulo-2 operation on the symbols by digital signal processing blocks:

$$a(M) = D_s \; mod \; 2 \tag{5.4}$$

It should be mentioned that the optical and analog electronic front-end proposed in this work can be used on the 5-level symbols generated to recover the original input bits from the precoded binary streams. Precoding of the input electrical bits is done at the transmitter before optical modulation, and a modulo-2 operation on each of the symbols is performed by the DSP blocks. In this work, we validated the concept of detecting the OOK data at $1/4^{\text{th}}$ data rate by processing the received data offline using the DSP blocks as shown in Fig. 5.8. The input bits were not precoded in this initial demonstration to simplify the transmitter implementation.

### 5.3.1 Voltage signal accumulation in the capacitive electronic circuit model

In this section, we analyze the voltage signal accumulation process in the capacitive load of the electronic front-end model. The RC bandwidth of the electronic front-end is much lower than the actual data rate of the input signal as the post processing circuit (ADC

and the DSP blocks) operates at $1/4^{\text{th}}$ of the input signal data rate. Therefore the values of '$R_{LOAD}$' and '$C_{LOAD}$' can be chosen such that $R_{LOAD}C_{LOAD} \gg T_b$, where $T_b$ is the one bit period of the input signal. We have found that this also facilitates voltage build-up across the load capacitor ($C_{LOAD}$) for every input bit '1', whereas the accumulated voltage in '$C_{LOAD}$' remains stable or unchanged for the input bit '0'. For $R_{LOAD}C_{LOAD} \gg T_b$, the incremental voltage across '$C_{LOAD}$' from its initial voltage '$V_0$' can be approximated as the following:

$$\begin{aligned} x(M-i) &= IR_{LOAD}\left[1 - exp\left(\frac{-T_b}{R_{LOAD}C_{LOAD}}\right)\right] + V_0\left[exp\left(\frac{-T_b}{R_{LOAD}C_{LOAD}}\right) - 1\right] \\ &\approx \frac{IT_b}{C_{LOAD}}, \text{ for every input bit "1", where } IR_{LOAD} \gg V_0 \\ &\approx \frac{-V_0T_b}{R_{LOAD}C_{LOAD}}, \text{ for every input bit "0", where } I = 0 \end{aligned} \tag{5.5}$$

From Eq. 5.5 it is seen that if '$R_{LOAD}$' can be chosen such that $IR_{LOAD} \gg V_0$ or $I \gg V_0/R_{LOAD}$ then the discharge in voltage (when input bit is '0') from the load capacitor ($C_{LOAD}$) is negligible compared to the voltage accumulation (when input bit is '1'). To confirm this, we simulated the electronic front-end model with the Cadence circuit simulation software for a 20 Gb/s input data rate. For these simulations, we chose a parasitic resistance, $R_{PD} = 110\ \Omega$, and a capacitance, $C_{PD} = 66$ fF (extracted from Sentaurus device and HFSS simulations) for the designed photodetector. The values of $R_{LOAD} = 1\ k\Omega$ and $C_{LOAD} = 2$ pF are chosen such that about 10 mV is accumulated across '$C_{LOAD}$' after one bit period for an input bit value of '1' or an input photocurrent of $I = 0.4$ mA (considering -2.4 dBm optical input at the PD of responsivity 0.7 A/W).

Fig. 5.9 shows the accumulated voltage across the load capacitor ($C_{LOAD}$) after 4 bits for the two cases out of total $2^4 = 16$ possible cases. From Fig. 5.9 it is seen that the

voltage discharge from the load capacitor for one '0' bit or three consecutive 0's is less than 0.5 mV. In section 5.4, we will show that the original input bits can be recovered using this circuit model within these voltage discharge limits.

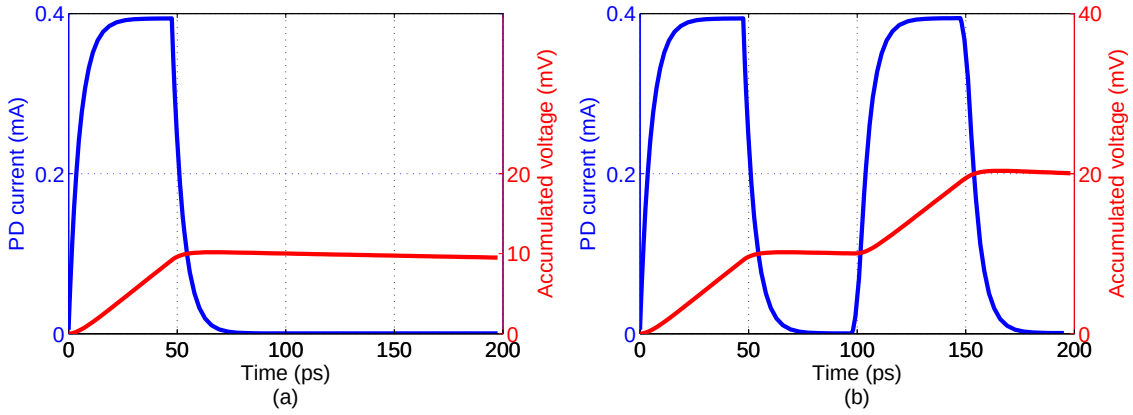



**Fig. 5.9** Voltage signal accumulation across the load capacitor for two types of input bit streams (a) '1000'and (b) '1010'.

## 5.4 Experimental demonstration and results

To verify that we achieve uniform optical power distribution over the four PD channels (Ch-1 to Ch-4), we designed passive test structures for the 10 Gb/s and 20 Gb/s optical front-ends. These test structures do not include the PDs and, therefore, allowed us to measure the average optical power over the four channels using the on-chip output grating couplers. Here, we describe the test result for the 10 Gb/s passive optical front-end, which incorporates longer delay line compared to the 20 Gb/s front-end.

A CW signal with an optical power of 3 dBm is tuned over the wavelength 1535 nm to 1575 nm and connected to a PC. At the output of the PC, the measured optical power is around $\sim$ 2 dBm. Then the polarized CW optical power goes to the input GC of the test device (see Fig. 5.4). The output optical power is measured at each of

the four output channels using an optical power meter. In addition, we recorded the optical power transmitted through a test GC pair (connected by a straight waveguide), and then used the results to normalize the output power of the test device. Fig. 5.10(a) shows the optical transmission response of the four output channels and the GC pair. From this figure it is seen that the total coupling in and out (GC pair loss) loss is around 9.5 dB (2 dBm - (-7.5 dBm)) at a wavelength of 1550 nm. Fig. 5.10(b) shows the normalized transmission response of the four channels, with the optical loss per channel around 10 dB near 1550 nm. The 10 dB channel loss includes the inherent 6 dB loss due to the one to four power splitting ratio from the input to the output channels. The extra 4.2 dB loss per output channels can be explained as follows. Each 100 ps delay line is $\sim$ 7.2 mm long. Therefore, Ch-1 has no loss (it does not include any delay waveguide in its optical path) and Ch-2 suffers (7.2/10) cm $\times$ 2.5 dB/cm = 1.8 dB loss. Then Ch-3 and Ch-4 suffer 3.6 dB and 5.4 dB loss, respectively. However, as mentioned before, the coupling ratios of the directional couplers are designed to compensate the extra delay waveguide loss suffered by Ch-2, Ch-3 and Ch-4 to ensure that all channels have an equal propagation loss. Therefore, because of the delay waveguides each channel suffers an extra loss of approximately 3.2 dB (calculated using Eq. 5.1). Hence, the total loss for each channel should be 6 + 3.2 dB = 9.2 dB by design (see Table 5.1). This predicted value is very close to the measured results (Fig. 5.10(a)) that show a loss per output channel of 10 dB. The additional 0.8 dB loss can be attributed to the directional coupler and bending waveguide losses. From Fig. 5.10(b) it is also seen that the loss variation across the four channels is less than 0.3 dB. It should be noted that without the power compensation obtained by engineering the coupling ratio of the directional couplers the loss difference between Ch-1 and Ch-4 would increase to 5.4 dB.

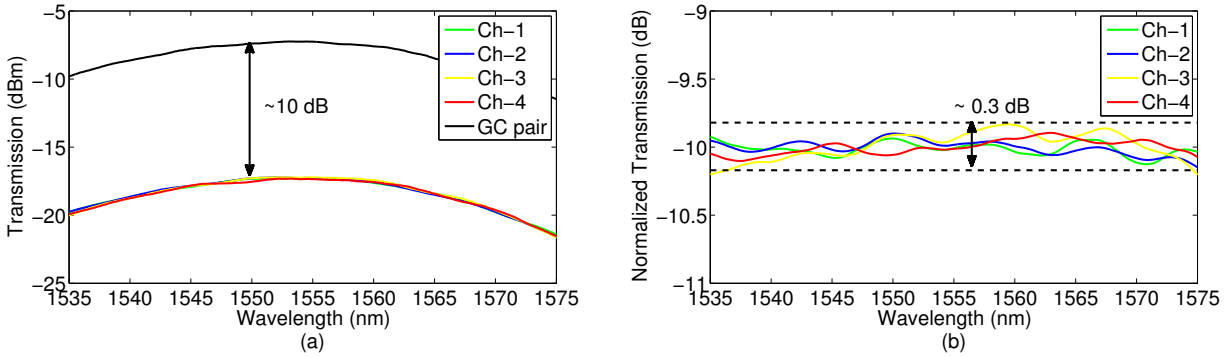



**Fig. 5.10** (a) Optical transmission response of the four output channels and grating coupler pair, (b) Normalized optical transmission response of the four output channels by grating coupler pair response.

Table 5.3 summarizes the experimental value of the propagation losses per channel for the four sampling photoreceivers presented in this chapter. From the experimental result listed in Table 5.3, it is seen that for each of the four optical front-ends, variation in the output optical power over the four channels is below 0.3 dB. Moreover, all the measured losses are within 1.0 dB of the projected losses listed in Table 5.1.

**Table 5.3** Measured optical loss per channels in the photoreceivers

| Component | Length of one bit delay waveguide | Loss per channel |
|---|---|---|
| 1. 10 Gb/s optical front-end with 220 nm × 500 nm cross-section SOI waveguide | 7.2 mm | 10±0.15 dB |
| 2. 20 Gb/s optical front-end with 220 nm × 500 nm cross-section SOI waveguide | 3.6 mm | 8.2±0.1 dB dB |
| 3. 10 Gb/s optical front-end with 220 nm × 3 $\mu$m cross-section SOI waveguide | 8.2 mm | 6.9±0.12 dB |
| 4. 20 Gb/s optical front-end with 220 nm × 3 $\mu$m cross-section SOI waveguide | 4.1 mm | 6.8±0.08 dB |

Next, we measured the BER of the PD channels for all four optical front-ends. Fig. 5.11

shows the experimental setup. A CW laser source emitting at a wavelength of 1550 nm and with an output power of 8 dBm is injected into a commercial $LiNbO_3$ MZM. A PRBS bit pattern of length $2^{31} - 1$ of NRZ OOK electrical data generated from a pulse pattern generator is used to drive the modulator. The MZM has an insertion loss of around 7 dB. To compensate this loss an EDFA with a noise figure (NF) of 5 dB is used before the DUT.

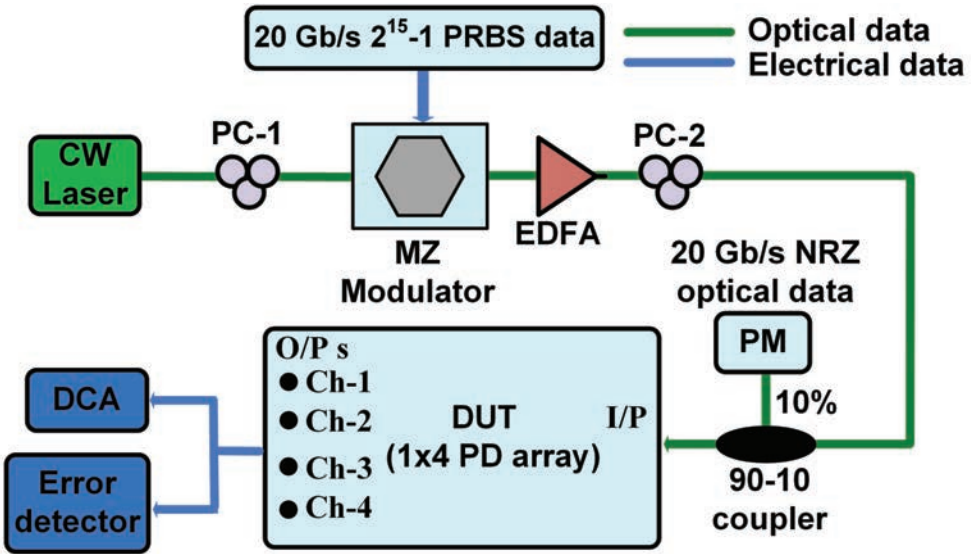



**Fig. 5.11** Experimental setup to measure BER and capture the PRBS data from each of the four PD channels. EDFA: Erbium doped fiber amplifier, PM: power meter, DCA: digital communication analyzer.

Fig. 5.12 shows eye diagrams and peak-to-peak voltages recorded for every PD channels for each of the four optical front-end variations for equal received average optical power. From this figure, it is seen that the peak-to-peak output voltages of the optical front-end with low-loss delay waveguides are higher compared to the optical front-ends with typical 220 nm $\times$ 500 nm cross-section SOI waveguides.

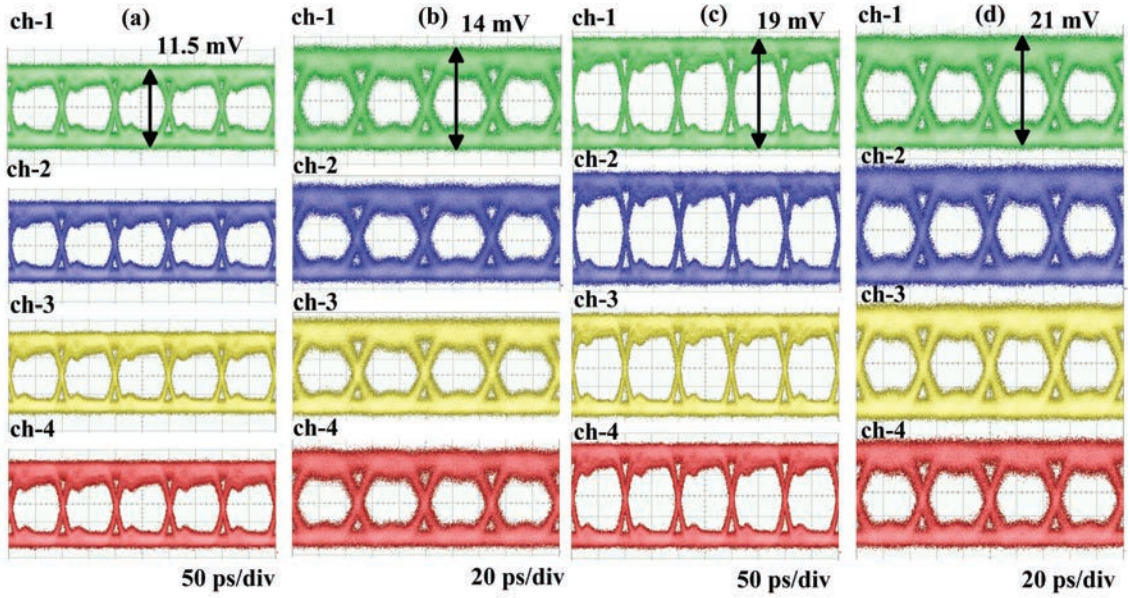



**Fig. 5.12** Electrical eye diagrams obtained for each of the four channels for the (a) 10 Gb/s, (b) 20 Gb/s, (c) low-loss 10 Gb/s and (d) low-loss 20 Gb/s time sampling optical front-end variations.

To measure the BER of the four PD channels of the optical front-ends, we use an off-chip post electrical amplifier to increase the peak-to-peak electrical signal voltage up to 60 $mV_{pp}$ such that the output signal is above the sensitivity limit of the BER tester (10 $mV_{pp}$ for the Anritsu MU181040A-002 error detector) for the minimum received optical power. Fig. 5.13 shows the BER versus average received power for the 20 Gb/s optical front-end with the typical and the low-loss delay waveguides. The average optical received power was measured at the input of the optical front-end and then adjusted to take into account the 4.75 dB loss caused by one grating coupler. From this figure it is seen that the 20 Gb/s optical front-end with low loss delay waveguides has a better sensitivity (∼1.6 dB at $1 \times 10^{-10}$ BER) than the 20 Gb/s optical front-end with typical 220 nm × 500 nm cross-section SOI waveguides.

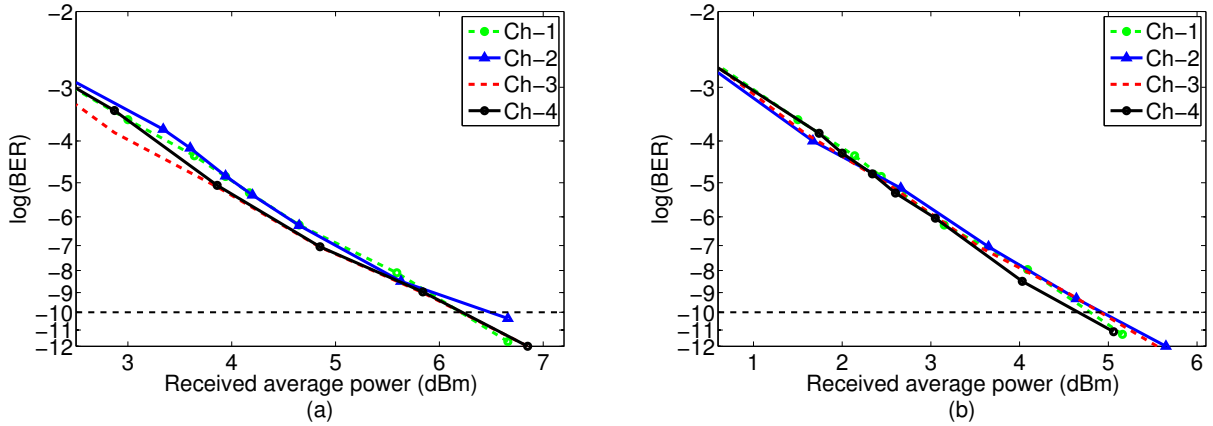



**Fig. 5.13** BER as a function of the average optical power at the input (*i.e.* after the grating coupler) of the 20 Gb/s time sampling optical front-end for all the 4 channels, (a) front-end with the typical 220 nm × 500 nm cross-section SOI waveguide and (d) front-end with the low-loss 220 nm × 3 $\mu$m cross-section SOI waveguide.

Next, to recover the original input bit stream at $1/4^{\text{th}}$ of the data rate, we captured and stored the 1 bit delayed $2^{15}-1$ PRBS data generated from each of the four channels, which for this demonstration are then further processed offline using the principle described in section 5.3 (see Fig. 5.7). Here, a $2^{15}-1$ PRBS bit stream is chosen instead of $2^{31}-1$ PRBS such that the data can be saved within the memory limit of the DCA. Fig. 5.14 shows a specific segment of the captured bits for all the four channels of each of the optical front-ends. From this figure it is seen that, one bit delay of ∼100 ps and ∼50 ps is obtained for the 10 Gb/s and 20 Gb/s optical front-ends with the 220 nm × 500 nm cross-section SOI waveguide. This accurate one bit time delay was expected from both components, as it is seen from the simulation result in Fig. 5.3 that the group index of the silicon waveguide varies by only ∼0.01 over the wavelength range from 1500 nm to 1600 nm. This variation of group index can induce only 0.24 ps delay mismatch in the 7.2 mm long one bit delay lines used in 10 Gb/s optical front ends. The low bandwidth post processing electronic circuit is transparent to this small value of time delay offset. However, in the 10 Gb/s and 20 Gb/s

optical front-ends with low-loss SOI waveguides, there is a ∼7 ps and ∼3 ps offset from the exact one bit delay between two successive channels. The time delay offset occurs in the low-loss optical front-ends due to the use of waveguide tapers in the bending regions and the comparatively large wavelength dependence of the group index (group index varied by ∼0.04 over the wavelength range from 1500 nm to 1600 nm, Fig. 5.3(b)). It is difficult to calculate the resultant time delay because of the variation of the group index as a function of the width of the tapered waveguides (from 500 nm to 3 $\mu$m and vice versa). Using the experimental time delay values obtained with these first prototypes, in future fabrication runs the time delay offset could be eliminated. In this work, we find that in the presence of this time delay offset it is possible to recover the original bit streams by tuning the sampling time duration in the post processing electronic circuit. The captured data from the four channels shown in Fig. 5.14 were processed offline in MATLAB.

The captured bits are passed through a low pass filter circuit, modelled by $R_{LOAD}$ = 1 $k\Omega$ and $C_{LOAD}$ = 2 pF (see Fig. 5.7(a) in section 5.3). The values of this resistor and capacitor were chosen such that the electronic front-end operates at $1/4^{\text{th}}$ of the bandwidth of the respective data channels, as discussed in section 5.3.1. In this model, we are processing the data captured by the DCA, which is essentially a voltage signal detected with a 50 Ω load. In a complete implementation, the electronic front-end will receive the PD current first, which will be used to charge the capacitor ($C_{LOAD}$ = 2 pF) and the resultant voltage from the capacitor will be sampled by the ADC. In [105], we have demonstrated error free detection of a 20 Gb/s optical bit stream generated from the optical front-end with the typical SOI delay waveguides of 2.5 dB/cm propagation loss. In this demonstration, we choose the data captured from the 20 Gb/s front-ends with the low-loss SOI waveguide based delay lines as an example to validate the proposed concept. Fig. 5.15 shows the cumulative voltage signal for every four bits from the charge storage

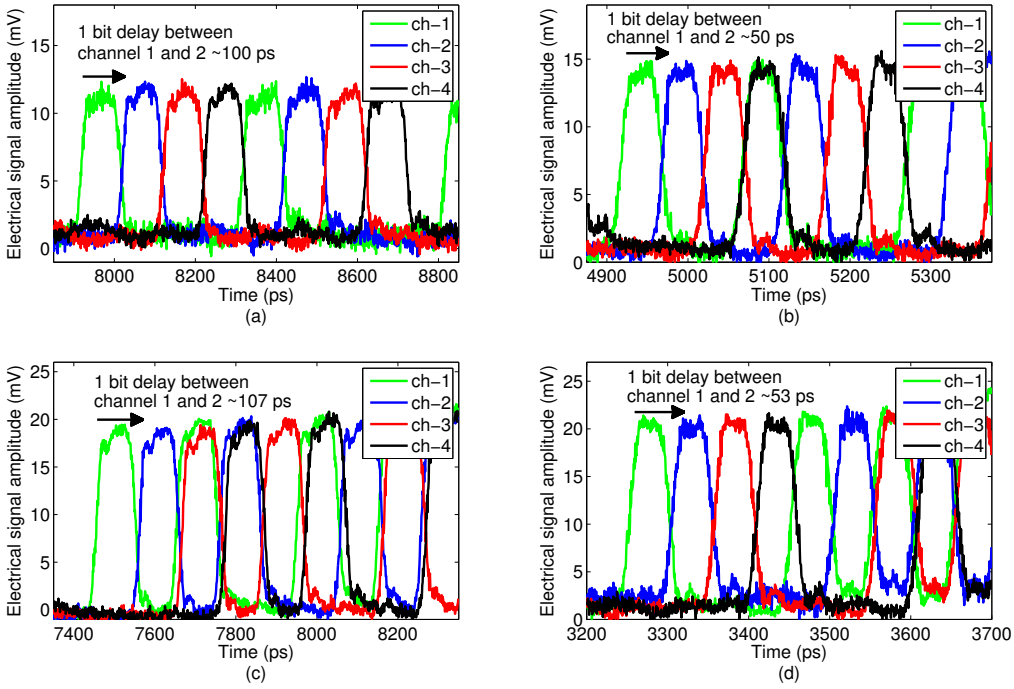



**Fig. 5.14** One bit delay between the adjacent four channels for (a) 10 Gb/s, (b) 20 Gb/s, (c) low-loss 10 Gb/s and (d) low-loss 20 Gb/s time sampling optical front-end.

mechanism of '$C_{LOAD}$' (voltage at point '$A$' in Fig. 5.7) and the sampled voltage at every four bit time interval (voltage at point '$B$' in Fig. 5.7) for the input bit stream generated from the 20 Gb/s front-end with low-loss 220 nm × 3 $\mu$m cross-section area SOI waveguide based delay line. The binary values of the input bit streams are also shown in Fig. 5.15 for illustration. As expected, the averaged signal at point '$A$' increases for every input bit '1' whereas it holds its previous value for every input bit '0'. It should be noted that for every input bit '0', there is no noticeable discharge from $C_{LOAD}$, as previously described in section 5.3.1. At every four bits interval the cumulative signal at point '$A$' is sampled and the sampled values are processed offline in MATLAB to solve a set of four linear equations using the algorithm described in section 5.3. It is seen from Fig. 5.15 that the sampled

signal values from each of the four channels (at point '$B$' in Fig. 5.7) are unique, although they are derived from the same input bit streams which are delayed by one bit duration from each other. Therefore, the four sampled values at each sampling period form a set of unique symbols that can be mapped to the original input bit stream by solving the four linear equations, as stipulated in the algorithm described in section 5.3.

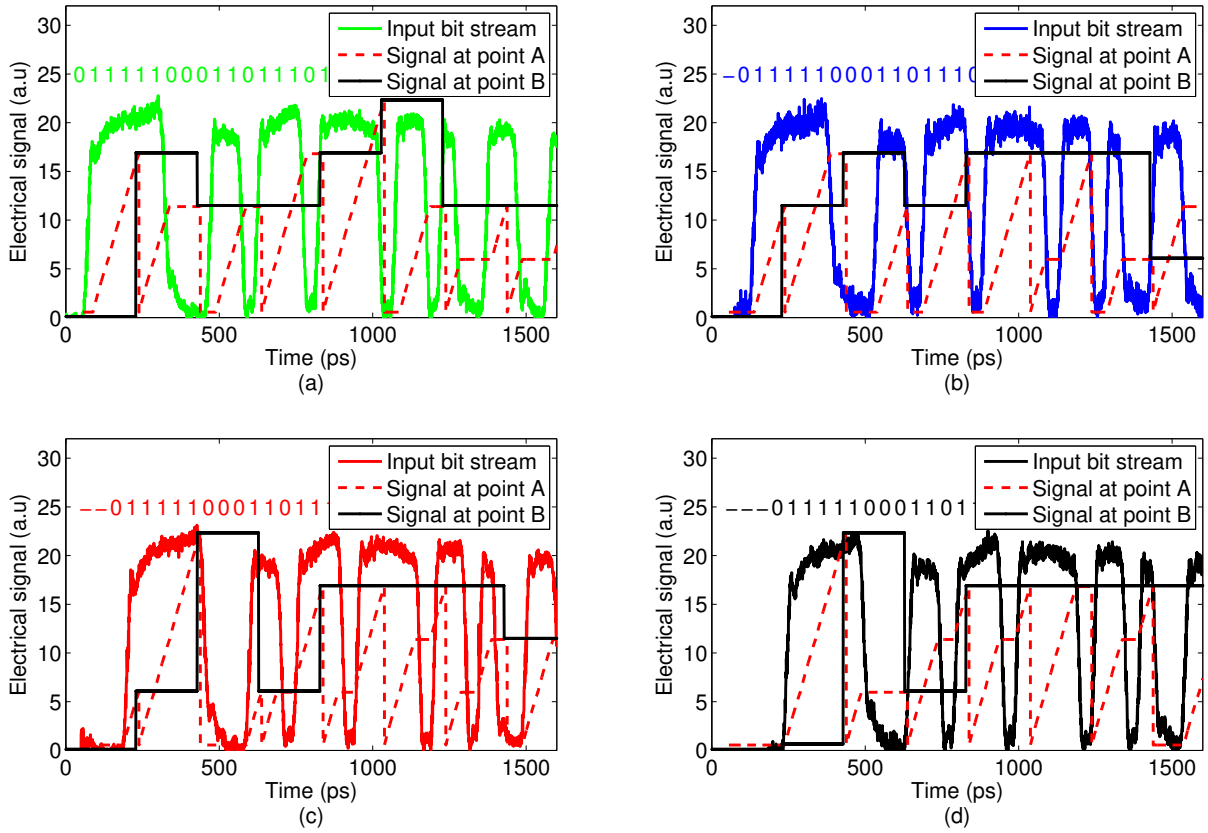



**Fig. 5.15** Averaged and sampled signals from the input bit stream from (a) Ch-1 or PD-1, (b) Ch-2 or PD-2, (c) Ch-3 or PD-3, and (d) Ch-4 or PD-4 of the 20 Gb/s optical front-end with low-loss delay waveguide.

Fig. 5.16 shows the regenerated original bit stream after solving the set of linear equation using the samples values at point '$B$' in fig. 7(a). From this figure, it is seen that all the bits in the $2^{15} - 1$ PRBS bit stream were regenerated accurately.

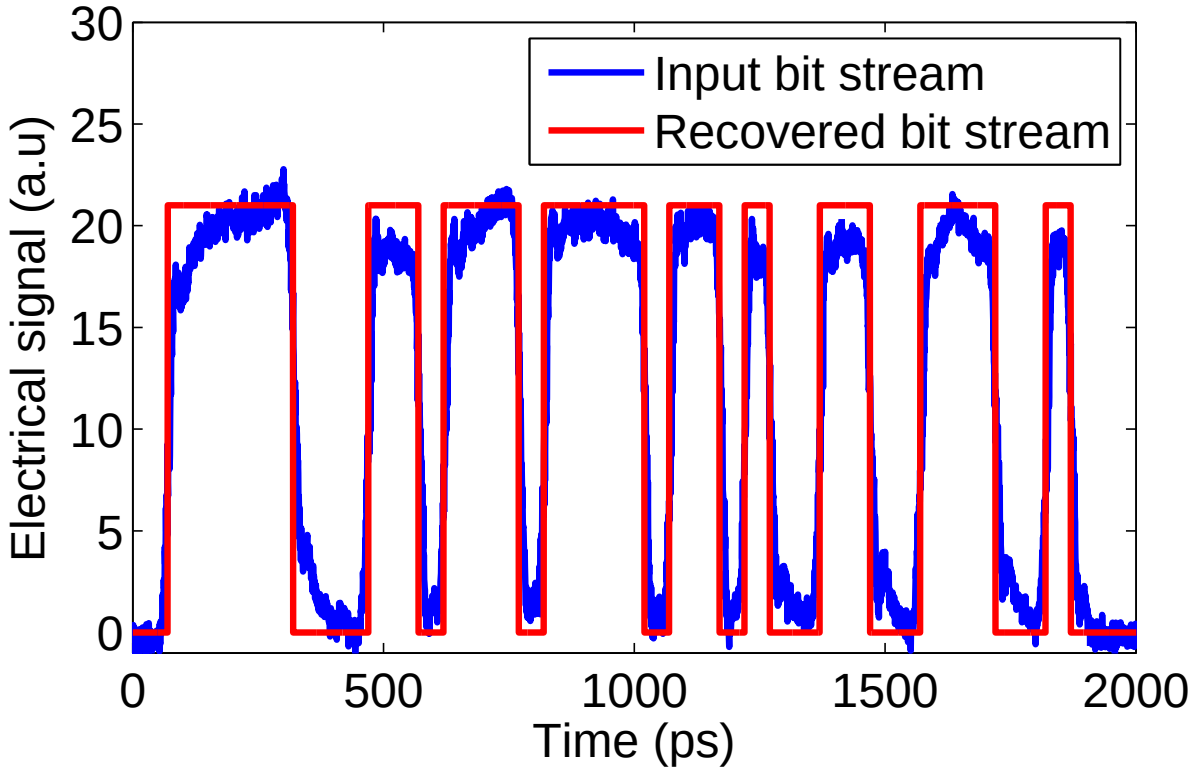



**Fig. 5.16** Recovered input bit stream by solving the four linear equations.

## 5.5 Discussion

The data rate of the optical receivers can be extended at a lower cost and with less complexity by using the methodology of the time sampling based optical front-end presented in this chapter. To increase the data rate of the photoreceiver, the bandwidth scalability of all the three important sections of the proposed receiver, *i.e.*, optical front-end, analog RC front-end and post-electronic digital circuit must be considered. If higher speed PDs need to be integrated with the electronic circuit, then the wire bonding and bandwidth requirement on the electronic front-end can be relaxed by increasing the number of PD channels in the optical front-end. The optical loss per channel will increase in this case due to the large optical power-dividing ratio, whereas the delay waveguide loss will decrease

due to the use of shorter one bit duration delay length waveguide at higher data rate. For example, if a 80 Gb/s data rate photoreceiver is achieved using the 60 GHz Si-Ge PD described in [65], then the same 5 Gb/s electronic front-end model presented in this chapter can be used, if the number of optical channels is increased from 4 to 16. However, the theoretical optical loss per channel would increase from 6.1 dB to ∼12 dB due to the 1 to 16 optical power-splitting ratio in this scenario. The analog part of the proposed electronic front-end model has a RC bandwidth of ∼80 MHz ($R_{LOAD}$ = 1 kΩ and $C_{LOAD}$ = 2 pF), which is much lower than the input signal bandwidth (∼14 GHz for 20 Gb/s data rate signal). A similar type of analog electronic front-end, which also does not require a TIA, is proposed in [66]. In this case the reported RC bandwidth of the circuit is ∼290 MHz ($R$ = 2.2 kΩ, $C$ = 250 fF), which is used to process a 24 Gb/s signal by using a different methodology than the one presented in that article. Therefore, in terms of bandwidth scalability of the whole receiver, the analog RC front-end does not impose any challenge. This facilitates simple and low-cost integration of optical and analog electronic front-ends by wire bonding. Incorporating tunable time-delay and/or couplers (either thermally or electrically) in the optical front-end section of the photoreceiver could make the proposed device more robust to fabrication process variations. The performance of the overall photoreceiver will improve by simultaneously tuning the optical time delay or the coupling ratio in the optical front-end and the sampling time duration in the electronic front-end. Recent progress in the silicon photonics fabrication process makes it possible to integrate thermally tunable delay-lines [106, 107] and directional couplers [108] within SiP PICs. Integrating these components with the proposed photoreceiver can achieve accurate one bit time delay and proper coupling ratios in the directional couplers such that uniform output power is achieved over all the four PD channels in case of fabrication process variation.

In the electronic front-end of an optical receiver, the TIA is the most power-consuming component, and the power budget for the receiver must increase with the bandwidth of the TIA [63,66]. Therefore, a TIA-less RC front-end, such as the one used in the proposed method, will lead to an overall more power efficient receiver architecture. In addition, since most of the post-processing is performed by a digital circuit, this receiver architecture can take advantage of the efficiency improvements offered by CMOS technology scaling [66]. The sensitivity of the electronic front-end could improve by replacing the passive RC circuit with a TIA. Nevertheless, the demonstrated optical front-end would require TIAs with a lower bandwidth than a conventional photoreceiver. Moreover, the need for TIAs with a smaller bandwidth will also reduce the integration and manufacturing cost of the receiver. However, the use of TIAs might not reduce the power budget of the receiver even with lower bandwidth of operation because the number of TIAs used in this approach scales with the speed reduction factor or number of PD channels in the optical front-end.

Speed reduction factor in the post-processing digital circuit is proportional to the number of PDs. However, this would require increasing number of delay waveguides and directional couplers (number of PDs – 1). The monolithic integration of increasing number of delay lines, directional coupler and photodetectors will not increase the design complexity of the optical frontend. However, due to the requirement of larger optical power splitting ratio optical loss per PD channel will increase and this will decrease the peak to peak voltage generated from the PD. The reduced peak to peak voltage and increasing number of RC passive integrator circuit will introduce more design complexity in the electrical front end. This will reduce the yield of the overall photoreceiver and increase the power budget of the both electrical and optical front end.

## 5.6 Summary

In this chapter, an optical front-end based on an optical sampling technique was presented. The error free detection of a $2^{15} - 1$ PRBS optical bit stream at 20 Gb/s data rate is demonstrated. The 20 Gb/s optical data detected by the optical front-end is processed offline by using a low bandwidth (∼80 MHz RC analog circuit and 5 Gb/s data rate post-processing digital circuit) electronic front-end model. The data reported here was obtained with an optical front-end with low-loss SOI delay waveguides but the proposed architecture is also compatible with standard SOI waveguides [105]. Simplified relation between the directional coupler power coupling ratio and fabrication dependent waveguide loss parameter is derived to achieve uniform power distribution across all the four output channels. This shows that optical front-ends with low-loss delay waveguides can be designed with relaxed coupling ratio. The experimentally demonstrated optical time sampling front-ends allow for the integration of high speed Si-Ge PDs with low cost and low-bandwidth electronic circuits. Therefore, the proposed architecture enables the utilization of the full bandwidth of high speed PDs while requiring TIAs and processing electronics that operate at significantly slower data rates. Harnessing the feasibility of one bit delay lines in optical domain leads to an overall low-power and low-cost photoreceiver architecture.

# Chapter 6

# Other Work

In this chapter, we present the result of two other research projects that were conducted in parallel with this work. We have designed a 16 GHz balanced photodetector [100] and a ring-based 25 Gb/s DAC-less PAM-4 modulator [109], on silicon photonics platform. In the next two sections, we will briefly discuss the design and performance results of these two devices.

## 6.1 A 16 GHz silicon-based monolithic balanced photodetector

Optical coherent detection is considered as the most favored solution for long-haul optical communication networks beyond 100 Gb/s data rate. The optical coherent communication link offers high capacity through polarization division multiplexing and supports complex modulation formats and digital signal processing based impairment mitigation techniques [99, 110, 111]. In a coherent receiver, the optical hybrid mixes the signal with a local oscillator with quadrature phases (0, 90, 180 and 270-degrees). The output of the hybrid has to be detected and subtracted for the out-of-phase ports to extract the in phase

and quadrature signals. This can be achieved either by using a balanced photodetector (BPD) [99] or a differential amplifier [112]. We have designed a BPD with on-chip biasing capacitors. The BPD subtracts the signal on chip and provides a large electrical output swing which eliminates the need for using external wide bandwidth linear TIAs. The BPD has a bandwidth of 16.2 GHz at 50 Ω load and supports 25 Gb/s optical signals without requiring signal post-processing. The photodetector has an output voltage signal of 28.5 $mV_{p-p}$ at a received power of –6.95 dBm providing greater margins in designing power efficient receiver.

Fig. 6.1 shows the cross-section of the Ge-on-silicon PD fabricated at the Institute of Microelectronics (IME), Singapore, the figure is taken from ref. [65]. Fig. 6.1(a) shows the thickness of the silicon waveguide (220 nm), two via layers (600 nm and 1.5 $\mu$m), and two metal layers (750 nm and 2 $\mu$m). The upper metal layer is used for on-chip routing and for designing electrical pads for probing or wire-bonding. The PD is built with the epitaxial grown Ge layer on top of the silicon. The Ge layer has a thickness of 500 nm (Fig. 6.1(b)) and it is $n$-doped to form the cathode electrode of the PD, whereas the silicon layer is $p$-doped to form the $p$-type electrode or anode.

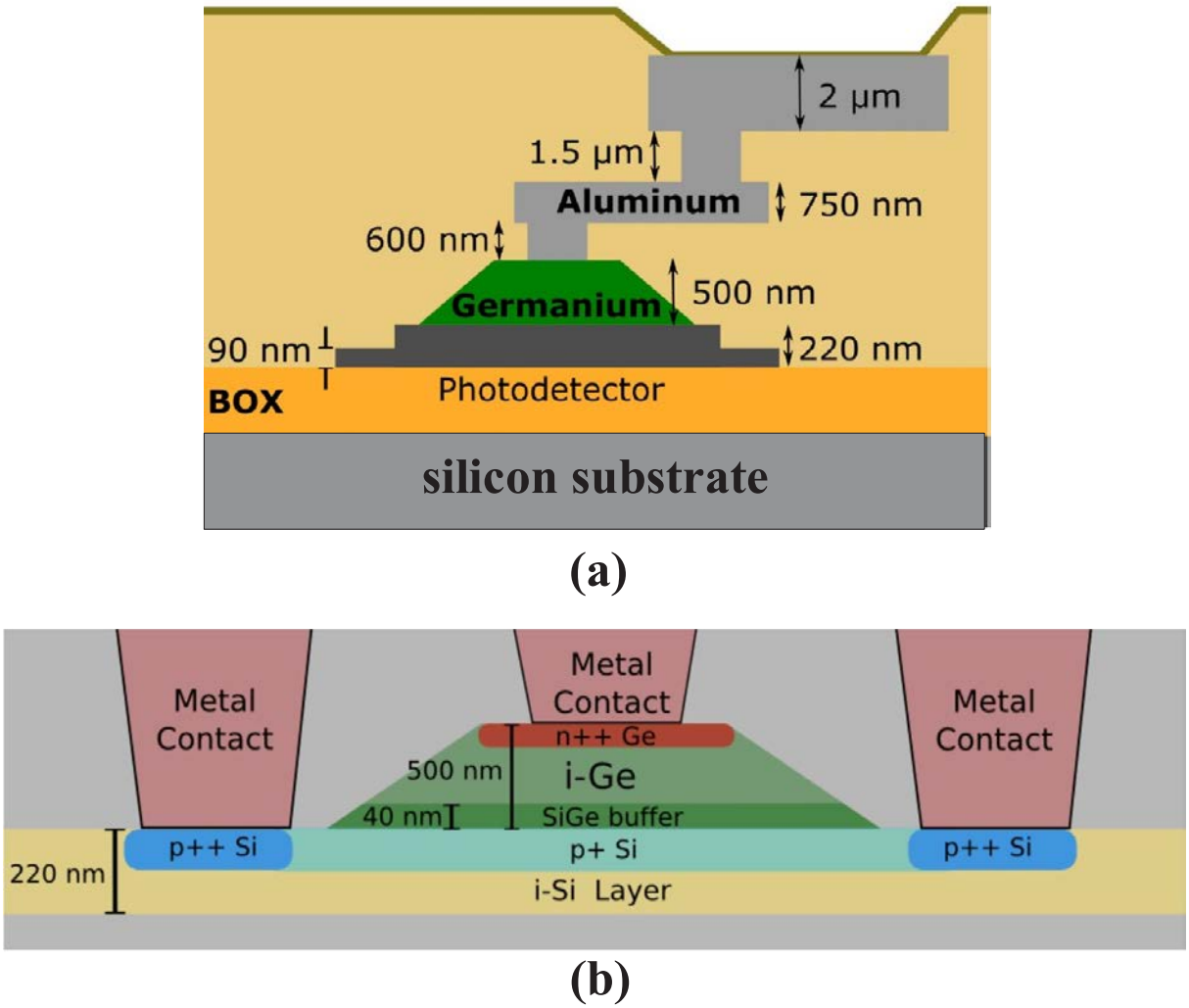



**Fig. 6.1** (a) Cross-section of the Ge-on-silicon photodetector with two metal layers for interconnection, (b) Cross-section of the photodetector showing the $p-i-n$ junction and metal contacts [65].

A photodetector requires a DC blocking capacitor to complete the electrical path through AC signal ground and to isolate the DC bias voltage from the output load. Off-chip capacitors with an external bias tee circuit can be used for this purpose. The design of off-chip bias tee with DC block capacitor is simpler for single PD. On the other hand for

BPD's design, the off-chip bias circuit becomes complex due to the need of two DC blocking capacitors. Integrating on-chip DC block capacitor with BPD can greatly simplify the integration of the BPD with other building blocks of a circuit such as coherent receiver or phase demodulator for DPSK and DQPSK at the optical input port. The electrical design of the coherent receiver requires a linear front-end. By integrating the photodetectors, improved sensitivity and voltage swing can be achieved, which simplifies the TIA and linear amplifier design, at the electrical output port of the BPD.

The DC blocking capacitor is designed using two parallel plate metal layers with a separation of 1.5 $\mu$m between them. A metal insulator metal (MIM) capacitor can be formed between these two layers as shown in Fig. 6.2. Metal areas of equal dimensions are used in metal layer 1 ($M1$) and 2 ($M2$). Upper metal layer of the MIM capacitor is used as the ground layer. The other end is connected to $M1$ and then to the bias supply in $M2$, through a VIA layer connecting both layers $M1$ and $M2$.

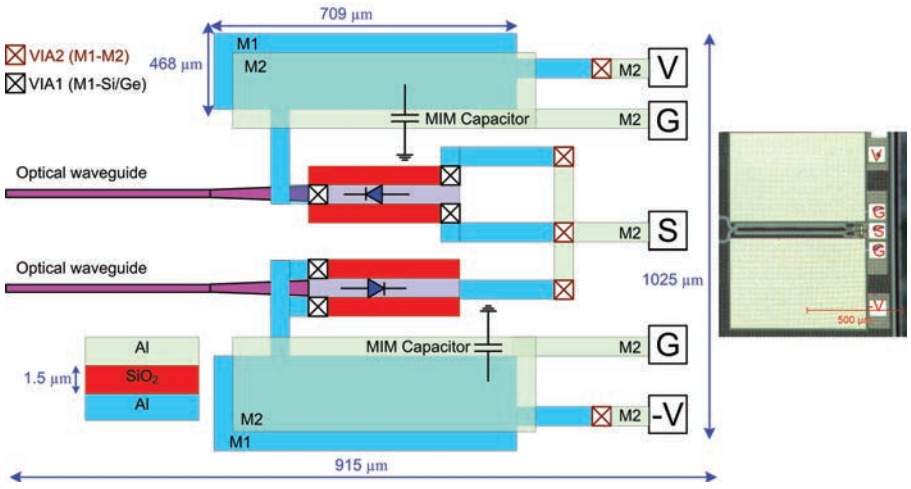



**Fig. 6.2** Photodetector with on-chip capacitor for biasing ($G$: ground, $M1$: metal 1, $M2$: metal 2, MIM: metal-insulator-metal, $S$: signal. The drawing is not according to the scale).

The required capacitor area is studied through simulation using ANSYS HFSS software. It is observed that a capacitor made of two metal plates of area 709 $\mu$m $\times$ 468 $\mu$m is a good design choice for biasing condition. First, the capacitance ($C$) of the parallel metal plate or MIM capacitor is determined using the following analytical formula in Eq. 6.1:

$$C = \frac{k\epsilon_0 A}{d} \tag{6.1}$$

where, $k\epsilon_0 = 3.9 \times 8.854 \times 10^{-12}$ F/m is the permittivity of $SiO_2$ (dielectric material between the two metal plates), $A = 0.33 \times 10^{-6}$ m$^2$ is the area of the metal layer, and $d = 1\ \mu m$ is the effective distance between the two parallel metal plates. The actual vertical distance between the two parallel metal layers is 1.5 $\mu$m. However, due to the large area of the metal plates, the vertical distance between the two metal layers decreases at the middle region during fabrication. Therefore, effective distance between the two metal plates is assumed to be 1 $\mu$m. The analytical value of the capacitance is 11.5 pF, calculated using Eq. 6.1.

Next, HFSS simulation is performed to obtain the frequency dependent capacitance of the MIM capacitor. In HFSS, first the reflection coefficient ($S_{11}$) and the admittance ($Y$) parameter of the circuit is found through numerical simulation and then the capacitance is calculated using Eq. 6.2:

$$C = \frac{1}{\omega \times Im(Y)} \tag{6.2}$$

where, $\omega$ is the angular frequency in radian. The admittance parameter ($Y$) is related to the reflection coefficient ($S_{11}$) according to the following formula in Eq. 6.3 [113]:

$$Y = G + j\omega C = \frac{(1 - S_{11})}{Z_0(1 + S_{11})} \tag{6.3}$$

In Eq. 6.3, $G$ and $Z_0$ are the conductance and characteristic impedance of the MIM capacitor, respectively. The resulting capacitance from HFSS simulation is presented in Fig. 6.3. From this figure, it is observed that over a bandwidth of 20 GHz the capacitance is always above 13.5 pF. The value of the capacitance obtained from the HFSS simulation is close to the analytical value of the capacitance calculated using Eq. 6.1.

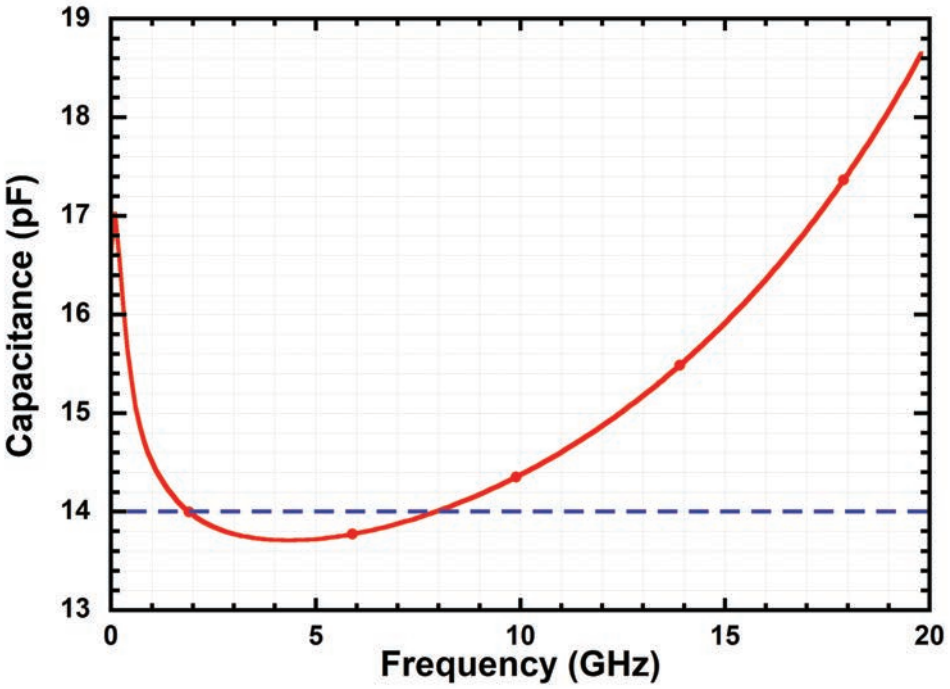



**Fig. 6.3** Simulated capacitance as a function of frequency of the MIM capacitor.

In Fig. 6.3 frequency dependence of the capacitance is observed, as the reflection coefficient ($S_{11}$) of the MIM capacitor is a frequency dependent parameter. The loss tangent ($\tan\delta$) of the dielectric ($SiO_2$) is also a frequency dependent parameter, which is generally calculated from the measured value of capacitance using the following formula:

$$\tan\delta = \frac{G}{\omega C} \tag{6.4}$$

The electrical model for the BPD is presented in Fig. 6.4 where $I_{SIG}$ is the current though the 50 Ω load ($R_L$) and $I_{PD1}$ and $I_{PD2}$ are the current through the complementary photodetectors. In the electrical model, the on-chip capacitors $C_{G1}$ and $C_{G2}$ provides a high speed ground to the load. The inductor in the DC supply ($L_{LINE}$) is used to model the low speed transmission line.

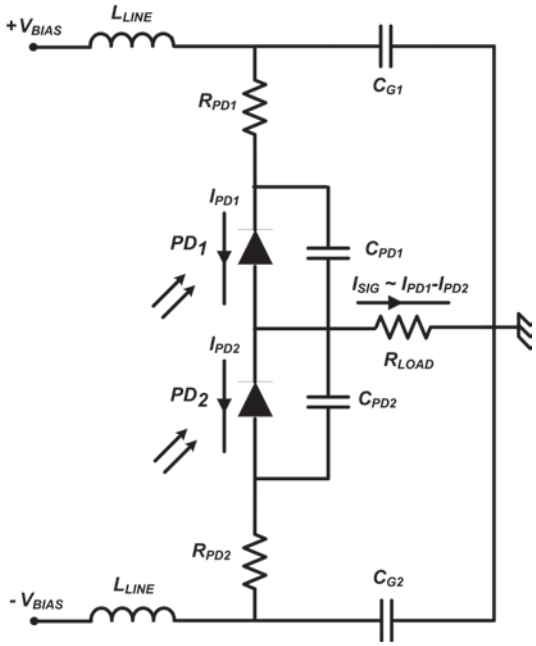



**Fig. 6.4** Schematic of the BPD with on chip capacitor.

The total dark current in the BPD with a bias of –1 V measured with a Keithley high precision picoammeter is ∼4.31 $\mu$A. The responsivity of the photodetector is presented in Fig. 6.5 as a function of the optical wavelength at –4.5 V bias. The responsivity of each of the photodetectors in the BPD is ∼0.7 A/W at 1550 nm wavelength.

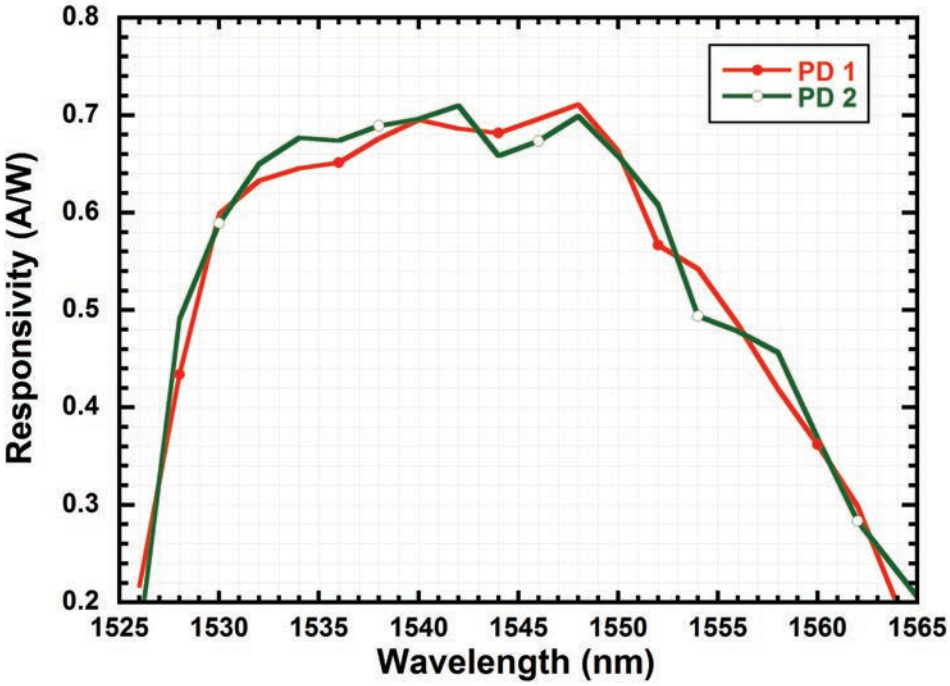



**Fig. 6.5** Responsivity as a function of frequency.

The frequency response of the BPD for different reverse biases is presented in Fig. 6.6. It is observed that with a bias of -4.5 V the balanced photodetector has a 3-dB bandwidth of approximately 16.2 GHz. An increase of the bias voltage beyond -4.5V does not improve the bandwidth. The common mode rejection ratio (CMRR) is also presented in Fig. 6.6. The measured value of CMRR is well above 30 dB for all the frequencies.

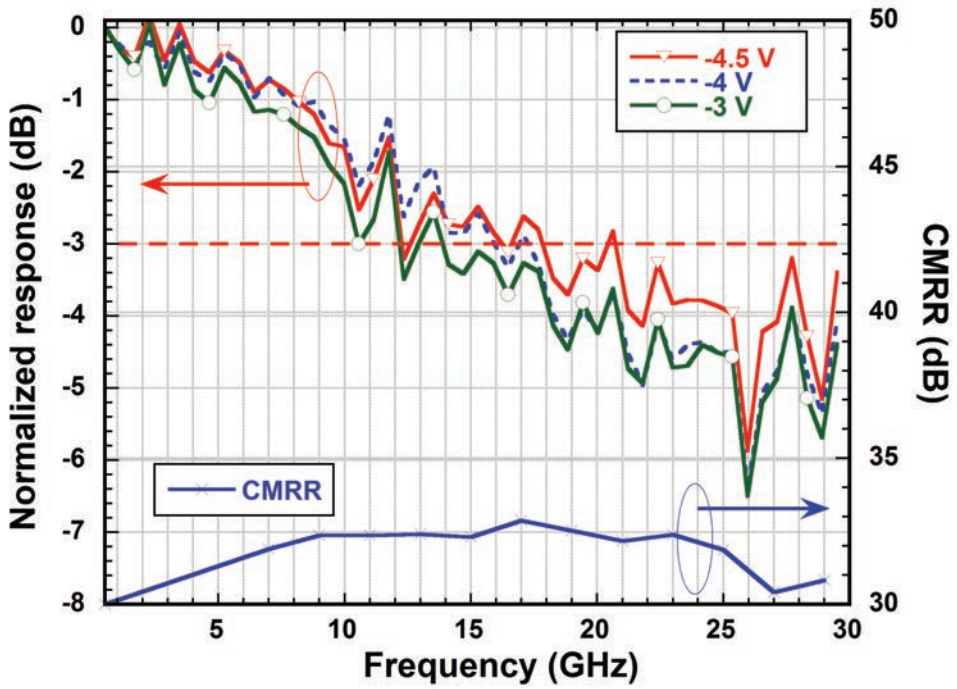



**Fig. 6.6** Normalized amplitude response as a function of frequency.

The BER performance of the of the balanced photodetector is evaluated in a 20 Gb/s return-to-zero differential phase shift keying (RZ-DPSK) system. The results of BER tests with a RZ-DPSK signal over 1 m of single mode fiber (SMF) are presented in Fig. 6.7. It is observed that with balanced detection and without any electrical amplification the photodetector has a sensitivity of –6.95 dBm. The results of the measurements at only the constructive (cnstr.) and destructive (destr.) port using single photodetector are also presented in Fig. 6.7. The sensitivity in this case is –3.84 dBm which is 3.1 dB worse than balanced detection. In order to verify the suitability of the photodetector at higher bit rates the results of BER tests with a NRZ OOK signal at 1550 nm at 25 and 30 Gb/s are also presented in Fig. 6.7. The results show that for 25 Gb/s the BER is $1.01 \times 10^{-12}$ for

a received power of –1.65 dBm. The output voltage swing in this case was about 48 mV. For a received power of -3.66 dBm, the BER is degraded to $\sim 10^{-9}$. At 25 Gb/s, the photodetector operates well over the hard and soft-decision forward error correction (FEC) threshold of $3 \times 10^{-3}$ and $1.8 \times 10^{-2}$, respectively [114].

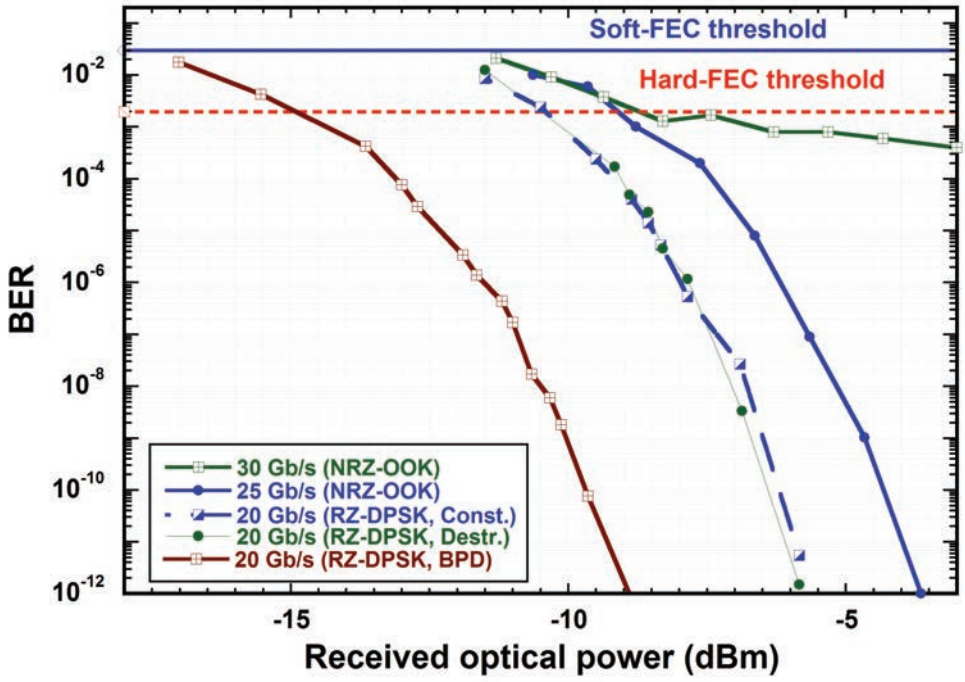



**Fig. 6.7** BER as a function of received optical power at the chip (coupling loss of 10 dB deducted).

These results confirm that the BPD is suited for a $4 \times 25$ Gb/s coherent receiver and 25 GBaud differential phase shift keying (DPSK or DQPSK) demodulator applications. At 30 Gb/s the best BER is observed at the received optical power of –1 dBm. The BER of $3.98 \times 10^{-4}$ is well above both hard and soft-decision FEC limit as well. Therefore, the BPD has the possibility of being used at higher bit rates when used with FEC and DSP techniques. At 25 Gb/s neither FEC nor DSP is required for short reach applications. It should

be noted that the sensitivity of the photodetector would improve if post-amplification is applied after the photodetector before BER testing. Recent results with post amplification show a sensitivity of -7.3 dBm at 28 Gb/s using a Ge on Si photodetector [63]. Overall, the photodetector has very good possibility of being used within coherent or DPSK/DQPSK receiver.

## 6.2 A ring-based 25 Gb/s DAC-less PAM-4 modulator

Intensity-modulated/direct-detection (IM/DD) based optical communication link is a promising low-cost solution to build 100 Gb/s/ data rate for short reach (200 m to 2 km) interconnects between data centers [40]. Advanced modulation format based MZM on silicon photonic platform offers the possibility of designing power efficient, low-cost and integrated IM/DD networks. The linear phase shift with an applied reverse bias voltage and long electrode structure of the MZMs facilitate the design of segmented electrode based PAM-4 (two segment electrode) or PAM-16 (four segment electrode) modulators [34]. However, to reduce the driving voltage amplitude and footprint of the transmitter, researchers are also investigating the operation principle of resonance based modulators (*i.e.*, ring modulators [115] or MZI assisted ring modulators [116]) to generate PAM-4 modulation format signal. It remains challenging to design multiple segment electrode structure on the small perimeter of ring modulator (e.g., 50 $\mu$m ring perimeter in [115]). For example, to circumvent the ring small radius in [115], a single electrode ring modulator generates 60 Gb/s (30 GBaud/s) PAM-4 optical signal. The PAM-4 electrical signal is initially generated using a three bit DAC.

We have designed a novel PAM-4 12.5 Gbaud/s inter-coupling modulator based on a Mach–Zehnder interferometer assisted ring resonator. The 25 Gb/s PAM-4 optical signal

is generated by driving the modulator with two independent electrical signals with an amplitude of 3 $V_{pp}$ at 2 V reverse bias. Reverse bias operation mode of the modulator enables achieving an electro-optic (EO) bandwidth of approximately 14 GHz without pre-emphasis of the electrical driving signals or equalization techniques. This configuration successfully simplifies the operation of the modulator in generating PAM-4 signals without the need for a DAC. Experimental results show proper generation of a PRBS data stream. The proposed modulator has a compact footprint of 0.48 $mm^2$ with a bandwidth density of 52.08 $Gb/s/mm^2$.

In the proposed MZI assisted ring modulator, two $p-n$ diode electrode segments are designed on the MZI arm for inter-coupling modulation. The phase of the two independent electrical driving signals are adjusted such that a 12.5 Gbaud/s PAM-4 signal is achieved at the output. We have also included a heater layer on top of the coupler arm to tune the coupling ratio of the modulator such that larger extinction ratio is achieved in the presence of thermal or fabrication variations. The schematic of the proposed multi-segmented inter-coupling PAM-4 modulator is shown in Fig. 6.8. The inter-coupling PAM-4 modulator can be driven with single ended electrical signals reducing the complexity of the voltage settings.

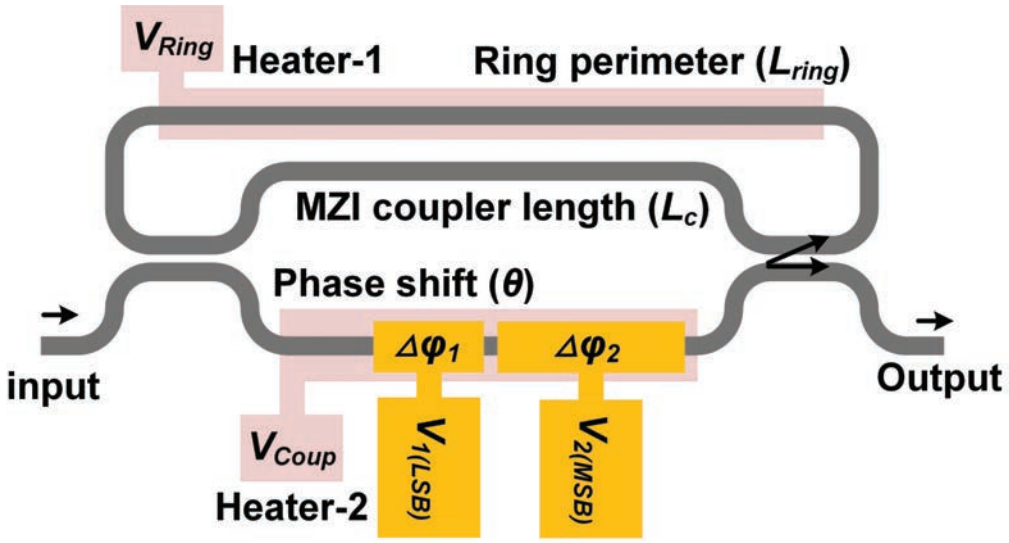



**Fig. 6.8** Schematic of the proposed inter-coupling modulation based PAM-4 ring modulator.

In the configuration, the optical signal modulation is enabled by coupling modulation, change in the round-trip phase shift and slight variation of its loss. The modulator has two $p-n$ diode segments in the lower arm of the balanced MZI with lengths of 220 $\mu$m and 330 $\mu$m. There are also two thermal heaters that were implemented with the top metal layer. The smallest $p-n$ diode segment generates a phase shift $\Delta\phi_1$ with an RF signal $V_1$ representing the lowest significant bit (LSB). The largest $p-n$ diode segment generates a phase shift $\Delta\phi_2$ with an RF signal $V_2$ representing the most significant bit (MSB). The heater in the ring (heater-1) is at the top of the cavity to enable a shift in the resonance wavelength so to align it with the laser to modulate. The heater in the lower arm of the MZI (heater-2) generates the required initial phase $\theta$ to optimize the extinction ratio and exploit the linear optical transmission portion of the modulator. In this device, the ring cavity length ($L_{ring}$) and MZI coupling length ($L_c$) is determined mainly based on

the total length of the two $p-n$ diode segments to generate the required phase shift for modulation. The optimized design of the modulator has a cavity feedback length of $L_{ring} =$ 885 $\mu$m and a MZI coupling length of $L_c = 694$ $\mu$m. Fig. 6.9 shows the simulated spectral response of the designed PAM-4 modulator for four voltage conditions. The simulation results show the inter-coupling effect where the resonance extinction ratio is changing for the applied voltages. The cavity phase shift effect on the resonance wavelength for various biasing voltages is also apparent. Based on the simulation results the FSR of the designed modulator is 0.39 nm.

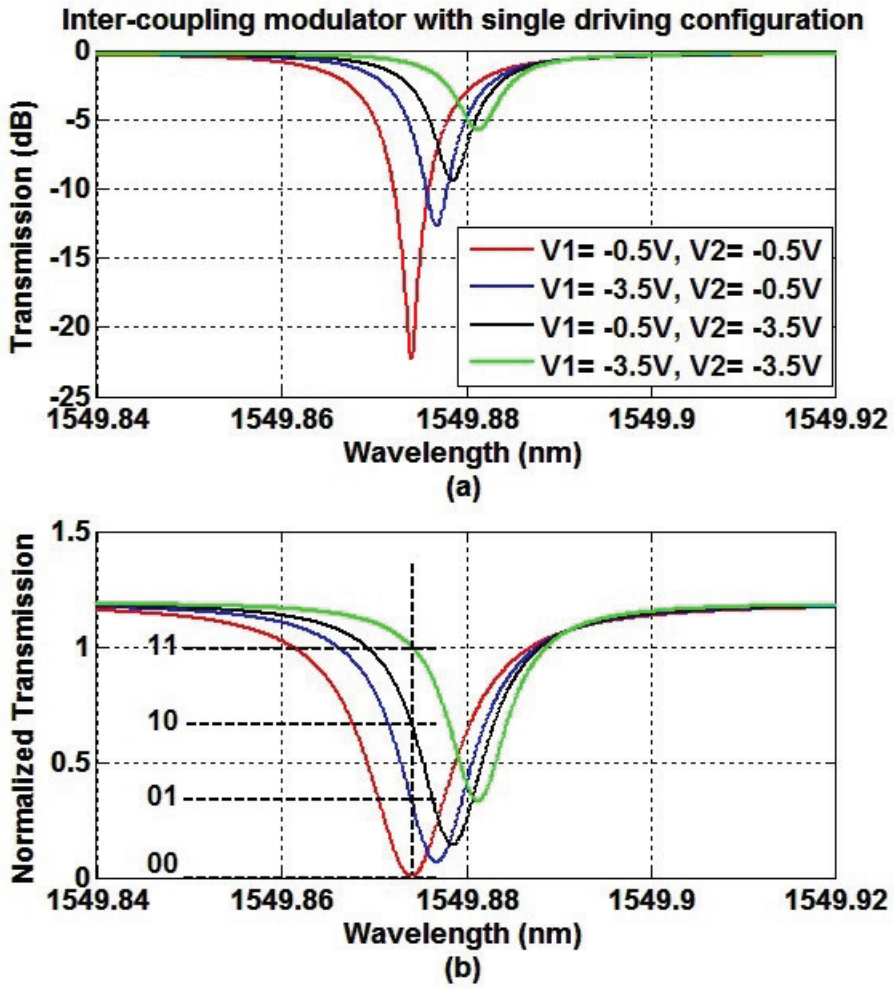



**Fig. 6.9** The simulated spectral response of the modulator at for four input voltage conditions, (a) in logarithmic scale, (b) in linear scale.

Fig. 6.10(a) shows the characterization test setup of the fabricated modulator with the two DC and two GSGSG RF probes. The DC probes are used to apply DC voltages to the heaters to optimize the ring modulators extinction ratio ($V_{COUP}$) and to shift the resonance wavelength ($V_{Ring}$) to match the wavelength of the CW light source. Both the DC signals share common electrical ground (G) with the RF signals. Fig. 6.10(b) shows photograph

of the external fiber array and electrical probe connections to the chip.

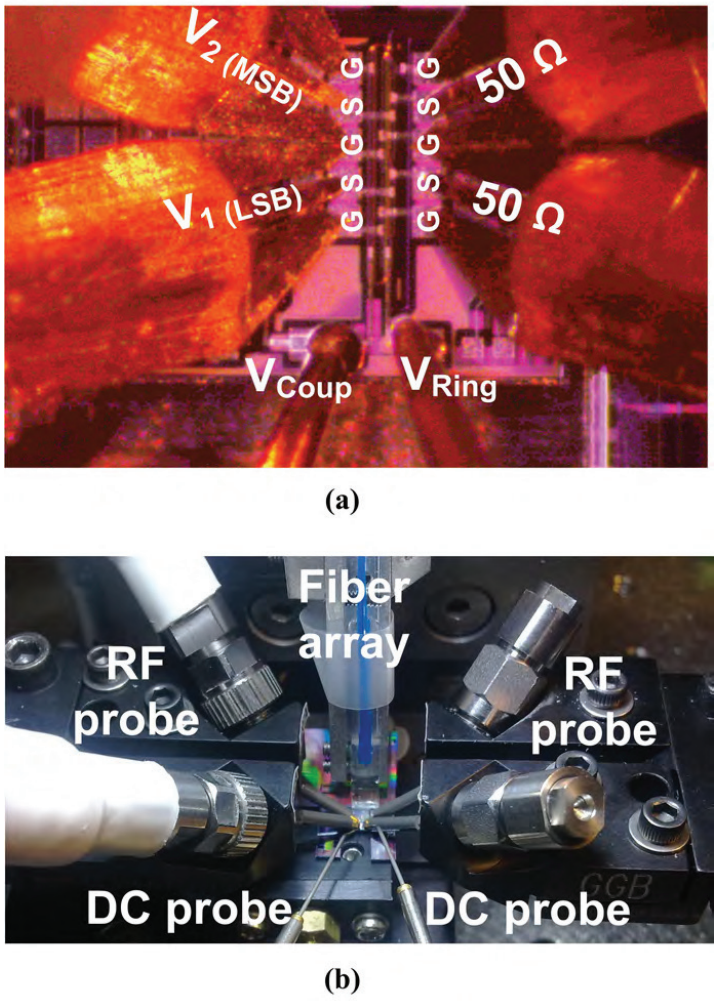



**Fig. 6.10** (a) Image of the chip test setup with DC and RF probes (b) Test setup photograph of the chip with fiber array and electrical probes.

We have tested the device to generate optical PAM-4 signal. To generate each of the two driving signals, we use two Anritsu-MU181020A PPG cards in synchronous mode to tune the phase of each of the electrical driving signal independently. As such, the rising

and falling edges of the two input signals occur at the same time. Fig. 6.11 shows the experimental setup to generate PAM-4 signal from the modulator. A 5 dBm CW light at the wavelength of 1552.8 nm is launched through the PC which optimizes the light coupled to the inter-coupling PAM-4 modulator. The average optical power at the output of the modulator is –9.6 dBm. The total optical loss from the laser to the modulator output consists of 0.6 dB insertion loss from the PC, 2 dB insertion loss from the modulator (DUT) and 6 dB loss per grating coupler. Two independent $2^{31}$-1 PRBS data from two PPGs are injected to two 20 GHz electrical amplifiers (model: Hittite HMC-C004) boosting the signal amplitude to 3 $V_{pp}$ and then be the input to two high-speed bias-T to add the desirable DC bias to the driving electrical signal. The DC bias is provided by two DC sources and reverse biased the diode segments. The two RF signal are injected to the LSB and MSB electrode segments of the inter-coupling ring modulator. The optically modulated signal is amplified with an EDFA to increase the received optical signal at the receiver. A 45 GHz photodetector converts the optical PAM-4 signal (responsivity: 0.5 A/W). The received optical power is 2 dBm. The electrical signal is finally captured with a sampling oscilloscope (DCA) with an RF bandwidth of 30 GHz.

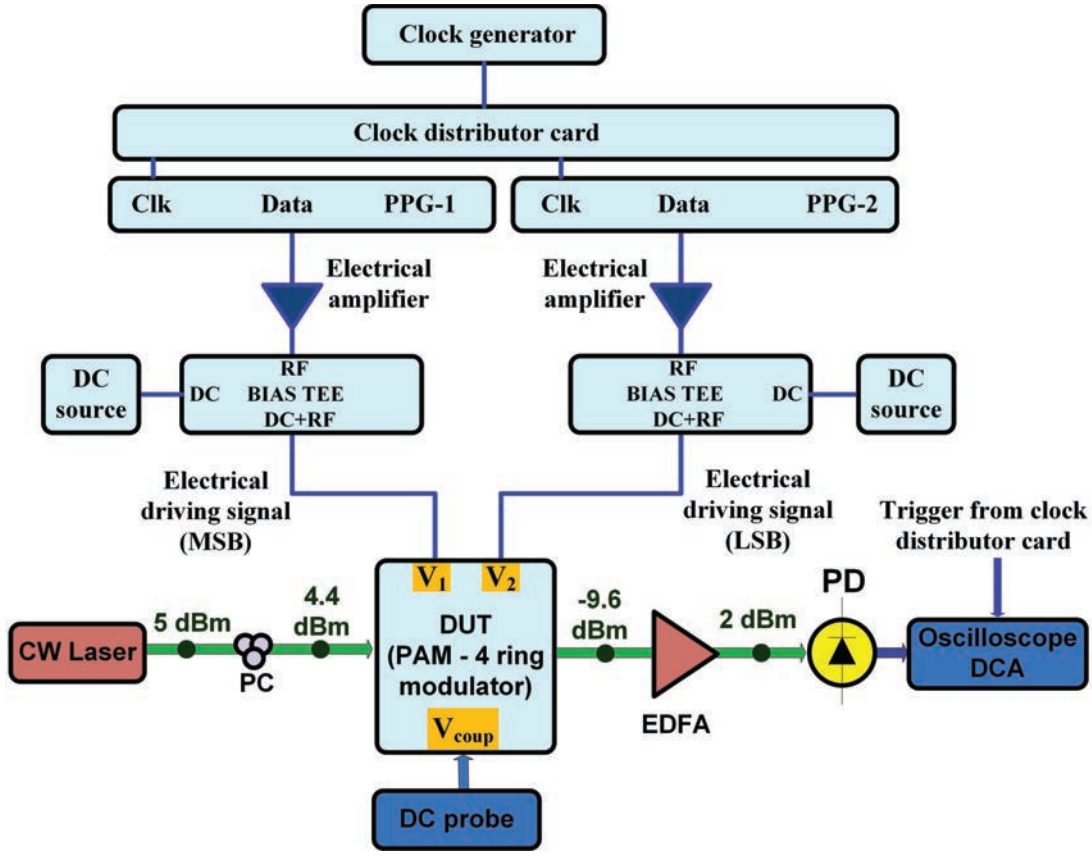



**Fig. 6.11** Experimental setup to generate PAM-4 modulated signal.

Fig. 6.12 shows the photodetected electrical eye diagrams from the output of the ring modulator when it is driven by $V_1$ (LSB) and $V_2$ (MSB), one at a time. The peak-to-peak voltage amplitude of the modulated signal for the shorter $p-n$ diode ($V_1$) is smaller (approximately half) than that of the longer segment ($V_2$) as the LSB diode segment (or phase shifter) length is smaller than the MSB segment length. Due to the nonlinear optical response to applied electrical voltage, the length ratio between the LSB and MSB segment is actually not half but 2/3 (220/330 = 0.66).

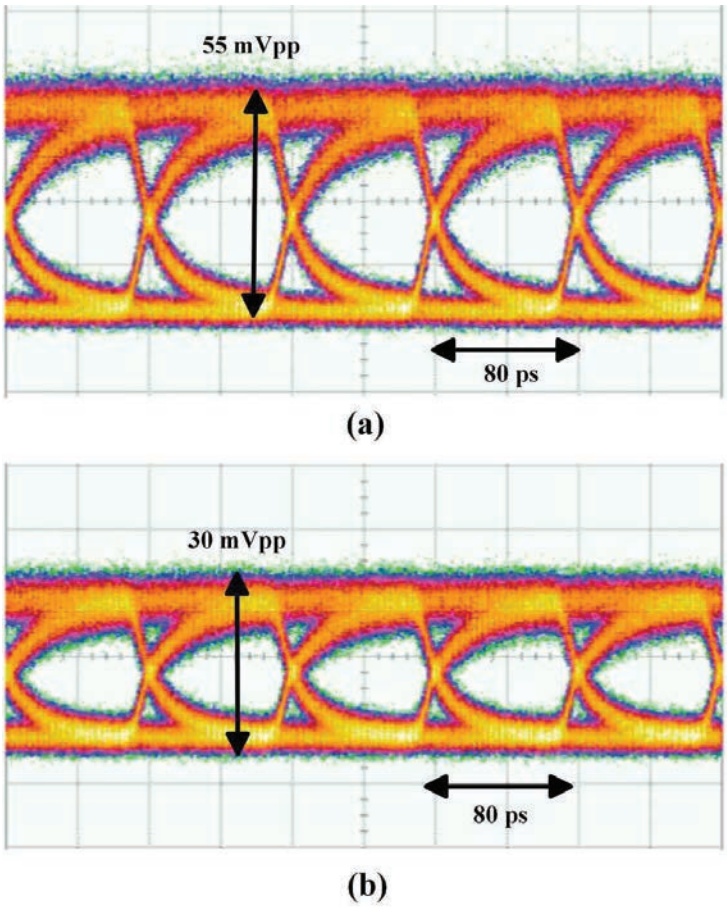



**Fig. 6.12** Eye diagram (12.5 Gb/s) at the output of the ring modulator when driven by (a) only $V_2$ (MSB), (b) only $V_1$ (LSB).

Fig. 6.13 shows the photodetected 25 Gb/s PAM-4 electrical eye diagram when the modulator is simultaneously driven by $V_1$ and $V_2$. The voltage difference between adjacent levels is approximately 25 mV leading to symmetric four level signal.

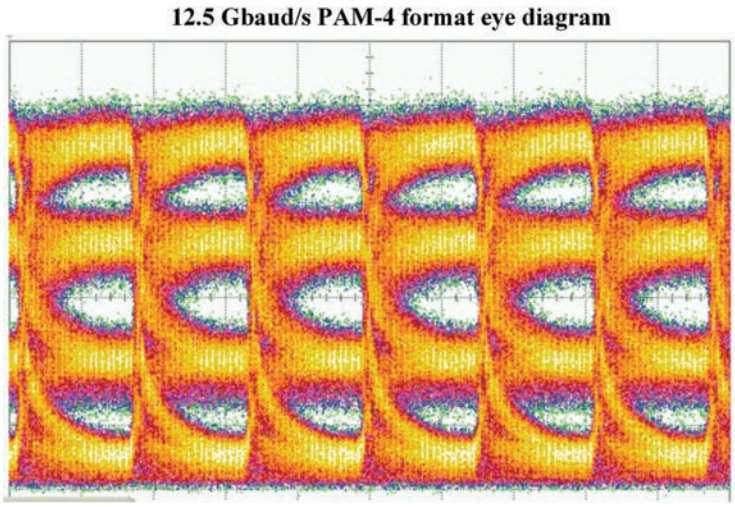



**Fig. 6.13** PAM-4 eye diagram (12.5 GBaud/s) at the output of the ring modulator when simultaneously.

## 6.3 Summary

In this chapter, in section 6.1, we have presented the performance result of a BPD with on-chip biasing capacitor. The photodetector exhibits a bandwidth of ∼16 GHz at –4.5 V of reverse bias. The photodetector exhibits a CMRR of 30 dB. The performance of the photodetector is evaluated in terms of BER versus received optical power. For 20 Gb/s DPSK signal the sensitivity of the photodetector is – 8.95 dBm with balanced detection. The results show that at 25 Gb/s, a BER of $1.01\times10^{-12}$ can be achieved for a received power of –3.65 dBm with a large output swing of 84 mV for NRZ-OOK signal. At 30 Gb/s BER of $3.98 \times 10^{-4}$ is achieved with received optical power of –3 dBm. The on-chip capacitors make the device compact and suitable for monolithic integration. The on-chip bias circuit in silicon photonic greatly facilitates packaging of the BPD alone with insignificant bandwidth

degradation. Overall, the photodetector has very good possibility of being used within coherent or DPSK/DQPSK receiver.

In section 6.2, we have demonstrated reverse bias operation of the MZI assisted ring modulator which enables generating PAM-4 signal with conventional OOK electrical driving signal. The 12.5 GBaud/s PAM-4 eye diagram obtained by inter-coupling modulation with 3 Vpp electrical driving signal shows promise towards the design of a power efficient optical modulator with small footprint of 0.48 $mm^2$. A test methodology was also presented to generate four level optical signals by tuning the extinction ratio of the device using DC heater. The heater layers on top of the waveguide demonstrated in this work introduce less optical waveguide loss (under 2 dB insertion loss) than conventional heavily doped heaters. Driving the modulator with single drive electrical signal further reduces the operation complexity of the modulator.

# Chapter 7

# Future work

In this chapter, we present two possible future research directions based on the work presented in this thesis. The two devices demonstrated in this work are fabricated using two different waveguide technologies: $Si_3N_4$ and silicon photonics platforms. We propose the possibility of designing the lattice MZI filter based optical demultiplexer to decrease the crosstalk between the wavelength channels in the PWSM device. We also present how the performance of the PWSM device can be improved by further decreasing the propagation loss of the waveguide. We finally propose the design of an integrated time sampling based optical front-end wire bonded to the CMOS electronic front-end.

## 7.1 Future work related to the two proposed photonic components

### 7.1.1 An eight-channel passive wavelength-striped mapping multiplexer

To increase the number of channels in the PWSM device from four to eight, two important challenges in designing the component should be addressed. First, the crosstalk between

the optical wavelength channels of the demultiplexer section of the PWSM device needs to be decreased. To achieve low crosstalk between channels, the optical phase shift in the delay arms of the MZI filters should be controlled by the thermal phase shifters. The thermal phase shifters consume electrical power and increase the operational complexity of the device. On the other hand, the AWG based demultiplexers demonstrate lower crosstalk (40 dB) than the MZI filter based optical demultiplexers (presented in this work) without the requirement of thermal tuning [37]. However, an AWG based PWSM device needs larger footprint due to the individual time delay requirements for each of the channels [46]. Therefore, other MZI based filter structures offering the benefit of individually time delaying the wavelength channels as well as generating low optical crosstalk should be investigated.

In optical lattice filters, two or three MZI filters are in a cascade for sharper frequency roll-off of the transmission response between passbands. In lattice filters, the optical insertion loss does not increase much and irrespective of the number of MZI stages, the number of input and output optical ports remains the same as the single stage MZI filter. A detailed synthesis algorithm to design an optical lattice filter can be found in [117]. Silica and silicon photonics based lattice filters demonstrating $> 15$ dB crosstalk have been proposed in [93] and [118], respectively. Fig. 7.1(a) shows the structure of the eight-channel lattice filter based demultiplexer reported in [93], where one three-cascaded, two two-cascaded and four single-stage $2 \times 2$ MZI filters were used to form the lattice structure. Fig. 7.1(b) shows the transmission spectra of the lattice filter with flat passband within 0.7 dB variation.

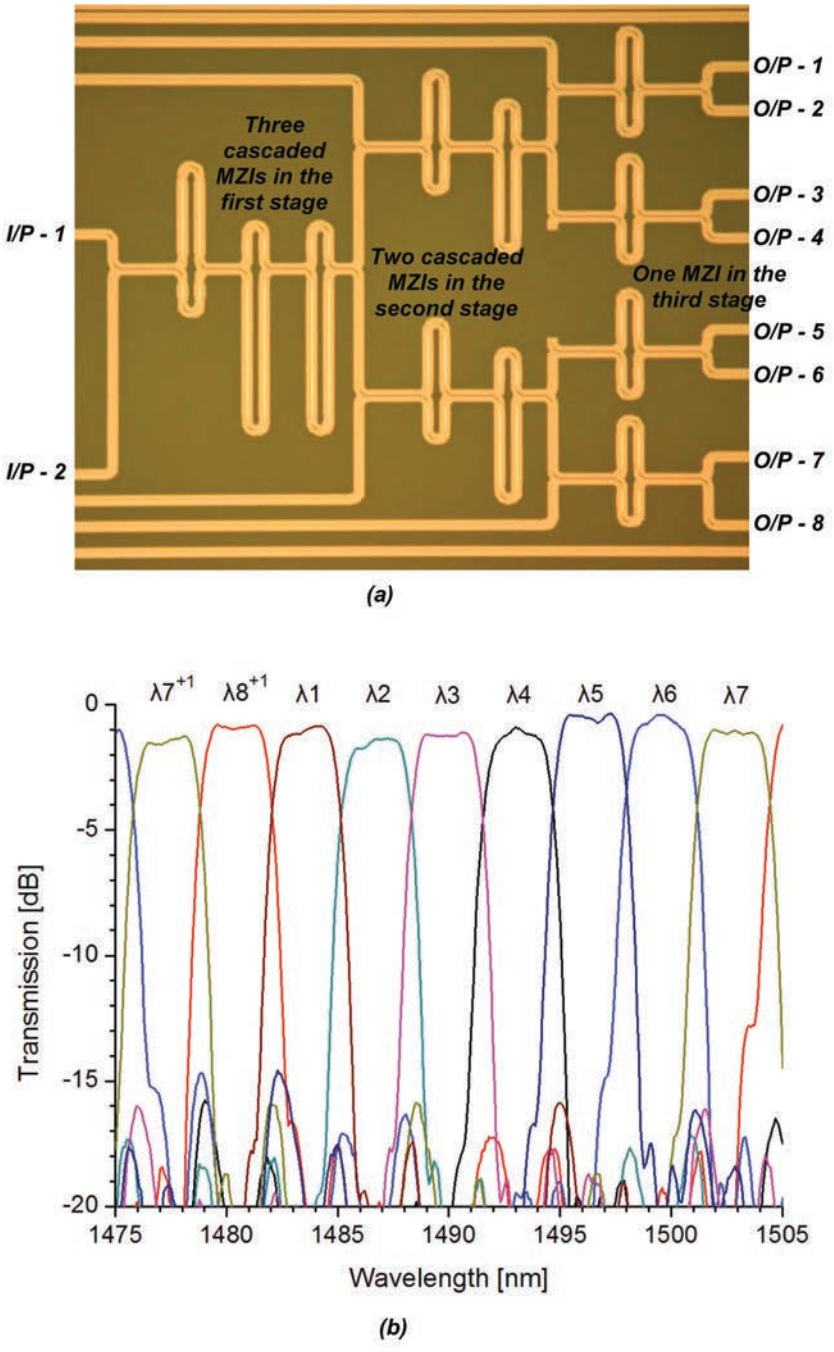



**Fig. 7.1** (a) Micrograph of the lattice MZI filter based eight-channel demultiplexer, (b) Normalized optical transmission spectra of the demultiplexer [93].

In an MZI based lattice filter, the filter coefficients are set by the coupling ratios of the intermediate couplers used in an MZI block. The coupling ratio varies from the 50:50 power splitting ratio. Therefore, the MZI filters need to be designed with the directional couplers, instead of the 3 dB 2 $\times$ 2 MMI couplers presented in this work, to create the arbitrary filter coefficients. Besides this, the position of the delay waveguides and structure of the delay arms of the MZI filters will remain similar to this work. Therefore, using the knowledge obtained from this work, it is possible to design a lattice filter on the $Si_3N_4$ waveguide platform to decrease the optical crosstalk of the PWSM device.

The optical insertion loss difference between $ch-1$ and $ch-3$ of the proposed PWSM device in this work is 28.8 dB (see fig. 4.6 in chapter 4). The loss difference is attributed to the 3.1 dB/m propagation loss in the 9.54 m long delay waveguide between the two channels. For the practical implementation of the proposed device in a wavelength-striped based network, it is important to design the $Si_3N_4$ waveguide with further low propagation loss. In [28], 0.1 dB/m propagation loss in the $Si_3N_4$ waveguide is achieved using the wafer bonding approach (thermally grown oxide). The low propagation loss (0.1 dB/m) is achieved using a wafer-bonded upper cladding structure on top of the $Si_3N_4$ waveguide to increase the modal overlap with high quality thermally grown $SiO_2$ layers. However, at this time, it is not certain that heaters can be integrated with the wafer-bonding approach. In this work, heaters are integrated on the PECVD oxide upper cladding. By using the PECVD top cladding (same as in this work) and by changing the waveguide geometry (50 nm $\times$ 6.5 $\mu$m) 0.5 dB/m propagation loss is achieved in [28] in the 1560 nm to 1600 nm wavelength region. Therefore, if 0.5 dB/m propagation loss is achieved by changing the waveguide cross-section and increasing the minimum bending radius (9.8 mm), then the loss difference between $ch-1$ and $ch-3$ of the proposed PWSM device will be 4.8 dB. This loss difference can be compensated by commercial SOA between the two complementary

PWSM devices. The low trending propagation loss (3.1 dB/m to 0.5 dB/m or 0.1 dB/m) in $Si_3N_4$ waveguides paves the way to increase the number of channels in the PWSM device from four to eight.

### 7.1.2 Wire-bonded optical and electrical front-ends of the time sampling photoreceiver

In the time sampling based optical front-end receiver demonstrated in this thesis, the four photodetected signals were processed offline using MATLAB. The theoretical model of the electronic front-end needs to be implemented using 130 nm or 65 nm CMOS technology nodes for the complete demonstration of the photoreceiver. Monolithic integration of the optical and electronic front-end is not feasible (or required), as silicon photonics devices can be fabricated using relatively affordable CMOS fabrication process. For example, the minimum feature size used in the optical front-end designed in this work is 340 nm, which is the width of the gratings in the grating couplers. On the other hand, to scale the bandwidth of the analog electrical front-end and specially the digital blocks of the electronic circuit, it is necessary to design the electronic front-end using the advanced low trending feature size (*i.e.*, 45 nm, or 65 nm) CMOS technology platform. The electronic front-end of the photoreceiver consists of four RC analog circuits and four five-level or 3-bit resolution ADCs. High data rate ADC, with the operating data rate 5 GS/s has been demonstrated in [119] using the 65 nm standard CMOS process. The 5 GS/sec and 5-bit resolution ADC demonstrated in [119] exhibits a power consumption of 110 mW. The ADCs for this work require 3-bit resolution, as the averaged signal or symbols generated from the photodetector and the analog electrical front-end have five voltage levels. The digital post-processing circuit will require four 3 bit XOR gates to perform the modulo-2 operation. Fig. 7.2 shows a model of the proposed photoreceiver, where the optical front-end is wire-bonded to the

electrical front-end. One important problem is to provide the high reversed bias voltage (2 to 4 V) to the PD, which is generally challenging to provide directly from a low threshold voltage CMOS IC. However, the DC bias voltage can be provided from the printed circuit board (PCB) onto which the PD is wire bonded to the CMOS IC.

## 7.2 Summary

In this chapter, we presented how the performance of the proposed PWSM device can be improved by using a lattice filter based optical demultiplexer. New simulation and analysis are required to design the directional couplers on the $Si_3N_4$ platform to generate the arbitrary power splitting ratios in the MZI filter blocks. We have also proposed that by changing the $Si_3N_4$ waveguide cross-section geometry and by increasing the minimum bending radius, it is possible to further reduce the propagation loss of the waveguide and hence reducing the loss difference between the wavelength channels. At the end of this chapter we have shown that, by utilizing the present state-of-art CMOS technology, the electrical front-end of the time sampling based photoreceiver can be experimentally demonstrated.

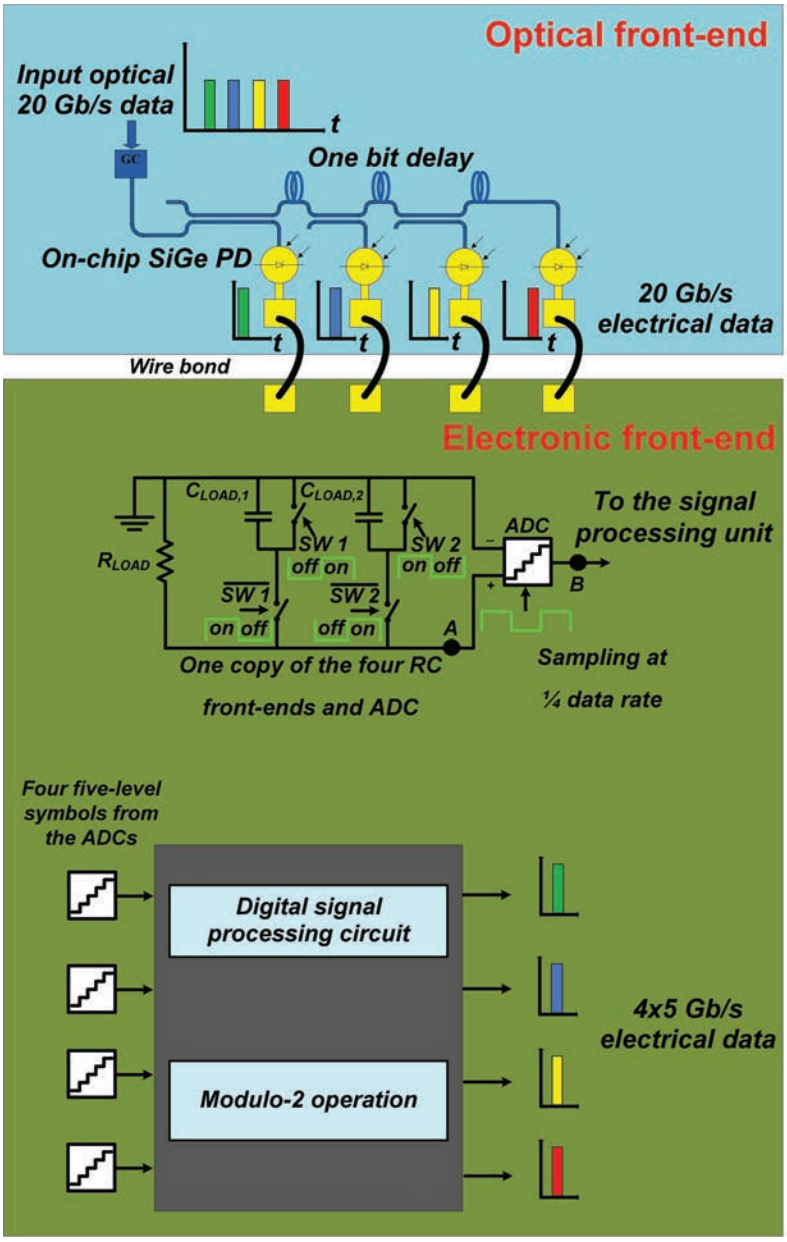



**Fig. 7.2** A schematic model of the overall photoreceiver architecture with the wire-bonded optical and electrical front-end.

# Chapter 8

# Conclusions

In this thesis, a $1 \times 4$ channel PWSM device is proposed for short-reach optical interconnect networks. The PWSM device functions as a serial-to-WDM interface to optically convert the serial stream of a data packet to parallel stream, *i.e.*, where different segments of the data packet are encoded to the four WDM channels in the same time slot. The PWSM PIC can be an important building block of the wavelength–striped based intra-card and inter-card schedulers in the TOR switches.

In addition to the PWSM device on $Si_3N_4$ waveguide platform, we have also designed and characterized an optical deserialiser time sampling based photoreceiver using SiGe photodetectors. The data rate of the optical receivers can be extended at a lower cost and with less complexity by using the time sampling based optical front-end presented in this thesis.

In chapter 1, we have introduced recent progress in the PIC based short-reach optical communication links. InP based PICs have shown an advanced roadmap of progressive improvement from the year 1990 to the present years. To further improve the performance of the PIC based short-reach optical links, other waveguide platforms such as silicon photonics

and $Si_3N_4$ waveguides are also being investigated. To meet the specification of the modern communication links, a complex integration of the active and passive photonic components are required both on chip and on the packaging level. Therefore, a PIC platform where InP-silicon photonics or silicon photonics-$Si_3N_4$ waveguide based components are integrated is becoming more common. We have also reviewed other works where the wavelength-striped mapping method is implemented using fiber based components. Recent works on the SiGe photodetectors augmenting the performance of the overall photoreceiver by leveraging the benefit offered by silicon photonics technology is also discussed in this chapter.

In chapter 2, we have described the theory of the optical wavelength-striped mapping method and the time sampling method in the photoreceivers. Motivation to design the PWSM device using the $Si_3N_4$ based waveguide platform is also discussed in this chapter.

In chapter 3, we have presented detailed design and characterization result of the thermally tunable $1 \times 4$ channel optical wavelength demultiplexer. The 4 channel demultiplexer is an important building block of the full PWSM device. The difference between the AWG based and MZI filter based optical demultiplexers is also discussed. It is found that MZI filter based optical demultiplexers are preferable than the AWG filters to design the PWSM device. FDTD simulation result is used to estimate the effective index ($n_{eff}$) and group index ($n_g$) of the 72 nm $\times$ 2.8 $\mu$m cross-section $Si_3N_4$ waveguide. At near 1550 nm wavelength region, the simulation value of the effective index and group index of the waveguide are equal to 1.4572 and 1.505, respectively. The experimentally measured group index value is closely matched with the simulation value. The $2 \times 2$ MMI couplers, demonstrated in this chapter, maintain 3 dB splitting ratio within the 0.3 dB power variation range. Two $2 \times 2$ MMI couplers were used to build each of the MZI filter block. The optical insertion loss of the demultiplexer varies from 1.5 dB to 2.2 dB per wavelength channel. 12 mm long Cr-based heaters placed on the delay arms of the MZI filters generate up to $\pi/2$ phase shift

at the dissipation of 150 mW electrical power. The optical crosstalk between the adjacent wavelength channels was ∼14.5 dB. We have measured BER of $1 \times 10^{-12}$, for all the four 40 Gb/sec channels at 10 Gb/sec data rate.

In chapter 4, design and characterization result of the PWSM device is proposed. The PWSM device is demonstrated as a WDM-to-serial interface, where, 16 ns long four data packets are serially combined in time domain to construct a 64 ns long data packet. The PWSM device implements 16 ns time delay between the adjacent wavelength channels using the 3.18 m long incremental delay lines. Due to the 9.5662 m delay waveguide length difference between $ch-1$ and $ch-4$, a 28.7 dB loss difference between the two channels is observed. For the practical implementation of the full PWSM process, where two complementary PWSM devices are placed back-to-back, such that uniform optical insertion loss is occurred in all four channels, it is important to further reduce the propagation loss of the $Si_3N_4$ waveguide from 3.1 dB/m to 0.5 dB/m or 0.1 dB/m. We have measured 2.3 dB power penalty between the 64 ns long data packets generated by the PWSM method and the back-to-back process, to obtain $1 \times 10^{-9}$ BER.

An integrated optical deserialiser time sampling based SiGe photoreceiver designed using silicon photonics waveguide technology is presented in chapter 5. The photoreceiver has a $1 \times 4$ time sampling SiGe PD array in the series architecture. Detailed methodology to obtain uniform optical power across all of the four PD channels compensating the delay waveguide loss is demonstrated. We found that, the low-loss 220 nm $\times$ 3 $\mu$m cross-section area silicon waveguide has much lower propagation loss compared to the conventional 220 nm $\times$ 500 nm cross-section area silicon waveguide, and thus the former waveguide relaxes the condition of achieving accurate power division ratios in the directional couplers of the time sampling based SiGe photoreceiver. FDTD simulation was performed to calculate the group index of both types of waveguides. The biasing capacitor

integrated PD leads toward simpler test setup and will facilitate low-cost integration with the electronic front-end in the future. A theoretical model of the analog *RC* front-end having ∼80 MHz bandwidth is proposed. The model of the electronic front-end having ∼80 MHz RC bandwidth and a 5 Gb/s post-processing digital circuit is used to process the 20 Gb/s photodetected signal in offline.

In chapter 6, we have included results from two other projects pursued in parallel with this Ph.D. research. We have presented performance result of the balanced photodetector and the PAM-4 ring modulator, designed on the silicon photonics platform.

In chapter 7 we have proposed two methods to increase the scalability of the four channel PWSM device by using the lattice MZI filter based optical demultiplexer and by further decreasing the propagation loss of the $Si_3N_4$ waveguide. In this chapter, we have also proposed that, the electronic front-end model of the photoreceiver presented in the work, should be fabricated using 65 nm or 130 nm CMOS technology and then wire-bonded to the optical front-end for the complete demonstration of the sampling photoreceiver prototype.

# References

[1] J.-X. Cai, Y. Cai, C. Davidson, D. Foursa, A. Lucero, O. Sinkin, W. Patterson, A. Pilipetskii, G. Mohs, and N. S. Bergano, "Transmission of 96 × 100-Gb/s Bandwidth-Constrained PDM-RZ-QPSK Channels With 300% Spectral Efficiency Over 10610 km and 400% Spectral Efficiency Over 4370 km," *Journal of Lightwave Technology*, vol. 29, no. 4, pp. 491–498, Feb. 2011.

[2] C. F. Lam, H. Liu, and R. Urata, "What Devices do Data Centers Need?," in *Proc. Optical Fiber Communication Conference (OFC)*, p. M2K.5, Mar. 2014.

[3] N. Farrington, G. Porter, S. Radhakrishnan, H. H. Bazzaz, V. Subramanya, Y. Fainman, G. Papen, and A. Vahdat, "Helios: a Hybrid Electrical/optical Switch Architecture for Modular Data Centers," *Proc. Comput. Commun. Rev.*, vol. 40, no. 4, pp. 339–350, Aug. 2010.

[4] D. Miller, "Device Requirements for Optical Interconnects to Silicon Chips," *Proceedings of the IEEE*, vol. 97, no. 7, pp. 1166–1185, July 2009.

[5] A. Benner, "Cost-Effective Optics: Enabling the Exascale Roadmap," in *Proc. 17$^{th}$ IEEE Symposium on High Performance Interconnects*, pp. 133–137, Aug 2009.

[6] D. Miller, "Rationale and Challenges for Optical Interconnects to Electronic Chips," *Proceedings of the IEEE*, vol. 88, no. 6, pp. 728–749, June 2000.

[7] K. Chen, A. Singla, A. Singh, K. Ramachandran, L. Xu, Y. Zhang, X. Wen, and Y. Chen, "OSA: An Optical Switching Architecture for Data Center Networks with Unprecedented Flexibility," *IEEE/ACM Transactions on Networking*, vol. 22, no. 2, pp. 498–511, Apr. 2014.

[8] J. Summers, T. Vallaitis, P. Evans, M. Ziari, P. Studenkov, M. Fisher, J. Sena, A. James, S. Corzine, D. Pavinski, J. Ou Yang, M. Missey, D. Gold, D. Lambert, W. Williams, M. Lai, F. Kish, and D. Welch, "40 Channels × 57 Gb/s Monolithically Integrated InP-based Coherent Photonic Transmitter," in *Proc. European Conference on Optical Communication (ECOC)*, p. P.2.5, Sept. 2014.

[9] M. Smit and K. Williams, "Progress in InP-based Photonic Integration," in *Proc. Frontiers in Optics*, p. FW5B.4, Oct. 2015.

[10] S. Chen, W. Li, J. Wu, Q. Jiang, M. Tang, S. Shutts, S. N. Elliott, A. Sobiesierski, A. J. Seeds, I. Ross, P. M. Smowton, and H. Liu, "Electrically Pumped Continuous-wave III-V Quantum Dot Lasers on Silicon," *Nature Photonics*, vol. 10, no. 5, pp. 307–311, Mar. 2016.

[11] C. R. Doerr, "Silicon Photonic Integration in Telecommunications," *Frontiers in Physics*, vol. 3, no. 37, Aug. 2015.

[12] *http://www.cisco.com/c/dam/assets/sol/sp/gci/global-cloud-index-infographic.html,"Cisco Global Cloud Index Forecast (2014-2019)"*.

[13] H. Nasu, "Short-Reach Optical Interconnects Employing High-Density Parallel-Optical Modules," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 16, no. 5, pp. 1337–1346, April 2010.

[14] K. Kurata, "A Review of Optical Interconnect (on Board or others) Development in Japan," in *Proc. 21$^{st}$ Annual Meeting of the IEEE Lasers and Electro-Optics Society (LEOS)*, pp. 517–518, p. WM2, Nov. 2008.

[15] J. Sakai, A. Noda, M. Yamagishi, T. Ohtsuka, K. Sunaga, H. Sugita, H. Takahashi, M. Oda, H. Ono, K. Yashiki, and H. Kouta, "20 Gbps/ch Optical Interconnection Between SERDES Devices over Distances from Chip-to-chip to Rack-to-rack," in *Proc. 34$^{th}$ European Conference on Optical Communication (ECOC)*, pp. 119–120, p. We.2.D.5, Sept. 2008.

[16] B. E. Lemoff, M. E. Ali, G. Panotopoulos, E. d. Groot, G. M. Flower, G. H. Rankin, A. J. Schmit, K. D. Djordjev, M. R. T. Tan, A. Tandon, W. Gong, R. P. Tella, B. Law, and D. W. Dolfi, "500-Gbps Parallel-WDM Optical Interconnect," in *Proc. 55$^{th}$ Electronic Components and Technology Conference*, pp. 1027–1031, May 2005.

[17] B. E. Lemoff, M. E. Ali, G. Panotopoulos, E. d. Groot, G. M. Flower, G. H. Rankin, A. J. Schmit, K. D. Djordjev, M. R. T. Tan, A. Tandon, W. Gong, R. P. Tella, B. Law, and D. W. Dolfi, "Parallel-WDM for Multi-Tb/s Optical Interconnects," in *Proc. 18$^{th}$ Annual Meeting of the IEEE Lasers and Electro-Optics Society(LEOS)*, pp. 359–360, p. TuW1, Oct. 2005.

[18] C. Doerr, L. Chen, D. Vermeulen, T. Nielsen, S. Azemati, S. Stulz, G. McBrien, X. M. Xu, B. Mikkelsen, M. Givehchi, C. Rasmussen, and S. Y. Park, "Single-chip Silicon Photonics 100-Gb/s Coherent Transceiver," in *Proc. Optical Fiber Communications Conference and Exhibition (OFC)*, pp. 1–3, p. Th5C.1, Mar. 2014.

[19] P. D. Dobbelaere, G. Armijo, J. Balardeta, S. Barabas, B. Chase, Y. Chi, A. Dahl, Y. D. Koninck, S. Denton, M. Eker, S. Fathpour, D. Foltz, F. Gholami, S. Gloeckner, K. Y. Hon, S. Hovey, S. Jackson, W. Li, Y. Liang, M. Mack, G. Masini, G. McGee, A. Mekis, S. Pang, M. Peterson, T. Pinguet, L. Planchon, K. Roberson, S. Sahni, J. Schramm, M. Sharp, C. Sohn, K. Stechschulte, P. Sun, G. Vastola, S. Wang, G. Wong, Xu, K. Yokoyama, S. Yu, and R. Zhou, "Silicon Photonics Transceivers for High Speed Optical Interconnect," in *Proc. Opto-Electronics and Communications Conference (OECC)*, pp. 1–3, Jul. 2015.

[20] K. Lawniczuk, C. Kazmierski, J. G. Provost, M. J. Wale, R. Piramidowicz, P. Szczepanski, M. K. Smit, and X. J. M. Leijtens, "InP-Based Photonic Multiwavelength Transmitter with DBR Laser Array," *IEEE Photonics Technology Letters*, vol. 25, no. 4, pp. 352–354, Feb. 2013.

[21] F. M. Soares, K. Janiak, J. Kreissl, M. Moehrle, and N. Grote, "Semi-insulating Substrate Based Generic InP Photonic Integration Platform," in *Proc. SPIE*, vol. 8767, May 22, 2013.

[22] Y. A. Vlasov and S. J. McNab, "Losses in Single-mode Silicon-on-insulator Strip Waveguides and Bends," *Optics Express*, vol. 12, no. 8, pp. 1622–1631, Apr. 2004.

[23] G. Li, J. Yao, H. Thacker, A. Mekis, X. Zheng, I. Shubin, Y. Luo, J.-H. Lee, K. Raj, J. E. Cunningham, and A. Krishnamoorthy, "Ultra Low-loss, High-density SOI Optical Waveguide Routing for Macrochip Interconnects," *Optics Express*, vol. 20, no. 11, pp. 12035–12039, May 2012.

[24] L. Stampoulidis, K. Vyrsokinos, K. Voigt, L. Zimmermann, F. Gomez-Agis, H. Dorren, Z. Sheng, D. Van Thourhout, L. Moerl, J. Kreissl, B. Sedighi, J. C. Scheytt, A. Pagano, and E. Riccardi, "The European BOOM Project: Silicon Photonics for High-Capacity Optical Packet Routers," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 16, no. 5, pp. 1422–1433, Sept. 2010.

[25] J. LeGrange, J. Simsarian, P. Bernasconi, D. Neilson, L. Buhl, and J. Gripp, "Demonstration of an Integrated Buffer for an All-optical Packet Router," in *Proc. Conference on Optical Fiber Communication*, pp. 1–3, p. OMU5, Mar. 2009.

[26] J. Mack, E. Burmeister, J. Garcia, H. Poulsen, B. Stamenic, G. Kurczveil, K. Nguyen, K. Hollar, J. Bowers, and D. Blumenthal, "Synchronous Optical Packet Buffers," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 16, no. 5, pp. 1413–1421, Sept. 2010.

[27] J. F. Bauters, M. J. Heck, D. John, D. Dai, M.-C. Tien, J. S. Barton, A. Leinse, R. G. Heideman, D. J. Blumenthal, and J. E. Bowers, "Ultra–low–loss High–aspect–ratio $Si_3N_4$ Waveguides," *Optics Express*, vol. 19, no. 4, pp. 3163–3174, Feb. 2011.

[28] J. F. Bauters, M. J. Heck, D. D. John, J. S. Barton, C. M. Bruinink, A. Leinse, R. G. Heideman, D. J. Blumenthal, and J. E. Bowers, "Planar Waveguides with Less than 0.1 dB/m Propagation Loss Fabricated with Wafer Bonding," *Optics Express*, vol. 19, no. 24, pp. 24090–24101, Nov. 2011.

[29] M. Streshinsky, A. Novack, R. Ding, Y. Liu, A. E. J. Lim, P. G. Q. Lo, T. Baehr-Jones, and M. Hochberg, "Silicon Parallel Single Mode 48 × 50 Gb/s Modulator and Photodetector Array," *Journal of Lightwave Technology*, vol. 32, no. 22, pp. 4370–4377, Nov. 2014.

[30] D. Dai, J. Bauters, and J. E. Bowers, "Passive Technologies for Future Large-scale Photonic Integrated Circuits on Silicon: Polarization Handling, Light Non-reciprocity and Loss Reduction," *Light: Science & Applications*, vol. 1, no. e1, pp. 1–12, Mar. 2012.

[31] J. F. Bauters, M. L. Davenport, M. J. R. Heck, J. K. Doylend, A. Chen, A. W. Fang, and J. E. Bowers, "Silicon on Ultra-low-loss Waveguide Photonic Integration Platform," *Optics Express*, vol. 21, no. 1, pp. 544–555, Jan. 2013.

[32] T. Baehr-Jones, R. Ding, Y. Liu, A. Ayazi, T. Pinguet, N. C. Harris, M. Streshinsky, P. Lee, Y. Zhang, A. E.-J. Lim, T.-Y. Liow, S. H.-G. Teo, G.-Q. Lo, and M. Hochberg, "Ultralow Drive Voltage Silicon Traveling-wave Modulator," *Optics Express*, vol. 20, no. 11, pp. 12014–12020, May 2012.

[33] M. Streshinsky, R. Ding, Y. Liu, A. Novack, Y. Yang, Y. Ma, X. Tu, E. K. S. Chee, A. E.-J. Lim, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "Low Power 50 Gb/s Silicon Traveling Wave Mach-Zehnder Modulator Near 1300 nm," *Optics Express*, vol. 21, no. 25, pp. 30350–30357, Dec. 2013.

[34] X. Wu, B. Dama, P. Gothoskar, P. Metz, K. Shastri, S. Sunder, J. Van der Spiegel, Y. Wang, M. Webster, and W. Wilson, "A 20Gb/s NRZ/PAM-4 1V Transmitter in 40nm CMOS Driving a Si-photonic Modulator in 0.13$\mu$m CMOS," in *Proc. IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 128–129, p. 7.7, Feb. 2013.

[35] P. Dong, X. Liu, S. Chandrasekhar, L. L. Buhl, R. Aroca, and Y. K. Chen, "Monolithic Silicon Photonic Integrated Circuits for Compact $100^{+}$Gb/s Coherent Optical Receivers and Transmitters," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, no. 4, pp. 150–157, Jul-Aug. 2014.

[36] S. Gundavarapu, T. Huffman, M. Belt, R. Moreira, J. Bowers, and D. Blumenthal, "Integrated Ultra-Low-Loss Silicon Nitride Waveguide Coil for Optical Gyroscopes," in *Proc. Optical Fiber Communication Conference*, p. W4E.5, Mar. 2016.

[37] D. Dai, Z. Wang, J. F. Bauters, M. C. Tien, M. J. R. Heck, D. J. Blumenthal, and J. E. Bowers, "Low-loss $Si_3N_4$ Arrayed-waveguide Grating (De)multiplexer Using Nano-core Optical Waveguides," *Optics Express*, vol. 19, no. 15, pp. 14130–14136, Jul. 2011.

[38] X. Luo, J. Song, X. Tu, Q. Fang, L. Jia, Y. Huang, T.-Y. Liow, M. Yu, and G.-Q. Lo, "Silicon-based Traveling-wave Photodetector Array (Si-TWPDA) with Parallel Optical Feeding," *Optics Express*, vol. 22, no. 17, pp. 20020–20026, Aug. 2014.

[39] B. Abiri, A. Zhou, F. Aflatouni, and A. Hajimiri, "An Adjustable Self-Equalizing Photo Detector," in *Optical Fiber Communication Conference*, p. W3A.3, Mar. 2015.

[40] N. Kikuchi and R. Hirai, "Intensity-modulated/direct-detection (IM/DD) Nyquist Pulse-amplitude Modulation (PAM) Signaling for 100-Gbit/s/$\lambda$ Optical Short-reach Transmission," in *Proc. European Conference on Optical Communication (ECOC)*, p. P.4.12, Sept. 2014.

[41] A. Konczykowska, J. y. Dupuy, F. Jorge, M. Riet, J. Moulu, V. Nodjiadjim, P. Berdaguer, and J. Godin, "42 GBd 3-Bit Power-DAC for Optical Communications with Advanced Modulation Formats in InP DHBT," *Electronics Letters*, vol. 47, no. 6, pp. 389–390, Mar. 2011.

[42] A. Shastri, C. Muzio, M. Webster, G. Jeans, P. Metz, S. Sunder, B. Chattin, B. Dama, and K. Shastri, "Ultra-Low-Power Single-Polarization QAM-16 Generation Without DAC Using a CMOS Photonics Based Segmented Modulator," *Journal of Lightwave Technology*, vol. 33, no. 6, pp. 1255–1260, Mar. 2015.

[43] A. Beling, J. C. Campbell, H. G. Bach, G. G. Mekonnen, and D. Schmidt, "Parallel-Fed Traveling Wave Photodetector for $>$ 100 GHz Applications," *Journal of Lightwave Technology*, vol. 26, no. 1, pp. 16–20, Jan. 2008.

[44] J. F. Bauters, M. J. Heck, D. John, M.-C. Tien, A. Leinse, R. G. Heideman, D. J. Blumenthal, and J. E. Bowers, "Ultra-low Loss Silica-based Waveguides with Millimeter Bend Radius," in *Proc. European Conference and Exhibition on Optical Communication*, p. We.8.E.6, Sept. 2010.

[45] M. Piels, J. F. Bauters, M. L. Davenport, M. J. R. Heck, and J. E. Bowers, "Low-Loss Silicon Nitride AWG Demultiplexer Heterogeneously Integrated with Hybrid IIIV/Silicon Photodetectors," *Journal of Lightwave Technology*, vol. 32, no. 4, pp. 817–823, Feb. 2014.

[46] O. Liboiron-Ladouceur, P. G. Raponi, N. Andriolli, I. Cerutti, M. S. Hai, and P. Castoldi, "A Scalable Space–Time Multi-plane Optical Interconnection Network Using

Energy-Efficient Enabling Technologies [Invited]," *Journal of Optical Communications and Networking*, vol. 3, no. 8, pp. A1–A11, Aug. 2011.

[47] M. Al-Fares, S. Radhakrishnan, B. Raghavan, N. Huang, and A. Vahdat, "Hedera: Dynamic Flow Scheduling for Data Center Networks," in *Proc. Networked Systems Design and Implementation (NSDI) Symposium*, 2010.

[48] V. Soteriou and L.-S. Peh, "Exploring the Design Space of Self-regulating Power-aware On/Off Interconnection Networks," *IEEE Transactions on Parallel and Distributed Systems*, vol. 18, no. 3, pp. 393–408, Mar. 2007.

[49] J. Lee, P.-C. Chiang, P.-J. Peng, L.-Y. Chen, and C.-C. Weng, "Design of 56 Gb/s NRZ and PAM4 SerDes Transceivers in CMOS Technologies," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 9, pp. 2061–2073, Sept. 2015.

[50] C. Menolfi, T. Toifl, R. Reutemann, M. Ruegg, P. Buchmann, M. Kossel, T. Morf, and M. Schmatz, "A 25Gb/s PAM4 Transmitter in 90 nm CMOS SOI," in *Proc. IEEE Solid-State Circuits Conference (ISSCC)*, pp. 72–73, p. 3.7, Feb. 2005.

[51] T. Toifl, C. Menolfi, M. Ruegg, R. Reutemann, P. Buchmann, M. Kossel, T. Morf, J. Weiss, and M. L. Schmatz, "A 22-Gb/s PAM-4 Receiver in 90-nm CMOS SOI Technology," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 4, pp. 954–965, Apr. 2006.

[52] H. Kimura, P. M. Aziz, T. Jing, A. Sinha, S. P. Kotagiri, R. Narayan, H. Gao, P. Jing, G. Hom, and A. Liang, "A 28 Gb/s 560 mW Multi-standard SerDes with Single-stage Analog Front-end and 14-tap Decision Feedback Equalizer in 28 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3091–3103, Dec. 2014.

[53] L. A. Buckman, B. E. Lemoff, A. J. Schmit, R. P. Tella, and W. Gong, "Demonstration of a Small-form-factor WWDM Transceiver Module for 10-Gb/s Local Area Networks," *IEEE Photonics Technology Letters*, vol. 14, no. 5, pp. 702–704, May 2002.

[54] Z. Deyu, B. C. Wang, R. J. Runser, I. Glesk, and P. R. Prucnal, "Perfectly Synchronized Bit-parallel WDM Data Transmission over a Single Optical Fiber," *IEEE Photonics Technology Letters*, vol. 13, no. 4, pp. 382–384, Apr. 2001.

[55] F. Dorgeuille, L. Noirie, J. P. Faure, A. Ambrosy, S. Rabaron, F. Boubal, M. Schilling, and C. Artigue, "1.28 Tbit/s Throughput 8 × 8 Optical Switch Based on Arrays of Gain-Clamped Semiconductor Optical Amplifier Gates," in *Proc. Optical Fiber Communication Conference*, p. PD18, Mar. 2000.

[56] B. E. Lemoff, M. E. Ali, G. Panotopoulos, E. d. Groot, G. M. Flower, G. H. Rankin, A. J. Schmit, K. D. Djordjev, M. R. T. Tan, A. Tandon, W. Gong, R. P. Tella, B. Law, L. K. Chia, and D. W. Dolfi, "Demonstration of a Compact Low-power 250-Gb/s Parallel-WDM Optical Interconnect," *IEEE Photonics Technology Letters*, vol. 17, no. 1, pp. 220–222, Jan. 2005.

[57] C. Woosuk, H. Sub, L. Jaehoon, K. Yonggyoo, and J. Jichai, "Transmission Performance Analysis of 8 × 10 Gb/s WDM Signals Using Cascaded SOAs Due to Signal Wavelength Displacement," *Journal of Lightwave Technology*, vol. 20, no. 8, pp. 1350–1356, Aug. 2002.

[58] A. Shacham, B. A. Small, O. Liboiron-Ladouceur, and K. Bergman, "A Fully Implemented 12 × 12 Data Vortex Optical Packet Switching Interconnection Network," *Journal of Lightwave Technology*, vol. 23, no. 10, pp. 3066–3075, Oct. 2005.

[59] T. Lin, K. A. Williams, R. V. Penty, I. H. White, and M. Glick, "Capacity Scaling in a Multihost Wavelength-Striped SOA-based Switch Fabric," *Journal of lightwave technology*, vol. 25, no. 3, pp. 655–663, Mar. 2007.

[60] C. P. Lai and K. Bergman, "Broadband Multicasting for Wavelength-striped Optical Packets," *Journal of Lightwave Technology*, vol. 30, no. 11, pp. 1706–1718, June 2012.

[61] O. Liboiron-Ladouceur, H. Wang, A. S. Garg, and K. Bergman, "Low-power, Transparent Optical Network Interface for High Bandwidth Off-chip Interconnects," *Optics Express*, vol. 17, no. 8, pp. 6550–6561, Apr. 2009.

[62] T. Yin, R. Cohen, M. M. Morse, G. Sarid, Y. Chetrit, D. Rubin, and M. J. Paniccia, "31 GHz Ge n-i-p Waveguide Photodetectors on Silicon-on-Insulator Substrate," *Optics Express*, vol. 15, no. 21, pp. 13965–13971, Oct. 2007.

[63] H. Pan, S. Assefa, W. M. J. Green, D. M. Kuchta, C. L. Schow, A. V. Rylyakov, B. G. Lee, C. W. Baks, S. M. Shank, and Y. A. Vlasov, "High-speed Receiver Based on Waveguide Germanium Photodetector Wire-bonded to 90 nm SOI CMOS Amplifier," *Optics Express*, vol. 20, no. 16, pp. 18145–18155, Jul. 2012.

[64] S. Assefa, H. Pan, S. Shank, W. Green, A. Rylyakov, C. Schow, M. Khater, S. Kamlapurkar, E. Kiewra, T. Topuria, P. Rice, C. W. Baks, and Y. Vlasov, "Monolithically Integrated Silicon Nanophotonics Receiver in 90 nm CMOS Technology Node," in *Proc. Optical Fiber Communication Conference*, p. OM2H.4, Mar. 2013.

[65] A. Novack, M. Gould, Y. Yang, Z. Xuan, M. Streshinsky, Y. Liu, G. Capellini, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "Germanium Photodetector with 60 GHz Bandwidth using Inductive Gain Peaking," *Optics Express*, vol. 21, no. 23, pp. 28387–28393, Nov. 2013.

[66] M. H. Nazari and A. Emami-Neyestanak, "A 24-Gb/s Double-sampling Receiver for Ultra-low-power Optical Communication," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 344–357, Feb. 2013.

[67] M. L. Loeb and G. R. Stilwell, "High-speed Data Transmission on an Optical Fiber Using a Byte-wide WDM System," *Journal of Lightwave Technology*, vol. 6, no. 8, pp. 1306–1311, Aug. 1988.

[68] M. Glick, M. Dales, D. McAuley, T. Lin, K. Williams, R. Penty, and I. White, "SWIFT: A Testbed with Optically Switched Data Paths for Computing Applications," in *Proc. of 7$^{th}$ International Conference on Transparent Optical Networks.*, vol. 2, pp. 29–32, p. We.B1.2, Jul. 2005.

[69] *https://www.shf.de/wp-content/uploads/datasheets/*datasheet_shf_803p.pdf*, "Datasheet: SHF 803P Broadband Amplifier".*

[70] J. Kim and J. F. Buckwalter, "A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 615–626, Mar. 2012.

[71] S. Saeedi and A. Emami, "A 25Gb/s 170$\mu$W/Gb/s Optical Receiver in 28nm CMOS for Chip-to-chip Optical Communication," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium*, pp. 283–286, June 2014.

[72] A. Emami-Neyestanak, D. Liu, G. Keeler, N. Helman, and M. Horowitz, "A 1.6 Gb/s, 3 mW CMOS Receiver for Optical Communication," in *Proc. Symposium on VLSI Circuits Digest of Technical Papers*, pp. 84–87, June 2002.

[73] L. Chrostowski and M. Hochberg, *Silicon Photonics Design: From Devices to Systems*. Cambridge University, 2015.

[74] E. F. Burmeister, J. P. Mack, H. N. Poulsen, M. L. Mašanovic, B. Stamenic, D. J. Blumenthal, and J. E. Bowers, "Photonic Integrated Circuit Optical Buffer for Packet–switched Networks," *Optics Express*, vol. 17, no. 8, pp. 6629–6635, Apr. 2009.

[75] J. D. LeGrange, J. E. Simsarian, P. Bernasconi, D. T. Neilson, L. L. Buhl, and J. Gripp, "Demonstration of an Integrated Buffer for an All–optical Packet Router," in *Proc. Optical Fiber Communication Conference*, p. OMU5, Mar. 2009.

[76] L. Chen, P. Dong, and M. Lipson, "High performance germanium photodetectors integrated on submicron silicon waveguides by low temperature wafer bonding," *Optics Express*, vol. 16, no. 15, pp. 11513–11518, Jul. 2008.

[77] T. Y. Liow, K. W. Ang, Q. Fang, J. F. Song, Y. Z. Xiong, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Silicon Modulators and Germanium Photodetectors on SOI: Monolithic Integration, Compatibility, and Performance Optimization," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 16, no. 1, pp. 307–315, Jan. 2010.

[78] M. Jinno, H. Takara, Y. Sone, K. Yonenaga, and A. Hirano, "Multiflow Optical Transponder for Efficient Multilayer Optical Networking," *IEEE Communications Magazine*, vol. 50, no. 5, pp. 56–65, May 2012.

[79] D. T. Spencer, J. F. Bauters, M. J. Heck, and J. E. Bowers, "Integrated Waveguide Coupled $Si_3N_4$ Resonators in the Ultrahigh–Q Regime," *Optica*, vol. 1, no. 3, pp. 153–157, Sept. 2014.

[80] P. Samadi, I. Kostko, A. Jain, B. Shia, C. L. Callender, P. Dumais, S. Jacob, and L. R. Chen, "Tunable Lattice-form Mach–Zehnder Interferometer for Arbitrary Binary Code Generation at 40 GHz," *Journal of Lightwave Technology*, vol. 28, no. 21, pp. 3070–3078, Nov. 2010.

[81] K. Wörhoff, R. G. Heideman, A. Leinse, and M. Hoekman, "TriPleX: a Versatile Dielectric Photonic Platform," *Advanced Optical Technologies*, vol. 4, no. 2, pp. 189–207, Mar. 2015.

[82] M. S. Hai, A. Leinse, T. Veenstra, and O. Liboiron-Ladouceur, "A Thermally Tunable 1×4 Channel Wavelength Demultiplexer Designed on a Low-Loss $Si_3N_4$ Waveguide Platform," *Photonics*, vol. 2, no. 4, pp. 1065–1080, Nov. 2015.

[83] D. Thomson, Y. Hu, G. Reed, and J.-M. Fedeli, "Low Loss MMI Couplers for High Performance MZI Modulators," *IEEE Photonics Technology Letters*, vol. 22, no. 20, pp. 1485–1487, Oct. 2010.

[84] C. K. Madsen and J. H. Zhao, *Optical Filter Design and Analysis*. Wiley-Interscience, 1999.

[85] B. H. Verbeek, C. H. Henry, N. A. Olsson, K. Orlowsky, R. Kazarinov, and B. Johnson, "Integrated Four-channel Mach–Zehnder Multi/demultiplexer Fabricated with Phosphorous Doped $SiO_2$ Waveguides on Si," *Journal of Lightwave Technology*, vol. 6, no. 6, pp. 1011–1015, June 1988.

[86] E. Dulkeith, F. Xia, L. Schares, W. M. J. Green, and Y. A. Vlasov, "Group Index and Group Velocity Dispersion in Silicon-on-insulator Photonic Wires," *Optics Express*, vol. 14, no. 9, pp. 3853–3863, Apr. 2006.

[87] I. Cerutti, P. G. Raponi, N. Andriolli, P. Castoldi, and O. Liboiron-Ladouceur, "Designing Energy–Efficient Data Center Networks Using Space–Time Optical Interconnection Architectures," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, no. 2, pp. 3700209–3700209, Mar. 2013.

[88] P. G. Raponi, N. Andriolli, I. Cerutti, and P. Castoldi, "Two–step Scheduling Framework for Space-wavelength Modular Optical Interconnection Networks," *IET Communications*, vol. 4, no. 18, pp. 2155–2165, Dec. 2010.

[89] M. S. Hai and O. Liboiron-Ladouceur, "Low-Loss Passive $Si_3N_4$ Serial-to-WDM Interface for Energy-Efficient Optical Interconnects," *Journal of Lightwave Technology*, vol. PP, no. 99, pp. 1–1, Oct. 2016.

[90] G. P. Agrawal, *Fiber-Optic Communication Systems*. Wiley–Interscience, 2002.

[91] Y. Li, M. Chen, H. Yu, H. Chen, S. Yang, and S. Xie, "Versatile Wideband Polarization-Insensitive Mode Converter Based on Wedge-Shaped Waveguide," *IEEE Photonics Journal*, vol. 8, no. 2, pp. 1–11, Apr. 2016.

[92] L. Zhuang, D. Marpaung, M. Burla, W. Beeker, A. Leinse, and C. Roeloffzen, "Low-loss, High-index-contrast $Si_3N_4/SiO_2$ Optical Waveguides for Optical Delay Lines in Microwave Photonics Signal Processing," *Optics Express*, vol. 19, no. 23, pp. 23162–23170, Nov. 2011.

[93] F. Horst, W. M. J. Green, S. Assefa, S. M. Shank, Y. A. Vlasov, and B. J. Offrein, "Cascaded Mach-Zehnder Wavelength Filters in Silicon Photonics for Low Loss and Flat Pass-band WDM (De-)Multiplexing," *Optics Express*, vol. 21, no. 10, pp. 11652–11658, May 2013.

[94] G. Maxwell, A. Poustie, C. Ford, M. Harlow, P. Townley, M. Nield, T. Lealman, S. Oliver, L. Rivers, and R. Waller, "Hybrid Integration of Monolithic Semiconductor Optical Amplifier Arrays Using Passive Assembly," in *Proc. $55^{th}$ Electronic Components and Technology Conf.*, vol. 2, pp. 1349–1352, May/June 2005.

[95] Lenovo, *RackSwitch G8264 and G8264T*, https://lenovopress.com/tips0815, 2015.

[96] Q. Xu and R. Soref, "Reconfigurable Optical Directed-logic Circuits Using Microresonator-based Optical Switches," *Optics Express*, vol. 19, no. 6, pp. 5244–5259, Mar. 2011.

[97] L. Yang, R. Ji, L. Zhang, J. Ding, and Q. Xu, "On-chip CMOS-compatible Optical Signal Processor," *Optics Express*, vol. 20, no. 12, pp. 13560–13565, June 2012.

[98] M. S. Hai, M. Ménard, and O. Liboiron-Ladouceur, "Integrated Optical Deserialiser Time Sampling based SiGe Photoreceiver," *Optics Express*, vol. 23, no. 25, pp. 31736–31754, Dec. 2015.

[99] C. R. Doerr, P. J. Winzer, Y. K. Chen, S. Chandrasekhar, M. S. Rasras, L. Chen, T. Y. Liow, K. W. Ang, and G. Q. Lo, "Monolithic Polarization and Phase Diversity Coherent Receiver in Silicon," *Journal of lightwave technology*, vol. 28, no. 4, pp. 520–525, Feb. 2010.

[100] M. S. Hai, M. N. Sakib, and O. Liboiron-Ladouceur, "A 16 GHz Silicon-based Monolithic Balanced Photodetector with on-chip Capacitors for 25 Gbaud Front-end Receivers," *Optics Express*, vol. 21, no. 26, pp. 32680–32689, Dec. 2013.

[101] M. H. Nazari and A. Emami, "A 15Gb/s 0.5 mW/Gb/s 2-Tap DFE Receiver with Far-end Crosstalk Cancellation," in *Proc. IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 446–448, p. 25.6, Feb. 2011.

[102] G. E. Cowan and C. Williams, "Phase-locked Loop Architecture for Enhanced Voltage-controlled Oscillator Phase-noise Suppression," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2476–2479, May 2013.

[103] S. Walklin and J. Conradi, "Multilevel Signaling for Increasing the Reach of 10 Gb/s Lightwave Systems," *Journal of lightwave technology*, vol. 17, no. 11, p. 2235, Nov. 1999.

[104] J. V. Olmos, L. F. Suhr, B. Li, and I. T. Monroy, "Five-level Polybinary Signaling for 10 Gbps Data Transmission Systems," *Optics Express*, vol. 21, no. 17, pp. 20417–20422, Aug. 2013.

[105] M. S. Hai, M. Ménard, and O. Liboiron-Ladouceur, "A 20 Gb/s SiGe Photoreceiver Based on Optical Time Sampling," in *Proc. European Conference on Optical Communication (ECOC)*, p. Tu.1.3.5, Sept. 2015.

[106] I. Giuntoni, D. Stolarek, D. I. Kroushkov, J. Bruns, L. Zimmermann, B. Tillack, and K. Petermann, "Continuously Tunable Delay Line Based on SOI Tapered Bragg Gratings," *Optics Express*, vol. 20, no. 10, pp. 11241–11246, May 2012.

[107] S. Khan and S. Fathpour, "Complementary Apodized Grating Waveguides for Tunable Optical Delay Lines," *Optics Express*, vol. 20, no. 18, pp. 19859–19867, Aug. 2012.

[108] P. Orlandi, F. Morichetti, M. J. Strain, M. Sorel, A. Melloni, and P. Bassi, "Tunable Silicon Photonics Directional Coupler Driven by a Transverse Temperature Gradient," *Optics Letters*, vol. 38, no. 6, pp. 863–865, Mar. 2013.

[109] M. S. Hai, M. Moayedi, and O. Liboiron-Ladouceur, "A Ring-based 25 Gb/s DAC-less PAM-4 Modulator," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 22, no. 6, pp. 1–8, Nov.-Dec. 2016.

[110] J. K. Fischer, R. Ludwig, L. Molle, M. Noelle, A. Beling, C. C. Leonhardt, A. Matiss, A. Umbach, R. Kunkel, H.-G. Bach, and C. Schubert, "Integrated Coherent Receiver Modules for 100G Ethernet and Beyond," in *Proc. Photonic Networks (ITG Symposium)*, pp. 1–5, p. 5, May 2011.

[111] Y. Painchaud, M. Pelletier, M. Poulin, F. Pelletier, C. Latrasse, G. Robidoux, S. Savard, J. Gagné, V. Trudel, M. Picard, P. Poulin, P. Sirois, F. D'Amours, D. Asselin, S. Paquet, C. Paquet, M. Cyr, M. Guy, M. Morsy-Osman, Q. Zhuge, X. Xu, M. Chagnon, and D. Plant, "Ultra-compact Coherent Receiver Based on Hybrid Integration on Silicon," in *Proc. Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC)*, p. OM2J.2, Mar. 2013.

[112] C. Doerr, L. Buhl, Y. Baeyens, R. Aroca, S. Chandrasekhar, X. Liu, L. Chen, and Y. K. Chen, "Packaged Monolithic Silicon 112-Gb/s Coherent Receiver," *IEEE Photonics Technology Letters*, vol. 23, no. 12, pp. 762–764, June 2011.

[113] D. C. Dube, J. Baborowski, P. Muralt, and N. Setter, "The Effect of Bottom Electrode on the Performance of Thin Film Based Capacitors in the Gigahertz Region," *Applied Physics Letters*, vol. 74, no. 23, pp. 3546–3548, June 1999.

[114] K. Onohara, T. Sugihara, Y. Konishi, Y. Miyata, T. Inoue, S. Kametani, K. Sugihara, K. Kubo, H. Yoshida, and T. Mizuochi, "Soft-Decision-Based Forward Error Correction for 100 Gb/s Transport Systems," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 16, no. 5, pp. 1258–1267, Sept.-Oct. 2010.

[115] R. Dubé-Demers, C. S. Park, S. LaRochelle, and W. Shi, "60 Gb/s PAM-4 Operation with a Silicon Microring Modulator," in *Proc. 12$^{th}$ IEEE International Conference on Group IV Photonics (GFP)*, p. WP59, Aug. 2015.

[116] M. S. Hai, M. M. P. Fard, and O. Liboiron-Ladouceur, "A Low-voltage PAM-4 SOI Ring-based Modulator," in *Proc. IEEE Photonics Conference (IPC)*, p. TuB3.3, Oct. 2014.

[117] K. Jinguji and T. Yasui, "Synthesis of One-Input M-Output Optical FIR Lattice Circuits," *Journal of Lightwave Technology*, vol. 26, no. 7, pp. 853–866, Apr. 2008.

[118] S. Kamei, M. Oguma, M. Kohtoku, T. Shibata, and Y. Inoue, "Low-loss athermal silica-based lattice-form interleave filter with silicone-filled grooves," *IEEE Photonics Technology Letters*, vol. 17, no. 4, pp. 798–800, Apr. 2005.

[119] O. Tyshchenko, A. Sheikholeslami, H. Tamura, M. Kibune, H. Yamaguchi, and J. Ogawa, "A 5-Gb/s ADC-Based Feed-Forward CDR in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1091–1098, June 2010.