Burst-Mode Clock and Data Recovery Circuits for Optical Multiaccess Networks

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To Stéphanie

Abstract

Optical multiaccess networks, and more specifically passive optical networks (PONs), can provide high bandwidth to the end user by extending the fiber into the local access network (fiber-to-the-home, -building, -curb). In a PON, multiple users share the fiber infrastructure in a point-to-multipoint (P2MP) network topology. This creates new challenges for the design of receiver front-ends and clock and data recovery circuits (CDRs). Moreover, the challenges depend on the multiple access method that is used to share the bandwidth among users. This thesis presents novel burst-mode CDR circuits for PONs and multiaccess networks. The two access methods considered are optical code division multiple access (OCDMA) and time division multiple access (TDMA).

We designed the first standalone OCDMA receiver with multiple access interference rejection, CDR, and forward error correction (FEC). The receiver supports a bit rate and a chip rate of 155.52 and 1244.16 Mb/s, respectively. We performed BER measurements in a 2D λ-t OCDMA network using the recovered clock. By not using a global clock, we demonstrated an OCDMA network with the receiver completely isolated from the transmitters. We measured a negligible power penalty when using the recovered clock as opposed to the global clock. With FEC, we measured a coding gain of approximately 3 dB at a BER of 10^{-9}. We used the coding gain to more than double the number of supported users (5 compared to 2). These experiments, together with the demonstration of a standalone OCDMA receiver, give weight to the argument that OCDMA could provide an alternative to TDMA in PONs.

We also designed two burst-mode CDRs for TDMA PONs. The common goal for both CDRs was to achieve fast phase acquisition to minimize the physical layer overhead for phase recovery. The first design is a 1244.16 Mb/s broadband CDR. We reduced the settling time of the CDR by increasing its bandwidth. We confirmed experimentally the trade off between settling time and jitter. We solved this tradeoff by designing a 622/1244

Mb/s burst-mode clock phase aligner (BM-CPA) based on 2× over sampling. The BM-CPA provides instantaneous phase acquisition (0 bit), much improved jitter characteristics, and meets the specifications of GPON Recommendation G.984.2.

Finally, we designed a burst-mode test solution that allowed us to measure the phase acquisition time of CDRs down to an accuracy of one bit.

Résumé

Les réseaux optiques à accès multiple, et plus spécifiquement les réseaux optiques passifs (PONs – "passive optical networks"), peuvent fournir à l'utilisateur une large bande passante en prolongeant la fibre jusqu'au réseau local (fibre optique jusqu'au domicile, à l'immeuble, ou au trottoir). Dans un PON, plusieurs utilisateurs partagent la même infrastructure de fibre jusqu'à la centrale en utilisant une liaison point à multipoint. Cette topologie de réseau crée de nouveaux défis pour la conception de circuits électroniques recevant les signaux des utilisateurs. En particulier, des circuits pouvant rétablir rapidement les impulsions d'horloge et les données (circuits BM-CDR – "burst-mode clock and data recovery circuits") sont nécessaires. De plus, les défis dépendent de la méthode d'accès multiple qui est utilisée pour partager la bande passante entre les utilisateurs. Cette thèse présente de nouveaux circuits CDR pour les PONs et les réseaux à accès multiple en général. Les deux méthodes d'accès multiple considérées sont CDMA (accès multiple par répartition en code) et TDMA (accès multiple par répartition dans le temps).

Nous avons conçu le premier récepteur autonome pour le CDMA optique. Le récepteur peut filtrer l'interférence dû à l'accès multiple, recouvrer l'horloge et les données, et effectuer la correction d'erreurs sans voie de retour (FEC – "forward error correction"). Le récepteur supporte un débit binaire de 155.52 Mb/s et un débit de chips de 1244.16 Mb/s, respectivement. Nous avons effectué des mesures de taux d'erreurs sur les bits (BER – "bit error rate") en utilisant un système CDMA optique bidimensionnel basé sur la longueur d'onde et le temps (2D λ-t). Nous avons évité l'utilisation d'une horloge globale pour démontrer une isolation complète entre les transmetteurs et le récepteur du réseau. Nous avons mesuré une pénalité de puissance négligeable en utilisant l'horloge rétablie par notre récepteur plutôt qu'une horloge globale. Avec FEC, nous avons mesuré un gain de codage d'environ 3 dB à un BER de 10^{-9}. Nous avons utilisé ce

gain de codage pour plus que doubler le nombre d'utilisateur supportés par le réseau (5 comparativement à 2). Ces expériences, combinées avec la démonstration d'un récepteur autonome, supportent l'argument voulant que le CDMA optique puisse offrir une alternative au TDMA dans les PONs.

Nous avons également conçu deux circuits BM-CDR pour les PONs utilisant la méthode d'accès multiple TDMA. Le but commun pour les deux circuits était de fournir un recouvrement rapide de l'horloge et des données pour minimiser le nombre de bits réservés pour l'acquisition de la phase. Le premier circuit fonctionne à 1244.16 Mb/s et est basé sur l'utilisation d'une bande passant large pour réduire le temps d'établissement ("settling time"). Nous avons confirmé expérimentalement le compromis entre le temps d'établissement et le vacillement de l'horloge et des données. Dans le but de trouver une solution à ce compromis, nous avons conçu un 2^e circuit, cette fois basé sur le suréchantillonnage et un nouvel algorithme de sélection de phase. Ce 2^e circuit supporte les débits binaires de 622 et 1244 Mb/s. Il recouvre l'horloge et les données instantanément (0 bit), produit une horloge et des données dont le vacillement est acceptable, et rencontre les exigences imposées par la recommandation G.984.2 pour GPON ("gigabit PON").

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Table of contents

Associated publications and contribution of authors

The work reported in this thesis has been published or will be published in the form of five journal articles [1]-[5] and five conference papers [6]-[10]. The author of this thesis designed

- the BM-CPA described in [1], [6];
- version 1 of the OCDMA receiver described in [4], [5], [9];
- version 2 of the OCDMA receiver described in [2], [7];
- the burst-mode test solutions described in [1], [10].

Mustansir Mukadam contributed to the design of the BM-CPA and version 2 of the OCDMA receiver. In particular, he participated in the development of the comma detector and the RS(255, 239) decoder. He also provided assistance during the testing and characterization of the BM-CPA and the OCDMA receiver. Rhys Adams designed the OCDMA system (encoders + decoder) described in [5], [9]. Simon Ayotte tuned and characterized the OCDMA system described in [2], [4], [7].

Alan Li designed the broadband CDR described in [3], [8]. The author of this thesis contributed to the behavioral modeling, circuit design, and test of the broadband CDR.

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[1] J. Faucher, M. Y. Mukadam, A. Li, and David V. Plant, "622/1244 Mb/s burst-mode clock phase aligner for GPON using commercial SONET CDRs in 2× over sampling mode," J. Lightw. Technol., submitted for publication, May 2006.

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Other publications that do not directly relate to this thesis

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with differential detection," IEEE Photon. Technol. Lett., vol. 17, no. 11, pp. 2490-2492, Nov. 2005.

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Abbreviations

BER	Bit error rate
BM-CDR	Burst-mode clock and data recovery
BM-CPA	Burst-mode clock phase aligner
BM-RX	Burst-mode receiver
CDR	Clock and data recovery
DUT	Device under test
FEC	Forward error correction
MAI	Multiple access interference
NRZ	Non-return-to-zero
OCDMA	Optical code division multiple access
OLT	Optical line terminal
ONU	Optical network unit
P2MP	Point to multipoint
P2P	Point to point
PD	Phase detector
PLL	Phase-locked loop
PLR	Packet lost rate
PON	Passive optical network
RS	Reed-Solomon
RZ	Return-to-zero
SONET	Synchronous optical network
TDMA	Time division multiple access
VCO	Voltage-controlled oscillator
WDM	Wavelength division multiplexing

CHAPTER 1

Introduction

The most exciting phrase to hear in science, the one that heralds new discoveries, is not "Eureka!" ("I found it!") but rather "Hmm....that's funny..."
– Isaac Asimov

1.1 Motivation

Passive optical networks (PONs) are an emerging access network technology that provides a low-cost method of deploying fiber-to-the-home. PONs are expected to solve the problem of limited bandwidth in the local access network, commonly known as the last mile problem. This thesis is about the design and test of burst-mode clock and data recovery circuits (CDRs) for PONs and multiaccess networks in general.

In PONs, multiple users share the same fiber infrastructure in a point-to-multipoint (P2MP) architecture. A multiple access method is needed to avoid collisions and share the bandwidth across all users. One possible method is time division multiple access (TDMA) [1]. Another possibility is optical code division multiple access (OCDMA) [2][3]. Wavelength division multiplexing (WDM) can be used in conjunction with or independently of both access methods. TDMA, which is used in the various existing types of PON technologies (APON[1], BPON [4], GPON [5], and EPON[6]), is currently the most popular. TDMA and OCDMA create very different signals, which in turn create their own set of challenges for the design and test of CDRs.

1.1.1 Receiver design problem

TDMA

In TDMA PONs, multiple optical network units (ONUs) transmit bursty data to the optical line terminal (OLT) in the central office. Each ONU is assigned a dedicated time

[1] The first PON standard was APON (ATM PON), which used ATM encapsulation of the transported data and was aimed primarily at business applications. APON was quickly followed by BPON, which has superior features.

slot. Due to optical path differences, packets can vary in phase and amplitude. To deal with these variations, the OLT requires a burst-mode receiver (BM-RX) and a burst-mode CDR (BM-CDR). The BM-RX is responsible for amplitude recovery[1] (or threshold extraction), whereas the BM-CDR is responsible for phase recovery. Amplitude recovery and phase recovery are two processes that must repeat at the beginning of every packet. Hence, the main challenge for BM-RX's and BM-CDRs is to recover the amplitude and the phase as close to instantaneously as possible. This is especially critical for networks using short packets. By reducing the number of preamble bits required for physical layer overhead functions like amplitude and phase recovery, more bits are left for the payload and information rate increases.

OCDMA

To date, most OCDMA system demonstrators have used a global clock for BER measurements. The pattern generator and the error detector must therefore be co-located in the same room. In a real network, however, 1) the transmitter and the receiver may be many kilometers apart, and 2) the protocol may not provide a separate channel for the clock. To build a more realistic system demonstrator, a receiver that can recover the clock from OCDMA data is needed. The recovered clock could then serve as a sampling signal for BER measurements, breaking the link between the transmit and receive sides of the network.

The design of the receiver is influenced by the OCDMA code family. In time-spreading OCDMA systems, user codes are created by dividing the bit period into a number of chips. As shown in Fig. 1.1, the output of the OCDMA decoder consists of cross-correlation peaks of duration equal to the chip time. The peaks can be regarded as return-to-zero (RZ) data with a short duty cycle. The short duration of the cross-correlation peaks complicates their sampling. For example, a conventional SONET CDR may successfully align the phase of the sampling (recovered) clock to the phase of the OCDMA signal, but fail to sample the signal correctly due to the short duty cycle. Multiple access interference (MAI) also complicates the design of the receiver. MAI could prevent the CDR from locking if not filtered. For OCDMA to gain more

[1] BM-RX can sometimes refer to a receiver handling both amplitude and phase recovery.

acceptance, digital signal processing functions like FEC must be demonstrated experimentally. The OCDMA receiver is therefore required to convert a multi-level RZ signal to a binary NRZ signal compatible with digital logic. Finally, if the OCDMA signal can step in phase and amplitude, then the receiver should be enhanced with burst-mode functionalities.

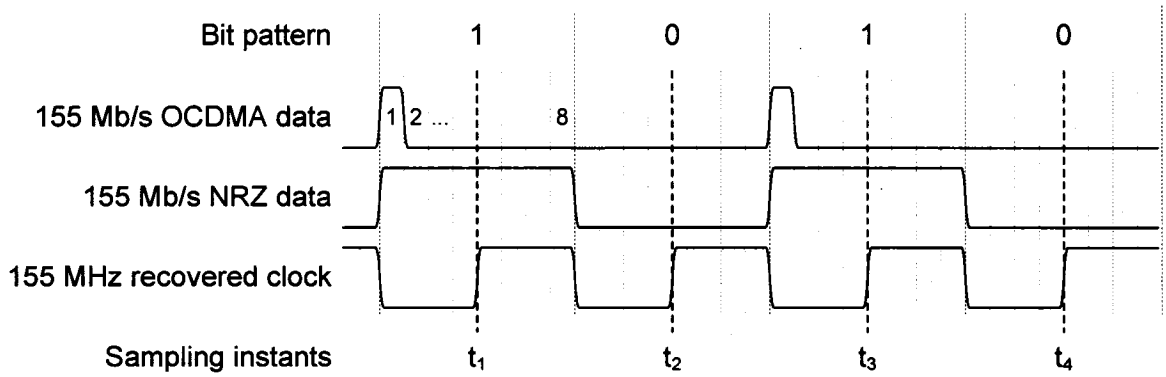

Fig. 1.1. OCDMA sampling problem.

1.1.2 Receiver testing problem

Pattern generation

One common problem to both BM-RX's/CDRs and OCDMA receivers is the difficulty of generating a test signal. This in turn complicates the testing, debugging, and characterization of the receivers before their use in a system demonstrator or a real application.

Testing a BM-RX/CDR requires the customization of conventional test equipment. On the transmit side, the pattern generator should be able to produce amplitude and phase steps. On the receive side, the error detector (ED) should be able to perform burst BER measurements on a device under test (DUT) that never really reaches steady state. For example, the phase step response of the BM-CDR can make the ED lose pattern synchronization at the beginning of every packet.

For OCDMA, one problem is to emulate the cross-correlation peaks and the MAI at the output of the OCDMA decoder. A DUT (the OCDMA network) must often serve as a pattern generator for characterizing another DUT (the receiver).

Measurement of phase acquisition time

One popular way of estimating the phase acquisition time of a CDR is to monitor the controlling voltage of the voltage-controlled oscillator (VCO). The settling time corresponds to the time required for the envelope of the signal to settle to within x% of the steady state value, where x is an arbitrary value (usually 2 to 5%). The problem with this solution is two-fold. First, it is only a qualitative measure of the phase acquisition time. Second, the VCO control voltage may not be available on a package pin, especially for commercial CDRs. An alternative method that does not rely on the VCO control voltage would be useful for measuring the phase acquisition time of CDRs.

1.1.3 CDR simulation problem

The design of CDR circuits, like any other complex circuits, is difficult without good simulation tools. One problem with PLL and CDR circuits is their long simulation time. Simulating PLLs and CDRs is time consuming because the dynamic response of the system is much slower than the output frequency. For example, the output frequency of an OC-12 CDR is 622.08 MHz. In order to simulate 10 samples per period, the sampling frequency must be 10 × 622.08 MHz. This corresponds to a time step of ~160 ps. Jitter simulations require an even smaller phase step to capture the cycle-to-cycle phase variations, equivalent to a fraction of the clock period. In comparison, the maximum bandwidth of an OC-12 CDR is 0.5 MHz [7], more than four orders of magnitude lower than the sampling frequency of 10 × 622.08 MHz. Thus, traditional simulators take a long time to compute the dynamic response of the system since many simulation samples are required. For an OC-12 CDR, the settling time to within 2% of the steady-state value is in the order of 1 μs (see Section 5.3.4.1). This represents more than 6000 samples just to simulate the phase step response of the CDR. 10's of thousands more samples are required in order for the circuit to reach steady state. The consequence is that transistor-level simulations of PLL and CDR circuits can take hours or even days to perform.

1.2 Thesis objectives

The objective of this thesis is to provide solutions for most of the problems enumerated above. In particular, we designed

1) a receiver for OCDMA networks;
2) a BM-CPA for TDMA networks;
3) a burst-mode test solution for the accurate measurement of phase acquisition time;
4) reusable models for fast and accurate behavioural and mixed-level simulations of CDR circuits.

The two problems that this thesis does not address are 1) the design of a BM-RX for amplitude recovery, and 2) the design of an OCDMA receiver that can handle amplitude and phase steps. We chose not to address the amplitude recovery problem because existing solutions are relatively mature, leaving less room for innovations. Instead, we chose to concentrate on the design of BM-CDRs, one of the most critical blocks of a PON according to [8]. In order to contribute to the field and provide a new alternative to existing solutions, the objective of the research was to design a BM-CDR with instantaneous phase acquisition (0 bit) and good jitter characteristics.

Unlike the BM-RX and the BM-CDR, for which designs had already been reported in the literature, a standalone OCDMA receiver capable of MAI rejection, CDR, and FEC had no precedent. The objective of the research was therefore to design such a receiver, leaving burst-mode functionalities for future work.

1.3 Thesis organization

We review in Chapter 2 the most relevant work to date on OCDMA receivers, burst-mode receivers (amplitude and phase recovery), and the modeling and simulation of CDRs.

We describe in Chapter 3 the implementation details of a 155.52 Mb/s OCDMA receiver. The receiver is capable of MAI rejection, CDR, and FEC. We measure the BER performance of an OCDMA network with ideal sampling (global clock) and non-ideal sampling (recovered clock). We also compare the experimental BER performance of an OCDMA network with and without FEC. We use the coding gain to increase the number of supported users, and compare the experimental and theoretical values of the coding gain.

In Chapter 4, we report on the design and test of two burst-mode CDRs: a 1.25 Mb/s broadband CDR, and a 622/1244 Mb/s burst-mode clock phase aligner (BM-CPA[1]). Both CDRs achieve fast phase acquisition, but using a different technique. The 1.25 Gb/s broadband CDR uses a wide bandwidth to reduce the settling time, whereas the BM-CPA uses over sampling and a novel phase picking algorithm. We discuss the trade offs of both techniques. We conclude the chapter by describing a high-speed (up to 10 Gb/s) packaging solution for the BM-CDRs.

We present in Chapter 5 the design of CppSim [19] behavioral models for three types of CDRs: SONET, broadband, and over sampling CDRs. We verify the models against the well-known baseband model [20], [21]. The CppSim models have the advantage of not making any linearity assumption and of being reusable in mixed-level simulations within the Cadence design environment. We use the models to simulate, analyze, and compare the phase acquisition time and the jitter characteristics of the three CDRs. We finally daisy chain eight CDRs of each type and simulate the jitter at the output. We report the time required for this numerically intensive simulation to demonstrate the capabilities of CppSim and of behavioral modeling in general.

In Chapter 6, we summarize our research and propose future research directions.

1.4 Original contributions

- Design of a 622/1244 Mb/s BM-CPA for GPON. The BM-CPA provides instantaneous phase acquisition for any phase step ($\pm 2\pi$). It also has excellent jitter characteristics, comparable to those of SONET CDRs. Hence, multiple BM-CPAs can be daisy chained if required.
- Design of the first standalone OCDMA receiver with MAI rejection, CDR, and FEC.
- Development of a measurement methodology to measure the phase acquisition time of BM-CDRs down to an accuracy of one bit. Our methodology is based on the measurement of packet lost rate and bit error rate.

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[1] BM-CPA is a synonym of BM-CDR. In this thesis, we will use BM-CDR to refer to a generic burst-mode clock and data recovery circuit. We will use BM-CPA to refer to the specific implementation of Section 4.2.

- First multi-user OCDMA system demonstrator with full clock and data recovery. We used the clock recovered by the OCDMA receiver for BER measurements, effectively breaking the link between the transmit and receive sides of the OCDMA network. By avoiding the use of a global clock, the demonstrator shows the viability of OCDMA as a multiple access technology for PONs.
- First experimental comparison of the BER performance of an OCDMA network with optimum sampling (global clock) and non-optimum sampling (recovered clock). We found a negligible power penalty when the CDR was operating at the same rate as the chip rate. Our results will help refine theoretical models of OCDMA systems, and provide input for establishing realistic power budgets.
- Experimental demonstration of FEC in the context of 2D λ-t OCDMA networks. To date, the work on OCDMA with FEC was either theoretical or required a global clock. We performed our measurements using our *standalone* OCDMA receiver with CDR, automatic detection of the payload chips, and RS(255, 239) decoding. In addition to filtering out MAI and recovering the clock, the receiver eliminated a BER floor and increased the number of simultaneous users in the detection window from two to five.
- Jitter analysis of the over sampling BM-CPA. We used fast and accurate behavioral models to simulate or derive the theoretical jitter transfer bandwidth and jitter tolerance of the BM-CPA. We also simulated the jitter at the output of a cascade of BM-CPAs. We performed the same simulations on a broadband CDR and a SONET CDR and compared the results with those obtained with the BM-CPA.

The journal articles [10]-[14] and conference papers [15]-[18] that have resulted from our work show evidence of our original contributions to knowledge.

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CHAPTER 2

Review of the state of the art

In this chapter, we review existing OCDMA and burst-mode receiver solutions. We also present an historical overview on the modeling of CDRs and we review some of the most popular simulation tools.

2.1 OCDMA

Generally, OCDMA techniques can be classified based on two criteria [28]: working principle and code dimension. Fig. 2.1 summarizes the classification of OCDMA techniques. First, the working principle is either incoherent OCDMA [1]-[10], where the coding is done on an optical power basis, or coherent OCDMA [3]-[6], [11]-[13], where the coding is done on a field amplitude basis. Second, the code dimension is either one-dimensional (1D), where coding operations are performed either in the time domain [1]-[7], [11]-[13] *or* the frequency domain [8]-[10], [14]-[17], or two-dimensional (2D), where coding operations are performed in the frequency *and* time domains simultaneously [18]-[25].

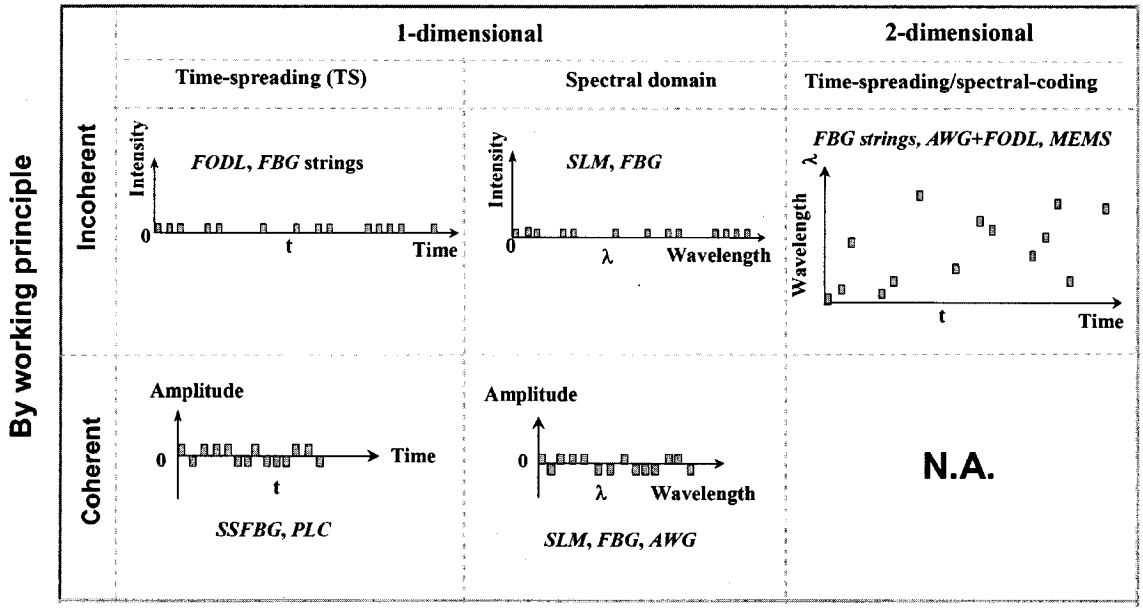

Fig. 2.1. Classification of different OCDMA schemes [29]. Devices that have been used as en/decoder for OCDMA include fiber optic delay line (FODL), spatial lightwave modulators (SLM), arrayed-waveguide grating (AWG), planar lightwave circuits (PLC), fiber-Bragg-gratings (FBG), superstructured FBG (SSFBG), and micro-electro-mechanical-systems (MEMS).

Incoherent time-spreading (TS) OCDMA is a popular OCDMA scheme because it is easy to implement at relatively low bit rates [1]-[9]. In TS-OCDMA, the codes are unipolar (0, 1) and data is encoded using on-off keying. The number of time chips is usually limited by the speed of the electronics. This leads to a small code size and poor correlation properties [1]-[4]. Coding in the frequency domain provides a new degree of freedom and a way to increase the code size while keeping the number of time chips relatively small. The resulting 2D λ-t OCDMA codes [18]-[25] provide better correlation properties than 1D solutions.

Even if 2D λ-t OCDMA systems have relatively good correlation properties, MAI still limits their performance as the number of users increase. Since MAI has a direct impact on the BER of the system, various solutions have been proposed to reduce it. We present a short overview of existing solutions in Section 2.1.1. Another way to improve the BER is to use FEC. Since FEC is a digital processing block, the receiver must provide it with a clock. In Section 2.1.2, we present OCDMA demonstrators that use a global clock and in Section 2.1.3, we discuss FEC in the context of OCDMA.

2.1.1 MAI rejection

Electrical thresholder

In an ideal OCDMA network, chip-rate detection is assumed [29]. For coherent TS-OCDMA employing long codes, the chip rate may be as high as several hundreds Gchip/s [30]. The bandwidth of the receiver cannot match such a high chip-rate detection requirement, the consequence being a BER degradation. Hence, electrical thresholders are only suitable for OCDMA codes with few time chips. An example is the 2D λ-t OCDMA codes used in [31].

Time gating

Optical time gating techniques have been proposed to improve the BER performance of OCDMA systems [26], [27], [32], [50]. The idea is to eliminate MAI outside the gating window to facilitate sampling. This operation is equivalent to narrow bandpass filtering in wireless spread spectrum systems. For example, in [50], a time gating signal derived from the supercontinuum source opens a sampling window for the autocorrelation peaks. The gating signal is sent over the network on a separate channel. Placing the optical time gate before the photodetector has the advantage of reducing the bandwidth requirement of the receiver [32] – a bandwidth equal to the bit rate is sufficient. If an electrical time-gate is placed after the photodetector, the receiver must have a bandwidth equal or greater than the chip rate. One disadvantage of time gating is that it requires chip-level synchronization, which makes OCDMA lose its asynchronous advantage over TDMA.

Optical thresholder

Optical thresholders provide another way to separate autocorrelation peaks from the MAI to eliminate the need for ultrafast receivers. Their advantage over time gating is that they do not require chip synchronization. Various optical thresholding techniques were proposed for OCDMA applications [51]-[54]. Most techniques are based on non-linear effects in fiber.

2.1.2 Sampling clock

To date, most or all OCDMA technology demonstrators have relied on the availability of a global clock in system implementation and testing [44], [46]-[51]. For example, in

[46], [47], a 13 Gb/s D flip-flop (DFF) is used to sample the data at the system data rate (1.25 GHz). As shown in Fig. 2.2, the clock input of the DFF is a global clock whose phase is manually adjusted to obtain optimum sampling of the decoded signal.

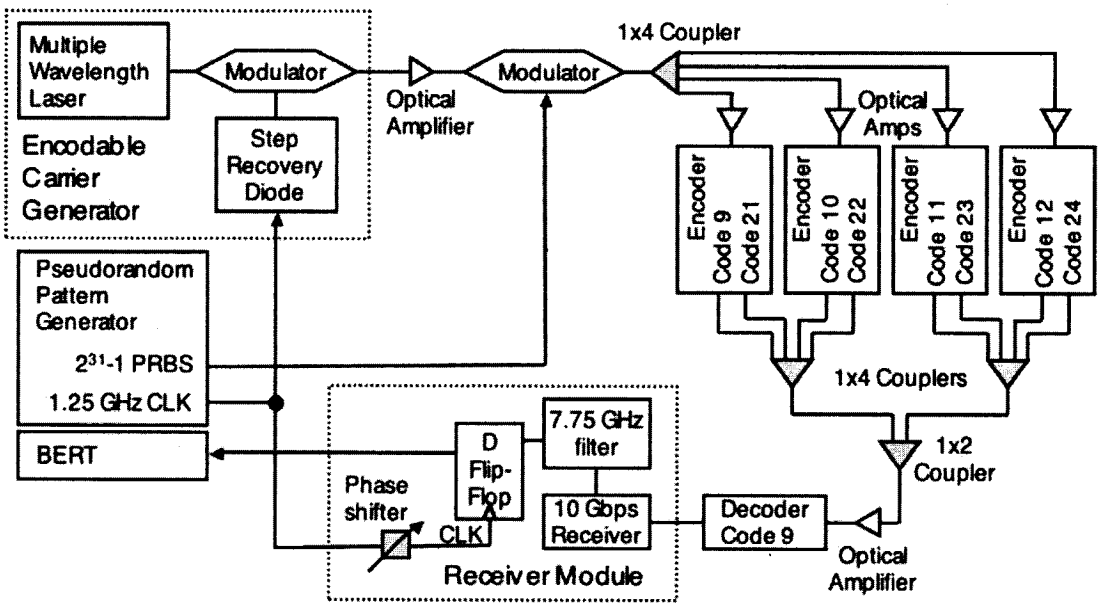

Fig. 2.2. OCDMA system demonstrator using a global clock [47].

Sampling with a global clock has the same disadvantages as time gating, namely that chip level synchronization is required and a signal must be sent from the transmitter to the receiver on a separate channel. An OCDMA system demonstrator without global signals for gating or sampling was reported in [45] (see Fig. 2.3). An optical thresholder filters out MAI and an optical receiver recovers the clock from the OCDMA data. Details on the CDR are not given in [45]. Moreover, it is not clear whether the OCDMA receiver performs an RZ to NRZ conversion for OCDMA compatibility with digital logic. To the author's knowledge, this is nevertheless the closest demonstration of a standalone OCDMA receiver reported to date. The only feature the receiver is missing is FEC, which we discuss in the next section.

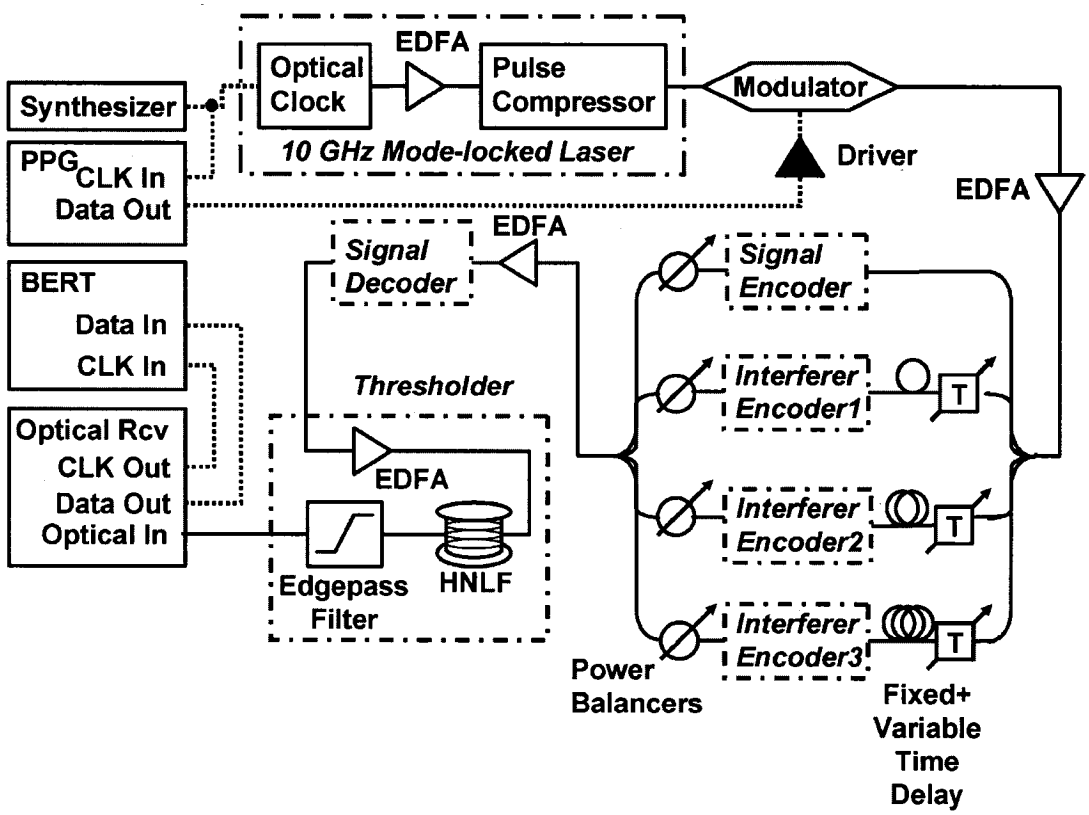

Fig. 2.3. OCDMA system demonstrator without a global clock [45].

2.1.3 Forward error correction

FEC is widely used to improve the BER of long-haul communication networks. For example, the RS(255, 239) code was adopted in ITU-T Rec. G.709 [42]. The benefits of FEC in OCDMA were demonstrated theoretically in [34]-[38], [55], but very few practical implementations have been reported to date. Table 2.1 summarizes the parameters of three OCDMA systems demonstrators with FEC [39]-[41].

Table 2.1
OCDMA system demonstrators with FEC

Reference	FEC code	# users	Data rate/user
[39]	RS(255, 241)	8	622.08 Mb/s
[40]	RS(255, 239)	12	10.71 Gb/s
[41]	RS(255, 239)	32	10 Gb/s

The demonstrator described in [40] uses the Anritsu MP1590B Network Performance Tester for FEC encoding, FEC decoding, and BER measurements. Since the same test equipment performs both pattern generation and error detection, it is probably safe to assume that a global clock was used. In [39] and [41], it is unclear whether a global clock was used.

2.2 Burst-mode receivers

The upstream TDMA traffic in a PON consists of packets with widely varying amplitudes [56]. To handle such traffic, the OLT in the central office of the PON must use a BM-RX [57], [58], [60]-[66]. In order for PONs to be successful economically, they must provide a long physical reach (distance between the central office and the subscribers) and a large splitting factor (number of subscribers served by a single PON). The development of BM-RXs is therefore aimed at providing a high sensitivity and dynamic range. These two performance characteristics determine the physical reach and the splitting ratio of the PON. When the BM-RX uses dc coupling, another aim is to minimize the burst-mode sensitivity penalty.

DC-coupled BM-RXs exhibit two sources of sensitivity penalties when compared to continuous-mode receivers. First, the extracted decision threshold is noisy, giving rise to a sensitivity penalty. This penalty, which can range from a few tenths of decibels up to a few decibels [59], was studied extensively in [67]-[70]. A second sensitivity penalty stems from unavoidable dc offsets. The penalty due to a fixed dc offset was studied in [70], whereas the penalty due to random dc offsets was studied in [59].

2.3 Burst-mode CDRs

The upstream traffic in a PON can vary in amplitude, but also in phase. The OLT in the central office of a PON must therefore use a BM-CDR with fast phase acquisition. Since the timing of each ONU is derived from the downstream traffic, the BM-CDR can assume a constant frequency. Different approaches have been proposed to build CDRs with short phase acquisition times.

The first approach consists in using a PLL-based CDR with a dynamic loop bandwidth [71]. While the CDR is acquiring lock, its closed-loop bandwidth is increased

to reduce the settling time. Once the CDR has locked, its bandwidth is restored to its original value for the rest of the packet to minimize output jitter.

The second approach is based on gated oscillators or some kind of gating circuit. The approach was first proposed by Banu [72] and then used in [56], [73]-[75]. These burst-mode CDRs perform clock phase alignment by triggering the local clock on each transition of the input. Phase acquisition is instantaneous, but this solution is susceptible to pulse distortions and does not filter out input jitter [43]. A jitter rejection method was proposed in [76], but involved complex circuits.

The last approach is based on over sampling [77], [78]-[80]. A correlation or phase picking algorithm is used to select the best sample. One can either over sample in time using a clock frequency higher than the bit rate, or over sample in space using a multiphase clock with a frequency equal to the bit rate. Over sampling in time requires faster electronics, whereas over sampling in space requires low skew between the multiple phases of the clock.

2.4 Behavioral simulations of CDR circuits

2.4.1 Models

The model of a PLL-based CDR is very similar to that of a PLL [81]. The main difference is that the CDR must deal with random data instead of periodic data. This imposes a frequency detection constraint on the phase detector (PD). Two popular PDs for random data are the Hogge PD [82] and the Alexander PD [83]. For the Hogge PD, whose average behavior is linear, PLL theory can be adapted for the analysis of CDRs. In particular, the effect of data transition density on the gain of the phase detector must be taken into account.

Historically, theories were first developed to analyze analog PLLs [84], in which the PD is an analog mixer that multiplies two analog signals: the reference and the feedback signals. When the PLL is nearly locked, the low frequency component of the mixer output is approximately linearly proportional to the phase difference. A linear model is obtained by assuming that the high frequency component is filtered out by the loop filter.

The theory was then extended to the analysis of charge-pump PLLs with digital phase and frequency detectors (PFDs) [85]. When the effect of the impulsive corrections are

averaged over time, the discrete-time system can be approximated by the same continuous-time model. This approximation is valid when the loop bandwidth is much lower than the reference frequency.

Discrete-time transfer functions [86], [87] have also been derived to account for the discrete-time nature of the signals in charge-pump PLLs. These theories also make linear assumptions and are therefore confined to the analysis of PLLs in a nearly locked state.

The linear models discussed up to here are based on the replacement of a non-linear PD/PFD with a linear block. These models do not provide accurate details on the individual cycles, with the result that they are fast to simulate. One disadvantage of linear models is that they cannot be used to simulate PLLs in the unlocked state. However, when some empirical rules of thumb are respected, linear theories prove to be very successful for practical designs.

Due to the wide applications of PLLs, there have been continual efforts on the development of models that hold even when the PLL is unlocked. Instead of replacing the PD with a linear block, a set of nonlinear equations describing the behavior of the PLL are linearized [88]-[91]. The equations are kept simple by considering individual cycles separately. Exact solutions can therefore be derived to model the behavior of the PLL until the PD changes the state of the system. The resulting models hold even if the PLL is unlocked and provide accurate details that take place in individual cycles.

2.4.2 Simulation tools

Various simulation tools are available to simulate the models described in the previous section. Spice/Spectre, Simulink/Matlab, and Verilog-AMS are some of the most popular. We discuss their pros and cons below.

Spice/Spectre

Spice and Spectre both simulate a netlist describing the interconnections between the blocks of the overall circuit or system. Node voltages and branch currents are determined by solving a set of simultaneous equations. Spice and Spectre provide the accuracy required for the simulation of analog and mixed-signal circuits. On the other hand, the solution of simultaneous equations is a slow process and the resulting simulation times are very long for complex circuits or systems.

Simulink

Simulink uses a state-space description of each of the individual blocks of the system. The response of the system is computed using standard matrix computations. The level of detail is much lower than with Spice or Spectre. Moreover, because there is no need to solve simultaneous equations, the computations are much faster. Simulink therefore provides an interesting framework for the architectural exploration of complex circuits and systems.

Unfortunately, there are a few disadvantages to Simulink. First, it requires that individual blocks be specified in terms of a state-space description. This may be rather cumbersome for certain circuits or systems. Second, Simulink operates much faster on vectorized expressions than on expressions within conditional loops. This may also be cumbersome since conditional loops provide a much more general computation structure than vectorized expressions. Finally, the graphical framework of Simulink is disjoint from other CAD tools used in integrated circuit (IC) design. This creates a significant disconnect between architectural exploration and circuit implementation.

Verilog-AMS

Verilog-AMS is one of the most promising simulation environments for the simulation of large circuits. This simulator combines the Spice/Spectre and Verilog simulators into a common simulator core. Certain blocks can be simulated at the transistor level while some others are simulated at the behavioral level. These mixed-level simulations are faster than pure transistor-level simulations. They can therefore enable the verification of a particular circuit in the context of the overall system. Another advantage of Verilog-AMS is that it provides a way of co-simulating analog and digital circuits. This enables certain types of simulations that would not otherwise be possible.

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CHAPTER 3

OCDMA receiver

This chapter consists of a collection of three journal articles [1], [2], [3] for which the author of this thesis was the main contributor. The main connection between the three papers is the OCDMA receiver. In the first experiment [1], we realized the first multi-user OCDMA system demonstrator with full clock and data recovery using a novel OCDMA receiver. The OCDMA encoders and the OCDMA decoder were designed and tested by Adams [4]. The author of this thesis designed the OCDMA pattern generator and the OCDMA receiver.

In the second experiment [2], we compared the experimental BER performance of a 2D λ-t OCDMA system with optimum sampling (global clock) and non-optimum sampling (recovered clock from our OCDMA receiver). The OCDMA system, which was assembled and characterized by Ayotte [5], [14], was different from the one we used in the first experiment. Through this work, we found that practical CDR for 2D λ-t OCDMA provides an acceptable BER penalty as compared to optimum sampling with a global clock.

In the third experiment [3], we demonstrated experimentally for the first time the impact of forward-error correction (FEC) on the performance of 2D λ-t OCDMA with no global clock. We used the same OCDMA system as in the second experiment. On the other hand, the OCDMA receiver was an enhanced version of the receiver that we used in the first two experiments. Additional features include better sampling, automatic detection of the payload chips, and RS(255, 239) decoding. The enhanced receiver more than doubled the number of supported users at a BER $< 10^{-10}$. We found a good agreement between analytical and experimental results.

3.1 OCDMA receiver with CDR

Reference: [1]

Abstract – We report the first multi-user optical code-division multiple access (OCDMA) system demonstrator with full clock and data recovery (CDR) using a novel OCDMA receiver. We achieve receiver sensitivities of -19.1, -16.3, and -9.2 dBm for 1, 2, and 3 users, respectively, at a BER $\leq 10^{-10}$ using a 2^{20}-1 PRBS. Our results show the viability of OCDMA as a transport technology for access networks.

3.1.1 Introduction

OCDMA is a promising technology for use in optical access networks carrying bursty and asynchronous traffic [6]. 2D wavelength-time (λ-t) OCDMA has been explored as a means to provide greater flexibility in code design, increase the number of simultaneous users, increase data throughput, and provide better scalability to accommodate more users [7]-[9]. To date, most or all OCDMA technology demonstrators have relied on the availability of a global clock in system implementation and testing, especially for performing bit-error-rate (BER) measurements [10]-[12], which is not representative of a real functional access network. For OCDMA to be a competitive alternative to conventional multiple access schemes, such as TDMA and WDMA, full clock and data recovery (CDR) at the receiver end must be demonstrated. In this paper, we report the first multi-user OCDMA system demonstrator with full CDR. This is enabled by a novel OCDMA receiver that was designed using commercially available components. In addition to recovering the clock from the OCDMA signal, the receiver converts the multi-level RZ signal with a 1/N duty cycle (N is the number of time chips) to a binary NRZ signal for further processing. The OCDMA receiver allows digital logic circuits to process OCDMA data in the same way as if TDMA or WDMA had been used in the transport network.

3.1.2 OCDMA system demonstrator

3.1.2.1 Experimental setup

Fig. 3.1(a) shows the OCDMA system that was implemented and tested. Unlike other OCDMA systems [10]-[12], no global clock is used at the receiving end to perform BER measurements. Instead, the clock is recovered from the data by the OCDMA receiver described in the next section.

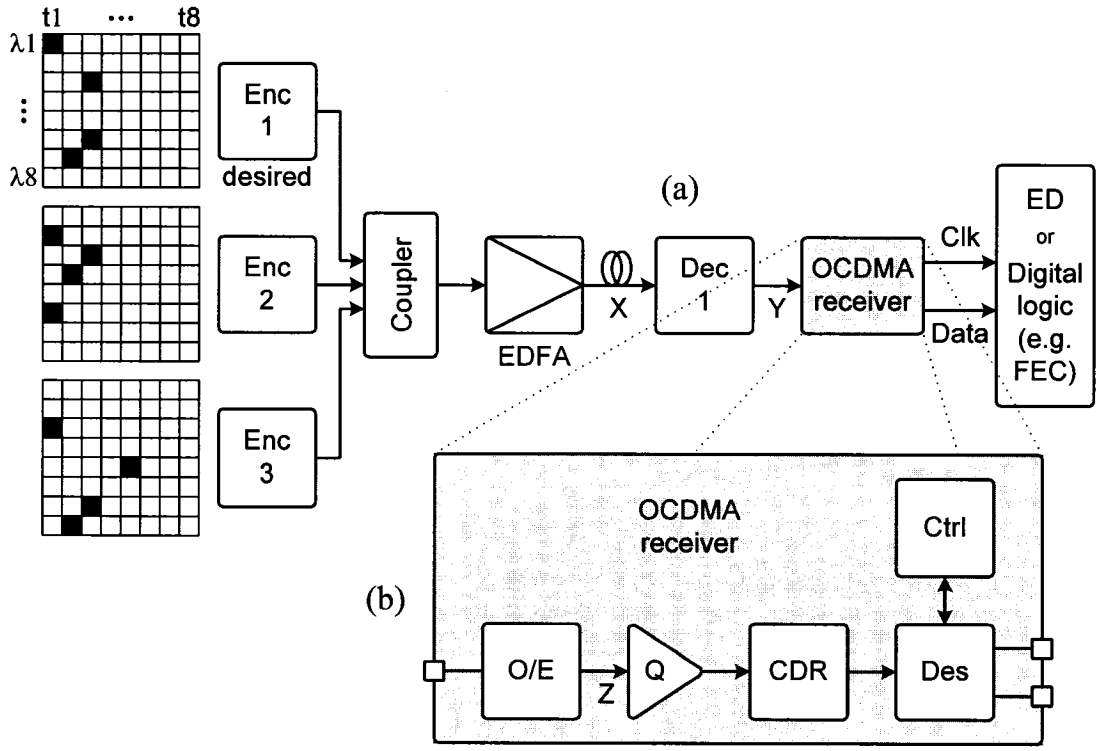


Fig. 3.1. (a) OCDMA demonstrator with CDR, (b) OCDMA receiver. ED: error detector.

The OCDMA system is based on the 2D λ-t depth first search codes (DFSCs) described in [9]. While many different 2D λ-t code families exist, we have focused on DFSCs since they possess the following key advantages: (1) the codes can be designed using fewer time chips and thus are able to support higher data rates and (2) since for a given code dimension a greater number of codes can be generated, they can fully exploit the gain provided by forward error correction (FEC) to allow for a large number of simultaneous users operating with good BER performance [9].

In our system demonstrator, we use codes having 8 wavelengths, 8 time chips, and a weight[1] of 4. The chip rate is OC-24 (1.24416 Gbps) and the bit rate is OC-3 (155.52 Mbps). Of the 31 possible codes generated by the DFS algorithm, we use the 3 codes illustrated in Fig. 3.1(a). The 2 interferers (Enc 2 and 3) were chosen such that each has 2 wavelengths in common with the desired user (Enc 1), thereby making the task of identifying the auto-correlation peak more difficult (this represents a worst-case scenario among the 31 codes generated by the DFS algorithm). A "1" data bit is represented by a broadband pulse (modulated ASE from a broadband source) having a duration equal to the chip time; no power is transmitted for a "0" bit. The data from the different users are then optically encoded. The encoders and decoder are constructed using commercially available wavelength de-/multiplexers, power splitters and combiners; the time delays are obtained by splicing appropriate lengths of fiber, each carefully measured to have less than ± 5% of a time chip of error in order to minimize the effects of encoder/decoder mismatch [4]. The decoder (Dec 1) performs matched filtering before detection. Erbium doped fiber amplifiers (EDFAs) are used to amplify the signals. The target BER is 10^{-10} using a PRBS length of 2^{20}-1 for each user. All three users transmit at the same power. Various lengths of decorrelating fiber, corresponding to time shifts of 8 to 16 bits, are used to emulate different bit streams for each user. The system parameters are summarized in Table 3.1.

Table 3.1
OCDMA system demonstrator parameters

Parameter	Value
Wavelength range	1547.6 nm - 1553.2 nm
Channel spacing	100 GHz (0.8 nm)
Data rate	155.52 Mb/s (OC-3)
Chip rate	1.24416 Gb/s (OC-24)
PRBS	2^{20}-1
Photoreceiver bandwidth	800 MHz

[1] The code weight is the number of '1' in the code.

3.1.2.2 OCDMA receiver

The OCDMA receiver is made of five building blocks [see Fig. 3.1(b)]: a photoreceiver [photodetector (PD) + transimpedance amplifier (TIA)], a quantizer (Q), a SONET CDR, a 1:16 deserializer (Des), and a controller (Ctrl). The quantizer and the CDR are from Analog Devices (part #ADN2819), while the deserializer is from Maxim-IC (part #MAX3885).

The quantizer applies a threshold on the incoming data in order to filter out multi-access interference (MAI) from the interferers. The CDR recovers the clock at twice the chip rate, or OC-48, to accommodate the 1:16 deserializer (2.48832 Gbps/16 = 155.52 Mbps). Clock recovery at OC-24 would also work, provided a 1:8 deserializer is available. With equal rise and fall times, a 1:8 deserializer is preferable since the auto-correlation peaks of the OCDMA signal are sampled in the middle. With unequal rise and fall times, it may be advantageous to sample the auto-correlation peaks at a slight offset from the middle. The 1:16 deserializer allows this, at the cost of a higher bandwidth CDR (OC-48 instead of OC-24).

The 1:16 deserializer produces a 155 MHz clock by dividing the clock output of the CDR by 16. It also converts the RZ signal with 1/8 duty cycle to an OC-3 NRZ signal. Port 1 of the 16-bit deserializer output serves as the OCDMA receiver output. Without the controller, data could appear on any one of the 15 unused ports of the deserializer output. When the link is first established, the controller configures the deserializer such that data is steered to port 1. This is accomplished by monitoring activity on port 1 and sending appropriate retiming/reframing signals to the synchronization input of the deserializer.

The OCDMA receiver can be used in OCDMA systems other that the one described here. The receiver supports chip rates of OC-3, OC-12, OC-48, Gigabit Ethernet (GbE), and 15/14 FEC rates. The supported bit rates depend on the number of time chips N in the OCDMA code and the availability of a 1:N deserializer. With higher-speed electronics, the design can be scaled up to higher chip and/or bit rates. For example, a receiver built from a 10 Gbps CDR and a 1:8 deserializer could support a bit rate of 1.25 Gbps (assuming 8 time chips). Such a receiver could enable the use of OCDMA in gigabit passive optical networks (ITU-T G.984 GPON and IEEE 802.3ah EPON), which currently use TDMA as an access method. Considering that 1) multi-access networks

typically operate at slower data rates than long-haul networks, and 2) the design is based on off-the-shelf SONET components, this solution will leverage the development of 10 and 40 Gbps electronics to support 1.25 to 5 Gbps bit rates cost and time effectively.

3.1.3 Measurement results

Figs. 3.2(a) and (b) show all 3 encoded and the decoded optical signals, respectively (measured with an optical sampling module having a 12.5 GHz bandwidth and 32× averaging); Fig. 3.2(b) confirms that the reconstructed desired signal (auto-correlation peak) is indeed distinguishable from the MAI. The cross-correlation pulses in the decoded waveform correspond to the interfering wavelengths that are retained by the decoder.

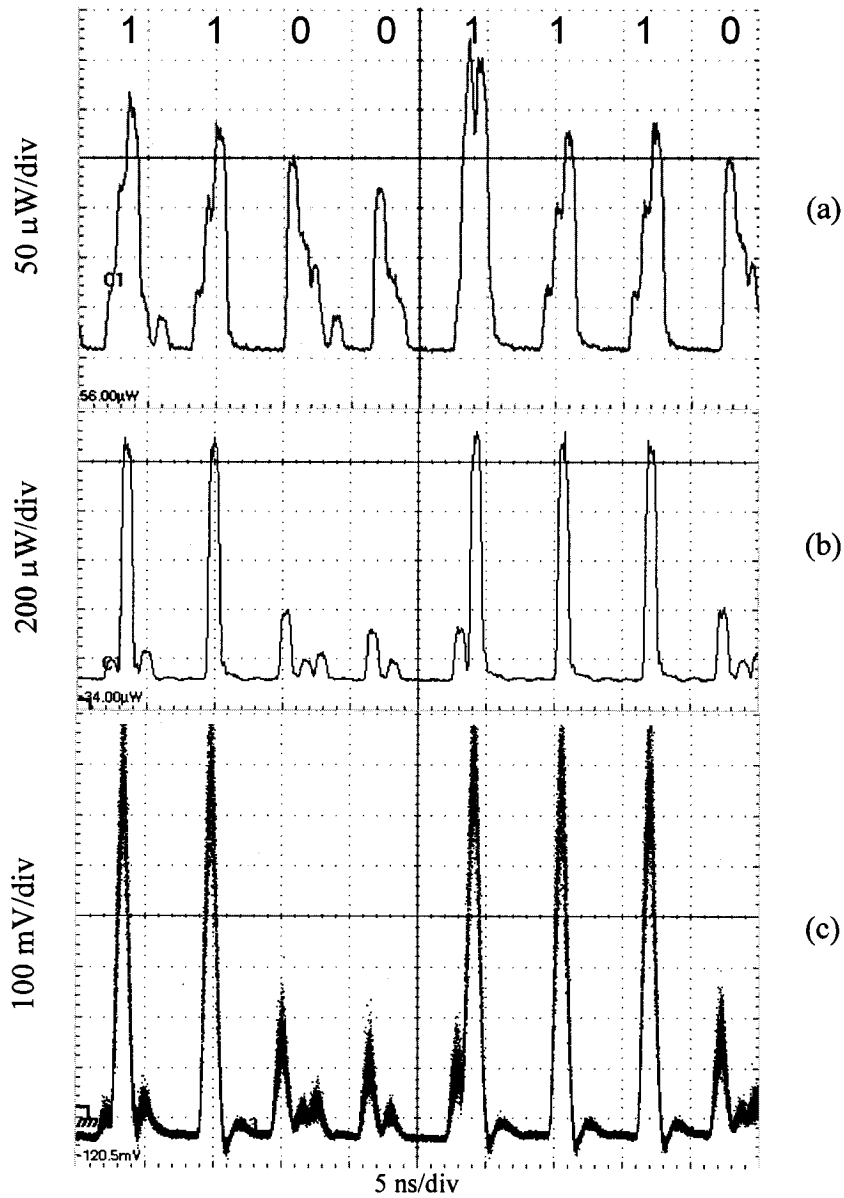


Fig. 3.2. (a) Three OCDMA encoded signals ("X" in Fig. 3.1) merged on the same fiber (8 bits of the 2^{20}-1 PRBS are shown), (b) decoded signal ("Y" in Fig. 3.1), (c) photoreceiver output ("Z" in Fig. 3.1), just before the quantizer.

Fig. 3.2(c) (no averaging, 10s persistence) shows the signal after the photoreceiver, which has a bandwidth of 800 MHz. The output of the OCDMA receiver, after 3R regeneration, is shown in Fig. 3.3. The measured root-mean-square (RMS) jitter on the recovered clock was 15.6 ps (0.002 UI rms). The receiver not only recovers the clock from the OCDMA signal, it also converts the multi-level RZ signal with a duty cycle of 1/8 to an OC-3 NRZ signal.

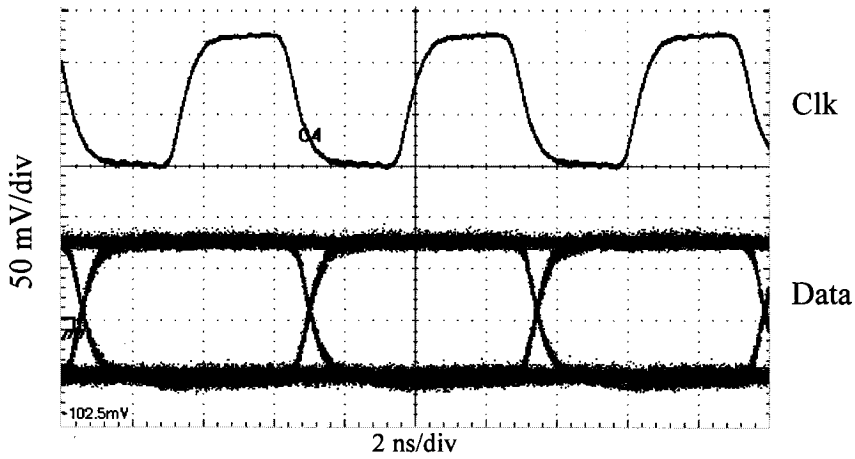


Fig. 3.3. Recovered clock and data. The width of the eye is about 6.4 ns, corresponding to a bit rate of 155.52 Mb/s (OC-3).

The sensitivity of the OCDMA receiver was measured using three different test conditions, listed in Table 3.2.

Table 3.2
Receiver Sensitivity Results

Case	Sensitivity* (dBm)	Power penalty (dB)
Desired user	-19.1	
Desired user + 1 interferer	-16.3	2.8
Desired user + 2 interferers	-9.2	9.9

*BER $\leq 10^{-10}$, 2^{20}-1 PRBS.

Fig. 3.4 shows the eye diagram of the signal after O/E conversion (signal "Z" in Fig. 3.1) for the worst case scenario (desired user + 2 interferers). Note that the sampling oscilloscope was triggered at the chip rate in Fig. 3.4, whereas it was triggered using the pattern sync signal from the pulse pattern generator in Fig. 3.2(c). For the situation with the desired user only, the measured sensitivity was -19.1 dBm at a BER $\leq 10^{-10}$ using a PRBS of length 220-1. The introduction of one and two interferers caused power penalties of 2.8 dB and 9.9 dB, respectively. We obtained a sensitivity of -15.5 dBm when only the desired user was transmitting over 7 km of single-mode fiber (with no dispersion compensation), corresponding to a power penalty of 3.6 dB relative to the

back-to-back case. We attribute the power penalties largely to MAI and beat noise. MAI is expected to vary with the OCDMA codes being used, while beat noise is known to limit performance in OCDMA networks [13].

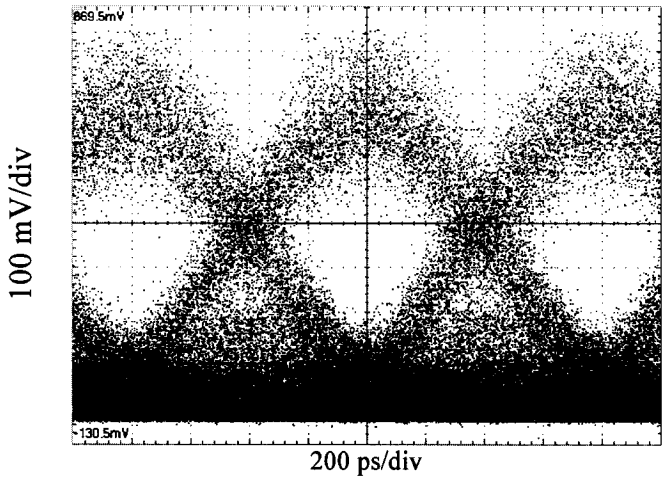


Fig. 3.4. Photoreceiver output ("Z" in Fig. 3.1) at receiver sensitivity (-9.2 dBm) with all three users present on the network. The width of the eye is about 800 ps, corresponding to a chip rate of 1.24416 Gbps (OC-24).

3.1.4 Conclusion

In summary, we have described a multi-user OCDMA system demonstrator with full CDR using a novel OCDMA receiver. No global clock was used in the system. The receiver functionality was demonstrated in a 2D λ-t OCDMA system, but can be used in other OCDMA systems. The receiver uses commercially available components and allows OCDMA to be compatible with digital logic circuits developed for TDMA and WDMA networks. Our results show the viability of OCDMA as a transport technology for access networks.

3.1.5 Notes

In [1], we did not include any details about the custom OCDMA pattern generator that we designed. The generator allowed us to test and debug the receiver before assembly of the OCDMA system (encoders + decoder) was complete.

The main requirements for the generator were that it be able to generate a signal with 1) short pulses to emulate chips of the OCDMA code, and 2) MAI. We created MAI by

combining eight independent signals on a single SMA cable. Each signal was generated by a separate port of the HP80000. We created short pulses (chips) by generating data at the chip rate as opposed to the bit rate. Given the OCDMA codes of Fig. 3.1, we used a Matlab script to calculate the amplitude of the cross-correlation peaks and MAI at the output of the decoder. By carefully choosing the amplitude and the chip pattern of each of the eight signals, we were able to emulate the output of the OCDMA decoder [see Figs. 3.2(b) and (c)] almost exactly (without the beat noise). MAI allowed to test the quantizing function of the OCDMA receiver, whereas the short pulses allowed us to verify that the CDR was sampling properly. We obtain error free operation (BER < 10^{-10}) for low levels of MAI. The OCDMA receiver operated error free up to the point where the amplitude of MAI was approximately as high as the amplitude of the cross-correlation peaks.

3.2 OCDMA with a recovered clock vs. a global clock: a BER comparison

Reference: [2]

Abstract – We compare experimentally the BER performance of a 2D λ-t OCDMA system with optimum sampling (global clock) and non-optimum sampling (recovered clock from an OCDMA receiver). We quantify the power and BER penalties of the receiver, and also determine the impact of interferers on its performance.

3.2.1 Introduction

The theoretical performance of networks based on optical code-division multiple-access (OCDMA) has been studied extensively. A number of OCDMA systems have been demonstrated experimentally, but they all used a global clock (optimum sampling) to perform bit error rate (BER) measurements [10], [14]. Any practical OCDMA system will require clock and data recovery (CDR). The OCDMA receiver reported in [1] performs CDR on OCDMA data and converts the OCDMA signal to an NRZ signal, thus enabling interoperability with standard digital circuits. In this letter, we extend these previous results by comparing experimentally the BER performance of an OCDMA system with optimum sampling (global clock) and non-optimum sampling (recovered clock). We performed BER measurements on a 4-user 2D λ-t OCDMA system, quantifying not only the power and BER penalties of the OCDMA receiver, but also determining the impact of interferers on the receiver performance. These results will help refine theoretical models of OCDMA systems, and provide input for establishing realistic power budgets.

3.2.2 System

The OCDMA system test bed is described in detail in [14]; the main parameters are listed in Table 3.3 and the block diagram is shown in Fig. 3.5. A broadband incoherent signal is passed through an electro-absorption modulator driven by a 2^{15}-1 PRBS RZ signal. The single train of optical pulses is amplified by an EDFA before being split and sent to four encoders, each with a delay line sufficiently long to decorrelate the pulses.

The encoders are fibre Bragg gratings (FBGs) written in series, whose passbands and physical position on the fibre determine the 2D λ-t codes. The OCDMA signals are recombined and amplified by an EDFA before entering the decoder for the desired user. A photodiode, followed by a 933 MHz Bessel-Thompson filter, converts the decoded signal to an electrical signal. In the global clock case, the BER tester (BERT) is triggered by the transmitter's clock. In the recovered clock case, the clock and data recovery unit is inserted after the electrical filter and the recovered clock and data are used as inputs to the BERT.

Table 3.3
System parameters

Parameter	Value
Code length	29
Code weight	8
Channel spacing	50 GHz
Each optical wavelength bandwidth	20 GHz
Data rate	155.52 Mbps (OC-3)
Chip rate	1.24416 Gbps (OC-24)

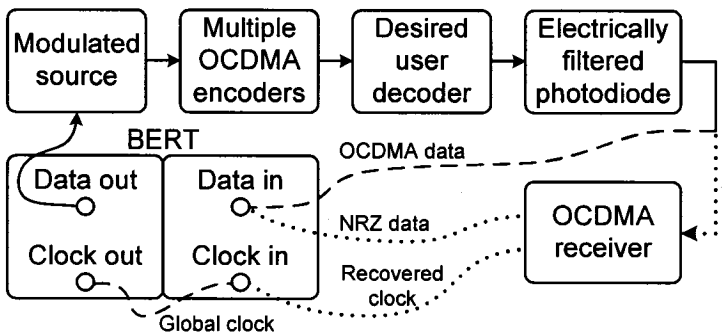


Fig. 3.5. Block diagram of the experimental setup. The dashed and dotted lines show the connections for the global and recovered clock configurations, respectively.

BER measurements were made for up to 4 simultaneous users: the desired user and 3 interferers. The 3 interferers each share 2 common wavelengths with the desired user (the other wavelengths are filtered out by the decoder). For the first interferer, both wavelengths appear under the auto-correlation peak (or inside the detection window) of

the desired user [Fig. 3.6(b)] – this represents a worst case interferer. For the other two interferers, only one of the two wavelengths appears inside the detection window [Figs. 3.6(c)-(d)].

3.2.3 Clock and data recovery

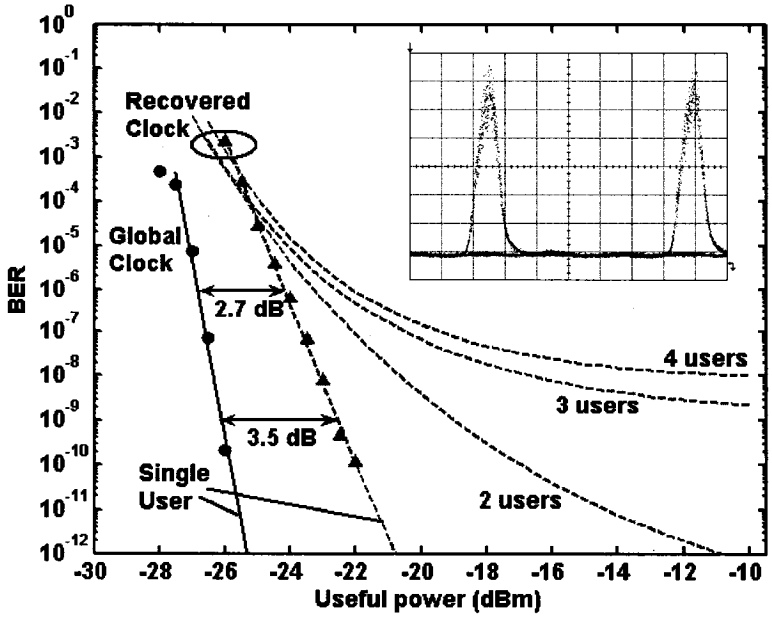
As described in [1], the CDR is made of four building blocks: a quantizer, an OC-48 SONET CDR, a 1:16 deserializer, and a controller. The quantizer filters out multi-access interference (MAI) by thresholding the incoming OCDMA data, both inside and outside the detection window. In the global clock case, only the MAI falling inside the detection window affects the system performance; MAI falling outside the detection window is filtered out by the global clock sampling at the bit rate. As the OCDMA receiver has no a priori information on where sampling should occur, the quantizer must eliminate the energy outside the detection window to help the CDR lock on the correct data edges. MAI outside the detection window and above the quantizer threshold creates spurious edges and usually prevents the CDR from locking.

The CDR recovers the clock at twice the chip rate (2.48832 Gb/s) in order to accommodate the 1:16 deserializer (2.48832 Gb/s/16 = 155.52 M/ps). Each OCDMA auto-correlation peak is therefore sampled twice in this configuration. Using the thresholded signal and the recovered clock, the 1:16 deserializer performs an RZ to NRZ conversion and divides the clock frequency by 16. The deserializer outputs NRZ data at the bit rate, together with its associated clock. When the link is first established, the controller sends realignment/reframing signals to the deserializer to steer the data to the correct output port.

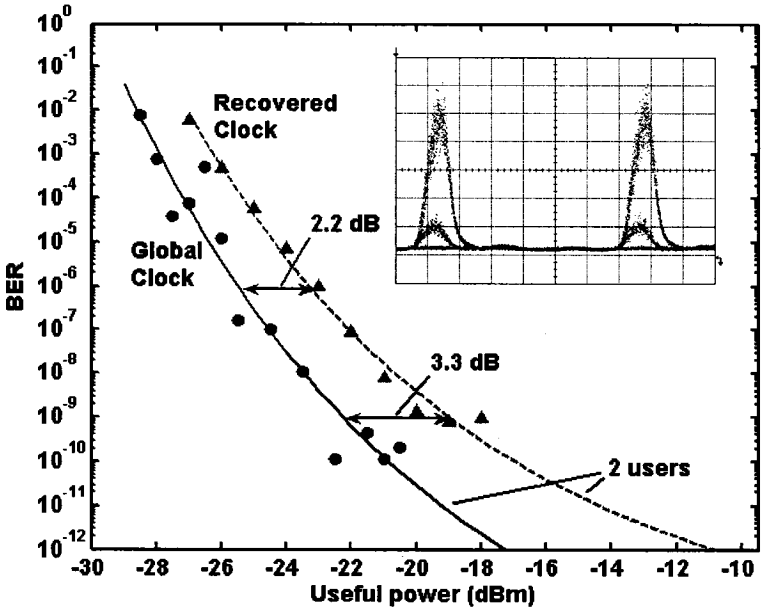
3.2.4 Results and discussion

The performance of the OCDMA system with global clock (solid curves) and recovered clock (dashed curves) is shown in Figs. 3.6(a)-(d). Each figure presents the power penalty of the receiver for a different case (1, 2, 3, or 4 users). Note that the abscissa is the useful power, i.e., the optical power contributed by the desired user at the photodiode. Oscilloscope traces of the OCDMA signal, after O/E conversion and

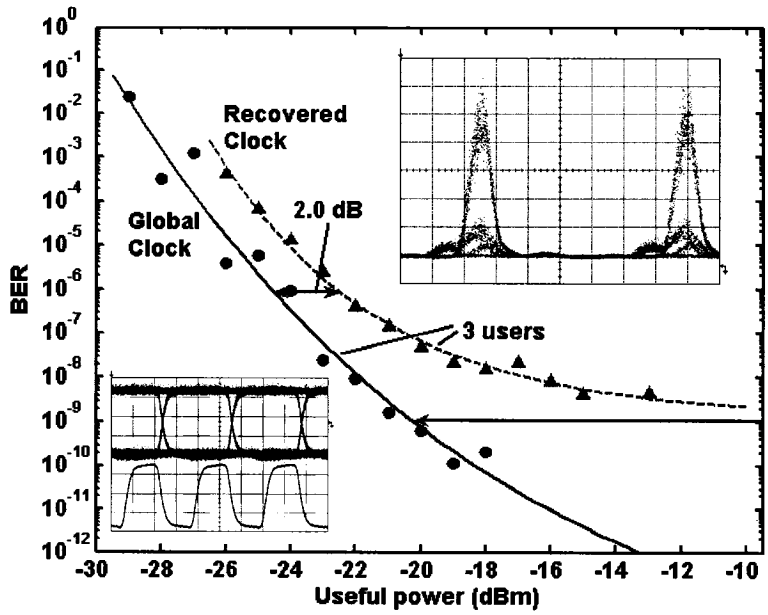
filtering, are shown as insets in each figure. The bottom left inset in Fig. 3.6(c) shows the OCDMA receiver outputs (clock and data).



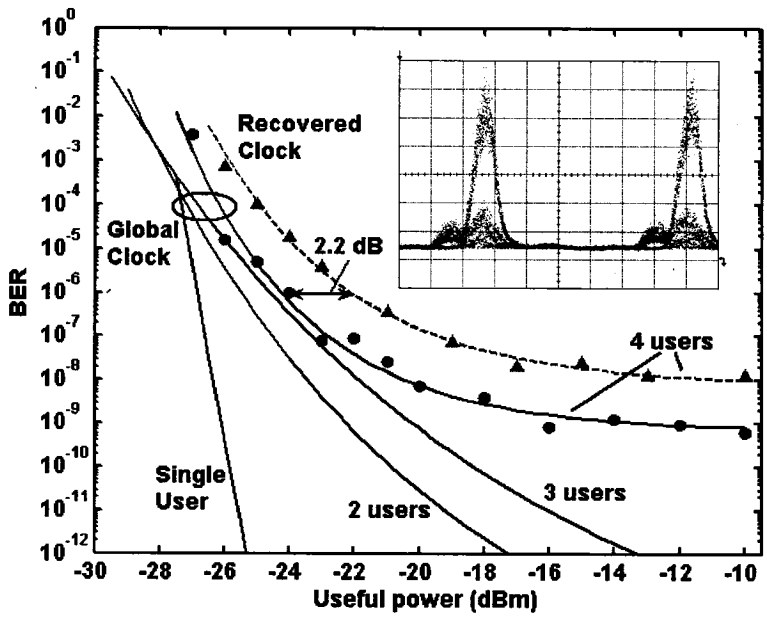
(a)



(b)



(c)



(d)

Fig. 3.6. BER performance of a 4-user OCDMA system with global clock (solid curves) and recovered clock (dashed curves); markers represent measurements, curves are fitted. Insets are oscilloscope traces for (a) 1 user, (b) 2 users, (c) 3 users, and (d) 4 users.

For the single user case [Fig. 3.6(a)], the power penalty due to clock extraction is 2.7 dB (BER ~ 10^{-6}) or 3.5 dB (BER ~ 10^{-9}). As users are added on the network, the power penalty stays relatively constant. For a BER of 10^{-6}, there is a power penalty difference of

0.7 dB between the worst case and the best case. For a BER of 10^{-9}, the power penalty difference between the 1 and 2 user cases is 0.2 dB. We could not measure power penalties for the 3 and 4 user cases due to BER floors, which were observed with three or more users in the recovered clock case, and after the fourth user in the global clock case. The BER floors are mainly due to the intensity noise of the source [15]. For all cases with no BER floor, we obtained error free operation for over one minute at 155.52 M/ps (BER $< 10^{-10}$).

Another way of assessing the performance of the receiver is to measure the power penalty due to interferers. In the global clock case [Fig. 3.6(d)], the addition of 1, 2, and 3 interferers causes power penalties of 1.3, 2.2, and 2.6 dB, respectively (BER ~ 10^{-6}). In the recovered clock case [Fig. 3.6(a)], the power penalties are 0.9, 1.6, and 2.1 dB, respectively (BER ~ 10^{-6}). These numbers suggest that the addition of interferers causes similar power penalties for the global and recovered clock cases.

3.2.5 Conclusion

We have found that practical CDR for λ-t OCDMA provides an acceptable BER penalty as compared to optimum sampling with a global clock. Moreover, our results show that MAI (the major source of impairment in OCDMA) is not detrimental to practical CDR. Performance could be enhanced by including a windowing function over the auto-correlation peaks, effectively filtering out MAI outside the detection window and thereby facilitating CDR. This is the subject of future work.

3.3 OCDMA receiver with FEC

Reference: [3]

Abstract – We demonstrate experimentally for the first time the impact of forward-error correction (FEC) on the performance of two-dimensional (2D) wavelength-time (λ-t) optical code-division multiple-access (OCDMA) with no global clock. A standalone receiver with clock recovery and (255, 239) Reed-Solomon decoding more than doubles the number of supported users at a BER < 10^{-10}. The receiver supports an information rate of 156.25 Mb/s. The measurements were performed at a bit rate of 167.4 Mb/s and a chip rate of 1.339 Gb/s (8 chips per bit), respectively, to account for FEC overhead. At a BER of 10^{-9}, the coding gain is approximately 3 dB for the one and two-user cases.

3.3.1 Introduction

The attractions of code division multiplexing lie in the asynchronous, completely decentralized and uncoordinated transmissions among users. Bit rates considered moderate by optical standards (155 Mb/s and 622 Mb/s) are more than sufficient to meet the requirements for video and data delivery for the first generation of fiber to the home (FTTH). The soft capacity of a code-division multiple-access (CDMA) system permits growing the client base beyond the nominal maximum capacity (while accepting some quality of service degradation) without extensive upgrades to the infrastructure.

Practical considerations such as imperfect clock recovery and the efficiency of forward error correction (FEC) are required to give system designers accurate estimates of the quality of service guarantees that can be delivered, while still providing margin for exploiting the soft capacity. Note that TDMA systems proposed for current passive optical networks standards have hard capacity, and they require infrastructure upgrades to expand the client base.

In [16], FEC was used in a coherent optical CDMA (OCDMA) system, whereas in [17] FEC was used in a spectral amplitude coding OCDMA system. In this paper, we present FEC for a two-dimensional (2D) wavelength-time (λ-t) OCDMA system. Moreover, we present for the first time a complete, standalone OCDMA receiver that includes a quantizer to eliminate multiple access interference (MAI), a clock and data

recovery (CDR) unit, and a FEC module. We address how soft capacity can be increased with the use of FEC while working with a recovered clock that provides practical, non-ideal sampling.

3.3.2 OCDMA system

The OCDMA test bed is presented in Fig. 3.7(a). The desired information rate was 156.25 Mb/s. Since we used 8 chips per bit and a Reed-Solomon (RS) code introducing 15/14 of overhead [RS(255, 239)], we used a chip rate and a bit rate of 1.339 Gchip/s and 167.4 Mb/s, respectively. A broadband erbium doped fiber source is modulated by a polarization insensitive electro-absorption modulator. The modulating signal is a 2^{15}-1 pseudorandom binary sequence. The data is FEC-encoded in a return-to-zero (RZ) format. The modulated signal is amplified and sent to the OCDMA encoders through an optical coupler. The encoders are preceded by optical delay lines to de-correlate their data. The OCDMA encoded signals are combined, amplified and sent to decoder 1. The optical power before the photo-detector is controlled with a variable optical attenuator. The output of the photo-detector is low pass filtered by a 4th order Bessel-Thomson filter whose -3 dB cutoff frequency is 0.7 × chip rate, or 933 MHz. Such a filter reduces intensity noise from the incoherent broadband source [18] while keeping inter-symbol interference to a minimum. Bit error rate (BER) measurements were performed on: 1) the RZ data (OCDMA receiver bypassed) sampled with a global clock, and 2) the recovered non-return-to-zero (NRZ) data sampled with the recovered clock. In the second case, BER measurements were performed with and without RS decoding to study the impact of FEC.

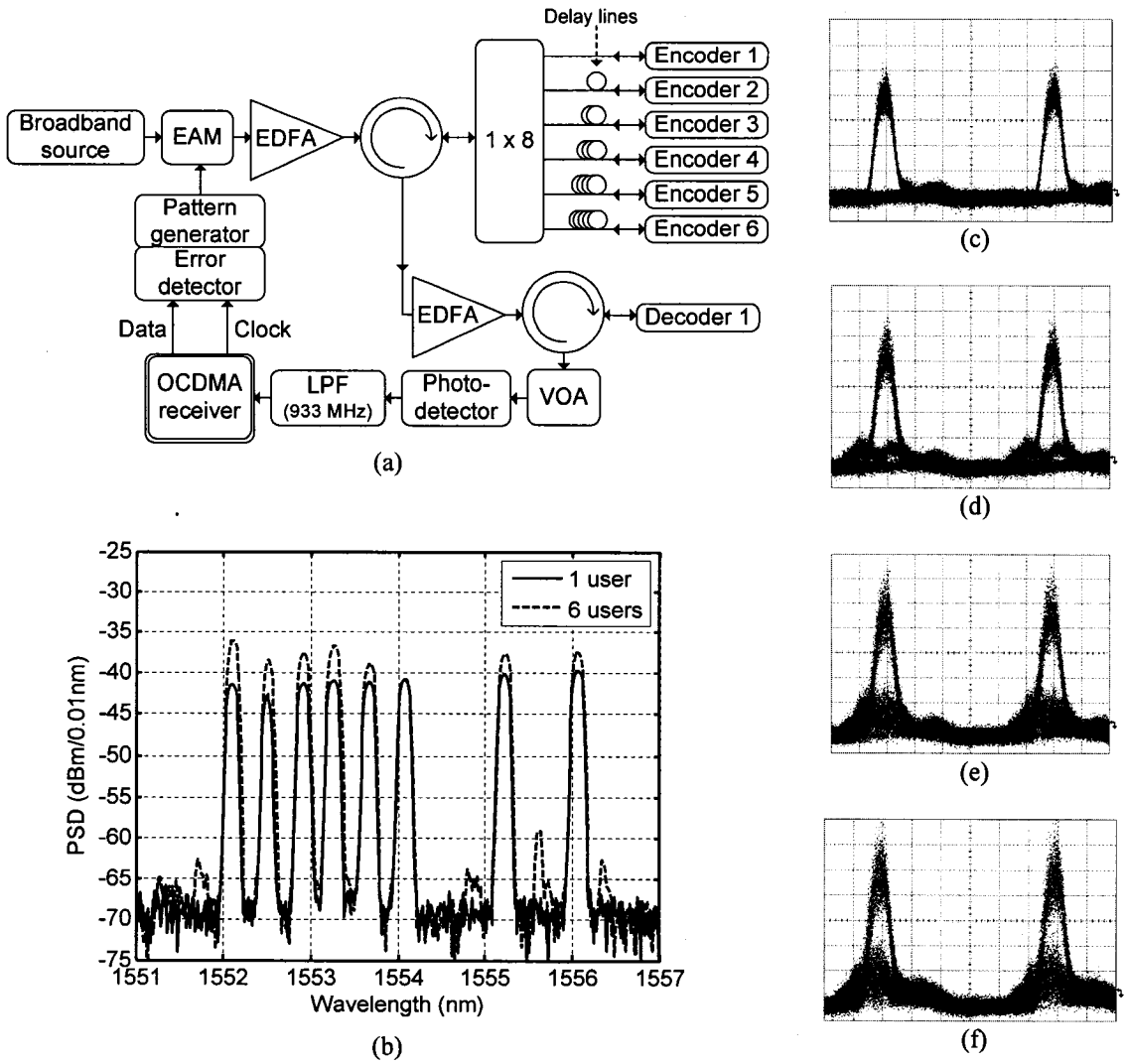


Fig. 3.7. (a) Block diagram of the experimental setup, (b) optical spectrum after decoder 1 for one and six users, and oscilloscope traces after the LPF for (c) one user, (d) two users, (e) four users and (f) six users. EAM: electro-absorption modulator, EDFA: erbium doped fiber amplifier, Enc: encoder, Dec: decoder, VOA: variable optical attenuator, LPF: low pass filter.

Fig. 3.7(b) presents the decoded optical spectrum before the photo-detector. The solid line is for user 1 alone while the dashed line is for all six users active. Note that the sixth wavelength of decoder 1 is used only by user 1. All other wavelengths are shared by at least one interferer. Each encoder in the system consists of eight fiber Bragg gratings (FBG) written in series, whose passbands and physical positions in the fiber determine the code. The FBG spectrums are 20 GHz wide and the channel spacing is 50 GHz. Code length and weight are 29 and 8, respectively. Encoder 2 has five common wavelengths

with encoder 1, whereas encoders 3 to 5 have two and encoder 6 has a single wavelength in common. The delays between decoded user 1 and the five interferers are adjusted such that interfering wavelengths appear within the autocorrelation peak of user 1 [Figs. 3.7(c)-(f)]. This corresponds to a worst case scenario, thus allowing testing of the OCDMA receiver under severe conditions. The codes for encoders 1 to 6 are given in [14], in which they are labeled respectively as K, O, I, G, H, and C.

3.3.3 OCDMA receiver

The OCDMA receiver that we used in our experiments is shown in Fig. 3.8. The blocks outside of the dotted area correspond to the receiver that was used in [1], [2]. The quantizer (Q) applies a threshold on the incoming data in order to filter out MAI. The CDR recovers the clock at the chip rate for optimum sampling. In [1], [2], the deserializer was used for RZ to NRZ conversion, whereas here it is used to reduce the frequency of the data for further processing by digital logic. The blocks inside the dotted area, which were implemented on a Virtex II Pro FPGA from Xilinx, enhance the OCDMA receiver described in [1], [2] with automatic detection of the payload chips and RS(255, 239) decoding. The RZ to NRZ converter determines the index (0 to 7) of the payload chips. This process happens quickly after reset. Once the RZ to NRZ converter has identified the payload index, it remains locked on that index until the receiver is reset again. Only the payload chips make it through the RZ to NRZ converter, therefore dividing down the parallel data rate by eight. Hence, the operating frequency of the comma detector, the framer, and the decoder is around 21 MHz (1.339 GHz/8/8). This frequency is easily supported by most FPGAs. Upon reset, the comma detector looks for a preprogrammed comma – a unique 16-bit character. The framer uses the comma to realign the data. The realigned data is then sent to the RS decoder, which either outputs decoded or undecoded data as selected by the operator. The 8:1 serializer finally performs a parallel-to-serial conversion to output NRZ data at 167.4 Mb/s (chip rate/number of chips per bit).

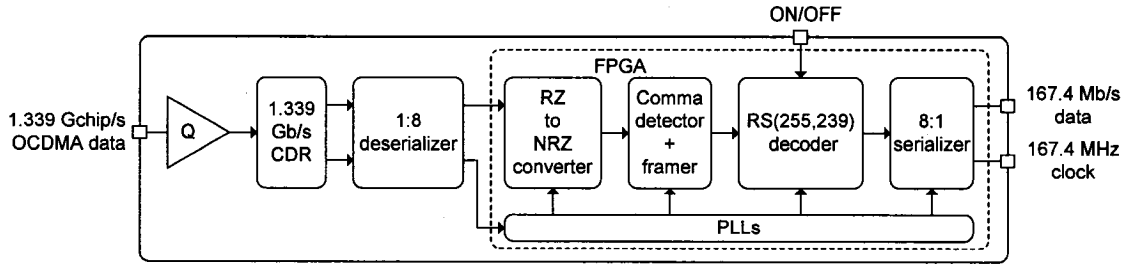


Fig. 3.8. Block diagram of the OCDMA receiver. The blocks within the dotted area were implemented on an FPGA. Q: quantizer, RZ: return-to-zero, NRZ: non-return-to-zero, RS: Reed-Solomon, PLL: phase-locked loop.

3.3.4 Results and discussion

The performance of the OCDMA system with the global clock (solid curves) and the recovered clock (dashed curves) is shown in Fig. 3.9(a). The results were obtained with worst-case MAI and no FEC. Note that the abscissa is the useful power, i.e., the optical power contributed by the desired user at the photodiode. When sampling with the recovered clock, we observe no appreciable power penalty compared to the global clock case. This result is an improvement over the result obtained in [2] where a power penalty of 3.3 to 3.5 dB was measured at a BER of 10^{-9}. The improvement is due to a sampling optimization. In this work, the CDR operates at the chip rate; in [2], the CDR was operating at twice the chip rate due to the unavailability of a 1:8 deserializer for RZ to NRZ conversion. The chips were therefore sampled on each side of the optimum sampling point, explaining the power penalty.

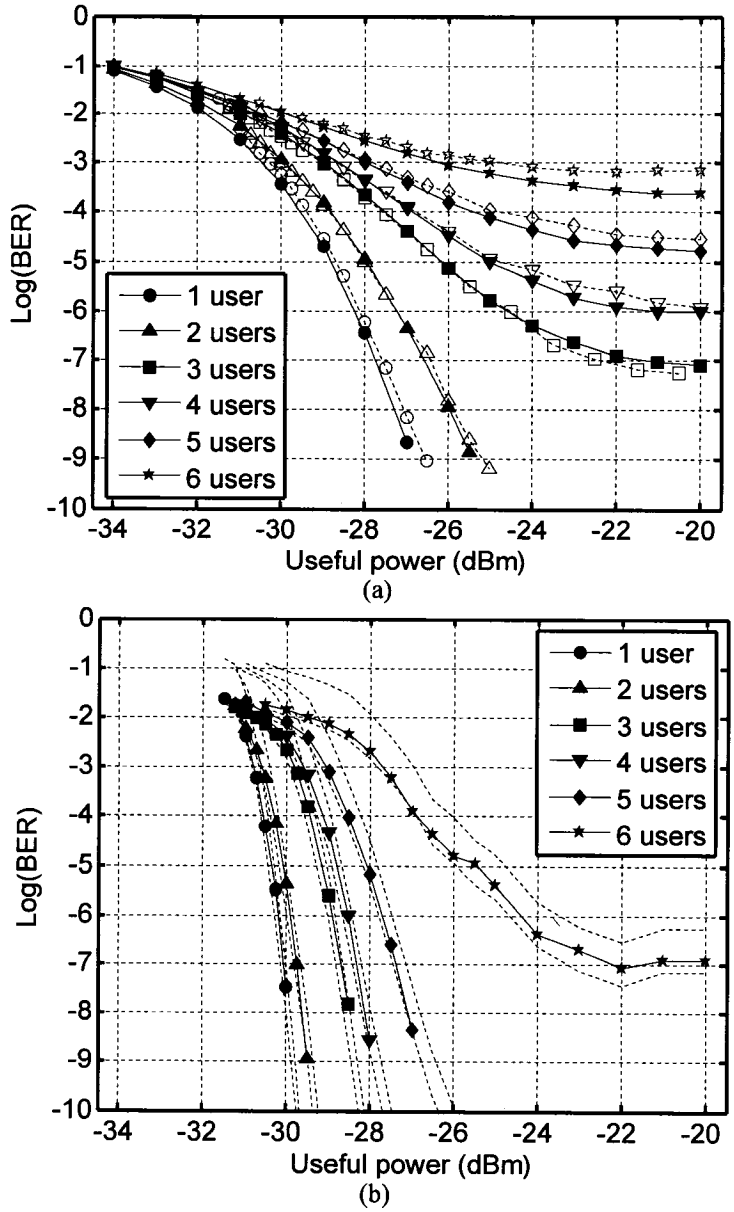


Fig. 3.9. BER performance of a 6-user OCDMA system. (a) BER with the global clock (solid curves) and the recovered clock (dashed curves), no FEC. (b) Experimental (solid curves) and theoretical (dashed curves) BER with the recovered clock and FEC. For all cases with no BER floor, we obtained error free operation for over one minute at 156.25 Mb/s (BER < 10^{-10}).

Fig. 3.9(b) shows the BER with FEC enabled. The system can support five users simultaneously in the detection window without error (compared to two users when FEC is disabled). The BER floor is eliminated for the three, four and five user cases. At a BER of 10^{-9}, the coding gain for the one and two-user cases is roughly 3 dB, as predicted by theory. The theoretical results were calculated with [19]

$$P_{S\_FEC} \approx \frac{1}{2^m - 1} \sum_{j=t+1}^{2^m-1} j \binom{2^m - 1}{j} P_S^j (1 - P_S)^{2^m - 1 - j} \tag{3.1}$$

where P_{S_FEC} and P_S are the symbol error probabilities after and before decoding, respectively, m is the number of bits per symbol (8 in this case), and t is the error correction capability of the RS(255, 239) code. Under the assumption of purely random bit errors,

$$P_S = 1 - (1 - P_B)^m \tag{3.2}$$

where P_B is the channel BER without FEC as measured in Fig. 3.9(a) for the recovered clock case. Finally, the upper and lower bounds in Fig. 3.9(b) are calculated using (3.1) and

$$P_{B\_FEC} = P_{S\_FEC} \times n/m \tag{3.3}$$

where n takes a value of 8 or 1 errors/symbol for the upper and lower bounds, respectively. As we can see in Fig. 3.9(b), the experimental results lie within the upper and lower bounds. The agreement between experimental and theoretical results allows us to draw the conclusion that the errors are statistically independent in our 2D λ-t OCDMA network, without having to introduce an interleaver.

3.3.5 Conclusion

We demonstrated experimentally that FEC can improve the soft-capacity of a 2D λ-t OCDMA network. No global clock was used in the system. Instead, we used a standalone OCDMA receiver with CDR, automatic detection of the payload chips, and RS decoding. In addition to filtering out MAI and recovering the clock, the receiver eliminated a BER floor and increased the number of simultaneous users in the detection window from two to five.

3.3.6 Notes

In Section 3.3.4, we reported a coding gain of 3 dB whereas ~6 dB is frequently quoted for the RS(255, 239) code. We explain the 3 dB difference in this section. First, the coding gain that we reported was for a BER of 10^{-9}, whereas the value of 6 dB is for a BER of 10^{-15}. As we can see in Fig. 3.10, the net coding gain decreases as the reference

BER decreases. The blue curve, which represents an un-coded channel, was plotted using [20]

$$BER(q) = erfc\left(\frac{q}{\sqrt{2}}\right) \tag{3.4}$$

where q is the electrical signal-to-noise ratio (SNR) at the input of the receiver. The Q-factor is simply $20log(q)$. The red curve was plotted using (3.1)-(3.3) and assuming the standard G.709 RS(255, 239) FEC algorithm [21]. Note that P_B in (3.2) is calculated using (3.4). The purple curve is a right-shifted version of the red curve. The 0.28 dB coding loss is to account for the 6.7% increase in bit rate when using FEC [20]. The net electrical coding gain (NECG) is the difference, in dB, between the coding gain (blue – red) and the coding loss (purple – red) at a given BER.

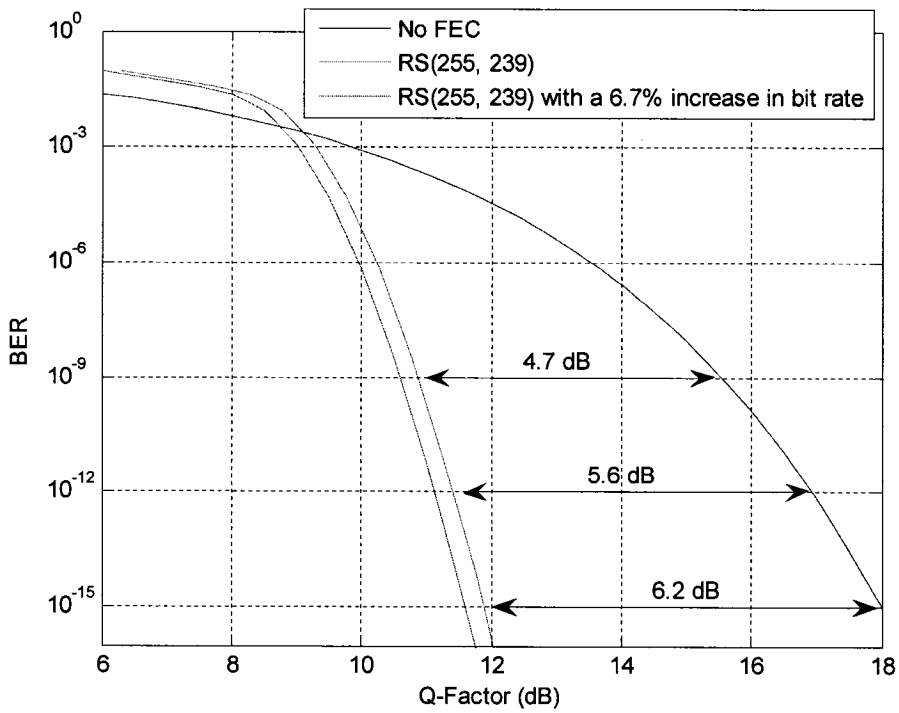


Fig. 3.10. BER versus Q-factor for three different channel conditions (see legend).

In Fig. 3.10, we read a theoretical NECG of 4.7 dB at 10^{-9}. This value is still 1.7 dB higher than the value of 3 dB that we reported in Section 3.3.4. To explain the difference, we must compare the x-axis of Figs. 3.9(b) and 3.10. In one case, the coding gain is

calculated by taking the difference between two received optical powers, whereas in the other case it is calculated in terms of electrical SNR. The coding gain difference could therefore be attributed to the type of receiver that we used in our experiment (a PIN-based receiver). Receivers using an avalanche photodiodes (APDs) provide optical amplification and are generally shot noise limited. In this case, BER vs. optical power curves will be similar to BER vs. electrical SNR curves. Receivers using a PIN detector do not provide optical amplification and are usually thermal noise limited. In this case, the optical coding gain will be a certain fraction of the electrical coding gain.

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CHAPTER 4

Burst-mode clock and data recovery

This chapter consists of two journal articles on BM-CDRs [1], [3] and a section on component integration. Each CDR uses a different technique to achieve fast phase acquisition. In one case [1], we used a large closed-loop bandwidth to accelerate settling time. In the second case [3], we used over sampling and a novel phase picking algorithm to achieve instantaneous phase acquisition and much improved jitter characteristics.

4.1 Solution 1: Broadband CDR

Reference: [1]

Abstract – Broadband PLLs are proposed for burst-mode clock and data recovery in optical multiaccess networks. Design parameters for a charge-pump PLL-based CDR with fast phase acquisition are derived using a time-domain model that does not assume narrow loop bandwidth or small phase errors. Implementation in a half-rate CDR circuit confirms a clock phase acquisition time of 40 *ns*, or 100 bits at 2.488 Gb/s rate, and data recovery at 1.244 Gb/s rate with a BER of $1x10^{-10}$ (2^{14}-1 PRBS with Manchester-encoding). The CDR was fabricated in CMOS 0.18-μm technology in an area of 1×1 mm^2 and consumes 54 mW of power from a 1.8 V supply.

4.1.1 Introduction

Demands for broadband access are predicted to exceed the potential of modern networks. Optical multiaccess networks based on an all-optical core, such as PON, have been proposed to enable services such as IP telephony and video on demand in metro and access areas [5], [6]. Technologies focusing on this all-optical core are already mature [7]. However, novel electronics are also required to support new functionalities at the network edges. Specifically, optical receivers must be adapted to deal with burst-mode traffic,

where data bursts originate from various sources and travel different distances due to the point-to-multipoint nature of the network. The amplitude and phase of successive packets may therefore vary anywhere between 0-20 dB and $-\pi$ to $+\pi$ rad, respectively [8]. Receivers with the following characteristics are therefore necessary: wide dynamic range, fast automatic threshold control (ATC), and fast phase acquisition, where ATC and phase acquisition must occur within ns to support short packet lengths at Gigabit rates. Burst-mode receiver front-ends have already been demonstrated with wide dynamic range and fast ATC [9]. This work focuses on the fast phase acquisition requirement. Whereas previous works have considered correlation algorithms [10] and gated oscillators [11] to decrease phase acquisition time in clock and data recovery (CDR), this work investigates the use of broadband phase locked loops (PLLs). While it is known that increasing the bandwidth of a PLL can tradeoff jitter performance in favor of phase/frequency acquisition time [12], this work addresses practical issues in applying this concept to burst-mode CDR. We demonstrate successful implementation of a burst-mode broadband PLL CDR through modeling and experimentation, and quantify the resulting tradeoff on line coding. In particular, the phase acquisition time of a broadband PLL CDR is measured and the effect of various coding schemes on the phase noise of the recovered clock is tested. The next section discusses the advantages and tradeoffs of broadband PLL CDRs. Section III describes modeling and implementation, while Section IV describes the experimental results.

4.1.2 The broadband PLL CDR

SONET CDRs are specified with a narrow PLL bandwidth in order to minimize jitter accumulation through long repeater chains in long-haul networks [13]. This is because narrowband PLLs are highly resistant to phase variations which cause jitter. However, this optimizes SONET CDRs for suppression of data jitter at the expense of other abilities: suppression of internal jitter from the voltage-controlled oscillator (VCO), frequency capture range, and phase/frequency acquisition time. This last tradeoff is central to the discussion. A narrowband PLL's resistance to phase variations implies a slow acquisition time to steps in the incoming phase. The phase acquisition time of a commercially available SONET OC-48 CDR was previously measured at 1400 bits ($\pm\pi$ rad phase steps) [4], which translates to μs at gigabit rates. In contrast to SONET

networks, optical multiaccess networks are typically deployed in metropolitan areas where few or no repeaters are necessary. This opens the possibility of relaxing the restriction on the PLL's loop bandwidth.

We therefore consider a broadband PLL CDR to achieve fast phase acquisition in optical multiaccess networks. Specifically, we modify the PLL parameters in a SONET CDR to increase loop bandwidth until a target phase acquisition time is obtained. Theoretically, this has the added benefits of increasing the CDR's frequency capture range and suppression of internal jitter, as the PLL behaves as a high-pass filter for jitter generated by the VCO [12]. However, as PLLs are unable to distinguish a true phase-step from cycle-to-cycle data jitter, increasing the loop bandwidth simultaneously increases the jitter transfer bandwidth. Also, broadband PLLs are more prone to clock drift when receiving data with low transition-density, making line coding necessary to eliminate low frequency components. Therefore, the tradeoffs are reduced suppression of data jitter and a strong requirement for line coding. We quantify these tradeoffs below.

4.1.3 Modeling and implementation

Although they are of higher order and complexity, charge-pump PLL-based CDRs are often simplified to 2^{nd}-order models used in the frequency-domain. However, their accuracy relies heavily upon two assumptions [14]: 1) The instantaneous phase error (φ_e) between the input and the recovered clock is small, which restricts the model to cases where the system does not deviate far from steady-state, and 2) The loop bandwidth (K) is a small fraction of the input frequency ($>> 10 \cdot K$ [14]), which allows a continuous-time approximation of the loop's behavior where digital switching granularity is ignored in favour of the average behavior over many cycles. The two assumptions produce a linear baseband model of charge-pump PLLs to facilitate analysis. However, these assumptions do not apply in the present case. Another consideration is that stability becomes an issue as a PLL's bandwidth is increased. This is especially true for charge-pump PLLs, which are time-variant due to the discontinuous sampling operation [14]. A more reliable model is therefore necessary for this application, particularly when modeling responses to large phase steps.

An alternative mathematical model for charge-pump PLLs was proposed in [14], [15]. The model is based on a system of nonlinear difference equations that account for the highly nonlinear nature of PLLs directly in the time-domain. It therefore places no restrictions on K or φ_e to produce transient responses to phase steps. The model was used here to derive component values which achieve fast phase acquisition in a half-rate CDR architecture intended for SONET [12] (Fig. 4.1). Specifically, parameters for a 2nd-order loop filter (R_1, C_1, C_2,) and linear gains for the phase detector (K_{PD} [V/rad]), charge-pump (g_m [A/V]), and VCO (K_{VCO} [Hz/V]) were derived for a target clock frequency of 1.244 GHz (Table 4.1).

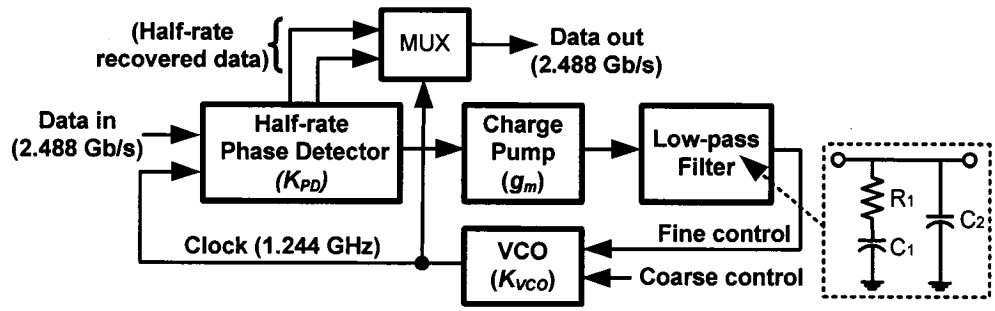


Fig. 4.1. Half-rate CDR architecture [12], targeting a 2.488 Gb/s bit rate.

Table 4.1
Circuit design parameters obtained from simulation

Parameter	Value
R_1	5 KΩ
C_1, C_2	2.5 pF, 300 fF
K_{PD}	25 mV/rad
g_m	400 μA/V
K_{VCO}	2.0 GHz/V
I_P (= $K_{PD} \cdot g_m$)	10 μA/rad

Fig. 4.2 shows the resulting transient responses (VCO control voltage) to phase steps within the range [0, ±π/2] rad, which were generated using the model. Note that the input is a periodic signal resembling a burst preamble and that frequency-lock is assumed as an initial condition. Stability is verified over all simulated phase steps. In all cases, the CDR requires 40 *ns* to settle to within approximately 10% of the steady-state value,

corresponding to 100 bits at 2.488 Gb/s data rate. In comparison, [12] exhibited a 350 *ns* lock time. To quantify the jitter tradeoff, the analysis and equations from chapter 5 of [12] were used to derive the loop bandwidth and jitter peaking resulting from the design parameters of Table 4.1. K was calculated to be 5.78×10^8 rad/s, or 92 MHz, while jitter peaking was 1.202 dB. These results denote a wider jitter transfer bandwidth and higher peaking than specified in ITU/Bellcore specifications for SONET OC-48 (2 MHz and 0.1 dB, respectively [13]). This confirms that a broadband PLL CDR has been achieved resulting in a tradeoff in data jitter-suppression abilities. Also, the ratio of clock frequency over K is only ~13.5, indicating that performance assessments from a baseband frequency-domain model would not be reliable [14].

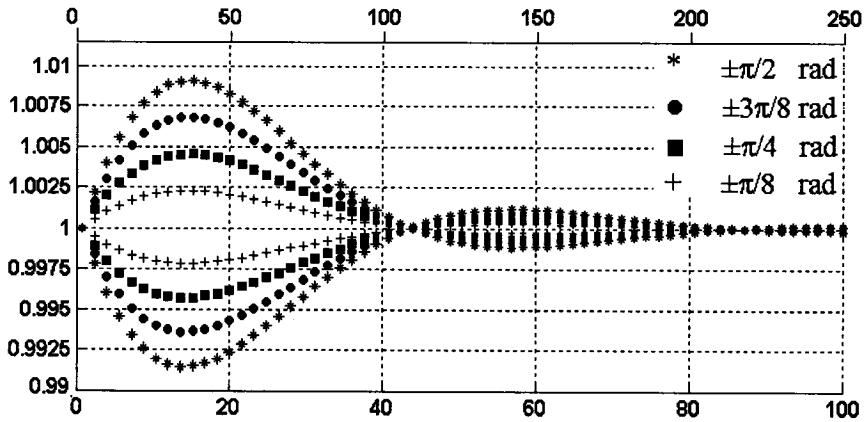


Fig. 4.2. Transient simulation from nonlinear time-domain model of VCO control voltage with respect to time and # bits of incoming data (2.488 Gb/s) in response to phase steps of ±π/8, ±π/4, ±3π/8, and ±π/2 rad.

The derived PLL parameters were implemented in the CDR architecture from [12], targeting a data rate of 2.488 Gb/s. The architecture is a half-rate CDR which samples data on both the rising and falling edges of the clock. Such architectures use a VCO running at half the data rate to facilitate implementation in CMOS, and offer significant advantages in the proposed application. Following a phase step, the worst case clock realignment is ±π/2 rad, as opposed to ±π rad for a full-rate architecture. Also, each recovered bit occurring on the negative-edge of the clock would not be sampled by subsequent positive-edge triggered systems. Therefore in the case of Manchester-encoded data this would automatically recover the original uncoded data if made to positively trigger on the correct cycle of bits.

The phase detector was implemented using CML logic to reduce switching noise and increase speed. The gains of the implemented phase detector, charge-pump, and VCO were 23.56 mV/rad, 395 μA/V, and 1.93 GHz/V, respectively. In order to observe phase acquisition, the differential control voltage of the VCO was brought off-chip using a buffer, to minimize loading effects, and an amplifier. This added significant power consumption but enabled observation of the internal PLL behavior during transients. 50-Ohm LVDS I/O buffers were used to bring high-speed signals on- and off-chip.

4.1.4 Experimental results

The circuit was fabricated in CMOS 0.18-μm in an area of 1×1 mm^2. The die was packaged in a 24-pin open-cavity ceramic package mounted on a custom designed FR-4 printed circuit board. The measured power consumption was 54 mW from a 1.8 V power supply. The VCO could operate anywhere between 622 MHz and 1.244 GHz using coarse tuning.

The phase acquisition time of the CDR was measured using a repeating 2.488 Gb/s pattern consisting of 32 consecutive zeros, representing a period of non-transmission, followed by a 112-bit "1010..." pattern, representing the preamble of a burst packet. Fig. 4.3 depicts a scope trace of the PLL's response (VCO control voltage). Note that the trace is an amplified version of the control voltage. The periods of non-transmission and preamble are each evident in the trend. During periods of non-transmission, the system is free-running and the phase of the VCO is random with respect to incoming data. The CDR begins locking at the beginning of the preamble and reaches steady-state within approximately 40 *ns*, or 100 bits at 2.488 Gb/s. The trend and timescale of the CDR response are comparable to simulation results (Fig. 4.2), which verifies the accuracy of the PLL model proposed in [15]. It also confirms that a greater than 10-fold improvement in phase acquisition time has been achieved over that of a SONET CDR [4].

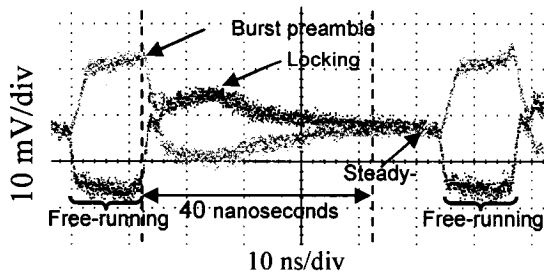
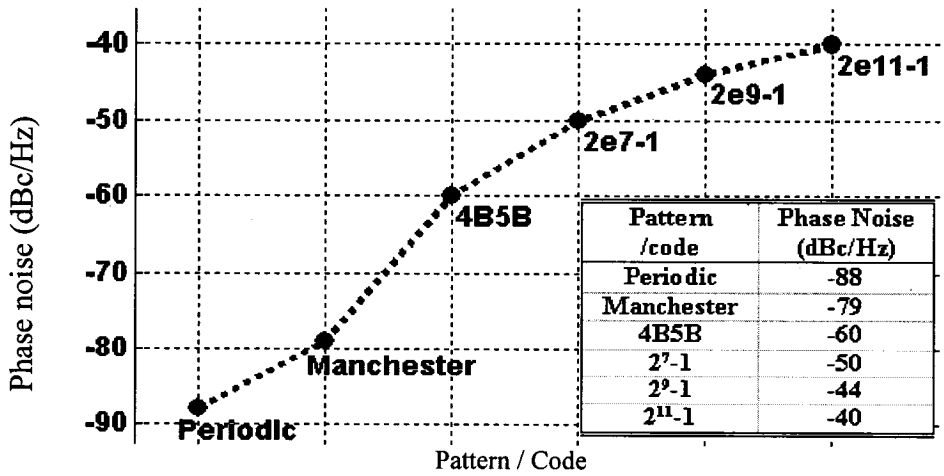


Fig. 4.3. Scope trace of differential VCO control signal from implemented circuit in response to data burst preamble.

The CDR was then tested with various line coding schemes. As expected, a strong dependence on transition density was observed (Fig. 4.4). Only Manchester-encoding resulted in a recovered clock of sufficient quality for BER testing. Manchester-encoded PRBS patterns of length 2^7-1, 2^{11}-1, and 2^{14}-1 were used to make BER measurements. Error free data recovery could not be achieved at 2.488 Gb/s due to poor performance of the data output buffers, which resulted in attenuation. The CDR was therefore tested at 1.244 Gb/s with a recovered half-rate clock of 622 MHz. This produced a baud rate of 1.244 Gb/s and an effective recovered bit rate of 622 Mb/s due to Manchester-encoding. BER measurements were performed by loading Manchester-encoded patterns into the pattern generator and the corresponding uncoded patterns into the error detector (ED). This resulted in a BER of 1×10^{-10} for all three patterns. Fig. 4.5 depicts a persistence scope trace of the recovered data. The small vertical eye opening (50 mV) is caused by attenuation by the data output buffers. Fig. 4.6 depicts the recovered clock spectrum for a Manchester-encoded pattern. A phase noise of -79 dBc/Hz was measured at a 1 MHz offset.



Pattern /code	Phase Noise (dBc/Hz)
Periodic	-88
Manchester	-79
4B5B	-60
2^7-1	-50
2^9-1	-44
2^{11}-1	-40

Fig. 4.4. Phase noise measured at 1 MHz offset from peak for various data patterns of decreasing transition density.

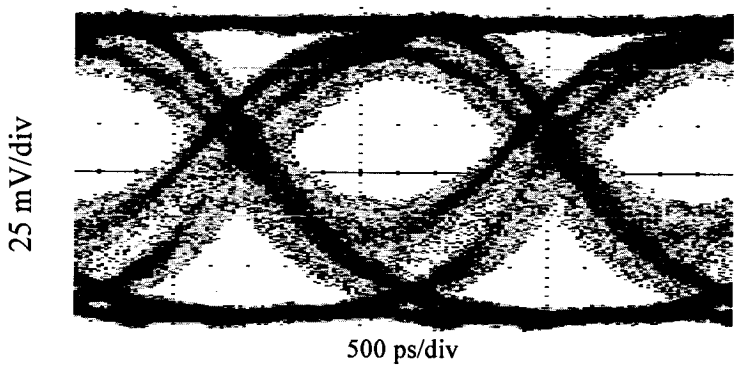


Fig. 4.5. Recovered data eye diagram (20 s persistence).

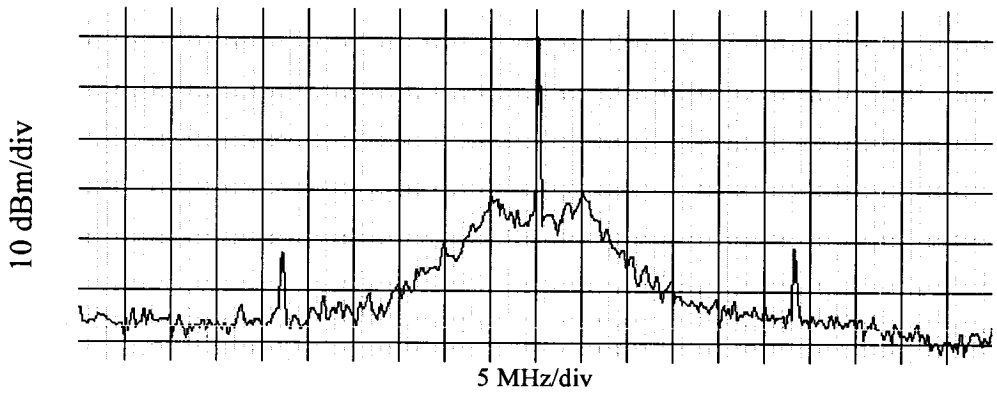


Fig. 4.6. Spectrum of recovered clock, 100MHz span (peak -17dBm at 622MHz).

4.1.5 Conclusion

We have designed a broadband PLL CDR for burst-mode applications. A time-domain model was used to design the CDR. The model was verified experimentally and a phase acquisition time of 100 bits was measured. This represents a greater than 10-fold improvement over corresponding SONET CDRs. Successful CDR was demonstrated and the tradeoff between lock acquisition time and PLL bandwidth resulted in the need for Manchester encoding. This work may be scaled to match the lock time and coding requirements of specific networks.

4.2 Solution 2: Over sampling CDR

Reference: [3]

Abstract – We propose the design of a 622/1244 Mb/s burst-mode clock phase aligner (BM-CPA) for GPON OLT applications using commercially available SONET CDRs operated in 2× over sampling mode. Our measurement results show that the BM-CPA meets the GPON physical media dependent layer specification defined in ITU-T recommendation G.984.2. The CPA provides instantaneous phase acquisition (0 bit) for any phase step (±2π rad) and a BER < 10^{-10}. Our phase picking algorithm exploits the 20-bit delimiter specified in G.984.2. The delimiter is typically used by the digital line termination for byte synchronization, but we demonstrate that it can simultaneously be used by the BM-CPA. The design provides low latency and fast response without requiring a reset signal from the network layer. We verified the design at 625 Mb/s using a 1250 Mb/s commercial CDR. In practice, a 1244.16 Mb/s (OC-24) CDR should be used to support 622.08 Mb/s. Our solution is scalable to 5 Gb/s using an OC-192 SONET CDR. Because the BM-CPA requires no preamble bits, the entire preamble (28 bits at 622.08 Mb/s, 44 bits at 1244.16 Mb/s) can be used to facilitate amplitude recovery and reduce the burst-mode sensitivity penalty. Alternatively, the preamble length can be reduced to increase the information rate.

4.2.1 Introduction

Passive optical networks (PONs) are an emerging access network technology that provides a low-cost method of deploying fiber-to-the-home. PONs are expected to answer the problem of limited bandwidth in the local access network, commonly known as the last mile problem. Fig. 4.7 shows an example of a PON network. In the downstream direction, the network is point-to-point: continuous data is broadcasted from the OLT to the ONUs using time division multiplexing (TDM). The transmit side of the OLT and the receive side of the ONUs can therefore use continuous mode ICs. The challenge in the design of a chip set for PONs comes from the upstream data path. In the upstream direction, the network is point-to-multipoint: using time division multiple access (TDMA), multiple ONUs transmit bursty data to the OLT in the central office. To use the

shared medium effectively, the ONUs require a burst-mode transmitter with a short turn-on/off delay [16]. Because packets can vary in phase and amplitude due to optical path differences, the OLT requires a burst-mode receiver (BM-RX) and a burst-mode clock phase aligner (BM-CPA). Within the OLT, the BM-RX is responsible for amplitude recovery, whereas the BM-CPA is responsible for phase recovery. This paper is about the design of a BM-CPA, which can also be referred to as a BM-CDR.

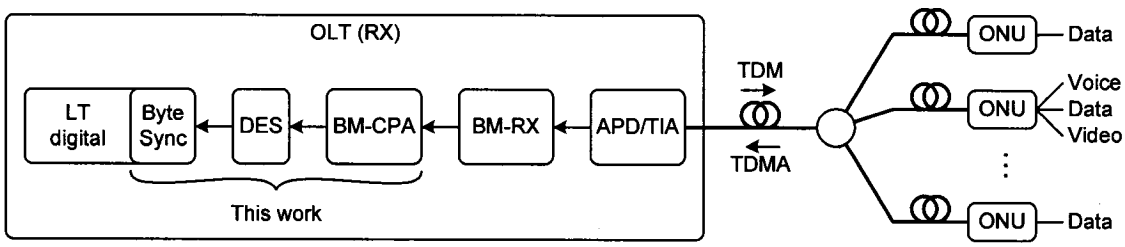


Fig. 4.7. Generic PON network with the BM-CPA put in context. OLT: optical line terminator; RX: receiver; LT: line terminator; DES: 1:16 deserializer; APD: avalanche photodiode; TIA: transimpedance amplifier; TDM: time division multiplexing; TDMA: time division multiple access; ONU: optical network unit.

The most important characteristic of the BM-CPA is its phase acquisition time. Throughout the paper, we will assume that the BM-CPA never lose frequency lock since all ONUs derive their timing from the downstream OLT signal. Different approaches have been proposed to build CDRs with short phase acquisition times. The first approach consists in increasing the bandwidth of a PLL-based CDR to reduce the settling time [1]. The disadvantages include stability issues, jitter peaking, and limited jitter filtering. If additional control logic or a reset signal is acceptable, then one workaround consists in using a dynamic loop bandwidth: the bandwidth is increased while the CDR is acquiring lock and restored to its original value for the rest of the packet to minimize output jitter [17]. The second approach is based on gated oscillators or some kind of gating circuit [18]-[20]. These burst-mode CDRs perform clock phase alignment by triggering the local clock on each transition of the input. Phase acquisition is instantaneous, but this solution is susceptible to pulse distortions and does not filter out input jitter. The last approach is based on over sampling [21]-[23]. One can either over sample in time using a clock frequency higher than the bit rate, or over sample in space using a multiphase clock with a frequency equal to the bit rate. Over sampling in time requires faster electronics,

whereas over sampling in space requires low skew between the multiple phases of the clock. The phase picking algorithm, which selects the best sample, can either be very sophisticated and consume a lot of power, or rely on a simple comparison with a known pattern.

In this work, we use the over sampling (in time) approach and propose a novel phase picking algorithm. We designed a 622/1244 Mb/s BM-CPA using SONET CDRs running at 2× the bit rate (1244/2488 Mb/s). Our solution exploits the design of components for long-haul networks, which are typically a generation ahead of the components for multiaccess networks. The 622.08 Mb/s BM-CPA inherits the low jitter transfer bandwidth (1 MHz) and the low jitter peaking (0.1 dB) of the 1250 Mb/s CDR from which it is built. Similarly, the 1244.16 Mb/s BM-CPA inherits the 2 MHz jitter transfer bandwidth and the 0.1 dB jitter peaking of the 2488.32 Mb/s SONET CDR from which it is built. The end result is a BM-CPA with instantaneous phase acquisition (0 bit) and the very good jitter characteristics of a SONET CDR. Hence, the BM-CPA could also find applications in burst/packet switched networks, which may require a cascade of BM-CPAs that each consumes some of the overall jitter budget of the system.

In Section II, we describe the burst-mode test setup that we used to characterize the BM-CPA. We also provide details on our measurement methodology. We explain the design of the 622/1244 Mb/s BM-CPA in Section III. Note that the 622 Mb/s BM-CPA is actually running at 625 Mb/s – we used a GbE (1250 Mb/s) CDR instead of a 1244.16 Mb/s CDR. The concept nevertheless holds and we will use the 622.08 and 625 Mb/s bit rates interchangeably throughout the paper. The same argument applies to the 1244.16 and 1250 Mb/s bit rates. Finally, we present measurement results in Section IV. Due to the 1 Gb/s bandwidth limitation of the burst-mode test setup, only the 622.08 Mb/s BM-CPA was characterized.

4.2.2 Burst-mode test setup

In order to test the BM-CPA, we had to get around some of the limitations associated with conventional test equipment. For example, the characterization of SONET CDRs does not require the generation of phase steps. This feature is therefore not supported by commercially available pattern generators known to the authors. There is also a problem

with commercial BERTs: they lose pattern synchronization while the sampling clock is being recovered by the CDR. To address these problems, we designed the custom burst-mode test setup (BM-TS) depicted in Fig. 4.8. The BM-TS can go up to 1 Gb/s. This limitation, which comes from the HP80000, explains why the design of the BM-CPA could only be experimentally verified at 622.08 Mb/s.

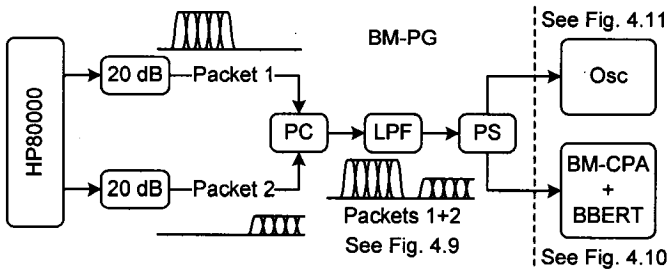


Fig. 4.8. Burst-mode test setup. The burst-mode packet generator is on the left of the dashed line. When testing the phase acquisition time, the two packets are set to have the same amplitude. BM-PG: burst-mode pattern generator; PC: power combiner; LPF: low-pass filter (4th order Bessel-Thomson); PS: power splitter; Osc: oscilloscope; BBERT: burst bit error rate tester.

The BM-TS has two main functionalities. First, it can generate alternating packets with adjustable phase and amplitude to emulate PON traffic. Second, it can perform burst bit error rate (BBER) measurements to determine the amplitude and phase acquisition times and the number of consecutive identical digits (CIDs) supported by the BM-CPA. Each of these two functions will be discussed next.

4.2.2.1 Burst-mode packet generator (BM-PG)

The BM-PG generates the upstream traffic shown in Fig. 4.9. Packet 1 serves as a dummy packet to force the BM-CPA to lock to a certain phase (ϕ_1) before the arrival of packet 2. The amplitude and phase acquisition times are measured on packet 2, which consists of guard bits (16), preamble bits (0 to 2^{15}), delimiter bits (20), payload bits (2^{15}), comma bits (48), and a '1010' pattern that can be circularly shifted in front of the delimiter to increase the preamble length. The guard, preamble, and delimiter bits correspond to the physical-layer upstream burst-mode overhead specified by the G.984.2 standard [24]. The guard bits provide distance between two consecutive packets to avoid collisions. The preamble is used to perform amplitude and phase recovery. The delimiter

is a unique pattern indicating the start of the packet to perform byte synchronization. Likewise, the comma is a unique pattern to indicate the end of the payload. The payload is a 2^{15}-1 PRBS with a zero appended at the end. As discussed in the next section, the packet lost rate (PLR) and the bit error rate (BER) are measured on the payload bits only. The lock acquisition time corresponds to the number of bits that need to be circularly shifted in front of the delimiter in order to get a PLR of zero for over three minutes at 622.08 Mb/s (> 10^6 packets received) and a BER < 10^{-10}.

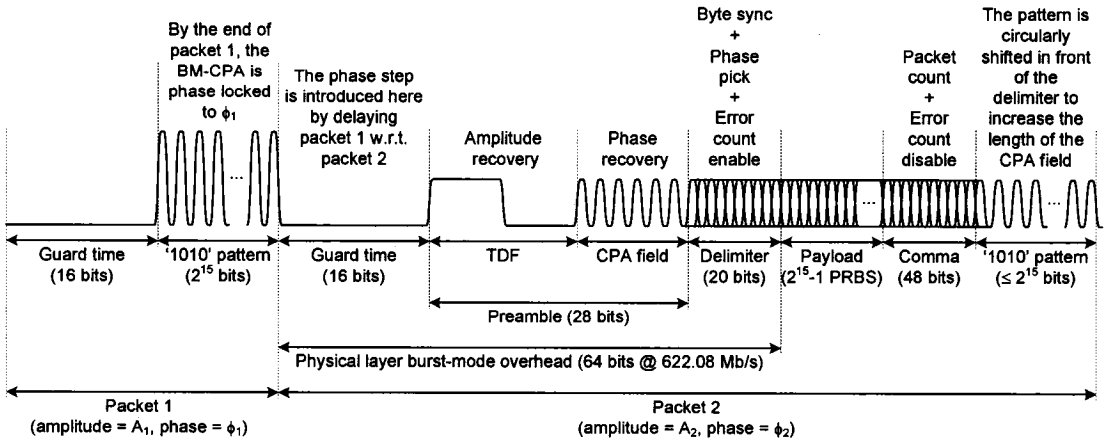


Fig. 4.9. Test signal and specification of the upstream burst-mode overhead at 622.08 Mb/s. When testing the phase acquisition time, the two packets are set to have the same amplitude. TDF: threshold determination field; CPA: clock phase alignment; PRBS: pseudo-random binary sequence.

The G.984.2 standard specifies an overhead length of 8 bytes at 622.08 Mb/s [24]. Hence, a GPON compliant OLT should require a preamble length of no more than 28 bits. The burst-mode test setup nevertheless supports any length between 0 and 2^{15} bits for amplitude and phase acquisition time measurements. As shown in Fig. 4.9, the preamble is split into two fields, a threshold determination field (TDF) for amplitude recovery and a CPA field for clock-phase recovery. As discussed in [26], [27], [28], and [29], a sensitivity penalty results from the quick extraction of the decision threshold and clock phase from a short preamble at the start of each packet. By reducing the length of the CPA field, as is done in this work, more bits are left for amplitude recovery, therefore reducing the burst-mode sensitivity penalty.

In order to generate the pattern of Fig. 4.9, we used two ports of an HP80000 pattern generator (see Fig. 4.8). The two packets are combined on the same line using an RF

power combiner, which emulates the optical power combiner of a PON network (see Fig. 4.7). We used 20-dB attenuators to control the maximum amplitude of the packets and minimize reflections [32]. To test the BM-CPA under stringent conditions, we stressed the input pattern in two different ways. First, we slowed down the edges of the input pattern with a 4th-order Bessel-Thomson filter having a -3-dB bandwidth of 467 MHz (0.75 × 622 MHz) (see the LPF block in Fig. 4.8). Second, we added a random noise generator (not shown in Fig. 4.8) after the filter. The noise generator consists of a transimpedance amplifier (TIA) powered by a supply voltage approximately 1 V lower than the nominal voltage of 3.3 V. The thermal noise generated by the TIA has a Gaussian distribution, which translates into random jitter in the eye diagram shown in Fig. 4.11(a).

In our setup, we can set the amplitude and the relative phase of the packets, the preamble length, and the number of CIDs. The BM-PG can generate a minimum amplitude of 0.4 V and a maximum amplitude of 3.1V. This corresponds to an 18 dB dynamic range, which would not be sufficient to reach the limits of most BM-RX. Although our experiments did not include a BM-RX, we verified that the BBERT described in the next section could accurately measure the dynamic range of a device by performing these measurements on the BM-CPA – note that sensitivity measurements are also possible. The phase step between packets 1 and 2 can be set anywhere between ±2 ns on a 2 ps resolution. This corresponds to ±1.25 UI at 622 Mb/s, and ±2.5 UI at 1244.16 Mb/s. The preamble length and the number of CIDs can be set anywhere between 0 and 2^{15} bits.

4.2.2.2 Burst BER tester (BBERT)

Fig. 4.8 shows the BBERT in the context of the overall BM-TS, whereas Fig. 4.10 shows its implementation details. The BBERT is partly implemented on the FPGA and partly implemented in software. There are a total of 19 counters on the FPGA to keep track of the PLR and the BER. 16 counters are used to count the number of errors in the deserialized data. The three remaining counters keep track of the number of packets received, the number of bits received, and the number of packets lost, respectively. Since divisions are slow and not area efficient in hardware, they are performed 4 times per

second in software. We used Matlab to compute and display the PLR and the BER in real time, and we used HyperTerminal to control and monitor the state of the BM-CPA. Both communicate with the FPGA core through the RS-232 protocol.

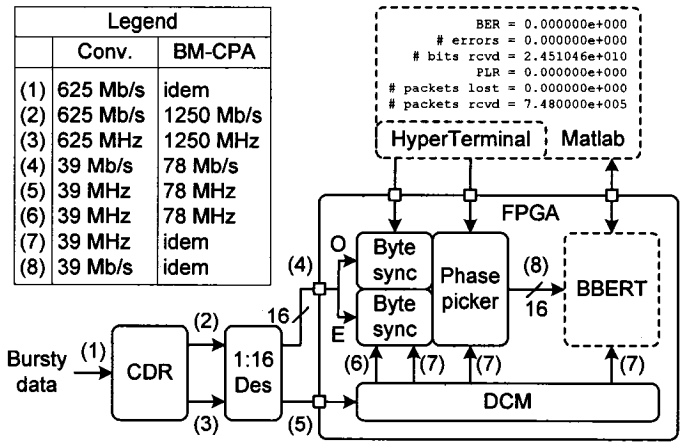


Fig. 4.10. BM-CPA (solid blocks) + BBERT (dashed blocks). The BBERT is partly implemented in hardware (counters) and partly implemented in software (divisions). CDR: clock and data recovery; Des: deserializer; DCM: digital clock manager; BBERT: burst bit error rate tester; O: odd bits (bits 15, 13, 11, ..., 1) of the 16-bit output of the deserializer); E: even bits (bits 14, 12, 10, ..., 0) of the 16-bit output of the deserializer. As shown in Figs. 4.11(g)-(i), odd and even bits are a result of sampling the bursty input at t_{odd} and t_{even} sampling instants, respectively.

In order to selectively perform BBER measurements on the payload of packet 2, we used the delimiter and the comma as gating signals for the 16 error counters. The 16-bit parallel data is compared with the 215-1 PRBS loaded into a memory block of the FPGA. The memory address is incremented each time a new 16-bit vector is clocked in. It is reset to zero when the comma is detected in order to arm the BBERT for the next packet. The packet and packet lost counters are always enabled. Since the comma is far away from the beginning of the packet, it is always detected. Moreover, we used a long comma (48 bits) in order to reduce the probability of getting a false positive. The packet counter is incremented every time a comma is detected. The packet lost counter is incremented when a comma does not pair up with a previously received delimiter. This situation arises when the CDR was not given a preamble long enough to recover the phase before the arrival of the delimiter. When a packet is lost, it does not contribute to the BER. Hence, a zero BER does not mean that there are no errors. Both the PLR and the BER must be monitored while measuring the phase acquisition time.

The novelty of the BBERT proposed herein is that it does not require a fixed synchronization between the incoming pattern and the reference pattern of the error detector. Synchronization happens instantaneously at the beginning of every packet, therefore enabling the measurement of amplitude, frequency, and phase acquisition times on non continuous, bursty data. This is unlike conventional BERTs, which require 1) a continuous alignment between the incoming pattern and the reference pattern, and 2) milliseconds to acquire synchronization. Since the BBERT can measure the amplitude, phase, and frequency acquisition times, it is useful to characterize BM-RXs, BM-CPA, and frequency synthesizers, respectively. Even though the BBERT can perform all three measurements, we concentrate on the phase acquisition time measurement in this paper.

4.2.2.3 Measurement methodology

For a given phase step, we measure the lock acquisition time of the BM-CPA by increasing the length of the preamble until we obtain error free operation, which we define as a PLR of zero for over three minutes at 622.08 Mb/s (> 10^6 packets received) and a BER < 10^{-10}. This method of measuring the phase acquisition time is more accurate than the qualitative method of monitoring the VCO control voltage. In the later case, the phase acquisition time is determined by measuring the settling time of the envelope of the VCO control voltage to within a certain percentage of the steady-state value.

Similarly, we measure the CID immunity of the BM-CPA by zeroing bits at the end of packet 1 until error free operation can no longer be maintained on packet 2. The phase step is set to zero for this measurement.

Finally, to measure the dynamic range, we fix the amplitude of packet 1 and increase or decrease the amplitude of packet 2 until the BM-CPA can no longer maintain error free operation on packet 2. The phase step is set to zero for this measurement also.

4.2.3 Burst-mode CPA

The main building blocks of the BM-CPA are a SONET CDR, a 1:16 deserializer, a byte synchronizer, and a phase picker (see Fig. 4.10). We used evaluations boards for all four of these blocks. The BM-CPA supports three modes of operation: 1) conventional mode, 2) 2× over sampling mode, and 3) burst mode. The conventional mode of operation effectively makes the BM-CPA look like a regular SONET CDR. The 2× over sampling

mode is similar to the burst mode, the only difference being that the phase picker is turned off in the former case. The modes of operation are useful to measure the performance improvement between a regular SONET CDR and a BM-CPA built using that same CDR. We used HyperTerminal to select the mode of operation of the BM-CPA. The three modes will be discussed further while we describe each block of the BM-CPA.

The CDR is from Analog Devices (part #ADN2819). It is a multirate CDR that supports the following frequencies of interest for a 622.08/1244.16 Mb/s BM-CPA: 622.08/1250 Mb/s for the conventional mode and 1250/2488.32 Mb/s for the 2× over sampling and burst modes. The deserializer, rated at 2488.32 Mb/s, is from Maxim-IC (part #MAX3885). Its main function is to reduce the bit rate by parallelizing the data. The parallel data and the divided clock are then brought onto a Virtex II Pro FPGA from Xilinx for further processing. The maximum data rate supported by the LVDS buffers of the FPGA is 840 Mb/s (420 MHz), which is more than the 155.52 MHz clock recovered by the 1244.16 Mb/s BM-CPA (2488.32 MHz/16 = 155.52 MHz). Hence, although the BM-CPA could only be tested at 622.08 Mb/s due to the 1 Gb/s bandwidth limitation of the BM-TS, 1244.16 Mb/s is also supported by the current hardware (CDR, deserializer, and FPGA).

The phase picker and the byte synchronizer are the most important blocks of the BM-CPA. They were implemented on the FPGA, alongside the BBERT (see Fig. 4.10). The 16-bit parallel data and the divided clock are brought onto the FPGA using a high-speed QSE connector from Samtec. Since the outputs of the deserializer and the inputs of the FPGA both use LVDS logic, no conversion other than a connector conversion was needed at the interface between the two.

Our phase picking algorithm is both simple and fast. As was explained in Section II.B, the BBERT uses the delimiter in order to trigger BBER measurements. The byte synchronizer is responsible for detecting the delimiter. The idea behind the phase picking algorithm is to replicate the byte synchronizer twice in an attempt to detect the delimiter on the odd and even samples of the data [see Fig. 4.11(g) for a graphical explanation of odd and even samples]. Fig. 4.10 shows the phase picker right next to two byte synchronizers to emphasize the fact that these three blocks work tightly together. For the conventional mode, all bits of the 16-bit vector are forwarded to path O (for odd path);

path E (for even path) is disabled. This amounts to disabling the phase picker. For the 2× over sampling and burst modes, odd bits of the 16-bit parallel vector are forwarded to path O and even bits are forwarded to path E. The difference between the two modes lies in the way the path is selected. For the 2× over sampling mode, the user selects the path manually with HyperTerminal. For the burst mode, a controller within the phase picker automatically selects the correct path based on information provided by the two byte synchronizers. Note that path O is selected by default no matter the mode of operation.

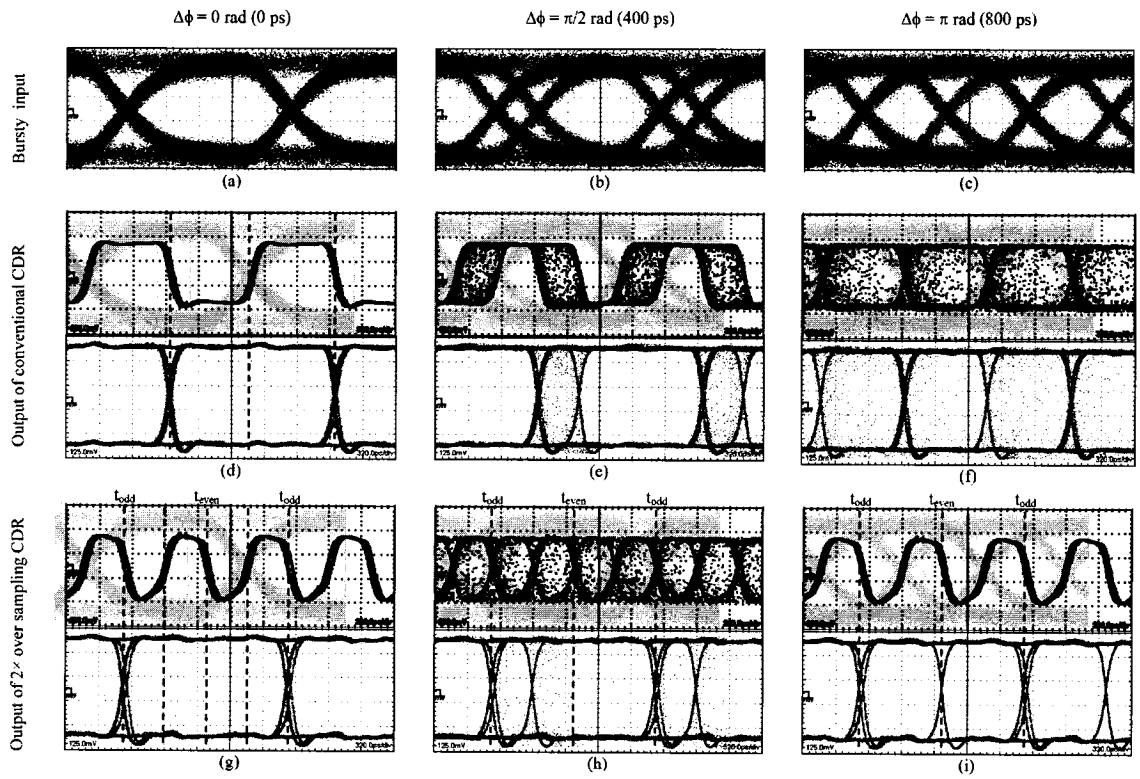


Fig. 4.11. (a)-(c) BM-CPA input signal for 0, π/2 and π rad phase steps, respectively. The jitter is 63 ps RMS. To demonstrate the phase alignment of the recovered clock relative to the phase of the input data, Figs. (a)-(c) reappear in gray under the clock signals of Figs. (d)-(i). (d)-(f) Clock and data recovered by the BM-CPA operated in conventional mode. (g)-(i) Clock and data recovered by the BM-CPA operated in 2× over sampling and burst modes. Bits resulting from the t_{odd} and t_{even} sampling instants are forwarded to the odd and even paths, respectively (see Fig. 4.10). The pattern dependant jitter (PDJ) that appears in the clock and data patterns of Figs. (d)-(i) [although less obvious in (d)-(f)] is one of many subtypes of deterministic jitter. PDJ, also known as intersymbol interference (ISI), is due to a pattern change from a clock like square wave ('1010' pattern) to a non clock-like pattern (PRBS) in the overall pattern shown in Fig. 4.9 [31]. In (i), it is clear that the recovered data associated with packet 1 does not exhibit PDJ (see the transition aligned with t_{even}). This is explained by the fact that packet 1 is made of a '1010' pattern exclusively. On the other hand, the recovered data associated with packet 2 does exhibit PDJ (see the transitions aligned with t_{odd}). This is explained by the fact that packet 2 is made of a 2^{15} PRBS followed by a 2^{15} '1010' pattern.

The following example will clarify the phase picking algorithm. We assume that the BM-CPA was configured to operate in burst mode. When there is no phase step, path O (the default) correctly samples the incoming pattern. This situation corresponds to t_{odd} in Fig. 4.11(g). For a π/2 phase step [see Fig. 4.11(h)], path O will sample the bits on or close to the transitions after the phase step. In this situation, the byte synchronizer of path

O will likely not detect the delimiter at the beginning of packet 2. On the other hand, the byte synchronizer of path E will have no problems detecting the delimiter [see t_{even} in Fig. 4.11(h)]. The phase picker controller monitors the state of the two byte synchronizers and selects the correct path accordingly (path E in this particular case). Once the selection is made, it cannot be overwritten until the comma is detected, which indicates the end of the packet. This process repeats itself at the beginning of every packet. For a $3\pi/2$ phase step (not shown in Fig. 4.11 because the scenario is similar to a $\pi/2$ phase step), path E samples the bits on or close to the transitions and the phase picker controller therefore selects path O. Using this simple algorithm, our experimental results show that we get instantaneous phase acquisition (see Section IV.A).

The two remaining blocks of the BM-CPA, the SMB-to-QSE interface PCB (not shown in Fig. 4.10) and the digital clock manager (DCM), would not be part of a commercial product. The interface PCB sits between the deserializer and the FPGA, but would not be needed if the main blocks (the CDR, the deserializer, the byte synchronizers, and the phase picker) were integrated on a single PCB or a single ASIC. The DCM, an IP block from Xilinx, is used to keep the frequency of the FPGA core constant as the mode of operation of the BM-CPA changes. When the BM-CPA operates in conventional mode, the CDR operates at 622.08 Mbps and the FPGA core runs at 38.88 Mb/s (622.08/16 Mb/s) (see Fig. 4.10). As mentioned earlier, in this mode, the BM-CPA simply looks like a regular SONET CDR. The phase acquisition time of the CDR is measured using the BBERT described in Section II.B and the measurement methodology described in Section II.C. When the BM-CPA operates in 2× over sampling or burst modes, the CDR operates at twice the bit rate, or 1250 Mb/s, to sample each bit twice. In these two modes, the input to the DCM is a 77.76 MHz clock. The DCM divides this frequency by 2 to generate a 33.88 MHz clock. The front-end of the byte synchronizers uses the 77.76 and 33.88 MHz clocks to retain only the even or the odd samples. The rest of the FPGA core, including the phase picker and the BBERT, runs at 33.88 MHz, just like in the conventional mode.

4.2.4 Results and discussion

We characterized the 622.08 Mb/s BM-CPA by measuring its phase acquisition time, its CID immunity, and its dynamic range. For the sake of comparison, we performed the same measurements on a conventional SONET CDR by simply turning off the burst-mode functionality of the BM-CPA. Table 4.2 summarizes our results and compares them against G.982.2 specifications. The results are discussed below.

Table 4.2
Measurement results compared with G.984.2 requirements

Item	Units	Conventional CDR[1]	BM-CPA (this work)	ITU-T G.984.2 [24]	
Bit rate of bursty data	Mb/s	622.08	625[2]	622.08	1244.16
Operating rate of CDR	Mb/s	622.08	1250	N/A	N/A
Guard time	bit	16	16	16	32
Preamble time	bit	40[3]	0[3]	< 28[4]	< 44[4]
Delimiter time	bit	20[5]	20[5]	20	20
Bit error rate	–	$< 10^{-10}$	$< 10^{-10}$	$< 10^{-10}$	$< 10^{-10}$
Jitter (RMS) of input signal	ps	62.64	62.64	N/A	N/A
CID immunity	bit	1070	590	> 72	> 72
Dynamic range (low to high)	dB	2.4	1.9	N/A	N/A
Dynamic range (high to low)	dB	1.8	0.8	N/A	N/A

[1] For SONET or GbE applications.

[2] A GbE CDR was used as a 2× over sampling CDR. 1244.16 and 2488.32 Mb/s CDRs should be used to support the 622.08 and 1244.16 Mb/s data rates, respectively.

[3] Clock phase recovery only.

[4] Amplitude AND clock phase recovery.

[5] As proposed in G.984.3 [30], we used 0xB5983 as a 20-bit delimiter.

4.2.4.1 Phase acquisition time

Figs. 4.12(a), (b), and (c) show plots of the PLR vs. phase step for the BM-CPA operated in conventional mode (SONET CDR), 2× over sampling mode (phase picker off), and burst-mode, respectively. *In all three figures, the preamble length was set to zero.* The plots of BER vs. phase step are not shown because the BER was $< 10^{-10}$ for all three modes of operation. This means that when a packet is not dropped (i.e. the delimiter

is successfully detected in path O, path E, or both), then the payload is transmitted error free. This argument is further discussed in Section 4.2.6.

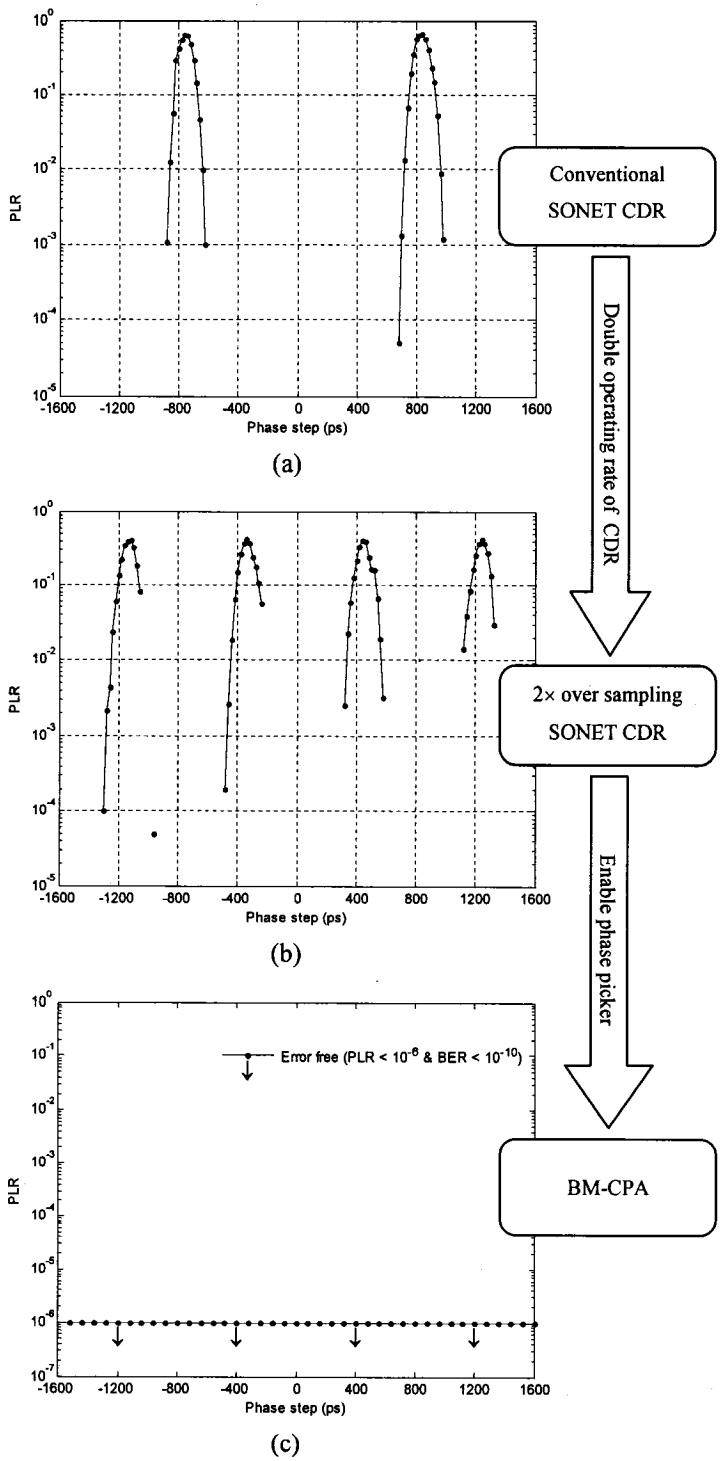


Fig. 4.12. PLR vs. phase step for a zero preamble length. The bit rate and jitter of the input signal are 622.08 Mb/s and 63 ps RMS, respectively [see Figs. 4.11(a)-(c)]. (a) CDR operated at 622.08 Mb/s (conventional SONET CDR). (b) CDR operated at 1250 Mb/s (2× over sampling). (c) Same as (b), but with the phase picker enabled.

At 622.08 Mb/s, a 800 ps phase step corresponds to half a bit period (π rad). As expected, this corresponds to the worst case phase step for the conventional mode [see Figs. 4.11(f) and 4.12(a)]. For the 2× over sampling mode, the worst case phase step is 400 ps (or $\pi/2$ rad) [see Figs. 4.11(h) and 4.12(b)]. It should be noted that whereas a π phase step represents the worst case scenario for a conventional CDR, a 2× over sampling CDR does not need to realign the clock in such a case [see Fig. 4.12(i)]. The progression from Fig. 4.12(a) to Fig. 4.12(c) shows that 2× over sampling, combined with appropriate phase picking, can turn a conventional CDR into a BM-CPA with instantaneous phase acquisition (0 bit). In order to compare this result with the phase acquisition time of the BM-CPA operated in conventional mode, we ran PLR vs. phase step measurements until we found the preamble length that gave us error free operation. The measurements are fully automated by the BM-TS. The user specifies a range of phase steps and a range of preamble lengths, together with their respective granularity, and the computer takes care of the rest. The results are shown in Fig. 4.13. For a preamble length of 32 bits, the PLR is $> 10^{-5}$; 40 bits were needed in order to obtain error free operation (PLR $< 10^{-6}$ and BER $< 10^{-10}$). This preamble length does not satisfy the 28-bit requirement of G.982.2 [24]. Moreover, assuming 2 bytes of the preamble are reserved for amplitude recovery, this leaves only 12 bits for phase recovery.

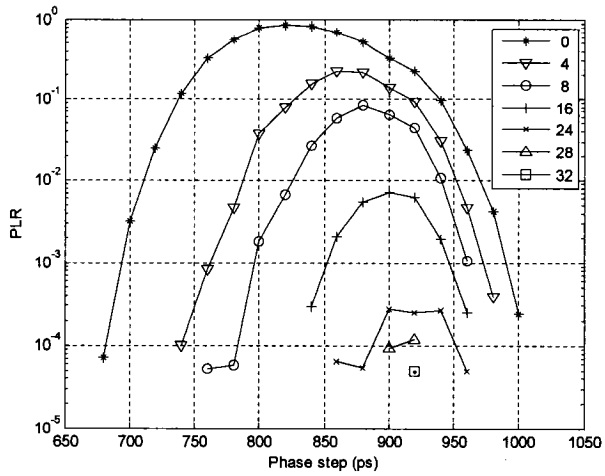


Fig. 4.13. PLR vs. phase step for a conventional 622.08 Mb/s CDR. As expected, the worst-case phase step is around π rad, or 800 ps. The legend shows some of the preamble lengths that were tested. A preamble length of 40 bits gave error free operation (PLR < 10^{-6} and BER < 10^{-10}).

Before concluding this section, we compare two methodologies for measuring the phase acquisition time. For the same SONET CDR, we measured a phase acquisition time of 40 bits in this work whereas a value of 1400 bits was reported in [4]. The 35-fold discrepancy is due to the use of a global clock in [4] to avoid losing synchronization while performing BER measurements. The phase of the global clock was adjusted for optimum sampling of the bits far away from the beginning of the packet. Errors were masked starting at the beginning of the packet until a zero BER was measured. With this measurement methodology, the preamble length corresponds to the number of bits that need to be masked in order to get a BER < 10^{-10}. The problem with this methodology is that while the CDR is recovering the phase, some of the errors detected at the beginning of a packet are due to the BERT not optimally sampling the output of the CDR. We addressed this shortcoming in this work by using the recovered clock to perform BER measurements, therefore guaranteeing an optimum phase between the sampling (recovered) clock and the recovered data. As discussed in Section II, the recovered clock could not be used with a conventional BERT because of the synchronization problem originating from the bursty nature of the packets. With the FPGA, we addressed this issue by synchronizing the internally generated PRBS with the incoming pattern at the beginning of every packet. The synchronization happens instantaneously as soon as the

delimiter is detected. The delimiter and the comma can therefore be thought of as gating signals for BBER measurements.

4.2.4.2 CID immunity

We now return to Table 4.2 and note that the CID immunity is shorter for the BM-CPA (590 bits) than it is for the conventional CDR (1070 bits). Despite the CID immunity penalty, 590 bits is still well above the requirement specified in G.984.2 (> 72 bits). One explanation to the CID penalty comes from the Bessel-Thomson filter. The filter has a -3-dB bandwidth of 467 MHz to standardize the input signal to the 622.08 Mb/s data rate and make the comparison fair between the conventional CDR and the BM-CPA. The resulting rise and fall times are slow for a 2× over sampling CDR running at 1250 Mb/s. Together with the fact that the bits are sampled on either side of the optimum point [see Fig. 4.12(g)], these arguments may explain the CID immunity penalty. The experimental results presented in Section IV.A nevertheless confirm that the BM-CPA, despite a CID immunity penalty, can provide instantaneous phase acquisition even with the rise and fall times of a 622.08 Mb/s signal.

4.2.4.3 Dynamic range

In an OLT, the BM-RX is responsible for amplitude recovery. Hence, the dynamic range of the BM-CPA does not carry much value, but its measurement verifies the functionality of the BM-TS and allows us to draw the following conclusion. In Table 4.2, we observe a 1 dB power penalty between the BM-CPA and the SONET CDR when a low amplitude packet follows a high amplitude packet – this is the worst-case scenario [25]. This dynamic range penalty due to 2× over sampling would not affect the dynamic range of the overall OLT since the BM-RX, responsible for amplitude recovery, still operates at the bit rate even when connected to a 2× over sampling BM-CPA like the one described in this work.

4.2.5 Conclusion

In conclusion, we successfully implemented a 622.08/1244.16 Mb/s BM-CPA that meets G.984.2 specifications and provides instantaneous phase acquisition. We verified the design at 622.08 Mb/s using a custom BM-TS rated at 1 Gb/s. Our test solution, aided

by a new test methodology based on both BER and PLR, can measure the amplitude, frequency, and phase acquisition times of devices like SONET CDRs, BM-RXs, BM-CPAs, and frequency synthesizers.

The price to pay to obtain instantaneous phase acquisition is faster electronics. On the other hand, our solution exploits the design of components for long-haul networks. These components are typically a generation ahead of the components for multiaccess networks. For example, 10 Gb/s is currently mainstream for long-haul networks, whereas GPON supports a maximum data rate of 2.5 Gb/s. Assuming this holds true in the future, our solution will scale with the scaling of components for long-haul networks. Moreover, we argue that the doubling in frequency for the CDR and the deserializer is a good trade off to obtain instantaneous phase acquisition in a very simple manner and without the costly need to design a new ASIC.

4.2.6 Appendix

We stated in Section IV.A that when a packet is not dropped, then error free operation can be expected on the payload. This was not true when we tried using a shorter delimiter (16 bits instead of 20). In this case, we observed that the BER was incrementing in bursts. The correlation between the length of the bursts and the length of the payload allowed us to determine that the problem was due to the byte synchronizer, which was generating false positives while searching for the delimiter. The false detection of the delimiter was typically happening over the first few bits of packet 2, but not exactly at the beginning, while the CDR is trying to recover the phase. The BBERT was therefore triggered too late, making the rest of the payload out of sync with respect to the internally generated PRBS pattern. This explains why the bursts of errors were more or less equal in length to the payload. This finding forced us to revert back to a 20-bit delimiter, which is what G.984.2 recommends. It should be noted that the error resistance of the delimiter depends not only on its length, but also on the exact implementation of the pattern correlator – a simple comparator was used in this work. More information on the optimum length for the delimiter can be found in [24].

4.2.7 Implementation details

In this section, we provide implementations details for the BM-CPA. These details were left out of [3] for the sake of conciseness. As shown in Fig. 4.14(a), the BM-CPA consists of three discrete integrated circuits (CDR, 1:16 deserializer, and FPGA) mounted on three evaluations boards. The CDR is mounted on the front most PCB, the deserializer is mounted on the rightmost vertical PCB, and the FPGA is mounted on the horizontal PCB.

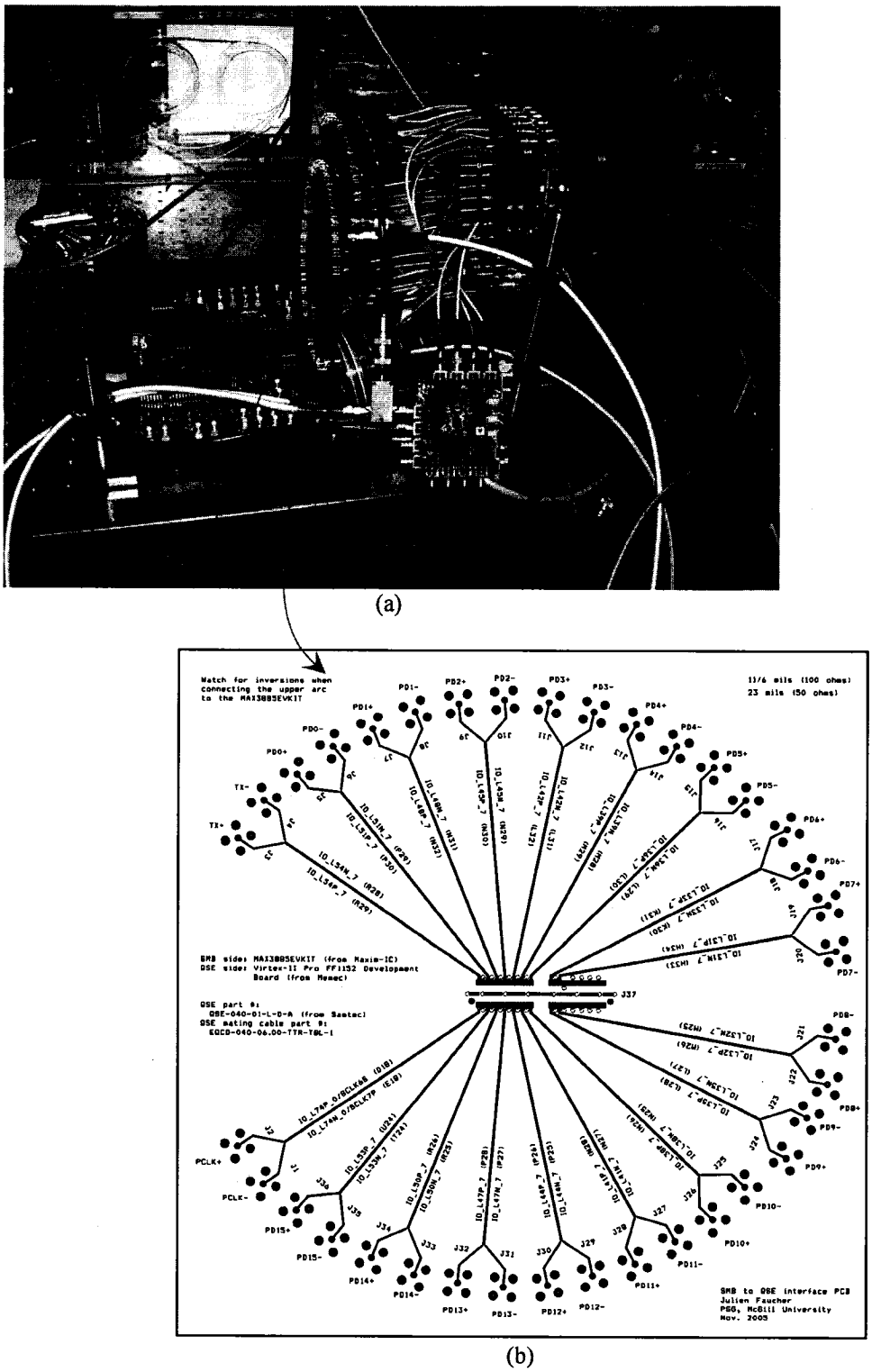
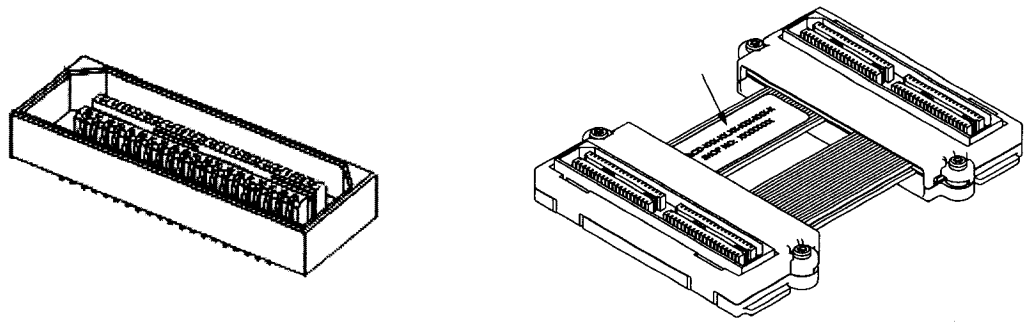


Fig. 4.14. (a) Current implementation of the BM-CPA (b) Custom SMB-to-QSE interface PCB.

The deserializer evaluation board uses SMB connectors, whereas the FPGA evaluation board uses two QSE connectors from Samtec [see Fig. 4.15(a)] – one for the

inputs, and one for the outputs. In Fig. 4.14(a), the two vertical PCBs next to the FPGA serve as SMB-to-QSE connector converters. Fig. 4.14(b) shows the PCB footprint of the custom SMB-to-QSE interface PCB. We used 34 six-inch SMB cables (16-bit differential data + 1 differential clock) to connect the deserializer outputs to the QSE-to-SMB interface PCB, and a high-speed parallel cable [see Fig. 4.15(b)] to complete the connections to the FPGA. The QSE connector is rated at 8 GHz (differential signaling), and its mating cable is rated at 1.74 GHz.



(a) (b)

Fig. 4.15. (a) QSE connector from Samtec (part # QSE-040-01-L-D-A). (b) Mating cable, also from Samtec (part # EQCD-040-06.00-TTR-TBL-1)

4.3 Component integration

4.3.1 Introduction

As we saw in Section 4.2.7, the BM-CPA, in its current form, is rather bulky. The use of evaluation boards allowed for quick prototyping, but now that the design is complete, a follow-up of this work would be to integrate the components of the BM-CPA on a single PCB or on an ASIC. Integration is particularly important if the BM-CPA is to be used in a burst or packet switched network requiring a BM-CPA at every switching node. Moreover, integration and packaging will become more critical if the design is to be scaled to 5 Gb/s using a 10 Gb/s CDR.

In this section, we present the design and characterization of a packaging solution for 10 Gb/s ASICs. The packaging solution was originally designed to test a 0.5 μm SiGe chip with 10 Gb/s current-mode logic (CML) blocks. It could be easily adapted for an ASIC integrating all the components of the BM-CPA. The signal, when entering the

SiGe chip, goes through a 50 Ω input buffer, an analog multiplexer, and a back-terminated 50 Ω output buffer. Our measurement results provide experimental evidence that the packaging solution would support the scaling of the BM-CPA up to a 2× over sampling rate of 10 Gb/s.

4.3.2 Description of packaging solution

The main component of our packaging solution is an open-cavity quad flat no lead (QFN) package. QFN packages were commercialized a few years ago, but *open-cavity* QFN packages were only introduced last year (2005). One of the first companies to ship it was Sempac. The JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council) defined the QFN outline as a good low cost alternative for chip scale packages (CSPs). CSP is about bringing the package size as close as possible to the die size. Fig. 4.16 shows a picture of a plastic molded QFN package.

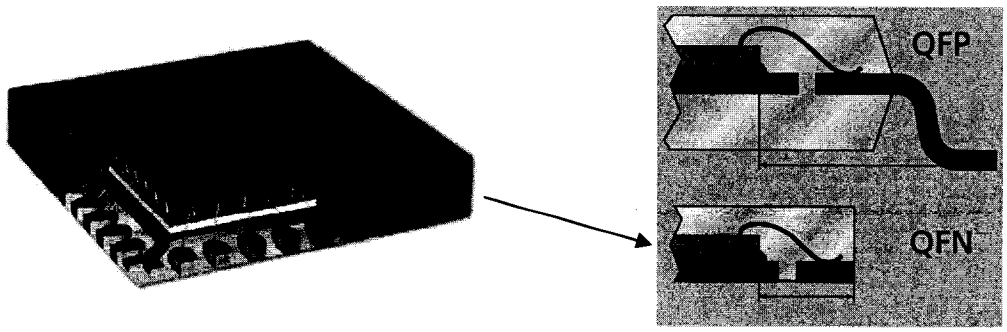


Fig. 4.16. Plastic molded QFN package. The die is attached to a metal leadframe. Connections to the leads are made by wire bonds. The leads of a QFN are very short and do not extend outside the package body. A realistic distance from die edge to package edge may be less than 1 mm. The same distance for a quad flat pack (QFP) package is at least around 3 mm. QFN packages have excellent thermal properties due to their metal die-attach pad extending to the bottom side of the package.

Fig. 4.17(a) shows the packaging solution that we designed and characterized. Our two main design goals were good signal integrity and low cost. The open-cavity QFN package was hand soldered onto an FR-4 PCB (standard 4 layer stack-up), the footprint of which is shown in Fig. 4.17(b). The QFN, because of its short leads, provides good signal integrity. Signal integrity is further improved by the very small cavity size, which translates into very short wire bonds [~1 mm with a die in the cavity, as shown in Fig.

4.17(d)]. With no die in the cavity for package characterization purposes [see Fig. 4.17(c)], the wire bonds are ~3.5 mm long. FR-4, being the most common dielectric for PCB manufacturing, keeps the cost low. The incentive to keep the cost low was to plan for design revisions, such as fine-tuning the impedance of the high-speed traces. The two high-speed differential microstrips in the middle of Fig. 4.17(e) are 11 mils wide (279.4 μm). The spacing is 6 mils (152.4 μm). This configuration, as we are about to see, provides a 100 Ω differential impedance. The pads of the QFN package are 10 mils wide (254 μm), which is close to the width of the microstrips. The QFN package is 4.554 mm × 4.554 mm. The center pad (ground) is 3.1 mm × 3.1 mm.

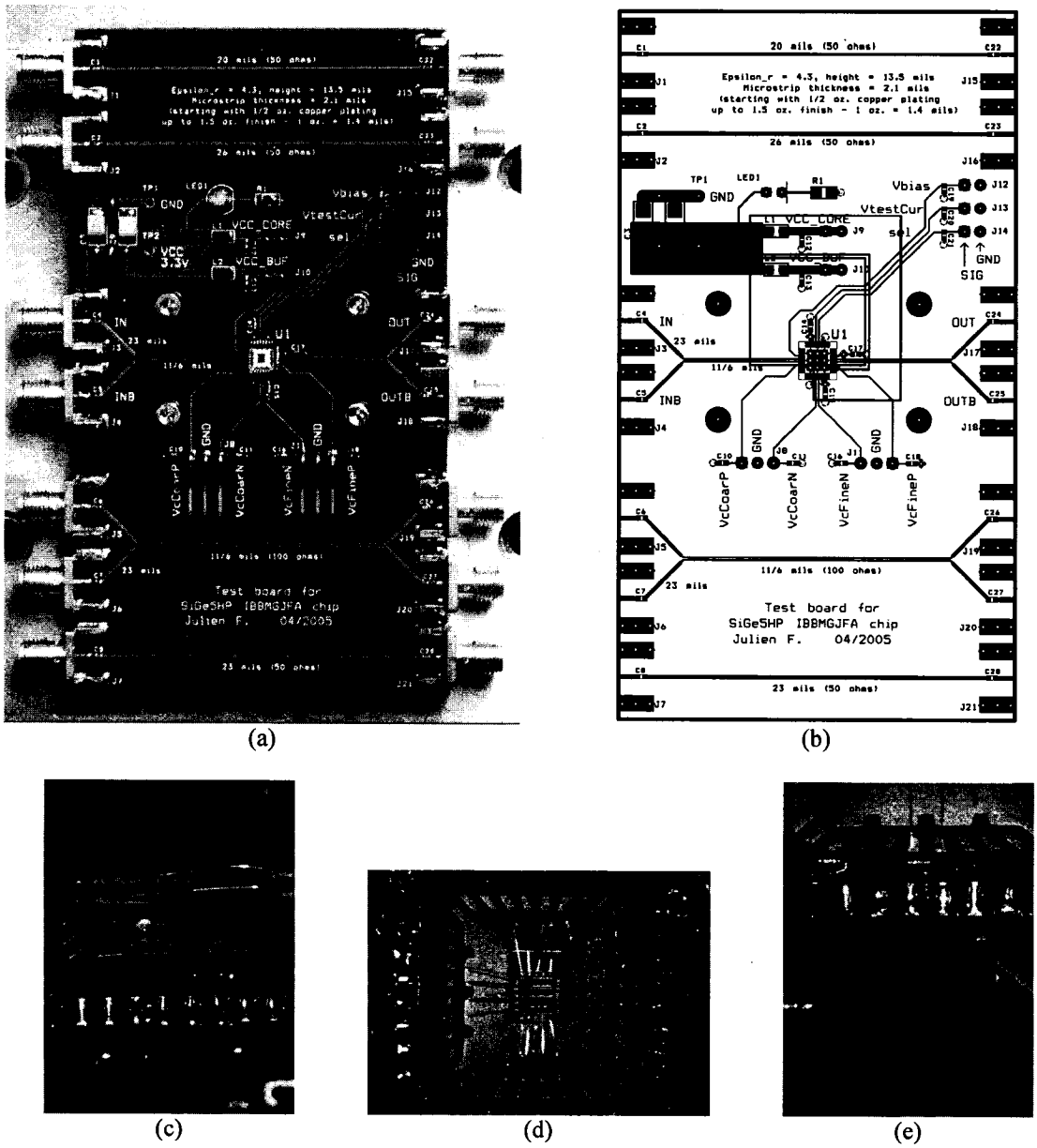


Fig. 4.17. (a) Populated PCB. (b) PCB footprint. (c) Feed through for characterizing the PCB and the QFN. The two wire bonds are ~3.5 mm long. (d) SiGe chip packaged in the QFN. The wire bonds are ~1 mm long. (e) 100 Ω differential microstrips [rotated 90° with respect to (a)].

As we will see in the next section, FR-4 works fine at 5 Gb/s, but at 10 Gb/s, it may be necessary to use a better (and more expensive) dielectric like Rogers. In trying to keep the cost low, we also considered a chip-on-board approach to avoid the need for a chip package. This approach, although simpler than the one we adopted, has two drawbacks. First, because wire bonds do not stick to the conventional solder plating (HASL), the PCB has to be gold plated. This requirement can easily multiply PCB manufacturing costs by

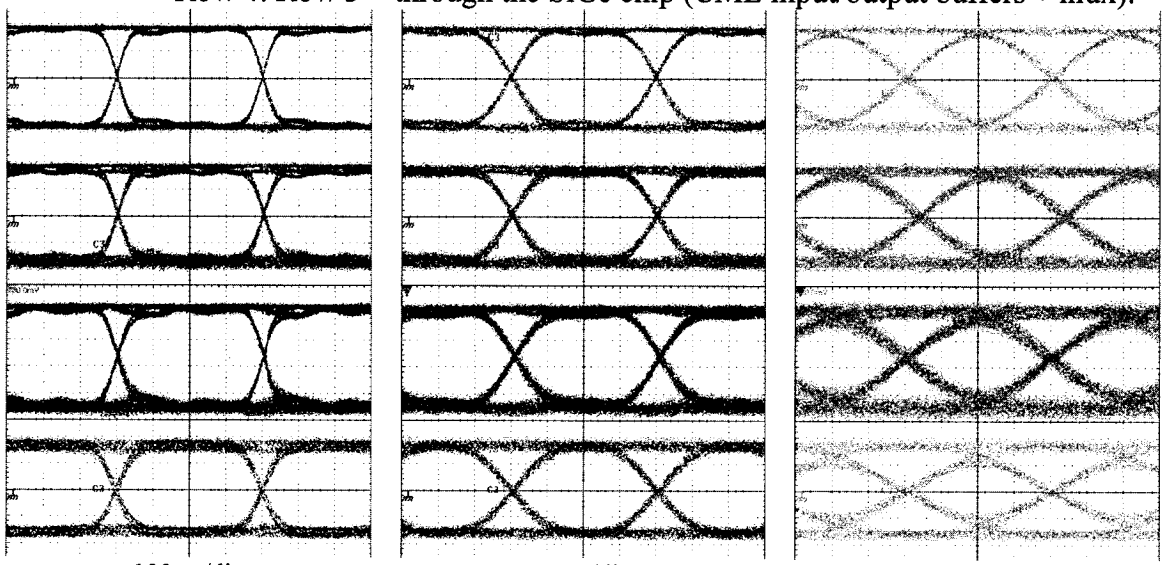
5. Second, the minimum line width and line spacing supported by PCB manufacturers dictates the minimum pad size and pad spacing. With a typical line width/spacing of 6 mils (152.4 μm), the chip-on-board approach quickly becomes pad limited if the wire bonds are to be kept short.

We will now look at oscilloscope traces and time-domain reflectometer (TDR) waveforms to assess the impact of the PCB and the QFN package on signal integrity.

4.3.3 Oscilloscope traces

Rows 1 and 2 in Fig. 4.18 show oscilloscope traces for 2.5, 5, and 10 Gb/s signals transmitted through single-ended and differential test coupons. Signal integrity is still good at 10 Gb/s, which is commonly accepted as the speed limit of FR-4; at higher speeds, the slow rise and fall times lead to intersymbol interference (ISI) and an increase of the BER.

Legend: Row 1: 50-ohm single-ended microstrip;
Row 2: 100-ohm differential microstrips (single-ended drive);
Row 3: Row 2 + through the CSP package + 3.5 mm wire bonds;
Row 4: Row 3 + through the SiGe chip (CML input/output buffers + mux).



100 ps/div (2.5 Gb/s) 50 ps/div (5 Gb/s) 25 ps/div (10 Gb/s)

Fig. 4.18. Oscilloscope traces (10 s persistence) taken at 2.5 Gb/s (column 1), 5 Gb/s (column 2), and 10 Gb/s (column 3). In all cases, the input signal was a 2^{15}-1 PRBS and the BER was < 10^{-10}. The amplitude of the input signal was set to 400 mV (800 mV differential); the vertical scale for all eye diagrams is 100 mV/div.

After adding the QFN package and 3.5 mm wire bonds to the data path, we obtained the oscilloscope traces of row 3. When comparing rows 2 and 3, we can conclude that the QFN package has negligible impact on signal integrity, even with 3.5 mm wire bonds. With the addition of the SiGe chip in the data path, we obtained the oscilloscope traces in row 4 (note that adding the chip reduced the length of the wire bonds from 3.5 mm to ~1 mm). Signal integrity is still very good, but the rise and fall times are a little longer. This is due to the CML output buffer on the SiGe chip, not to the rest of the package.

4.3.4 TDR measurements

As shown on the PCB footprint of Fig. 4.17(b), we have put three single-ended and one differential test coupons on the PCB. The three single-ended test coupons have a width of 20, 23, and 26 mils (508, 584.2, and 660.4 μm, respectively). We used the following formula to calculate the impedance of each microstrip layout [33]

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98 \cdot H}{0.8 \cdot W + T}\right) \tag{4.1}$$

where each variable is defined in Table 4.3. We then used a 2D field solver [34] to to get more accurate results. The theoretical impedance values of the single-ended microstrips appear in Table 4.4.

Table 4.3
Physical parameters of the microstrips

Parameter	Symbol	Units	100-Ω differential	50-Ω single-ended
Relative dielectric constant of FR-4	ε_r		4.3	4.3
Height of the traces[1]	H	mils	13.5	13.5
Width of the traces	W	mils	11	20, 23, or 26
Spacing between the traces	S	mils	6	N/A
Thickness of the traces	T	mils	2.1[2]	2.1

[1] Above the ground plane (2nd layer).

[2] Starting with 0.5 oz. copper plating up to 1.5 oz. finish (1 oz of copper corresponds to a thickness of 1.4 mil).

The differential test coupon is made of two 11-mil (279.4 μm) microstrip traces separated by 6 mils (152.4 μm). This configuration is identical to the differential microstrips connected to the QFN package. Using the same 2D field solver and the parameters of Table 4.3, we verified that this configuration gave a differential impedance close to 100 Ω (see Table 4.4).

We measured the impedance of the test coupons using TDR test equipment. Fig. 4.19 shows the TDR waveforms. Of the three single-ended microstrips, the one with a width of 23 mils offers the closest match to 50 Ω [see the insets of Figs. 4.19(b)-(d)]. As shown in Fig. 4.19(e), the differential microstrips have an impedance of 54 Ω (single-ended measurement). A more accurate measurement could be obtained with a differential TDR probe instead of a single-ended TDR probe like we used. With the QFN package and 3.5 mm wire bonds in the data path, the TDR measurement exhibits a series inductance discontinuity caused by the wire bonds [see Fig. 4.19(f)]. Table 4.4 summarizes the calculated and measured impedance values and shows a good agreement between the two.

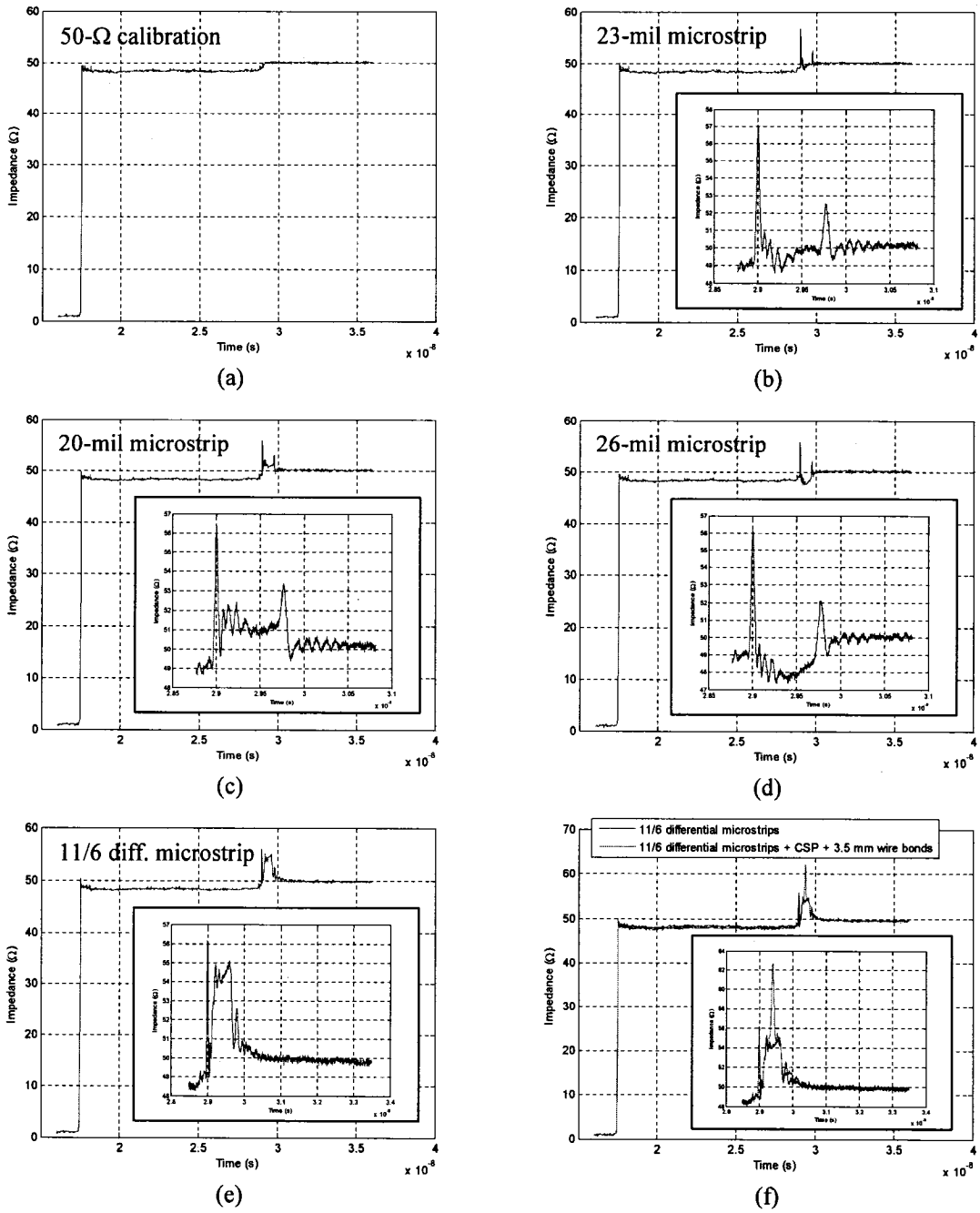


Fig. 4.19. (a) 50 Ω calibration of TDR setup. (b) 23-mil single-ended microstrip. (c) 20-mil single-ended microstrip. (d) 26-mil single-ended microstrip. (e) Differential microstrips, single-ended drive (width = 11 mils, separation = 6 mils). (f) Same as (e), but through the CSP package and 3.5 mm wire bonds.

Table 4.4
Calculated vs. measured impedance

Microstrip width (W)	Calculated impedance[1] (Ω)	Measured impedance (Ω)
11 mils[2] (279.4 μm)	49[3]	55[3]
20 mils (508 μm)	56	51
23 mils (584.2 μm)	52	50
26 mils (660.4 μm)	48	48

[1] Using a 2D field solver [34].

[2] 6 mil spacing (152.4 μm).

[3] This is the odd mode impedance. The differential impedance is 2× the odd mode impedance.

4.3.5 Conclusion

In summary, we have proposed a low-cost packaging solution that provides good signal integrity at up to 10 Gb/s. The small size, short leads, and good thermal properties of the QFN make it a sound choice for packaging 10 Gb/s ASICs. The open cavity of the QFN is especially useful for prototyping. We characterized the PCB with TDR test equipment. The measured and calculated impedance values are in close agreement. Our packaging solution will be useful to scale the BM-CPA described in Section 4.2 to 5 Gb/s (2× over sampling rate of 10 Gb/s).

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CHAPTER 5

Behavioral simulations of CDR circuits

As we pointed out in Section 4.3, scaling the BM-CPA to 5 or 10 Gb/s will likely pass by the design of an ASIC. In this chapter, one goal is to develop behavioral models to facilitate and speed up the simulation of CDR circuits. Such circuits, as we argued in Section 1.1.3, can take hours or even days to simulate at the transistor level. This is where mixed-level simulations, in which blocks at the behavioral level are co-simulated with blocks at transistor level, become useful. Another goal of this chapter is to exploit the models developed to compare the jitter characteristics and phase acquisition time of three types of CDRs: SONET compliant CDRs, BM-CPAs based on 2× over sampling, and broadband CDRs.

In Section 4.1, we described a behavioral simulator to analyze the loop dynamics of a broadband CDR. CDR parameters like the gain of the VCO, the charge-pump current, and the resistor and capacitor values of the loop filter, were chosen to obtain the desired loop parameters. Because the Matlab-based behavioral model was incompatible with Cadence and the Spice simulator, we had to generate a new schematic and a new test bench to perform simulations at the transistor level.

In a more efficient system-to-circuit design flow, the system design phase and the circuit design phase use the same behavioral models. The Verilog-A and Verilog-AMS hardware description languages (HDLs) and the Virtuoso AMS Designer simulator from Cadence were developed with this philosophy in mind. Verilog-A/AMS HDLs provide a mean of performing mixed-level simulations, but they have a few drawbacks. First, they lack good libraries for complex circuits such as CDRs. Second, HDLs in general do not support as many mathematical functions as Matlab or C++, which often limit or complicate the development of behavioral models.

In this chapter, we look at an alternative to Verilog-A/AMS: CppSim. CppSim is a free behavioral simulation package that leverages the C++ language to allow very fast

simulations of circuits and systems. CppSim is especially useful for the simulation of phase-locked loops – it achieves fast and accurate simulation of these systems using a uniform time step and the area conservation principle, as described in [1].

CppSim can be run standalone, from Matlab to facilitate post-processing analyses, and more recently from the Cadence design environment using VppSim. VppSim is a Unix-based framework that is a superset of three different, but related, simulation environments:

- CppSim: C++ only behavioral simulation;
- VppSim: C++ and Verilog co-simulation;
- AMS with VppSim modules: C++, Verilog, VHDL, and SPICE co-simulation.

CppSim is the most mature and has been widely used in the form of a freely available Windows package. The primary difference between the CppSim and VppSim distributions is the schematic capture program. CppSim uses Sue2, whereas VppSim uses the Virtuoso Schematic Editor from Cadence. The VppSim framework has the advantage of allowing very sophisticated and fast simulation of complex mixed-signal circuits and systems at the behavioral level by using CppSim within the Cadence design environment. The user can seamless move from behavioral-level simulations to mixed-level simulations using VppSim. The user can co-simulate C++ behavioral models with Spice, Verilog, and VHDL models by using AMS in conjunction with VppSim modules. A beta version of VppSim is currently available, but some components are still under development. We therefore used CppSim to run our simulations, knowing that the models developed will be useful for simulations in Cadence when the full version of VppSim becomes available.

In Section 5.1, we first generate benchmark results using a baseband model that is well documented in the literature [2]. We then compare, in Section 5.2, the simulation results obtained with CppSim to the benchmark results. Once we have verified that our models can be trusted, we use them to produce various results that we discuss in Section 5.3. For example, we discuss the dependence of phase acquisition time on bit rate and the type of preamble, we evaluate the jitter bandwidth/peaking/tolerance of the BM-CPA described in Chapter 4, and we simulate the jitter at the end of two cascades of CDRs, one using broadband CDRs, and one using BM-CPAs. We report on the speed of the CppSim

simulator in the conclusion. Whenever appropriate, we compare simulation results obtained with the baseband model to those obtained with CppSim.

5.1 Baseband linear model

Fig. 5.1(a) shows the schematic of a charge-pump PLL-based CDR. We developed baseband and CppSim models for this popular CDR architecture. The baseband model of Fig. 5.1(b) assumes a linear model for the combination of the phase detector, the charge-pump, and the low-pass filter. The baseband model further assumes that the VCO has a linear response. These assumptions only hold when the CDR is locked, i.e. the frequency of the input signal is close to the VCO frequency). Hence, we cannot use the baseband model to simulate the frequency acquisition time of a CDR starting from an unlocked condition.

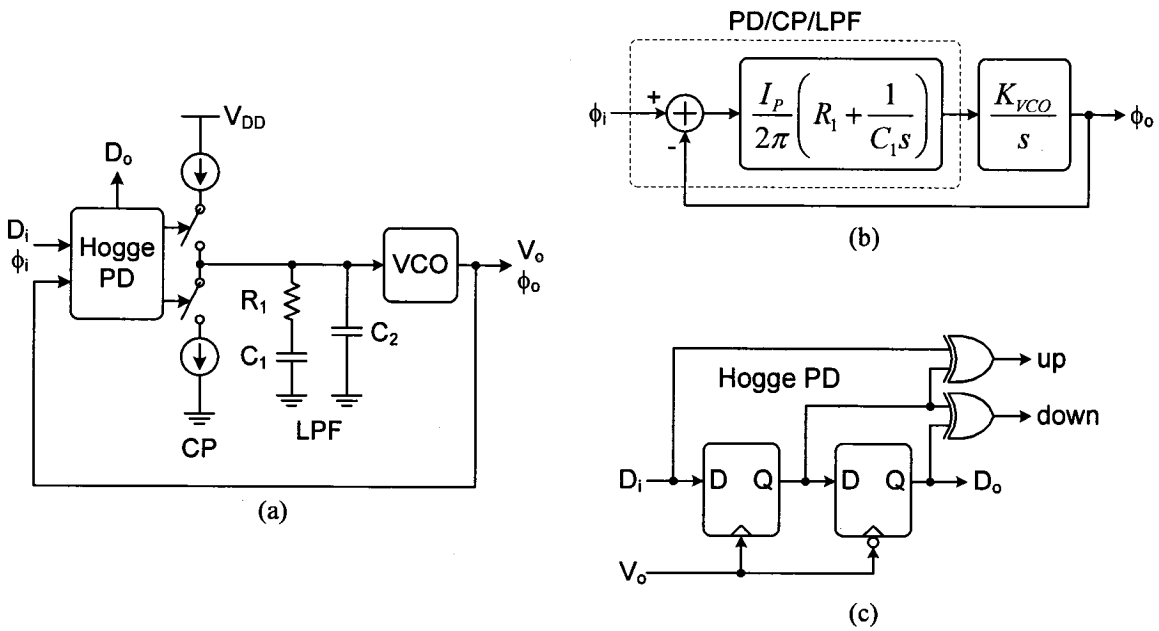

Fig. 5.1. (a) 3rd-order charge-pump CDR simulated in CppSim. (b) 2nd-order baseband model of the charge-pump CDR with C_2 neglected (s-domain model) [4]. (c) Hogge phase detector. D_i: input data; ϕ_i: input phase; D_o: recovered data; V_o: recovered clock; ϕ_o: output phase; PD: phase detector; CP: charge pump; LPF: low-pass filter; VCO: voltage-controlled oscillator.

In Section 5.1.1, we set up the equations that describe the generic baseband model of Fig. 5.1(b). We then customize the generic model to create three specific SONET CDR models, each running at a different frequency (622.08, 1244.16, and 2488.32 Mb/s). The

CDRs meet the jitter requirements of Telcordia GR-253-CORE [3], which we verify with simulation results in Section 5.1.2.

5.1.1 Determination of the CDR parameters

The jitter transfer requirements in Table 5.1 limit the amount of jitter on an input OC-N electrical signal that can be transferred to the output [3]. For SONET CDRs, the jitter transfer function shall be *under* the mask of Fig. 5.2. Table 5.1 also lists the jitter tolerance requirements of SONET CDRs. For OC–N interfaces, jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes a 1-dB power penalty (BER < 10^{-10}). SONET compliant CDRs must have a jitter tolerance *above* the jitter tolerance mask of Fig. 5.3.

Table 5.1
SONET specifications[1] for the jitter transfer mask of Fig. 5.2 and the jitter tolerance mask of Fig. 5.3 [3]

		Jitter transfer		Jitter tolerance	
SONET rate	Line rate (Mb/s)	f_c[2] (kHz)	J_P[3] (dB)	f_4[4] (kHz)	A_1[5] (UIpp)
OC-3	155.52	130	0.1	65	0.15
OC-12	622.08	500	0.1	250	0.15
OC-24[6]	1244.16	1000	0.1	500	0.15
OC-48	2488.32	2000	0.1	1000	0.15

[1] A data transition density of 1/2 is assumed.

[2] f_c: jitter transfer bandwidth.

[3] J_P: jitter peaking.

[4] f_4: fourth corner frequency of the jitter tolerance mask. Note that $f_4 = f_c/2$.

[5] A_1: input jitter amplitude at f_4.

[6] Not defined in Telcordia GR-253-CORE [3], but the parameters can be inferred from the OC-12 and OC-48 data rates.

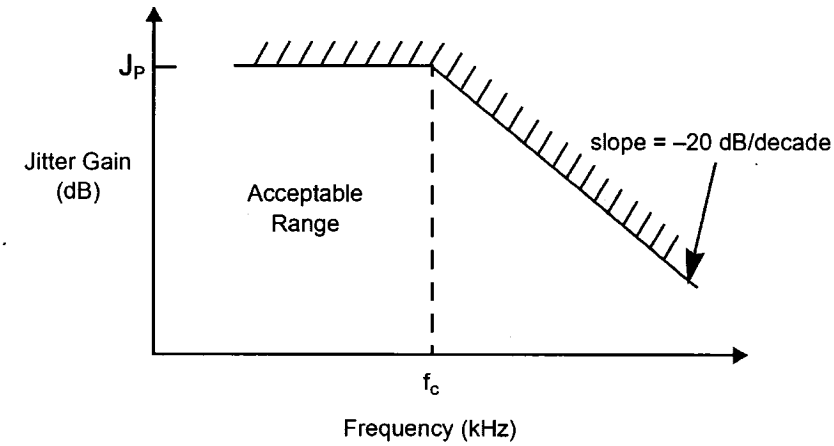

Fig. 5.2. SONET jitter transfer mask [3]. f_c: jitter transfer bandwidth.

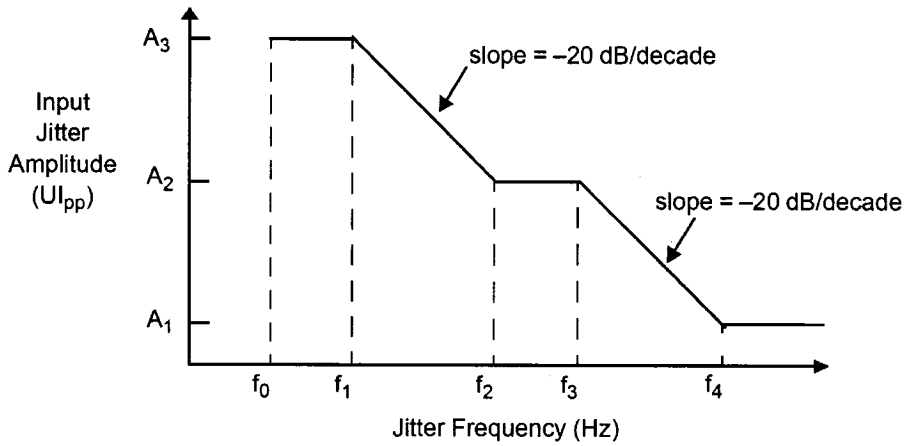

Fig. 5.3. SONET jitter tolerance mask [3]. f_0 to f_4: corner frequencies.

In order to match the jitter requirements of Table 5.1, we treat the CDR as a linear feedback system. The open-loop transfer function of the CDR in Fig. 5.1(b) is

$$L(s)=\left.\frac{\Phi_{out}}{\Phi_{in}}\right|_{open}=\frac{I_P}{2\pi}\left(R_1+\frac{1}{C_1 s}\right)\frac{K_{VCO}}{s} \tag{5.1}$$

and its closed-loop transfer function is

$$H(s)=\left.\frac{\Phi_{out}}{\Phi_{in}}\right|_{closed}=\frac{\frac{I_P K_{VCO}}{2\pi C_1}(R_1 C_1 s+1)}{s^2+\frac{I_P}{2\pi}K_{VCO}R_1 s+\frac{I_P}{2\pi C_1}K_{VCO}} \tag{5.2}$$

Note that we neglected C_2 in Fig. 5.1(b) in order to simplify the analysis. The main function of capacitor C_2 is to filter out the ripples at the input of the VCO. These ripples,

in practice, cause jitter at the output of the VCO. If C_2 is smaller than one fifth to one tenth of C_1, the closed-loop time and frequency responses remain relatively unchanged [4].

We can rewrite the second-order transfer function of (5.2) using a familiar form used in control theory, $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ζ is the "damping ratio" and ω_n is the "natural frequency". That is,

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{5.3}$$

where

$$\omega_n = \sqrt{\frac{I_P D_T K_{VCO}}{2\pi C_1}} \tag{5.4}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P D_T C_1 K_{VCO}}{2\pi}} \tag{5.5}$$

Note that in (5.4) and (5.5), the charge-pump current is scaled by D_T to model the effect of data transition density on the gain of the phase detector. For example, the '1010' pattern has a transition density of 1 (the Hogge PD sees a transition on every rising edge of the clock), whereas a PRBS pattern has a transition density of 1/2. Using the closed-loop transfer function of (5.3), one can show that the -3dB bandwidth of the CDR is given by

$$\omega_{-3dB} = \sqrt{\left[\left(2\zeta^2 + 1\right) + \sqrt{\left(2\zeta^2 + 1\right)^2 + 4}\right]\omega_n^2} \tag{5.6}$$

In order to guarantee loop stability, ζ must exceed $\sqrt{2}/2$. Moreover, as we will see in Table 5.2, ζ must be greater than 4.66 to ensure jitter peaking is less than 0.1 dB. If $2\zeta^2 >> 1$, then (5.6) reduces to

$$\begin{aligned} \omega_{-3dB} &\approx 2\zeta\omega_n \\ &= \frac{R_1 I_P D_T K_{VCO}}{2\pi} \end{aligned} \tag{5.7}$$

Jitter peaking (J_P) can be calculated using [4]

$$J_P = \frac{2.171}{\frac{R_1^2}{4} I_P D_T C_1 K_{VCO}} \tag{5.8}$$

Note that J_P is in dB. We will now use (5.7) and (5.8) to determine the physical parameters (I_p, K_{VCO}, R_1, and C_1) for the three SONET compliant CDRs. Since we have two equations for four unknowns, we must assume values for two of the parameters. In practice, the VCO may come from a library and have a predetermined sensitivity (K_{VCO}). We will assume a value of 500 MHz/V. Moreover, we assume that all three CDRs share the same VCO, as may be the case in a multirate CDR architecture. We finally assume a charge-pump current of 62.5 μA for the OC-12 CDR; we double and quadruple this current for the OC-24 and OC-48 CDRs, respectively. This leaves us with two equations for two unknowns. To find R_1 for each CDR, we use (5.7) with $D_T = 1/2$ (PRBS data) and the -3-dB bandwidths of Table 5.1. We can then use (5.8) to find C_1, assuming a jitter peaking of 0.1 dB for all three CDRs. Table 5.2 shows the calculated values for I_p, K_{VCO}, R_1, C_1, ζ, and ω_n.

Table 5.2
Parameters for SONET compliant CDRs

CDR parameter	OC-12 CDR (622.08 Mb/s)	OC-24 CDR (1244.16 Mb/s)	OC-48 CDR (2488.32 Mb/s)
I_P	62.5 μA	125 μA	250 μA
K_{VCO}	500 MHz/V	500 MHz/V	500 MHz/V
R_1	201.06 Ω	201.06 Ω	201.06 Ω
C_1	137.48 nF	68.741 nF	34.371 nF
ζ	4.66	4.66	4.66
ω_n	0.337×10^6 rad/s	0.674×10^6 rad/s	1.35×10^6 rad/s

5.1.2 Benchmark simulation results

We first verify the stability of the CDRs by plotting the bode diagram of their open-loop transfer function. Fig. 5.4 shows the bode diagram for the OC-12 CDR only – similar bode diagrams are obtained for the other two CDRs.

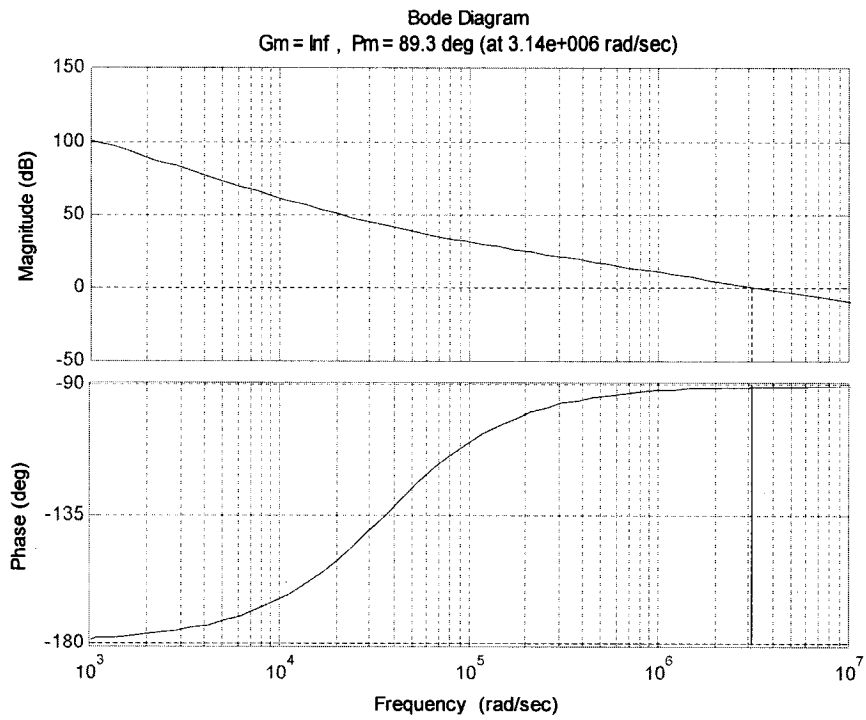

Fig. 5.4. Bode diagram of the OC-12 CDR.

The phase margin for all three CDRs is 89.3°, therefore guaranteeing their stability. Note that it would not be possible to achieve such a good phase margin in practice since we neglected C_2 in our analysis. We can also assess the stability of the CDRs by looking at the value of ζ, which is 4.66 in all three cases. As expected, this value is greater than the threshold for stability ($\sqrt{2}/2$). Moreover, the value of 4.66 is sufficiently high to guarantee a jitter peaking of less than 0.1 dB (see the bottom-left inset in Fig. 5.5). The top-right inset in Fig. 5.5 confirms that the bandwidth of the OC-12, -24, and -48 CDRs is 500, 1000, and 2000 MHz, respectively.

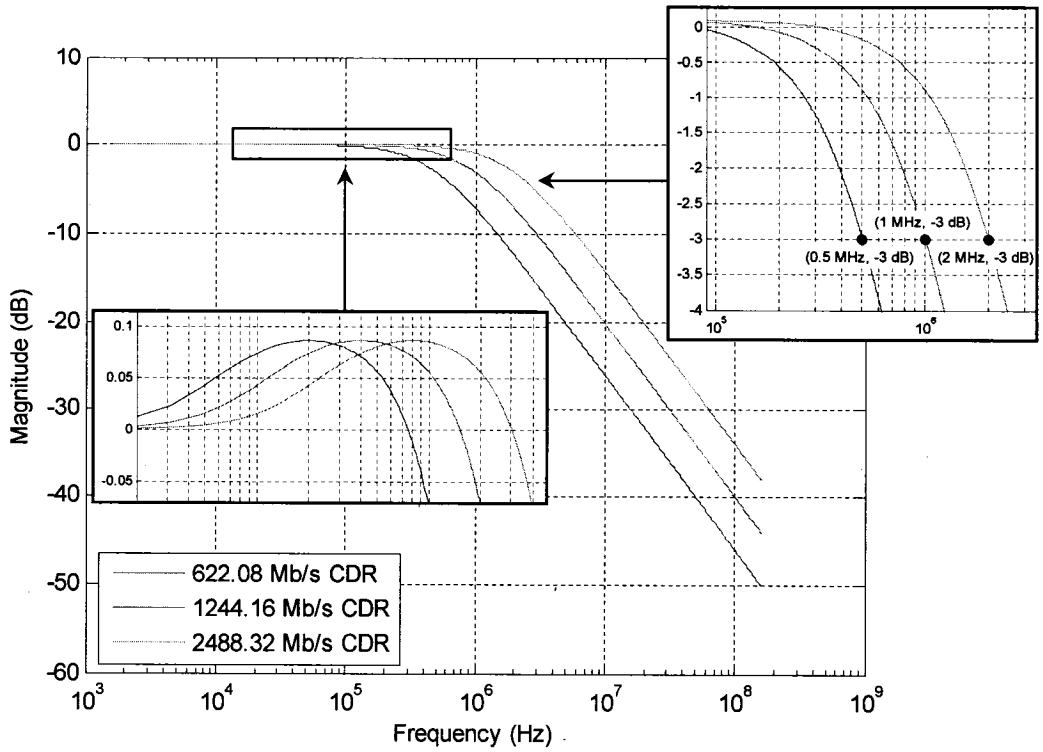

Fig. 5.5. Jitter transfer characteristic of three SONET CDRs. The input signal is assumed to be a PRBS (D_T = 1/2).

With the stability and SONET compliance of the CDRs verified, we can now evaluate their phase acquisition time by looking at their time-domain response. We apply, at $t = 0$, a phase step θ at the input:

$$\phi_i(t) = \theta u(t) \tag{5.9}$$

where $u(t)$ is the unit step function and ϕ_i is the input of the CDR in Fig. 5.1(b). The Laplace transform of (5.9) gives

$$\Phi_i(s) = \frac{\theta}{s} \tag{5.10}$$

The output phase, Φ_o, is obtained from

$$\Phi_o(s) = H(s)\Phi_i(s) \tag{5.11}$$

where $H(s)$ is from (5.3). The normalized response of the CDR to a phase step $\phi_i(t) = \theta$ is found by taking the inverse Laplace transform of (5.11). The result, for $\zeta > 1$, is [5][6]

$$\frac{\phi_o(t)}{\phi_i(t)} = 1 - e^{-\zeta\omega_n t}\left[\cosh\omega_n\sqrt{\zeta^2-1}\ t - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\omega_n\sqrt{\zeta^2-1}\ t\right] \quad (\zeta > 1) \qquad (5.12)$$

The CDR's response to a phase step, and hence its settling time, is independent of the size of the phase step *(θ)*. We therefore conclude that the settling time provides, at best, a relative measure of the phase acquisition time – we described and tested a more accurate measurement methodology in Section 4.2. We can nevertheless associate phase acquisition time with settling time, knowing only relative results make sense. Fig. 5.6 shows a plot of (5.12). The lowest rate CDR has the longest phase acquisition time. We will revisit this argument in Section 5.3.1 and will analyze the effect of transition density on settling time in Section 5.3.2.

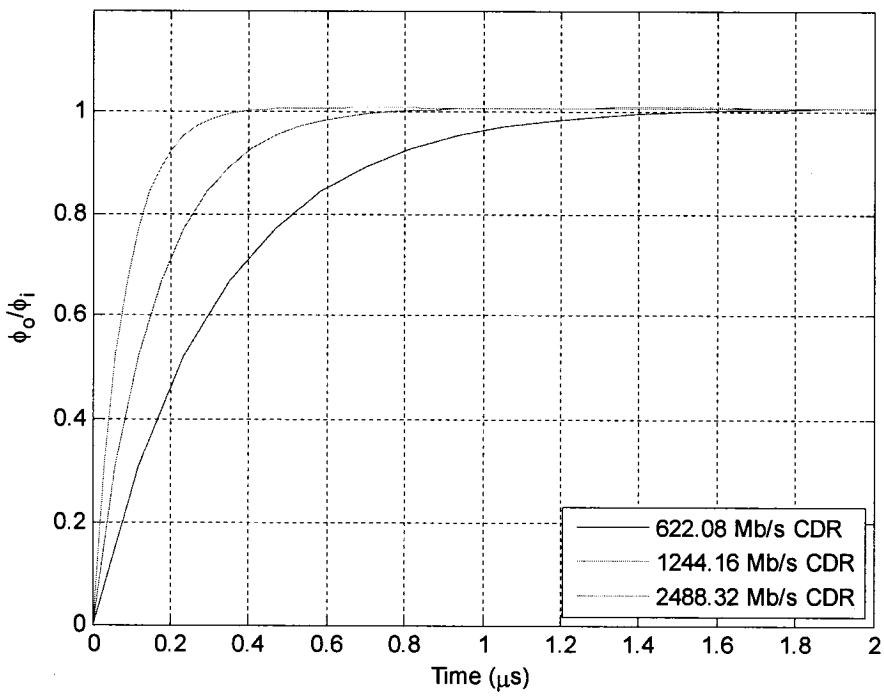

Fig. 5.6. Transient simulation of a phase step. The input signal is assumed to be a PRBS ($D_T = 1/2$).

5.2 CppSim model

In the previous section, we used the linear baseband model of Fig. 5.1(b) to derive the parameters of SONET compliant CDRs. We then used the model to plot the CDRs' response to a phase step. In order to simplify the analysis, the baseband model does not depend on the carrier frequency and assumes a locked CDR.

In this section, we look at CppSim, a time-domain simulator whose accuracy does not depend on the lock condition of the CDR. Another advantage of the CppSim models over the baseband model is their reusability in a system-to-circuit design flow. In the system design phase, the models are used to run purely behavioral simulations; in the circuit design phase, the same models are used to run mixed-level simulations. We developed basic behavioral models for each block of the CDR in Fig. 5.1(a). We verified the models by comparing, for a locked CDR, the results obtained with CppSim to the results obtained with the baseband model.

5.2.1 Test bench

Fig. 5.7 shows the test bench that we used to produce the simulation results of Section 5.2.2. All the blocks come from the cell libraries of CppSim, except the CDR. We designed our own CDR model using the schematic in Fig. 5.1(a). Within the CDR, the only custom block is the Hogge phase detector of Fig. 5.1(c), which we easily implemented using standard CppSim cells.

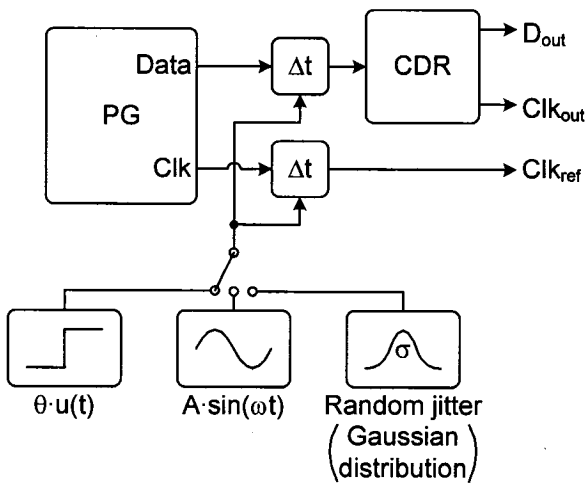

Fig. 5.7. Test bench for the CppSim simulations. The θ·u(t) block is to simulate the phase step response of the CDRs. The A·sin(ωt) block is for simulating the jitter transfer characteristic. The random jitter block is for simulating the jitter at the output of a chain of CDRs. Δt: delay cell.

5.2.2 Model verification

Simulating the jitter transfer characteristic of a CDR was straightforward with the baseband model. With a time-domain simulator, like CppSim, we obtained the jitter

transfer characteristic by taking the ratio of the output and input jitter amplitudes over a range of jitter frequencies. The same approach is used for experimental jitter transfer measurements. Fig. 5.8 shows simulation results for the OC-12 CDR. When the input jitter has a frequency of 0.5 MHz, it goes through the CDR with approximately 3 dB of attenuation. This is what we expected since the -3-dB bandwidth of the OC-12 CDR is 0.5 MHz. Note that in order to avoid bit errors at all frequencies of interest, we limited the input jitter amplitude to 0.1 UI, a value less then A_1 (0.15 UI) in Table 5.1.

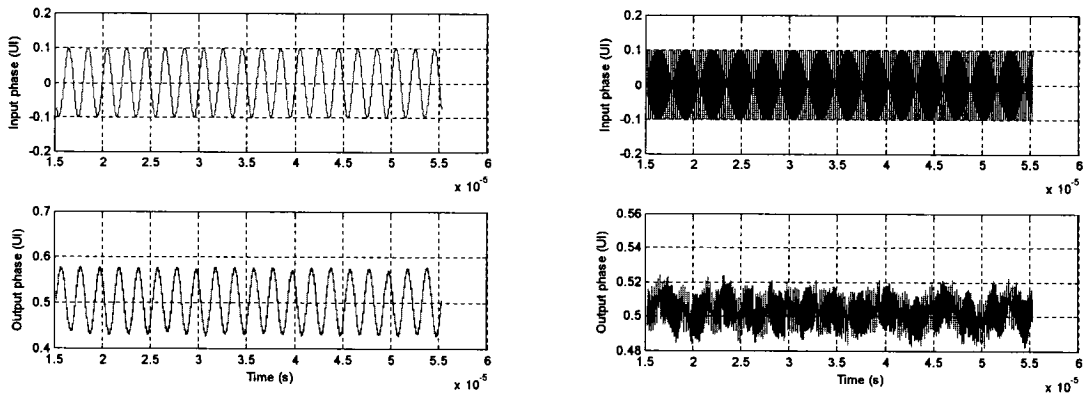

Fig. 5.8. Time-domain jitter transfer simulations. (a) Input jitter frequency = 0.5 MHz. (b) Input jitter frequency = 5 MHz.

Fig. 5.8(b) shows that the output jitter amplitude is very small for an input jitter frequency of 5 MHz. Above a certain jitter frequency, it became difficult to take the ratio of the output and input jitter amplitudes in the time domain. We therefore took the ratio in the frequency domain by computing the Fourier transform of the input and output phases. We ran simulations over a range of discrete jitter frequencies to obtain the jitter transfer characteristic of Fig. 5.9 (discrete points).

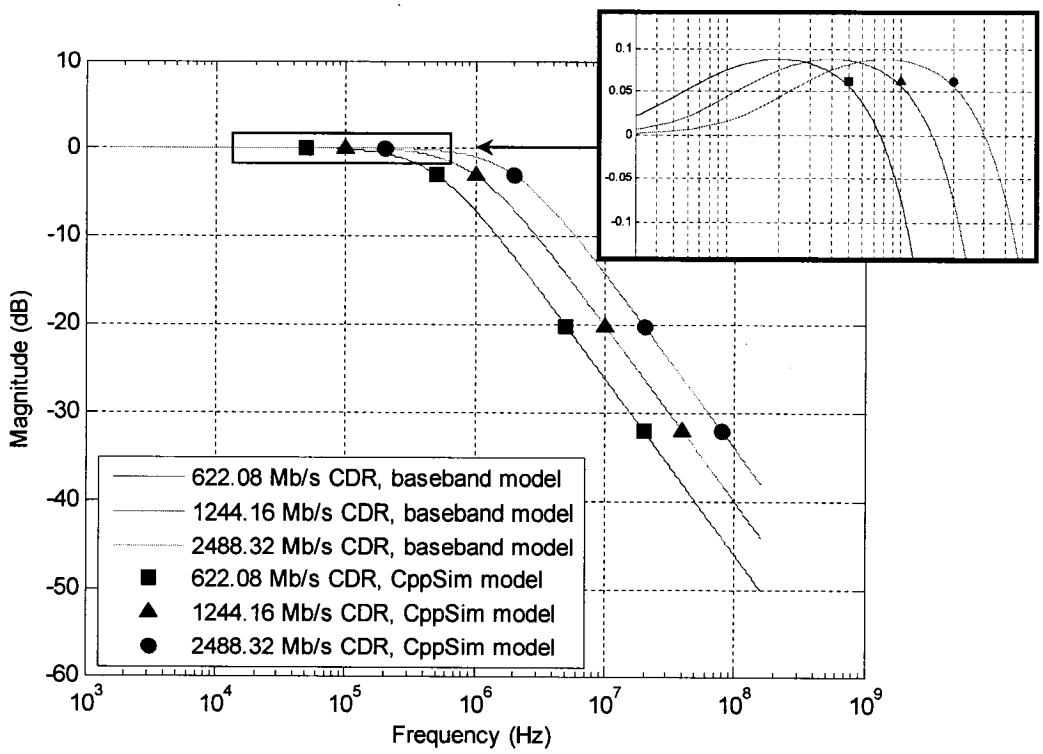

Fig. 5.9. Jitter transfer characteristic of three SONET CDRs (baseband vs. CppSim model). The input signal is assumed to be a 2^{11}-1 PRBS (D_T = 1/2).

We note in Fig. 5.9 a good agreement between the simulation results obtained with the baseband model (solid lines) and those obtained with CppSim. We also observe a good agreement for the CDRs' responses to a phase step (see Fig. 5.10). These simulation results confirm the accuracy of the simulation algorithm [1] used in CppSim. They also verify our basic CDR model, which could provide a base frame for modeling thermal noise, phase noise, and non-linearity effects. More accurate and realistic models would result, but this is beyond the scope of this thesis.

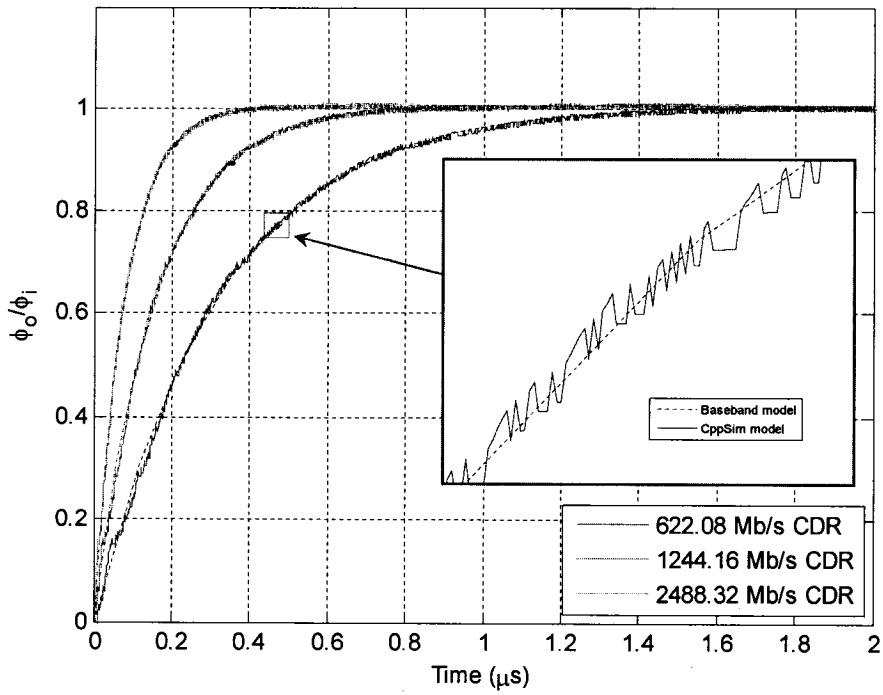

Fig. 5.10. Transient simulation of a phase step. The inset shows a good agreement between the baseband and CppSim models. The input signal is assumed to be a 2^{11}-1 PRBS.

5.3 Discussion

In this section, we use the CDR models that we developed to answer the following questions:

1. Does the phase acquisition time of a CDR depend on bit rate?
2. How does the phase acquisition time of a CDR vary with the preamble pattern? Does a 2× over sampling CDR settle faster or slower than a conventional CDR?
3. What is the jitter tolerance of the BM-CPA described in Section 4.2?
4. What does jitter look like at the end of a cascade of broadband CDRs similar to the one described in Section 4.1. How does jitter improve if the BM-CPA described in Section 4.2 replaces the broadband CDR?

5.3.1 Phase acquisition time vs. bit rate

In Section 5.1.2, we found that the OC-12 CDR had the longest phase acquisition time of the three SONET CDRs. In absolute time, this argument is true, but if we normalize the x-axis of Fig. 5.6 to the bit rate, we find that all 3 CDRs settle in the same number of bits [see Fig. 5.11]. Note that this conclusion holds only for CDRs that are scaled in a very specific way, like CDRs that meet the SONET specifications of Table 5.1.

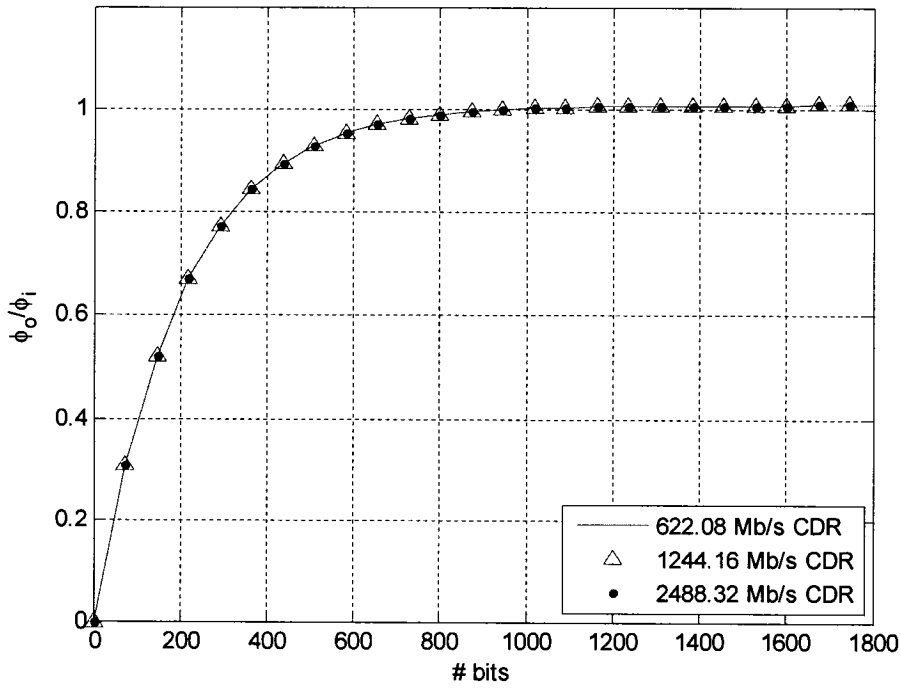

Fig. 5.11. CDRs' response to a phase step, normalized to bit rate. The input signal was a 2^{11}-1 PRBS. The input data rate is equal to the CDR operating rate for all three CDRs.

5.3.2 Phase acquisition time vs. preamble pattern

In this section, we study the impact of the preamble pattern on the phase acquisition time (settling time) of a CDR. We also determine the impact of 2× over sampling on settling time. We first derive an analytical approximation for the settling time of a CDR, and then analyze the exact solution graphically.

For $\zeta >> 1$, (5.12) simplifies to

$$\frac{\phi_o(t)}{\phi_i(t)} \approx 1 - e^{-\zeta\omega_n t}\left[\cosh\zeta\omega_n t - \sinh\zeta\omega_n t\right] \quad (\zeta >> 1) \tag{5.13}$$

where

$$\cosh x = \frac{e^{x} + e^{-x}}{2} \tag{5.14}$$

and

$$\sinh x = \frac{e^{x} - e^{-x}}{2} \tag{5.15}$$

Substituting (5.14) and (5.15) in (5.13), we get

$$\frac{\phi_o(t)}{\phi_i(t)} = 1 - e^{-2\zeta\omega_n t} \quad (\zeta >> 1) \tag{5.16}$$

In order for $\phi_o(t)/\phi_i(t)$ to settle to within d% of its final value, we let $e^{-2\zeta\omega_n t} = d$. Hence,

$$t = \frac{1}{-2\zeta\omega_n}\ln(d) \tag{5.17}$$

If we plug (5.4) and (5.5) into (5.17), we find that the settling time is inversely proportional to data transition density, D_T. We verified this analytical conclusion by simulating an OC-12 CDR with two different preambles: the '1010' pattern (D_T = 1), and a PRBS (D_T = 1/2). Fig. 5.12 shows the simulation results (blue and red curves). Note that the '11001100' pattern is equivalent to a PRBS as far as transition density is concerned (1/2 in both cases) – see the inset of Fig. 5.12. As expected, the '1010' pattern gives the shortest settling time.

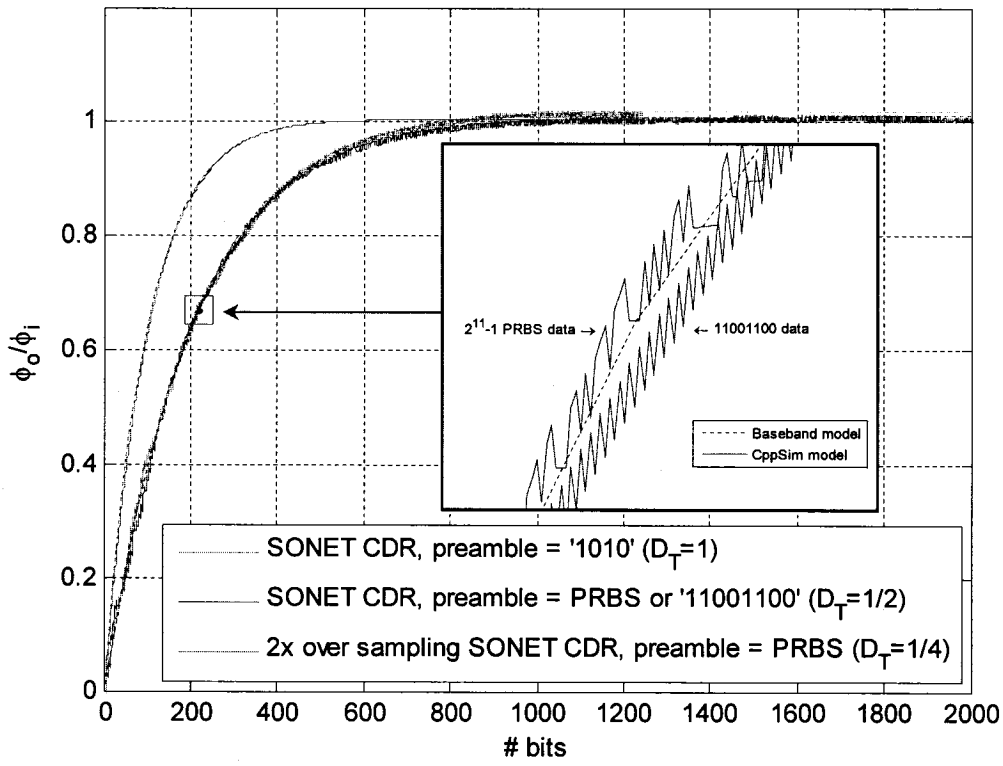

Fig. 5.12. Phase step response of a 622.08 Mb/s SONET CDRs and a 2× over sampling SONET CDR for different preambles.

We then verified the impact of 2× over sampling on settling time. For a PRBS input, a 2× over sampling CDR sees a transition density of 1/2×1/2 = 1/4, compared to 1/2 for a conventional CDR. Simulation results appear in Fig. 5.12 (magenta curve). A 2× over sampling CDR, despite seeing a lower data transition density for a given input pattern, settles as fast as a conventional SONET CDR. In other words, there is no settling time penalty caused by 2× over sampling. Moreover, as we saw in Section 4.2.4.1, instantaneous phase recovery (0 bit) could be achieved when 2× over sampling is combined with an appropriate phase picker.

5.3.3 Jitter tolerance of the BM-CPA

For OC–N interfaces, jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter (applied on the input signal) that causes a 1-dB power penalty (BER < 10^{-10}) [3]. There is a tradeoff between the jitter transfer bandwidth and the jitter tolerance requirements of a CDR. A low bandwidth is desirable to filter out input jitter, but the

CDR is best able to track out incoming jitter by having the widest possible bandwidth. The jitter transfer bandwidth must therefore be as high as possible while still meeting the jitter transfer specification across all temperature and process variations.

Since jitter tolerance must be measured at a very low error rate ($< 10^{-10}$), it is difficult (if not impossible) to simulate directly. In practice, it is common to focus only on the simulation of jitter transfer and jitter generation and assess the jitter tolerance in an indirect way. We take this approach to analyze the jitter tolerance of the BM-CPA described in Section 4.2.

We assume that the input of the BM-CPA is a PRBS pattern at 622.08 Mb/s. To achieve 2× over sampling, the BM-CPA uses a 1244.16 Mb/s SONET CDR. For such a CDR, the fourth corner frequency (f_4) of the jitter tolerance mask is 500 kHz (see Table 5.1). For a 622.08 Mb/s SONET CDR, f_4 is half (250 kHz). One could argue that the BM-CPA is more jitter tolerant than a conventional CDR, but this argument neglects the effect of transition density (D_T). The specifications in Table 5.1 assume that $D_T = 1/2$, whereas the BM-CPA sees a transition density of 1/4 (see Section 5.3.2). Hence, according to (5.7), the 2× over sampling CDR has the same bandwidth as a conventional CDR. This is confirmed by Fig. 5.13, which plots the jitter transfer characteristic of the two CDRs. Note that the -3-dB bandwidths are approximately equal, but that the jitter peaking of the 2× over sampling CDR is 0.07 dB higher than that of the conventional CDR (0.16 dB vs. 0.09 dB).

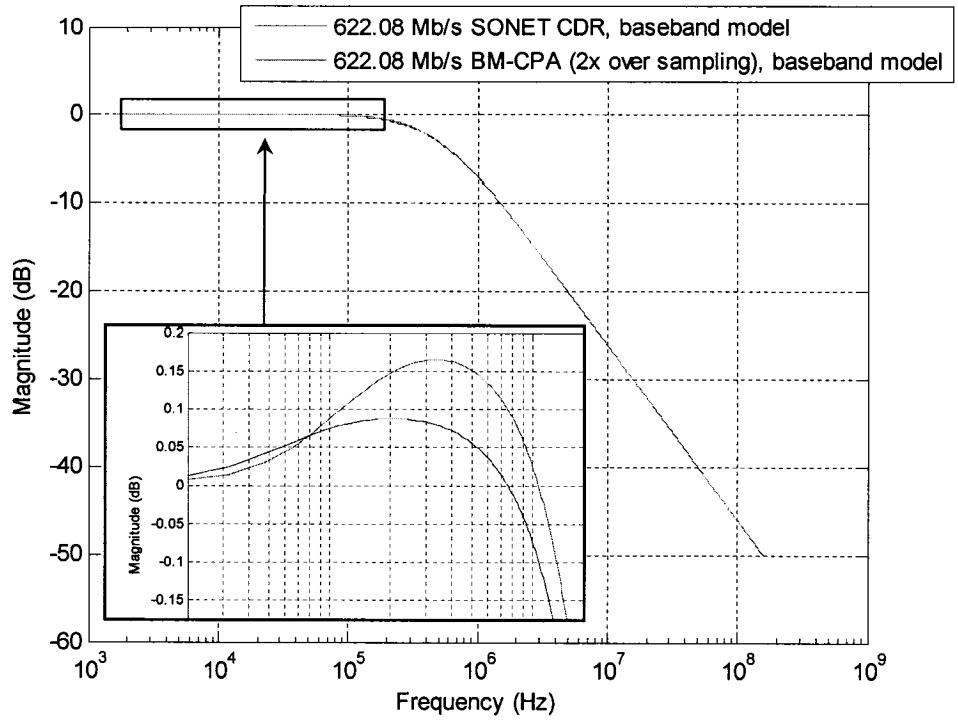

Fig. 5.13. Comparison of the jitter transfer characteristic of a 622.08 Mb/s SONET CDR and a 622.08 Mb/s BM-CPA using 2× over sampling.

To estimate the jitter tolerance of the BM-CPA, we use the fact that the fourth corner frequency (f_4) of the jitter tolerance mask is half the bandwidth of the CDR (f_c) – see Table 5.1. Since the BM-CPA has the same bandwidth as a conventional CDR, we conclude that it must have a similar jitter tolerance.

5.3.4 Jitter transfer of multiple broadband CDRs vs. BM-CPAs

In Chapter 4, we described the implementation and testing of two burst-mode clock and data recovery circuits: a broadband CDR, and a BM-CPA. We stated in Section 4.2.1 that the BM-CPA could be cascaded to support applications like burst/packet switched networks. On the other hand, we argued that a broadband CDR, because of its high jitter transfer bandwidth and jitter peaking, would not be appropriate for such applications.

Our goal in this section is three-fold. First, we describe the model of a broadband CDR similar to the one of Chapter 4. Second, we simulate the jitter at the output of three chains of CDRs, one using SONET CDRs (the reference), one using BM-CPAs, and one

using broadband CDRs. Third, we will use this numerically intensive simulation to demonstrate and report on the speed of the CppSim simulator in the conclusion.

5.3.4.1 Broadband CDR model

Table 5.3 shows the parameters of a 622.08 Mb/s broadband CDR having a jitter transfer bandwidth of 28 MHz and a jitter peaking of 1.44 dB. We repeated the parameters of the 622.08 Mb/s SONET CDR for the sake of comparison. The broadband CDR has a jitter transfer bandwidth that is approximately 56 times larger than that of the SONET CDR (0.5 MHz). Jitter peaking is 1.32 dB higher than the maximum peaking allowed for a SONET CDR (0.1 dB).

Table 5.3
Parameters for the broadband CDR

CDR parameter	Broadband CDR (622.08 Mb/s)	OC-12 CDR (622.08 Mb/s)
I_P	62.5 μA	62.5 μA
K_{VCO}	500 MHz/V	500 MHz/V
R_1	8.04 kΩ	201.06 Ω
C_1	4.30 pF	137.48 nF
C_2	$C_1/20$	$C_1/20$[1]
ζ[2]	1.04	4.66
ω_n[2]	60.3×10^6 rad/s	0.337×10^6 rad/s

[1] C_2 is only included in the 3rd-order baseband model. It is neglected in the 2nd-order baseband model.

[2] ζ and ω_n were calculated for the 2nd-order models.

To derive the parameters of the broadband CDR, we used the 2nd-order baseband model of Fig. 5.1(b). We then added capacitor C_2, which turned the model into a 3rd-order model. The function of C_2, as we stated earlier, is to filter out the ripples at the input of the VCO. Without C_2, the phase step response for the time-domain simulation was buried

in excessive jitter because of the high bandwidth of the CDR. The 3rd-order open-loop transfer function[1] is [7]

$$L(s)=\left.\frac{\Phi_{out}}{\Phi_{in}}\right|_{open}=\frac{K_{VCO}I_P}{2\pi}\frac{s+\dfrac{1}{R_1C_1}}{C_2s^2\left(s+\dfrac{1}{R_1[C_1C_2/(C_1+C_2)]}\right)} \tag{5.18}$$

The jitter transfer characteristic of the broadband CDR appears in Fig. 5.14, together with that of the SONET CDR and the BM-CPA for the sake of comparison. There is a good agreement between all three broadband CDR models: the 2nd-order baseband model (C_2 neglected), the 3rd-order baseband model (C_2 included), and the CppSim model (C_2 included).

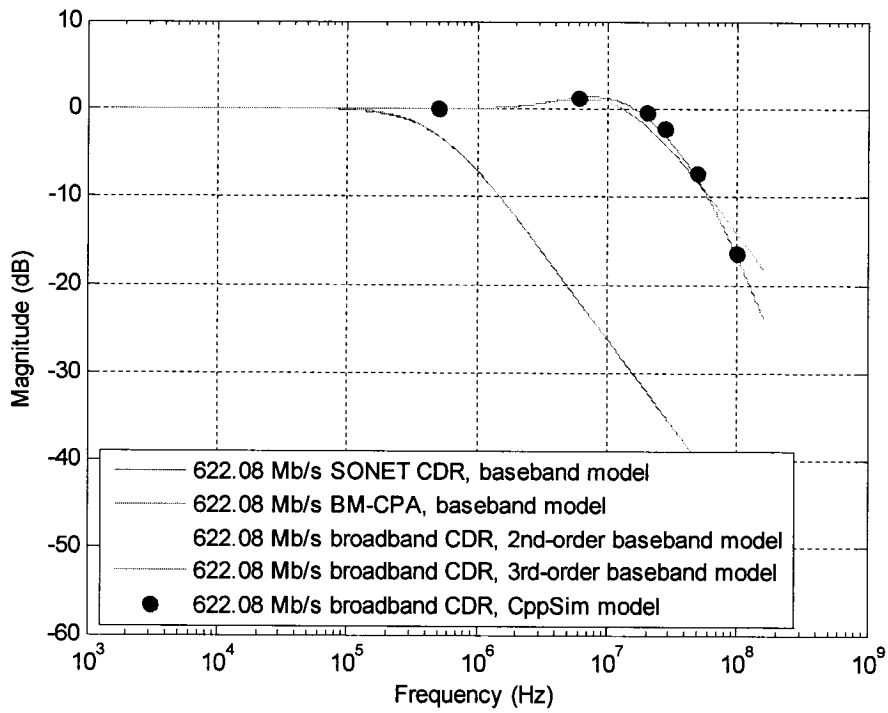

Fig. 5.14. Jitter transfer characteristic of the broadband CDR.

We draw the following two conclusions from Fig. 5.14:

[1] The 3rd-order model is more accurate than the 2-order model. Because of its simplicity, the 2nd-order model is nevertheless useful to derive the parameters of a CDR that must meet a given set of specifications.

- The 2nd- and 3rd-order baseband models give similar results. This verifies the assumption that we made in Section 5.1.1, namely that C_2 could be neglected if it is smaller than one fifth to one tenth of C_1.
- Simulation results obtained with the baseband and CppSim models are in good agreement. This verifies the CppSim model, which we will use to simulate the jitter at the output of a cascade of broadband CDRs.

To verify the stability of the broadband CDR, we plotted in Fig. 5.15 the bode diagram of the 3rd-order open-loop transfer function. The phase margin is 65.3°. An optimal choice of the capacitor ratio C_1/C_2 leads to a phase margin that is relatively immune to process and temperature variations.

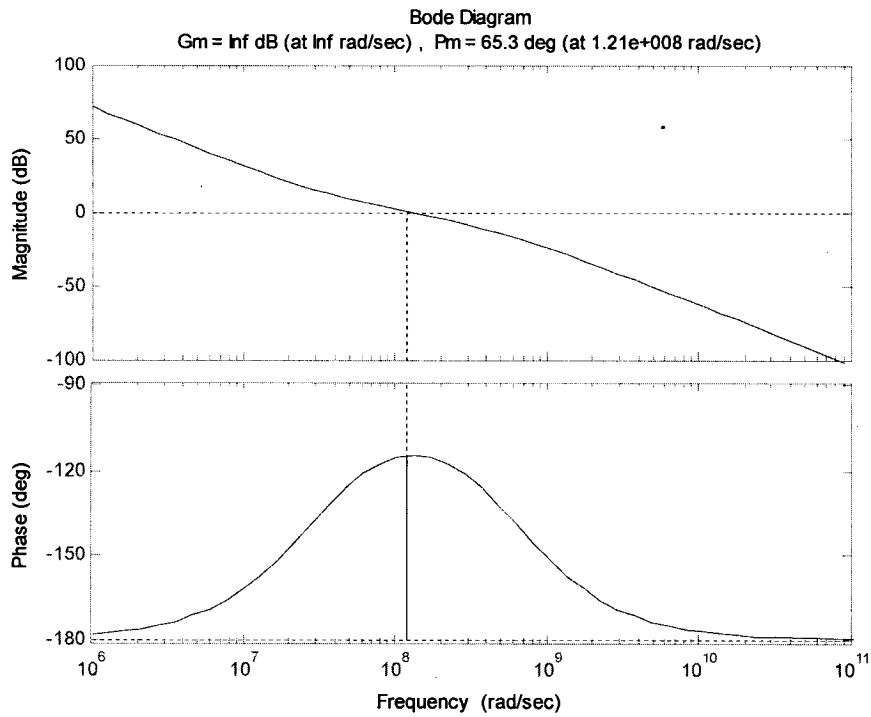

Fig. 5.15. Bode diagram of the 622.08 Mb/s broadband CDR.

Fig. 5.16 plots the phase step response of the broadband CDR, the SONET CDR, and the BM-CPA. For the SONET CDR and the BM-CPA, the settling time to within 2% of the steady-state value is 697 bits. The broadband CDR, in comparison, settles in only 56 bits. As we will see in the next section, this 12-fold improvement was obtained at the expense of less jitter rejection and more jitter peaking.

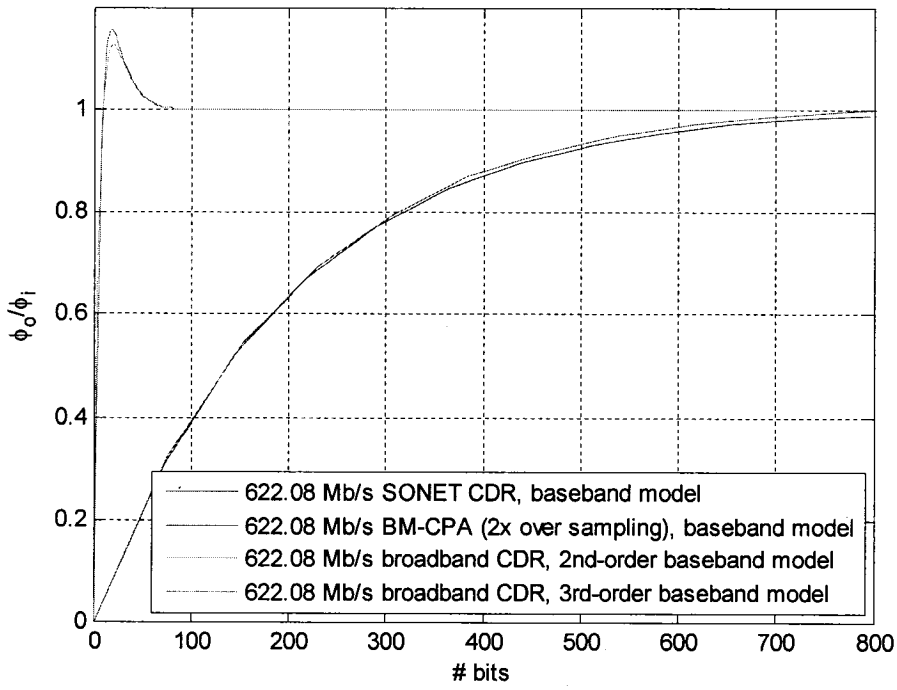

Fig. 5.16. Phase step response of the broadband CDR compared to the phase step response of the SONET CDR and the BM-CPA. The bits on the x-axis have a period of $1/(622.08\times10^6)$.

5.3.4.2 Simulation results

Using CppSim, we simulated three chains of eight CDRs. Each chain uses one of the following CDRs:

- 622.08 Mb/s broadband CDR;
- 622.08 Mb/s BM-CPA (without the phase picker);
- 622.08 Mb/s SONET CDR.

The input to the chains of CDRs is a 2^{11}-1 PRBS at 622.08 Mb/s (see Fig. 5.17). For a more realistic simulation, we added 63 ps RMS jitter (Gaussian distribution) to the input signal. This is the same amount of jitter as we used for our experimental measurements on the BM-CPA (see Fig. 4.11). The test bench is similar to that shown in Fig. 5.7, with the random jitter block controlling the delay blocks.

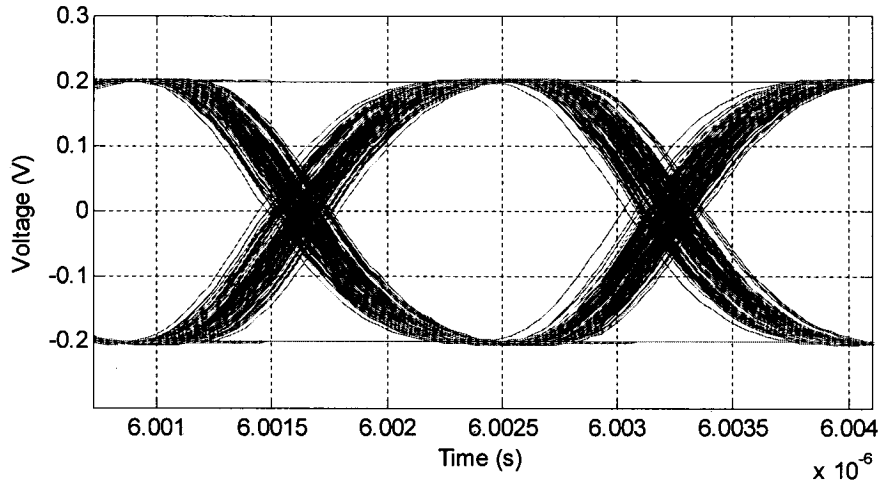

Fig. 5.17. Input signal (2^{11}-1 PRBS at 622.08 Mb/s) with random jitter (63 ps RMS).

Figs. 5.18(a) and (b) show the output of the first and eighth CDRs in the chain, respectively. It is clear from the simulation results that a broadband CDR would not be suitable for applications requiring long chains of BM-CDRs. On the other hand, the BM-CPA inherits the good jitter characteristics of the SONET CDR from which it is built and could be daisy chained multiple times.

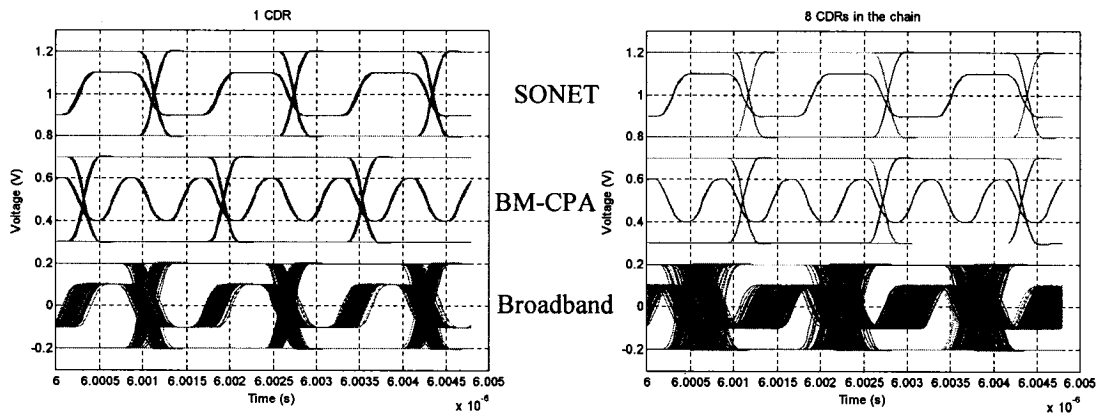

Fig. 5.18. Simulation of three chains of eight 622.08 Mb/s CDRs, each chain using a different type of CDR. (a) output of the first CDR in the chain, (b) output of the eighth CDR.

To get more insight in the performance of each CDR, we plotted the equivalent transfer function of eight of them in Fig. 5.19. Jitter peaking is 0.69 dB for the SONET CDRs, compared to 1.32 dB for the BM-CPAs and 11.53 dB for the broadband CDRs. The jitter transfer bandwidth of a chain of CDRs is smaller than that of a single CDR.

This explains why, in Fig. 5.18, the signal at the output of 8 SONET CDRs and 8 BM-CPAs is less jittery than after only one. After 10's of CDRs, the negative effects of jitter peaking would dominate the benefits of a lower jitter bandwidth. Consequently, the jitter increases and limits the number of CDRs that can be daisy chained. On the other hand, the large jitter peaking of the broadband CDR quickly dominates over the reduced jitter bandwidth. This explains why we observe a very jittery signal after only 8 CDRs in the chain.

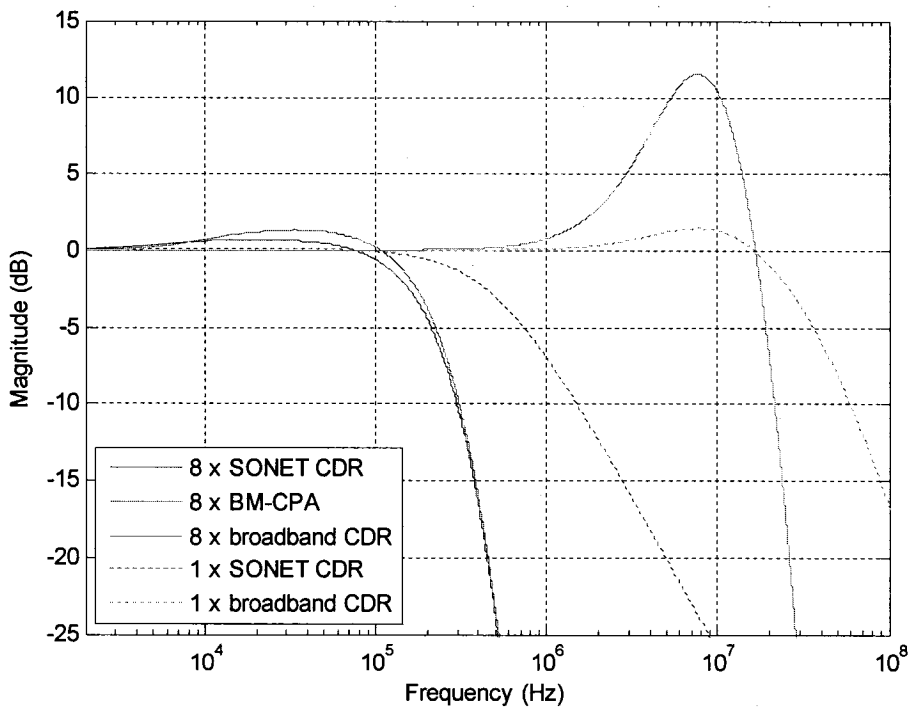

Fig. 5.19. Jitter transfer characteristic of a chain of eight CDRs for three types of 622.08 Mb/s CDRs. The jitter transfer characteristic for a single CDR is provided for reference. Note that the plot for 1 × BM-CPA is not shown because it is almost identical to the plot for 1 × SONET CDR (see Fig. 5.13).

5.4 Conclusion

We list in Table 5.4 the simulation time for some of the results obtained with CppSim in this chapter. The accuracy of the simulation results and the speed at which they can be obtained make CppSim an interesting alternative or complement to Verilog-A/AMS for mixed-level simulations in Cadence, especially for PLLs and CDRs. The basic CDR model that we developed can serve as a base frame for more realistic and accurate

models. Model refinement could be part of a top-down design, bottom-up verification methodology, where behavioral models are refined as the performance characteristics of each block of the CDR become available from transistor-level simulations.

Table 5.4
Time to complete three types of simulation on an OC-12 CDR using CppSim[1]

	Jitter transfer	Phase step	3 chains of 8 CDRs[2]
Transient simulation time	8 μs	8 μs	8 μs
Time step	1.6 ns[3]	1.6 ns	1.6 ns
Time to complete the simulation	9 s[4]	2 s	21 s

[1] The simulations were performed using a 2.6 GHz Pentium IV PC with 1 GB of memory.
[2] In addition to 8 SONET CDRs, 8 BM-CPAs and 8 broadband CDRs were also simulated.
[3] 1.6 ns corresponds to 50 points per cycle at 622.08 Mb/s.
[4] This is the time to simulate four discrete jitter frequencies, as in Fig. 5.9.

The models that we developed and verified in this chapter allowed us to compare SONET CDRs, BM-CPAs, and broadband CDRs in terms of their jitter characteristics and phase acquisition time. While it is clear that SONET CDRs are the most suitable for applications requiring long chains of CDRs, the BM-CPA performs almost as well and has the advantage of supporting burst-mode applications. Broadband CDRs are an alternative, but their high jitter peaking and jitter transfer bandwidth precludes their use in long chains of CDRs.

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CHAPTER 6

Conclusions

6.1 Summary

PONs are considered one of the most promising technologies for the deployment of fiber-to-the-home infrastructures. Current access technologies, including DSL, VDSL, and cable, use a point-to-point network topology. In contrast, PONs are point-to-multipoint, which creates unique challenges for the design and test of receivers.

We identified some key research problems in Chapter 1, reviewed existing solutions in Chapter 2, and presented original solutions in Chapters 3 to 5. We gave a list of original contributions in Section 1.4, which we summarize in Fig. 6.1. Each contribution belongs to one of three research areas: OCDMA receivers, burst-mode test solutions, or burst-mode receivers. For convenience, we indicated the relevant thesis section and publication under each contribution.

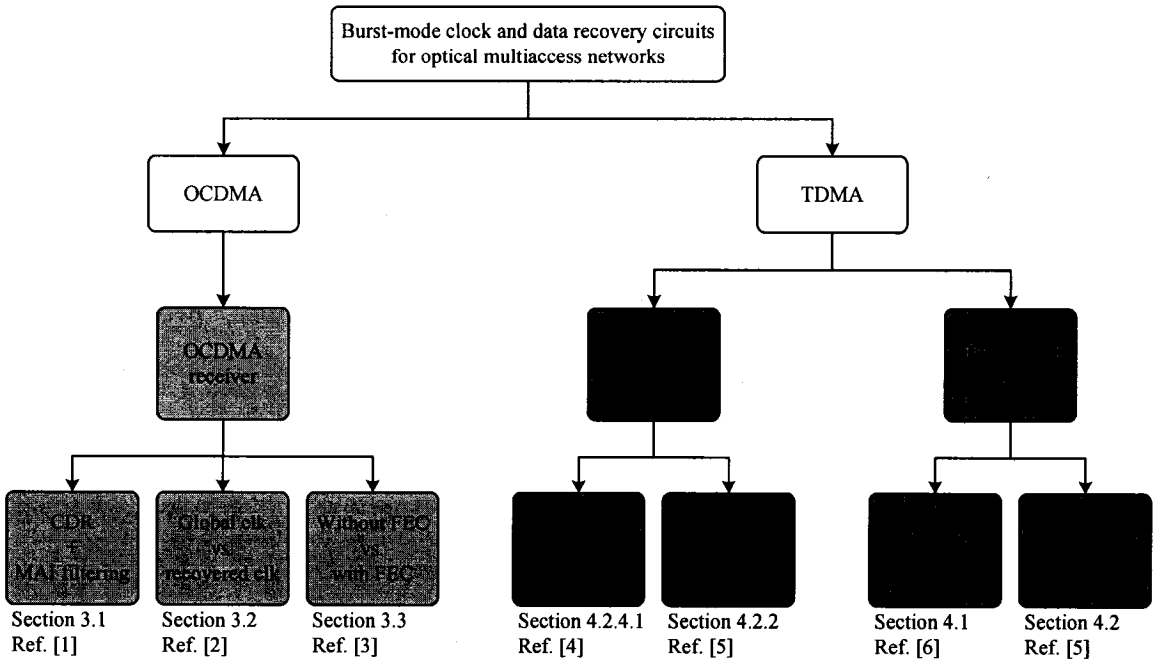

Fig. 6.1. Summary of the work described in this thesis. Chapter 5 (behavioral simulations + jitter analysis) is a subset of the work on burst-mode CDRs and does not appear in the figure.

In this thesis, we described CDR circuits for two access methods: OCDMA and TDMA.

OCDMA

We presented the design of a 155.52 Mb/s OCDMA receiver for 2D λ-t OCDMA networks. The first version of the receiver [1], [2] used 2× over sampling and required manual selection of the payload chips. We used over sampling because of the unavailability of a 1:8 deserializer to match the number of chips per bit. We measured a power penalty of approximately 3 dB when using the recovered clock instead of the global clock [2]. The power penalty originates from 2× over sampling, which causes the CDR to sample the chips on each side of the optimum sampling point. We fixed this problem in version 2 of the design [3], in which we used an FPGA to process the output of the 1:16 deserializer and emulate a 1:8 deserializer. The CDR could therefore run at the same rate as the chip rate for optimum sampling. We obtained a negligible power penalty with version 2 of the receiver [see Fig. 3.9(a)]. Two more features of the receiver are: 1) automatic detection of the payload chips and 2) RS(255, 239) decoding. When the link is first established, the receiver automatically identifies the payload chips and forwards

them to the RS decoder for error correction. Error correction provided ~3 dB of coding gain, which we used to increase the number of error free users from 2 to 5 [3].

TDMA

We designed a burst-mode test solution that we debugged and tested using conventional SONET CDRs. Our test methodology consisted in using a delimiter and a comma as gating signals for burst BER measurements. Pattern synchronization is performed at the beginning of every packet. This overcomes the limitations of conventional test equipment, which require continuous synchronization. Only payload bits contribute to the BER. Commas that do not pair up with a delimiter increment the packet lost counter by one. We measured the phase acquisition time of a CDR by increasing the length of the preamble until we obtained error free operation for any phase step. This test methodology allowed us to measure the phase acquisition time of CDRs down to an accuracy of one bit.

We also described the design of two burst-mode CDRs. The first design was a broadband CDR [6]. We reduced the settling time of the CDR by increasing its bandwidth. We experimentally confirmed the trade off between settling time and jitter. The CDR required Manchester coding, otherwise it lost frequency and/or phase lock very quickly. The two conclusions that we drew from the design and test of the broadband CDR are 1) the need for a high transition density, and 2) poor jitter characteristics. In an attempt to solve these problems, we designed a BM-CPA based on 2× over sampling and a novel phase picking algorithm [5]. The BM-CPA provides instantaneous phase acquisition (0 bit).

We finally performed behavioral simulations to determine the theoretical jitter characteristics of the BM-CPA. Our simulation results indicate that the BM-CPA has the same jitter transfer bandwidth and jitter tolerance as a SONET CDR.

6.2 Future research

In this section, we propose a few research directions that could derive from the work presented in this thesis.

BM-CPA

- *Scale the BM-CPA to 5 and 10 Gb/s:* To design the 622/1244 Mb/s BM-CPA presented in this thesis, we used a 1244/2488 Mb/s multirate CDR to achieve 2× over sampling. In order to scale the design to 5 Gb/s, one could use a 10 Gb/s (OC-192) CDR and a 10 Gb/s 1:16 deserializer. Both of these components are commercially available. The LVDS input buffers on the Virtex II Pro FPGA from Xilinx support a maximum data rate of 840 Mb/s (420 MHz). Since the parallel output interface of the deserializer is 16 channels × 622 Mb/s/channel, the same FPGA could be used to implement the phase picking algorithm and the custom burst BER tester. Note that the divided clock at the output of the deserializer is running at 622 MHz. Since this frequency is higher than 420 MHz, the data will have to be clocked into the FPGA using the double data rate (DDR) functionality of the LVDS buffers. The design may not scale easily to 10 Gb/s or more because of the really fast electronics involved. One could nevertheless attempt the design of a 10 or 20 Gb/s BM-CPA using a 20 or 40 Gb/s CDR, respectively.
- *Test the BM-CPA in combination with a BM-RX:* This would demonstrate a full burst-mode solution for both amplitude and phase recovery.
- *Add FEC to the BM-CPA:* One could use the same RS(255, 239) decoder as we used in the design of the OCDMA receiver.
- *Measure the frequency acquisition time of the BM-CPA:* This measure will be useful for burst/packet switched networks, which may not impose a limit on the number of consecutive identical digits (CIDs), like GPON. With too many CIDs, the BM-CPA will start drifting and eventually lose frequency lock. Frequency acquisition must be taken into account in the determination of the preamble length. The test methodology described in Section 4.2.2.3 could be used for measuring the frequency acquisition time. The BM-CPA should be unlocked before its frequency acquisition time is measured. To unlock the BM-CPA, all the bits of packet 1 should be set to zero in Fig. 4.9. Note that the measure will include both frequency and phase acquisition times. It should nevertheless be a very good estimate because frequency acquisition is a process that takes much longer than phase acquisition.

- *Measure the jitter transfer bandwidth, jitter peaking, and jitter tolerance of the 622/1244 BM-CPA:* In Section 5.3.3, we demonstrated theoretically that the jitter tolerance of the 622.08 Mb/s BM-CPA is similar to that of a 622.08 Mb/s SONET CDR. We also demonstrated that the BM-CPA, despite using a 1244.16 Mb/s CDR, had the same jitter transfer bandwidth (0.5 MHz) as a 622.08 Mb/s SONET CDR. These theoretical results should be compared to experimental results – a jitter analyzer will be required for the measurements.

OCDMA receiver

- *Add burst-mode functionalities to the OCDMA receiver:* The current design assumes no amplitude and phase fluctuations. In a real P2MP OCDMA network, packets will travel different distances and arrive asynchronously at the receiver. To support amplitude steps, the receiver should adjust its threshold automatically 1) as MAI fluctuates due to the increase or decrease of user activity on the network, and 2) at the arrival of a new packet. To support phase steps, the receiver should phase lock as close to instantaneously as possible.
- *Scale the OCDMA receiver to 1.25 Gb/s:* The current design is rated at 155 Mb/s and supports 8 chips per bit. The design could be scaled to 1.25 Gb/s using an OC-192 (10 Gb/s) CDR.
- *Replace the RS(255, 239) decoder by a turbo decoder:* Turbo codes are known to provide a coding gain near the Shannon capacity. Decoding turbo codes is more complex than decoding RS codes. Therefore, it may not be possible to synthesize a 155 Mb/s turbo decoder on the Virtex II Pro FPGA from Xilinx. One could measure the coding gain of various other FEC codes (e.g. Golay, BCH, Viterbi, etc.) using the current OCDMA receiver architecture.

Measurement of phase acquisition time

- *Correlate the settling time of a CDR to its phase acquisition time:* One popular way of estimating the phase acquisition time of a CDR is to monitor the controlling voltage of the voltage-controlled oscillator (VCO). The settling time corresponds to the time required for the envelope of the signal to settle to within x% of the steady state value, where x is an arbitrary value (usually 2 to 5%). In Section 4.2.2.3, we described a

measurement methodology to determine the phase acquisition time of a CDR down to an accuracy of one bit. It may be possible to use the accurate measurement of phase acquisition time to derive the following function: BER = f(x), where we are interested in finding the function that relates x, the offset from the steady state value, to BER.

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