WIDE-TEMPERATURE RANGE CMOS INTERFACE CIRCUITS FOR CAPACITIVE MEMS SENSORS

Yucai Wang

Department of Electrical and Computer Engineering

McGill University, Montreal, Canada

June, 2015

A thesis submitted to McGill University in partial fulfillment of the requirements of the degree of Doctor of Philosophy

ACKNOWLEDGEMENTS

I would first and foremost like to thank my advisor, Dr. Vamsy P. Chodavarapu, for his supervision, guidance, constant encouragement and inspiration during my Ph.D. studies. Without his support, this work would not have gone through. It was my great honor and pleasure to work with him.

I would also like to thank my Ph.D. supervisory committee members, Dr. Zetian Mi and Dr. Ishiang Shih, for their valuable comments and help towards my Ph.D. research projects.

I would like to thank all my previous and current colleagues in the Sensor Microsystems Laboratory for their assistance during the past four years. Special thanks go to Adel Merdassi for his help in the French abstract.

I acknowledge the financial support provided by the Natural Sciences and Engineering Research Council of Canada (NSERC) and McGill Engineering Doctoral Awards (MEDA) program. I would like to thank the fabrication service and CAD tool support provided by Canadian Microelectronics Corporation (CMC).

I am deeply indebted to my parents for their everlasting support and encouragement. Finally, the most important, I would like to thank my wife Mingqin for her constant love and patience. I wish to dedicate this thesis to my newborn daughter, Helene. I wish her a joyful life ahead with liberty, freedom, and dignity.

TABLE OF CONTENTS

ABSTRACT

Many applications require MEMS sensors to operate over wide temperature range, typically from -55 ºC to 225 ºC. It is desirable to place the sensor readout circuits in close proximity to the sensor devices to improve signal-to-noise ratio and system reliability. Therefore, the sensor readout circuits must also be able to function over the same temperature range as the sensor devices. The main challenges for designing CMOS sensor readout circuits working over wide-temperature range (especially at the high temperature end) include: 1) increased junction leakage current, 2) reduced carrier mobility, and 3) decreased threshold voltage in MOS transistors. In this thesis, constant-g_m biasing and other design techniques are used to mitigate the circuit performance degradation at high temperatures and three readout circuits for capacitive MEMS sensors are developed using standard CMOS process which can operate over wide temperature range from -55 ºC to 225 ºC.

First, several proof-of-concept core building blocks are designed and tested, including a constant-g_m biasing circuit, a single-ended folded-cascode amplifier, and a fully-differential folded-cascode amplifier with a switched capacitor common mode feedback circuit. The single-ended folded-cascode amplifier showed DC gain of 68.5 dB at 225 °C and DC gain variation of 2.8 dB from -20 °C to 225 °C. The fully-differential folded-cascode amplifier with the switched capacitor common mode feedback circuit showed a DC gain of 68.9 dB and DC gain variation of 2.1 dB from -20 °C to 225 °C.

Then, using these core building blocks, three readout circuits for capacitive MEMS sensors were constructed, including: 1) a differential capacitance to voltage readout circuit for sensors with a wide range of the steady-state capacitance values from 0.5 pF to 10 pF, 2) a capacitance to frequency readout circuit which converts the sensor capacitance into digital pulse signal modulated in frequency, and 3) a capacitance to digital readout circuit which uses a sigma-delta technique to convert the input ratio between sensor capacitance and reference capacitance into a high-accuracy digital output. All these three capacitive sensor readout circuits are simulated over temperature range from -55 °C to 225 °C and tested over temperature range from -20 °C to 225 °C. Measurement results show that these circuits have good accuracy and temperature stability over the wide temperature range.

All the circuits developed in this thesis are implemented using IBM 0.13 μm standard CMOS technology which incorporates a 2.5 V power for the advantages of high level of integration and low power consumption. The design techniques used here are universal and they can be readily ported to other standard CMOS processes and even SOI processes. Future improvement and development for these circuits are proposed. More sophisticated sensor readout circuits could be built based upon the prototypes developed in this thesis.

RÉSUMÉ

De nombreuses applications nécessitent des capteurs MEMS pour fonctionner sur une large plage de température, typiquement entre -55 ºC à 225 ºC. Il est souhaitable de placer les circuits de conditionnement des capteurs à proximité des dispositifs de détection afin d'améliorer le rapport signal sur bruit et la fiabilité du système. Par conséquent, les circuits de conditionnement des capteurs doivent également être en mesure de fonctionner sur la même plage de température que les dispositifs de détection. Les principaux défis pour la conception de circuits de conditionnement pour capteur CMOS fonctionnant sur une large plage de température (surtout à la fin haute température) sont : 1) courant de fuite de jonction croissant, 2) réduction de la mobilité des porteurs de charge, et 3) diminution de la tension de seuil des transistors MOS. Dans cette thèse, la polarisation constante g ainsi que d'autres techniques de conception sont utilisées pour atténuer la dégradation des performances du circuit à des températures élevées ainsi que trois circuits de conditionnement dédiés à des capteurs capacitifs MEMS ont été développés en utilisant le procédé standard CMOS qui peut fonctionner sur une large plage de température de -55 ºC à 225 ºC.

En premier lieu, quelque blocks de construction de base preuve de concept sont conçus et testés, y compris un circuit de polarisation à base de constante-g_m, un amplificateur en amont mis en cascade avec un amplificateur différentiel sont entièrement repliées en cascade avec un circuit de rétroaction à capacités commutées de mode commun. L'amplificateur replié en cascade en amont a montré un gain DC de 68.5 dB à 225 °C et une variation de gain DC de 2.8 dB à partir de -20 °C jusqu'à 225 °C. L'amplificateur différentiel est entièrement replié en cascade avec un

circuit de rétroaction à capacités commutées en mode commun a montré un gain DC de 68.9 dB et une variation de gain DC de 2.1 dB de -20 °C à 225 °C.

Ensuite, en utilisant ces blocs de construction de base, trois circuits de conditionnement pour capteurs MEMS capacitifs ont été construits, notamment: 1) un circuit de conditionnement des capteurs à base de conversion capacité-tension (C-V) avec un large éventail de valeurs de capacité à l'état stable de 0.5 pF à 10 pF, 2) un circuit de conditionnement à base d'un convertisseur capacité-fréquence permettant la conversion de la capacité du capteur en un signal numérique à impulsions modulées en fréquence, et 3) un circuit de conditionnement à base d'un convertisseur de capacité en un signal numérique en utilisant une technique d'acquisition sigma-delta pour convertir le taux d'entrée entre la capacité du capteur et de la capacité de référence en une sortie numérique à haute précision. Tous ces trois circuits de conditionnement pour capteurs capacitifs sont simulées sur toute la plage de température de -55 °C à 225 °C ainsi que testés sur toute la plage de température de -20 °C à 225 °C. Les résultats des mesures montrent que ces circuits ont une bonne précision et une stabilité de température sur une large plage de température.

Tous les circuits développés dans cette thèse sont implémentés en utilisant la technologie standardisée d'IBM (CMOS à base de 0.13 μm) qui intègre une puissance de 2.5 V grâce aux avantages de haut niveau d'intégration et de faible consommation d'énergie. Les techniques de conception utilisées ici sont universelles et ils peuvent être facilement portés à d'autres procédés CMOS standard et même aux procédés SOI. L'amélioration et le développement futur de ces circuits sont proposés. Plus de circuits de conditionnement sophistiqués pour capteurs pourraient être construits sur la base des prototypes actuellement développés dans cette thèse.

LIST OF FIGURES

LIST OF TABLES

PUBLICATIONS

JOURNAL PUBLICATIONS:

- **Y. Wang**, V. P. Chodavarapu, *"Differential Wide Temperature Range CMOS Interface Circuit for Capacitive MEMS Pressure Sensors"*, Sensors, vol. 15, iss. 2, pp. 4253-4263, 2015.

- **Y. Wang**, V. P. Chodavarapu, *"Wide-Temperature Range CMOS Capacitance to Digital Convertor for MEMS Pressure Sensors"*, Sensors and Actuators: A Physical, vol. 233, pp. 302-309, 2015.

CONFERENCE PUBLICATIONS:

- **Y. Wang**, V. P. Chodavarapu, *"Design of a sigma-delta modulator in standard CMOS process for wide-temperature applications"*, Proceedings of IEEE 2015 16th International Symposium on Quality Electronic Design (ISQED), Santa Clara, California, March 2015.

- **Y. Wang**, V. P. Chodavarapu, *"High-Temperature General Purpose Operational Amplifier in IBM 0.13µm CMOS Process"*, Proceedings of IEEE International Conference on Electron Devices and Solid-State Circuits (*EDSSC*), Chengdu, China, June 2014.

- **Y. Wang**, V. P. Chodavarapu, *"Design of a CMOS Readout Circuit for Wide-Temperature Range Capacitive MEMS Sensors"*, Proceedings of IEEE 2014 15th International Symposium on Quality Electronic Design (ISQED), Santa Clara, California, March 2014.

- A. Merdassi, **Y. Wang**, G. Xereas and V. P. Chodavarapu, "*Design and fabrication of 3-axis accelerometer sensor system for harsh environment applications using semi-custom process*", Proceedings of SPIE MOEMS-MEMS Conference, San Francisco, Feb 2014.

- **Y. Wang**, V. P. Chodavarapu, *"Design of CMOS Capacitance to Frequency Converter for High-Temperature MEMS Sensors"*, Proceedings of IEEE Sensors Conference, Baltimore, November 2013.

- **Y. Wang**, C. Allen, S. AL-Qahtani, A. Merdassi, V. P. Chodavarapu, E. Harvey, and J. Henderson, *"Towards Wireless Implantable Pressure Sensor to Monitor Compartment Syndrome in Trauma Victims"*, Proceedings of NanoTech Conference, Washington DC, May 2013.

CONTRIBUTIONS OF AUTHORS

This thesis is based on four published manuscripts. The candidate, Yucai Wang, is the primary author for all these manuscripts.

Chapter 2 is based on the published paper entitled *"High-Temperature General Purpose Operational Amplifier in IBM 0.13μm CMOS Process"*, Proceedings of IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Chengdu, China, June 2014.

Chapter 3 is based on the published paper entitled "*Differential Wide Temperature Range CMOS Interface Circuit for Capacitive MEMS Pressure Sensors*", Sensors, vol. 15, iss. 2, pp. 4253-4263, 2015.

Chapter 4 is based on the published paper entitled "*Design of CMOS Capacitance to Frequency Converter for High-Temperature MEMS Sensors*", Proceedings of IEEE Sensors Conference, Baltimore, November 2013.

Chapter 5 is based on the published paper entitled "*Wide-Temperature Range CMOS Capacitance to Digital Convertor for MEMS Pressure Sensors*", Sensors and Actuators: A Physical, vol. 233, pp. 302-309, 2015.

CHAPTER 1 INTRODUCTION

1.1 INTRODUCTION TO MEMS

1.1.1 BRIEF HISTORY OF MEMS

Microelectromechanical systems (MEMS), also referred to as microsystems technology (MST) or micromachines in different countries, are micro devices or systems which integrate electrical and mechanical components. They are fabricated using methods similar to integrated circuit (IC) batch-processing technologies and their physical dimensions can range from several tens of nanometers to several hundreds of millimeters [1]. Most MEMS have at least one mechanical element that is either movable or immovable, such as beams, cantilevers, springs, gears, membranes, channels, holes, cavities, valves, and other structures.

Starting in late 1950s and early 1960s, MEMS began to evolve when several pioneering researchers began to make micromechanical devices using microfabrication technology developed for the IC industry [2]. Piezoresistive effect was discovered in germanium and silicon and strain gauges based on that property began to be commercialized in 1958 [3]. The resonant gate transistor (RGT), a new type of transistor which was the earliest demonstration of micro-electrostatic actuators, was developed in 1967 [4]. In the 1970s, diaphragm-type silicon pressure sensor was developed at the IBM research laboratory. In 1978, Hewlett-Packard developed the thermal inkjet technology where MEMS technology is used to manufacture arrays of inkjet printer nozzles. Around 1982, the term “micromachining” was introduced to name the fabrication of micromechanical sensors. In the late 1980s, researchers in the micromachining

field mainly used silicon (single-crystalline bulk silicon or thin film polycrystalline silicon) as processing material. The use of thin film silicon led to development of surface micromachining technology. In 1989, researchers at the University of California at Berkeley demonstrated the first silicon micromachined rotary micromotor driven by electrostatic forces [5]. By 1990s, the term "microelectromechanical systems (MEMS)" gained international acceptance as MEMS entered an era of tremendous growth. A number of MEMS devices became commercially successful, including the ADXL series accelerometers by Analog Devices Inc. for airbag deployment [6] and the digital light processing (DLP) chip by Texas Instruments Inc. for digital optical projector [7, 8]. From that period, many new MEMS spin-off branches emerged, including optical MEMS, BioMEMS, microfluidics, radio frequency (RF) MEMS, and Nano Electromechanical Systems (NEMS). A mature and sustainable MEMS ecosystem has been formed and the MEMS market is rapidly growing every year. In 2013, the annual MEMS revenue is 12 billion US$, and it is expected to reach 22 billion US$ by 2018 [9]. The top five players in MEMS industry in 2013 are Robert Bosch, STMicroelectronics, Texas Instruments, Hewlett-Packard, and Knowles. The top five applications are pressure sensors, accelerometers, digital compass, inkjet heads, and microfluidics [10].

MEMS devices now play an important role in our society and are ubiquitous in almost every aspect of our daily lives. We can find them in automobiles (accelerometers for crash detection and air-bag deployment, pressure sensors for tire pressure monitoring, chemical sensors for exhaust analysis), smartphones (accelerometers for automatic screen rotation, fingerprint sensors for identification, microphones for detecting audio signals), telecommunication systems (radio frequency switches for wireless communication, micromirrors for fiber optic switching), digital optical projectors (arrays of micromirrors for high definition optical displays), GPS navigation

systems (accelerometers and gyroscopes for orientation and rotation detection), inkjet printers (printer nozzles to eject ink droplets), biomedical applications (pressure sensors to monitor blood pressure and microprobes to record neural electropotentials).

1.1.2 ADVANTAGES OF MEMS

While they can perform most of the same tasks as their macroscopic counterparts, MEMS devices offer three distinct advantages; First and foremost is miniaturization, the typical physical dimensions of MEMS devices range from micrometers to millimeters. Their small sizes allow miniaturization applications to be developed which are bulky when implemented using conventional sensors. For example, it is impractical to integrate bulky mechanical accelerometers, gyroscopes (with feature sizes of at least several centimeters) with smartphones and cameras. Also, due to their small sizes, MEMS devices require smaller amount of materials to produce, therefore making them less expensive than macroscopic devices. Moreover, small sizes offer other performance advantages including, higher accuracy, sensitivity, and resolution [11].

Ease of integration with microelectronics is another advantage of MEMS devices. Because they are fabricated with similar processes used in integrated circuit fabrication, MEMS devices can be readily integrated with microelectronic circuits which are used to control MEMS devices or process output signals from them, forming standalone monolithic microsystems. Systems integration can significantly reduce the length of signal path and wiring complexity, hence it offers improved signal quality and system reliability. A typical example of system integration of MEMS and microelectronics is the DLP chip by Texas Instruments, where more than 2 million micromirrors arranged in 11.93 mm diagonal array are controlled individually for 1920×1080

resolution [12], with each mirror controlled by a microelectronic circuit buried directly underneath. It would be impractical to separately address mirrors in such a large and dense array without monolithic integration with microelectronics.

Last but not least, MEMS devices can be batch fabricated with accurate dimension and good uniformity control guaranteed by lithographic processing. Many two or three dimensional microstructures, such as cantilevers, beams, membranes, inverted pyramid cavities, springs, gears, channels, through-wafer holes, and high aspect ratio trenches, can be made with combination of bulk micromachining, surface micromachining, and micromolding methods. As thousands of MEMS devices can be fabricated in the same time, batch fabrication can significantly reduce the cost of fabrication. As a result, the price of MEMS devices is much cheaper than their macro scale counterparts. It is one of the most important reasons why MEMS have gained unprecedented commercial success.

1.2 EXAMPLES OF MEMS SENSORS

Most MEMS devices can be categorized as being either a sensor or an actuator. A sensor is a device which can detect or measure a physical quantity, property or condition such as pressure, temperature, light, and heat. An actuator is a device which can produce mechanical motion, force, or control a system. For example, an accelerometer is a sensor which measures mechanical acceleration and converts it to an output electronic signal. The DLP chip by Texas Instruments is an actuator which moves micromirrors under the control of electrical signals. Sensors and actuators are collectively called transducers, which convert power from one energy domain to

another. Energy domains include (but are not limited to) electrical, mechanical, chemical, radioactive, optical, magnetic, acoustic, and thermal [11].

Based on the principles of operation, MEMS sensors can be generally classified into the following categories:

Capacitive sensor: A capacitor is formed when two overlapping conductors are separated by a nonconductive material. Capacitance characterizes the ability of the capacitor to store an electrical charge and it is determined by the overlapping area and the gap size between the two conductors, and the permittivity of the nonconductive material in the gap. The capacitance will change when any of the above three parameters is changed by an applied stimulus, such as acceleration or pressure. By measuring the capacitance value, we can quantify the applied stimulus. Capacitive sensors can be used to measure acceleration, pressure, position or displacement, proximity, and humidity. Capacitive sensors often have static capacitance values on the order of picofarads (pF) and the capacitance change caused by an applied stimulus is

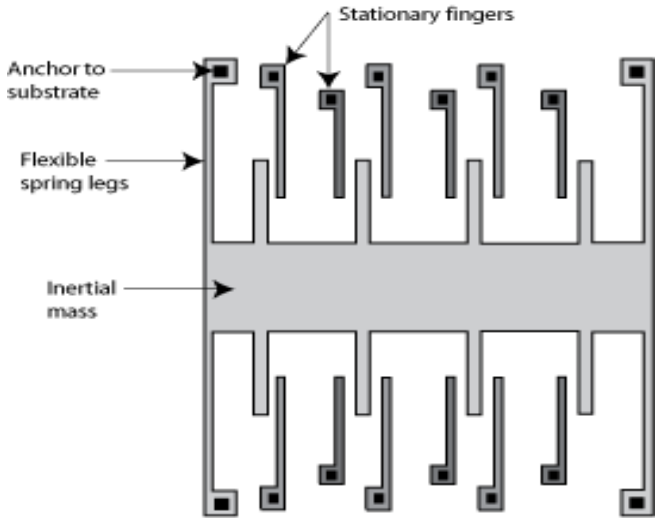


Figure 1.1 A schematic of a capacitive MEMS accelerometer (taken from [13])

usually on the order of femtofarads (fF). High resolution electronic circuits are needed to register such small capacitance changes. Figure 1.1 shows the schematic of a capacitive MEMS accelerometer. The applied acceleration causes a displacement of the inertial mass and changes the capacitance between the stationary and moving comb fingers.

Resistive sensor: The resistance R of a conductor is determined by its resistivity, length, and cross-sectional area. In resistive sensors, a material's resistance is changed by the applied stimulus and this resistance change is often detected using a circuit configuration called the Wheatstone bridge. Usually a piezoresistive material is used where its resistivity can be changed by an external applied force. Most materials have piezoresistive property, but it is particularly evident in some semiconductors like doped silicon. Piezoresistive sensors provide an easy and direct signal converting mechanism between the mechanical and electrical domains and they are widely used to measure physical quantities including acceleration, pressure, force, and flow rate. Some materials' resistance changes under a magnetic field. These magnetoresistive materials are used to build resistive sensors to measure magnetic field. Heating can also change a material's

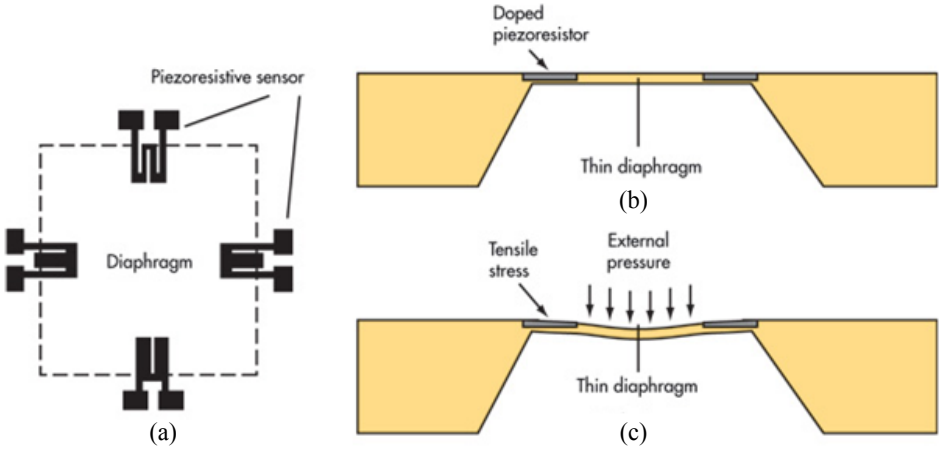


Figure 1.2 Schematic of a piezoresistive MEMS pressure sensor. (a) top view (b) side view without applied pressure (c) side view with external pressure. (taken from [14])

resistance and some materials highly sensitive to heat are used to make temperature sensors [15]. Figure 1.2 shows the schematic of a piezoresistive MEMS pressure sensor. The external pressure causes a tensile stress on the thin silicon membrane and it changes the resistance of the piezoresistors on the membrane's surface.

Piezoelectric sensor: Some materials can generate an electrical charge (or voltage) when an external force is applied. This is known as piezoelectric effect. When a piezoelectric material is pressed, positive ions get accumulated on the pressed side, and negative ions become more concentrated on the opposite side. The commonly used piezoelectric materials are quartz, lead zirconate titanate (PZT), polyvinylidene difluoride (PVDF), and zinc oxide (ZnO). Electrodes are placed on the piezoelectric material to collect the charge. As the piezoelectric materials are nonconductive, this configuration forms a capacitor where the piezoelectric materials are located in the gap between the two electrodes. The voltage between the electrodes can be measured by placing a charge amplifier before the subsequent measurement system. Piezoelectric sensors are used to measure physical quantities including acceleration, pressure, force, strain, flow rate, and temperature. Figure 1.3 shows the schematic of a piezoelectric MEMS accelerometer. A thin

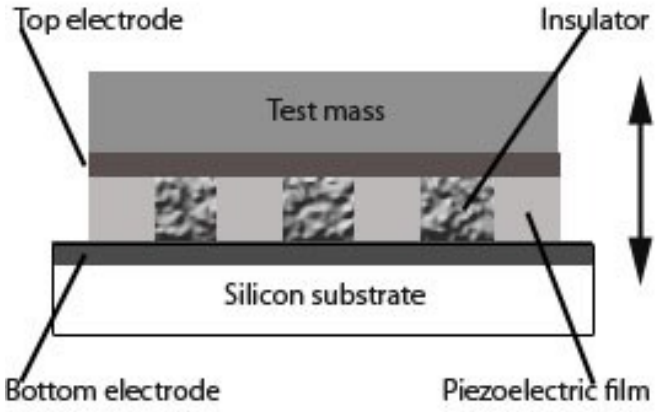


Figure 1.3 Schematic of a piezoelectric MEMS accelerometer (taken from [16])

piezoelectric film is placed between a test mass and a silicon substrate. When an acceleration is applied along its sensitive axis (marked using the arrow in Figure 1.3), the piezoelectric film is subject to stress due to coupling to the test mass and electrical charge is generated and can be converted to a voltage output.

Resonant sensor: At certain frequencies, a system vibrates with abnormally large amplitude than at other frequencies. This phenomenon is called resonance and the frequencies are called resonance frequencies. Resonant sensor, which contains a mechanical structure (called resonator) such as a beam that vibrates with small displacements, is based on the principle of resonance. The resonance frequency is determined by the mass, stiffness, and damping of the resonator. In resonant sensor, the physical quantities to be measured, such as pressure and acceleration, impose a strain on the resonator and change its stiffness. As a result, the resonance frequency of the sensor also changes in accordance with the physical quantities. In the application of sensing a magnetic field, the resonance frequency of the resonator is fixed and the amplitude of the vibration changes with the magnitude of the magnetic field. By measuring the resonance frequency or vibration magnitude, the physical quantities can be quantified. Figure 1.4 shows the

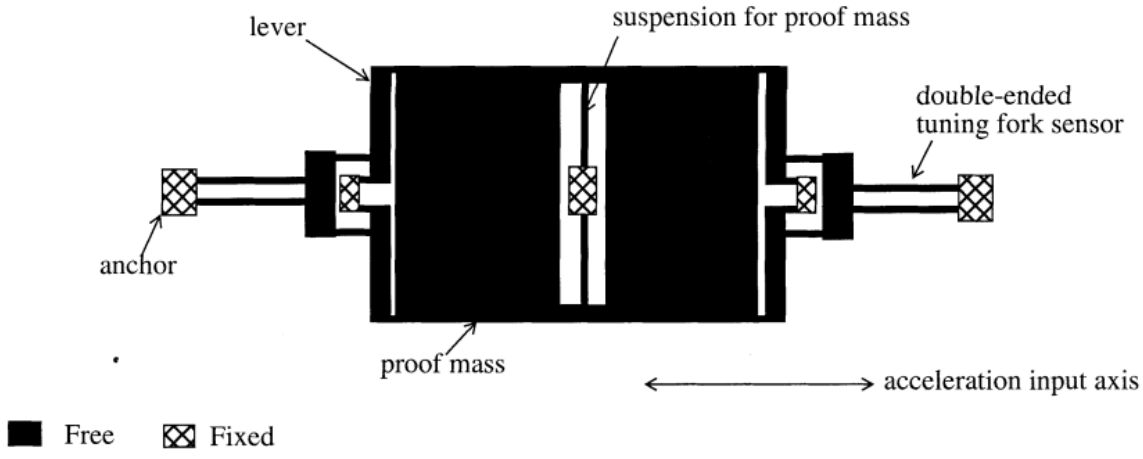


Figure 1.4 Schematic of a MEMS resonant accelerometer (taken from [17])

schematic of a MEMS resonant accelerometer. In this device, the tuning forks are actuated at resonant frequency using lateral comb drives and the resonance is maintained by incorporating the mechanical structure in the feedback loop of an oscillator circuit [17]. When an external acceleration is applied to the proof mass along the sensitive axis (marked using the arrow in Figure 1.4), a force is generated axially onto the double-ended tuning fork sensors, resulting in a shift in the resonant frequency of the double-ended tuning fork sensors.

Thermoelectric sensor: For some materials, an electric voltage will be generated when a temperature difference is applied between the two points and the materials are called thermoelectric materials. This effect is called thermoelectric effect and it is the basis of the thermoelectric sensors. A thermocouple is a typical thermoelectric sensor which is used to measure temperature. It is built with two dissimilar thermoelectric materials which connect each other at their endpoints. When the temperature at one endpoint is different from the reference temperature at the other endpoint, a voltage output will be produced, which is determined by the two thermoelectric materials and the temperature difference between the two endpoints. In case of larger output voltage is desired, several thermocouple pairs can be connected in series to build

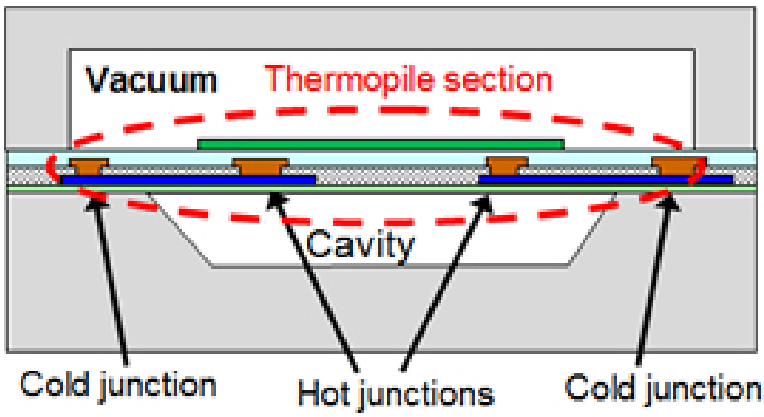


Figure 1.5 Schematic of a MEMS thermal sensor (taken from [18])

a thermopile, which is primarily used to measure temperature and infrared radiation. Thermo-electrical sensors can be used to measure physical quantities including pressure, acceleration, position, flow rate, and displacement. Figure 1.5 shows the cross-section view of a MEMS thermal sensor. Thermopiles are constructed by serial connection of thermocouples consisting of N+ poly silicon and P+ poly silicon. Hot junctions are created on highly-resistant dielectric membranes and cold junctions are created on highly heat-conductive silicon [18]. The thermopiles are sealed in a vacuum to prevent the heat from dissipating into the air hence increasing sensitivity.

Magnetic sensor: Magnetic sensors use either reluctance sensing or inductive sensing principles. Reluctance is the inverse of permeance, which is used to describe magnetic field energy storage. The equation Q=CV is used for capacitive energy storage, where Q is the charge, C is capacitance, and V is voltage. Analogously, the equation Φ=PM is used for magnetic field energy storage, where Φ is magnetic flux, P is permeance, and M is magnetomotance (also called magnetomotive force). Similar to capacitance of a parallel plate capacitor, the value of

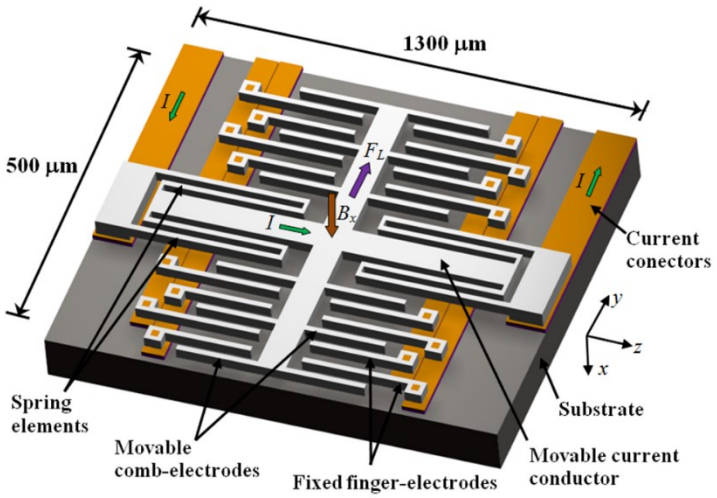


Figure 1.6 Schematic of a MEMS resonant magnetic field sensor (taken from [19])

permeance (and reluctance) is determined by the overlap area, the gap size, and magnetic permeability of the material in the gap. When a physical quantity (pressure or displacement) causes any of the three parameters changes, the magnetomotive force changes accordingly and it can be measured by the current it induces in a coil. If a physical quantity causes a conductive coil to move in a magnetic field, a current will be induced in the coil. The current can be measured to represent the input physical quantity. This is the underlying principle of inductive sensing [15]. Figure 1.6 shows the schematic of a MEMS resonant magnetic field sensor which contains a large movable conducting microbeam, movable comb electrodes and fixed finger electrodes. A Lorentz force (F_L) is generated when an ac current (I) flows through the conducting beam under the presence of an external magnetic field (B_x) [19]. As a result, the distance between the movable electrodes and the fixed electrodes is changed and the capacitance between them is changed consequently. The magnetic field can be measured by quantifying the capacitance variation.

Many physical quantities can be measured using more than one sensing principle. For example, pressure can be measured using all the above mentioned sensing principles. Sensor developers must assess the different sensing principles according to their performance characterizations and practicality characterizations to select the best sensing principle for a particular application. Performance characterizations describe sensor's technical performance, including but not limited to sensitivity, linearity, resolution, signal-to- noise ratio, dynamic range, bandwidth, drift, reliability, repeatability, cross-sensitivity, temperature stability, and response time [11]. Practicality characterizations refer to the feasibility to suit a sensor into a specific application, including but not limited to size, weight, sensing material, fabrication method, yield, cost, power consumption, manufacturing ease, packaging compatibility, robustness, and

intellectual property rights. Table 1.1 compares the advantages and disadvantages of four types of most commonly used sensors.

Table 1.1 Comparison of various sensors (taken from [11])

Sensors	Advantages	Disadvantages
Capacitive sensor	• Simplicity of materials • Low-voltage, low-current operation • Rapid response	• Large footprint of device necessary to provide sufficient capacitance • Complexity of readout electronics • Sensitive to particles and humidity
Thermal sensor	• Simplicity of materials • Elimination of moving parts	• Relatively large power consumption • Generally slower response than capacitive sensing
Piezoresistive sensor	• High sensitivity achievable • Simplicity of materials (metal strain gauge)	• Requires doping of silicon to achieve high performance piezoresistors • Sensitive to environmental temperature changes
Piezoelectric sensor	• Self generating-no power necessary	• Complex material growth and process flow • Cannot sustain high-temperature operations

1.3 MEMS SENSORS FOR WIDE-TEMPERATURE APPLICATIONS

In recent years, there is an increasing demand for the development of MEMS sensors capable of sustained operation at wide temperature range well beyond the military temperature specification (-55 ºC to 125 ºC) [20]. In particular, high operating temperatures can either result from high ambient temperature or due to difficulties of effective heat removal for high power dissipation. Typical high-temperature applications are found in automobile industry, oil and gas exploration, aerospace, and industrial process control, where different kinds of MEMS sensors are widely used to improve system performance, reliability, and reduce cost.

The automobile industry is considered the largest market for high-temperature MEMS sensors. Since 1970s, governments have been applying regulations mandating emissions control and fuel economy. These complex regulations could not be achieved using traditional mechanical systems, driving the automobile industry to migrate from purely mechanical system to MEMS sensor systems [21, 22]. As a result, a variety of MEMS sensors are being introduced in automobiles to help optimize engine operation, reduce emissions of exhaust pollutants, provide better fuel economy and enhance safety, comfort and convenience. The number of MEMS sensors used for engine control applications have increased from around ten in 1995 to more than thirty in 2010 [23]. Under the hood of an automobile, temperature is usually beyond 150 °C, and can even reach 200 °C [21, 24], depending on the specific location on the engine block or the exhaust system. Moreover, the trend towards hybrid electrical vehicles is driving MEMS sensors into even harsher environments, such as on or near the brakes, where temperatures can go up to 250 °C [25].

The oil and gas industry is another large user of high-temperature MEMS sensors, where sensors are extensively used to steer the drilling equipment and log the surrounding geologic information in oil, gas and geothermal wells. The parameters logged include temperature, pressure, flow rate, density, resistivity and chemical composition. These data enable the geologists to optimize the productivity of the well and, in extreme situation, prevent the well from being completely blocked [26]. In such applications, the operating temperature increases as the well goes deeper, with a typical geothermal gradient 25 °C per km of depth [27]. Currently, most deep-well drilling operation temperature is not over 200 °C [28]. As the easily accessible natural resources are being depleted, wells must go deeper, where operation temperature can reach up to 400 °C [29].

The aerospace industry now has a growing demand toward the high-temperature MEMS sensors. The main driving force is the desire for reduced weight, improved system performance and reliability. Conventionally sensors are used only in limited locations on engines to monitor propulsion component, and their use usually involve certain active and passive cooling techniques [30]. With high-temperature MEMS sensors, they can be used both sensing around the engine casing and in the hottest parts of the engine itself, where the temperature is 500 °C to 600 °C [31]. Improved combustor control offers substantial fuel saving and decreased engine emissions. Without the need for necessary peripheral cooling systems, high- temperature MEMS sensors enable significant reduction in weight, size and cost.

Currently most wide-temperature MEMS sensors use principles of capacitive sensing, piezoelectric sensing, and piezoresistive sensing [32-39]. As mentioned in Table 1.1, the piezoresistive coefficient of piezoresistive sensors has inherent temperature dependence and it has to be compensated. For piezoelectric sensors, as the operating temperature increases, piezoelectric effect of a piezoelectric material decreases, and ultimately complete and permanent depolarization will occur. Capacitive MEMS sensors are preferred in many of the wide-temperature applications because the physical quantities to be measured can be converted to an electrical signal by a capacitor placed in vacuum, which has no inherent temperature dependence [40]. Capacitive sensors also have other advantages including low thermal drift, good reliability, high accuracy and sensitivity, good noise performance, and low power consumption [41, 42].

1.4 INTERFACE ELECTRONICS FOR WIDE-TEMPERATURE MEMS SENSORS

Sensor interface electronics are indispensable to MEMS sensors which provide power supply to the sensor, convert the sense signal to an electrical signal (usually a voltage or current), condition and digitize the electrical signal for easy transfer and storage. In wide-temperature range applications, the conventional sensor interface electronics will fail to work properly or their performance will degrade. Traditionally, these electronics had to be remotely placed in a cooler region or they must be actively or passively cooled, which inevitably introduce additional overhead in the form of longer wires, additional connectors, and/or bulky cooling system, resulting increased size, weight, complexity and accordingly increased potential for failure to the system [27, 43, 44]. Moreover, in some applications, due to constraint of size and weight, cooling is not a feasible option. Hence, it is more favorable for the interface electronics to reside in close proximity to sensors to reduce noise, interference, wiring complexity, system size, production cost, and improve system reliability [45]. For example, in automobile applications, sensor interface electronics are placed in the engine compartment to improve fuel economy, and reduce exhaust emission. In oil and gas exploration, electronics are mounted in deep bores to acquire data about the surrounding geologic formations and thereby identify possible oil or gas deposits. In modern aircrafts, electronics are placed near the engine and braking system to reduce component weight, cost and wiring complexity, and improve performance and reliability. In such wide-temperature applications, the sensor interface electronics must be subject to the same operating temperature as the MEMS sensors. Table 1.2 summarizes the operating temperature ranges for typical high temperature applications. As can be seen, the operating temperatures of a majority of applications are between -55 °C to 225 °C. For such wide temperature range, the

design of sensor interface electronics is challenging and requires special design considerations, especially at the high temperature end.

Table 1.2 Temperature range for typical wide-temperature applications (taken from [46])

Applications		Temperature Range (°C)
Automotive Industry	Compartment	-40 ~ 85
	Engine/Gear Box	-40 ~165
	Brakes	-40 ~250
Avionics	Aircraft Surface	-40 ~80
	Engine Intake	-40 ~185
	Jet Engine	-40 ~320
Satellites		-150 ~ 200
Space Exploration		-150 ~450
Oil Exploration		-40 ~175
Geothermal Exploration		-40 ~ 320

Most electronics fabricated today use bulk Complementary Metal-Oxide-Semiconductor (CMOS) processes, which offers numerous advantages including low power consumption, low fabrication cost, easy of technology scaling, and the ability to integrate analog and digital blocks on the same chip and thereby reducing the chip size. However, conventional electronics made in bulk CMOS technology suffer from many drawbacks at high temperatures, including degradations in electron/holes mobility, reduction in MOS transistors threshold voltage, increase of bulk junction leakage currents [47, 48], and increase in silicon intrinsic carrier density [49]. Among which, mobility reduction, threshold voltage drop are inherit to the physics of silicon material and field-effect transistor. Excess junction leakage current at high temperature is the

most harmful for bulk CMOS circuits, which can increase self-heating, shift analog operation points, reduce open loop gain and bandwidth of amplifier, increase offset, erase charge stored at dynamic node, and even cause chip failure due to latch-up [45]. The silicon intrinsic carrier density is comparable to doping level at temperature beyond 300 ºC, which imposes the theoretical temperature upper limit for CMOS technology [49].

Fabricating circuits using silicon-on-insulator (SOI) technology can effectively address junction leakage current problem as the buried insulator layer in the SOI structure eliminate the p-n junction diodes between the source/drain and substrate/well. SOI technology also offers better latch-up immunity [50]. And circuit designs in CMOS technology can be easily migrated to SOI CMOS technology. SOI technology has been proven effective to extend operating temperature of electronics to 300 ºC [51-54]. However, the threshold voltage drop and carrier mobility decrease at high temperatures which are innate to silicon still limit the circuits performance, and analog circuits in SOI technology have reduced performance due to hysteresis in the I-V characteristics of MOS transistors [49]. Furthermore, SOI technology is much more expensive than CMOS technology and is available from fewer suppliers [49].

Wide bandgap semiconductors such as silicon carbide (SiC) [55-58] and gallium nitride (GaN) [59] are promising materials for high temperature electronics which extends the operating temperature up to 600 ºC [55, 57]. But they share the same cost problem with SOI technology and the fabrication processing is yet maturely developed. Further, reliable and durable interconnecting and packaging technologies are needed for electronics built of wide bandgap semiconductors to work at high temperature.

In recent years, various design techniques were developed to mitigate the aforementioned high temperature induced effects in bulk CMOS technology. Monolithic bulk CMOS circuits, including logic gates, memories, oscillators, amplifiers, and analog-to-digital convertors (ADC), have been demonstrated functional at temperatures beyond 200 ºC [60-67]. Many of these previous works used technology with feature sizes of 1.5 μm and more and power supplies of 5 V. As the feature size of CMOS process continues to scale down, it is desirable to take advantage of process with smaller feature size for the benefits of low cost, low power consumption and high level of integration.

Many research groups have previously implemented high temperature interface circuits for piezoresistive and piezoelectric MEMS sensors. In 2000, Jong *et al*. [68] reported a high-temperature pressure-transducer interface for piezoresistive pressure sensors. This interface circuit uses an instrumentation amplifier with continuous auto-calibration and dynamic feedback and it can operate at temperatures up to 250-275 ºC with 15-16 bit accuracy [61]. In 2006, Yu *et al*. [45] reported a high-temperature bulk CMOS data acquisition system for piezoresistive Wheatstone-bridge sensors which can operate at temperature up to 300 ºC. In 2006, Levinzon [69] reported a silicon base hybrid charge amplifier for miniature piezoelectric accelerometer which can operate over temperature range from -55ºC to 175ºC. However, there are no available wide temperature range CMOS sensor interface circuits for capacitive MEMS sensors implemented to date. Further, commercially available capacitance readout circuits that interface with MEMS sensors from Analog Devices Inc. (Model: AD7152) [70] and ISC8 Inc. (Model: MS3110) [71] work only between the commercial temperature range from -40 ºC to 85 ºC.

The goal of this thesis is to develop various sensor interface circuits for capacitive MEMS sensors in IBM 0.13 μm bulk CMOS process which incorporates a 2.5 V power supply and

which can operate at temperature range between -55 ºC to 225 ºC. For wide temperature range from -55 ºC to 225 ºC, several key device parameters, including intrinsic carrier concentration, carrier mobility, threshold voltage, and junction leakage current, vary with temperature and limit the high temperature operation of CMOS devices and circuits. They must be properly investigated and accounted for before the circuit design. These key device parameters are studied in Section 1.5 shown below.

1.5 CHALLENGES FOR WIDE-TEMPERATURE CMOS CIRCUITS DESIGN

1.5.1 INTRINSIC CARRIER CONCENTRATION

The concentration of intrinsic carrier n_i of a semiconductor is dependent upon the temperature and can be expressed by Equation (1.1) **[72]**,

$$n_i(T) = \sqrt{N_C N_V}\, e^{-E_g/2kT} \quad (1.1)$$

where, N_C is the effective density of states for electrons in the conduction band, N_V is the effective density of states for holes in the valence band, E_g is the energy bandgap of the semiconductor, T is the temperature in Kelvin, and k is the Boltzmann constant (8.62×10^{-5} eV/K). Most semiconductor devices create sufficient local free carrier concentration in excess of the thermal intrinsic carrier n_i through intentional introduction of impurities using doping process, and the typical doing level in CMOS process is between 10^{14} to 10^{18} atoms per cubic cm (cm^{-3}). Maintaining the local free carrier concentration sufficiently larger than the intrinsic carrier n_i is vital to operation of any semiconductor device. In CMOS devices operating at room temperature, the dopant is fully ionized and the local free carrier concentration is almost equal to the doping level. Figure 1.7 shows the intrinsic carriers concentration n_i of silicon bandgap=1.12 eV at 300

K) versus temperature, calculated from Equation (1.1). The intrinsic carriers concentration of gallium arsenide (GaAs) (bandgap=1.42 eV at 300 K) is also shown for comparison. The *Eg*, N_C, and N_V of silicon have much less temperature dependence as compared with the temperature exponential term (-Eg/2kT) of Equation (1.1). Their temperature dependence is also taken into account in Figure 1.7. The detailed equations about the temperature dependence of *Eg*, N_C, and N_V can be found in [73]. From Figure 1.7, the silicon intrinsic carrier concentration at room temperature (300 K) is around 10^{10} cm^{-3}, which is negligible to the CMOS process doping levels (10^{14} to 10^{18} cm^{-3}). However, as the ambient temperature increases beyond 600 K, the silicon intrinsic carrier concentration is more than 10^{15} cm^{-3} and it is comparable to the device lighter doping level. Hence, the designed doping profile at lighter doping region of a given silicon device will be undesirably affected by the intrinsic carriers and the device performance will

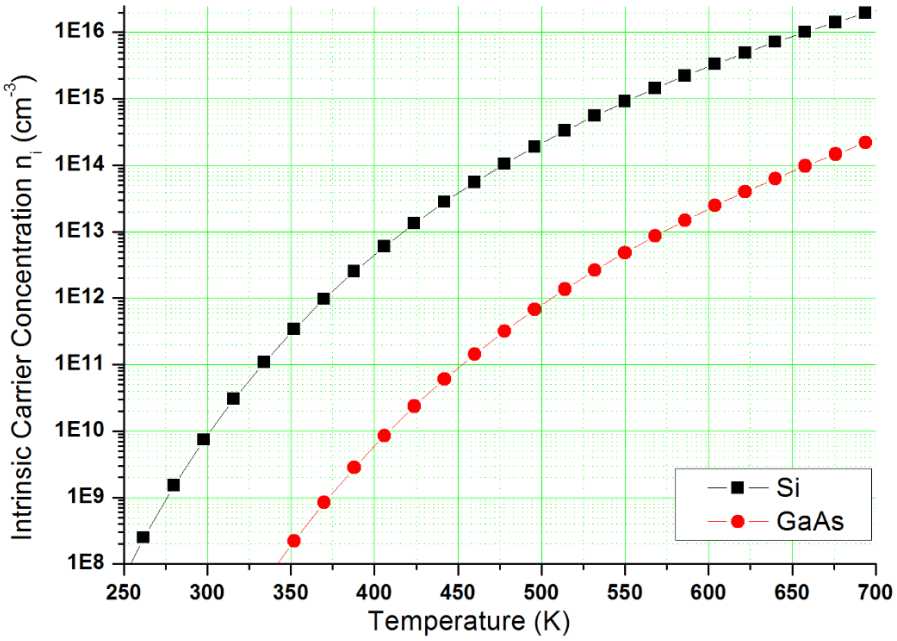


Figure 1.7 Intrinsic carrier concentration (n_i) of Si and GaAs versus temperature

inevitably deteriorate. The intrinsic carrier density dependence on temperature imposes an insurmountable theoretical limit for silicon devices to operate beyond 300 ºC. From Equation (1.1) it can be seen that at the same temperature, the intrinsic carrier density is much lower for a semiconductor with larger energy bandgap E_g. This explains why wide bandgap materials like silicon carbide (SiC) and gallium nitride (GaN) with bandgaps around 3 eV are desirable for operation above 300 ºC.

1.5.2 CARRIER MOBILITY

In the absence of an electrical field, free carriers (electrons and holes) in the semiconductor randomly move inside it and frequently change direction. When an electrical field E is applied across the semiconductor, the free carriers are subject to an electrostatic force F (F = -qE, q is the carrier charge) and electrons will move against the direction of electrical field, while holes will move following the direction of electrical field. The carriers acquire momentum under the electrostatic force F and will lose it when they are scattered after a period of τ_c, which is called mean free time and defined as the average time between the scattering events. According to the law of momentum conservation, the average velocity v of the carriers during τ_c can be obtained by Equation (1.2) [73],

$$-qE\tau_c = mv \quad (1.2)$$

where, m is mass of the carriers. The mobility μ of the carrier is defined as the ratio of the velocity to the electrical field and given by Equation (1.3) [73],

$$\mu = \frac{q\tau_c}{m} \quad (1.3)$$

The mean free time τ_c is affected by two scattering mechanisms: lattice scattering and impurity scattering. Lattice scattering is the scattering of carriers by lattice waves and includes the absorption or emission of phonons. The density of phonons in a semiconductor increases with temperature and the mean free time τ_c will decrease. As a result, the mobility will decrease with a temperature dependence of $T^{-3/2}$ [72]. Impurity scattering is the scattering of carriers by impurity atoms (such as ionized donors and acceptors) in the semiconductor. It depends on the velocity of the carriers and the concentration of the impurity atoms. Higher impurity concentration leads to a lower carrier mobility. When temperature increases, the velocity of carriers increases and the amount of scattering decreases, causing a mobility increase with temperature dependence of $T^{3/2}$ [72]. The effect of impurity scattering becomes less significant compared to lattice scattering above certain temperature value, and the overall temperature effect cause carriers mobility to decrease as temperature increases. The temperature dependence of the carrier mobility can be expressed using a simplified model given by Equation (1.4) [74],

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-1.5} \quad (1.4)$$

where, $\mu(T_0)$ is the carrier mobility value at reference temperature T_0. Figure 1.8 shows the electron and hole mobility of silicon at different temperatures for doping level of 10^{16} cm^{-3} (data taken from [75]). As can be seen, from room temperature (300 K) to 500 K, the electron and hole mobility values reduce about by half.

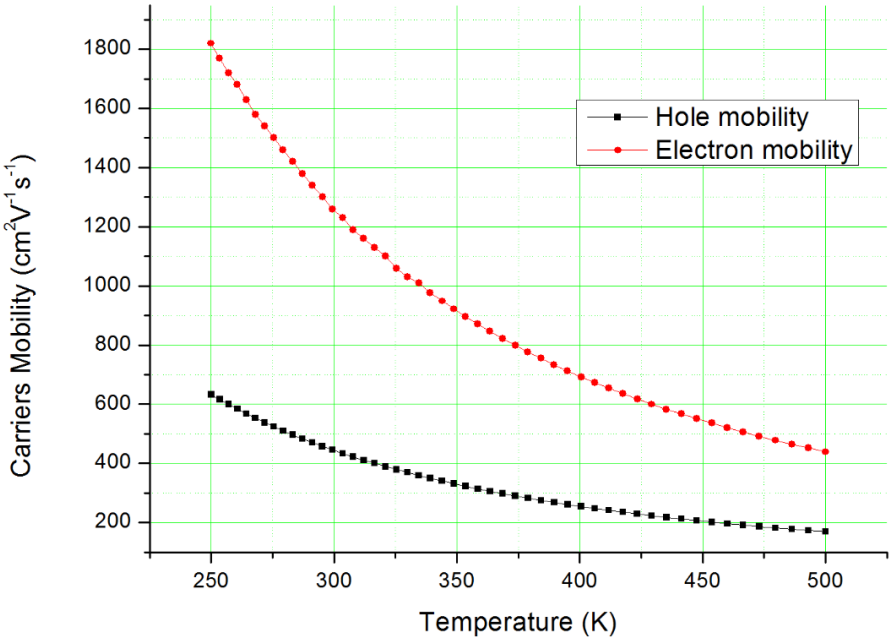


Figure 1.8 Carriers (electron and hole) mobility of silicon versus temperature

1.5.3 THRESHOLD VOLTAGE

The threshold voltage V_T of a long-channel MOSFET (metal–oxide–semiconductor field-effect transistor) with 0 V substrate bias is given by Equation (1.5) [72],

$$V_{T0} = \phi_{ms} - \frac{Q_f}{C_{ox}} \pm 2\phi_F \pm \frac{\sqrt{4q\varepsilon_{si}N_{sub}\phi_F}}{C_{ox}} \qquad (1.5)$$

where, + sign is for NMOS and – sign is for PMOS. Q_f is the fixed oxide charges due to surface states which may arise from dangling bonds at the oxide silicon interface. C_{ox} is the gate capacitance per unit area, q is the electronic charge, N_{sub} is the substrate doping concentration, ϕ_F is the Fermi potential of the substrate and it is given by Equation (1.6) [72],

$$\phi_F = \frac{kT}{q}\ln(\frac{N_{sub}}{n_i}) \quad (1.6)$$

And ϕ_{ms} is the work function difference between the gate material and substrate, which can be expressed by Equations (1.7) and (1.8) [45],

$$\phi_{ms} = -\frac{kT}{q}\ln(\frac{N_{sub}N_g}{n_i^2}) \quad \text{(for NMOS)} \quad (1.7)$$

$$\phi_{ms} = -\frac{kT}{q}\ln(\frac{N_g}{N_{sub}}) \quad \text{(for PMOS)} \quad (1.8)$$

where, N_g is the gate doping level.

When a voltage V_{sb} is applied between the source and substrate, the threshold voltage can be expressed by Equation (1.9),

$$V_T = V_{T0} + \gamma_{n,p}\left[\sqrt{2\phi_F + V_{sb}} - \sqrt{2\phi_F}\right] \quad (1.9)$$

where, $\gamma_{n,p}$ is the body effect parameter.

The temperature dependence of ϕ_{ms} and ϕ_F can be expressed by Equations (1.10), (1.11) and (1.12) [76],

$$\frac{\partial\phi_{ms}}{\partial T} = \frac{1}{T}\left(\phi_{ms} + \frac{E_g}{q} + \frac{3kT}{q}\right) \quad \text{(for NMOS)} \quad (1.10)$$

$$\frac{\partial\phi_{ms}}{\partial T} = \frac{\phi_{ms}}{T} \quad \text{(for PMOS)} \quad (1.11)$$

$$\frac{\partial(2\phi_F)}{\partial T} = \frac{1}{T}\left(2\phi_F - \frac{E_g}{q} - \frac{3kT}{q}\right) \quad (1.12)$$

The second term in Equation (1.5) has no temperature dependence, so from Equations (1.5), (1.9), (1.10), and (1.12), the temperature dependence of the threshold voltage for an NMOS transistor can be expressed as Equation (1.13) [77],

$$\frac{\partial V_T}{\partial T} = \frac{\phi_{ms}}{T} + \frac{2\phi_F}{T} + \frac{\gamma_n}{\sqrt{2\phi_F}}\frac{\partial \phi_F}{\partial T} \quad (1.13)$$

Numerical calculation [77] using parameters for a typical CMOS process shows that at 300 K, the first term in Equation (1.13) is -3.10 mV/ ºC, the second is 2.70 mV/ºC, and the last term is about -0.4 mV/ºC. So the overall threshold voltage temperature dependence of an NMOS transistor is -0.8 mV/ºC, i.e., the threshold voltage decreases when the temperature increases.

From Equations (1.5), (1.9), (1.11), and (1.12), the temperature dependence of the threshold voltage for a PMOS transistor can be expressed as Equation (1.14) [45],

$$\frac{\partial V_T}{\partial T} = \frac{\phi_{ms}}{T} - \frac{2\phi_F}{T} - \frac{\gamma_n}{\sqrt{2\phi_F}}\frac{\partial \phi_F}{\partial T} + \frac{1}{T}\left(\frac{E_g}{q} + \frac{3kT}{q}\right) \quad (1.14)$$

At 300K, the first term in Equation (1.14) is about -0.5 mV/ºC, the second is -2.70 mV/ºC, the third term is about 0.4 mV/ºC, and the last term is about 4.3 mV/ºC. The overall threshold voltage temperature dependence of a PMOS transistor is 1.5 mV/ºC, i.e. the threshold voltage increases when the temperature increases, and the threshold voltage change of PMOS is faster than NMOS. Experimental results show that the threshold voltages of NMOS and PMOS almost halve from 25 ºC to 250 ºC for a typical CMOS process [74].

1.5.4 LEAKAGE CURRENT

Two sources of leakage current exist in a MOSFET: subthreshold channel current and junction leakage current. When the gate to source voltage V_{GS} is below the threshold voltage, the MOSFET works in its subthreshold region and its channel is weakly inverted. The subthreshold channel current of a MOSFET has strong dependence on carrier mobility and threshold voltage, and it increases exponentially with temperature. Subthreshold channel current can be reduced significantly by biasing MOSFET in strong inversion region and it is not considered in this thesis.

In bulk CMOS technology, P substrate is biased to most negative voltage and N well are connected to most positive voltage to form reverse biased diodes to isolate neighboring devices. Figure 1.9 shows two reverse biased diodes between the source/drain region and the P substrate. The leakage current from these diodes unfavorably limit high temperature operations of MOSFETs.

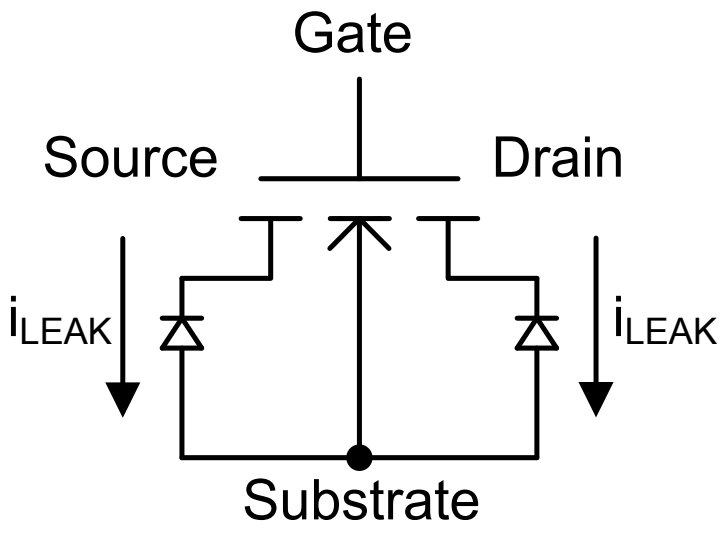


Figure 1.9 Schematic of an NMOS transistor with parasitic diodes

The junction leakage currents measured in the drain of an NMOS and a PMOS transistor is described by de Jong, *et al.* [61]. At room temperature, the leakage current is on the order of pA and is negligible with respect to the drain current in operation (usually on the order of μA). As temperature increases, electron/hole pairs are thermally generated in the depletion region and will be swept across the junction by electrical field, as a result, a drift current will flow. This drift current is proportional to the intrinsic carrier concentration and prevails at temperature up to 100-150 ºC.

When temperature increases higher, minority carriers are thermally generated and diffuse away from the junction area. These carriers, which are proportional to the square of the intrinsic carrier concentration, will reach the edge of the depletion region and swept across the junction by electrical field. As a result, the diffusion current will flow and prevails at higher temperature. Because the concentration of minority carriers is inversely related to the doping concentration, PMOS transistor generally has much less leakage current than NMOS at the same temperature.

The total leakage current of a reverse biased diode, including the drift current and the diffusion current, can be expressed as Equation (1.15) [72],

$$I_L = I_{L,diffusion} + I_{L,drift} = qAn_i\left[\frac{n_i}{N_D}\sqrt{\frac{D_p}{\tau}} + \frac{W}{2\tau}V_A\right]\left(e^{qV_A/kT} - 1\right) \quad (1.15)$$

where, A is the area of the p-n junction, V_A is the voltage applied to the diode, N_D is the n-type doping level, W is the width of the junction depletion region under voltage V_A, Dp is the minority carrier diffusion constant, and τ is the effective minority carrier lifetime. Equation (1.15) can be further simplified, assuming a negative V_A (reverse bias) greater than a few tenths of a volt and the temperature is lower than 1000 ºC as given by Equation (1.16),

$$I_L = -qAn_i\left[\frac{n_i}{N_D}\sqrt{\frac{D_p}{\tau}} + \frac{W}{2\tau}V_A\right] \quad (1.16)$$

From Equation (1.16), it can be seen that the intrinsic carrier concentration n_i dominates the leakage current of a reverse biased diode. Recall from Equation (1.1) that n_i has exponential temperature dependence, so the leakage current increases exponentially with temperature. As shown by de Jong, *et al.* [61] , an NMOS transistor has drain leakage current of several μA at 300 ºC. Excess leakage current causes adverse influence to circuits operate at high temperatures, including self-heating, shifting in the operating points in analog circuits, lowering of output resistance at high impedance nodes, loss of charge stored at dynamic nodes, latchup, and significant offset increase between matching devices [45]. Therefore, leakage current is one of the most difficult challenges to overcome in high temperature bulk CMOS circuits.

1.6 HIGH TEMPERATURE CIRCUIT DESIGN TECHNIQUES

Many circuit design techniques have been previously proposed to relieve the above mentioned high temperature induced effects. Notable techniques include zero temperature coefficient (ZTC) gate biasing, leakage current cancellation, and substrate biasing feedback.

As shown in Section 1.5, the threshold voltage V_T and the carrier mobility both decrease when the temperature increases. While the gate voltage is maintained constant, reduced threshold voltage leads to increased drain current, while reduced carrier mobility leads to decreased drain current. When the gate of a MOSFET is biased at a point where these two opposing effects are cancelled, the MOSFET has almost constant drain current at certain temperature range [47, 74, 77]. This gate biasing voltage is known as ZTC biasing point. The main limitations about ZTC

gate biasing are that it is highly process dependent and has poor reproducibility, it only works for a limited temperature range, and the ZTC biasing voltage is usually much larger than the threshold voltage, which leads to a large overdrive voltage and limits the output swing.

It is possible to cancel the leakage current using a matched leakage path with complementary diodes [74]. However, for the cancellation to be effective, the complementary diodes must have identical leakage current over temperature. So this method cannot work with a conventional single N-well CMOS process, where an NMOS has much larger leakage current than a PMOS at high temperature. An alternative leakage current cancellation method has been proposed where replica leakage generators are used to replace the complementary diodes. Nevertheless, this method requires leakage current matching between junctions and MOSFETs in the leakage generator to operate in the subthreshold region, which is difficult to achieve over a wide temperature range.

The threshold voltage of a MOSFET can be adjusted by applying a substrate bias voltage. So it is possible to reduce the temperature sensitivity of threshold voltage and could even be made constant over temperature by applying a proper substrate bias voltage [47]. However, this method is not applicable to the standard N-well bulk CMOS process, as all NMOS transistors are tied to the same substrate and it is difficult to apply substrate bias voltages to individual transistors considering practical and cost-effective chip sizes.

In recent years, researchers have proposed alternative techniques to design high temperature circuits using bulk CMOS process [45, 49, 60, 78]. These techniques acknowledge that the high temperature induced performance degradations will occur and it is not necessary to compensate individual devices, but use circuit architectures which are dependent on parameters (geometry,

capacitance) with little or no temperature sensitivity or on parameters (transconductance) where their temperature sensitivity can be stabilized. These high temperature circuit design techniques are summarized as follows and will be applied in the high temperature capacitance readout circuits described in this thesis.

1.6.1 HIGH TEMPERATURE TOLERANT CIRCUIT ARCHITECTURES

Generally speaking, single-ended circuits are more susceptible to high temperature induced noises and leakage currents, which usually appear in common mode and can be differentially rejected. Using fully-differential circuitry can effectively suppress these common mode errors and improve the circuit performance at high temperatures. The accuracy of switched-capacitor circuit mainly depends on the ratio of capacitors, which is largely insusceptible to temperature changes. Also, for circuits using sigma-delta modulating technique, the stringent requirement for high-precision analog components is relaxed due to the over-sampling principle.

1.6.2 CONSTANT-GM BIASING TECHNIQUE

Transconductance (g_m) is perhaps the most important parameter in CMOS analog circuits which affects gain, bandwidth, and stability of an amplifier. The constant-g_m biasing technique has been proven effective to stabilize the impact of mobility degradation over wide temperature range. In the circuit shown in Figure 1.10, a current I_b is generated with its magnitude inversely proportional to the carrier mobility [49]. When a MOSFET is biased using a copy of this current, its transconductance can be expressed as Equation (1.17),

$$g_m = \frac{2}{R_b}\sqrt{\frac{W}{L}}\left(\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}}\right) \quad (1.17)$$

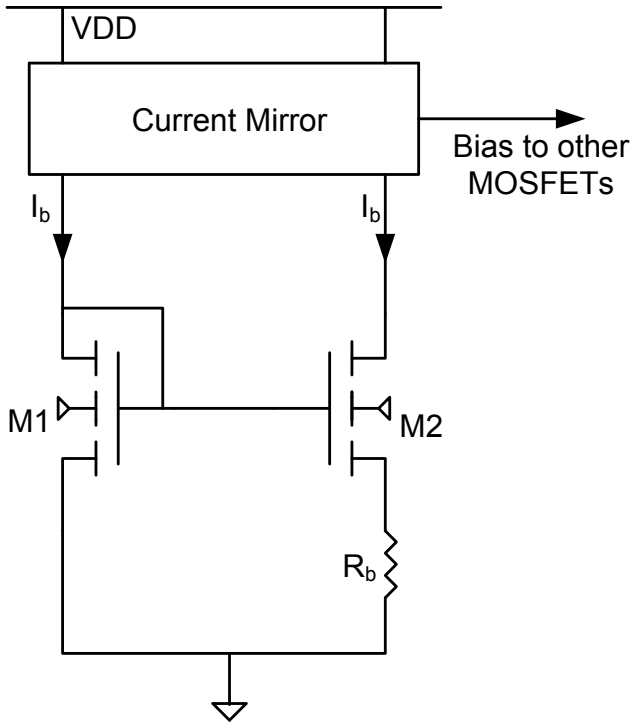


Figure 1.10 A constant-g_m biasing circuit

where, R_b is the biasing resistor and W, L are the width and length, respectively, of the transistors. Because the transistor dimensions are independent of temperature, the transconductance is determined by the resistor R_b. When a resistor with low temperature coefficient is used, the transconductance is almost constant over temperature change. This is why it is called as constant-g_m biasing circuit. This circuit will be discussed later with more details in this thesis.

1.6.3 ANALOG SWITCH OPTIMIZATION

Transmission gates which are constructed by a pair of NMOS and PMOS transistors are often used as switches in sample/hold and switched-capacitor circuits. At high temperatures, the

junction leakage current in the switch can cause a voltage drop on the hold capacitor, which can be explained as follows.

Figure 1.11 shows a transmission gate including the leakage diodes and the hold capacitor [49]. When $V_{Control}$ is high, the transmission gate is turned on and the voltage on the hold capacitor C_{Hold} is charged to V_{IN}. When $V_{Control}$ is low, the transmission gate is turned off and the stored voltage on the hold capacitor C_{Hold} is supposed to be maintained. However, junction leakage current will flow from VDD to C_{Hold} in the PMOS transistor and from C_{Hold} to VSS in the NMOS transistor. And the leakage current in NMOS transistor is about 10 times larger than in PMOS transistor. Due to the leakage current mismatch, a net leakage current of 9x I_{LEAK} will drain charge from the hold capacitor C_{Hold}, causing a significant voltage drop on the stored voltage. Recall from Equation (1.15), the leakage current is proportional to the p-n junction area. To alleviate the voltage drop at high temperature, minimum size transistors should be used in the transmission gate and ring-shaped layout should be used to minimize the diode junction area and therefore limit the leakage current on the sample node. PMOS-based transmission gates should be used where applicable to reduce the leakage current. In this case, however, the range of the voltage to be passed through the transmission gate is limited by the PMOS transistor.

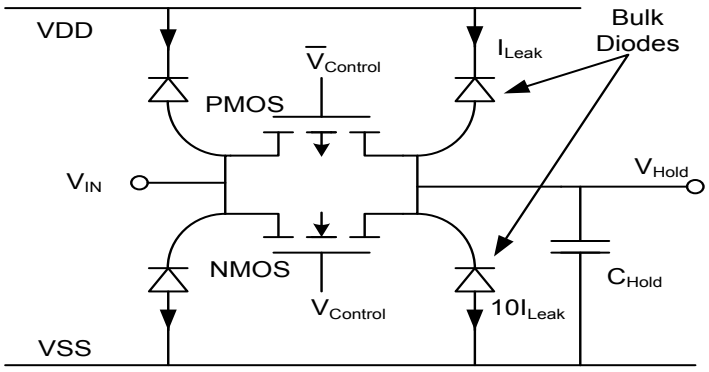


Figure 1.11 CMOS transmission gate with the leakage diodes and the hold capacitor

1.7 THESIS OBJECTIVES AND ORGANIZATION

The major objective of the work presented in this thesis is to develop various capacitance readout circuits for capacitive MEMS sensors in IBM 0.13 μm bulk CMOS process which includes a 2.5 V power supply. Three capacitance readout circuits, including capacitance to voltage, capacitance to frequency, and capacitance to digital circuits, are designed and tested. These proof-of-concept circuits are expected to operate at temperature range between -55 ºC to 225 ºC with temperature-stable performance. The detailed circuits design and measurement results will be introduced in the next chapters.

The organization of the thesis is as follows. In Chapter 2, the constant-g_m biasing technique is studied in detail and the core building blocks in the readout circuits including the amplifiers are designed and tested. These building-block circuits will be used in the capacitance readout circuits in Chapters 3, 4 and 5.

Chapter 3 presents a differential capacitance to voltage interface circuit which offers the flexibility to interface with MEMS capacitive sensors with a wide range of the steady-state capacitance values from 0.5 pF to 10 pF. Simulation and experimental results from -55 ºC to 225 ºC are presented and discussed. This interface circuit is tested with a commercially available MEMS capacitive pressure sensor.

Chapter 4 describes a capacitance to frequency interface circuit where a current to frequency conversion circuit is used to convert the sensor capacitance into digital pulse signal modulated in frequency. Pulse width control is implemented using off-chip components to adjust the pulse width of the output digital signal. The pulse width is adjustable with off-chip components.

Simulation and experimental results over temperature range between -55 ºC and 225 ºC are provided and further improvement is proposed.

Chapter 5 focuses on the design of a capacitance to digital readout circuit which uses a sigma-delta technique to convert the input ratio between sensor and reference capacitors into a high-accuracy digital output. The basic circuit architecture and the working principle of the capacitance to digital readout circuit are described first. Then, an improved circuit is presented to reduce sensitivity to non-ideal effects and high temperature effects. Simulation and experiments results for wide temperature range are shown and discussed.

Finally, chapter 6 summarizes the major contributions of this thesis and provides some suggestions for possible future improvements.

1.8 CLAIMS OF ORIGINALITY

To the best of my knowledge, the works included in this thesis are original and contain no materials previously published by another person except where due references are made. The originality of this thesis is listed below.

In Chapter 3, we develop a novel CMOS differential capacitance to voltage readout circuit for capacitive MEMS pressure sensors that is functional over a wide temperature range between −55 °C and 225 °C. The circuit offers the flexibility to interface with MEMS sensors with a wide range of the steady-state capacitance values from 0.5 pF to 10 pF.

In Chapter 4, we present a CMOS capacitance to frequency readout circuit for capacitive MEMS sensors which can operate over temperatures from −55 °C to 225 °C. A current to

frequency conversion circuit is used to convert the sensor capacitance into digital pulse signal which is modulated in frequency. The pulse width is adjustable with off-chip components.

In Chapter 5, we describe a CMOS capacitance to digital readout circuit for capacitive MEMS sensors which can work for the temperature range from -55 ºC to 225 ºC. Sigma-delta technique is used to offer the potential to achieve high accuracy and ease of signal processing and transmission.

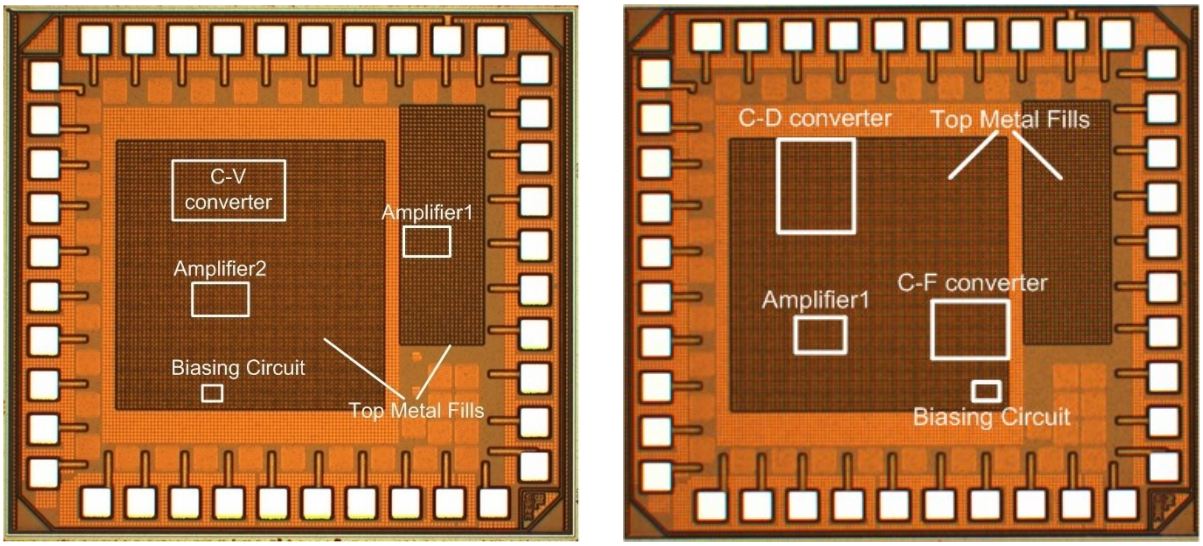
CHAPTER 2 DESIGN OVERVIEW AND BASIC CIRCUIT BUILDING BLOCKS

As mentioned in Chapter 1, the constant-g_m biasing is a popular high-temperature design technique and it has been proven effective to stabilize the performance of CMOS analog circuits at temperatures up to 300ºC. In this chapter, the constant-g_m biasing technique is studied in detail. The amplifier is an indispensable building block in any sensor interface circuits and its overall performance, including open-loop gain, bandwidth, stability, degrades significantly at high temperatures. Two amplifiers, one with single-ended folded-cascode structure, and another one with fully differential folded-cascode structure, are designed and biased using the constant-g_m biasing circuit. Their performance over wide temperature range is simulated and verified with experimental results.

2.1 CIRCUIT DESIGN OVERVIEW AND TESTING ENVIRONMENTS

All the circuits in this thesis are designed using Cadence custom IC design tools with IBM 0.13 μm CMOS process (IBM 8RF-DM CMOS Process). The circuit design tools and the circuit fabrication and packaging service are provided through the Canadian Microelectronics Corporation (CMC). IBM 0.13 μm CMOS process is chosen because of its good balance between low cost and high level of integration. This process has 8 layer metal stacks, including 3 thin metal layers (M1/M2/M3), 2 thick metal layers (MQ/MG), and 3 thick RF metal layers (LY(Al), E1(Cu), and MA(Al)). Two types of MOS transistors are available from this process: 1)

Transistor with thin gate oxide, the minimum width/length is 0.16/0.12 μm and the supply voltage is 1.2 V. 2) Transistor with thick gate oxide, the minimum width/length is 0.36/0.24 μm and the supply voltage is 2.5 V. More information about this process can be found at the Metal Oxide Semiconductor Implementation Service (MOSIS) website [79]. To get larger voltage headroom, thick gate oxide transistors are used in this thesis and hence 2.5 V power supply is used accordingly. For IBM 0.13 μm CMOS process, the device models provided by the foundry are only valid from -55 ºC to 125 ºC. Previous work has verified that there is still a good agreement between the device models and the experimental results at temperature up to 180 ºC for MOS transistors with medium length (L=2.5× of the minimum length) [80]. The circuits in this thesis are simulated at temperature range from -55 ºC to 225 ºC by simply changing the temperature setting in the Cadence Spectre simulator. The actual performance of these circuits at different temperatures is verified with experimental results.



(a) (b)

Figure 2.1 Micrograph of the fabricated IC chips. The chip label is at the lower right corner (a) the chip with chip label BLV32E (b) the chip with chip label ALV38C

Two IC chips were fabricated through the IC fabrication service provided by CMC. Figure 2.1 shows both the fabricated IC chips. The circuits are beneath the top metal fills (MA layer) of the chips so their details cannot be seen under the microscope. Their positions in the chips are highlighted using a white box. The first chip (with chip label BLV32E) was delivered in March 2013. It included a constant-g_m biasing circuit, a single-ended folded-cascode amplifier (amplifier 1), a fully differential folded-cascode amplifier (amplifier 2), a capacitance to voltage readout circuit (C-V converter), and other testing structures. The second chip (with chip label ALV38C) was delivered in February 2014. It included a constant-g_m biasing circuit, an improved single-ended folded-cascode amplifier (amplifier 1), a frequency readout circuit (C-F converter), a capacitance to digital readout circuit (C-D converter), and other testing structures. It should be noticed that these two chips used the same top metal fills so they look like same.

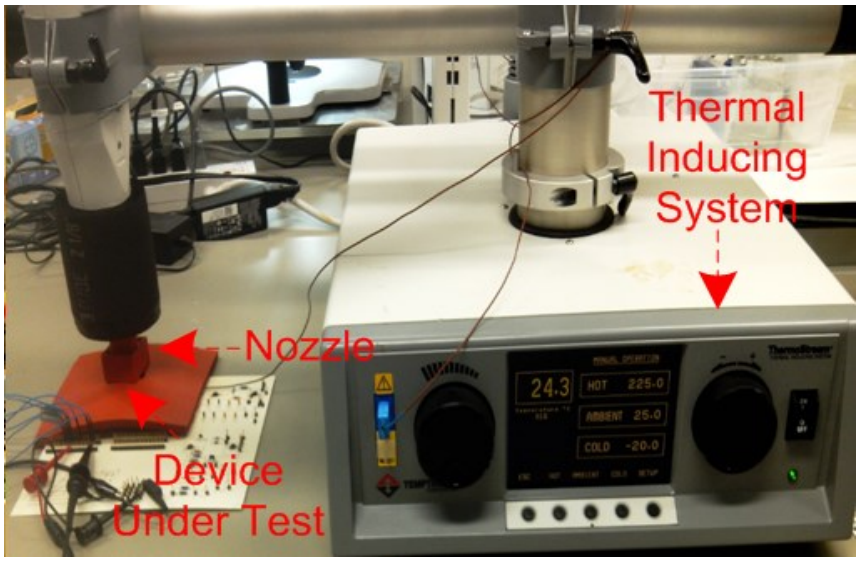


Figure 2.2 The chip testing setup

The chips are tested at different temperatures using a thermal inducing system (Thermostream TP04100A, Temptronic Corp., Mansfield, MA, USA) shown in Figure 2.2. The chip to be tested is mounted on a PCB board made of Rogers 4350B, a material with glass transition temperature of 280 °C. The thermal inducing system can change the temperature of the chip under test by blowing cold or hot air flow through the nozzle. In the testing, only the chip temperature is changed. The actual temperature of the chip is monitored by a thermocouple with ± 1 °C accuracy. The chip temperature can be changed from -20 °C to 225 °C, which is the maximum temperature range the thermal inducing system can offer. Generally, colder temperatures between −55 °C and −20 °C do not have detrimental effects on CMOS electronics and further help to improve signal to noise ratio due to reduced noise effects.

2.2 CONSTANT-GM BIASING TECHNIQUE

A biasing circuit using constant-g_m biasing technique is shown in Figure 2.3. Transconductance (g_m) is a critical parameter which affects open-loop gain, bandwidth, and stability of an amplifier. The g_m of a MOS transistor in saturation region, when neglecting channel length modulation and the body effect, can be expressed by Equation (2.1),

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \quad (2.1)$$

where, W and L are the channel width and length of the transistor, μ is carrier mobility, C_{ox} is the oxide capacitance per unit area, and I_D is the drain current of the MOS transistor. Equation 2.1 shows that as temperature increases, carrier mobility decreases, hence g_m decreases. In Figure 2.3, the current in the left branch is forced to be equal to the current in the right branch by current

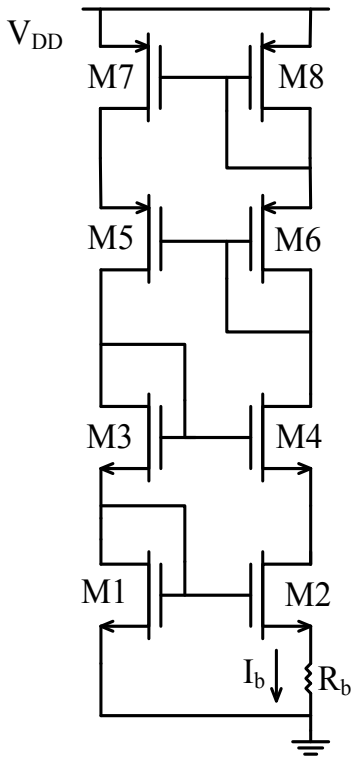


Figure 2.3 Constant-g_m biasing circuit

mirrors formed using M7/M8, M5/M6, and M3/M4. For transistors M1 and M2, since their gates are tied together, we can write the following Equation (2.2),

$$V_{GS1} = V_{GS2} + I_b R_b \quad (2.2)$$

where, R_b is the biasing resistor and I_b is the current flowing through it. Neglecting the channel length modulation effect, the drain current of a NMOS transistor operating in saturation region can be expressed by Equation (2.3),

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (2.3)$$

Further, Equation (2.2) can be rewritten as Equation (2.4),

$$\sqrt{\frac{2I_b}{\mu_n C_{ox} W_1 / L_1}} + V_{TH1} = \sqrt{\frac{2I_b}{\mu_n C_{ox} W_2 / L_2}} + V_{TH2} + I_b R_b \quad (2.4)$$

Neglecting the body effect, and considering the convention that M1 and M2 have same length but different width, then the threshold voltages V_{TH1} and V_{TH2} are equal. And from Equation (2.4), the current I_b flowing through the biasing resistor R_b can be expressed by Equation (2.5),

$$I_b = \frac{2}{\mu_n C_{ox} R_b^2} \left(\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}} \right)^2 \quad (2.5)$$

As can be seen, this current I_b is inversely proportional to the carrier mobility μ_n and the biasing resistor R_b, which change with temperature. When a MOSFET is biased using a copy of the biasing current I_b, the transconductance of this MOSFET can be expressed as, by inserting Equation (2.5) into Equation (2.1), as given by Equation (2.6),

$$g_m = \frac{2}{R_b} \sqrt{\frac{W}{L}} \left(\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}} \right) \quad (2.6)$$

It is realistic to make an assumption that the sizes of transistors do not change with temperature in our working range. Hence, in Equation (2.6), the only parameter which varies with temperature is the biasing resistor, R_b. Hence, if R_b has a zero temperature coefficient (TC), then ideally, g_m would not change with temperature variations. The IBM 0.13 μm CMOS technology offers a poly resistor with TC around 100 ppm/ºC. So the constant-g_m biasing circuit implemented with this resistor can bias MOS transistors for considerably stable g_m over a wide temperature range. The temperature stability of this circuit can be further improved by replacing the biasing resistor R_b using two different kinds of resistors, one with positive TC and another

with negative TC, connected in series with proper ratio to achieve a combined resistor with near zero TC [78].

In the above calculation, $V_{TH1}=V_{TH2}$ is assumed by neglecting the body effect, which introduces some error and can significantly affects the temperature coefficient of g_m. When the body effect is taken into account, because the voltage difference between the source and body of M2 in Figure 2.3, the threshold voltage of M2 can be expressed from Equation (1.9) as Equation (2.7),

$$V_T = V_{T0} + \gamma_n \left[\sqrt{2\phi_F + V_{sb}} - \sqrt{2\phi_F} \right] \quad (2.7)$$

where, V_{sb} is the voltage difference between source and body, V_{T0} is the threshold voltage when $V_{sb}=0$, and γ_n is the body effect parameter. Substituting Equation (2.7) into Equation (2.4) yields Equation (2.8),

$$\sqrt{\frac{2I_b}{\mu_n C_{ox} W_1 / L_1}} + V_{T0} = \sqrt{\frac{2I_b}{\mu_n C_{ox} W_2 / L_2}} + V_{T0} + \gamma_n \left(\sqrt{2\phi_F + I_b R_b} - \sqrt{2\phi_F} \right) + I_b R_b \quad (2.8)$$

The term $\left(\sqrt{2\phi_F + I_b R_b} - \sqrt{2\phi_F} \right)$ can be written as $\sqrt{2\phi_F} \left(\sqrt{1 + \frac{I_b R_b}{2\phi_F}} - 1 \right)$, which can be approximated as $\sqrt{2\phi_F} \left(\frac{1}{2} \cdot \frac{I_b R_b}{2\phi_F} \right)$ when $\frac{I_b R_b}{2\phi_F}$ is designed to be much smaller than 1 [45]. Then Equation (2.8) can be written as Equation (2.9),

$$\sqrt{\frac{2I_b}{\mu_n C_{ox}}} \left(\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}} \right) = \frac{\gamma_n}{2} \frac{I_b R_b}{\sqrt{2\phi_F}} + I_b R_b \quad (2.9)$$

Solving Equation (2.9), I_b can be expressed as Equation (2.10),

$$I_b = \frac{2}{\mu_n C_{ox}} \cdot \frac{1}{R_b^2 \left(1 + \frac{\gamma_n}{2\sqrt{2\phi_F}}\right)^2} \left(\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}}\right)^2 \tag{2.10}$$

Substituting Equation (2.10) into Equation (2.1), then g_m can be expressed as Equation (2.11),

$$g_m = \frac{2}{R_b \left(1 + \frac{\gamma_n}{2\sqrt{2\phi_F}}\right)} \sqrt{\frac{W}{L}} \left(\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}}\right) \tag{2.11}$$

Comparing Equation (2.11) with Equation (2.6), we can see that the body effect introduces a term $\left(1 + \frac{\gamma_n}{2\sqrt{2\phi_F}}\right)^{-1}$ to the expression of g_m. This term has a negative temperature coefficient because the term $2\Phi_F$ shows a temperature dependence of about -2.3 mV/ºC at 300 K [77]. In a standard bulk CMOS process, the substrate (body) is shared by all NMOS transistors, so it is not practical to cancel the body effect by connecting the source of M2 to the body. Because the N well of PMOS transistors are separated, a possible remedy to body effect is to place the biasing resistor in the source of M8 and tie the source and body of each PMOS transistor [81].

Figure 2.4 shows the detailed constant-g_m biasing circuit which includes the start-up circuit, constant-g_m biasing core, cascode biasing generator, and the biasing testing current. Biasing voltages P_{bias}, P_{cas}, N_{cas}, V_{CM}, and N_{bias} will be used to bias amplifiers shown in the next section. I_{bias} is an identical copy of current I_b generated by current mirror and it will be used for testing. In this work, a 9 kΩ precision poly resistor (model name “oprppres”) is used as the biasing resistor and M2 is designed to be 4 times bigger than M1. For an “oprppres” resistor with 740

nm width, simulated result shows it has a TC of 72.5 ppm/ ºC from 25 ºC to 125 ºC. The simulated biasing current I_b from -55 ºC to 225 ºC is shown in Figure 2.5. As can be seen, the biasing current I_b in the constant-g_m biasing circuit increases almost linearly from 8.4 µA at -55 ºC to 11.7 µA at 225 ºC. This biasing current is large enough to minimize the leakage current effect in the biasing circuit.

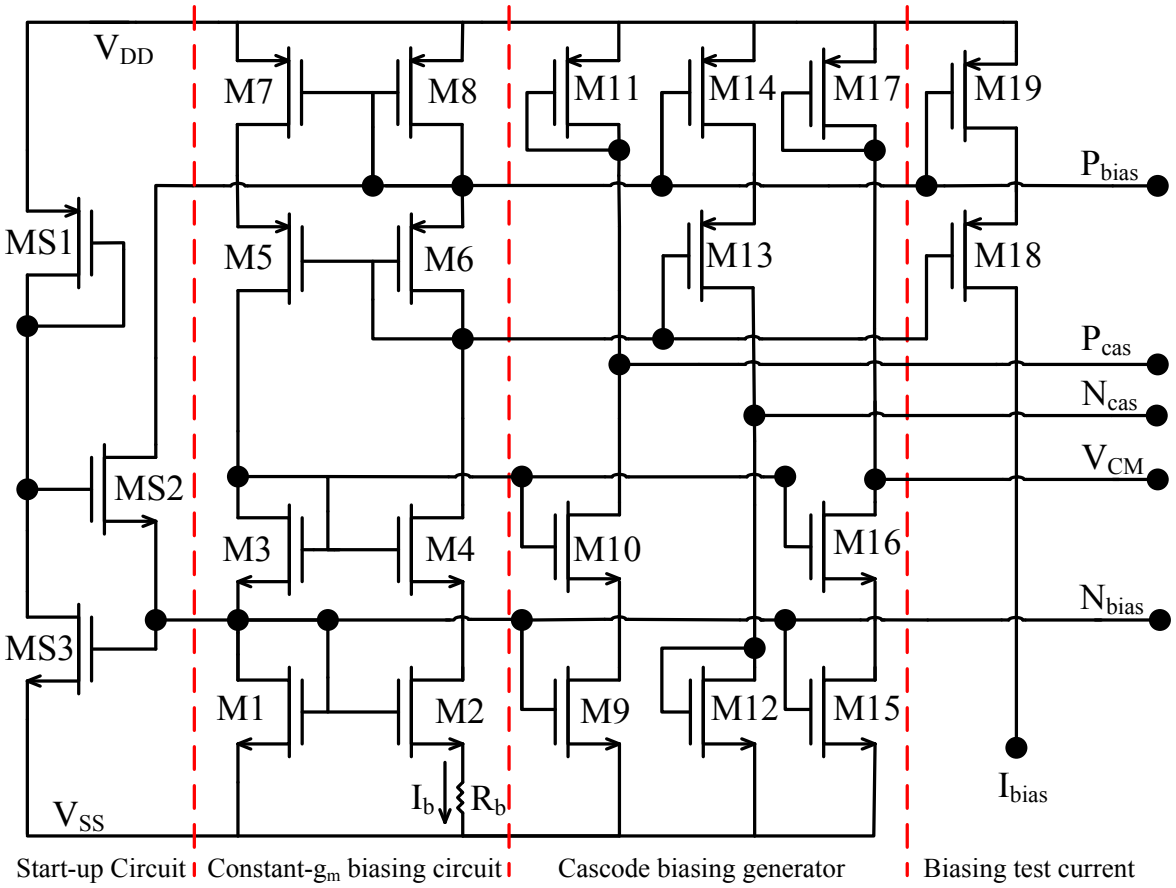


Figure 2.4 Detailed constant-g_m biasing circuit

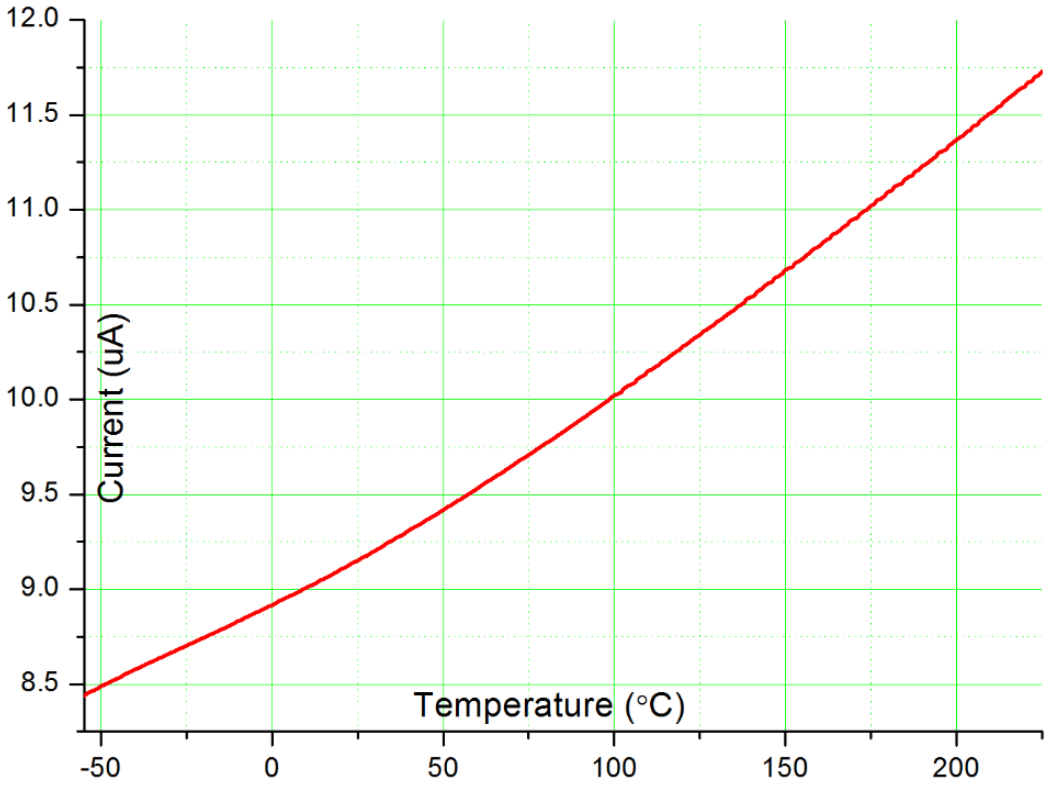


Figure 2.5 Simulated constant-g_m biasing current I_b

2.3 General Purpose High-Temperature Amplifiers

As temperature increases, open loop gain of an amplifier decreases. Thus, a large open loop gain is required for high-temperature amplifier such that it still has sufficient gain at target temperature. Further, sensor interface circuits typically include an analog to digital converter (ADC) circuit. Hence, the front-end amplifier should be capable of driving a capacitance load. The commonly used two-stage amplifier will be unstable for large capacitance load if a nulling resistor is not added. As shown in Figure 2.6, a single-ended folded-cascode amplifier structure is chosen in this work as it not only has the gain of a two-stage amplifier but also offers self-

compensation, good input common-mode range, and better power supply rejection ratio. Compared to the telescopic structure, the folded-cascode amplifier has lower voltage headroom requirement and it also provides better performance stability [81].

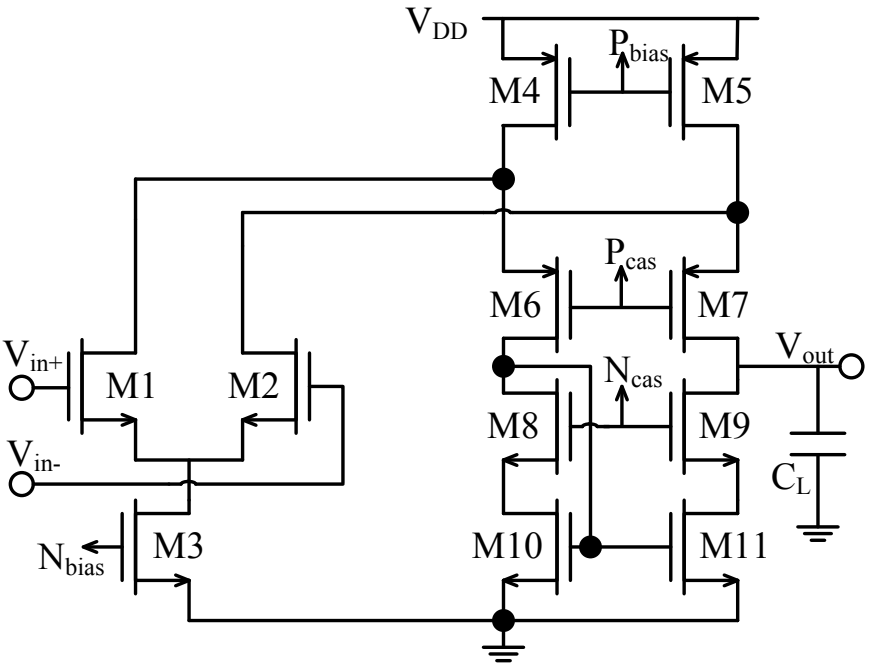


Figure 2.6 Schematic of the folded-cascode amplifier

All the biasing voltages are provided by the constant-g_m biasing circuit shown in Figure 2.4. An NMOS input pair is chosen to achieve larger gain with reasonable device sizes. The current in the differential input pair does not need to be perfectly balanced because the biasing DC current can flow into or out of the cascode current mirror to compensate it. The drain current in M4 and M5 is designed bigger than the current flowing through M3 to make sure the cascode current mirror never goes to zero. The detailed information for analyzing and designing a folded-cascode amplifier can be found in [82].

Figure 2.7 shows the simulated open-loop frequency response of the folded-cascode amplifier with an output load capacitance 2 pF over the temperature range from -55 ºC to 225 ºC. For such a wide temperature range, the DC gain variation is 4.2 dB and the phase variation is 11.2 degree. At 125 ºC, it has open loop gain of 72.1 dB, unity gain frequency of 31.4 MHz and phase margin of 64.8 degree.

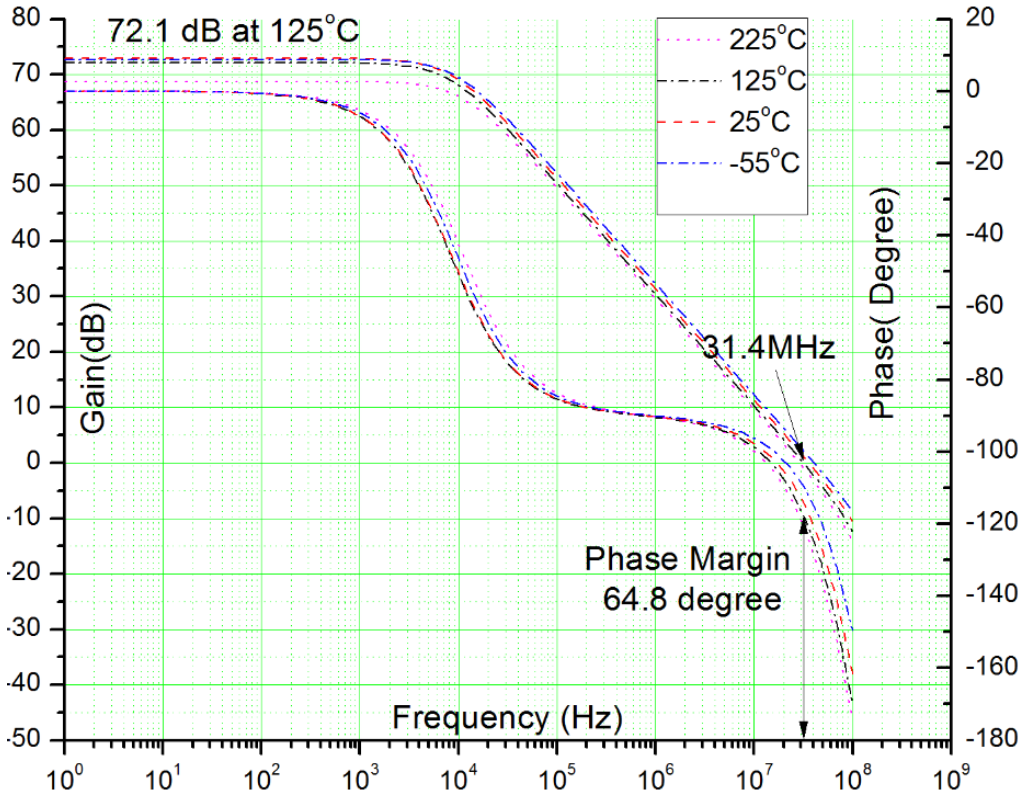


Figure 2.7 Simulated open-loop frequency response of the folded-cascode amplifier

As mentioned in Chapter 1, single-ended circuits are more susceptible to high temperature induced noises and leakage currents, which usually appear in common mode and can be differentially rejected. The fully-differential circuit structure can effectively reject these common mode errors and improve the circuit performance at high temperature. Figure 2.8 shows a fully-

differential folded-cascode amplifier modified from the amplifier shown in Figure 2.6. This amplifier structure has been proven to be stable operation at temperatures up to 250 ºC [45]. All the biasing voltages are provided using the constant-g_m biasing circuit.

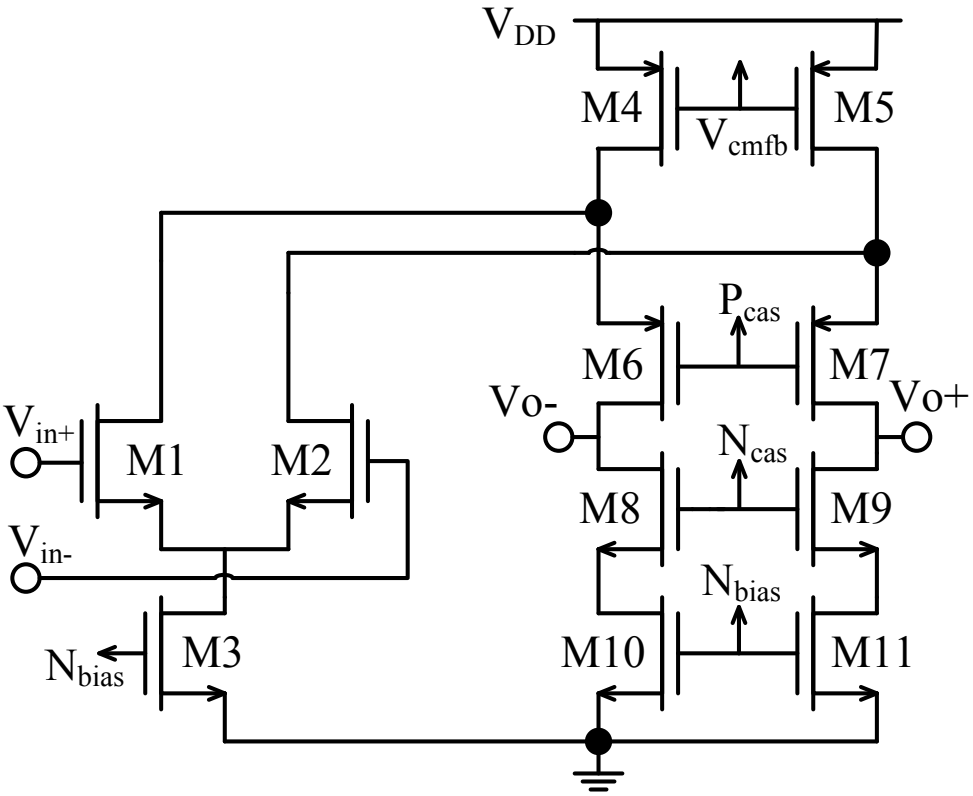


Figure 2.8 Schematic of the fully differential folded-cascode amplifier

A switched capacitance (SC) common mode feedback (CMFB) circuit, shown in Figure 2.9, is used to maintain the common mode of the differential output to be V_{CM}, half of the power supply. All the switches are implemented using CMOS transmission gates. V_{Pbias} and V_{CM} are the biasing voltages generated using the constant-g_m biasing circuit. When CLK_1 is high, capacitors C_1 sense the difference between V_{Pbias} and V_{CM}. When CLK_2 is high, charge in C_1 is quickly

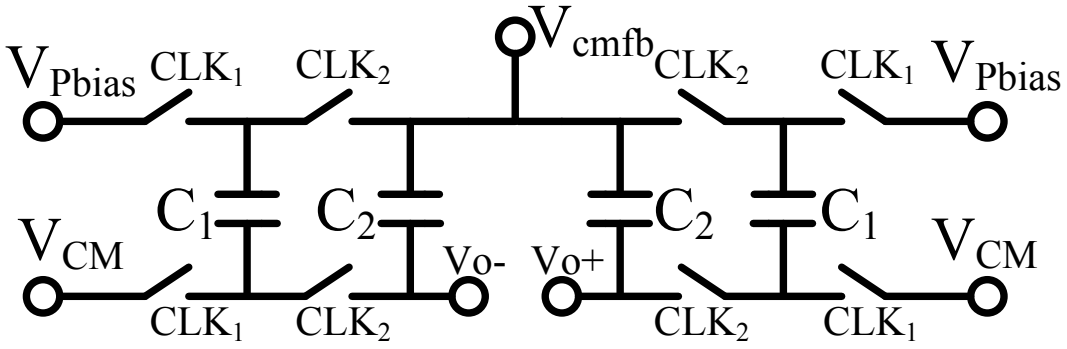


Figure 2.9 Schematic of the SC CMFB circuit

redistributed between C_1 and C_2. The common mode voltage difference between V_o and V_{cmfb} can be expressed as Equation (2.12) [83],

$$V_{o,cm}(n+1) - V_{cmfb}(n+1) = \left[1 - \left(\frac{C_2}{C_1 + C_2}\right)^{n+1}\right](V_{CM} - V_{Pbias}) \quad (2.12)$$

In steady state, the common mode voltage difference between V_o and V_{cmfb} is equal to V_{CM}-V_{Pbias}. Because V_{Pbias} is designed to be equal to V_{cmfb}, then the common mode voltage of V_o will be equal to V_{CM}, usually with a less than 10 mV difference caused by device mismatch.

Figure 2.10 shows the simulated single-ended open-loop frequency response of the fully differential folded-cascode amplifier with SC CMFB with an output load capacitance 2 pF over the temperature range from -55 ºC to 225 ºC. The DC gain variation is 3.9 dB and the phase variation is less than 5 degree when temperature changes from -55 ºC to 225 ºC. At 125 ºC, it has open loop gain of 70.3 dB, unity gain frequency of 13.01 MHz and phase margin of 77.9 degree.

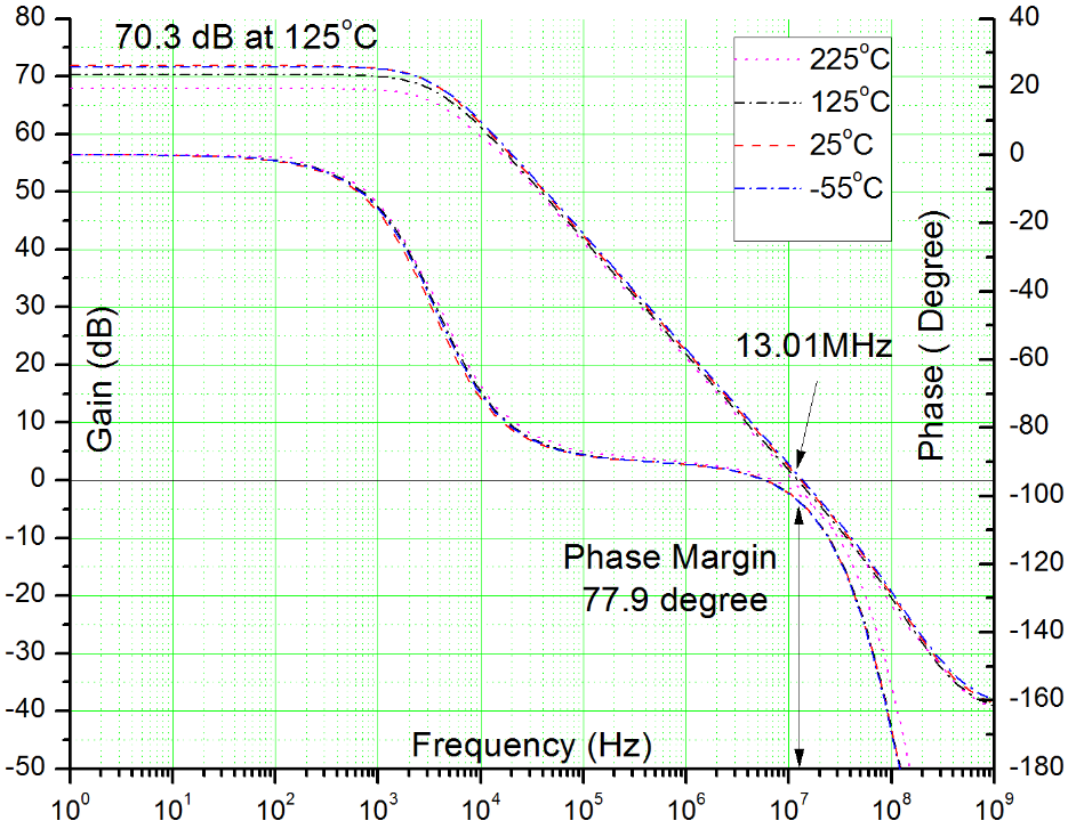


Figure 2.10 Simulated single-ended open-loop frequency response of the fully differential folded-cascode amplifier with CMFB

Figure 2.11 shows the simulated transient response of the fully differential folded cascode amplifier with CMFB circuit at 125 ºC. The input is a 200 Hz sine wave signal. At the beginning, the common-mode of the output voltage is close to zero because the leakage current of NMOS transistor at high temperature is higher than that of PMOS transistor and it pulls down the voltage. This effect decreases the voltage V_{cmfb} in the SC CMFB circuit so the bias current in the PMOS current source (M4 and M5 in Figure 2.8) is increased to compensate for the increased leakage current in the NMOS transistors. In this way, the common-mode of the output voltage is maintained at the desired value. As can be seen from Figure 2.11, the SC CMFB circuit

gradually pulls up the common-mode of the output voltage and after 25 ms it reaches the desired value of half of the power supply (V_{dd}/2=1.25V). If V_{cmfb} was instead connected to the gate of NMOS transistors (M10 and M11 in Figure 2.8), decrease of V_{cmfb} may cause the NMOS transistors to turn off and the circuit will fail.

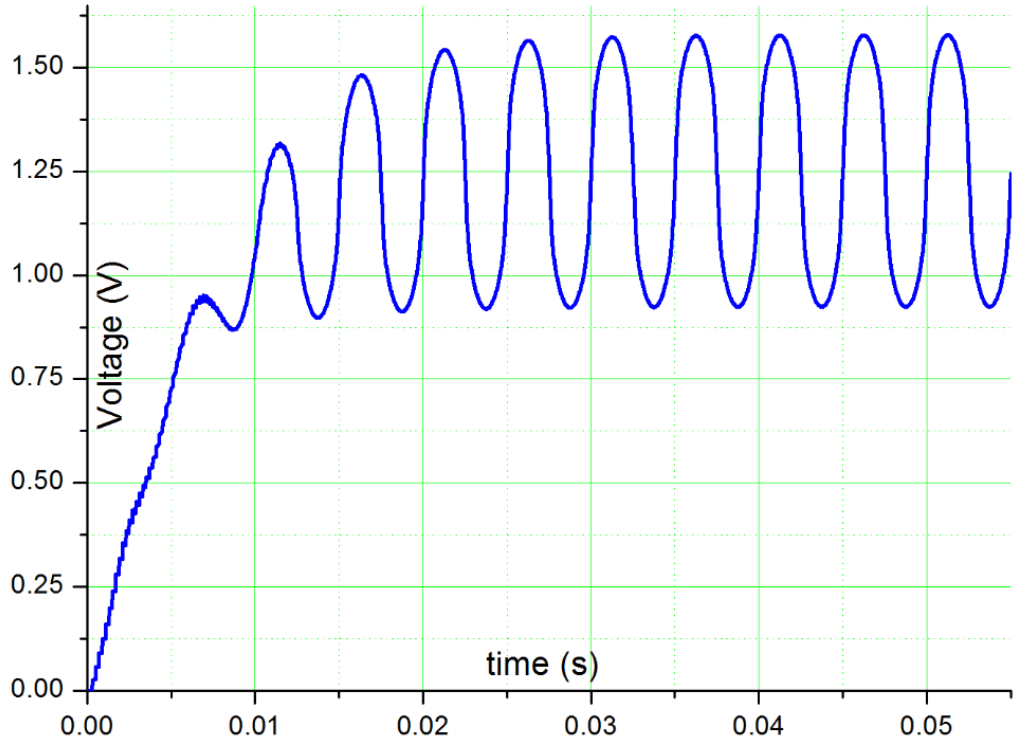


Figure 2.11 Simulated transient response of the fully differential folded-cascode amplifier with CMFB circuit at 125 ºC

2.4 EXPERIMENTAL RESULTS

The constant-g_m biasing circuit, the single-ended folded-cascode amplifier, and the fully-differential folded-cascode amplifier with SC CMFB circuit have been tested over the temperature range from -20 ºC to 225 ºC using the testing setup shown in Figure 2.2. The

measured constant-g_m biasing current I_b at different temperatures is shown in Figure 2.12. The data are averaged from ten measurements and the standard deviation is less than 0.01 uA. As can be seen, I_b changes almost linearly from 8.89 µA at -20 ºC to 12.94 µA at 225 ºC. Recalling Equation (2.5), this is because the carrier mobility decreases almost linearly with temperature, while other parameters remain largely unaffected.

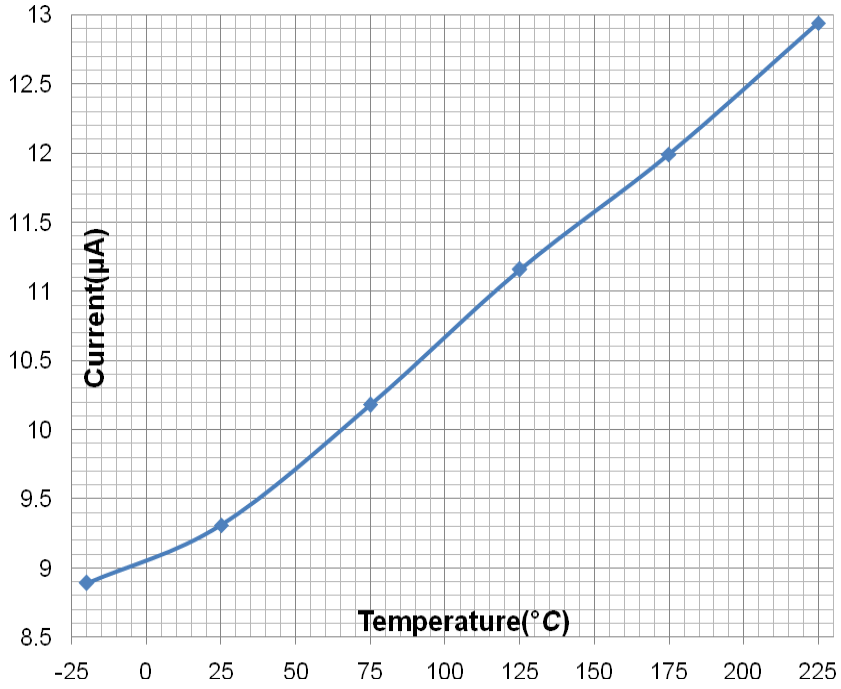


Figure 2.12 Measured constant-g_m biasing current I_b at different temperatures

The open loop frequency response of the single-ended folded-cascode amplifier with an output load capacitance of 2 pF is shown in Figure 2.13. From -20 °C to 225 °C, the DC gain varies only by 2.8 dB. At 225 °C, the amplifier still has a large DC gain (68.5 dB). The measured amplifier power consumption (including constant-g_m biasing circuit) at 225°C is 0.69 mW.

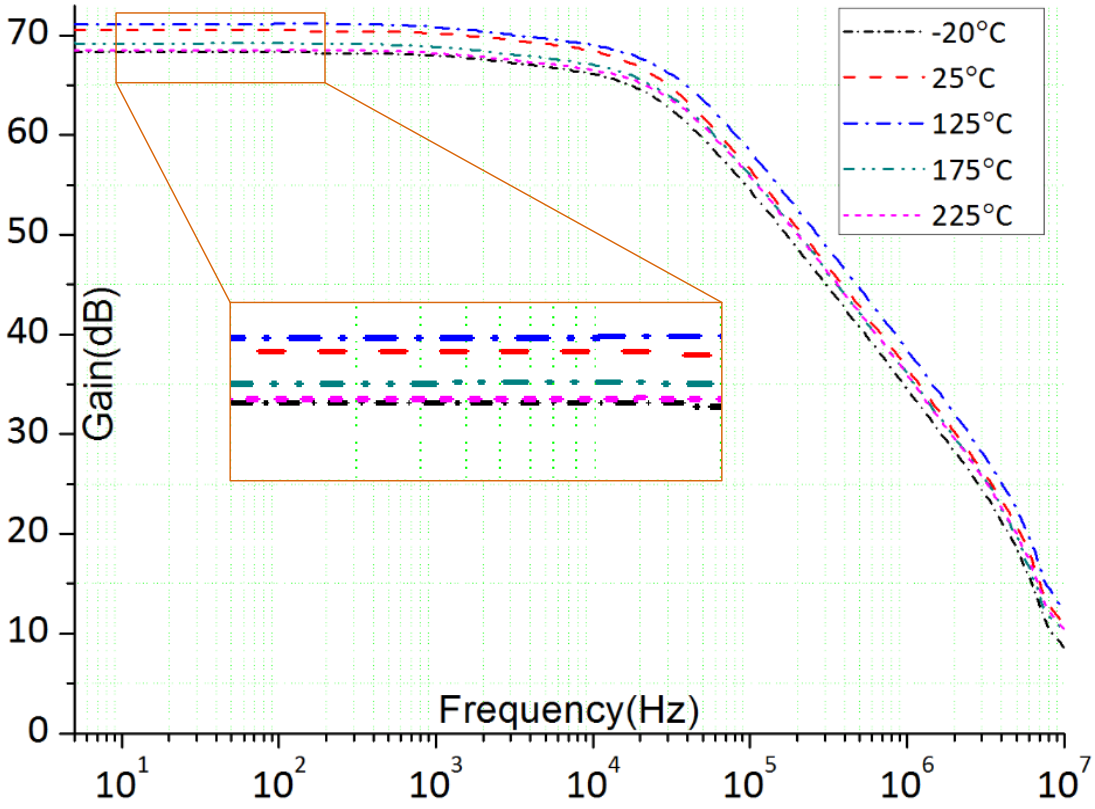


Figure 2.13 Measured open-loop frequency response of the single-ended Folded-cascode amplifier (with 2 pF load capacitance)

The measured open loop frequency response of the fully differential folded-cascode amplifier with SC CMFB circuit (single-ended output) with a load capacitance of 2 pF is shown in Figure 2.14. From -20 °C to 225 °C, the DC gain varies only by 2.1 dB. At 225 °C, the amplifier has DC gain of 68.9 dB. The measured amplifier power consumption (including constant-g_m biasing circuit) at 225 °C is 0.51 mW.

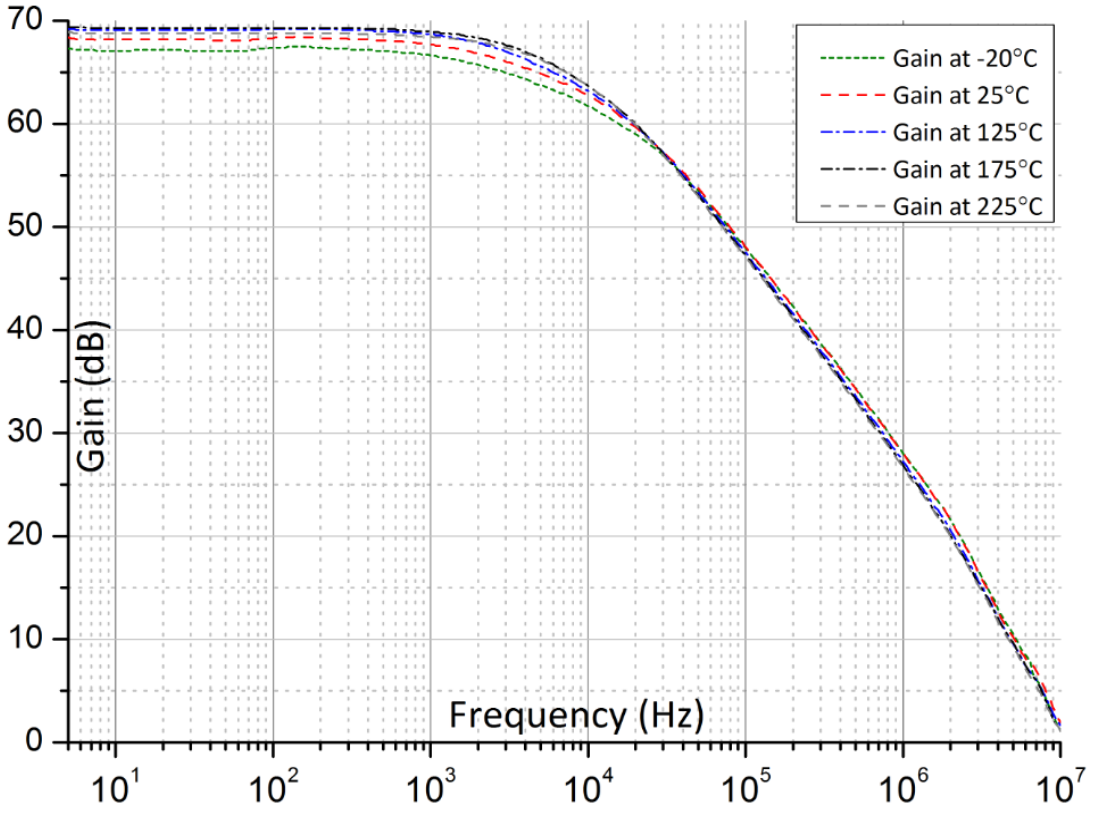


Figure 2.14 Measured open-loop frequency response of the fully-differential folded-cascode amplifier (single-ended output with 2 pF load capacitance)

The measurement results show that constant-g_m biasing technique can effectively stabilize amplifier gain over a wide temperature range. For IBM 0.13 μm CMOS technology, the foundry models provided are only valid between temperatures -55 ºC and 125 ºC, but they still have certain validity at temperatures beyond 125 ºC. Compared to the single-ended folded-cascode amplifier, from -20 °C to 225 °C, the fully-differential differential folded-cascode amplifier with SC CMFB circuit has slightly lower DC gain variation, due to the advantage of fully-differential structure.

2.5 SUMMARY AND CONCLUSIONS

In this chapter, we first introduced the circuit design and testing environments, including the IBM 0.13 μm CMOS process and the chip testing setup. The constant-g_m biasing technique is explained in detail. A single-ended folded-cascode amplifier and a fully-differential folded-cascode amplifier with SC CMFB circuit are designed, with biasing voltages provided by the constant-g_m biasing circuit. The constant-g_m biasing circuit and the two amplifiers are simulated at temperature from -55 °C to 225 °C and measured at temperature from -20 °C to 225 °C. The measurements results show that the constant-g_m biasing technique is an effective way to stabilize amplifier gain over wide temperature range, and the foundry models of the IBM 0.13 μm CMOS process still have certain validity at temperatures beyond 125 ºC.

In the following chapters, we will use the constant-g_m biasing circuit, the single-ended folded-cascode amplifier, and the fully-differential folded-cascode amplifier with SC CMFB circuit as key building blocks to construct several interface circuits for capacitive MEMS sensors.

CHAPTER 3 CMOS DIFFERENTIAL CAPACITANCE TO VOLTAGE READOUT CIRCUIT

In this chapter, we present a novel CMOS differential interface circuit for capacitive MEMS pressure sensors that is functional over a wide temperature range between −55 °C and 225 °C. The circuit offers the flexibility to interface with MEMS sensors with a wide range of the steady-state capacitance values from 0.5 pF to 10 pF. Simulation results show that the circuitry has excellent linearity and stability over the wide temperature range. Experimental results confirm that the temperature effects on the circuitry are small, with an overall linearity error around 2%.

3.1 CIRCUIT ARCHITECTURE

Several capacitance to voltage readout circuits for MEMS sensors have been developed [84-91]. These circuits can be categorized in three general groups: switched capacitor (SC) circuit, ac-bridge with voltage amplifier, and transimpedance amplifier [92]. Among the three groups of capacitive to voltage readout circuits, the SC readout circuit it offers the best tradeoff between complexity and performance. The commercially available MS3110 IC from ICS8 Inc. is a typical capacitance to voltage readout circuit using the SC technique. It offers high readout resolution and ultra-low noise. However, it can only work over the commercial temperature range from -40 °C to 85 °C. In our work, we use the similar circuit architecture as the MS3110 IC but extend the circuit operational temperature to the range from −55 °C to 225 °C. Figure 3.1a illustrates the schematic diagram of the differential wide temperature CMOS interface circuit for capacitive MEMS pressure sensors. The circuit uses a SC technique and a similar circuit has been used

previously by our group [93] for MEMS air flow sensors and by Patel *et al*. [94] towards chemocapacitive sensing of volatile organic compounds. Here, we use a differential input circuit

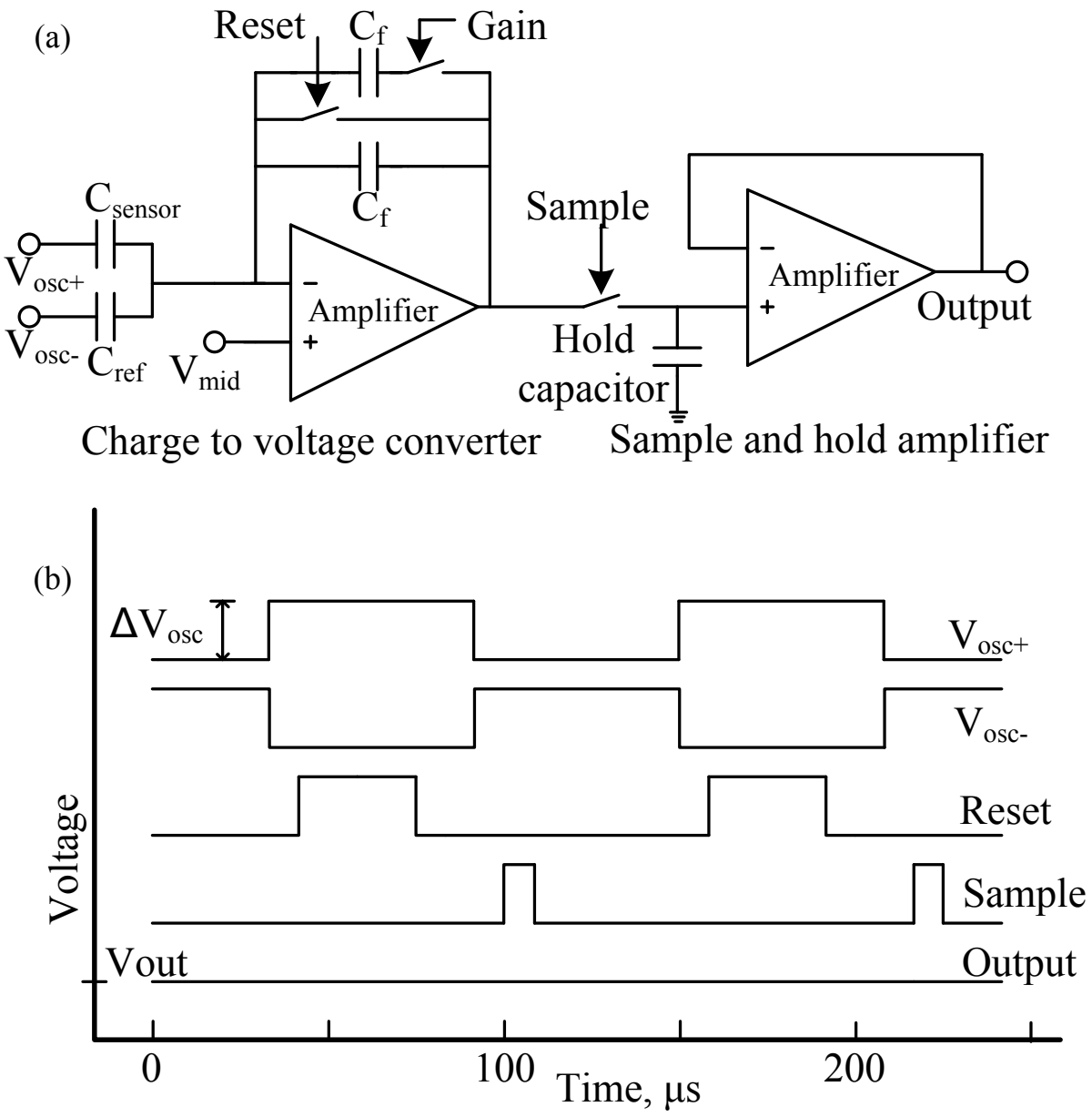


Figure 3.1 (a) Schematic diagram of the CMOS capacitance to voltage readout circuit; (b) Waveforms of the control and output signals for the CMOS circuit.

that enables working with MEMS sensors that have a wide range of the steady-state capacitance values from 0.5 pF to 10 pF. The circuit measures the capacitance of external sensor, C_{sensor}, and produces an analog output voltage, V_{out}. A reference capacitor, C_{ref} is needed that has a similar steady-state capacitance value as the sensor device, C_{sensor}, to extend the detection dynamic range while providing good capacitance detection resolution required for MEMS pressure sensors.

In operation, two 10 kHz square wave signals V_{OSC+} and V_{OSC-} with same amplitude but opposite phase are used to drive the sensor capacitor, C_{sensor} and reference capacitor, C_{ref}. Their amplitude is defined as ΔV_{OSC}. V_{mid} is a DC voltage applied to the non-inverting node of the amplifier. Reset, Sample and Gain are control signals where the Gain switch can adjust the feedback capacitance C_f in the circuit. A sample/hold circuit samples the voltage at the output of the first amplifier and the hold capacitor maintains the sampled voltage. In the present design, the hold capacitor C_H is set to 1 pF. The waveforms of the control and output signals for the converter circuit are shown in Figure 3.1b. The amplitude of the output voltage can be expressed as Equation (3.1),

$$V_{out} = V_{mid} + \Delta V_{osc} \frac{(C_{sensor} - C_{ref})}{C_{feedback}} \quad (3.1)$$

3.2 DETAILED CIRCUITS DESIGN

The fully-differential folded-cascode amplifier with a SC CMFB circuit (with single-ended output) designed in Chapter 2 is used as the amplifiers in Figure 3.1a. It is biased using the constant-g_m biasing circuit described earlier in Chapter 2. The control switches are implemented using transmission gates. Since the junction leakage current in PMOS transistor is much smaller

than in NMOS transistor [49], minimum size NMOS transistor is used in the transmission gates. PMOS transistor is sized such that $(W/L)_p = (\mu_n/\mu_p)*(W/L)_n$ to make the on-resistance of the switch relatively stable over wide voltage range. For the chip layout, common-centroid structures

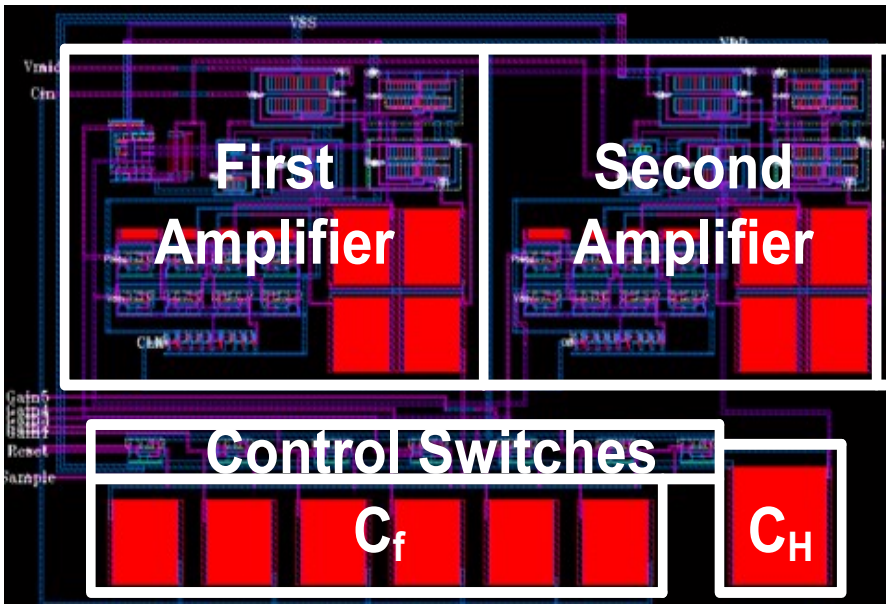


Figure 3.2 Layout of the capacitance to voltage readout circuit

are used wherever applicable to reduce temperature induced common mode errors. Guard rings are placed around performance sensitive blocks to prevent latch-up at high temperatures. Figure 3.2 shows the layout of the capacitance to voltage readout circuit. The effective area of the circuit is 440 μm×280 μm.

3.3 Experimental Results and Discussion

The capacitance to voltage readout circuit is simulated at temperatures from −55 °C and 225 °C and tested at temperatures from −20 °C and 225 °C. Again, the measured temperature

range is less due to the limit of the Thermostream testing system. Generally, colder temperatures between −55 °C and −20 °C do not have detrimental effects on CMOS electronics and further help to improve signal to noise ratio due to reduced noise effects. A calibration process is done first. The calibration capacitance, C_{sensor}, is constructed using nine capacitors, C_1 to C_9 with nominal capacitance value of 1 pF which are connected in series (shown in inset of Figure 3.3). By appropriately changing connections from C_1 to C_9, the capacitance value of C_{sensor} is varied and measured using a high resolution universal capacitance readout circuit, MS3110 from ICS8 Inc. that is maintained at room temperature (25 °C).

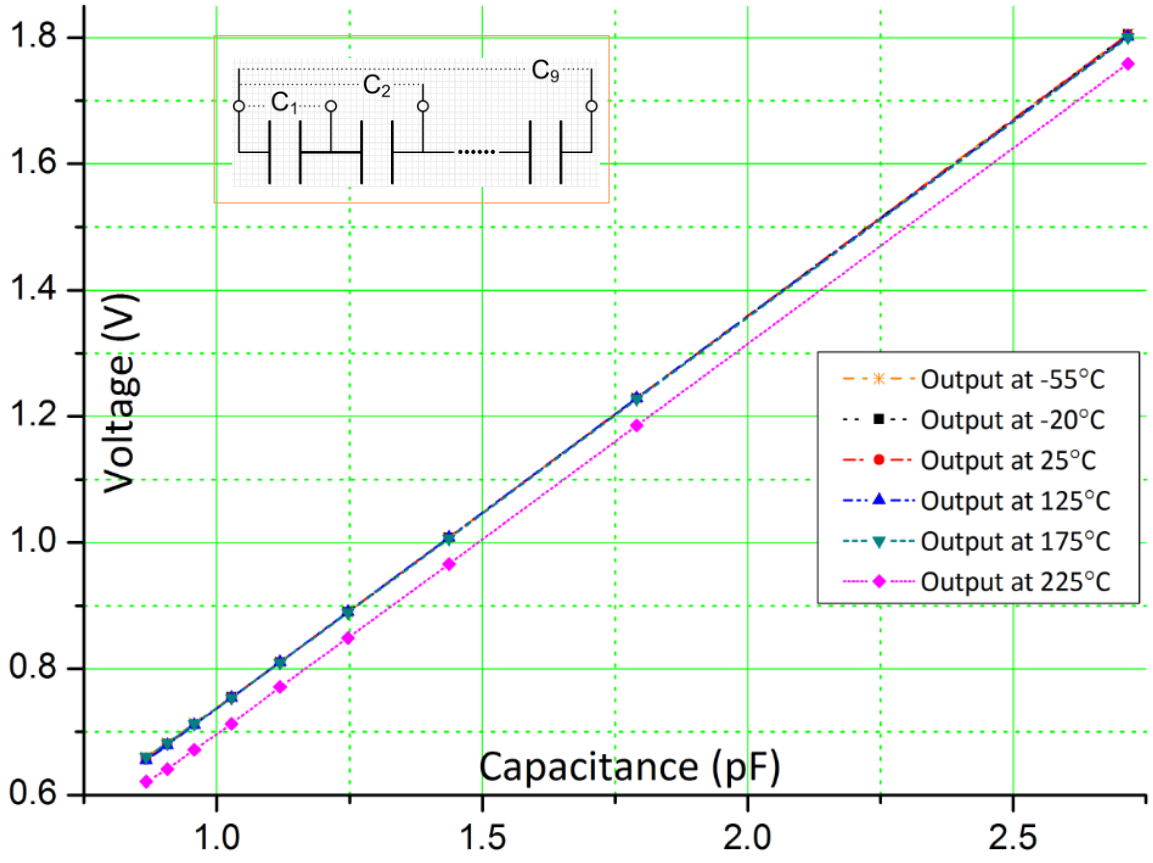


Figure 3.3 Simulated output voltages of the converter circuit at different temperatures

The control signals, V_{OSC+}, V_{OSC-}, Reset and Sample are generated by a data acquisition card, NI USB-6259 (National Instruments Inc., Austin, TX, USA). The amplitude of V_{OSC} is set to 1.25 V, V_{mid} is set to analog ground 1.25 V, the feedback capacitance, C_f is set to 2 pF, and the reference capacitance, C_{ref} is fixed to 1.805 pF. The sensor capacitor, C_{sensor}, and reference capacitor, C_{ref}, are placed at room temperature (25 °C) with only the test chip which includes the on-chip feedback capacitor C_f exposed to the temperature change from −20 °C to 225 °C.

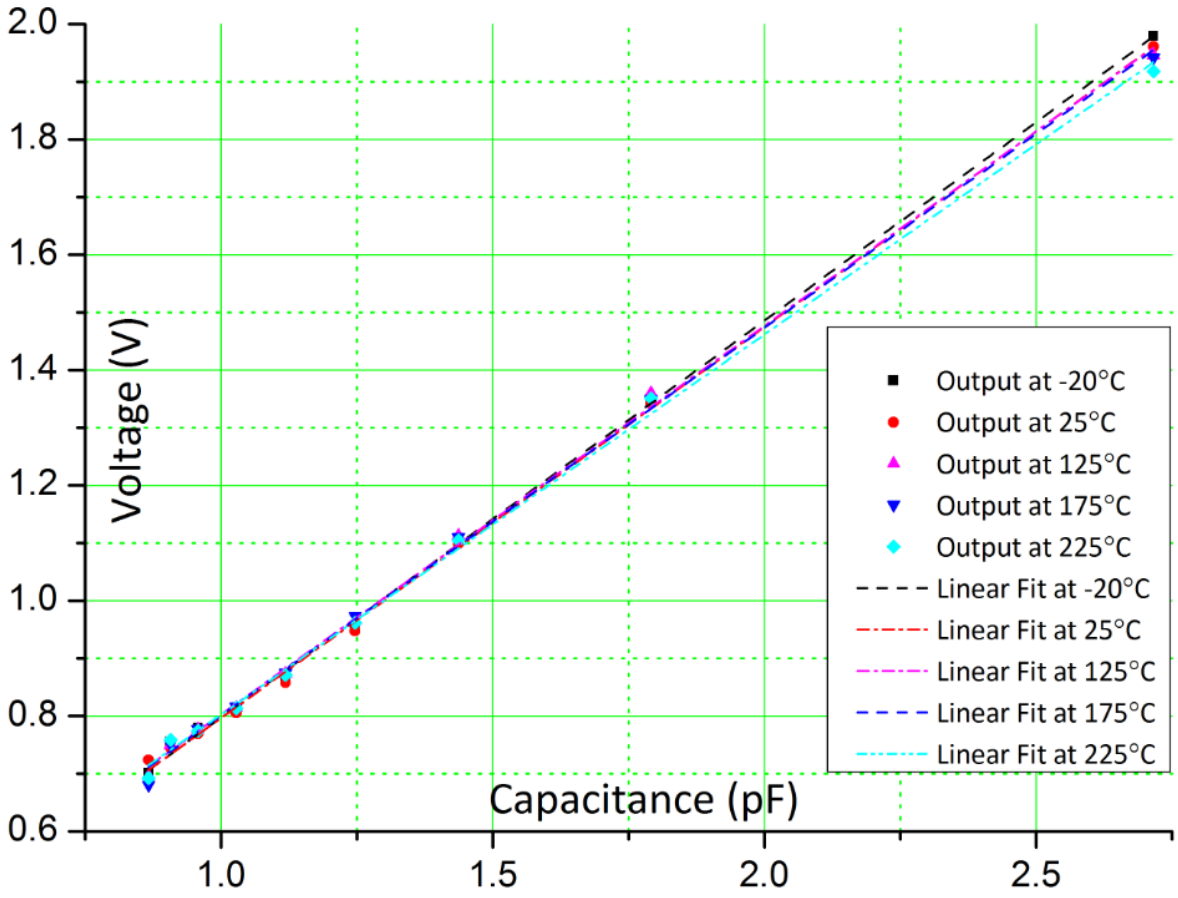


Figure 3.4 Measured output voltages of the converter circuit at different temperatures

Figure 3.3 shows the simulated output voltage of the capacitance to voltage readout circuit and Figure 3.4 shows the measured output voltage and both results show similar response. Over the wide temperature range, the circuit converts the input capacitance to output voltage with

goodness-of-fit of *linear* regression of 0.998 (R^2). Figure 3.5 shows the difference between the measured results and the linear fits, which is defined as, (measured value-fitted value)/(fitted value). The overall difference is around 2%, and larger difference is observed when the sensor capacitance is smaller and at high temperatures. The tested linearity is worse than the simulated results, especially when the capacitance is smaller and its probable cause could be interconnect parasitic capacitance in the experimental setup.

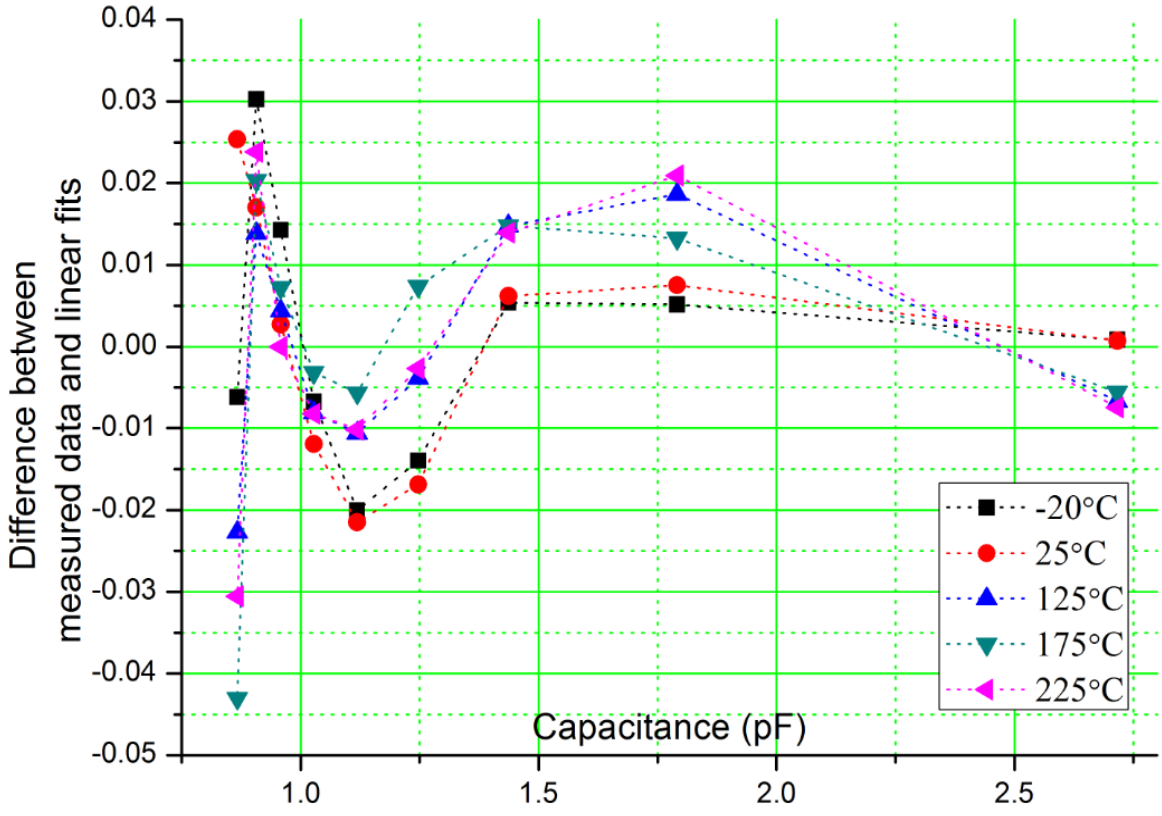


Figure 3.5 Difference between measured results and linear fits

The CMOS circuit is interfaced with a capacitive MEMS pressure sensor from Protron Mikrotechnik GmbH, Germany [95] by replacing the C_{sensor} with the pressure sensor in Figure

3.1. The micrograph of the MEMS pressure sensor is shown in Figure 3.6. The feedback capacitance, C_f is set to 2 pF. The sensor operates within a temperature range from −40 °C to +85 °C with a sensitivity of 1 fF/mbar. During our experimental testing, the MEMS pressure sensor is maintained at room temperature (25 °C) and placed in a pressure vessel so that its capacitance output does not change with ambient temperature and only varies when external pressure is applied to the pressure vessel.

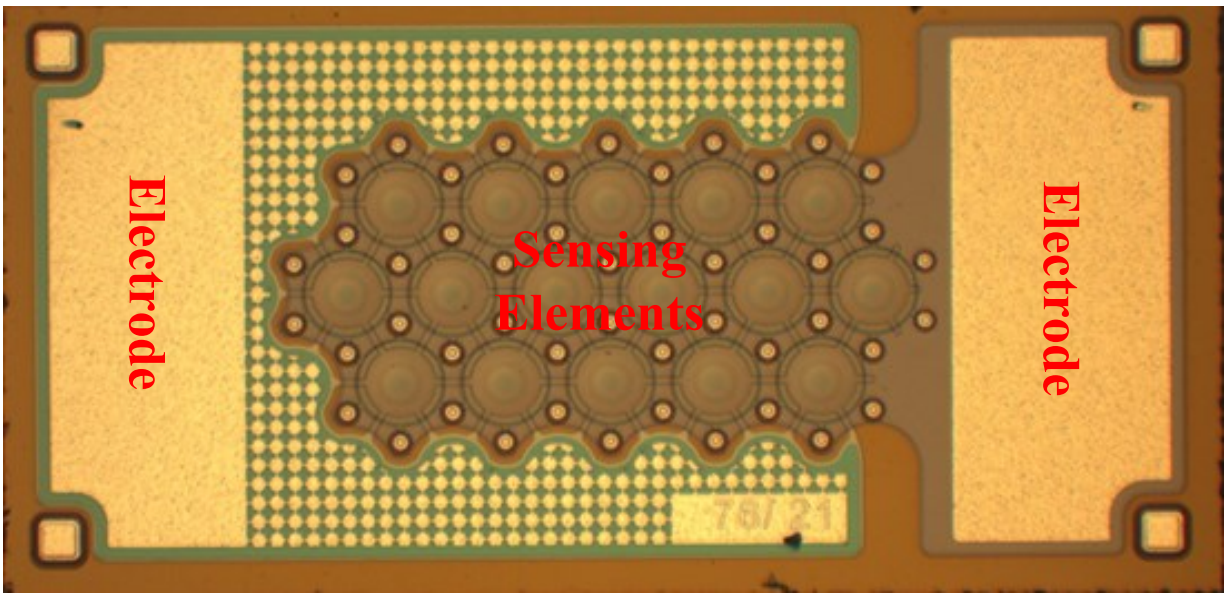


Figure 3.6 Micrograph of the capacitive MEMS pressure sensor

Figure 3.7 shows the measured capacitance change with the MS3110 capacitance readout circuit when the capacitive MEMS pressure sensor is exposed to different ambient pressures at 25 °C. Figure 3.8 shows the measured output voltage with our capacitance to voltage readout circuit when the MEMS pressure sensor undergoes different pressures. The CMOS capacitance to voltage readout circuit is exposed to temperature range from −20 °C to 225 °C, but the MEMS pressure sensor is maintained at 25 °C and exposed to only pressure variation from −0.25 bar to

+0.25 bar. All measurements are done in triplicate with the average value noted in Figure 3.8. As can be seen, the output voltage from the CMOS circuit changes in accordance with the capacitance change of the pressure sensor and provides a stable response over a temperature range from −20 °C to 225 °C. The estimated readout resolution is 2.32 mV/mbar at 225 °C.

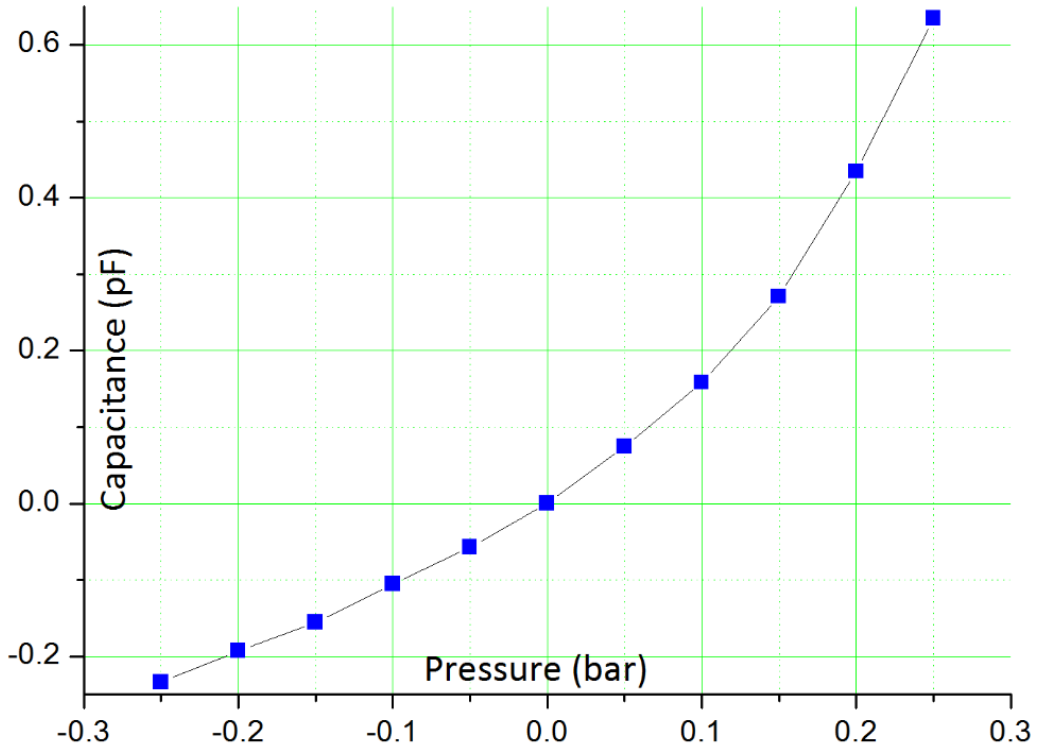


Figure 3.7 Measured Capacitance output change versus pressure change for the capacitive MEMS pressure sensor

As temperature increases, the output noise becomes larger. The simulated noise analysis shows the noise level at the output of the circuit in Figure 3.1a increases from 0.134 $mVHz^{-1/2}$ to 0.184 $mVHz^{-1/2}$ when temperatures changes from −55 °C to 125 °C. Another major error source at high temperatures is the leakage current in the Sample switch, which can cause a voltage drop or rise on the hold capacitor, depending on the direction of the leakage current. This problem can

be alleviated using higher sampling speed, or increasing the capacitance of the hold capacitor. A sample/hold circuit with dynamic switch leakage compensation [96] can also be used, with the penalty of increased circuit complexity.

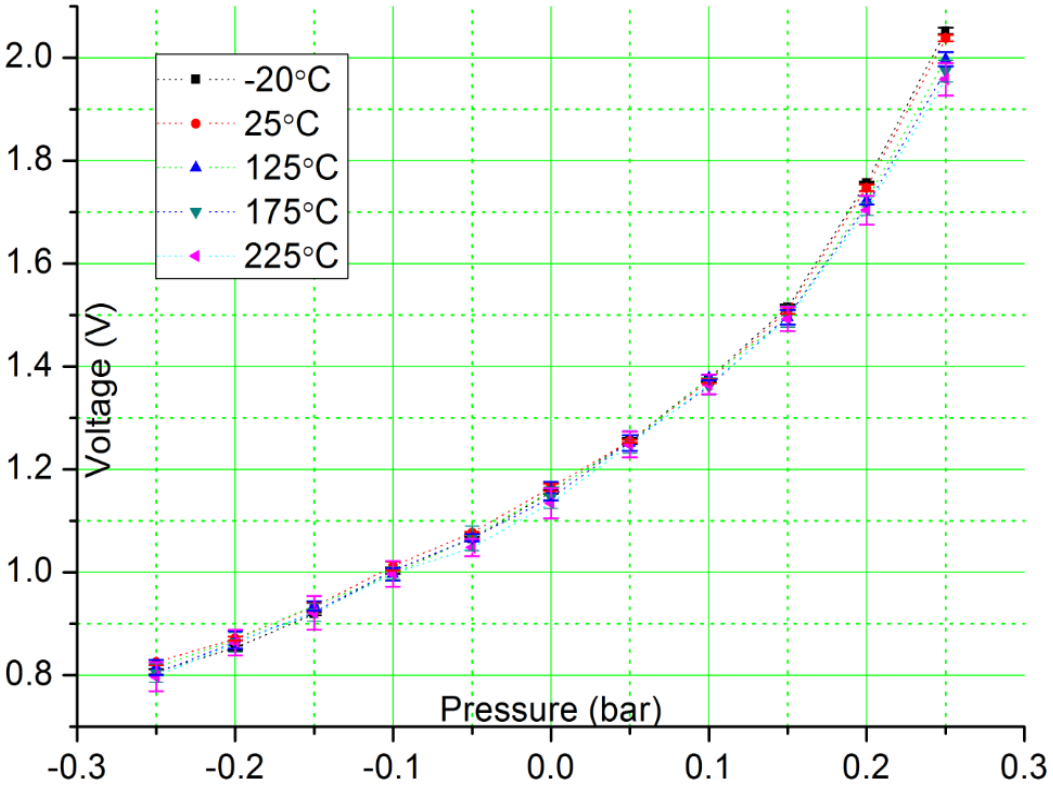


Figure 3.8 Measured output response of the capacitance to voltage readout circuit with a capacitive MEMS pressure sensor

In our experiments, the temperature for the sensor and reference capacitors is fixed at 25 °C. In real world applications, the sensor capacitor and reference capacitors will also undergo wide temperature change. The sensor capacitor and reference capacitor are often identical and they usually have the same TCs, around 100 ppm/°C. The TC of the on-chip feedback capacitor is about 13 ppm/°C according to the IBM 0.13 μm CMOS process design manual. According to Equation 3.1, some errors could be introduced due to the TC difference. The sensor capacitance,

C_{sensor} is comprised of a steady-state capacitance defined as C_0 and a capacitance change during operation defined as, ΔC. And the reference capacitance, C_{ref} is usually about the same value of C_0. Now Equation (3.1) can be written as Equation (3.2),

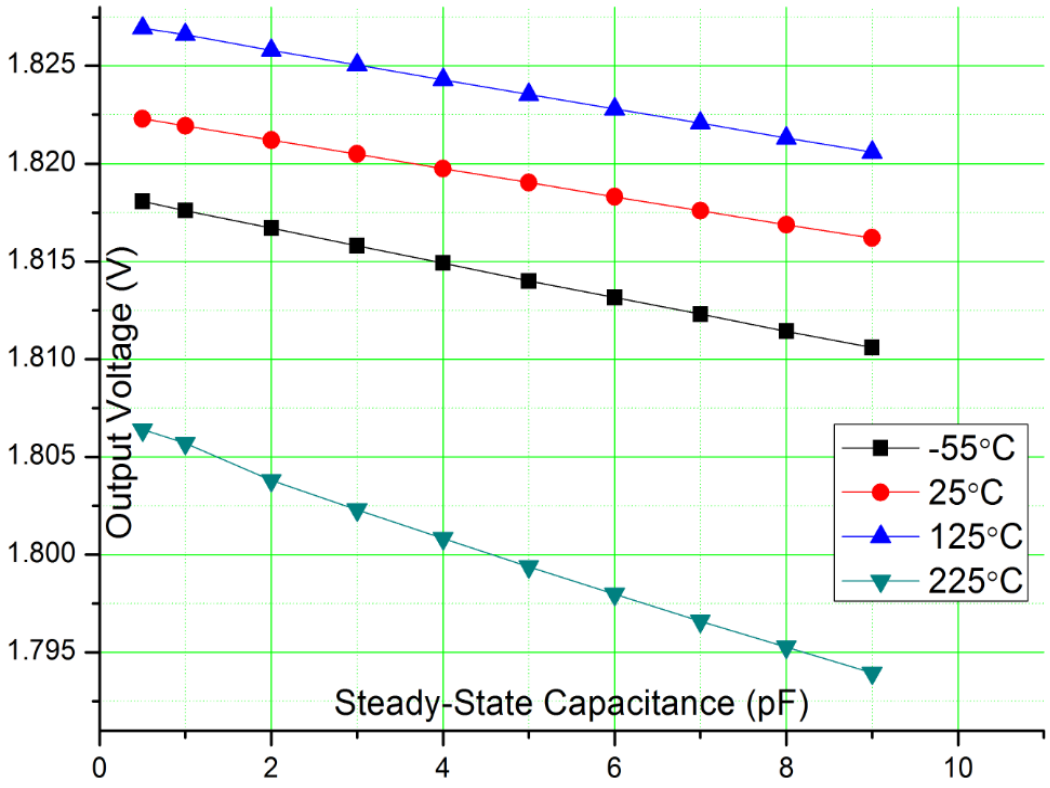


Figure 3.9 Simulated output voltage for different steady-state capacitance

$$V_{out} = V_{mid} + \Delta V_{osc} \frac{\Delta C}{C_{feedback}} \quad (3.2)$$

As can be seen, due to the differential readout scheme, the C_0 component is cancelled and only ΔC is considered. Figure 3.9 shows the simulated output voltage for different steady-state capacitance from −55 °C to 225 °C. The TCs of sensor capacitor and reference capacitor are set

to 100 ppm/°C. ΔC is set to 0.5 pF at 25 °C, V_{mid} and ΔV_{osc} are set to 1.25 V, and $C_{feedback}$ is set to 1 pF. As can be seen, when the steady-state capacitance changes from 0.5 pF to 10 pF, the output voltages decrease only about 20 mV. This shows the circuit has good flexibility to interface with MEMS sensors with a wide range of the steady-state capacitance values. At a fixed steady-state capacitance, the output voltages change by less than 30 mV when temperature varies from −55 °C to 225 °C. This means the TC difference has very limited impact to the interface circuit. For MEMS sensors which don't have a reference capacitor, low TC mica capacitor (with TC about 50 ppm/°C) can be used as reference capacitor.

3.4 SUMMARY AND CONCLUSIONS

In this chapter, a novel CMOS differential interface circuit for capacitive MEMS pressure sensors is designed, fabricated and tested. This circuit can be functional over a wide temperature range between −55 °C and 225 °C. The circuit offers the flexibility to interface with MEMS sensors with a wide range of the steady-state capacitance values from 0.5 pF to 10 pF. Simulation results show that this capacitance to voltage readout circuit has excellent linearity and stability over the wide temperature range between -55 °C to 225 °C. Experimental results show that the circuitry has excellent temperature stability and an overall linearity error of around 2% over -20 °C to 225 °C with goodness-of-fit of linear regression of 0.998 (R^2). The circuit was tested using a commercial capacitive MEMS pressure sensor and provided a stable response over the wide temperature range.

CHAPTER 4 CMOS CAPACITANCE TO FRENQUENCY READOUT CIRCUIT

In the last chapter, we presented a capacitance to voltage readout circuit, which converts the sense signal (capacitance change) to an analog voltage output. In this chapter, we describe a CMOS capacitance to frequency readout circuit for capacitive MEMS sensors, where the output is less susceptible to noises and interference introduced at the high-temperature environment. A current to frequency conversion circuit is used to convert the sensor capacitance into digital pulse signal which is modulated in frequency. The pulse width is adjustable with off-chip components. The circuit is fabricated using IBM 0.13 μm CMOS technology with 2.5 V power supply. Simulation and experimental results show that the capacitance to frequency readout circuit is functional over the wide temperature range between -55 ºC and 225 ºC. This design has high integration level, low power consumption, and provides a frequency output which is less susceptible to noise and interference.

4.1 CIRCUIT ARCHITECTURE

Several capacitance to frequency readout circuits for MEMS sensors have been developed [97-99]. All these circuits are designed for applications over commercial temperature range from -40 ºC to 80 ºC. In our work, we design a capacitance to frequency readout circuit which can operate over temperature range between -55 ºC and 225 ºC. Fig. 4.1 shows the schematic of the capacitance to frequency readout circuit, which we described in an IEEE Sensors conference

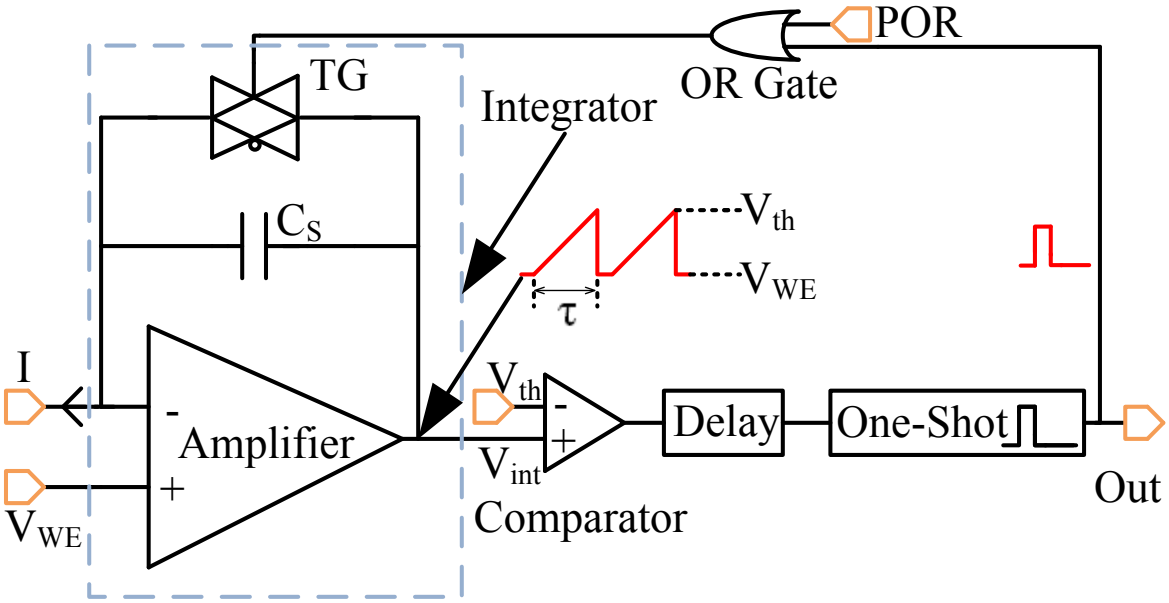


Figure 4.1 Schematic diagram of the capacitance to frequency readout circuit

proceedings [100]. During operation, the input of this circuit is C_S, which is the capacitance of a MEMS capacitive sensor to be measured and the output is a frequency modulated digital signal. A voltage V_{WE} is applied to the non-inverting node of the amplifier. An integration current, I (generated by a cascode current sink which will be described later), is applied to the inverting node of the amplifier. The current I is integrated into voltage, V_{int}, by the integrator circuit which consists of the amplifier, the sensor capacitor C_S, and a reset transmission gate (TG). The relationship between the integration current I and the voltage V_{int}, when the TG is off, can be expressed by Equation (4.1),

$$V_{\text{int}} = V_{WE} + \frac{I \cdot t}{C_S} \quad (4.1)$$

where, t is the integration time. The voltage V_{int} is then compared with the threshold voltage, V_{th}, using a comparator circuit. When V_{int} is higher than V_{th}, the comparator generates a rising edge, which is delayed by time t_d with a delay module to guarantee that a complete rising edge is generated within the feedback loop. The rising edge triggers the one-shot module to generate a pulse with fixed pulse width, t_{pw}, which resets the integrator through the reset TG and initializes the next pulse generation loop. The power-on-reset (POR) signal is used to initialize the entire circuitry when the chip is powered on. The time required for V_{int} to reach V_{th} can be expressed by Equation (4.2),

$$\tau = \frac{C_S \cdot (V_{th} - V_{WE})}{I} \quad (4.2)$$

And from the above description, the output pulse frequency can be expressed by Equation (4.3),

$$f = \frac{1}{\tau + t_d + t_{pw}} \quad (4.3)$$

The delay time, t_d and pulse width, t_{pw} are designed to be much smaller than the integration time τ ($\tau >> t_d + t_{pw}$). Using Equations (4.1), (4.2) and (4.3), the output signal frequency can be simplified as Equation (4.4),

$$f = \frac{1}{\tau + t_d + t_{pw}} = \frac{1}{\frac{C_S \cdot (V_{th} - V_{WE})}{I} + t_d + t_{pw}} \approx \frac{I}{C_S \cdot (V_{th} - V_{WE})} \quad (4.4)$$

From Equation (4.4), we can see that the output signal frequency is inversely proportional to the capacitance of the MEMS capacitive sensor.

4.2 DESIGN OF DETAILED CIRCUITS

The CMOS capacitance to frequency readout circuitry mainly consists of three sub-blocks: 1) integrator; 2) comparator; and 3) digital conversion block, which consists of a delay module, a one-shot circuit, and an OR gate.

4.2.1 INTEGRATOR DESIGN

The integrator converts the current I, flowing through the capacitance C_S, into a voltage signal V_{int} at the output node of the integrator. The single-ended folded-cascode amplifier designed in Chapter 2 is used as the amplifier in this integrator. The integration current I is generated by a cascode current sink, as shown in Figure 4.2. The biasing voltages N_{cas} and N_{bias} are provided by the constant-g_m biasing circuit shown in Figure 2.4 in Chapter 2. From Equation (4.4), the integration time τ must be much bigger than the delay time t_d and pulse width t_{pw} to make the approximation valid. To increase the integration time τ, according to Equation (4.2), the integration current I should be very small. The NMOS transistors M1 and M2 in the current source are designed to have small W/L ratio to get an integration current I of 0.5 μA at 25 ºC. The output voltage of the integrator is between V_{WE} and V_{th}, as shown in Figure 4.1.

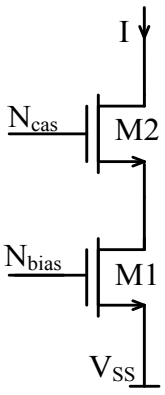


Figure 4.2 Schematic of the current sink which provides the integration current I

4.2.2 COMPARATOR DESIGN

The comparator compares the output voltage of the integrator V_{int} with a threshold voltage V_{th} and provides a rising edge signal when V_{int} is bigger than V_{th}. output. The schematic of the comparator is shown in Figure 4.3. It is implemented using a clocked regenerative comparator followed by a static latch. Two identical cascaded pre-amplifiers are placed before the regenerative comparator to amplify the voltage difference at the input to a large level to achieve high precision. The schematic of the pre-amplifier is shown in Figure 4.4. The pre-amplifiers are also biased by the constant-g_m biasing circuit so that its gain and bandwidth can be maintained over a wide temperature range. Simulation results show that the comparator has resolution better than 0.1 mV with a 10 MHz clock at 125 ºC.

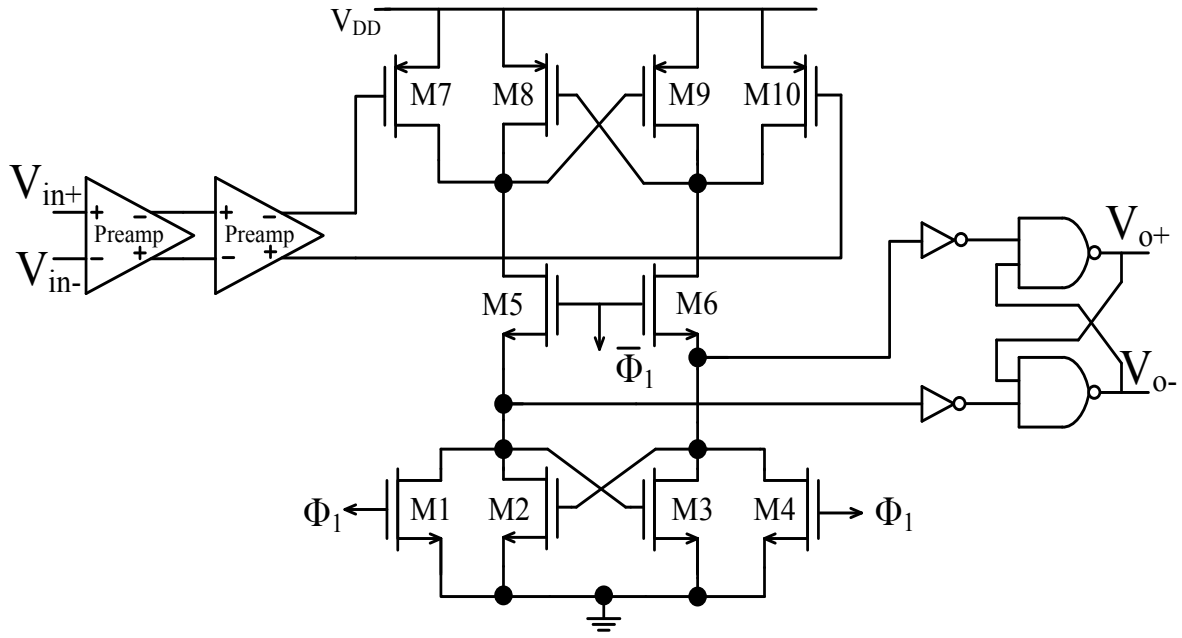


Figure 4.3 Schematic of the comparator

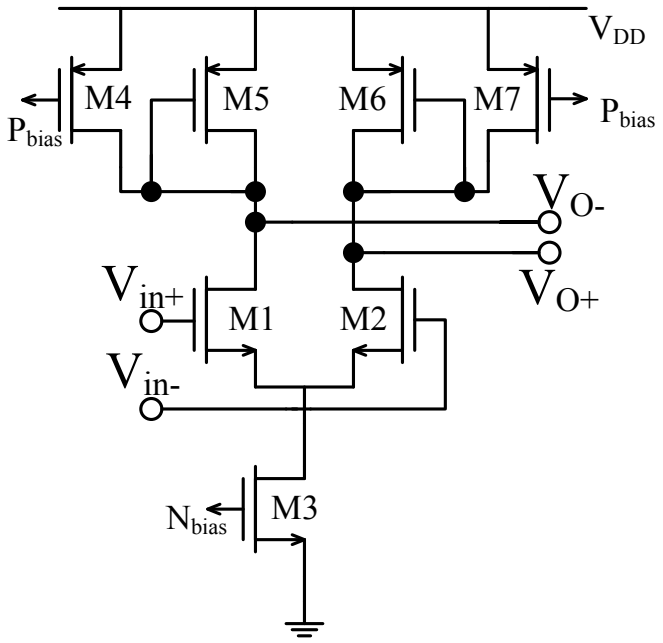


Figure 4.4 Schematic of the pre-amplifier in the comparator

4.2.3 DIGITAL CONVERSION CIRCUIT

The digital conversion circuit generates a digital pulse with fixed pulse width when it is triggered by the rising edge from the comparator. It also resets the integrator through the transmission gate and initializes the next pulse generation loop. The core part of the digital conversion circuit is the one-shot circuit which is shown in Figure 4.5 [101]. The rising edge generated by the comparator triggers the D flip-flop, passing the voltage VDD at node D to the output node Q, and charging the capacitor C_{OS} through the resistor R_{OS}. Theoretically, once the input node of the inverter is charged beyond half of VDD, the reset signal RST is enabled and the output voltage at node Q becomes 0. In this case, a complete pulse signal is generated with a fixed pulse width t_{pw}, which is determined by the time constant of $R_{OS} \times C_{OS}$. The capacitor C_{OS} and the resistor R_{OS} are implemented off-chip to make the pulse width t_{pw} adjustable.

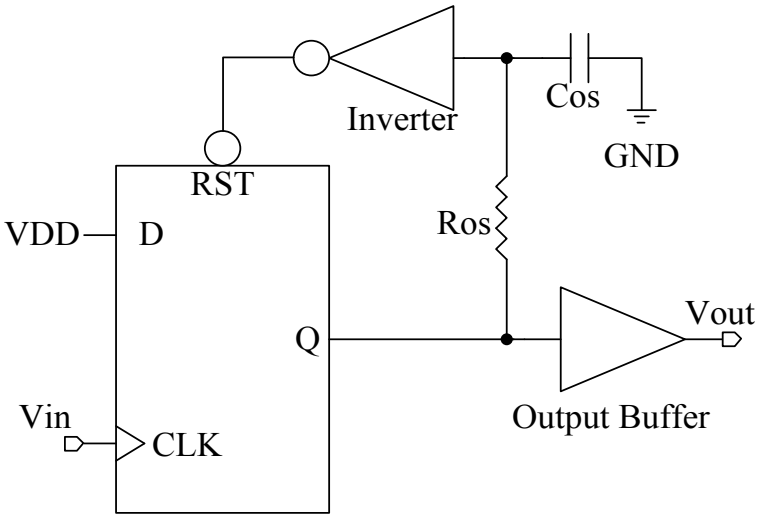


Figure 4.6 Schematic of the one-shot circuit

A delay module is placed between the comparator and the one-shot module to delay the output signal of the comparator by delay time t_d to make sure that a complete rising edge is generated for the D flip-flop [101]. The schematic of the delay module is shown in Figure 4.6. An externally applied voltage V_b is used to adjust the delay time t_d.

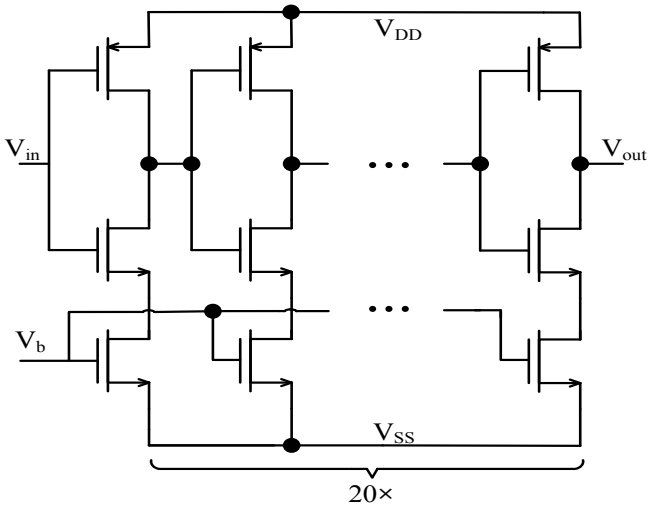


Figure 4.5 Schematic of the delay module

The digital conversion circuit is implemented without special considerations for high temperature operation, as standard CMOS digital circuits have been proven operational at temperature around 300 ºC [102]. For the resetting transmission gate, minimum size NMOS transistor is used in the transmission gates. PMOS transistor is sized such that $(W/L)_p = (\mu_n/\mu_p)*(W/L)_n$ to make the on-resistance of the switch relatively stable over wide voltage range.

4.2.4 Layout of The Capacitance to Frequency Readout Circuit

Figure 4.7 shows the layout of the capacitance to frequency readout circuit. The OR gate is integrated with the one-shot circuit. For the layout, common-centroid structures are used wherever applicable to reduce temperature induced common mode errors. Guard rings are placed around performance sensitive blocks to prevent latch-up at high temperatures. The effective area of the layout is 150 μm×185 μm.

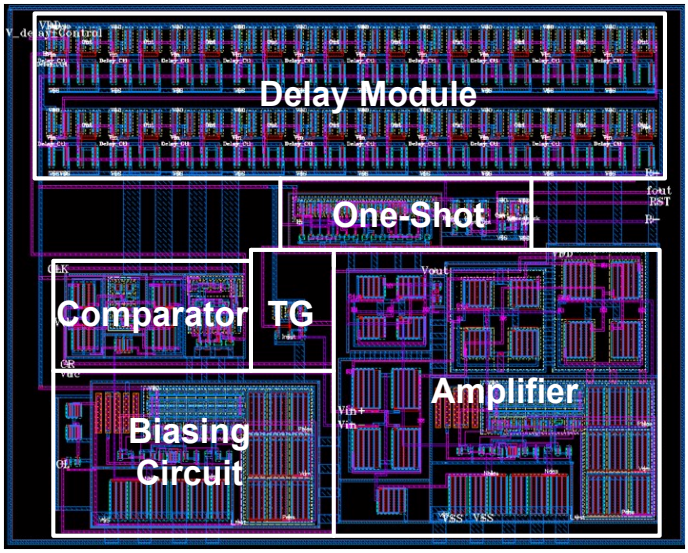


Figure 4.7 Layout of the capacitance to frequency readout circuit

4.3 EXPERIMENTAL RESULTS AND DISCUSSION

The capacitance to frequency converter is fabricated using the IBM 0.13 μm CMOS process and packaged in 40-pin DIP. It is tested at the temperature range from -20 °C to 225 °C with temperature accuracy better than ±1 °C.

Fig. 4.8 shows typical waveforms at the output nodes of the capacitance to frequency readout circuit and the integrator at 225 °C. The DC voltage V_{WE} is set to 1.2 V and V_{th} is set to 1.6 V. In the one-shot circuit, Ros=100 kΩ and Cos=1 pF are used to get a theoretical pulse width, t_{pw}=0.1 μs. The actual t_{pw} is slightly larger due to parasitic capacitances. As can be seen, the output signal of the capacitance to frequency readout circuit is pulse signal with fixed pulse width. And as expected, the output signal of the integrator is serrated signal with the lowest voltage equal to V_{WE} and the highest voltage equal to V_{th}.

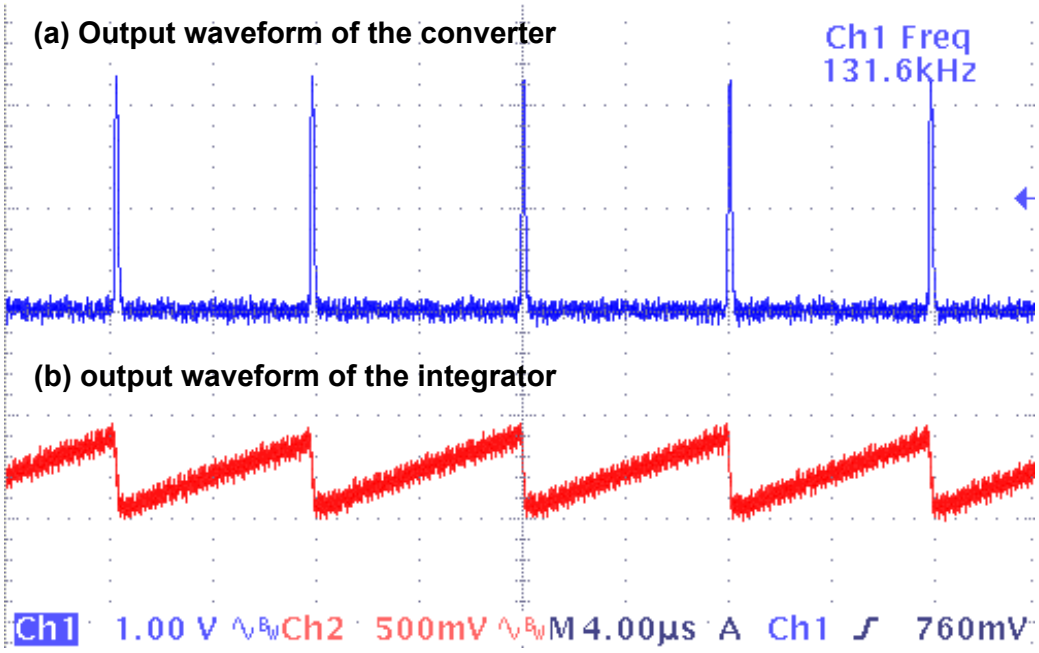


Figure 4.8 (a) Output waveform of the converter, and (b) output waveform of the integrator

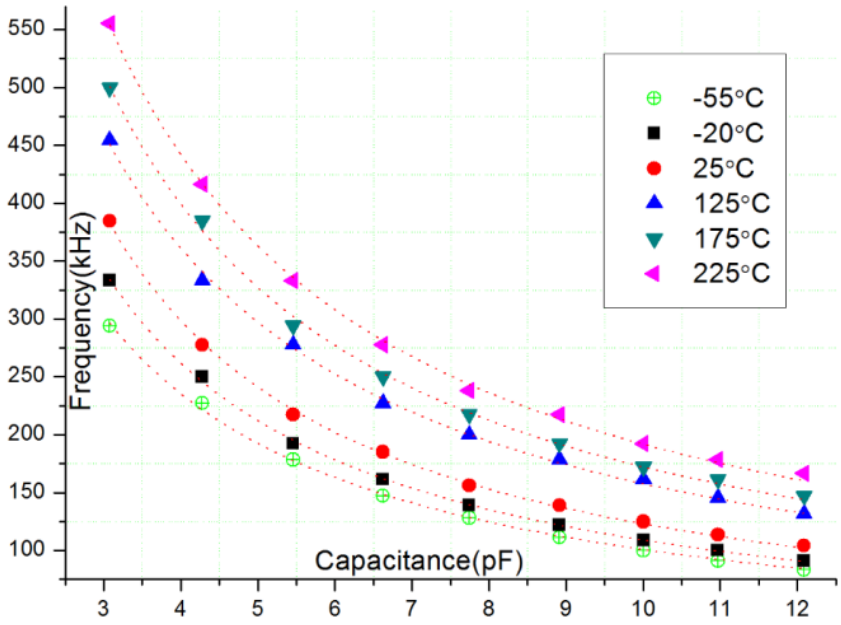


Figure 4.9 Simulated output frequency of the frequency readout circuit

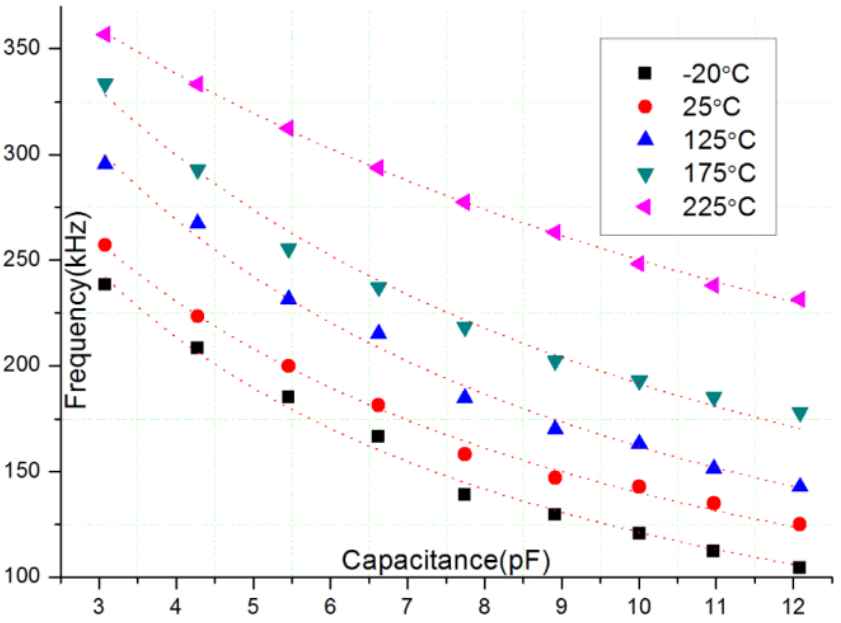


Figure 4.10 Measured output frequency of the frequency readout circuit

Figure 4.9 shows the simulated output frequency of the capacitance to frequency readout circuit at temperature range from -55 °C to 225 °C. Figure 4.10 shows the measured output frequency of the circuit at temperature range from -20 °C to 225 °C. The measured data are averaged from three consecutive measurements. In both cases, V_{WE} is set to 1.2 V, V_{th} is set to 1.6 V, and V_b in the delay module is set to 1.5 V. The designed integration current, I, is 0.5 μA at 25 ºC. The sensor capacitor C_s is constructed using 9 capacitors with nominal value of 1 pF connected in parallel, as shown in Figure 4.11. Its capacitance can be varied from 3.076 pF to 12.087 pF (the actual value is measured using the high resolution universal capacitance readout circuit MS3110) by removing/placing jumpers. During experiments, the sensor capacitor is maintained at 25 ºC.

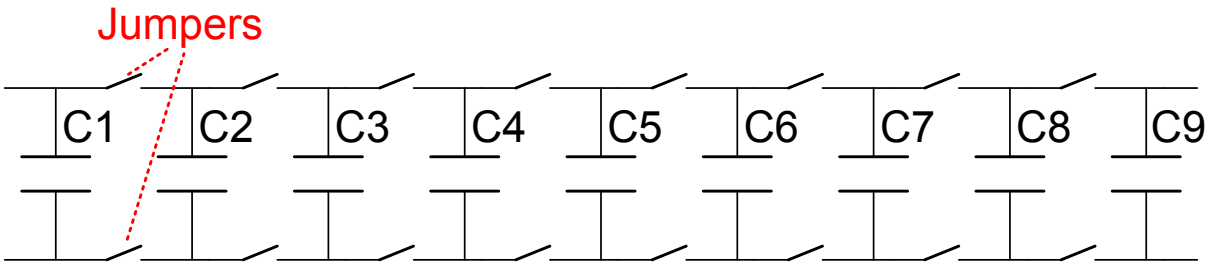


Figure 4.11 Construction of the sensor capacitor C_s

In Figure 4.9 and 4.10, red dotted lines stand for reciprocal fittings using function $f(x)=1/(a+bx)$, where a is the sum of t_d and t_{pw} , and b is $(V_{th}-V_{WE})/I$ in Equation (4.4). As can be seen, both the simulated and the measured output frequencies show good reciprocal characteristics. The measured results match well with the simulation results, and the converter shows good accuracy from -20 ºC to 225 ºC.

The overall measured frequencies are larger than the simulated frequencies, because the delay time t_d and pulse width t_{pw}, and the actual sensor capacitance C_s are all larger than the simulated

values due to interconnect parasitic capacitances. The discrepancy between the measured and simulated frequencies is larger when the sensor capacitance C_s is smaller. Recall Equation (4.2), the integration time τ is proportional to the sensor capacitance C_s. When C_s is small, the assumption $\tau >> t_d + t_{pw}$ is no longer valid, leading to measurement errors. To solve this problem, according to Equation (4.2), the integration current should be made smaller to increase the integration time τ and make t_d and t_{pw} negligible.

Both the simulated and measured output frequency curves shift upwards as temperature increases. Recall Equation (4.4), the output frequency is proportional to the integration current I. Because the current I is generated using biasing voltages provided by the constant-g_m biasing circuit, it is actually proportional to the biasing current I_b the biasing circuit, which increases as temperature increases, as shown in Chapter 2. To make the frequency shift with temperature smaller and thus improve the performance of the capacitance to frequency circuit, an integration current with less temperature dependence is needed. Figure 4.12 shows a circuit which can generate an integration current with small temperature dependence. An amplifier is used to force the voltage at the source of the NMOS transistor to be equal to a fixed reference voltage V_{REF}. So the drain current of the transistor can be expressed by Equation (4.5),

$$I = \frac{V_{REF}}{R_1} \quad (4.5)$$

When the resistor R_1 is implemented using a poly resistor with TC around 100 ppm/ºC (the same type of the resistor is used as the biasing resistor in the constant-g_m biasing circuit shown in Chapter 2), the integration current will be almost constant over wide temperature range.

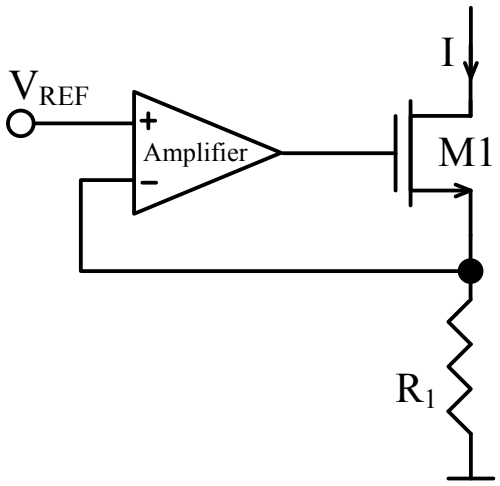


Figure 4.12 Schematic of the constant circuit sink

4.4 SUMMARY AND CONCLUSIONS

In this chapter, a CMOS capacitance to frequency readout circuit for capacitive MEMS sensors is presented. A current to frequency conversion method is used to convert the sensor capacitance into digital pulse signal which is modulated in frequency. This circuit is simulated at temperatures ranging from −55 °C to 225 °C and tested at temperature from -20 °C to 225 °C. In both cases, it shows considerable accuracy and stability over the wide temperature range. The causes which lead to the difference between the simulated and measured results are explained, and possible solutions to improve the circuit accuracy with temperature variation are proposed. The advantages of this circuit include high integration level, low power consumption, and achievement of a frequency output signal which is less susceptible to noise and interference. However, frequency output signal is only a quasi-digital signal. A real digital signal is more desirable for easy of signal processing and transmission. In the next chapter, we will present a capacitive sensor interface circuit which can convert sensor capacitance to a digital output signal.

CHAPTER 5 CMOS CAPACITANCE TO DIGITAL READOUT CIRCUIT

In this chapter, we present a CMOS capacitance to digital readout circuit for capacitive MEMS sensors which is functionally tested over a wide temperature range from -20 ºC to 225 ºC. The proposed circuit uses a sigma-delta technique to convert the input ratio between sensor capacitance and reference capacitance into a high-accuracy digital output. Constant-g_m biasing technique and other design considerations are used to alleviate performance degradation at high temperatures. The circuit is implemented using the IBM 0.13 μm CMOS process technology which incorporates a 2.5 V power supply. The simulation results show that the circuit offers 0.03% accuracy between -55 ºC to 225 ºC. The circuit is tested with a commercial MEMS capacitive pressure sensor. Experimental results show that the circuit offers good temperature stability, resolution of 1.44 fF, and accuracy of 2.4% between -20 ºC to 225 ºC.

5.1 CIRCUIT ARCHITECTURE

Figure 5.1 shows the schematic implementation of a basic CMOS capacitance to digital readout circuit previously implemented by other research groups [103, 104]. This circuit uses a simple oversampled architecture where negative feedback is used to control the input branch to keep the integrator output, V_o, oscillating around analog ground, V_{AG}. Its working principle is similar to a conventional sigma-delta analog-to-digital converter (ADC), except that it has no internal digital-to-analog converter (DAC) and separate input and reference voltages [103].

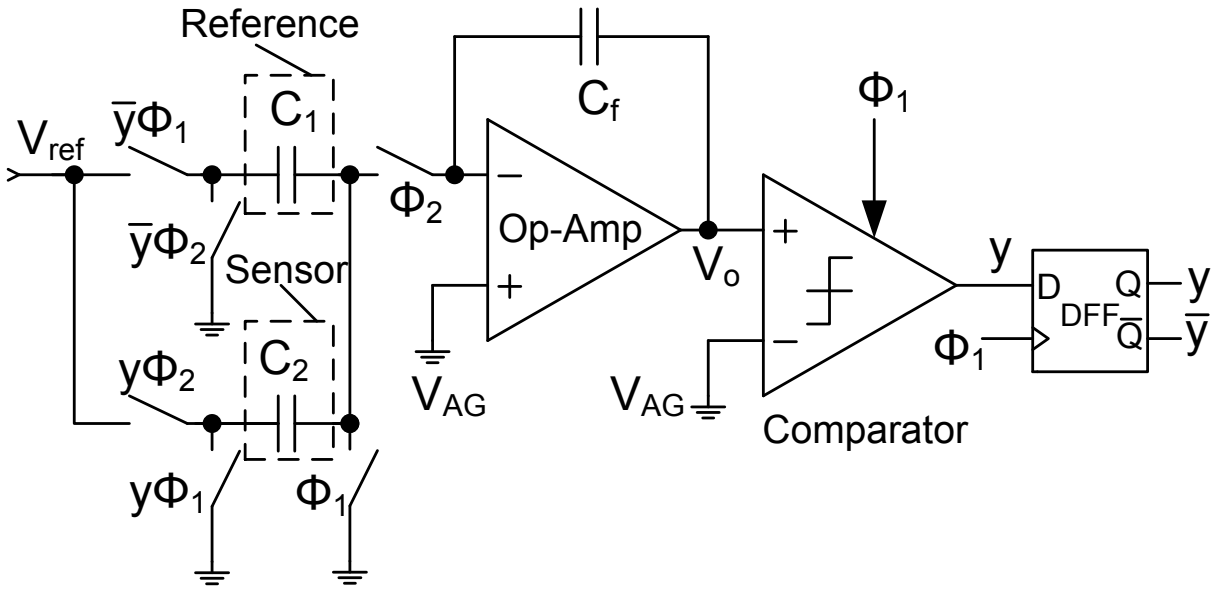


Figure 5.1 Schematic of a basic capacitance to digital readout circuit

In operation, assuming output y is "1", when Φ_1 is high, C_1 is disconnected from the input reference voltage, V_{ref}, and C_2 is discharged. The integrator output, V_o, remains unchanged since no charge is transferred to the integrating capacitor, C_f. At the next clock phase, Φ_2 becomes high, a positive charge of C_2V_{ref} is delivered into C_f via C_2, causing V_o to decrease by C_2V_{ref}/C_f. This operation continues until V_o is smaller than V_{AG} and now y becomes "0". Then, during the time when Φ_1 is high, C_1 is charged to V_{ref}. Next, when Φ_2 is high, a negative charge of $-C_1V_{ref}$ is delivered into C_f via C_1, causing V_o to increase by C_1V_{ref}/C_f. This operation continues until V_o is bigger than V_{AG} and now y becomes "1" again. The negative feedback forces the voltage V_o to vary around V_{AG}, and the average charge on C_f delivered from C_1 and C_2 should be 0. So, the following Equation (5.1) can be obtained [105],

$$nC_2V_{ref} - (N-n)C_1V_{ref} \approx 0 \quad (5.1)$$

where, N is the total clock cycles and n is the number of clock cycles when y is "1". If y_{ave} is defined as n/N, the average of the output binary data, y(n), then the ratio of $(C_2-C_1)/(C_1+C_2)$ can be estimated as Equation (5.2) [103, 104],

$$\frac{C_2-C_1}{C_1+C_2}=1-2y_{ave} \quad (5.2)$$

The above circuit structure shown in Figure 5.1 can be used in applications where C_1 and C_2 may be both constant capacitors (e.g., in the case of matching on-chip CMOS capacitors for ADC and DAC applications), or they may be time-varying capacitances and C_1+C_2 is relatively constant (e.g., in the applications of capacitive accelerometers or pressure sensors) [104]. In a typical capacitive MEMS sensor readout scenario, C_1 is the reference capacitor while C_2 is the sensor capacitor to be measured.

The circuit described in Figure 5.1 is susceptible to various non-ideal effects, including finite operational amplifier gain, operational amplifier offset, thermal noise, 1/f noise, clock-feedthrough noise, charge injection, and bulk junction leakage currents. Wang et al. [104] proposed an improved capacitance to digital readout circuit as shown in Figure 5.2 that can significantly reduce sensitivity to the abovementioned non-ideal effects. The novelty of our work deals with extending the performance of the improved capacitance to digital readout circuit shown in Figure 5.2 to operate over the wide temperature range from -55 ºC to 225 ºC and integrating the capacitance to digital readout circuit with a capacitive MEMS pressure sensor.

The performance of the integrator in Figure 5.1 is critical since it is used to realize the noise-shaping transfer function. Ideally, the operational amplifier of the integrator should have infinite gain and zero offset voltage. Finite operational amplifier and nonzero offset voltage can cause

errors in the transfer function of the first stage integrator and increase quantization noise at low frequencies. The thermal noise can be effectively attenuated using large input capacitors. The 1/f noise and clock-feedthrough noise are prevailing at low frequencies. Since the signal of capacitive sensors is usually located at low frequencies, these low frequency noises must be reduced to achieve accurate measurement.

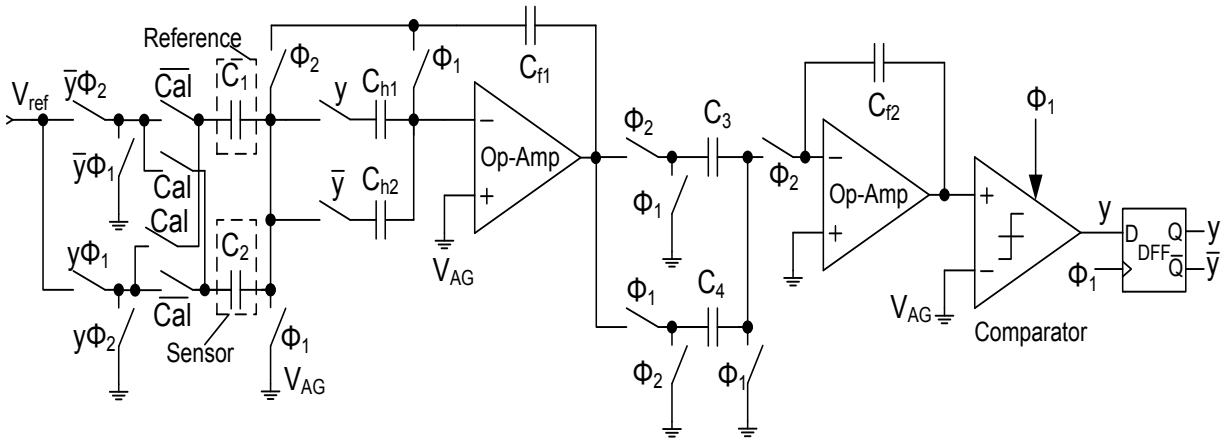


Figure 5.2 Schematic of the improved capacitance to digital readout circuit

Correlated double sampling (CDS) technique is used to cancel low frequency noises. It can also increase the effective operational amplifier gain and decrease its input offset voltage. As shown in Figure 5.2, two holding capacitors C_{h1} and C_{h2} are used to store and subtract the virtual-ground voltage (caused by low frequency noises, and finite gain and offset of the operational amplifier) during the y=0 and y=1 clock phases, respectively [104]. Using CDS technique, the effective value of the operational amplifier offset becomes V_{os}/A, and the effective operational amplifier gain becomes nearly A^2 (V_{os} is the Op-Amp offset and A is the operational amplifier open loop gain) [106, 107]. The values of C_{h1} and C_{h2} do not significantly influence the accuracy of the operation, as they are only used to store and cancel the offset voltages.

In Figure 5.1, the first order modulator requires a very high sampling ratio to get high resolution. However, a higher order structure can be used to achieve the same resolution with a smaller oversampling ratio. Here, a second order structure is chosen because its structure is simpler and more stable, as compared with even higher order structures. In Figure 5.2, a second order sigma-delta modulator is formed by adding a second integrating stage. The second order modulation is guaranteed by making $C_3=2C_4$ [105]. The other capacitors are carefully chosen so that they make the modulator stable and the operational amplifiers of the integrators are working in their linear range.

To further reduce noises introduced by clock-feedthrough, charge injection, and junction leakage current of the switches, a calibration method is used in the circuit shown in Figure 5.2. The measurement is divided into two phases. First, signal Cal is set to "0", the circuit is in normal operation phase and y_{ave} is measured. Then, signal Cal is set to"1", the circuit works in calibration phase and the positions of C_1 and C_2 are exchanged. The average of output data under this condition is defined as y'_{ave}. Both y_{ave} and y'_{ave} contain errors due to clock-feedthrough, charge injection, and junction leakage current of the switches. By subtracting y_{ave} from y'_{ave}, the errors are cancelled [104, 105]. Finally, the ratio of $(C_2-C_1)/(C_1+C_2)$ can be readily deduced from Equation (5.2) as given below by Equation (5.3),

$$\frac{C_2-C_1}{C_1+C_2} = y'_{ave} - y_{ave} \qquad (5.3)$$

5.2 DETAILED DESIGN OF CIRCUITS

The CMOS capacitance to digital readout circuit contains several analog blocks including two amplifiers, a comparator, and some transmission gates. It also contains several digital blocks including a D flip-flop, a non-overlapping two-phase clock generator, some 2-input NAND gates and inverters to generate the control signals. Since a CDS technique is used, the gain and offset voltage requirement for amplifiers in Figure 5.2 are relaxed. The single-ended folded-cascode amplifier designed in Chapter 2 is used as the amplifiers in Figure 5.2. The clocked comparator shown in Figure 4.3 in Chapter 4 is used as the comparator here. The noise and offset voltage of the comparator will increase at high temperature. Since the comparator is located after the second integrator, its noise and offset are shaped the same way as the quantization noise and attenuated by the large DC gain of the first and second integrators. So, the circuit performance is generally insensitive to noise and offset of the comparator. Both the amplifiers and the comparator are biased using the constant-g_m biasing circuit shown in Figure 2.4 in Chapter 2. The transmission gates are built using parallel NMOS and PMOS transistors. At high temperatures, the junction leakage current of NMOS transistor is much larger than that of PMOS transistor, causing a net temperature-dependent leakage current to drain charge from the sample/hold node [49]. Minimum size NMOS transistors are used in transmission gates to reduce the junction leakage current. PMOS transistors are sized such that $(W/L)_p=(\mu_n/\mu_p)(W/L)_n$ to improve the linearity of the switch turn-on resistance. The digital blocks are implemented without special design considerations as standard CMOS digital circuits have been demonstrated to be operational at temperature around 300 ºC [102].

5.3 SIMULATION RESULTS

The circuit level simulation is done in Cadence using all of the circuit blocks discussed in Section 5.2. For a typical MEMS capacitive sensor, its steady-state capacitance is on the order of few picofarads, and the capacitance change during operation is from several tens to few hundred femtofarads. In the simulation, the sensor reference capacitance C_1 is set to 5 pF, and the sensor capacitance C_2 is set to 5.2 pF, as a reasonable representation for a MEMS capacitive pressure sensor. The following other parameters are used in the simulation: $C_{f1} = 4C_1$, $C_{h1}=C_{h2}=C_3=C_{f2}=2$ pF, $C_4=1$ pF, $V_{ref}=0.2$ V, and clock frequency is 1 MHz. At every clock cycle a data point of y is generated, so the number of data means the number of clock cycles needed to make the estimation. For example, the number of data is 500 means 500 data points are acquired. The acquired data points are passed through a Hanning window with the same length of the data to obtain the y_{ave} value. The Hanning window used here acts as a digital lowpass filter. The estimation error is defined as $|(C_2'-C_2)|/C_2$, where C_2' is the estimated value of C_2 using Equation (5.2) and Equation (5.3) for the circuit architecture shown in Figure 5.2 with and without calibration, respectively.

Figure 5.3 shows the estimation error for different number of data points at different temperatures. The dashed lines show errors without calibration and solid lines show errors with calibration. As can be seen, the estimation errors without calibration become stable after 500 data, while the estimation errors with calibration settle after 2000 data. From -55 °C to 125 °C, the errors before calibration are almost the same (around -60 dB). After calibration, the errors are reduced to below -90 dB. At 225 °C, the error without calibration increased to -28 dB, showing that the high temperature induced detrimental effects are significant. However, after calibration, the error is reduced to -71 dB, a -43 dB improvement. For the full wide temperature range from

-55 °C to 225 °C, the circuit has better than 0.03% accuracy. These results show that the calibration scheme can effectively suppress the no-ideal effects and improve the accuracy of the circuit architecture in Figure 5.2.

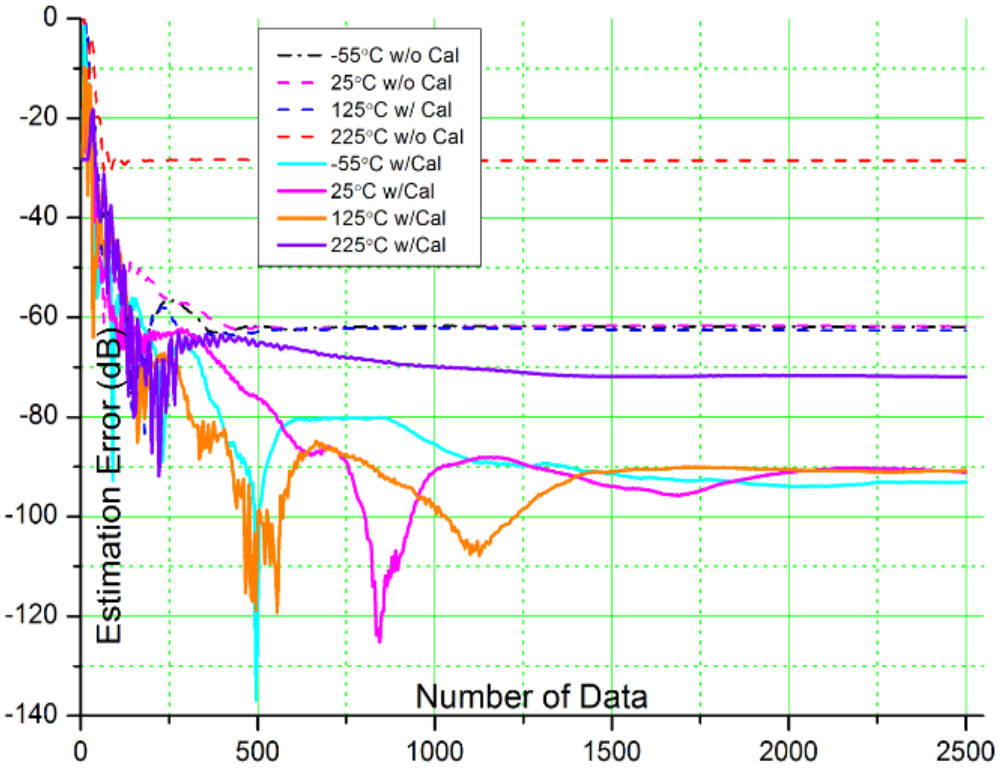


Figure 5.3 Estimation error of the capacitance to digital readout circuit for different number of data points at various temperatures

To calculate the estimation error for different C_2 capacitance value, C_2 is varied from 4.75 pF to 5.25 pF and all other parameters remain unchanged. Figure 5.4 shows the estimation error with calibration for different C_2 values at temperatures from -55 °C to 225 °C. We used 2500 data points in all the simulations. At all temperatures, the estimation errors become smaller when the sensor capacitance C_2 is close to the reference capacitance C_1 (5 pF). For same C_2 value,

from -55 °C to 125 °C, there is no significant difference between the estimation errors. However, the estimation errors at 225 °C are about 20 dB higher due to high temperature induced errors.

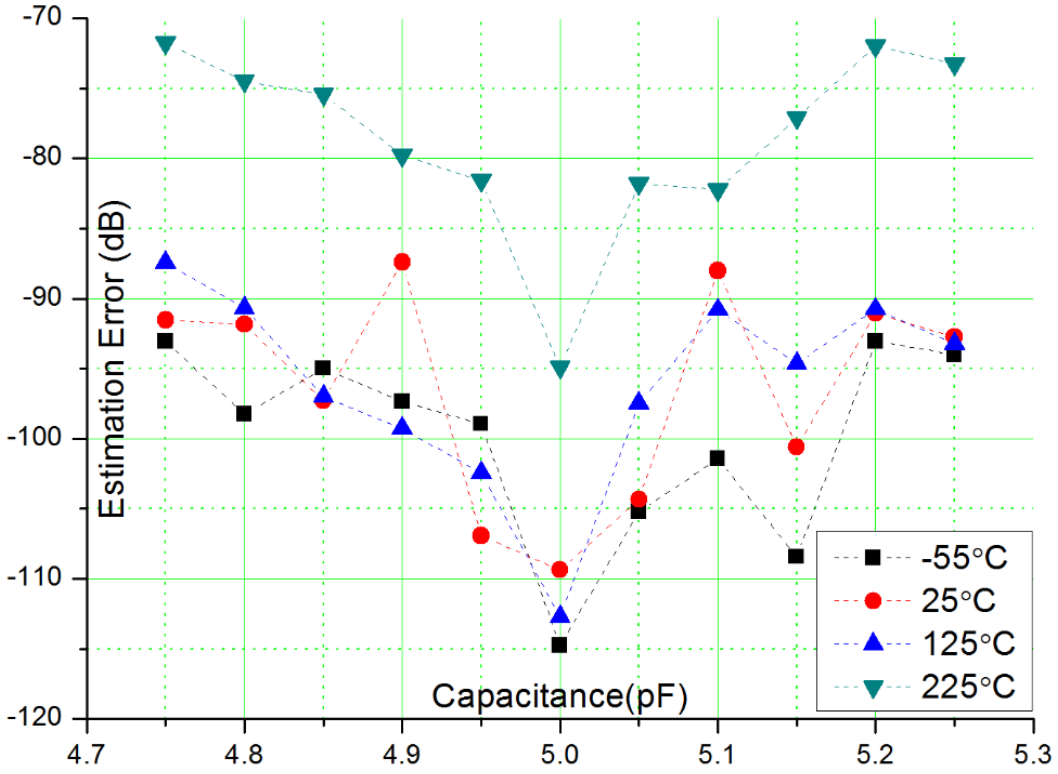


Figure 5.4 Estimation error versus C_2 values

5.4 Experimental Results and Discussion

The improved CMOS capacitance to digital readout circuit in Figure 5.2 is implemented using the IBM 0.13 µm CMOS process available through the Canadian Microelectronics Corporation (CMC). Figure 5.5 shows the layout of the circuit. The effective area of the circuit layout is 263 µm×354 µm. The fabricated chip is mounted on a PCB board made of Rogers 4350B, a material with glass transition temperature of 280 °C. The temperature of the chip is changed from -20 °C to 225 °C by the thermal inducing system mentioned in Chapter 2. Other testing instruments

include a function generator, a DC power supply, a network analyzer (Agilent E5061B-3L5, Agilent Technologies Inc., Santa Clara, California), a data acquisition card (NI USB-6259, National Instruments Inc., Austin, Texas), and a laptop running LabVIEW program to interface with the data acquisition card.

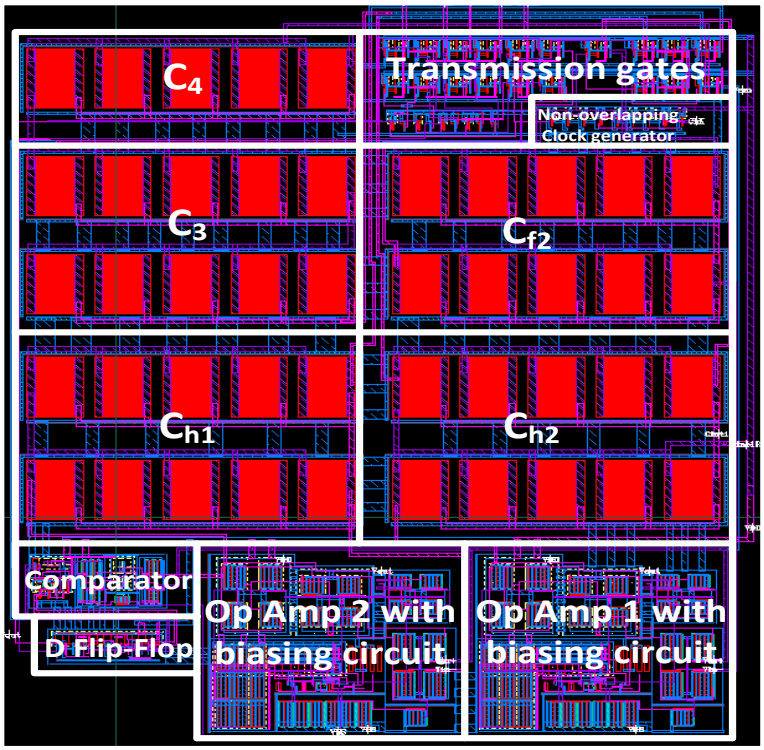


Figure 5.5 Layout of the capacitance to digital readout circuit

Two off-chip capacitors with nominal capacitance of 5 pF are used to test the CMOS capacitance to digital readout circuit. Their actual capacitances are measured with a high resolution universal capacitance readout circuit, MS3110 (MicroSensors, Costa Mesa, California) at room temperature of 25 ^{o}C. The reference capacitor C_1 is around 5.018 pF, and the sensor capacitor C_2 is around 4.945 pF. The first integrating capacitor C_{f1} is also implemented off-chip

with a capacitor with nominal capacitance of 20 pF. C_1, C_2 and C_{f1} are low temperature coefficient mica capacitors and they are placed at room temperature (25 ^oC), only the test chip is exposed to the temperature change from -20 ^oC to 225 ^oC. A 500 kHz clock is used, and at every clock cycle a data point is generated. The output data y are acquired with the data acquisition card and processed using Matlab software. The data are passed through a Hanning window before they are averaged. Equations 5.2 and 5.3 are used to calculate C_2 value, while assuming C_1 is 5.018 pF.

In the simulations, the real values of C_1 and C_2 are known and the readout accuracy can be readily obtained by comparing simulated C_2 value with its real value. However, the real values of C_1 and C_2 are difficult to obtain due to the influence of interconnect parasitic capacitances. Alternatively, the accuracy of the circuit is characterized using a term called "repeatability". Repeatability is defined as the standard deviation σ of a number of repeated measurements in a short time interval with the same measurement method and conditions. The equivalent resolution of the measurements can be defined as 3σ, with a confidence level better than 99% [105].

Figure 5.6 shows the measured standard deviation of C_2 at temperatures from -20°C to 225°C with different numbers of data averaged. A set of 40 measurements is performed for every temperature, with a measurement interval of about 60 seconds. As can be seen, the standard deviation of C_2 decreases when the number of data averaged increases. And it increases when temperature increases. This effect is especially apparent when temperature is beyond 125 °C. When 10000 data are averaged, the standard deviation σ is 0.31 fF at 25 °C and 0.48 fF at 225 °C. The equivalent resolution (3σ) is 0.93 fF and 1.44 fF, respectively.

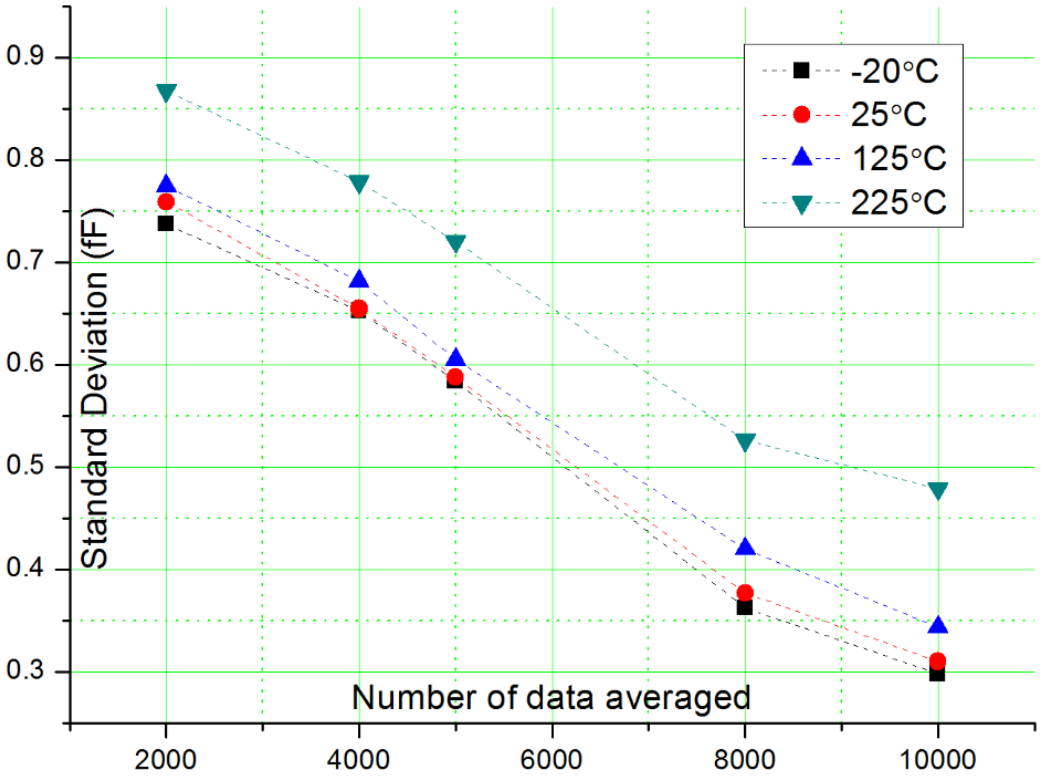


Figure 5.6 Standard deviation of C_2 versus temperatures

Figure 5.7 shows the measurement errors of C_2 at different temperatures, with and without calibration. The C_2 values are averaged from 40 measurements. In every measurement, 1000 data points are used to calculate the average value of y. The calculated C_2 value at -20 °C with calibration is used as reference, and the error is defined as (calculated C_2 value-reference value)/ (reference value). It can be seen that the measurement errors increase with temperature. Without calibration, the errors increase from 1.3% at -20 °C to 9.9% at 225 °C due to high temperature effects. With calibration, the error is effectively reduced to 2.4% at 225 °C. However, the improvement with calibration is worse as compared with the simulation results. This will be discussed later. Table 5.1 summarizes the overview of the capacitance to digital readout circuit.

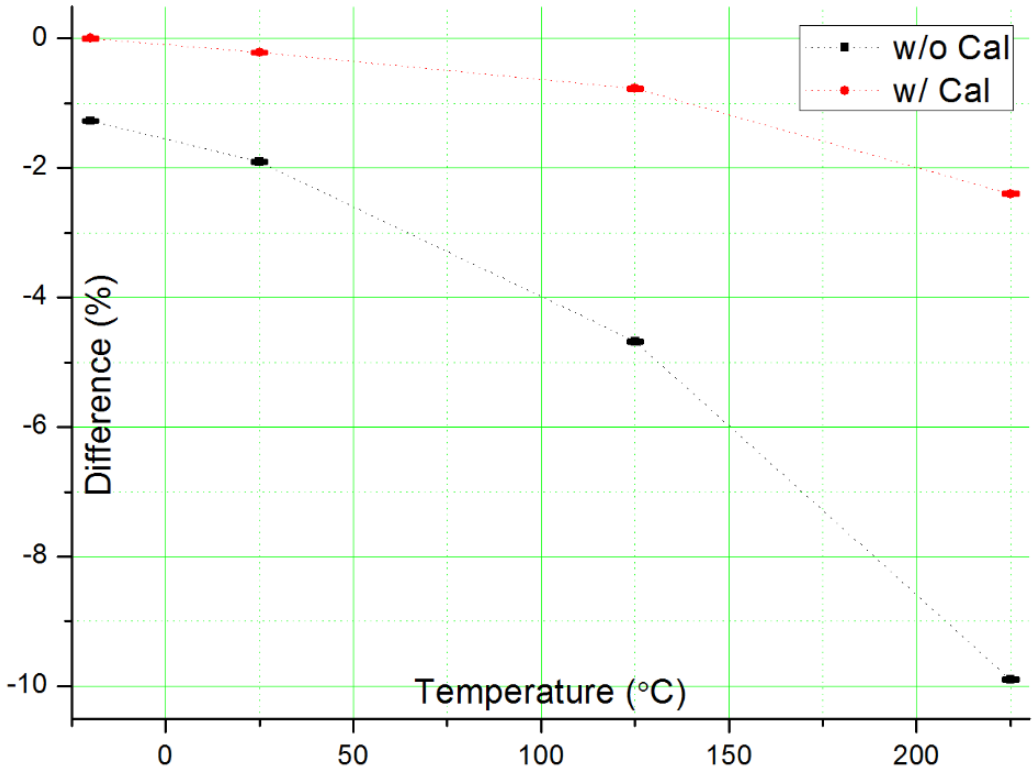


Figure 5.7 Measurement errors versus temperatures

Table 5.1 Overview of the capacitance to digital readout circuit

Parameter	Simulation	Measurement
Power Supply	2.5V	2.5V
Value of $C_1$and C_2	C_1=5pF C_2=5.2pF (accurate value)	C_1=5.018pF C_2=4.945pF (nominal value)
Clock Frequency	1MHz	500kHz
Error@125°C	-90.7dB Defined as $\|(C_2'-C_2)\|/C_2$	0.34fF Defined as standard deviation
Power Consumption	1.89mW	2.06mW

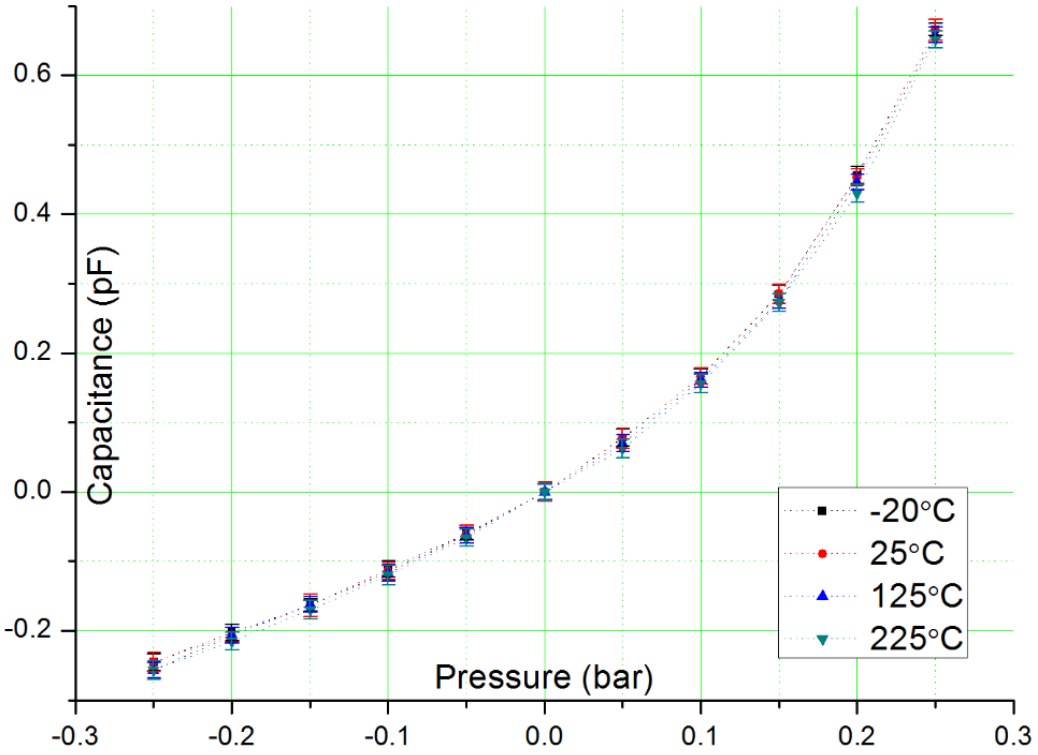


Figure 5.8 Measured response of the capacitance to digital readout circuit with a MEMS capacitive pressure sensor

A capacitive MEMS pressure sensor from Protron Mikrotechnik GmbH, Germany [108] is tested with the CMOS capacitance to digital readout circuit. It is connected as C_2 in Figure 5.2. Another capacitor with 9.87 pF capacitance is used as reference capacitor C_1. During the testing, the pressure sensor is placed in a pressure vessel where the pressure is varied from -0.25 bar to +0.25 bar. C_1 and the pressure sensor are maintained at room temperature (25 °C) so their capacitances don't change with temperature. Figure 5.8 shows the measured capacitance change with calibration versus the pressure change when the CMOS capacitance to digital readout circuit undergoes temperature changes from -20 ºC to 225 ºC. The data shown in Figure 5.8 are averaged from 10 measurements. As can be seen, the measured capacitance changes are in

accordance with the pressure changes and the response is stable over a temperature range from -20 ºC to 225 ºC. The measured capacitance change is slightly lower when the temperature increases. The overall difference between the data at -20 ºC and 225 ºC is about 4%. The estimated sensor readout resolution is 1.82 fF/mbar over the pressure range from -0.25 bar to +0.25 bar.

While the simulations are done at temperature range from -55 ºC and 225 ºC, the measurements are done at temperature range from -20 ºC and 225 ºC, which is the maximum temperature range that the thermal inducing system can achieve. Generally speaking, colder temperatures between -55 ºC and -20 ºC do not have detrimental effects on CMOS electronics and can further improve signal to noise ratio due to reduced noise effects. The measurement errors with calibration in Figure 5.7 are worse as compared with the simulation results in Figure 5.3. One possible cause is the noise coupled from the substrate and power supply, which is not considered in the simulations. Another cause could be the interconnect parasitic capacitances and noise coupled from the testing instruments. The single-ended circuit structure has poor noise rejection and is susceptible to clock-feedthrough, charge injection, and high temperature induced noise and errors. Calibration can minimize clock-feedthrough and charge injection, but it cannot effectively cancel the junction leakage currents which dominate at high temperatures. The errors due to high temperature effects can often be localized by design to common mode effects and can be differentially rejected. In the future, a fully differential architecture [105] could be used to improve the circuit performance. The fully differential architecture is relatively insensitive to noise and errors induced at high temperature. It can also more effectively suppress clock-feedthrough, charge injection, and noise coupled from the substrate and power supply.

5.5 SUMMARY AND CONCLUSIONS

A CMOS capacitance to digital readout circuit for capacitive MEMS sensors is designed, fabricated and tested for the wide temperature range from -55ºC to 225ºC. Sigma-delta technique is used to achieve a high accuracy digital output. The circuit is implemented using the IBM 0.13 μm CMOS process technology which incorporates a 2.5 V power supply. Simulation results show that the circuit has better than 0.03% accuracy between -55 ºC to 225 ºC. Experimental results show that it has good temperature stability, resolution better than 1.44fF, and accuracy better than 2.4% between -20 ºC to 225 ºC. The circuit is tested with a commercial capacitive MEMS pressure sensor and shows stable response over the wide temperature range. The advantages of this circuit are that a digital output is obtained for ease of signal processing and transmission, and it has the potential to achieve very high accuracy. The performance of this circuit at high temperatures could be further improved with a fully differential architecture.

CHAPTER 6 CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSIONS

Capacitive MEMS sensors are used in numerous applications that operate over the temperature range from -55 ºC to 225 ºC. To improve signal to noise ratio and reduce wiring complexity, it is desirable to place the sensor readout circuits in close proximity to the sensor devices. And the sensor readout circuits must also be capable of operating over the same temperature range as the sensors. Designing sensor readout circuits for wide-temperature range operation is challenging, especially at the high-temperature end. Several circuit design challenges need to be addressed, including degradation in carrier mobility, reduction in MOS transistors threshold voltage, and increase of bulk junction leakage current.

In this dissertation, we develop a variety of readout circuits in standard CMOS process for capacitive MEMS sensors which are functional over a wide temperature range between -55 ºC to 225 ºC. The circuits are implemented using IBM 0.13 μm CMOS technology with 2.5 V power supply for the advantages of high level of integration and low power consumption.

In order to mitigate the circuit performance degradation which stems from adverse effects induced by high temperatures, several high-temperature circuit design techniques are used, including:

1) A constant-g_m biasing technique to stabilize gain, bandwidth and stability of amplifiers over the wide temperature range of interest.

2) Several high-temperature tolerant circuit architectures, including fully-differential circuitry, sigma-delta modulating structure to improve the circuit performance at high temperatures.

3) Optimization of analog switches (transmission gates). Minimum size NMOS transistors are used in analog switches to minimize the leakage current in the switches.

4) In the layout, common-centroid structures are used wherever applicable to reduce temperature induced common mode errors. Guard rings are placed around performance sensitive blocks to prevent latch-up at high temperatures.

To examine the effectiveness of the above-mentioned high-temperature circuit design techniques, several proof-of-concept core building blocks are designed and tested, including a constant-g_m biasing circuit, a single-ended folded-cascode amplifier, and a fully-differential folded-cascode amplifier with a switched capacitor common mode feedback circuit. The single-ended folded-cascode amplifier shows DC gain of 68.5 dB and power consumption of 0.69 mW at 225 °C. And from -20 °C to 225 °C, the DC gain varies only by 2.8 dB. The fully-differential folded-cascode amplifier with the switched capacitor CMFB circuit shows DC gain of 68.9 dB and power consumption of 0.51 mW at 225 °C. And from -20 °C to 225 °C, the DC gain varies only by 2.1 dB.

Using these core building blocks, three readout circuits for capacitive MEMS sensors are constructed, including:

1) A novel CMOS differential capacitance to voltage readout circuit for capacitive MEMS pressure sensors with a wide range of the steady-state capacitance values from 0.5 pF to 10 pF.

2) A CMOS capacitance to frequency readout circuit for capacitive MEMS sensors to convert the sensor capacitance into digital pulse signal which is modulated in frequency for ease of signal transmission in noisy environments.

3) A CMOS capacitance to digital readout circuit for capacitive MEMS sensors which uses a sigma-delta technique to convert the input ratio between sensor capacitance and reference capacitance into a high-accuracy digital output.

All these three capacitive sensor readout circuits are simulated over temperature range from -55 °C to 225 °C and tested over temperature range from -20 °C to 225 °C. Measurement results show that these circuits have good accuracy and temperature stability over the wide temperature range.

The circuit modules developed in this dissertation can be used as building blocks to construct even more sophisticated wide-temperature sensing systems. Although the high-temperature circuit design techniques are only verified in IBM 0.13 μm CMOS technology, the concepts used in these techniques are universal and they can be readily ported to other standard CMOS processes and even SOI processes.

6.2 FUTURE WORK

For the biasing resistor in the constant-gm circuit shown in Section 2.2, a poly resistor with TC around 100 ppm/ºC is used. Theoretically, the temperature stability of this circuit can be further improved if the TC of the biasing resistor can be further reduced. This could be achieved

by implementing the biasing resistor using two different kinds of resistors, one with positive TC and another with negative TC, connected in series with proper ratio to construct a combined resistor with TC near to zero.

In the capacitance to voltage readout circuit shown in Figure 3.1, the sample/hold switch could be replaced with a sample/hold circuit with dynamic switch leakage compensation [96] to reduce the leakage current at high temperatures and further stabilize the output voltage. Also, a larger hold capacitor or higher sampling clock could be used.

In the capacitance to frequency readout circuit, the integration current can be implemented using the circuit shown in Figure 4.12. Where the resistor R_1 can be implemented using the above-mentioned combined resistor with TC near to zero. The resulted integration current will be almost constant over wide temperature range and the accuracy of the capacitance to frequency readout circuit could be significantly improved.

For the capacitance to digital readout circuit, a fully differential architecture [105] could be used to more effectively suppress noises induced by clock-feedthrough, charge injection, and noise coupling from the substrate and power supply improve the circuit performance at high temperatures.

A sigma-delta ADC could be constructed using the fully-differential folded-cascode amplifier with a switched capacitor CMFB circuit developed in Chapter 2. This ADC could be placed after the capacitance to voltage readout circuit shown in Chapter 3 to realize a high-accuracy capacitance to digital readout circuit.

In all the three readout circuits for capacitive MEMS sensors developed in this dissertation, external clock signals are used. In the future, an on-chip oscillator and signal generation circuits

could be integrated with these readout circuits. In this case, stand-alone sensor readout circuits can be developed which only need wire connections for power supply and output signals. This can significantly simplify the wiring complexity and packaging for the fabricated chips.

Long-term temperature stability and reliability are key issues to be investigated before commercializing the wide-temperature sensor readout circuits. In our study, the fabricated wide-temperature readout circuits for capacitive MEMS sensors are tested for only short time periods (about 20 hours) undergoing several temperature cycles from -20 ºC to 225 ºC as shown in the results described in previous chapters. Long-term tests (>1000 hours) should be performed to verify the performance stability and reliability issues of these circuits over the desired wide temperature range.

REFERENCES

[1] *Microelectromechanical systems*. Available: https://en.wikipedia.org/wiki/Microelectromechanical_systems

[2] W. F. Brinkman, D. E. Haggan, and W. W. Troutman, "A history of the invention of the transistor and where it will lead us," *Solid-State Circuits, IEEE Journal of,* vol. 32, pp. 1858-1865, 1997.

[3] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Physical review,* vol. 94, p. 42, 1954.

[4] H. C. Nathanson, W. E. Newell, R. Wickstrom, and J. R. Davis Jr, "The resonant gate transistor," *Electron Devices, IEEE Transactions on,* vol. 14, pp. 117-133, 1967.

[5] L.-S. Fan, Y.-C. Tai, and R. S. Muller, "IC-processed electrostatic micromotors," *Sensors and actuators,* vol. 20, pp. 41-47, 1989.

[6] D. S. Eddy and D. R. Sparks, "Application of MEMS technology in automotive sensors and actuators," *Proceedings of the IEEE,* vol. 86, pp. 1747-1755, 1998.

[7] J. M. Younse, "Mirrors on a chip," *Spectrum, IEEE,* vol. 30, pp. 27-31, 1993.

[8] P. F. Van Kessel, L. J. Hornbeck, R. E. Meier, and M. R. Douglass, "A MEMS-based projection display," *Proceedings of the IEEE,* vol. 86, pp. 1687-1704, 1998.

[9] R. C. Johnson. (2013). *MEMS Market to Top $22 billion by 2018*. Available: http://www.eetimes.com/document.asp?doc_id=1320035

[10] *PRESS RELEASES GALLERY-MEMS*. Available: http://www.yole.fr/2014-galery-MEMS.aspx

[11] C. Liu, *Foundations of MEMS*: Pearson Education India, 2006.

[12] (2014). *DLP4710 DMD*. Available: http://www.ti.com/lit/ds/symlink/dlp4710.pdf

[13] *Introduction to Microelectromechanical Systems (MEMS)*. Available: https://compliantmechanisms.byu.edu/content/introduction-microelectromechanical-systems-mems

[14] J. Jayapandian. (2011). *Measure Laser Power With A Modified MEMS Pressure Sensor*. Available: http://electronicdesign.com/energy/measure-laser-power-modified-mems-pressure-sensor

[15] T. M. Adams and R. A. Layton, *Introductory MEMS: fabrication and applications* vol. 70: Springer Science & Business Media, 2009.

[16] R. J. Noriega-Manez. (2007). *Inertial Navigation*. Available: http://large.stanford.edu/courses/2007/ph210/noriega1/

[17] A. Seshia, M. Palaniapan, T. Roessig, R. T. Howe, R. W. Gooch, T. R. Schimert*, et al.*, "A vacuum packaged surface micromachined resonant accelerometer," *Microelectromechanical Systems, Journal of,* vol. 11, pp. 784-793, 2002.

[18] (2013). *OMRON Develops the World's First* 16x16 Element MEMS Non-Contact Thermal Sensor for Use in Human Presence Sensors Utilizing Wafer-Level Vacuum Packaging Technology*. Available: http://www.omron.com/media/press/2013/05/e0529.html

[19] A. L. Herrera-May, L. A. Aguilera-Cortés, P. J. García-Ramírez, and E. Manjarrez, "Resonant magnetic field sensors based on MEMS technology," *Sensors,* vol. 9, pp. 7785-7813, 2009.

[20] *Operating temperature*. Available: http://en.wikipedia.org/wiki/Operating_temperature

[21] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson, and M. Christopher, "The changing automotive environment: high-temperature electronics," *Electronics Packaging Manufacturing, IEEE Transactions on,* vol. 27, pp. 164-176, 2004.

[22] W. J. Fleming, "Overview of automotive sensors," *Sensors Journal, IEEE,* vol. 1, pp. 296-308, 2001.

[23] M. B. Barron and W. F. Powers, "The role of electronic controls for future automotive mechatronic systems," *Mechatronics, IEEE/ASME Transactions on,* vol. 1, pp. 80-88, 1996.
[24] R. Sharp, "The current status of high temperature electronics for automotive use," in *Automotive Electronic Standareds; Are They?(Ref. No. 1999/206), IEE Seminar on*, 1999, pp. 6/1-6/5.
[25] F. McCluskey, "Power Modulation Investigation for High Temperature (175-200 degrees Celcius) Automotive Application," Oak Ridge National Laboratory (ORNL), Oak Ridge, TN2007.
[26] R. Sharp, "High temperature electronics-possibilities and prospects," in *Advances in Semiconductor Devices (Ref. No. 1999/025), IEE Colloquium on*, 1999, pp. 1/1-1/4.
[27] G. C. Jeff Waston, "High-Temperature Electronics Pose Design and Reliability Challenges," *Analog Dialogue,* vol. 46, pp. 1-7, 2012.
[28] B. Parmentier, O. Vermesan, and L. Beneteau, "Design of high temperature electronics for well logging applications," in *Proc. of Int. Conf. on High Temperature Electronics (HITEN), Oxford, UK*, 2003, pp. 77-83.
[29] S. Lande, "Supply and demand for high temperature electronics," in *High Temperature Electronics, 1999. HITEN 99. The Third European Conference on*, 1999, pp. 133-135.
[30] A. Behbahani, B. Wood, D. Benson, A. Berner, B. Hegwood, J. Dejager*, et al.*, "Technology Requirements and Development for Affordable High-Temperature Distributed Engine Controls," 2012.
[31] C. Johnston, A. Crossley, and R. Sharp, "The possibilities for high temperature electronics in combustion monitoring," in *Advanced Sensors and Instrumentation Systems for Combustion Processes (Ref. No. 2000/080) IEE Seminar*, 2000, pp. 9/1-9/3.
[32] L. Chen and M. Mehregany, "A silicon carbide capacitive pressure sensor for in-cylinder pressure measurement," *Sensors and Actuators A: Physical,* vol. 145, pp. 2-8, 2008.
[33] D. G. Senesky, B. Jamshidi, K. B. Cheng, and A. P. Pisano, "Harsh environment silicon carbide sensors for health and performance monitoring of aerospace systems: A review," *Sensors Journal, IEEE,* vol. 9, pp. 1472-1478, 2009.
[34] D. J. Young, J. Du, C. A. Zorman, and W. H. Ko, "High-temperature single-crystal 3C-SiC capacitive pressure sensor," *Sensors Journal, IEEE,* vol. 4, pp. 464-470, 2004.
[35] X. Li, Q. Liu, S. Pang, K. Xu, H. Tang, and C. Sun, "High-temperature piezoresistive pressure sensor based on implantation of oxygen into silicon wafer," *Sensors and Actuators A: Physical,* vol. 179, pp. 277-282, 2012.
[36] K. Kasten, J. Amelung, and W. Mokwa, "CMOS-compatible capacitive high temperature pressure sensors," *Sensors and Actuators A: physical,* vol. 85, pp. 147-152, 2000.
[37] S. Zhang and F. Yu, "Piezoelectric materials for high temperature sensors," *Journal of the American Ceramic Society,* vol. 94, pp. 3153-3170, 2011.
[38] D. Damjanovic, "Materials for high temperature piezoelectric transducers," *Current Opinion in Solid State and Materials Science,* vol. 3, pp. 469-473, 1998.
[39] X. Jiang, K. Kim, S. Zhang, J. Johnson, and G. Salazar, "High-temperature piezoelectric sensing," *Sensors,* vol. 14, pp. 144-169, 2013.
[40] K. Kasten, N. Kordas, H. Kappert, and W. Mokwa, "Capacitive pressure sensor with monolithically integrated CMOS readout circuit for high temperature applications," *Sensors and Actuators A: Physical,* vol. 97, pp. 83-87, 2002.
[41] W. P. Eaton and J. H. Smith, "Micromachined pressure sensors: review and recent developments," in *Smart Structures and Materials' 97*, 1997, pp. 30-41.
[42] K. D. Wise, "Integrated sensors, MEMS, and microsystems: Reflections on a fantastic voyage," *Sensors and Actuators A: Physical,* vol. 136, pp. 39-50, 2007.
[43] M. Carlin and J. Ray, "The requirements for high temperature electronics in a future high speed civil transport," in *Proc. 2nd Int. High Temp. Electron. Conf.(HiTEC), Charlotte, North Carolina, USA*, 1994.
[44] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-temperature electronics-a role for wide bandgap semiconductors?," *Proceedings of the IEEE,* vol. 90, pp. 1065-1076, 2002.

[45] X. Yu, "High-temperature bulk CMOS integrated circuits for data acquisition," Case Western Reserve University, 2006.
[46] M. Verbeck, C. Zimmermann, and H.-L. Fiedler, "A MOS switched-capacitor ladder filter in SIMOX technology for high temperature applications up to 300 C," *Solid-State Circuits, IEEE Journal of,* vol. 31, pp. 908-914, 1996.
[47] M. Willander and H. Hartnagel, *High temperature electronics* vol. 2: Springer, 1997.
[48] F. P. McCluskey, T. Podlesak, and R. Grzybowski, *High temperature electronics*: CRC press, 1996.
[49] S. Majerus, W. Merrill, and S. L. Garverick, "Design and long-term operation of high-temperature, bulk-CMOS integrated circuits for instrumentation and control," *Energytech, 2013 IEEE,* pp. 1-6, 2013.
[50] M. Huque, B. Blalock, C. Su, R. Vijayaraghavan, S. Islam, and L. Tolbert, "SOI based integrated circuits for high-temperature applications," in *Proceedings of International Conference and Exhibition on High Temperature Electronics (HiTEC 2008), Albuquerque, New Mexico*, 2008.
[51] M. Assaad, P. Gérard, L. Francis, and D. Flandre, "Ultra low power, harsh environment SOI-CMOS design of temperature sensor based threshold detection and wake-up IC," in *SOI Conference (SOI), 2010 IEEE International*, 2010, pp. 1-2.
[52] P. Francis, A. Terao, B. Gentinne, D. Flandre, and J.-P. Colinge, "SOI technology for high-temperature applications," in *Electron Devices Meeting, 1992. IEDM'92. Technical Digest., International*, 1992, pp. 353-356.
[53] L. Toygur, A. Patil, J. Guo, X. Yu, and S. Garverick, "A 300 C, SOI transimpedance amplifier with application to capacitive temperature sensing," in *Sensors, 2012 IEEE*, 2012, pp. 1-4.
[54] J. Pathrose, X. Gong, L. Zou, J. Koh, K. T. Chai, M. Je*, et al.*, "High temperature bandgap reference in PDSOI CMOS with operating temperature up to 300 C," 2012.
[55] S. L. Garverick, C.-W. Soong, and M. Mehregany, "SiC JFET integrated circuits for sensing and control at temperatures up to 600 C," *Energytech, 2012 IEEE,* pp. 1-6, 2012.
[56] P. G. Neudeck, S. L. Garverick, D. J. Spry, L. Y. Chen, G. M. Beheim, M. J. Krasowski*, et al.*, "Extreme Temperature 6H‐SiC JFET Integrated Circuit Technology," *Silicon Carbide: Power Devices and Sensors, Volume 2,* pp. 121-155, 2010.
[57] C.-W. Soong, A. C. Patil, S. L. Garverick, X. Fu, and M. Mehregany, "550 Integrated Logic Circuits using 6H-SiC JFETs," *Electron Device Letters, IEEE,* vol. 33, pp. 1369-1371, 2012.
[58] P. G. Neudeck, G. M. Beheim, and C. S. Salupo, "600 C Logic Gates Using Silicon Carbide JFET's," 2000.
[59] S. Pearton, J. Zolper, R. Shul, and F. Ren, "GaN: Processing, defects, and devices," *Journal of applied physics,* vol. 86, pp. 1-78, 1999.
[60] X. Yu and S. L. Garverick, "A 300 Â° C, 110-dB Sigma-Delta Modulator with Programmable Gain in Bulk CMOS," in *Custom Integrated Circuits Conference, 2006. CICC'06. IEEE*, 2006, pp. 225-228.
[61] P. C. de Jong, G. C. Meijer, and A. H. van Roermund, "A 300 C dynamic-feedback instrumentation amplifier," *Solid-State Circuits, IEEE Journal of,* vol. 33, pp. 1999-2009, 1998.
[62] C. Davis and I. Finvers, "A 14-bit high-temperature ΣΔ modulator in standard CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 976-986, 2003.
[63] C. Tai-Hua, L. T. Clark, and K. E. Holbert, "Memory design for high temperature radiation environments," in *Reliability Physics Symposium, 2008. IRPS 2008. IEEE International*, 2008, pp. 107-114.
[64] J. Prince, B. L. Draper, E. Rapp, J. Kronberg, and L. Fitch, "Performance of digital integrated circuit technologies at very high temperatures," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on,* vol. 3, pp. 571-579, 1980.
[65] X. Yu and S. L. Garverick, "Mixed-signal, 275/spl deg/C instrumentation amplifier in bulk CMOS," in *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, 2005, pp. 641-644.

[66] J. Haslett, F. Trofimenkoff, I. Finvers, F. Sabouri, and R. Smallwood, "High temperature electronics using silicon technology," in *Solid-State Circuits Conference, 1996. Digest of Technical Papers. 42nd ISSCC., 1996 IEEE International*, 1996, pp. 402-403, 481.
[67] I. G. Finvers, J. Haslett, and F. Trofimenkoff, "A high temperature precision amplifier," *Solid-State Circuits, IEEE Journal of,* vol. 30, pp. 120-128, 1995.
[68] P. C. de Jong and G. C. Meijer, "A high-temperature electronic system for pressure-transducers," *Instrumentation and Measurement, IEEE Transactions on,* vol. 49, pp. 365-370, 2000.
[69] F. A. Levinzon, "175 Silicon-Based Hybrid Charge Amplifier for 175 and 100-mV/G Miniature Piezoelectric Accelerometer," *Sensors Journal, IEEE,* vol. 6, pp. 1164-1169, 2006.
[70] *http://www.analog.com/en/analog-to-digital-converters/capacitance-to-digital-converters/products/index.html#Capacitive_to_Digital_Converters*.
[71] *MS3110 datasheet*. Available: http://www.isc8.com/assets/files/ms3110_datasheet.pdf
[72] S. M. Sze, *Semiconductor devices: physics and technology*: John Wiley & Sons, 2008.
[73] B. Van Zeghbroeck, "Principles of semiconductor devices," *Colarado University,* 2004.
[74] F. Shoucair, "Design consideration in high temperature analog CMOS integrated circuits," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on,* vol. 9, pp. 242-251, 1986.
[75] B. V. Zeghbroeck. (2011). *Principles of Electronic Devices*. Available: http://ecee.colorado.edu/~bart/book/book/title.htm
[76] F. Klaassen and W. Hes, "On the temperature coefficient of the MOSFET threshold voltage," *Solid-state electronics,* vol. 29, pp. 787-789, 1986.
[77] I. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on,* vol. 48, pp. 876-884, 2001.
[78] N. Sadeghi, S. Mirabbasi, and C. P. Bennington, "A 2.5 V 0.13 µm CMOS amplifier for a high-temperature sensor system," in *Circuits and Systems and TAISA Conference, 2009. NEWCAS-TAISA'09. Joint IEEE North-East Workshop on*, 2009, pp. 1-4.
[79] *IBM 8RF-DM CMOS Process*. Available: https://www.mosis.com/vendors/view/ibm/8rf-dm
[80] N. Sadeghi, "Design techniques for high-temperature analog and mixed-signal integrated circuits," PhD Thesis, The University of British Columbia, 2012.
[81] B. Razavi, *Design of analog CMOS integrated circuits*: The McGraw-Hill Companies, Inc., 2000.
[82] P. E. Allen and D. R. Holberg, *CMOS analog circuit design*: Oxford Univ. Press, 2002.
[83] H. Daoud, S. Bennour, S. BenSalem, and M. Loulou, "Low power SC CMFB folded cascode OTA optimization," in *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, 2008, pp. 570-573.
[84] K.-L. Chau, S. Lewis, Y. Zhao, R. Howe, S. Bart, and R. Marcheselli, "An integrated force-balanced capacitive accelerometer for low-g applications," *Sensors and Actuators A: Physical,* vol. 54, pp. 472-476, 1996.
[85] J. Wu, G. K. Fedder, and L. R. Carley, "A low-noise low-offset capacitive sensing amplifier for a 50- µ g/ √ Hz monolithic CMOS MEMS accelerometer," *Solid-State Circuits, IEEE Journal of,* vol. 39, pp. 722-730, 2004.
[86] W. Yun, R. T. Howe, and P. R. Gray, "Surface micromachined, digitally force-balanced accelerometer with integrated CMOS detection circuitry," in *Solid-State Sensor and Actuator Workshop, 1992. 5th Technical Digest., IEEE*, 1992, pp. 126-131.
[87] J. Geen, S. J. Sherman, J. F. Chang, and S. R. Lewis, "Single-chip surface micromachined integrated gyroscope with 50/h Allan deviation," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 1860-1866, 2002.
[88] N. Yazdi, A. Mason, K. Najafi, and K. D. Wise, "A generic interface chip for capacitive sensors in low-power multi-parameter microsystems," *Sensors and Actuators A: Physical,* vol. 84, pp. 351-361, 2000.

[89] M. Liu, G. Zhang, J. Dong, and C. Zhao, "Interface circuit for capacitive microaccelerometer," in *Circuits and Systems, 2008. MWSCAS 2008. 51st Midwest Symposium on*, 2008, pp. 654-657.
[90] T. Kevin, D. Han, P. Ravinder, D. Duy, Y. Chin, W. Jian*, et al.*, "118-dB dynamic range, continuous-time, opened-loop capactance to voltage converter readout for capacitive MEMS accelerometer," in *Solid State Circuits Conference (A-SSCC), 2010 IEEE Asian*, 2010, pp. 1-4.
[91] M. Liu, L. Xie, and X. Jin, "Design and realization of a universal capacitive readout integrated circuit," *Analog Integrated Circuits and Signal Processing,* vol. 82, pp. 449-456, 2015.
[92] N. Yazdi, H. Kulah, and K. Najafi, "Precision readout circuits for capacitive microaccelerometers," in *Sensors, 2004. Proceedings of IEEE*, 2004, pp. 28-31.
[93] A. Merdasi, Y. Wang, G. Xereas, and V. Chodavarapu, "Design and fabrication of a three-axis accelerometer sensor microsystem for wide temperature range applications using semi-custom process," in *SPIE MOEMS-MEMS*, 2014, pp. 89730O-89730O-12.
[94] S. Patel, T. Mlsna, B. Fruhberger, E. Klaassen, S. Cemalovic, and D. Baselt, "Chemicapacitive microsensors for volatile organic compound detection," *Sensors and Actuators B: Chemical,* vol. 96, pp. 541-553, 2003.
[95] (2014). *http://www.protron-mikrotechnik.de/download/Protron-Pressure-Sensor-11_2014.pdf*.
[96] L. Zou, J. Pathrose, K. Chai, M. Je, and Y. Xu, "Sample-and-hold circuit with dynamic switch leakage compensation," *Electronics Letters,* vol. 49, pp. 1323-1325, 2013.
[97] S. Chatzandroulis and D. Tsoukalas, "Capacitance to frequency converter suitable for sensor applications using telemetry," *Analog Integrated Circuits and Signal Processing,* vol. 27, pp. 31-38, 2001.
[98] C.-T. Chiang, C.-S. Wang, and Y.-C. Huang, "A CMOS integrated capacitance-to-frequency converter with digital compensation circuit designed for sensor interface applications," in *Sensors, 2007 IEEE*, 2007, pp. 954-957.
[99] F. Krummenacher, "A high-resolution capacitance-to-frequency converter," *Solid-State Circuits, IEEE Journal of,* vol. 20, pp. 666-670, 1985.
[100] Y. Wang and V. P. Chodavarapu, "Design of CMOS capacitance to frequency converter for high-temperature MEMS sensors," in *Sensors, 2013 IEEE*, 2013, pp. 1-4.
[101] L. Yao, P. Lamarche, N. Tawil, R. Khan, A. M. Aliakbar, M. H. Hassan*, et al.*, "CMOS conductometric system for growth monitoring and sensing of bacteria," *Biomedical Circuits and Systems, IEEE Transactions on,* vol. 5, pp. 223-230, 2011.
[102] F. Shoucair, "Potential and problems of high-temperature electronics and CMOS integrated circuits (25–250° C)-an overview," *Microelectronics Journal,* vol. 22, pp. 39-54, 1991.
[103] Y. Cao and G. C. Temes, "High-accuracy circuits for on-chip capacitance ratio testing or sensor readout," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on,* vol. 41, pp. 637-639, 1994.
[104] B. Wang, T. Kajita, T. Sun, and G. Temes, "High-accuracy circuits for on-chip capacitive ratio testing and sensor readout," *Instrumentation and Measurement, IEEE Transactions on,* vol. 47, pp. 16-20, 1998.
[105] B. Wang, "High-accuracy circuits for on-chip capacitor ratio testing and sensor readout," PhD Thesis, Oregon State University, 1998.
[106] A. Baschirotto, R. Castello, and F. Montecchi, "Finite gain compensation techniques for high-Q bandpass SC filters," in *Circuits and Systems, 1990., IEEE International Symposium on*, 1990, pp. 2813-2816.
[107] R. Schreier, G. Temes, A. Yesilyurt, Z. Zhang, Z. Czarnul, and A. Hairapetian, "Multibit bandpass delta-sigma modulators using N-path structures," in *Circuits and Systems, 1992. ISCAS'92. Proceedings., 1992 IEEE International Symposium on*, 1992, pp. 593-596.
[108] (2014). Available: http://www.protron-mikrotechnik.de/download/Protron-Pressure-Sensor-11_2014.pdf