Development of Front-End Electronics for a Non-Invasive Positron Detector to Monitor the Arterial Input Function in Dynamic PET

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Abstract:

Positron emission tomography (PET) is used for monitoring biological activity/function (functional imaging). It is widely used for diagnostics of cancer, heart disease, and neurological disorders over time. Injecting a radiotracer with a positron-emitting radioisotope that provides information about the physiological activity in vivo. Dynamic PET is a more advanced version of PET where mathematical models, called kinetic models, are used to represent the underlying biology. Unfortunately, time-course information of the radiation activity concentration in the patient's arteries, called the arterial input function (AIF), is required to perform these models. This method causes discomfort for the patient and requires the presence of a medical professional for assessing the patient and the variation of nuclear activity in the blood with respect to the AIF. It is an expensive and time-consuming procedure. This project focuses on the development of a front-end electronics prototype that process the signal coming from the detector for a PET scan without the need for blood withdrawal from the patient and it frequently tracks the radioactivity of the blood. The time resolution of the detector depends on the total noise of the front-end electronics, the signal amplitude, and the rise time of the signal in the scintillator. The design and implementation of the front-end electronics are the goals of the project. The signal is obtained by designing front-end electronics with high bandwidth low-noise amplifier and an active RC-CR filters network with a gain of 47.69 dB. A leading-edge discriminator was designed with 20 ns delay time to measure the time of the event.

L'abstrait

La tomographie par émission de positrons (TEP) est utilisée pour surveiller l'activité/fonction biologique (imagerie fonctionnelle) Elle est largement utilisée pour le diagnostic du cancer, des maladies cardiaques et des troubles neurologiques Injection d'un radiotraceur avec un radio-isotope émetteur de positrons qui fournit des informations sur l'activité physiologique dans vive. La TEP dynamique est une version plus avancée de la TEP où des modèles mathématiques, appelés modèles cinétiques, sont utilisés pour représenter la biologie sous-jacente. Malheureusement, des informations sur l'évolution temporelle de la concentration d'activité de rayonnement dans les artères du patient, appelées fonction d'entrée artérielle (AIF), sont nécessaires pour réaliser ces modèles. Cette méthode provoque une gêne pour le patient et nécessite la présence d'un professionnel de la santé pour évaluer le patient et la variation de l'activité nucléaire dans le sang par rapport à l'AIF. C'est une procédure coûteuse et longue. Ce projet se concentre sur le développement d'un détecteur qui mesure l'activité du sang artériel au cours d'une TEP sans qu'il soit nécessaire de prélever du sang sur le patient et qui suit fréquemment la radioactivité du sang. La résolution temporelle du détecteur dépend du bruit total de l'électronique frontale, de l'amplitude du signal et du temps de montée du signal dans le scintillateur. La conception et la mise en œuvre de l'électronique sont les objectifs du projet. L'énergie est obtenue en concevant une électronique frontale avec un amplificateur à faible bruit à large bande passante et un réseau de filtres RC-CR actifs. Un discriminateur de fraction constante a été conçu avec un temps de retard de 20 ns pour mesurer le temps de l'événement.

Acknowledgements

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Contributions of Authors

The thesis was written by Ali Ali. The photodetector setup was developed by Liam Carroll. The equipment used belong to the Enger lab located at JGH. Dr. Shirin Abbasi Enger supervised the project and provided general guidance.

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List of Abbreviations

ADP: Avalanche photodiode

ASIC: Application specific integrated circuit

CSA: Charge sensitive amplifier

CR-RC: Capacitor-Resistor Resistor-capacitor

dPET: dynamic positron emission tomography

FEE: Front-end electronics

IC: Integrated circuit

LED: Leading edge discriminator

Opamp : Operational Amplifier

PET: positron emission tomography

S-K: Sallen-Key

SiPM: Silicon photomultipliers

List of Symbols

τ: time constant

C_f: Feedback capacitor

R_F: Feedback resistor

A_o: Open-loop gain

f_c: Cut-Off frequency

R_X: Resistance used in CR-RC active filter

C_z: Capacitance used in CR-RC active filter

Chapter 1: Introduction:

1.1 Importance of Radiation physics and Applications

The development of radiation sensors have paved a path for new methods in science. Analyzing the radiation particles provides a great way to understand the natural phenomena that occurs in various field like physics, chemistry and even immunology [1, 2]. The energy and other properties of radiation signals are useful for analysis of matter. There are plenty of examples that highlight the importance of radiation physics and detectors. Namely, radiation detectors are used in astrophysical applications to analyze matter in the universe. In medicine, radiation particles are used in cancer treatment. As an example, precise targeting of the protons onto cancer sites has repetitively caused apoptosis of malignant and benign cells. It is used as an alternative for surgery and chemotherapy [3]. Combining both the physics of radiation particles and pathology produces techniques for diagnostics. Radiation is used for a potential Malaria vaccine. The parasites are irradiated along with parasite to produce a weaker version of the pathogen for vaccine production [4]. Radiation is used to study materials. For instance, high energy radiation damages silicon. This affects the electronics used for nuclear experiments and facilities and therefore the electronics require more shielding [5]. In most applications, radiation signals must be processed by external detectors that converts their energy into a readable electric signal. It is challenging to develop a device for radiation since high energy particles are harmful and interact with the surrounding matter which leads to a noisy signal. For example, in medical imaging using radiation, the signal is continuously exposed to environmental interference. Additionally, safety protocols were implemented when dealing with radiation devices.

1.2 PET Mechanism

Positron emission tomography (PET) is an imaging modality based on radiation detection from the body. The modality has been used to diagnose cancer, myositis, and neuro-degenerative diseases [6-8]. The process begins when a radiotracer is injected inside the patient. It is composed of a positron emitting isotope attached to a radiopharmaceutical molecule, and once injected the targeted cells consume the radiopharmaceutical, and the radiotracer is trapped inside the cell. It decays into a positron, which travels for a few millimeters before undergoing annihilation process where the particles are converted into two γ rays at almost 180° apart at 511 keV. A number of detectors surround the patient to capture these rays. They are related by time and position. An Anti-coincidence circuit is used to distinguish these rays for image production. More information regarding PET scan mechanism is found in [9].

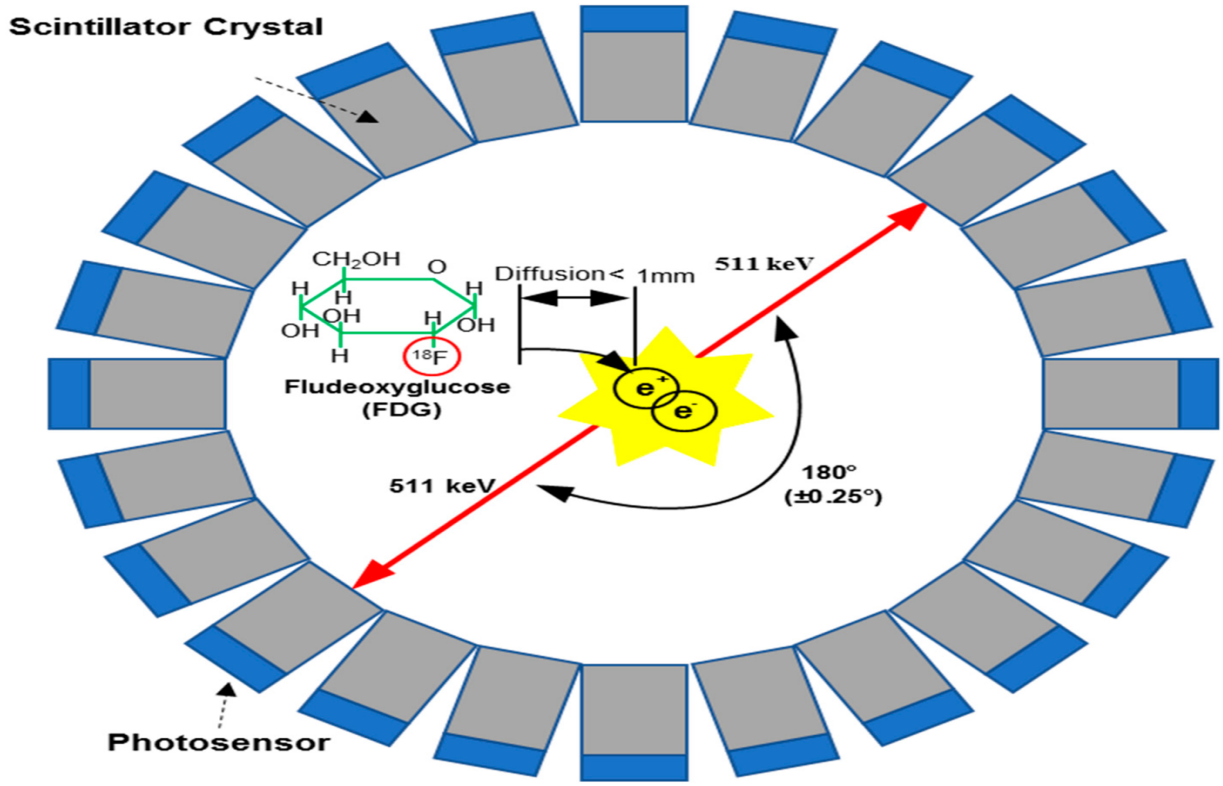


Fig 1: PET Mechanism

1.3 Dynamic Imaging

To obtain accurate information regarding the radiotracer uptake *in vivo*, real-time images are acquired. There are two techniques for image acquisition. The widely used method for PET is static imaging. A radiotracer is injected inside the patient followed by a waiting period of 5-10 min [9]. During that period, the radiotracer reaches the organs in question for imaging. However, dynamic imaging begins right after the injection of the radiotracer. Dynamic PET is used for functional imaging in time. Radiation detection begins directly when the radiotracer is injected inside the body. It keeps track of the tracer as it gets distributed to the organs via the blood by the heart. This method is referred to a dPET.

To obtain data required for dynamic imaging, a system of differential equations models the behavior of the radiotracer inside the body [10]. These are acquired by the arterial input function (AIF). It is part of the three-compartment model. It consists of continuous sampling of the blood from the patient to detect the radio-distribution in the body [11]. This method is invasive and requires a medical professional assistance for a long period of time. Another method to obtain the AIF is microfluidics. There are multiple techniques for AIF acquisition.[12-14] However, they have their limitations with regards to data sampling.

To acquire the AIF, the processing time must be fast. With the development of imaging methods, time-of-flight (TOF) is the solution for fast imaging. Traditionally, the particle can be located along a line of response (LOR). However, TOF localizes the particle accurately using a probability distribution among the location of the event (within centimeters). TOF has been used along with AIF for amyloid imaging [15]. The mechanism is demonstrated below.

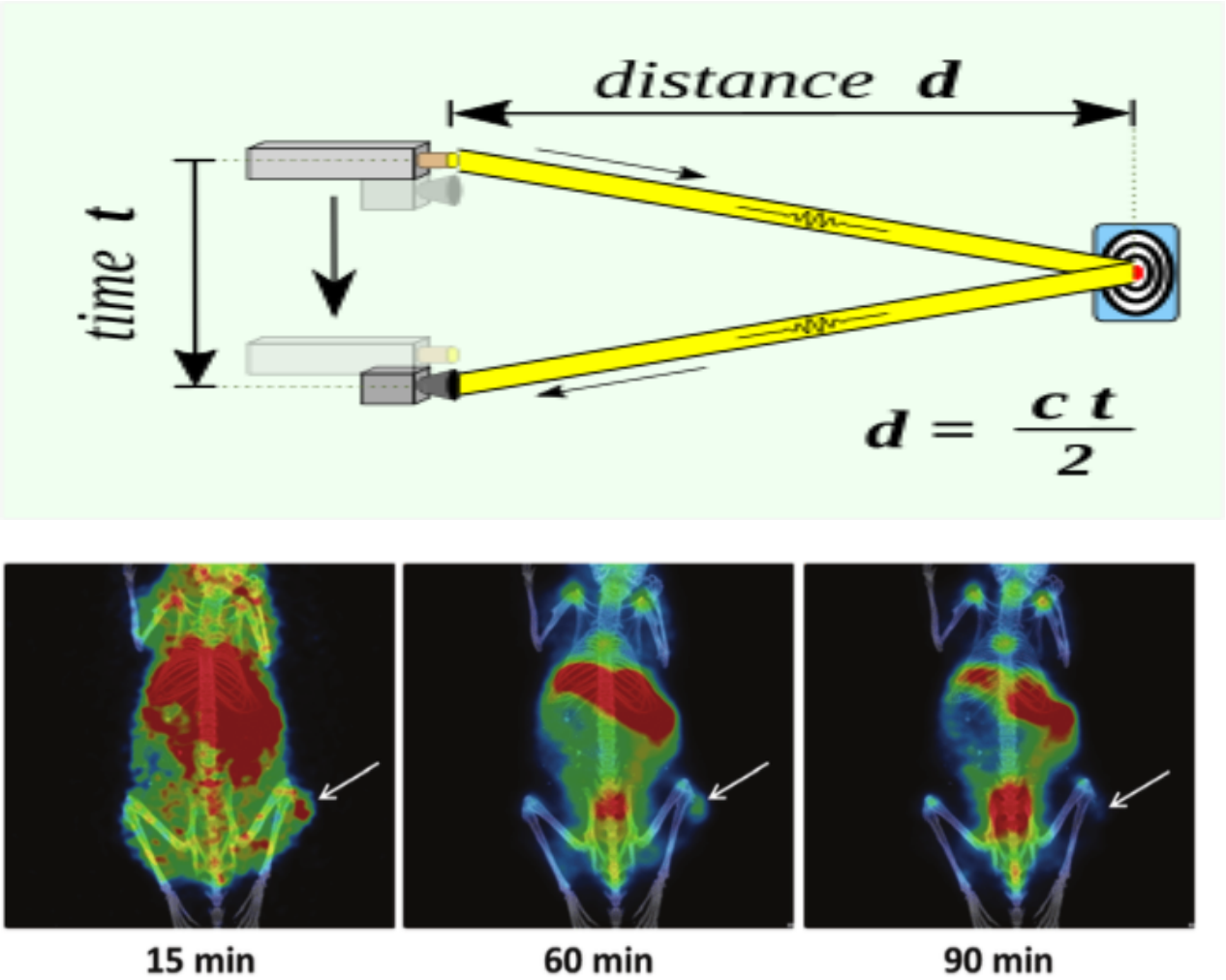


Fig 2: TOF mechanism (top), image produced by dPET to monitor the biodistribution of a radiotracer for 90 min[16]

1.4 Front-end Electronics

In any device that receives an electrical signal (voltage pulse or current pulse), having suitable front-end electronics (FEE) is required to procure accurate data. It consists of the interphase between a sensor and a processor. A well-known example is the radio frequency (RF) FEE. An electromagnetic wave is sent and received by an antenna. Subsequently, it produces a small and noisy voltage. The RF FEE has an amplifier and filter to manage the noise and amplitude of the signal [17]. At the output of the FEE, the signal must be interpreted by the microprocessor. FEE is used in many medical devices for bio-signal processing. For example, a low power FEE was developed for continuous monitoring of an ECG signal. This device was used for patients with severe heart complications to diagnose arrythmia [18]. For medical Imaging, FEE are essential in magnetic resonance imaging (MRI) to produce an image with high resolution [19] and in PET scans. In general, FEE are composed of a low noise amplifier (LNA) and a network of filters. LNA are used to produce a signal with high gain and the filters to shape the signal. The signal is followed by an analog-to-digital converter (ADC) for digital analysis. Designing the proper FEE depends on the input signal and its nature. In addition, noise analysis is dependent on the nature of the signal.

When multiple systems are combined, a part of the signal is lost. As an illustration, when piezoelectric sensors are used, the electric signal produced by pressure isn't fully linear. There's a mismatch that causes a loss of energy. Therefore, designing FEE is highly dependent on the input to the system.

1.5 Detector Motive and Description

As discussed in the previous section, acquisition of the AIF is important for dPET. The methods are invasive, time consuming and error prone. A new proposal was made for a *non-invasive* radiation detector that will be used to measure the AIF. The device measures the radiotracer's distribution by sensing radiation coming from the radial vein and radial artery. It is made up out of scintillator fibers, photodetector, and electronics. The output of the FEE is a distinguishable pulse for peak sensing. It produces a pulse containing the time of the event. An older version was produced by PhD student Liam Carroll. The FEE used are two ZFL-1000LN+ amplifiers connected in series. Timing was measured using a CAEN discriminator and a digitizer. These are expensive units. In this project, a prototype of FEE was developed using off-the-shelf components assembled on a breadboard. The output produced is comparable to the signal generated by the expensive electronics. In addition, the prototype can be easily soldered on a printed chip board (PCB) and ASIIC (application specific integrated circuit). It consumes less power and its more flexible. The design process of the FEE involved circuit simulations, testing the selected IC and implementing the circuit. A signal optimization was achieved by selecting the appropriate parameters.

Chapter 2: Background

2.1 SiPM

The first stage of the detector is scintillation where a high energy particle produces photons in the visible range. Light is conducted to the photodetector that produces a current pulse. The silicon photomultipliers (SiPM) are composed of an array of a modified p-n structures. Each structure is an avalanche photodiode (APD). The diode operates by applying a bias voltage creating a high electric field. Once light is absorbed, charged electrons are accelerated which produces more electron-hole pairs. This mechanism is called the impact ionization where a single electron-hole pair leads to the production of multiple charges.[20] They are collected at the output. The multiplication factor for SiPM ranges from 10^5-10^7 [21]. Once the amount of electron-hole produced, the charge will dissipate. It can be calculated based on the following equation:

$$Q_{cell} = C_{cell}(V_{bias} - V_{breakdown}) \qquad [2.1]$$

C_{cell} is the capacitance obtained from the inner depletion region of the p-n substrate. Once the cell reaches the breakdown voltage, a quenching resistor (R_q) is placed for charge dissipation. The output of each cell is summed, and a larger current pulse is produced. Electrical modelling of the SiPM relies on the overall intrinsic capacitance. For APD cell, the capacitance is estimated to have a capacitance 100 fF [21]. However, it differs based on the size, material, and optical properties. The photodetector is modeled as two RC circuits in parallel. The quenching part is composed of parasitic capacitance C_q and a R_q. The diode is modeled as switch that closes once an event is triggered.

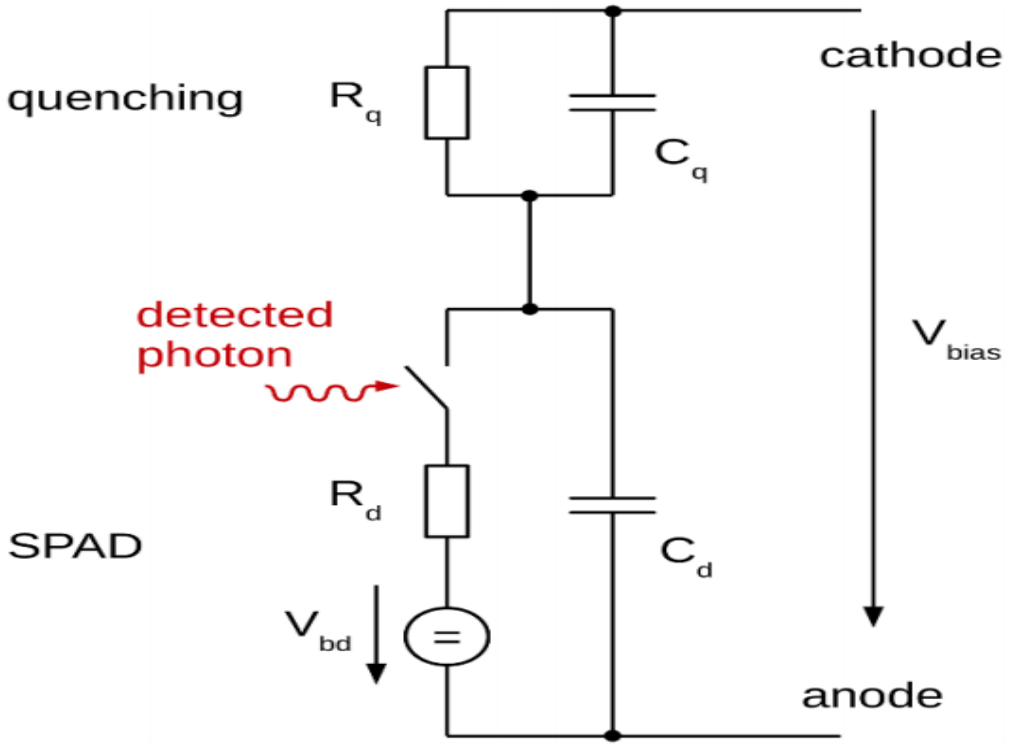


Fig 3: The electrical model of a SPAD [22]

Once the SPAD is triggered, the pulse discharges through C_d. It provokes a voltage variation across C_q. The discharge time is calculated as follows:

$$\tau_r = R_d(C_q + C_d) \qquad [2.2]$$

As the current increases across R_d, the voltage drop reaches a maximum. Once the avalanche process is quenched, the cell enters a recovery mode where the output pulse is produced. It is modeled as a delta-Dirac function. Nonetheless, the impurities cause the output to be broadened. The amplitude of the pulse depends on the current i_d produced. Output capacitance affects the electronics in the next stage. The pulse amplitude ranges from 100 pA to 20 mA depending on the SiPM.

2.2 Front-end Electronics Architecture for Radiation Detection

The design of radiation detectors consists of mainly extracting the energy of the particle and the time of the event. As discussed in the previous section, the pulse generated at the photodetector can vary from 100 pA to 20 mA. The rise and decay time ranges been 1 ns to 80 ns. There are many techniques by which an electrical pulse is processed. However, the objective of the FEE is to amplify and produce a distinguishable signal that is readable to a microprocessor. Furthermore, the output of the signal must have a high signal-to-noise ratio [23]. The objective of FEE is to both isolate peaks for energy measurement and count the time of the radiation event. For energy measurement, a gain stage followed by a shaping network are used to isolate the peak of the pulse. As for time measurement, an amplifier is required followed by a time discriminator with high speed to measure the event.

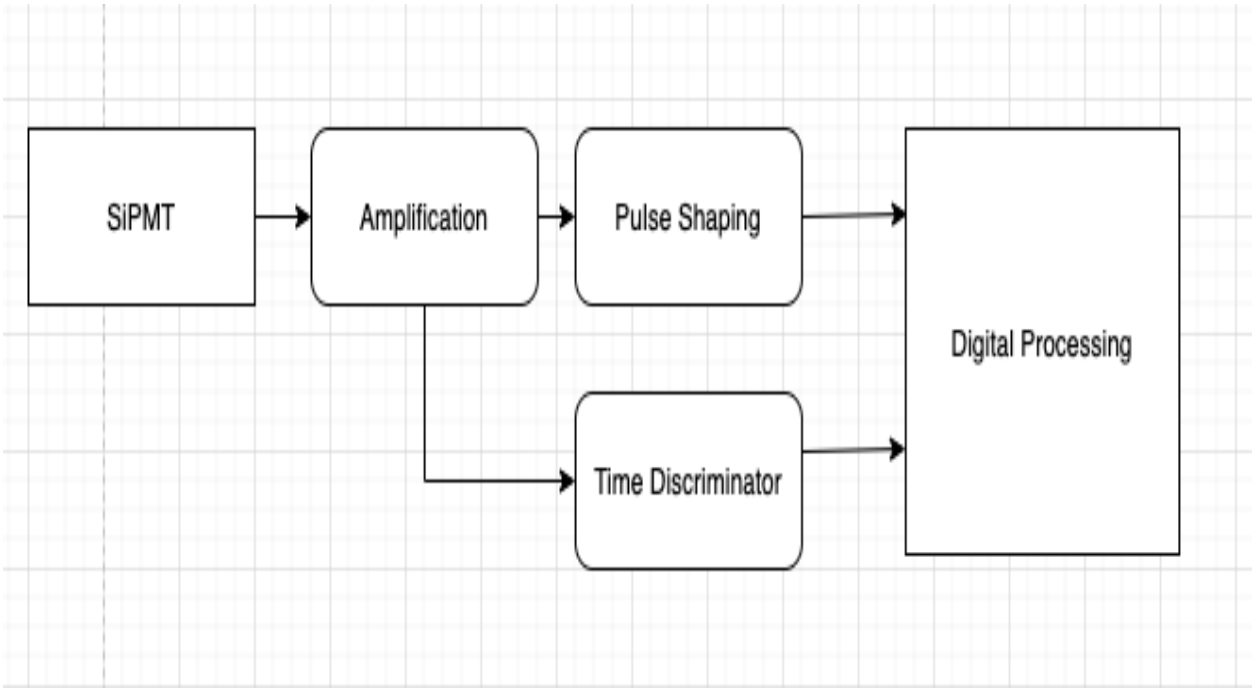


Fig 4: Block Diagram of FEE Electronics

There are multiple considerations for this topology. Namely, for accurate measurement, the rise and decay times of the pulse are matched with time constant of the circuit.

For instance , a fast FEE was developed to measure fast pulses (30 ps r.m.s) [24]. It consisted of wide-band amplifier followed by gain stage and fast comparator. It measured time as well using a time-to-digital (TDC) converter. Another fast circuit was implemented as PET scanner for animals called RatCap [25]. It contained a preamp, shaping network and a comparator. It detected peaks with 10-100 ns rise time. The time resolution is 2.5 ns. An AISC for detecting high-energy neutrons produced by the deuterium-tritium fusion reaction consists of charge sensitive amplifier (CSA) followed by a gain stage which consisted of two amplifiers in series and shaper A comparison table is shown below for different FEE architectures and their application.

Table 1: A comparison of different values of the FEE architectures

	Gain (dB)	Time resolution (ns)	SNR (dB)	Number of channels
TOFPET2 [24]	200e/15fF	0.05	30	64
RatCap [25]	15.15	6.7	--	32
Nino [26]	1070	1	38.6	8
$^{10}BF_3$ Tube[27]	10	200	--	1
TGER [28]	54.1	0.03	--	64

Depending on the application, FEE varies from a single channel readout system to 2560 channels [29].

2.3 Energy measurement Electronics

2.3.1 The Gain Stage

Charge sensitive Amplifier

The main purpose of the gain stage is amplifying the signal. For radiation, the pulses must be summed. The integration is performed at the feedback loop of the LNA. A RC network must have a time constant that allows the pulse to be fully accumulated. Additionally, the value of the intrinsic capacitance of the photodetector affects the speed of the summation. Compensation capacitance is required at the input of LNA. A graph is shown below (Fig.5) demonstrating the effect of the normalized output of the intrinsic capacitance of the photodetector affecting the output with and without compensation of the detector. Therefore, a compensation capacitor is added between the SiPM and the gain stage.

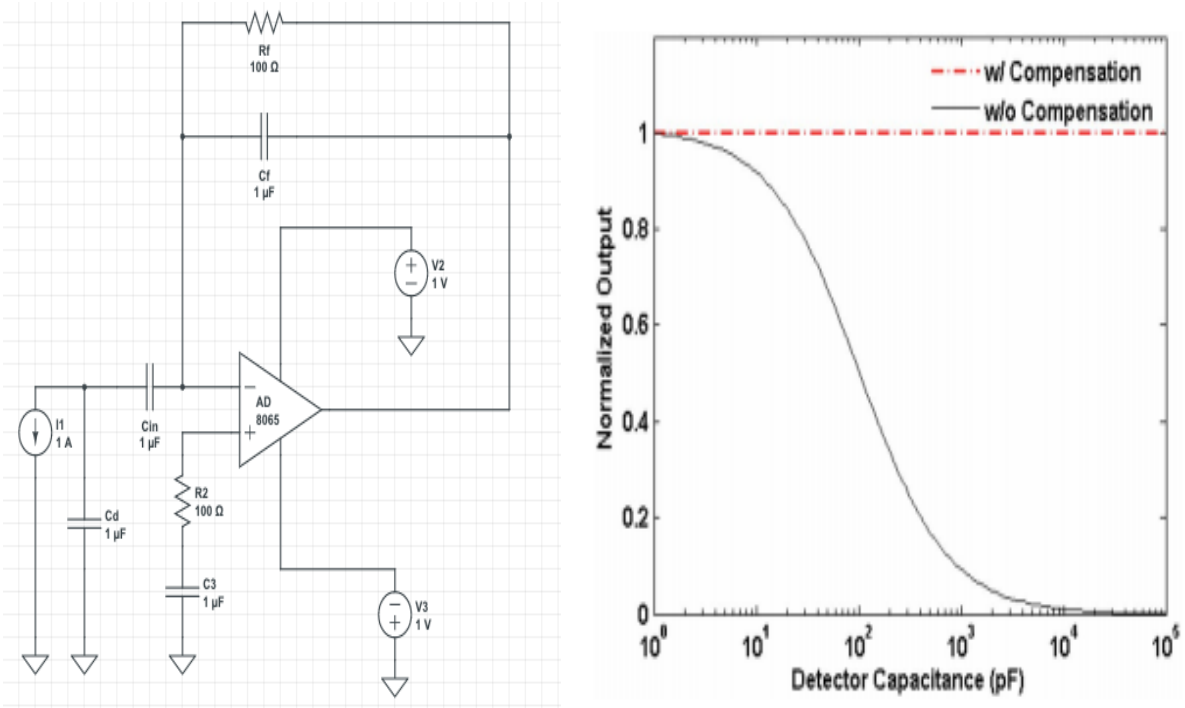


Fig 5: Charge sensitive amplifier schematics (to the left) and the effect of intrinsic capacitance of SiPM with and without compensation capacitance (to the right) [30]

The time constant (τ) is described by the following equation:

$$\tau = C_f R_f \qquad [2.3]$$

For instance, if a pulse of a rise time of 20 ns is detected, then C_f and $R_f$must be selected accordingly such that the pulse is fully summed without dissipation.

More information regarding CSA design equations is provided in Appendix A. The second role of the CSA is amplification. The device used should provide a gain of approximately 60 dB. The gain of the CSA is inversely proportional to the value of the feedback capacitor. It can be approximated as follows:

$$V_{out} \sim \frac{Q_{in}}{C_f} \qquad [2.4]$$

Furthermore, the signal cannot exceed the power provided. Therefore, the amplification ratio is chosen correspondingly to allow the pulse to swing up to a maximum value. In that way, the energy of particle is fully captured. The ratio between the minimal detectable pulse and the maximum value should be high to be processed by an analog-to-digital converter. This value is called the linear dynamic range. As part of the integration, the expected output has a long decay in comparison with the input. It can reach up to 10 μs. However, the energy information is obtained from the peak of the pulse. This method is called peak sensing detection [31]. The gain is related to the bandwidth of the amplifier used as well as the parasitic capacitance. However, having a wideband amplifier allows additional noise to be included in the output. The energy of the signal is converted from electron-volts to volts. Therefore, any noise added onto the signal may result in false detection. There are multiple proposed designs for gain stage of radiation detectors. A rest CSA was developed to detect pulse of a NaI(TI) detector [32]. It had a 47 pF at the feedback loop. Additionally, the pulse produced had an integration time of 1-10 μs. However, instead of using a

feedback resistor for pulse dissipation, they've used a digital AND gate controlled by a comparator with a series of diodes to manipulate the speed of the signal produced at the output. This approach has reduced the noise coming from the dark current since the capacitor will charge if the pulse is above the noise level. The gain reached was 60.82 dB. The gain was calculated from [33] by unit conversion in which they had a charge sensitivity of 4.26×10^{10} V/C and an output of 51.09 fC with slope of 1.98 fC/pF. Furthermore, a CSA was designed with a fast recovery time that's capable of producing a signal with a 50 ns peaking time [33]. The CSA had a gain-bandwidth of 140 MHz and a feedback capacitance of 1.3 pF. It used a resetting network as well to eliminate signal distortion. A CSA was designed with JEFT technology due to its low noise. For detecting fast pulses produced by the photodetector, a 0.9 pF with 500 M Ω impedance was used [34]. The bandwidth of the amplifier was 100 MHz producing a gain of 67 V/V. The output pulse had a 1.8 μs. CSA are used in other applications as the gain stage of FEE [35]. Some FEEs have designed a gain stage with multiple amplifiers to maximize the SNR. Other have used a wideband amplifier to minimize components and noise while maintaining high amplification.

2.3.2 Shaper Network

The main role of a shaper is trimming the output of the gain stage. It allows fast processing time of the pulse and cut additional noise. Essentially, shapers are filters applied in the time domain and the design relies on the filter's parameters such as: cut-off frequency, quality factor and noise optimization.

- Cutoff frequency (f_c): The frequency at which the signal starts attenuating
- Quality Factor (Q): Describes the smoothness of the filter. The higher it is, the narrower the bandwidth is

The output of the shaper's output is a pulse with fast rise and fast decay time while reaching the amplified amplitude. There are many methods to obtain a shape pulse by implementing a high-pass filter followed by a low-pass filter. Ideally, the delta-Dirac function is integrated by the CSA. The result is a unit step function. The shaper produces ideally a delta-Dirac function. However, the peak is higher.

Passive Shapers

A Passive shaper is used in radiation detection as an integral part of the shaping network. It consists of a CR-RC network. The resistor and capacitor value determine the cut-off frequency.

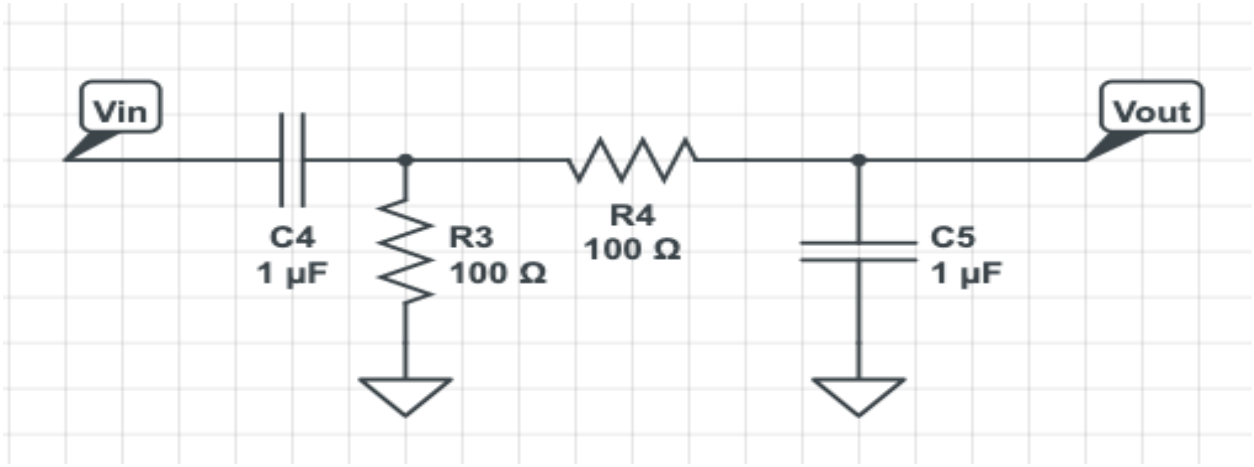


Fig 6: A CR-RC passive shaper

For instance, if a 100 ns is required, the selection of the low-pass filter's cut-off frequency is around 17.93 MHz. CR-RC network has been used as an integral part of shaper used for readout electronics of the accelerator detecting kaon decays [36]. The shaper has 72 ns pulse with a rise of 40 ns. Evidently, the main issue with passive shaper is signal attenuation. A 7-pole filter was used for the ATLAS Tile calorimeter [37]. The detector is capable of measuring energy from 220 MeV to 1.3 TeV. The pulse width of the shaper designed is 50 ns. It had a bandwidth of 12.5 MHz

CR-RC Active shapers

Evidently, a passive network attenuates the signal. Therefore, an amplifier is required to shape the pulse without losing power. This concept is referred to as active filters. The network configuration is similar to the passive shaper. However, the amplifier has intrinsic capacitance and resistance. Consequently, it contributes to the pulse shaping as well. In addition, the amplifiers possess a feedback with a resistor and a capacitor. It adds controllability over the rise and decay of the shaper without attenuation of the pulse. Details on the synthesis of active CR-RC shaper are provided in Appendix B.

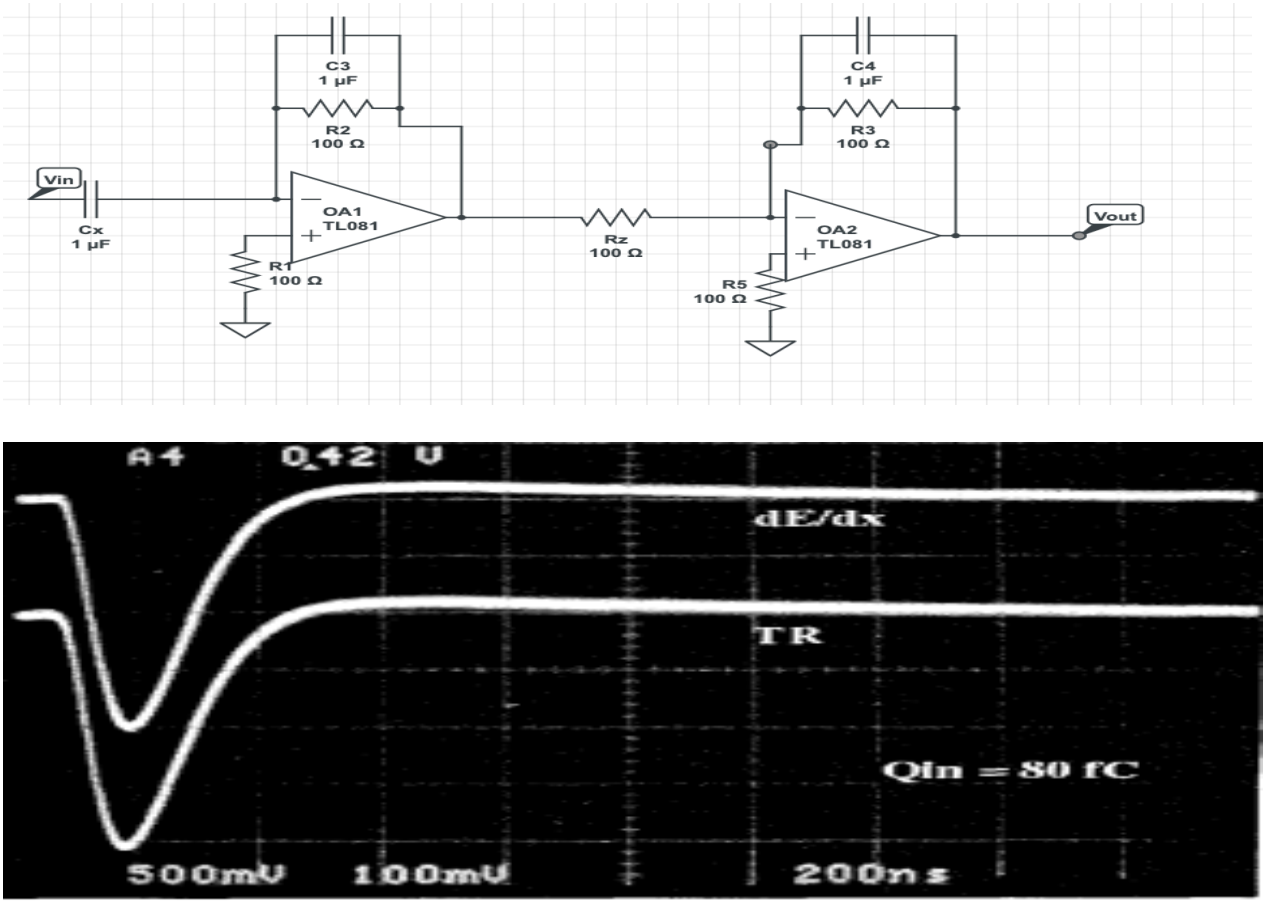


Fig 7: Topology of 1st order CR-RC active shaper The results of an active 2nd 3rd CR-RC shaper[38]

A fast 1st order CR-RC active shaper was developed using off-the-self IC in conjunction with an field programmable gates arrays (FPGA) board. The design was able to capture gamma rays and produce energy profile for multiple components such as: Co, Am, Sr-Y and Cs [39]. A 1st order CR shaper was design for CZN/Si detector[40]. It had a peaking time of 250 ns.

Sallen-Key Active Shapers

Another widely used shapers are Sallen-Key (S-K) active filters. It employs a faster synthesis process due to the relation between the parameters used. It's used part of the quasi-Gaussian filter used in nuclear electronics. S-K filters have the advantage of maintain the same cut-off frequency and quality factor while producing a signal with a higher amplitude [41]. More details on the design parameters of an S-K filter can be found in [42]

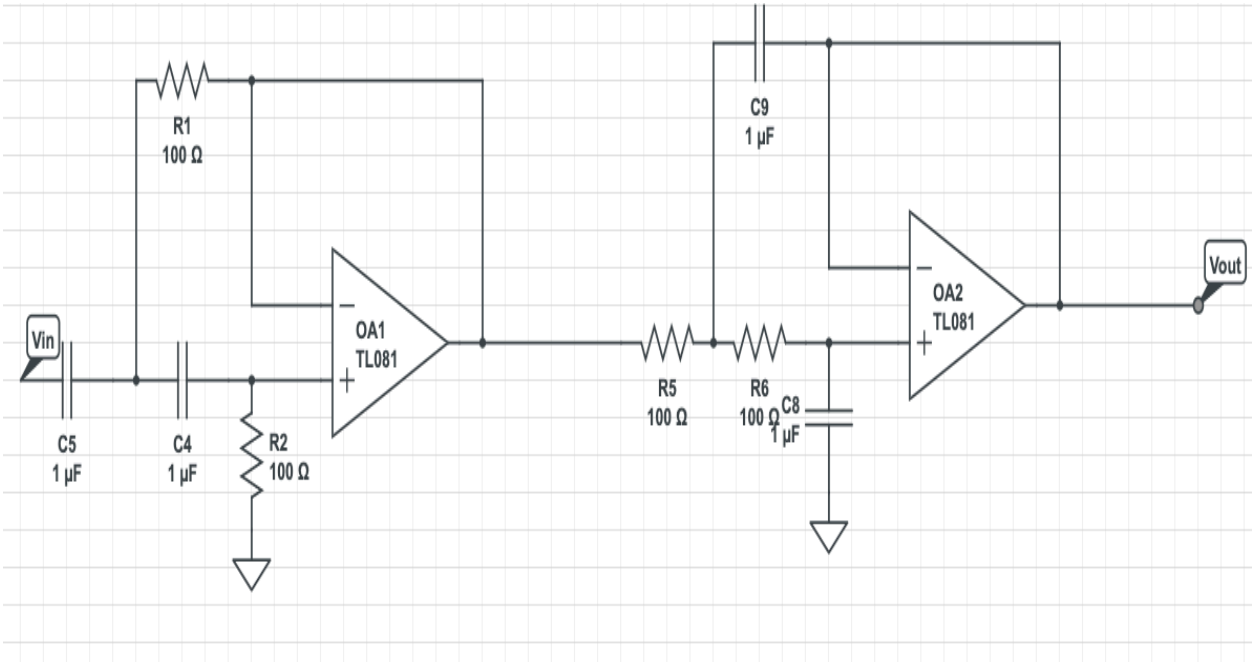


Fig 8: A high pass 2nd order S-K filter followed by a 2nd order S-K low pass filter

An algorithm was developed to design shaper based on S-K filter for a pulse with 1 µs duration [43].

2.5 Time Discriminator

The timing branch consists of a gain stage followed by a time discriminator. Timing discrimination is a process by which multiple comparators produce a logical high signal containing the duration of an event. This system is used for high-speed counting and coincidence detection.

Analog Comparators

An analog comparator is a device that compares its positive input to the negative. The mathematical operation is described below:

$$\begin{cases} V_{out} = 0 \; or \; V_{EE} \; if \; V_+ > V\_ or \; V_+ < V\_ \\ V_{out} = V_{DD} \; if \; V_+ = V\_ \end{cases} \qquad [2.5]$$

A DC voltage threshold is set on the inverting input while the input signal is connected to the non-inverting pin of the comparator. They don't have a high gain in contrast to the amplifier. Nevertheless, they have a high slew-rate which is the maximum output change of an amplifier per microsecond. Another parameter considered for comparator optimization is propagation delay. When a signal is compared to the threshold, the output is produced following a delay. The minimum input signal measured by the comparator is an important parameter as well. It iscalculated as follows:

$$\Delta V_{H,L} = V_H - V_L \qquad [2.6]$$

$$V_{min} = \frac{\Delta V_{H,L}}{A_o} \qquad [2.7]$$

There are many examples of fast comparators used for analog-to-digital converters (ADC). However, designs that uses an FPGA board had a built-in comparators [44]. A TL3016 comparator

was used for a voltage discriminator [45]. It has a 7.8 ns propagation time and a minimum input of 20 mV.

Leading Edge Discriminators (LED)

LED measures the rise of a signal in comparison with a baseline. It is suitable for large signals. Following a shaper circuit, the signal splits into the input of two comparators, and each compares the signal to a threshold. The comparator with a high threshold has a delay line. This allows the signal to last for the whole pulse to be processed. At the final stage, another comparator on an AND gate is used to compare the output of the preceding IC. The output is sensed by a counter for timing registration. For instance, when there's no pulse at the input, the LED produces a logic "HIGH". As a signal is compared, the output is a logic "LOW". At that moment, timing registration begins. Once a logic "HIGH" is produced again, it means that there's no longer a pulse and the counters stop. Practically, the low threshold isn't ground. It selected such that the noise floor is irrelevant to the output.

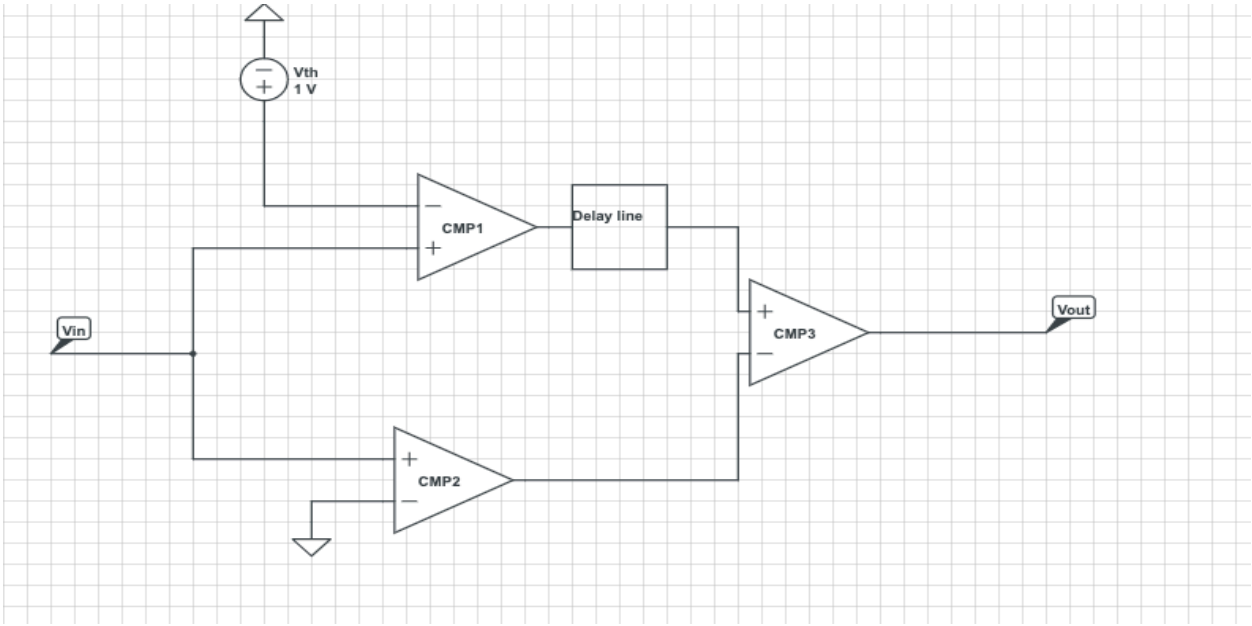


Fig 9: Circuit Topology of a LED

A LED was developed for coincidence detection in PET.[46]. The ORTEC584 was used in LED mode which measured particles at 367.3 ps range. A width modulated LED was developed as well for gamma rays detection [47]. It can vary the time window at which the comparators' output is processed resulting in a decrease of dead time. The time resolution was 3.64 ns. A LED was developed using AD96687 IC which had a 2.2 ns propagation time [48]. It can detect a 30 mV amplitude with a timing error of 90 ps. LED was used for charge timing at 35.3 ps [49].

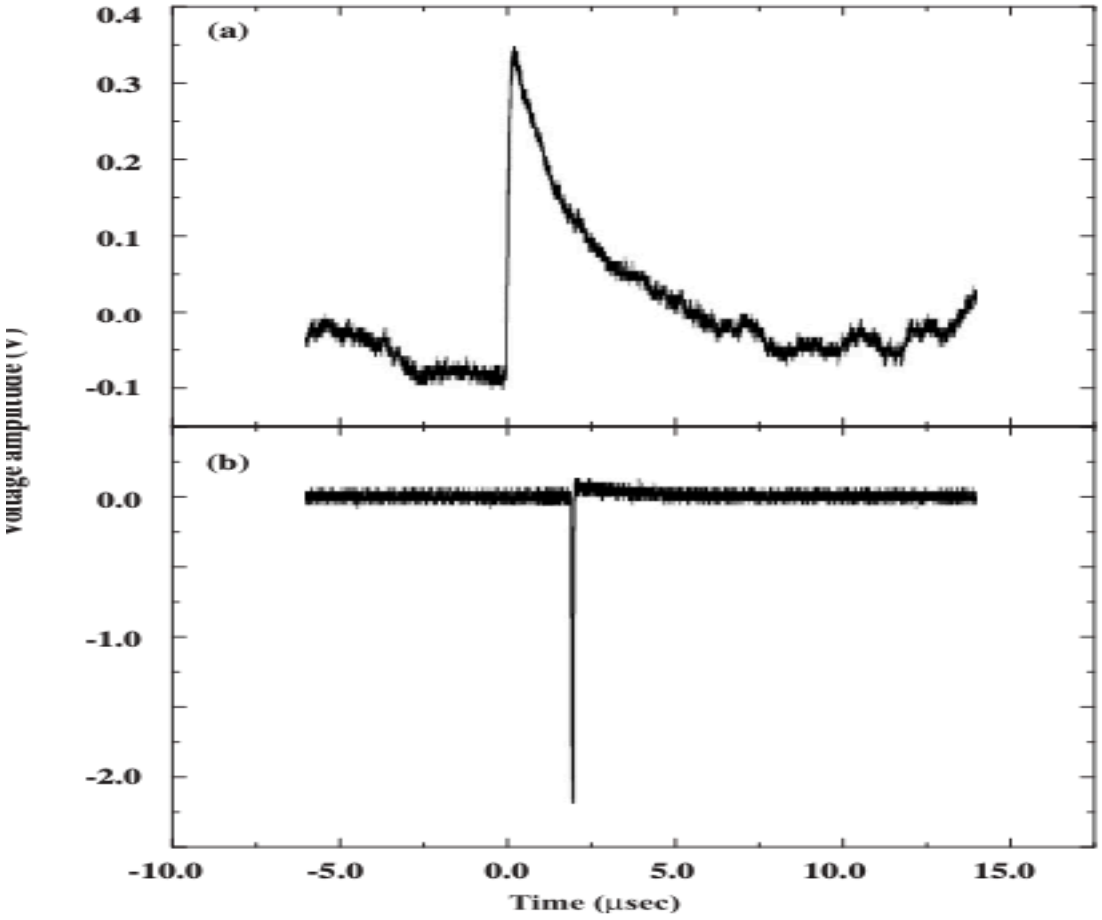


Fig 10: Output of a pulse shaper from a germanium detector (upper graph), the ouput of leading time discriminator (lower graph) with a 20 nsec timing. [50]

2.6 Noise types in FEE

Noise in electronics is described as unwanted variations of the current/voltage signal. When developing FEE for radiation detection, noise may affect energy and timing measurements. The electronics components used are supposed to add as low of a noise as possible. There are three main types of noise analyzed in FEE [51]:

- Thermal noise: It is caused by the random motion of electrons in any resistive material. Small voltage spikes are observed at the output. It is Calculated as follows:

$$e_n^2 = 4KTR \qquad [2.8]$$

  R is the value of resistance, T is the temperature and K in the Boltzmann constant

- 1/f noise: It is observed at lower frequencies resulted by the impurities in the semiconductors used.

$$i_n^2 = 2Ie \qquad [2.9]$$

  I is the current and e is electron charge

- Shot noise: It is caused by the current fluctuations. Unlike thermal noise, it has a constant power spectrum.

$$e_n^2 = \frac{Af}{f} \qquad [2.10]$$

  Af is the constant of the power desnity at DC and f is the frequency

Equivalent noise charge (ENC) is the quantity to measure the voltage produced by a capacitor. Namely, the intrinsic capacitance of the photodetector and capacitance of the CSA. There are many parameters that contributes to the value of ENC. Mainly, the detector current and feedback capacitance. The width and length of the transistors at the input of each IC are inversely proportional to the total value of ENC.

Chapter 3: Methodology

3.1 Photodetector Setup and Electrical Setup

To measure the pulse generated by visible light, an organic SiPMT was used. Purchased from DigiKey, the sensI MicroFC-SMA-10020 has a rise time of 15 ns and decay time of 50 ns. It has the bias voltage as an input and a slow and fast outputs. The device is connected to Fluke 412B high voltage power supply for biasing. It required positive polarity ranging from 28 V to 34 V. For more information, the datasheet provided by the vendor has more details on the optical input properties such as: responsivity, dark count, and efficiency. The slow output is used for this project. The fluorescent light is conducted through optical fibers onto the detector. It is placed inside a metal box for light shielding. Additionally, there's a cap that's placed onto the conducting fibers for shielding from any light source that might interfere with the signal.

Fig 11: The photodetector is enclosed in the metal box. Light is guided by the optical fiber (right) to the photodetector enclosed in the case (middle)

Lumerical INTERCONNECT simulation software was used to simulate the optical setup. The light produced by the scintillation fibers was in the range of 415-445 nm. Converting the wavelength to frequency by inversely dividing it by the light speed (c) give 68.96 THz . The optical properties of the SiPM for the photodetector are used to define the properties of APD. The responsivity of the SiPM was $1.1x10^6$ A/W and the intrinsic multiplication factor was 10^5. The optical fiber has a length of about 60 cm.

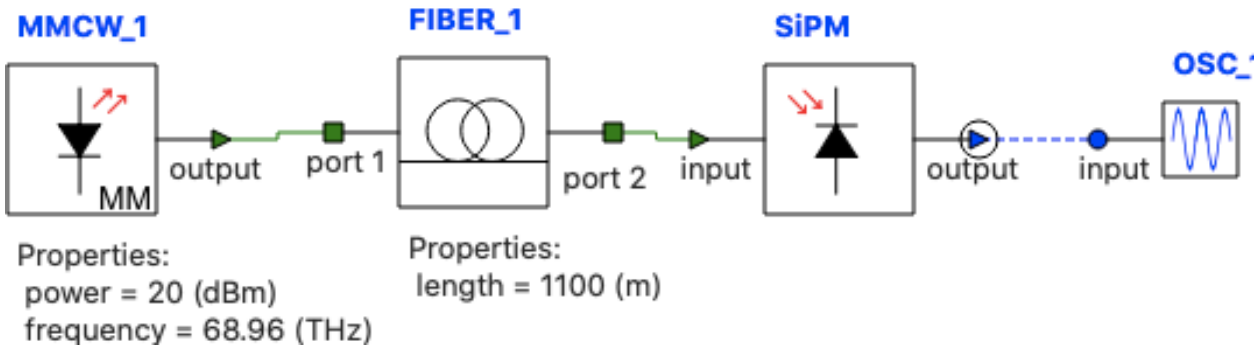


Fig 12: The optical set up in Lumerical INTERCONNECT

The software used for electrical simulations was advanced design system (ADS) by KeySight. It has spice fundamentals, and it has the tools to analyze high speed circuits. Each integrated circuit's properties were made according to the specifications form the vendor's data sheet. The input source is current pulse with a 15 ns rise time and 50 ns decay time which mimics the SiPM. A 50-pF capacitor modelling the intrinsic capacitance is placed in parallel with current pulse source. The source peaks at 20 mA. This was provided by the vendor's sheet

As for electrical testing, two wave generators are used. The oscilloscope for this project has a wave generator function and an additional HP generator. These are used to test the circuit with fast pulses. The FEE is developed on two breadboards (energy and time). An additional power supply is used for the circuit (Keysight E3631A). The breadboard has though hole components only. Therefore, an adapter is required to connect the photodetector to the electronics.

3.2 Energy Front-end Electronics Design and Implementation

3.2.1 Gain stage Design and Implementation

To implement the gain stage for energy measurement, multiple operational amplifiers were considered. The requirements for the energy FEE circuit are:

- Bandwidth: the gain bandwidth must be high (5 MHz < GBW)
- Gain: The gain must be at least 60 dB
- Noise Density: The lower it is, the better (15 nV/√Hz > Noise density). For this choice, JFET technology was considered due to its low noise.
- Input bias: Specified by each vendor
- Power consumption: 15 > DC supply voltage, the previous electronics used had a maximum of 15 V supply voltage. Therefore, the new design FEE must be lower than that for power consumption improvement.

The values mentioned above are used as a reference for comparisons at the simulation stage and testing. The simulation of parameters is shown in the appendix section. Multiple IC were purchased for testing and the selected ones yielded the best response to electrical and optical inputs. Additionally, the process by which the energy FEE are designed is shown below:

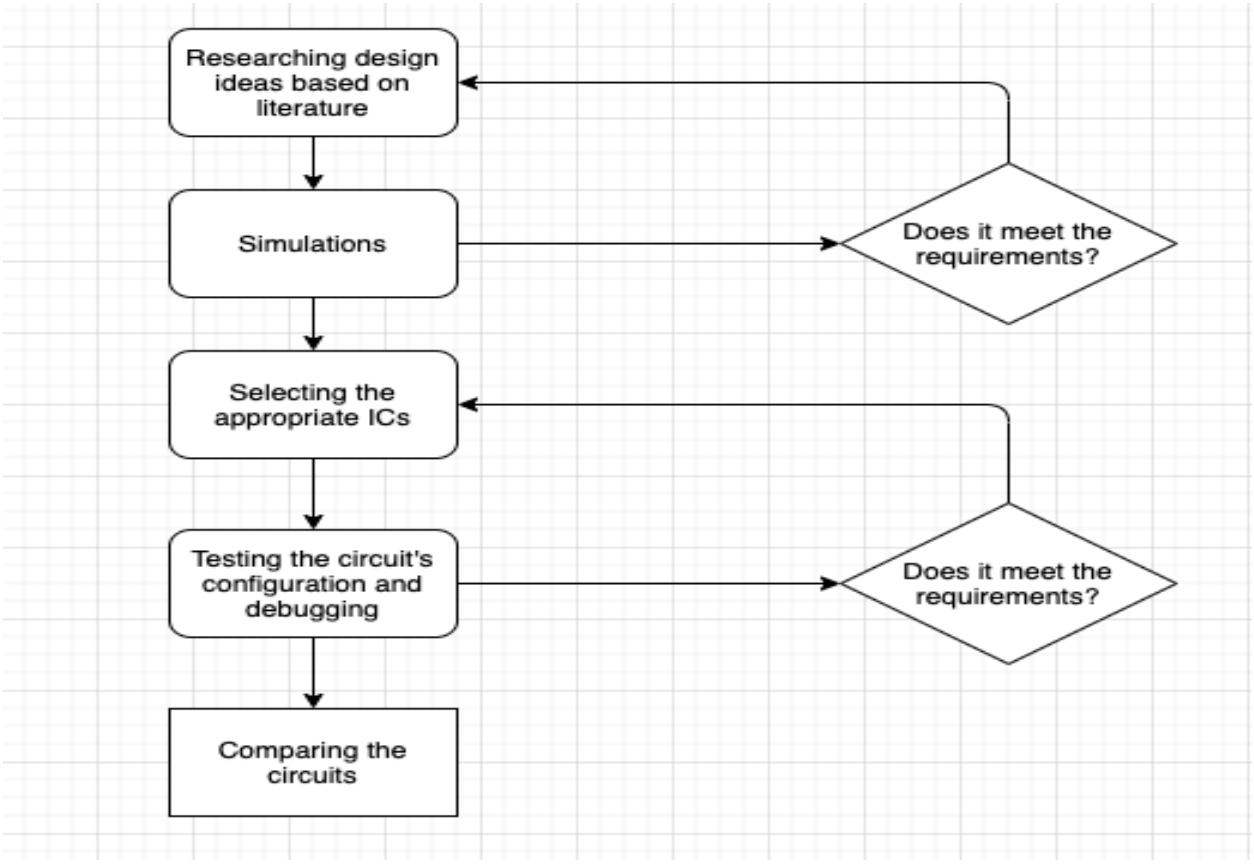


Fig 13: Block Diagram demonstrating the method by which the design and implementation are validated

For gain stage implementation, two topologies were considered:

- CSA followed by an instrumentation amplifier
- A wide band CSA

Two Amplifiers Circuit:

It consists of a CSA followed by a high gain instrumentation amplifier; The initial stage of the design was the selection of an appropriate compensation network. The intrinsic capacitance of the photodetector affected the pulse produced. The compensation capacitance of the device must be larger than the photodetector's intrinsic capacitance and the feedback capacitor.

$$C_D < C_f \leq C_c$$

Therefore, an additional capacitor was placed between the detector and the detector and amplifier to increase the input capacitance of the amplifier relative to the photodetector.

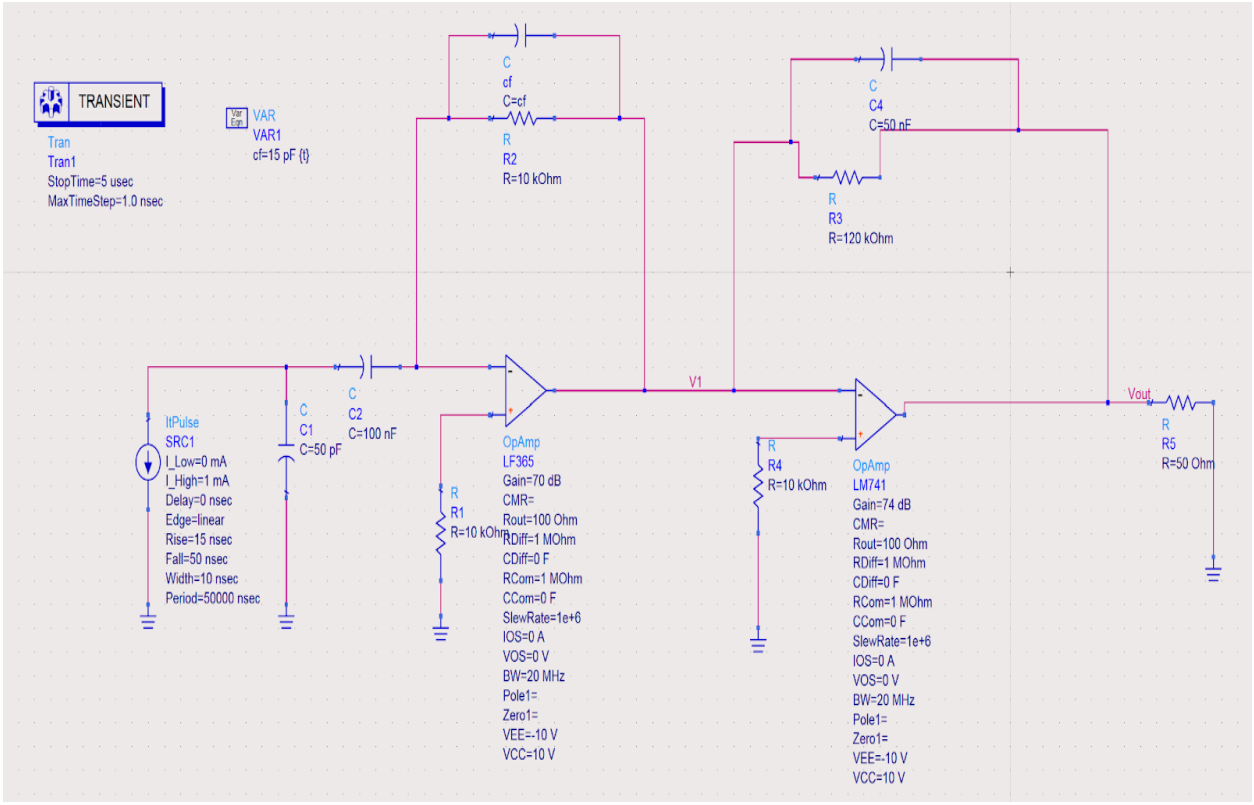


Fig 14: Circuit schematic of two amplifiers gain stage

It wasn't shown in the schematic, but it is assumed that there's a 100 nF capacitor between the V_{EE} and V_{cc}. A 50 Ω resistor is placed at the output to model the oscilloscope. Using the tunning function, All the resistor and capacitors were varied. The values of the gain, power supply, bandwidth and input impedance are based on actual devices that were selected for implementation.

Multiple parameters were varied for this design such as: compensation capacitance, the amplifier's bandwidth, biasing resistance, and the feedback network. As for the amplifier itself, according to the requirements mentioned above and the simulations, a list of amplifiers are purchased from DigiKey for testing. The table is given below:

Table 2: The ICs selected for the gain stage

IC Number	Gain (dB)	Gain Bandwidth (MHz)	Noise Density (nV/√Hz)	Offset Voltage (mV)	Operating Voltage Supply (V)
OPA2132	120- 130	8	8	0.25	2.5-18
LF356	70- 100	20	12	3	15-20
OPA350	100- 120	38	5	1	2.7-5.5
TLE2062	73	2 MHz	43	3.5	5-15
OPA657	65-70	275	4.8	2.2	4.-6
AD8065	100- 113	145	7	0.4-1.25	5-24

To test the gain characteristics of each device, a CSA configuration is built. Then, a 20 ns pulse was used as an electrical input by wave generator function from the oscilloscope. The frequency was varied from 10 kHz to 10 MHz Additionally, the peak of the input pulse was varied from 10 mV to 500 mV. Lastly, the SNR was measured by comparing the noise floor to the signal at the output. An additional test is performed with fluorescent light by connecting the photodetector.

Using the photodetector, measuring the peak of the pulse by varying the feedback capacitor and feedback resistor of the CSA with the ICs mentioned above was performed to optimize the gain as well.

Due to the feedback from the output the input and power supply inputs, oscillations appeared when testing the circuits at both the input and output. The oscillations reached as high as 5 V with a frequency of 100 kHz. Consequently, the photodetector's pulse became undetectable. The problem was solved by adding 0.1 μs capacitors in parallel with power inputs to the device. As for

oscillations caused by the feedback loop, a RC network are added at the output to filter the oscillations. These oscillations can damage the device if the current withdrawn is too high.

The IC mentioned in the table were tested using a variety of capacitors ranging from 1 pF to 1 μF and 1 k Ω to 1M Ω for feedback resistance. It produces a time constant of 50 ns. The instrumentation amplifier was the LM725. It had a 129 dB gain and a low noise. For this design were LF351 as the CSA followed by LM725. It had a feedback connection at the CSA of 47 pf with a 12.5 k Ω. The compensation capacitance was 1 μF. The DC power used was 12 V

High Bandwidth Amplifier Circuit

As suggested by some designs discussed in the previous chapter, only one amplifier can realize both gain and low noise without the need of an additional gain amplifier. The wide bandwidth amplifiers (LF356 and AD8065) provide high gain. They have a quick response as well. Therefore, designing a gain stage with a CSA alone was beneficial since the circuit will use less power and less noise is introduced to the circuit. Additionally, the signal won't clip due to the limited gain provided.

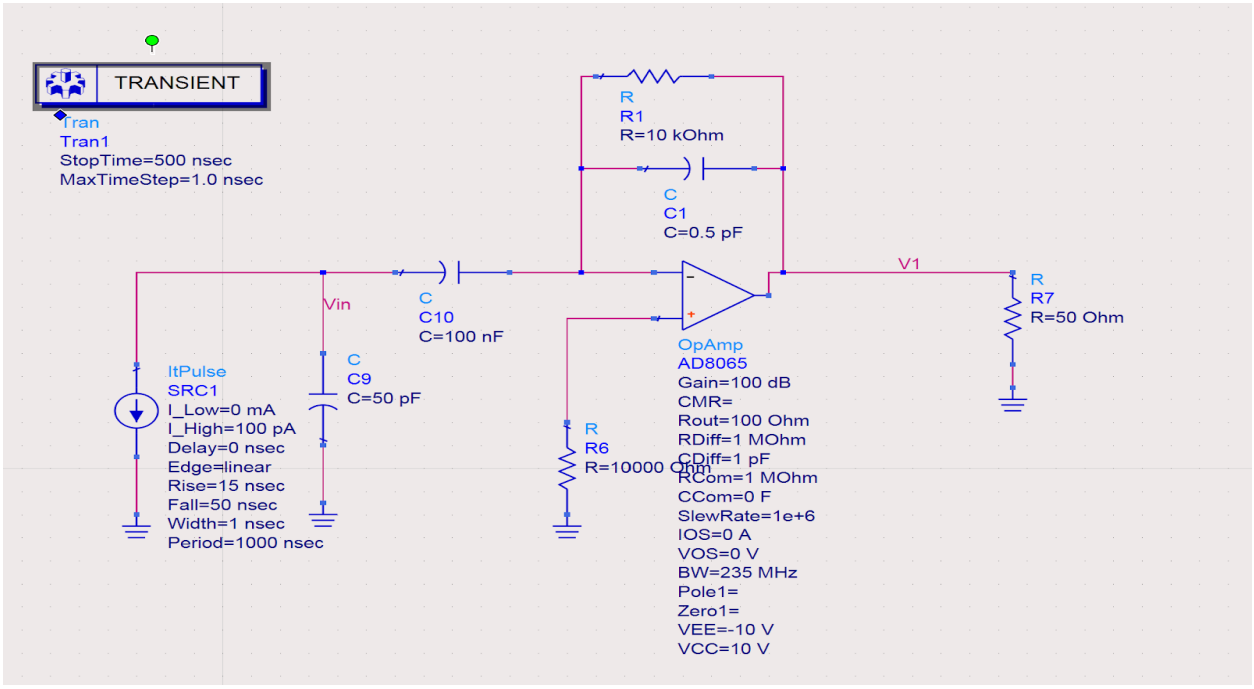


Fig 15: Circuit Schematic of the gain stage using a wideband amplifier

Since we're using a breadboard, a socket (LCQT-SOIC8-8 and SOT-23-5) is used as a surface mount to through whole adapter for the AD8065. The ICs are soldered onto the socket.

Testing the devices is carefully done as they are sensitive to the input bias current. Adding a capacitor at the non-inverting input of the amplifier minimized the current withdrawn from the power supply along with a control resistor. Testing was performed with the wave generator and fluorescent light.

3.2.2 Shaper Design and Implementation

Active Filter Design

For a pulse shaping network design, two shapers are simulated and tested. The first circuit is Sallen-Key high pass followed by a low pas filter. The parameters for selecting the bandwidth are described in Appendix B.

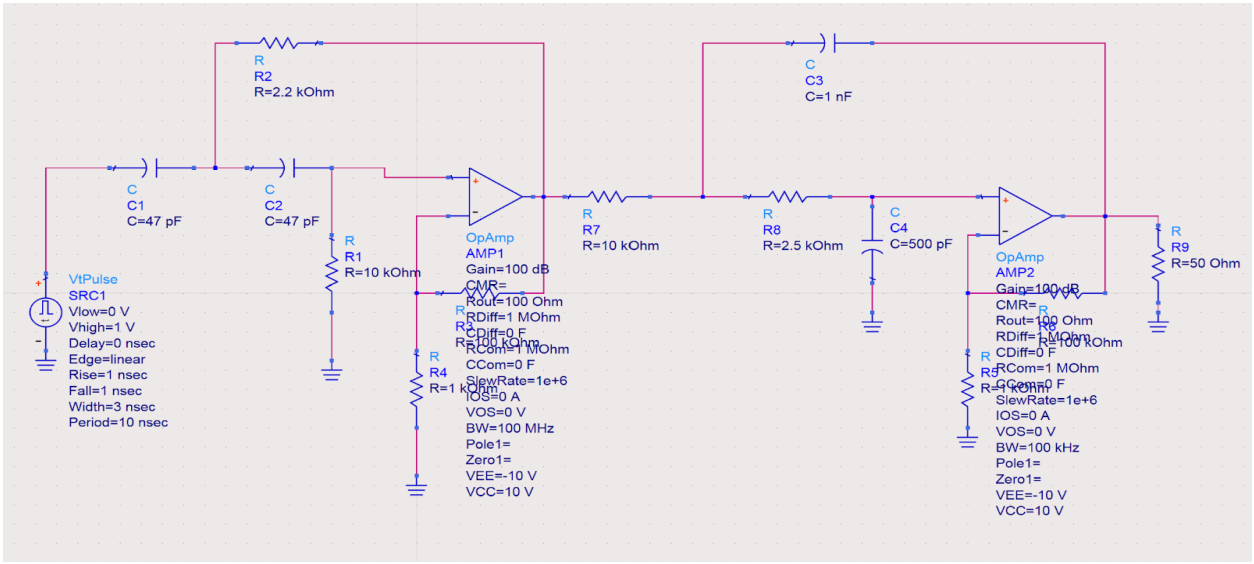


Fig 16: 2nd order S-K filters schematics

Tunning function was used to configure the best shaping. At the input, a voltage square signal was used to mimic the output of the gain stage.

Based on literature and simulations, general characteristics of the amplifiers used as active filters are highlighted. The ICs purchased for filter designed are mentioned below:

Table 3: The ICs selected for active filter design

IC Number	Gain (dB)	Bandwidth (MHz)	Minimum input (mV)	DC power supply (V)
LM358AN	100	0.1	300	5-30
OPA350PA	100	38	300	7
OPA134PA	104	8	700	2.5-18
OPA2137	86	1	3000	15

To test the filter, an AC input form wave generator was used with a 1 V peak-to-peak at different frequencies. The objective of this test is finding the cut-off frequency and construct a Bode plot. Using the design equations mentioned in Appendix B, the values of the resistors (R1 and R2) and capacitors (C1 and C2) were selected and varied with respect to the cut-off frequency. The challenge faced in filter design is finding the relation between the cutoff frequency and the timing constant. The filter worked for an AC signal. However, there was attenuation when integrated with the gain stage. The filter was tested with fluorescent light as well. The selected gain stage was used in all tests for active filters

Passive Filter Design

Generally, passive filters are unpreferable due to power dissipation. However, the signal goes as high as 4V. Therefore, some dissipation can be afforded. The advantages of the passive network are easier controllability, faster and less wiring (less parasitic capacitance). The circuit consists of first order CR-RC network. The equations describing the passive network can be found in Appendix B.

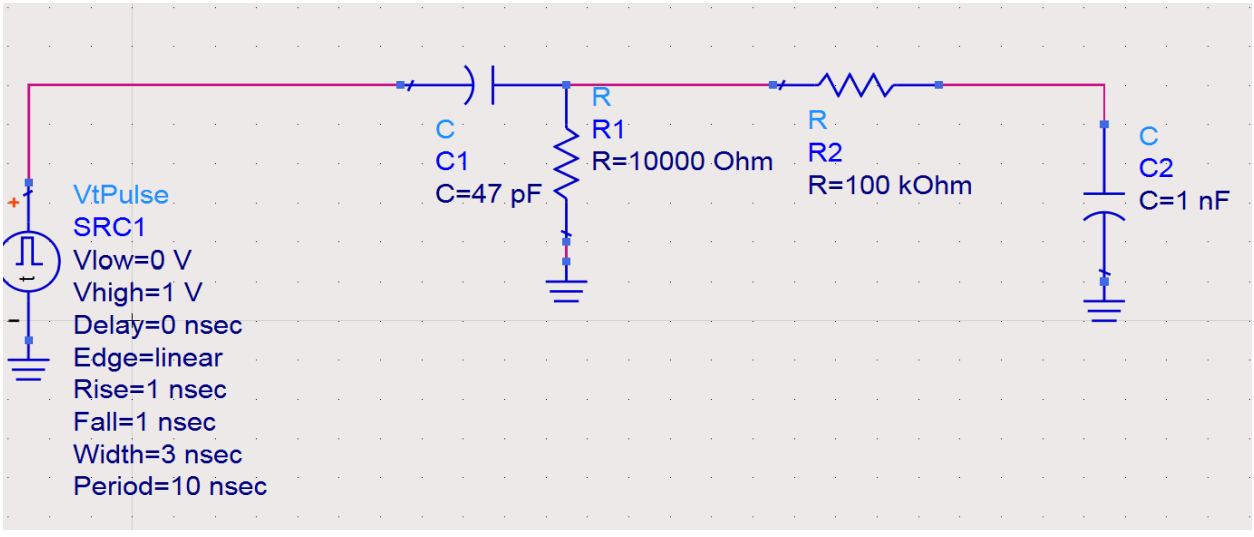


Fig 17: Circuit schematics of a passive CR-RC shaping network

Active CR-RC Shaper:

The same IC used in the gain stage along with the active filter were tested for an active CR-RC shaper. The requirements of the amplifiers are the same. The design equations are found in Appendix B.

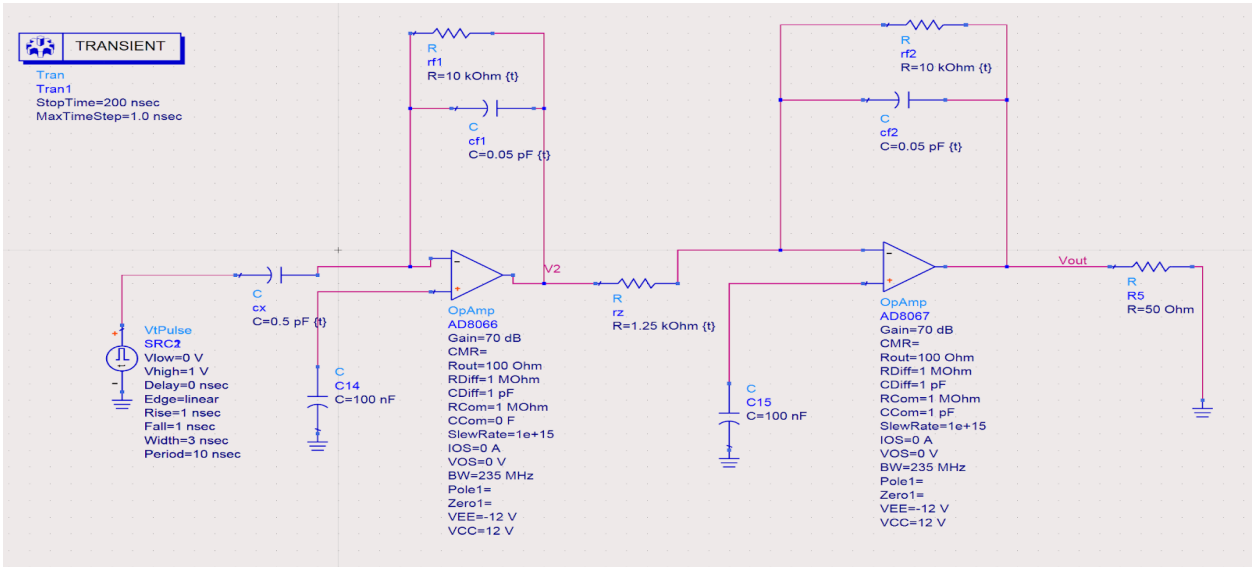


Fig 18: Schematics of active CR-RC filter

All the parameters were varied. Those that affect the shaping of the pulse are C_x, R_X and C_{f2}. Therefore, when testing, these values were varied as well to optimize the pulse. Testing was done directly with fluorescent light.

Integrating the Gain Stage and the Shaping Network

Based on the tests performed for gain stage and shaping network selection, simulations were performed for design analysis.

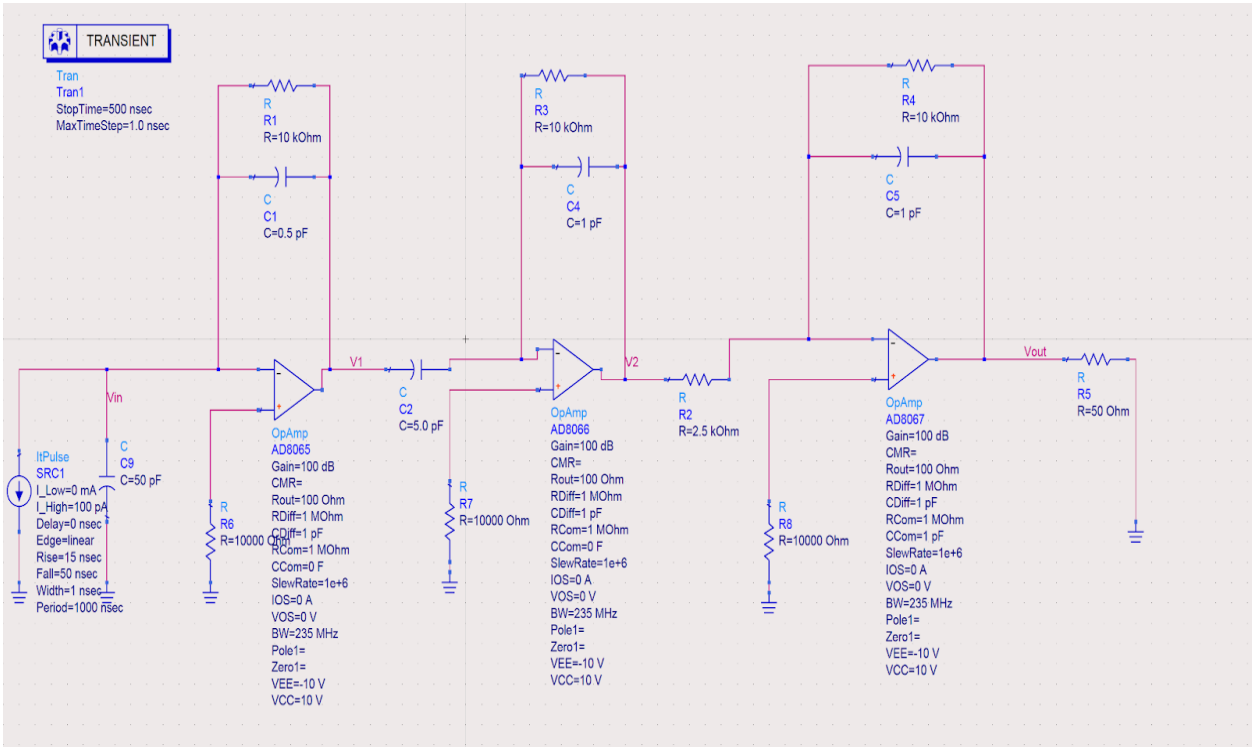


Fig 19: Schematics of the Energy FEE Selected

The circuit was tested with a 80 ns pulse with 50 mV amplitude. Additionally, it was tested with fluorescent light. Based on these tests, the parameters are chosen for an optimized signal.

3.3 Time Front-end Electronics Design and Implementation

Gain Stage

The gain stage design process of the timing branch is similar to the gain stage described in the previous stage. The only additional requirement is a short processing time. Therefore, a high-speed amplifier should be selected. The same amplifier setup was used for timing circuit.

Comparators Testing

To design a leading-edge discriminator, fast comparators are required. Simulations were performed to identify the slew-rate effects on the output. Based on the results, there were couple

of comparators acquired. Propagation time and delay time were also taking into consideration when selecting the comparators

Table 4: The ICs selected for LED discriminator

IC Model Number	Propagation Delay (ns)	Power Supply (V)
MAX9693EPE+	1.8	5
TL714CP	6	5
AD96687BQ	2.5	5

The comparators were tested with a DC supply providing a threshold of 1 V. they were compared to square wave for quality assurance.

LED Testing

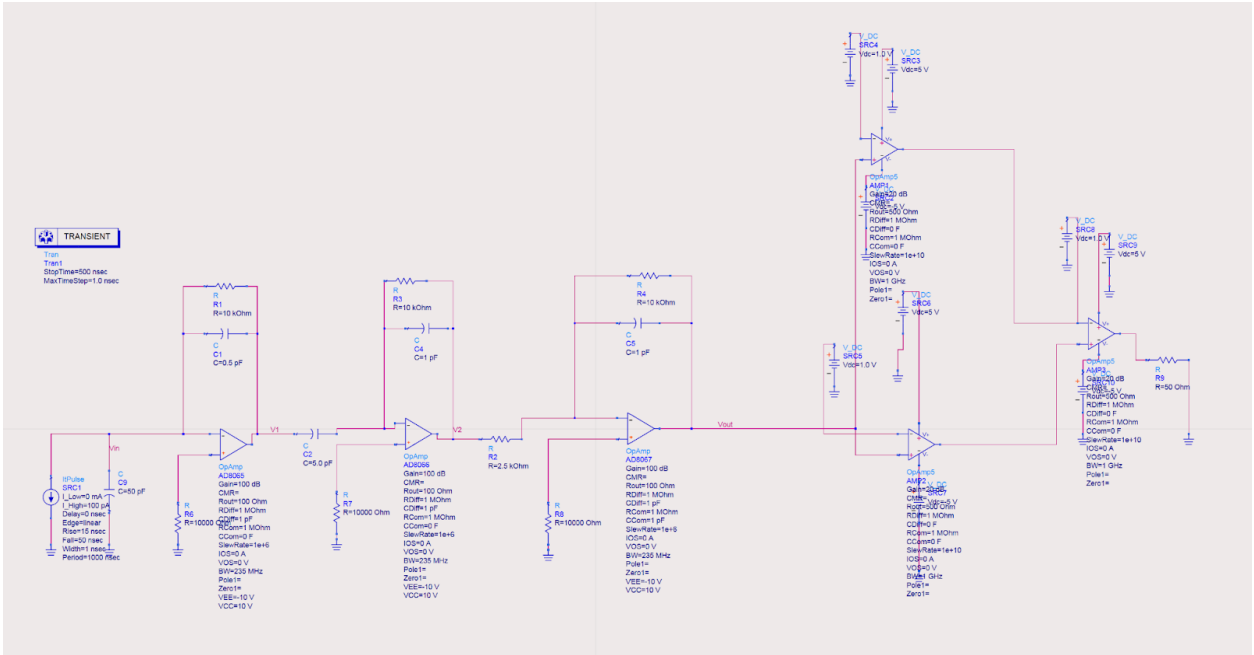


Fig 20: LED schematic

Testing the LED was performed based on the minimum timing pulse that the wave generator can provide. It had a 20 ns width. It had the rise of 10 ns. The values set for the upper threshold was 4.98 V. This was achieved using a voltage divider between a 2.2 k Ω AND 120 k Ω resistors that were connected to the positive rail of the power supply. The comparators selected were: AD96687BQ for High and low threshold comparisons and TL714CP for the output. The MAX9693EPE+ drew a lot of current in comparisons to the other ICs. The gain stage was the same used for energy branch. The only difference is the feedback capacitor was chosen to be 1 pF. The LED was tested with fluorescent light as well.

3.4 Radiation Source

To test the final design of the FEE, a radiation source was aquired from the MPU at the JGH. It was a 90 Stronium.

Fig 21: The radiation Source

A safety protocol was followed. The detector was exposed to the radiation for less than a minute. Noise signal was observed at the output.

Chapter 4: Results

4.1 Output of the photodetector

The pulse from the photodetector has an amplitude of 5 mV with a rise time of 15-20 ns. It decays over a time of 30 ns approximately

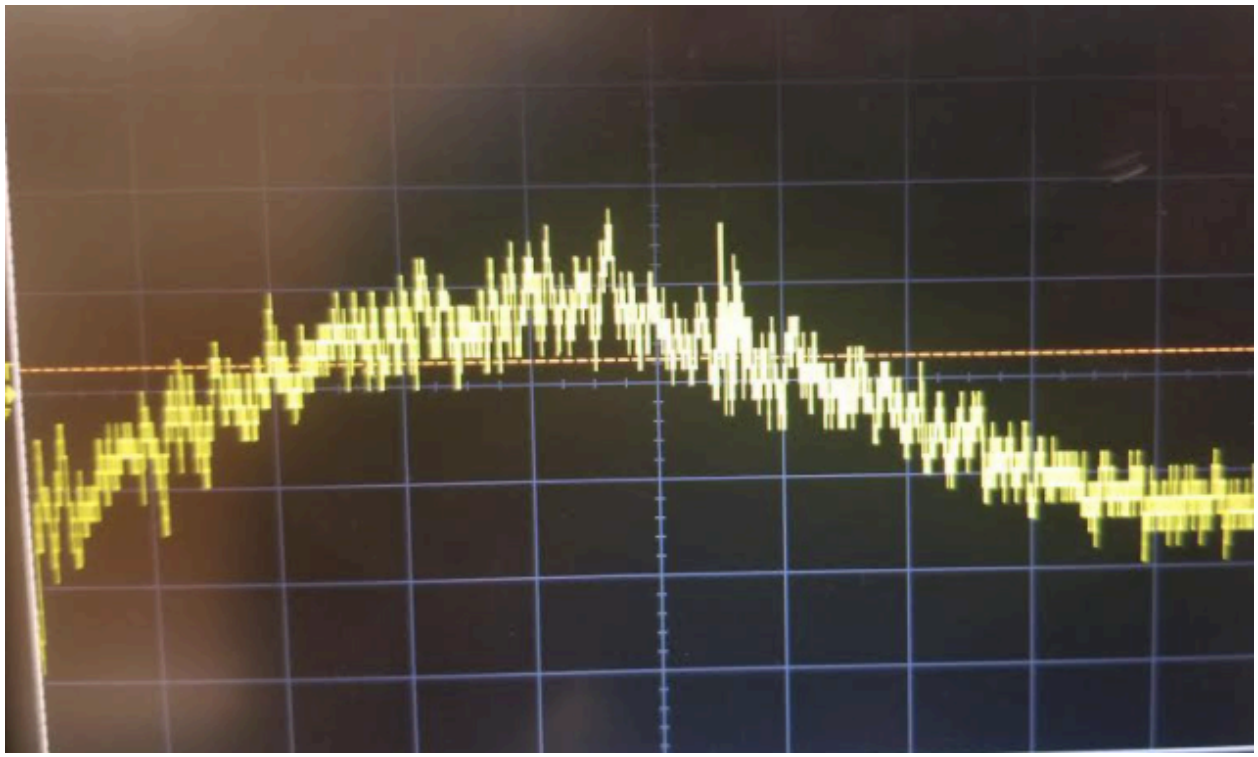


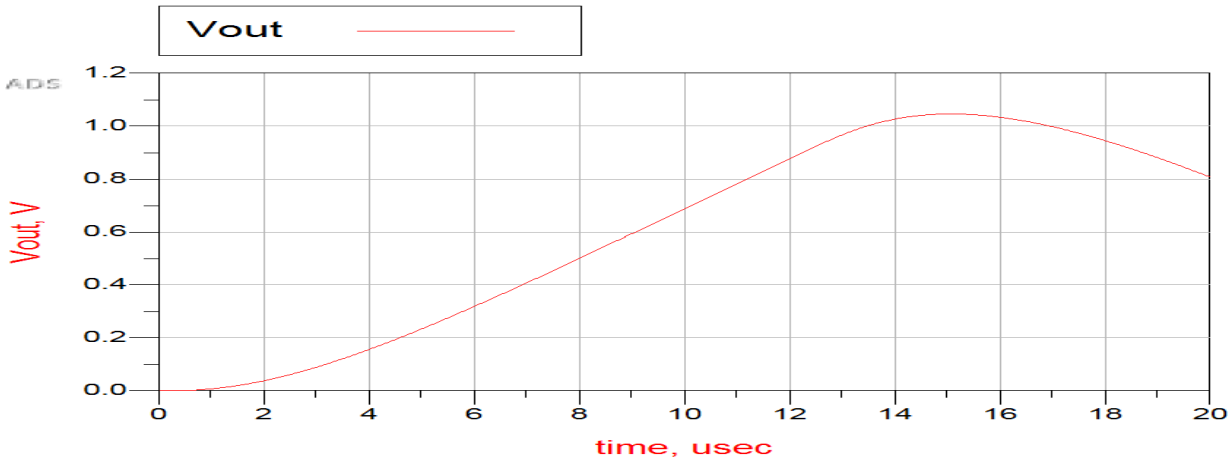
Fig 22: The input signal from the photodetector when light is conducted at 20 ns/div

The values measured across a 500 Ω resistor were:

Maximum Signal (47 mV)	**Current (μA)**	**Minimal Pulse (mV)**	**Noise Level (mV)**
47	94	8	5

4.1 Energy Measurement FEE

Two circuit Design:



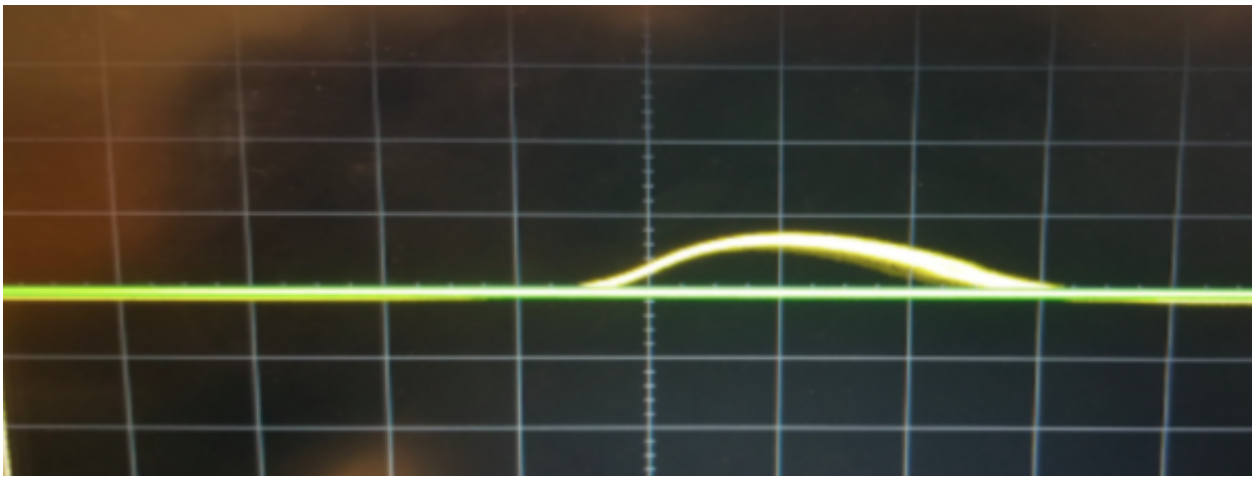


Fig 23: Simulation results for the two amplifier circuits (upper) Output of the two-amplifiers gain stage when the photodetector is saturated with light at 840 ns/div with 1.8 V (lower)

One Circuit Design:

Table 5: The results obtained from the one circuit design using two different ICs

IC Name	Vout (V)	Rise Time (ns)	Pulse Duration (ns)	Cf (pF)	Rf (k Ω)	Gain (dB)	SNR (dB)	Dynamic range (dB)
AD0865	7.4	1600	2400	0.5	10	51.4	63.4	59.3
LF365	1.24	1000	3400	0.5	2.2	35	47	43

AD8065 was compared with LF365 is selected for the wideband circuit in a CSA configuration. The images of the results are shown below:

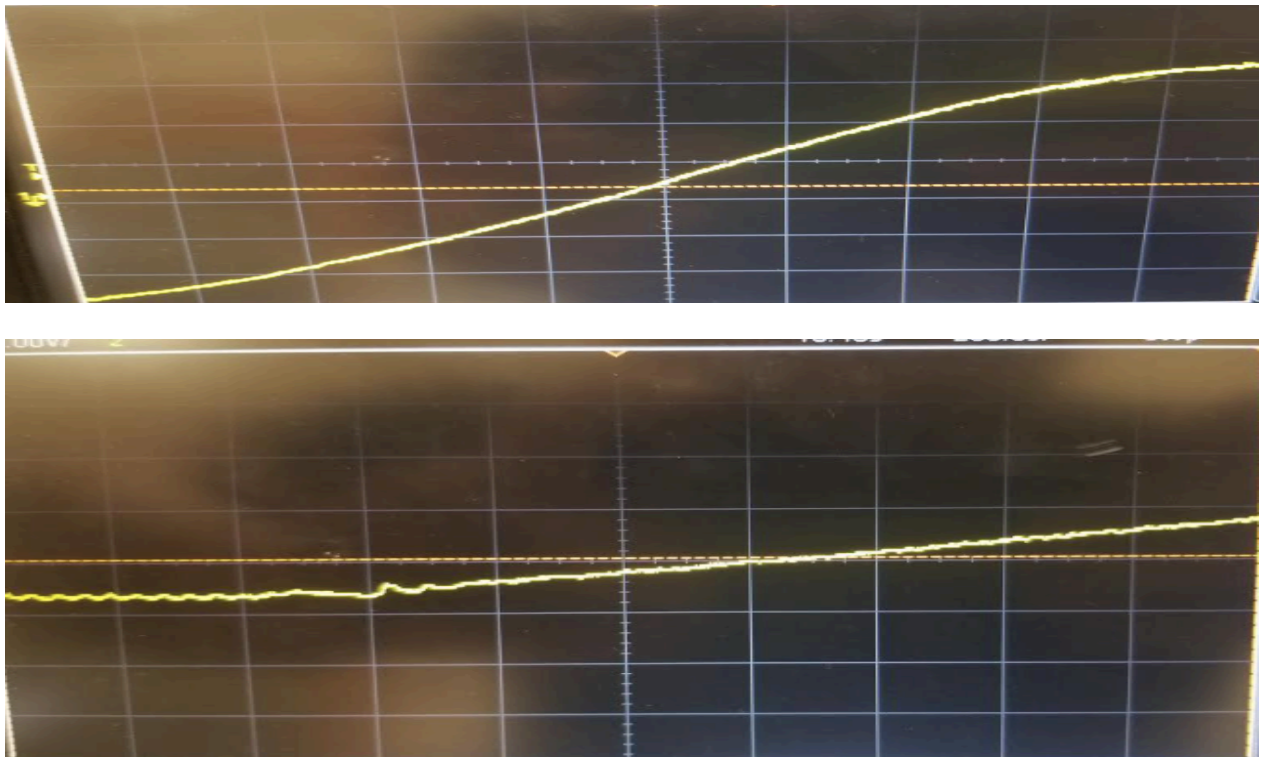


Fig 24: The output of LF351 (Upper graph) at 400 ns/div and AD8065 at 200 ns/div(Lower graph)

Shaping Network

As for the shaping network, both S-K and active CR-RC shapers were considered. However, attenuation was observed for S-K.

Table 6: The results of two different implementations of the shaper

	Output Voltage (V)	Rise Time (ns)	Decay time (ns)	Pulse duration (μs)
S-K	0.9	550	640	1.190
Active CR-RC	11.4	30	380	410

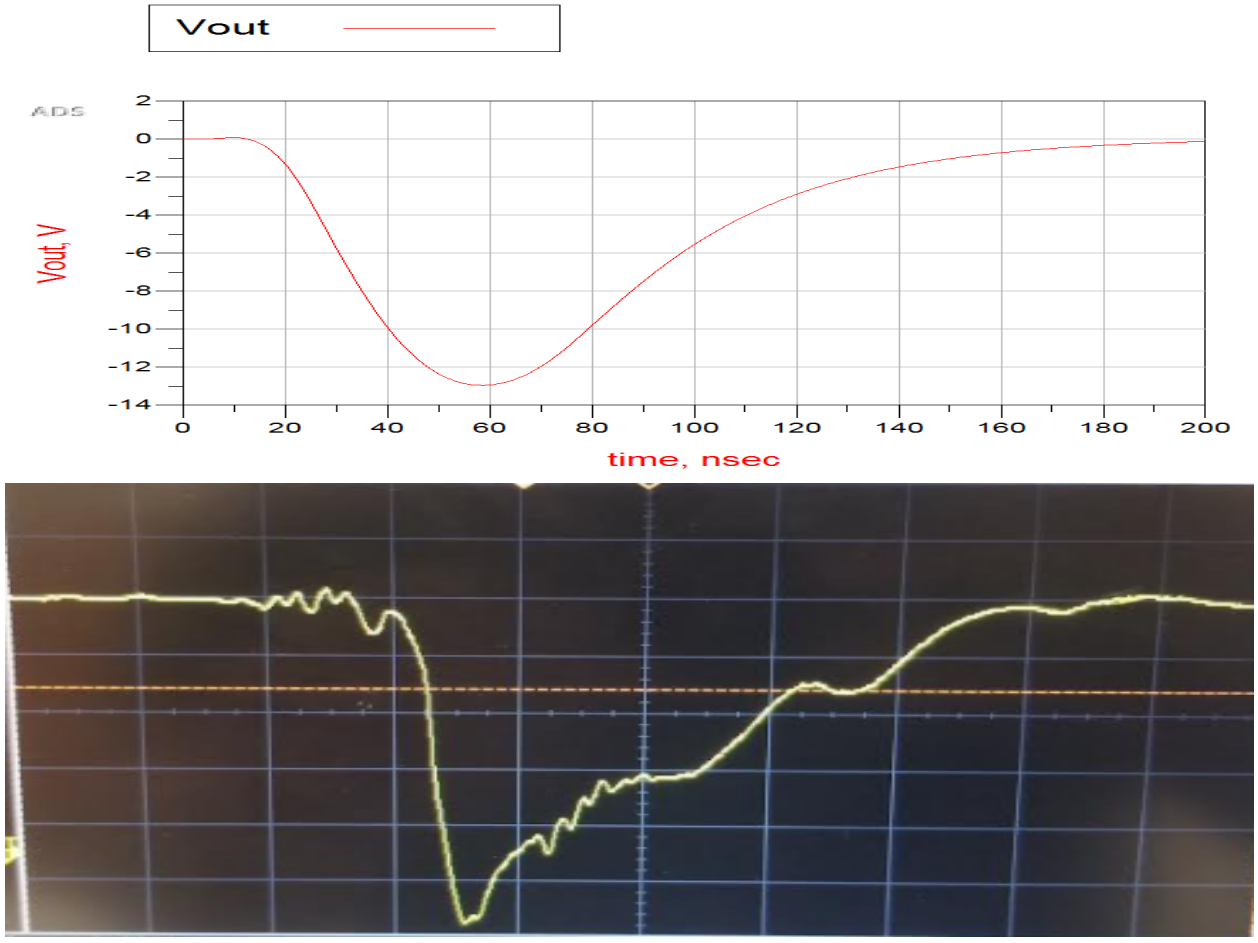


Fig 25: Simulations results for FEE energy branch (Upper)Energy FEE output A 11.4 Volts signal at 80 ns/division (lower)

The rise time of this signal is 35 ns and the decay is 250 ns.

Table 7: The final characteristics of the energy FEE

Gain	47.69 dB
Dynamic Range	63.07 dB
SNR	67.15 dB
Pulse Duration	280 ns
Rise Time	35 ns
Maximum Output	11.4 V
Power Consumption	104 mW

4.2 Timing Branch Results

The output of leading-edge discriminator based on a 20 ns pulse input with a 1V amplitude.

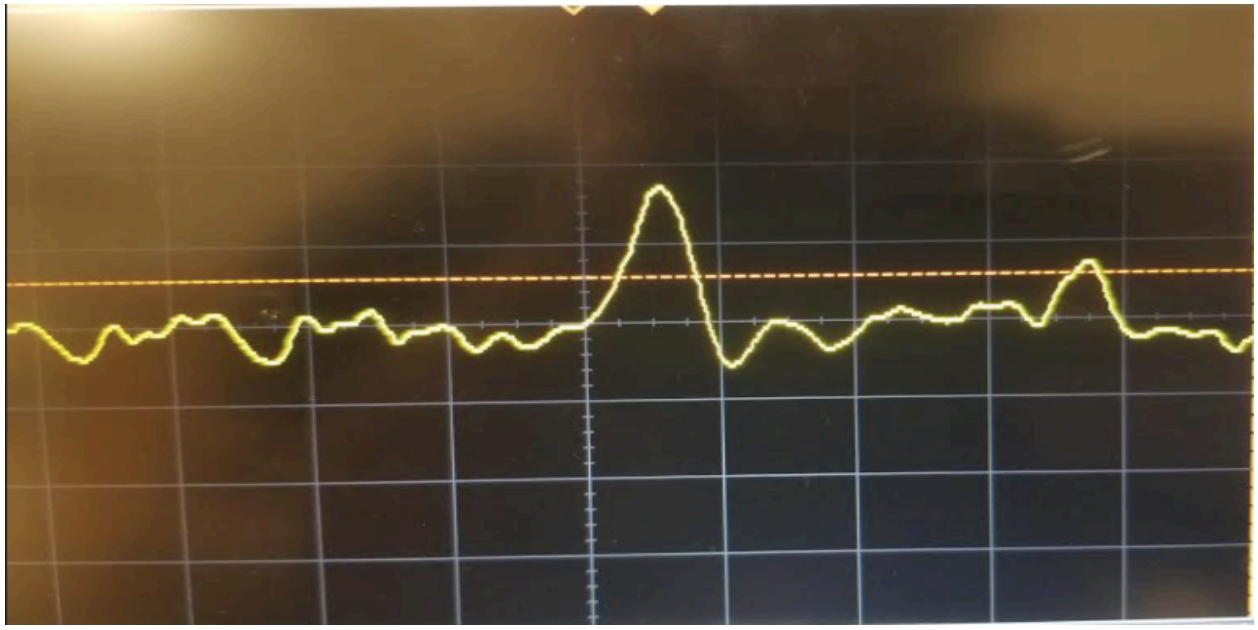


Fig 26: The output of the leading-edge discriminator at 20 ns/div with a 4.8 V

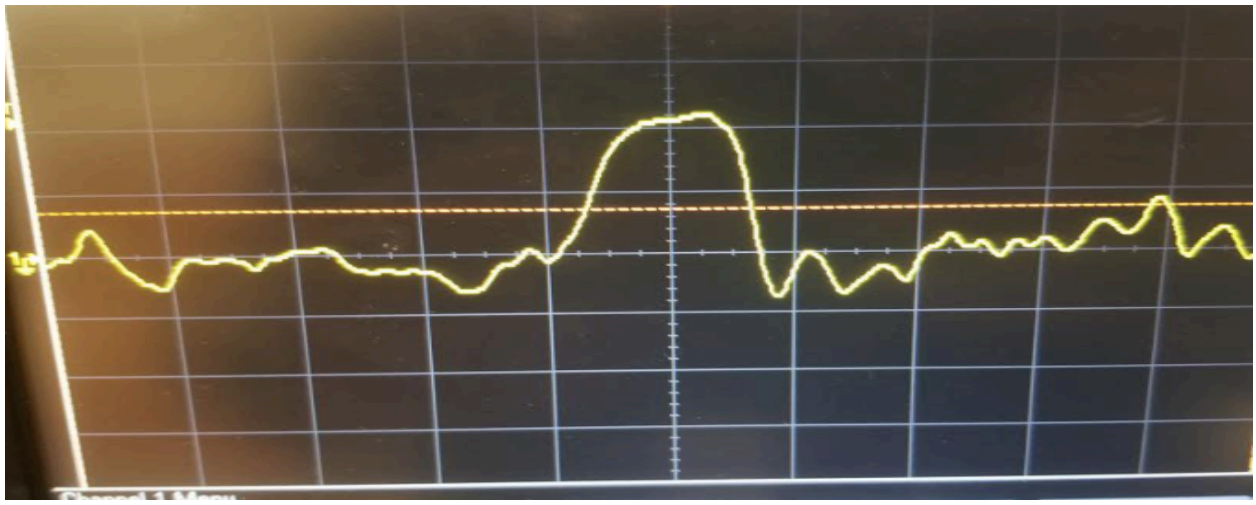


Fig 27: The output of the leading-edge discriminator at 20 ns/div at 4.8 V proceeded by the shaper

4.3 Radiation Detection :

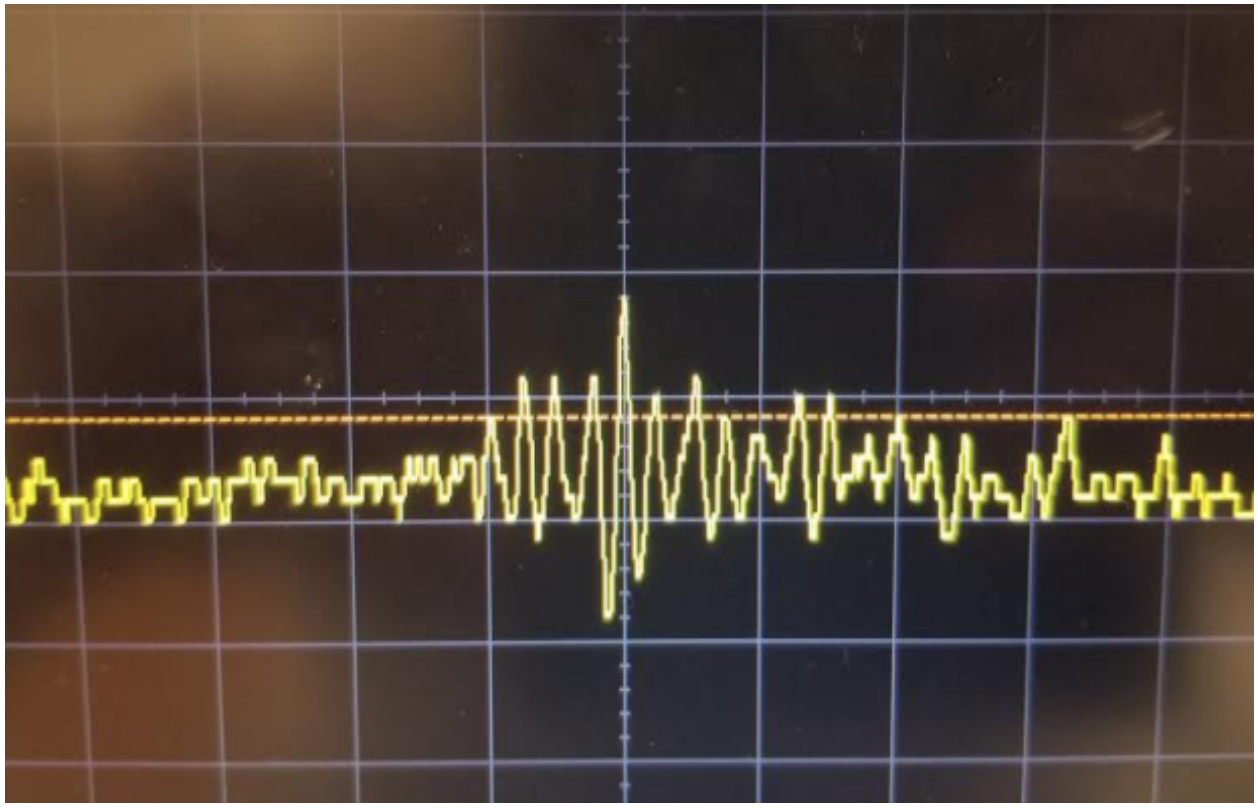


Fig 28 : Output of Energy FEE during radiation

Chapter 5: Discussion

5.1 Input Stage

The objective of the FEE is processing the pulse produced from the SiPM. The photodetector was placed inside a metal box and the slow output is connected to the circuit. The pulse produced had a peak of 47 mV and a noise floor measured of 5 mV which is regarded as the noise floor across 500 Ω. The minimum pulse was observed around 8 mV measured by allowing minimum fluorescent light at the scintillating fibers and was processed and amplified by the electronics. However, the noise remained an issue due to the distance traveled by the pulse to the circuit. In modern design, the detector's output is directly connected to the electronics. As mentioned in section 2.5, the thermal noise was proportional to resistance value. Having an additional cable adds noise to the signal. The electric model of a transmission cable has shown that resistance is significant for long coaxial cable. As observed in Fig 22, there were oscillations on top of the pulse reaching 2 mV peak-to-peak. Furthermore, multiple cable adapters were used at the input stge. SMA cable connected to the slow output of the photodetector. Next, a SMA to BNC adapter was used. The BNC coaxial cable connected to an additional breadboard adapter. At each stage, there was thermal noise addition. The second source of noise was the breadboard. It has been shown that the noise could reach as much as 25% of the signal using a breadboard. It was caused by the connections that were made up from a conductors which were shared for the same rows. It has contributed to the noise greatly since there was constant change from wire to conductor of breadboard. The third source of noise at the input was grounding. The BNC coaxial to wire adapter had an input to the breadboard and an output to ground. If the signal wasn't grounded properly, high oscillations were observed, and the pulse disappeared. Subsequently, the input's stage had to be isolated from the rest of connections to reduce interference. The input signal was connected to

compensation capacitor. The value of the capacitor depended on the amplifier selected. A 100 nF was selected. The input stage was very sensitive to the compensation capacitor. For instance, if capacitance of 1 nF was connected, the pulse wouldn't be process and the output was attenuated. This was caused by the combination of input impedance of amplifier and the feedback capacitance. Once the feedback capacitance and IC were varied, the compensation capacitance had to be adjusted accordingly. The input pulse reached a maximum of 20 mV. The rise and decay times were in accordance with the vendor's sheet.

5.2 Energy FEE

Charge Sensitive Amplifier

The CSA was implemented using a wideband amplifier. The output was expected to have a slower rising time than the input pulse and a longer decay. The parameters measured were gain, output's rise and decay times, pulse duration, dynamic range, SNR, and noise. The values were reported in table 5. As a result, the CSA was implemented using AD8065 IC. Two designs were considered for the CSA which consisted of either two amplifiers or a wideband amplifier. Initially, the IC used didn't provide a high gain. Therefore, adding an instrumentation amplifier was considered. From Fig 23, the simulations demonstrated a longer pulse duration than the value obtained for the two-amplifier implementation. Afterwards, the simulations have demonstrated that for a large gain bandwidth, the gain is increased. Additionally, the designs mentioned in the literature used one amplifier for the CSA. Consequently, large bandwidth amplifiers were selected for testing. The results obtained from ADS showed that high gain could be achieved using a high bandwidth amplifier. As demonstrated in Fig 24, charge integration was achieved. Since 12 V DC power supply was used for the two amplifiers stage and 13 V for the wideband amplifier, clipping

considerations wasn't considered. An inverse relation was observed as well with respect to the feedback capacitance and output voltage. A low value capacitance (0.5 pF) was selected to provide a high gain. The feedback resistor was selected based on time constant and noise contribution to the output. If higher resistance was used, then the signal observed was distorted. There was an increase for fluctuations as well on the top of the signal if a larger resistance was used mainly for 100 k Ω – 1 M Ω. It adds thermal noise at the output of the signal. Thermal noise contribution was estimated to be 1384 e^- rms based on the model used in [52]. Power oscillations were removed by adding a 100 nF capacitors at every power supply's input. There was an incident during testing of the resistance at the non-inverting input where the wideband CSA was damaged due to high current withdrawn from the power supply. To ensure device's protection, a 10 k Ω resistor was used in series with a 100 nF capacitor at the non-inverting input limiting the current withdrawn. The articles mentioned is section 2.4 showed a variety of CSA designs. The designed CSA has lower noise than in Reference 32 by 9.4 dB in which they used the same amplifier (AD8066). However, instead of using a traditional feedback resistor, they used a reset network by placing a transistor connected to an analog comparator and an AND gate. This contributed to a higher pulse selection. Additionally, they constructed a PCB at which the excess noise was removed. Transmission cable was estimated to have a 1-100 pF of intrinsic capacitance and they used 47 pF feedback capacitor. The time traits of the pulse produced by the CSA mentioned in the article had a maximum of 5 μs. The CSA implemented for this project had a 2.4 μs duration. In the project, the design of fast electrical components without losing information about the pulse was selected. In the article, speed wasn't the objective. In [34], they have used a large feedback resistance of 500 M Ω with a very small capacitance of 0.9 pF. They achieved a gain of 67 V/V. Additionally, they have added an and operational amplifier (AD811) to further amplify the signal using a non-inverted amplification.

They designed pulse procession of 185 ns. For the implementation of the gain stage, the two amplifiers had a much lower performance then a wideband amplifier. There were trade-offs for the values of the parameters such as: speed vs. gain, SNR vs. faster decay time. The optimization process for the gain stage designed relied mostly on gain. Noise was inevitable on a breadboard with a long signal transmission cable. The limitations of the gain stage for this project were:

- Pulse duration: although the rise time of the output was fast, the pulse duration was long.
- Noise: since a wideband amplifier was used, noise produced at high frequencies due to the parasitic capacitance showed up on the signal. The fluctuation increased with the amount of light conducted onto the photodetector. For digital processing, this could potentially cause reading errors.

Shaper

To design the shaper, shortening the rise and decay time was the objective. The other requirement was increasing gain. Three different circuit implementations were considered. First, the passive CR-RC network. This was selected at first because the output of the CSA was high enough. Therefore, some attenuation was allowed. The bandwidth selected started at 50 kHz and ended at 10 MHz. This allowed the pulse to fully reach the peak in less than 100 ns. However, upon selecting the values of C1, C2 and R1, R2, a high attenuation was observed. The output of the CSA was 7.4 V. After it was processed by the passive filter, 6 V were lost and the signal was noisy as well. Fluctuations were observed. Therefore, an active filter was considered. The 2^{nd} order S-K filter provided control parameters and had less attenuation. Simulations had shown that pulse shaping with the frequencies mentioned above led to a 500 ns pulse. The ICs were purchased according to optimized parameters such as: bandwidth, gain and noise. A CR-RC active filters were considered as well. As seen in appendix B, there are direct relation between CSA equations

and CR-RC filters in the time domain. Additionally, they provided gain. Both designs were implemented and compared based on the output pulse produced. The CR-RC active filters had a superior characteristic than a S-K filter. This was mainly due to the use of AD8065 for active CR-RC. Additionally, the feedback loop's impedance at each stage was selected such that it was twice as higher as the CSA. The capacitance and resistance were selected to provide fast shaping time. The optimized parameters were selected to allow the pulse to have a fast rise time to the maximum peak. The design equations are provided in Appendix B. As a result, a signal was achieved with a 30 ns rise time and a 380 ns decay time using a pulse of 80 ns width. In [38], a second-order CR-RC active filter was designed for 70 ns rise time. It used a 10 pF as Cx. We have achieved a 30 ns rise time using a 5 pF Cx. The ICs differed. The total pulse duration was around 1.1 μs.

Couple of difficulties were experienced when designing the shaper. First, the integration of the gain stage and the shaper stage required noise optimization due to the additional noise coming from ground and resistors. Therefore, the value of Rx selected was kept low (2.5 K Ω). Second, as seen from Fig. 25, there were fluctuations. The signal wasn't smooth. That's mainly due to the amplified noise observed in both the input signal (Fig.22) and the output of the wideband CSA (Fig. 24). This can be removed by making the wires shorter. However, that would lead to the interference of the signal from different devices on the breadboard. Third, all the devices were powered with 13 V DC. The signal obtained reached 11.4 V. This could cause clipping and some of the energy information of the pulse can be lost. Lastly, the signal was inverted. Consequently, an additional inverter might be needed depending on the ADC used.

5.3 Time discrimination

The design considerations for an LED were propagation delay and providing a voltage discrimination based on the output obtained from the CSA for a time over threshold (ToT) method. First, the electric pulse was used as an input to the setup to optimize the threshold voltage and delay line. The comparators used operated at 5 V. Therefore, the results obtained at 4.8 V up to 5 V meant a logic HIGH. It performed a discriminator functionality. Nevertheless, there were certain issues caused by noise. A 4.98 V, using a voltage divider between 120 k Ω and 2.2 k Ω, was selected to obtain a high value for the threshold such that it's above noise and fluctuations. From Fig 25, we expected the logical pulse to last 200 ns because the pulse was above 4.98 V for that amount of time. However, it lasted 40 ns instead due to the lack of comparator hysteresis. As observed in Fig 27, the pulse was high for 40 ns seconds. But there were additional pulses followed by the logical pulse around 2 V. There was a continuous HIGH and LOW switching due to the oscillations on top of the signal. To solve this issue, a high voltage threshold is required along with signal smoothing by designing a high order $(CR\text{-}RC)^n$ for a better quality factor. The same issue was raised when an electrical input was used. Pulse was very noisy. The noise floor increased due the lower voltage limit. It was compared to ground. On a breadboard, ground was connected to the DC power supply. Even though capacitance was used to eliminate the oscillations, noise was still high from the power supply. The threshold voltage couldn't be increased because 5 V was the maximum. An additional DC supply could've been used to test the discriminator with a high voltage at the threshold. By comparison, the discriminator designed in [47], LED had a timing resolution of 4.6 ns. The width of the time window was achieved using a digital rest configuration. This was a possibility that could've been exploited in this project using Q flip-flops in a FPGA board for example. Nevertheless, this might have produced more noise and the time window would

affect the time resolution even more. In [48], the AD96687 was used for LED. They achieved a 4 ns time resolution. They've used an MC10131 flip flop for setting a modulated time window to capture the pulse. It should be noted that the input was obtained from a PMT which may have variable noise characteristics. Additionally, a PCB was used for the design. The discriminator designed for SiPM has noise limitations. These can be removed by using voltage regulators for the power input and PCB to lower resistance/capacitance in the design. The time resolution should be improved for a TOF application.

5.4 FEE Limitations

A prototype of energy processing FEE for SiPM was developed the characteristics mentioned in Table 7 demonstrated a charge integration and pulse shaping. The FEE designed was meant to be used in peak sensing measurements where the peak indicates the amount of energy deposited in the detector. There was a linear relation between the light intensity and the output of the FEE. The FEE has succeeded in amplification, pulse shaping and time discrimination. For this specific SiPM setup, the signal was noisy due to the current electronics setup. Nevertheless, energy discrimination could be observed in variation with the intensity of the light. The results showed that the maximum of the signal was attained when the photodetector was saturated. In comparison with the previous electronics used, the pulse reached a 10 V when the detector was saturated. Furthermore, the pulse had a rising time of 10 ns and a decay time of 50 ns. It used a 15 V DC supply with a total current withdrawn of 103 mA. For this prototype, the signal reached 11.4 V with a rising time of 35 ns, while the decay time was longer (250 ns). However, 13 V were used with a total current of 8 mA. For a clinical setup, power usage is important. If a transportable device is desired, then a battery of 5 or 9 V can be used to power the electronics. Therefore, using

a lower voltage was preferrable. The timing characteristics, in comparison with the older setup, were lower. The constant fraction discriminator (CFD) had a time resolution of 1.6 ns. For the LED designed, the best time resolution achieved was 20 ns. For TOF purposes, a 100 ps time resolution is desired. As in comparison with Table 1, the FEE mentioned were designed for different types of detectors. The electrical components used were similar. They all consisted of a CSA, semi-gaussian shaper, and a time discriminator. The parameters desired were similar as well. For [25], [26], and [28], they obtained a high output. Subsequently, they didn't consider SNR measurements. For this project, a better FEE can be implemented on a PCB to lower noise (thermal, flicker and shot). Additionally, the input stage must be close to the CSA so that no transmission cable impedance affects the pulse generated. As expected, the FEE couldn't process the signal produced from radiation of Sr90 radiation source due to low pulses detection. Fig 28 demonstrated the noise produced at the output during radiation. It peaked around 26 mV. The pulse produced at the input was lower than 8 mV which is the minimal detectable signal. Therefore, the FEE wouldn't process the signal. There are couple of methods to fix this issue with regards to the prototype:

- Lowering the noise at the input stage which lead to lower detectable signal. This can be done by minimizing the distance from the detector to the FEE
- PCB implementation leads to less noise at the conductors which minimize cables
- Optimization on parameters such that pulse with low peaks falls within the bandwidth of the system which means component with higher bandwidth

5.5 Future Works

The FEE had many limitations including time resolution, noise increase, and weak radiation detection. The new version of the detector has to use fewer passive components. Instead, digital components have to be implemented for signal control. The FEE should be mounted on a PCB. Additionally, the power used for the circuit shouldn't exceed 9 V for a practical clinical setting implementation. The timing characteristics can be further improved by using comparators with shorter delay time. As shown in LED section, similar components were used that led to high time resolution due to the usage of active components on PCB. Perhaps a CFD followed by a TDC. The timing resolution for the new design must use comparators with less than a 100 ps time delay. Furthermore, the distance between the input stage and the gain stage must be shortened. A filter with higher quality factor will lead to a smoother signal. This can be achieved with a higher-order filters. For this application, a filter with 3^{rd} order will lead to smoother signal The prototype has demonstrated the possibility of capturing a signal and process it. However, a PCB will lead to a better performance.

Chapter 6: Conclusion

In this thesis, a summary of the building blocks of analog FEE for radiation detectors was covered along with a brief explanation of the mechanism of PET scan, dynamic imaging, AIF and TOF. The detector was aimed to be used for dynamic imaging using the TOF to obtain the AIF. A prototype of analog of-the-shelf electronics were designed in comparison to the previous expensive components used for the detector. It consisted of two separate circuits that perform different functions. The first was designed for peak sensing method that distinguish the energy of the particle detected based on the peak of the pulse. It had a CSA followed by a shaping network. Different designs were considered and compared such as: CSA followed by an instrumentation amplifier, a wideband amplifier. As for the filter, passive and active CR-RC were considered along with a 2^{nd} order S-K. The final design obtained was a wideband with a CR-RC active shaper. It achieved a gain of 61.3 dB with a 35 ns rise time. Parameters' optimization was examined based on simulations and testing. Fluorescent light was used as input along with an electrical pulse produced by a wave generator. The second branch determined the time of the pulse to be counted as a detected event. A LED was developed based on the signal received from a CSA and a CR-RC shaper. It was able to produce a logical pulse for 40 ns based on the rise and fall times of the signal between 4.98 V. Additionally, the discriminator was tested with a 20 ns pulse from the wave generator. Further for a new version of the FEE will be made. This includes a high time resolution of the LED and perhaps the development of TDC. Furthermore, this could possibly reach a 100 ps time resolution which would make the discriminator performance suitable for TOF. A PCB will be developed to minimize noise and to obtain a higher quality signal. For instance, it will lower the distance between the SiPM and FEE. For a clinical setup, an ASIC should be designed as well with a 9V battery. A microprocessor should be added in the ASIC to obtain the data quickly. A

mountable FPGA will be considered for the new design. To conclude, the circuit has demonstrated the appropriate functionality of a FEE with some limitations such as: noise, weak radiation detection and low time resolution relative to TOF application.

Chapter 7: Bibliography

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Chapter 8: Appendices

CSA Design Equations [53,54,55]

The ideal input to a CSA:

$$I_{in} = Q_{in}\delta(t)$$

The ideal output of a CSA:

$$V_{out} = \frac{1}{C_f}\int \delta(t)i(t)dt$$

$$V_{out} \sim \frac{Q_{in}}{C_f}u(t)$$

SiPM output current:

$$I_d(t) = \frac{Q_d}{\tau_r}e^{\frac{-t}{\tau_r}} = \frac{\Delta V}{R_q}\frac{C_d}{C_d + C_q}e^{\frac{-t}{\tau_r}}$$

Closed-loop gain of CSA:

$$G = \frac{A}{1 + A\beta} = \frac{-v_o}{v_{in}}$$

Where $\beta = \frac{Z_D}{Z_D + Z_f}$

Maximum amplitude of the CSA:

$$V_{peak} = i_d R_F(1 - e^{-\frac{t_d}{R_f C_f}})$$

Gain band with equation

$$\omega_F = GBW \frac{C_f}{C_{eq} + C_f}$$

Appendix B

Passive CR-RC Design Equations

High-pass passive and low-pass RC filter's cut-off frequency:

$$f_c = \frac{1}{2\pi RC}$$

S-K Filter Design Equations:

S-K Transfer Function in s-domain:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{R_1 C_1 R_2 C_2}}{s^2 + s\left(\frac{1}{C_2 R_2} + \frac{1}{C_1 R_1}\right) + \frac{1}{C_1 R_1 C_2 R_2}}$$

Cut-off frequency:

$$f_c = \frac{1}{2\pi\sqrt{C_2 R_2 C_1 R_1}}$$

Quality factor:

$$Q = \frac{\sqrt{C_2 C_1 R_2 R_1}}{C_2(R_1 + R_2)}$$

Active CR-RC Design Equations

$$V_{out}(s) = \frac{Q_{in}}{sC_f} sC_z \frac{R_1 R_2}{R_c} \frac{1}{(1+s\tau)^2} = Q_{in} \frac{C_z}{C_f} \frac{R_1 R_2}{R_c} \frac{1}{(1+\tau s)^2}$$

$$V_{out}(t) = Q_{in} \frac{C_x}{C_f} R_1 \frac{R_c}{R_2} \frac{1}{\tau} (\frac{t}{\tau}) e^{\frac{-t}{\tau}}$$

Where, $\tau = C_1 R_1 = C_2 R_2$

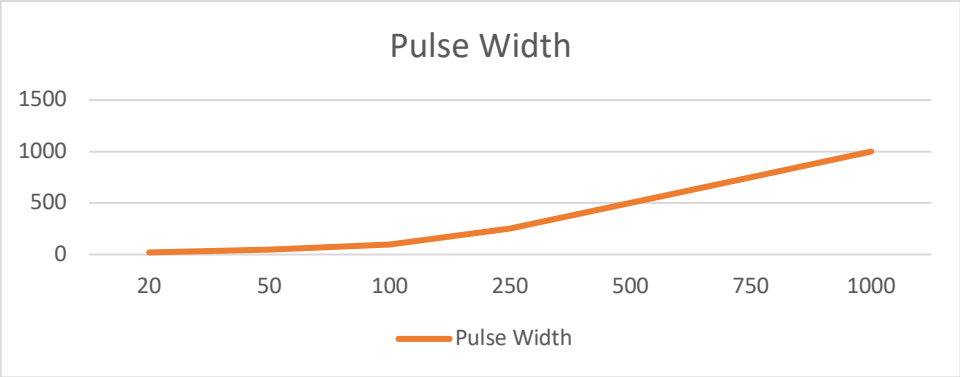
Time Relation of CR-RC shapers:

$$\frac{C_z}{C_1} \frac{R_2}{R_x} = ne$$

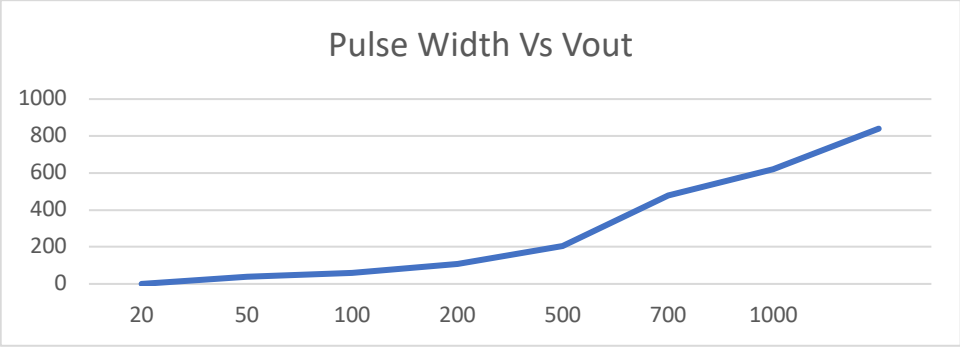
Where e is the chare pulse captured

Appendix C

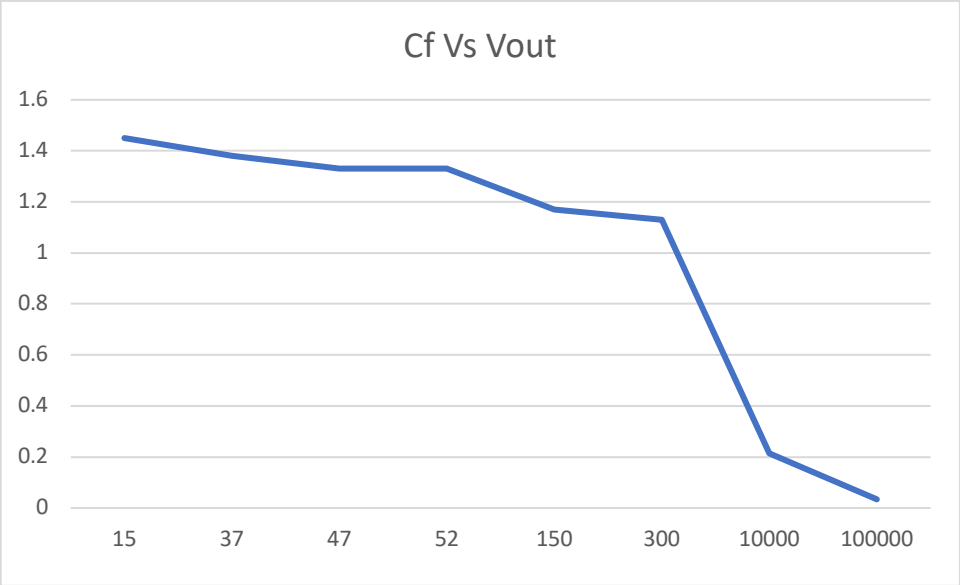
Raw Data Obtained for Design Considerations



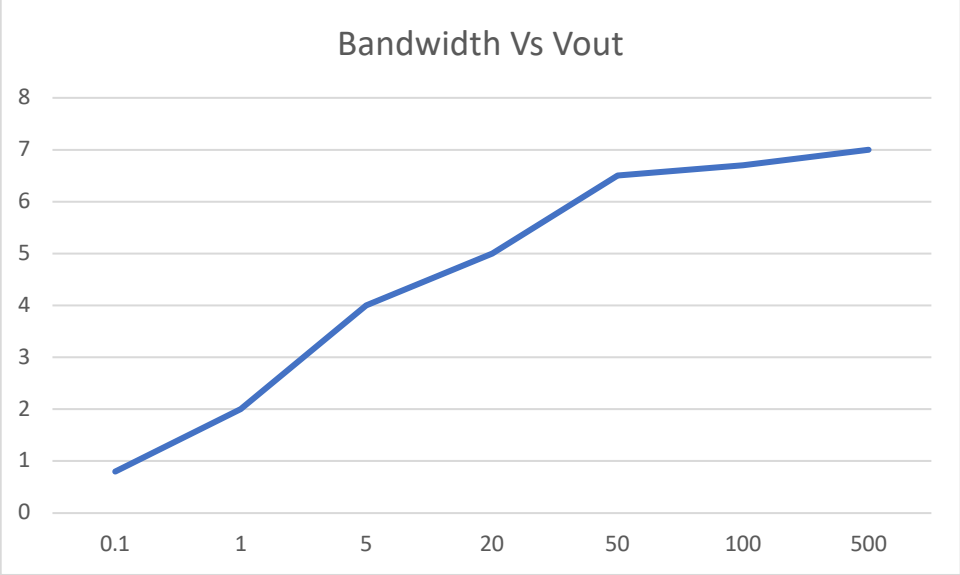
AD8065 response to an electrical pulse with different width



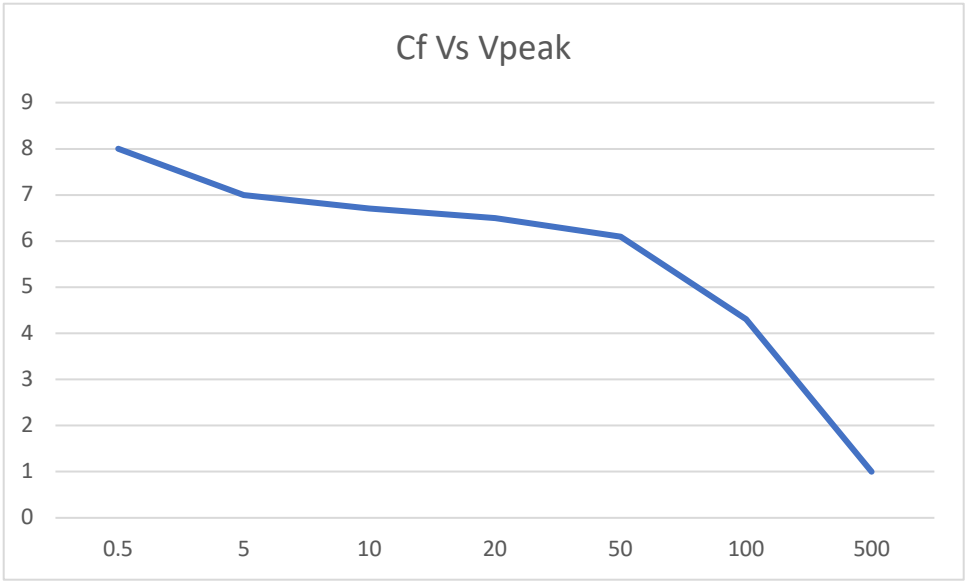
LF365 response to an electrical pulse with different width



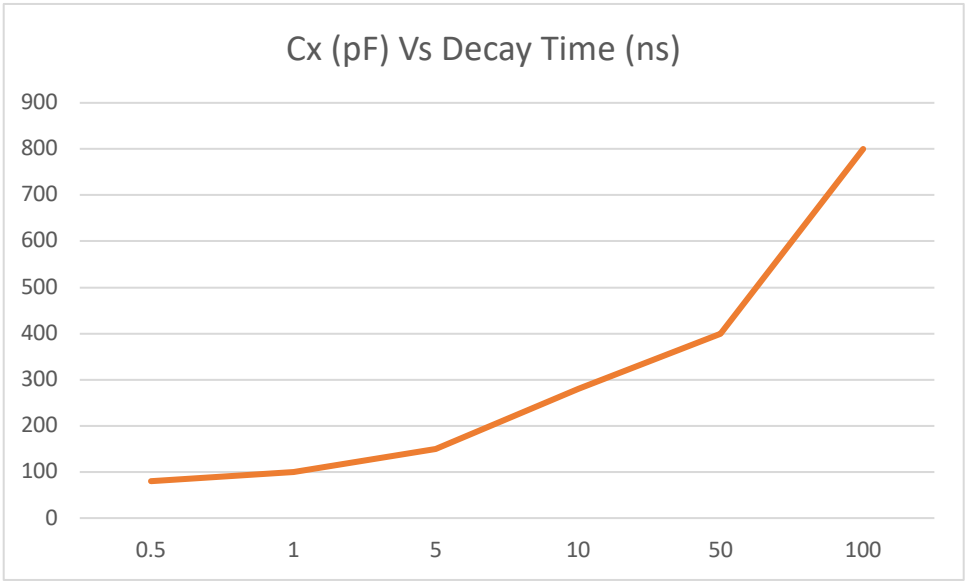
Measured output variation using light as an input with load resistor of 10 k



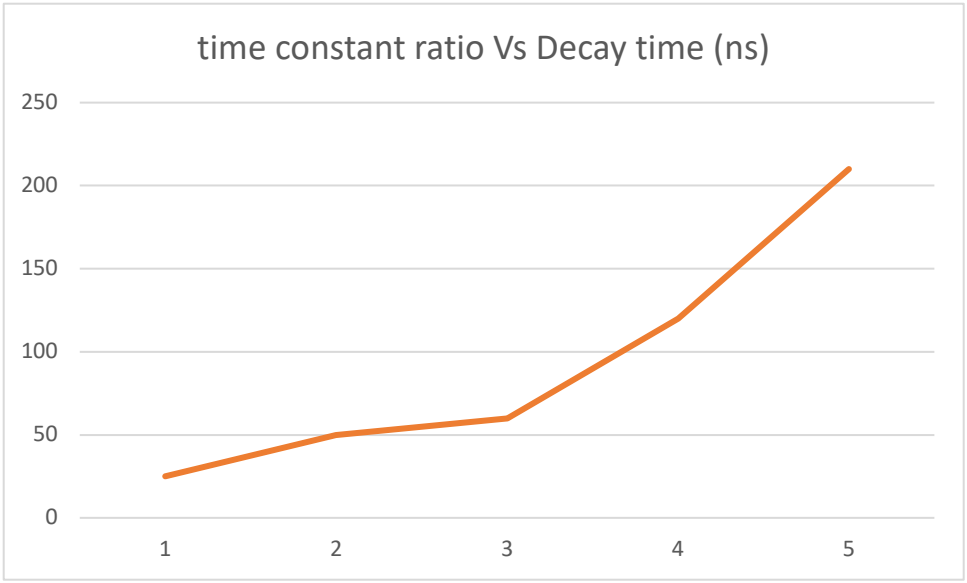
Values obtained from simulations of the CSA bandwidth variations vs the output of FEE of energy



Values obtained from simulations of feedback capacitance variations vs the output of FEE of energy



Values obtained from simulations of active CR-RC capacitance variations vs the output of FEE of energy



Simulated variation of ratio of time constants of CSA and CR-RC active filter vs decay time of the pulse