Analysis of Modern Power Distribution Networks

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LIST OF ABBREVIATIONS

1-D	One-Dimensional
2-D	Two-Dimensional
3-D	Three-Dimensional
ADC	Analog to Digital Converter
ADS	Advanced Design System
AI-EBG	Alternating Impedance Electromagnetic Band-Gap
BGA	Ball-Grid Array
BER	Bit Error Rate
CAD	Computer Aided Design
cm	Centimetre(s)
CMOS	Complementary Metal–Oxide–Semiconductor
CPU	Central Processing Unit
DC	Direct Current
DDR	Double Data Rate
EM	ElectroMagnetic
HFSS	High Frequency Structure Simulator
HIS	High-Impedance Surface
IC	Integrated Circuit
I/O	Input/Output
EBG	Electromagnetic Band-Gap
EMI	ElectroMagnetic Interference
FDTD	Finite-Difference Time-Domain
FEM	Finite elements Method
FIT	Finite Integration Technique
FPGA	Field Programmable Gate Array
GSM	Global System for Mobile communications
MoM	Method of Moments
mm	Millimetre(s)

PCB	Printed Circuit Board
PDN	Power Distribution Network/Power Delivery Network
PEC	Perfect Electric Conductor
PMC	Perfect Magnetic Conductor
PML	Perfect Matched Layer
PPW	Parallel-Plate Waveguide
PCML	Pseudo Curent Mode Logic
PRBS	Pseudo Random Bit Sequence
RAM	Random-Access Memory
RF	Radio Frequency
RTL	Radial Transmission Line
SIP	System-In-Package
SMA	SubMiniature version A
S/N	Signal to Noise ratio
SOP	System-On-Package
SPICE	Simulation Program with Integrated Circuit Emphasis
SSN	Simultaneous Switching Noise
TDR	Time-Domain Reflector
TEM	Transverse ElectroMagnetic
UC-PBG	Uniplanar Compact Photonic-Band-Gap
VNA	Vector Network Analyzer
VRM	Voltage Regulator Module

ABSTRACT

Analysis and proper design of power distribution networks (PDNs) are critical steps in developing modern electronic systems. Parallel-plate structures with vias are the core components of PDN configuration at any scale of system implementation from chip to package and printed circuit board. Voltage fluctuations induced by vias with carrying time-varying currents are interpreted as power/ground noise. In this thesis, this type of noise is quantified by two fast prediction methods, i.e. using radial transmission line theory and resonant cavity analysis. A number PDN structures containing single or multiple parallel-plates and vias are simulated using the developed analytical models. These models are portable to the commercial circuit simulators, provide a fast means of PDN analysis and enable global system simulations. Suppression of power/ground noise by using discrete decoupling capacitors and differential signalling is investigated using the developed models. The validity of the models is tested against full-wave simulations and prototype measurements. Improvement of power integrity is also studied by using a uniplanar EBG structure in a parallel-plate stack-up. The main challenge in employing EBG structures in compact low frequency designs is the relatively large footprint of the EBG unit cell. This thesis reviews two techniques for miniaturization of a uniplanar EBG and demonstrates their efficacy through full-wave simulations.

ABRÉGÉ

L'analyse et la conception appropriée du réseau de distribution d'énergie (RDE) sont des étapes critiques lors du développement de systèmes électoniques modernes. La composante principale d'un RDE est une structure de plaques parallèles avec *vias*, et ce à toutes les étapes de l'implémentation, du désign circuit à la carte imprimée. Les fluctuations du voltage induites par le courant variable qui transite par les vias sont typiquement interprétées comme du bruit sur la source de tension ou la mise à la terre. Dans la présente thèse, ce type de bruit est quantifié à l'aide de deux méthodes rapides de prédiction. Celles-ci sont la théorie radiale des lignes de transmissions ainsi que l'analyse des cavités résonnantes. Plusieurs structures RDE contenant une ou plusieurs plaques parallèles combinées à des vias sont simulées à l'aide des modèles analytiques présentés. Ces modèles sont facilement transférables vers des simulateurs de circuits commerciaux, ce qui fournit un moyen rapide d'effectuer l'analyse du RDE dans une simulation globale. Nous analysons également la suppression de bruit de source/mise à la terre effectuée à l'aide de condensateurs discrets de découplage ou à l'aide de signalement différentiel. Les modèles sont validés par comparaison avec des simulations à onde complète et des mesures sur prototype. Nous étudions les améliorations à l'intégrité de la source de puissance à l'aide de structure EBG dans un empilage de plaques parallèles. Le défi principal relié à l'emploi de structures EBG dans un désign compact et basse fréquence est dû à la grande taille des unités EBG. Nous passons en revue deux techniques pour miniaturiser un EBG uniplanaire et démontrons leur efficacité à l'aide de simulation à onde complète.

Chapter 1 Introduction

1.1 Overview

Power supply delivery network is an indispensable part in any electronic system design. However, in the earlier low frequency systems, these supply networks were rarely designed and analyzed dedicatedly except for calculation of their current handling capacity. Since the 1960's, the power delivery or distribution network (PDN) has grown from an almost non-significant part to a very important subsystem [1]. With the dramatic evolution of device fabrication technologies in the past couple of decades, operating frequencies of electronic systems have crept into millimetre-wave range and switching times of digital devices have reduced to 10s of picoseconds. The supply voltages have reduced consistently and chip, package and board layouts and input/output (I/O) pins have become much denser throughout these years. Distribution of reference voltages to sometimes millions of circuits is a major challenge in present-day electronic system design. With gigabit signal rates being processed in highly integrated packages and boards, the ability to supply clean power/ground voltages to the circuits becomes very critical [2]. Therefore, in the past ten years a new field of study known as power integrity has emerged, which deals with integrity evaluations and analysis of power delivery system.

Power/ground noise is one of the performance-limiting factors in modern high-speed digital, analog and mixed-signal circuits that has become even more significant in recent years. This noise is excited when a time-varying current like

the switching current passes through the PDN [3]. As devices scale down and more transistors are integrated into a single chip, millions of transistors induce the switching noise to the PDN. This phenomenon is known as simultaneous switching noise (SSN), which is one of the causes for failure of digital systems when it is not accounted for at the design and simulation stage [4]. To alleviate the problems due to power/ground noise, efficient methods for PDN simulations and engineering should be investigated. This objective constitutes the rationale behind this thesis.

1.2 Thesis Rationale and Objectives

In order to investigate voltage fluctuations interpreted as noise in a PDN, the physical structure of the PDN should be modeled and analyzed. Since modern electronic systems have become very complicated, cost-effective, fast and accurate modeling techniques are needed to enable simulation and engineering of the PDN structure before system implementation. The increasing operating frequencies and data rates of modern electronic systems necessitate modeling of the PDN as a distributed component rather than a lumped element. Full-wave methods can be used to simulate PDN's performance like any other distributed circuit component and predict the power/ground noise very accurately; however, they often require excessive computational resources and can be very time consuming [1]. Therefore, developing fast simulation methods is very important for noise prediction in engineering practice. In this process, the structure of the

PDN is inspected to identify the core elements responsible for supporting and distributing the power/ground noise.

A multilayer conductor stack-up is a typical PDN structure in electronic systems and three dimensional (3-D) package designs. In this configuration, solid conductor plane pairs are used to distribute various reference voltages throughout the system. To interconnect signals and deliver ground and supply voltages, more and more vertical interconnects, i.e. vias, are employed that penetrate these power/ground planes.

If a basic PDN, which is composed of a pair of conductor planes to supply the power and ground voltages, is considered, it can be observed that, in fact, a parallel-plate waveguide (PPW) structure is configured [3]. Vias and any discontinuity in this geometry can excite PPW modes. A via with a time-varying current acts as an excitation source for the waveguide modes. The dominant propagating transverse electromagnetic (TEM) mode with a direct current (DC) cut-off frequency is potentially excited in any electronic application. Due to the cylindrical symmetry of the via, it can be seen that cylindrical waves are excited [3]. According to reference [3], [5]-[7], radial transmission line (RTL) theory can be used to represent this phenomenon. In another viewpoint, the PDN forms a PPW cavity with perfect magnetic conductor (PMC) sidewalls, which confines most of the unwanted electromagnetic (EM) energy excited by the vias in the PDN structure. Therefore, cavity models of PPW are also utilized to model parallel-plate PDNs and investigate power/ground noise [8]-[11]. Both the RTL and cavity modeling methods can dramatically reduce the simulation time and

enable global system simulations, as they can be integrated with other circuit components in the commercial circuit simulators.

Another aspect in PDN design and power integrity analysis is implementation and evaluation of methods for suppression of power/ground noise. In this thesis, along with fast analysis and modeling of the PDNs, various methods for suppression of PDN noise are studied. These methods include adding decoupling capacitors, differential signaling, and employing electromagnetic band-gap (EBG) structures that provide omnidirectional noise suppression [12]-[13]. Modern PDN noise suppression should cover a wide frequency range often starting from below 1GHz. At this low frequency, the relatively large footprint for the EBG structure may prevent usage of this suppression technique in compact systems such as mobile devices. Hence, a new research direction has emerged that focuses on miniaturization of the EBG structures by using specialized materials with high dielectric constant or optimization of the EBG layout [14]-[15]. This advanced topic has also been investigated through the full-wave simulations in this thesis. Modeling of these modern PDN structures is not a trivial task and is out of the scope of this Master's thesis.

1.3 Thesis contributions

In addition to the extensive literature survey conducted in this thesis, many new topics have been investigated during the course of this research. The contributions of this thesis are listed as follows:

1) Implementation of the analytical models based on the RTL method in [3] and simulations of a few test cases and comparisons with the measurements of a fabricated prototype.

2) Implementation of the analytical models based on the cavity method in [11] and simulation of a few test cases and comparison with the measurements of the fabricated prototype.

3) For the first time, global simulations of a high-speed field programmable gate array (FPGA) system, including the accurate representation of the PDN structure are conducted in this thesis. The system model incorporates the PDN model derived from the studied analytical techniques.

4) The analytical models are developed to rapidly simulate PPW PDNs with perfect electric conductor (PEC) and PMC sidewalls, PDNs including discrete decoupling capacitors, differential vias, multilayer PPW stack-ups as well as multiple via structures.

5) Investigating noise suppression when differential signalling is used, generating the noise map and studying the effect of changing via spacing or input risetime.

6) Investigating two methods for miniaturization of a uniplanar EBG structure.

7) Combining differential vias and the EBG structure to further suppress power/ground noise.

The research work of this thesis has resulted in publishing one conference paper so far [16], and a journal paper that will be submitted soon.

1.4 Thesis outline

This thesis starts with a description of a PDN and its typical components in Chapter 2. Two main components of a typical PDN, i.e. PPW and via, are introduced with their respective equivalent circuits. Two simulation methods based on analytical solutions of a PPW using the RTL theory and cavity analysis are explained in Chapter 2. This is followed by derivation of the circuit models for various test structures and conducting global system simulations using the RTL method in Chapter 3 and the cavity method In Chapter 4. These models predict power/ground noise in a matter of a few minutes.

In Chapter 3, the RTL models are also used to investigate the impact of adding decoupling capacitors and employing differential vias in noise suppression. The simulation results of time-domain noise waveforms by the RTL method are provided and compared with those from a commercial 3-D full-wave simulator. Moreover, measurements of a simple test structure and system simulations of an FPGA transceiver circuit are presented in this chapter.

In Chapter 4, a similar set of investigations are conducted but with using cavity method analysis. The important feature of this method is the easy inclusion of two kinds of boundary conditions, i.e. PMC and PEC, in the analysis of the PDN structure. Self- and transfer impedances of several typical structures are investigated and compared with the simulation results of two popular 3-D full-wave simulators. As well, parametric study of a differential via structure when varying via spacing or input rise-time is conducted and patterns of PDN noise progression are generated. The validity of this method is verified with full-wave

simulations. The FPGA transceiver system investigated in Chapter 3 is revisited in Chapter 4 using the models derived from the cavity method. As well, measurements of the simple test prototype are presented and compared with the circuit simulations.

Chapter 5 covers various miniaturization methods applicable to a uniplanar EBG structure. A number of techniques are applied to the design of the unit-cell of the studied uniplanar EBG structure and extensive simulations are conducted to investigate the efficacy of the employed technique in ultimate miniaturization of the layout. Furthermore, a differential via pair embedded in this uniplanar EBG structure is simulated using full-wave simulations. Finally, Chapter 6 presents a summary of the thesis and provides concluding remarks and suggestions for future work.

Chapter 2 Power distribution networks

2.1 Introduction

In general, the basic functions of a PDN are delivering sufficiently clean supply voltages, providing a reference path for signal lines and not causing unwanted radiations [1]. To meet these requirements, more and more parallel-plate conductor structures are used as the main PDNs in electronic systems. Investigating the performance of the PDNs in terms of supporting and propagating noise and unwanted modes is now an important step in designing electronic products. Tight production schedules drive designers to employ fast noise prediction methods to evaluate and verify their designs. Therefore, developing PDN models that enable rapid performance predication is of critical importance in PDN research and design.

In this chapter, first a typical parallel-plate PDN structure is investigated and its characterization and modeling are discussed in detail. Since vias are essential in multilayer and 3-D routing of signals and reference voltages, equivalent circuits for vias are presented. These models are also coupled with the PDN model. Then, with use of the various modeling methods introduced herein, power integrity problems and some commonly practiced solution methods are investigated. Finally, simulation and measurement methods are provided.

2.2 Parallel-plate PDN structures

In earlier single-sided or double-sided printed circuit boards (PCBs), the power and ground were often delivered by printed traces that shared the same conductor layer with signal traces. The loop created by the power and ground traces resulted in the addition of parasitic inductance to the power delivery path, which in turn added an unwanted supply voltage drop [17]. With the progress of electronic systems and availability of cost effective multilayer fabrication technologies, designers increasingly opted for using solid metal layers for the distribution of reference voltages to reduce the parasitic inductance of the power supply paths and provide an unambiguous return path for signal traces. Hence, the basic PDN configuration used in contemporary electronic systems is composed of a pair of parallel conductor planes separated by a dielectric layer. These planes deliver DC current from the power supply source to various circuits. However, they also form a PPW structure that can support and propagate voltage fluctuations and electromagnetic waves.

In practical system implementation, a typical power distribution network may also include voltage regulator modules (VRMs), decoupling capacitors and their delivery paths, as shown in the expanded circuit schematic of Fig. 2.1 [2].

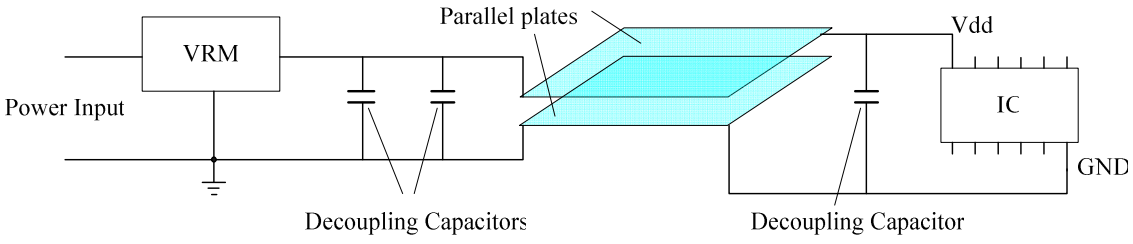


Fig. 2.1. Components of a typical PDN.

Modern electronic systems commonly use multiple parallel-plate structures where two or more planes are dedicated to delivering reference voltages and ground. One example is a 22-layer PCB used in the central processing unit (CPU) module of a Sun Microsystems server (V890). In this design, four plane pairs separated by thin-laminates are assigned to power distribution [1].

At a smaller scale like integrated circuits (ICs), parallel-plate PDN are also employed. One example, from [18], is shown in Fig. 2.2 for ball-grid array (BGA) ICs mounted on a board. An IC package can have several power and ground plane layers as well. In the new generation of packaging techniques, like multiple stacked chips in system-in-packages (SIPs) and system-on-packages (SOPs), which include both active and passive components (passives in thin-film form) in microminiaturized packages, parallel-plate PDN configurations are prevalently employed [19].

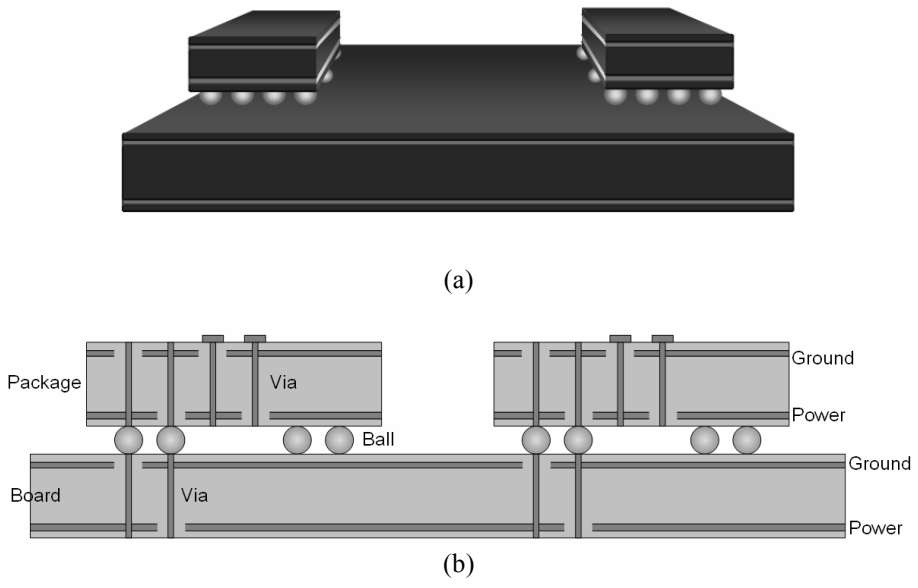


Fig. 2.2. A hierarchical power/ground network which contains one board and two BGA type packages. (a) Perspective view. (b) Side view [18].

In some electronic systems, in order to provide isolation or due to compact routing consideration, a power/ground delivery plane may be partitioned; thus, irregularly shaped parallel-plate PDNs are created. In such cases, the irregular complicated shapes can be segmented to several small regular areas for ease of modeling [20]. However, as a rule of thumb in many engineering practices, it is seen that the quality of the delivered power is often improved when regular shape PDN planes are used. Therefore, in this thesis only the regular solid power/ground planes are investigated.

To focus more on the main component of the typical PDN of Fig. 2.1., i.e. the parallel-plate structure, a sample PPW shown in Fig. 2.3 is presented.

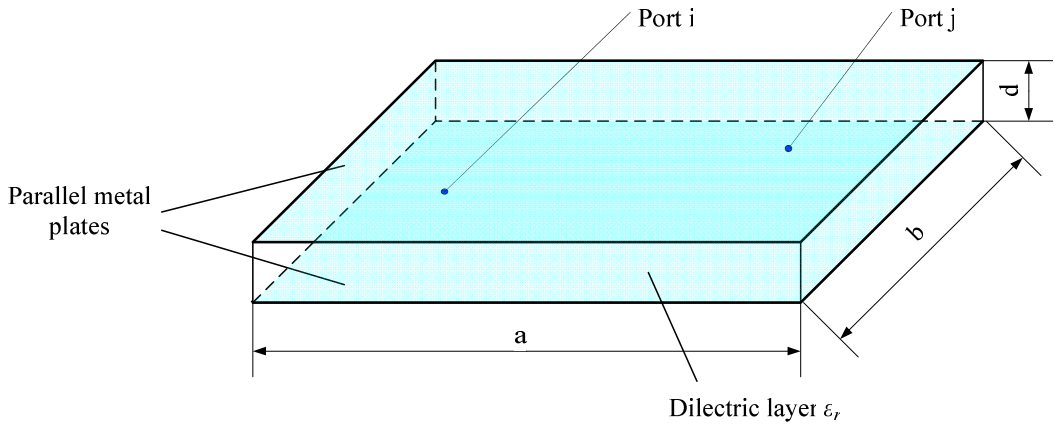


Fig. 2.3. A sample PPW configured by the parallel conductor planes in a PDN.

Often, the lateral dimensions (*a* and *b*) of the PPW can be many multiples of the wavelength of the highest frequency component of the signals in the system, and the dielectric thickness *d* is much smaller than that wavelength. Any point on these planes can be used for connection of a via or a component pin for tapping out power or ground voltages. These points are considered as the excitation or measurement ports in analysis of the PPW as a distributed network component

using electromagnetic wave theory. For example, the ports represent nodes where the impedance can be measured. These measurements are always made between a point on the top plane and the projection of the point on the bottom plane. The impedance provides the relationship between the voltage and current of the parallel planes at the location of the port [2]. At low frequencies, the PPW structure resembles a parallel-plate capacitor and shows capacitive characteristics, whereas as frequency increases, it becomes more inductive due to the dominating parasitic inductance of the planes. However, this inductance is much smaller than that of any other configuration (like using power/ground traces) used in packages and boards. Hence, PPW planes are often used to supply the charges needed for switching of digital circuits.

Since the PPW configured in PDNs has a finite size, it exhibits cavity characteristics due to reflections from the side walls. These resonances can create signal and power integrity problems because the self-impedance around resonances becomes large [2].

The parallel-plate component of the PDN is a distributed circuit that supports electromagnetic (EM) waves. The EM modes are excited and propagate in this structure when a time-varying current source is present [3]. These modes introduce fluctuations on the reference voltage planes that are interpreted as noise. This is a common problem in RF and high-speed digital systems. In complementary metal–oxide–semiconductor (CMOS) circuits, the transient switching current of the transistors generates voltage drops across the parasitic inductance in the PDNs as well as exciting the PPW modes and resonances that

degrade the performance of the systems. For investigating the PDN noise in high-speed circuits, it is important to model the parallel-plates in order to estimate and analyze the unwanted affects before fabrication.

In the initial modeling approaches, the parallel-plates are modeled using lumped elements networks. In earlier publications and simplified modeling attempts, the parallel-plates are either modeled as a lumped inductor or as an inductive network [2], [21]. However these modeling methods are not suitable at high frequencies where the PDN configures a PPW to support wave propagation. In reference [20], partial inductance is used for modeling; the planes are divided into many unit-cells and each one is represented by an inductor. However, the bandwidth of such a model is limited because the distributed capacitances are not taken into account. Therefore, this approach is applicable under the condition that the plane size is much smaller than the shortest wavelength being considered in the medium [2]. There are other modeling approaches that include the effect of distributed capacitances [20], [22], [23]. These models consider a transmission line representation that could happen in the Cartesian or Cylindrical coordinates [20], [22]. One of these approaches uses circular sector segmentation of the parallel-plates [22]. The models of the unit-cells in these methods are like two dimensional (2-D) bed-springs or T-type *RLCG* components [2].

The benefit of lumped circuit models is that they can be simulated using conventional simulators like a simulation program with integrated circuit emphasis (SPICE). However, when the planes become electrically large, the

equivalent circuits become very complex and the simulation time increases significantly.

Full-wave methods employ time-domain or frequency-domain techniques to obtain numerical solutions of Maxwell's equations directly for physical parallel-plate structures. These EM field solvers use numerical techniques, such as finite-difference time-domain (FDTD), finite-element method (FEM), finite integration technique (FIT), and method of moments (MoM) [3]. Analysis of the PDNs using the full-wave EM simulators provides accurate results while often taking enormous CPU time and memory. Thus, many designers favour compromising the accuracy with fast simulations by using analytical techniques.

Instead of the full-wave solutions, the parallel-plate PDN is solved for its dominant mode (TEM). Therefore, it can be modeled using transmission line circuits. In another analytical approach, the PPW is considered as a cavity resonator and from field derivations the performance over a wider frequency range, including a higher number of modes, is predicted. The details of PDN modeling using the RTL method and cavity resonator analysis will be discussed in Section 2.5.

2.3 Vias in PDNs

Vias provide the conducting paths for vertical interconnections of signals or delivery of power/ground to various layers in multilayer packages or boards. A typical via consists of a barrel, two or more pads, and anti-pads. The barrel is a conductive cylinder (in PCB structures) that allows electrical connections

between layers. The pad is used to connect the via barrel to a signal or power/ground trace. The anti-pad is the clearance or perforation in the solid conductor plane to avoid shorting the pad with the surrounding conductor [1]. The via configurations include through, buried and blind vias, depending on their sizes and extensions in the multilayer substrates. The through via is the most common and economical type used in PCB fabrication.

2.3.1 Modeling of vias

A via is modeled using a lumped circuit with Π or T topology [3] composed of inductor and capacitor elements. Often a simplified model of via consisting of an inductor is also used. This inductor introduces a voltage drop in the path of a signal or in a power/ground connection (with a switching current); therefore, it is essential to derive an expression for calculating the via inductance. The partial self-inductance of a via can be derived from analytical formulas derived from either energy or field relations [1], [17].

When two vias are neighbouring each other, the current flowing through one can induce a current return on the other via. This loop current path results in an additional inductance. There are other ways to account for the coupling between vias, including the addition of mutual inductance and capacitance. Often this coupling is ignored when the vias are well spaced. The relations for calculation of the coupling between vias are discussed in [1], [17].

The Π model of a via, including conductive losses, is shown in Fig. 2.4, which is modified from [24]. In this *RLC* model, the two shunt capacitors represent the

capacitance between the via barrel and the return references, and the series inductor includes partial self-inductance of the via and the partial mutual inductance when it exists. The capacitor values can be obtained from 3-D quasi-static field solvers, such as Ansoft Q3D Extractor. In a more complicated structure, like differential multilayer vias, the vias are divided into segments based on the number of existing parallel-plate substrates. The equivalent circuit of each segment is extracted separately using quasi-static numerical tools and closed-form formulas, and then these circuits are cascaded to create the model for the entire multilayer structure [25], [26].

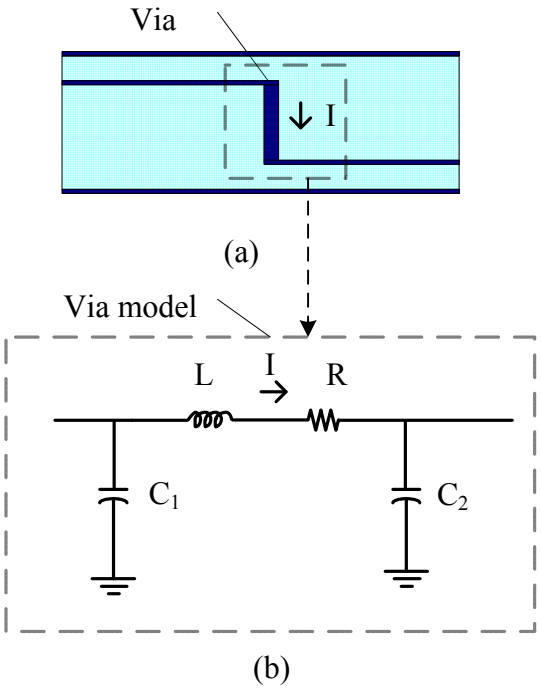


Fig. 2.4. (a) Structure of a via with signal traces inside a PPW. (b) Π model of the via [24].

2.3.2 Coupling the via and parallel-plate PDN models

The parallel plates in a PDN are normally perforated by or connected with vias. Thus, the effects of the parallel-plate environment around the via, or in another

term, the effects of this vertical current source in the PPW should be taken into account in complete system modeling. Moreover, as the frequency increases the corresponding coupling becomes more remarkable and cannot be ignored [3]. To incorporate the coupling between the via and the parallel-plates, the Π-type via model should be modified as shown in Fig. 2.5, which is from [23]. The parallel plates are modeled by two perpendicular *LC* ladder networks. The via current is coupled to the parallel plates by a dependent current source. The coupling from the parallel-plates back to the via is captured by adding a dependent voltage source in the Π circuit. The two dependent sources have a coupling coefficient determined by the via length and the spacing between the parallel-plates [3], [23]. This model can be extended to multiple vias as described in [3].

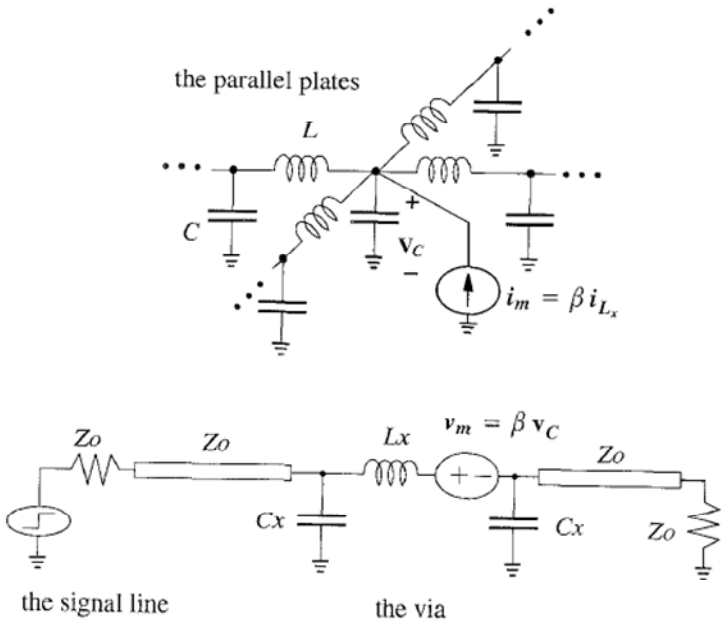


Fig. 2.5. Equivalent circuit of a via including the parallel-plate effects [23].

2.4 Power integrity

Power integrity refers to the quality of delivered power from the supply at the load end. Sufficiently clean supply voltages are always desired in electronic circuit design. However, the switching currents in digital circuits and activity-dependent power drain in analog circuits create transient currents that excite EM modes and generate unwanted voltage (and current) fluctuations interpreted as power/ground noise. This noise must be kept below a predefined limit so that it does not interfere with the analog or digital signals [1].

2.4.1 Power/ground noise problems

Power/ground noise is a widely-known adverse effect in CMOS digital circuits. When a time-varying current such as a logic transition passes through a via, EM modes are excited and propagate in the PPW. At the sidewalls of the board or package, part of the wave energy is reflected back and the rest is radiated outside [27]. Since the dielectric and the loss metal can not absorb and attenuate these waves immediately, the reflected waves can form resonances at certain frequencies; the board or package structure acts as a cavity resonator while its open sidewalls radiate into the surrounding environment. Other vias penetrating the same parallel-plate pair are impacted by these resonances even if they do not carry time-varying current themselves. They absorb the noise and distribute it back throughout the entire system. A worse scenario occurs when most logic transitions happen at the clock edges. The voltages fluctuations superimpose at

the same time and create simultaneous switching noise (SSN) on the power/ground planes [28]-[30].

SSN can cause false switching, thereby increasing the bit error rate (BER) in data communication. This reduces the reliability of the system and could create severe malfunctions.

With the development of the nanometre CMOS technologies, higher operating frequencies and faster rise/fall times have been enabled while the supply voltages are decreased and chip layouts become much denser [3]. Therefore, the SSN problems are even more significant and become a major constraint in board, package and chip design.

Mixed signal circuits and systems, such as radio frequency (RF) front-ends and baseband processors, analog to digital converters (ADC) in mobile wireless products and many sensors, are composed of analog, RF and digital circuits. The combination of noisy digital and sensitive analog and RF circuits in these systems makes them very susceptible to power/ground noise. For example, when a common power supply is employed, noise distribution happens through the shared PDN. Analog and RF circuits are very sensitive to SSN due to their intrinsic limited tolerance to supply voltage variations. SSN reduces signal to noise ratio (S/N) of the system and can cause failure [13]. Therefore, suppressing SSN is one of the major challenges in designing mixed-signal circuits.

2.4.2 Suppression of power/ground noise

To solve the problem of excitation of SSN and power/ground noise, the direct approach is to suppress the noise at its source and damp down the propagated waves in order to avoid the resonance effects [27]. The commonly used methods include adding discrete decoupling capacitors [31], [32]; use of embedded capacitors to minimize the length of the problematic leads [33], [34]; employing differential signalling [3], [35]; use of dissipative and loss components along the PCB edges [36], [37]; dividing the power planes into power islands [38]; and finally, via stitching [39]. Recently, a novel approach based on utilizing electromagnetic band-gap (EBG) structures in the power/ground planes was proposed in [12], [13], which results in efficient noise suppression for all azimuthal directions on the parallel-plate PDNs.

A. Adding discrete decoupling capacitors

Adding decoupling capacitors is the most widely used method in PCB and packaging design. Normally, large value capacitors are placed nearby the noise source so that shorting paths for the voltage fluctuations in the PDN are provided by the capacitors. In fact, from frequency domain analysis it can be observed that the impedance between the power and ground planes is reduced by the decoupling capacitors in the lower frequency bands. This method is effective and low-cost, but ineffective at high frequencies where the connecting leads, pins, vias, and bonding wires, all of which connect the capacitor to the board or package, become inductive. Therefore, the impedance between power and ground planes is increased rather than decreased [40]. The inductance associated with the

connecting components determines the frequency range at which the decoupling capacitors are effective [40]. Typically, decoupling capacitors are effective only when their total impedance is lower than the impedance seen looking into the power/ground planes [40]. To ensure system performance and reliability, typically, on-chip, on-module and on-board decoupling capacitors are used to suppress high, middle and low frequency noise respectively [41]. In most engineering practices, selection of the decoupling capacitors is often an engineering estimation and is based on well-established guidelines from experience [41].

B. Employing buried decoupling capacitors and embedded capacitance

In this method, a decoupling capacitor is configured by a parallel plate pair laid out and embedded in the system. In comparison with discrete capacitors, buried capacitors are less prone to parasitics and offer better performance at higher frequencies [13], thereby offering a promising alternative as opposed to discrete decoupling capacitors. In some cases, even the natural capacitance between the power and return planes are utilized to provide power-bus decoupling [42]-[44]. By minimizing the spacing between the two solid planes and filling this space with a material with high relative permittivity, the inter-plane capacitance can be greatly enhanced. Consequently, it is possible to eliminate most or all of the decoupling capacitors mounted on the surface of the board, freeing up valuable surface routing areas, and improving product reliability [45]. The drawback of this technique is that the capacitance value is limited by the structure dimensions.

C. Using differential signalling

Differential signalling is an alternative method with intrinsic noise and common mode rejection features. For example, in the case of two differentially excited vias embedded in a PPW, it can be seen that the two vias induce out-of-phase noise waveforms, ultimately resulting in overall noise reduction in comparison with a single via or two vias with common mode excitation [3]. In fact, study of differential vias in parallel-plate environments reveals that complete noise suppression can be achieved along a certain direction. Indeed, the level of noise suppression is primarily a function of the difference between the arrival times of the noise waveforms generated by the two vias [16]. On the power/ground planes, maximum noise suppression is achieved along the direction of the perpendicular bisector of the line connecting the two vias and minimum noise suppression occurs along the line connecting the two vias [16]. Hence, it can be concluded that differential vias provide a variable noise suppression factor that can be 100% along a specific direction. The level of noise suppression obtained by employing a differential routing technique depends on the location of the observation point with respect to the two vias and the shapes of the noise waveforms due to dispersive propagation in the PPW [3]. The variation of noise suppression along different directions produces high and low noise areas on the power/ground planes. Identifying the quiet and noisy regions of the reference voltage planes is an important design step, as it can be applied to the pin assignment in chip packaging and the component placement in PCBs [16].

Nonetheless, differential signalling adds to the complexity of the system and implementation costs, and increases the pin count.

D. Employing EBG structures

The suppression techniques discussed earlier only provide localized noise suppression, while an omnidirectional noise mitigation is always desired. Moreover, the typical power/ground noise suppressing methods using decoupling capacitors are found to be inadequate for wideband and over gigahertz frequency ranges. Recently, employing EBG structures in the PDNs has been proposed for high frequency and broadband power/ground noise suppression in high-speed digital mixed-signal and analog systems [12], [13]. This solution has been further developed and extended in [14]-[15], [27], and [46], showing outstanding performance in the power/ground noise suppression.

EBG structures are initially employed as high-impedance surfaces (HISs) to suppress surface waves in antenna applications [47]. Various kinds of EBG designs have been introduced and investigated [12]-[13], [14]-[15], [48]-[50]. One of the most popular structures that has been used for noise suppression is mushroom type geometry. As shown in Fig. 2.6, a PDN with embedded mushroom-type EBG structure is composed of three metal layers, including square (or other symmetrically shaped) patches in the middle layer, sandwiched by the two solid metal layers on the top and bottom. The patches are connected to one of the solid conductor layers by vias [13]. It has been demonstrated that this type of EBG can provide wide stopband and excellent port isolation [13]. It has

been speculated that this type of EBG takes up a signal routing layer, and adding vias, especially blind vias, increases the fabrication costs. Therefore, two-mental-layer EBG structures have been investigated to be employed as PDNs in [14]-[15], [51]-[52]. The various configurations of this kind of EBG structure include alternating impedance (AI)-EBG [51], slit-EBG [53], uniplanar compact photonic-bandgap (UC-PBG) [54], and L-bridged EBG [55].

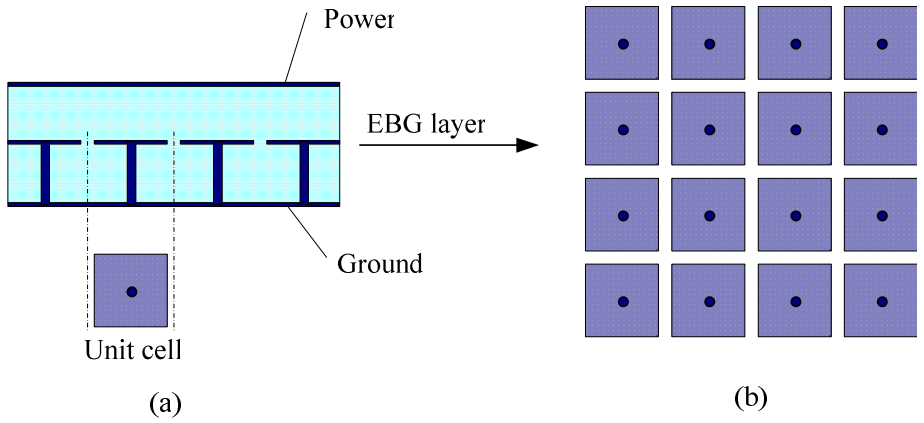


Fig. 2.6. Two-layer metallo-dielectric EBG structure. (a) Side view. (b) Top view of the EBG layer.

The EBG structures act as band reject filters and evanesce unwanted voltage fluctuations generated at one end of a PDN to reach other parts of the substrate [56]. The insertion loss and the width of the stopband region are two important measures of the efficiency of this noise suppression. Therefore, prediction of the attenuation characteristics and the frequency range of the induced stopband are required in proper design of an EBG structure for a target application. The EBG structure can be easily integrated into PCB or a package fabrication process and guarantee a much lower noise coupling and timing jitter in system operation [57], [58].

In order to increase the insertion loss, an adequate number of unit cells (four in many applications) is needed. Hence, the overall EBG structure can take up a large area, especially if it is designed for low frequency operation. This creates a problem in their applications in packages and compact electronic systems, such as portable wireless devices. For example, if GSM-850 bands are considered (824 MHz to 894 MHz [59]), the unit-cell of an EBG should be designed such that the lower corner frequency of its induced stopband is lower than 824 MHz. The size of the unit cell has an inverse relation with the stopband frequency [14], especially when conventional methods of fabrication and common materials are used. If the size of the unit cell is large, sufficient isolation may not be obtained, while, in a compact system, the number of unit-cells between the noise source and the noise sensitive component is reduced. To meet the general demand for more compact design, it is desirable to miniaturize the structure of EBG unit cell while ensuring the achievement of the desired stopband.

To reduce the dimensions of a uniplanar EBG structure, according to references [14] and [15], there are three approaches: 1) employing novel geometries, such as introducing narrow slits into the patches [14], [15]; 2) using high permittivity substrate materials [14], [15], [49]; 3) application of high permeability magnetic material sheets [15]. Each approach was found to contribute to reducing the size of the EBG structure. Applying all approaches simultaneously made it possible to achieve a highly minimized EBG structure with sufficient insertion loss at the stopband [14], [15].

In this thesis, miniaturization approaches initially introduced in [14] are employed to investigate a uniplanar EBG structure. Details of this investigation are presented in Chapter 5.

2.5 Simulation methods to analyze PDN structures

As referred to earlier, there are four major types of simulation methods used to predict the responses of PDNs: 1) full-wave simulations, which use numerical electromagnetic field solvers; 2) analytical solutions, which derive closed-form analytical expressions for simple cases; 3) lumped circuit modeling and use of commercial circuit simulators; 4) hybrid methods, which combine full-wave simulations, analytical solutions, or measurement results with circuit simulators [3], [6].

In this thesis, analytical derivations based on the RTL solution and the cavity methods are used in combination with circuit simulators, i.e. two hybrid approaches. In both methods, analytical expressions are employed to obtain the representative impedance matrices of the PPW. Then, the equivalent circuits of vias and the rest of circuits are combined with the impedance matrices and simulations are performed using Agilent Advanced Design System (ADS). Full-wave simulations are also conducted to evaluate the accuracy of the proposed methods.

Full-wave solvers take all electromagnetic effects into account, including all loss mechanisms, distributed effects, and all parasitics [1]. Generally, the field distribution and currents in the structure can be observed as well, thereby

providing a deep understanding of the intrinsic mechanism [1]. In order to take full advantage of the tools, the geometry and materials should be set accurately. Moreover, boundary conditions, port definitions and meshing setup need to be carefully considered [1].

In order to verify the proposed methods, two 3-D full-wave commercial field solvers, Ansoft HFSS and CST Microwave Studio, are employed. Ansoft HFSS is an FEM field solver [1]. Only frequency-domain results such as *Z*- or *S*-parameters can be obtained by this solver. CST Microwave Studio uses FIT for field calculations [1]. Both time- and frequency-domain results can be directly obtained by this solver. For analysis of PDN noise, often time-domain responses are preferred, as the noise progression, spikes and voltage fluctuations can be directly observed and compared with the global hybrid system simulations using the RTL and cavity methods.

2.5.1 RTL method

As mentioned before, the conductor plane pairs in a PDN configure a PPW. Any alteration in the field inside the structure can excite PPW modes. Thus, any discontinuity such as a via embedded in the parallel-plate structure, (see Fig. 2.7), can be regarded as a waveguide excitation source resulting in propagation of cylindrical waves.

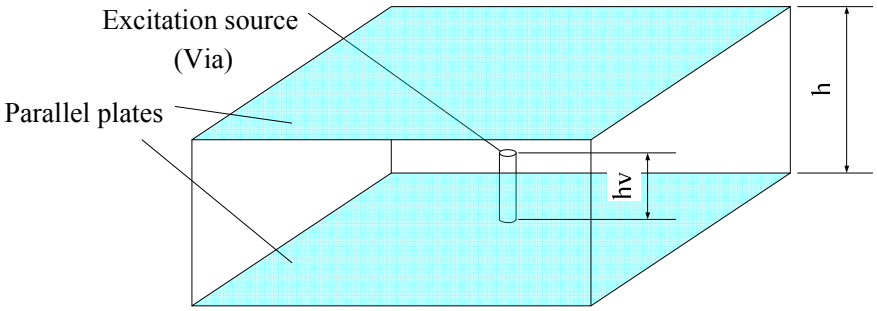


Fig. 2.7. A parallel-plate waveguide with a buried via.

The PPW supports propagation of the dominant cylindrical TEM wave and the parallel-plate pair can be viewed as an RTL. Based on the RTL theory, the solution for fields and voltage and current waves in the RTL structure with the cylindrical source can be obtained by solving Helmholtz' equation in the cylindrical coordinates [3]. The voltage and current wave functions are found from the following equations:

$$V(\rho) = V^{+} H_0^{(2)}(k\rho) + V^{-} H_0^{(1)}(k\rho) \qquad (2.1)$$

$$\frac{j\eta h}{2\pi\rho} \cdot I(\rho) = V^{+} H_1^{(2)}(k\rho) + V^{-} H_1^{(1)}(k\rho) \qquad (2.2)$$

Where, η is the intrinsic impedance of the dielectric layer, $\eta = \sqrt{\mu/\varepsilon}$,

h is the thickness of the dielectric layer,

ρ is the radial distance,

j is the imaginary unit,

μ is the permeability of the dielectric,

ε is the permittivity of the dielectric,

k is the wave number in the dielectric, and $k = \omega\sqrt{\mu\varepsilon}$,

$H^{(2)}$ represents the forward travelling Hankel function, and $H^{(1)}$ represents the backward travelling Hankel function; the subscripts represent the order of the functions.

The input impedance at any point on an infinite RTL can be derived from the voltage and current equations [3]. For an infinite or relatively large RTL, the input impedance can be expressed by [3]:

$$Z_{\text{in}} = \frac{j\eta h}{2\pi\rho}\frac{H_0^{(2)}(k\rho)}{H_1^{(2)}(k\rho)} \tag{2.3}$$

Generally, the point where excitation is located is considered as Port 1 and the observation point is Port 2. Therefore, the parallel-plate pair is represented by a two-port admittance network element, for example, a "*Y*-network". To emulate an infinite RTL, Port 2 of this network component should be connected to the input impedance of an infinite transmission line called element "*Z*" [3]. This arrangement of *Y* network and *Z* element models a section of the PPW and its terminating impedance, respectively [3]. These network elements are derived from the analytical solution of Maxwell's equations for the fundamental TEM mode of a radial waveguide, and are expressed by Hankel functions [3]. The admittance network between two ports at distances ρ_1 and ρ_2 from the center can be obtained by the following formulas [3].

$$Y_{11} = \frac{1}{jZ_1}\cdot\frac{H_1^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2) - H_0^{(2)}(k\rho_2)H_1^{(1)}(k\rho_1)}{H_0^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2) - H_0^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1)} \tag{2.4}$$

$$Y_{12} = \frac{1}{jZ_1}\cdot\frac{H_0^{(2)}(k\rho_1)H_1^{(1)}(k\rho_2) - H_1^{(2)}(k\rho_1)H_0^{(1)}(k\rho_1)}{H_0^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2) - H_0^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1)} \tag{2.5}$$

$$Y_{21} = \frac{1}{jZ_2} \cdot \frac{H_0^{(2)}(k\rho_2)H_1^{(1)}(k\rho_2) - H_1^{(2)}(k\rho_2)H_0^{(1)}(k\rho_2)}{H_0^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2) - H_0^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1)} \tag{2.6}$$

$$Y_{22} = \frac{1}{jZ_2} \cdot \frac{H_1^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1) - H_0^{(2)}(k\rho_1)H_1^{(1)}(k\rho_2)}{H_0^{(2)}(k\rho_1)H_0^{(1)}(k\rho_2) - H_0^{(2)}(k\rho_2)H_0^{(1)}(k\rho_1)} \tag{2.7}$$

Where, Z_1 and Z_2 are characteristic impedance at ρ_1 and ρ_2, and

$$Z_1 = \eta h / 2\pi\rho_1 \tag{2.8}$$

$$Z_2 = \eta h / 2\pi\rho_2 \tag{2.9}$$

These formulas and the parameters of the network elements can be easily calculated and plotted in Mathworks Matlab.

A sample structure is shown in Fig. 2.8 in which a single via interconnects to the striplines. The representation of the parallel-plate PDN with the RTL model and the striplines with model for via discontinuity are shown in Fig. 2.9. The PPW is represented by "*Z*" and "*Y*". The via is modeled with the Π-type *LC* circuit. The partial self-inductance of the via can be obtained from expression (2-10) [1], [17].

$$L = \frac{h}{5}[\ln(\frac{2h}{r}) - \frac{3}{4}] \tag{2.10}$$

Where, *h* is the length of the via, *r* is the radius of the via, both of their units are mm, and the unit of *L* is nH.

Losses are ignored and the resistive component of via model is not added in this model. The capacitance between the via and the conductor planes can be extracted by Ansoft Q3D Extractor. The coupling of the via current to the PPW, and the reciprocal induction of the voltage fluctuations on the PPW back to the

via are represented by the dependent current and voltage sources, respectively [3], [23].

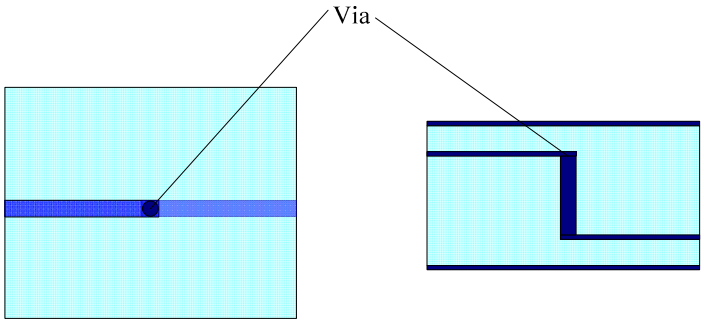


Fig. 2.8. A PPW with striplines connected by a buried via.

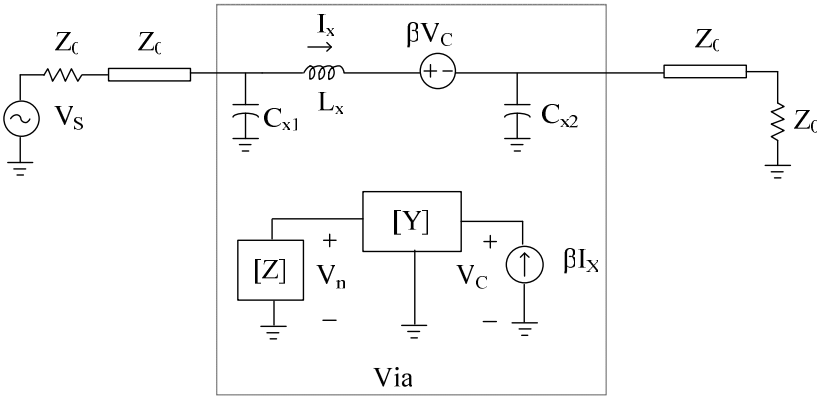


Fig. 2.9. Equivalent circuit of the RTL model for the structure shown in Fig. 2.8 [3].

The circuit shown in Fig 2.9 can be easily created in circuit solvers like in an Agilent ADS schematic window and simulated using the transient solver with the convolution engine. The "*Y*-network" is represented by a two-port data item and the terminating *"Z"* is expressed by a one-port data item. Consequently, the noise waveform at the observation point can be obtained.

If more than one observation point is needed, a three-port network is required. It can be shown that for a PPW with n ports, the number of $n \times (n-1)/2$ pairs of elements is needed. This method assumes that the parallel plates are infinite. To account for finite substrate dimensions, which is the case for practical applications, images of the via source with respect to the side-walls should be included. The detail of this technique is elaborated in [3]. Adding images further increases the simulation time and requires an advanced computing platform.

2.5.2 Cavity method

Cavity method is a useful analytical technique that accounts for the finite size of a PDN. The parallel planes behave as a cavity resonator supporting waves that propagate back and forth between the edges of the structure. The reflections of these waves at the edges cause resonances or create resonating modes. These modes can be captured by solving wave equations and accounting for the boundary conditions [8]-[9]. This process is followed by computing the self- and transfer impedances of the PPW ports. Analytical expressions for these impedance parameters are available for simple shapes, such as rectangular, square, triangular, and circular PPW cavities [1], [60]. The parallel-plate pairs are considered to be separated by a uniform dielectric material in these analytical impedance expressions.

There are three possibilities of boundary conditions for the cavity sidewalls: 1) closed by metal (like a via fence), which is represented by a PEC; 2) open, as in most cases, and represented as a PMC; 3) infinite size board, which is represented

by a perfect matched layer (PML). The analytical impedance formulas for PEC and PMC boundary conditions are available in the forms of infinite double summations [61]. Formulas for PMC and PEC boundary conditions are shown as (2-11) to (2-13).

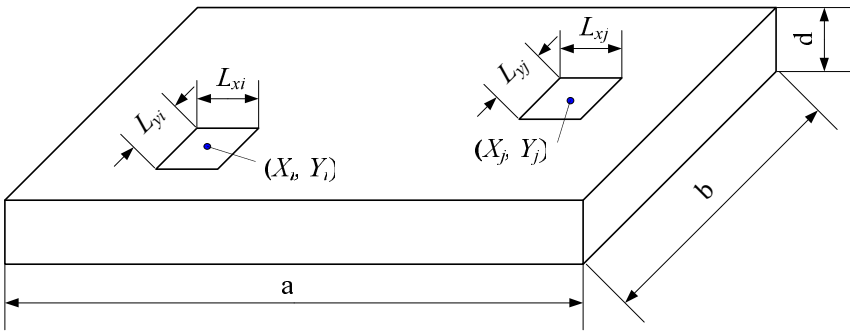


Fig. 2.10. Multi-port single dielectric layer board.

According to references [8]-[11], self- and transfer impedances of the ports shown in Fig. 2.10 can be derived from the Green function of 2-D Helmholtz equation. The general impedance function is expressed by the following closed-form double summation infinite series:

$$Z_{ij} = \frac{j\omega\mu_d d}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{C_m C_n \sin c(k_{xm}\frac{L_{xi}}{2})\cdot\sin c(k_{xm}\frac{L_{xj}}{2})\cdot\sin c(k_{yn}\frac{L_{yi}}{2})\cdot\sin c(k_{yn}\frac{L_{yj}}{2})}{k_{xm}^2+k_{yn}^2-k^2}\cdot f_{boundary}(X_i,X_j,Y_i,Y_j) \tag{2.11}$$

For PMC boundary conditions,

$$f_{boundary}(X_i,X_j,Y_i,Y_j) = \cos(k_{xm}X_i)\cdot\cos(k_{xm}X_j)\cdot\cos(k_{yn}Y_i)\cdot\cos(k_{yn}Y_j) \tag{2.12}$$

For PEC boundary conditions,

$$f_{boundary}(X_i,X_j,Y_i,Y_j) = \sin(k_{xm}X_i)\cdot\sin(k_{xm}X_j)\cdot\sin(k_{yn}Y_i)\cdot\sin(k_{yn}Y_j) \tag{2.13}$$

Where, $C_n = 1$ if $n = 0$, otherwise 2, $k_{xm} = \frac{m\pi}{a}$, $k_{yn} = \frac{n\pi}{b}$, $\sin c(x) = \frac{\sin(x)}{x}$, and

$$k^2 = \omega^2 \mu_d \varepsilon_d - \frac{j2\omega\varepsilon_d(1-\tan\delta)(1+j)}{d\sigma_c\sqrt{\frac{2}{\omega\mu_c\sigma_c}}} \tag{2.14}$$

Where, j is the imaginary unit,

ω is the angular frequency,

d is the thickness of the dielectric layer,

a is the length of the board,

b is the width of the board,

L_{xi} is the length of the i^{th} port,

L_{yi} is the width of the i^{th} port,

L_{xj} is the length of the j^{th} port,

L_{yj} is the width of the j^{th} port,

μ_d is the permeability of the dielectric,

μ_c is the permeability of the metal on the power/ground planes,

σ_c is the conductivity of the metal, and

ε_d is the permittivity of the dielectric.

The equation (2.11) has taken into account the dielectric and conductor losses, which are included in the expression (2.14).

Using Equation (2.11) to (2.14) the impedance matrix (*Z*-parameters) of a general multi-port single dielectric layer rectangular board as Fig. 2.10 can be readily calculated.

Although the double summation in equation (2.11) provides an accurate impedance estimation, it is very time-consuming, especially when many ports need to be calculated. Moreover, it is not fast to converge in calculations of self-

impedance, i.e. when *i* is equal to *j* [1], [9]-[10], and is very slow around the magnitude minima [1], [11]. One option to reduce the complexity of the calculations is to use a single summation. This is done in [11] which offers a computationally efficient method that is suitable for modeling a PPW [11].

2.5.3 Fast cavity method

To achieve a good compromise between the simulation time and accuracy, a fast cavity model is proposed in [11], [62]. Recently, its convergence property is studied extensively in [11], [63]. The fast cavity method is derived from the original cavity method by simplifying the 2-D port to a 1-D port, resulting in the simplification from a double to a single infinite summation [11].

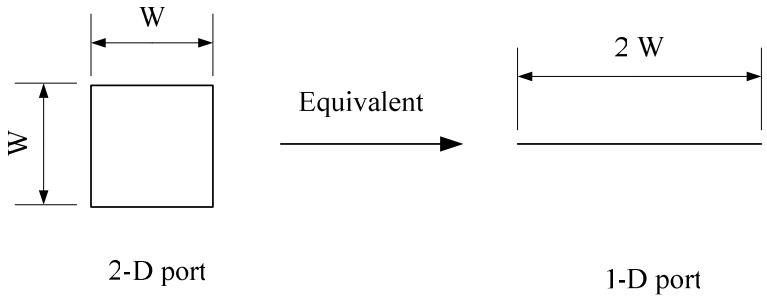


Fig. 2.11. A 2-D port is reduced to a 1-D port [11]

The summation formula of a Fourier series [64] [see Equation (2.15)] is used in this simplification process [11].

$$\sum_{m=0}^{\infty} \frac{C_m \cos mx}{m^2 - \alpha^2} = \frac{\pi}{\alpha} \cdot \frac{\cos(x-\pi)\alpha}{\sin \pi\alpha} \tag{2.15}$$

Where, $\alpha = \frac{a}{\pi}\sqrt{k^2 - k_{yn}^2}$.

When the 2-D port is regarded as a 1-D port, the following approximation is applied [11]:

$$\sin c(k_{xm}\frac{L_{xi}}{2}) = \sin c(k_{ym}\frac{L_{xj}}{2}) = 1 \tag{2.16}$$

Where, the parameters are same as those in the previous section.

As before, the single summation expressions of the fast cavity method are obtained for different boundary conditions.

A. PMC boundary conditions

Impedance matrix Z is calculated by applying Equation (2.15) and (2.16) to (2.11) for the PMC boundary conditions [11]:

$$Z_{ij} = \frac{j\omega\mu_d da}{2b}\cdot\sum_{n=0}^{\infty} C_n \sin c(k_{yn}\frac{L_{yi}}{2})\cdot\sin c(k_{yn}\frac{L_{yj}}{2})\cdot\cos(k_{yn}y_j)\cdot\cos(k_{yn}y_i)\cdot\frac{\cos(\alpha_n x_-)+\cos(\alpha_n x_+)}{\alpha_n \sin(\alpha_n)} \tag{2.17}$$

Where, $\alpha_n = a\sqrt{k^2 - k^2{}_{yn}}$,

$$x_- = \frac{x_i - x_j}{a} - 1,$$

$$x_+ = \frac{x_i + x_j}{a} - 1.$$

The numerical error between the single summation and the double summation can be adjusted to an acceptable level by assuming that the dimension of the port is much smaller compared to the size of the board [11].

B. PEC boundary conditions

For PEC boundary conditions, similarly, the impedance matrix is obtained by the following single summation:

$$Z_{ij} = \frac{j\omega\mu_d da}{2b}\sum_{n=0}^{\infty} C_n \sin c(k_{yn}\frac{L_{yi}}{2})\sin c(k_{yn}\frac{L_{yj}}{2})\sin(k_{yn}y_j)\sin(k_{yn}y_i)\times\frac{\cos(\alpha_n x_-)-\cos(\alpha_n x_+)}{\alpha_n \sin(\alpha_n)} \tag{2.18}$$

For any general case of a PPW PDN with n ports, an n-dimensional *Z*-parameter matrix is derived using the above formulas. It should be emphasized here that, in this thesis, only the fast cavity method (single summation) is implemented; for brevity, it is called *the cavity method*.

To use the cavity model in PDN simulations, a similar circuit set-up as shown for the RTL method is created in ADS. The cavity model for the structure of Fig. 2.8 is shown in Fig. 2.12, which is based on what is shown in [61]. Like the RTL model, the coupling between the via and the PPW is represented by dependent sources. In this thesis, all circuits are ported to Agilent ADS for transient simulations and observations of noise waveforms.

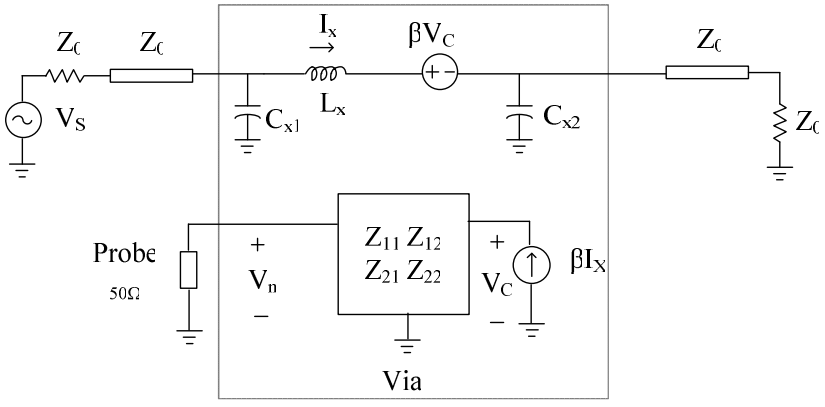


Fig. 2.12. Equivalent circuit based on the cavity model of PDN for the structure shown in Fig. 2.8.

As mentioned earlier, this method is suited for finite size package or board structures. For practical complicated geometries, the cavity method can reduce the simulation time significantly compared to the full-wave solvers [11].

2.6 Measurement of power integrity

To validate the modeling approaches and evaluate the simulation results, measurements are often conducted in time or frequency domains when test prototypes are available.

In time domain techniques, often time domain reflectometry (TDR) is used to monitor the reflected and transmitted signals. This information is utilized to characterize and locate discontinuities. A step signal generator and an oscilloscope are required for excitation and detection. In signal integrity evaluations, the TDR system generates a fast risetime step signal to excite an interconnect, and detect the reflected and transmitted signals. Degradation of risetime at the output is an indication of losses and a dispersive characteristic of the interconnect. To characterize differential interconnects in the earlier TDR systems, a power splitter is used to generate two equal signals. Now modern TDR systems with differential and common sources are available. For example, the system used for the measurements in this thesis is a Tektronix TDS 8200 oscilloscope with the 80E04 electrical sampling module. It generates two step signals with the amplitudes of ±250 mV, and the (10%-90%) rise time of 29 ps. The signal mode type can be chosen as differential- or common-mode on this

system. It should be noted that the lengths of the cables launching the two step signals should be equal to create equal delays for the two step inputs.

In power integrity evaluations, the same set up of source and high-speed digitizing oscilloscope of a TDR system can be used to create a time-varying current for excitation of a PPW, and to monitor noise waveforms and measure their peak values at various observation ports. If noise characterization for the case of differential systems is needed, the differential sources available at the Tektronix TDR system are used.

Other important power integrity tests are conducted using a vector network analyzer (VNA), which measures frequency-domain response of components in the form of scattering parameters. These parameters can be imported into a commercial circuit simulator such as Agilent ADS to obtain time-domain noise waveforms. This technique is referred to in Section 2.5 as one of the ways to conduct hybrid method simulations.

Compared with TDR measurements, VNA provides a wider dynamic range and higher accuracy. However, it can not provide real-time observation of noise waveform along with other circuit measurements that are often carried in the time-domain.

2.7 Conclusions

In this chapter, a general overview of the simulation and measurement methods used for the analysis of power deliver networks along with power integrity problems and the commonly practiced solutions are presented. At the core of any

PDN structure is a parallel-plane pair, which configures a PPW. Power/ground noise is a major problem in PDN design. To predict the noise in PDN rapidly and in a cost effective manner, two fast and accurate modeling techniques, namely the RTL and the cavity methods, are introduced in this chapter. The background formulations needed in using the RTL and the cavity methods for analysis of PDNs are discussed in detail.

Models for a simple case of a PPW with only one via are presented using these techniques. Investigation of more test-cases using the RTL and the cavity methods are discussed in Chapters 3 and 4, respectively.

Chapter 3 Noise prediction using radial transmission line models

3.1 Introduction

RTL analytical models for via structures in single and multilayer PPWs have been developed in [3]. Since these models use transmission line theory to extract the pertinent representative network files needed in global circuit simulations, they are referred to as physics-based models [3]. This chapter focuses on this modeling method. A few studied cases, including single and multiple via structures, a via with a decoupling capacitor, and differential vias embedded in multilayer PPWs, are modeled using the RTL approach. Then, time domain global circuit simulations are conducted, and the results are compared with full-wave simulations using CST Microwave Studio. Finally, the approach is applied to a practical case of an FPGA circuit and the overall circuit including the RTL model of differential vias are co-simulated using Agilent ADS. In addition, a simple single-layer board prototype with differential vias and probe vias is fabricated and measured for validation of the simulated results.

3.2 RTL modeling

The general modeling approach using the RTL theory was explained in Chapter 2. Here, more specific examples in single PPW or multiple PPW environments are investigated.

3.2.1 Parallel plates with a single via

A common interconnect structure often seen in packages and boards is shown in Fig. 2.8, where two signal tracks are connected by a via. In the same chapter the general representative RTL model for this structure is presented in Fig. 2.9. In this section, more elaboration about the components of the model is provided. As explained in Section 2.5.1, the parallel plates are presented with a "*Y*" component that accounts for the propagation delay from the excitation source to the observation point. The coupling from the buried via to the parallel plates is represented by a dependent current source βI_x. β is the coupling coefficient and can be expressed with the ratio of the height of the dielectric to the via length. In [3], a general relation for calculation of this coupling coefficient is derived. The dependent voltage source βV_c in the signal path represents the reciprocal coupling from the parallel plates to the via using the same β coefficient. The signal traces are off-set striplines and their characteristic impedance can be calculated using ADS. A signal source is connected to the stripline and the output port of the stripline at the lower layer is terminated to a matching resistance, as shown in Fig. 2.9. With the connection of the source, current I_x goes through the via and induces a current on the parallel plate which creates the voltage fluctuations. At the observation point the amplitude of this noise voltage is measured as V_n. As indicated in Chapter 2, the via is modeled by an inductor and two capacitors. The value of the inductor L_x is calculated using equation (2.10) [1], [17]. The capacitors C_{x1} and C_{x2} represent the capacitance between the via and the plates, and are equal for a symmetric structure. They can be extracted by a quasi-static commercial simulator, i.e. Ansoft Q3D Extractor.

3.2.2 Parallel plates with multiple vias

The structure of Fig. 2.8 is made more complete by adding another via at the observation point in Fig. 3.1. This via is needed in practice for attaching any component like a connector, probe, or load. The second via is a through via connected to the bottom metal plate and isolated from the top metal plate with an anti-pad clearance. In measurements, this via is connected to an oscilloscope by a cable and SMA connector. This probe via also contributes to the parallel plates noise. Fig. 3.2 illustrates the equivalent circuit of the structure of Fig. 3.1. V_{s21} is the noise voltage generated by the active via and viewed at the observation point, and V_{s12} is the noise voltage by the probe via and observed at the location of the active via. The dependent voltage source $\beta_1 V_{s12}$ represents the noise generated by the probe via and intercepted by the active via. The coupling of the noise generated by the active via back to itself is shown by $\beta_1 V_{c1}$. The model of the observation via is similar to that of the active via. The inductor L_{x2} and the capacitor C_{p2} are calculated by the same way as those of the active via. One end of the observation via model is shorted to the ground because it connected to the bottom plate. The other end is terminated to Z_o , the input impedance of the measurement instrument, which is normally 50Ω. The dependent voltage source $\beta_2 V_{s21}$ accounts for the noise generated by the active via and coupled back to the probe via. The coupling of the noise voltage induced by the probe via back to itself is presented by $\beta_2 V_{c2}$, which represents the coupling from the parallel plates.

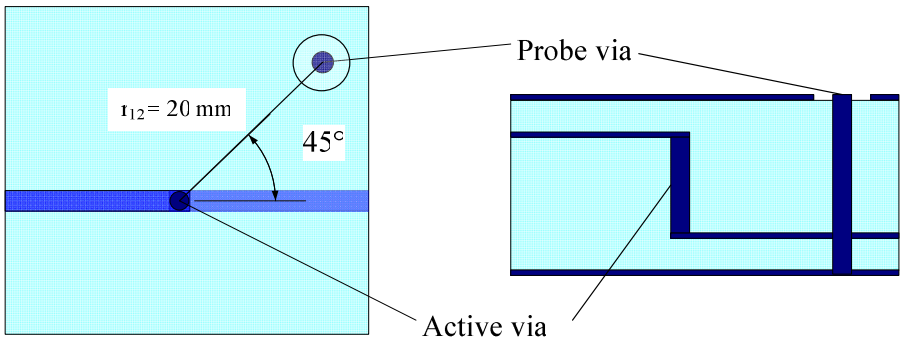


Fig. 3.1. A PPW with a buried via and an observation via.

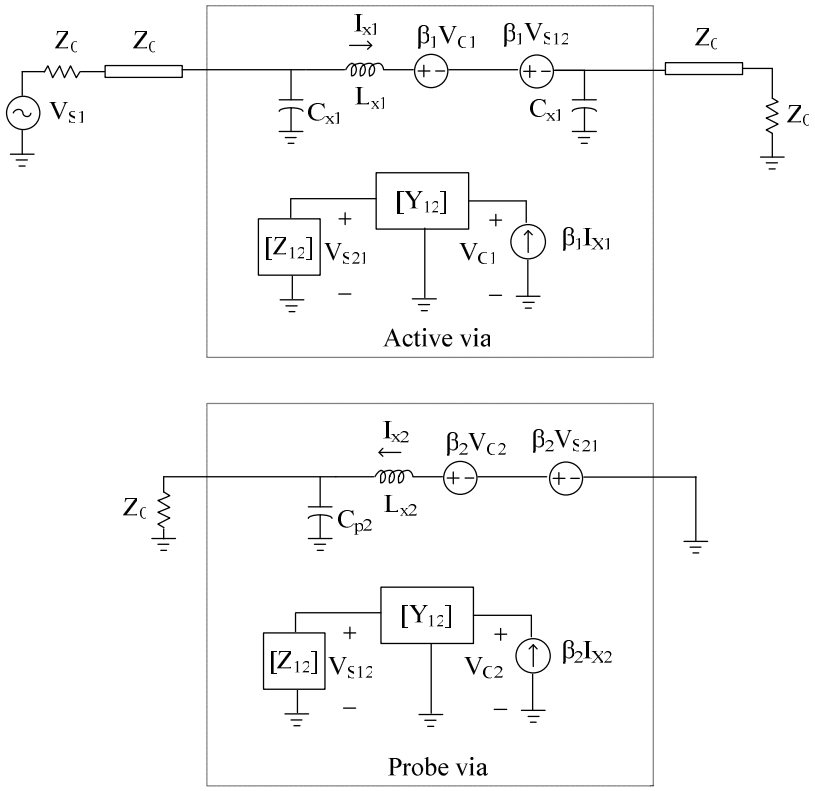


Fig. 3.2. Equivalent circuit of the structure shown in Fig. 3.1 [3].

3.2.3 Including a decoupling capacitor

Adding decoupling capacitors is the most common method of suppressing noise in PDNs. In order to achieve the maximum noise suppression, decoupling capacitors are placed as close as possible to the active via that generates the noise.

Therefore, the parallel plate fields generated by the via interconnect of the decoupling capacitor are out of phase with those of the active via and cancel each other [3]. The diagram in Fig. 3.3 shows placement of a decoupling capacitor with its via interconnect at the midpoint of the line connecting the active via and the probe via ($r_1=r_{12}+r_2$). One end of the decoupling capacitor is connected to the top plate, and the other end is connected to the bottom plate by a through via.

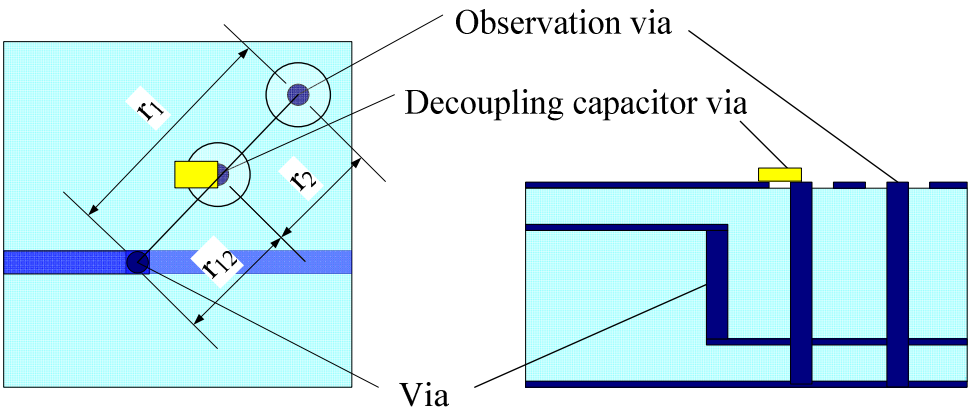


Fig. 3.3. A PPW with a buried active via, an observation via and a decoupling capacitor.

The model of the structure is modified according to the guidelines in [3]. As shown in Fig. 3.4 [65], for each via model, the couplings of the noise generated by other vias and propagated in the PPW are considered by dependent voltage sources. The noise voltage at the observation point is found from superposition of the noise voltages generated by the active via and the decoupling capacitor via, $V_{S31}+ V_{S32}$. Other components of the model are the same as those explained in the previous sections.

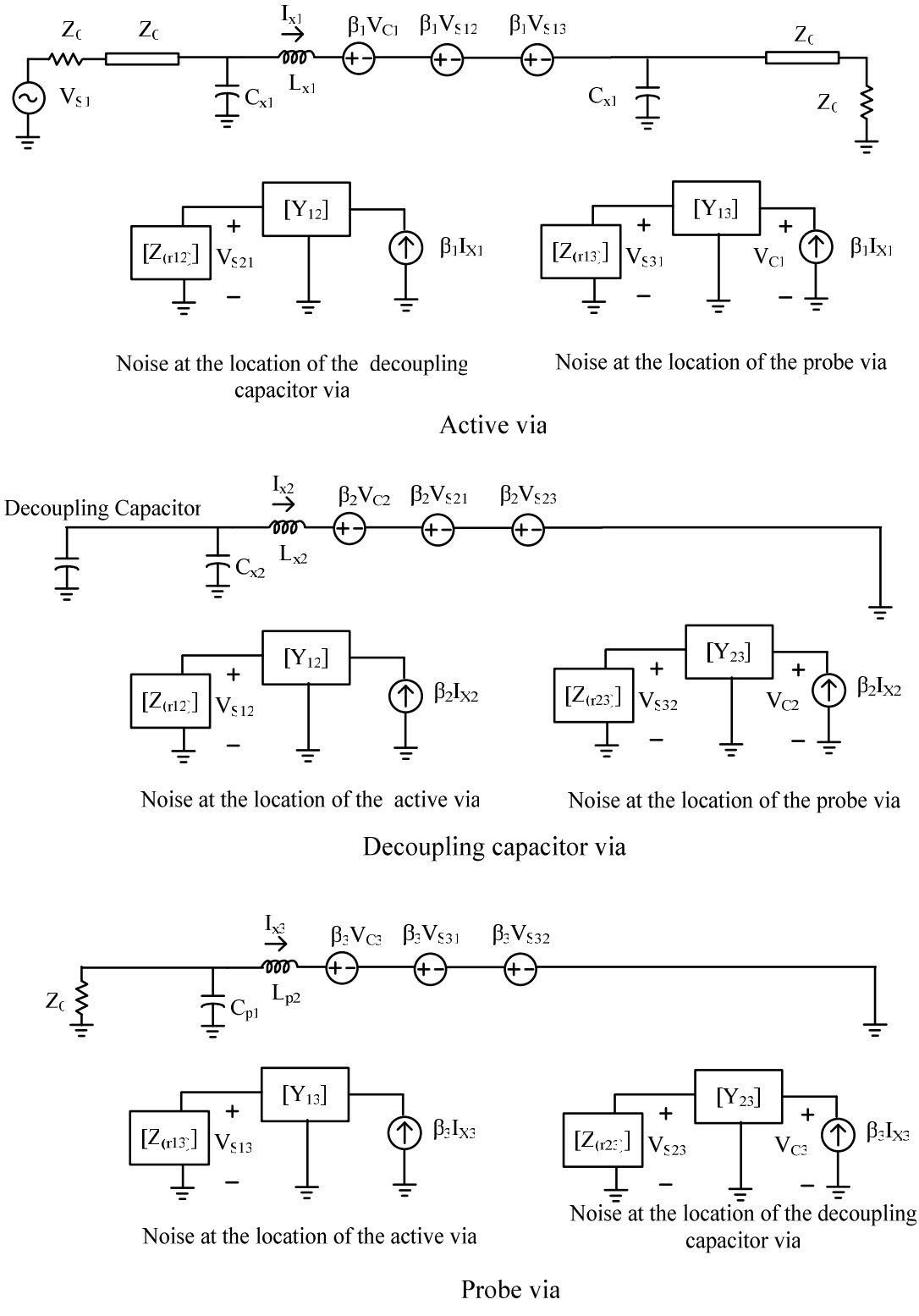


Fig. 3.4. Equivalent circuit of the structure shown in Fig. 3.3 [65].

3.2.4 Multilayer parallel plates with differential vias and a probe

To investigate efficacy of noise suppression by using differential vias, the structure shown in Fig. 3.5 is considered. Differential stripline pairs are interconnected by two vias, which penetrate in a reference voltage plate [16]. Thus, the PPW modes are potentially excited in the two stacked-up parallel plate environments.

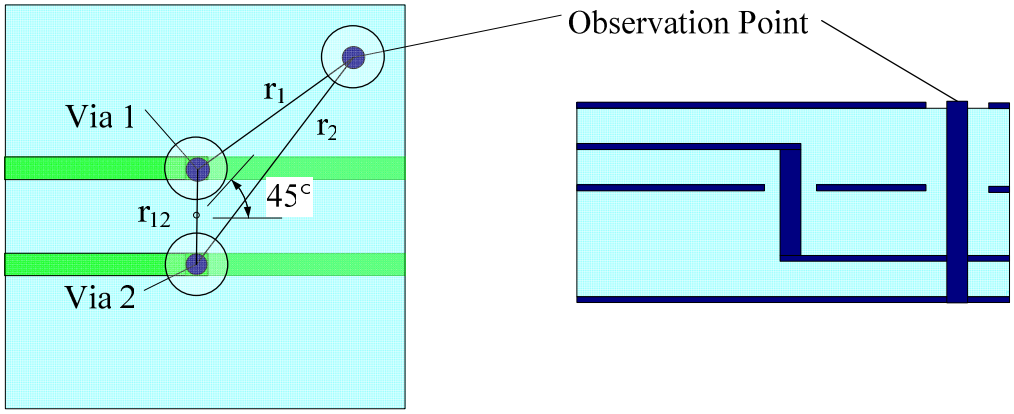


Fig. 3.5. Two PPWs with differential vias and a probe via [16].

The equivalent circuit of this structure is shown in Fig. 3.6, which is based on the model in [3]. The additional component of this circuit is the model for the probe via. The discontinuity effect due to the vias in the stripline signal path is represented by the conventional Π equivalent circuit, as explained in the previous sections. However, the couplings between the via barrels are ignored in the model to focus on the couplings through the PPW environments. As well, the spacing between the two striplines is set to more than three times the width of the striplines. Therefore, the coupling between the striplines can be ignored and it is not included in the model. The induction of currents on the PPWs and the reciprocal couplings of the voltage fluctuations on the PPWs back to the vias are

represented by the dependent current and voltage sources as before. There are two parallel-plate waveguides and, for each, a separate set of *Y* networks and terminating impedance elements are calculated. The parameters of these components are derived using equations (2-3) to (2-7). The excitation sources are differential signals with equal amplitude and opposite phases. The overall noise is predicted by using superposition in the same manner as explained earlier. At the location of the observation via, the noise voltage on the top parallel plates is $V_{st31}+ V_{st32}$, and is $V_{sb31}+ V_{sb32}$ on the bottom parallel plates. Thus, the total noise voltage at this location is $V_{st31}+ V_{st32}+ V_{sb31}+ V_{sb32.}$

3.3 Simulation results

In the previous section, the general methodology for development of the equivalent circuits for four major types of PDN structures with vias was presented. In this section, a few simple test structures based on these major types are investigated to evaluate the developed models.

In order to verify the proposed models, the *"Y"* and *"Z"* matrices are calculated by developing a simple Matlab code. The equivalent circuits are created in Agilent ADS and transient simulations are performed when appropriate excitation sources are applied. In this manner, noise waveforms at the observation points in time-domain are generated. For validation, the studied structures are simulated using a commercial 3-D full-wave solver, i.e. CST Microwave Studio. The accuracy of the RTL models is demonstrated by comparing the circuit simulation results with those of full-wave simulations.

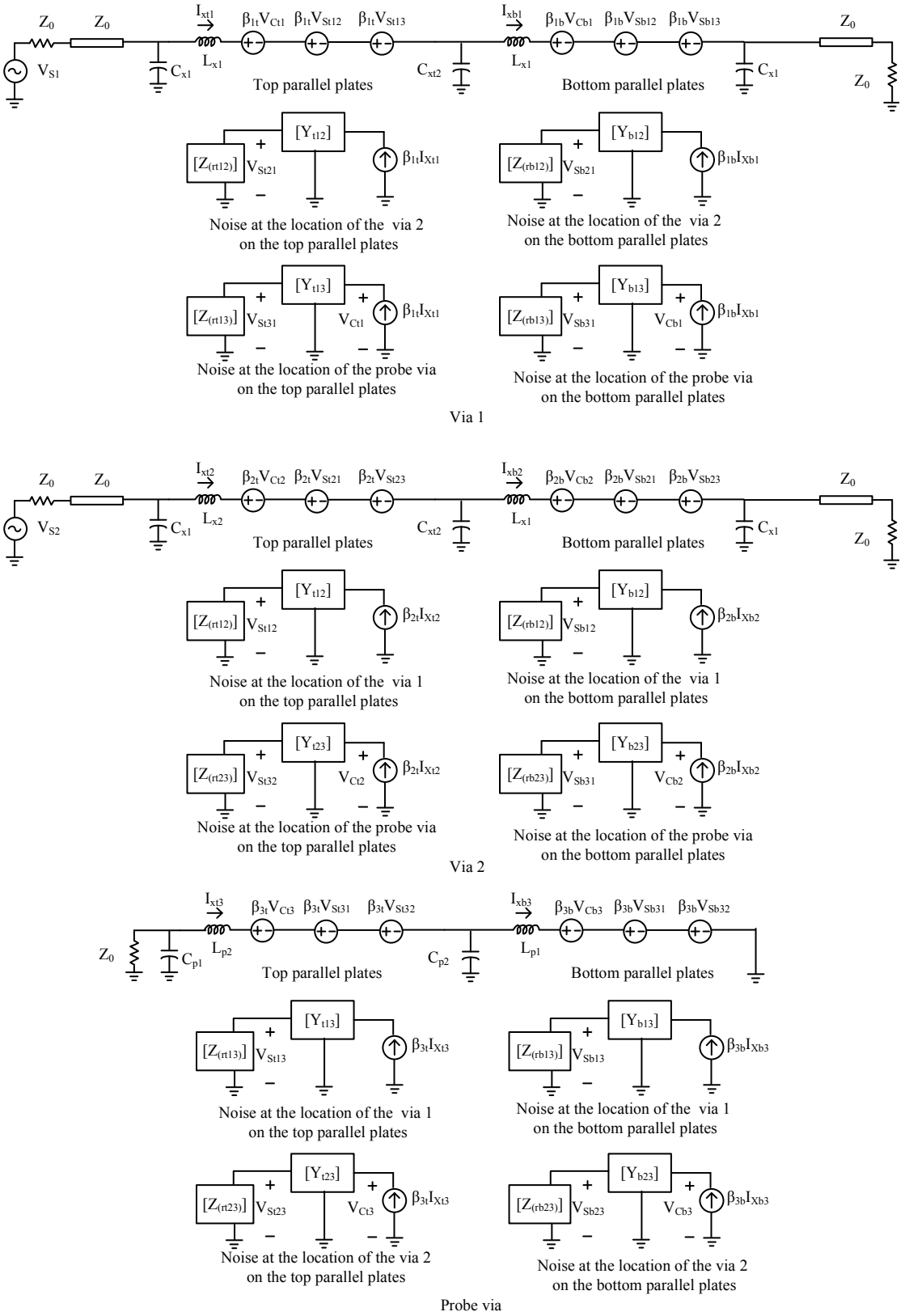


Fig. 3.6. Equivalent circuit of the structure shown in Fig. 3.5.

3.3.1 Parallel-plate PDN with two through vias

In the first case study, the structure in Fig. 3.7 is investigated. This structure is a modification of the structure shown in Fig. 3.1, where a through via is used instead of the buried via. For simulations using the RTL model, the equivalent circuit is the same as the circuit of Fig. 3.2. The parameters in the model are as follows:

$\beta_1 = \beta_2 = 1$, $L_{x1} = L_{x2} = 0.34$ nH, $C_{x1} = C_{p2} = 100$ fF. In calculations of network parameters using the equations (2.3)-(2.7), $\rho = \rho_2 = 20$ mm, $\rho_1 = 0.5$ mm, h = 1.54 mm, $\varepsilon_r = 4.2$ were used. The active via is connected with 50Ω cable to a signal generator with 50Ω internal resistance, and the probe via is connected to a 50Ω input impedance oscilloscope with a 50Ω cable, $Z_o = 50\Omega$. This equivalent circuit is created in Agilent ADS. The excitation source in the simulations generates a step voltage with 0.25 V amplitude and 36 ps (0%-100%) risetime. The board size is assumed to be infinite. Therefore, the reflections from the sidewalls are avoided, and the simulation results only show the first peak of the noise waveform.

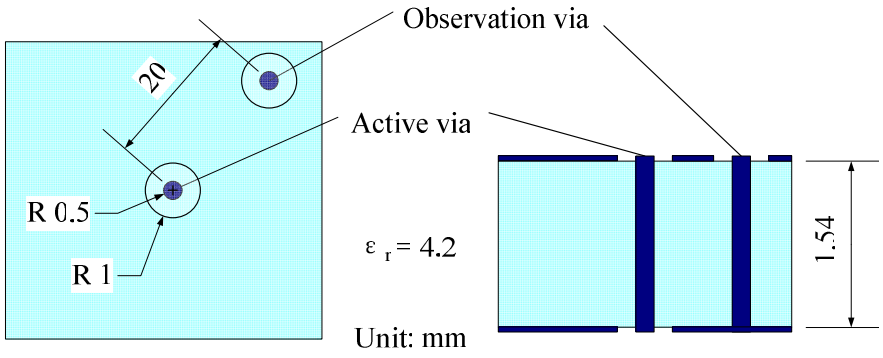


Fig. 3.7. An infinite PPW PDN with active and observation through vias.

Next, the structure of Fig. 3.7 is created in CST Microwave Studio to conduct full-wave time domain simulations. The material of the metal plates and vias are

set as loss copper. The dielectric material is FR4 (ε_r = 4.2, tanδ=0.02). The boundary conditions of the sidewalls are PML. The launched excitation is the same as the one used in the RTL circuit simulations. This type of source and definition of the conductor and dielectric materials are used for all CST simulations in this chapter.

Fig. 3.8 shows the noise waveforms predicted by the RTL circuit simulations and CST simulations. As can be seen the waveforms match well with the exception of some minor differences. The noise peak predicted by the RTL method is 20.2 mV and 16.12 mV is obtained from CST simulation. The differences can be attributed to the following reasons: 1) In the RTL method, the dielectric is considered lossless and the loss tangent (tanδ) is not included in calculating the network parameters. However, in CST simulations the dielectric is regarded as loss material and the loss tangent is 0.02; 2) In the RTL method only TEM mode is considered while CST is a full-wave solver, thus all modes are calculated.

The simulation time for the RTL method is 4 minutes 30 seconds, and for CST is 1 hour 23 minutes. Both simulations are conducted using the same workstation with Intel Pentium 4 CPU with 2.66 GHz clock frequency and 1.5 GB DDR RAM. It can be concluded that the RTL method predicts the power/ground noise with comparable accuracy while taking much less simulation time.

3.3.2 Adding a decoupling capacitor

The structure shown in Fig. 3.7 is modified to include a decoupling capacitor and a connecting through via. Both distances from the decoupling via to the active via and to the probe via are 10 mm. The structure is simulated using the RTL model shown in Fig. 3.4. The parameters of the model are: $\beta_1 = \beta_2 = \beta_3 = 1$, $L_{x1} = L_{x2} = L_{p1} = 0.34$ nH, $C_{x1} = C_{x2} = C_{p2} = 100$ fF, $Z_o = 50\Omega$, and the decoupling capacitor is 0.01 μF. The excitation source is the same as the one in the previous section.

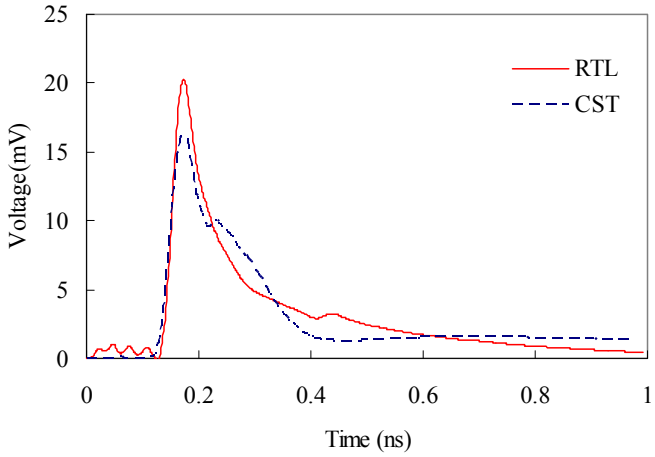


Fig. 3.8. Noise waveforms predicted by RTL circuit simulations and CST simulations when a step excitation is used [250mV step input, 36 ps risetime (0%-100%)].

The simulated noise waveforms at the location of the observation probe are shown in Fig. 3.9 for two cases before and after adding the 0.01 μF decoupling capacitor. The noise peak for the case without the decoupling capacitor is 20.2 mV. However, it decreases to 13 mV when the 0.01μF capacitor is added. Therefore, this decoupling capacitor reduces the noise peak by 36%.

Further simulations show that, if a decoupling capacitor bigger than 0.5 nF is used, both the peak voltage and noise waveform remain almost the same. This means that 0.5 nF decoupling capacitor is enough for suppressing the noise and

higher values cannot improve the suppression. This conclusion is coherent with what is suggested in [3].

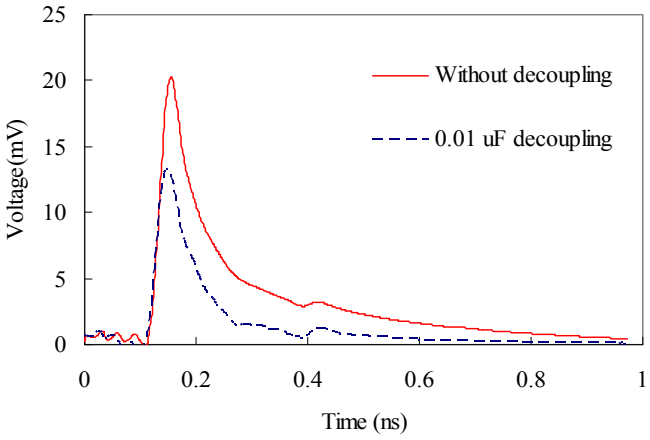


Fig. 3.9. Noise waveforms before and after adding the decoupling capacitor [250mV step input, 36 ps risetime (0%-100%)].

3.3.3 Differential through vias

Fig. 3.10 shows a structure of a PPW with through differential vias and one probe via. The RTL model for this structure is shown in Fig. 3.11, which is similar to the one presented in Fig. 3.6 with some adjustments. The values of the components in Fig. 3.11 are: $\beta_1 = \beta_2 = \beta_3 = 1$, $L_{x1} = L_{x2} = L_p = 0.34$ nH, $C_{x1} = C_{x2} = C_p = 100$ fF, $Z_o = 50\Omega$. The excitation sources are ±0.25 V step voltages with 36 ps (0%-100%) risetime applied to Via 1 and Via 2.

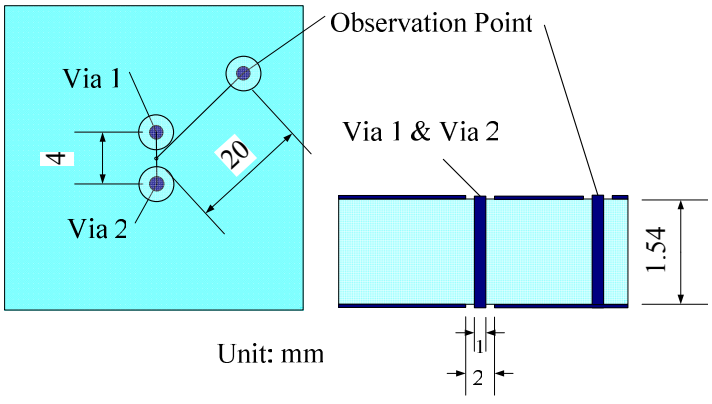


Fig. 3.10 Structure with differential vias and a probe via.

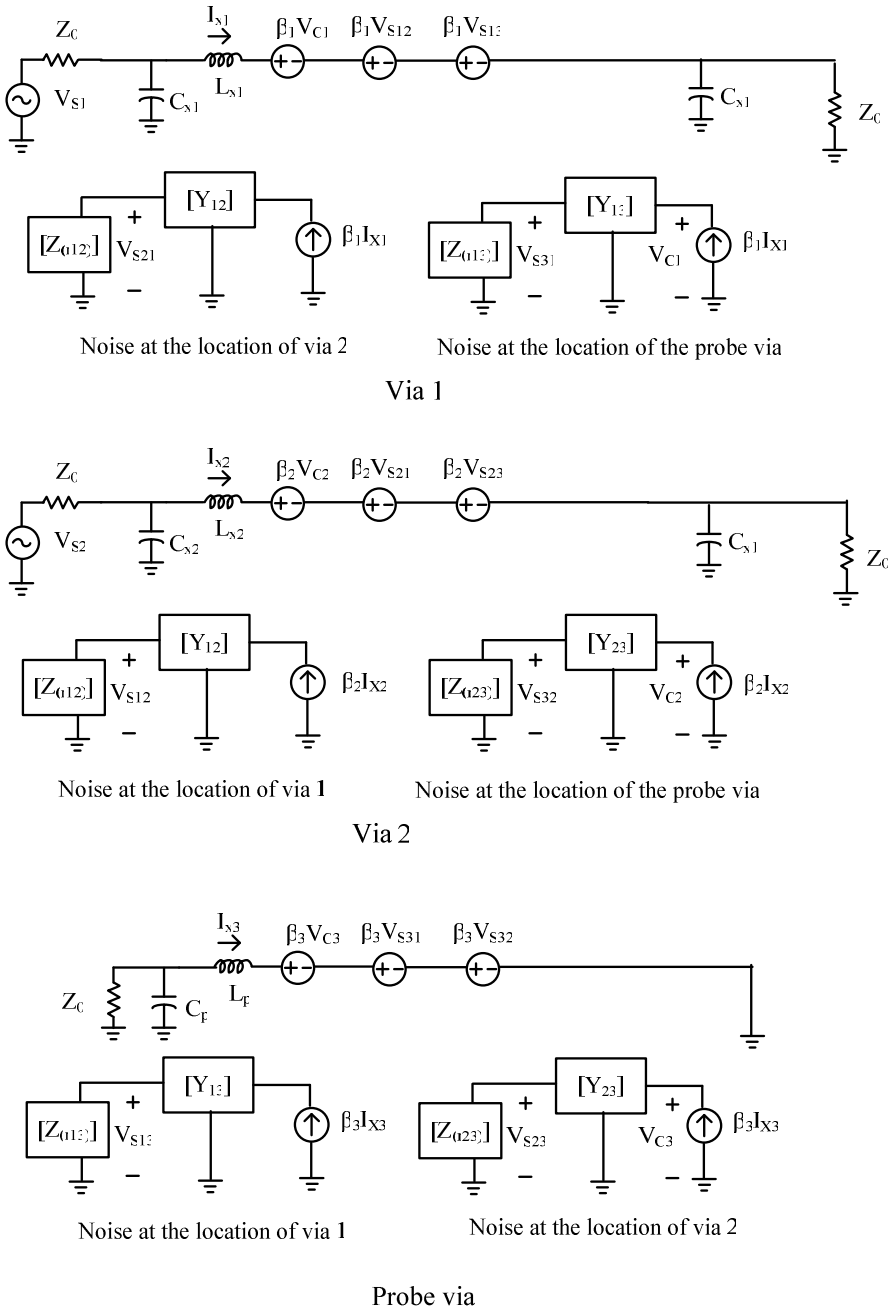


Fig. 3.11. Equivalent circuit of the structure shown in Fig. 3.10.

The simulated noise waveforms by CST and the RTL model are shown in Fig. 3.12. As can be seen, the results are in very good agreement with minor differences. The predicted noise peak is 9.63 mV by CST and is 11.1 mV by the RTL method. Compared with the noise peaks shown in Fig. 3.8, noise suppression

of 40% from the CST simulations and 45% from the RTL method can occur by using differential signalling. It demonstrates that differential structures have a significant effect in suppressing power/ground noise.

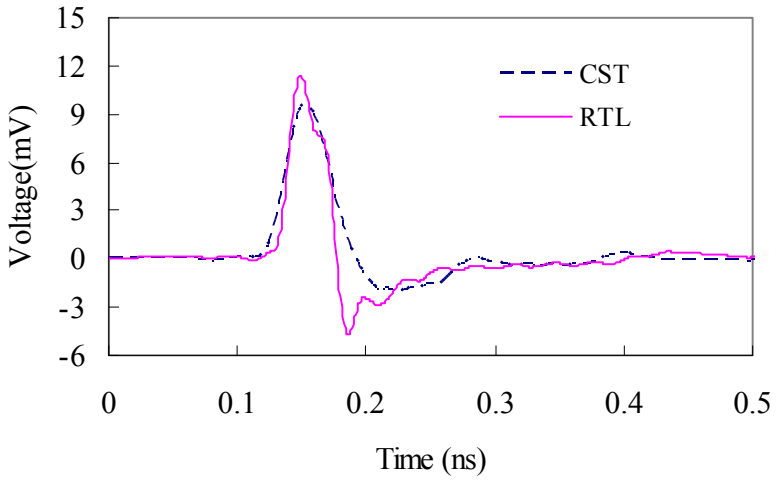


Fig. 3.12. Noise waveforms by the differential vias with the differential excitations [250mV step input, 36 ps risetime (0%-100%)].

3.4 Measurements

To validate the RTL modeling by measurements, a simple double-metal-side board with differential vias at the center was fabricated by using a 30 cm by 30 cm FR-4 substrate with 1.54 mm thickness, as illustrated in Fig. 3.13. The purpose of selecting a relatively large board is to create more delay for reflections from the sidewalls and avoid the overlapping of reflected noise waveforms with the first noise peak. The through differential vias have a 4 mm spacing and the observation probe via is placed 20 mm away from the center. The relative locations of these three vias are the same as those in Fig. 3.10. Therefore, the simulation results and measurements can be compared. Note in Fig. 3.13 that the two active vias are connected in the opposite directions to avoid the connector

assembling problem. This is because the spacing between the two active vias is smaller than the diameter of the SMA connectors.

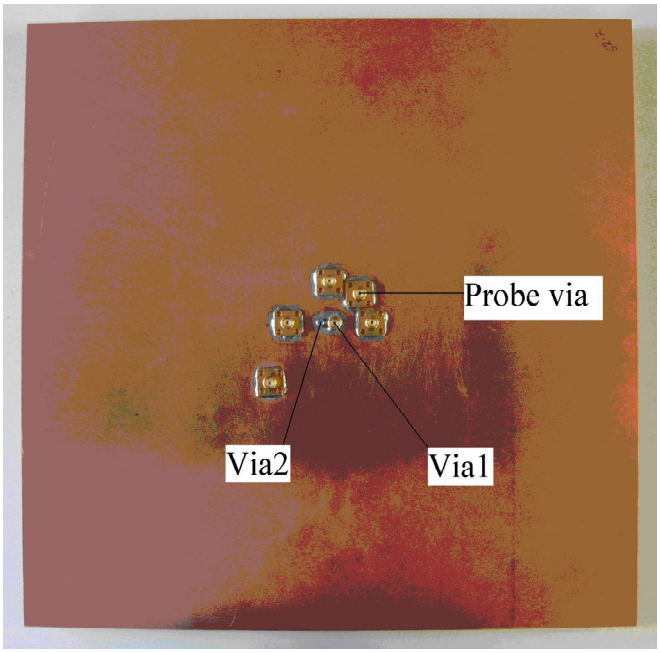


Fig. 3.13. The measurement prototype.

The amplitudes of the differential step signals are ±250 mV, and the risetime is 29 ps (10%-90%), which is approximately equivalent to 36 ps for a 0%-100% risetime. The source signals are generated by a Tektronix TDS8200 oscilloscope with an 80E04 electrical sampling module, and transferred to the board by two same-length cables.

The measurement waveform at the observation probe is shown in Fig. 3.14 along with two simulated waveforms from the RTL method and CST simulations. These waveforms show the accuracy in the prediction of the first noise peak from model simulations. As expected, a better agreement exists between measurements and the CST simulation, while the RTL method offers the lowest possible cost in noise prediction. Due to reflections from the edges of the board, the rest of the

measured waveform is not consistent with the simulated results, as the board size is assumed infinite in the simulations.

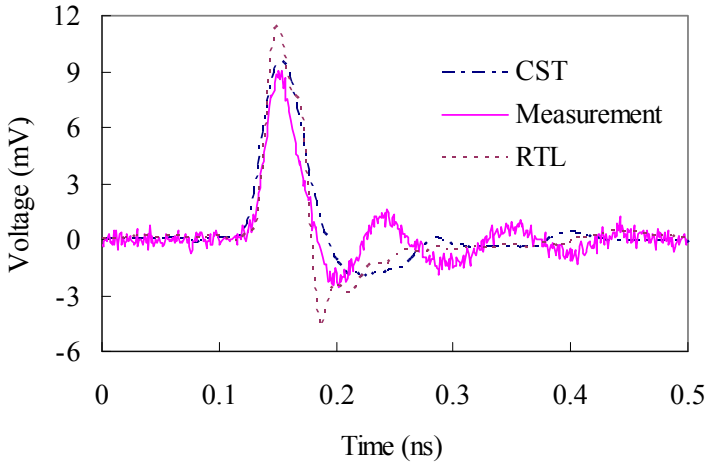


Fig. 3.14. Noise waveforms obtained from CST and RTL model simulations and measurement [250mV step input, 29 ps risetime (10%-90%)].

3.5 Global circuit simulation using RTL modeling technique

To investigate the application of the RTL method in global simulation of high-speed circuits, a typical FPGA circuit is simulated in Agilent ADS. The FPGA driver and receiver are interconnected by differential interconnects. To model the FPGA for simulations, the SPICE model of the transceiver of *Stratix II GX* FPGA from Altera Corporation is used. *Stratix II GX* family FPGA devices include 4 to 20 high-speed serial transceivers and each device has a logic array. The transceiver can process up to 6.375 gigabits per second (Gbps) data rate. The devices are used in high-speed data communication applications and in their backplane interfaces [66]. The input signal to the FPGA is a 6 Gbps pseudo random bit sequence (PRBS). The FPGA driver and receiver have differential input and output circuits.

Pseudo current mode logic (PCML) signals are launched to the interconnects and pass through the differential vias. PCML is a high-speed differential architecture derived from current mode logic and is capable of speeds in excess of 2 Gbps over a standard PCB [67]. Recently, a version of PCML was introduced that operates with 1.2/1.5 V supply voltage thus facilitating even faster speeds. PCML has been widely adopted for use at data rates of 2.5 Gbps and above [67], and is utilized in a variety of applications including networking and data communications.

The structure of Fig. 3.10 is the considered physical interconnect structure for this FPGA system. Fig. 3.15 shows the equivalent circuit of this FPGA system including the RTL model for the differential interconnects. Note the model in the rectangular block is basically Fig. 3.11 except for the sources and loads. V_{in+} and V_{in-} are the input voltages applied to Via 1 and Via 2 (top plate is the reference), respectively. Similarly, V_{out+} and V_{out-} are the voltages at the other ends of Via 1 and Via 2, respectively. V_{probe} is the noise voltage at the observation point. The generated data rate of the FPGA is 6 Gbps and the risetime is 10 ps (0%-100%). The SPICE models of the driver and the receiver, and the RTL model of the structure are all imported to Agilent ADS for transient simulations.

Fig. 3.16 and Fig. 3.17 present the input and output voltage waveforms of the differential via structure. It can be seen that the output waveforms have a small delay with respect to the input waveforms, and they differ slightly from the input waveforms due to the via discontinuity.

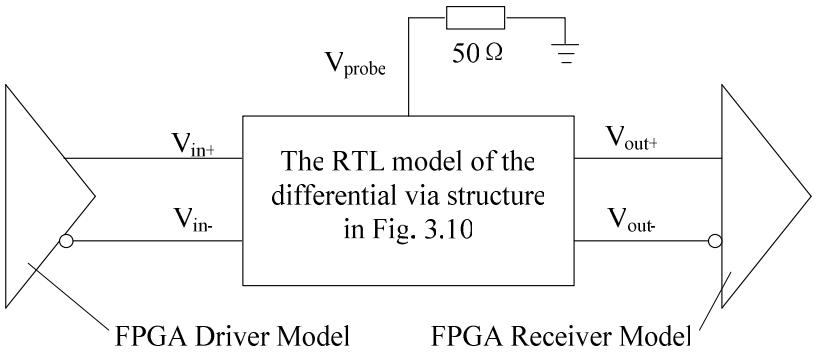


Fig. 3.15. Block diagram of the model of the FPGA system interconnected with differential vias which are represented by the RTL model.

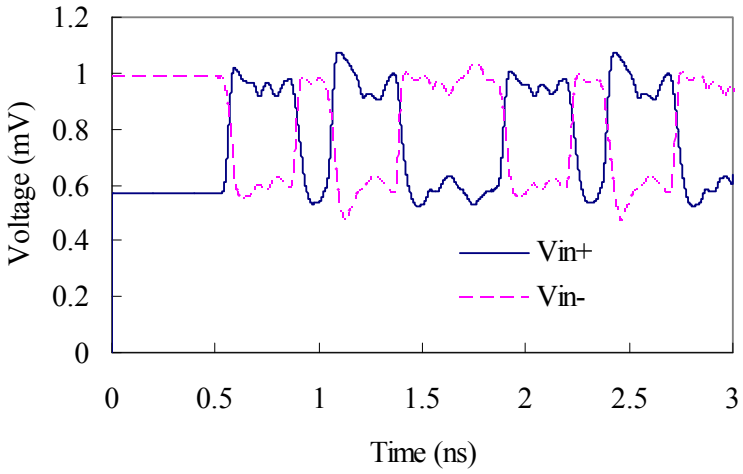


Fig. 3.16. The input waveforms of the differential vias.

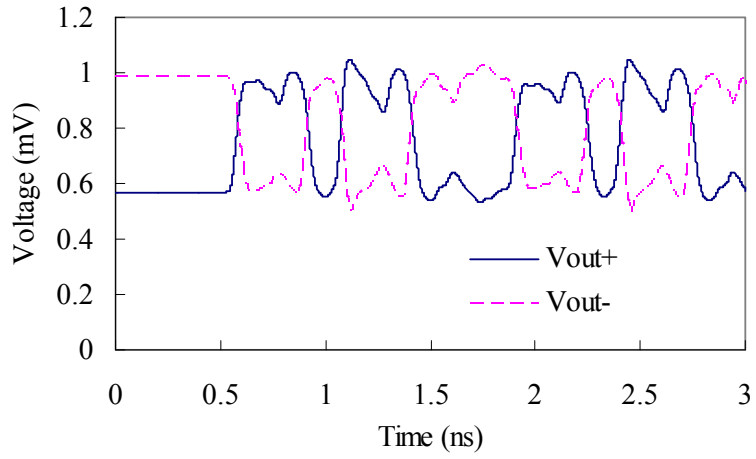


Fig. 3.17. The output waveforms of the differential vias.

To evaluate the RTL method in this application, the system simulations are also conducted using *S*-parameter results from the CST Microwave Studio simulation of the structure shown in Fig. 3.10. From the CST solver, a five-port *S*-parameter matrix is obtained to represent the structure. The ports are defined at the inputs and outputs of the differential vias and the observation via. Fig. 3.18 shows the block diagram of the model of the FPGA driver and receiver and the *S*-parameter matrix. The SPICE models of the driver and the receiver, as well as the *S*-parameter matrix, are ported to Agilent ADS and transient simulations are performed.

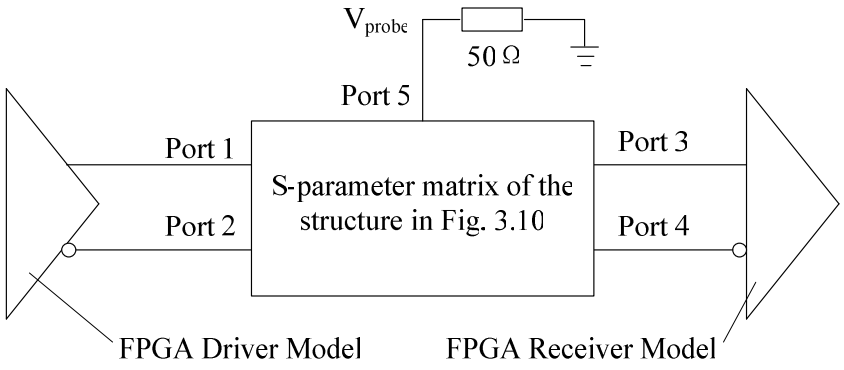


Fig. 3.18. Block diagram of the model of the FPGA system interconnected with differential vias, which are represented with S-parameter matrix from the CST simulation.

Fig. 3.19 shows the noise waveforms simulated by the RTL method and the CST method at the observation point in the structure. The four positive pulses are related to the four rising edges of the V_{in+} (shown in Fig. 3.16.), because the waves excited by Via 1 arrive at the observation point first. The waveforms match well, but the magnitudes of the voltage spikes are different. The peaks predicted by CST are about 25% less than those by the RTL model. This is attributed to the

full-wave calculations in CST solver, as opposed to single mode consideration in the RTL model as mentioned before in Section 3.3.

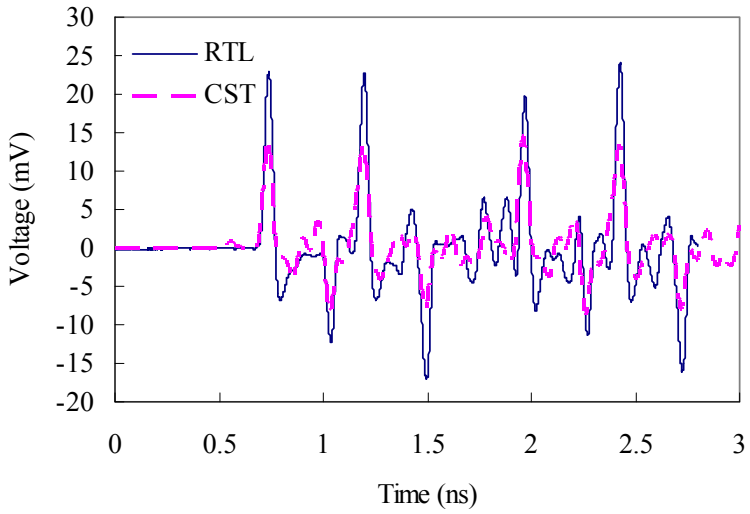


Fig. 3.19. Noise waveforms at the observation point predicted from global system simulations using the RTL model and the S-parameter file from CST.

3.6 Conclusions

In this chapter, the RTL method for modeling parallel-plate PDNs containing vias is presented. The parallel plates can be represented by the network elements, which are derived from radial transmission line theory. In this approach, the couplings between parallel plates and vias, and crosstalk between vias, are included in the forms of circuit components. The developed models are versatile and can be applied to a variety of structures. Several typical cases are studied including a single active via followed by adding a probe via. Structures with a decoupling capacitor and differential vias in multilayer environments are investigated. All these models can be conveniently imported to Agilent ADS to perform transient simulations.

To evaluate the RTL method, full-wave simulations of the studied cases are also performed using CST Microwave Studio. From comparisons and analysis of the simulated results, a few conclusions can be reached: 1) the RTL method is relatively accurate because the predicted noise waveforms match well with those predicted by CST simulations and measurement results; 2) the RTL method is much faster and less costly in terms of computational resources in comparison with the full-wave simulations; 3) both adding decoupling capacitor and employing differential signalling are effective ways to suppress power/ground noise.

The RTL models can be ported to commercial simulators such as Agilent ADS and enable global system simulations. This capability is demonstrated by the simulations of the sample FPGA system.

With the increasing via number, the RTL model becomes more complex and the simulation time will increase, which would be a drawback for this approach. Furthermore, for simulations of finite-size board sizes, images of the vias must be included in the models, which also increase the complexity of the circuit. In the next chapter, the cavity method is investigated, which is also suitable for the analysis of finite size parallel-plate PDNs for predicting power/ground noise.

Chapter 4 Noise prediction using cavity method

4.1 Introduction

In this chapter, another analytical method is utilized to represent a parallel-plate PDN. First, a cavity model for a single layer PPW is introduced and extended to a multilayer structure. Then, these models are validated by comparing them with the simulation results obtained from two 3-D full-wave simulators. The developed models are employed to conduct parametric studies of PDN noise in a differential via structure when varying the spacing between the vias and the excitation risetime. Furthermore, the global system simulations of a FPGA system including the PDN structure are performed and the noise in power/ground planes is predicted. In addition, measurements on a test structure with differential through vias are presented and compared with the simulation results of the cavity method.

4.2 Modeling of parallel-plate PDNs using cavity method

The cavity method has been introduced in Chapter 2. In this chapter, two parallel-plate PDN structures are modeled using this cavity approach: one contains a single dielectric layer and the other is a multilayer structure. Ansoft HFSS and CST Microwave Studio full-wave simulations are used for validation of the developed models where frequency-domain impedance profiles are generated and compared.

4.2.1 Single layer parallel-plate PDN

A single-layer PPW with two through vias is shown in Fig. 4.1. The dimensions of the structure are as follows: both *a* and *b* are 10 mm, the dielectric thickness *d* is 0.3 mm, the metal thicknesses are 35 μm, the spacing between the two via centers is 2 mm, the radii of the vias are 0.25 mm, the widths of the clearances between vias and planes are 0.25 mm, and the relative permittivity of the dielectric is 4.2. To obtain the self- and transfer impedance at the locations of the vias, two ports are defined at the positions of the vias.

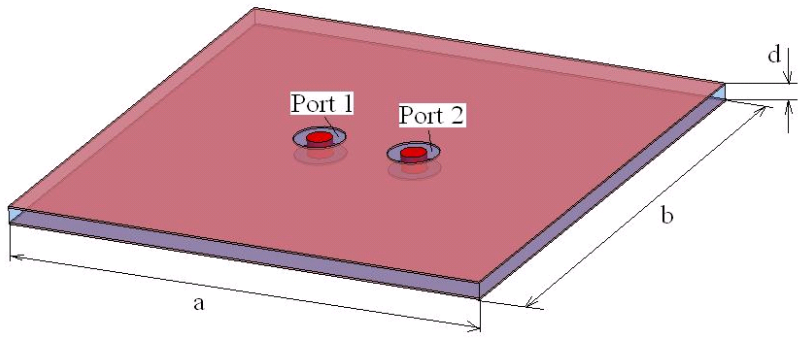


Fig. 4.1. Structure of a single-layer PPW with two through vias.

The equivalent circuit of this structure containing the network file of the PPW obtained from cavity analysis is shown in Fig. 4.2. The bottom layer is assumed to be the reference ground. C_1 and C_2 represent capacitance between the top end of the via barrels and the top conductor layer in the anti-pad region. They are calculated using a quasi-static commercial simulator, i.e. Ansoft Q3D Extractor, to be 35 fF. *Zo*=50 Ω is the standard termination in a measurement system.

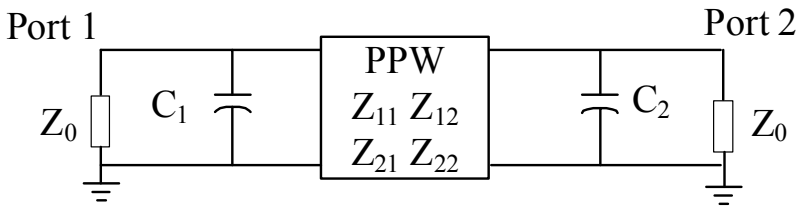


Fig. 4.2. Circuit model of the single layer PPW structure with two through vias.

If PEC boundary conditions are considered for the PPW sidewalls, the impedance matrix in Fig. 4.2 is calculated using Equation (2.18). The circular ports are approximated by square ports with the same perimeter. The circuit in Fig. 4.2 is simulated in Agilent ADS and the resultant self-impedance at Port 1 is shown in Fig. 4.3.

The same structure is also simulated in Ansoft HFSS and CST Microwave Studio. The obtained results are also shown in Fig. 4.3 for comparisons. As one can see, the two 3-D full-wave simulators generate very similar impedance profiles as expected. The self-impedance from the cavity model closely matches the full-wave results up to 30 GHz but the differences increase beyond this frequency. This is attributed to the following factors: 1) the effects of the via barrel are ignored in the cavity model while they are included in the full-wave solvers; 2) the cavity method uses a finite summation of three thousand terms; 3) the representation of the capacitance in the via anti-pads with the two capacitors is an approximation. The simulation time by HFSS is 2 minutes 52 seconds, the time by CST is 11 minutes 30 seconds, and the time by the cavity method is 1 minute 27 seconds. All are based on a computational platform of Pentium 4 with 2.66 GHz CPU and 1.5 GB RAM. Therefore, the cavity method is much faster than the full-wave simulators.

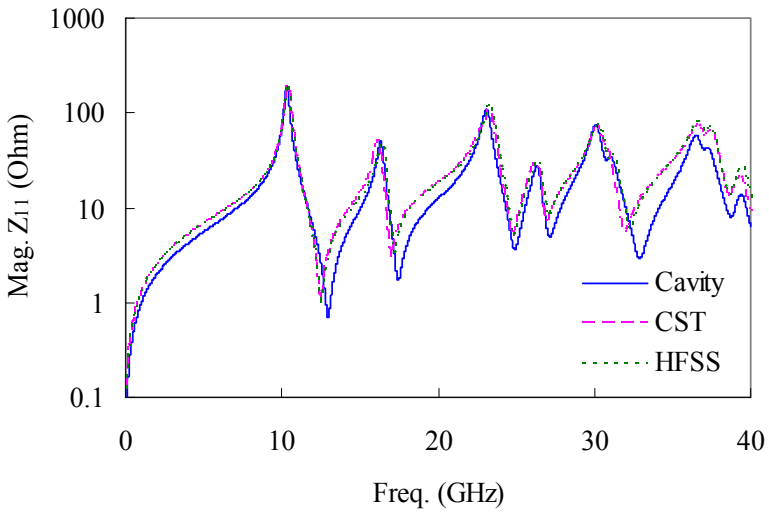


Fig. 4.3. Self-impedance at Port 1 of the single layer structure with PEC boundary conditions.

The transfer impedance from Port 1 to Port 2 is shown in Fig. 4.4. Similarly, the impedance curves obtained from the three methods closely match up to 30 GHz.

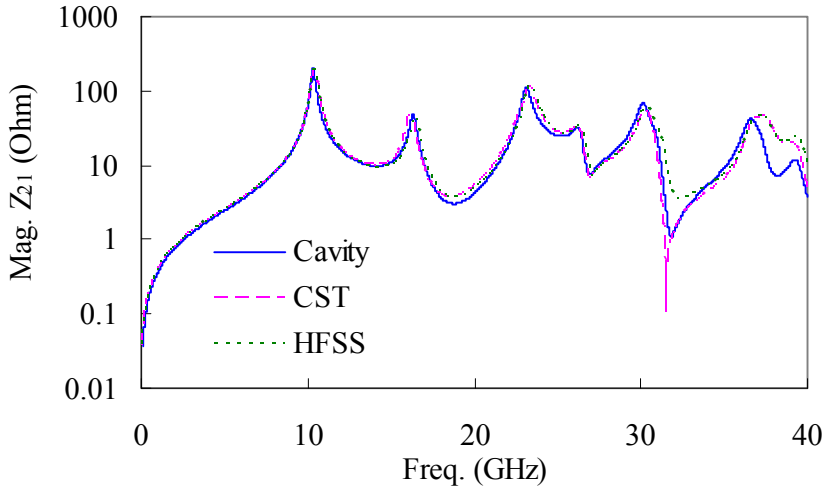


Fig. 4.4. Transfer impedance of the single layer structure with PEC boundary conditions.

As for PMC boundary conditions, similarly, the impedance matrix of the PPW is calculated from Equation (2.17), and the circuit model in Fig. 4.2 is simulated

in Agilent ADS. The self-impedance at Port1 and transfer impedance Z_{21} are compared with the results predicted by 3-D full-wave HFSS and CST simulators in Fig. 4.5 and Fig. 4.6, respectively. It can be observed that they match very well up to 30 GHz and above.

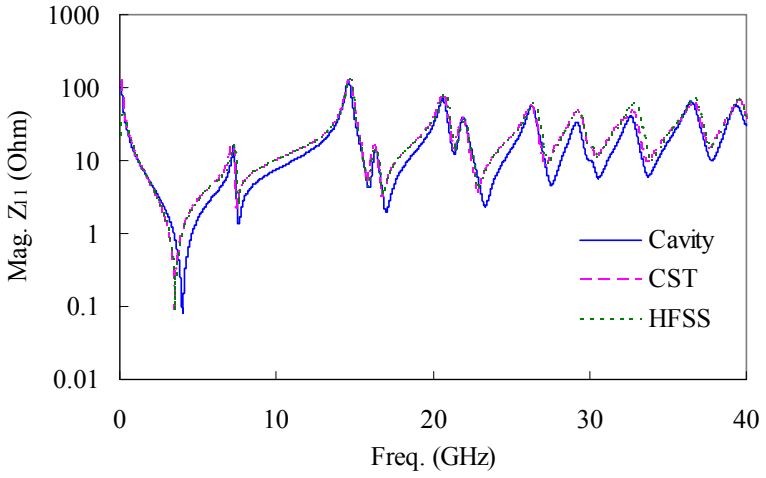


Fig. 4.5. Self-impedance at Port 1 of the single layer structure with PMC boundary conditions.

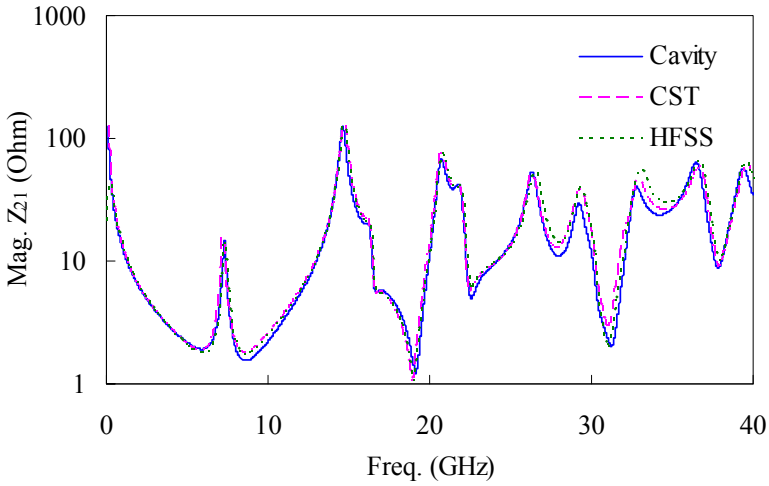


Fig. 4.6. Transfer impedance of the single layer structure with PMC boundary conditions.

4.2.2 Multilayer parallel-plate PDN

The model for a multilayer structure is implemented by cascading the individual models for single layer PPW structures while taking the parasitic capacitance between vias and metal planes into consideration [3], [61].

A five-layer board with two through vias is considered and simulated with both PEC and PMC boundary conditions, as illustrated in Fig. 4.7. The parallel plates exist in the dielectric interfaces. All five dielectric layers are the same material. The dimensions of the structure are: both *a* and *b* are 10 mm, d_1, d_2, *d4*, and d_5 are 0.3 mm, d_3 is 0.2 mm, the metal thicknesses are 35 μm, the spacing between the two via centers is 2 mm, the radius of each via is 0.25 mm, the widths of the clearances between via barrels and surrounding metal planes are 0.25 mm, and the relative permittivity of the dielectric is 4.2.

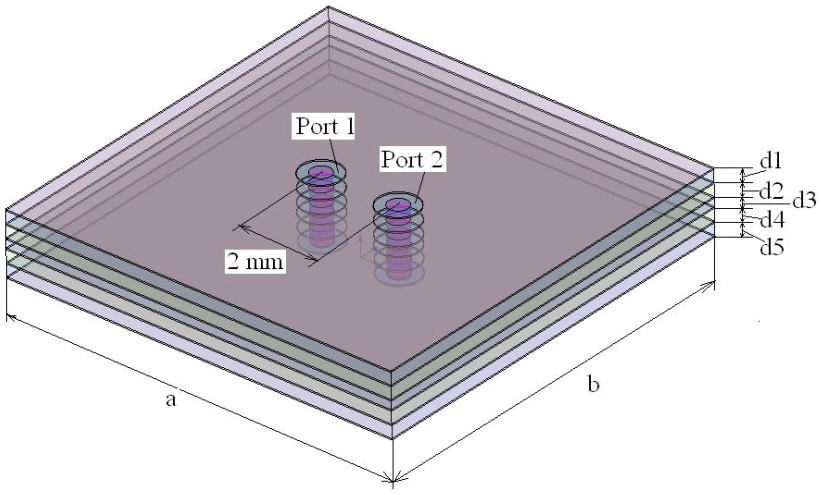


Fig. 4.7. Diagram of a multilayer board composed of stacking up of five PPWs.

The cavity model for this multilayer structure is shown in Fig. 4.8. In this circuit, the bottom conductor layer is assumed to be the reference ground, and parasitic capacitance in the anti-pads is added to the PPW model of each layer in

order to get more accurate simulation results. The values of these capacitors are calculated by Ansoft Q3D Extractor. The impedance matrices of PPWs are derived using the single summation Equation (2.17) or (2.18) depending on the boundary conditions of the sidewalls. The C_{31}, C_{32}, C_{41}, and C_{42} are calculated to be 39 fF, and the other capacitors are found to be 46 fF. Z_o is 50 Ω.

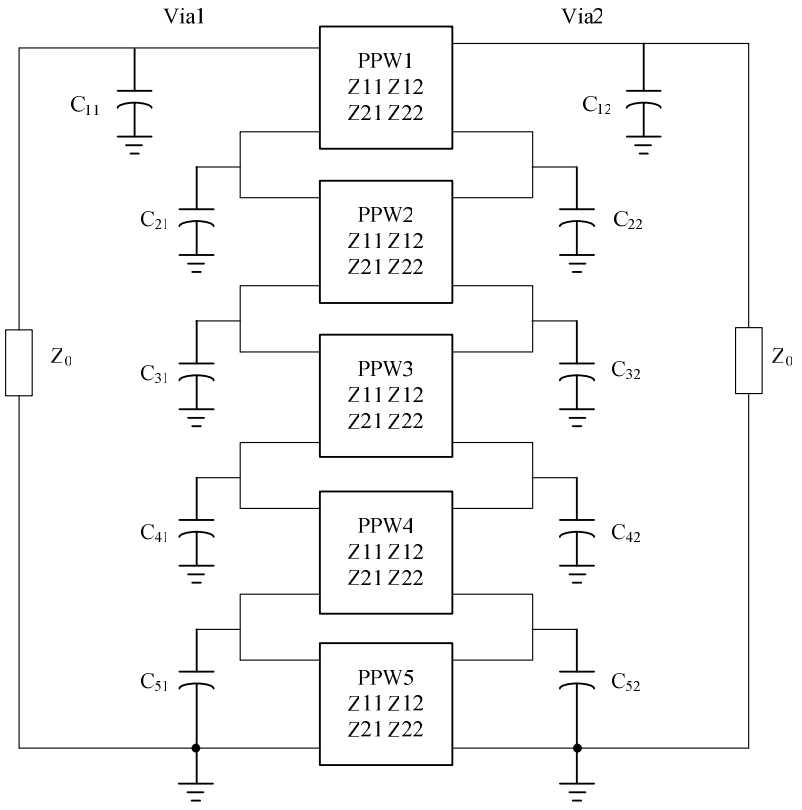


Fig. 4.8. Equivalent circuit of the structure shown in Fig. 4.7.

When the PEC boundary conditions are considered, the self-impedance magnitude at Port 1 is generated as shown in Fig. 4.9. Fig. 4.10 illustrates the transfer impedance Z_{21}. Both results are consistent with the 3-D full-wave simulations obtained from the two solvers up to about 15 GHz. As mentioned in the single PPW layer case, the differences are due to the approximations in the

summations (three thousand terms are computed) and to ignoring the physical via barrel in the cavity simulations.

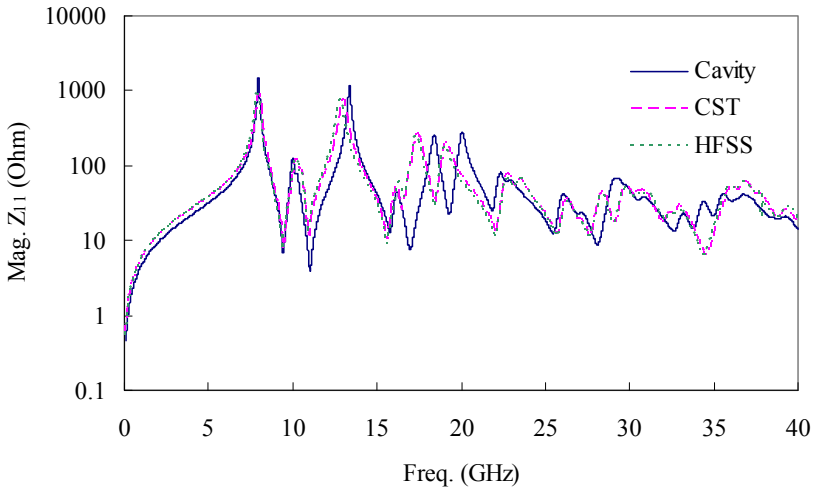


Fig. 4.9. Self-impedance at Port1 of the structure shown in Fig. 4.7 with PEC boundary conditions.

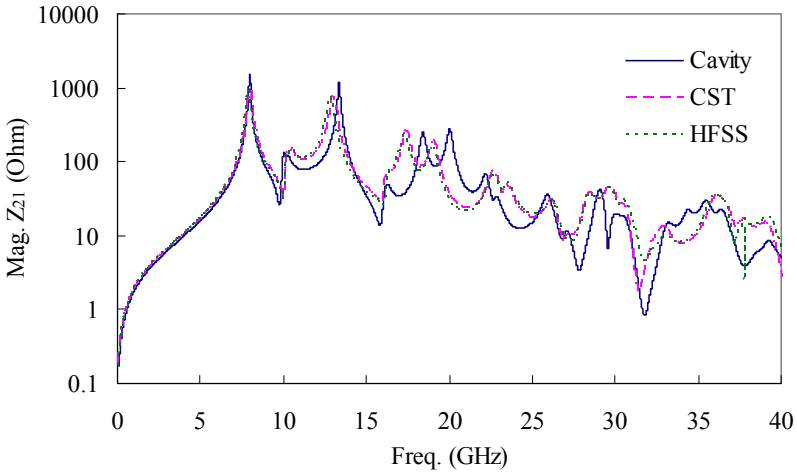


Fig. 4.10. Transfer impedance of the structure shown in Fig. 4.7 with PEC boundary conditions.

Next, PMC boundary conditions are employed. The magnitude plots of Z_{11} and Z_{21} are generated by these three methods as shown in Fig. 4.11 and Fig. 4.12, respectively. It can be seen that the simulation results by the cavity model match

quite well with those of the full-wave solvers up to 20GHz in this case. The simulation time by HFSS is 8 minutes 42 seconds, the time by CST is 1 hour 16 minutes 14 seconds, and the time by the cavity method is 4 minutes 27 seconds. All are based on using the same computational platform mentioned before.

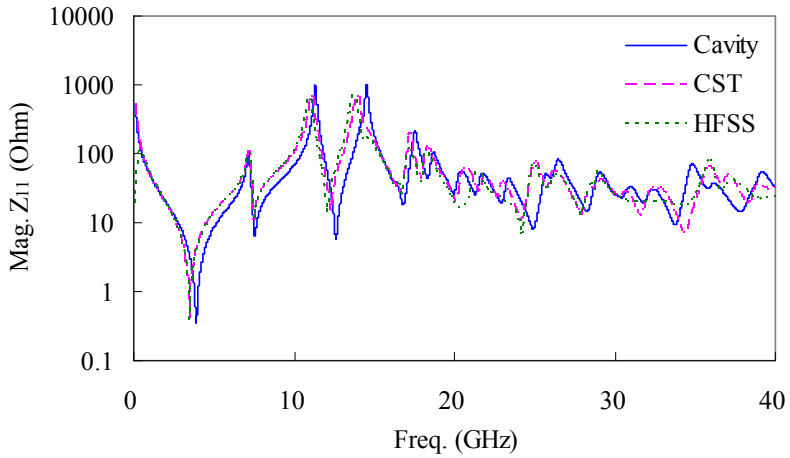


Fig. 4.11. Self-Impedance at Port 1 of the structure shown in Fig. 4.7 with PMC boundary conditions.

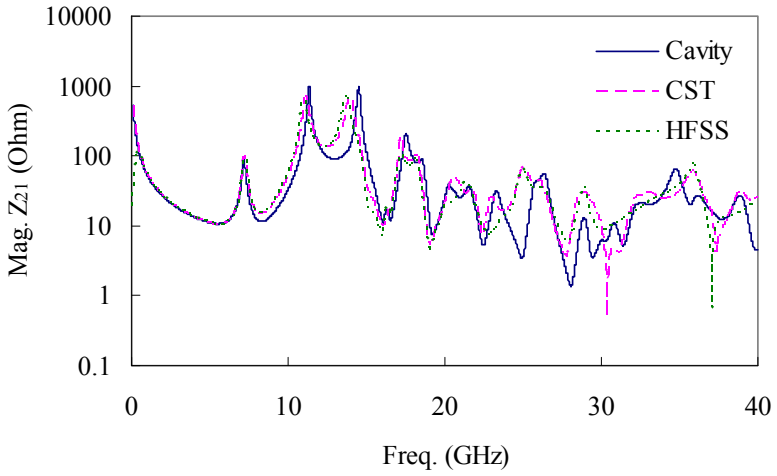


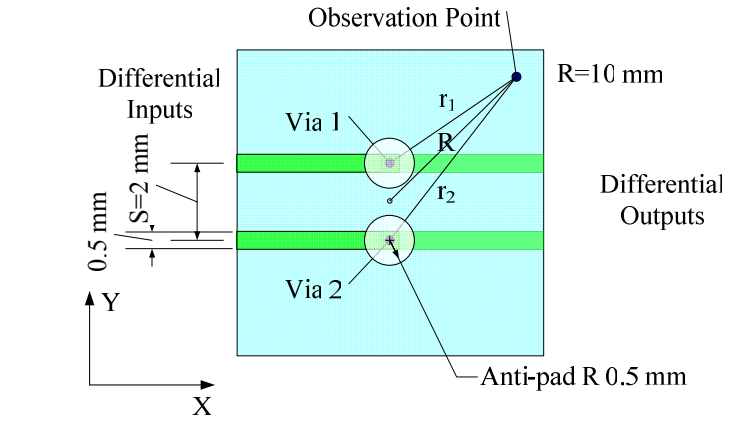
Fig. 4.12. Transfer impedance of the structure shown in Fig. 4.7 with PMC boundary conditions.

From the simulations, it is demonstrated that the cavity method has comparable accuracy to that of the full-wave methods. However, the 3-D full-wave simulations can be very time consuming — possibly taking hours to finish — depending on the board dimensions. A typical simulation of a similar structure using the cavity method finishes within a few minutes. In the cavity method, the simulation time only depends on the number of ports.

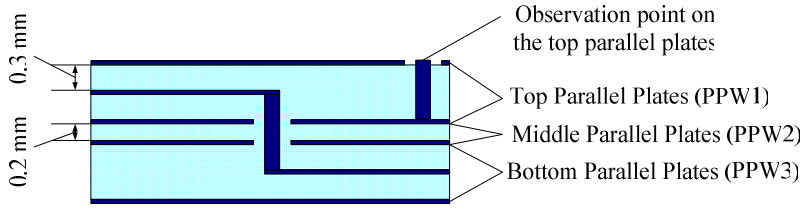
4.3 Modeling of differential vias in a multilayer PDN

To study the effectiveness of differential structure parameters for noise suppression, a multilayer structure shown in Fig. 4.13 is designed. This differential interconnect geometry contains two pairs of striplines in different layers of the PCB. The stripline pairs are interconnected by two buried vias that penetrate through two reference voltage planes; therefore, they potentially excite the PPW modes in all three configured parallel plates. The dimensions of the striplines and thicknesses of the dielectrics are designed to achieve 50 Ω characteristic impedance as marked in the figure. The center-to-center spacing between the striplines is 2 mm, which is three times the width of each stripline. Therefore, the couplings between them can be ignored [68]. The observation point is on the top plane and 10 mm away from the center of the board. Only the noise in the top PPW is monitored. PDN noise in other PPW layers can be investigated in the same manner if needed. As before, since the first noise peak contains the main characteristics of the noise signature, it is focused to investigate the first peak in all simulations [3]. The board size is one meter by one meter, which is

large enough to avoid reflection from the sidewalls overlapping with the first peak in the noise waveforms. In all of the cavity and full-wave simulations, PMC boundary conditions are applied for the sidewalls.



(a) Top view



(b) Side view

Fig. 4.13. Multilayer PPWs with buried differential vias [16].

The cavity model of the structure is developed as shown in Fig. 4.14 [16]. Since the observation probe is a through via in the top PPW, the top PPW can be modeled with a 3 by 3 impedance matrix. The three ports are located at the positions of Via 1, Via 2, and the probe via. The other two PPWs have only 2 ports at the locations of Via 1 and Via 2, thus each PPW is modeled with a 2 by 2 impedance matrix. The dependent current and voltage sources present the couplings between the vias and PPWs as explained in Chapter 2. The coefficient β

of each PPW is obtained from the ratio of the via length to the pertinent PPW thickness. Thus, in the top and bottom PPWs, β is 0.5, whereas in the middle PPW, β is 1. Via 1 and Via 2 are each represented by the Π-type model described in Chapter 2. For simplification, the probe is only represented by a 50 Ω resistor and the model of the via itself is not included. The capacitor values are obtained from Ansoft Q3D Extractor simulations. The inductors are calculated by Equation (2.10).

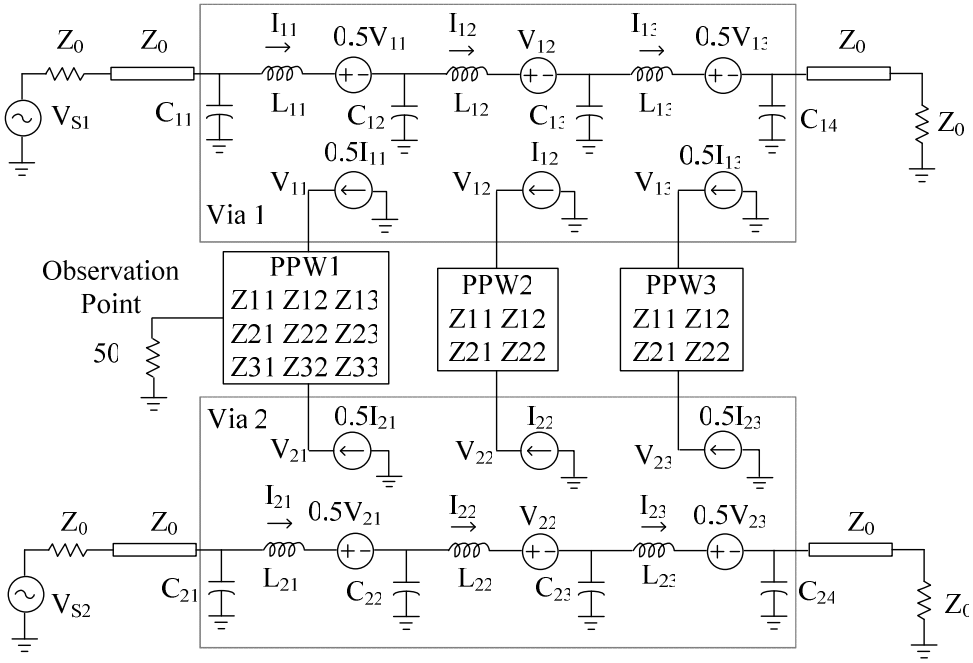


Fig. 4.14. Equivalent circuit including sources and loads for the multilayer PPWs with buried differential vias.

4.3.1 Comparison of noise generated by a single via and differential vias

To measure the effectiveness of the differential signalling in the suppression of the PPW noise, the induced differential noise peak is compared to the noise peak generated by only one via. In differential signalling simulations, the inputs to the

striplines are ±1 V step signals with 115 ps (10%-90%) risetime. In single via simulations, only Via 1 in the structure of Fig. 4.13 is excited by the 1 V step signal with 115 ps (10%-90%) risetime. The source V_{s2} attached to Via 2 is set to 0 volt and both ends of the stripline are still terminated to 50 Ohms. The structure layouts and models for the two simulations are identical. The impedance matrices of the PPWs are calculated using Equation (2.17). The simulation results are shown in Fig. 4.15. It can be seen that the noise peak is 27.7 mV in single via (Via 1) excitation, which is about ten times higher than the noise peak of 2.42 mV obtained in differential excitation of two vias. Therefore, it can be confirmed again that differential signalling can significantly reduce the noise in comparison with single-ended routing.

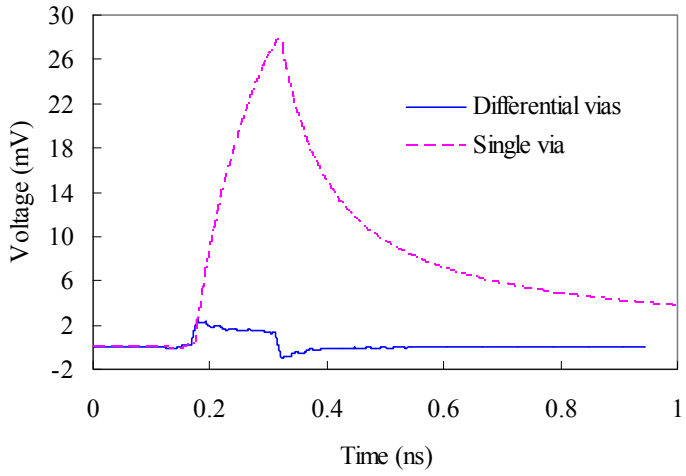


Fig. 4.15. Noise waveforms by a single and differential excitation of striplines shown in Fig. 4.13 at the labelled observation point [1 V / ±1 V step input, 115 ps risetime (10%-90%)].

4.3.2 Changing the spacing between the vias

It is shown in [69] that the noise suppression can be further improved by reducing the spacing between the vias. To verify this by the cavity model, the

center-to-center spacing between the two differential vias in Fig. 4.13 is changed from 1 mm to 4 mm by 1 mm steps, while the striplines are excited by the same step voltage sources in all cases. The predicted noise waveforms on the top parallel plates from the cavity method equivalent circuit simulations are shown in Fig. 4.16. It can be observed that the noise peak obviously diminishes when decreasing the spacing between the vias. This is due to the fact that the arrival times of the opposite phase parallel plate modes at the observation point become closer for smaller via spacings, and more effective out phase interaction happens. The noise peak obtained from circuit simulations is 4.5 mV for 4 mm spacing, and 1.4 mV for 1 mm spacing, which is only 31% of the 4 mm spacing case. Therefore, higher power/ground noise suppression is achieved.

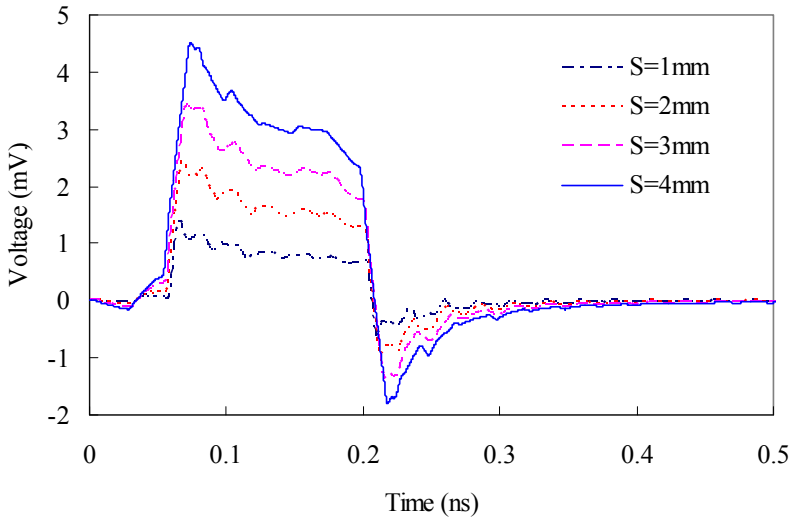


Fig. 4.16. Noise waveforms on the top PPW when different spacings between vias are used [S = 1mm, 2mm, 3mm, 4mm; ±1 V step input at the striplines, 115 ps risetime (10%-90%)].

4.3.3 Changing the risetime of the excitation signals

In another set of transient simulations, the effect of varying the risetime of input excitations on noise suppression is investigated. As explained in [3], the

coupling to the PPW noise becomes stronger when the input risetime (or falltime) decreases, as more significant high frequency components exist in the respective spectrum. This is apparent from the differential noise waveforms shown in Fig. 4.17, where the PPW noise is generated for three different risetimes t_r: 200 ps, 115 ps and 40 ps (all in 10%-90%). It can be seen that the noise peak induced by a step voltage of 40 ps risetime is 4.2 times larger than the noise peak that resulted from a step input with a 200 ps risetime. The results indicate that the shorter risetime induces the larger noise peak. This is due to the fact that, for the 40 ps risetime case, the noise waveforms generated by Via 1 and Via 2 become very narrow. Therefore, when the noise excited by Via 2 arrives at the observation point, the noise excited by Via 1 has reached and almost passed its peak and cannot be fully cancelled by that of Via 2. As a result, for the same geometry, the effectiveness of noise suppression depends on the risetime of the differential inputs.

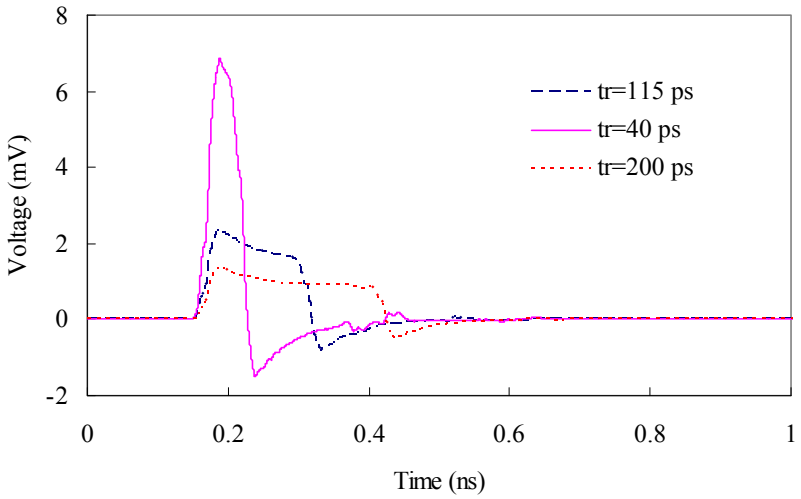


Fig. 4.17. Noise waveforms on the top PPW of the differential via structure when the input risetime is varied (±1 V step inputs; t_r=40 ps, 115 ps, 200ps, 10%-90%).

4.4 Generating noise map on the power/ground planes

Differential noise signature is determined by the two noise waveforms generated by the individual vias. The noise peak value is a function of the difference between the arrival times of the PPW modes excited by the differential vias at the observation point. Therefore, the noise peak value at different locations on the power/ground planes is related to the location of the observation point. The noise distribution on the power/ground planes is called the noise map [70].

The difference between the arrival times of the two noise waveforms is referred to as delta delay (Δr) for brevity [16]. The loci of the points with the same delta delay are hyperbolic functions [16]. Two groups of points are considered to generate the noise map in this section: one is on a circumference of a circle centred at the midpoint of the line connecting the two differential vias, i.e. equidistant points from the board center, and the second is a hyperbola with Via 1 and Via 2 at its focal points, i.e. a constant delta delay contour. For brevity, the former is referred to as a *constant distance circle* and the latter is *constant delta delay loci*.

4.4.1 At a constant distance from the center of the board

A smaller delta delay can introduce a more efficient noise cancellation. In Fig. 4.18 the differential vias are located at the board center and the center-to-center spacing between the two vias is 2 mm. It is seen that the delta delay varies from a minimum value of zero for all the points on the perpendicular bisector of the line connecting the two vias (*X* axis direction in Fig. 4.18), to a maximum value

pertaining to the r_2-r_1= *2 mm* on the line connecting the two vias (*Y* axis direction in Fig. 4.18). The line from Via 2 to Via 1 (*Y* axis) is the reference line and the angle is positive when it rotates clockwise. As well, it can be seen that an odd symmetry with respect to *Y* direction and even symmetry with respect to *X* direction exists [16]. Consequently, investigating the noise in one quadrant of the plane is sufficient to determine the noise map of the entire plane [16]. As one can see, four points A, B, C, and D are investigated in one quadrant at the circumference of the 10mm-radius circle at different angles, i.e. 0°, 30°, 60°, and 90°.

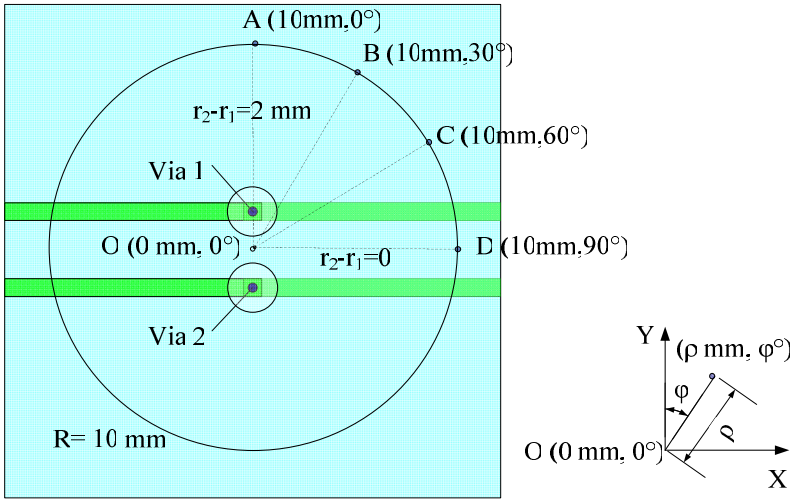


Fig. 4.18. Observation points on a constant radius circle on the PPW structure of Fig. 4.13.

Fig. 4.19 shows the noise waveforms of the four observation points in the first quadrant of the board generated by the cavity model simulations. In all cases, ±1 V step voltage sources with 115 ps (10%-90%) risetime are considered as the differential inputs. These waveforms show the evolution of noise waveforms along a circular path with a 10 mm radius measured from the board center, and

demonstrate that a smaller delta delay provides a more efficient noise cancellation. At the observation points on the perpendicular bisector of the line connecting the two vias (at 90° angle), the delta delay is zero; thereby, the noise can be entirely cancelled.

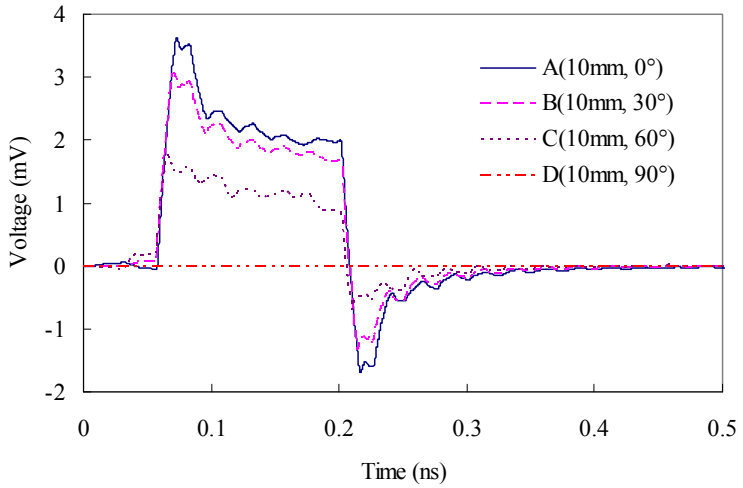


Fig. 4. 19. Noise waveforms at various angles along a circle with 10mm radius generated by the cavity method [±1 V step inputs, 115 ps risetime (10%-90%)].

4.4.2 Along one of the constant delay contours

In the planar top view shown in Fig. 4.20, the four points of E, F, G, and H are on the same delta delay hyperbolic contour. The difference between the distances of any point on this contour from the two vias is constant and equal to 1.41 mm.

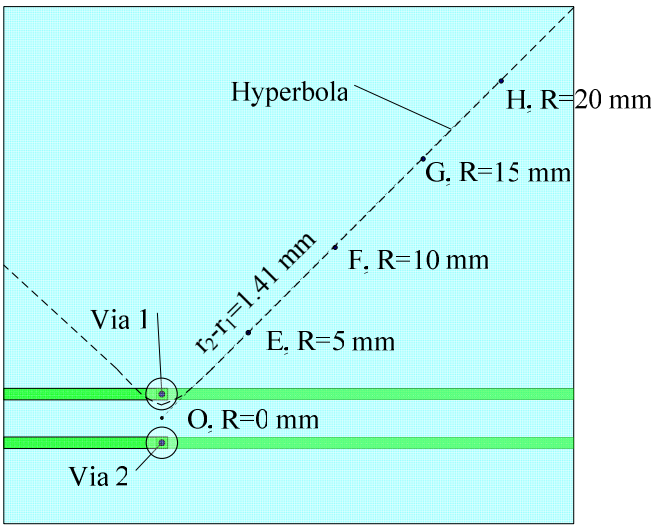


Fig. 4.20. Observation points along a hyperbola with constant delta delay Δr = 1.41 mm.

For all the points along this hyperbolic curve, the time difference between the arrival times of the two parallel plate modes is fixed and the same noise suppression is anticipated. The cavity model simulations pertaining to each observation point are conducted. The evolution of noise waveforms can be observed in Fig. 4.21. In all cases, $\pm$1 V step voltage sources with 115 ps (10%-90%) risetime are used as the differential inputs. Due to mainly the cylindrical wave propagation of the parallel plate modes excited by the vias and the conductor and dielectric losses, the amplitude of the noise voltage decreases at the farther distance from the sources, and the noise peak is further delayed.

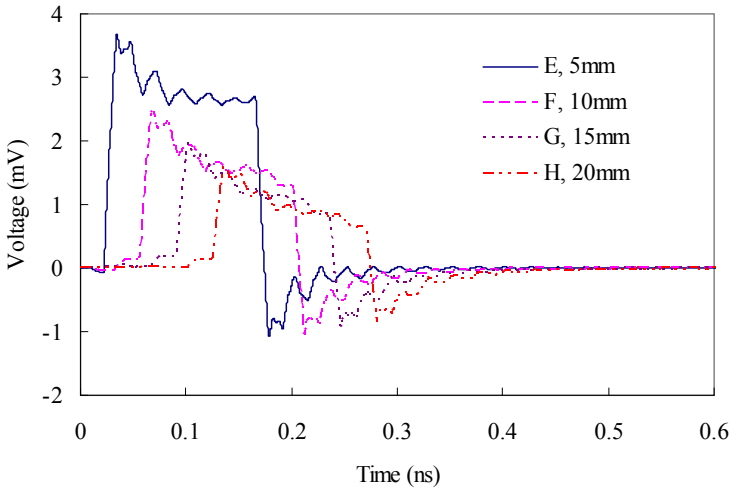


Fig. 4.21. Noise waveforms at constant delta delay points generated by the cavity method [±1 V step inputs, 115 ps risetime (10%-90%)].

4.5 Comparisons between the cavity model and full-wave simulations

In order to verify the cavity model, the layout of the structure presented in Fig. 4.13 of Section 4.3 is drawn in CST Microwave Studio and simulated using CST transient solver. The noise waveforms for this structure, following the parametric simulations described in Sections 4.4.1 and 4.4.2, and shown in Fig. 4.19 and Fig. 4.21, are simulated in CST and presented in Fig. 4.22 to Fig. 4.29. The overall comparisons of these results demonstrate a good agreement between the two methods with some minor differences in the prediction of the peak values. However, for each case shown is Figures 4.22 to 4.29, the simulation times by CST are around 1 hour 4 minutes, while it takes only 8 minutes to conduct circuit simulations using the cavity model on the same computing platform. Therefore, with this fast simulation technique, power/ground plane regions where noise peaks exceed a critical limit can be easily identified at a minimum simulation cost.

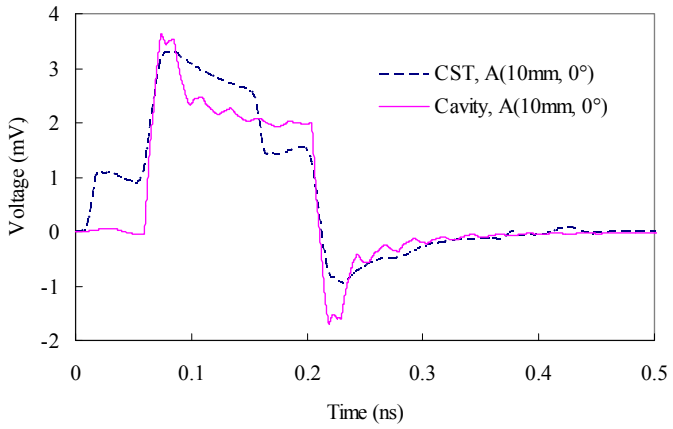


Fig. 4.22. Noise waveforms generated by CST and the cavity method at point A (10 mm, 0°) of the structure shown in Fig. 4.18 [±1 V step inputs, 115 ps risetime (10%-90%)].

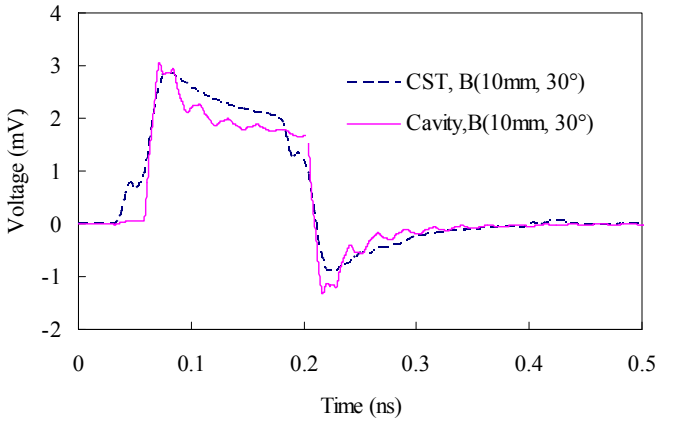


Fig. 4.23. Noise waveforms generated by CST and the cavity method at point B (10 mm, 30°) of the structure shown in Fig. 4.18 [±1 V step inputs, 115 ps risetime (10%-90%)].

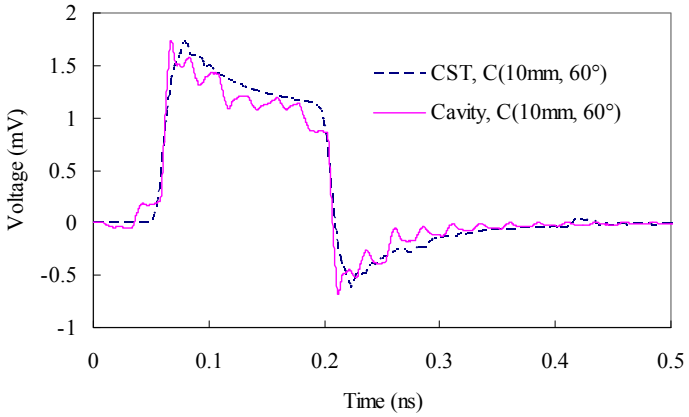


Fig. 4.24. Noise waveforms generated by CST and the cavity method at point C (10 mm, 60°) of the structure shown in Fig. 4.18 [±1 V step inputs, 115 ps risetime (10%-90%)].

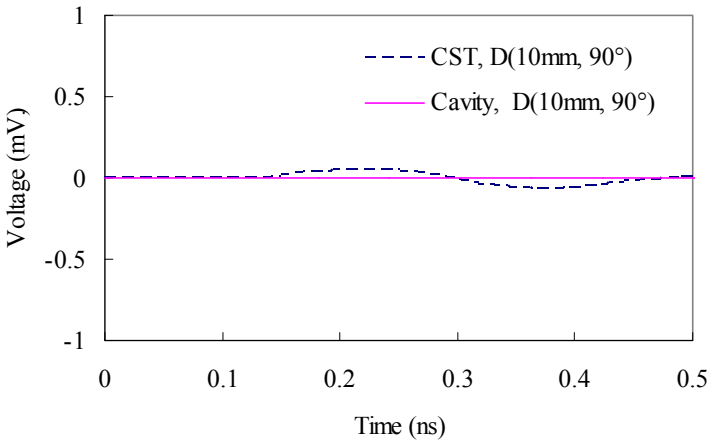


Fig. 4.25. Noise waveforms generated by CST and the cavity method at point D (10 mm, 90°) of the structure shown in Fig. 4.18 [±1 V step inputs, 115 ps risetime (10%-90%)].

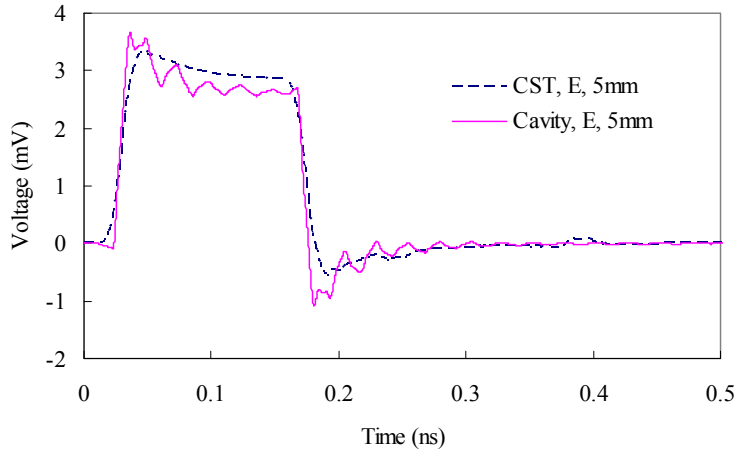


Fig. 4.26. Noise waveforms generated by CST and the cavity method at point E (5 mm, Δr=1.41 mm) of the structure shown in Fig. 4.20 [±1 V step inputs, 115 ps risetime (10%-90%)].

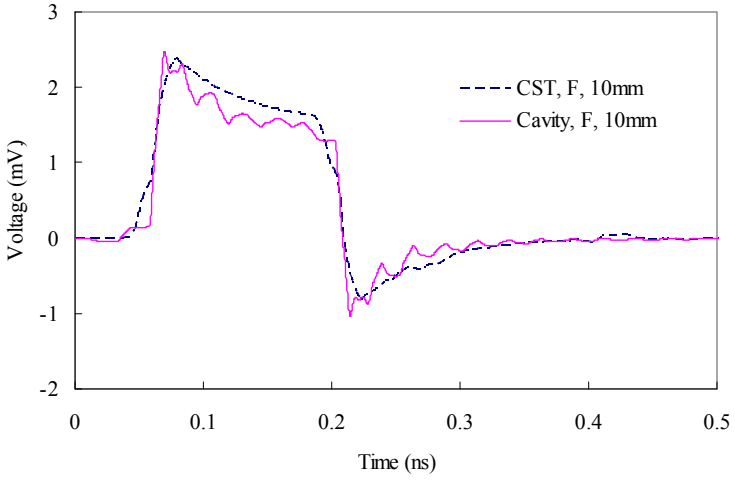


Fig. 4.27. Noise waveforms generated by CST and the cavity method at point F (10 mm, Δr=1.41 mm) of the structure shown in Fig. 4.20 [±1 V step inputs, 115 ps risetime (10%-90%)].

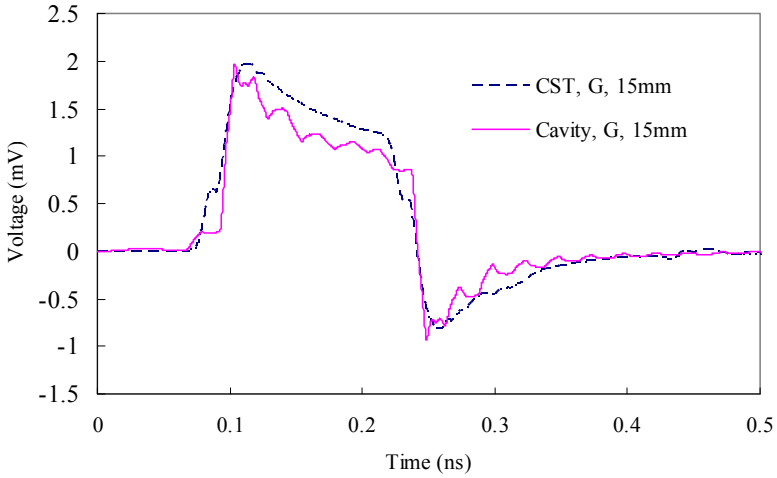


Fig. 4.28. Noise waveforms generated by CST and the cavity method at point G (15 mm, Δr=1.41 mm) of the structure shown in Fig. 4.20 [±1 V step inputs, 115 ps risetime (10%-90%)].

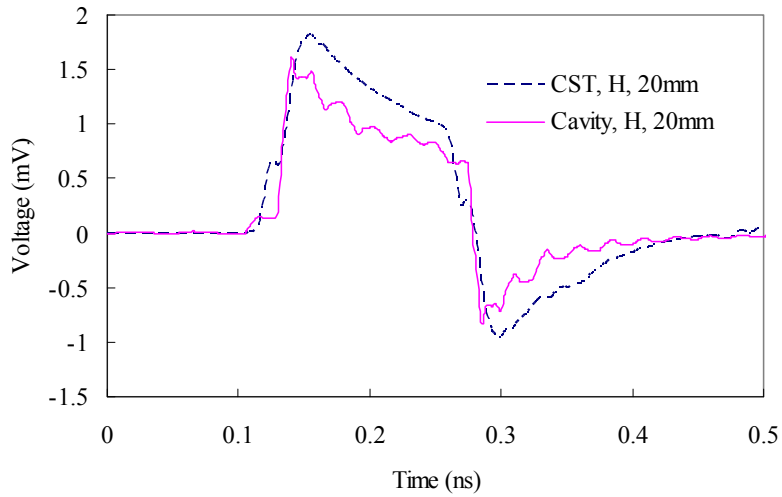


Fig. 4.29. Noise waveforms generated by CST and the cavity method at point H (20 mm, Δr=1.41 mm) of the structure shown in Fig. 4.20 [±1 V step inputs, 115 ps risetime (10%-90%)].

4.6 Measurements

To validate the modeling approach through measurement, the test prototype shown in Fig. 3.13 is used again but tested at the new observation points as marked in Fig. 4.30. The through differential vias are separated by a 4 mm center-

to-center spacing. There are five observation points at the board, located at J (2 cm, 45°), K (2 cm, 0°), L (2 cm, 90°), M (2 cm, 180°), and N (4 cm, 225°) positions.

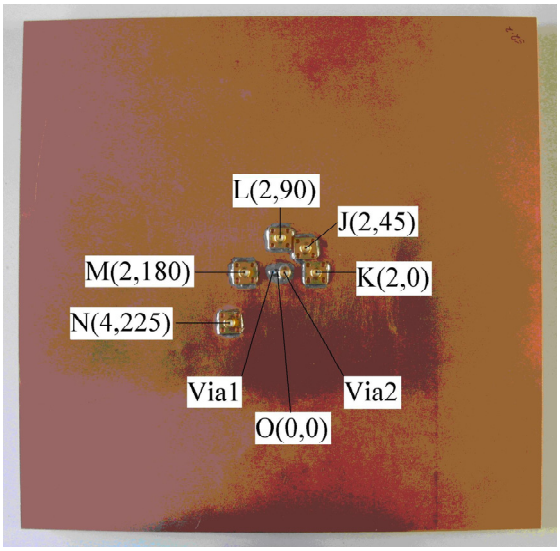


Fig. 4.30. The fabricated measurement prototype.

The differential signals are generated by the Tektronix TDS8200 oscilloscope with an 80E04 electrical sampling module, and launched to the board with two same-length SMA cables. The amplitudes of signals are 250 mV, and the rise time is 29 ps (10%-90%). The waveforms at the observation points are detected by the oscilloscope. To compare with the cavity method, the multiport impedance matrices of the structure are calculated, as shown in Figure 4.30, where one port is defined at each observation point. The corresponding cavity model is close to what is shown in Fig. 4.14 except for the use of multilayer, while the structure of Fig. 4.30 has only one dielectric layer. Transient simulations of this circuit are performed in Agilent ADS.

The noise voltages at the five observation points detected by the oscilloscope are shown in Fig. 4.31 to Fig. 4.35. As one can see, the simulated noise spikes exhibit very good agreement with the measurements. Only for the case of L (2 cm, 90°) observation point shown in Fig. 4.33, circuit simulation predicts 0 mV at all times, while minute noise spikes of less than 2.5 mV are seen in the measurement. This is due to the fabrication tolerances in the positioning of the observation point, and in the lengths of the cables and connectors that create not exactly equal delay paths. This means that the delta delay is not exactly zero at the observation point L in the fabricated prototype.

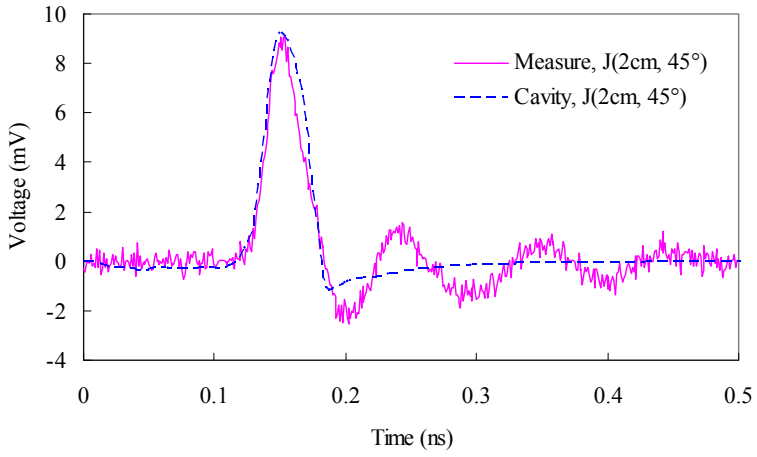


Fig. 4.31. Noise waveforms from the measurement and the cavity method simulation at point J (2 cm, 45°) of the structure shown in Fig. 4.30 [±250 mV step inputs, 29 ps risetime (10%-90%)].

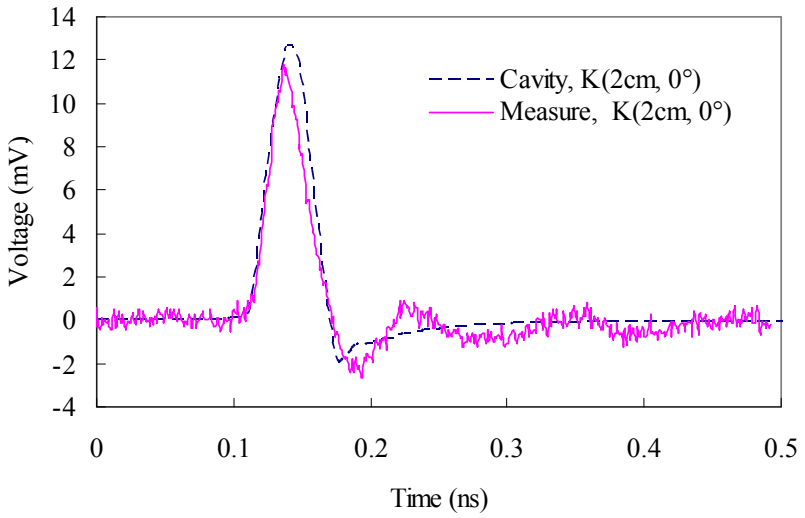


Fig. 4.32. Noise waveforms from the measurement and the cavity method simulation at point K (2 cm,0°) of the structure shown in Fig. 4.30 [±250 mV step inputs, 29 ps risetime (10%-90%)].

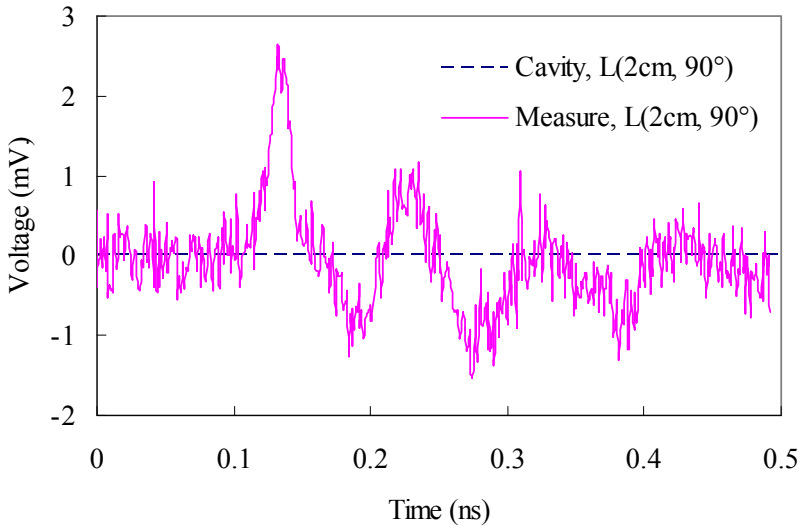


Fig. 4.33. Noise waveforms from the measurement and the cavity method simulation at point L (2 cm, 90°) of the structure shown in Fig. 4.30 [±250 mV step inputs, 29 ps risetime (10%-90%)].

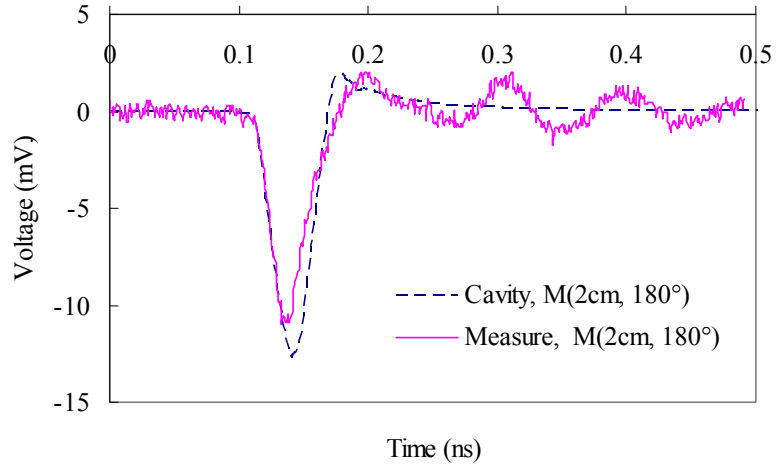


Fig. 4.34. Noise waveforms from the measurement and the cavity method simulation at point M (2 cm, 180°) of the structure shown in Fig. 4.30 [±250 mV step inputs, 29 ps risetime (10%-90%)].

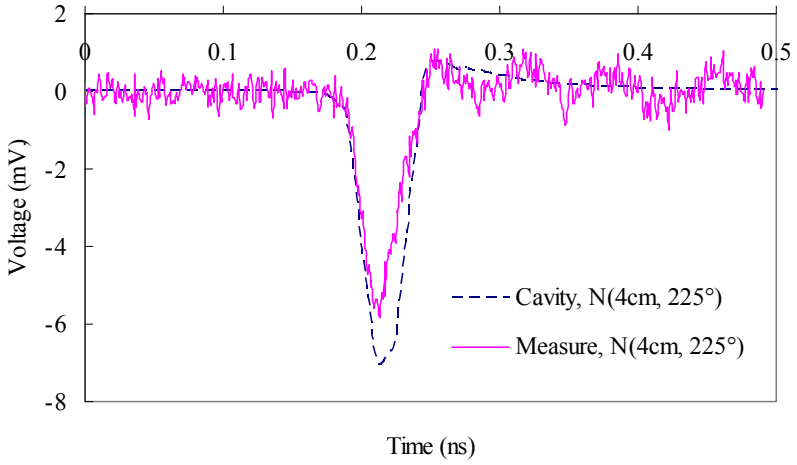


Fig. 4.35. Noise waveforms from the measurement and the cavity method simulation at point N (4 cm ,225°) of the structure shown in Fig. 4.30 [±250 mV step inputs, 29 ps risetime (10%-90%)].

To conduct an overall comparison, the structure shown in Fig. 4.30 is considered and noise waveforms at the J (2 cm, 45°) observation point are obtained from four different approaches: CST full-wave time domain simulation,

the RTL modeling and ADS circuit simulation, the cavity modeling (with PMC boundary) and ADS circuit simulation and measurement.

Fig. 4.36 depicts the noise waveforms generated by these four methods representing very good agreement among all four in the prediction of the noise peak. Only the results from the RTL method simulation have slightly larger overshoot and undershoot in comparison with the rest. It is demonstrated in this figure that, in comparison of the two methods based on the analytical approaches, the cavity method is more accurate than the RTL method in noise prediction due to its full-mode considerations.

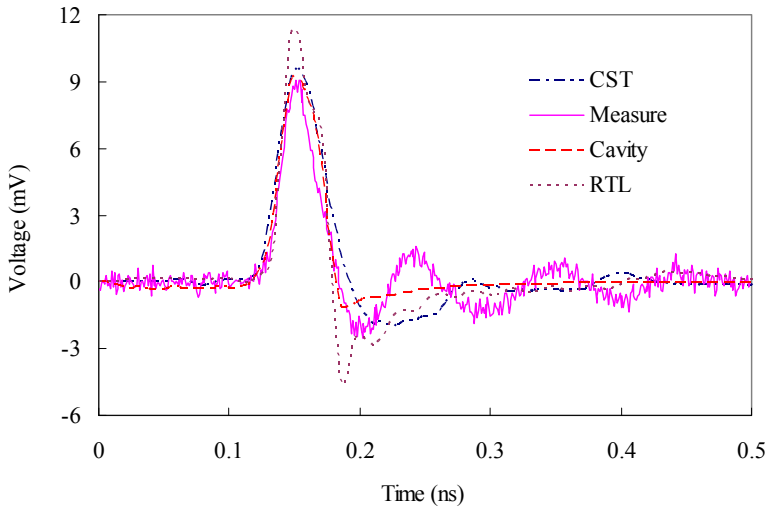


Fig. 4.36. Noise waveforms from the measurement, the CST transient solver simulation, the RTL model simulation and the cavity model simulation at point J (2 cm, 45°) of the structure shown in Fig. 4.30 [±250 mV step inputs, 29 ps risetime (10%-90%)].

4.7 Global circuit simulations using the cavity modeling technique

In order to evaluate the performance of the cavity model in high-speed circuits, the same FPGA system presented in Chapter 3, Section 3.5 is considered to conduct global co-simulations. The FPGA interconnects and the PDN structure

shown in Fig. 4.37 is considered as the system integration platform. This is the same geometry as that of Fig. 4.13 except for an increased number of observation points. The observation point P (10 mm, 45°) in Fig. 4.37 is at the same location as the observation point in Fig. 4.13, and only noise at the top PPW is investigated.

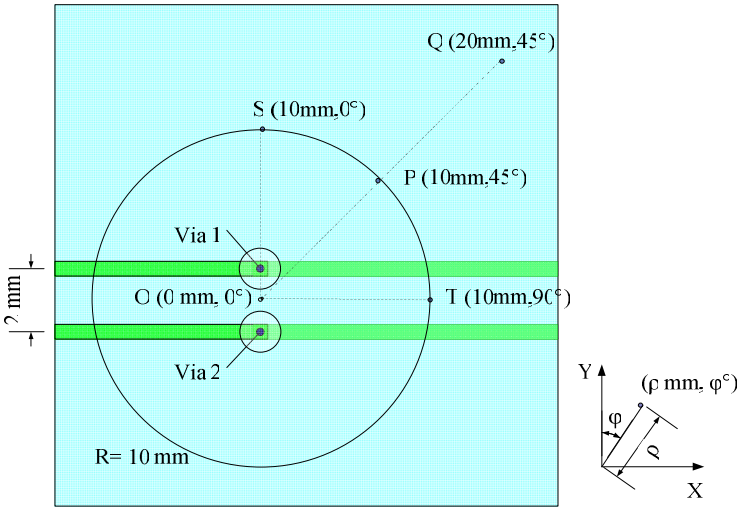


Fig. 4.37. Multilayer PPW with buried differential vias used as the PDN and the interconnect in the FPGA system simulations.

The block diagram of the overall system and the connections between the PDN structure and the driver and receiver models is shown in Fig. 4.38. V_{probe} is the noise voltage at the observation point. The cavity model here is the same as the circuit shown in Fig. 4.14 except for the sources and loads. The SPICE models of the FPGA driver and receiver are imported into Agilent ADS and transient simulations are performed. The source data has a PCML format with the rate of 6 Gbps and the risetime of 10 ps for each pulse. The noise waveform at the observation point P (10 mm, 45°) is shown in Fig. 4.39.

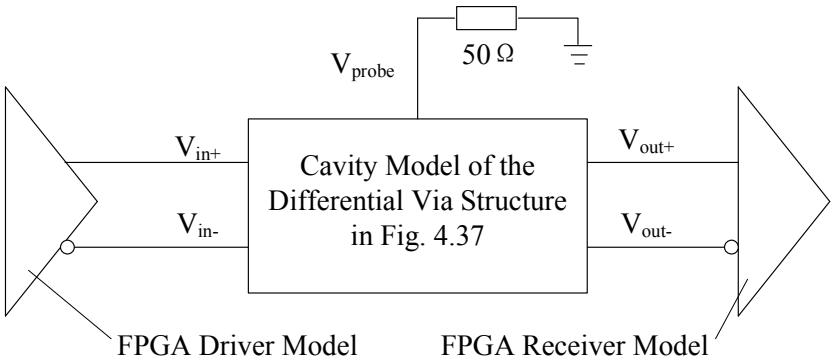


Fig. 4.38. Block diagram of the model of the FPGA system interconnected with differential vias which are represented with the cavity model.

4.7.1 Simulations

To evaluate the impedance matrix calculated using the cavity model in this application, in the same manner as mentioned in Chapter 3, the layout of the multilayer structure is drawn and simulated in CST Microwave Studio and five-port *S*-parameter matrix is also obtained. Then, the SPICE model of the FPGA transceiver and the S-parameter matrixes (from CST and Cavity calculations) are imported to Agilent ADS to conduct transient simulations.

Fig. 4.39 depicts the noise waveforms at the observation point P (1 cm, 45°) obtained using the *S*-parameter matrices from CST simulations and the cavity model, showing very good agreement. As one can see, the first noise peak obtained by CST is 6.02 mV and is 4.74 mV by the cavity method. The minor differences between the two waveforms are introduced by the approximations in the cavity model. Three thousand terms are computed in the summation.

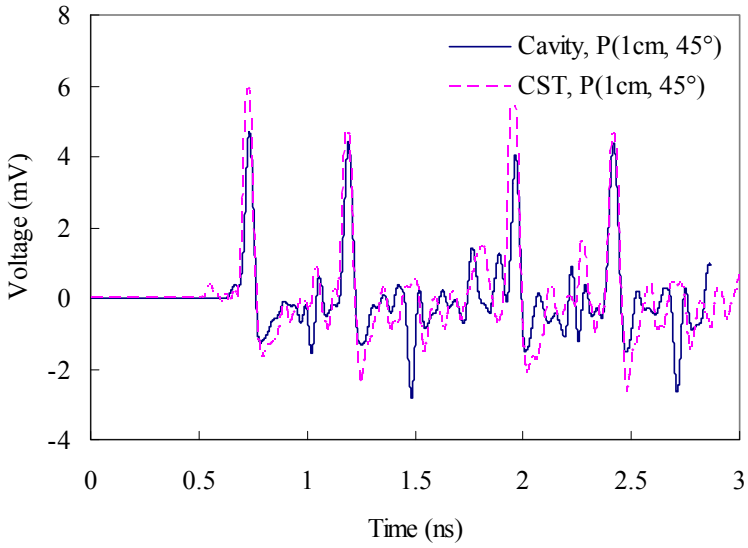


Fig. 4.39. Noise waveforms generated when using CST and the cavity model in global simulations of an FPGA transceiver system at point P (10 mm, 45°).

4.7.2 Noise map

To evaluate the noise distribution map on the power/ground planes in the studied FPGA system, several observation points in Fig. 4.37 are selected and simulations are conducted in ADS using the cavity model. Firstly, two points, P (10 mm, 45°) and Q (20 mm, 45°), are chosen to represent two different distances from the board center. Fig. 4.40 shows the simulated noise waveforms at these two points. It is seen that the amplitude of the noise voltage decreases at the farther distance from the sources as expected.

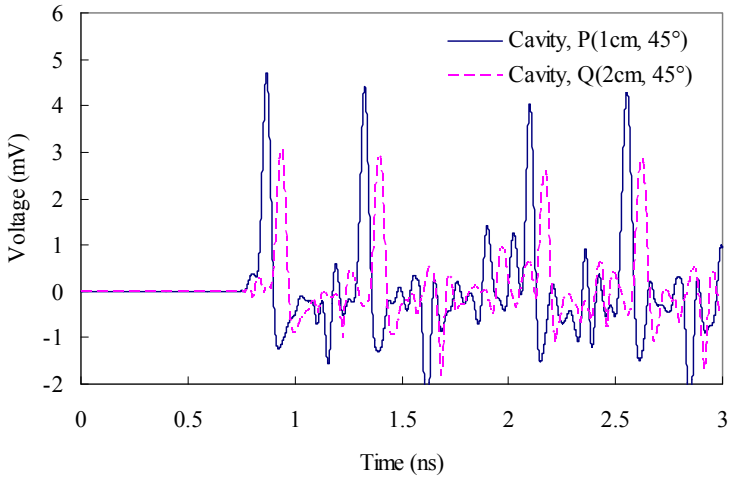


Fig. 4.40. Noise waveforms generated when using CST and the cavity model in global simulations of an FPGA transceiver system at points P (10 mm, 45°) and Q (20 mm, 45°).

Next, three points, P(10mm, 45°), S(10mm, 0°), and T(10mm, 90°), located at the same distance (10 mm) from the board center are chosen and the pertinent cavity model calculations are performed. Fig. 4.41 shows the simulated noise waveforms in ADS using the calculated cavity method data files. Obviously, bigger delta delay introduces bigger noise peak. This phenomenon matches with the conclusion presented in Section 4.4. As before, the noise voltage at point T (10 mm, 90°) is not ideally zero. The reason is that the difference in the delays can cause the transmitted signals to not be completely differential.

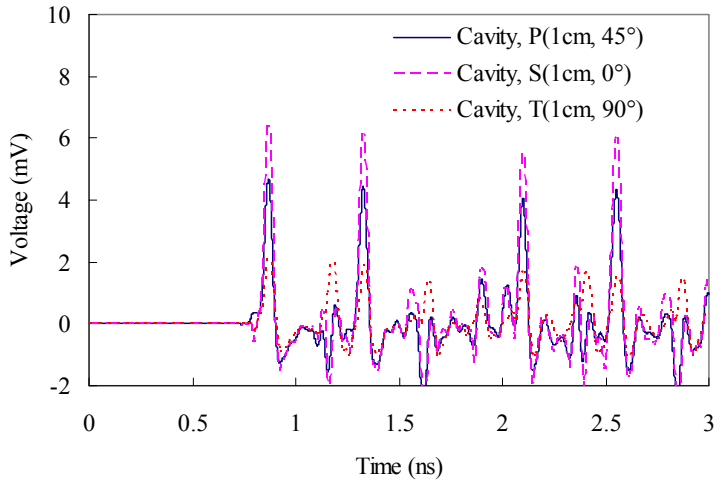


Fig. 4.41. Noise waveforms generated when using CST and the cavity model in global simulations of an FPGA transceiver system at points P (10 mm, 45°), S (10 mm, 0°), and T (10 mm, 90°).

4.8 Conclusions

In this chapter, modeling of various types of parallel-plate PDN structures using the fast cavity method is investigated. The developed equivalent circuits are used to monitor power/ground noise in many practical scenarios, including multilayer differential via structures. Like the previous chapter, the PDN models derived from this analytical technique are easily imported to commercial circuit simulators such as Agilent ADS. Simulation results for various cases are compared with those of full-wave simulations demonstrating excellent accuracy with drastic reduction in the simulation time. It should be pointed out here that, for all cases simulated in Sections 4.3 to 4.7 of this chapter, PMC boundary conditions for the sidewalls are used. Parametric studies of the differential structure are conducted to reaffirm that differential signalling can suppress PDN noise effectively. As well, noise maps for few cases are created using this fast simulation technique. Such diagnostic evaluation is very useful in package design

and system integration. Simulation results obtained from the cavity method, the RTL method, and the CST transient solver show excellent agreement and closely match measurements of the fabricated prototype. It is observed in this study that the cavity model is more accurate compared to the RTL model. Finally, one practical system of the FPGA transceiver is simulated, including the model for the differential interconnects and the multilayer PDN.

Chapter 5 Miniaturization of EBG structures used in PDN

5.1 Introduction

Although adding decoupling capacitors and differential signalling can provide noise suppression, they only work effectively at low frequencies (below 1-2 GHz) and in specific regions of a PDN. EBG structures offer wideband omnidirectional noise suppression at high frequencies as well as below the 1 GHz range. However, for low frequency implementation, the dimensions of the EBG structures may become too large for compact systems. This chapter focuses on investigating miniaturization of a two-layer uniplanar EBG. Two methods are introduced, including optimization of the design geometry and employing high-K materials. A combination of the two methods is also studied and the impact of using differential vias in the PDN containing an EBG surface is evaluated in both time and frequency domains.

5.2 Studied uniplanar EBG structure

The uniplanar EBG structure can be easily and cost-effectively developed using the standard PCB fabrication technology. The two metal layers act as power and ground planes of the PDN. The uniplanar EBG structure shown in Fig. 5.1[14], [15] is studied herein, which is a 2-D periodic lattice consisting of square patches (side length of a_p) connected with small branches (width of a_b). Only square-shaped patches connected with thin branches are investigated in this thesis.

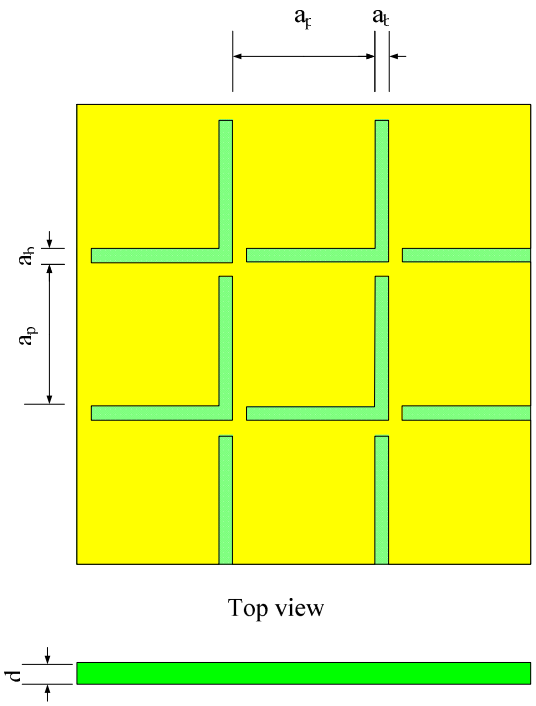


Fig. 5.1. A 2-D uniplanar EBG structure, top and side views are shown. The bottom plane is a solid conductor.

At low frequencies, the square patches and the solid conductor plane at the bottom layer predominantly behave in a capacitive manner. The thin branches act in a more inductive manner because their equivalent capacitance is much smaller compared to that of the large square patches. Therefore, the structure forms a distributed *LC* network that is viewed as a low-pass filter at low frequencies [15]. At high frequencies, the inductance of large patches and capacitance of small branches cannot be ignored, and series and parallel resonances occur alternately in the patches and branches [14]. Due to the impedance variations caused by these resonance mechanisms, the EBG structure exhibits passbands and stopbands alternatively.

5.2.1 Unit cell of the EBG

Fig. 5.2 shows the unit cell of the 2-D uniplanar EBG structure and its *LC* equivalent circuit. The overall EBG structure is represented by a 2-D *LC* ladder network composed of series inductors and shunt capacitors. From filter theory, the corner frequency of a low-pass *LC* filter is calculated by $f = 1/\pi\sqrt{LC}$ [56]. This corner frequency marks the lower end of the stopband region at which noise suppression happens. In any attempt to miniaturize the unit cell of the EBG, this frequency should be maintained at the desired value and not shifted. Reducing the size of patches decreases the capacitance and, consequently, the on-set of the stopband shifts to a higher frequency. Therefore, in order to keep the lower corner frequency of the first stopband, the decreased *C* capacitance should be compensated by increasing inductance of *L*. This is realized by adding slits to the geometry. Alternatively, *C* can be maintained by employing a high-K dielectric material [14].

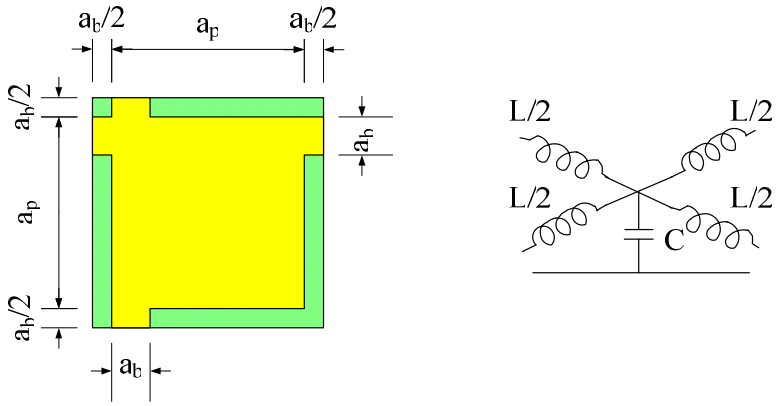


Fig. 5.2. Unit cell of the 2-D uniplanar EBG structure and its equivalent circuit. .

5.2.2 Investigation of the stopband in 1-D periodic structure

To see the impact of cascading the unit cells in forming an EBG structure and create a simple and fast evaluation in testing the miniaturization approaches, first 1-D periodic configurations are studied. Hence, a 1-D EBG structure is created using the unit cell shown in Fig. 5.2 only along one dimension. This structure is shown in Fig. 5.3(a). The patch size is 10 mm × 10 mm (a_p=*10 mm*), and the branch is 0.2 mm × 0.2 mm (a_b=*0.2 mm*). The dielectric constant of the substrate is 4.2 and has the height of d=0.2 mm. As a benchmark for comparison, a parallel-plate structure with the same area as the 1-D EBG structure and using the same substrate is also considered [see Fig. 5.3(b)]. The locations of the ports are marked on the two layouts.

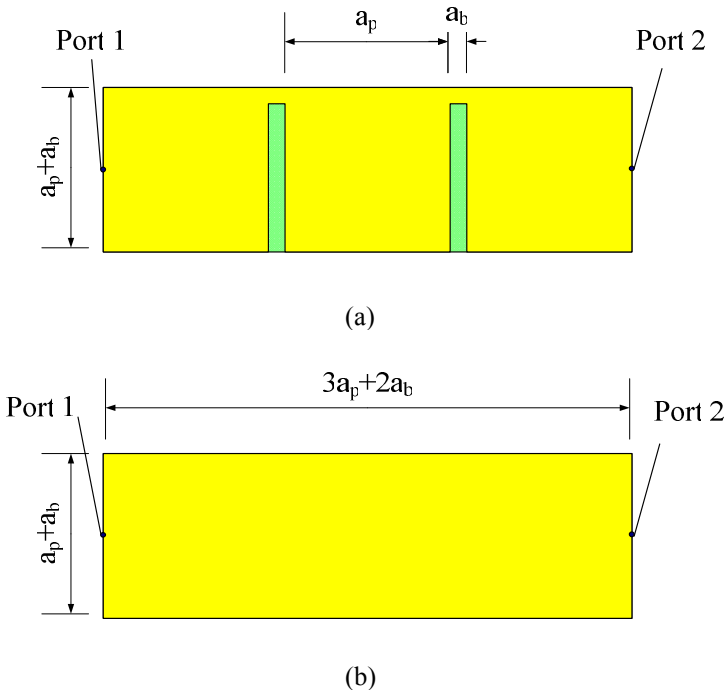


Fig. 5.3. (a) 1-D uniplanar EBG structure. (b) a parallel-plate geometry with the same area as the structure in (a).

The transmission coefficients S_{21} of both structures are shown in Fig. 5.4, which are obtained by a full-wave commercial solver, Ansoft SIwave. The S_{21} of the 1-D EBG shows the creation of multiple stopbands with more than 60 dB insertion loss in comparison with the S_{21} profile of the solid parallel-plate geometry. These yield excellent isolation between the ports in broad frequency bands.

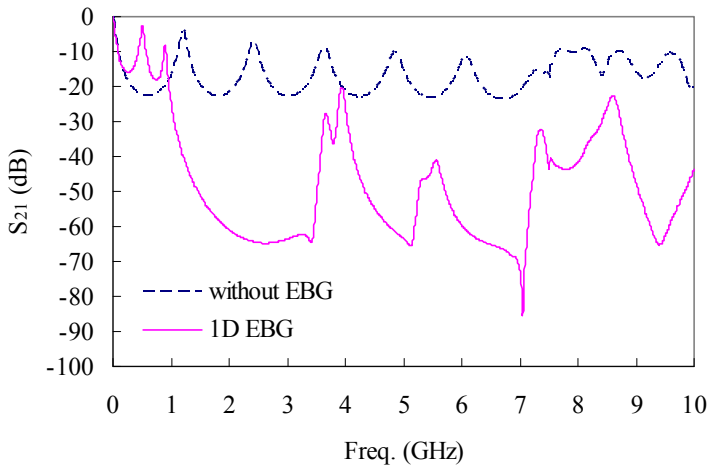


Fig. 5.4. Magnitudes of simulated S_{21} of the structures in Fig. 5.3.

The branch dimensions influence the EBG performance. This is studied using full-wave simulations and by changing a_b from 0.2 mm to 1 mm. Fig. 5.5 shows the S_{21} profiles. It can be seen that the smaller branch offers a broader stopband.

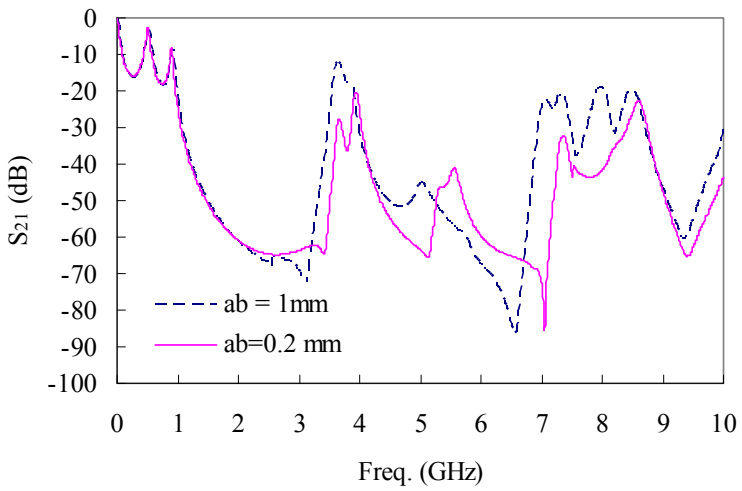


Fig. 5.5. Magnitudes of simulated S_{21} of the structure in Fig 5.3 (a) when the branch length (a_b) is changed.

5.3 Miniaturization by modification of layout geometry

In Section 5.2.1, it is analyzed that reducing the size of layout can result in changing the stopband while the ultimate objective in miniaturization is to maintain the stopband characteristics. Many research works have focused on applying other layout modifications to achieve this goal [14], [71], [72]. One of them is by adding slits in the large patches to increase L and compensate for any decreasing in the C that may happen in the miniaturization of the unit cell. In this section, this approach is investigated for the 1-D structure, which provides a faster means for evaluation of the concept as opposed to the 2-D simulations.

5.3.1 Adding narrow slits

Narrow slits with the width of w_s are created on the patches as shown in Fig. 5.6. In fact, the narrow slits equivalently extend the length of the branches from a_b to $a_b + L_r a_p$. Hence, it is expected that they increase the branch inductance L and

decrease the lower corner cut-off frequency. It can be speculated that the slits reduce the patch areas and result in decreasing the shunt capacitance of patches, but this side effect is negligible due to the relatively small slit size in comparison with the patch area. The length of the slit is defined as $L_r a_p$, where L_r is a ratio of slit-length to the patch side a_p , which can take a value between 0% and 100% in an optimization process [14].

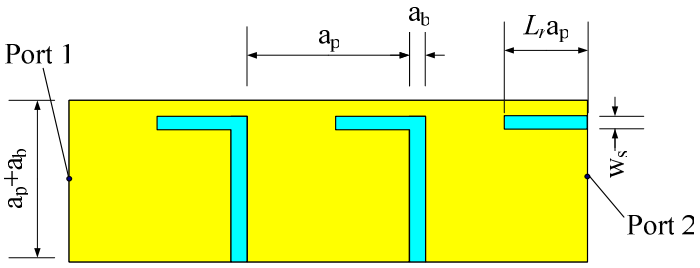


Fig. 5.6. 1-D EBG structure with slits.

The structure in Fig. 5.6 is simulated using the same substrate as structure in Fig. 5.3, the same dimensions, and the following geometrical parameters for the additional slits: w_s = 0.2 mm and $w_s+L_r a_p$ = 10.2 mm, L_r is considered to be 50%. The port locations are the same as those shown in Fig. 5.3.

Full-wave simulation results of S_{21} are shown in Fig. 5.7. As one can see, the lower corner frequency of the first stopband decreases for the case of adding the slits. This means that the EBG with narrow slits shifts the stopband towards the lower frequencies without changing the dimensions of the unit-cell. Hence, it is concluded that if a smaller unit cell is used and slits are added to the design, the objectives of miniaturization and maintaining stopband can be achieved, as the properly designed slits counteract the reduction in the physical size of the unit cell

and push the lower cut-off to the original place. It can be seen from Fig. 5.7 that the EBG with narrow slits also provides isolation in the same frequency band as the EBG without slits. In addition, the isolation characteristics are improved in applying this layout modification method.

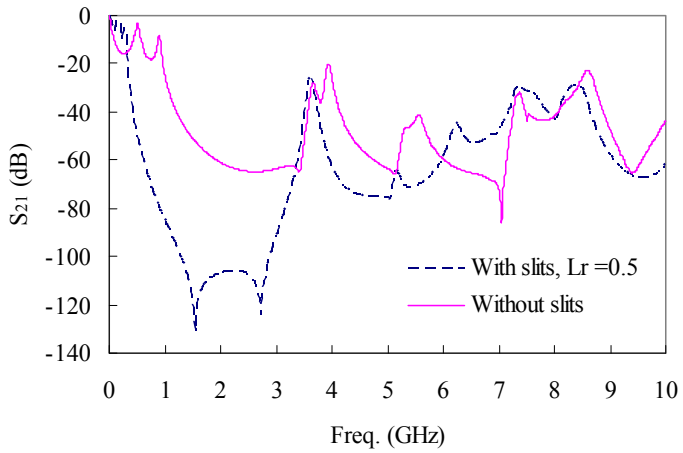


Fig. 5.7. Magnitudes of simulated S_{21} of the studied 1-D uniplanar EBG structures with and without slits.

5.3.2 Different slit arrangements

There are several possibilities for adding more slits and positioning them on the square patches of the studied 1-D EBG structure of Fig. 5.3. Three of these arrangement patterns are illustrated in Fig. 5.8. The lengths of all slits are 10 mm. Note that the same substrate with a height of 0.2 mm and a dielectric constant of 4.2, and the same port locations as before are used in these three structures.

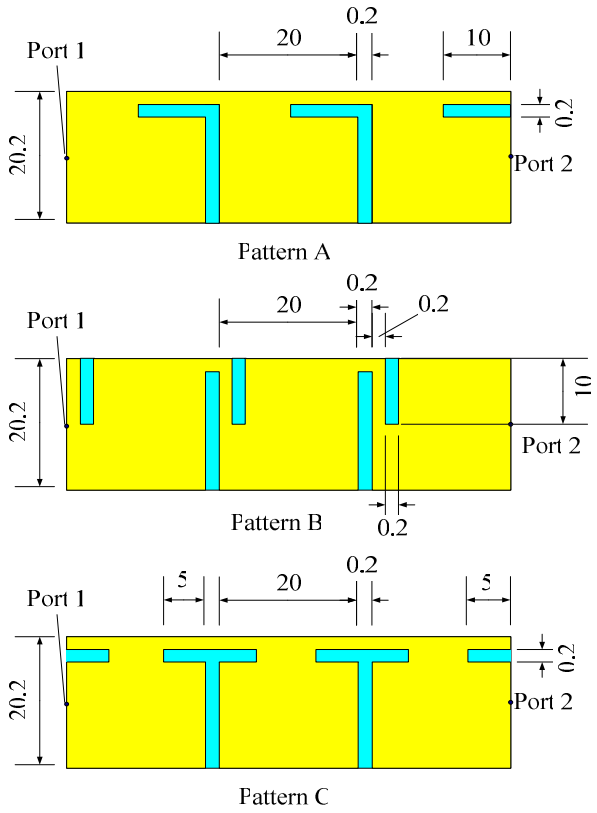


Fig. 5.8. 1-D EBG structure of Fig. 5.3 with three types of slit patterns (unit: mm).

The transmission coefficients of the three new designs by Ansoft SIwave are shown in Fig. 5.9. It can be observed that all provide almost similar insertion loss signatures. Pattern B performs the worst, and Pattern C offers the highest isolation and slightly widest overall bandwidth among the three. Pattern A is easiest for 2-D EBG design, thus it is chosen for further investigation.

5.3.3 Changing the slit length to patch width ratio

Another alternative for modification of the unit cell layout is changing the slit-length to patch width ratio (L_r). Fig. 5.10 shows the three studied geometries of the 1-D EBG structure with L_r ratio of 0%, 50%, 99%, respectively. The patch and

branch dimensions, the substrate parameters and the port locations are the same as before.

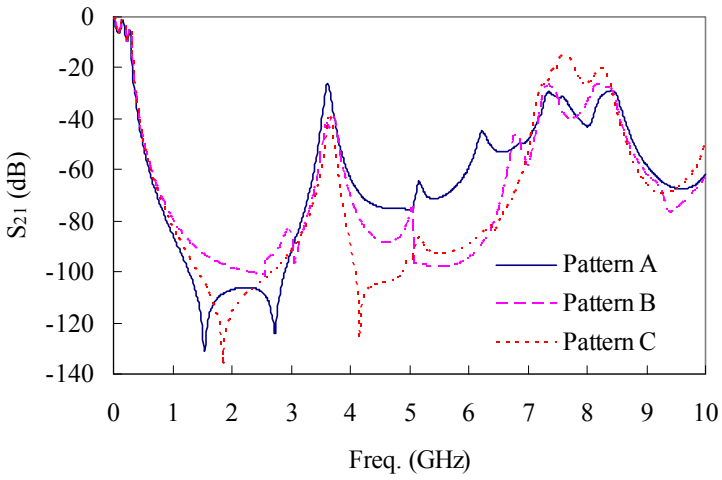


Fig. 5.9. Magnitudes of simulated S_{21} of the three patterns shown in Fig. 5.8.

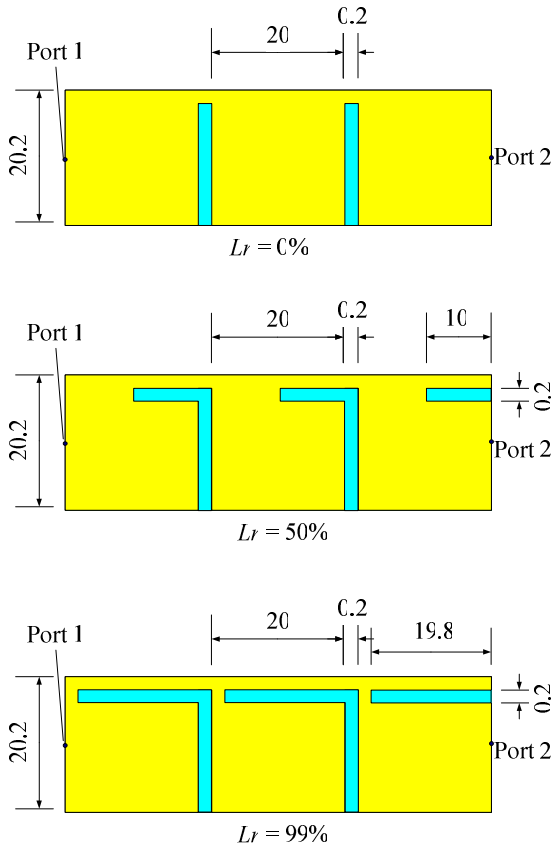


Fig. 5.10. 1-D EBG structures with various L_r ratios of 0%, 50% and 99% (unit: mm).

The full-wave simulation results by Ansoft SIwave are shown in Fig. 5.11. It can be seen that the lower corner frequency decreases with increasing L_r. The structure with slit-length to patch width ratio of L_r = 99% provides the lowest lower corner frequency, however there is very little improvement in comparison to the L_r = 50% case. Therefore, the slit-length to patch width ratio of 50% is chosen in [14] and in this thesis for development of the 2-D uniplanar EBG structure.

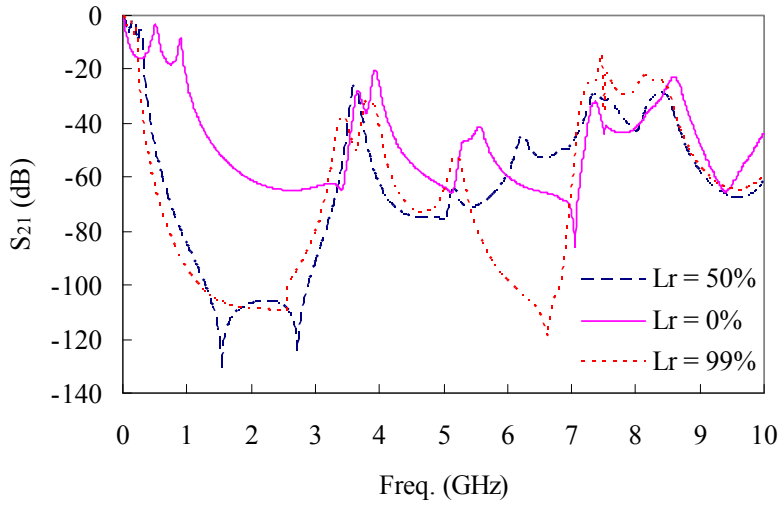


Fig. 5.11. Magnitudes of simulated S_{21} for the structures shown in Fig. 5.10.

5.3.4 Employing slits in the 2-D EBG structure

As mentioned in the previous section, the unit cell of the 1-D EBG structure of Pattern A shown in Fig. 5.8 with L_r = 50% is chosen to develop the 2-D EBG structure. Fig. 5.12 depicts two realizations of this 2-D EBG structure. Pattern D structure is the 2-D version of the uniplanar EBG structure without slits. Then, more slits are added to the structure according to references [14] and [15], and

Pattern G is created. Three ports are defined for each pattern as shown. The unit cell of both structures has the following parameters (see Fig. 5.6 for definition of variables): a_p = 20 mm, a_b = 0.2 mm, d = 0.2 mm, w_s = 0.2 mm, L_r = 50% for pattern G and 0% for Pattern D, and ε_r = 4.2.

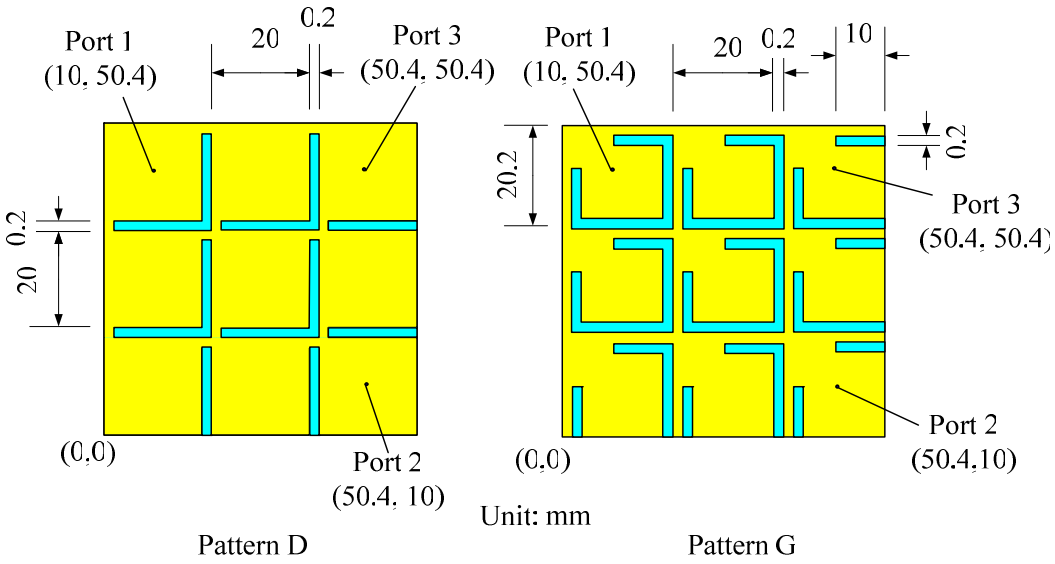


Fig. 5.12. 2-D EBG structures Pattern D and Pattern G (with L_r = 50%).

Fig. 5.13 shows the transmission coefficients S_{21} of the two patterns simulated by Ansoft SIwave. It is seen that the lower corner frequency of the first stopband (measured at -40 dB) is at 1.23 GHz for Pattern D structure and is at 0.43 GHz for Pattern G while having the same size unit cell. Both designs provide good isolation over an ultra-wide band frequency range.

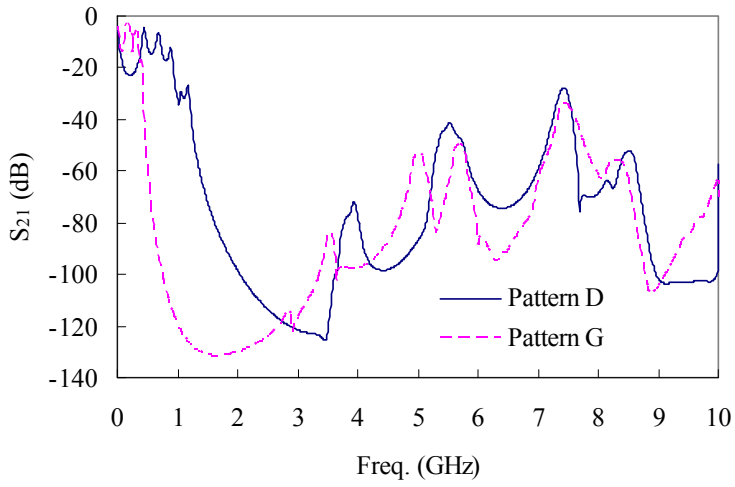


Fig. 5.13. Magnitudes of simulated S_{21} of the 2-D EBG structures of Patterns D and G.

The transmission coefficients between Port 1 and Port 3 S_{31} of the two pattern structures are shown in Fig. 5.14. The lower corner frequencies of the first stopbands measured at -40dB are 1.33 GHz and 0.47 GHz for Pattern D and Pattern G, respectively. As one can see, both structures induce omnidirectional stopbands. Pattern G exhibits a better isolation characteristic compared to the Pattern D EBG structure, demonstrating the efficiency of the employed layout modification approach [14], [15].

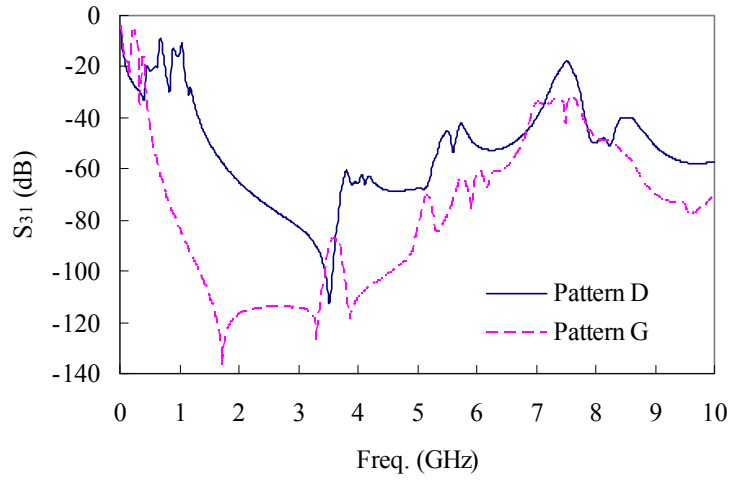


Fig. 5.14. Magnitudes of simulated S_{31} of the 2-D EBG structures of Pattern D and G.

Fig. 5.15 shows the transmission coefficients of the three ports of the Pattern G EBG structure. The lower corner frequencies of the first stopbands in all are almost the same, around 0.45 GHz. Ultra-wide omnidirectional stopbands, more than 7 GHz when measured at -40dB, are achieved while obtaining isolation levels exceeding 70dB. However, the dimensions of the unit cell are 20.2 mm by 20.2 mm, which are still large for compact PCBs and packages, especially since a few unit cells are needed between the ports in order to yield a desired level of isolation. Therefore, other methods, such as employing new substrate materials, should be examined for achievement of further miniaturization.

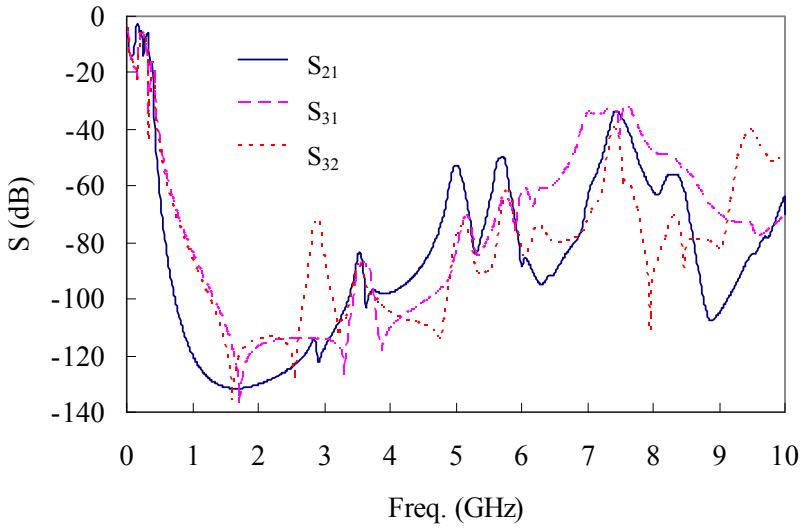


Fig. 5.15. Magnitudes of simulated S_{21}, S_{31} *and* S_{32} of the 2-D EBG structure of Pattern G.

5.4 Designing miniaturized 2-D EBG structure using high-K materials and slits

The second miniaturization approach is utilizing higher dielectric constant dielectric substrates, as this increases the effective capacitance of the EBG patches and lowers the corner frequency of the first stopband [14]. In another

words, the decreased capacitance of the EBG patch in reducing the size is compensated for by increasing ε_r. Another method to lower the corner frequency is to increase the equivalent L of branches by using high permeability magnetic materials in the substrate [15]. Common materials used in PCB fabrication are non-magnetic (μ_r =1), thus this approach can increase fabrication costs. In this thesis, only employing high relative permittivity ε_r is investigated. Combination of this method and the modification of layout design for more aggressive miniaturization of the EBG unit cell is discussed later in this section.

5.4.1 Using high permittivity dielectric

The commonly used dielectric material used in PCB fabrication is FR-4 (ε_r =4.2). If it is replaced by a high-K dielectric, the propagation wavelength is reduced, which directly influences the dimensions of the EBG layout. According to [15], the size reduction factor k_r is defined by the following expression (5.1):

$$k_r = \sqrt{\frac{\varepsilon_{r,low}}{\varepsilon_{r,high}}} \qquad (5.1)$$

where $\varepsilon_{r,low}$ and $\varepsilon_{r,high}$ are the dielectric constants of FR-4 and the high-K material, respectively.

According to [73]-[74], commercially available high-K dielectric materials with ε_r = 20 and higher can be employed for these studies. The equivalent shunt capacitance of the patches in the EBG structure increases to $k_r^2 C$, as opposed to C, when $\varepsilon_{r,low}$ is used. Now, if the side length of the square patch is reduced by k_r factor, the patch capacitance reduces by $1/k_r^2$ factor and overall equivalent

capacitance of the patch reverts back to C [15]. To start the design process, if Pattern D EBG in Fig. 5.16, which has an FR-4 dielectric, is considered and then its substrate is replaced with a high-K material with $\varepsilon_r = 17$, $k_r = 0.5$ is obtained. This reduces the geometry by 50% to Pattern E as illustrated in Fig. 5.16. The dimensions of Pattern D are 20 mm × 20 mm patches and 0.2 mm × 0.2 mm square branches. Then, Pattern E becomes an EBG layout with 10 mm × 10 mm patches and 0.2 mm × 0.2 mm square branches. The thicknesses of dielectric substrates in both cases are 0.2 mm. Port locations in these 3 by 3 EBG geometries are indicated in Fig. 5.16.

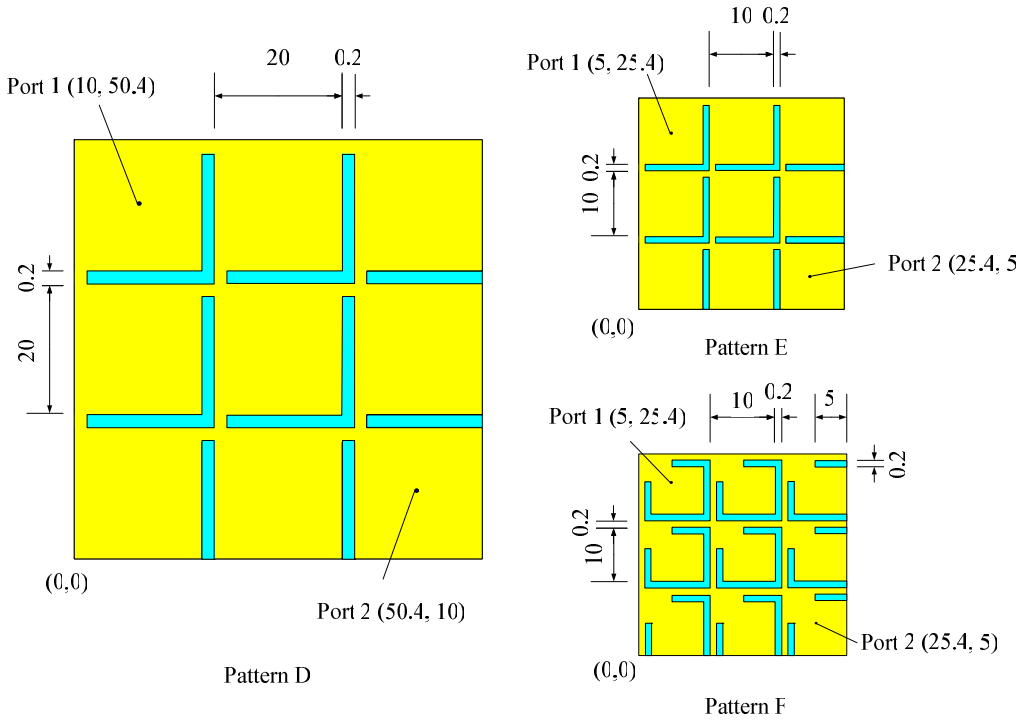


Fig. 5.16. The studied 2- D EBG structures: Pattern D uses FR-4 dielectric ($\varepsilon_r = 4.2$), Pattern E uses a high-K dielectric ($\varepsilon_r = 17$) and Pattern F uses the high-K dielectric ($\varepsilon_r = 17$) and multiple slits for EBG miniaturization.

The S_{21} of the Pattern D and E structures are simulated. For investigation of the impact of adding the high-K dielectric, one more set of simulation is conducted when the dielectric used for Pattern E is FR-4. All the results are shown in Fig. 5.17. For the case of Pattern E with FR-4 dielectric the lower corner frequency of the first stopband is 2.93 GHz; for Pattern D, which is twice the size, the lower corner frequency is 1.23 GHz. When high-K material is used in Pattern E the corner frequency is reduced back to 1.25 GHz. The bandwidth of Pattern E with the high-K material measured at -40 dB is almost the same as Pattern D. Therefore, the size reduction compensated by the high-K material is achieved as expected.

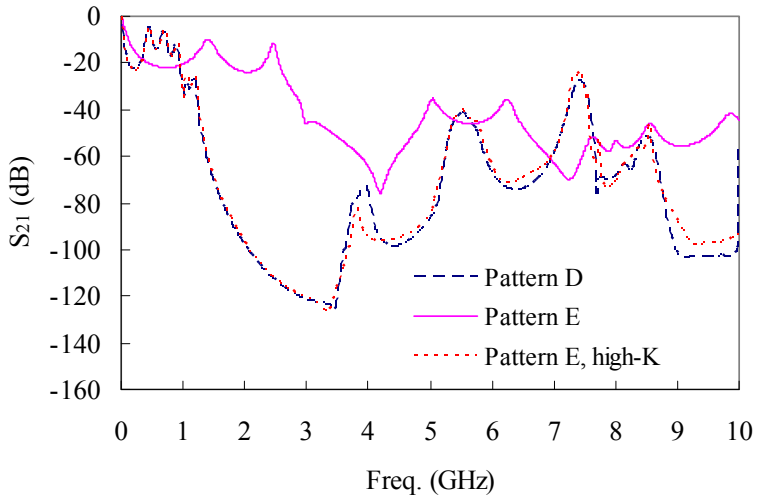


Fig. 5.17. Magnitudes of simulated S_{21} of Pattern D, Pattern E, and Pattern E with the high-K material.

The next design investigation is done by adding additional slits with L_r = 50% to the patches of the Pattern E EBG structure. The resultant geometry is called Pattern F, also shown in Fig. 5.16. The port locations are the same as those in

Pattern E and the dielectric constant is 4.2. Fig. 5.18 plots the transmission coefficients (S_{21}) of Pattern F, Pattern D, and Pattern E with the high-K dielectric. The lower corner frequency of the first stopband for this new structure Pattern F EBG is around 1.21 GHz, which is close to what is obtained for Pattern D with twice the area. The bandwidth obtained for the Pattern F case is wider compared to that of Pattern D (8.22 GHz). In comparison with the transmission coefficient of pattern E with the high-K dielectric, it can be observed that the same effect is obtained by adding the slits.

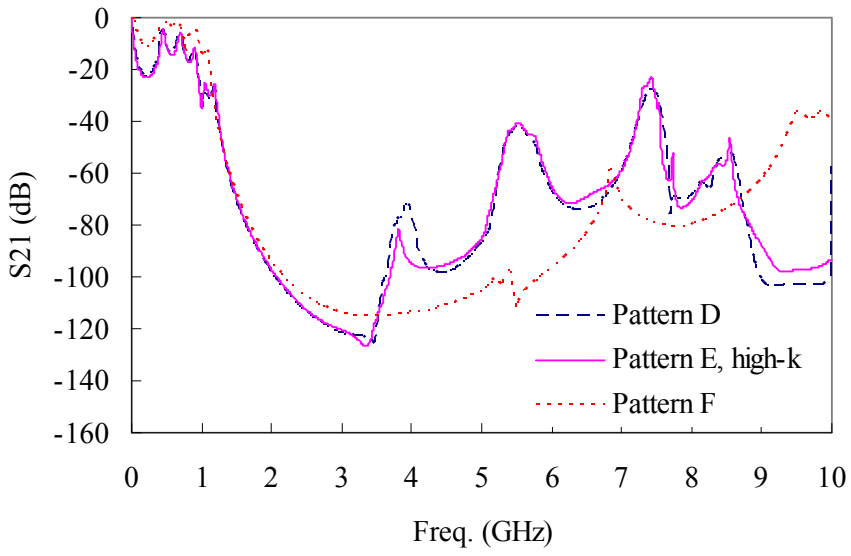


Fig. 5.18. Magnitudes of simulated S_{21} of Pattern D, Pattern F, and Pattern E with the high-K material.

5.4.2 Size reduction by combining the two approaches

In order to obtain more size reduction or further lower the cut-off frequency, the Pattern F EBG structure is examined when the high-K material is used. Fig. 5.19 shows the S_{21} for Pattern F with FR-4 ($\varepsilon_r = 4.2$), Pattern E with the high-K

material (ε_r = 17), and Pattern F with the high-K material (ε_r = 17). It is seen that adding extra narrow slits and high-K material shifts the lower corner frequency to 560 MHz while the isolation characteristic is also improved. Note that all the S_{21} simulations in Sections 5.2 to 5.4 are generated by using Ansoft SIwave solver.

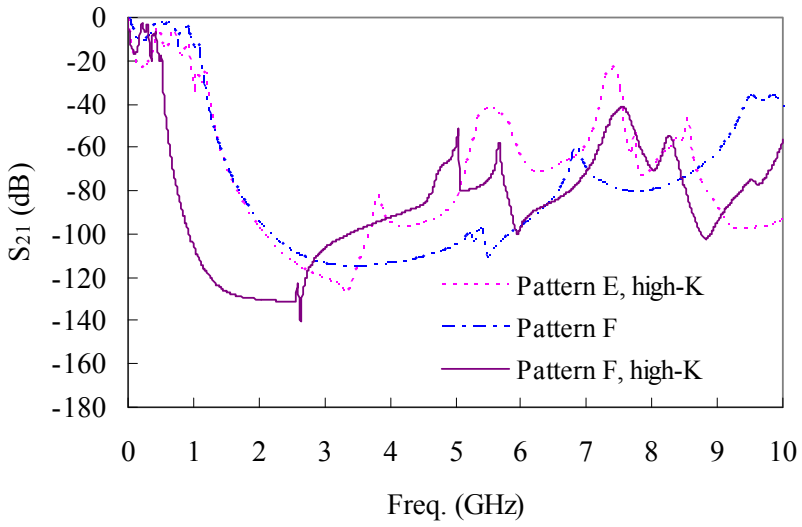


Fig. 5.19. Magnitudes of simulated S_{21} of Pattern F with FR-4 dielectric, Pattern E with high-K material, and Pattern F with high-K material.

Table 5.1 summarizes the dimensions and stopband characteristic of all investigated EBG structures.

Table 5.1. Summary of simulation results and geometrical characteristics of the 2-D EBG structures studied in Sections 5.3 to 5.4

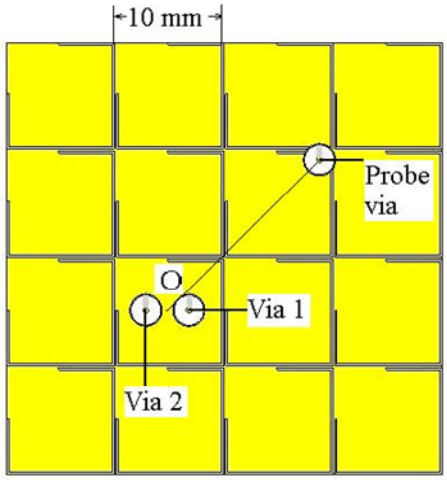
Pattern	Material (ε_r)	Patch side-length (mm)	Branch width (mm)	Slit length (mm)	Dielectric thickness (mm)	Lower corner freq.(GHz) (at -40 dB)	Bandwidth of the first stopband (GHz)
D	FR-4 (4.2)	20	0.2	0	0.2	1.23	4.43
E	FR-4 (4.2)	10	0.2	0	0.2	2.93	2.02
F	FR-4 (4.2)	10	0.2	5	0.2	1.21	8.22
E	high-K (17)	10	0.2	0	0.2	1.25	5.97
F	high-K (17)	10	0.2	5	0.2	0.56	7.05

5.5 Investigation of differential vias backed by an EBG structure

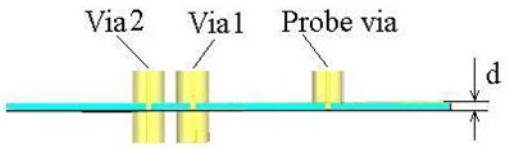
As described in Chapters 3 and 4, differential interconnects have the intrinsic property of reducing power/ground noise. These interconnects use a solid conductor as the reference ground. In this section, the effect of adding the studied uniplanar EBG as the reference ground in a differential interconnect system is studied to observe the combined effects in power/ground noise suppression.

The studied structures is shown in Fig. 5.20, in which the through via interconnect arrangement composed of Via 1, Via 2, and the Probe via, and their respective locations are the same as those in Fig. 3.13. The spacing between the differential vias is 4 mm. The probe via is 20 mm away and at the 45° direction to the midpoint of the line connected two differential vias. The board size is 40.6 mm by 40.6 mm and the thickness of the dielectric is d = 1.54 mm. The top metal layer is a 4 by 4 EBG structure with a unit-cell the same as Pattern F (shown in

Fig. 5. 16) except for the dielectric thickness. Three ports are at the locations of Via 1, Via 2, and Probe via, and are named as Port 1, Port 2, and Port 3, respectively. To evaluate the impact of adding the EBG structure, the configuration of Fig. 3.13 having a solid top conductor instead of the uniplanar EBG pattern is simulated as a benchmark for comparisons. Simulations are conducted using CST Microwave Studio which allows for full-wave time domain simulations.



(a)



(b)

Fig. 5.20. Differential vias with EBG structure. (a) Top view. (b) Side view.

The noise waveforms observed at the probe via are illustrated in Fig. 5.21. The differential input signals are ±250 mV and the risetime is 36 ps (0%-100%). As

one can see, the structure with EBG reduces the noise peak from 7.28 mV to 4.04 mV yielding about 45% noise suppression.

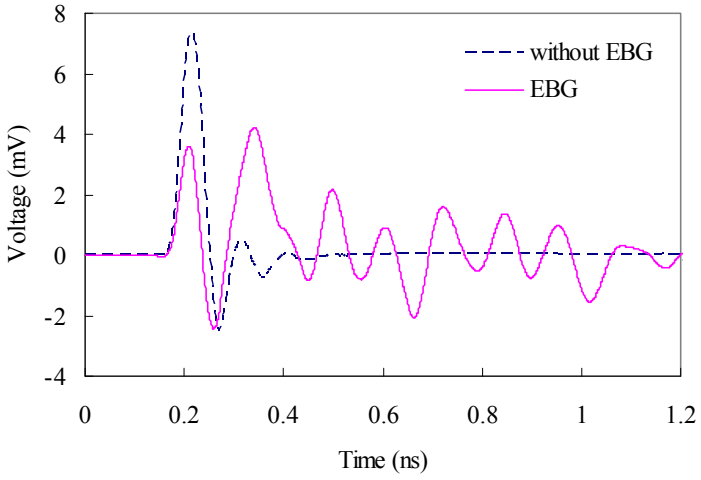


Fig. 5.21. The noise waveforms of the differential vias with and without the EBG structure.

It can be observed from Figure 5.21 that the noise waveform shows oscillatory behaviour when EBG is present. To further monitor this, the uniplanar EBG structure is modified. It is expected that creating wider stopband and lowering the beginning of the stopband can filter out the observed oscillations. First, the thickness of the dielectric is reduced to 0.2 mm. Then, three EBG structures are examined; 1) 10 mm × 10 mm EBG patches as shown in Fig. 5.20; 2) 20 mm × 20 mm EBG patches as shown in Fig. 5.22; 3) 10 mm × 10 mm EBG patches with a high-K dielectric material with $\varepsilon_r = 20$. All board sizes are 40.6 mm × 40.6 mm, and the slit length to patch width ratio is 50%. Widths of all slits and branches are 0.2 mm. The port locations are as shown in Figures 5.20 and 5. 22.

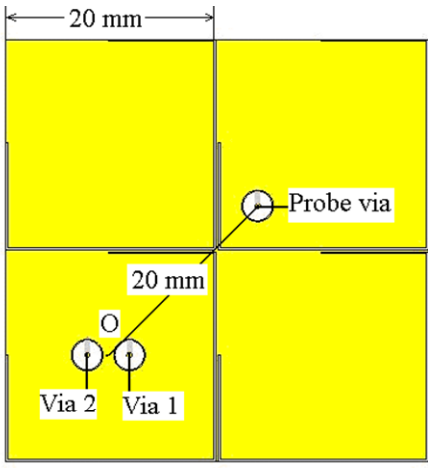


Fig. 5.22. Differential vias with EBG structure (20mm patches).

The noise waveforms in time-domain simulations by CST are plotted in Fig. 5.23. The differential excitations are ±250 mV and the risetime is 36 ps (0%-100%). The noise peak voltage of the solid planes is 1.5 mV. (Note that the thickness of the substrate is reduced compared to the previous case.) When EBG with 10 mm-length patches replaces one of the planes, the noise peak decreases to 0.48 mV, which presents 68% noise suppression. If the patch size increases to 20 mm, the noise peak voltage further decreases to 0.16 mV, which means 89% noise suppression. If 10 mm patches with ε_r=20 dielectric are employed, the noise peak is 0.25 mV, which causes 83% noise suppression. The EBG of 20 mm patches provides the best noise suppression. More importantly, the oscillations are reduced, which demonstrates filtering of this unwanted frequency in the induced stopband by the EBG structure.

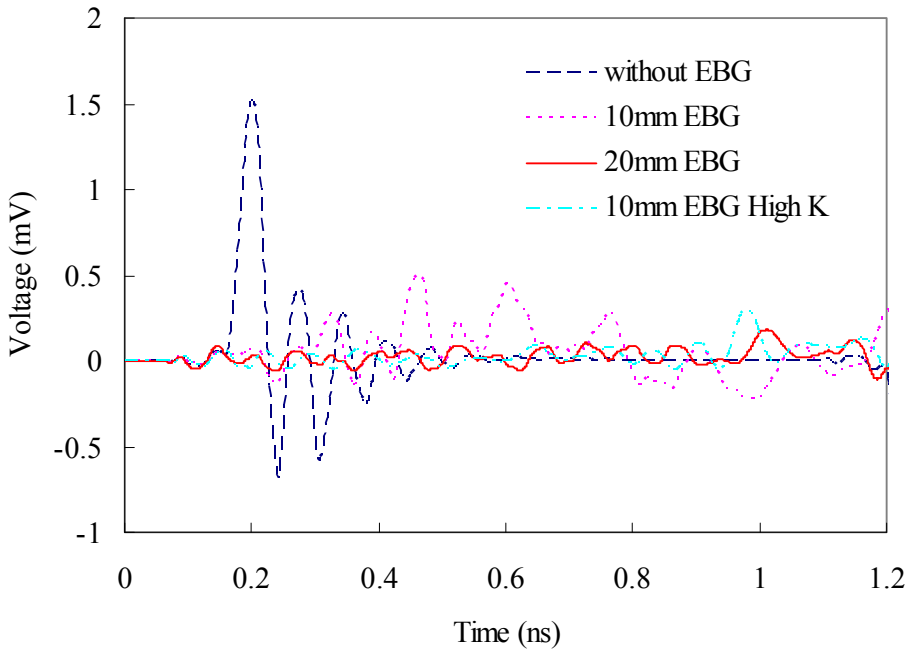


Fig. 5.23. The noise waveforms of the four examples generated by CST, all dielectric thicknesses are 0.2 mm.

5.6 Conclusions

To reduce the EBG footprint for low frequency operations, three effective approaches proposed in references [14]-[15] are applied to the uniplanar EBG and investigated through the simulations. These techniques include: introduction of narrow slits into the patches of the uniplanar EBG geometry; application of high dielectric constant materials; and combination of these two methods. Each approach is found to contribute to size reduction of the EBG structure. By applying the combination approach, a 30 mm × 30 mm EBG structure is designed at the GSM-850 bands providing excellent isolation characteristics. As well, a differential via structure penetrating the uniplanar EBG stack-up is investigated. The digital signals are transmitted through the differential via interconnects and voltage waveforms at another via port are observed. A noise peak reduction of

89% is achieved in one studied case by using this combination noise suppression technique.

Chapter 6 Conclusions

6.1 Summary of thesis and conclusions

Power/ground noise is a rising problem in modern electronic systems that are characterized by faster edge rates, higher operating frequencies, lower supply voltages, and denser layouts. This kind of noise excited by vias carrying time-varying currents creates power/ground noise and SSN in high-speed digital and mixed-signal circuits and results in additional electromagnetic interference (EMI) problems. The field of power integrity has become very popular due to the critical nature of designing power delivery network (PDN) of modern electronic systems. System designers look for fast methods for prediction of power/ground noise and quest for optimum methods to suppress this unwanted effect. 3-D Full-wave solvers can simulate any complicated PDN and predict the power/ground noise accurately, but they are costly in terms of simulation time and computational requirements. Hence, two analytical approaches that solve the electromagnetic problem of a parallel-plate PDN structure are investigated in this thesis. These techniques allow for the development of network models for PDN structures that are composed of a single parallel-plate pair, i.e. a parallel-plate waveguide (PPW), or a stack-up of parallel-plate pairs. Various PDN geometries with single or multiple vias are studied to predict the power and ground noise.

The two analytical approaches utilized in these studies are based on previous research works published in [3], [11], [16], [61], and [65]. The first one is the RTL method, which employs transmission line theory to derive analytical

expressions for calculating the network component model of the parallel-plate PDN. This model is easily integrated with other circuit components enabling global system simulations. Simulations using the RTL models are much faster and less accurate compared to the full-wave simulations, since the RTL method only considers a cylindrical coordinate TEM mode. As well, the analytical expressions do not include conductor and dielectric losses, thereby introducing some minor differences. This method is used to evaluate noise suppression by using discrete decoupling capacitors.

The other analytical approach uses a resonant cavity model for the PPW PDN. The derivations for the cavity method analysis of a parallel-plate structure are available in [11], [62]. The single summation equations for the PMC boundary conditions presented in [11] are used and extended for the case of PEC boundary conditions.

These expressions consider higher order modes, are full-wave, and include conductor and dielectric losses. In the same manner as the RTL model simulations, models based on the cavity method are obtained and ported to a commercial circuit simulator for global circuit simulations. It is found that this method provides quite accurate results compared to those of the commercial full-wave simulators while drastically reducing the simulation time, especially for the case of multilayer PDN structures. Moreover, the cavity method is employed to investigate noise suppression by using differential vias embedded in a PPW. This approach offers a fast means for conducting parametric studies and generating the

noise map on the power/ground planes. It is demonstrated that noise suppression by differential vias changes with the location of the observation point.

A simple test structure is fabricated in order to evaluate the analytical models developed by using the RTL and the cavity methods. Measurement results prove to be consistent with the simulation results from the RTL and the cavity models.

EBG structures have been recently proposed as another means for power/ground noise suppression. To investigate this method, a uniplanar EBG structure is studied in Chapter 5 of this thesis. Designing an EBG structure for operation at the low frequencies needed for noise suppression can be challenging due to the relatively large footprint of the unit cell. In order to obtain a compact size uniplanar EBG structure, miniaturization approaches are investigated in this thesis. Two design methods, which are originally in [14], [15], are employed. It is shown herein that either modification of the layout of the EBG unit cell or employing high-K dielectric materials pushes the EBG stopband to lower frequencies; thus, each are applicable as a design miniaturization approach. Furthermore, combination of the two methods provides a stopband starting from a much lower frequency. Thus, when system design specifications include compactness and low noise low frequency operations, these techniques can be employed to achieve the desired stopband by using a smaller EBG structure. Finally, a differential via pair going through the uniplanar EBG PDN is simulated in the time domain in order to monitor the EBG impact on the noise peak. It is demonstrated that employing EBG structures and differential signalling can further reduce the noise on power/ground planes. The EBG design is optimized in

this study in order to minimize the noise peak and eliminate the excess ringing in the noise signature.

6.2 Future work

In practice, the power/ground planes in multilayer packages and boards are perforated by many vias and their pertinent anti-pads (clearances). Moreover, sometimes split power/ground planes or partitioned conductor planes are needed in order to isolate a high noise section from noise sensitive circuits. This is especially practiced in mixed-signal circuits. Often, the power/ground planes take irregular shapes while the studied methods herein only account for regular shapes. Therefore, further investigation of power/ground noise should include these practical situations. For this situation, new models to represent these practical situations and account for the possible common discontinuities are needed. This might introduce overly complex models that would require longer time for implementation and simulations, thus losing the fast prediction advantage of the technique. Therefore, this direction for generalizing the models needs further investigation.

It is very important that more examples of system co-simulations are investigated and that the approach is extended from a simple FPGA system to a more populated digital analog and mixed-signal circuits.

Another significant direction for extending this thesis is the application of miniaturization methods to other EBG geometries. Fabrications and

measurements of test prototypes to evaluate this technique are the next needed steps.

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