Fabrication and characterization of gallium nitride high electron mobility transistors

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Abstract

Compound semiconductor gallium nitride high electron mobility transistors (HEMTs) have significant potential for use in the electronics industry, including radar applications and microwave transmitters for communications. These wide band gap semiconductors have unique material properties that lead to devices with high power, efficiency, and bandwidth compared with existing technologies. In this work, the electrical properties of gallium nitride HEMTs on silicon substrates were studied in the context of drain characteristics and breakdown voltage. The design, fabrication, and characterization of different devices are presented, in addition to a discussion on the effects of annealing and different gate contact materials. While demonstrating considerable promise in the field of high power radio frequency (RF) applications, this technology is yet immature and several fabrication issues still need to be addressed. The goal of this work is to represent a stepping stone in further developing this technology to be used in high power devices.

Résumé

Les transistors à haute fréquence (HEMTs) composés de nitrure de gallium (GaN) possède un énorme potentiel dans l'industrie de l'électronique, y compris les applications radar et les émetteurs à micro-ondes. Ces semi-conducteurs à large bande ont des propriétés matérielles uniques qui mènent à des appareils d'haute puissance, haute efficacité et possédant une bande passante élevée par rapport aux technologies existantes. Ce travail étudie les propriétés électriques des HEMTs de nitrure de gallium dans le contexte des caractéristiques de drain et de la tension de claquage. La conception, la fabrication et la caractérisation des HEMTs différents sont présentées, en plus d'une discussion sur les effets de différents matériaux de contact de grille et sur le recuit. Quoique cette technologie promet d'être fructueuse dans le domaine des radiofréquences (RF), elle demeure immature et les obstacles liés aux procédures de fabrication doivent être adressés. Dont, ce travail représente une étape dans le développement de cette technologie utilisable dans les appareils à haute puissance.

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1 Introduction

Silicon is the most commonly used material in semiconductor fabrication, due to its abundance and the low cost. However, recently focus has shifted to wide bandgap semiconductors, which have shown considerable promise for use in power electronics. While several III-V materials such as gallium arsenide (GaAs) and indium phosphide (InP) have long been developed, gallium nitride (GaN) has more recently attracted attention in this field. With a direct bandgap of 3.4-3.5eV, GaN has several unique attributes such as superior voltage breakdown properties that make it appealing for optoelectronics, high power, and high frequency devices. In particular, GaN-based high electron mobility transistors (HEMTs) have demonstrated excellent high-power performance and output power densities exceeding that of any other RF field effect transistors. Application fields include communications, signal processing, imaging, and much more.

The concept of modulation doping was first demonstrated by Dingle et al. of Bell Labs in 1978 [1.1]. Made possible through the atomic layer precision growth abilities of molecular beam epitaxy (MBE), modulation doping leads to the formation of a two-dimensional electron gas (2DEG) at the interface between two materials with different bandgaps. The spatial separation between the dopants and electrons thus results in high mobility due to less ion scattering. Though modulation doping is not the only way of achieving a 2D carrier system, and polarization doping and applying a vertical electric field to an appropriate heterostructure both work as well, it was based on this first work on modulation that the invention of the heterostructure field effect transistor or HEMT came

about in 1980, credited to Takashi Mimura from Fujitsu Laboratories [1.2]. A high electron mobility transistor is a type of field effect transistor that employs high mobility electrons generated by a heterojunction instead of a doped region as the channel. The 2DEG-produced enhanced electron mobility allows for higher gain, higher frequency operation, and faster switching speeds, compared to conventional devices such as gallium arsenide (GaAs) metal semiconductor field effect transistors (MESFETs). In their initial version, Mimura and his group demonstrated enhanced mobility of the 2DEG in selectively doped GaAs/*n*-AlGaAs heterojunctions and confirmed the material's potential for high-speed integrated circuits. Representing a triumph in bandgap engineering, the HEMT's significance lies in its high performance capabilities where it demonstrates excellence noise and power characteristics.

In 1985, HEMTs entered the commercial field, as a cryogenic low-noise amplifier developed by Fujitsu for radio telescopes and have been in use ever since, far outperforming their GaAs MESFET counterparts [1.3]. Commercialization significantly increased in 1987 in the communications area as GaAs MESFETs started to get replaced in broadcasting satellite receivers, due to the excellent f_T and high aspect ratio of the channel of AlGaAs/GaAs HEMTs.

Besides the start of commercialization, the mid-1980's were also an important time for HEMT development, as new innovations came about. One of these was the development of the pseudomorphic HEMT (pHEMT), with an AlGaAs/InGaAs/GaAs quantum well structure [1.4]. A pHEMT avoids the problem of lattice mismatch (where two materials such as AlGaAs and GaAs have different lattice constants, resulting in crystal defects) by using a thin layer of one

of the materials, which stretches to fit the other. In this structure, the enhanced electron transport properties and carrier confinement in the InGaAs quantum well contributed to improved device scalability and performance.

A metamorphic HEMT, or mHEMT, is a pHEMT variant, where a buffer layer is placed between materials of different lattice constants. This structure has been realized in a GaInAs/AlInAs device [1.5]. GaInAs/AlInAs on InP has in fact demonstrated particularly good characteristics in terms of noise and frequency.

While GaAs as a material has undergone extensive research, several other materials have experienced parallel work. Examples of these materials include the aforementioned GaInAs/AlInAs [1.6], as well as InAs/AlSb [1.7] and Si/SiGe [1.8]. Modulation-doped two dimensional hole gases and high hole mobility transistors are yet another development in this field, with materials such as InGaAs/GaAs [1.9], GaInAs/InP [1.10], GaSb/AlSb [1.11], and InGaSb/AlGaSb [1.12].

These studies on other materials have thus led to an interest in AlGaN/GaN. GaN has a wide bandgap, which results in a high breakdown voltage, making it very attractive for high voltage operation transistors. Other properties such as its high heat capacity and high electron saturation velocity have led to much excitement over this material and its prospects for use in HEMT structures. While major research into GaN crystal growth started in the 1960's and the first successful growth of GaN on a sapphire substrate was in 1969 by Maruska and Tietjen [1.13], a 2DEG was not observed until 1992 by Kahn et al. [1.14]. Following up on this work, the first AlGaN/GaN HEMT was developed in 1994 [1.15]. Grown in a low pressure metal-organic chemical-vapor deposition

reactor, the AlGaN/GaN heterostructure may be seen in Figure 1.1. With a gate length and width of 0.25 μm and 150 μm, the device had GaN and $Al_{0.13}Ga_{0.87}N$ layers that were 0.6 μm and 250Å thick, respectively. Refractory metals TiAu and TiW were used for the source-drain and gate contacts.

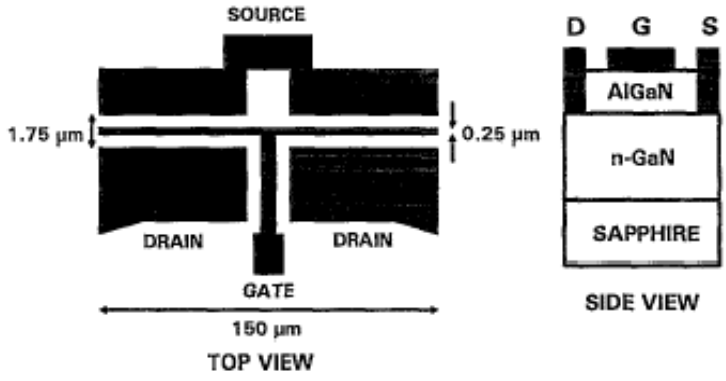


Fig. 1.1 – AlGaN/GaN HEMT structure [1.15]

Since this initial device, interest has grown enormously and several efforts have been made to improve device operation. One innovation was the introduction of Si_xN passivation in 2000, which reduced surface trap state-caused DC-to-RF dispersion and resulted in a significant increase in output power [1.16]. Another development came about in 2003, with the use of a field plate, which both increased the breakdown voltage and helped to further reduce dispersion [1.17], and in 2006, an improvement over this field plate was made, with the use of a slant field plate [1.18]. More recent work has focused on optimizing device performance through various fabrication procedures, such as through thermal oxidation treatments [1.19] and annealing [1.20]. Several key milestones in the evolution of GaN HEMT development may be found in Table 1.1, while a future roadmap of the market for this technology for respective frequencies is summarized in Figure 1.2.

Table 1.1 – Key milestones in GaN HEMT development

1969	First successful GaN growth on sapphire substrate [1.13]
1978	Introduction of modulation doping [1.1]
1980	Invention of HEMT [1.2]
1992	Observation of 2DEG in AlGaN/GaN heterostructure [1.14]
1994	First AlGaN/GaN HEMT [1.15]
2000	Introduction of surface passivation [1.16]
2003	Use of a field modulation plate [1.17]

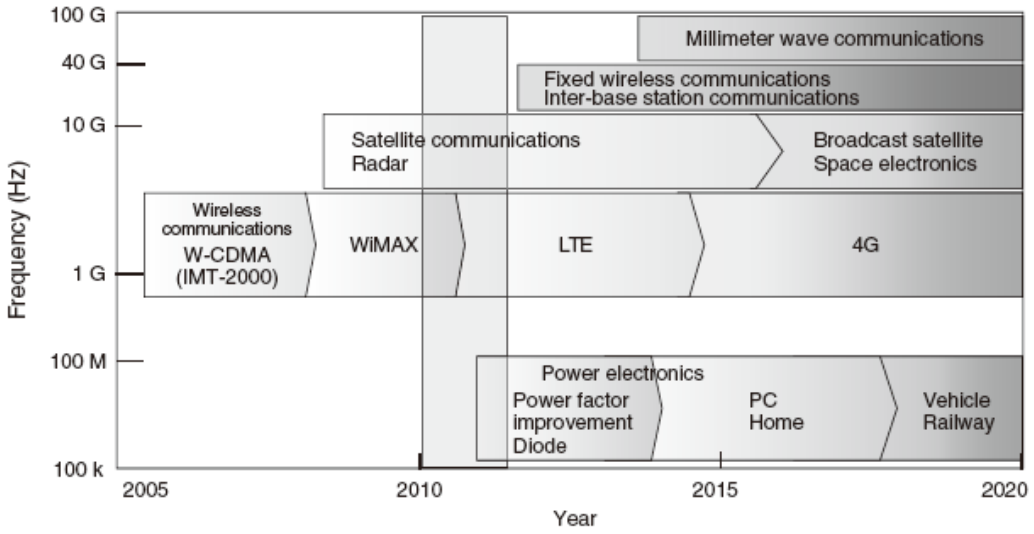


Fig. 1.2 – Future prospects of GaN HEMTs [1.21]

While GaN transistors have lately been introduced to the semiconductor market, there still remains much work to be done in order to further establish this

technology. This work represents a preliminary step to further the development of GaN-based HEMTs since this technology is not yet mature and much remains to be done before it can reach the level of advancement of more conventional devices with materials such as silicon or gallium arsenide. For this work, we have designed and fabricated various AlGaN/GaN HEMTs on silicon substrates, using different gate contact combinations of titanium/gold, nickel/gold, platinum/gold, and chromium/gold. We have investigated the performance of these devices by performing electrical measurements at room temperature, characterizing them in terms of breakdown voltage and current-voltage measurements. We have also investigated the effects of annealing on device behavior.

In this work, chapter 2 describes the properties and characteristics of semiconductors, with further details on gallium nitride as a material. Chapter 3 explains the physics behind heterostructures, as well as the operational principles, structure, and characteristics of HEMTs, while also discussing the specific features and applications of GaN HEMTs. Chapter 4 introduces the details of the device fabrication procedure. Chapter 5 describes the experimental setup and elaborates on the electrical measurement methods used to characterize the devices. Finally, chapter 6 presents the results of the experimental measurements and provides a discussion on these results.

2 Semiconductors

2.1 Semiconductor Characteristics and Properties

Semiconductors are materials with an electrical conductivity between that of a conductor and that of an insulator. They are very useful materials for electronic devices, as they are quite versatile and their electrical properties can be greatly varied through factors such as impurity concentration, optical excitation, and temperature. Semiconductors are formed by either elements from group IV of the periodic table such as silicon, or composed from a combination of elements that lie in columns of one less or one more valency from column IV, such as III-V materials like gallium nitride. Ternary and other compounds can also form semiconductors, such as copper indium diselenide.

Different materials act in different ways and have diverse properties that can be applicable to many areas. An intrinsic semiconductor is a pure semiconductor composed of either one element or one single compound that does not contain any dopants. An extrinsic semiconductor, on the other hand, is a semiconductor that has been doped, which can dramatically change the material properties. Materials are doped with impurities that take the form of acceptors (holes) or donors (electrons), forming a p-type or n-type semiconductor, respectively. Group III atoms act as acceptors to group IV semiconductors, while group V atoms act as donors. Similarly, for III-V binary compounds, group II atoms act as acceptors and group VI atoms act as donors, while group IV atoms can be used as either. In n-type semiconductors, electrons are the majority carriers with holes as the minority carriers, and vice versa for p-type semiconductors.

Materials are often characterized by their crystal structure, which can affect many properties such as electronic band structure and optical transparency. While atom arrangement in a material can be named as crystalline, polycrystalline, or amorphous, semiconductors of concern are typically crystalline. The crystal structure of a material can be described through a unit cell, which is its simplest form, and which can describe the structural properties of the bulk material. Examples of these unit cells are the diamond lattice unit cell for carbon and the zincblende lattice unit cell for GaAs. Some materials can exist in more than one crystal structure, which is called polymorphism. Crystal orientation is important as well, as it determines the surface density of atoms, which can affect both the electrical and optical properties of a material.

Energy bandgaps also play an important role in semiconductor physics, as several material properties such as electrical conductivity are related to the bandgap. The bandgap is the energy range in which no electron states exist, and is the difference between the top of the valence band and the bottom of the conduction band. It is also the energy that an outer shell electron needs to escape from its orbit around the nucleus and become a mobile charge carrier, which it gains by absorbing either a photon or a phonon. Large bandgaps are typical of insulators, whereas semiconductors usually have smaller bandgaps and metals have either a very small or no bandgap. A larger bandgap implies more energy required for an electron to move from the valence band to the conduction band. Materials with large bandgaps are often used for high-temperature and high-voltage applications.

The semiconductor lattice will expand or contract with changes in temperature, which also changes the electron-lattice interaction. Thus, the bandgap depends on temperature and follows Varshni's equation:

$$E_g(T) = E_g(0) - \frac{AT^2}{T+B}. \quad \text{(Eq. 2.1)}$$

In this equation, $E_g(0)$ is the energy bandgap at 0K, and A and B are constants, with temperature T measured in Kelvins. The bandgap can also be affected by other forces, such as strain or stress. When compressive hydrostatic pressure is applied, for example, the interatomic spacing is decreased, which results in an increase in the bandgap. The composition of semiconductor alloys, such as InGaAs, also plays a role in controlling the bandgap of the material.

Another classification of bandgaps is whether they are direct or indirect. A direct bandgap occurs when the momentum for electrons and holes is the same in both the conduction and valence bands. In semiconductors with direct bandgaps, energy and momentum are conserved through the emission or absorption of a photon. For semiconductors with indirect bandgaps, the conduction band minimum and valence band maximum do not match and a phonon-assisted emission is needed. Silicon, as an example, has an indirect bandgap, limiting its applicability in optoelectronics, while III-V materials such as GaAs usually have direct bandgaps and are required to build efficient emitters and amplifiers.

Mobility is the ability of holes or electrons to move through a medium in response to an electric field, and the product of mobility and carrier concentration is directly related to conductivity. Semiconductor device behavior greatly depends on mobility, whether there are many electrons with low mobility or few electrons

with high mobility, and so on. Mobility itself depends on impurity, defect, and carrier concentrations, as well as temperature and the applied electric field. Mobility is defined by the equation:

$$v_d = \mu E \quad \text{(Eq. 2.2)}$$

where v_d is the magnitude of the electron drift velocity, μ is the electron mobility, and E is the magnitude of the electric field applied. Besides effective mass, the main factor that affects drift velocity is scattering time. The most common scattering sources are ionized impurity scattering and lattice scattering (acoustic phonon scattering). The former is when Coulombic forces deflect an electron or hole approaching an ionized (charged) impurity. The latter is when vibrating atoms create phonons, which can collide with an electron or hole and scatter it.

There are many other material properties that are important for semiconductors and their applications. Thermal conductivity, as an example, is the ability of a material to conduct heat. It is an important parameter to take into account for applications with high operating temperatures. Wide bandgap semiconductors tend to have high thermal conductivities. Saturation velocity is another important parameter. As the maximum velocity a charge carrier can reach when submitted to an electric field, fast response times of semiconductor devices depend on this value. A final relevant characteristic that should be discussed is the breakdown field of a material. The breakdown voltage is the maximum reverse bias magnitude that can be applied before a device starts to conduct with a large reverse current. Some devices also have a forward breakdown voltage. GaN devices in particular have been lauded for their high thermal conductivity and

breakdown voltage properties. A table of several important properties for various materials may be found in Table 2.1.

Table 2.1 – Semiconductors and their properties [2.1, [a]2.2, [b]2.3, [c]2.4]

	Si	**GaAs**	**InP**	**6H SiC**	**GaN**
Crystal Structure	Diamond	Zincblende	Zincblende[c]	Hexagonal[b]	Wurtzite[b]
Band Gap (eV)	1.12	1.424	1.35	3.26	3.49
Band Gap Type	Indirect	Direct	Direct[a]	Indirect	Direct
Electron Mobility ($cm^2/V{\cdot}s$)	1450	8500	5400[a]	700[a]	1000-2000[a]
Thermal Conductivity (W/cm·K)	1.5[a]	0.5[a]	0.7[a]	4.5[a]	>1.5[a]
Saturated (peak) Electron Velocity ($*10^7$ cm/s)	1.0 (1.0)[a]	1.3 (2.1)[a]	1.0 (2.3)[a]	2.0 (2.0)[a]	1.3 (2.1)[a]
Breakdown Field (MV/cm)	0.3	0.4	0.5[a]	3.0[a]	>3.0[a]

2.2 Gallium Nitride

While silicon has long been the dominant material in the semiconductor industry, as a result of its abundance and low manufacturing cost, many other materials have become popular especially in areas where the properties of silicon

fall short. Wide bandgap semiconductors such as III-V materials have bandgaps much larger than 1eV (far greater than that of silicon or gallium arsenide). As mentioned, these materials are often used in high-temperature and high-voltage operations, especially since silicon-based devices are reaching their limits in terms of operating frequency, breakdown voltage, and power density. Materials that have small atoms with strong electronegative atomic bonds tend to have wider bandgaps and III-V nitrides such as gallium nitride have the largest bandgaps.

Gallium nitride is a III-V semiconductor with a direct bandgap of about 3.4-3.5eV. GaN usually takes on a non-centrosymmetric hexagonal wurtzite crystal structure, which is a structure that lacks inversion symmetry. This crystal structure is similar to the zincblende structure, though it has a hexagonal close-packed Bravais lattice instead of a face centered cubic structure. One of the differences between the two structures is in their parameters; whereas zincblende structures have only one lattice constant to specify the crystal, the wurtzite structure has three: lattice constant *a* (3.19Å for GaN), the *c/a* ratio (1.627), and the ratio of bond length along the *c* direction to the other three bond lengths (1.004) [2.5]. The bond length *d* (1.951Å) is also used to scale various physical quantities [2.5]. GaN's piezoelectric and pyroelectric properties are a result of this crystal structure. Pyroelectricity is the electric potential that can result from heating a certain material, while piezoelectricity is the electric charge that accumulates in a material due to an applied mechanical stress.

Due to its direct bandgap and high frequency characteristics, GaN originally found use in optoelectronics and RF applications. Shuji Nakamura of Nichia Chemical Industries was able to fabricate green, blue, and other light emitting diodes in the 1990's using GaN [2.6-2.8]. However, it was also seen that GaN has potential for high power electronics applications. One of the most important attributes of GaN as a result of its large bandgap is its breakdown field, at more than 3 MV/cm, far outclassing that of silicon and even GaAs, the more conventional industry materials [2.2]. With a higher electric breakdown field, a higher breakdown voltage is obtained and higher doping levels can be achieved, so that device layers can be made thinner, resulting in smaller drift region resistances, thus promising far superior devices compared to conventional silicon.

GaN also has excellent thermal conductivity at over 1.5 W/cm·K and can operate at much higher temperatures than silicon. As temperature increases, the thermal energy of electrons in the valence band increases and once they have enough energy, the electrons move up to the conduction band, which represents unwanted uncontrolled conduction, which occurs at around 140°C for silicon [2.2]. Since GaN has such a large bandgap, electrons in the valence band require more thermal energy to move to the conduction band. A similar situation can be said for radiation hardening, as radiation energy can excite an electron as well. Thus, GaN can withstand higher amounts of heat and radiation while maintaining its electrical characteristics, and can be used in extreme conditions. Along with its high electron mobility, high saturation velocity, and other excellent properties (see Table 2.1), GaN presents an excellent material for devices such as high electron mobility transistors.

Of course there are challenges with this material. GaN does not have a native oxide (such as silicon dioxide for silicon), which is a drawback for MOS devices. Furthermore, GaN has a rather poor crystal quality, with a dislocation density of about 10^8-10^9 cm^{-2} [2.9]. GaN and AlGaN/GaN heterostructures are typically grown epitaxially on various substrates, though there is currently no inexpensive substrate material for it. As there is great difficulty in growing GaN boules, most experiments use sapphire or SiC substrates, with 14.8% and 3.3% lattice mismatch, respectively [2.2]. A typical growth method for GaN is metal-organic vapor phase deposition.

As this technology has not yet matured, there is low yield due to processing problems and difficulties, as well as high cost, limited availability, and the need for high-temperature packaging techniques. There is thus much work to be done before this technology can compete on fairer ground with already-established materials.

3 GaN High Electron Mobility Transistors

3.1 Heterostructure Physics

Heterostructures are a key component in modern devices such as HEMTs. A heterostructure is structure that consists of two or more semiconductors of different bandgaps chemically bonded together. A heterojunction is the interface between two such materials and is an essential component to most electronic and optoelectronic devices. It forms a two-dimensional channel for carriers with superior transport properties. There are three types of heterojunctions, seen in Figure 3.1: a straddling gap, a staggered gap, and a broken gap. Type 1 heterojunctions are the most common and GaN/AlGaN forms this type. These three junctions can be classified through work function, electron affinity, and bandgap. The work function φ represents the difference in energy between the chemical equilibrium energy (Fermi level) and the vacuum level, while the electron affinity χ represents the difference in energy between the conduction band and the vacuum level. The band offsets (conduction band and valence band differences, ΔE_c and ΔE_v) are also important for characterizing a heterojunction.

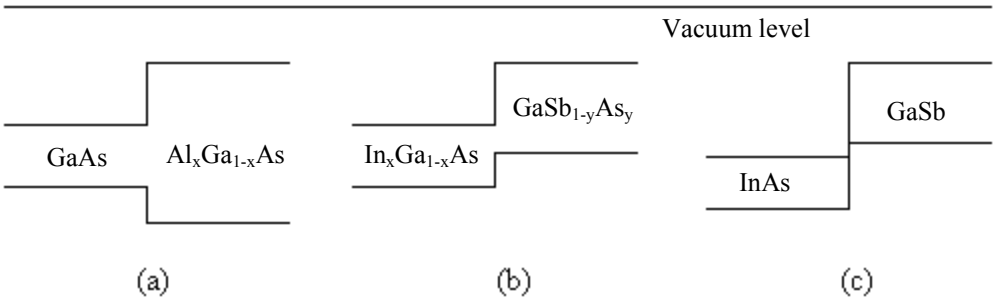


Fig. 3.1 – (a) Type 1 (b) Type II and (c) Type III semiconductor heterojunction types

Anderson's model can be used to construct energy band diagrams of ideal heterojunctions, based on aligning the vacuum levels of the two semiconductors at the same energy. However, it is an idealized model and does not predict actual band offsets. This model ignores the fact that the material components of the heterostructure are crystalline and that their electrical properties are dictated by a periodic arrangement of atoms, with this periodicity broken at the heterojunction interface. While early research favored materials with similar lattice constants, it is also possible to grow good quality heterostructures from semiconductors with different lattice constants. As long as the grown layer thickness does not exceed a certain critical value, lattice mismatch can be accommodated through dislocations and other interfacial defects.

An AlGaAs/GaAs heterojunction is shown in Figure 3.2. Once the two materials are combined to form the heterojunction, electrons are transferred from the AlGaAs to GaAs, due to the smaller electron affinity of AlGaAs. The electrons thus form a depletion region in the AlGaAs and an accumulation region in the GaAs. The accumulation region can form a triangular potential well, and the electrons in this well form a two-dimensional electron gas (2DEG), with quantized energy [3.1]. Similarly, in a p-type isotype heterojunction,

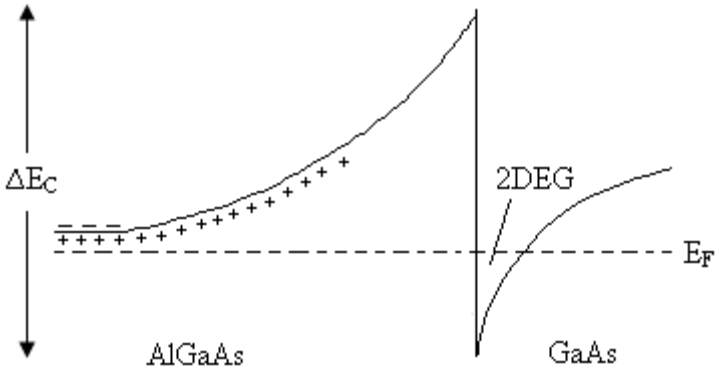


Fig. 3.2 – Energy band diagram of an *n*-AlGaAs/GaAs heterojunction

a 2D hole gas will be formed in the well created by the valence band discontinuity.

Generally fabricated using MBE or chemical vapor deposition, heterostructures are used in many applications, such as in lasers, as the base-emitter junction of a bipolar junction transistor, and, most particularly, in HEMTs.

3.2 HEMT Structure and Operation Principle

A high electron mobility transistor is a field effect transistor (FET) similar to a metal-oxide-semiconductor FET (MOSFET), with the exception that it uses the two-dimensional electron gas created at the heterojunction as the channel instead of a doped region. Current flows through the channel between the source and drain and is controlled by the space charge, which is affected by applying a voltage to the gate contact. When a positive voltage is applied to the drain, current transport along the 2DEG will start due to the potential drop between the source and the drain, and the magnitude of this current is controlled by the gate bias.

Electrons pass through a couple of heterojunctions between the source terminal and the 2DEG, and between the 2DEG and the drain terminal. The electrons tunnel from the N^+ GaAs source into the N^+ AlGaAs layer and from the drain end of the 2DEG back into the N^+ AlGaAs, resulting in significant source and drain resistances, which negatively affect high-speed and noise performance. The gate resistance can also have a considerable effect on noise performance. The gate takes the form of a Schottky contact created between the source and drain and controls the device current. A negative gate voltage reduces the channel electron concentration and can completely repel the electrons, thus turning off the device. HEMTs act therefore as a depletion-type FET.

While electrons exhibit properties of both particles and waves, the wave properties are negligible when device dimensions are much larger than the electron wavelength. However, as the width of the triangular potential well of a HEMT approaches zero at the tip, the electron wavelength becomes larger than the well width and quantum-mechanical effects come into effect. No electron can be placed at an energy level lower than that corresponding to the half-wavelength of the electron, which is the first energy subband. Here, electrons appear as standing waves. They do not move freely and are not randomly scattered in the direction of the well cross-section. As the potential well is larger in the other two directions, electrons are free to move and are randomly scattered in those directions. The 2DEG of a HEMT is a gas of electrons confined to a triangular quantum well that are able to move freely in these two dimensions, but not in the third.

The second energy subband is the energy level corresponding to a full electron wavelength. The energy separation between subbands depends on electron wavelength and the slope of the side of the potential well, which is related to the electric field that creates the well in the first place. The effect of the separation between particular subbands is called the quantization effect. A pure 2DEG appears when the lowest subband is populated, with the others empty. In an AlGaAs/GaAs heterojunction, for example, the conduction band discontinuity, energy band bending, and electron wavelength in GaAs combine to give a high amount of energy level quantization. The Fermi level in this case is actually positioned above the lowest energy subband, meaning that the lowest subband is populated with electrons, so that no external field is needed to create the 2DEG.

The unique properties of a HEMT are attributed to the 2DEG carrier channel. Modulation doping is a concept that leads to a 2DEG with high carrier mobility. While modulation doping was later found to not be the only method of forming two-dimensional carrier systems, it is the primary and earliest mechanism that led to these devices. A modulation-doped structure is a heterostructure consisting of a doped wide-bandgap semiconductor and a narrow-bandgap semiconductor. Carriers from the dopants in the wide bandgap semiconductor are transferred to the other material due to the presence of lower energy states, causing band bending. A free electron gas is created in the narrow bandgap material at the interface between the two. Electrons are spatially separated from donors, reducing ionized-impurity scattering, and can be further separated with a spacer layer. This separation allows for extremely high mobility.

Besides the traditional HEMT design, there are several design variations. The pseudomorphic HEMT or pHEMT is one such variation. As the materials forming a heterostructure generally have different lattice constants, crystal defects are formed, which lead to the creation of deep-level traps, reducing device performance. To alleviate this effect, a pHEMT employs an extremely thin layer of one of the materials so that the crystal lattice stretches to fit the other material, allowing the fabrication of devices with larger bandgaps than would otherwise be possible. Another variation, the metamorphic or mHEMT is similar in that it uses a buffer layer between the two semiconductors with different lattice constants.

HEMTs have several advantages over other FETs. A small channel compared to gate-to-channel distance is desirable, along with a small gate-to-channel distance compared to gate length, and these are more easily obtained in a

HEMT than with a MESFET. Additionally, it is possible to achieve high transconductance and thus higher speed due to the high channel mobility, which also results in a reduction of parasitic and access resistances. This reduction in turn allows for lower-noise performance and high power efficiency.

3.3 Polarization and Surface States

One of the unique characteristics of heterostructures of wurtzite semiconductors such as AlGaN/GaN is their polarization mechanisms. There are two particular polarization types that contribute to the overall polarization in an AlGaN/GaN heterostructure: spontaneous and piezoelectric polarization. Spontaneous polarization, also called pyroelectricity, is the built-in polarization field that exists in an unstrained crystal. This electric field is due to the lack of inversion symmetry of the crystal and the fact that the atoms are not purely covalently bonded, which results in the electron charge cloud being displaced toward one atom in the bond. The asymmetric electron cloud produces a net positive charge at one face of the crystal and a net negative charge at the other.

Piezoelectric polarization is the polarization field that results from crystal lattice distortions. As there is a large lattice mismatch between AlGaN and GaN, the AlGaN layer grown on the GaN buffer layer is strained and due to the large piezoelectric coefficients of the respective materials, this strain leads to a sheet charge at both faces of the AlGaN layer.

Values of the spontaneous and piezoelectric polarization and dielectric constants of AlN and GaN may be found in Table 3.1, along with elastic constants

of wurtzite and cubic AlN and GaN in Table 3.2. The strain in the AlGaN layer due to the Al content is given by:

$$\varepsilon = (1 - r)(\frac{a_{AlGaN} - a_{GaN}}{a_{AlGaN}}) \quad \text{(Eq. 3.1)}$$

with *a* being the in-plane lattice constant and *r* being the amount of strained relaxation [3.2]. Following this, with c_{13} and c_{33} as elastic constants given in Table 3.2, the piezopolarization component of AlGaN is given by [3.2]:

$$P_{pz}(AlGaN) = 2\varepsilon[e_{31} - e_{33}(\frac{c_{13}}{c_{33}})] \quad \text{(Eq. 3.2)}$$

Thus, assuming the GaN bulk is fully relaxed and the spontaneous polarization along the *c*-axis of the wurtzite crystal is $\mathbf{P}_{SP} = P_{sp}z$, the total polarization vectors for GaN and AlGaN are given by [3.2]:

$$P_{Tz}(GaN) = P_{sp}(GaN) + 0,$$

$$P_{Tz}(AlGaN) = P_{sp}(AlGaN) + P_{pz}(AlGaN) \quad \text{(Eq. 3.3)}$$

The total heterointerface charges (σ) can be evaluated for the AlGaN surface and the AlGaN/GaN interface [3.2]:

$$\sigma_{surf} = -[0 - P_{TZ}(Al_xGa_{1-x}N)] \quad \text{(Eq. 3.4)}$$

$$\sigma(m) = \sigma_{AlGaN/GaN}(x) = -[P_{TZ}(Al_xGa_{1-x}N) - P_{Tz}(GaN)] \quad \text{(Eq. 3.5)}$$

Finally, the total piezoelectric and spontaneous polarizations can be given by [3.2]:

$$P_{pz}(Al_xGa_{1-x}N) = 2(\frac{a(0)-a(x)}{a(x)}) \times [e_{31}(x) - e_{33}(x)\frac{c_{13}(x)}{c_{33}(x)}]\frac{C}{m^2} \quad \text{(Eq. 3.6)}$$

$$P_{sp}(Al_xGa_{1-x}N) = -0.052x - 0.29\frac{C}{m^2} \quad \text{(Eq. 3.7)}$$

$$P_{sp}(GaN) = -0.029\frac{C}{m^2} \quad \text{(Eq. 3.8)}$$

with *a(0)* and *a(x)* being lattice constants.

Table 3.1 – Spontaneous polarization, piezoelectric polarization, and dielectric constants of AlN and GaN [3.3]

wurtzite	AlN	GaN
P_{SP} [C/m^2]	−0.081	−0.029
	1.46	0.73
e_{33}	1.55	1
[C/m^2]		0.65
		0.44
e_{31}	−0.60	−0.49
[C/m^2]	−0.58	−0.36
		0.33
		−0.22
e_{15}	−0.48	−0.3
[C/m^2]		−0.33
		−0.22
ϵ_{11}	9.0	9.5
ϵ_{33}	10.7	10.4

Table 3.2 – Elastic constants of wurtzite and cubic AlN and GaN [3.3]

GPa	AlN	GaN
wurtzite		
c_{11}	396	367
c_{12}	137	135
c_{13}	108	103
c_{33}	373	405
c_{44}	116	95
B	207	202
zincblende		
c_{11}	304	293
c_{12}	160	159
c_{44}	193	155

The total polarization field in the AlGaN layer depends on the crystal orientation of the GaN. Metal-organic chemical vapor deposition can produce a GaN crystal orientation that makes the polarization-induced sheet charges add

constructively and thus the polarization field in the AlGaN layer will be greater than that of the buffer layer. A high sheet charge will thus be present in the AlGaN/GaN interface due to this polarization field discontinuity.

For a non-ideal surface, with available donor-like states, the crystal energy will increase along with the AlGaN layer thickness. Thus beyond a certain thickness, the energy of the states will reach the Fermi level and electrons will be able to drift from the occupied surface states toward the heterointerface to free conduction band states. This process creates the 2DEG and leaves a positive surface sheet charge. For an ideal surface with no surface states, occupied states are available only in the valence band and the 2DEG can exist if the AlGaN layer is thick enough for the valence band to reach the Fermi level at the surface. Electrons can thus transfer from the AlGaN valence band to the GaN conduction band, leaving surface holes, which result in a surface positive sheet charge. Thus, both cases require the presence of a positive surface sheet charge for the formation of a 2DEG. The 2DEG density of an AlGaN/GaN HEMT can be given by the following equation:

$$n_s = \frac{\sigma_{AlGaN}\ t_{AlGaN}\ - \frac{\varepsilon\varepsilon_0}{q}\Phi_B + \frac{\varepsilon\varepsilon_0}{q^2}(\Delta E_{c,AlGaN}\ )}{t_{AlGaN}\ + d_0} \qquad \text{(Eq. 3.9)}$$

where σ_{AlGaN} is the net polarization charge density of AlGaN, t_{AlGaN} is the thickness of the AlGaN layer, $\Delta E_{c,\ AlGaN}$ is the conduction band discontinuity, and d_o is the thickness of the GaN layer [3.2].

Surface states act as electron traps in the access regions between the metal contacts. As they are prevented through surface passivation from being neutralized by trapped electrons, they maintain a positive surface charge. Without

good passivation, the electric field arising from high power operation will cause the electrons to leak from the gate metal and get trapped. In this case, the reduction in surface charge will lead to a reduction in the 2DEG charge as well, reducing channel current. The amount of trapped electrons depends on the applied voltage and the extent to which the device is overdriven beyond the linear gain. As trapped electrons are modulated with low frequency stimulating voltages, they can contribute to the 2DEG channel current, but cannot follow the high frequency stimulating voltages and so in this case, would actually reduce the channel current. This current reduction for RF operation is known as surface trap induced current dispersion.

The effects of surface states and spontaneous and piezoelectric polarization are important for the understanding of AlGaN/GaN HEMTs. They imply that a 2DEG can be formed at the AlGaN/GaN interface even when there is no intentional doping of the AlGaN layer. Thus, the formation mechanism of the 2DEG at the heterointerface is different in an AlGaN/GaN HEMT than in an AlGaAs/GaAs HEMT and a 2DEG with high sheet carrier density can be achieved without any doping due to the strong polarization field across the AlGaN/GaN heterojunction with surface states acting as the source of electrons for the 2DEG.

3.4 GaN HEMTs

AlGaN/GaN HEMTs have attracted much attention due to their excellent breakdown characteristics and other unique properties. Both AlGaN and GaN have large breakdown fields over 3 MV/cm, significantly higher than those of

silicon or gallium arsenide. This characteristic is important as it allows for device operation at high voltages. AlGaN/GaN heterostructures have unique physical mechanisms that allow them to yield a 2DEG with a high sheet charge density around 10^{13} cm^{-2}, which is on the order of five times higher than conventional AlGaAs/GaAs structures [3.4]. This high sheet charge density allows for high DC and RF currents, leading to high RF output power. Along with high electron mobility, these characteristics lead AlGaN/GaN HEMTs to achieve a high breakdown voltage, high current density, and high channel operating temperature capabilities, as well as high operating frequency and high drain power added efficiency. A diagram demonstrating material properties and their corresponding benefits is shown in Figure 3.3.

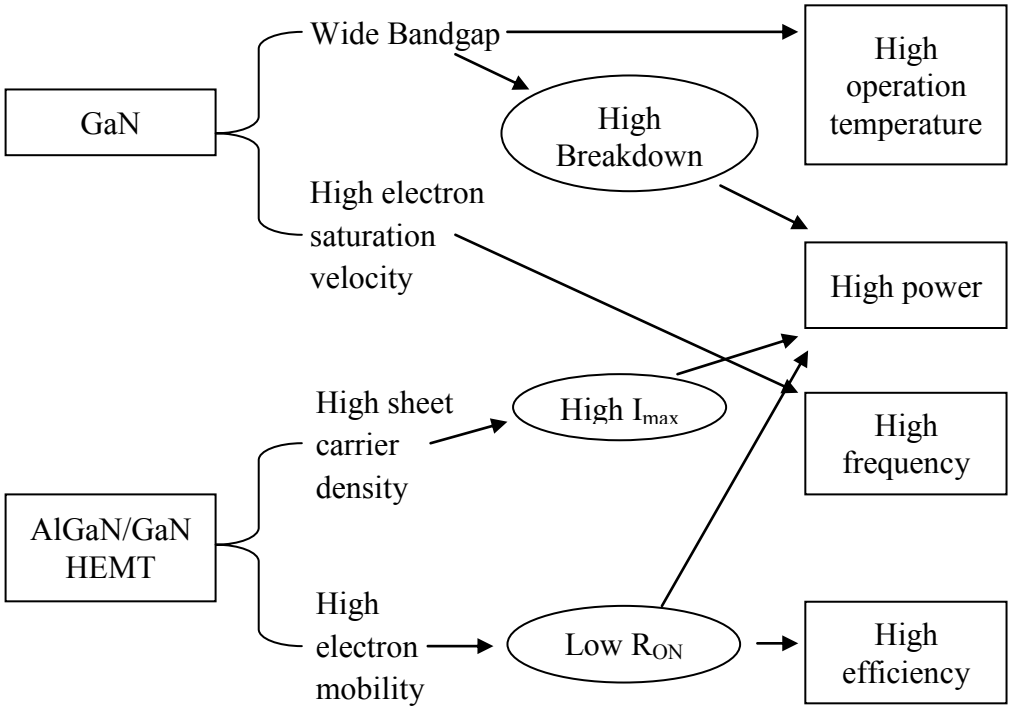


Fig. 3.3 – Electronic properties of an AlGaN/GaN HEMT [3.5]

The cross-sectional view for an AlGaN/GaN HEMT can be seen in Figure 3.4 along with the corresponding energy band diagram. Wide-bandgapped AlGaN lies on top of GaN, with a sharp dip in the conduction band occurring at the heterointerface. As mentioned, a 2DEG may be formed in the heterostructure even when it is undoped. The built-in static electric field in the AlGaN layer induced by spontaneous and piezoelectric polarization alters the band diagram and the electron distribution of the heterostructure. A considerable number of electrons thus transfer from the surface states to the heterointerface, resulting in a 2DEG with high density.

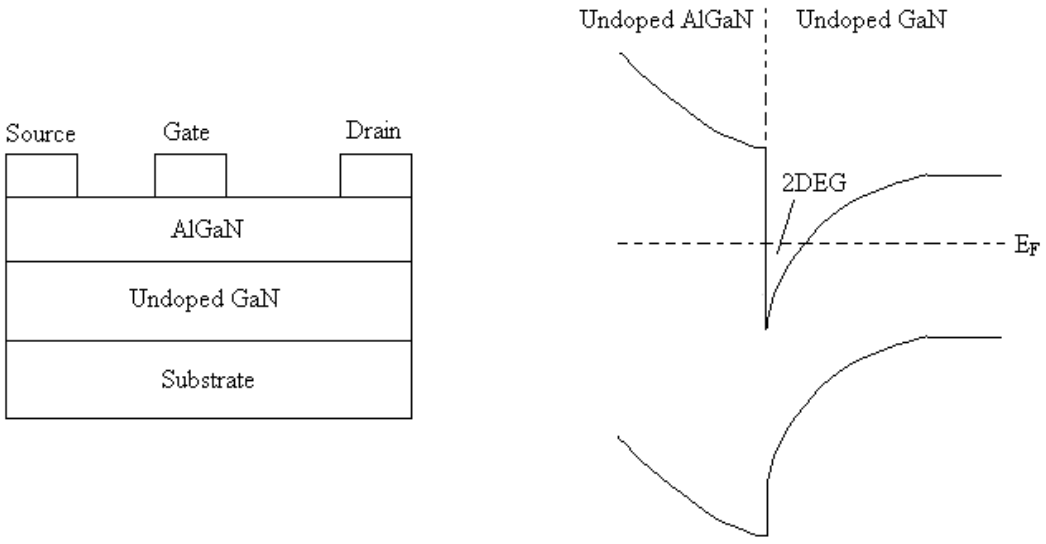


Fig. 3.4 – (a) Simplified AlGaN/GaN HEMT structure and (b) corresponding band diagram

A more detailed view of a typical AlGaN/GaN HEMT can be seen in Figure 3.5. Above the substrate lies the nucleation layer, which can be made of GaN, AlN, AlGaN, or graded AlGaN layers. Its purpose is to reduce the density of threading dislocations in the subsequent GaN buffer layer due to the large

lattice mismatch between GaN and the substrate. The buffer layer should be of high quality with few defects and a high resistivity to avoid charge trapping of 2DEG electrons and high buffer leakage. It should also be smooth so as to provide a good interface between itself and the following AlGaN barrier layer, resulting in high mobility and good confinement of the 2DEG electrons. The barrier layer supplies electrons for the 2DEG and is usually Si-doped. Increasing the Al concentration also increases the 2DEG density, though as the thickness of the layer increases, the 2DEG density increases less. A thin cap layer can follow the barrier layer and can reduce gate leakage and increase Schottky barrier height. Finally, Ohmic source and drain contacts and a Schottky gate contact top the structure.

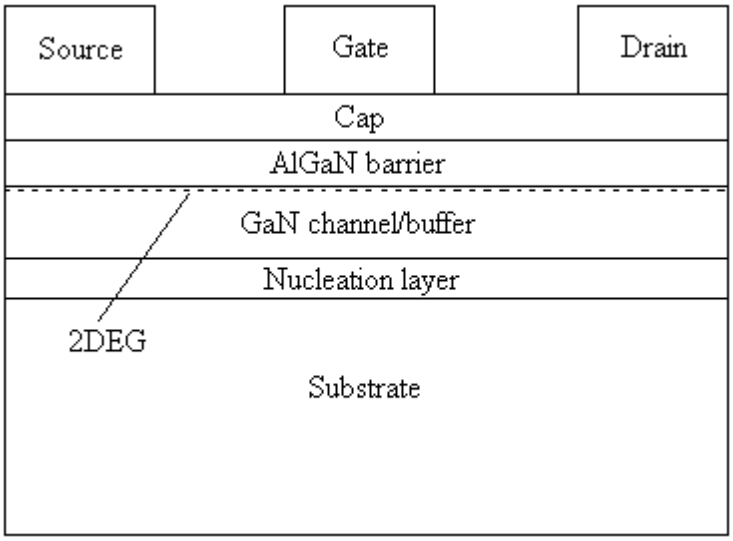


Fig. 3.5 – Cross-sectional view of an AlGaN/GaN HEMT

There are no GaN substrates large enough to grow GaN channels, and thus currently sapphire (Al_2O_3) and SiC are the most commonly used substrates.

Sapphire substrates can have a large area availability (6 inches) and can provide good quality, high temperatures stability, and good insulating and mechanical properties. However, while sapphire is cheaper than SiC, it has a low thermal conductivity (0.3W/cm·K) [3.6], which is a challenge for packaging high power devices, as well as a large lattice mismatch to GaN of about 16%, resulting in a high dislocation density [3.7]. SiC, on the other hand, has a relatively low lattice mismatch with GaN (3.3%) [3.7], though defects still occur. It also has a higher thermal conductivity, though it does suffer from lower quality and small area wafer availability (3 inches). Silicon is a third substrate alternative and its main attraction lies in its low cost, large area wafers (12 inches), and integration possibilities with silicon electronics, as well as its acceptable thermal conductivity, though it has an even higher lattice mismatch of 16.9% [3.8].

Several other issues remain with GaN HEMT development. One of these key issues concerns traps in the device, where electrons are excited and captured in the traps between the gate and drain. These trapped electrons cannot follow the AC signal as the de-trapping time constant is too long and so are unavailable for conduction in the on state for the transistor. Trapping effects include transconductance frequency dispersion, current collapse of the drain characteristics, light sensitivity, gate- and drain-lag transients, and restricted microwave power output [3.9]. Other issues include the high cost and reliability concerns for commercialization.

3.5 Applications

GaN-based HEMT structures have various material and device properties that make them attractive for a wide range of applications, especially in power and RF applications. A few key fields for GaN devices include broadband communications, radar components, automotive applications, and sensors, a few of which will be discussed in this section. The main characteristics for GaN-based devices that result in its excellent performance are high dielectric strength, high operating temperature, high current density, high-speed switching, and low on-resistance, useful for power supply circuits and RF circuits. This rugged and reliable technology is suitable for both commercial and military applications, a few of which are shown in Figure 3.6. Military applications include radar (shipboard, airborne, and ground) and high-performance space electronics, while commercial applications include base-station transmitters, C-band Satcom, Ku-K band small aperture terminal and broadband satellites, local multipoint distribution systems, and digital radio [3.10].

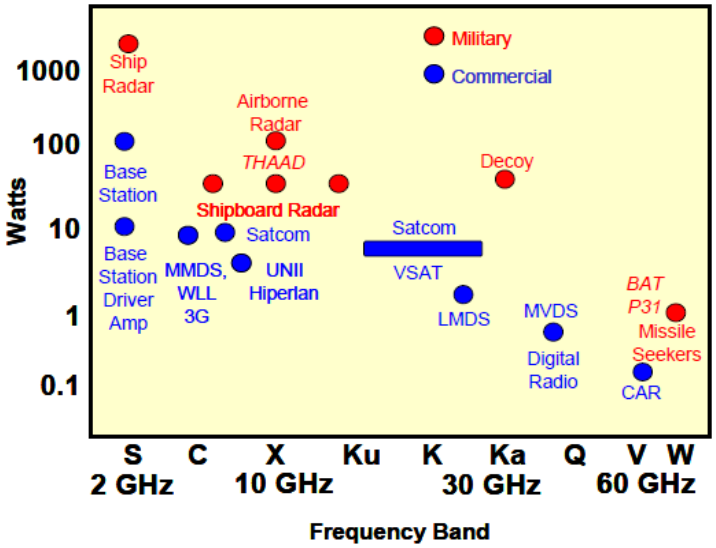


Fig. 3.6 – GaN applications [3.10] © 2012 IEEE

3.5.1 RF Applications:

Wireless mobile technology has matured in the past few decades, with fourth generation networks currently available and fifth generation systems emerging. Small-signal low-noise transistors are needed to amplify incoming signals in receiver front-ends and power transistors with low on-resistance high on-current are needed for transmitters. For these systems, a major limiting factor is microwave power amplifier performance, which affects power consumption, volume, and weight for both the subscriber and base station side. Efficiency is especially important, as a low efficiency will increase power consumption and thus the necessary cooling equipment complexity as well. While several power-amplifier technologies are available, such as silicon lateral-diffused metal-oxide-semiconductors and bipolar transistors, GaAs MESFETs, GaAs and GaAs/InGaP heterojunction bipolar transistors, and SiC MESFETs, GaN HEMTs far outclass these conventional technologies in terms of system performance [3.10]. GaN devices have high power per unit width, which results in smaller, high-impedance devices that are also easy to fabricate, making it easier to match them to the system. Furthermore, their high voltage capabilities reduce the need for voltage conversion. A list of power device requirements and GaN related features and advantages may be found in Table 3.3 with particularly significant benefits highlighted.

GaN-based amplifiers have been reported in a wide frequency range, from the S- [3.11], C-, and X-bands [3.12] up to the Ku- [3.13] and Ka-bands [3.14] and more. Small-signal low-noise applications include collision avoidance radar at 77 GHz and military radar at 94 GHz, while power applications include base

station applications at 40 GHz, mobile communication at 0.9/1.9 GHz, and switching power supplies at < 1 MHz [3.15]. Both Japanese and American manufacturers have had growing interest in high frequency radar applications (>10 GHz), while also working on improving bandwidth, power output, and efficiency. Companies such as Nitronex, M/A-COM, Sumitomo Electric Device Innovations, Toshiba, and Fujitsu are all production-qualified GaN suppliers, though Nitronex is the only supplier that uses a GaN-on-silicon manufacturing process while the others prefer SiC substrates. RF Micro Devices (RFMD) has been tailoring their GaN technology for radar systems and other applications such as military communications and cellular infrastructure and has several successful high-power GaN HEMT process technologies along with the world's largest III-V commercial wafer factory. Cree, Inc. is another major company deeply involved in GaN HEMT technology and has GaN HEMT devices designed for broadband amplifiers, L-, S-, C-, X-, and Ku-band radar applications, and various telecom and communications applications.

Table 3.3 – Competitive advantages of GaN devices [3.10] © 2012 IEEE

Need	Enabling Feature	Performance Advantage
High Power/Unit Width	Wide Bandgap, High Field	Compact, Ease of Matching
High Voltage Operation	High Breakdown Field	Eliminate/Reduce Step Down
High Linearity	HEMT Topology	Optimum Band Allocation
High Frequency	High Electron Velocity	Bandwidth, μ-Wave/mm-Wave
High Efficiency	High Operating Voltage	Power Saving, Reduced Cooling
Low Noise	High gain, high velocity	High dynamic range receivers
High Temperature Operation	Wide Bandgap	Rugged, Reliable, Reduced Cooling
Thermal Management	SiC Substrate	High power devices with reduced cooling needs
Technology Leverage	Direct Bandgap: Enabler for Lighting	Driving Force for Technology: Low Cost

3.5.2 Automotive Applications:

The development of hybrid vehicles, electric vehicles, and fuel cell hybrid vehicles is important as it provides a solution for the problems of growing fuel consumption and exhaust gas in urban areas. With their need for high electric power inverters used for driving high power motors, the current silicon devices are severely limited in their performance due to their material limits. Thus, devices based on materials with superior properties such as high operating temperatures and low on-resistances are required for the improvement of future vehicles. GaN power devices are used in automotive applications, especially in hybrid vehicles. With their high breakdown voltage and low on-resistance, AlGaN/GaN HEMT devices are quite suitable for such applications.

Figure 3.7 shows the vehicle power electronics while Figure 3.8 depicts the motor power and power source voltages of several of Toyota's electric and hybrid vehicles, with the dotted lines indicating current flow in the wiring harnesses. The battery voltage of a vehicle is raised to the power source level by a voltage booster (DC-DC converter) and supplied to the motor through the inverter. The DC-DC converter and the inverter control the high electric power over 10kW [3.16]. To suppress the high current flow over 200A, a high source voltage of 650V was recently introduced by Toyota for high power motors in their hybrid vehicle systems [3.16]. It can be seen that the trend is that newer power devices will require high breakdown voltages due to increasing motor power and for protection against surge voltage [3.16]. Middle and low power modules with power levels below 5kW have required breakdown voltage lower than 600V [3.16]. For these modules, high frequency operation is expected, which leads to small capacitors and reactors, resulting in compact designs and lower costs [3.16]. The main issue for high power modules is the high electric power loss, which requires a water cooling system. A low on-resistance and high operation temperature of over 200°C are also required of these power devices to simplify the cooling system of the inverter [3.16]. Normally-off, or enhancement mode operation is also required for a fail-safe point of view. Wide bandgap semiconductors such as GaN come through with fulfilling these requirements when silicon-based devices cannot. An example of an integrated one phase inverter built from AlGaN/GaN is shown in Figure 3.9.

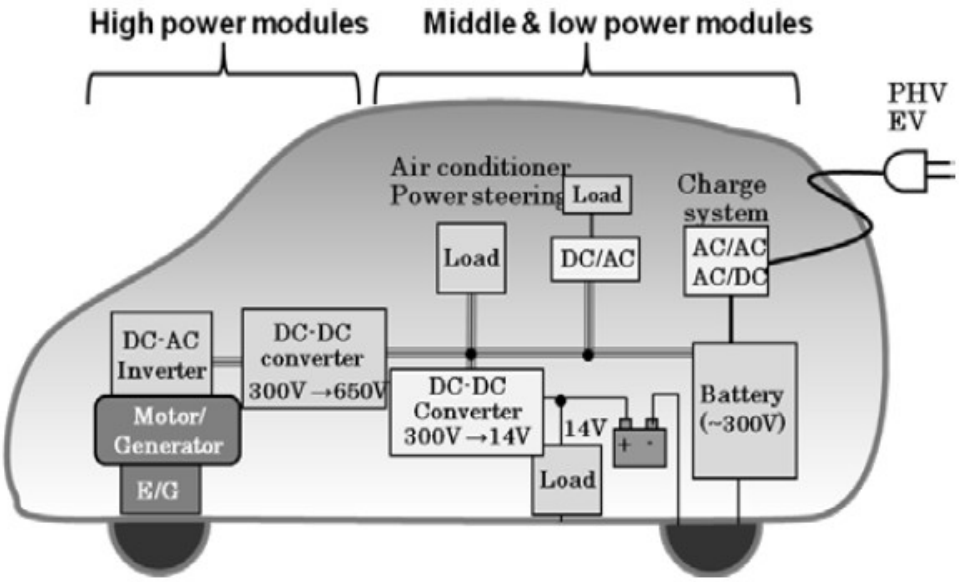


Fig. 3.7 – Power electronics in electric and hybrid vehicles [3.16] © 2002 IEEE

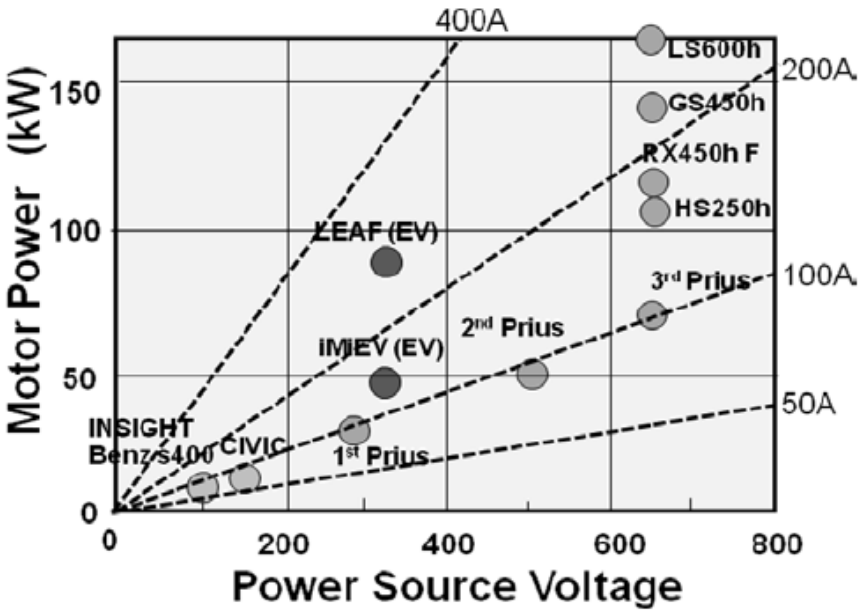


Fig. 3.8 – Motor power vs. power source voltage [3.16] © 2002 IEEE

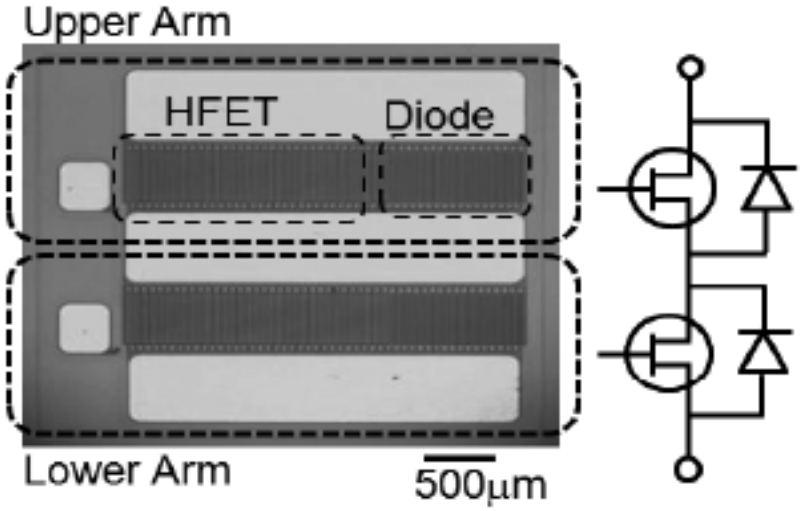


Fig. 3.9 – An integrated one phase inverter made of AlGaN/GaN on Si substrate [3.16] © 2002 IEEE

4 Growth and Fabrication

The GaN-AlGaN epitaxial layer structure that was used in the present work is shown in Figure 4.1. The epitaxial layers were grown by metal-organic chemical vapor deposition (MOCVD) on a monocrystalline silicon (111) wafer using an Aixtron G5 reactor. With the exception of the AlN layer, each layer was deposited at temperatures of over 900°C, with the total thickness of the layer stack being about 2.5µm. The 2DEG is created in the GaN layer immediately below the AlGaN barrier layer with an electron mobility of about 1800cm^2/V·s and a sheet resistance of 400Ω/square. On top of the structure, a 20µm layer of titanium (Ti) is used for its good adhesion between the semiconductor and the metal and a 150µm layer of gold (Au) is used as an Ohmic contact, due to its high electrical conductivity.

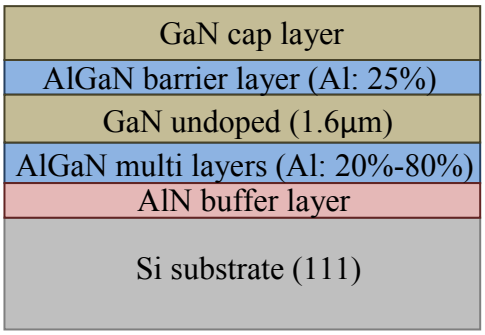


Fig. 4.1 – Cross-sectional view of wafer (not to scale)

4.1 Wafer Growth

Metal-organic chemical vapor deposition was used to grow AlGaN/GaN heterostructures on the silicon susbstrate. It is also known as organometal chemical vapor deposition (OMCVD), metal organic vapor phase epitaxy

(MOVPE) and OMVPE. It is a chemical vapor deposition method in which crystal growth occurs through a chemical reaction, where reactants from metal organic and hydride precursors in the gas phase are deposited. MOCVD grows new layers with the same crystal structure (i.e. lattice structure and crystal orientation) as the substrate below it, which allows for the growth of sequential epitaxial layers of varying material composition. This operation permits the growth of a wide variety of materials unlike other CVD techniques and is thus a very versatile method. The MOCVD procedure may be divided into the following steps, as described by Dapkus and Veuhoff [4.1, 4.2]:

1. Mass transport of the reactants/precursors in the reaction chamber to the substrate surface by a carrier gas
2. Surface reactions involving thermal decomposition of the reactants, i.e. separation of a compound into its elements via thermal energy, followed by adsorption/desorption, surface diffusion and nucleation
3. New layer growth, one two-dimensional monolayer at a time
4. By-product removal from the reaction chamber

Here, the first step, involving the transport of the group III element such as Ga to the substrate surface, is the growth-limiting step [4.1, 4.2]. Group V elements are more likely to desorb from the surface than group III elements and thus an excess of group V elements is required. It is also possible to include dopants in the carrier gas and incorporate them into the grown layer. The ability to select the reactants entering the reaction chamber with the carrier permits the

formation of abrupt heterojunctions by varying the gas composition. High flow rates are required in order to produce the required abruptness [4.2]. A schematic representation of the MOCVD process may be found in Figure 4.2.

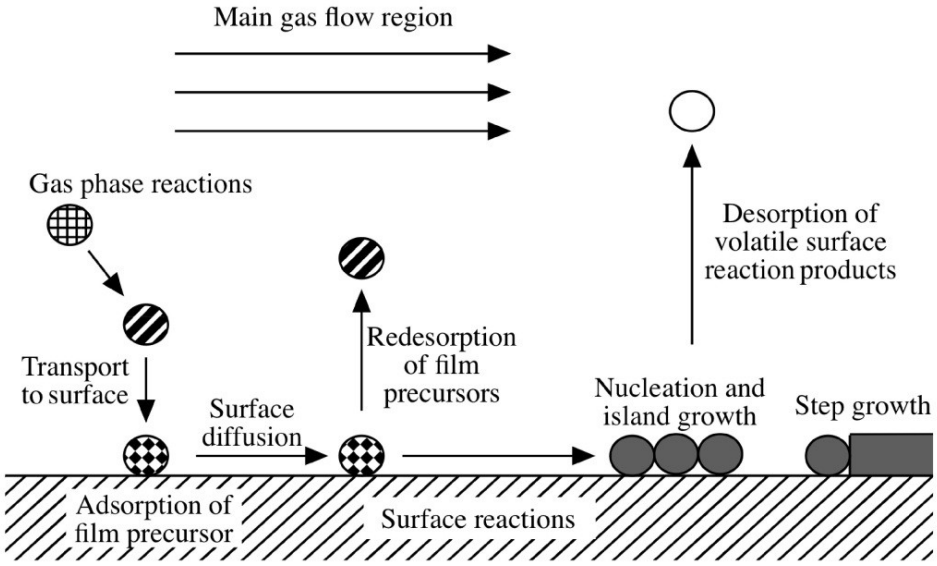


Fig. 4.2 – Schematic representation of the fundamental transport and reaction steps underlying MOCVD [4.3]

4.2 Mask Fabrication

Metal masks were used for the photolithography processes during HEMT fabrication. These metal masks, consisting of chromium on a glass plate, are used to transfer the desired pattern of the device design onto the sample by protecting specific areas covered by photoresist from ultraviolet light exposure.

The templates for the four masks to be used were designed using Microsoft PowerPoint, seen in Figure 4.3. The inked region of the template results in a clear window on the metal mask, while the white region represents the sections of the mask that would be covered in metal.

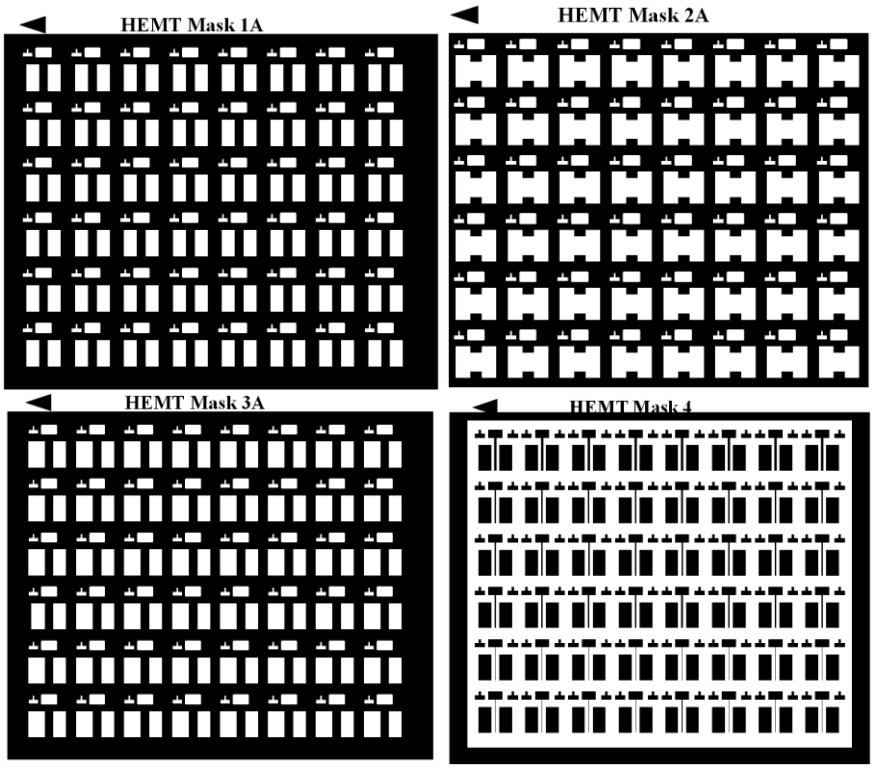


Fig. 4.3 – The four photomask templates used in device fabrication

The mask templates were printed out onto 8.5x11-inch transparencies and placed on a lit screen in a darkroom, seen in Figure 4.4. Light was shone through the designs, to be captured by a calibrated camera several meters away, shown in Figure. 4.5. A 3x3-inch glass plate covered in photosensitive material is placed within the camera to act as the initial shadow mask. The pattern is then created by exposing the photosensitive material to light and using a developer and fixer. Keeping this plate as the master copy, the pattern is transferred to a chromium coated plate through basic photolithography by spin coating the metal plate with photoresist, exposing it to ultraviolet light, developing it, and etching the chromium. This plate is to be used as the working mask.

The first mask is used to create the source and drain contact windows. The second mask is used to isolate the individual HEMT devices from each other.

Mask 3 is used to remove the unwanted metal and top GaN cap layer between the source and the drain. Finally, Mask 4 is used to deposit the gate metal between the source and the drain. In each mask design, there is a small T-shaped section for each device that is used for alignment purposes.

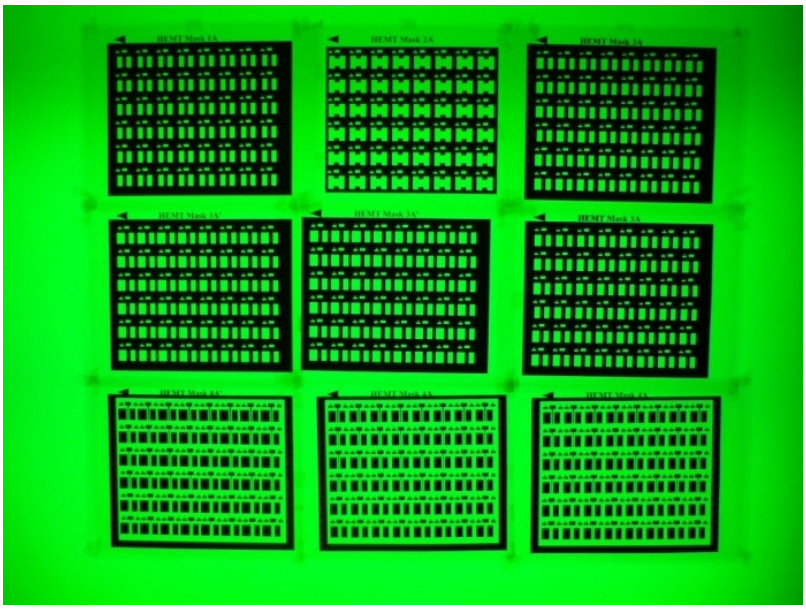
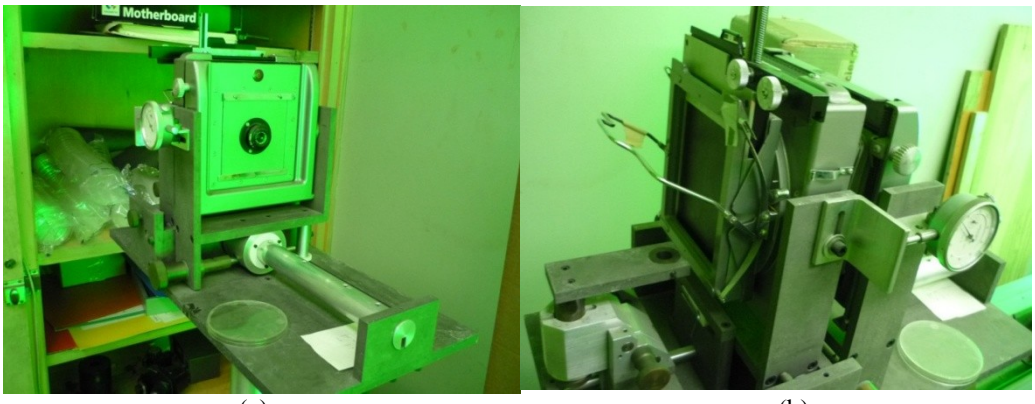


Fig. 4.4 – Printed mask templates, placed onto a lit screen in a darkroom



(a) (b)

Fig. 4.5 – (a) Front and (b) back sides of the camera used to capture light passing through the design templates

4.3 Device Fabrication

After cutting the wafer into appropriate dimensions using a diamond scriber, the HEMT devices may be fabricated. Details on device fabrication are found in Appendix A, along with process photos from individual procedure steps. A view of several unprocessed samples may be seen in Figure 4.6.

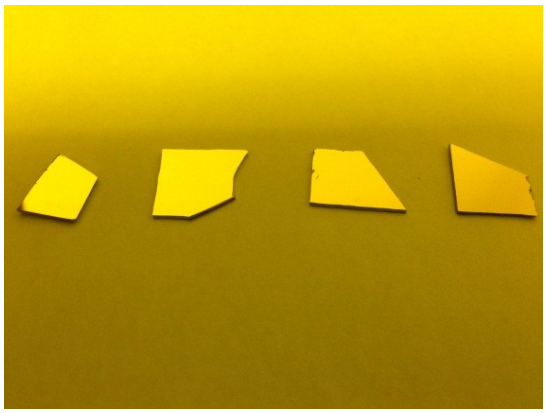


Fig. 4.6 – Unprocessed samples

The windows for the drain and source contacts are patterned using Mask 1 (Figure 4.3). Photoresist is deposited and the wafer is spun using a Laurell Technologies Corporation WS-400B-6NPP/LITE spinner. The wafer is then exposed to ultraviolet light and developed. The light source used for the exposure is an Oriel Corporation 68810 arc lamp power supply (200-500 Watt Hg source), seen in Figure 4.7.

The top layers of gold and titanium can be etched using an iodine solution and buffered hydrofluoric acid (BHF), respectively. Titanium deposition through vacuum evaporation (setup shown in Figure 4.8) ensues to create drain and source contacts. This process involves the evaporation of a titanium wire wound tightly around a tungsten heater mounted inside a vacuum chamber.

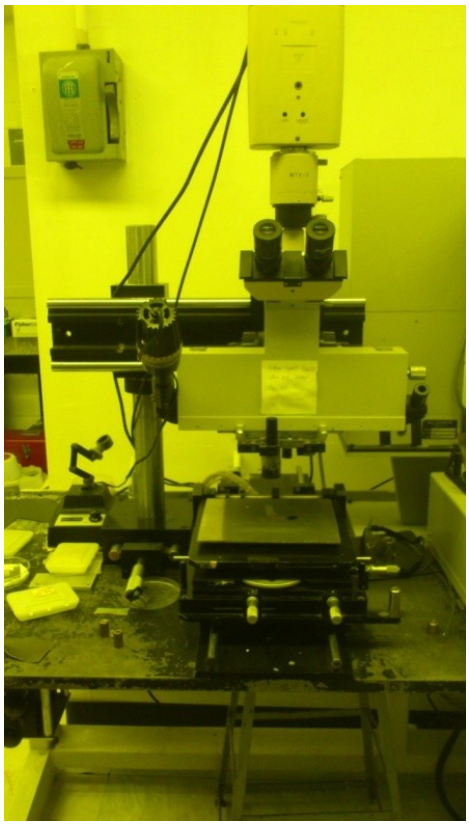


Fig. 4.7 – Light source for UV light exposure

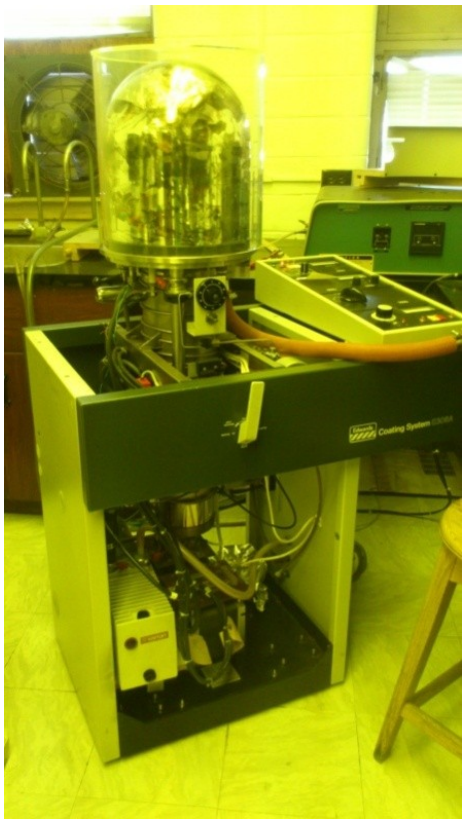


Fig. 4.8 – Vacuum evaporation setup

Photolithography is used again with Mask 2 (see Figure 4.3), whose pattern covers the entire device in order to prepare for the reactive ion etching step through device isolation. The exposed titanium is again etched using BHF. Reactive ion etching (RIE) removes the uncovered *n*-doped GaN and AlGaN layers in addition to part of the intrinsic GaN layer from the original wafer. This etching serves to isolate and prevent electron flow between devices. RIE involves applying a strong radio frequency electromagnetic field to the wafer platter, which ionizes the gas molecules, stripping them of electrons and creating a chemically reactive plasma. Under the effect of the electromagnetic field, the electrons strike the wafer platter, causing a build-up of positive charges on the platter due to its DC isolation. Meanwhile, the plasma develops a negative charge due to the higher

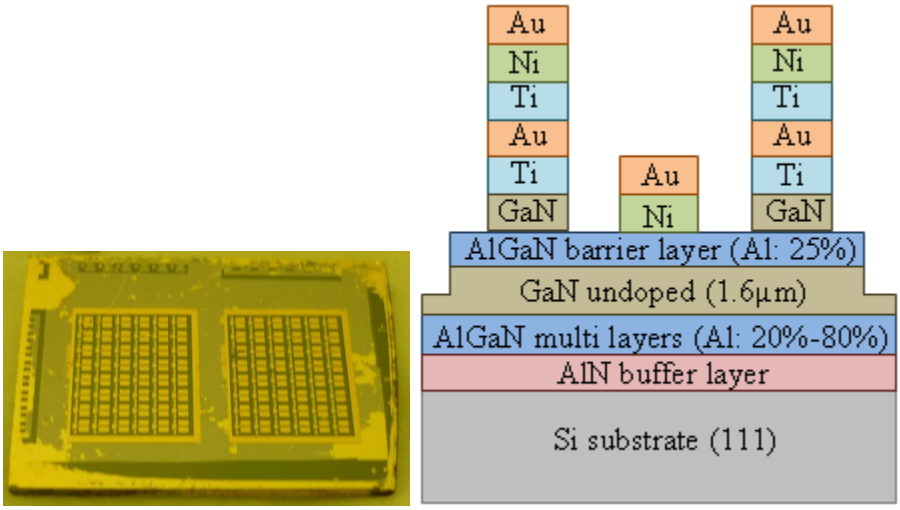
concentration of negative ions compared to the free electrons in the chamber. As a result of the voltage difference, the negative ions drift toward the wafer platter and collide with the sample, reacting with the material though also potentially knocking off some of the material. RIE is an anisotropic process due to the largely vertical delivery of reactive ions and thus photoresist can be used as a protective layer for the devices. This photoresist is later removed by immersing the samples in acetone.

Mask 3 (see Figure 4.3) is the same as Mask 1 and serves to expose the titanium at the gate, which is etched using BHF. To prevent an unwanted flow of electrons under the gate and between the source and drain in the *n*-GaN layer, this layer is etched using a 0.3M KOH + 0.1M $K_2S_2O_8$ solution exposed under a Dymax ultraviolet light source.

In order to obtain a precise gate site and simpler metal removal after the gate metal deposition, an initial photoresist layer was deposited before the deposition of a layer of aluminum, to be used as a protection layer. A second photoresist layer is then deposited and Mask 4 (see Figure 4.3) is used to pattern the final set of contacts, covering everything but the source, drain, and gate. After developing the sample and exposing the aluminum at the source, drain, and gate areas, the aluminum was etched away with an aluminum etchant. The remaining photoresist was removed using acetone, exposing the gate to prepare for the gate metal deposition step.

A variety of contact combinations were used for the gate metal contact, namely titanium/gold (Ti/Au), nickel/gold (Ni/Au), platinum/gold (Pt/Au), and chromium/gold (Cr/Au). The work functions for titanium, nickel, platinum, and

chromium are 4.3 Φ/eV, 5.2 Φ/eV, 5.6 Φ/eV, and 4.5 Φ/eV, respectively [4.4]. Two samples were also fabricated without the layer of titanium for the drain and source contacts. A completed sample with Ni/Au as its gate contact along with the cross-sectional view of one device can be seen in Figure 4.9. The top view of one device may be seen in Figure 4.10.



(a) (b)

Fig. 4.9 – (a) A completed sample and (b) the cross-sectional view of a HEMT device

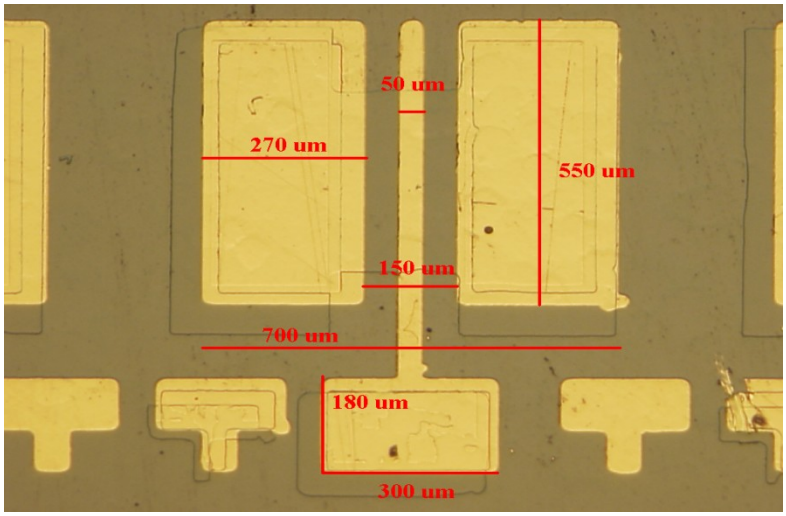


Fig. 4.10 – Top view of a HEMT device

5 Electrical Measurements

Several measurements were performed on the fabricated HEMTs in order to test their functionality and characterize their performance. The current-voltage (I-V), breakdown voltage, and capacitance-voltage (C-V) characteristics were measured and these testing procedures are described in the following two sections. The sample was placed on a grounded metal stage with conducting probes connected to the source, drain, and gate contacts. Testing was performed in ambient air, at room temperature and the setup can be seen in Figure 5.1. Measurements were performed on all samples fabricated in the lab, as well as on another sample fabricated by the National Research Council (NRC), which was used for comparison. NRC GaN HEMT devices are processed on 3-inch diameter epitaxial layers grown on insulating silicon carbide wafers. Further specifications concerning the processing of these devices may be found in [5.1]. The sample fabricated by NRC may be seen in Figure 5.2.

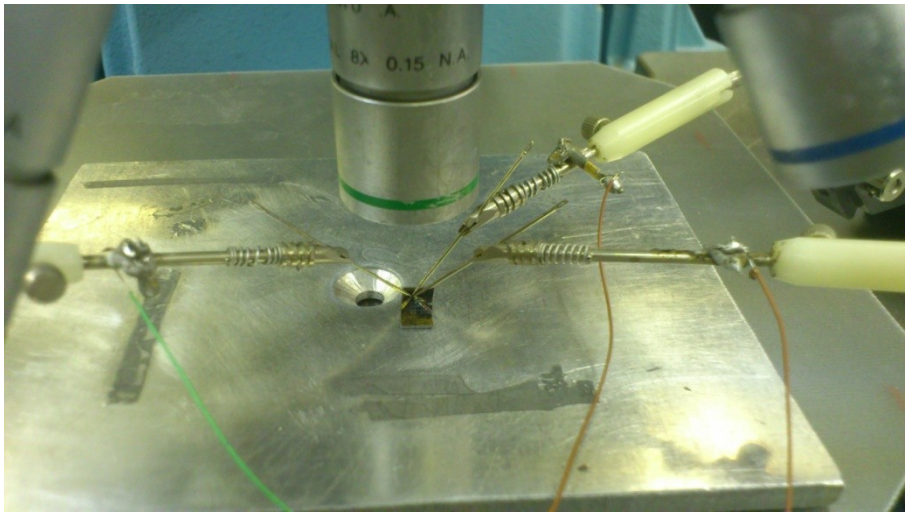


Fig. 5.1 – Experimental test setup

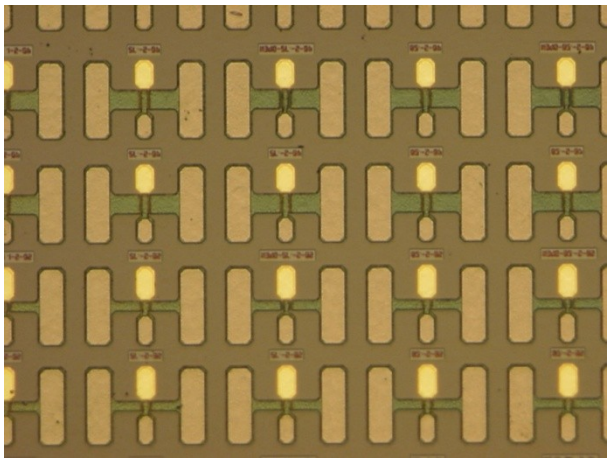


Fig. 5.2 – NRC-fabricated HEMTs

5.1 I-V Measurement Methods

For current-voltage (I-V) measurements, the experimental setup can be seen in Figure 5.3. The source, drain, and gate contacts were connected to a Hewlett-Packard (HP) 4145A semiconductor parameter analyzer through an HP 16058A test fixture. Voltage sweeps were performed as the current from the power source was extracted and measured via a LabVIEW virtual instrument. A screenshot of the virtual instrument may be seen in Figure 5.4. The I-V curves were produced while keeping the source grounded as the bias was applied across the other two device terminals. Maintaining a fixed voltage across one terminal, the bias for the remaining terminal is varied linearly between the two end values (e.g. 0-10V), with the current compliance set to 100mA to prevent accidental burning of the HEMT devices. The current is then extracted and plotted against the voltage. During measurements, the microscope light source is turned off and the lid of the test fixture box is closed in order to minimize noise generation.

Fig. 5.3 – Experimental test setup for measuring I-V characteristics (HP 4145A semiconductor parameter analyzer is shown at the bottom right)

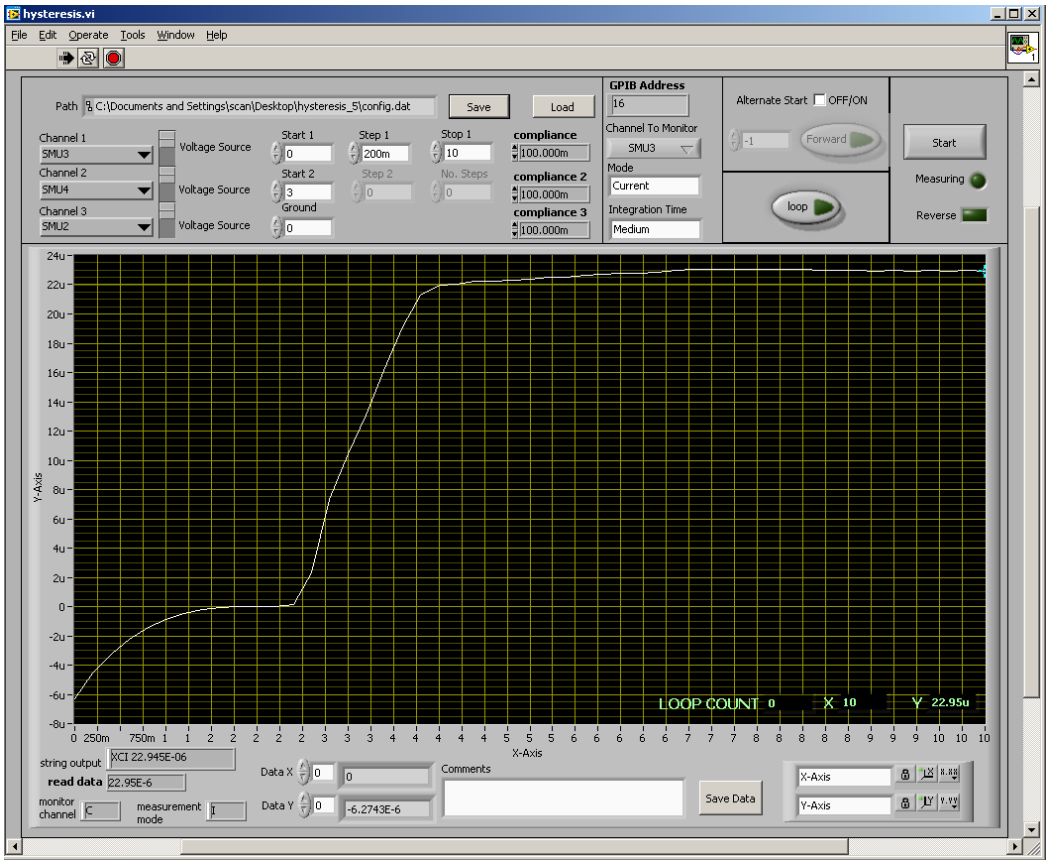


Fig. 5.4 – LabVIEW virtual instrument used to acquire electrical measurement data

The drain voltage was swept from 0V to 10V in increments of 0.2V while measuring the drain current and fixing the gate voltage (the source was kept grounded). Another set of measurements was performed, tracking the drain current with respect to a varying gate voltage for a fixed drain bias while again maintaining a grounded source.

After an initial set of measurements, the samples were annealed at 400°C, 450°C, 500°C, and 550°C for two minutes in a nitrogen environment and measurements were repeated after each annealing.

5.2 C-V Measurement Methods

Capacitance-voltage (C-V) measurements were also performed on the HEMT devices to characterize their performance. The device to be measured was connected to an HP 4274A multi-frequency LCR meter, which can be seen in Figure 5.5. The measurement frequency was set to 100 kHz with a magnitude of 100mV. The applied voltage was set by an HP 16023B bias controller (measured through an HP 3478A multimeter).

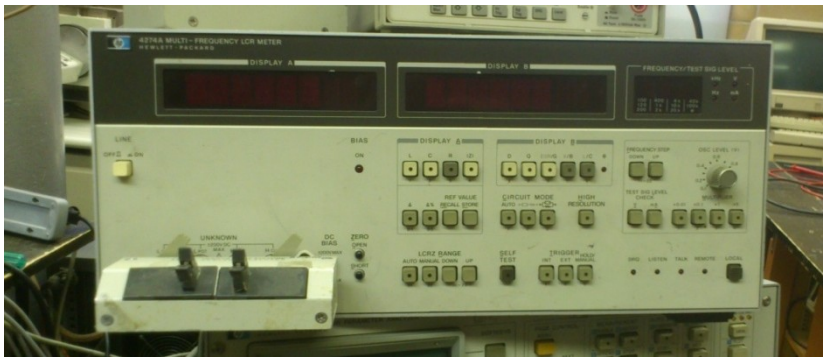


Fig. 5.5 – HP 4274A multi-frequency LCR meter

The HEMT device area is quite small and thus the capacitance is small as well. To overcome the problem of unwanted parasitic capacitance from the connecting wires and probes, the measurements were taken in a systematic fashion: the reading for capacitance was taken while the probes were not connected to the sample and taken again after connecting them. The difference between these two capacitance values was taken to be the capacitance of the sample. Resistance measurements, such as the drain-source series resistance, were also taken in this fashion at the same time, using the resistance measurement setting instead of the capacitance measurement setting.

5.3 Breakdown Voltage Measurement Methods

In addition to low voltage I-V characteristics, the breakdown voltage performance of the devices was also examined. As the semiconductor parameter analyzer can only provide a limited voltage supply of up to 100V, an HP 712C power supply with capability of up to 600V (V_1) was used. This source as used to set the bias for the drain and source. A Farnell L30BT stabilized power supply was used to set the gate bias, V_2. The voltage drop across a small resistor R_s in series with the HEMT device was measured using the HP 3478A multimeter in order to calculate the drain current of the transistor. Furthermore, a voltage divider consisting of two resistors, R_1 and R_2, was used in parallel with the HEMT. This scheme provided the means of accurately measuring the voltage administered by the power supply, due to the measurement limitations of the voltmeter. The testing circuit used is shown in Figure 5.6. All components were connected with wires and resistors that were soldered by hand.

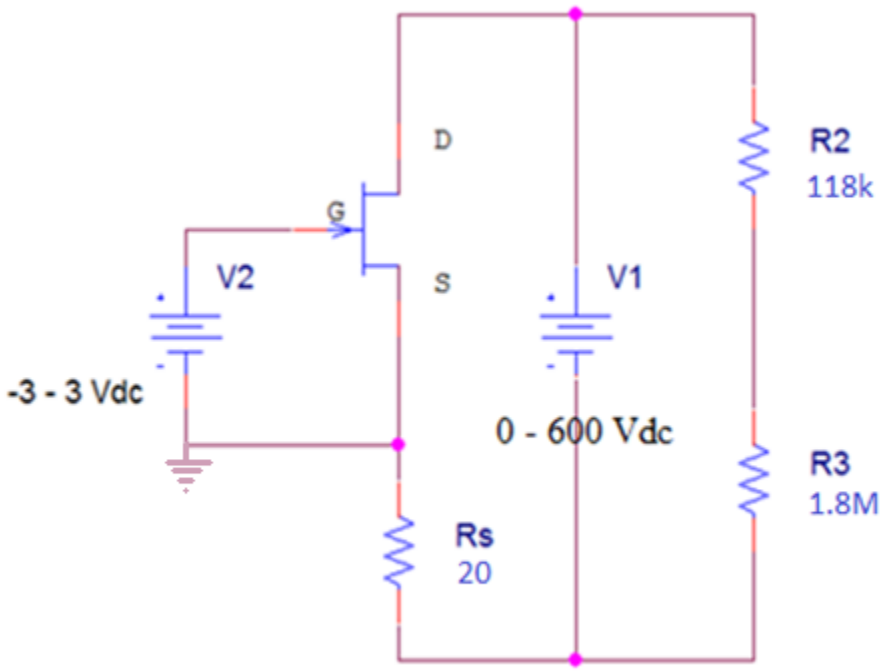


Fig. 5.6 – Breakdown voltage test Setup

The high voltage I-V characteristics and breakdown voltage for various devices was tested for by grounding the source, fixing the gate voltage (at -3V, -1V, 0V, 1V, and 3V), and varying the drain voltage. The breakdown voltage is when there is a sudden increase in the current. The drain voltage was gradually increased from 0V while measuring the voltage drop across R_s and simultaneously calculating the drain current and thus the breakdown voltage was inferred when a sudden increase in current was noted.

6 Results and Discussion

The current-voltage (I-V) and capacitance-voltage (C-V) measurements for the fabricated HEMTs are presented in this section. Hundreds of devices were made after going through multiple iterations of the fabrication procedure. Several devices from samples with different contact combinations that best represent the general behavior trends are presented here, with their specific behaviors outlined. The samples are named Sample A (Ti/Au contacts without titanium for the drain and source), Sample B (Ni/Au contacts without titanium for the drain and source), Sample C (Ni/Au contacts with titanium for the drain and source), Sample D (Pt/Au contacts with titanium for the drain and source), and Sample E (Cr/Au contacts with titanium for the drain and source). These samples are identical in their structures with the exception of their contact materials.

Samples A, B, C, D, and E display similar characteristics to those of traditional MOS devices. In Figure 6.1, the drain current vs. drain-source voltage (I_D vs. V_{DS}) characteristics at different gate biases for Device 1 from Sample A are shown. The device exhibited a maximum saturation current density on the order of 4mA/mm. This saturation current density is two to three orders of magnitude less than that of typical HEMTs, which can be attributed to the large gate to drain length (L_{gd}), which is about 50μm. This value is at least twice as large as similar devices reported. A larger L_{gd} contributes to larger parasitic resistance and an unwanted series resistance, measured to be on the order of 1-10kΩ.

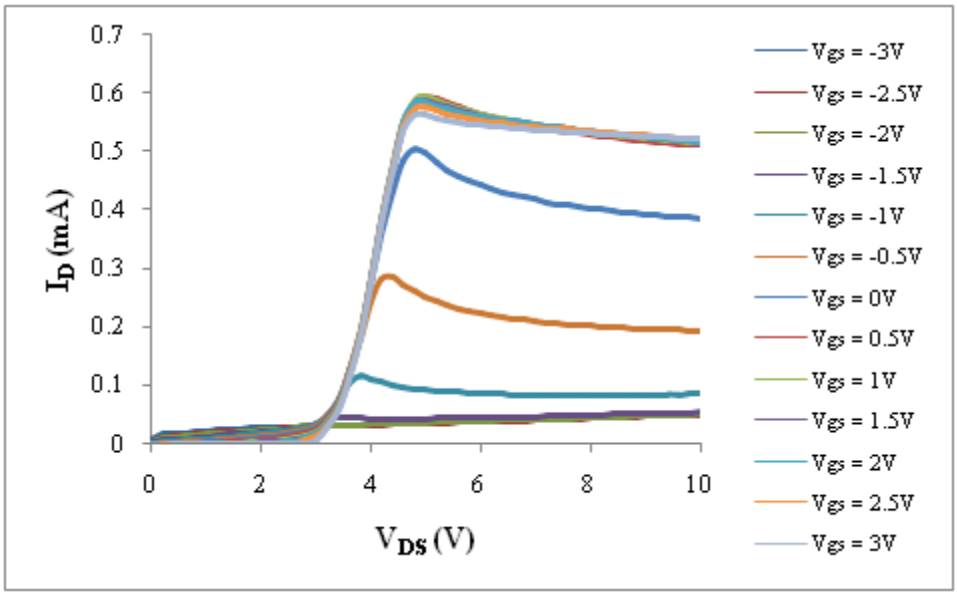


Figure 6.1 – I_D-V_{DS} characteristics for Device 1

There is some evidence of bad pinch-off characteristics seen in the graph. These characteristics are likely a result of a leakage current generated through the buffer, due to the background electron concentration in the buffer from native shallow donors. This effect could be compensated for through the addition of deep acceptors in the buffer layer. An improvement in the I-V characteristics was seen after annealing. The bad pinch-off effects were also shown to be improved. An example is shown in Figure 6.2, where the device was annealed at 550°C. The progression of the changes in I-V characteristics after annealing at different temperatures may be seen in Figure 6.3. After the first annealing step at 350°C, there is a sharp drop in saturation current. There is then a small increase in current after 400°C and another drop after 450°C. The current steadily rises for each subseuqent annealing step due to the decrease in resistance of the Ohmic contacts.

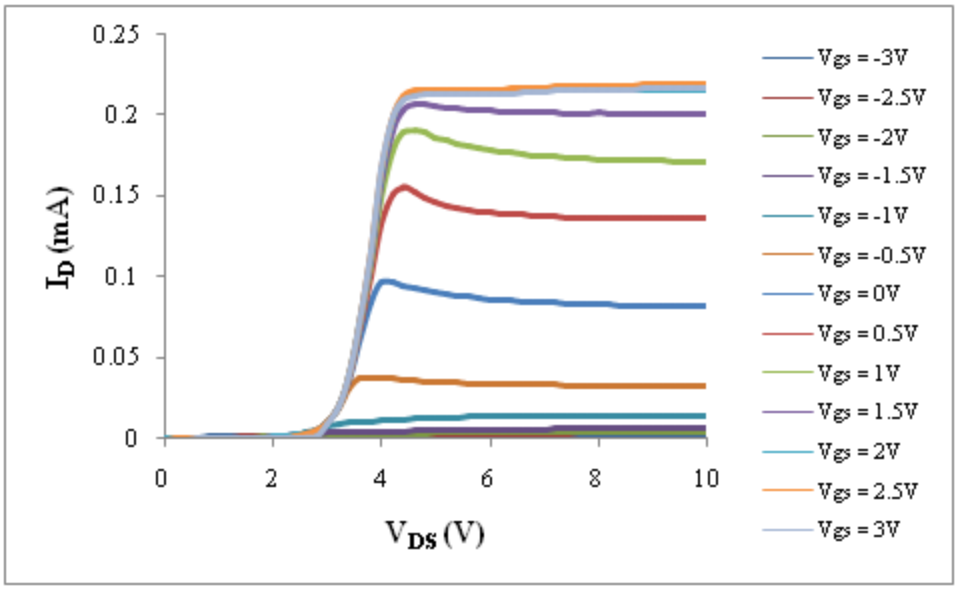


Figure 6.2 – I_D-V_{DS} characteristics for Device 1 after annealing at 550°C

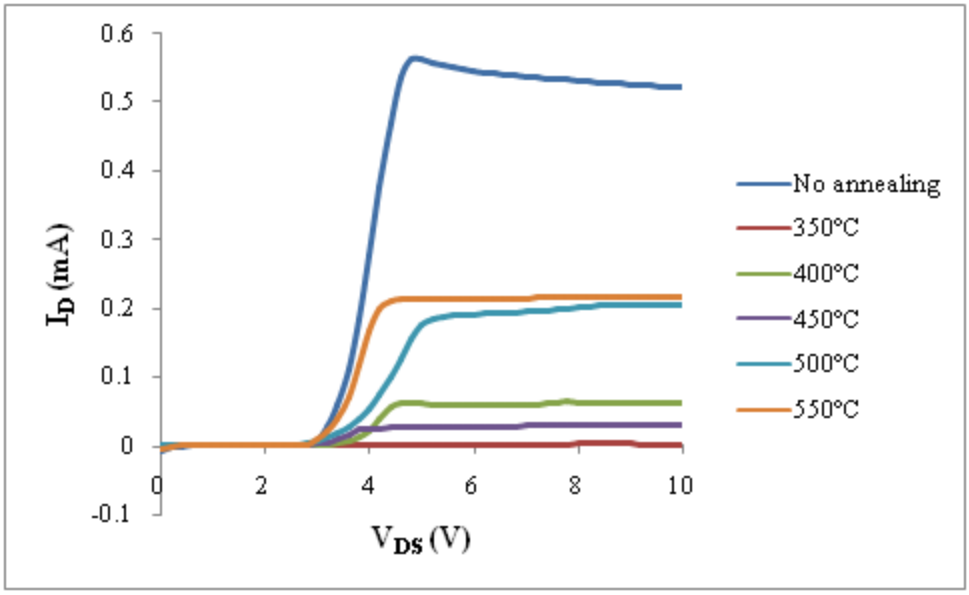


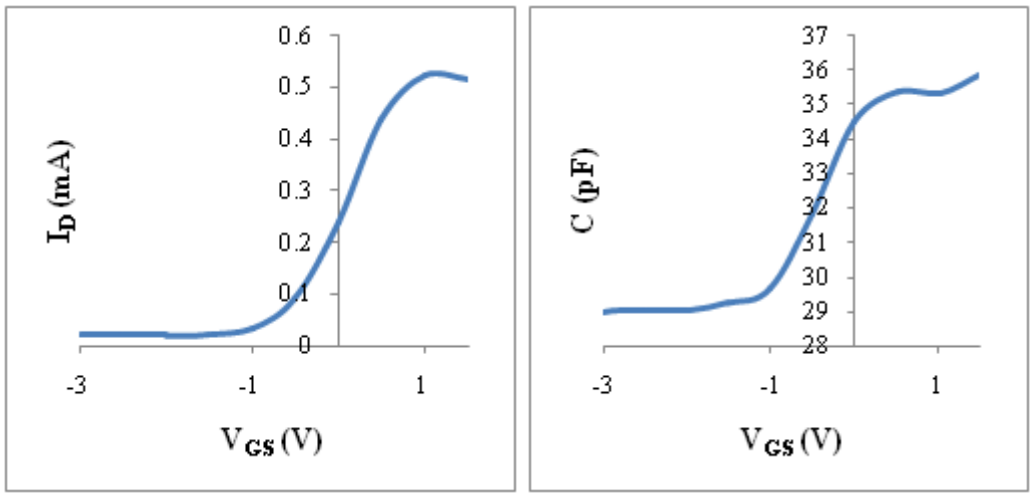
Figure 6.3 – Progression of I_D-V_{DS} characteristics (V_{GS} = 3V) for Device 1 after each annealing step

The drain-source current vs. gate-source voltage (I_D vs. V_{GS}) characteristics were also measured along with the gate capacitance-voltage (C-V) characteristics, as seen in Figure 6.4. The I_D-V_{GS} and C-V curves for other devices displayed similar characteristics. Parameters such as transconductance and

threshold voltage can be obtained from the I_D-V_{GS} curve. The transconductance curve, g_m, can be plotted using a centered difference equation:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{I_D(V_{GS}+\Delta V_{GS}) - I_D(V_{GS}-\Delta V_{GS})}{2\Delta V_{GS}}. \quad \text{(Eq. 6.1)}$$

Using the I_{DS}-V_{GS} plot found below as an example, the resulting g_m curve for Sample A is found in Figure 6.5. The transconductance was measured to be about 2.3mS/mm. This low transconductance is an attribute of the low saturation current. A sudden increase in capacitance is noted at the same point where a sudden increase in drain current is observed, confirming the voltage at which the transistor turns on. The threshold voltage V_t, which is a measure of when the device will begin conducting, can thus be deduced, and is approximated to be about -1V. This negative threshold voltage implies that the device is inherently on at zero gate bias. Techniques such as recessed gates and aluminum oxide passivation can be employed to obtain a positive threshold voltage, which would lead to less wasted power during idle times.



(a) (b)

Figure 6.4 – (a) I_D-V_{GS} and (b) C-V characteristics for Device 1

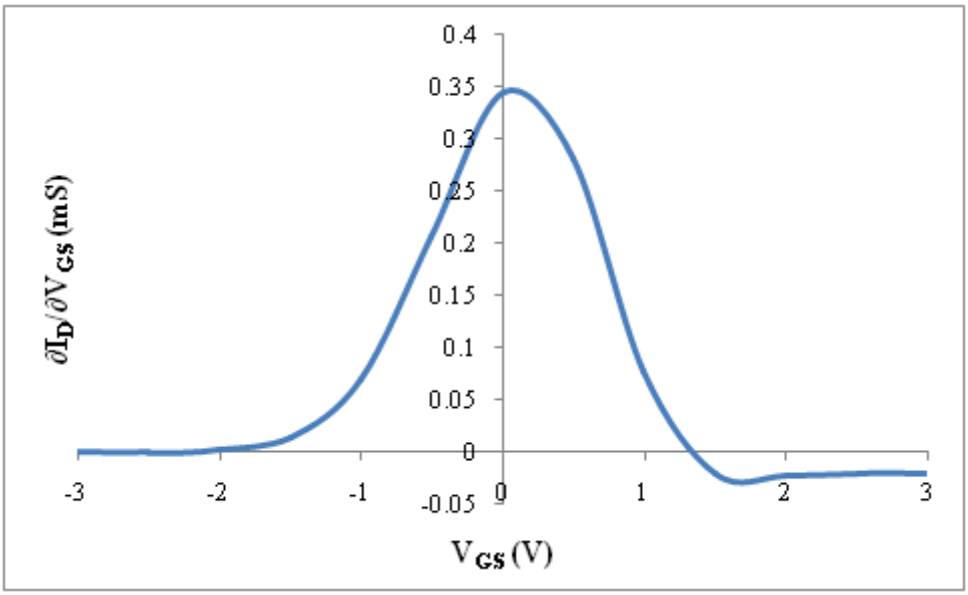


Figure 6.5 – Derivative curve of I_D with respect to V_{GS} for Device 1

It should also be noted that this and most other devices experienced a delay in current increase, where the current did not increase until a relatively high drain voltage is reached (~1.8-2.4V). This behavior is a result of the non-ideal nature of the drain and source contacts. The drain and source contacts should be Ohmic, but in this case, display unintentional Schottky characteristics. A reason for this phenomenon could be that the doping concentration in the GaN cap layer is not high enough to create a proper Ohmic contact region.

The I-V characteristics for Device 2 from Sample B were also measured. This device has poor current saturation, seen in Figure 6.6, due to channel length modulation, which increases output conductance. These effects are seen to be improved upon annealing, as seen in Figures 6.7, similar to the results of Device 1. There is, however, a slight kink effect that developed after annealing, seen in curves with a positive applied V_{GS} bias, representative of the effects of buffer traps, which are deep levels in the buffer layer. These effects are caused by hot

electrons being injected into buffer traps under a high applied drain bias and depleting the 2DEG, reducing the drain current. The kink effect is due to impact ionization and/or trapping/detrapping in buffer traps.

Regarding the summary of the annealing results seen in Figure 6.8, as with Device 1, there is a drop in saturation current after 350°C. There is another drop at 400°C, after which the current rises with each annealing process. Similar techniques to those mentioned previously were employed to calculate the transconductance and threshold voltage for this device, which were found to be 1.3mS/mm and -1V, respectively.

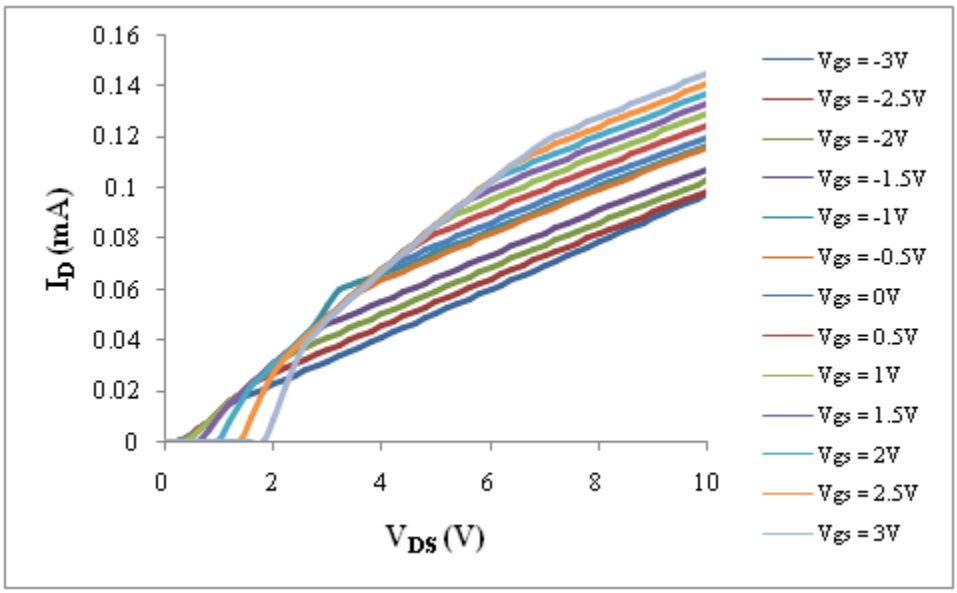


Figure 6.6 – I_D-V_{DS} characteristics for Device 2

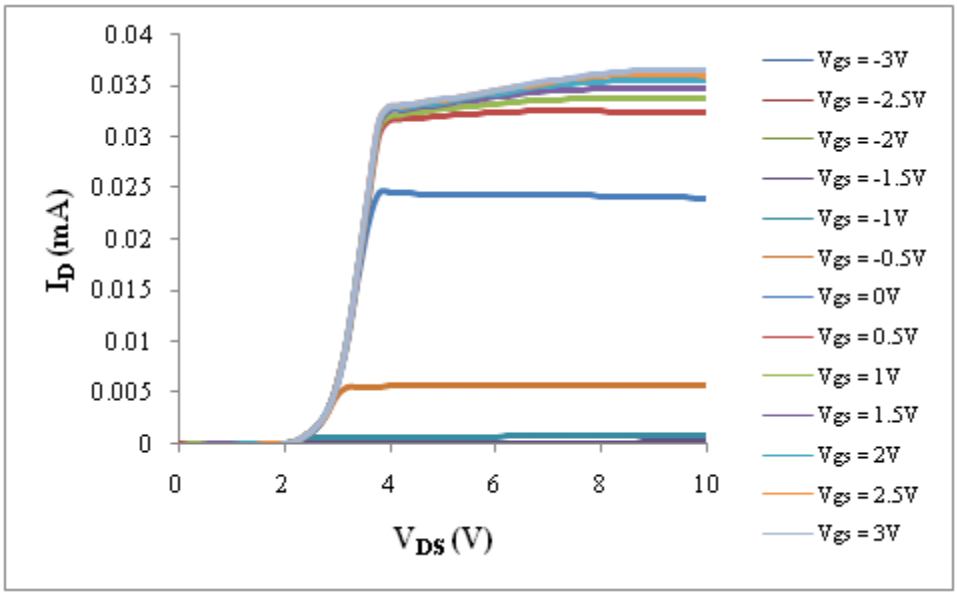


Figure 6.7 – I_D-V_{DS} characteristics for Device 2 after annealing at 550°C

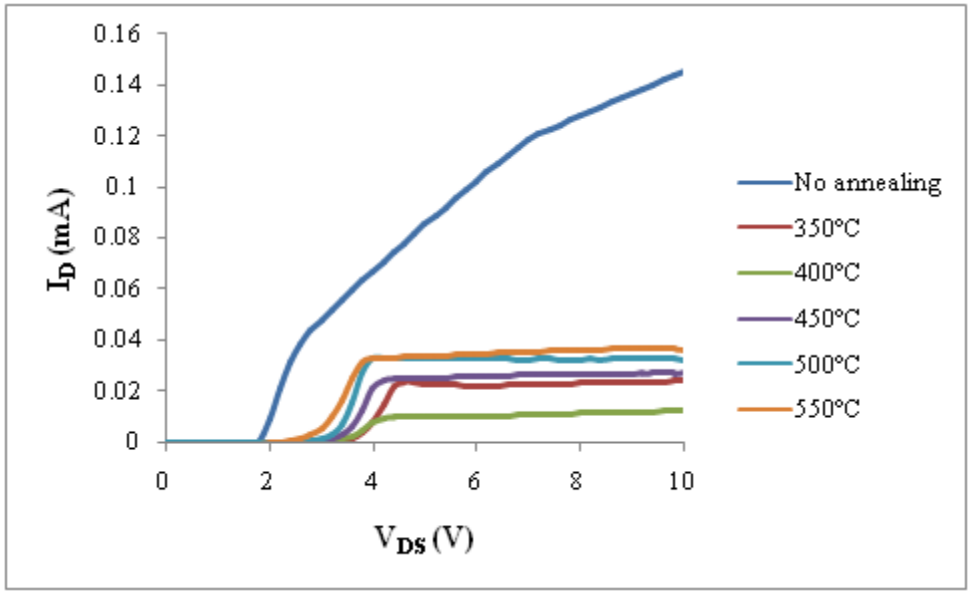


Figure 6.8 – Progression of I_D-V_{DS} characteristics (V_{GS} = 3V) for Device 2 after each annealing step

Device 3 from Sample C exhibited similar characteristics to Device 2 before annealing, where the current did not really saturate, seen in Figure. 6.9. Contrary to Device 2, however, even after annealing at various temperatures, the

current still did not saturate, seen in Figure 6.10. The annealing results summary is shown in Figure 6.11.

Unlike the previous samples, after the first annealing step, there is an increase in saturation current, followed by gradual decreases. It can also be seen that there is a distinct progression in current saturation after the first annealing step. The transconductance and threshold voltage for this device were found to be 0.3mS/mm and -2V, respectively.

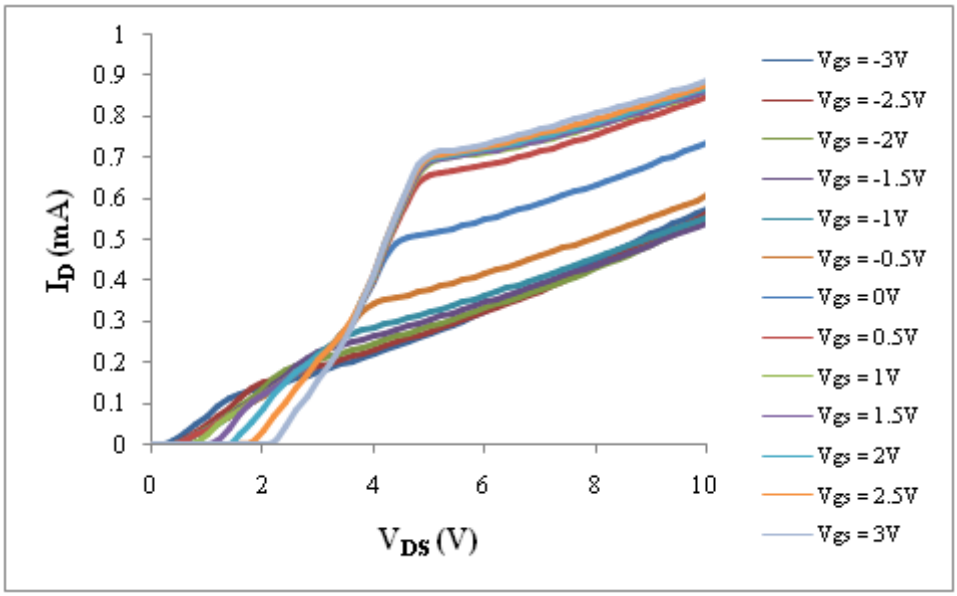


Figure 6.9 – I_D-V_{DS} characteristics for Device 3

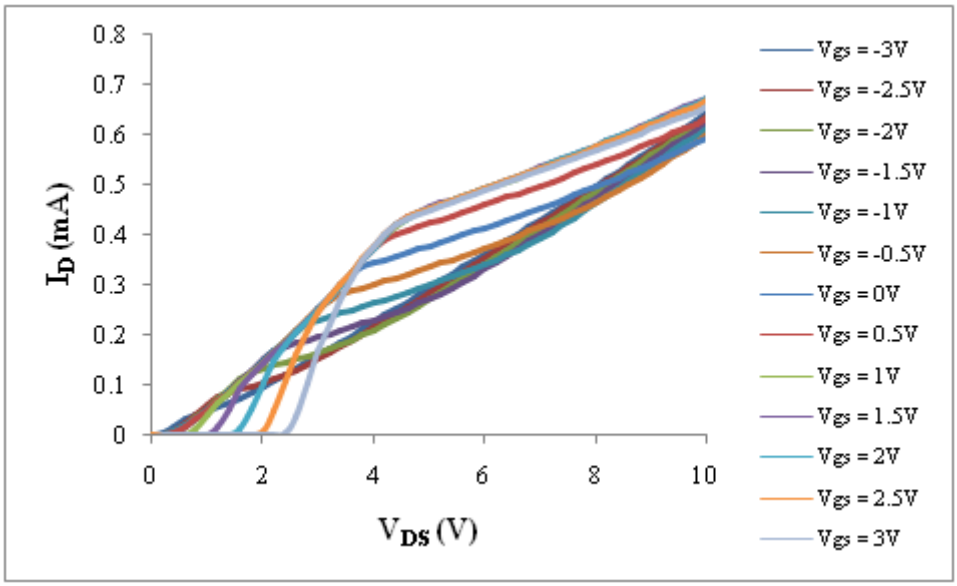


Figure 6.10 – I_D-V_{DS} characteristics for Device 3 after annealing at 550°C

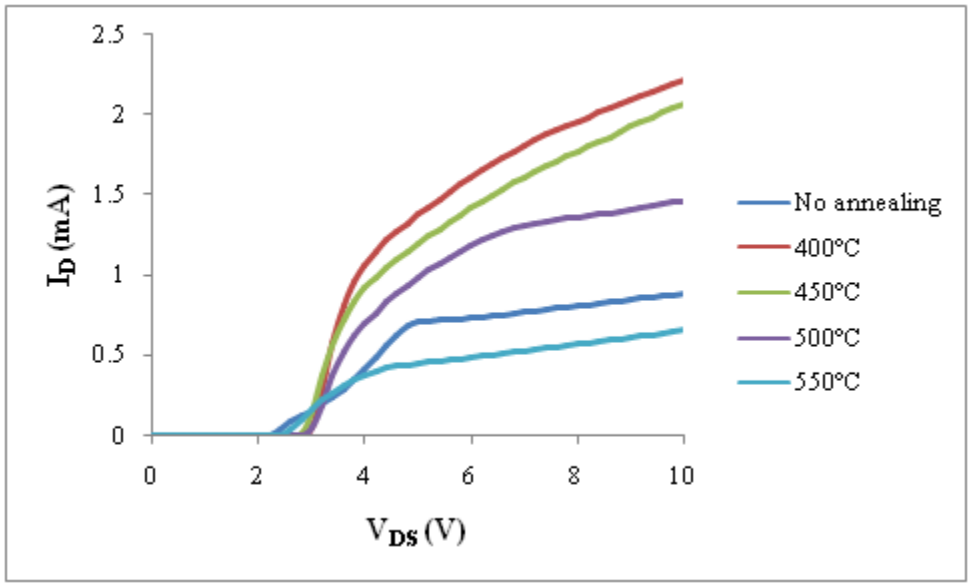


Figure 6.11 – Progression of I_D-V_{DS} characteristics (V_{GS} = 3V) for Device 3 after each annealing step

Device 4 from Sample D showed very similar characteristics to those of Device 2, both before and after annealing, as can be seen in Figures 6.12 and 6.13, respectively. Before annealing, the current did not quite saturate, but these characteristics were improved upon with annealing, and did not possess a kink. A

summary of these results can be seen in Figure 6.14. The transconductance and threshold voltage for this device were calculated as 0.3mS/mm and -1V, respectively.

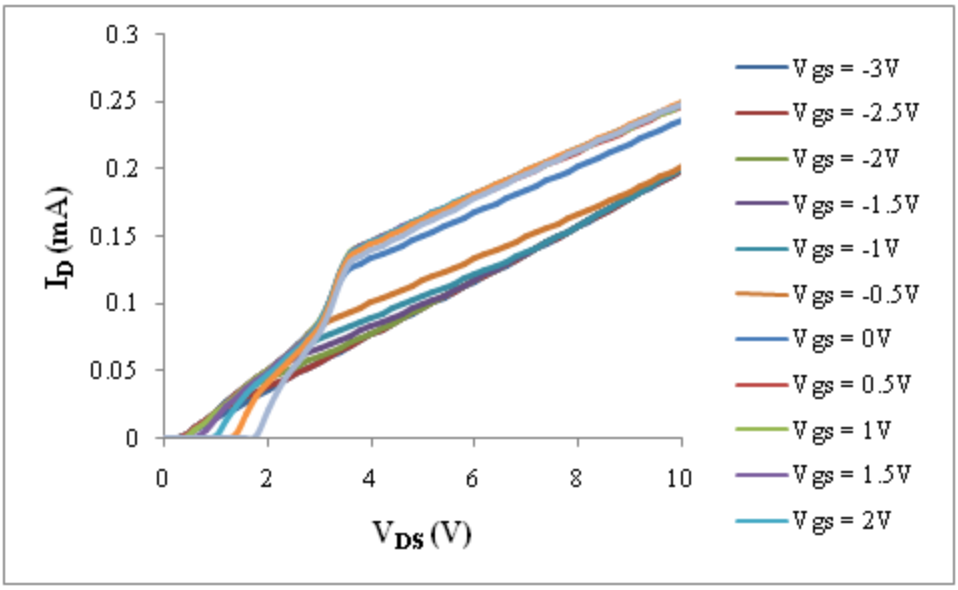


Figure 6.12 – I_D-V_{DS} characteristics for Device 4

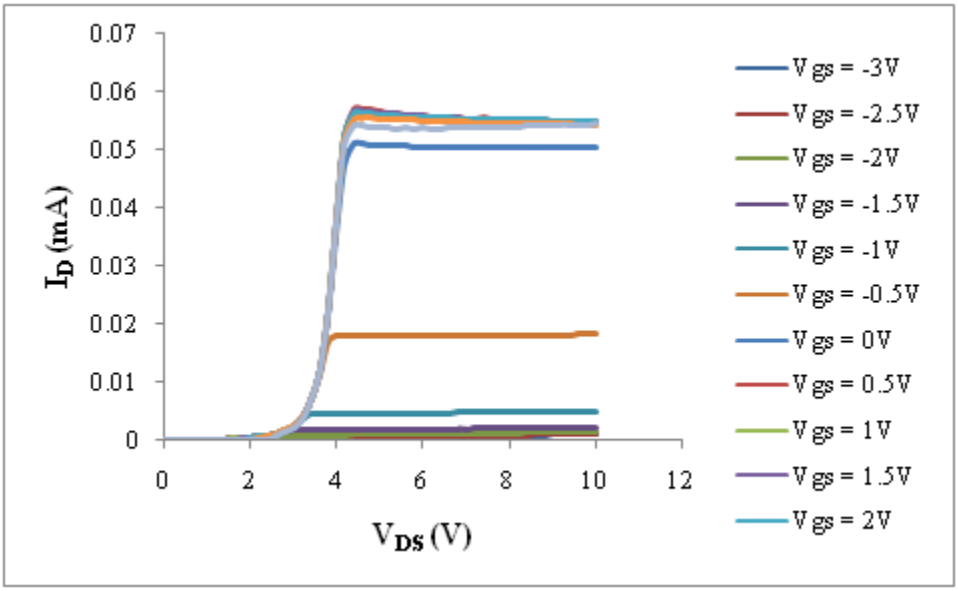


Figure 6.13 – I_D-V_{DS} characteristics for Device 4 after annealing at 550°C

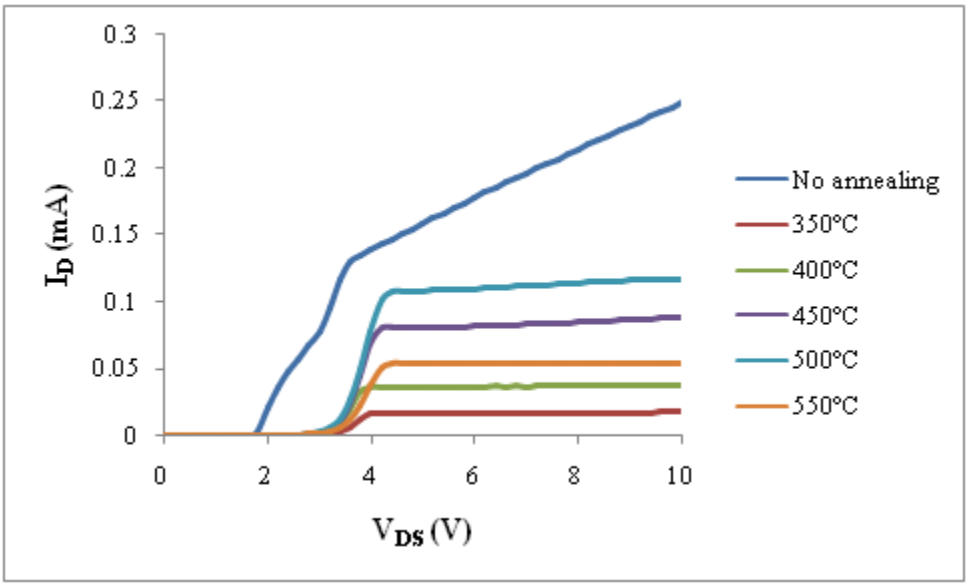


Figure 6.14 – Progression of I_D-V_{DS} characteristics (V_{GS} = 3V) for Device 4 after each annealing step

Finally, Device 5 from Sample E was measured and its I-V characteristics may be seen in Figure 6.15. This device displayed a larger current increase with increasing gate bias. However, the kink effect can already be seen even before annealing, and is further amplified after annealing, seen in Figure 6.16. An increase in current saturation for a negative applied gate bias and a decrease in current saturation for a positive applied gate bias can also be seen after annealing. A summary of the annealing results can be seen in Figure 6.17. Similarly to other devices after annealing, a drop in current was noted, and higher temperatures (500°C and 550°C) were actually found to be detrimental to the current-voltage characteristics and accentuated the kink effect.

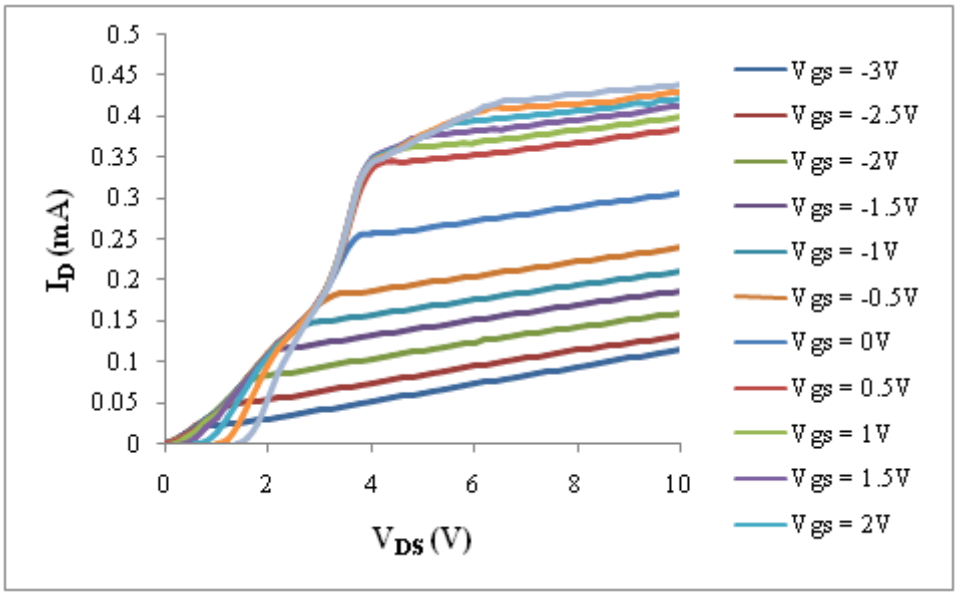


Figure 6.15 – I_D-V_{DS} characteristics for Device 5

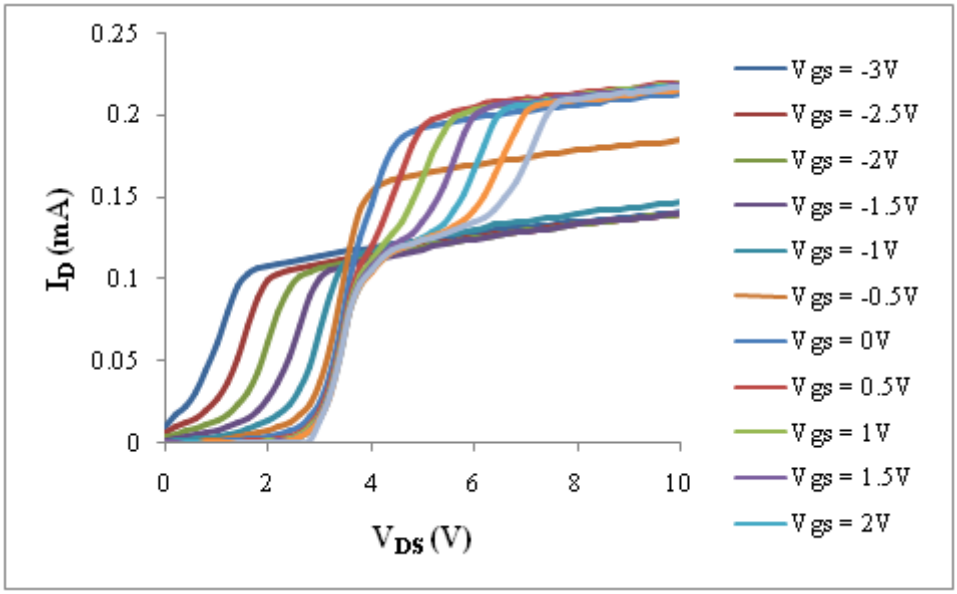


Figure 6.16 – I_D-V_{DS} characteristics for Device 5 after annealing at 550°C

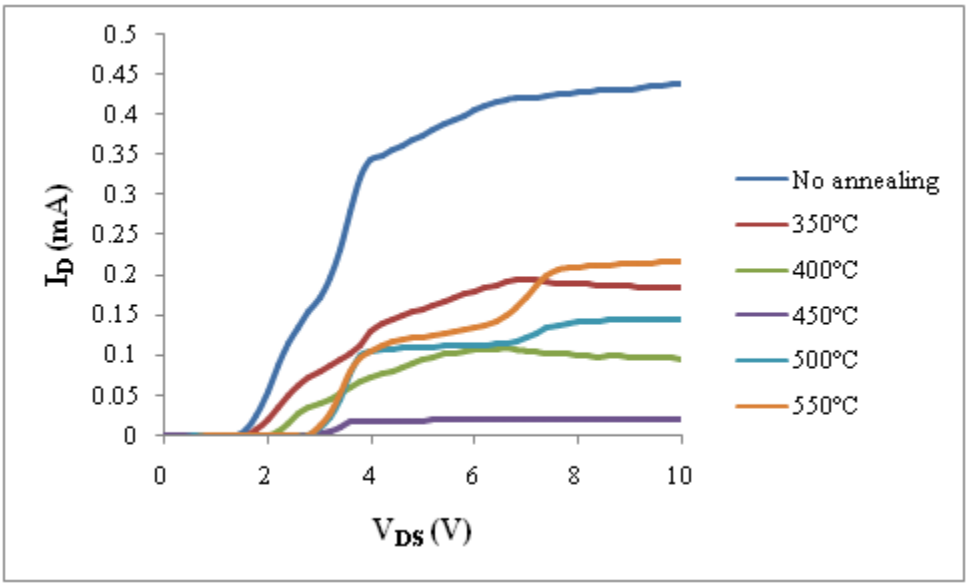


Figure 6.17 – Progression of I_D-V_{DS} characteristics (V_{GS} = 3V) for Device 5 after each annealing step

It can thus be seen that most devices exhibited similar characteristics. Annealing generally results in an improvement in current saturation by reducing the output conductance, as seen with Devices 2 and 4. It also, however, results in a current reduction, which could be due to a decrease in mobility due to increased scattering caused by defects in the area near the channel. At higher temperatures, the performance can be recovered, as atoms rearrange themselves due to annealing, reducing the defect density at the interface. There is, however, a limit in annealing temperature that can be reached before device performance is compromised and the sample suffers damage, as seen with Device 5.

As mentioned, one reason for the low saturation current is the large distance between the gate and drain (L_{gd}), which increases the series resistance. While a reduction of this length can be beneficial for both transconductance and on-resistance, there are also tradeoffs, such as with negative breakdown voltage

and punch-through effects. Thus, a compromise between aspects such as on-resistance and breakdown voltage must be found.

The breakdown voltage (V_{BR}) of a device is the voltage at which the phenomenon of avalanche breakdown occurs. This process occurs when the free electron carriers of a device are subjected to a strong acceleration by an electric field. These electrons can move fast enough to knock other electrons free, creating more free electron-hole pairs through impact ionization, resulting in a current increase due to the increased number of carriers. Breakdown voltage characterization was done for all samples. An example of a typical I_D-V_{DS} graph including breakdown voltage may be found in Figure 6.18. Devices would usually display hard breakdown, where the current would suddenly increase due to the device short circuiting at the breakdown voltage. However, soft breakdown did occasionally occur, where the current started to increase beyond the maximum saturation current before short circuiting. Upon breakdown, the transistor would short circuit and be destroyed. A comparison of the breakdown characteristics of a device from each sample is shown in Figure 6.19. Average breakdown values for each sample may be found in Table 6.1, along with a summary of the rest of the device results and the results obtained from the NRC sample and several devices found within the literature.

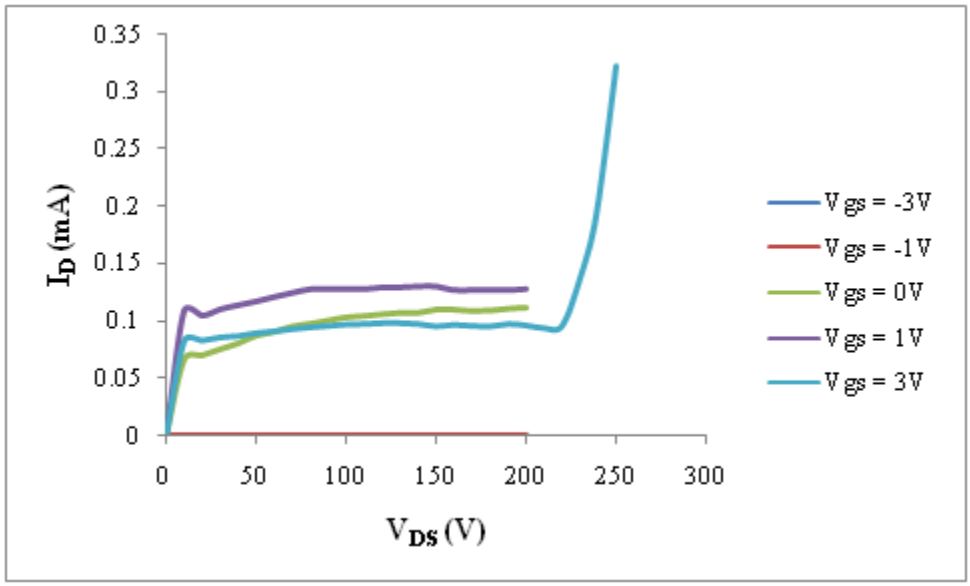


Figure 6.18 – Typical I_D-V_{DS} characteristics for Sample C at different gate voltages showing breakdown around 230V

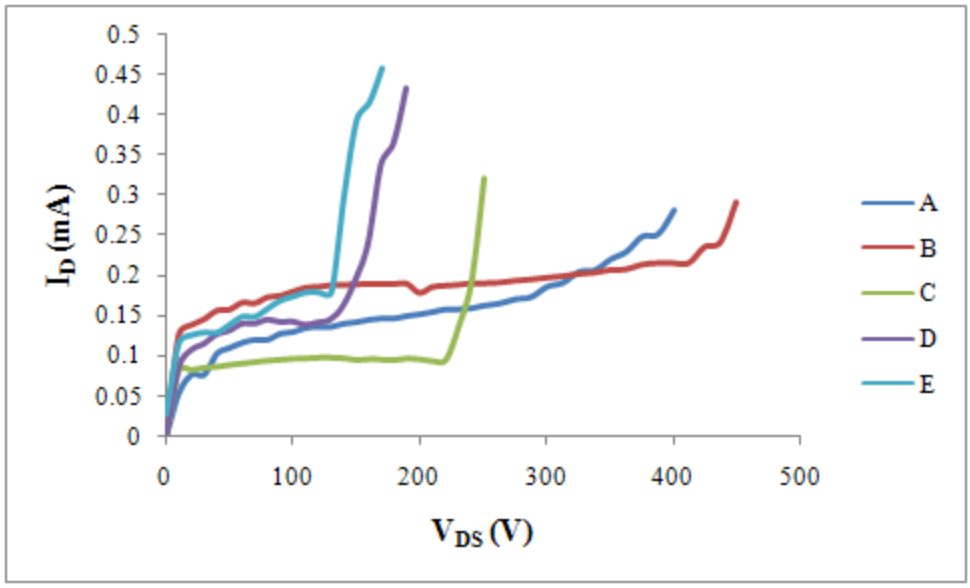


Figure 6.19 – Breakdown characteristics for one device from each of the five samples

Table 6.1 – Summary of average device characteristics

Device	L_{gd} (μm)	g_m (mS/mm)	V_t (V)	I_S (mA/mm)	V_{BR} (V)
Sample A	50	2.3	-1	3	350
Sample B	50	1.3	-1	1	450
Sample C	50	1.2	-2	4.5	230
Sample D	50	0.4	-1	1	160
Sample E	50	1	-1	3	160
NRC HEMT	5	12	-2	100	100
GaN on sapphire substrate [6.1]	13	150	-	500	570
GaN on SiC substrate [6.2]	20	105	-4	500	962
GaN on silicon substrate [6.3]	1.35	122	-9	910	40
GaAs [6.4]	0.5	-	0.5	200	30

The high voltage results for each device were found to be similar. However, the breakdown voltage of the fabricated devices was found to be dependent on the contact metal combination used, which could be attributed to the difference in work function among the metals. It was found that the addition of titanium for the drain and source reduced the breakdown voltage (comparing Samples A and B), though those devices also had lower resistance and thus higher saturation current.

While these devices did not reach the level of breakdown voltage of 1.9kV attained by devices on substrates such as silicon carbide [6.5], the breakdown voltages of these devices have been found to be comparable with other devices

found within the literature, particularly those on silicon substrates. Silicon substrates also maintain the distinct advantages of technology maturity, substantially lower cost compared to silicon carbide, as well as a higher thermal conductivity compared to sapphire, which allows for more efficient heat removal.

The maximum breakdown voltage of AlGaN/GaN HEMTs on silicon substrates was suggested by [6.6] to be limited by the GaN-to-Si substrate vertical leakage. Moreover, [6.7] explained that the drain-to-substrate forward bias leakage is due to hole generation in the buffer and electron injection from the silicon substrate into the buffer. Device performance could thus be improved significantly by removing the silicon substrate and transferring the HEMTs to a glass wafer through wafer bonding. Additional improvements to the devices could be made through procedures such as optimization for high breakdown voltage through the incorporation of a gate and mesa field plate, as well as the use of SiO_2 passivation.

7 Conclusions

The objective of this work was to design and fabricate AlGaN/GaN high electron mobility transistors and to characterize the devices in terms of current-voltage measurements and breakdown voltage. The effects of different contact metals as well as annealing were investigated, studying five different samples with titanium/gold (Sample A), nickel/gold (Samples B and C), platinum/gold (Sample D), and chromium/gold (Sample E) gate contact combinations, with (Samples C, D, and E) and without titanium (Samples A and B) drain and source contacts. These five samples, grown by MOCVD on silicon substrates and patterned in the lab using standard photolithography, were measured and their electrical performance was evaluated and compared to similar devices in the literature.

The various measured devices showed high breakdown voltage values, ranging from 160V to almost 500V. These values, though not as high as the breakdown for devices on other substrates such as silicon carbide, are comparable to or superior to others on silicon substrates and far outclass other materials such as AlGaAs/GaAs HEMTs. They are also higher than many other devices on silicon substrates found in the literature. Particularly due to the maturity and low cost of the technology, there is growing interest in silicon substrates for AlGaN/GaN HEMTs. Thus, this work has expanded on the current base of AlGaN/GaN HEMTs on silicon substrates, studying the performance of these devices compared with others.

It was discovered that the devices without titanium for their drain and source contacts exhibited higher breakdown voltage and the device with nickel/gold gate contacts had particularly high breakdown characteristics, with an average device breakdown around 450V. Future investigation is needed to determine the specific mechanisms dictating the effects of the Schottky gate contact metals.

The devices measured exhibited high drain-source series resistance, resulting in a low maximum saturation current density and transconductance, due to the large gate to drain distance. While a decrease in channel length would result in a lower resistance, it would also negatively impact the breakdown voltage and punch-through effects of the device. Thus, a compromise had to be made, taking into account these tradeoffs. Indeed, devices with lower breakdown generally displayed lower resistance and higher maximum saturation current. Future work could explore the effects of different channel lengths.

A few devices displayed high output conductance with poor current saturation. These effects were improved upon after annealing at temperatures ranging from 350°C to 550°C. While there was a drop in saturation current after the first annealing step, the current would tend to increase again with higher annealing temperatures. However, the electrical performance of several devices actually deteriorated with very high temperatures (500°C and 550°C) as the samples would get damaged, implying that there is an upper limit for annealing temperature that should be adhered to.

Potential future work would involve the optimization of the devices and trying new modifications to see the effect on the breakdown voltage and other

characteristic such as saturation current and transconductance. The breakdown voltage could be improved by techniques such as the incorporation of a gate and mesa field plate or SiO_2 passivation. The I-V characteristics could be improved through the development of better Ohmic drain and source contacts. Finally, other adjustments could be made, such as shifting the threshold voltage to a positive voltage in order to save power using techniques such as recessed gates and aluminum oxide passivation.

8 References

Chapter 1:

[1.1] Dingle, R., Stormer, H.L., Gossard, A.C., Wiegmann, W. (1978). Electron mobilities in modulation-doped semiconductor heterojunction superlattices. Appl. Phys. Lett., 33, 7, 665-667.

[1.2] Hiyamizu, S., Mimura, T., Fujii, T., Nanb, K. (1980). High mobility of two-dimensional electrons at the GaAs/n-AlGaAs heterojunction interface. Appl. Phys. Lett., 37, 9, 805-807.

[1.3] Mimura, T. (2005). Development of high electron mobility transistor. Japanese Journal of Applied Physics., 44, 12, 8263-8268.

[1.4] Ketterson, A., Moloney, M., Masselink, W.T., Peng, C.K., Klem, J., Fischer, R., Kopp, W. (1985). IEEE Electron Device Letters, 6, 12, 628-630.

[1.5] Wang, G-W., Chen, Y-K., Schaff, W.J., Eastman, L.F. (1988). A 0.1-um gate $Al_{0.5}In_{0.5}As/Ga_{0.5}In_{0.5}As$ MODFET fabricated on GaAs substrates. IEEE Transactions on Electron Devices, 35, 7, 818-823.

[1.6] Cheng, K.Y., Cho, A.Y. (1982). Electron mobilities in modulation doped $Ga_{0.47}In_{0.53}As/Al_{0.48}In_{0.52}As$ heterojunctions grown by molecular beam epitaxy. Appl. Phys. Lett., 40, 147, 147-149.

[1.7] Chang, C-A., Chang, L.L., Mendez, E.E., Christie, M.S., Esaki, L. (1984). Electron densities in InAs-AlSb quantum wells. Journal of Vacuum Science and Technology B, 2, 2, 214-216.

[1.8] Abstreiter, G., Brugger, H., Wolf, T. (1985). Strain-induced two-dimensional electron gas in selectively doped Si/Si_xGe_{1-x} superlattices. Physical Letter Reviews, 54, 22, 2441-2444.

[1.9] Fritz, I.J., Doyle, B.L., Schirber, J.E., Jones, E.D., Dawson, L.R. (1986). Influence of built-in strain on Hall effect in InGaAs/GaAs quantum well structures with p-type modulation doping. Appl. Phys. Lett., 49, 10. 581-583.

[1.10] Razeghi, M., Maurel, P., Tardella, A., Dmowski, L., Gauthier, D. (1986). First observation of two-dimensional hole gas in a $Ga_{0.47}In_{0.53}As/InP$ heterojunction grown by metalorganic vapor deposition. Journal of Applied Physics, 60, 7, 2453-2456.

[1.11] Hansen, W., Smith, T.P., Piao, J., Beresford, R., Wang, W.I. (1990). Magnetoresistance measurements of doping symmetry and strain effects in GaSb-AlSb quantum wells. Appl. Phys. Lett., 56, 81, 81-83.

[1.12] Klem, J.F., Lott, J.A., Schirber, J.E., Kurtz, S.R. (1993). Strained quantum well modulation-doped InGaSb/AlGaSb structures grown by molecular beam epitaxy. Journal of Electronic Materials, 22, 3, 315-318.

[1.13] Maruska, H.P., Tietjen, J.J. (1969). The preparation and properties of vapor-deposited single-crystalline GaN. Appl. Phys. Lett., 15, 10, 327-329.

[1.14] Khan, M.A., Kuznia, J.N., Van Hove, J.M., Pan, N., Carter, J. (1992). Observation of a two-dimensional electron gas in low pressure Metalorganic chemical vapor deposited $GaN-Al_xGa_{1-x}N$ heterojunctions. Appl. Phys. Lett., 60, 24, 3027-3029.

[1.15] Reprinted with permission from Khan, M.A., Kuznia, J.N., Olson, D.T., Schaff, W.J., Burm, J.W. et al. (1994). Microwave performance of a 0.25 um gate AlGaN/GaN heterostructure field effect transistor. Appl. Phys. Lett., 65, 9, 1121-1123. Copyright 1994, American Institute of Physics.

[1.16] Green, B.M., Chu, K.K., Chumbes, E.M., Smart, J.A., Shealy, J.R., Eastman, L.F. (2000). The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMT's. IEEE Electron Device Letters, 21, 6, 268-270.

[1.17] Ando, Y., Okamoto, Y., Miyamoto, H., Nakayama, T., Inoue, T., Kuzuhara, M. (2003). 10-W/mm AlGaN-GaN HFET with a field modulating plate. IEEE Electron Device Letters, 24, 5, 289-291.

[1.18] Dora, Y., Chakraborty, A., McCarthy, L., Keller, S., DenBaars, S.P., Mishra, U.K. High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates. IEEE Electron Device Letters, 27, 9, 713-715.

[1.19] Liu, S., Wang, J., Gong, R., Lin, S., Dong, Z., Yu, M., Wen, C.P., Zeng, C., Cai, Y., Zhang, B., Xu, F., Zhang, J., Shen, B. (2011). Enhanced device performance of AlGaN/GaN high electron mobility transistors with thermal oxidation treatment. Japanese Journal of Applied Physics, 50, 04DF10-1-4.

[1.20] Wang, C., Cho, S.J., Lee, W.S. Kim, N.Y. (2012). A novel method for the fabrication of AlGaN/GaN HEMTs on Si (111) substrates. International Journal of Advanced Manufacturing Technology, 10.1007/s00170-012-4583-4.

[1.21] Kikkawa, T., Joshin, K., Kanamura, M. (2012) GaN device for highly efficient power amplifiers. Fujitsu Sci. Tech. J., 48, 1, 40-46.

Chapter 2:

[2.1] Bhattacharya, P. (1997). *Semiconductor Optoelectronic Devices*. (2nd ed., pp. 2, 63, 210-211, 549). Prentice Hall, Inc.

[2.2] Eastman, L.F., Mishra, U.K. (2002). The Toughest Transistor. IEEE Spectrum, 39, 5, 28-33.

[2.3] Morkoc, H., Strite, S., Gao, G.B., Lin, M.E., Sverdlov, B., Burns, M. (1994). Large-band-gap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies. Journal of Applied Physics, 76, 3, 1363-1398.

[2.4] Adachi, S. (1992). *Physical Properties of III-V Semiconductor Compounds: InP, InAs, GaAs, GaP, InGaAs, and InGaAsP*. (pp. 4, 11). John Wiley & Sons.

[2.5] Chen, A-B., Sher, A. (1995). *Semiconductor Alloys*. (p. 2). Plenum Press.

[2.6] Nakamura, S., Mukai, T., Senoh, M. (1994). Candela-class high-brightness InGaN/AlGaN double-heterostructure blue-light-emitting diodes. Appl. Phys. Lett., 64, 13, 1687-1689.

[2.7] Nakamura, S., Senoh, M., Iwasa, N., Nagahama, S. (1995). High-brightness InGaN blue, green and yellow light-emitting diodes with quantum well structures. Japanese Journal of Applied Physics, 34, L797-L799.

[2.8] Nakamura, S., Senoh, M., Nagahama, NS., Iwasa, N., Yamada T., Matsushita, T., Kiyoku, H., Sugimoto, Y. (1995). InGaN-based multi-quantum-well-structure laser diodes. Japanese Journal of Applied Physics, 35, L74-L76.

[2.9] Schubert, M.F., Chhajed, S., Kim, J.K., Schubert, E.F. (2007). Effect of dislocation density on efficiency droop in GaInN/GaN light-emitting diodes. Appl. Phys. Lett., 91, 23, 231114-1-3.

Chapter 3:

[3.1] Yu, P.Y., Cardona, M. (2010). *Fundamentals of Semiconductors: Physics and Materials Properties*. (4th ed., p. 223).Springer.

[3.2] Lenka, T.R., Panda, A.K. (2011). Characteristics study of 2DEG transport properties of AlGaN/GaN and AlGaAs/GaAs-based HEMT. Semiconductors, 45, 5, 660-665.

[3.3] Reprinted with permission from Ambacher, O., Smart, J., Shealy, J.R., Weimann, N.G., Chu, K., Murphy, M., Schaff, W.J., Eastman, L.F. (1999). Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures. Journal of Applied Physics, 85, 6, 3222-2233. Copyright 1999, American Institute of Physics.

[3.4] Trew, R.J. (2002). SiC and GaN Transistors – Is there one winner for microwave power applications? Proceedings of the IEEE, 90, 6, 1032-1047.

[3.5] Jarnadal, A.H. (2007). *Large-Signal Modeling of GaN Device for High Power Amplifier Design*. (p. 13). University of Kassel.

[3.6] Dobrovinskaya, E.R., Lytvynov, L.A., Pishchik, V. (2009). *Sapphire: Material, Manufacturing, Applications*. (p. 110). Springer.

[3.7] Ahmed, N.M., Hashim, M.R., Hassan, Z. (2006). Effects of Si, Al_2O_3 and SiC substrates on the characteristics of DBRS structure for GaN based laser. Journal of Physical Science, 17, 2, 151-159.

[3.8] Dadgar, A., Schulze, F., Wienecke, M., Gadanecz, A., Blasing, J., Veit, P., Hempel, T., Diez, A., Christen, J., Krost, A. (2007). Epitaxy of GaN on silicon – impact of symmetry and surface reconstruction. New Journal of Physics, 9, 10, 389.

[3.9] Binari, S.C., Ikossi, K., Roussos, J., Kruppa, W., Park, D., Dietrich, H.B., Koleske, D.D., Wickenden, A.E., Henry, R. L. (2001). Trapping effects and microwave power performance n AlGaN/GaN HEMTs. IEEE Transactions Electron Devices, 48, 3, 465-471.

[3.10] Mishra, U.K., Parikh, P. Wu, Y-F. (2002). AlGaN/GaN HEMTs – An overview of device operation and applications. Proceedings of the IEEE, 90, 6, 1022-1031.

[3.11] Krishnamurthy, K., Martin, J., Landberg, B., Vetury, R., Poulton, M.J. (2008). Wideband 400 W pulsed power GaN HEMT amplifiers. *Microwave Symposium Digest, 2008. IEEE/MTT-S International*, 303-306.

[3.12] Shigematsu, H., Inoue, Y., Akasegawa, A., Yamada, M., Masuda, S., Kamada, Y., Yamada, A., Kanamura, M., Ohki, T., Makiyama, K., Okamoto, N., Imanishi, K., Kikkawa, T., Joshin, K., Hara, N. (2009). C-band 340-W and X-band 100-W GaN power amplifiers with over 50-% PAE. *Microwave Symposium Disgest, 2009. IEEE/MTT-S International*, 1265-1268.

[3.13] Takagi, K., Takatsuka, S., Kashiwabara, Y., Teramoto, S., Matsushita, K., Sakurai, H., Onodera, K., Kawasaki, H., Takada, Y., Tsuda, K. (2009). Ku-Band AlGaN/GaN-HEMT with over 30% of PAE. *Microwave Symposium Digest, 2009. IEEE/MTT-S International*, 457-460.

[3.14] Takagi, K., Matsushita, K., Kashiwabara, Y., Masuda, K., Nakanishi, S., Sakurai, H., Onodera, K., Kawasaki, H., Takada, Y., Tsuda, K. (2010). Developing GaN HEMTs for Ka-band with 20W. *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2010 IEEE*, 1-4.

[3.15] Karmalkar, S., Shur, M.S., Gaska, R. (2003). GaN-based Power High Electron Mobility Transistors, Chapter 3 in *Wide Energy Bandgap Electronic Devices*. (pp. 175-218). World Scientific.

[3.16] Kachi, T., Kikuta, D., Uesugi, T. (2012). GaN power device and reliability for automotive applications. *Reliability Physics Symposium (IRPS), 2012 IEEE International*, 3D.1.1, 3D.1.4, 15-19.

Chapter 4:

[4.1] Dapkus, P.D. (1984). A critical comparison of MOCVD and MBE for heterojunction devices. Journal of Crystal Growth, 68, 1, 345-355.

[4.2] Veuhoff, E. (1995). MOCVD of Compound Semiconductor Layers, Chapter 2 in *Handbook of Compound Semiconductors: Growth, Processing, Characterization, and Devices*, (pp. 29-74). Noyes Publications.

[4.3] Barron, A.R. (2010). Chemical Vapor Deposition, Module 6 in *Chemistry of Electronic Materials*. Rice University.

[4.4] Haynes, W.M. (2012-2013). *CRC Handbook of Chemistry and Physics* (93rd ed., p. 12-124). CRC Press.

Chapter 5:

[5.1] "Gallium Nitride MMIC Foundry Design Manual," Revision 1.0, National Research Council Canada, 2011.

Chapter 6:

[6.1] Zhang, N-Q., Keller, S., Parish, G., Heikman, S., DenBaars, S.P., Mishra, U.K. (2000). High breakdown GaN HEMT with overlapping gate structure. IEEE Electron Device Letters, 21, 9, 421-423.

[6.2] Kim, M., Choi, Y-H., Lim, J., Kim, Y-S., Seok, O., Han, M-K. (2010). High breakdown voltage AlGaN/GaN HEMTs employing recessed gate edge structure. *CS Mantech Conference, 2010*, 237-240.

[6.3] Javorka, P., Alam, A., Wolter, M., Fox, A., Marso, M., Heuken, M., Luth, H., Kordos, P. (2002). AlGaN/GaN HEMTs on (111) silicon substrates. IEEE Electron Device Letters, 23, 1, 4-6.

[6.4] Pala, V., Hella, M., Chow, T.P. (2011). Safe operating area of AlGaAs/InGaAs/GaAs HEMT power transistors. *Proceedings of the 23rd International Symposium on Power Semiconductor Devices & IC's*. 243-246.

[6.5] Dora, Y., Chakraborty, A., McCarthy, . Keller, S., DenBaars, S.P., Mishra, U.K. (2006). High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates. IEEE Electron Device Letters, 27, 9, 713-715.

[6.6] Lu, B., Piner, E.L., Palacios, T. (2010). Schottky-drain technology for AlGaN/GaN high-electon mobility transistors. IEEE Electron Device Letters, 31, 4, 302-304.

[6.7] Lu, B., Piner, E.L., Palacios, T. (2010). Breakdown mechanism in AlGaN/GaN HEMTs on Si substrate. *Proceedings of the Device Research Conference (DRC), 2010*, 193-194.

Appendix A – Fabrication Procedure

HEMT fabrication procedure:

1. Cut wafer into appropriate dimensions using a diamond scriber (Figure A.1).

Fig. A.1 – Sample before processing

2. Photolithography process using Mask #1:
    a. Put the sample on the holder of the spinner.
    b. Apply 5 drops of 1827 photoresist on the sample.
    c. Spin the sample at 3000 rpm for 30 seconds.
    d. Pre-bake the sample at 90°C for 10 minutes.
    e. Align the sample to Mask #1 and expose it under UV light (300W) for 6 minutes).
    f. Develop the exposed photoresist in concentrated developer for 30 seconds.
    g. Rinse the sample with de-ionized (DI) water for one minute and blow-dry (Figure A.2).

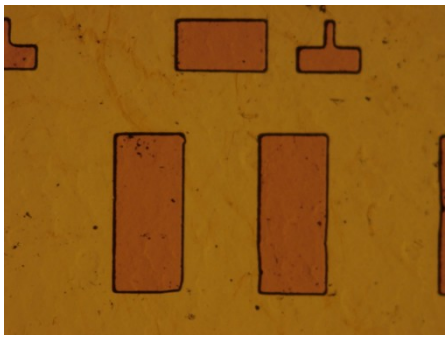


Fig. A.2 – Sample after Mask 1 patterning and development

h. Immerse the sample in iodine for 2 minutes to remove exposed Au.

i. Rinse the sample with DI water for one minute and blow-dry (Figure A.3).

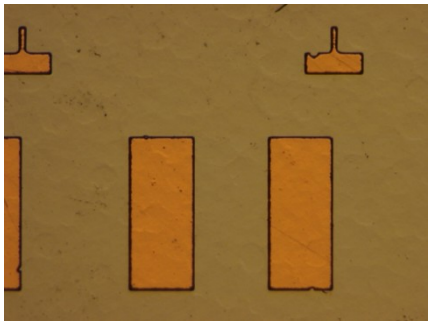


Fig. A.3 – Sample after Mask 1 patterning and gold etching

j. Immerse the sample in buffered hydrofluoric acid (BHF) for 30 seconds to remove the exposed titanium.

k. Rinse the sample with DI water for 5 minutes and blow-dry (Figure A.4).

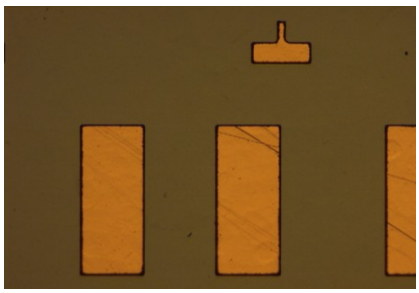


Fig. A.4 – Sample after Mask 1 patterning and titanium etching

l. Immerse the sample in acetone for 3 minutes to thoroughly remove the photoresist.

m. Rinse the sample with DI water for at least 30 seconds and blow-dry (Figure A.5).

n. Post-bake the sample at 90°C for 5 minutes.

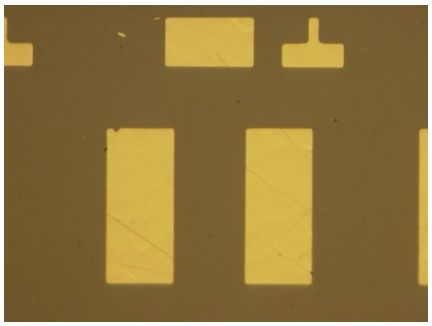


Fig. A.5 – Sample after Mask 1 patterning and photoresist removal

3. Titanium deposition (Figure A.6).

Fig. A.6 – Sample after titanium deposition

4. Photolithography using Mask #2:

a. Put the sample on the holder of the spinner.

b. Apply 5 drops of 1827 photoresist on the sample.

c. Spin the sample at 3000 rpm for 30 seconds.

d. Pre-bake the sample at 90°C for 10 minutes.

e. Align the sample to Mask #2 and expose it under UV light (300W) for 6 minutes.

f. Develop the exposed photoresist in the concentrated developer for 30 seconds.

g. Immerse the sample into DI water for one minute and blow-dry (Figure A.7).

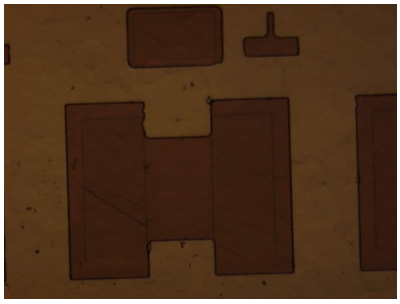


Fig. A.7 – Sample after Mask 2 patterning and development

h. Immerse the sample in BHF for 30 seconds to remove the exposed titanium.

i. Rinse the sample with DI water for 5 minutes and blow-dry (Figure A.8).

j. Post-bake the sample at 90°C for 5 minutes.

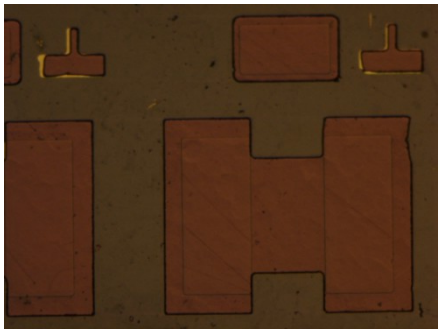


Fig. A.8 – Sample after Mask 2 patterning and titanium etching

5. Reactive ion etching:

    a. Etching process described in chapter 4 (Figure A.9).

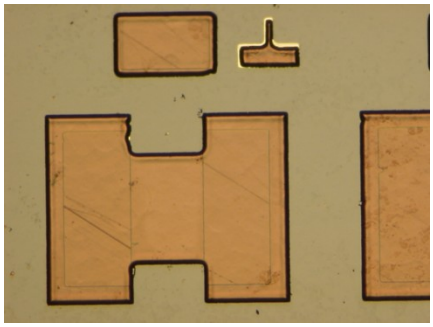


Fig. A.9 – Sample after reactive ion etching

    b. Immerse the sample in acetone for 20 minutes.

    c. Rinse the sample with DI water for 5 minutes and blow-dry (Figure A.10).

    d. Post-bake the sample at 90°C for 5 minutes.

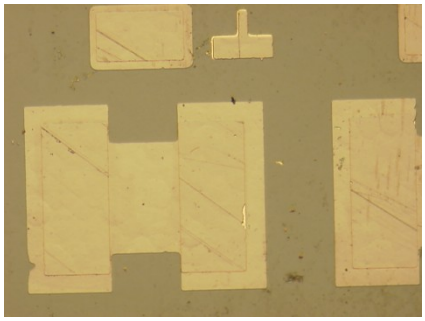


Fig. A.10 – Sample after reactive ion etching and after photoresist removal

6. Photolithography using Mask #3:

    a. Put the sample on the holder of the spinner.

    b. Apply 5 drops of 1827 photoresist on the sample.

    c. Spin the sample at 3000 rpm for 30 seconds.

    d. Pre-bake the sample at 90°C for 10 minutes.

e. Align the sample to Mask #3 and expose it under UV light (300W) for 6 minutes.

f. Develop the exposed photoresist in the concentrated developer for 30 seconds.

g. Immerse the sample into DI water for one minute and blow-dry (Figure A.11).

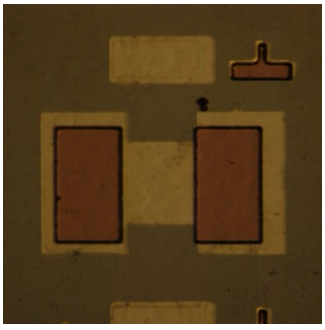


Fig. A.11 –Sample after Mask 3 patterning and development

h. Immerse the sample in BHF for 30 seconds to remove the exposed titanium in the gate area.

i. Rinse with DI water for 5 minutes and blow-dry (Figure A.12).

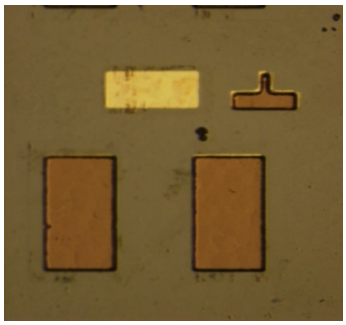


Fig. A.12 – Sample after Mask 3 patterning and titanium etching

j. Immerse the sample in acetone for 3 minutes to thoroughly remove the photoresist.

k. Rinse with DI water for at least 30 seconds and blow-dry (Figure A.13).

l. Post-bake the sample at 90°C for 5 minutes.

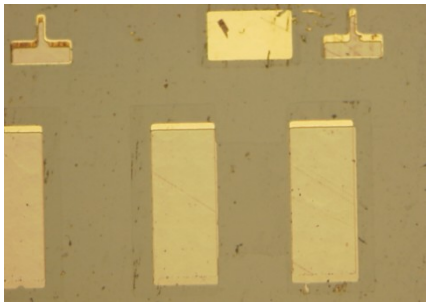


Fig. A.13 – Sample after Mask 3 patterning and photoresist removal

7. GaN etching:

a. Turn on the Dymax UV light source to warm up and put the bottle containing the 0.3M KOH + 0.1M $K_2S_2O_8$ solution in a warm water bath for 3 minutes.

b. Put the sample in a petri dish and pour in the warm solution.

c. Expose the sample to the Dymax UV light for 20 seconds while turning the petri dish to ensure uniform light illumination.

d. Rinse the sample in DI water for 20 minutes and blow-dry (Figure A.14).

e. Post-bake the sample at 90°C for 10 minutes.

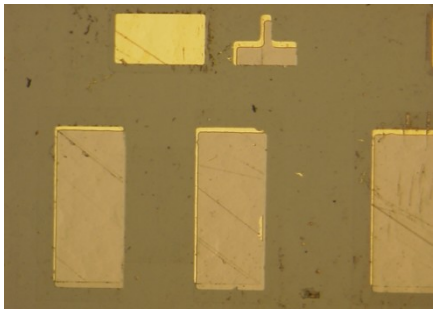


Fig. A.14 – Sample after GaN etching

8. Photolithography using Mask #4:

    a. Put the sample on the holder of the spinner.

    b. Apply 5 drops of 1827 photoresist on the sample.

    c. Spin the sample at 4000 rpm for 20 seconds.

    d. Bake the sample at 95-98°C for 10 minutes.

    e. Load sample into the vacuum with 5 pieces of aluminum (d = 9 cm) and evacuate for 2 hours.

    f. Evaporate aluminum (Figure A.15).

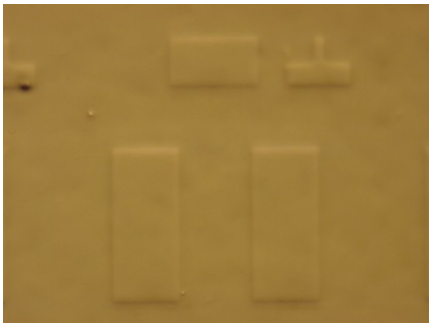


Fig. A.15 – Sample after aluminum deposition

    g. Put the sample on the holder of the spinner.

    h. Apply 5 drops of 1928 photoresist on the sample.

    i. Spin the sample at 4000 rpm for 20 seconds.

    j. Bake the sample at 80°C for 7 minutes.

    k. Align the sample to Mask #4 and expose it under UV light (300W) for 5 minutes.

    l. Develop the exposed photoresist in the concentrated developer for 30 seconds.

    m. Immerse the sample into DI water for one minute and blow-dry (Figure A.16).

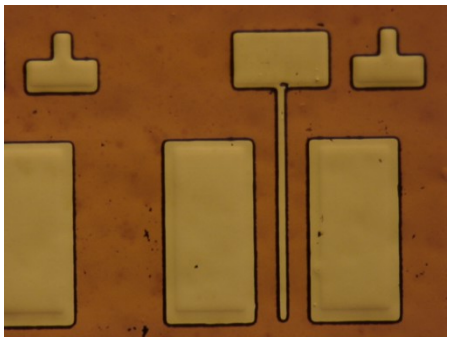


Fig. A.16 – Sample after Mask 4 patterning and development

n. Etch the aluminum at 50ºC, rinse thoroughly, and blow-dry (Figure A.17).

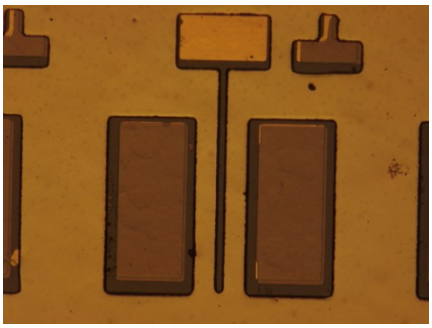


Fig. A.17 – Sample after Mask 4 patterning and aluminum etching

o. Expose the sample under UV light for 6 minutes.

p. Develop the exposed photoresist in the concentrated developer for 30 seconds, rinse, and blow-dry.

q. Expose the sample under UV light for 4 minutes.

r. Develop the exposed photoresist in the concentrated developer for 30 seconds, rinse, and blow-dry (Figure A.18).

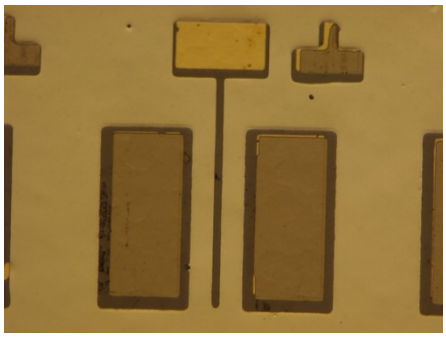


Fig. A.18 – Sample after Mask 4 patterning and photoresist removal

9. Gate contact deposition:

    a. Evaporation of gate metal (nickel, titanium, platinum, or chromium) and then gold (Figure A.19).

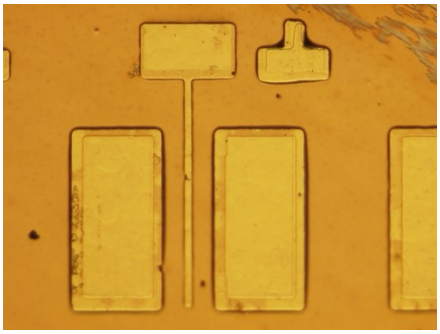


Fig. A.19 – Sample after gate metal deposition (Ni/Au pictured)

    b. Immerse sample in acetone twice, rinse in DI water, and blow-dry (Figure 4.10).

    c. Bake sample at 90ºC for 10 minutes.