NOTE TO USERS

TEXTURE AND MICROSTRUCTURE IN COPPER DAMASCENE INTERCONNECTS

BY

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ABSTRACT

Copper has been recently used as an interconnecting material since it has high conductivity and good electromigration failure resistance. Recent studies show the close relationship between texture and reliability of Cu damascene interconnects. However, textural and microstructural evolutions of Cu damascene interconnects as function of substrate texture, current density, line width and annealing process are still not well understood.

At first, to understand the influence of substrate texture and electroplating conditions on the texture and surface morphology of Cu electrodeposits, three different polycrystalline copper specimens were used as substrates and electrodeposits were plated using different current densities. The mechanism of growth of Cu electrodeposits and the importance of smooth surface morphology were discussed.

To analyze the effect of line width and annealing process on textural and microstructural evolution of Cu damascene interconnects, Cu interconnects samples which have a different line width and different annealing process were investigated. According to x-ray diffraction (XRD) and electron backscattered diffraction (EBSD) results, the directional changes of (111) plane orientation with the different line width and annealing were observed. In addition, the analysis of microstructure and grain boundary character distribution (GBCD) of Cu damascene interconnects demonstrated that bamboo-like microstructure was developed in the narrow line and a polygranular structure was developed in the wider line. Also, the fraction of $\Sigma 3$ boundaries was changed depending on the line width and annealing process.

To analyze a relationship between the stress distribution and textural and microstructural evolution in the samples investigated, stress was calculated using finite element method (FEM), and these results were verified by physical stress simulation of copper in the Chapter 7. Through this investigation, it was found that the inhomogeneity of stress distribution in Cu damascene interconnects is an important factor which is necessary for understanding textural transformation after annealing, and the effects of stress on textural and microstructural evolution of Cu depends on the crystallographic texture and the annealing temperature.

A new interpretation of textural and microstructural evolution in Cu damascene interconnects lines after annealing and possible factors responsible for the texture transformation are suggested, and the optimum processing conditions are recommended.

RÉSUMÉ

Le cuivre a été recemment utilisé pour les interconnection vue sa conductivité élevée et sa bonne resistance à la rupture par electromigration. Des études récentes montrent le rapport étroit entre la texture et la fiabilité des interconnections damascène en Cu. Cependant, l'évolution de la texture et de la microstructure des interconnections damascène en Cu en fonction de la texture du substrat, de la largeur du ligne et du procédé de recuit sont toujours non bien compris.

Tout d'abord, pour comprendre l'influence de la texture du substrat et des conditions de l'electrodeposition sur la texture et la morphologie du dépôt du cuivre, trois différents échantillons en cuivre polycrystallins ont été utilisés comme substrat et le procédé de l'electrodeposition a été réalisé avec des densités de courant différentes. Le mécanisme de la croissance du dépôt de cuivre et l'importance d'une morphologie douce de la surface ont été discutés.

Pour analyzer l'effet de la largeur de la ligne et du procédé de recuit sur l'évolution de la texture et de la microstructure des interconnections damascène en Cu, des échantillons des interconnections en Cu avec des largeurs de ligne différentes et des procédés de recuit différents, ont été étudiés. Les résultats de la diffraction des rayon x (XRD) et de la diffraction des électrons (EBSD) montrent un changement directionnel de l'orientation du plan (111) avec les différentes largeurs du ligne et les différents procédés de recuit. En plus, l'analyse de la microstructure et de la distribution du charactère du joint de grain (GBCD) des interconnection en Cu a demontré qu'une microstructure "bambou" a été developpée dans la ligne étroite et qu'une structure polygranulaire a été

developpée dans la ligne la plus large. Aussi, la fraction des joints Σ3 a été changée dépendemment de la largeur du ligne et du procédé de recuit.

Pour étudier une relation possible entre la distribution des contraintes et l'évolution de la texture dans les échantillons étudiés, la contrainte a été calculée avec la méthode des elements finis, et les résultats ont été verifiés avec une méthode de simulation des contraintes physiques du cuivre dans le chapite 7. Cette étude a révélée que l'inhomogénéité de la distribution des contraintes dans les interconnection damascène en Cu est un facteur important et nécessaire pour comprendre la transformation de la texture après recuit, et que les effets de contraintes sur l'évolution de la textura et de la microstructure du cuivre dependent de la texture crystallographique et de la temperature de recuit.

Une nouvelle interpretation de l'évolution de la texture et de la microstructure dans les interconnections damascène en Cu après recuit et des facteurs pouvant être responsables de la transformation de la texture sont suggérés, les conditions optimales du procédé d'électrodeposition sont recommendés.

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Chapter 1

Introduction

Integrated circuits chips consist of 10^8 individual components (transistors, resistors, capacitors, etc.), fabricated side by side in a common substrate and wired together to perform a particular circuit function. These wires are usually simply referred to as interconnects. In the industry, it is a trend to make more complex circuit through making the individual components smaller which allows more of them to be integrated in a given area. The higher levels of integrated circuits permitted by these smaller devices have made it possible to build progressive, more complex, higher-performance, and more economical integrated systems. Decreasing component size is often characterized in IC technology by the minimum width of interconnect line. This dimensional change is plotted in Figure 1.1 [1-3].

Since interconnects occupy a large fraction of the total volume of IC chips, reducing the average interconnect width allows an increase in the packing density of the

devices in a circuit. Also, by reducing interconnect width, the transmission distances are reduced and thus operation speed can be increased. Consequently, there is a tremendous incentive to produce designs with interconnects that carry higher current density. During the operation of an IC, interconnects carry current densities as high as 5×10^5 A/cm^2. In comparison, the maximum current density allowed for house wiring is of 10^2 A/cm^2.

At the same time, the signal delay caused by interconnect becomes a dominant factor limiting speed performance as the features of integrated circuitry (IC) chips are scaled to submicron dimensions, because resistance and capacitance of the interconnects increase due to the reduction of line cross-sectional area and space between lines [4-8]. As a result, a highly reliable wiring which allows high current density is required.

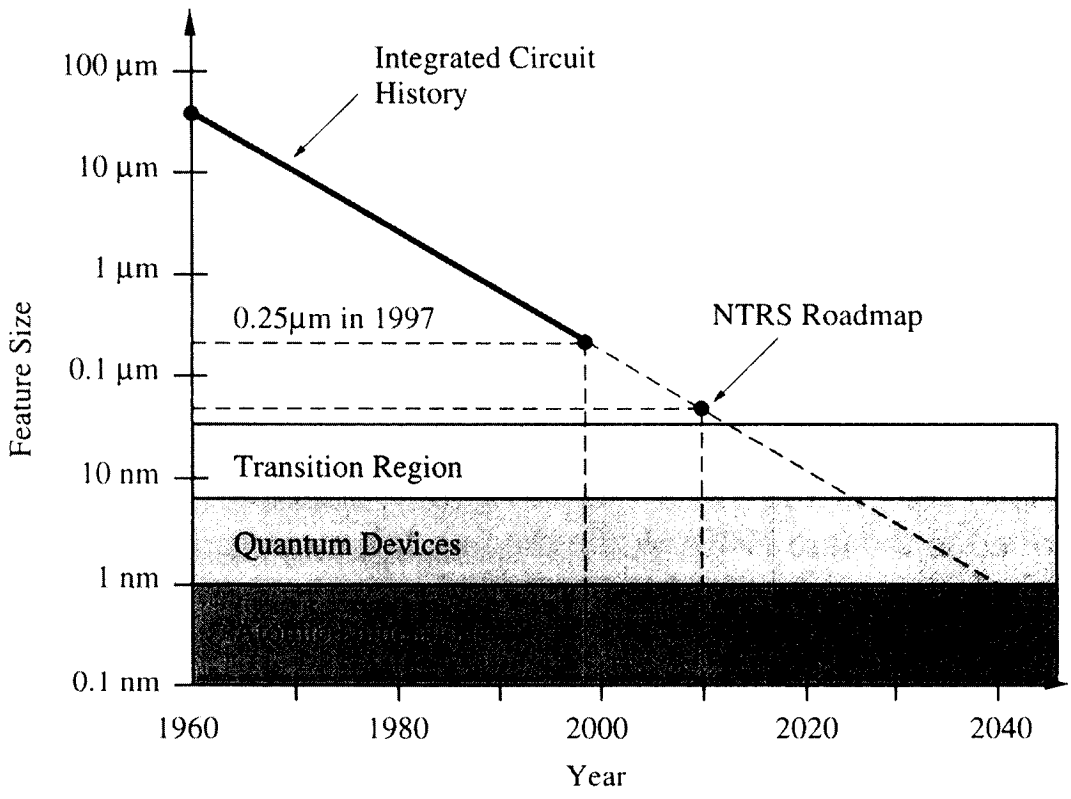


Figure 1.1. Historical trends and future projections for the minimum feature size used integrated circuits in manufacturing [1-3].

Recently, copper has been the new metallization material and replaces aluminum in ultra-large scale integration (ULSI) devices and electronic packaging due to its high conductivity, low electrical resistivity and good electromigration resistance. However, the use of Cu as an alternative materials to Al(Cu) in ULSI wiring offers processing challenges because of its tendency to corrode under standard chip fabrication conditions and presents poor adhesion to dielectric materials (e.g. SiO_2, polyimide). Therefore, it is needed to develop the reproducible and cost-effective processing techniques for chip fabrication, so called Cu damascene process which will be explained in Chapter 2.

Since the Cu damascene process has been introduced in the IC, significant progress and extensive research on the Cu damascene interconnects technology has been done in the past few years [4-15]. One of the most important stages in this technology is Cu electroplating process which is characterized by excellent gap filling, high deposition rate, low temperature processing, system simplicity, and good process control [4, 16-20]. To fill a trench without creating voids, the substrate (Cu seed layer) for electroplating should have continuous and smooth structure along the sidewalls and bottom of the trench. Until now, it is known that the best material for seed layer is copper itself [4, 5]. It is well known that electroplating process conditions such as current density, pH value and bath temperature, can change the quality of the electrodeposits [21, 22]. Also, strong {111} texture increases the resistance to electromigration failure and this failure can be correlated with the frequency of the occurrence of CSL (coincidence site lattice) boundaries or low or high diffusivity boundaries and the strength of {111} texture in aluminum thin films [23-28]. However, such relationships for the Cu have not been firmly established and the driving forces which can affect the texture and microstructure transformation during annealing were not clearly identified at present. Since reliability

and performance of interconnects are greatly influenced by specific microstructural features rather than by the average material properties, understanding the effects of microstructure and texture on electroplated Cu damascene interconnect are critical.

The main objectives of this study are: 1) to improve the understanding of the effect of substrate texture and electroplating conditions on texture and surface morphology of the electroplated copper, 2) to understand the effects of line width on textural and microstructural evolution of Cu damascene interconnects, 3) to study the influence of the annealing process on textural and microstructural evolution of Cu damascene interconnects, and 4) to verify the stress contribution to textural and microstructural evolution of Cu through the physical simulation and suggest recommendations to industry for reliable Cu interconnects.

Before trying to understand the influence of texture on the reliability of Cu interconnects, a review of the basics of the texture and failure mechanisms of interconnects is needed. A general review on texture description and the details on the reliability concerns are described in Chapter 2. In this chapter, a brief review on Cu integrated circuit technology and damascene process are also presented. Chapter 3 describes the experimental techniques and the equipments used to characterize texture, microstructure and morphology of specimens. In Chapter 4, the effect of substrate texture and electroplating conditions on texture and surface morphology of Cu electrodeposits is presented. Chapter 5 and 6 show the effects of line width and annealing process on textural and microstructural transformation of Cu interconnects. Stress contribution to the textural and microstructural evolution of Cu was verified through the physical simulation, in Chapter 7. Finally, Chapter 8 presents the conclusions of this investigation, a list of the contribution to original knowledge and future works.

Chapter 2

Literature Review

In this chapter, a brief introduction to texture description will be outlined. Also a brief review of integrated circuit technology and research on Cu damascene interconnects will be presented. The following sections cover the failure modes in metallization, and effects of microstructure and texture on the reliability of interconnects.

2.1. General Description of Texture

Most commonly used materials such as metals, ceramics, and often polymers are aggregates of crystals. The crystallographic orientation of their crystals is generally non-random. Such materials where crystals have preferred orientations are called textured. Texture is developed at all stages of the manufacturing process and the mechanism of texture development is a very complex function of the mechanical and thermal processes as well as of the material structure, phase composition and chemical composition. Texture plays a very important role in understanding the physical and mechanical properties of materials, such as elastic modulus, Poisson's ratio, strength, ductility, toughness, magnetic permeability, and the energy of magnetization [29, 30].

The starting point of all standard x-ray texture analysis is the measurement of the pole figure. The term 'pole' is used to define the normal to a particular crystallographic plane, {hkl}. In the textured specimen, the poles from all grains are not evenly distributed in the specimen reference frame and cluster along certain directions depending on the crystal symmetry and texture. The {hkl} pole figure represents the variation of the {hkl} pole density as a function of the pole orientation within the specimen reference frame. The pole orientation is usually specified by the azimuthal (β) and polar (α) angles of a spherical polar coordinate systems defined in the RD-TD-ND reference frame of the specimen where RD represents the rolling direction, TD is the transverse direction and ND is the normal direction. A pole density distribution is then described as $P\{hkl\}(\alpha, \beta)$. The standard presentation of the pole figure is a stereographic projection of the hemisphere of pole density data onto the RD-TD plane. Figure 2.1a shows how the sheet

specimen is placed in the center of the stereographic sphere. The orientation of a single grain in this sample can be represented by plotting orientation of its three {100} poles at the appropriate positions in relation to the reference directions of the specimens reference frame, as shown in Figure 2.1b. For a polycrystalline sample in this figure, all grains should be considered and all of their respective {100} poles should be plotted. The poles tend to cluster together in certain areas of the pole figure if the material is textured, as shown in Figure 2.1c. Iso-density contour lines connecting the projected data are usually plotted to produce the pole figure as shown in Figure 2.1d.

While the pole figure shows how the chosen crystallographic direction of grains are distributed in the sample reference frame, the inverse pole figure shows how the selected direction in the sample reference frame is distributed in the reference frame of the crystal. Since the properties of many important engineering materials are strongly direction-dependent, the inverse pole figure is very useful in predicting and calculating the average properties of polycrystalline material along a chosen specimen direction. Due to the crystal symmetry, a complete inverse pole figure usually contains many areas where the same information is repeated. For example, there are 24 symmetric sections in the inverse pole figure for cubic system, as shown in Figure 2.2. Therefore, only one section is used usually.

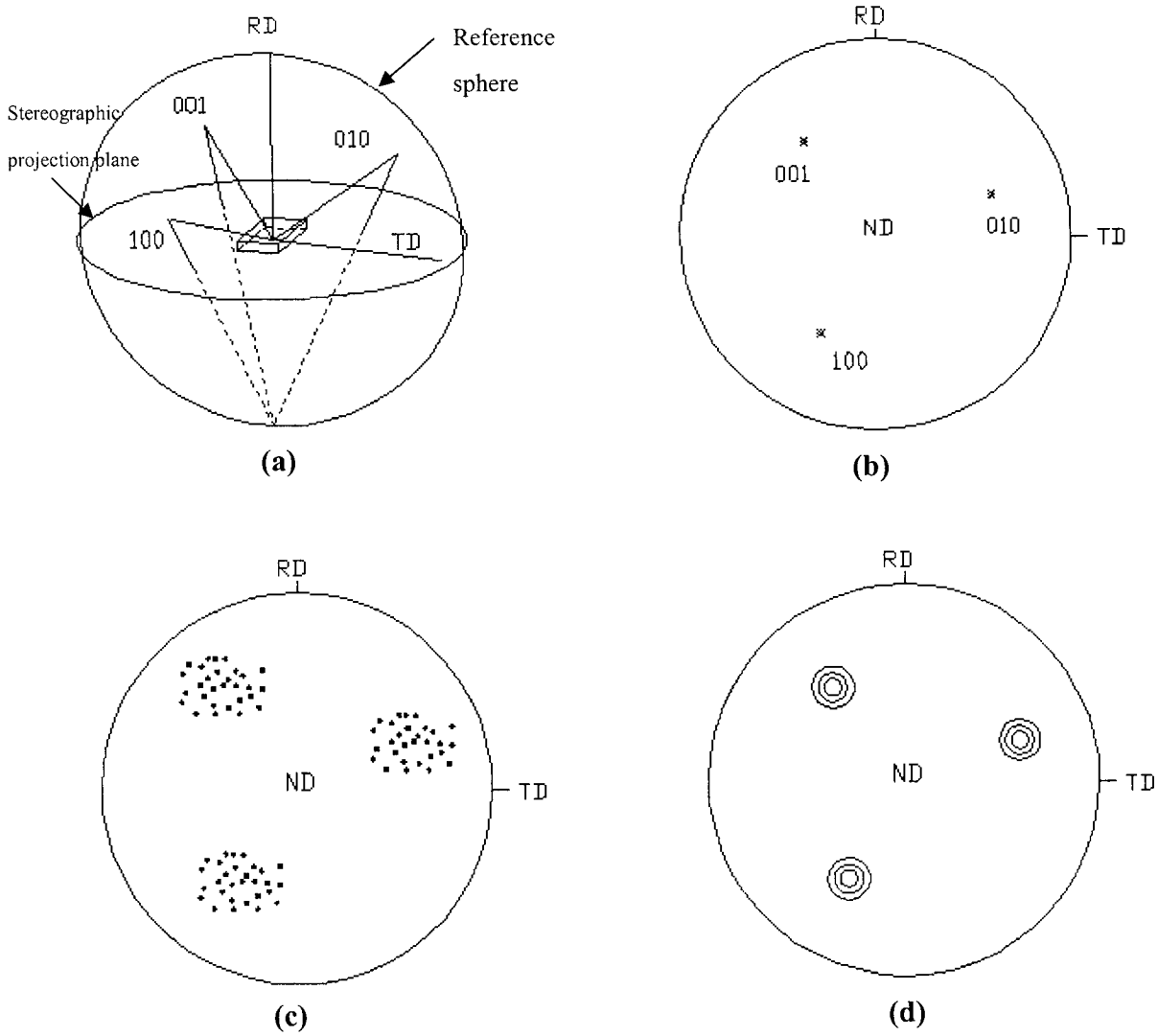


Figure 2.1. The presentation of pole figure: (a) projection sphere and reference frame of the sheet, (b) projection of poles for a single grain, (c) projection of pole from texture grain, (d) pole figure with iso-density contour lines [31].

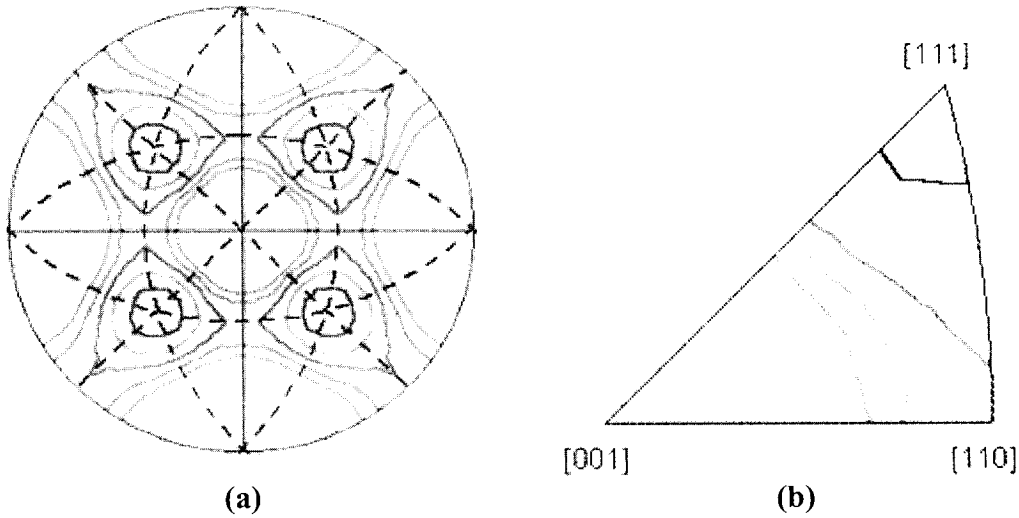


Figure 2.2. Inverse pole figure: (a) a complete inverse pole figure, (b) a partial inverse pole figure.

The fully quantitative method is based on a description of the orientation of crystallite. In order to describe the orientation of individual crystallites, a rotation g, which transforms a sample-fixed coordinate system into a crystal-fixed coordinate system, must be defined, as shown in Figure 2.3. This figure shows both sample-fixed coordinate system and the crystal-fixed coordinate system. In 1755, Euler introduced the "three rotation concept", one of the most widely used methods in describing the orientations of crystals. It is defined by assuming that, initially, the axes of the crystal coordinate system are parallel to those of the sample coordinate system.

The Euler angles are then introduced by describing the rotation of one system around the other. First of all, the crystal coordinate system is rotated around the Z'-axis

through the angle ϕ_1, then around X'-axis through Φ and finally around the Z'-axis again through the angle ϕ_2 as illustrated in Figure 2.4.

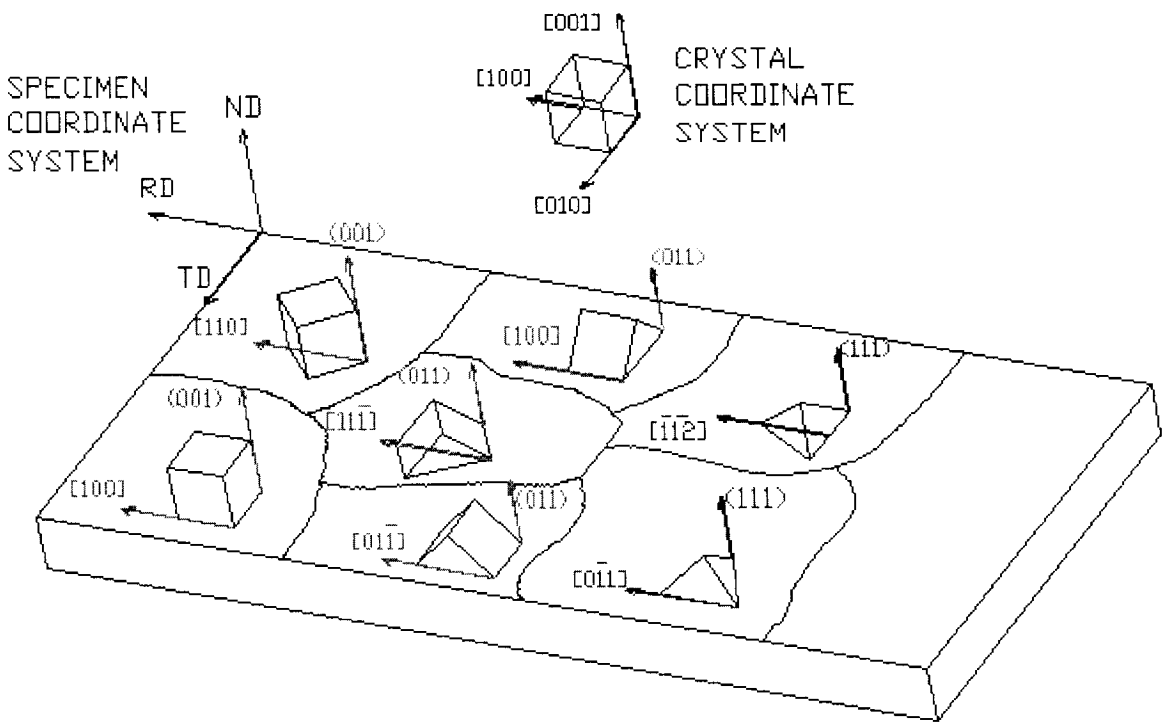


Figure 2.3. Schematic diagram showing the specimen and crystal coordinate systems and different orientations of grains in textured sheet.

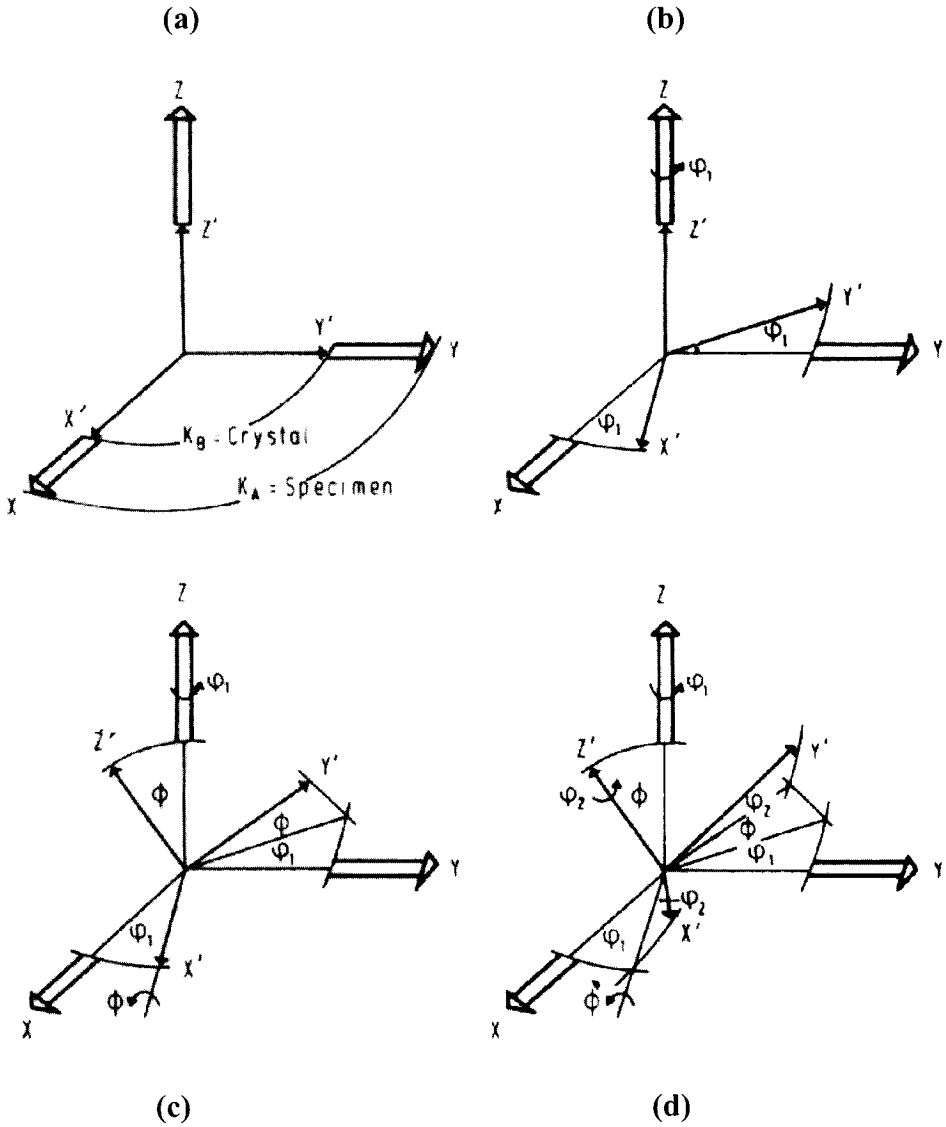


Figure 2.4. The definition of the Euler angle ϕ_1, Φ, ϕ_2: (a) the crystal coordinate system (X'Y'Z') lies parallel to the sample coordinate system (XYZ), (b) the crystal coordinate system is rotated around the Z' axis through the angle ϕ_1, (c) the crystal coordinate system is rotated around the X' axis through the angle Φ, (d) the crystal coordinate system is rotated around the Z' axis through the angle ϕ_2 [32].

The rotation g is thus represented by the three Eulerian angles ϕ_1, Φ, ϕ_2.

$$g = \{\varphi_1, \Phi, \varphi_2\} \tag{2.1}$$

All possible ranges of these Euler angles are as follows.

$$0 \le \phi_1 \le 2\pi, \quad 0 \le \Phi \le \pi, \quad 0 \le \phi_2 \le 2\pi$$

Another standard method used to describe texture is the orientation distribution function (ODF). The ODF is a statistical measure of orientation distribution which describes the volume fraction of individual crystallites as a function of their orientation g. The ODF represents the volume fraction of crystallites in the material, dV/V, which lies with a spread of dg for the orientation g, as in Equation (2.2) and (2.3).

$$\frac{dV}{V} = f(g)dg \tag{2.2}$$

$$dg = \frac{1}{8\pi^2} \sin\Phi \, d\varphi_1 \, d\Phi \, d\varphi_2 \tag{2.3}$$

The ODF is also represented by one-dimensional plots of f(g) along certain lines, called fibers, in the Euler space. The alpha fiber contains orientations where $\varphi_1 = 0°$ and $\varphi_2 = 45°$, while Φ changes from 0° to 90°. These orientations have their (110) crystallite directions parallel to the rolling direction (RD). The gamma fiber contains orientations where $\Phi \cong 55°$, $\varphi_2 = 45°$and φ_1 goes from 0° to 90°. Orientation along the gamma fiber

have {111} planes parallel to the sheet of the plane. The eta fiber contains the orientations where $\varphi_1 = 0°$, $\varphi_2 = 0°$ for the range of $0° < \Phi < 90°$. The (100) directions along the eta fiber are parallel to the rolling direction. The $\varphi_1 = 0°$ and $\varphi_2 = 0°$ sections of the ODF are generally used to describe these fibers and some other important orientations. Figure 2.5 shows α, γ, and η fibers and some low index orientations on the $\varphi_1 = 0°$and $\varphi_2 = 45°$ sections of the ODF.

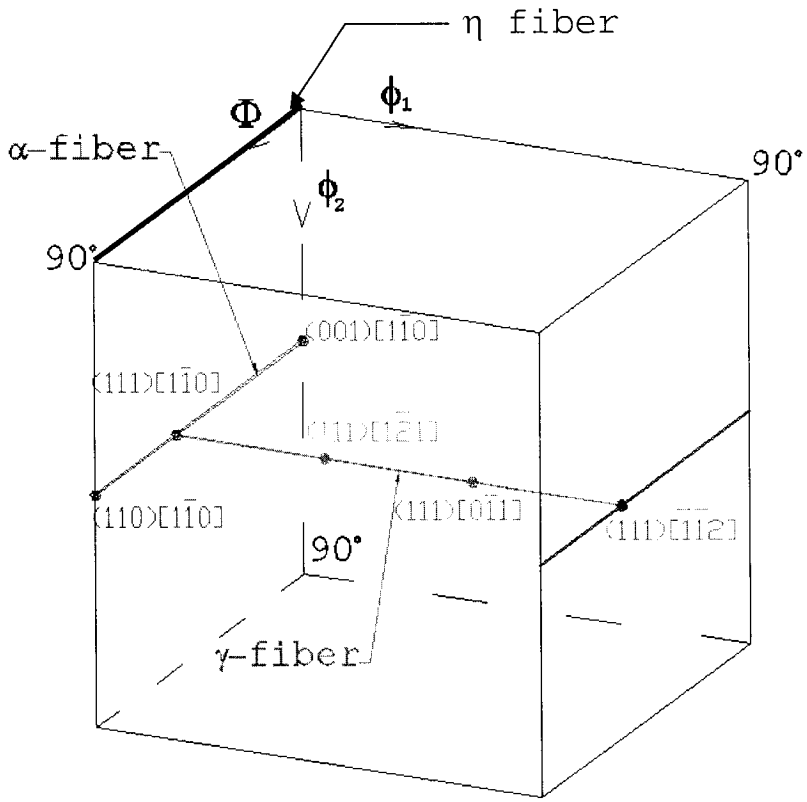


Figure 2.5. Three dimensional view of Euler space with locations of some important ideal orientations and fibers (Bunge notation).

2.2. Copper Metallization in the Integrated Circuit

2.2.1. Integrated Circuit Technology

Since the transistor was invented in 1947, the semiconductor industry keeps trying to create more powerful CPU (Central Processing Unit) and IC (Integrated Circuit) chips, as shown in Figure 2.6. The speed of individual devices is increased mainly through the reduction of the minimum size of various features of the devices. Along with this goes an increase in device density on the chip. Another area of improvement is related to connecting individual devices into circuits using increasingly complex interconnects. These chips now have multilayer structures made up of several levels of interconnects which are metal wirings separated by an interlayer dielectric (ILD), as shown in Figure 2.7.

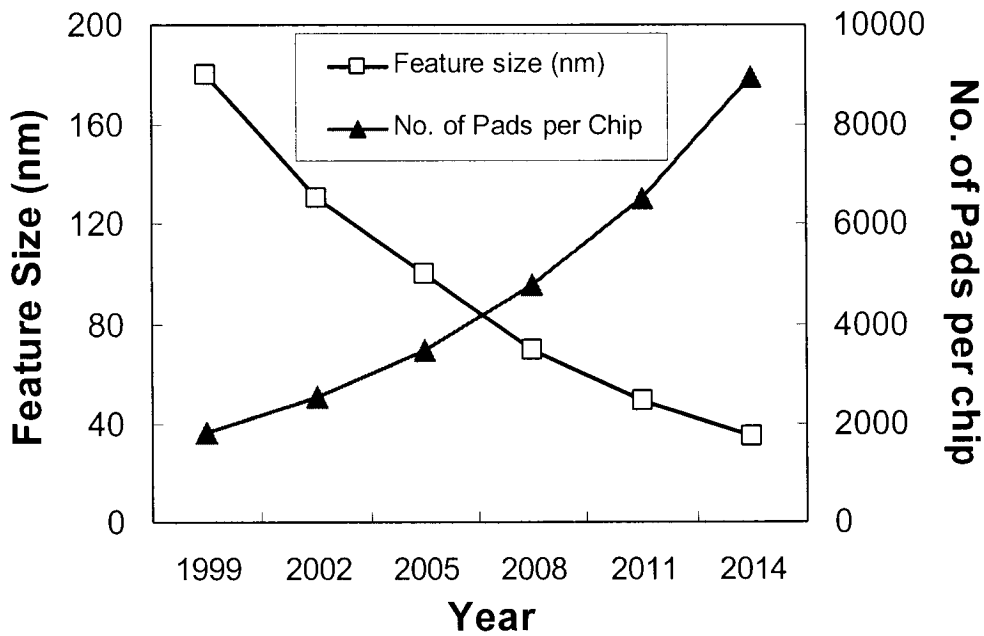
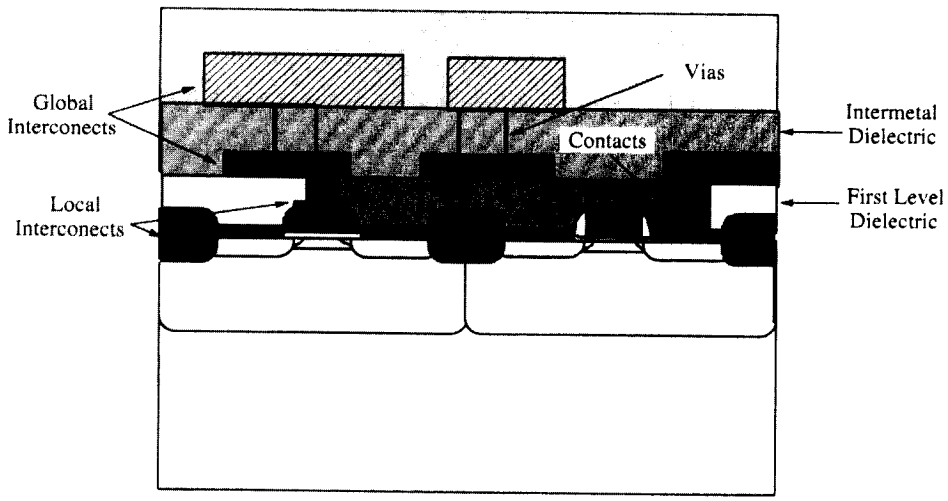
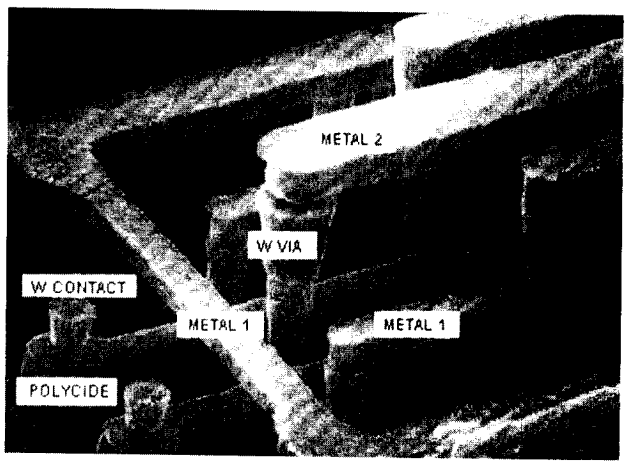


Figure 2.6. A trend of the semiconductor industry from SIA roadmap [33].



(a)



(b)

Figure 2.7. The structure of interconnects in the circuit chip: (a) schematic cross section of chips, showing interconnects, contacts and vias, separated by dielectric layers, (b) SEM micrograph of an IBM circuit showing the interconnects with the dielectric layers etched away [2].

Interconnects can be either local or global. In general, local interconnects are the first, or lowest, level of interconnects. They usually connect gates, sources, and drains in MOS (Metal-Oxide Semiconductor) technology, and emitters, bases, and collectors in bipolar technology. Local interconnects can tolerate higher resistivities than global interconnects since they are not very long. But they must also, in most cases, be able to withstand higher processing temperatures because they are deposited earlier in the process than global interconnects. Global interconnects are generally all the interconnect levels above the local interconnect level. They often cover large distances between different devices and different parts of the chip and therefore are always low-resistance metals.

In most cases, the sophisticated device and circuit design help the efforts in the improvement of performance since the exact nature of the relationship between the individual device and interconnect performance depends on details of the circuit architecture. However, it is now generally recognized that the overall circuit performance is going to be dominated by the efficiency with which devices are connected rather than by the speed of the individual devices. From the materials point of view, a better efficiency of the interconnects may be achieved with various combinations for the metal and the interlayer dielectric (ILD). It is now becoming apparent that a major component of improved interconnect performance is related to replacement of aluminum with copper.

Copper and copper alloys constitute one of the major groups of commercial metals. They are widely used because of their excellent electrical and thermal conductivities, ease of fabrication, and good strength and fatigue resistance. In computer chip manufacturing industry, copper is the main on-chip conductor for all types of integrated circuits (ICs). Compared to aluminum, which has been used almost exclusively as the main interconnect

material until recently, copper has a lower resistance (<2 μΩ-cm as compared to >3 μΩ-cm for aluminum alloys). This lower resistance is critical in high-performance microprocessors and RAMs (random access memory), since it enables signals to move faster by reducing the so-called RC (resistance and capacitance) time delay [4-8].

The advantages of copper are so important that many see it being adopted for most types of ICs. For example, copper enables a reduction in not only the resistance, but the capacitance as well, since the metal lines can be made thinner. This helps reduce the amount of power consumption, which makes it attractive for use in battery-powered applications, such as notebook computers. Another major benefit of copper is that it has superior resistance to electromigration, a common reliability problem in aluminum lines. This means that copper can handle higher power densities, such as those found in high-power transistors, which broadens its application to a whole new range of analog devices. A detailed explanation of electromigration induced failure will be presented in the failure modes of copper interconnects. A third benefit of copper is that it can actually lead to lower manufacturing costs when compared to aluminum. This can be established by one of two ways. First, because copper is difficult to etch, a new strategy called "damascene" patterning was needed to form the interconnect lines shown in Figure 2.8. This damascene process requires 20-30% fewer steps than traditional subtractive patterning. The second way copper can reduce costs is that because smaller lines can be used to carry the same amount of current, a tighter packing density can be achieved per level. This means that fewer levels of metal are needed, leading to significantly reduced manufacturing costs, as shown in Figure 2.9.

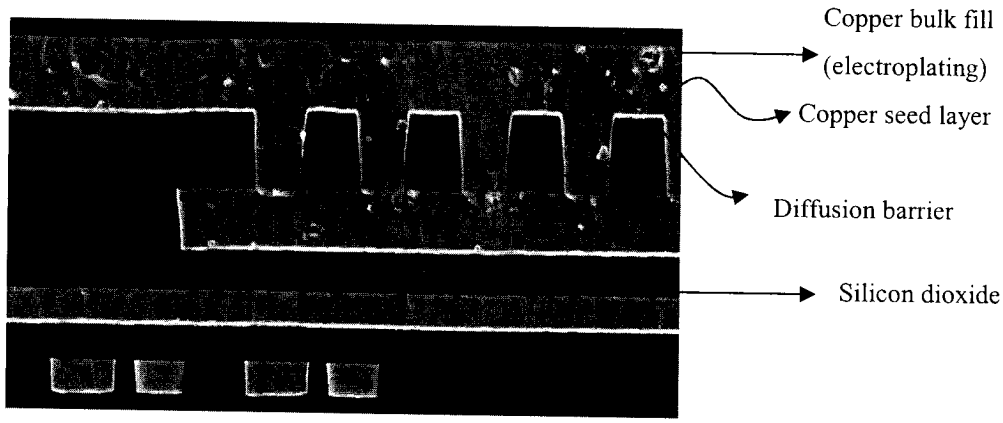


Figure 2.8. The cross-sectional structure of Copper damascene interconnects [34].

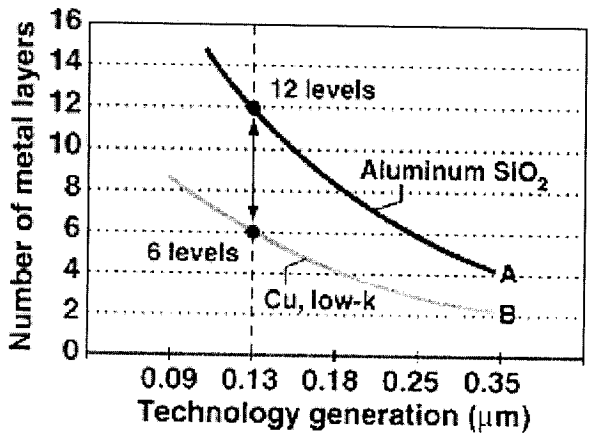


Figure 2.9. The reducing complexity of IC chips manufacturing: the number of metal levels can potentially be reduced – reducing cost [4].

In spite of all advantages of copper, there are several problems that must be solved. One is that copper is a known fast diffuser and can poison a device, creating a failure, once it gets into the active area (i.e., source/drain/gate region of the transistor) [6]. This

has required the development of new and advanced diffusion barriers to eliminate this threat, as well as different fabrication layouts to isolate the copper production part of the line from the rest of manufacturing. Another problem is that copper patterning requires the implementation of an entirely new manufacturing technique, so called damascene process. In this process the bulk of the copper would not be deposited by conventional methods (such as PVD or CVD), but by electroplating.

2.2.2. Damascene Process of Copper

As mentioned earlier, the reason why Cu damascene process should be introduced is that there are difficulties in patterning of copper. Wet etching is not useful for patterning sub-micron structures due to its isotropic nature. Moreover, reactive ion etching (RIE) of copper is also not practical because of the lack of volatile copper's compounds at low temperature [10]. Unlike conventional patterning methods where a metal layer is first deposited and then unwanted metal is etched away, leaving the desired pattern of wires or vias, damascene patterning involves the same number of steps, but in the reverse order. The pattern of wires or vias is first formed by etching the oxide (Figure 2.10). After this, a diffusion barrier is deposited, consisting of tantalum/titanium with light amounts of nitrogen doping or a full tantalum/titanium nitride compound. These will be deposited by ionized physical vapor deposition (PVD), which produces thin, conformal, continuous titanium/titanium-based barriers (Figure 2.10b), and copper seed layers inside small structures. An ideal barrier layer should have a dense, amorphous microstructure and a smooth surface morphology free of micro-defects. The dense,

amorphous microstructure of the Ta/TiN_x film makes it an excellent barrier since there are no fast diffusion paths for Cu. In order to deposit copper on the surface of a wafer by electroplating, it is first necessary to cover the surface with a seed layer, whose function is to conduct the current from a contact at the wafer edge to all points on the wafer where a deposit is desired (Figure 2.10c). Until now, it is known that the best material for the seed layer is copper itself [35-37]. Then, the trench will be filled with copper by electroplating which will be explained in Chapter 2.2.3 (Figure 2.10d). The plated copper covers the entire surface; excess copper must be removed by a planarization step such as chemical-mechanical polishing (CMP). Damascene electroplating is ideally suited for the fabrication of interconnect structures, since it allows inlaying of metal simultaneously in via holes and overlying line trenches by a process called dual damascene [10]. Further, it is compatible with the requirement for a barrier layer between the seed layer and the insulator; the barrier prevents interaction between the metal and the insulator [38, 39]. Next, copper will be planarized with a chemical-mechanical polishing (CMP) step (Figure 2.10e). The main challenge here is to obtain the same polishing rate on the tantalum/titanium, which is a hard refractory metal, and the copper, which is comparatively soft. During this process, insufficient adhesion between layers can cause layer peeling. After this, a silicon nitride (Si_3N_4) layer will cap off the copper, keeping it totally encapsulated (Figure 2.10f).

During processing, plated copper is subjected to at least one annealing during polyimide curing at 200°C or 400°C; recrystallization and significant grain growth are subsequently observed in the microstructure.

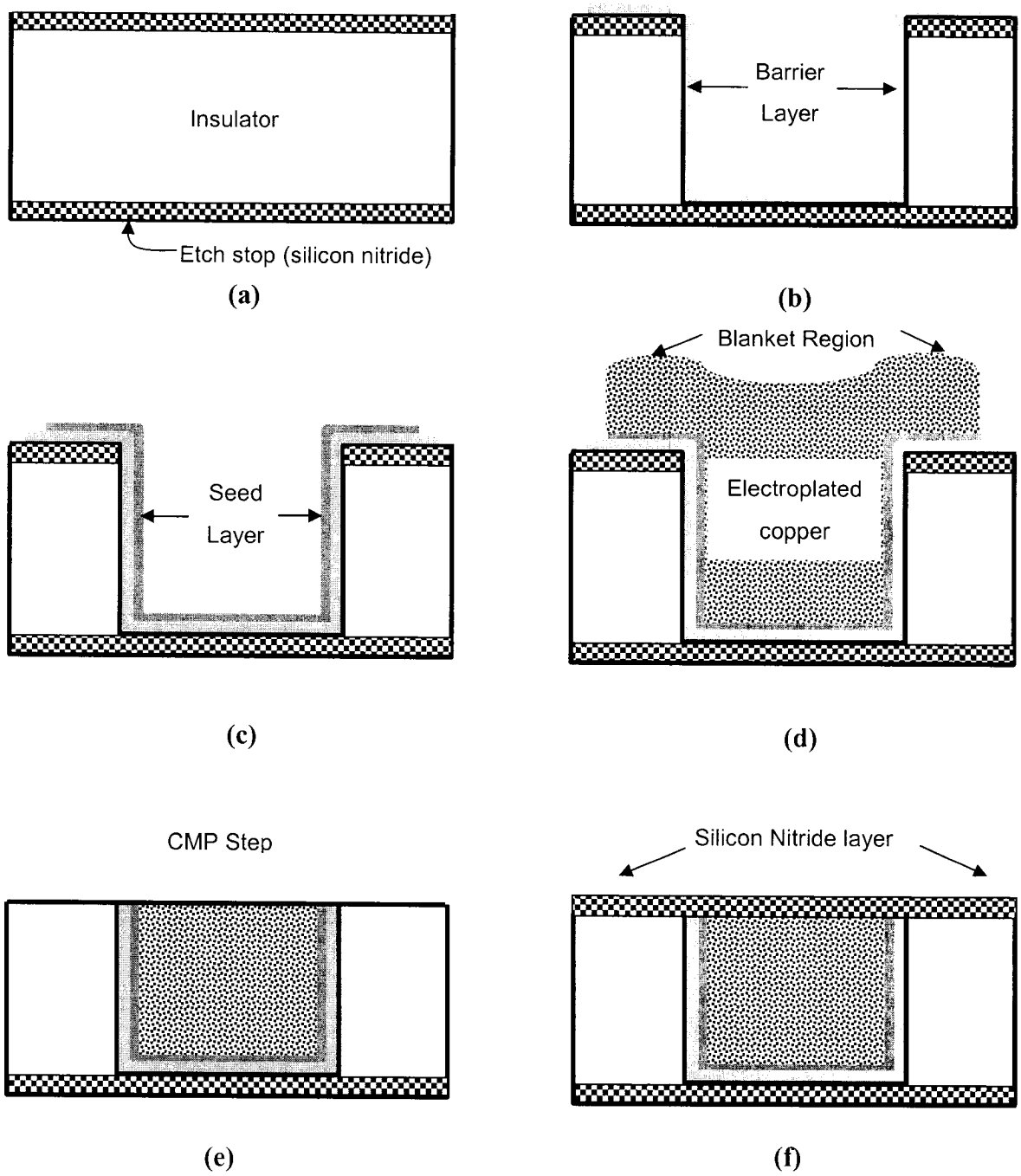


Figure 2.10. Process steps for the fabrication of line level by the damascene approach: (a) insulator deposition, (b) barrier layer deposition, (c) seed layer deposition, (d) copper electroplating, (e) planarization step (CMP), (f) silicon nitride layer deposition.

2.2.3. Electroplating of Copper

Electroplating is a relatively simple process which does not require ultrahigh vacuum, nor does it require complex heating. The wafer is connected to the cathode and immersed in a solution containing cupric ions and the anode. The amount of copper deposited is dependent on the current delivered. As with other types of deposition, the success of the process is measured by factors such as film morphology, step coverage, filling capability, and uniformity across the wafer [40-42].

Electrodeposition of metal is performed by immersing a conductive surface in a solution containing ions of the metal to be deposited. The surface is electrically connected to an external power supply, and current is passed through the surface into the solution. This causes reaction of metal ions M^{z-} with electrons e^- to form metal (M), as shown in Equation 2.1.

$$M^{z+}_{solution} + ze \rightarrow M_{lattice} \qquad (2.1)$$

In the case of electrodeposition of copper onto a silicon wafer, the wafer is typically coated with a thin conductive layer of copper (seed layer) by PVD and immersed in a solution containing cupric ions. Electrical contact is made to the seed layer, and current is passed such that the reaction (Equation 2.2) occurs at the wafer surface, as shown in Figure 2.11.

$$\mathbf{Cu^{2+} + 2e^- \rightarrow Cu\ (O)} \qquad (2.2)$$

The wafer, electrically connected so that metal ions are reduced to metal atoms, is referred to as the cathode. Another electrically active surface, known as the anode, is

present in the conductive solution to complete the electrical circuit. At the anode, an oxidation reaction occurs that balances the current flow at the cathode, thus maintaining electrical neutrality in the solution. In the case of copper plating, all cupric ions removed from solution at the wafer cathode are replaced by dissolution from a solid copper anode.

In the absence of any secondary reaction, the current delivered to a conductive surface during electroplating is directly proportional to the quantity of metal deposited (Faraday's law of electrolysis). Using this relationship, the mass deposited can be readily controlled through variations of plating current and time.

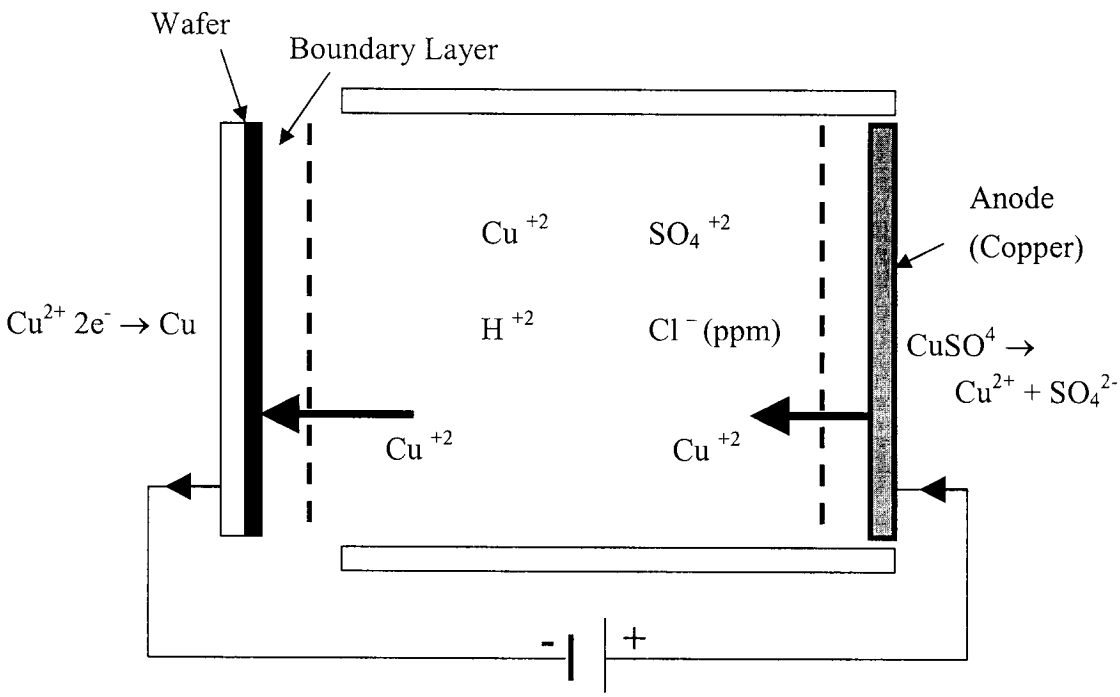


Figure 2.11. Schematic of electrochemical plating (ECP) cell for Cu deposition.

With no applied potential or current flow across the interface between a metal and a solution, an equilibrium potential exists between the two. Once the potential is shifted by an external power source away from the equilibrium potential, the current will be driven across the interface. Under conditions typical of most plating processes, this current flow is approximated by an exponential relationship known as the Tafel equation.

Figure 2.12 shows a current-potential curve typical of a copper deposition process. As the potential is scanned from the equilibrium potential to more negative values, the current increases in an exponential manner (Tafel region) where the overall deposition rate is determined largely by the charge transfer or reaction rate kinetics at the cathode. This strong dependence of the current upon potential results in the need for plating cell designs that yield uniform potentials across the wafer surface.

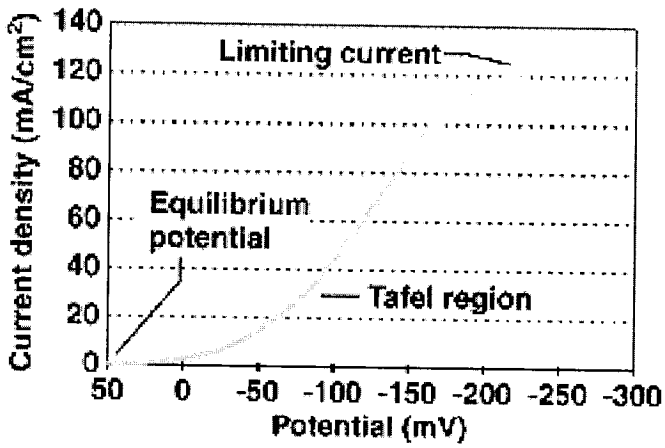


Figure 2.12. A current-potential curve typical of a copper electroplating process [4].

As the potential continues to increase, mass transfer effects become predominant, and a limiting current plateau is reached. As a result of this, the species reacting at the cathode (Cu^{2+}) no longer reach the interface at a rate sufficient to sustain the high rate of reaction. Generally, plating processes are operated at currents no greater than 30-50% of the limiting current in order to avoid undesirable deposit characteristics.

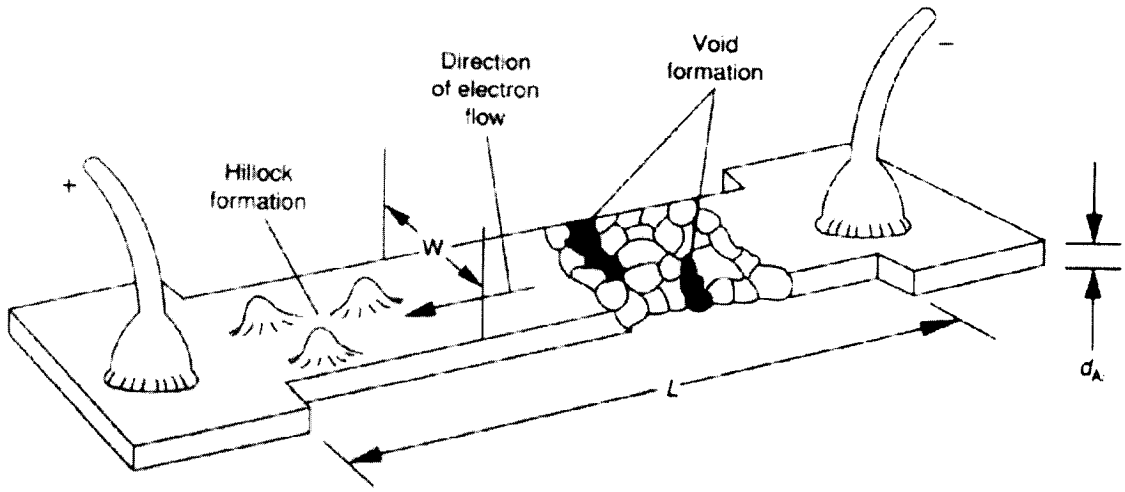
To ensure that the rate of mass transfer of electroactive species to the interface is large compared to the reaction rate and uniform across the wafer surface, the rates of migration, diffusion and convection must be understood and controlled. Convection is the most important mode of mass transfer and can vary from stagnant to laminar or turbulent flow. It includes impinging flow caused by solution pumping, flows that are due to substrate movement and flows resulting from density variations. Electroplating can be carried out using a constant current, a constant voltage, or variable waveforms of current or voltage. Using a constant current, accurate control of the mass of deposited metal is easily obtained. The plating at the constant voltage and using variable waveforms requires more complex equipment and control but can be useful in tailoring specific thickness distributions and film properties.

2.3. Failure modes of copper interconnects

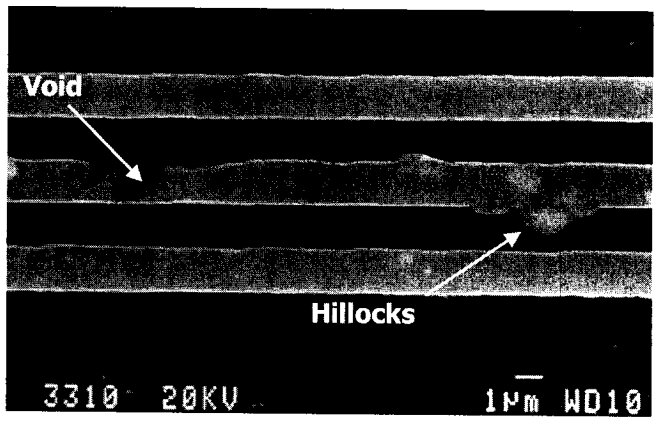
2.3.1. Electromigration

Electromigration is a phenomenon where moving electrons that constitute the electrical current in the interconnect collide with the stationary atoms of the interconnect (whether Al or Cu) and make them move in the direction of the electron flow, as shown in Figure 2.13. The effect of thousands of electrons colliding with a single atom is similar to the moving air molecules of the wind pushing a sailing boat. In fact, it is customary to talk loosely of an 'electron wind' in describing electromigration. If the net flow of atoms in the interconnect becomes unbalanced, particularly at a physical defect site, either pileup or depletion of material can lead to failure. The defects are very strongly dependent on the way the material has been deposited and patterned. For the same metal, it is possible to change the electromigration failure time by several orders of magnitude due to differences in processing [43-50].

Cu atoms are heavier and more tightly bound together, so they resist electromigration better than Al. The direct comparison of these two metallizations in Figure 2.14 clearly shows that the electromigration resistance of Cu is far superior to that of Al(Cu). However, electromigration failure is due to moving atoms interacting with defects, so a Cu line with defects can fail earlier than an Al line without defects.



(a)



(b)

Figure 2.13. Electromigration failure: (a) a schematic diagram [51], (b) voids and hillocks formation at Al interconnects [23].

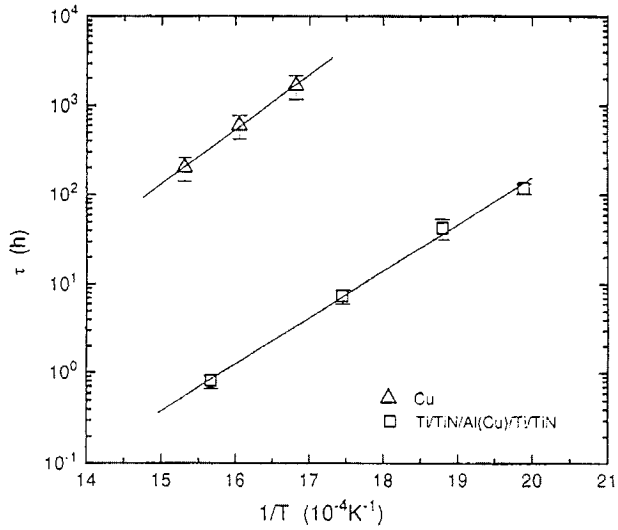


Figure 2.14. Plot of log (τ) vs. *1/T* for Cu and Al(Cu): τ is the mean lifetime [52].

2.3.2. Failure during Processing

The foremost requirement for success of the plating process is its ability to fill trenches, vias, and their combinations completely, without any voids or seams. How plating makes it possible to obtain void-free and seamless deposits is the key point in many studies.

Successful integration of electroplated copper damascene structures requires two critical metallization steps. First, it requires a barrier layer since Cu diffuses readily into oxides and low-k dielectrics, causing line-to-line leakage, and it can react with Si at temperatures below 200°C. The barrier layer must prevent Cu diffusion, exhibit low film resistivity, have good adhesion to both dielectrics and Cu, and be CMP compatible. Also, the barrier layer must be conformal and continuous to fully encapsulate the Cu lines with

a layer as thin as possible. Due to the higher resistivity of the barrier material, its thickness should be minimized to allow for Cu to occupy the maximum cross-sectional area. Following the barrier layer, a thin, continuous Cu seed layer promotes adhesion and facilitates the subsequent growth of the bulk copper fill by electroplating. The seed layer carries current along the contours of the patterned damascene structure, serving as the nucleation layer. The seed layer should be thin, smooth, and continuous to ensure void-free fill. In addition, the Cu seed layer should be highly pure so as not to compromise the effective resistivity of the filled copper interconnects structure. Sequential processing enhances the adhesion between the barrier and seed layer, and also produces a highly oriented Cu seed layer that influences the growth of the subsequent electroplated copper interconnect.

The filling trenches and vias with Cu without creating a void or seam is another challenge in copper damascene process, as shown in Figure 2.15. For defect-free filling, a higher deposition rate in the bottom than on the sides of the feature is desired. To improve deposit properties, additives-compounds added in Cu plating solutions are consumed on the wafer surface and suppress the kinetics of Cu deposition. Since interior locations of trenches are less accessible to additives, less suppression of the reaction kinetics occurs there, causing higher deposition rates [10]. This superconformal process seems to be a unique property of electroplating, which is therefore a particularly suitable technology for the fabrication of Cu chip interconnections, as shown in Figure 2.16.

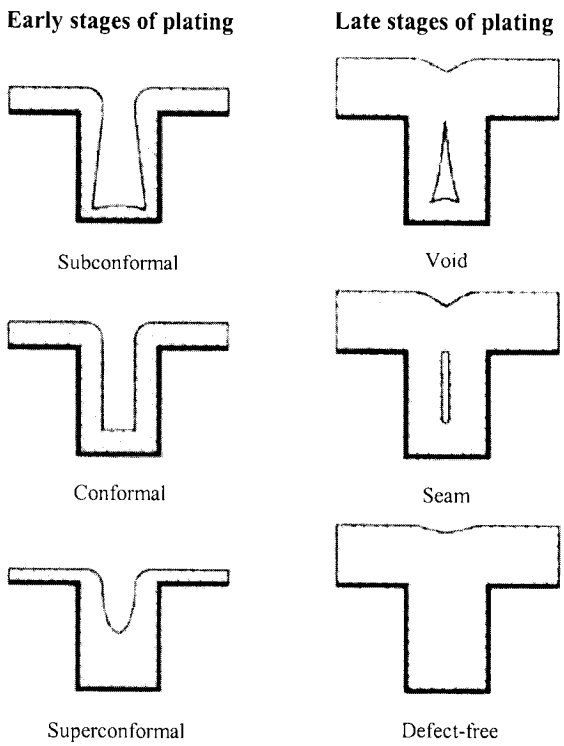


Figure 2.15. Types of profile evolution in damascene plating [10].

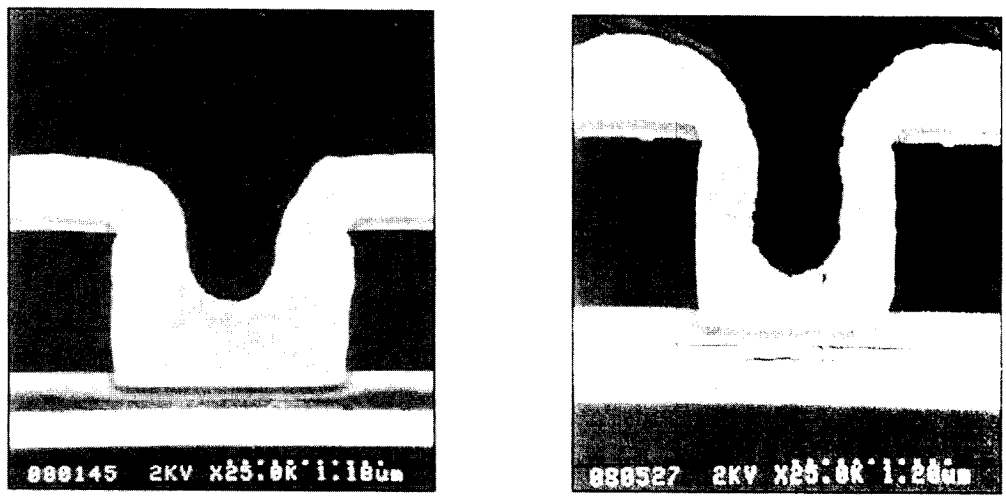


Figure 2.16. Cross section of partially filled lines showing the profiles of electroplated copper: (a) superconformal filling, (b) edge-rounding only [10].

2.4. Effects of Microstructure and Texture on the Reliability of Interconnects

Microstructure and texture of Cu films can affect interconnect reliability such as electromigration resistance. Therefore, it is necessary to control the microstructure and texture to guarantee a reliable Cu interconnect, as line dimensions reach the 90 nm range. Accordingly, it is important to know the phenomena and the mechanism of microstructure and texture evolution during fabrication. There are several papers discussing the effects of microstructure and texture on the reliability of Al and Cu interconnects [53-57], however, this problem is still not well understood.

Grain size and texture are found to be critical factors that affect interconnects lifetime in Al alloys where for long time to failure, large grains with strong {111} texture are desirable (Figure 2.17). Especially, the strong {111} texture minimizes the presence of high-angle grain boundaries along the interconnect line, thus minimizing the diffusion path and electromigration mass transport. Although it is very tempting to extend the results of Al alloys to Cu interconnects, Cu is very different from Al in many respects. With Cu thin films, the {111} texture is not always strong, and the presence of {200} or {220} oriented grains and twins are frequently observed. Also, the grain size distribution is often bimodal, with the evidence of abnormal grain growth occurring during annealing, during which some grains grow substantially larger than the average grain size. Copper alloys have shown some unusual effects including dramatic grain growth and texture changes upon annealing at temperatures well below 400 °C, as shown in Figure 2.18. An abundance of twin boundaries (parallel, high-contrast regions) visible in the larger grains

is indicative of the low stacking fault energy in Cu. They also point to the involvement of twinning as a factor in the grain growth process and evolution of texture. This phenomenon will be discussed later in this study. However, it was found that the electromigration induced failure is still strongly affected by texture and deposition methods which can affect grain size (Figure 2.19).

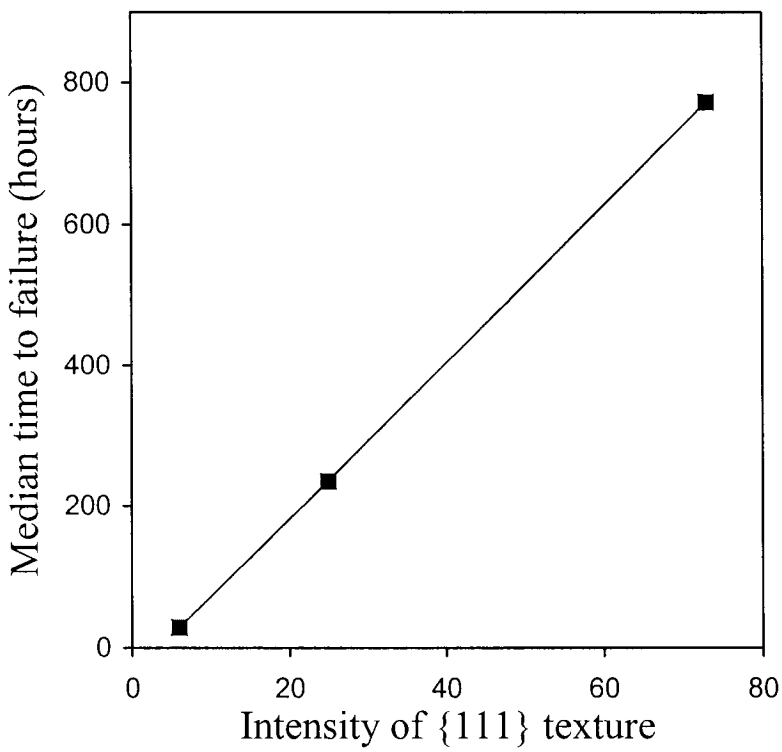
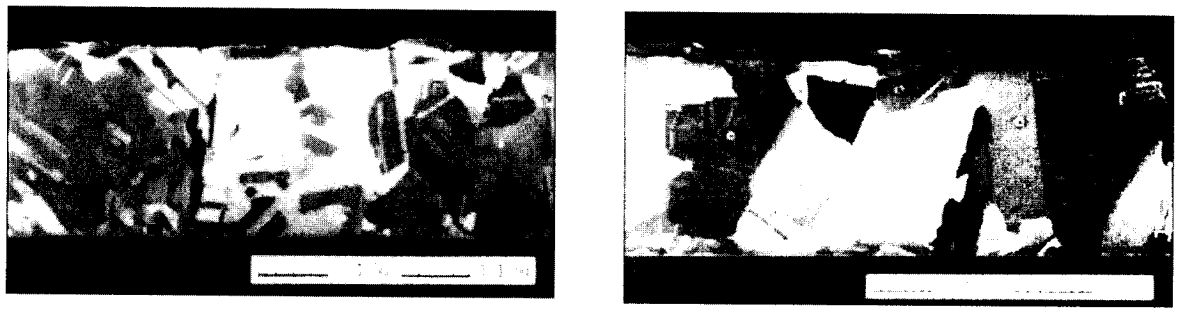
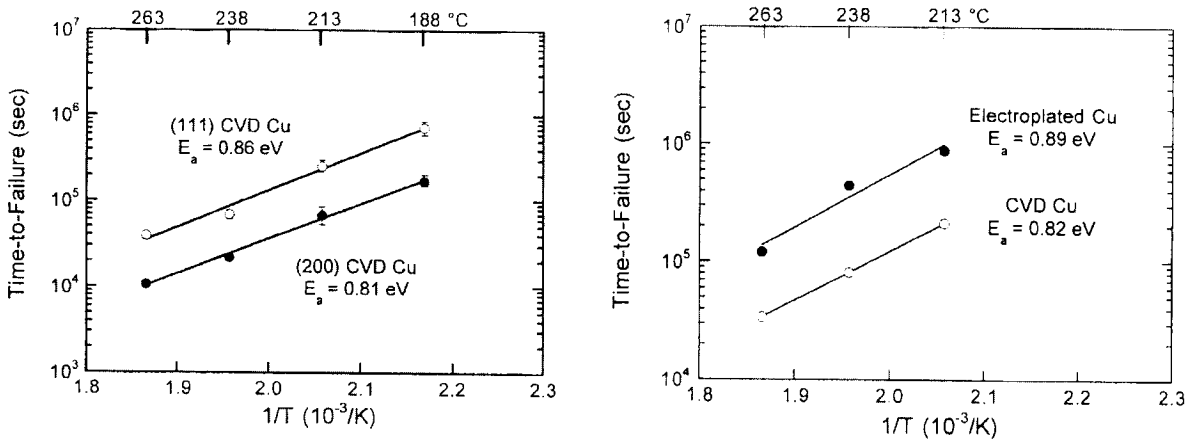


Figure 2.17. Intensity of {111} texture as a function of median time-to-failure in Al interconnects [23].



(a) (b)

Figure 2.18. Focused ion beam (FIB) cross sections of plated copper lines showing characteristic microstructure: (a) as plated, (b) after a two stage 400°C annealing [16].



(a) (b)

Figure 2.19. The influence of texture and deposition methods on electromigration induced failure in the Cu interconnects: (a) texture, (b) deposition methods [56].

The texture of the interconnect line is complicated by the fact that the nucleation during metal deposition occurs on the sidewalls and the bottom of the interconnect trench, rather than only on the bottom as in conventionally fabricated Al lines. As the aspect ratio (ratio between depth and width of the trench) exceeds 1:1, the role of the sidewalls is expected to become increasingly important in defining the microstructure and texture of the interconnect line.

In order to see the development of texture and microstructure after copper deposition, Vanasupa *et al.* [57] analyzed the texture of electroplated Cu lines with Ta and TiN barrier layers using x-ray pole figures and electron backscatter diffraction (EBSD) techniques. In this investigation, the strongest {111} texture of the electroplated Cu in both TiN/no-anneal and Ta/anneal copper electroplated specimens is found on the blanket regions, as shown in Figure 2.20.

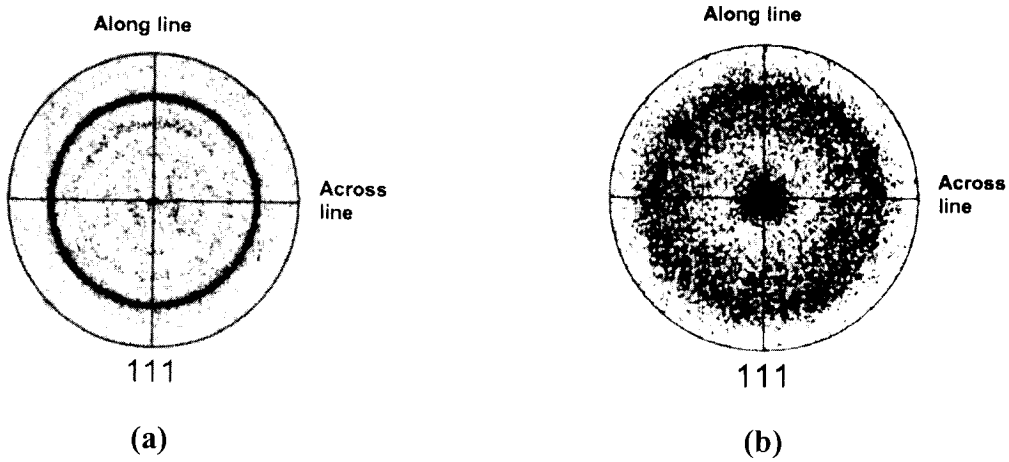


Figure 2.20. Stereographic projection of the (111) pole figure: (a) Ta/anneal electroplated copper, (b) TiN/no-anneal electroplated copper [57].

There is also a lower volume fraction of randomly oriented (111) poles resulting from the Ta/anneal treatment (5%) compared to the TiN/no-anneal treatment (27%). These results are consistent with another study that showed a strong {111} fiber texture on a Ta barrier layer and a weak texture on a chemical vapor deposited (CVD) TiN barrier layer [56]. It is suspected that the high degree of texture on the Ta/anneal samples can be attributed to a combination of (or interaction between) the Ta barrier layer and the post-electroplating anneal. Cu deposited by electroplating forms epitaxy, suggesting that the Cu seed may be strongly textured in the Ta/anneal sample. Previous studies have shown that strong textures can be inherited from barrier layers and developed further during post-deposition annealing [36].

Chapter 3

Experimental Methodology

To understand the texture, microstructure and surface morphology of investigated Cu samples, various methods and equipments are used in this study. The x-ray diffraction (XRD) technique is used to measure the sample texture. For grain boundary character distribution (GBCD) measurements and the investigation of the grain size and grain orientation, the electron backscattered diffraction (EBSD) technique was used to generate orientation images. A fundamental difference between both techniques is that the x-ray technique collects information from a relatively large scan area and the entire thickness of the thin film, whereas EBSD technique covers a small scan area and receives backscattered electrons from the top 10-50 nm, due to the limited depth of the penetration of electrons [11]. For the analysis of surface morphology, atomic force microscopy (AFM) was used. The stress distribution is simulated using finite element model (FEM) to understand the contribution of stress distribution to textural and microstructural evolution in the Cu interconnects after annealing.

3.1. X-Ray Diffraction Technique (XRD)

In this study, x-ray diffraction techniques were used to study the crystallographic structure of copper. The Bragg law (equation 3.1) describes the conditions required for diffraction to occur in crystalline materials.

$$n\lambda = 2d_{\{hkl\}} \sin \theta_B \qquad (3.1)$$

where n is the order of reflection; it may take on any integer number consistent with $\sin \theta$ not exceeding unity and is equal to the number of wavelengths in the path difference between ray scattered by adjacent planes, λ is the x-ray wavelength, $d_{\{hkl\}}$ is the interplanar spacing of the diffracting plane and θ_B is the diffracting angle. The diffracted intensity, $I_{\{hkl\}}$,depends on the volume of crystallites satisfying the Bragg law, which are illuminated by the x-ray beam and many other structural and geometrical factors.

Angular dispersive diffractometry measures the variation of scattered intensity as a function of the diffraction angle, θ_B, for a fixed x-ray wavelength; in this case, the diffraction maxima occur at well-defined angles for each diffraction plane, as shown in Figure 3.1. A specimen C is located on the table H, which can be rotated about an axis O perpendicular to the plane of the drawing. The x-ray emerging from the x-ray source, S; diverge from this source and are diffracted by the specimen to form a convergent diffracted beam that comes to a focus at the slit F and then enters the counter G. A and B are divergence and receiving slit respectively, which define and collimate the incident and diffracted beam. The receiving slit and counter are located on the carriage E, which can be rotated about the axis O and whose angular position 2θ can be read on the graduated scale K. The supports E and H are mechanically coupled so that a rotation of the

specimen through half of 2θ degrees. This coupling ensures that the angles of incidence on, and reflection from, the flat specimen will always be equal to one another and equal to half the total angle of diffraction.

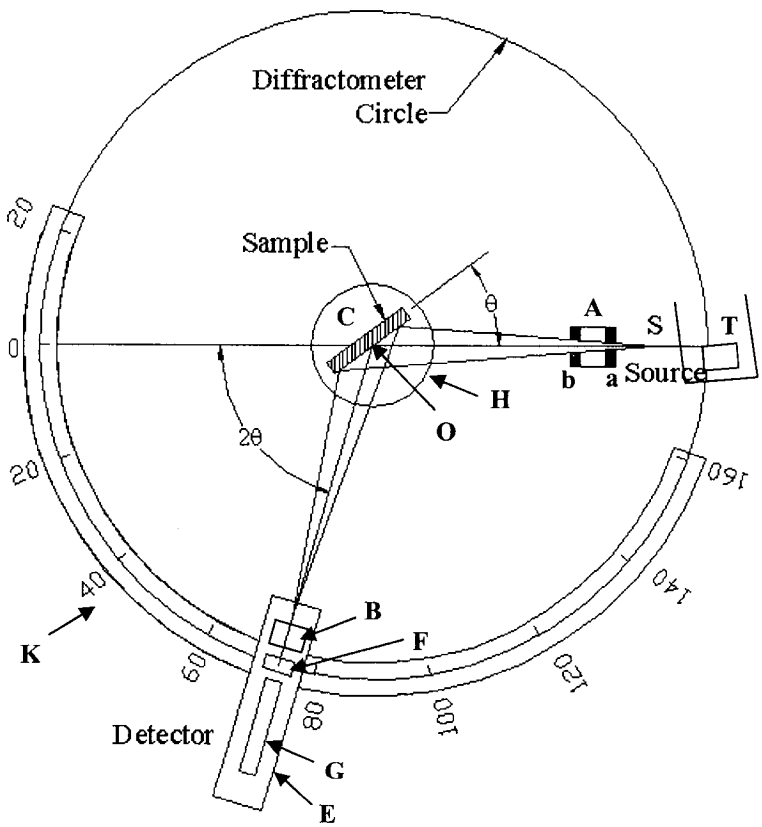


Figure 3.1. Schematic of x-ray diffractometer [29].

In textured materials, as the specimen is tilted or rotated with respect to the incident and diffracted beams, the volume of the crystallites satisfying Bragg law changes. Figure 3.2 presents schematic diagrams for a vertical-axis texture goniometer, in which the four rotation axes, $\hat{\Theta}_2$, $\hat{\Theta}_1$, $\hat{\chi}$ and $\hat{\eta}$, are defined; the scattering plane, defined by the incident ($\hat{i}_i$) and diffracted ($\hat{i}_d$) beams, is always horizontal in this type of goniometer. The $\hat{\Theta}_2$ rotation axis is perpendicular to the scattering plane and rotates the detector to select the diffracting plane of the pole figure being measured. The $\hat{\Theta}_1$ axis is coincident with the $\hat{\Theta}_2$ axis, and rotated the Eulerian cradle – the mechanism, which allows the two specimen rotations, η and χ. The $\hat{\eta}$ axis tilts the specimen normal, ND, out of the scattering plane about an axis perpendicular the Eulerian cradle. The axis rotates the specimen about the axis normal to its surface. The four rotations combine to move the detector and specimen such that the pole figures can be measured.

A standard pole figure measurement for the {hkl} family of planes are performed by rotating the $\hat{\Theta}_2$ and $\hat{\Theta}_1$ axis to: $\Theta_2/2 = \Theta_1 = \theta_{B\{hkl\}}$ is the Bragg angle; diffraction data are then acquired by stepping the χ and η rotations in 2.5° or 5° increments through the ranges, $0^\circ \leq \chi \leq 80^\circ$ and $0^\circ \leq \eta \leq 355^\circ$. The diffracted intensity measured at each step is proportional to the volume of crystallites within the specimen that have their poles, $n_{\{hkl\}}$, parallel to the angular bisector of the incident and diffracted beams. The variation of the diffracted intensity from one complete scan can be written as $I_{\{hkl\}}(\alpha, \beta)$, where, α and β are the polar and azimuthal angles describing the orientation of the scattering poles in the RD-TD-ND reference frame of the specimen.

Using this geometry, the diffracted intensity measurements can be processed to obtain direct, quantitative information on the sample texture. However, the diffracted intensity measurement is not an absolute measure of the specimen's texture because it contains systematic errors and has to be corrected and normalized. Typical systematic errors are caused by background and absorption variation and defocusing effects. In standard texture measurements, the background and defocusing effects vary with the specimen tilt angle, and are corrected using measurements made on a randomly-oriented specimen of the same chemical composition and density; theoretical corrections are used to correct absorption effects. After the error corrections, the intensities are normalized using the integrated intensity of the entire pole figure. The correction and normalization produces values, $P_{\{hkl\}}(\alpha,\beta)$, in the traditional 'times-random' unit of the pole figure. The pole densities are the basic, quantitative measure of textural information and can be used to calculate coefficients of the ODF using a number of different methods.

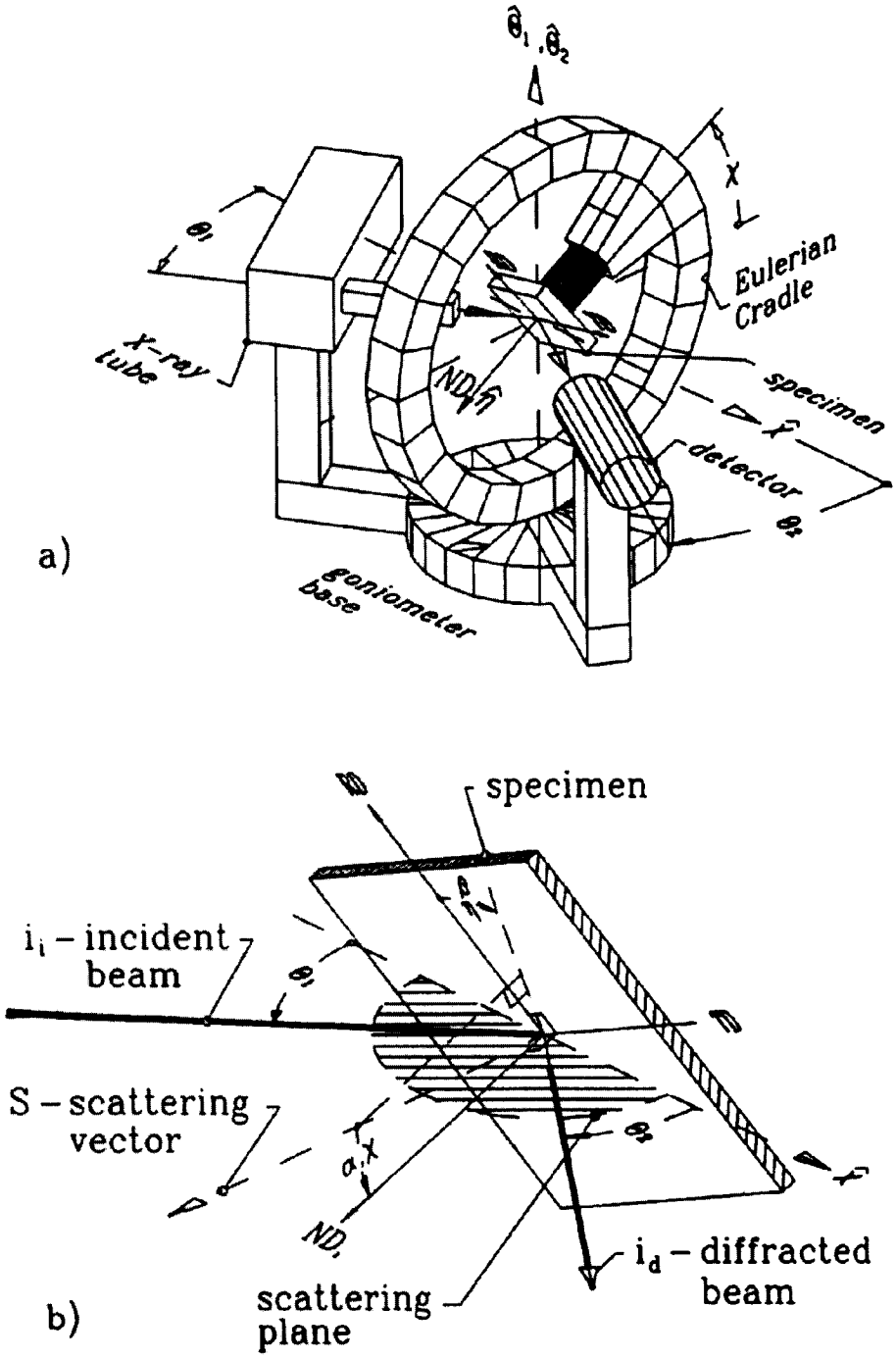


Figure 3.2. Schematic diagrams of (a) a vertical-axis texture goniometer, (b) the specimen rotation angles [58].

3.2. Electron Backscattered Diffraction Technique (EBSD) - Orientation Imaging Microscopy (OIM)

To obtain information on texture and microstructure from the sample surface, a new microscopy, called an orientation imaging microscopy (OIM), was used (Figure 3.3). The microscopy is called 'orientation imaging', owing to the fact that contrast is formed by gradients of the local lattice orientation. More specifically, electron backscattered diffraction (EBSD) patterns are analyzed to determine the lattice orientation in small localized regions. Grain boundaries are drawn by identifying the orientation of each grain. By rapidly capturing and processing EBSD patterns from the surface of samples in the scanning electron microscope (SEM), an OIM system can produce thousands of orientation measurements, linking local lattice orientation with grain morphology.

OIM data is collected by moving an electron beam across a sample to prescribed points. Generally, these points are defined by a regular hexagonal array. At each point, an electron backscatter diffraction pattern is digitized and then automatically indexed by the computer. The orientation is obtained and recorded as a set of three Euler angles (ϕ_1, Φ, ϕ_2). Along with the orientation, the position of the electron beam in the form of x, y coordinates is also recorded. A parameter describing the quality of the diffraction pattern and a confidence index describing the confidence of the automatic indexing algorithm in the orientation obtained from the diffraction pattern are also recorded. These data can be used to form a wide variety of images and data plots which give insight into the microstructure.

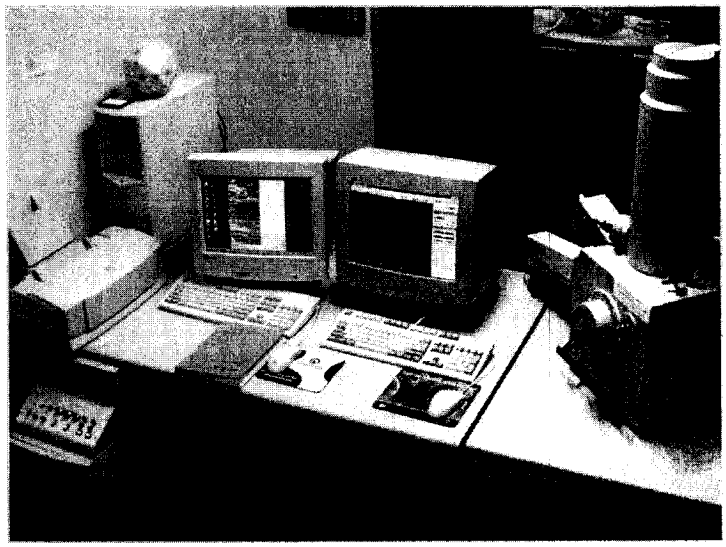


Figure 3.3. Scanning Electron Microscopy with the OIM attachment.

A schematic of the current hardware configuration of the orientation imaging microscope is shown in Figure 3.4. The sample is examined first in the SEM using normal secondary electron imaging or backscatter imaging mode to seek the area from which crystallographic information is sought. The beam is collimated and positioned on the area of interest. When an electron beam of narrowly defined energy strikes a crystal with an inclined surface (~70°), the electrons disperse beneath its surface and subsequently diffract in a systematic manner. A phosphorous screen is placed approximately 40 mm from the specimen, and a pattern composed of intersecting bands is formed by the diffracted electrons on the phosphorous screen. The bands in the pattern are termed Kikuchi bands and are representative of lattice planes in the diffracting crystal. The width and intensity of the bands are directly related to the spacing of atoms in the crystal planes, and the symmetry of the crystal lattice is reflected in the pattern. Thus, information regarding the structure of an unknown crystal lattice can be obtained from such patterns [59-62].

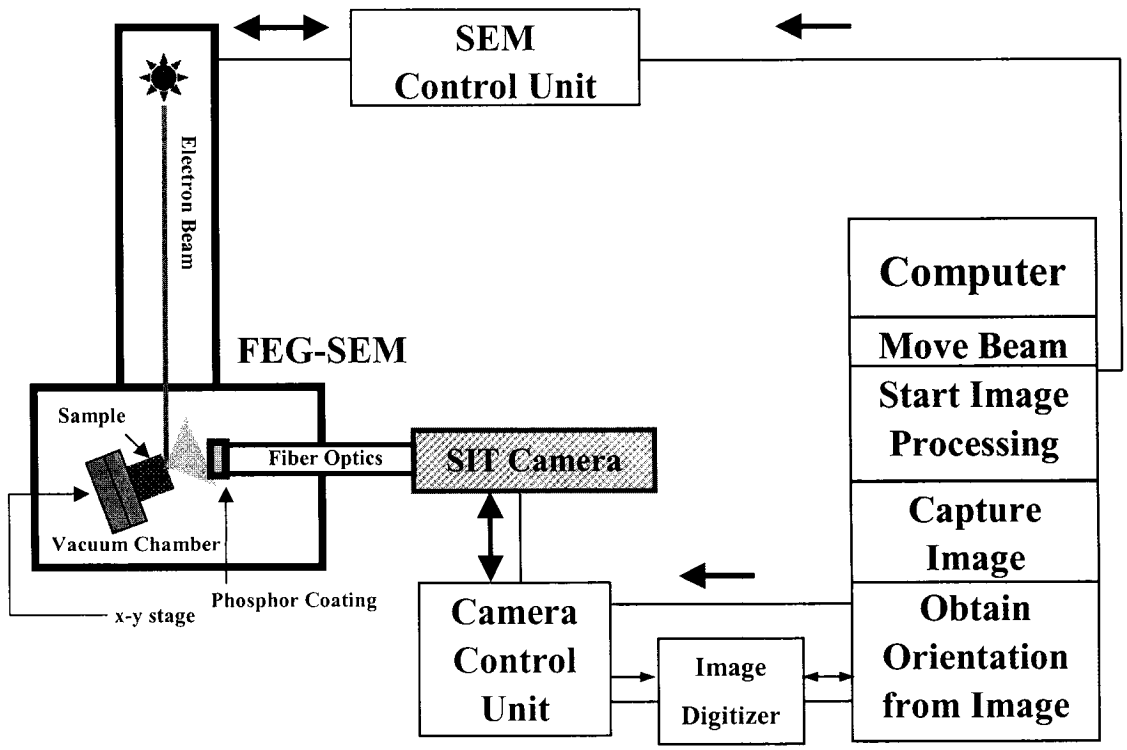


Figure 3.4. Schematic description of the orientation imaging microscope (OIM) [59].

High quality electron backscatter diffraction (EBSD) patterns are obtained using a low light camera such as a silicon-intensified target (SIT) or a charge-coupled device (CCD) camera. A digital signal processor is capable of averaging a variable number of video images. The choice is usually dictated by the quality of the EBSD patterns, and is a function of atomic number, strain level in the sample, and the quality of the sample preparation. This averaged pattern is enhanced by flat fielding using a stored background image obtained by scanning over a large number of grains on the surface. This flat fielding removes intensity gradients in the image that were not fully removed by the camera control unit and enhances contrast [59].

EBSD patterns are used to determine the orientation of the crystal lattice with respect to some laboratory reference frame in a material of known crystal structure. To obtain the orientation from a diffraction pattern, the pattern must be indexed. Electron backscatter diffraction patterns are made up of many bands at different angles and positions. Given the angle and position of three or more bands in a diffraction pattern, the software can determine the orientation. The angles between the bands are compared against the theoretical angles stored in a look-up-table for the given material being examined to identify the (hkl) of the reflecting plane associated with the bands. If the (hkl) of two bands can be determined, a corresponding orientation can be calculated. The angles in the look-up-table are calculated for a set of user-specified planes. The optimum planes to be used are the strong reflecting planes, which produce the highest contrast bands in the diffraction patterns. The angles between the bands digitized by software usually do not precisely match the theoretical ones in the look-up-table. Therefore, some deviation is allowed when matching the theoretical angles to the measured ones. This may lead to more than one solution for a set of bands. For each possible triplet of bands in the set, all possible solutions are tracked. The solutions are ranked according to how often they appear for the different triplets. The highest-ranking solution is recorded to file. One of the examples of an indexed EBSD pattern is shown in Figure 3.5.

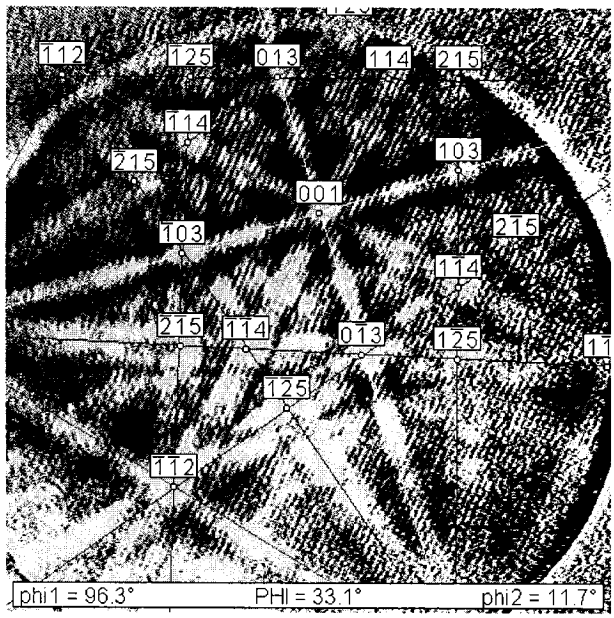


Figure 3.5. Copper EBSD pattern indexed using OIM.

The image is displayed in a video window of the computer workstation. Sophisticated crystallographic software analyzes the image and automatically indexes the diffraction pattern. The following data are calculated and stored: three Euler angles defining the orientation of the crystal, (x, y) coordinates giving the position where the data was obtained on the specimen, a quality factor defining the sharpness of the diffraction pattern, a "confidence index" indicating the degree of confidence that the indexing is correct, and the crystallographic phase of the area from which the pattern was obtained. This process can be repeated to collect large amounts of crystallographic data from the specimen at different positions of the electron beam on the specimen. Using automatic control, the beam can be positioned on the points of a grid to completely cover

the area of interest on the specimen. An alternative to automatic beam control is automatic stage control. A sample holder is fixed upon a mechanical x-y stage, which is mounted such that the outward normal of the sample makes an angle of approximately 70° from the vertical line of the electron beam. The flat sample surface is stationed parallel to the plane of motion of the stage such that x-y motions remain in eucentric focus.

The stored data (location, orientation, and image quality) can be processed to create Orientation Imaging Micrographs, enabling a visual representation of the microstructure. Each location is represented by a pixel, to which a color or gray scale value is assigned on the basis of the local details of lattice orientation or the quality of the EBSD patterns. Figure 3.6 shows an example of an image that has been generated from OIM data obtained on a sample of a recrystallized copper.

In addition to the visualization of microstructure, many tools are available for performing quantitative analysis of the orientation aspects of microstructure. This is the area where OIM provides a wealth of insight that traditional microscopy techniques are simply not capable of providing. OIM can be used to investigate preferred orientation in polycrystals similar to conventional x-ray and neutron diffraction pole figure techniques. However, since electron diffraction provides point specific orientation measurements, OIM can be used to investigate the misorientation between points in the microstructure. Thus, the preferred misorientation or grain boundary character distribution can be investigated using OIM. As an example of the use of OIM to investigate the distribution of orientations, sample discrete and shaded (100) pole figures measured in a sample of recrystallized copper foil are shown below in Figure 3.7.

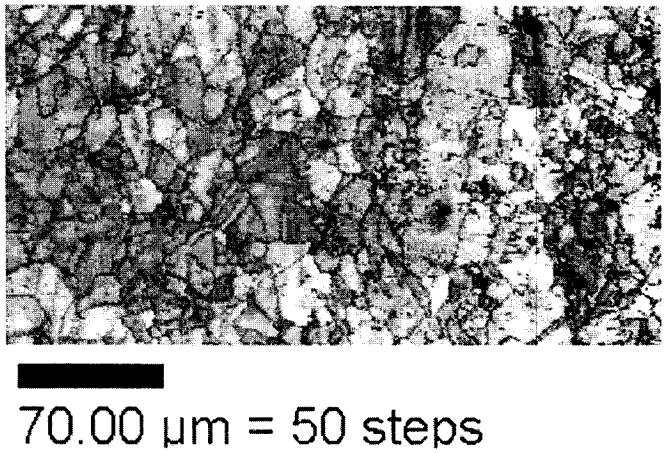


Figure 3.6. OIM map of a recrystallized copper.

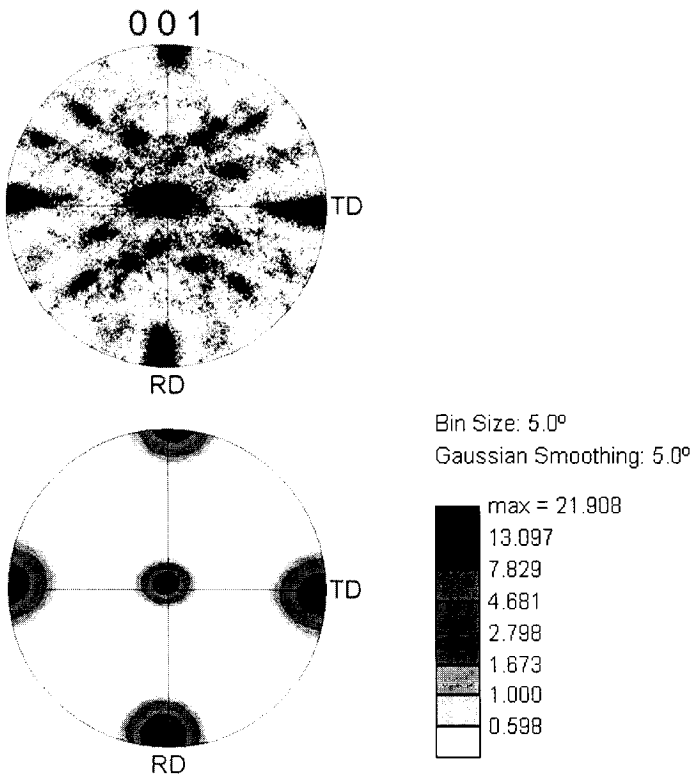


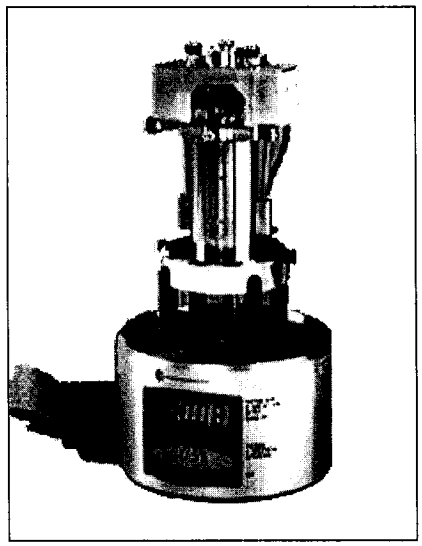
Figure 3.7. Discrete and shaded (100) pole figures for recrystallized copper foil.

3.3. Atomic Force Microscopy (AFM)

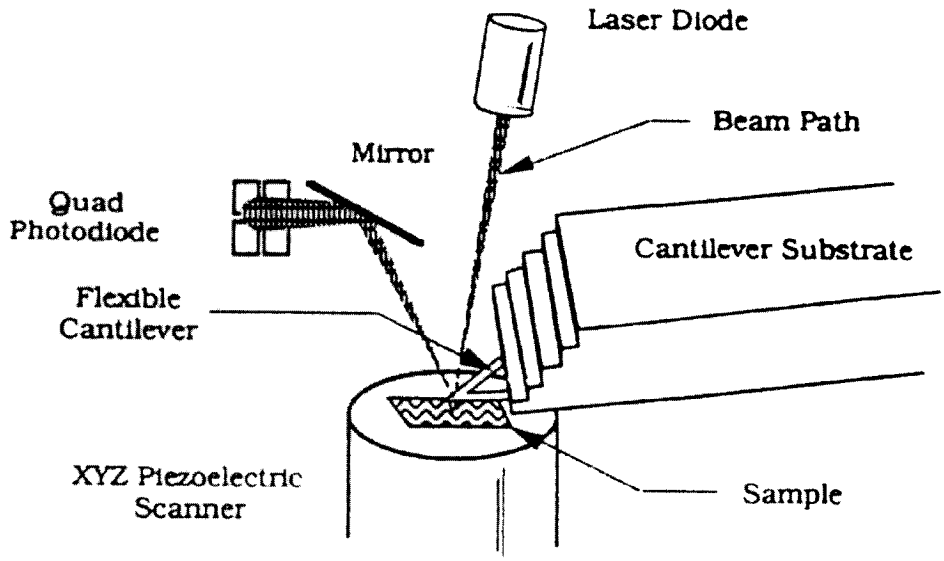
The critical factor for success of the copper electroplating process is the copper seed layer which must be thin, smooth, and continuous to ensure void-free fill. To observe the very precise morphology of a sample surface, atomic force microscopy (AFM) which gives the nanoscale morphology of sample surface was used in this study.

AFM is a technique to analyze the surface morphology of materials by measuring the interatomic forces between the probe and sample surface. A schematic of the sensing system of the AFM is illustrated in Figure 3.8. A micro-fabricated silicon nitride cantilever with a sharp tip is lowered onto the sample surface with a tip force of $\approx 10^{-9}$ N. The surface is scanned using piezoelectric scanners. The beam from a laser diode is focused onto the back of the cantilever. The laser beam reflects off the back of the cantilever onto a segmented photodiode. The deflection of the cantilever is detected using a reflected laser beam. The amplified differential signal between the upper and lower photodiodes provides the sensitive measure of the cantilever deflection. Any variation during scanning of the sample is corrected by retracting or extending the sample mount on a third piezoelectric scanner. A computer processes output signals and generates a three-dimensional image of the sample surface.

In this investigation, a Digital Instrument Nanoscope III contact-mode AFM fitted with a 0.12 Nm^{-1} cantilever was used. Samples were mounted on a piezoelectric scanner with a maximum lateral scan range of 12.5 μm and maximum vertical range of 5 μm. Data files of 400×400 points were collected under conditions of constant force at scan rates of between 2 and 9 Hz.



(a)



(b)

Figure 3.8 Atomic force microscope (AFM): (a) NANOSCOPE III by Digital Instrument, (b) the schematic of the sensing system.

3.4. Finite Element Modeling (FEM) for the Calculation of Stress Distribution in the Cu Damascene Interconnects

From previous research [63-66], it was found that the stress which is generated by the difference in the thermal expansion coefficient (CTE) can affect the texture and microstructure of Cu damascene interconnects during annealing.

In practice, copper damascene process for chip interconnections is fairly complicated, especially when one considers the aspect ratios and geometries of the trenches. In addition, the subsequent processes, such as annealing, strongly affect the nature of Cu interconnects. Because of this complex process it is difficult to measure and analyze the stress distribution in the Cu trench. To understand the effect of stress distribution on the textural and microstructural evolution of copper interconnects after annealing, finite elements modeling (FEM) of stresses in the trench will be needed to help explain the transformation of texture and microstructure.

The finite element method is a numerical technique widely used for finding solutions to partial differential equations. FEM is based on discretizing a domain into elements (and nodes) and constructing basis (or interpolation) functions across the elements.

In this study, ABAQUS v.5.8™ [67] and FEMLAB v.2.3a™ [68], both are commercial software, were used. In order to analyze the impact of line width on the stress distribution, the cross-sectional stress distributions were calculated as the line width decreased, using ABAQUS v.5.8. The details of stress distribution on the top surface area of Cu damascene interconnects during annealing were calculated by FEMLAB v. 2.3a.

The basic mathematical structure with which FEMLAB operates is a system of partial differential equations (PDEs). In FEMLAB, one can represent PDEs in two ways: coefficient form (suitable for linear or nearly linear problems) or general form (intended for nonlinear problems).

When solving the PDEs that describe a model, FEMLAB applies the finite element method (FEM). The software runs that method in conjunction with adaptive meshing and error control as well as with a variety of numerical solvers. An example of modeling is shown in Figure 3.9.

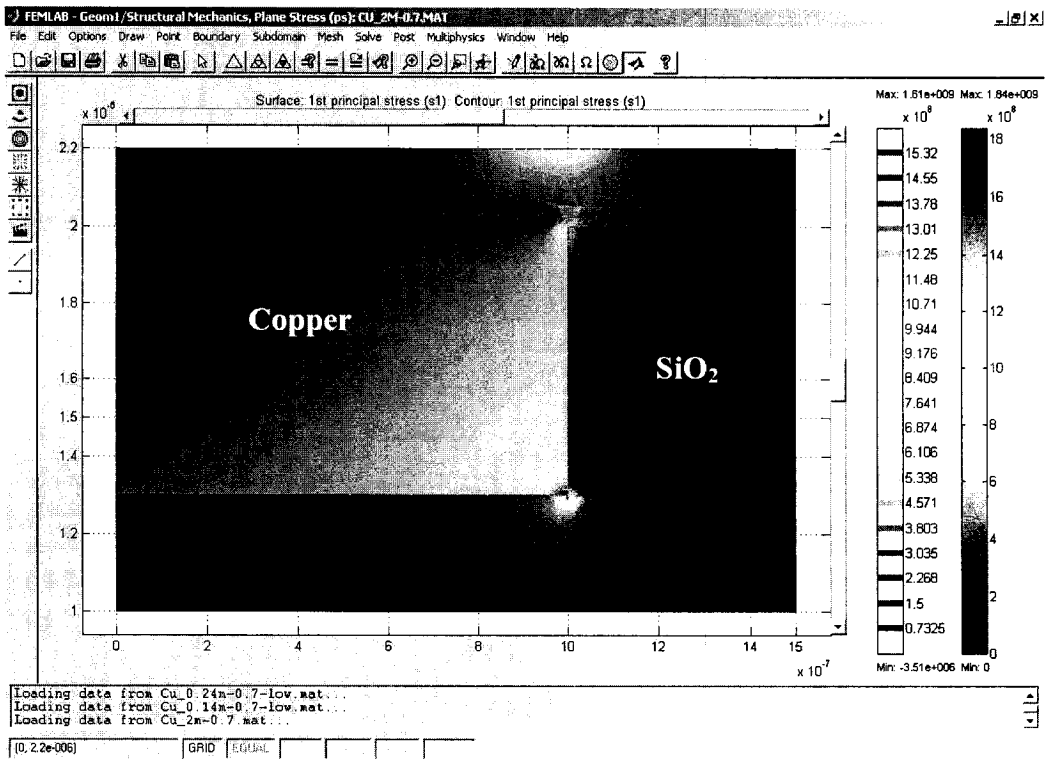


Figure 3.9. The captured image of stress calculation in the Cu interconnect using FEMLAB.

Chapter 4

The Effects of Substrate Texture and Electroplating Condition on Texture and Surface Morphology of Copper Electrodeposits

Cu electroplating is a key process in manufacturing interconnects in electronic chips. It is therefore very important to understand the effect of substrate texture and electroplating conditions on the texture and surface morphology of Cu electrodeposits. Texture of electrodeposit is very closely related with the failure of electronic interconnect caused by electromigration and void formation during fabrication. The electroplating techniques have been studied extensively in the past, however the influence of substrate texture and electroplating conditions on the texture and surface morphology of electrodeposits is still unclear. In this chapter, a role of different electroplating conditions and substrates having different texture is investigated. To do that, three different polycrystalline copper specimens are used as substrates and electrodeposits are plated using different current densities.

4.1. Experimental Procedure

4.1.1. Sample Preparation

From previous research [69-74], it is known that copper substrate texture and microstructure can strongly affect the electroplated copper. In order to understand the effect of substrate texture and electroplating conditions on texture and surface morphology of copper electrodeposits, pure single crystals and polycrystalline copper substrate samples having different textures were electroplated, using conditions as shown in Table 4.1. The single crystal substrates which have (100), (110) and (111) orientations were prepared and analyzed by scanning electron microscopy (SEM). Three polycrystalline samples which have different textures were prepared and analyzed by x-ray diffraction (XRD) technique, orientation imaging microscope (OIM), SEM and atomic force microscopy (AFM).

Table 4.1. Various substrates and electroplating conditions (current density) used in this investigation.

Substrates		**Electroplating Condition (Current Density)**	
Single crystalline	Polycrystalline	X-ray	OIM
(100) (110) (111)	**Po6:** Weak {110} **Po8:** Strong {100} **Po9:** Strong {100} & {111}	1 mA/cm^2 50 mA/cm^2 100 mA/cm^2 1000 mA/cm^2	1 mA/cm^2 10 mA/cm^2 100 mA/cm^2 1000 mA/cm^2

A copper film having the thickness of 50 μm was deposited on the copper substrate by electroplating in an acidic copper bath. The bath composition was copper sulfate ($CuSO_4.5H_2O$) 200 g/l, sulfuric acid (H_2SO_4) 75 g/l, and the deposition was carried out at a temperature 40 C°, and current densities was varied from 1 to 1000 mA/cm^2 (Table 4.1). A schematic illustration of the electrodeposition set used in study is shown in Figure 4.1 [68].

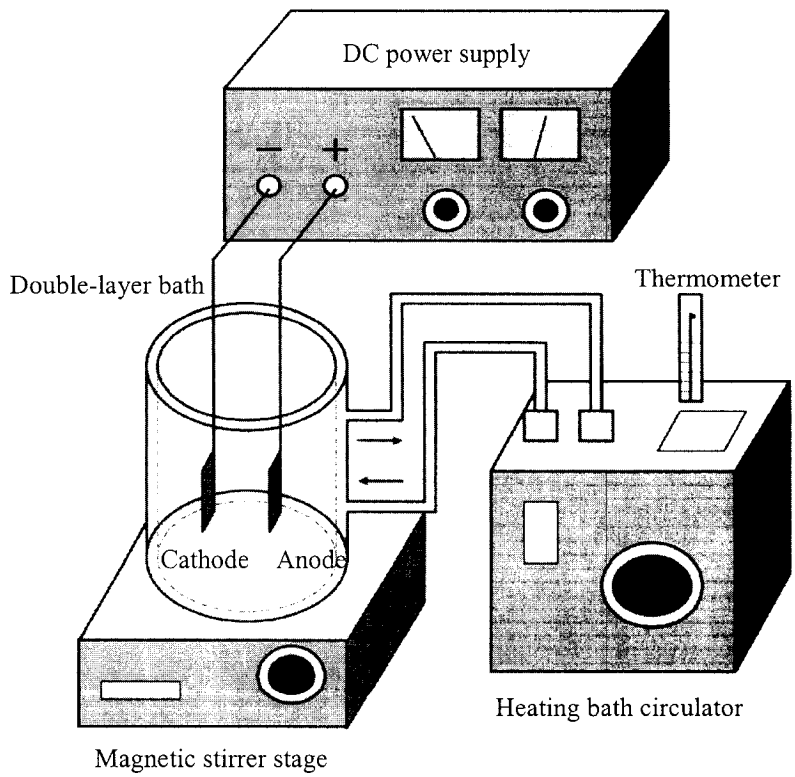


Figure 4.1. Schematic illustration of the electrodeposition set.

The thickness of electroplated copper was calculated by Faraday's law (Equation (4.1) and (4.2)) [75, 76].

$$W = \frac{It}{96{,}500} \times \frac{A}{z} \tag{4.1}$$

$$T = \frac{W}{a \times d} \tag{4.2}$$

where, W is the weight of deposit, I is the current, t is time (second), A is the atomic weight, z is the valency, T is the thickness of deposit, a is the plated area, and d is the density of metal.

Copper polishing is rather difficult. Unlike tungsten, copper is a soft metal and subject to scratching and embedded particles during polishing. Also, because copper is highly electrochemically active and does not form a natural protective oxide, it corrodes easily. Therefore, to acquire clean surface of sample for XRD measurement, both mechanical polishing and electropolishing were performed. At first, a rough specimen surface was polished grading up to 0.05 micron final polish, and then, was electropolished in a solution composed of 175 ml distilled water and 825 ml H_3PO_4 at room temperature and a voltage 1.2 V for 20 minutes.

For the OIM investigation, the cross-sectional area of sample which is normal to the transverse direction (TD) of samples was analyzed. Figure 4.2 shows the sample was mounted with respect to the reference frame of the specimen. The sample was mounted using the supporting metal plates to protect the edge of the electroplated copper during grinding and polishing.

This mounted sample was ground down by 2-3 mm from the mount surface using SiC 120 grit and a grinding wheel speed 150 rpm. Subsequent grinding steps involved

SiC 240 grit, 320 grit, 400 grit and 600 grit papers at 150 rpm, followed by SiC 1200 grit and 2400 grit at 100 rpm. Finally, the samples were subjected to polishing with the 0.05 μm colloidal silica solution for 6-12 hours in the VIBROMET 2, Buehler Vibratory Polisher (Figure 4.3). This polisher vibrates a 12-inch diameter platen at a frequency of 7200 Hz with virtually no vertical motion. The vibratory polishing is an excellent technique for polishing soft materials without excessive deformation and scratches and for coated materials and metals exhibiting corrosion products without edge rounding.

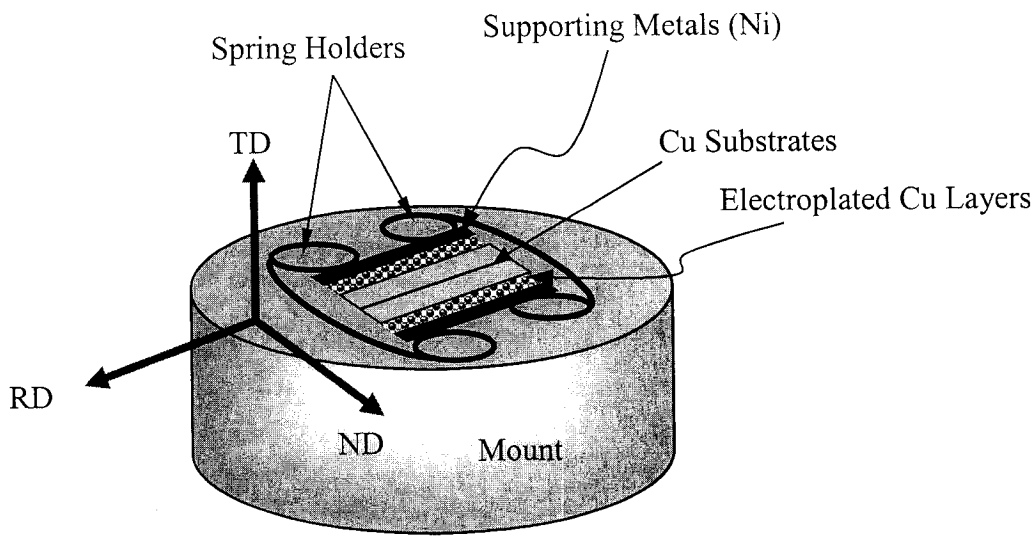


Figure 4.2. The schematic structure for the mounting assembly, consisting of the Cu substrates, the electroplated Cu layer, the supporting metal pieces and the pair of spring holders.

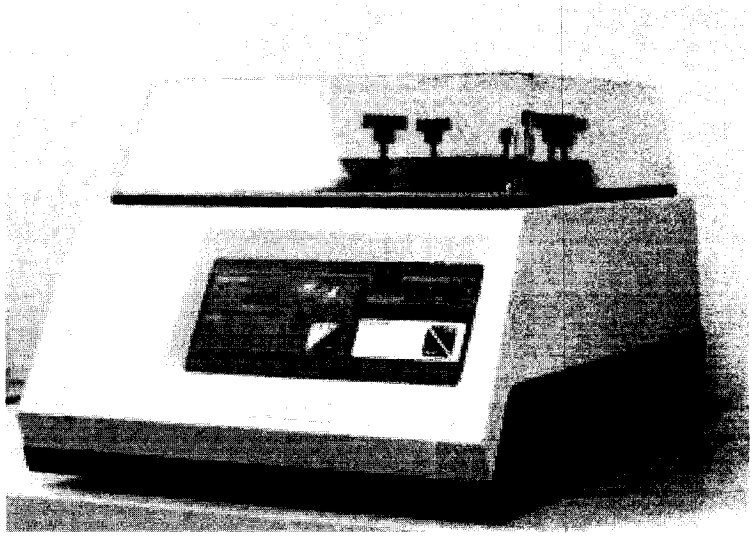


Figure 4.3. VIBROMET 2, Buehler Vibratory Polisher.

4.1.2. Texture, Microstructure and Surface Morphology Measurement

The crystallographic texture of copper electrodeposits was measured using a Siemens D500 x-ray goniometer. Pole figures were obtained using the reflection technique, up to maximum tilt of the specimen of 80 deg in 5 deg intervals and the inverse pole figure (IPF) for the normal direction was calculated by TexTools v.3.2, commercial software for texture analysis [77].

The orientation imaging microscope (OIM) mounted on a Philips XL30 field-emission-gun scanning electron microscopy (FEG-SEM) was used to identify the orientation of each grains and type of grain boundaries in the cross-section of the electroplated copper sample. The coincidence site lattice (CSL) grain boundaries were

identified from the electron backscattered pattern (EBSP). The frequency of occurrence of these boundaries up to $\Sigma 29$ was calculated.

For the XRD analysis, the substrate textures of each sample were measured, and then, 50 μm copper electroplating was performed on the substrates and analyzed. Using OIM, the details of cross-sectional changes in the microstructure and texture of Cu electrodeposits was observed. The morphology of electroplated copper surface was analyzed using AFM and FEG-SEM.

4.2. Texture of Copper Electrodeposits

In order to analyze the effects of substrate texture and current density on the texture of electrodeposits after electroplating, three incomplete pole figures of specimens (Po6, Po8 and Po9) were measured by XRD.

Po6 sample has a weak {110} fiber texture, as shown in Figure 4.4. This figure shows ODF at $\varphi_2 = 0°$ section and illustrates changes of intensity as the current density increases. It was found that the {110} texture becomes stronger as current density increases. To describe directional changes of {110} texture, the plots of {110} fiber as the current density increases, are shown in Figure. 4.5. After electroplating, {110} texture developed as current density increases, especially at 1000 mA/cm^2. In addition, a minor texture component which is (001)[0$\bar{1}$0] is detected as the current density increase as illustrated in the Figure 4.6. This figure shows that (001)[0$\bar{1}$0] texture component developed at low current density after electroplating, and its intensity decreases gradually until 100 mA/cm^2. At 1000 mA/cm^2, there is some increase of intensity.

The result of Po8 sample shows a strong {100} cube texture (Figure 4.7). This figure illustrates that no major change of type of texture, however, as the current density increases, the intensity changes. To illustrate this trend, the intensity of cube texture was plotted in Figure 4.8. In this figure, one can see that the cube texture was developed at the low current density, and its intensity decreases as the current density increases. The changes of the minor component, (221)[1$\bar{2}$2] which can be generated by twinning are plotted in Figure 4.8b. It is clearly seen that its intensity decreases at low current density

after electroplating and increases as the current density increases. It seems that the cube texture of Cu electrodeposits can grow easily at low current density consuming the twin component. This observation will be discussed later in this chapter.

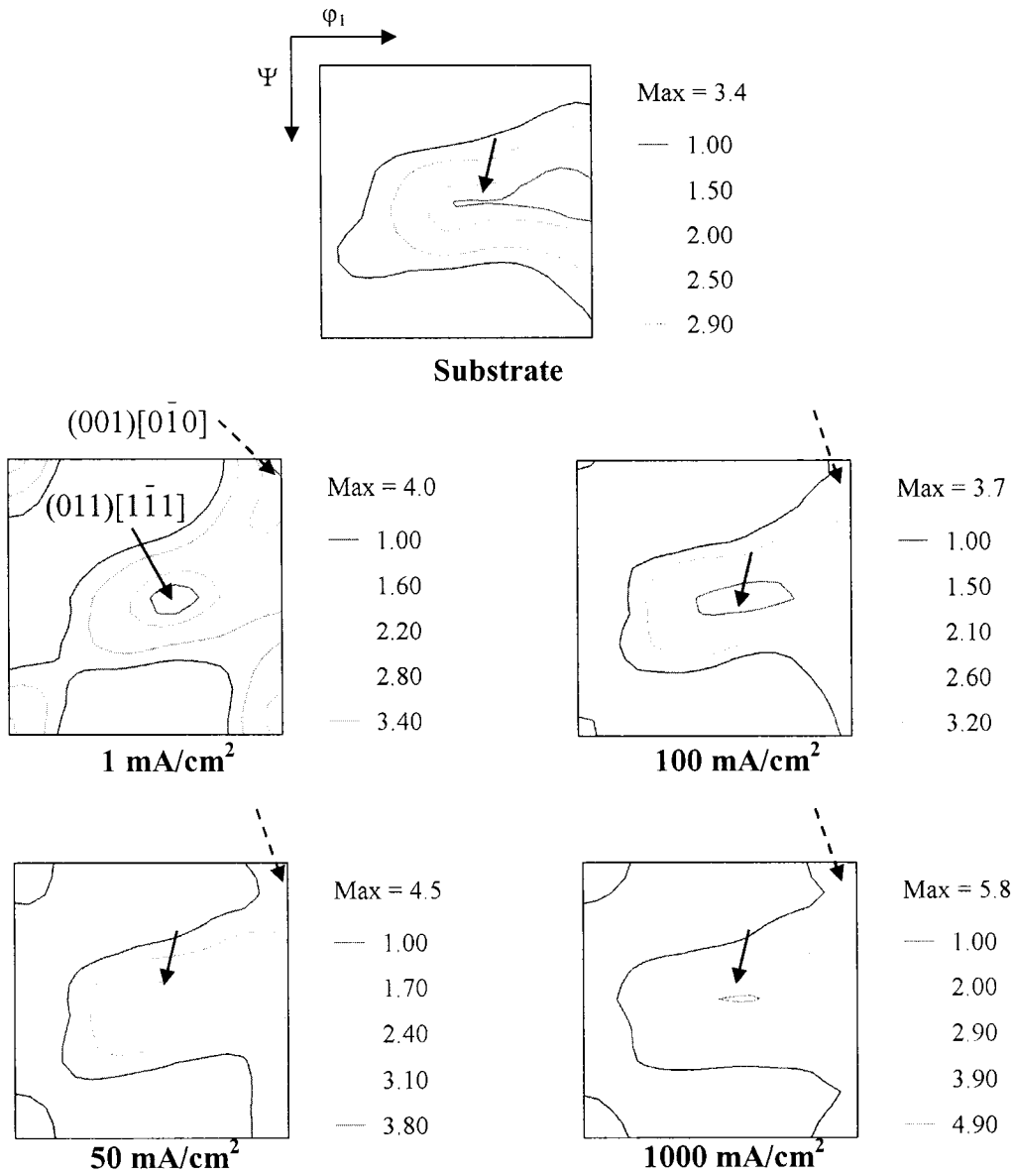


Figure 4.4. Sections of ODFs for $\varphi_2 = 0°$ with different current densities: arrows indicate (011)[1$\bar{1}$1] and (001)[0$\bar{1}$0] textures (Po6).

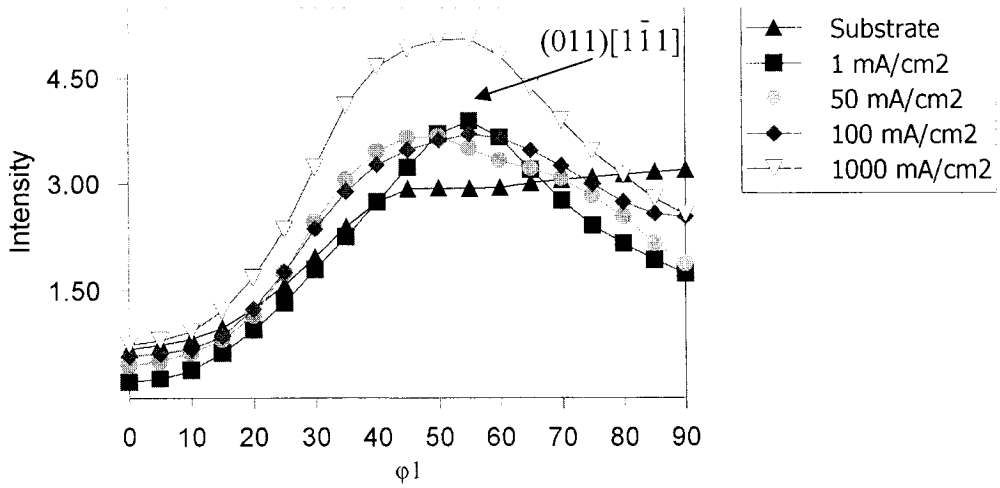


Figure 4.5. {110} fiber plots for the substrate and electrodeposits obtained with different current densities (Po6).

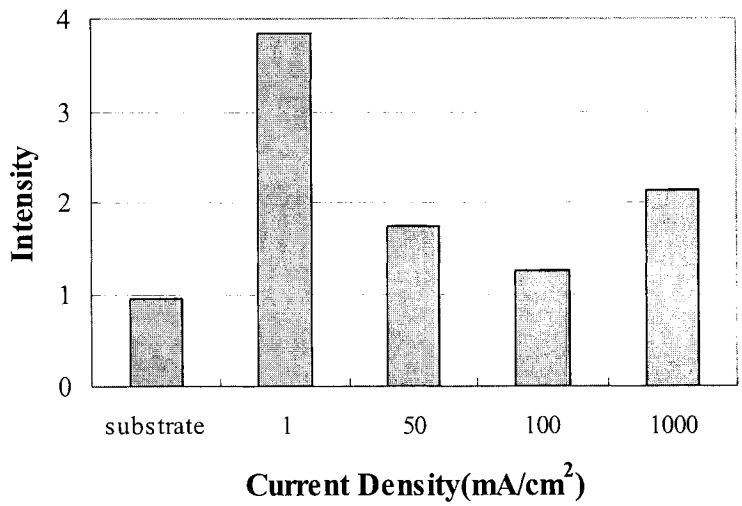


Figure 4.6. (001)[0$\bar{1}$0] texture of substrate and electrodeposits obtained using different current densities (Po6).

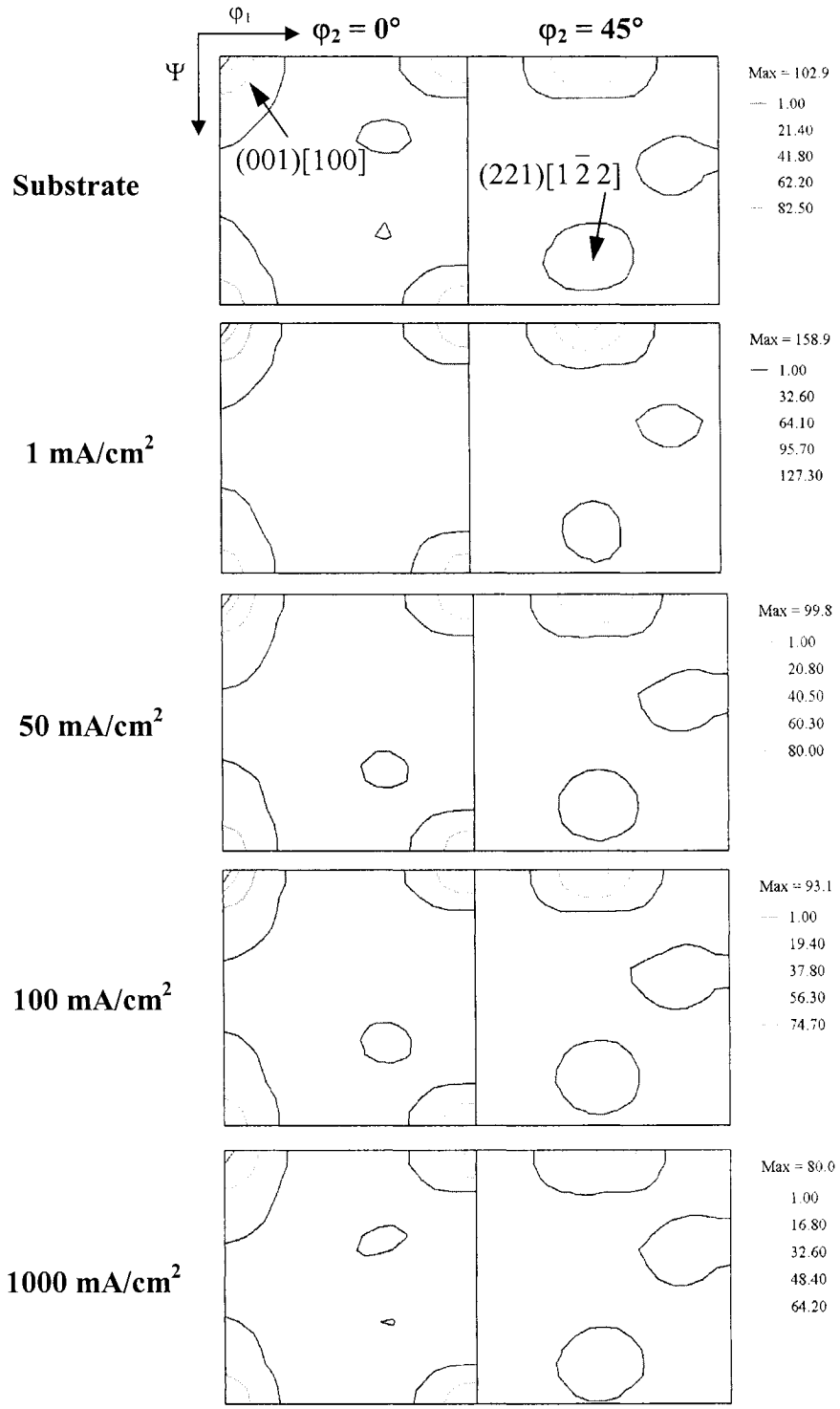
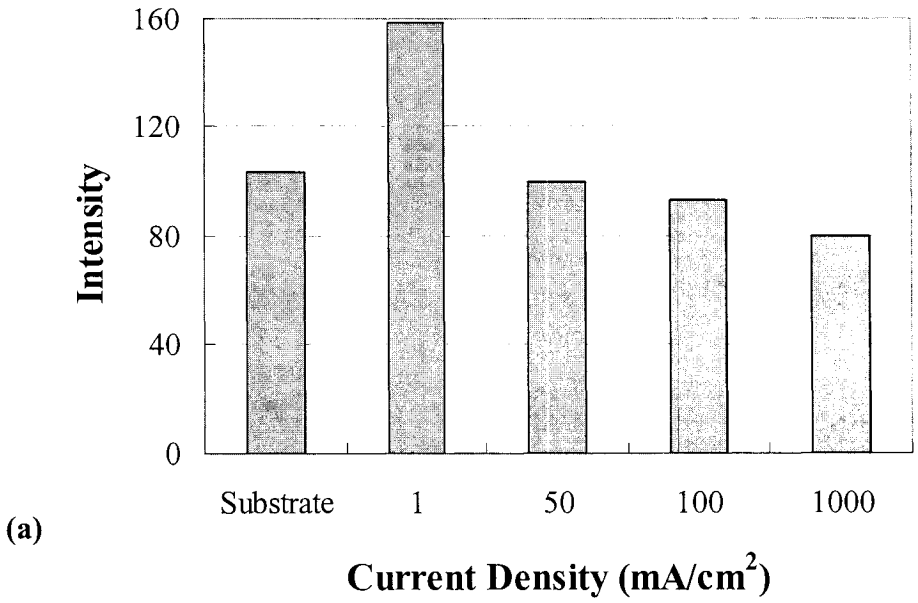
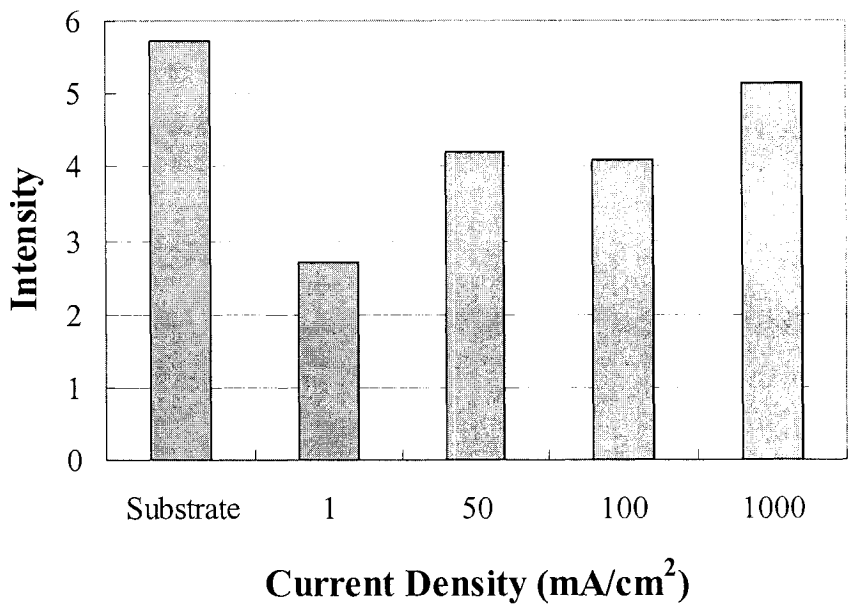


Figure 4.7. Sections of ODFs for φ_2 = 0 and 45° of substrate and electrodeposits obtained using different current densities: arrows indicate (001)[100] and (221)[1 $\bar{2}$ 2] textures (Po8).



(a)



(b)

Figure 4.8. The intensity changes of substrate and electrodeposits obtained using different current densities (Po8): (a) (001)[100], (b) (221)[1 $\bar{2}$ 2].

Po9 sample, which has a strong {111} and weak {100} texture shows very interesting results (Figure 4.9). The substrate texture can be represented by (001)[1 $\bar{2}$ 0], (111)[3 $\bar{4}$ 1] and (111)[$\bar{1}$ $\bar{1}$ 2]. After electroplating with low current density (1 mA/cm^2), (001)[2 $\bar{3}$ 0] and (111)[1 $\bar{2}$ 1] textures are developed instead of (001)[1 $\bar{2}$ 0] and (111)[3 $\bar{4}$ 1] texture, as shown in Figure 4.9. At 50 mA/cm^2 current density, (111)[1 $\bar{2}$ 1] changes back to (111)[3 $\bar{4}$ 1] with the increase of its intensity, however, (001)[2 $\bar{3}$ 0] doesn't change. At 100 and 1000 mA/cm^2 current density, the intensity of (111)[$\bar{1}$ $\bar{1}$ 2] texture is getting stronger than (111)[3 $\bar{4}$ 1]. To see the development of fiber component after electroplating, {111} fiber texture was plotted, as shown in Figure 4.10. This figure shows the fiber components are developed for the current densities higher than 100 mA/cm^2, stronger fiber texture developed. To see the directional changes of {111} planes, the intensity changes of (111)[3 $\bar{4}$ 1] and (111)[$\bar{1}$ $\bar{1}$ 2] textures are plotted in Figure 4.11. This figure shows that at low current density, the intensity of (111)[3 $\bar{4}$ 1] is higher than (111)[$\bar{1}$ $\bar{1}$ 2], however, at high current density, the intensity of (111)[$\bar{1}$ $\bar{1}$ 2] is higher than (111)[3 $\bar{4}$ 1]. For Po9 sample, it seems that the stress in Cu electrodeposits which is generated by the high current density may have influence on the development of (111)[$\bar{1}$ $\bar{1}$ 2] texture. This stress energy can be minimized when the absolute maximum principal stress direction is parallel to minimum Young's modulus direction which is <112> direction in this case [78-81]. Explanation of this phenomenon will be discussed in the Chapter 5. These results demonstrate that the substrate texture strongly affects the texture of the electrodeposits, however, this substrate influence can be changed by electroplating condition such as current density: strongly textured sample (Po8) shows the decrease of texture strength, weakly textured sample (Po6) shows the increase of texture intensity, and Po9 sample shows the fiber texture as the current density increases.

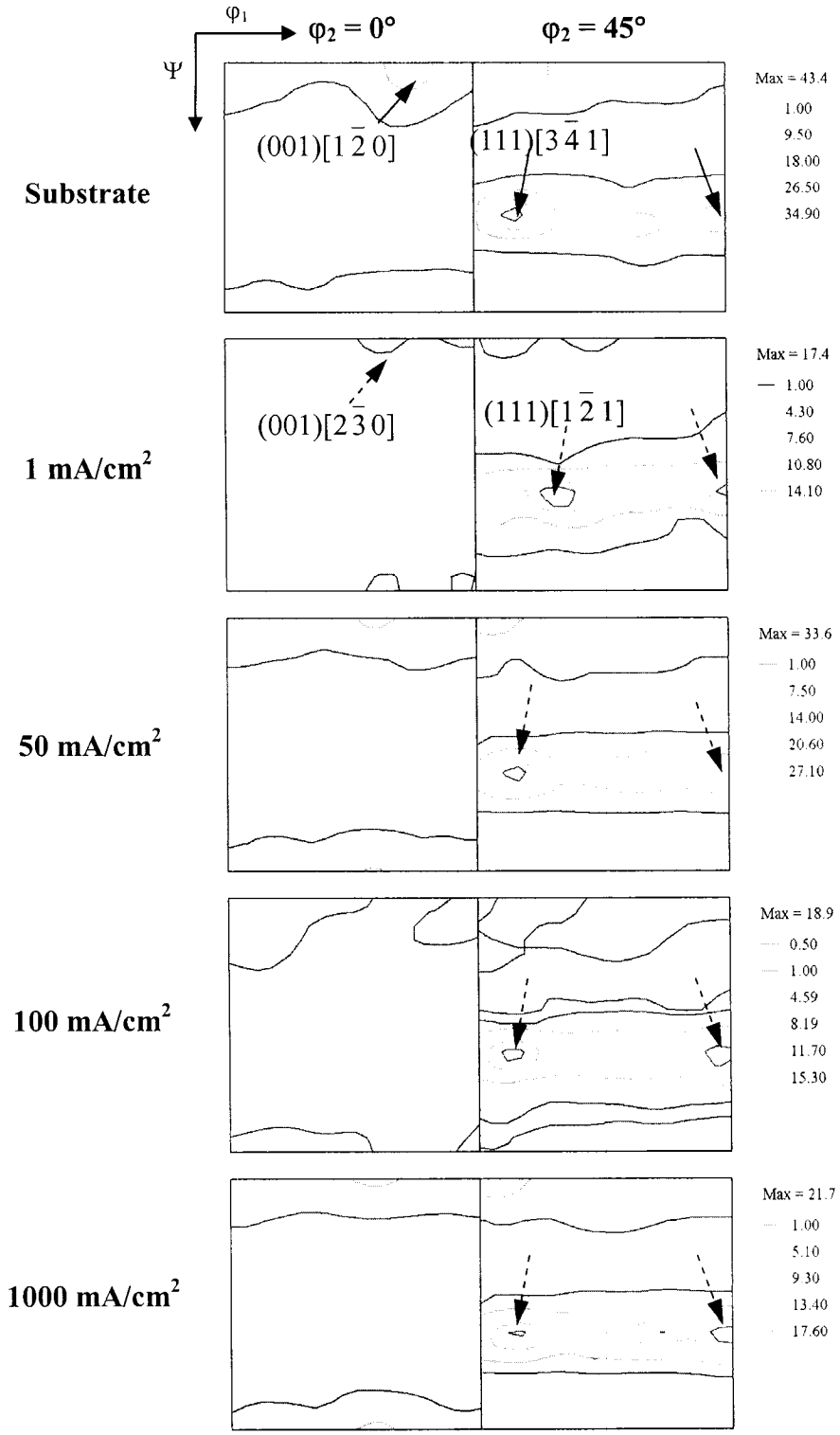


Figure 4.9. Sections of ODFs for φ_2 = 0 and 45° of substrate and electrodeposits obtained using different current densities: arrows indicate (001)[1 $\bar{2}$ 0], (111)[3 $\bar{4}$ 1] and (111)[$\bar{1}$ $\bar{1}$ 2] textures (Po9).

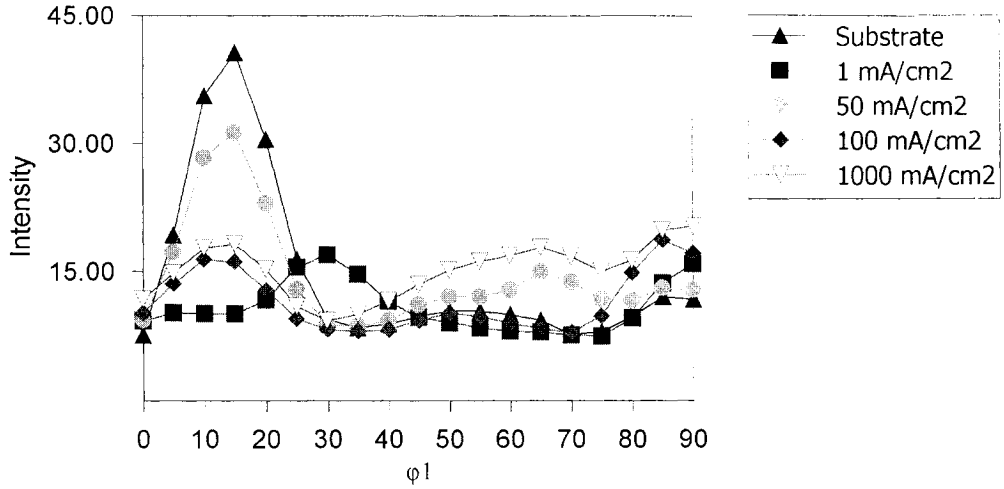


Figure 4.10. {111} fiber plots of substrate and electrodeposits obtained using different current densities (Po9).

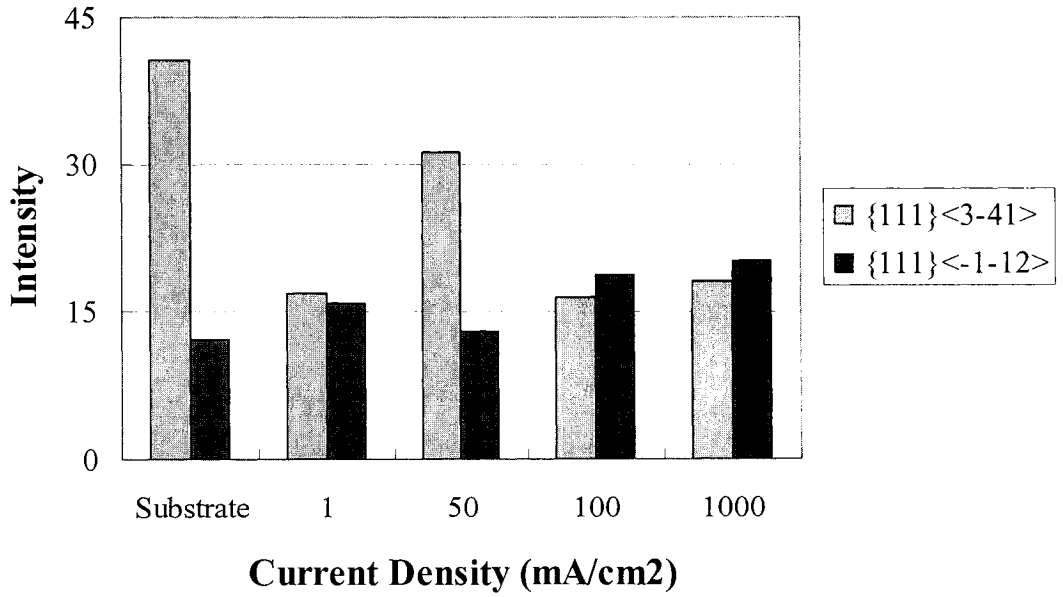


Figure 4.11. The intensity changes of substrate and electrodeposits obtained using different current densities: (111)[3 $\bar{4}$ 1] and (111)[$\bar{1}$ $\bar{1}$ 2].

4.3. Microstructure and Grain Boundary Character Distribution (GBCD) of Copper Electrodeposits

To have more detailed information on the textural and microstructural evolution, the maps of cross-sectional area of electrodeposits were generated from OIM analysis, as shown in Figure 4.12. This figure represents the cross-sectional image of Po9 specimen and shows clearly the growth of the electrodeposits, however, it is hard to distinguish the interface between the substrate and electrodeposits since both are from the same materials. In this investigation, it was found the large columnar grains grow in the deposit. However, the irregular shape of surface morphology illustrates that there is a competition between grains during the stage of growth. These results also indicate that crystallites of different orientations have different growth rate. The fastest growing crystals have conical shape and are narrow at the bottom and become wider as they grow. This shape results from the tendency to minimize the surface energy [82].

In order to understand the effect of current density on grain boundary character distribution, the misorientation distributions and fractions of CSL boundaries were calculated from OIM results, as shown in Figure 4.13. As the current density increases, the fraction of low angle grain boundaries is decreased in all samples (Figure 4.13a) and the fraction of total CSL boundaries is decreased for the Po9, however, the other samples shows little changes (Figure 4.13b). Among these boundaries, Σ3 boundaries, known as twin boundaries, are of special interest because copper is a low stacking fault energy material and can produce twin easily [83-86]. As shown in Figure 4.13c, the number

fraction of Σ3 boundaries increased as the current density increases, especially in the Po8 sample which has a strong cube texture. This can be explained if one assumes that a higher current density during electroplating produces higher stresses in the electrodeposit, these stresses should facilitate twinning in the microstructure of electrodeposits. Comparing to Figure 4.8, it can be concluded that a higher current density generates plenty of twin boundaries which subsequently decreases the intensity of cube texture. In this sense, electromigration induced failure in the Cu damascene interconnects should be minimized by a higher current density since the cube texture has a weak resistance to failure and twin boundaries have a strong resistance to electromigration.

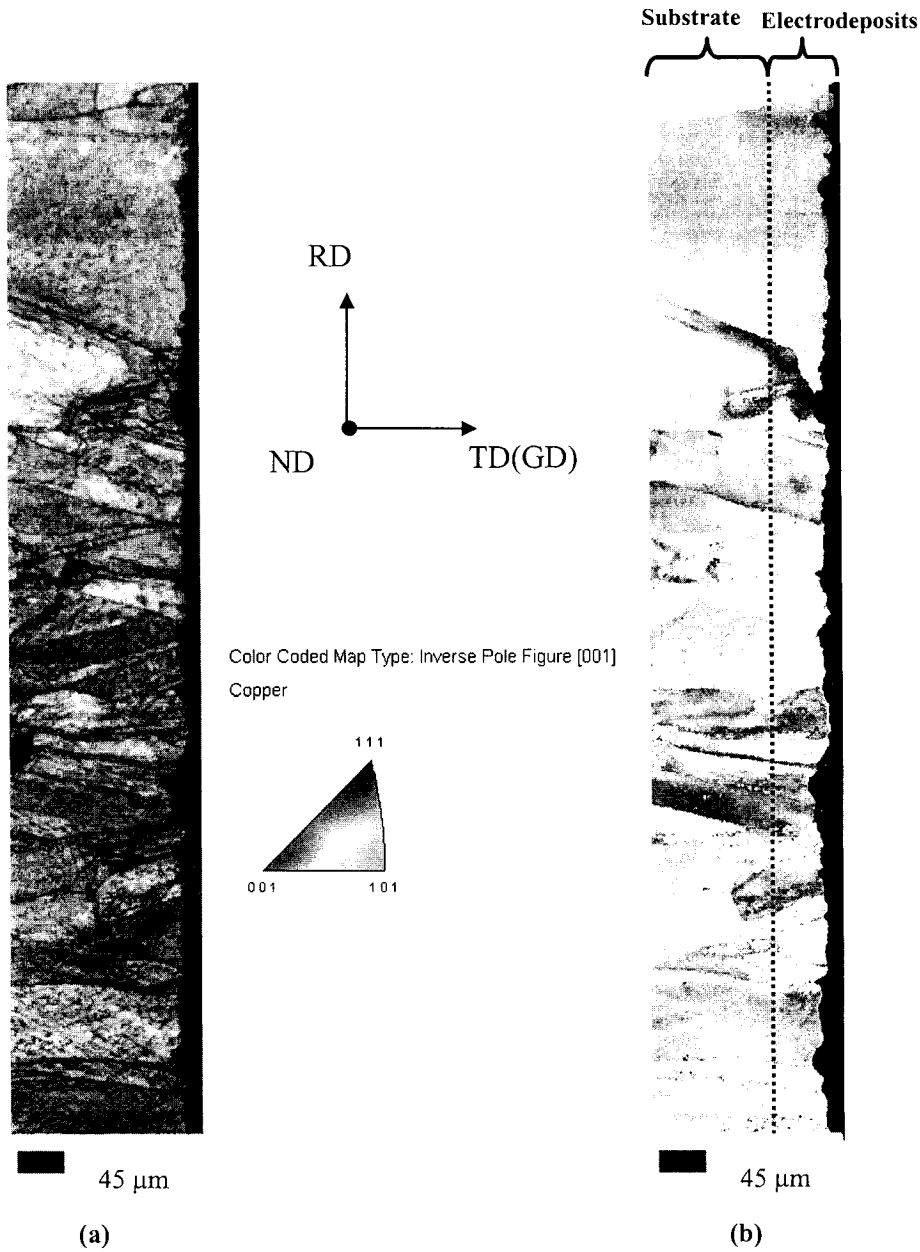


Figure 4.12. Microstructure of grains at a cross-section of copper electrodeposits plated on the polycrystalline copper substrate (Po9): (a) OIM image quality map, (b) inverse pole figure map for the normal direction [001] – TD is the growth direction of electrodeposits (GD).

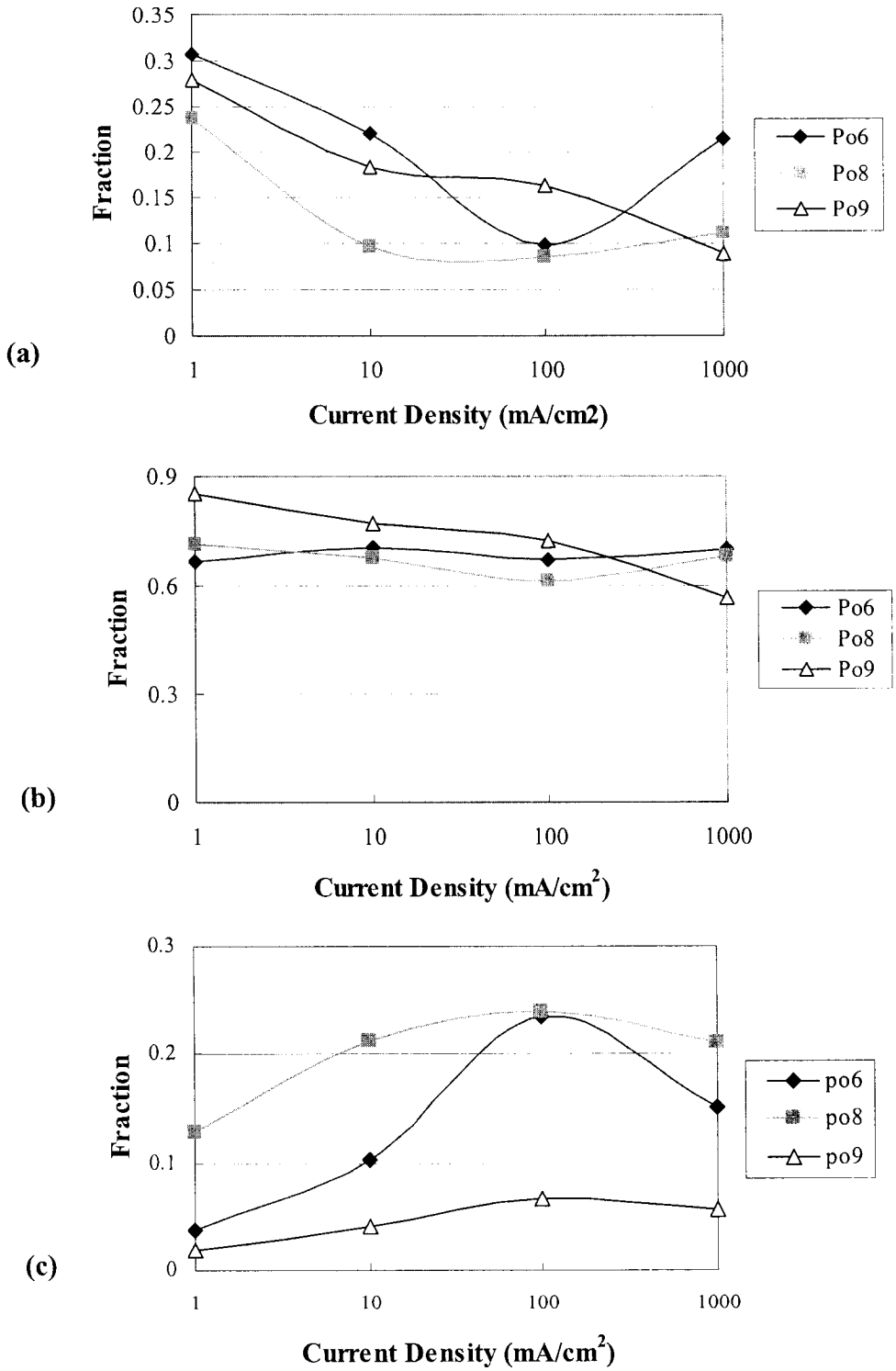


Figure 4.13. Grain boundary character distribution (GBCD) of three samples (Po6, Po8 and Po9) as function of different current densities: (a) number fraction of low angle grain boundaries (< 15°), (b) total CSL boundaries, (c) Σ3 boundaries.

4.4. Surface Morphology of Copper Electrodeposits

Understanding the surface morphology evolution after electroplating is critical for the reliability of Cu damascene interconnects since rough morphology can generate voids inside the trench, as shown in Figure 4.14. In this figure, it is assumed that two different kinds of grain which have a different growth rate are present in the trench. During electroplating to fill the trench, fast growing grain can encapsulate the trench and produce a void.

In order to understand the effects of substrate texture and current density on the rate of deposit growth and the surface morphology, SEM and AFM were used. At first, single crystalline substrates which have (100), (110) and (111) orientations were investigated, as shown in Figure 4.15. At low current density, the surface morphology of deposit formed on different crystallographic planes is different and has specific characteristic. Using the same electroplating condition for single crystalline substrate, polycrystalline Cu substrates were electroplated and the morphology is shown in Figure 4.16. The grain A and B grain shown in this figure have different growth rates and as a result the morphology of the surface is rough, the difference between levels of growth of these two grains is approximately 2 μm. In addition, the AFM investigation (Figure 4.16b) shows that the difference between facets of the grains is around 300 nm which is high enough to produce voids in the trench of the electrodeposits.

The surface morphology obtained for different current density is illustrated in Figure 4.17. This figure shows that a very rough morphology was produced at a low

current density, and the surface of electrodeposits becomes smoother as the current density increases. It is apparent that the surface morphology of electrodeposits is strongly affected by substrate texture at low current density, however, the deposit surface is smoother at high current density where the effect of substrate texture is negligible.

These obtained results demonstrate that an increase of current density during electroplating will allow to generate the smoother surfaces which are beneficial to filling trench. At present it is customary to add additives into electrolyte to fill the trench in damascene process [87-89]. However, the impurities and additives may increase the resistance of copper, therefore such treatment is working against the main advantage of introducing the damascene process of Cu deposits and makes difference in resistivity between aluminum and copper smaller. Therefore, optimizing electroplating conditions by taking into account the substrate texture is critical for optimizing the texture and morphology of the electrodeposits.

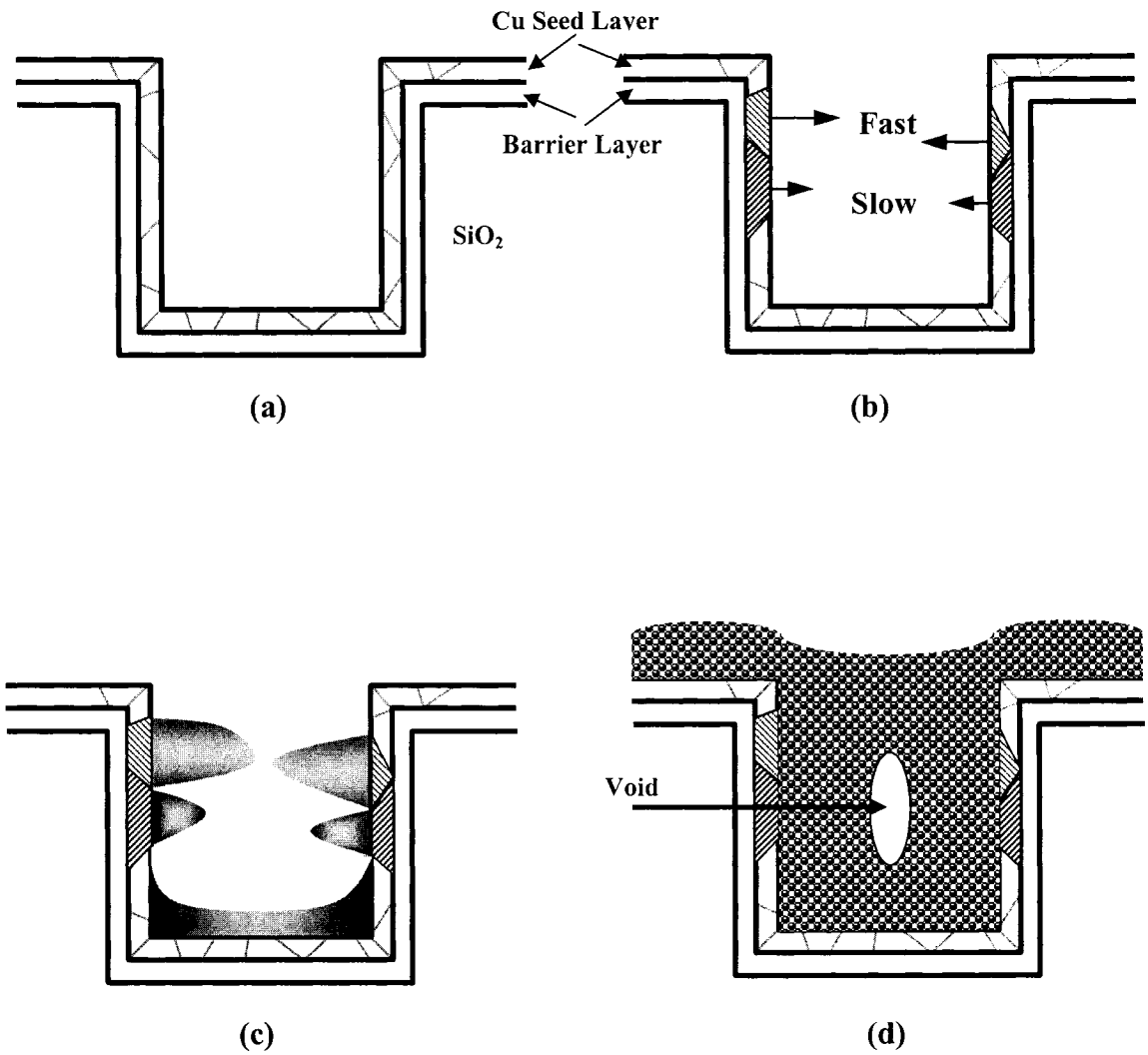
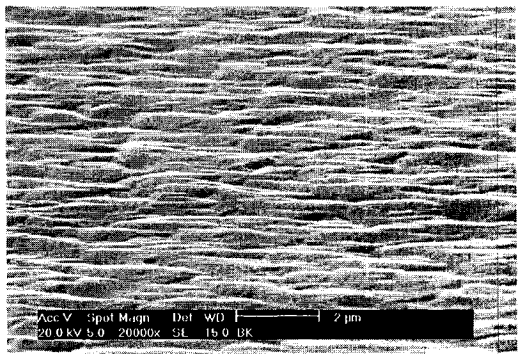
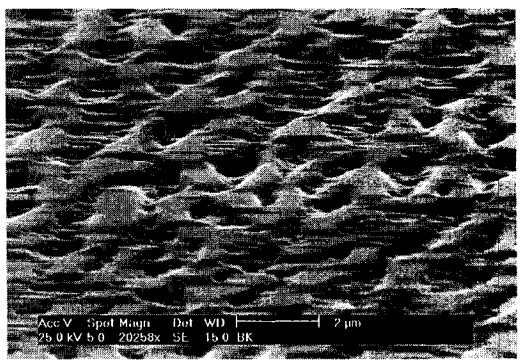


Figure 4.14. Schematic illustration of void formation in the trench due to irregular growth rate of grains.

(100)



(110)



(111)

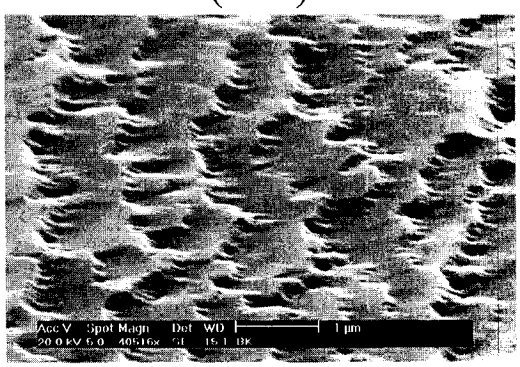
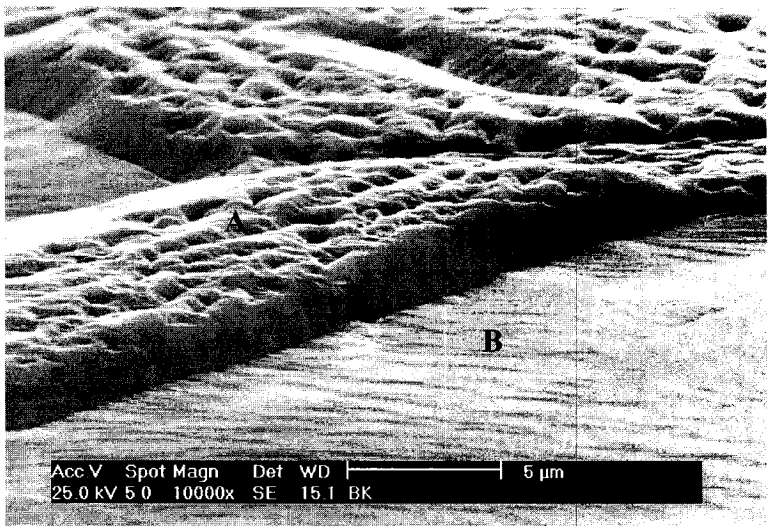
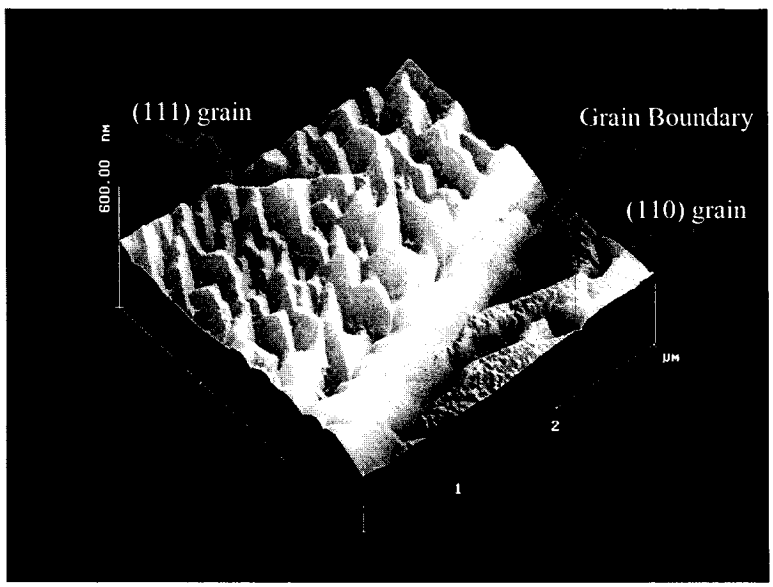


Figure 4.15. Surface morphology after Cu electroplating on the single crystalline copper substrates: (100), (110), and (111).



(a)



(b)

Figure 4.16. Surface morphology observations after copper electroplating on polycrystalline copper substrate: (a) SEM image, (b) AFM image.

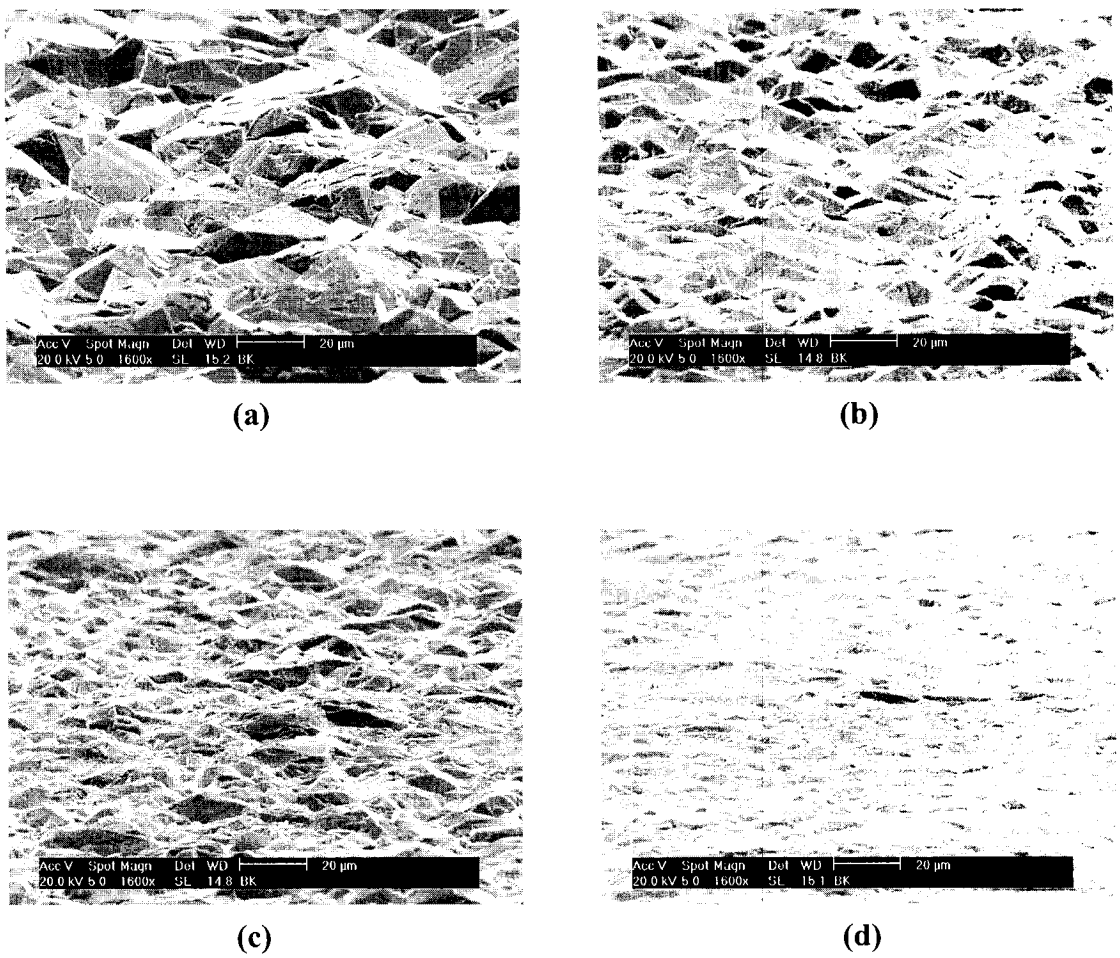


Figure 4.17. Morphology of the surface evolution after copper electroplating on polycrystalline specimen (Po8) using different current density: (a) 1 mA/cm^2, (b) 10 mA/cm^2, (c) 100 mA/cm^2, (d) 1000 mA/cm^2.

4.5. Summary

In this study, the influence of substrate texture and electroplating conditions on the texture and surface morphology of electrodeposits is investigated. It was demonstrated that the substrate texture plays an important role in formation of texture of electrodeposits and surface morphology of the electrodeposits. Three different polycrystalline copper substrates were used and the electrodeposits are plated with different current densities. In a specimen with a weak {110} texture, the texture increase in strength when electroplating was carried with 1000 mA/cm^2 current density. However, in a specimen having a strong {100} texture, the texture strength increased when plating with 1 mA/cm^2 current density. In Po9 sample, which has a strong {111} and a weak {100} texture, the strength of the {111} decreases as the current density increases. The examination of the cross-sections of electrodeposits by OIM demonstrated that the number fraction of $\Sigma 3$ boundaries increased as current density increased. Using SEM and AFM data it was demonstrated that grains of different orientations have different growth rate and produce a rough morphology at a low current density. The surface of electrodeposits is smoother when the current density is high and this minimizes the effect of substrate texture on the surface morphology. Taking into account texture of the substrate is important since the reliability of Cu damascene interconnects can be affected by both the texture and difference in rate of growth of electrodeposits.

Chapter 5

The Effects of Line Width on Textural and Microstructural Evolution of Copper Damascene Interconnects

In order to understand the effect of line width on textural and microstructural evolution of Cu damascene interconnects, three Cu interconnects samples which have a different line width were investigated. According to x-ray diffraction results, (111) plane was parallel to the interconnect surface in all investigated lines. {111}<110> texture was developed in 2 μm width interconnect lines and scattered {111}<112> and {111}<110> texture component were present in 0.18 μm width interconnect lines. The directional changes of (111) plane orientation with decreased line width were investigated by x-ray diffraction. In addition, microstructure and GBCD (grain boundary character distribution) in Cu interconnects were investigated using electron backscattered diffraction (EBSD) techniques. This measurement demonstrated that a polygranular structure is developed in

the wide line and bamboo-like microstructure is developed in the narrow line. The fraction of Σ3 boundaries is decreased as the line width decreases but is increased in the blanket film. A new interpretation of textural evolution in damascene interconnects lines having different line width is suggested, based on the constraints of sidewalls, surface/interface energy and the state of stress in the trench.

5.1. Experimental Procedure

5.1.1. Sample Preparation

Three copper damascene lines in TEOS (tetraethylorthosilicate) oxide having different line widths from 0.18 to 2 μm all having a trench depth of 0.5 μm, and one copper blanket film were investigated. These are listed in Table 5.1. 400Å thick TaN was deposited on the surface of single crystalline Si (100) wafer as the barrier layer, a copper seedlayer and then copper electrodeposits are deposited by electroplating on the top of the barrier layer, as shown in Figure 5.1a. After CMP (chemical mechanical polishing) process was used to remove the overburden of Cu electrodeposits and to prepare a smooth surface, the overlayers of 7000Å SiN and TEOS oxide were deposited on the top of Cu interconnects (Figure 5.1b). The Cu damascene lines and the blanket film were fabricated using the same processing conditions. The passivation layer had to be removed to reveal the underlying interconnect lines for investigation of the microstructure and grain boundary character distribution using orientation imaging microscopy (OIM). It was found that etching in 15% HF for 5 to 10 minutes allows the removal of the top passivation layer without causing damage to the copper interconnect lines.

Table 5.1. Details of the investigated samples.

Line Width	**0.18 μm**	**0.25 μm**	**2 μm**	**Blanket**
Intervals	0.2 μm	0.3 μm	2 μm	Encapsulated by Silicon Nitride and TEOS oxide on the top surface
Size	8468 × 9536 μm	8469 × 9505 μm	8478 × 9034 μm	
Number of Line	22302 lines horizontally and 19 vertically	15408 lines horizontally and 19 vertically	2119 lines horizontally and 19 vertically	

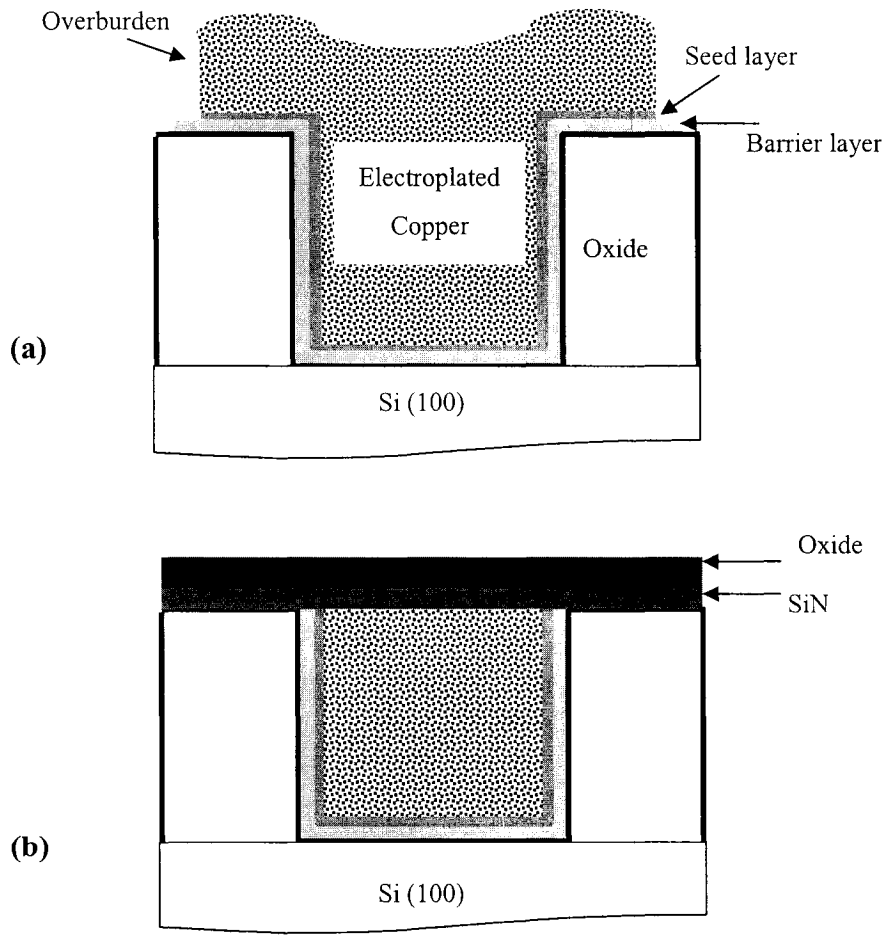


Figure 5.1. An illustration of the fabrication of Cu damascene lines: (a) Cu after electroplating, (b) the silicon nitride layer and the oxide after CMP.

5.1.2. Analysis of Texture, Microstructure and Stress

To obtain direct, quantitative information on the sample surface texture, diffracted intensity measurements were performed at low grazing incidence angle using Rigaku X-ray diffractometer. The crystallographic texture of copper interconnects was measured using a Siemens D500 x-ray goniometer with copper tube and analyzed using TexTools v.3.2.

To analyze the changes of microstructure as the line width decreases in the copper interconnects and blanket film, OIM mounted on a Philips XL30 FEG-SEM was used.

In order to analyze the impact of line width on the stress distribution, the cross-sectional stress distributions as the line width decreases are calculated using finite element method (FEM). For this calculation, a commercial software, ABAQUS v.5.8. was used.

5.2. Texture of Copper Damascene Interconnects

Crystallographic texture of copper damascene interconnects was analyzed with x-ray diffraction (XRD) and electron backscattered diffraction (EBSD) techniques. However, the XRD method was used in this texture analysis since it allows to acquire more statistically reliable information about texture than EBSD [56, 90]. Therefore, orientation imaging microscopy (OIM) was used only for analysis of microstructure and GBCD (grain boundary character distribution) of copper damascene interconnects.

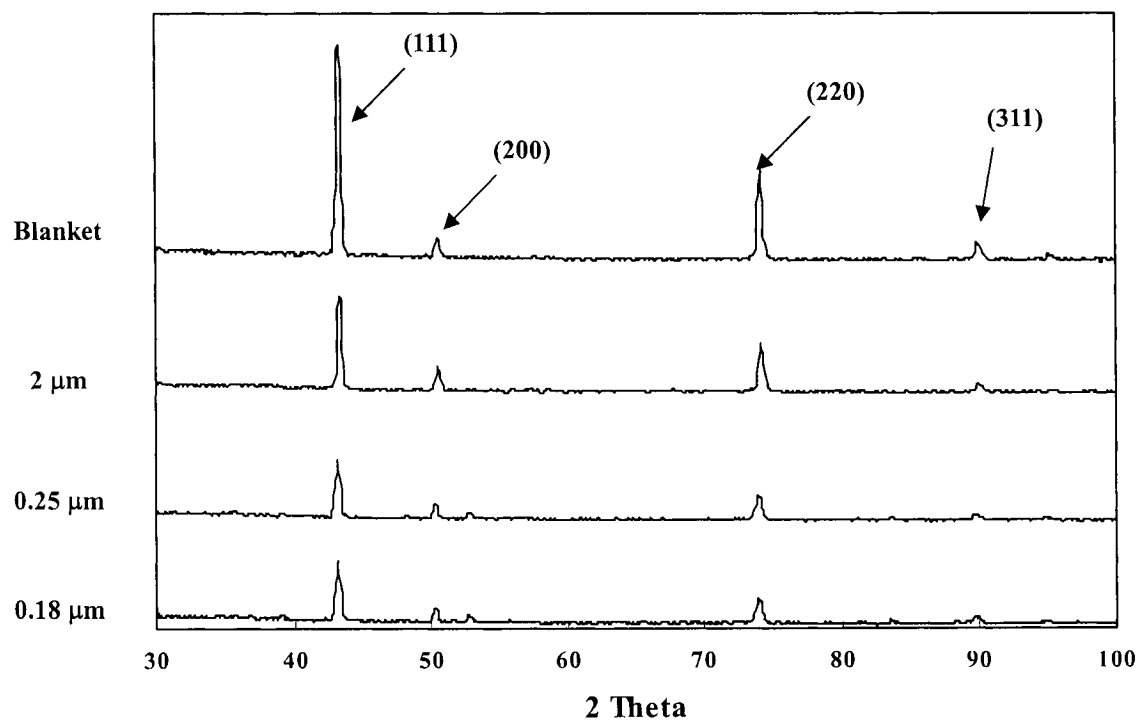


Figure 5.2. XRD θ-2θ scan obtained using grazing incidence diffraction geometry.

In order to analyze the changes of texture in copper interconnects as line width increases, XRD scan using the grazing beam incidence geometry were performed, as shown in Figure 5.2. In spite of a relatively weak texture, it seems that {111} component is dominant in all the samples. To obtain quantitative information about texture of Cu damascene interconnects, three pole figures were measured, ODF (orientation distribution function) were calculated and the same pole figures were re-calculated from the ODF. The results presented in Figure 5.3, indicate that weak {111} fiber texture exist in all samples, however its intensity is slightly increased as the line width decreases. There is no clear trace of sidewall growth of {111} component. From the (220) pole figure, directional texture development in the Cu damascene lines can be observed. From the Figure 5.3, one can conclude that the texture is a weak {111} fiber texture with a preference of certain crystallographic directions along the line of 0.18, 0.25 and 2 μm width interconnects.

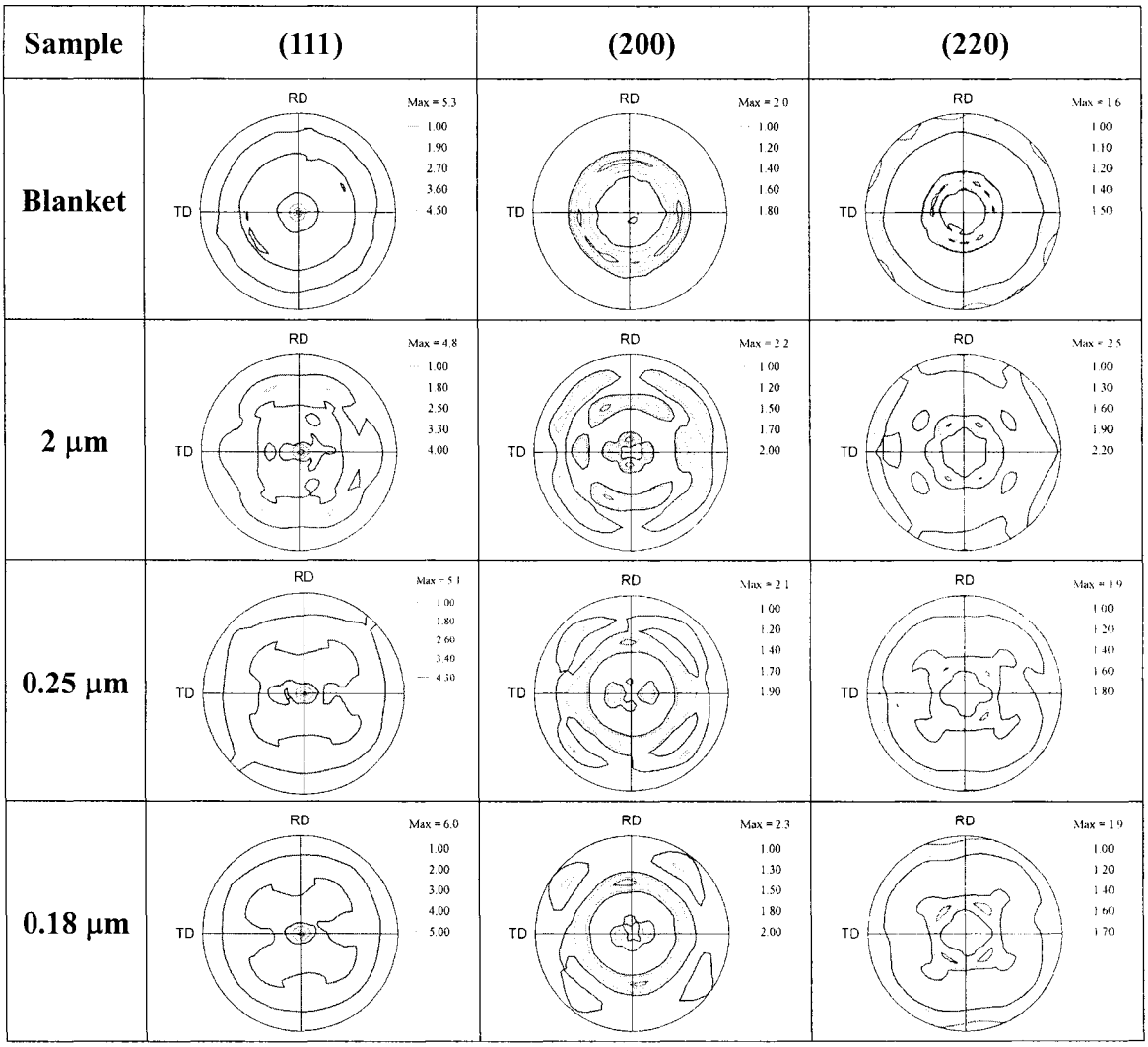


Figure 5.3. Pole figures of copper interconnect having a different line width.

To get more detailed textural information on the directional changes of {111} texture as the line width increases, the ODF (orientation distribution function) was calculated and {111} fiber texture was plotted, as shown in Figure 5.4. This figure shows ODF at $\varphi_2 = 45°$ section and illustrates changes of the intensity along the {111} fiber as the line width decreases. In this figure, it was found that the {111}<uvw> characterizes well the most important aspects of texture evolution as the line width decreases, in particular a strong maximum develops in the 2 μm line, for the {111}<110> ideal orientation (Figure 5.4a). This strong maximum moves to other orientations, such as $(111)[2\bar{3}1]$, $(111)[\bar{1}\bar{1}2]$ and $(111)[0\bar{1}1]$, in 0.24 μm line width interconnects (Figure 5.4b). In the 0.18 μm line width, it is clearly demonstrated that the {111} fiber has a rather scattered maximum intensity at $(111)[1\bar{1}0]$, $(111)[1\bar{1}2]$ and $(111)[1\bar{4}5]$ orientations as indicated by the arrows (Figure 5.4c).

In addition, some minor texture components are detected as the line width decreases. Figure 5.5 show that the minor components have {115} or {114} planes parallel to the specimen surface and these orientations can be produced by twin formation. The intensity of minor texture components decreases as the line width decreases. This finding will be further supported by EBSD investigation.

The obtained results demonstrate that the {111} plane is parallel to the Cu interconnects surface for different line width, however, the direction <uvw> parallel to line directions varies. The mechanism of transformation of texture as the line width changes will be discussed later in this chapter.

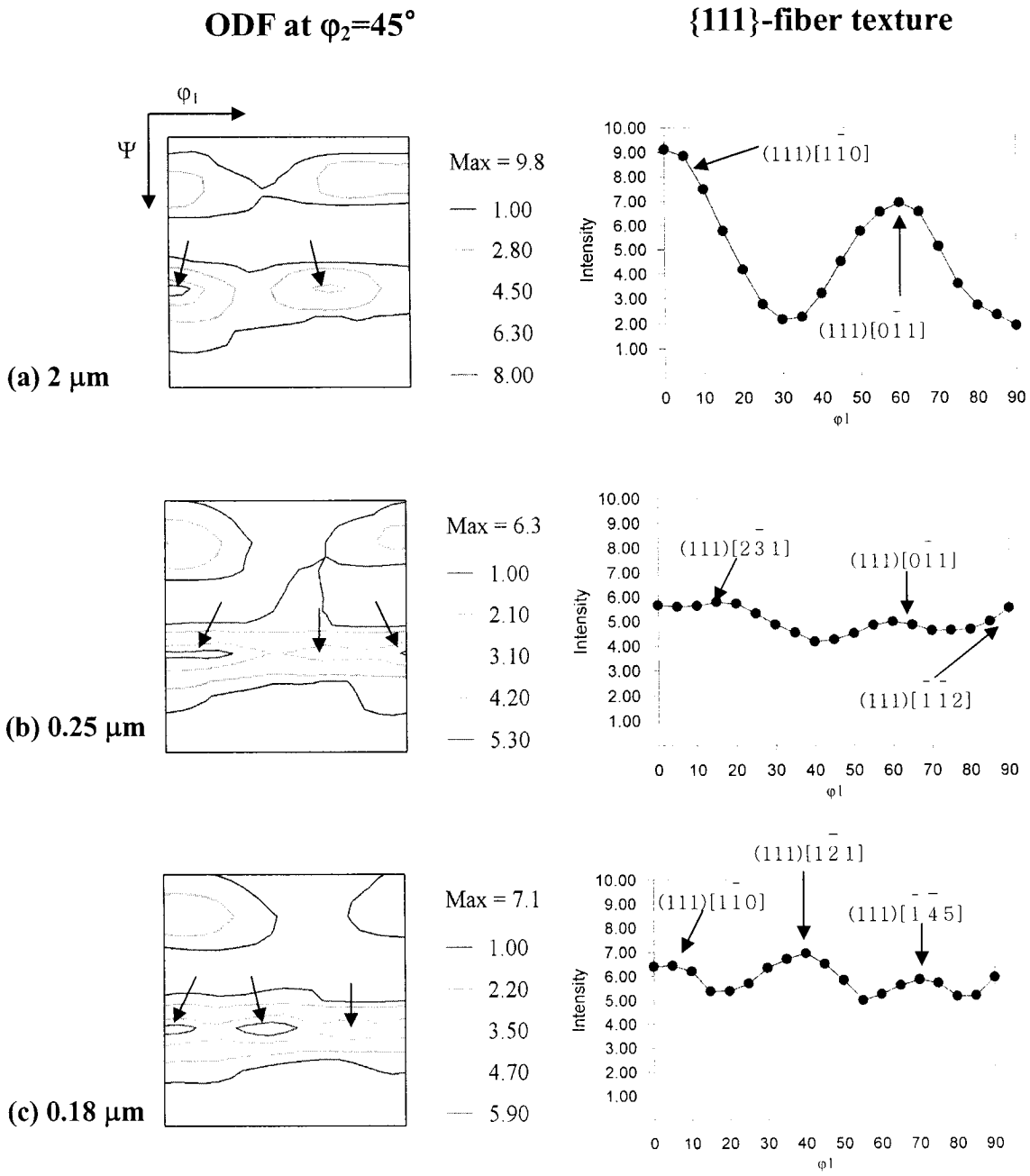
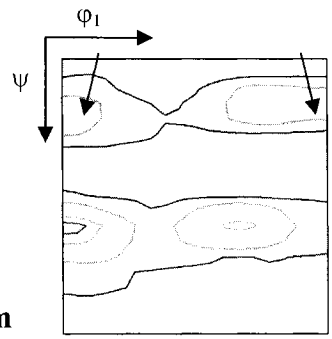


Figure 5.4. Sections of ODFs for $\varphi_2 = 45°$ and {111} fiber plots: (a) 2 μm, (b) 0.25 μm, (c) 0.18 μm.

ODF at φ_2=45°

Minor Components

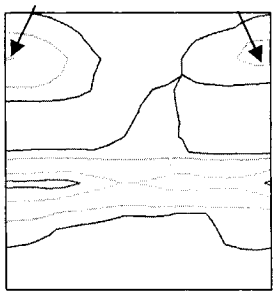
(a) 2 μm



Max = 9.8
1.00
2.80
4.50
6.30
8.00

Texture	Intensity
(114)[1$\bar{1}$0]	4.4
(115)[$\bar{1}$ $\bar{4}$ 0]	4.2

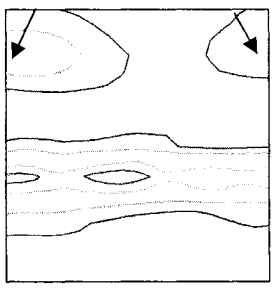
(b) 0.25 μm



Max = 6.3
1.00
2.10
3.10
4.20
5.30

Texture	Intensity
(115)[1$\bar{1}$0]	4.2
(115)[$\bar{2}$ $\bar{3}$ 0]	2.4

(c) 0.18 μm



Max = 7.1
1.00
2.20
3.50
4.70
5.90

Texture	Intensity
(115)[1$\bar{1}$0]	3.5
(115)[$\bar{2}$ $\bar{3}$ 0]	2.2

Figure 5.5. Minor texture components in the interconnect trench for different line width: (a) 2 μm, (b) 0.25 μm, (c) 0.18 μm.

5.3. Microstructure and GBCD of Copper Damascene Interconnects

To identify the orientation of grains and types of grain boundaries in the copper interconnect lines and the blanket film, inverse pole figure maps were constructed using EBSD technique (see Figure 5.6). These maps demonstrate that the blanket film and 2 μm line width sample has typical polycrystalline structure with a mixture of large and small grains, as shown in Figure 5.6a and b. However, semi-bamboo structure is observed in 0.25 μm line width Cu interconnects sample (Figure 5.6c) and bamboo-like microstructure is found in 0.18 μm line width interconnects (Figure 5.6d)

In addition, the GBCD (grain boundary character distribution) was analyzed using the EBSD results. Figure 5.7 shows the variation of low angle grain boundary representing misorientation less than 15°, with different line width. In this figure, the fraction of low angle grain boundaries increases as line width decreases, but it is high in the blanket film. The frequency of CSL (coincidence site lattice) boundaries were also measured using EBSD technique, as shown in Figure 5.8, and the results obtained clearly demonstrate that the fraction of Σ3, Σ9 and Σ27 boundaries decreases as line width decreases. The highest fraction of these twin boundaries is observed in the 2 μm line.

From these results, one can say that the microstructure and the grain boundary character distribution of Cu interconnects are different for different line width.

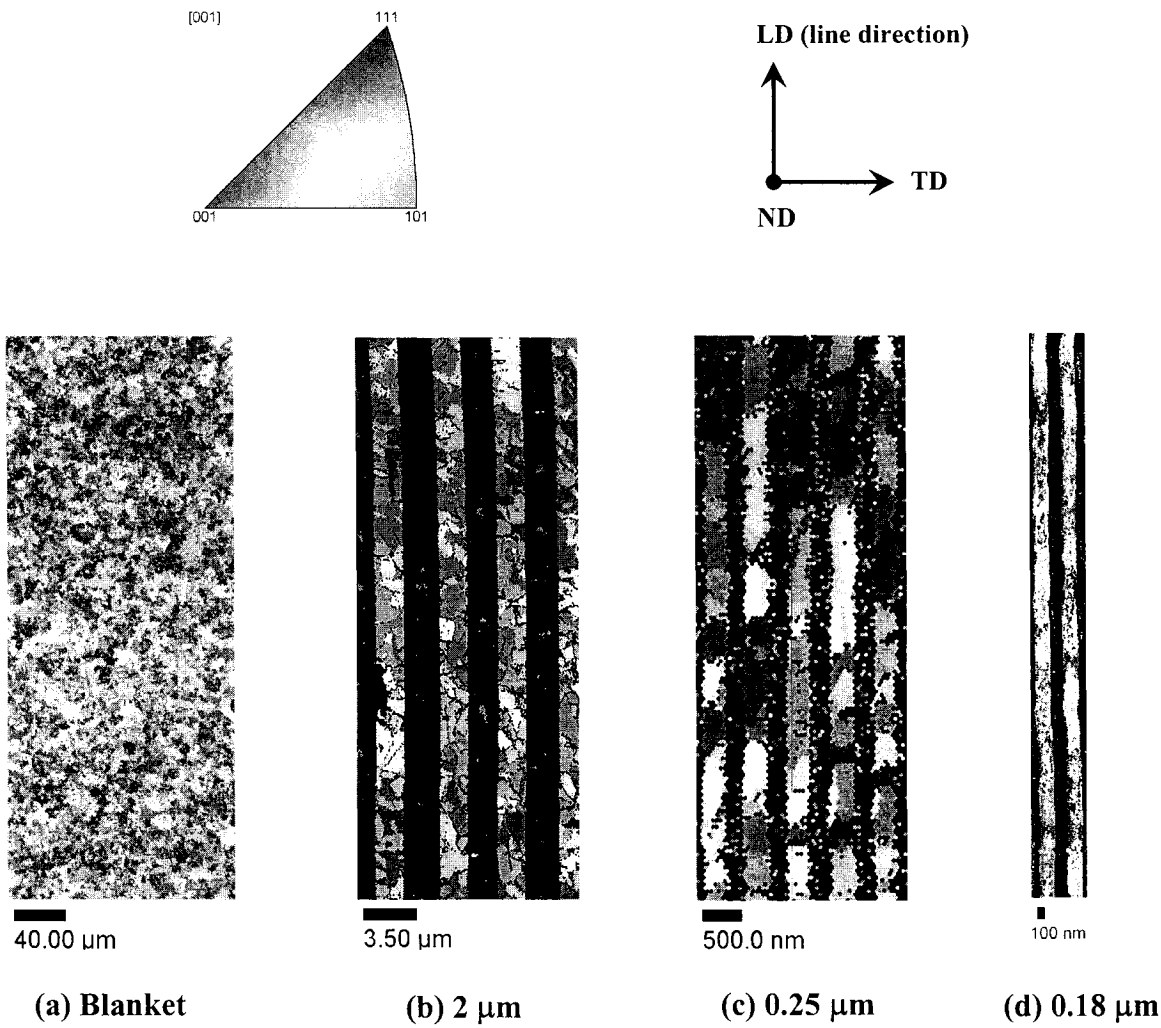


Figure 5.6. Inverse pole colored map representing orientation of planes parallel to the surface of the interconnect lines: (a) blanket film, (b) 2 µm, (c) 0.25 µm, (d) 0.18 µm line width.

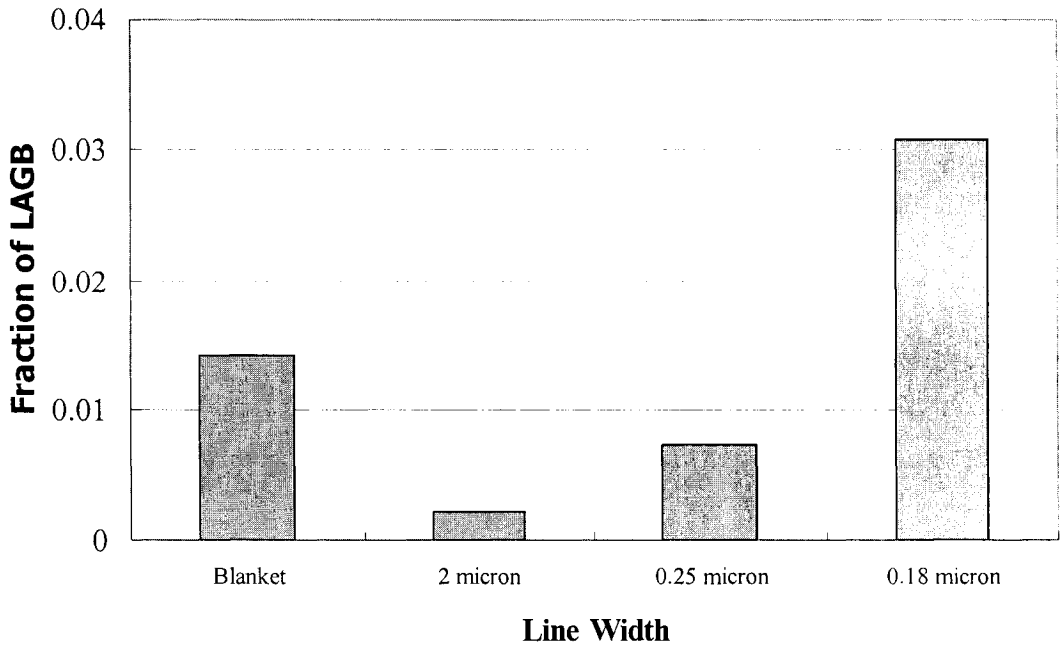


Figure 5.7. Fraction of low angle grain boundaries in Cu interconnects lines having different line width.

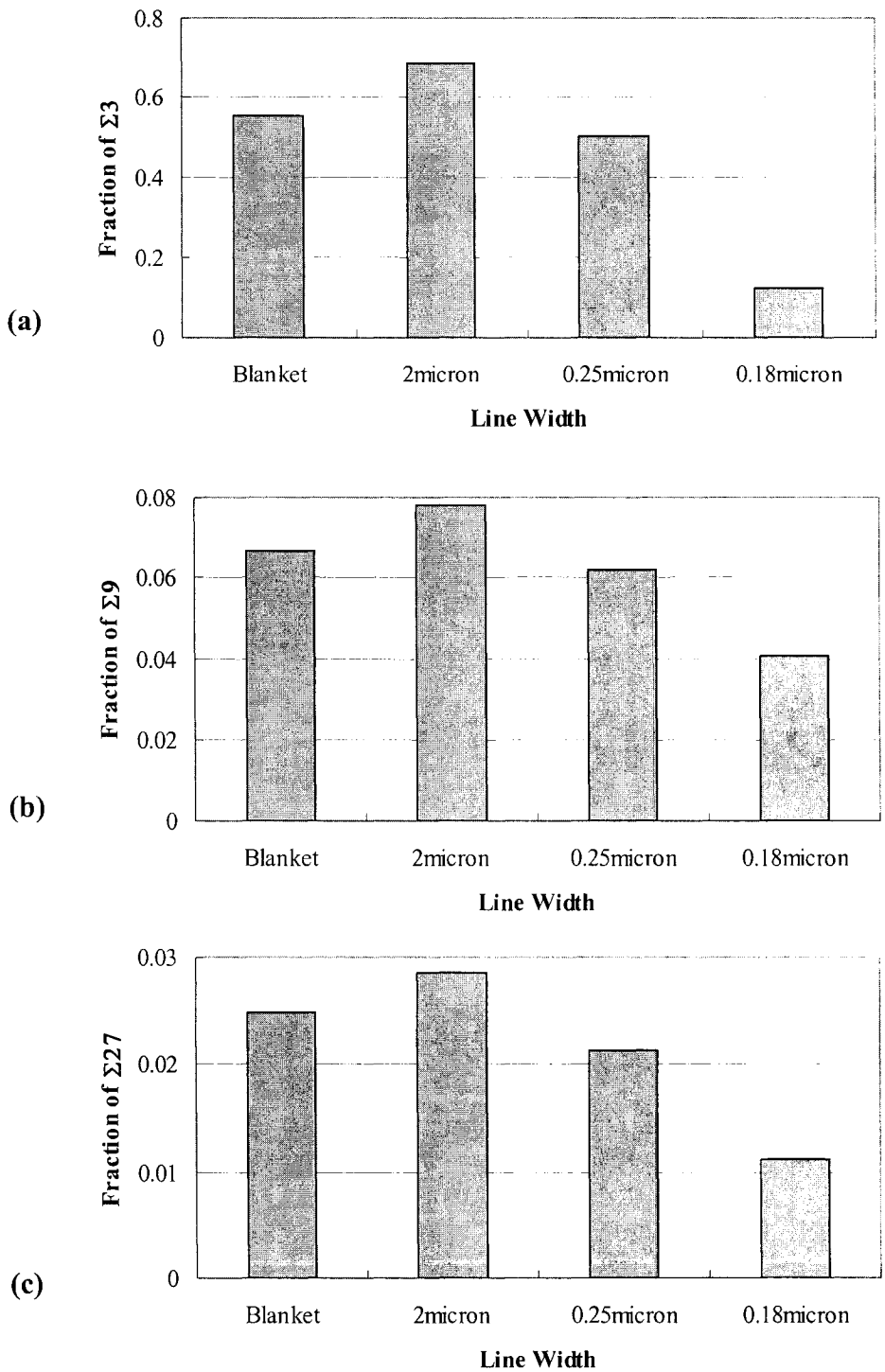


Figure 5.8. Fraction of (a) Σ3, (b) Σ9 and (c) Σ27 CSL boundaries in Cu interconnects lines having different line width.

5.4. Discussion

It is difficult to propose a precise interpretation of texture transformation after electroplating, since this texture cannot be easily measured and it is transformed even at room temperature [91-95] and then further changed as a result of the annealing which is done during one of the fabrication stages. In this discussion, possible effects of sidewall constraints, the surface/interface energy, the stresses and the substrate orientation on the texture evolution of Cu damascene interconnects are presented.

In order to represent the textural evolution of Cu damascene interconnects as the line width decreases, a schematic illustration is presented with {111} fiber texture plot, in Figure 5.9. This schematic illustration shows two kinds of {111}<110> texture components (A and B: φ_1=0, 60°) in the 2 μm Cu interconnects. These components represent different rotation directions (A_1 and A_2 and B_1 and B_2), clockwise and anti-clockwise with respect to the direction normal to the specimen surface. As these texture components rotate, the intensity of {111}<110> texture decreases and {111}<112> texture increases (Figure 5.9a). Directional rotation angles between the line direction and <110> direction are approximately 13 and 22° for the 0.25 and 0.18 μm line width respectively. Accordingly, one can say that two texture components which have different rotational direction can make a strong or weak texture in the Cu damascene interconnects as the line width decreases.

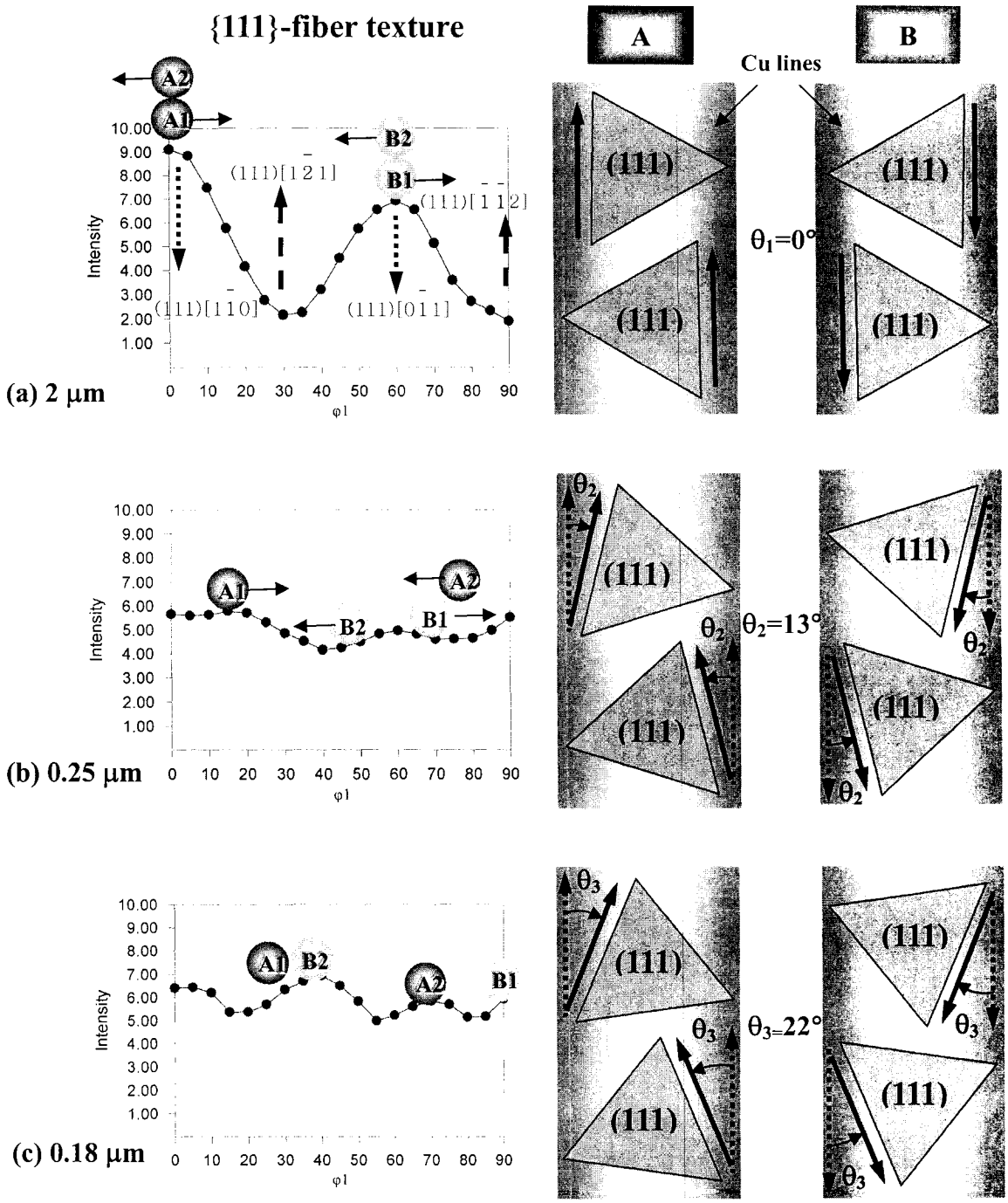


Figure 5.9. The schematic illustration of the texture changes in the specimens with different line width: (a) 2 μm, (b) 0.25 μm, (c) 0.18 μm.

These textural differences of the Cu damascene interconnects having different line width must be related to the different states of stress. It is rather obvious that the texture of copper interconnects develops under thermal stress which is generated during the fabrication process. We observe that changes in the texture of the damascened copper depends on the aspect ratio (the ratio of depth and width of interconnect line). Figure 5.10 shows the thermal stress (S_{11}) distribution in damascene copper with different line width at 400°C. This was calculated by FEM under the assumption that the copper deposit has isotropic mechanical properties, the expansion coefficients of surrounding silicon and TEOS oxide are small compared to that of copper, and the copper can expand freely along the normal direction (ND) of the trench. Therefore, the data presented in Figure 5.10 should be considered as a qualitative representation of the stress changes. It can be seen from the data in Figure 5.10 that the thermal stresses are compressive and the location of the maximum value of S_{11} moves from the corner of the trench width to the middle in the bottom. Figure 5.11 shows stresses along the trench width S_{11}, depth S_{22} and length S_{33} as a function of distance from the surface center. The absolute magnitudes of the stresses along the trench width and length are respectively the largest and the second largest in the bottom region of trench and are opposite in the upper region. This is attributed to the fact that constraints along the trench depth are larger in the bottom region than in the upper region. One can assume that the stress along the trench width would be increasingly dominant as the aspect ratio of the trench increases, because the constraints along the trench depth would increase with increasing aspect ratio. Since the sidewall constraints are increased as the line width decreases, these can be considered as main factors affecting texture evolution in Cu damascene interconnects as the line width decreases.

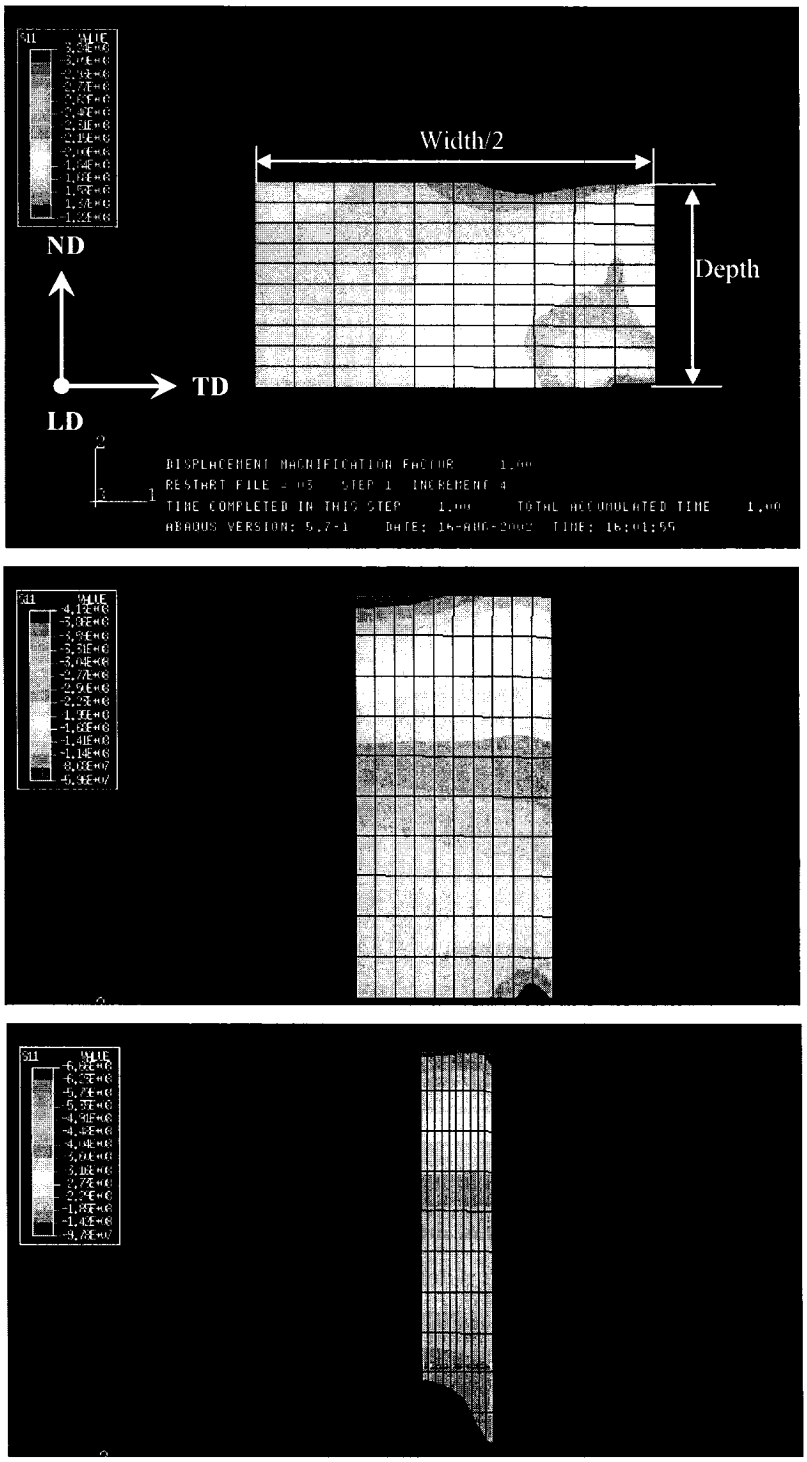
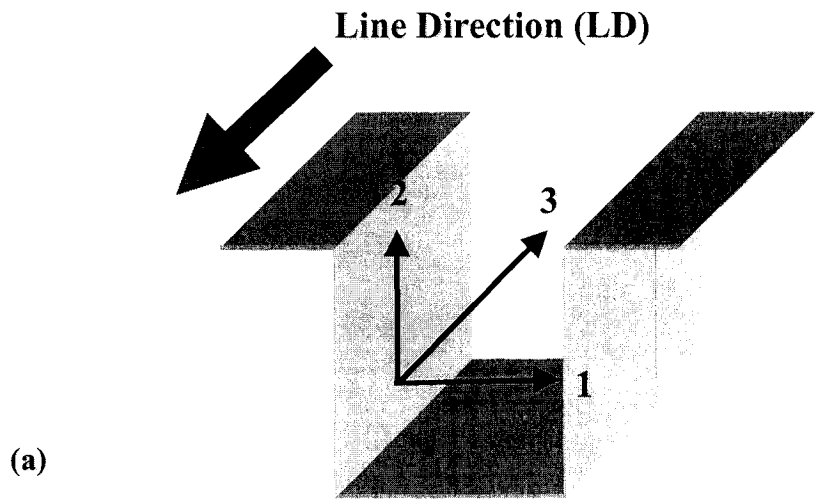
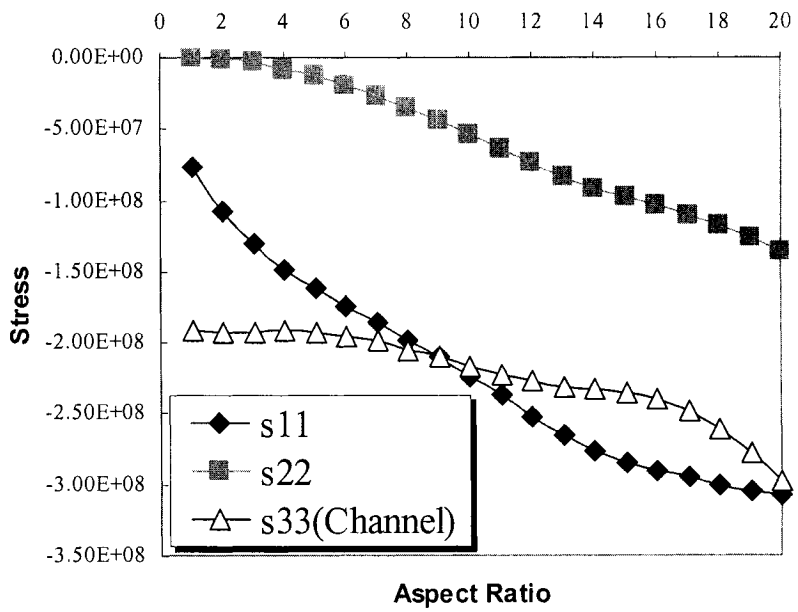


Figure 5.10. Distribution of S_{11} which indicates stress along the width direction of the trench in the cross-section of damascened copper interconnects: (a) 2 μm, (b) 0.5 μm, (c) 0.18 μm line width.



(a)



(b)

Figure 5.11. Stress distribution along the copper interconnects: (a) the schematic illustration of the stress axis, (b) stress changes as function of the aspect ratio along width S_{11}, depth S_{22}, and length S_{33} of the interconnect line.

Another way of explaining the development of texture in the different line width is that at first, it can be assumed that the texture components in the copper trench can be classified as "sidewall" and "bottom" components roughly, as shown in Figure 5.12. In previous research [10, 16-18, 22], it was confirmed that in super-conformal filling, the growth from the bottom of the trench should be dominant over the growth from the sidewall to eliminate possibilities of void formation in the Cu trench. Considering this super-conformal filling, the bottom component contribution to overall texture is greater than the sidewall component in the 2 μm line, therefore the {111}<110> texture component should be decided as the bottom texture component in 2 μm line width interconnects (Table 5.2). Through this, the other texture components can be consider as the sidewall texture components as shown in Table 5.2.

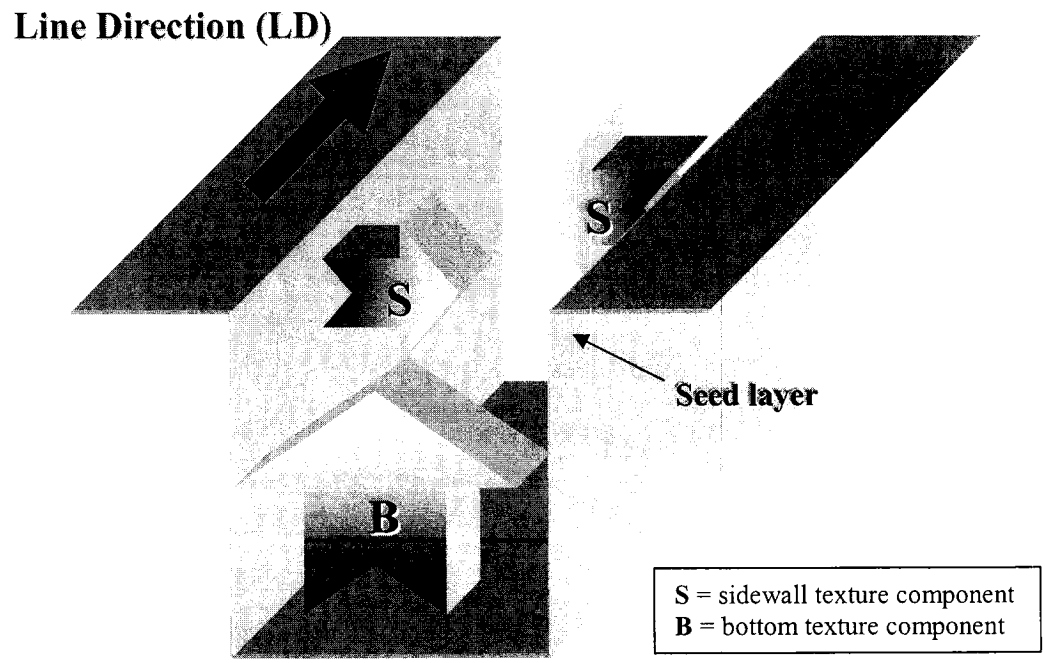


Figure 5.12. The schematic illustration of the classification of texture component in the Cu damascene interconnects.

Table 5.2. The classification of texture components in the copper interconnects.

	2 μm	**0.25 μm**	**0.18 μm**
Bottom (B)	{111}<110>	{111}<110>	{111}<110>
Sidewalls (S)	-	{111}<123> {111}<112>	{111}<112> {111}<145>

Another possible explanation of the {111}<110> texture development in the electrodeposits might be related to the strong influence of the substrate texture which was found in Chapter 4. The support for this explanation is found in the texture of the blanket film. Without this substrate-electrodeposits epitaxial relationship, the texture of the copper film should be the fiber type texture. However, it is found that the texture of the blanket film shows some peaks in the ODF space, as shown in Figure 5.3 and 5.13a. To see this more clearly, the {111} fiber of the blanket film was plotted in Figure 5.13b and the {111}<110> and {111}<112> texture components along the {111} fiber texture were indicated by arrows. To produce this blanket film sample, a TaN barrier layer was deposited on the surface of a single crystalline Si (100) wafer, and then a copper seedlayer and copper electrodeposits were deposited on the top of the barrier layer. As shown in Figure 5.14, the single crystalline Si substrate has {100}<110> orientation which may through epitaxial relationship support the growth of the {111}<110> texture.

The 2 μm interconnect line has a polycrystalline structure. The grains at the interface are free to be oriented with the <110> direction parallel to the line length

because of less constraints by sidewalls. In addition, any 60° rotation around <111> axis will create the grain orientation that is a twin to that original grain. In this way, minimization of the total energy of the system will be realized by creating the polycrystalline structure with a high density of twin (secondary twin etc.) boundaries [96-99]. Figure 5.8 illustrates a significant increase in the fraction of twin boundaries as interconnect line width increases. This also can be related with the strongest texture formation in the narrow line since multiple twinning contributes to texture randomization [100-104]. However, the fraction of twin boundaries is decreased in the blanket film. It can be explained that the blanket film presents less driving force, such as stress and/or interface energy for the formation of twins during the fabrication process.

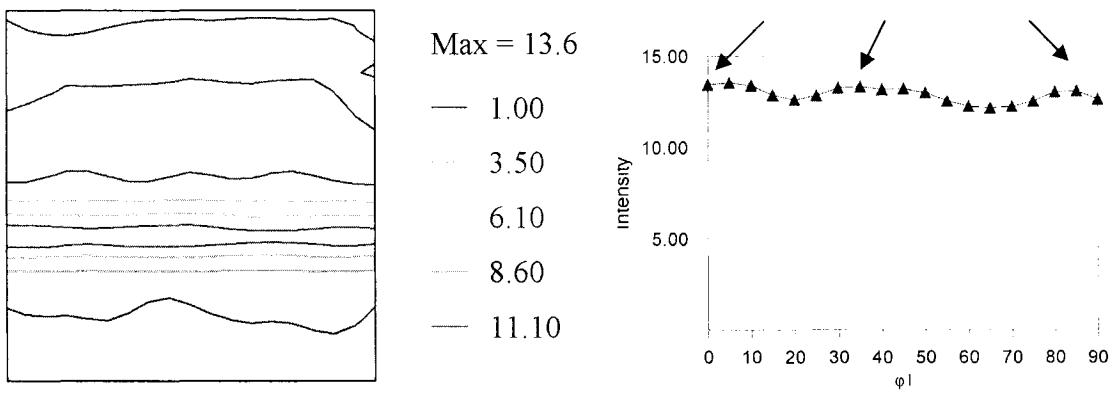


Figure 5.13. Texture of the copper blanket film: (a) ODF section for $\varphi_2 = 45°$, (b) {111} fiber plot.

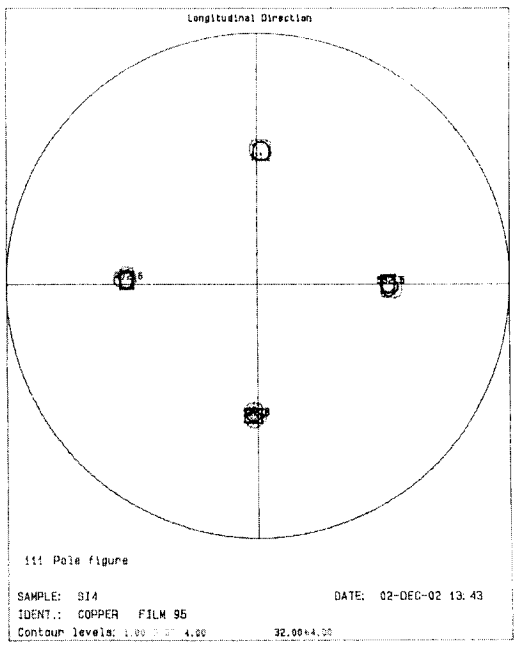


Figure 5.14. (111) pole figure of single crystalline Si (100) wafer.

5.5. Summary

Significant differences were registered in texture of Cu damascene interconnect lines of different widths. These differences are contained within the {111}<uvw> fiber orientation. For the 0.18 μm line, no strong tendency of alignment with any crystallographic direction along the interconnect length is observed, while the {111}<110> texture is dominant in 2.0 μm interconnect line. This directional transformation of texture is gradual and takes place as the width of the line increases and can be described by the competition of the sidewall and bottom texture components in the

trench. Scattered {111}<112> and {111}<110>texture in the 0.18μm line width changes to a strong {111}<110> component in the 2 μm line width.

Differences in the structure of grains, grain boundary character distribution and fraction of twin boundaries are used to propose an interpretation based on difference in the compression stress relaxation in different interconnects during annealing to observed transformation of texture. The proposed interpretation of texture development assigns an important role to differences in the state of stress, but also demonstrates that the texture of copper electrodeposits may be inherited from the substrate texture. In the 2 μm line width the minimization of the energy of the system will generate a high number of twin type boundaries. Bamboo type structure was found in the 0.18 μm sample, however the 2 μm line width sample has polycrystalline structure. The fraction of Σ3 boundary is increased as line width increases, however it decreased in the blanket film.

Chapter 6

The Effects of Annealing Process on the Textural and Microstructural Evolution of Copper Damascene Interconnects

In order to understand the effects of annealing process on the textural and microstructural transformation of Cu interconnects having different line widths, two different samples, as-deposited and annealed at 200°C for 10 minutes, were investigated. Texture of Cu damascene interconnects which have different cross-sectional profiles after electropolishing was measured by x-ray diffraction and the top surface layer of Cu interconnects was investigated using EBSD (electron backscattered diffraction) techniques. To analyze the relationship between the stress distribution and textural evolution in the samples investigated during annealing, micro stress were calculated for the interconnects having different line width at 200°C using FEM (finite element method).

It was demonstrated that the inhomogeneity of stress distribution in Cu interconnects is an important factor which is necessary for understanding textural transformation during annealing. Interpretation of textural evolution in damascene interconnects lines after annealing is suggested, based on the state of stress and the growth mechanisms of Cu electrodeposits in the trench.

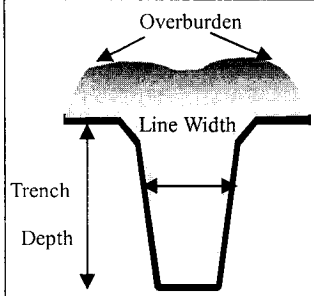
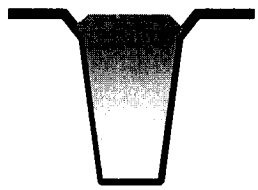
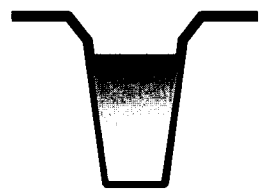
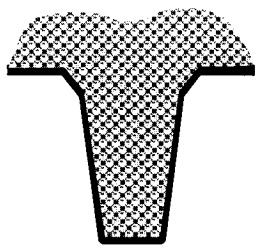
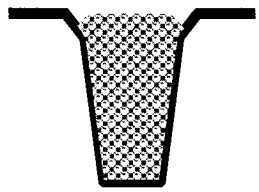
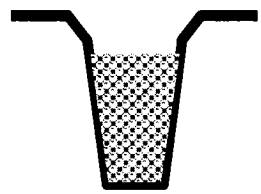
6.1. Experimental Procedure

6.1.1. Sample Preparation

Two kinds of samples which underwent different annealing processes, one as-deposited and another annealed having a different cross-sectional profile, were used for the x-ray texture measurement as shown in Table 6.1. Both samples were fabricated using the same conditions and were kept at room temperature for 6 months. 400Å thick TaN was deposited on the surface of the Si (100) wafer as a barrier layer, and then a copper seedlayer was deposited on the barrier layer. The trenches were then filled with copper by electroplating in a sulfuric acid bath using a 24 mA/cm^2 current density. To remove the overburden of Cu interconnects, the samples were electro-polished for 120 and 130 seconds respectively in a H_3PO_4 solution using a 17 mA/cm^2 current density. Then, they were annealed at 200°C for 10 minutes in the vacuum furnace to avoid oxide formation on top of Cu interconnects. Each sample has different line widths from 0.14 to 2 μm and every line has the same trench depth of 0.7 μm. After electropolishing for 120 seconds

(Table 6.1), the top surface area of the trench was analyzed using EBSD (electron backscattered diffraction) method.

Table 6.1. Schematic diagram of the cross-sectional profile of Cu interconnects.

	After Electroplating	**Electropolished**	
	Overburden ▲	**Top surface (120 sec) ■**	**Inside of trench (130 sec) ●**
As-deposited			
Annealed			

6.1.2. Analysis of Texture, Microstructure and Stress

To obtain quantitative information on texture from the sample surface, the crystallographic texture of copper interconnects was measured using a Siemens D500 system with x-ray goniometer with a copper tube. Three pole figures ((111), (200) and (220)) were obtained using the reflection technique, up to a maximum tilt of the specimen

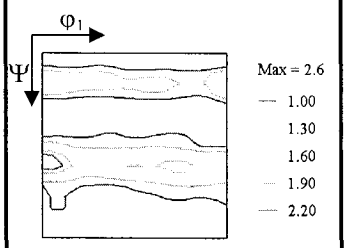
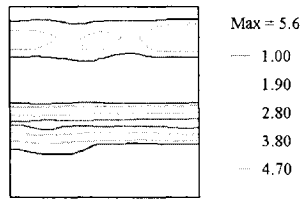
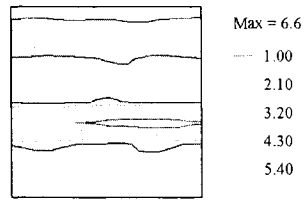
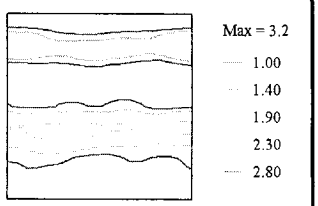
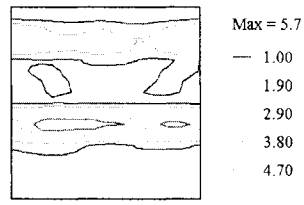
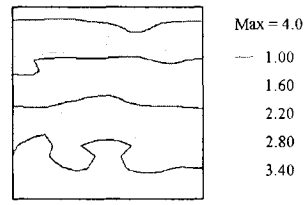
of 80 deg in 5 deg intervals. The orientation distribution function (ODF), {111} fiber texture and the percentage of different texture components were calculated using TexTools v.3.2, commercial software. To observe the details of microstructure evolution of Cu damascene interconnects after annealing process, OIM which is mounted on a Philips XL30 FEG-SEM was used.

The stress distribution on the top surface area of Cu damascene interconnects was calculated by FEM (finite element methods) using FEMLAB v.2.3a, commercial software.

6.2. Through Thickness Inhomogeneity of Texture in Copper Damascene Interconnects

In order to acquire quantitative information on the crystallographic texture of copper interconnects, x-ray diffraction (XRD) and electron backscattered diffraction (EBSD) techniques were used. Since the XRD method has a wide-range scan area and deeper scan depth than EBSD, it was used only to obtain an average through thickness information about texture and EBSD was used for the detailed analysis of texture, microstructure and grain boundary character distribution (GBCD) of copper interconnects on the top surface area for different line widths.

Table 6.2. Sections of ODFs for φ_2 = 45°at a different cross-sectional profile of Cu interconnects before and after electropolishing.

	Overburden▲ (after electroplating)	**After Electropolishing**	
		120 second■	**130 second●**
As-deposited			
Annealed			

To obtain quantitative information about the through thickness inhomogeneity of texture, three pole figures were measured and the ODF (orientation distribution functions) were calculated, as shown in Table 6.2. This table shows ODF at φ_2 = 45° section and illustrates the intensity changes of the {111} fiber texture at each cross-sectional profile of Cu electrodeposits in the trench: weak fiber texture was found after electroplating, however its intensity becomes stronger as it goes into the trench bottom of Cu interconnect in the "as-deposited" sample. After annealing, it was noticed that its intensity varies and some other texture components developed depending on the cross-sectional profile of Cu electrodeposits in the trench. To describe the details of these through thickness texture changes, the plots of {111} fiber at each cross-sectional profile are

shown in Figure 6.1. The texture of the as-deposited sample shows a weak {111} fiber, however, after removing the overburden layer of copper by electropolishing, the intensity of fiber texture increases. After annealing, the texture of the overburden layer does not change much, however, textures of the trench under this layer are transformed. At first, after electropolishing for 120 seconds which means removing of overburden of Cu electrodeposits only (Table 6.1), specific directions on the {111} fiber texture are developed as indicated by the arrows (Figure 6.1b). After electropolishing for 130 seconds which means removing of overburden and a half depth of Cu electrodeposits in the trench (Table 6.1), the {111} fiber texture component is decreased in strength and a weak (111) $[1\bar{1}0]$ texture is developed. This must be related to an increases of constraints generated by the sidewall of the trench and may affect the directional texture development of copper in the trench which was mentioned in Chapter 5. The obtained results demonstrate strong through thickness inhomogeneity of texture in the trench after annealing. The possible influence of the stress which is related to the sidewall constraints on the directional texture development of Cu interconnects will be discussed later.

In addition, a minor texture component described by the {115} fiber is detected as shown in Figure 6.2. In this figure, it is demonstrated that the intensity of {115} fiber after annealing increases at (115)$[1\bar{1}0]$, (115)$[0\bar{5}1]$ and (115)$[\bar{2}\,\bar{3}\,1]$ orientations as indicated by the arrows in Figure 6.2b. All minor components which have the {115} plane parallel to the specimen surface can develop as a result of twin formation during annealing. This finding is supported by high number of twin boundaries registered by EBSD. These obtained results also suggest that the through thickness texture of Cu interconnects is inhomogeneous in the trench. The mechanism of possible transformation of texture after annealing will be discussed later in this thesis.

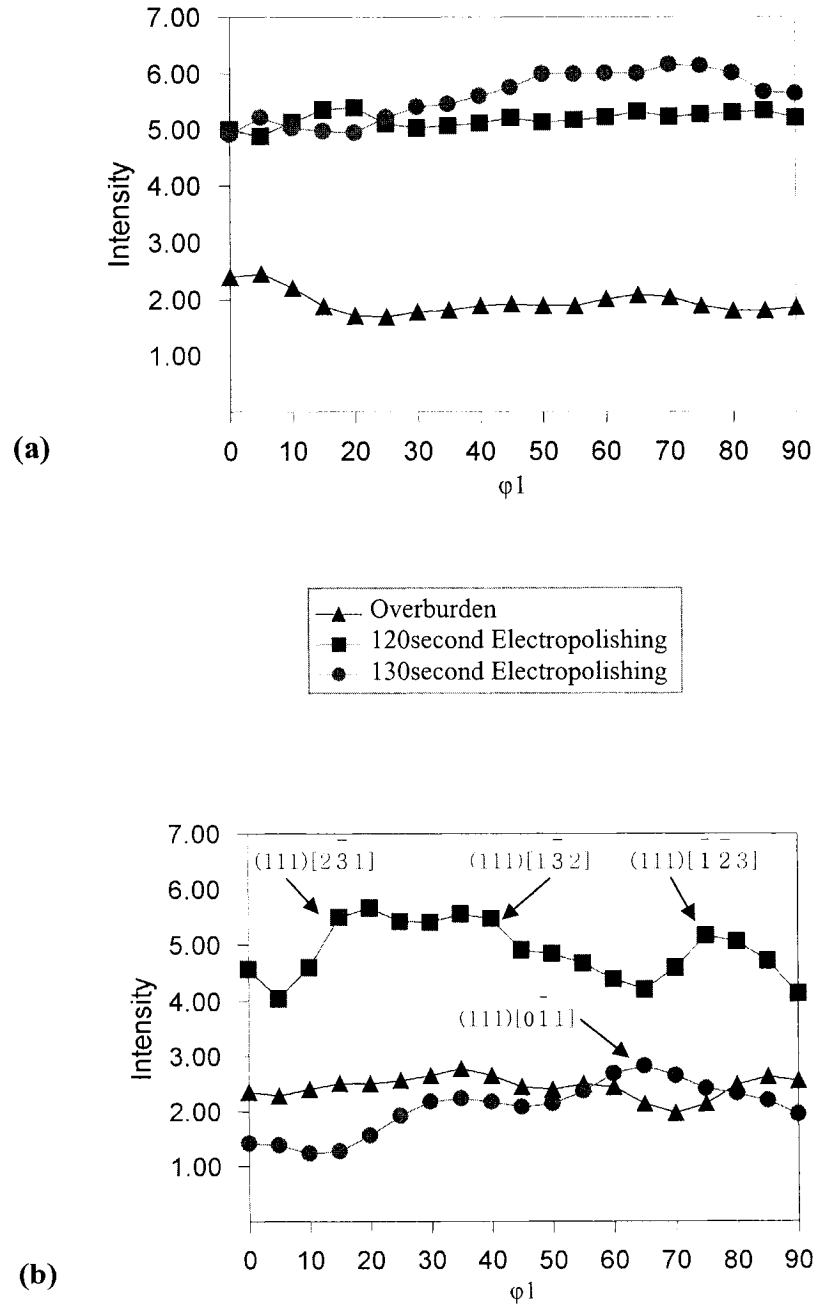
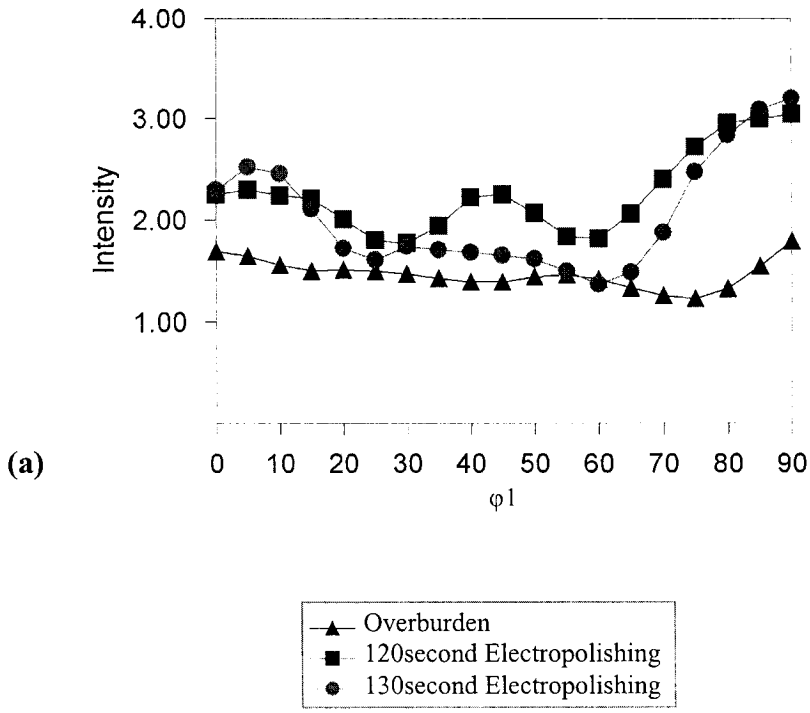
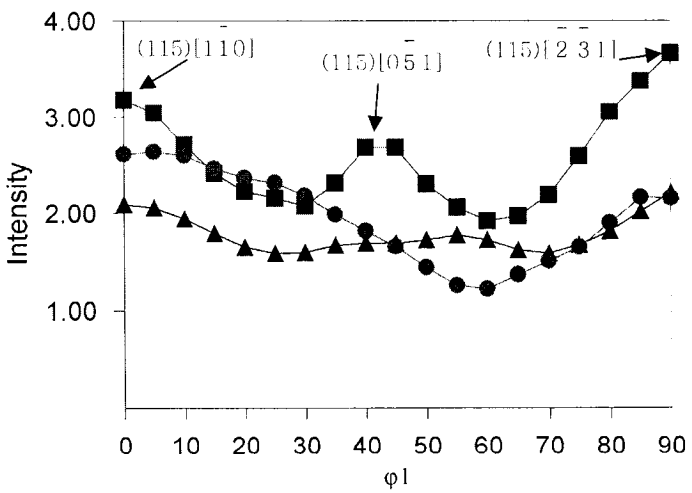


Figure 6.1. {111} fiber plots at the different cross-sectional profile of Cu interconnects: (a) as-deposited, (b) after 200°C annealing.



(a)



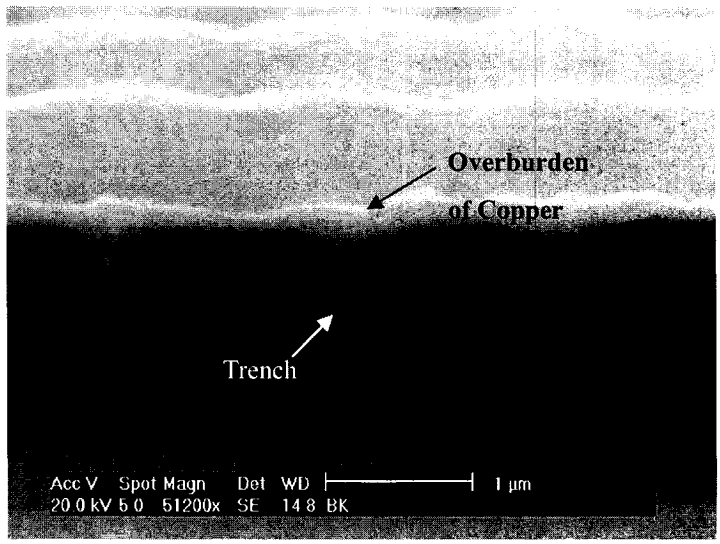
(b)

Figure 6.2. {115} fiber plots at the different cross-sectional profile of Cu interconnects: (a) as-deposited, (b) after 200°C annealing.

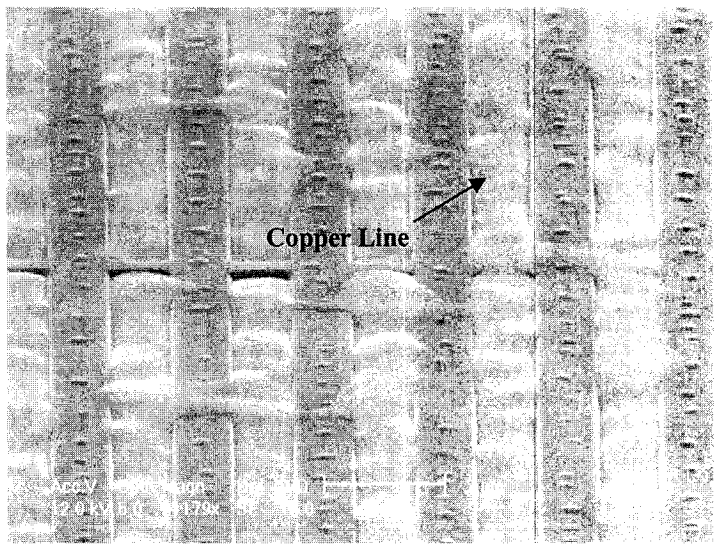
6.3. Texture, Microstructure and GBCD on the Top Surface Area of Copper Damascene Interconnects

6.3.1. Texture

After filling the trench by Cu electroplating, irregular surface morphology is generated, as shown in Figure 6.3a. To remove the overburden of copper and make the surface smooth, CMP (chemical-mechanical polishing) is performed in the industry. In this study, electropolishing was used to make a smooth surface of Cu interconnects and the EBSD technique is used to analyze the surface microstructure, the orientation of each grain, and types of grain boundaries in the copper interconnects. However, the results from a 130 second electropolishing are not reliable since it produces much more surface charge from the oxide layer than the 120 second electropolishing and cannot be interpreted accurately. Therefore, in this investigation, only a 120 second electropolished sample which comes from the top surface area of Cu interconnects was analyzed (Figure 6.3b).



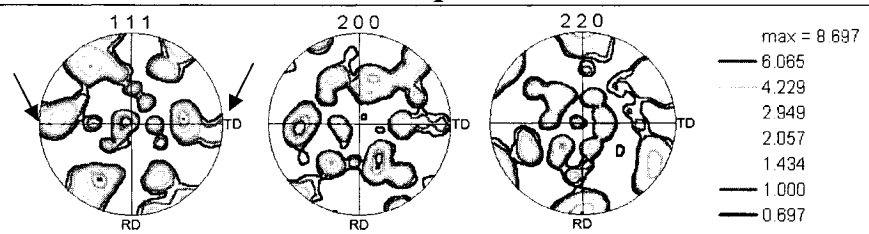
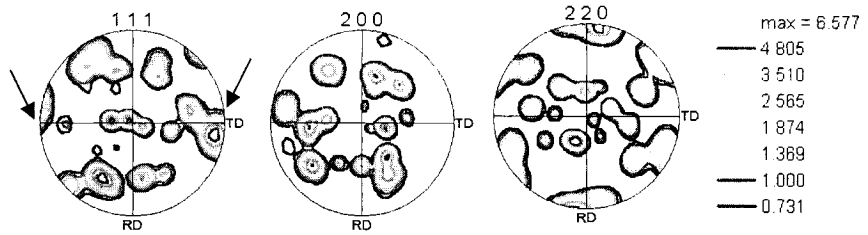
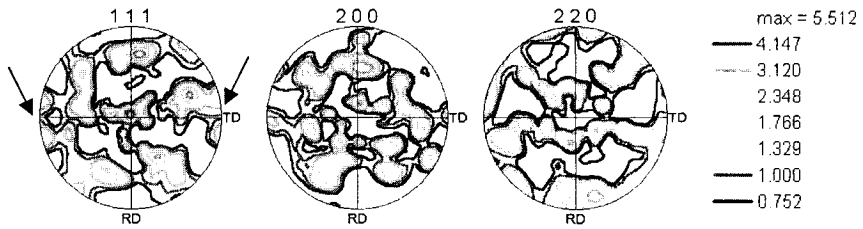
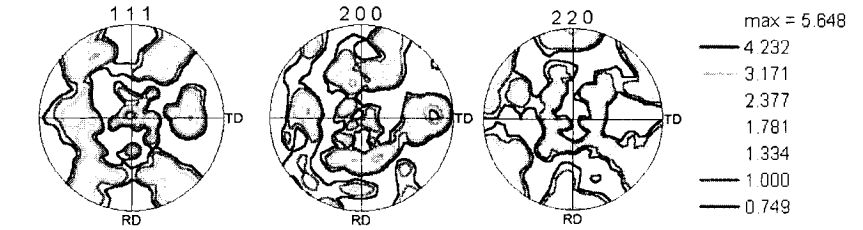
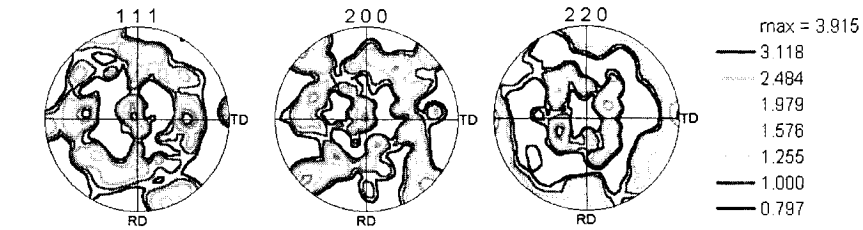
(a)



(b)

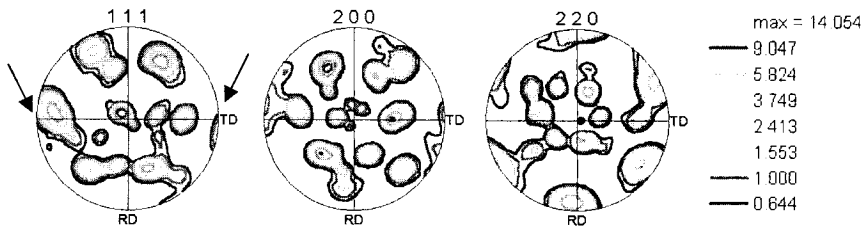
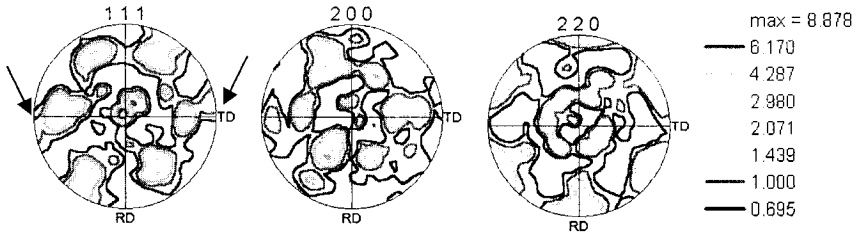
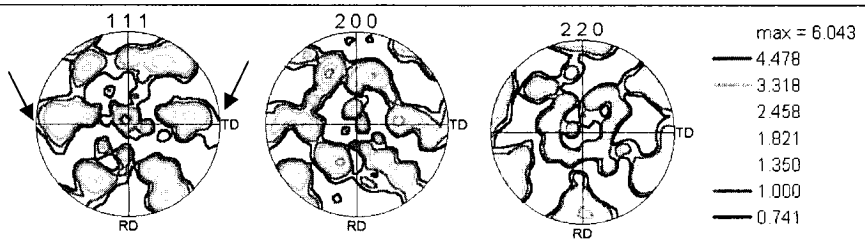
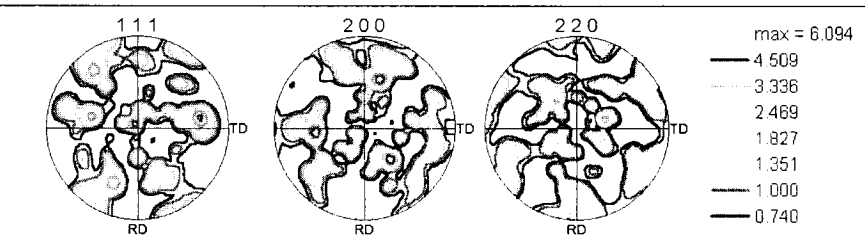
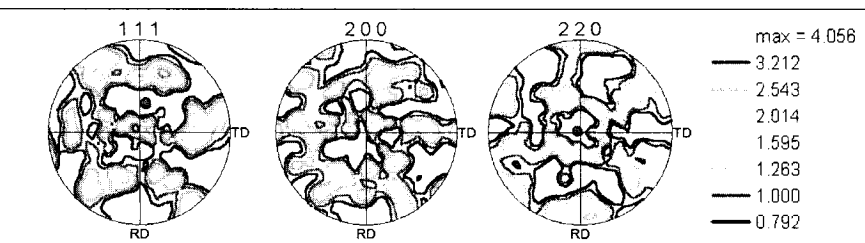
Figure 6.3. SEM photos: (a) cross-sectional profile of Cu interconnects after electroplating, (b) top view after a 120 second electropolishing to remove overburden of Cu.

To obtain quantitative information about texture, three pole figures were measured from the top surface of the Cu interconnects using the EBSD technique. The results presented in Figure 6.4, indicate that {111}<110> textures exist in all samples, however it becomes fiber-like as the line width increases. Compared to the "as-deposited" sample, the texture of the "annealed" sample becomes stronger. As shown in Figure 6.5, the maximum intensity is the strongest in the narrowest line and it decreases as the line width increases. The difference in intensity between the "as-deposited" and "annealed" sample is highest for the narrow lines and decreases as the line width increases; there is almost no difference in texture intensity at the 2 μm line width. In addition, a weak {111} sidewall component in the narrow lines, such as 0.14, 0.24 and 0.5 μm line width, was found as indicated by the arrows in Figure 6.4. To make it clear, the intensity of the sidewall {111} component was plotted, as shown in Figure 6.6. This figure shows that the strength of the sidewall {111} component changes as the line width increases. In this figure, the strongest intensity was found at the narrowest lines, and it decreases when the line width increases up to 1 μm and then increases to 2 μm line width in both specimens. The intensities of the "as-deposited" sample are always higher than the "annealed" sample. It seems that the annealing process minimizes the sidewall contribution to overall texture in the Cu interconnects. To explain these textural evolutions as the line width decreases after annealing, a new texture development model will be suggested in the discussion.

Line Width	As-deposited
0.14 μm	
0.24 μm	
0.5 μm	
1 μm	
2 μm	

(a)

Figure 6.4. (111), (200) and (220) pole figures of copper damascene interconnects having a different line width: (a) as-deposited.

Line Width	Annealed
0.14 μm	
0.24 μm	
0.5 μm	
1 μm	
2 μm	

(b)

Figure 6.4. (111), (200) and (220) pole figures of copper damascene interconnects having a different line width: (b) after 200°C annealing.

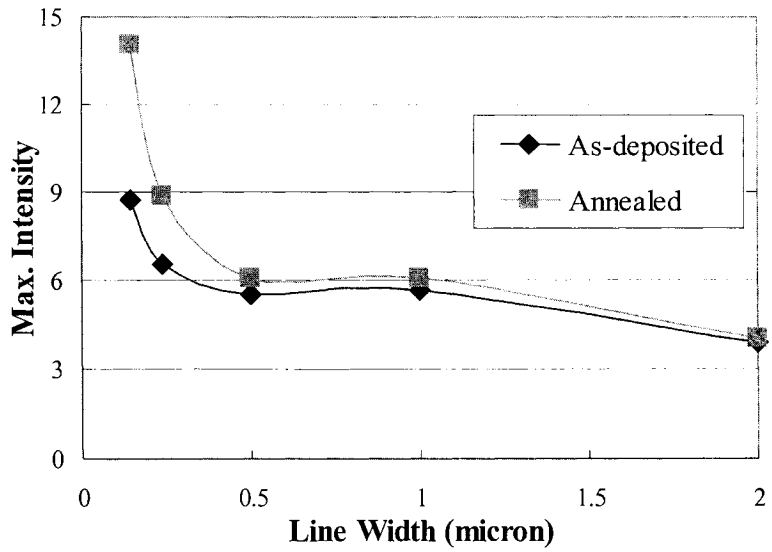


Figure 6.5. The changes of maximum intensity in as-deposited and annealed sample as a function of line width.

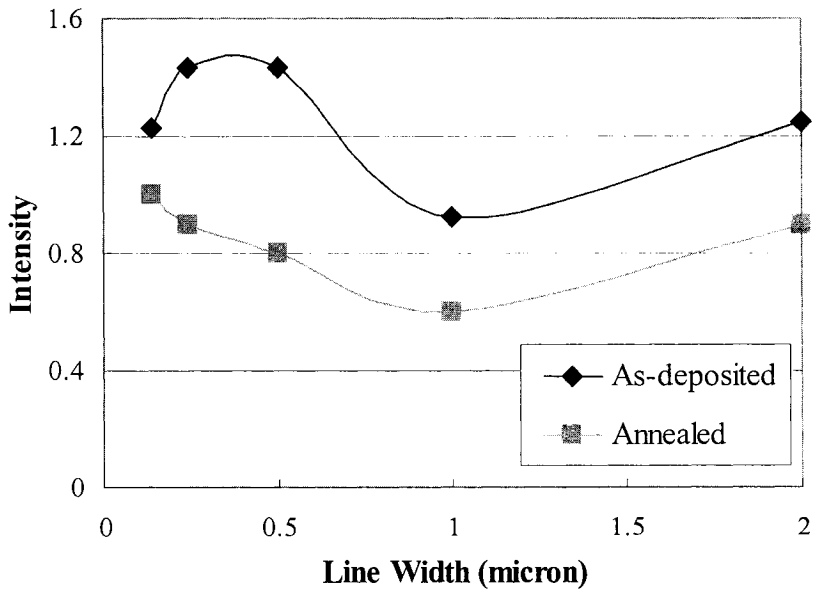


Figure 6.6. The intensity of the sidewall {111} texture component from the transverse direction inverse pole figures in the as-deposited and annealed sample as a function of line width.

6.3.2. Microstructure and GBCD

To analyze the microstructural evolution after annealing, the orientation of grains and types of grain boundaries on the top area of the Cu interconnect, EBSD technique were used. The results are shown in Figure 6.7. These inverse pole figure maps demonstrate that the so-called bamboo structure is found in the 0.14 μm line and that a semi-bamboo structure is observed in 0.24 and 0.5 μm line width samples. However, 1 and 2 μm lines show a polycrystalline microstructure with a mixture of large and small grains. Regardless of the difference in line width, every Cu interconnect shows a high number of twin boundaries. After annealing, it seems that the microstructure of Cu interconnects contain less twin boundaries and grains are larger. The frequency of CSL boundaries as measured by the EBSD technique is shown in Figure 6.8. The results obtained demonstrate that the fraction of Σ3 boundaries increase as the line width increases. Also, a higher fraction of twin boundaries is observed in 2 μm lines. However, it decreases after annealing, especially in the 0.14 μm line width interconnects sample (Figure 6.8a). On the contrary, Figure 6.8b shows that the fraction of the low angle grain boundaries (LAGB) increases after annealing, especially in the 0.14 μm line. From these results, it can be concluded that the annealing process enhanced the grain growth of Cu interconnects consuming the twin boundaries and producing low angle boundaries. Through this finding, the directional development of the {115} texture which is produced by twining [87-91] can be explained like this: the {115} texture and twin boundaries were generated by twinning at the beginning of annealing process, and then this {115} textured grains which have certain directions underwent grain growth consuming twin boundaries.

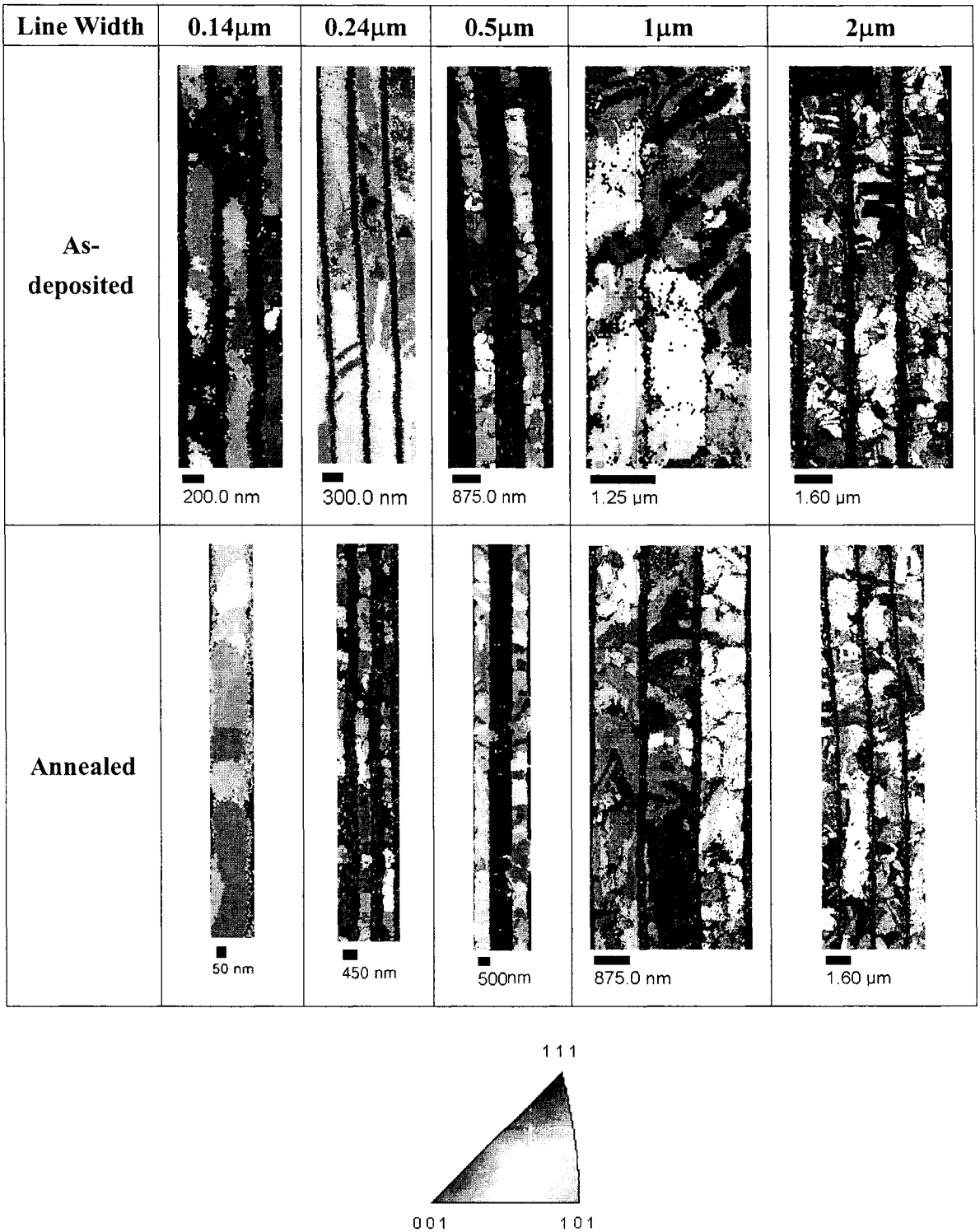
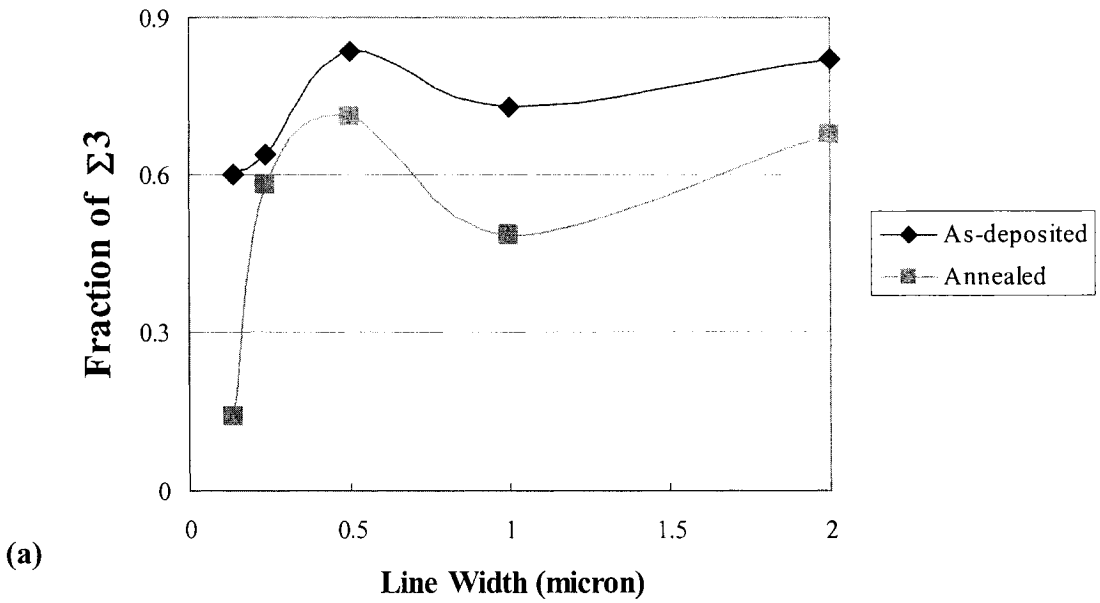
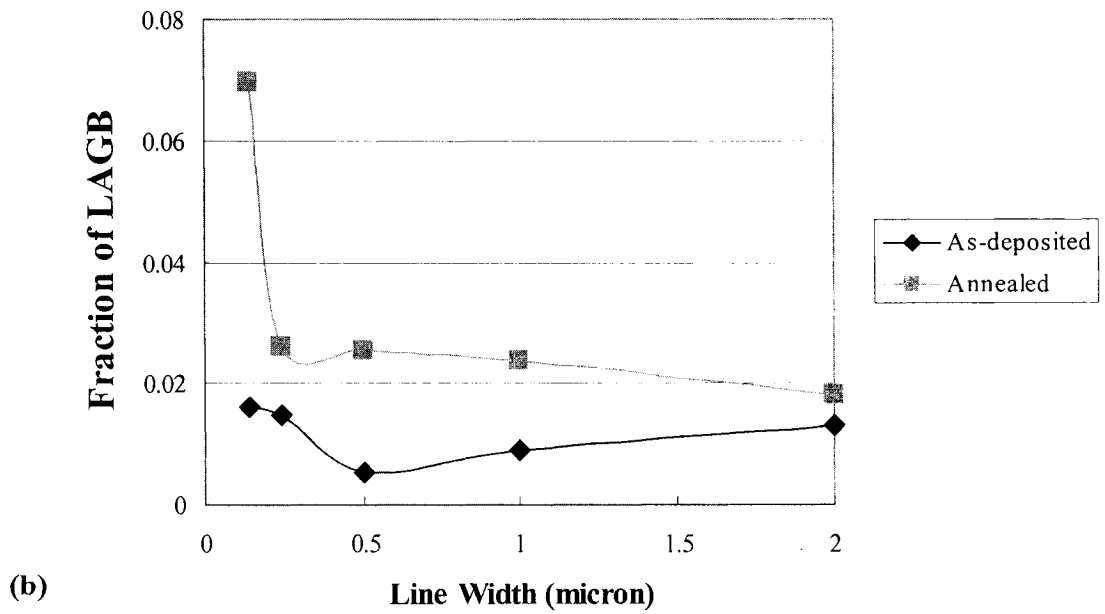


Figure 6.7. Inverse pole colored map representing orientation of planes parallel to the surface of the interconnect lines after electropolishing.



(a)

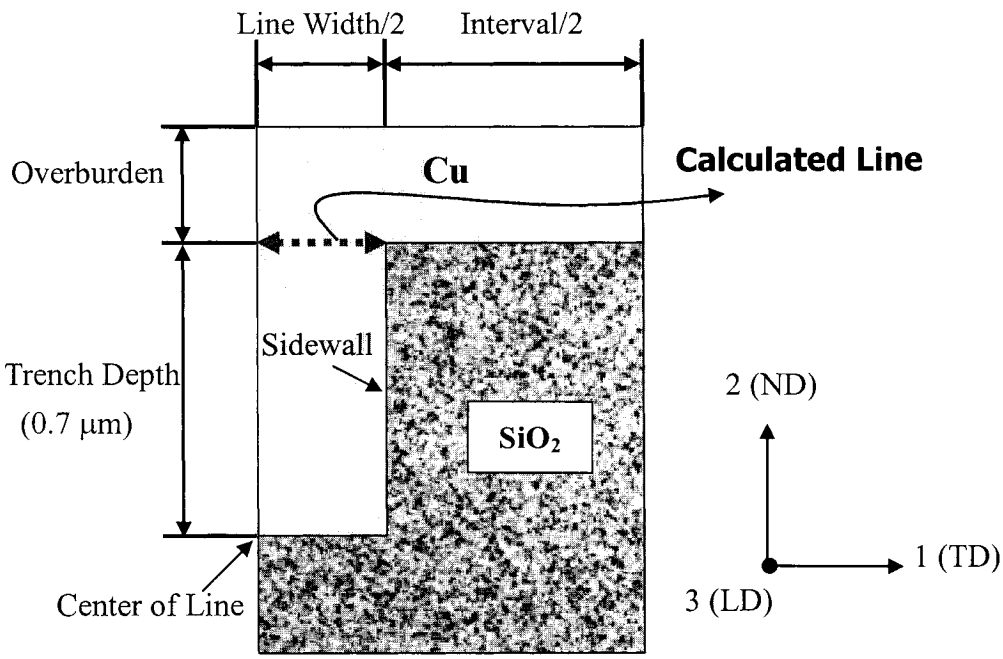


(b)

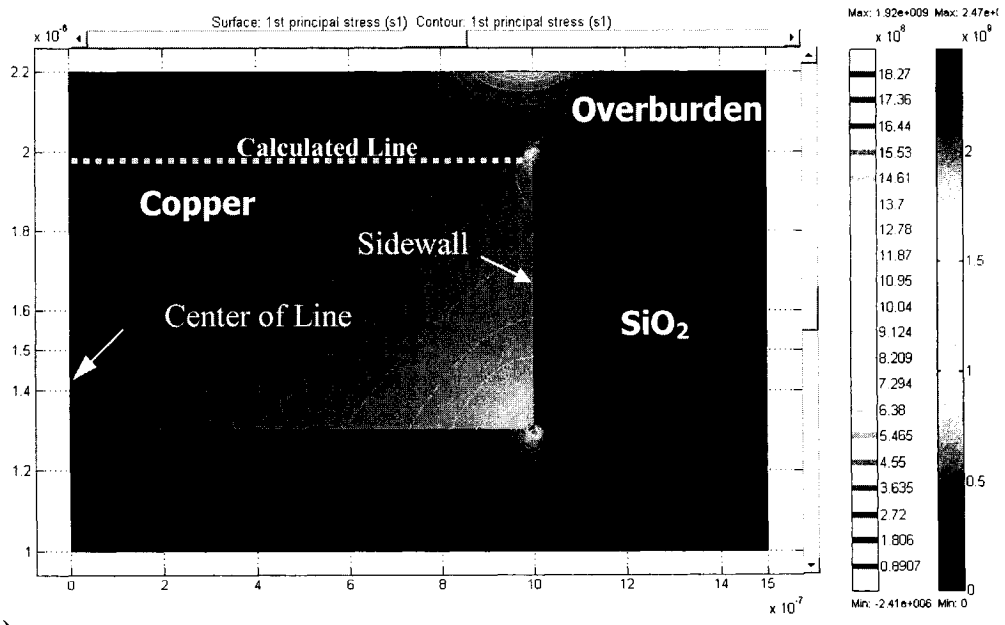
Figure 6.8. GBCD in Cu interconnects lines having a different line width after annealing: (a) Σ3 CSL boundaries, (b) low angle grain boundaries (<15°).

6.4. Stress on the Top Surface Area of Copper Damascene Interconnects

There might be several reasons for textural evolution of Cu interconnects after annealing, such as the stress or/and strain energy, surface/interface energy and grain boundary energy. Since it should be undergone annealing process at high temperature during fabrication, it is possible that the thermal stress or/and strain energy during annealing might be the most important factor for the textural and microstructural evolution during annealing. The role of stress distribution in the trench and overburden area was simulated using FEM and the geometry and coordinate system for simulation are illustrated in Figure 6.9. In this calculation, it is assumed that the finite element mesh can expand freely along the ND (normal direction) when Cu interconnect with overburden is annealed at 200°C. Since the mirror symmetry is applied along the ND and the LD (line direction), only the half of Cu interconnect line was modeled in this investigation (Figure 6.9a). To calculate the thermal stress (S_{11}) distribution in Cu damascene interconnects having different line width at 200°C, it is also assumed that the copper interconnect has isotropic mechanical properties and that the expansion coefficients of surrounding silicon oxide is compared to that of copper. Therefore, the data obtained from this modeling should only be considered as a qualitative representation of the stress changes at high temperature. As shown in Figure 6.9b, S_{11} stress is inhomogeneously distributed inside the trench. Since texture, microstructure and GBCD were analyzed on the top surface area of Cu interconnect by EBSD technique, the stress is calculated on this area to understand the relationship between texture and stress distribution.



(a)



(b)

Figure 6.9. Stress distribution calculated by FEM: (a) cross-sectional schematic diagram of Cu interconnects, (b) captured image of S_{11} stress distribution at the 2μm line width from FEMLAB.

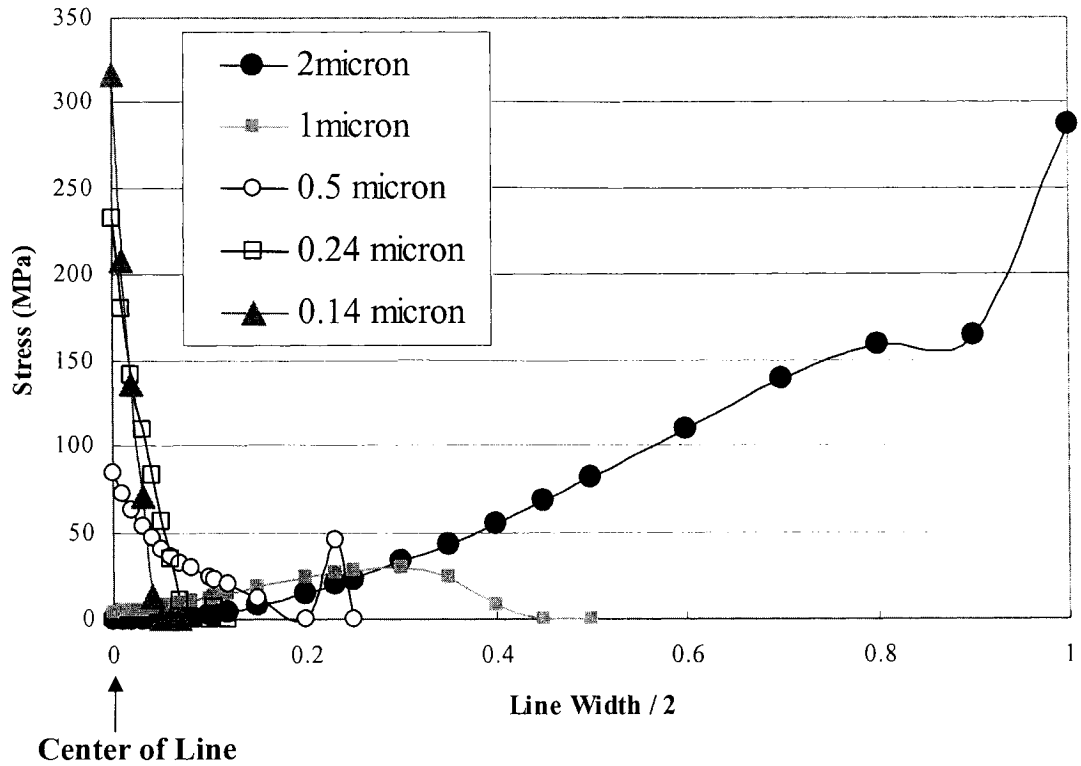


Figure 6.10. S_{11} stress distribution from the center of the Cu line to the sidewall on the top surface area at 200°C.

Figure 6.10 shows the S_{11} stress distribution along the width from the center of the Cu line to the sidewall, on the top surface area (Figure 6.9) at 200°C. From the data in Figure 6.10, one can see that the thermal stresses are very strong near the sidewall and are weak at the middle of the line in the 2 μm line width interconnect, however the location of the maximum value of S_{11} moves from the corner (sidewall) of the trench to the middle as the line width decreases. To characterize these stress distributions, the average stress is

calculated and plotted in Figure 6.11. This figure shows that the absolute magnitudes of the stresses along the trench width are the largest in the 0.14 and 2 μm line width and the smallest in 1 μm line width. Comparing to Figure 6.5, these results show that stress helps the development of texture in the narrow line during annealing, however, the effect of stress on the texture development seems negligible in the wider line even though it has the strongest stress. Further explanation about this relationship will be presented in the discussion. From these results, it was found that the distributions of S_{11} stress and the average S_{11} stress are inhomogeneous on the top surface area of Cu damascene interconnect during annealing, and it can be a factor for the textural and microstructural evolution in each Cu interconnects line.

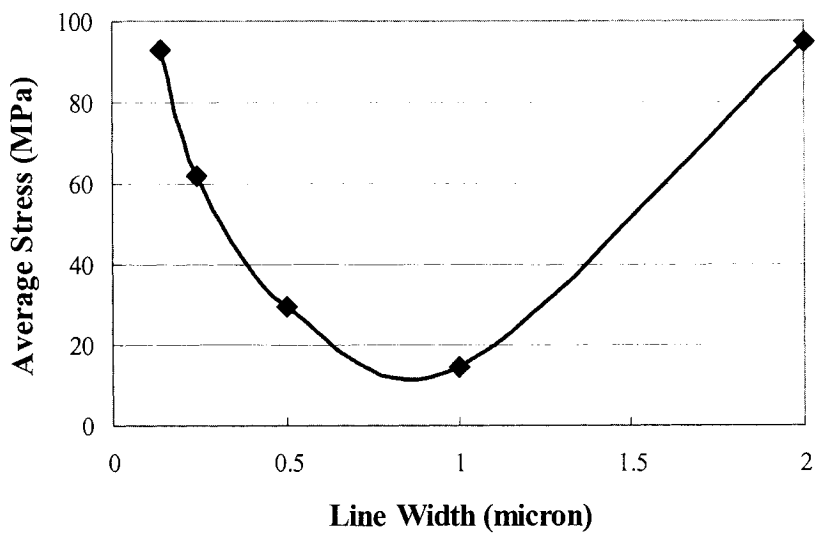


Figure 6.11. Average S_{11} as a function of line width at 200°C.

6.5. Discussion and Summary

In the investigation described in this chapter, two different kinds of samples were used: as-deposited and annealed at 200°C. Both samples were kept at room temperature for over 6 months, which provides adequate time for room-temperature recrystallization which is a known phenomena in Cu electrodeposits to occur. Therefore, comparing both samples will only allow the investigation of grain growth mechanisms which take place during the annealing process. To investigate the textural changes after annealing, two different methods were used: XRD and EBSD techniques. Using XRD, three different cross-sectional profiles of Cu interconnects were investigated. The advantages of the XRD method are that it collects information from the whole volume (from bottom to surface) of the trench and is statistically more reliable than EBSD methods. The obtained XRD results demonstrate strong differences between the texture of the overburden area and inside the trench after electroplating and annealing (Figure 6.2). Especially, the difference in texture of 120 and 130 seconds electropolished samples indicates that the constraint by the sidewalls generates different stress during annealing and can be responsible for differences in texture evolution. Obviously the constraints at a higher depth are larger than in the upper (surface) region since Cu layers close to the surface can expand more freely. It seems that the stress distribution along the trench depth is as important in the textural and microstructural evolution as the average stress.

The importance of stress on the texture evolution in Cu damascene interconnects has been emphasized by several researchers because differences in the thermal expansion

coefficients of copper and dielectric (silicon dioxide) generate stress in the interface area between different layers [105-113]. However, the mechanism of textural transformation imposed by the stress in the damascene copper interconnects remains unclear. Lee et al. [78-81] suggested that the strain energy can be minimized when the absolute maximum principal stress direction is parallel to the minimum Young's modulus direction. It is known that the copper electrodeposits just after plating consist of grains of several nanometers in size and have the texture of {111} // growth direction, because the sputtered copper substrate has the {111} texture. The nanocrystalline copper electrodeposits must have some fiber textures component as well, that is, grains have the {111} orientations parallel to the trench depth direction while the orientation normal to the depth direction is random. When annealed, the copper electrodeposits grow under compression stresses. During grain growth, the texture of electrodeposits develops along the direction in which the strain energy of the grains is minimized when the absolute maximum principal stress direction is parallel to the minimum Young's modulus direction. The minimum Young's modulus direction of copper is the <100> direction, as shown in Figure 6.12a [78-81]. Therefore, copper grains whose <100> is parallel to the absolute maximum stress direction will be in better position to grow than others. However, the <100> orientations are not on the {111} plane. Therefore, it is most probable that grains having <112> direction, which is on the {111} plane, and is at the smallest angle with the <100> direction, will grow favorably [81], as shown in Figure 6.12b. Therefore, texture is likely to approach {111}<112>// trench width direction which is {111}<110>// trench length direction (Figure 6.12c). This prediction is consistent with the experimental results, as shown in Figure 6.4.

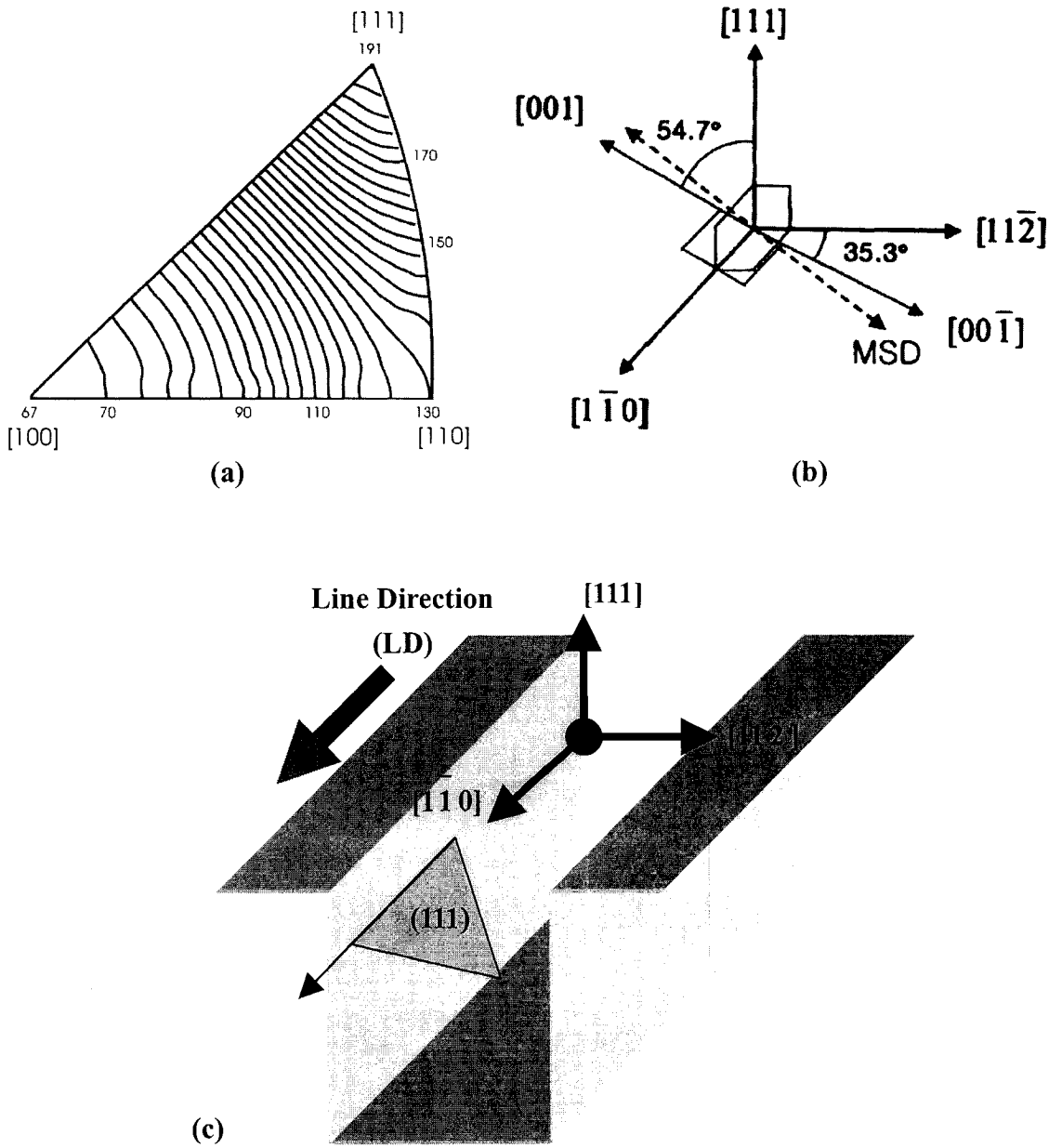


Figure 6.12. Relationship among orientations in the trench: (a) Young's moduli along various directions of copper at 298 K [78-80], (b) [111], [1$\bar{1}$0], [11$\bar{2}$], and [001] directions - maximum stress direction (MSD) and [111], [001], and [11$\bar{2}$] directions are on the same plane [81], (c) schematic illustration.

It was also found that the maximum value of S_{11} moves from the corner (sidewall) of the trench to the middle as the line width decreases during annealing and the average stress value at 200°C on the top surface of the trench shows the higher value at 0.14 and 2 μm line widths. Comparing Figure 6.5 and 6.6 with Figure 6.10 and 6.11, these results show that stress helps the development of texture in the narrow line during annealing, however, the effect of stress on the texture development seems negligible in the wider line even though it has the strongest stress. In the narrow lines, the stresses generated from the constraint of sidewalls and the difference in thermal expansion coefficients between layers help grains to align and grow to the {111}<110> orientation and decrease the sidewall {111} component. However, in spite of the high value of stress in the 2 μm line width, the intensity of {111} texture decreases since it has less of a constraint and generates a high number of twin type boundaries, and a fiber-like texture component. In this investigation, it is important that the stress distribution along the trench width influences textural and microstructural evolution of Cu interconnects. Figure 6.10 indicates that the highest value of stress was found near the sidewall in the 2 μm line width, however, in the 0.14 μm line width, the highest value was found in the middle of the trench width. Therefore, including Figure 5.10 in the Chapter 5, it can be concluded that both stress distributions along the trench depth and width are important in the textural and microstructural evolution of Cu damascene interconnects during annealing. The disagreement between x-ray and EBSD results supports this explanation.

Besides stress, another important factor affecting the textural and microstructural evolution in the damascene Cu interconnects after annealing could be the growth mechanism of the copper electrodeposits in the trenches during electroplating. It has been reported in the literature that narrow Cu trenches can be completely filled during

electroplating using super-conformal filling [16-21]. To eliminate possibilities of void formation in the trench, this super-conformal filling assures that the growth from the bottom of the trench is dominant over the growth from the sidewall [10] (Figure 6.13).

Several bodies of research [56, 90, 114-116] have reported that the importance of the sidewall {111} component is increased in the narrow lines and the intensity of the overall texture can be minimized by this. However, considering super-conformal filling conditions where the bottom growth is much more dominant than the sidewall growth, such an observation is questionable. Proposed explanation is illustrated in Figure 6.14 where the growth mechanisms in the trench can be classified as "bottom growth components" and "sidewall growth components". In the wide line, one can easily see that the bottom growth component is dominant over the sidewall. According to this, it can be misunderstood that the sidewall growth component may greater than the bottom as the line width decreases since the area fraction of sidewall is higher than the bottom at the narrow line. However, considering the super conformal filling conditions, the bottom growth components should always be higher than the sidewall, even though interconnects have a narrow line width. In our investigation, weak sidewall components were found on the top surface area of the "as-deposit" sample in the narrow line because the relative volume fraction of the sidewall versus the bottom increases as the line width decreases. However, even such a weak sidewall component is minimized after the annealing process. Therefore, it can be concluded that the contribution by the sidewall component on the overall texture of Cu damascene interconnects after annealing is negligible and stress influences textural evolution during annealing.

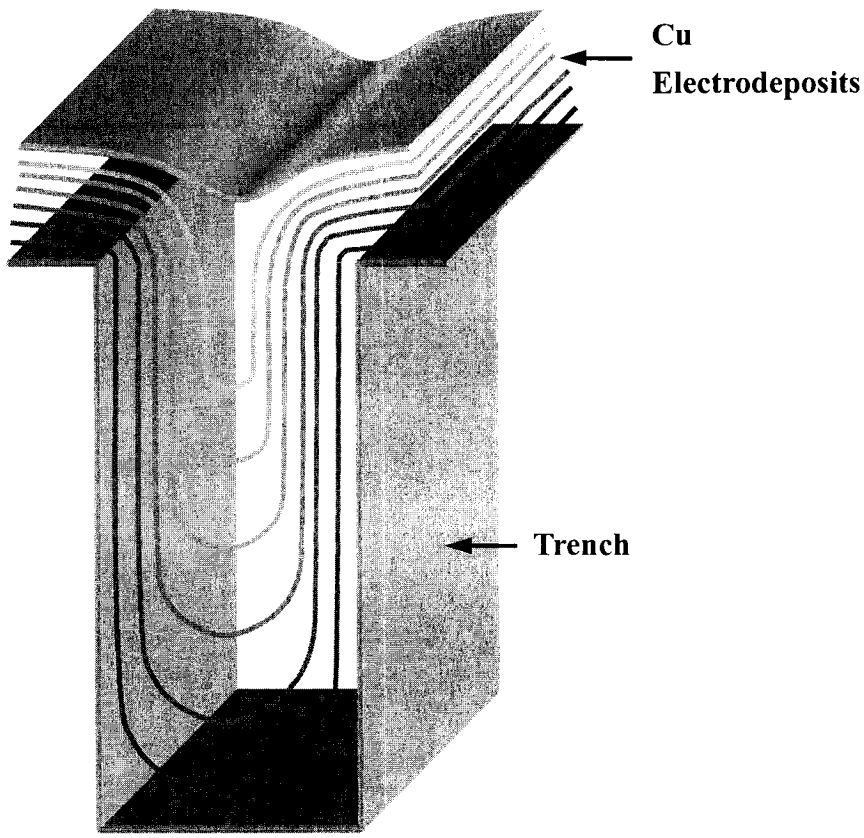


Figure 6.13. Cross-sectional schematic illustration of super-conformal filling in the trench after Cu electroplating without void formation.

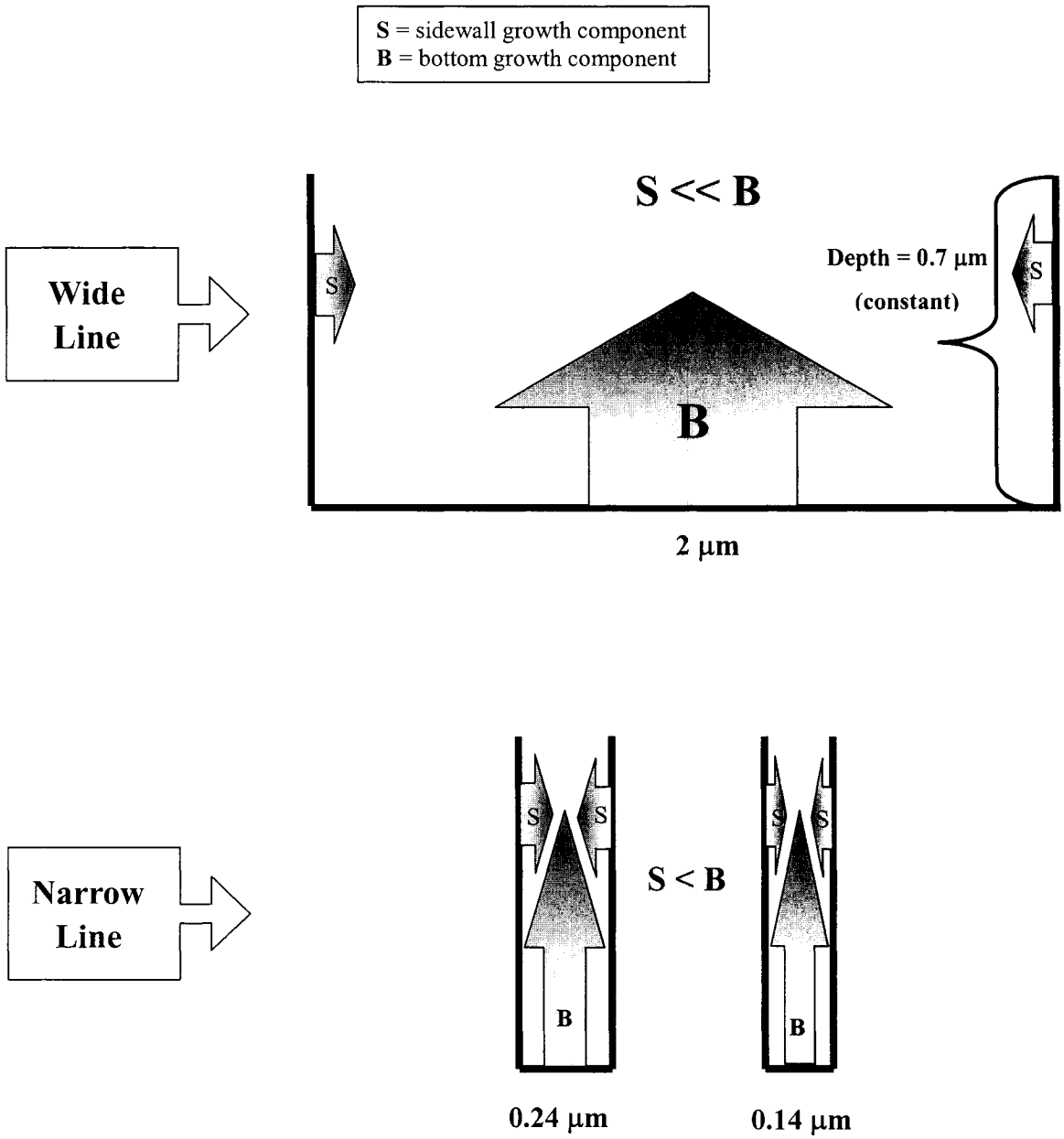


Figure 6.14. Schematic illustration of texture evolution with the different line width in the copper trench according to the condition of the super-conformal filling.

Chapter 7

Stress Contribution to Textural and Microstructural Evolution of Copper during Annealing

As mentioned in Chapter 6, stress is an important factor in the textural and microstructural evolution of Cu damascene interconnects during annealing. However, this conclusion was only supported qualitatively by FEM. In order to understand the effect of the stress on textural and microstructural evolution of Cu interconnect during annealing, a physical simulation was performed using two different samples of copper after different annealing schedules (200°C and 400°C), and applying static compression stress to each sample. Textural and microstructural evolution was investigated using ODF obtained from x-ray diffraction and grain boundary character distribution using orientation imaging microscopy. The mechanism of textural and microstructural evolution of copper after annealing with stress and without stress is discussed.

7.1. Experimental Procedure

7.1.1. Sample Preparation

In order to understand the stress contributions to textural and microstructural evolution of copper during annealing, two different kinds of Cu sample were prepared and annealed with and without stress as shown in Figure 7.1. Sample A has {110} fiber texture and sample B has {111} and {100} textures (Table 7.1). Five identical specimens for each Cu sample are prepared and polished to remove the notches from the sample surface before annealing.

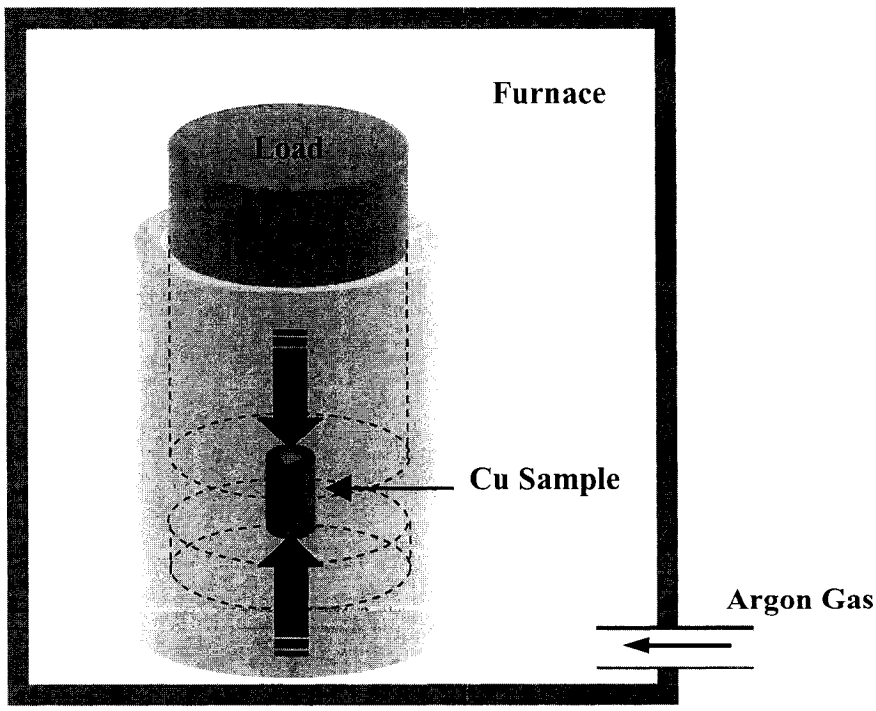
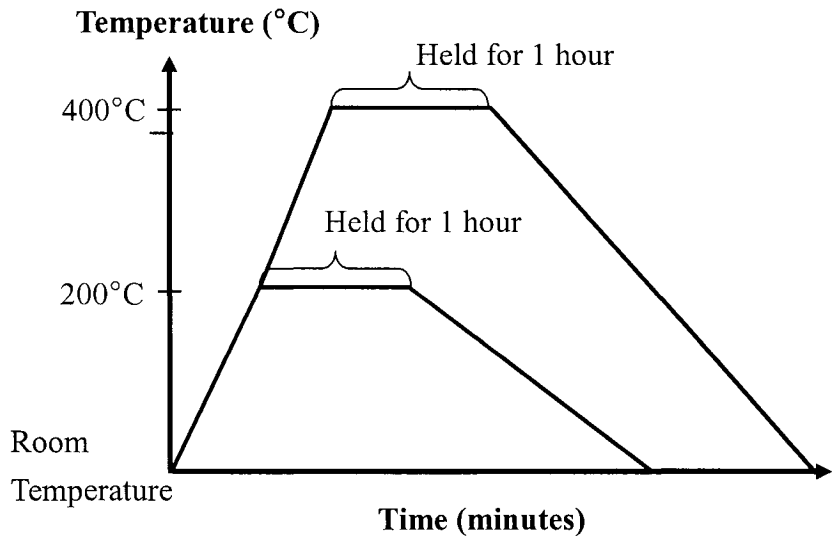


Figure 7.1. Schematic diagram of experimental setup for the compressive stressed Cu samples during annealing.

Table 7.1. Sample conditions depending on crystallographic texture, annealing temperature and stress.

Sample Name	**Sample A** {110} Fiber Texture	**Sample B** {111}+{100} Texture
1. Before Annealing	Before Annealing	Before Annealing
2. Stress 200	200°C Annealing with Stress	200°C Annealing with Stress
4. No Stress 200	200°C Annealing without Stress	200°C Annealing without Stress
3. Stress 400	400°C Annealing with Stress	400°C Annealing with Stress
5. No Stress 400	400°C Annealing without Stress	400°C Annealing without Stress

Two different kinds of annealing schedules were used: in one, the specimen is heated from room temperature to 200°C where it is held for one hour and then cooled, in the another schedule, the specimen is heated up to 400°C where it is held for an hour and then cooled to room temperature, as shown in Figure 7.2. During both annealing schedules argon gas is blown through the furnace to minimize oxidation on the surface of the Cu samples. For each schedule, the Cu sample was annealed under compressive stress, or without stress (4 samples per schedule).



Figures 7.2. Two different annealing schedules (200°C and 400°C).

7.1.2. Texture and Microstructure Measurement

The crystallographic texture of Cu was measured using both a Siemens D500 X-ray goniometer and the orientation imaging microscopy. Three (111), (200) and (220) pole figures were obtained using the reflection technique, up to maximum tilt of the specimen of 80 deg in 5 deg intervals. The details of microstructure and grain boundary character distribution are observed using OIM which is mounted on a Philips XL30 FEG-SEM.

7.2. Textural and Microstructural Evolution of Copper after Annealing with Static Compressive Stress

In order to understand the stress contribution to textural and microstructural evolution of copper during annealing, the details of texture and microstructure changes after annealing under static compressive stress were analyzed by XRD and EBSD techniques. Two different crystallographic texture samples, sample A and B which have {110} fiber texture and {111} and {100} texture respectively were investigated in this study since the influence of stress on texture and microstructure of copper during annealing can be different depending on texture of copper.

7.2.1. Sample A – {110} Fiber Texture Copper

In this investigation, sample A which has a strong $(011)[1\bar{1}1]$ with weak fiber component, as shown in Figure 7.3. This figure shows ODF at $\varphi_2 = 0°$ and 45° sections and illustrates changes of intensity with or without stress at the different annealing temperature. It was found that $(011)[1\bar{1}1]$ component is stronger and the fiber components are lost, especially without the presence of compressive stresses after annealing at 200°C. High temperature (400°C) annealed specimens shows very weak $(011)[1\bar{1}1]$texture and the development of {110} and {100} fiber texture. Overall, stressed specimens show weaker texture than samples annealed without stress. The

development of other components, such as (011)[100] which is only shown at 400°C annealing is interesting. To see the details of textural changes of copper after annealing with and without compressive stress, the {110} fiber texture was plotted, as shown Figure 7.4. After annealing at 400°C without compressive stress, the intensity of $(011)[1\bar{1}1]$ decreases and $(011)[2\bar{1}1]$ develops

From the ODF results presented in Figure 7.3, it was noticed that static compressive stress suppresses the development of the $(011)[1\bar{1}1]$ texture component while the fiber components are lost during annealing at 200°C, and is also hindered the development of $(011)[2\bar{1}1]$ texture components with the development of fiber texture including the {100} fiber texture during annealing at 400°C. The detail explanation of this textural evolution of copper with and without static compressive stress after the different annealing schedules will be presented in the discussion of this chapter.

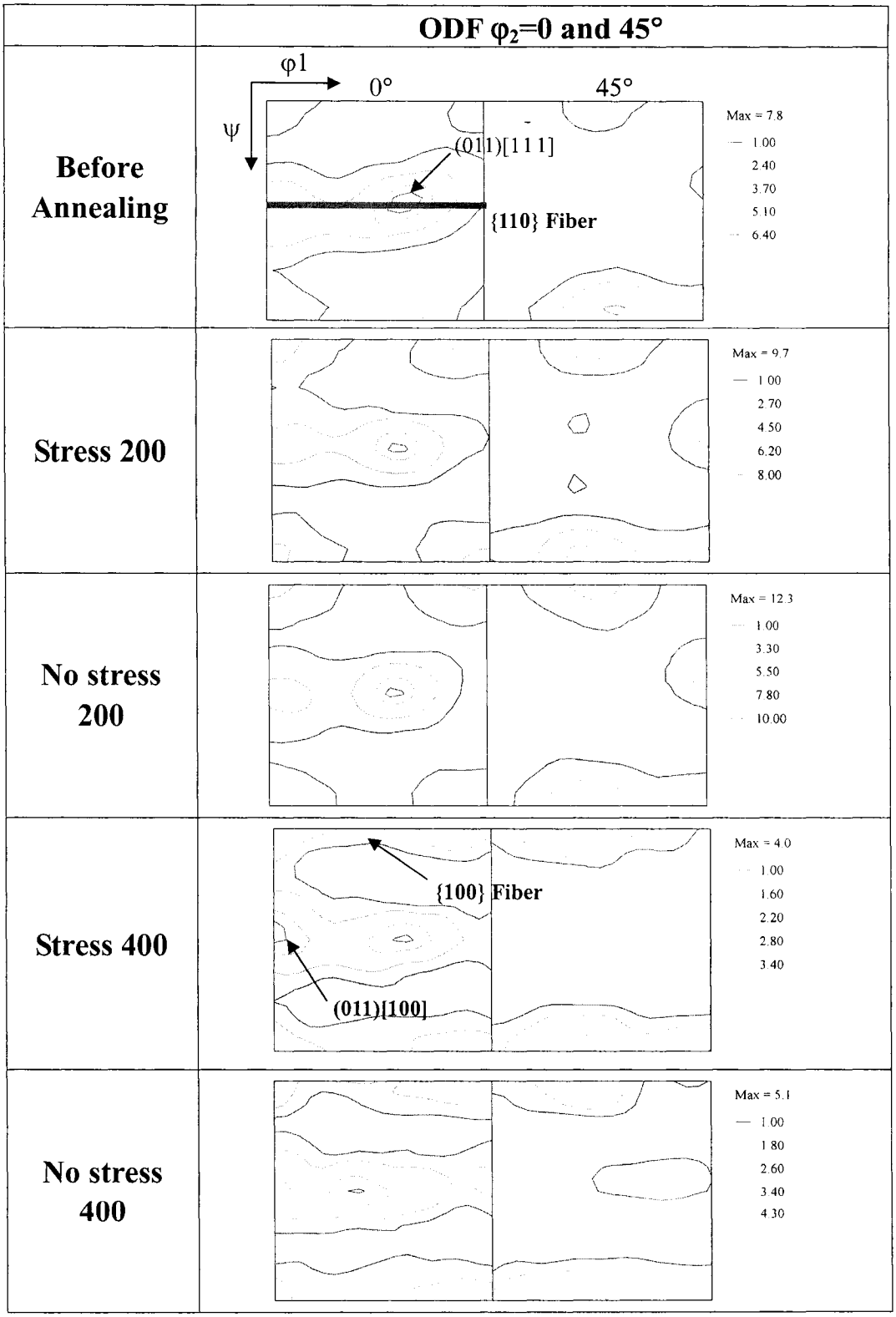


Figure 7.3. ODF φ_2=0 and 45° sections of sample A with and without static compressive stress after the different annealing schedules.

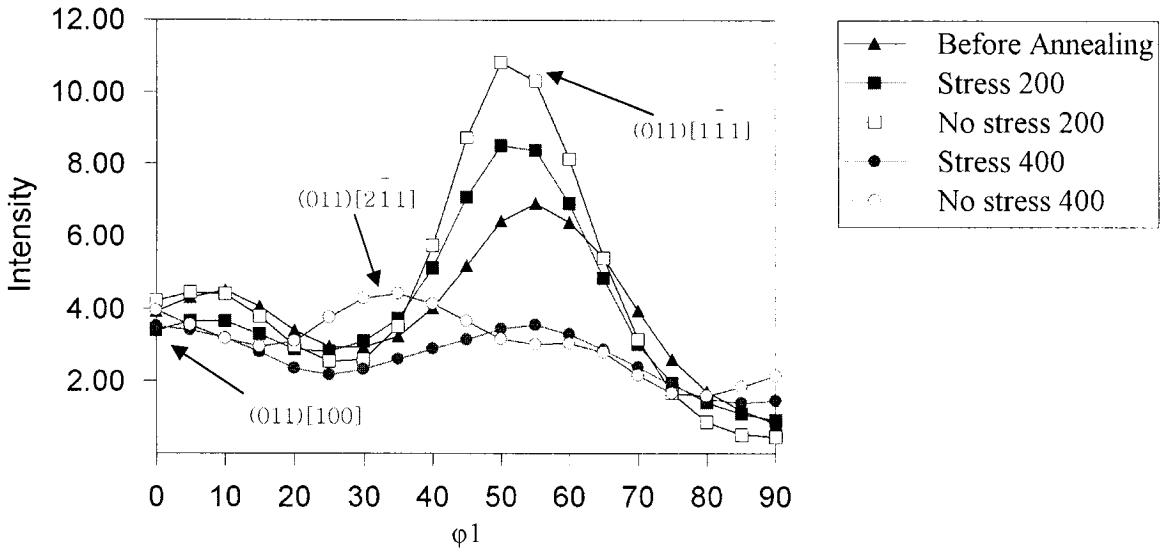


Figure 7.4. The plot of {110} fiber texture component of sample A with and without static compressive stress after the different annealing schedules.

To understand the effects of the stress on microstructure and grain boundary character distribution of Cu during annealing, the orientation of grains and types of grain boundaries of Cu were measured by EBSD technique. As shown in Figure 7.5, these inverse pole figure maps demonstrate that grains are elongated and heavily deformed before annealing. After annealing at 200°C, grain shape remains constant regardless of the presence of compressive stress. After annealing at 400°C, one can see that grain shape is more equiaxed with lots of twins since recrystallization and grain growth have taken place. To understand of the details of these changes, the grain size, frequency of CSL boundaries and misorientation angle distributions were measured using OIM, as shown in Figure 7.6 and 7.7. At first, Figure 7.6 shows that the annealing process enhance the recrystallization and grain growth of grains overall, especially at 400°C, however, stress

seems not affect these that much (Figure 7.6). Since Cu is a low stacking fault energy materials, it can easily generate twin boundaries in the microstructure during process [83-86]. Accordingly many Σ3 boundaries, known as twin boundaries, were observed using OIM. Figure 7.6b shows that the number fraction of Σ3 boundaries dramatically increased after 400°C annealing regardless of the presence of the compressive stress.

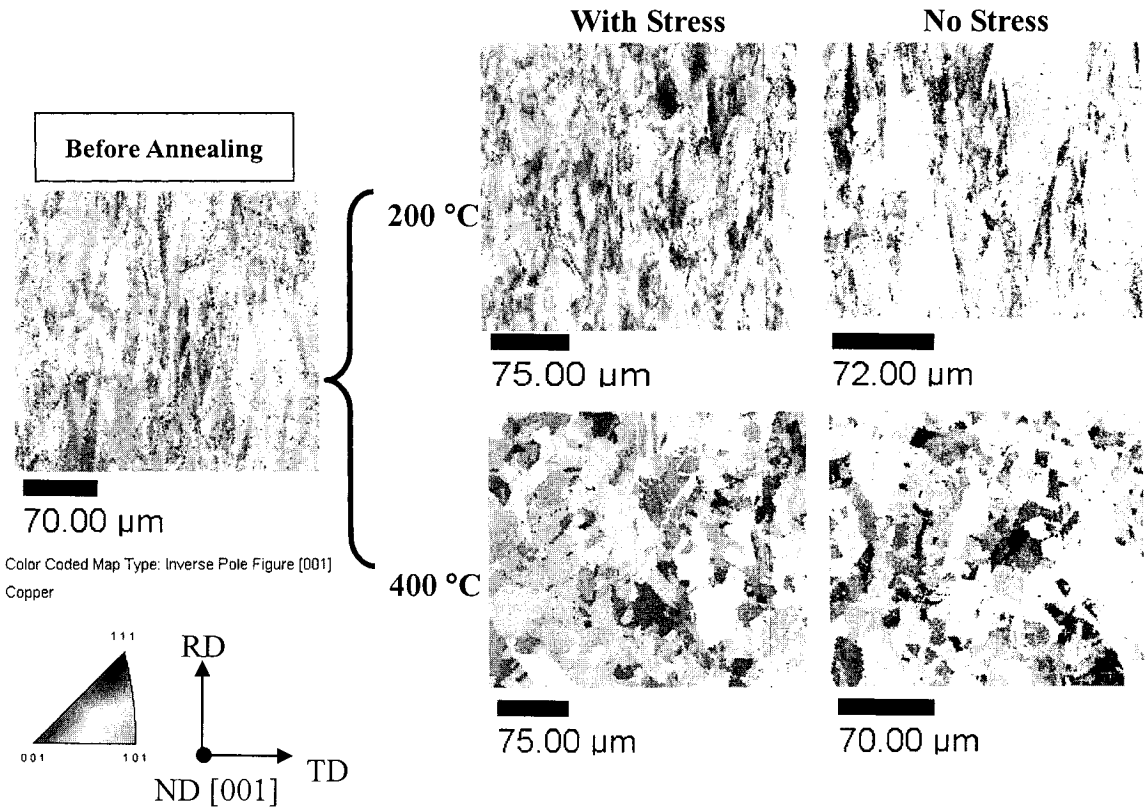
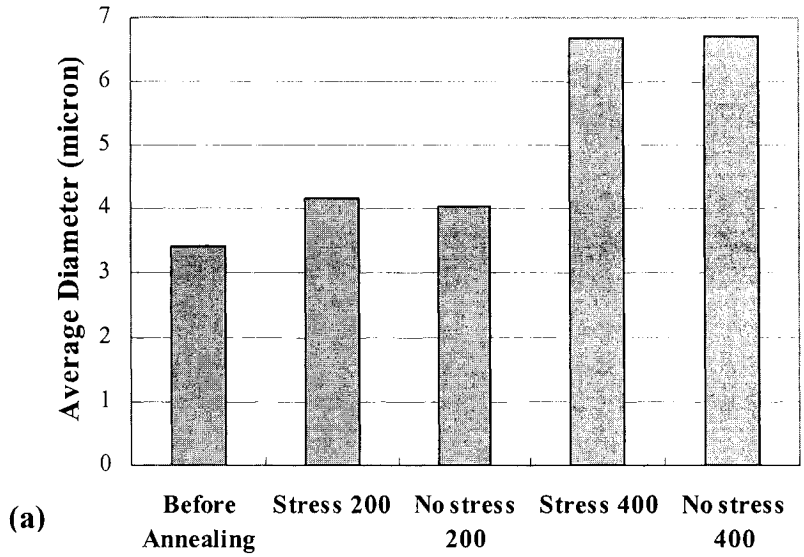


Figure 7.5. Microstructural evolution of sample A with and without compression stress after the different annealing schedules using inverse pole figure maps for the normal direction [001] obtained from OIM.



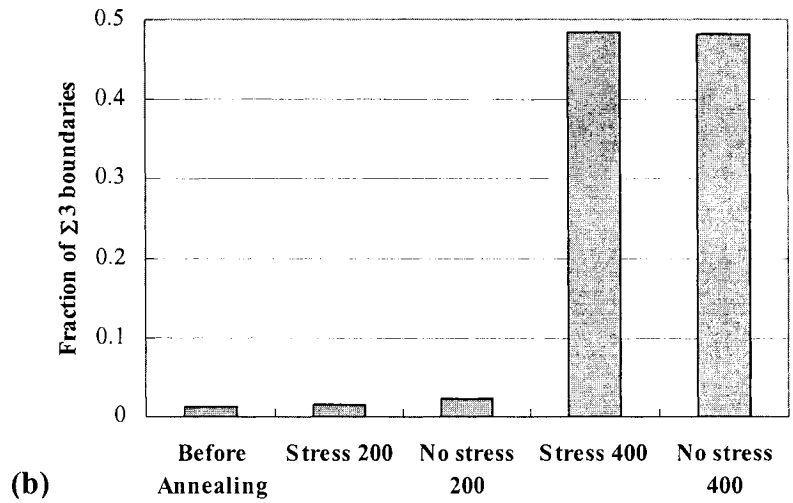
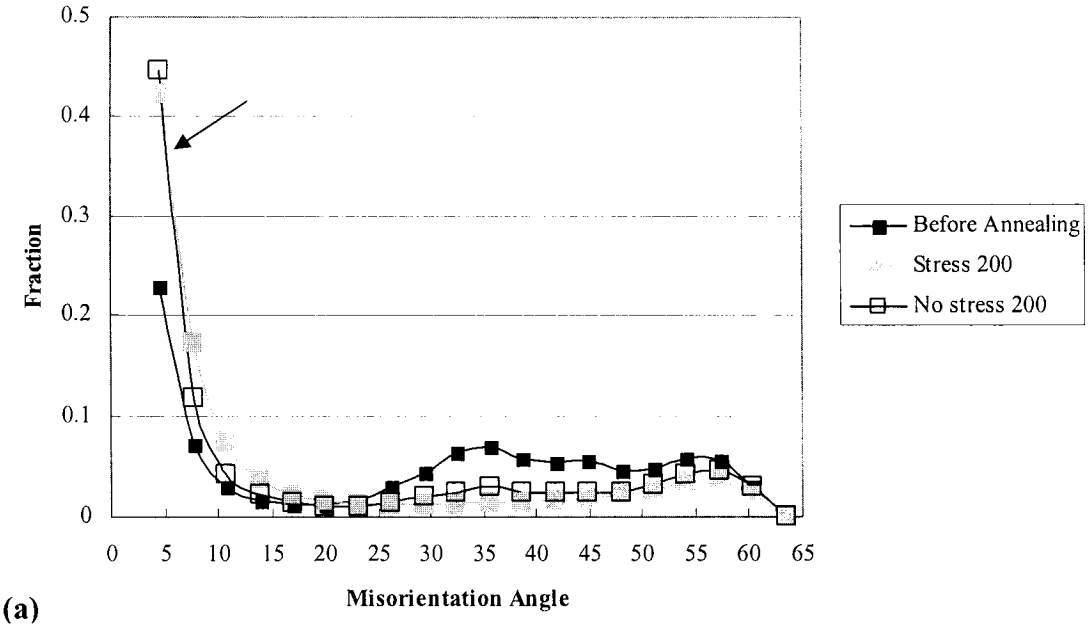
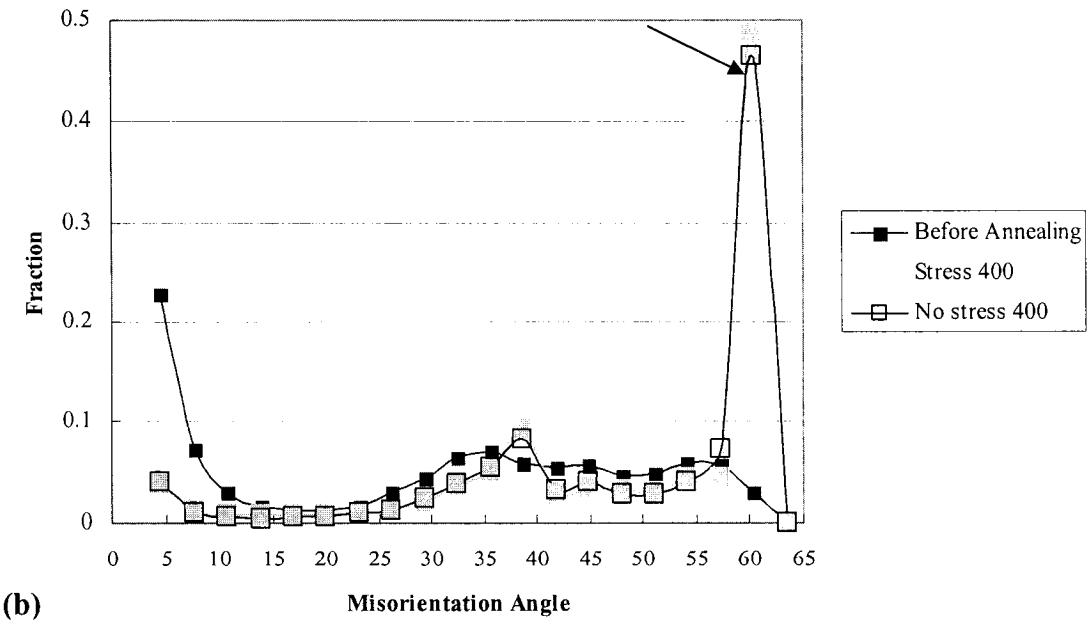


Figure 7.6. Microstructural evolution of sample A annealed with and without compressive stress during two different annealing schedules: (a) average grain size, (b) Σ3 boundary distribution.

In addition, misorientation distributions of Cu are measured and calculated by OIM analysis software, as shown in Figure 7.7. This figure illustrates that low angle grain boundaries are developed during annealing at 200°C regardless of the presence of compressive stress. After annealing at 400°C, the number of 60 degree rotation grain boundaries which are twin boundaries increases regardless of the presence of the compressive stress (Figure 7.7b). From these results (Figure 7.6 and 7.7), one can see that Cu undergoes recovery process during annealing at 200°C, however, recrystallization and grain growth process are dominant during annealing at 400°C. In addition, it seems that the annealing temperature is more important than static compressive stress in microstructural evolution of the sample A during annealing.



(a)



(b)

Figure 7.7. Misorientation distribution of sample A after annealing with and without compressive stress: (a) at 200°C, (b) at 400°C.

7.2.2. Sample B – {111} and {100} Texture Copper

In order to analyze the textural and microstructural evolution of {111} and {100} textured copper samples during annealing under compressive stress, the sample surfaces were carefully polished after annealing and analyzed using OIM. Figure 7.8 represents (111), (200) and (220) pole figures that are constructed from large area scans for better statistically reliable data. This figure shows that {111} and {100} textures are dominant, having weak fiber component in the sample B. After annealing at 200°C, its maximum intensity increases with keeping their fiber components, however, it is higher at the absence of stress (No stress sample). After annealing at 400°C with stress, it shows that its maximum intensity decreases with loosing their fiber components and the development of some minor components, however, its maximum intensity does not change after annealing at 400°C without stress.

From previous studies [53-57], it was known that texture is strongly related to electromigration failure: {111} texture shows stronger resistance against electromigration induced failure than {100}. Therefore, strong {111} texture will be favorable for the copper damascene interconnects. The ratio between {111} and {100} texture might be of interest in this investigation. As shown in Figure 7.9, this ratio changes after annealing with and without static stress. During annealing at 200°C, it seems that static compressive stress suppresses the development of {111} texture and enhances the development of {100}. However, during annealing at 400°C, stress enhances the development of the {111} component and weakens {100} texture.

According to these results, it can be concluded that the effect of static compressive stress on the textural evolution of copper during annealing strongly depends on the temperature of the annealing schedule: {100} texture is strengthened at low temperature annealing and the development of {111} texture is enhanced at high temperature annealing.

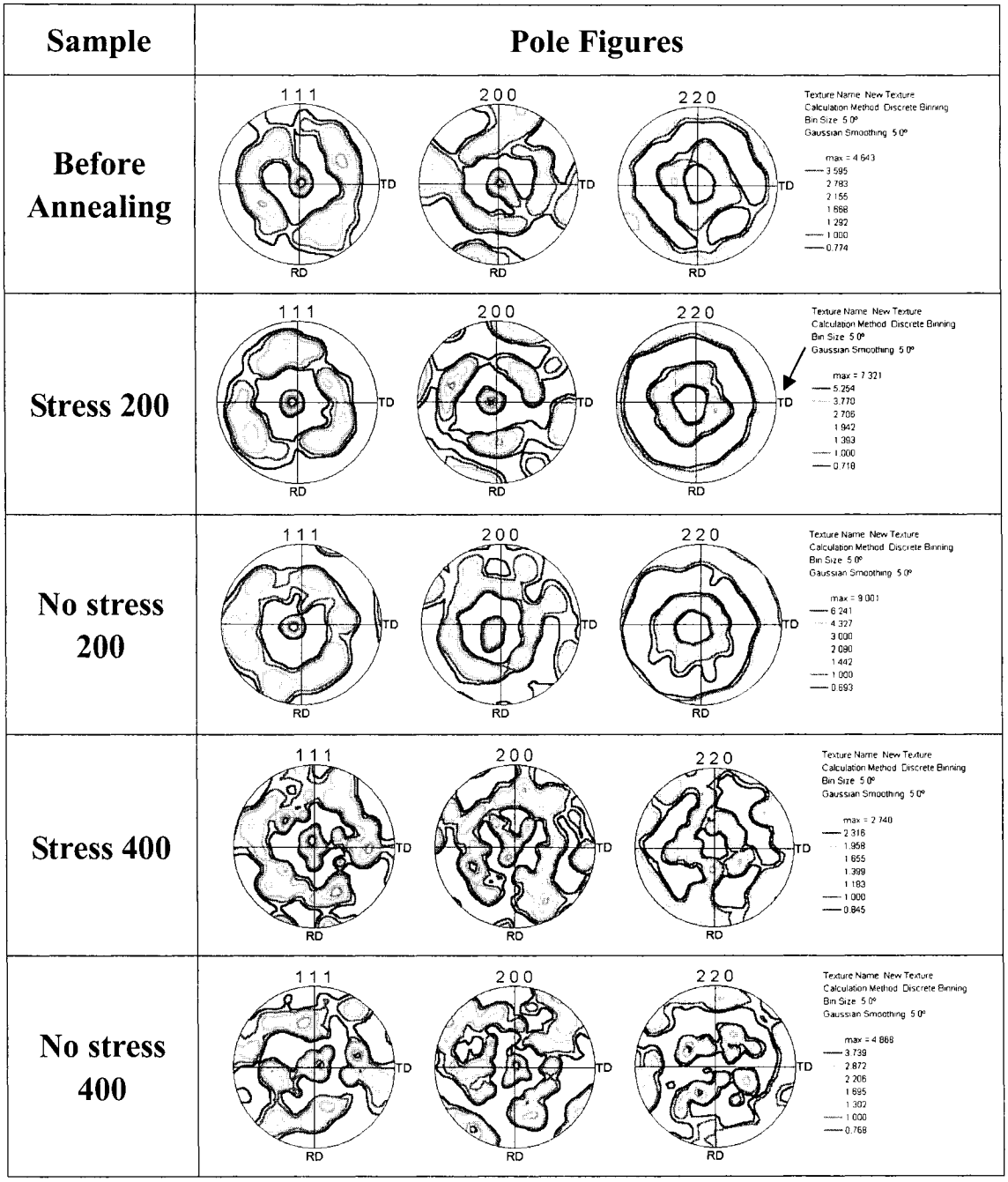


Figure 7.8. (111), (200) and (220) pole figures of sample B with and without static compressive stress after the different annealing schedules.

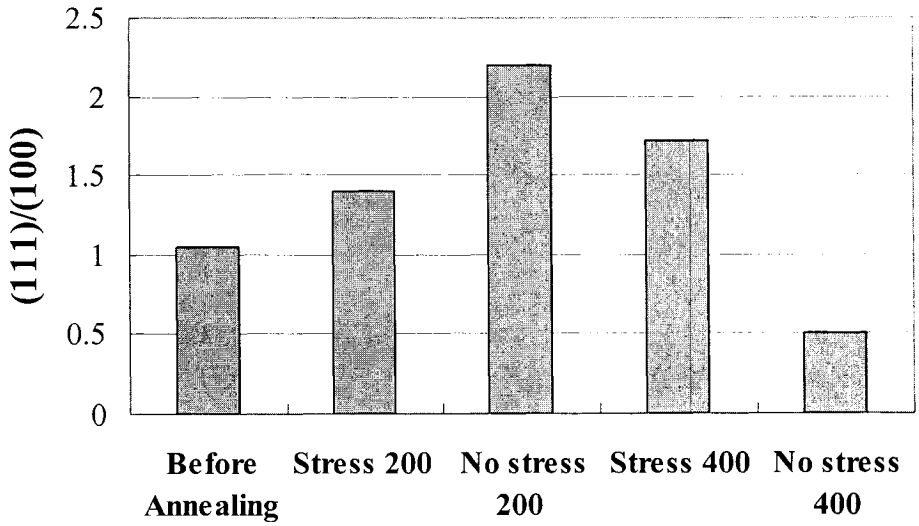


Figure 7.9. The intensity ratio between {111} and {100} texture of sample B with and without static compressive stress after the different annealing schedules.

In addition, the effects of the stress on microstructure and grain boundary character distribution of Cu during annealing in sample B were investigated using OIM, as shown in Figure 7.10. Comparing the results of sample A to sample B, sample B have a bigger grain size and are heavily deformed as well, as shown in Figure 7.10. After annealing at 200°C, it seems that non-stressed specimen has a bigger grain than stressed sample. This indicates that static compressive stress hinders the grain growth during the 200°C annealing schedule. After annealing at 400°C, one can see that the grain shape is more equiaxed with lots of twins regardless of static compressive stress since it undergone recrystallization and grain growth process. To understand the details of these changes, Σ3 boundaries and misorientation distribution were measured and calculated by OIM, as shown in Figure 7.11 and 7.12. Figure 7.11 shows that the fraction of Σ3 boundaries doesn't increase much after annealing at 200°C, however, it dramatically increases after

annealing at 400°C, especially in non-stressed sample. From this, one can see that static compressive stress hinders the development of Σ3 boundaries during annealing at 400°C. In addition, misorientation distribution was measured using OIM, as shown in Figure 7.12. This figure shows that the static compressive stress decreases the fraction of low angle grain boundaries after annealing at 200°C and the fraction of twin boundaries dramatically increase in non-stressed sample (Figure 7.12b). Comparing the results of sample A to sample B, it can be concluded that the development of Σ3 boundaries and misorientation distribution of copper during annealing strongly depends on the crystallographic texture of copper, compressive stress and annealing temperature.

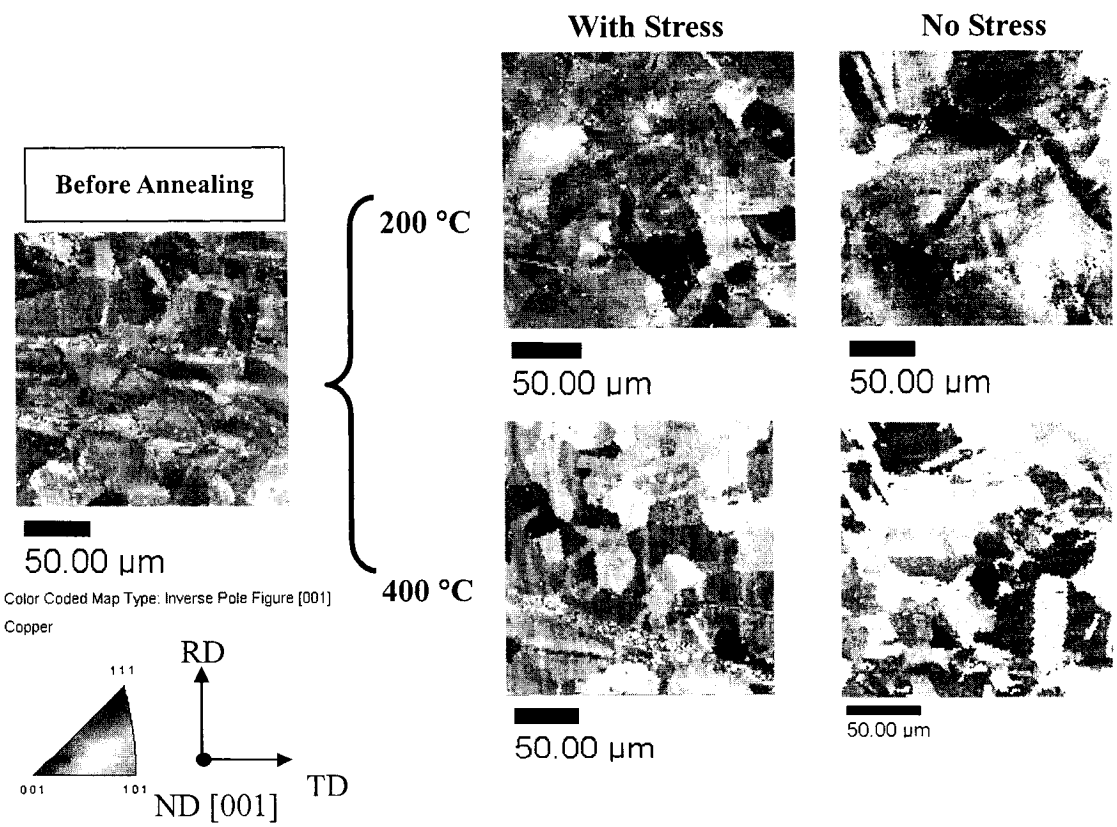


Figure 7.10. Microstructural evolution of sample B with and without compression stress after the different annealing schedules using inverse pole figure maps for the normal direction [001] obtained from OIM.

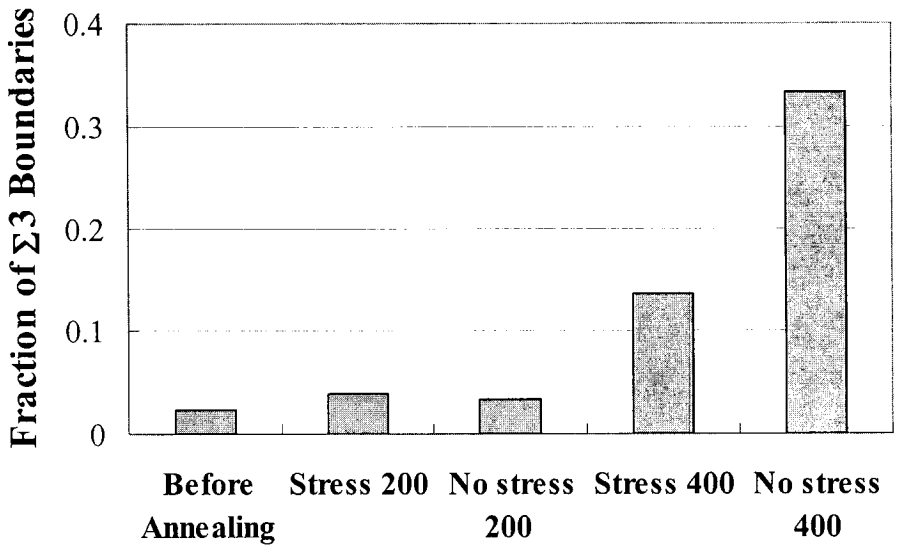


Figure 7.11. Σ3 boundary distribution of sample B with and without static compressive stress after the different annealing schedules.

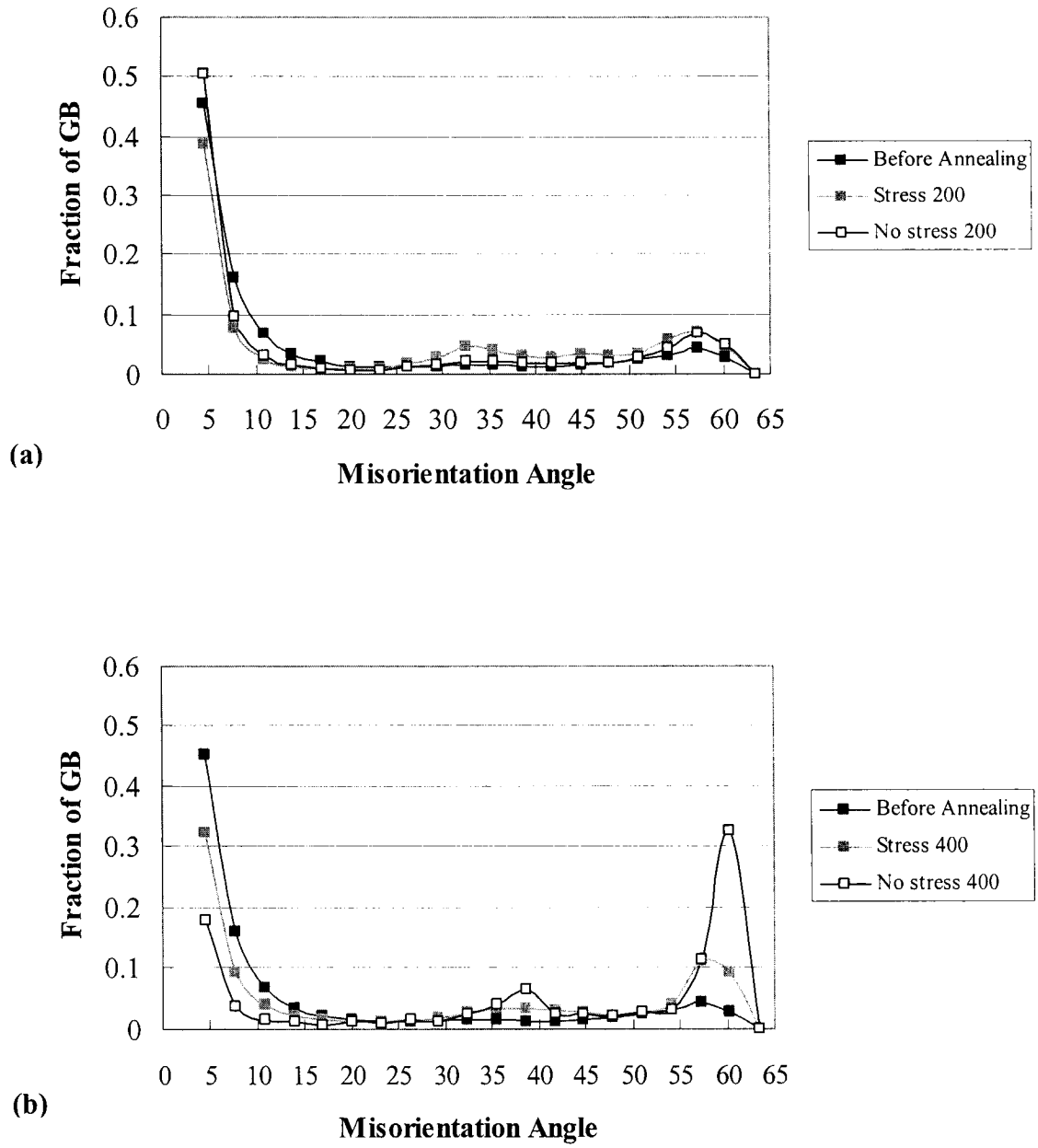


Figure 7.12. Misorientation distribution of sample B after annealing with and without compressive stress: (a) at 200°C, (b) at 400°C.

7.3. Discussion and Summary

In this investigation, it was found that the effect of compressive stress on the textural and microstructural evolution of copper strongly depends on the crystallographic texture of copper prior to annealing and the annealing temperature.

At first, in sample A which has {110} fiber texture, static compressive stress hinders the development of (011)[1$\bar{1}$1] texture after annealing at 200°C, however, the strength of (011)[1$\bar{1}$1] texture decreases with the development of fiber texture component and cube texture becomes stronger after high temperature (400°C) annealing. The effect of compressive stress on the GBCD of copper is negligible and the annealing temperature affects the GBCD of copper significantly: low angle grain boundaries are developed during annealing at 200°C, and twin boundaries are generated by annealing twin formation during annealing at 400°C.

Sample B which has {111} and {100} texture is affected by stress depending on the annealing temperature. After low temperature annealing (200°C), it seems that static compressive stress suppresses the development of {111} texture and enhances the development of {100} texture, however, it helps the development of {111} texture only during annealing at 400°C. Also, the effect of compressive stress on the GBCD of copper is noticeable especially during high temperature annealing. This can be seen through observation of changes in the frequency of $\Sigma 3$ boundaries and differences in grain misorientation distribution after annealing with and without compressive stress.

From the previous results presented in the Chapter 6, it was found that the {111}<112> texture can be developed during annealing along the sidewall direction such alignment approximately satisfy the minimum Young's modulus model [78-81]. Similar observations can be derived from Figure 7.8 as indicated by the arrows for bulk copper sample. The "Stress 200" sample which is annealed at the same temperature has {111}<112> texture. Also, it is known that strong {111} texture, large grain size and high percentage of twin and low angle boundaries would lower the probability of electromigration induced failure [53-57]. According to the result of this physical simulation, it can be recommended that low temperature annealing without stress will be beneficial in developing strong {111} texture, however, high temperature annealing is advisable to achieve optimum GBCD of copper.

Chapter 8

Summary and Conclusions

The main objectives of this study were (1) to understand the influence of substrate texture and electroplating condition on the texture and surface morphology of Cu electrodeposits, (2) to analyze the effects of line width and the annealing process on textural and microstructural evolution of Cu damascene interconnects, and (3) to explain the stress contribution to the textural and microstructural evolution of Cu damascene interconnects during annealing.

Cu electroplating is the most important process in manufacturing Cu damascene interconnects in the electronic chips. Without understanding this process, it is practically difficult to acquire reliable Cu damascene interconnects. Therefore, it is very important to understand the role of various electroplating conditions and substrate texture in the

development of texture and surface morphology of Cu electrodeposits. Three different polycrystalline copper specimens were used as substrates and electrodeposits were plated using different current densities. The mechanism of growth of Cu electrodeposits was discussed and the importance of smooth surface morphology for void-free filling of the Cu trench was emphasized.

In order to understand the influence of line width on textural and microstructural evolution of Cu damascene interconnects, three Cu interconnect samples having different line width were investigated. A new interpretation of textural evolution in damascene interconnects lines with different line widths was suggested, based on the constraints of the sidewalls, substrate texture and the state of stress in the trench.

Also, the effect of the annealing process on textural and microstructural transformation of Cu interconnects having different line widths were studied. In this study, two different samples, as-deposited and annealed at 200°C for 10 minutes, were investigated. To analyze the relationship between the stress distribution and textural evolution in the samples investigated, micro stress changes were calculated as the line width decreased at 200°C using FEM. It was found that the inhomogeneity of stress distribution in Cu interconnects is an important factor which is necessary for understanding textural transformation after annealing. A new interpretation of textural evolution in damascene interconnect lines after annealing is suggested, based on the state of stress and the growth mechanisms of Cu electrodeposits in the trench.

It was realized by FEM investigation that understanding the effect of the stress on textural and microstructural evolution of Cu damascene interconnect during annealing is important, therefore, physical stress simulations were performed using samples having different texture and annealed according to the different annealing schedules (200°C and 400°C). Static compression stress was applied to each sample. The mechanism of textural and microstructural evolution of copper after annealing under compressive stress is discussed.

8.1. Conclusions

The following conclusions are drawn from the work presented in this thesis.

- **The Effects of Substrate Texture and Electroplating Condition on the Texture and Surface Morphology of Copper Electrodeposits**

1. Results obtained from the texture measurements and surface morphology observation showed that substrate texture plays an important role in the formation of texture and surface morphology of copper electrodeposits after electroplating.
2. It was found that the electroplating conditions such as current density can change the texture intensity of Cu electrodeposits: A weak {110} textured specimen revealed the increasing value in the texture intensity with high current density, however, a strong {100} textured specimen has the highest

maximum intensity when plated with low current density. The Po9 sample, which has a strong {111} and weak {100} texture shows fiber texture with a weaken texture intensity as the current density increases.

3. The examination of cross-sections of electrodeposits by OIM demonstrated that the interface between the substrate and electrodeposits isn't distinguishable and the number fraction of Σ3 boundaries increased as current density increased.

4. Using SEM and AFM data it was demonstrated that, at low current density, grains of different orientations have different growth rates and produce a rough morphology. However, the surface of electrodeposits is smoother when the current density used during copper electroplating is high and therefore the effect of substrate texture on the surface morphology is minimized.

5. To improve the resistance of Cu damascene interconnects against failures, such as electromigration induced failure and void formation inside of trench, the optimization of electroplating conditions for different substrate texture is important.

- **The Effects of Line Width on Textural and Microstructural Evolution of Copper Damascene Interconnects**

1. Significant differences were registered in the texture of interconnect lines which have different widths. These differences are, however, contained

within the {111}<uvw> fiber orientation. For narrow 0.18 μm line, there is no clear alignment of <uvw> direction along the line direction, while the <110> direction is dominant in 2.0 μm line width.

2. Textural evolution takes place gradually as the line width decreases and can be explained by the reaction between two different kinds of texture components which have different rotational direction and by the competition of the sidewall and bottom texture components in the trench: scattered {111}<112> and {111}<110> texture in 0.18 μm line width change to {111}<110> in the 2 μm line width interconnects.

3. The proposed interpretation of texture development assigns an important role to differences in the stress state, but also demonstrates that the texture of copper electrodeposits may be inherited from the substrate texture.

4. Bamboo type grain structure was found in the 0.18 μm sample, however the sample with the 2 μm line width has a typical polycrystalline structure. The fraction of Σ3 boundaries is increased as line width increases, however it decreased in the blanket film.

- **The Effects of Annealing Process on Textural and Microstructural Evolution of Copper Damascene Interconnects**

1. A relationship between the stress distribution in the trench and textural and microstructural evolution was established: the stress enhances the {111} <110> texture component and minimize the {111} sidewall components

contribution to overall texture of Cu damascene interconnects.

2. The textural evolution of copper damascene interconnects after annealing depends on the differences in the thermal stress state in the trench and the texture of copper electrodeposits can be affected by the growth mechanism of copper electrodeposits during filling of the trench by copper electroplating.

3. Annealing at 200°C helps the microstructural evolution of Cu damascene interconnect through grain growth: the fraction of the Σ3 boundaries decreases and the fraction of the low angle grain boundaries (LAGB) increases.

● Stress Contribution to Textural and Microstructural Evolution of Copper during Annealing

1. In this investigation, it was demonstrated the role of compressive stress on textural evolution of copper strongly depends on the crystallographic texture of copper and the annealing temperature: In sample A which has {110} fiber texture, static compressive stress hinders the development of (011)[1 $\bar{1}$ 1] texture after annealing at 200°C, however, after high temperature (400°C) annealing, it weakens the texture and strengthens fiber and cube texture. In sample B which has {111} and {100} textures, it seems that static compressive stress suppresses the development of {111} texture and enhances the development of {100} texture during annealing at

200°C, however, it enhances the development of {111} components and weakens {100} texture during annealing at 400°C.

2. In addition, the effect of compressive stress on microstructural evolution of copper strongly depends on the crystallographic texture of copper and annealing temperature: In sample A which has {110} fiber texture, the effect of annealing temperature on the GBCD of copper is much more significant than the effect of compressive stress. However, in sample B which has {111} and {100} textures, static compressive stress decreases the fraction of low angle grain boundaries after annealing at 200°C and the fraction of twin boundaries after annealing at 400°C.

3. After annealing at 200°C, sample B which has {111} and {100} textures with static compressive stress shows the development of {111}<112> texture: it shows a good agreement with the result of copper damascene interconnect which underwent annealing at 200°C (see Chapter 6).

4. Based on the results obtained from the analysis of copper damascene interconnects and the physical simulation of copper, one can conclude that strong (111) texture which improves the resistance against electromigration can be acquired by low temperature annealing without stress, however, high temperature annealing will increase the fraction of low angle grain boundaries and twin boundaries.

8.2. Statement of Originality

The following aspects of the present work constitute original contributions to the field.

1. Strong effects of substrate texture and current density on the texture, microstructure and surface morphology of copper electrodeposits were documented. In particular, it was demonstrated that high current density minimized the effect of substrate texture on the texture, microstructure and surface morphology of copper electrodeposits and allows to generate smooth surface morphology which is beneficial for minimizing probability of void formation in the trench.
2. The details of textural evolution of Cu interconnects as the line width decreases were explained and possible factors responsible for the texture transformation were analyzed.
3. The origin of textural and microstructural evolution of Cu damascene interconnects after annealing was suggested and through thickness inhomogeneity of texture in the trench was described.
4. Contrary to previous studies, it was found that the contribution of sidewall texture components on the overall texture of copper damascene interconnect is negligible: small fraction of sidewall texture component found after Cu electroplating is minimized during the annealing process.
5. The physical simulation of textural evolution of copper during annealing under compressive stress directly illustrates that stress influences texture development: these data can be of use in the optimizing fabrication of Cu damascene interconnects.

8.3. Future Work

1. It was found that the texture and microstructure of Cu damascene interconnects were changed as the line width decreases. According to this, it can be assumed that the specific geometry of the trench, such as the angle between sidewall and bottom which is not always 90°, may affects the textural evolution of Cu interconnects. Therefore, the effect of the geometry of the trench on the textural evolution should be further investigated.
2. The thermal stress which can be generated by the annealing process is the most important factor in textural and microstructural evolution of Cu damascene interconnects. However, the difference between the elastic properties of dielectric materials (from silicon dioxide to the porous low-k materials which is softer than silicon dioxide) and anisotropy of elastic properties of textured Cu electrodeposits can change the states of stress in the Cu trenches.
3. To make a smooth surface after Cu electroplating, CMP (chemical and mechanical polishing) process is needed. However, this process can change the texture and microstructure of the top surface layer of interconnects because the friction forces between abrasive materials and Cu depends on orientation of Cu grains. In this investigation, it was found that each layer of copper in the trench after filling may have different texture. Therefore, it will be of interest to understand the relationship between the friction which can be generated by CMP and the texture of Cu damascene interconnects.

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