An Investigation of The Circuit Parasitics in Flexible Hybrid Electronics

Mohammad Muhtady Muhaisin

Master of Science in Engineering
Electrical and Computer Engineering
McGill University
Montreal, Canada

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Dedication

To the front-line and mental health workers across the world who have served valiantly during the COVID pandemic.

Acknowledgments

This thesis has come to fruition not only because of my contribution but also due to the presence and contribution of other people in my professional and personal life. I would like to take the opportunity to sincerely acknowledge their support and help.

First and foremost, I am grateful to God for blessing me with the success.

Secondly, I want to convey my sincere gratitude to Professor Gordon W. Roberts. Because of Professor Roberts, I got the opportunity to work in this exciting area and learned how to do research. His constant support and mentorship has been one of the biggest contributing factors behind the success of the thesis. In addition to being the student of a good researcher, I have been blessed to work with an excellent educator and a wonderful human being. His passion for research and teaching as well as his genuine concern for the betterment of his students make him the best advisor one can get.

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This thesis would not have been possible without the sacrifice and support of my parents and sisters. Their genuine care, concern, and love have been a source of motivation for me. Thank you for being so strong and supportive.

Lastly, I want to take a moment to thank everyone who has helped me come this far in life by being a part of it, even if for just a minute. My graduate life at McGill University has been a huge learning curve and a surreal experience. This institution and city have widened my eyes and made me a better person. I am truly grateful for this wonderful experience.

Abstract

This thesis investigates the parasitic elements present in the Flexible Hybrid Electronic (FHE) system. Parasitic resistance, inductance, and capacitance from the post-assembly FHE prototypes are extracted by introducing and employing measurement techniques. Subsequently, the proposed techniques are used to demonstrate the susceptibility and record the variation of the aforementioned parasitic components due to the application of the mechanical stress. In doing so, it is evinced that parasitic circuit components do vary due to the application of mechanical stress. Firstly, a modular bending machine is designed to perform Radius of Curvature test on the assembled prototypes. Secondly, a DC-based measurement technique is introduced to extract the individual parasitic contact resistances present between the individual pins of an IC package and the substrate of the post-assembly FHE system. Subsequently, using the measurement technique, variation of the contact resistance due to bending of the substrate is tracked. Thirdly, an AC measurement-based approach is propounded to extract the parasitic resistance, capacitance, and inductance present in the post-assembly FHE system. Variation of these parameters are documented using the method which shows that these parasitic elements are susceptible to the variation of the form factor of the substrate under mechanical stress. Finally, the impact of varying parasitics on the circuit performance and the significance of including varying parasitics in the circuit design are demonstrated. In doing so, the effect of the presence and variation of parasitic shunt capacitance in between the signal forward path at each node and the return path on the start-up of a second-order Wien Bridge oscillator are examined. At first, the steady state oscillation of a second-order Wien Bridge oscillator circuit is investigated using a piecewise linear approach to establish that a pair of right half plane complex conjugate poles is necessary for the oscillation to build up. Then, it is demonstrated that the position of this complex conjugate pole pair responsible for oscillation build-up is sensitive to the variation of the parasitic shunt capacitance. Thereafter, the results illustrate that an increase in the parasitic capacitance, caused by the change in the form factor due to bending, can lead to the failure of the oscillation build-up. Hence, the variation of the parasitics needs to be accounted for and assessed in the design of a flexible and hybrid electronic system.

ABRÉGÉ

Dans cette thèse, les éléments parasites présents dans le système FHE ont été étudiés. Une machine à cintrer a été conçue pour exercer une contrainte mécanique sur les prototypes assemblés de manière contrôlée. Des techniques de mesure ont été introduites pour extraire la résistance parasite, l'inductance et la capacité des prototypes FHE post-assemblage. De plus, lors de l'enregistrement de la variation de ces composants parasites due à l'application de la contrainte mécanique, il a été montré que les éléments parasites varient en raison de l'effet de la contrainte mécanique appliquée. Ensuite, l'importance de considérer et d'inclure l'effet de la variation des parasites sur la conception d'un circuit fonctionnel a été démontrée en étudiant son effet sur le démarrage d'un système électronique omniprésent comme un circuit oscillateur. Le chapitre deux a fourni un flux de travail chronologique et détaillé de la construction de prototypes FHE et a également discuté des défis associés à chaque étape. Au chapitre trois, la conception de la machine à cintrer utilisée pour effectuer le test ROC a été définie. Le chapitre quatre a articulé une approche basée sur la mesure CC pour mesurer les résistances parasites individuelles présentes entre les broches individuelles d'un boîtier IC et le substrat du système FHE post-assemblage. Par la suite, en utilisant la technique de mesure, la variation de la résistance de contact due à la flexion du substrat a été suivie. Ensuite, le chapitre cinq a présenté une approche basée sur la mesure du courant alternatif pour extraire les trois composants parasites - résistance, capacité et inductance présents dans le système FHE post-assemblage. En utilisant la technique, il a été montré qu'en raison de la variation du facteur de forme du substrat sous contrainte, les trois éléments parasites varient. Dans le chapitre six, dans un premier temps, l'oscillation en régime permanent d'un circuit oscillateur WB de second ordre a été étudiée en utilisant une approche linéaire par morceaux qui a démontré qu'une paire de pôles conjugués complexes RHP est nécessaire pour que l'oscillation se développe. Plus tard, l'effet de la présence d'une capacité parasite shunt entre le trajet aller du signal à chaque nœud et le trajet de retour sur ces positions polaires et par la suite, sur le démarrage de l'oscillation a été examiné. Les résultats de la simulation ont déduit que la position de la paire de pôles conjugués complexes est sensible à la variation de la capacité de shunt parasite. Par conséquent, une augmentation de la capacité parasite, provoquée par le changement du facteur de forme dû à la flexion, peut conduire à l'échec de l'accumulation d'oscillation. Par conséquent, il est

évident que la variation des éléments parasites est critique pour les systèmes conçus pour une mise en œuvre dans un domaine flexible et hybride et c'est pourquoi elle devrait être incluse et prise en compte dans la conception de systèmes pour de telles applications.

List of Publications

- **M. M. Muhaisin**, R. A. Khan, J. Telfort, W. Heger, and G. W. Roberts, "Opportunities and challenges in desktop-inkjet based flexible hybrid electronics," in *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 746-749, IEEE, 2019.

- R. A. Khan, **M. M. Muhaisin**, and G. W. Roberts, "An in-situ technique for measuring the individual contact resistance between the pins of an ic package and the board of a flexible hybrid electronic system," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, IEEE, 2020.

- R. A. Khan, **M. M. Muhaisin**, and G. W. Roberts, "Extracting RLC Parasitics from a Flexible Electronic Hybrid Assembly Using On-Chip ESD Protection Circuits." under peer-review in *IEEE Transactions on Circuits and Systems-1*.

Contribution of Author

The contents of this thesis are the result of both collaborative and individual projects under the supervision of Professor Gordon W. Roberts. The contributions of the author of the thesis are:

- The author led the investigation of the workflow of developing FHE systems and identification of the opportunities and challenges that were subsequently investigated in the latter chapters of the thesis.
- The author led the project to design the in-lab built bending machine to perform mechanical tests on the developed prototypes.
- The author contributed to the verification and validification of the technique discussed in chapter four and led the design and execution of the experiments within the scope of this project.
- The author contributed to the design of the experiments and led the execution of the experiments to investigate the variation of the parasitic elements due to bending discussed in chapter five.
- The author individually explored and investigated the project discussed in chapter six.

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List of Acronyms

AC	Alternating Current
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DUT	Device Under Test
ESD	Electrostatic Discharge
FHE	Flexible Hybrid Electronics
FR4	Flame Retardant 4
GND	Ground
IC	Integrated Circuit
I/O	Input and Output
LHP	Left Half Plane
PCB	Printed Circuit Board
PE	Printed Electronics
PUT	Pin Under Test
R2R	Roll to Roll
RLC	Resistance, Inductance, and Capacitance
RHP	Right Half Plane
TDR	Time Domain Reflectometry
UV	Ultraviolet
TL	Transmission Line
VCVS	Voltage-Controlled Voltage Source
WB	Wien Bridge

Chapter 1

Introduction

Flexible Hybrid Electronics is the unification of conventional rigid electronics and flexible, printed electronics. FHE platforms house Si-based integrated circuit (IC), packaged circuit components on flexible substrates that can have other printed components. As a result, it can feature the advantages of a flexible form factor as well as that of conventional circuit components. This combination of attributes has opened the door to a vast array of sensing applications in agricultural, environmental, and predominantly in healthcare sector [1–5]. IDTechEx, a renowned market research agency, forecasts that the worldwide demand for FHE will reach a value of over USD 3 billion in 2030 [6]. Similar market forecasts combining with already visible surge in the demand for FHE products are compelling indicators of the huge potential this technology possesses.

1.1 Background and Literature Review

The emergence of FHE technology is the result of a necessary compromise which aims to capture the beneficial features of rigid and flexible electronics and reduce the effect of their limitations. The concept of printed electronics came into being with a view to manufacturing integrated electronic systems using a technology similar to the conventional printing technology instead of much more expensive and complex integrated circuit (IC) manufac-

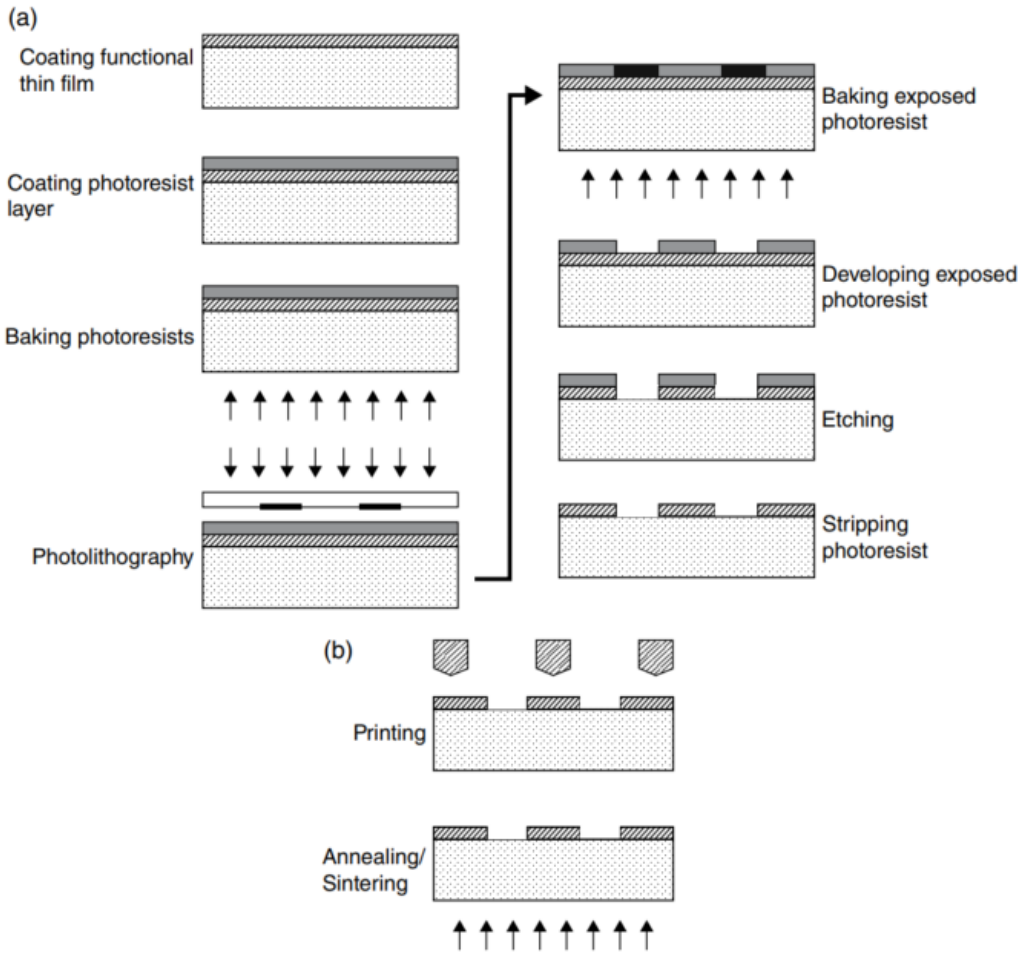


Fig. 1.1 Comparison of IC manufacturing and printing processes: (a) conventional IC manufacturing process, (b) additive printing process.

turing technology [7]. As the IC fabrication industry is heavily investment intensive, the industry is comprised of only a few companies. Conversely, printing is a simple, additive manufacturing process similar to the deposition process in microfabrication. It deposits appropriate materials in form of inks on to a substrate and forms required patterns. This involves lesser steps in comparison to conventional IC fabrication technology as shown in Fig. 1.1 [7]. While fabricating ICs, conventional subtractive manufacturing process removes materials using lithographic patterning and etching. Although this process is very cost efficient, it wastes a lot of material and consumes a lot of energy. An additive process like printing can significantly reduce both the waste of material and energy consumption due to

the absence of thermal evaporation and sputtering deposition steps. Besides being additive in nature, another distinctive feature of printed electronics is that the functionality of the printed device is not restricted to any particular substrate material. As a result, many inexpensive materials can be used in place of silicon as substrates. Besides IC fabrication, subtractive process is also involved in the manufacturing of printed circuit board (PCB). Conventional PCB manufacturing process involves lithographic patterning and acidic etching of copper (Cu)-filled sheets to layout the conductive traces. Acidic etching generates a large amount of waste material detrimental to the environment and wastes most of the Cu. Subtractive etching, if replaced by additive printing to print the conductive traces, can not only reduce the amount of material waste generated and environmental pollution caused, but also reduce the cost of manufacturing due to lesser amount of stages involved. Hence, printed electronics is deemed to have the potential to pave the way to manufacturing low cost, large-area, and green electronic products.

Printed electronics technology can accommodate the use of a wide range of functional materials, both organic and inorganic, in form of inks to form patterns with conducting, semiconducting, dielectric, and optoelectronic properties that form a variety of electronic, optoelectronic, or photovoltaic devices. Wide selection of ink materials, in turn, opens up the possibility of using different kinds of substrates to print the device onto depending on the compatibility and application. As a result, heavier, rigid substrates can be replaced with biodegradable, thin, flexible, lighter substrates - and that is exactly what flexible electronics is. The flexible nature of the substrates allows the circuit to conform to a variety of shapes which contributes to an immense mechanical advantage. As opposed to rigid and bulky nature of the conventional substrates like FR4, flexible substrates like polyimides and elastomeric substrates are conformal by nature. Therefore, they offer better interfacing with arbitrary surfaces. This has resulted a huge surge in the wearable medical sensor research which has the potential to revolutionize healthcare [8–11].

Despite its unique advantages, printed electronics is far from being the ideal method to fabricate electronic devices. Some of the major drawbacks are-

- Poorer resolution of the printed features than that made by the subtractive fabrication method. For example, screen and inkjet printing can attain a maximum resolution of

50 μm and 20 μm respectively. On the other hand, current extreme UV lithography can attain 20 nm of resolution [7].

- Materials deposited using printing technology lack sufficient surface smoothness which causes electric breakdown and charge leakage.
- In spite of having the potential for high throughput due to the roll-to-roll (R2R) feature of the printing technology, there is a dearth of alignment and overlay accuracy, which is essential to the device performance.
- Printed elements, especially transistors, show high process variations. The mismatch varies from 30% to 100% [12–14], which increases to 300% when the substrate is bent [15]. The mismatch severely impacts the circuit performance.

Due to these limitations, printed electronics are still largely confined to small functional blocks [16] such as electrodes [17, 18], energy harvesters [19, 20], flexible thin-film batteries [21], and very simple conditioning circuits [22]. Due to these major limitations in terms of low performance, high power consumption, and limited lifetime, printed electronics is yet to challenge the conventional Si-based rigid electronics. To overcome these limitations, and to leverage the unique advantage of printed electronics, FHE technology is seen as the key enabler. Figure 1.2 illustrates prototypes of a fully printed and a hybrid flexible electronic systems.

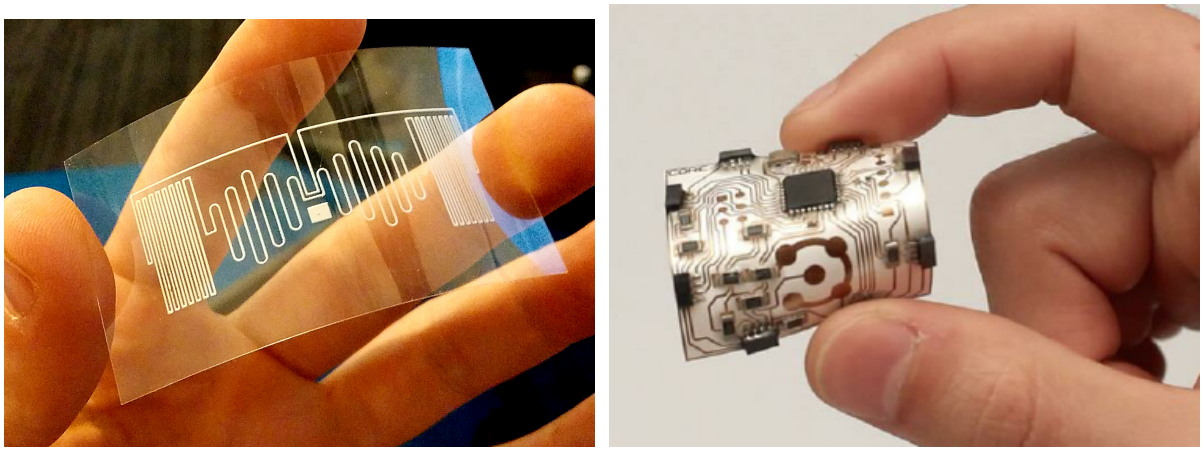


Fig. 1.2 Prototypes: (a)printed electronics, (b) flexible hybrid electronics.

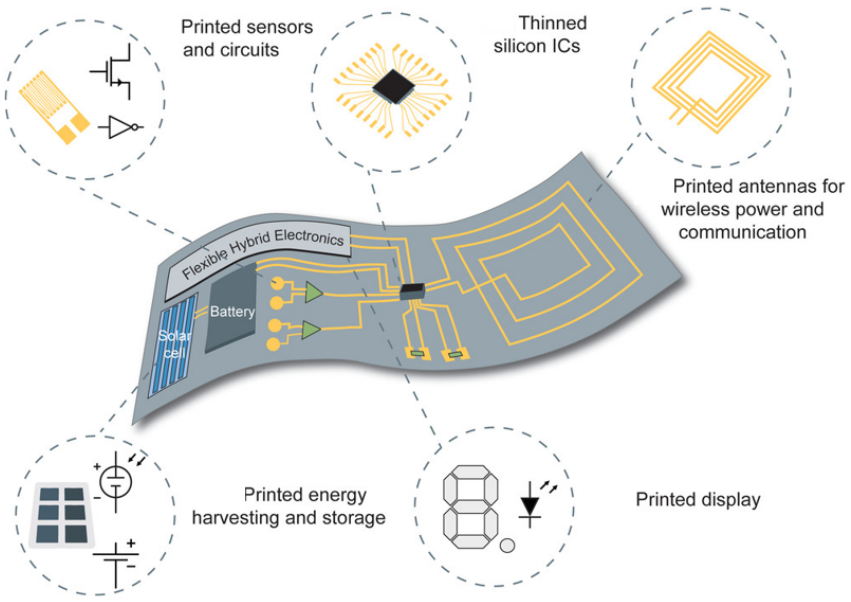


Fig. 1.3 Key building blocks that can be present in an FHE system.

FHE can utilize the flexibility and scalability of printed electronics without compromising the unparalleled performance provided by the Si-based ICs. This has paved a way for the next generation of electronics capable of conforming to the curves of a structure. Figure 1.3 shows the key constituent blocks of an FHE system and Table 1.1 shows a performance comparison of printed electronics with Si ICs [23].

Researchers are utilizing these flexibility features to interface electronics with biology and nature [24–26]. Healthcare is turning out to be one of the biggest application field of FHE as this technology is being utilized to build medical-grade wearable sensors [23]. Soft, conformal, high performance electronic system like FHE can travel around the barrier

Table 1.1 Performance comparison of printed electronics and silicon ICs.

Performance parameter	Silicon ICs	Printed electronics
Charge carrier mobility ($cm^2V^{-1}s^{-1}$)	$\sim$ 1 (organics)	$\sim$ 1000
Switching speed (MHz)	$\sim$ 1	$\sim$ 5000
Operating voltage (V)	$\sim$ 10	$\sim$ 1
Lifetime (year)	$\sim$ 0.1	$\sim$ 10

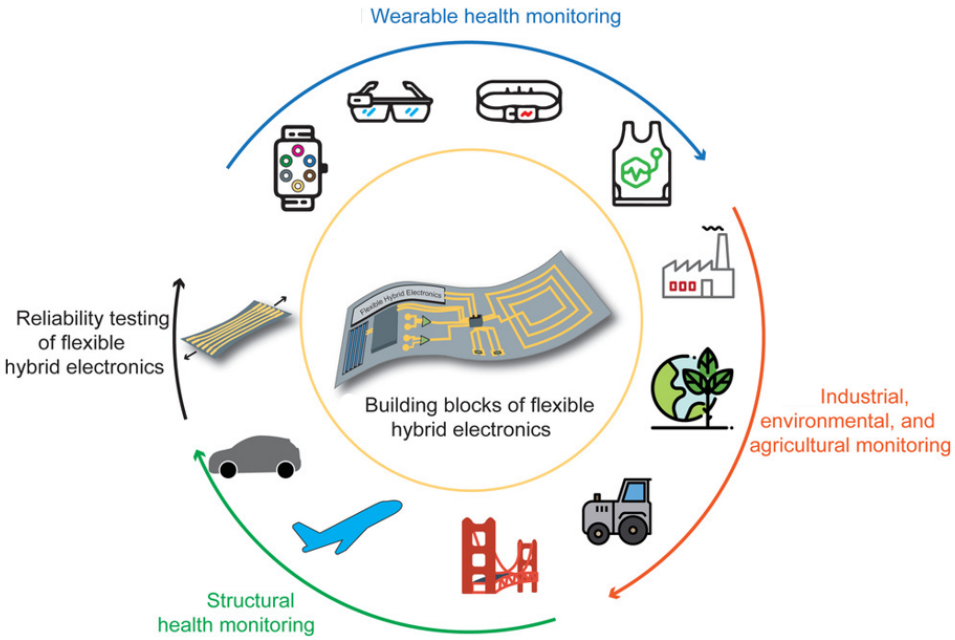


Fig. 1.4 Major research and application domains of FHE systems.

of discomfort without compromising measurement accuracy. FHE have also spread to other application areas such as infrastructural, environmental, and agricultural monitoring. Figure 1.4 illustrates the major application and research domains of FHE systems [23].

Although FHE is capable of providing a more superior system-level performance than fully printed electronics at this stage, it is still an emerging technology. There are a number of design and technological challenges that are needed to be overcome. One of the most critical aspect that requires further research and development is the electrical and mechanical reliability concern of the system. The study of the mechanical reliability encompasses observation and evaluation of the undesired variation of the mechanical properties. Whereas, the study of electrical reliability is the study of observation and evaluation of the undesired variations in the electrical properties, for example, signal integrity of a designed system. As rigid electronic components are being assembled on flexible substrates for applications that assert mechanical stress on the assembly, structural, i.e., mechanical integrity of FHE devices vary hugely in their susceptibility to the effects of mechanical stress. Furthermore, different mechanical stresses also affect the electrical parameters of the system differently [15]. Structural integrity concerns that arise from one-time or repeated

application of mechanical stress transduces into signal integrity concerns of the system. For example, alteration of the form factor of the substrate as well as the integrity of the attachment of the circuit components with the substrate is a potential source of circuit parasitics, which can be detrimental to the circuit performance. Hence, investigation of the parasitic elements in assessing the electrical and mechanical reliability of an FHE assembly exposed to mechanical stress is important towards achieving success for this technology.

The technology being nascent, the literatures found on the electrical and mechanical reliability of FHE are limited in number. Most of the studies are centered around the study of mechanical reliability of printed conductive traces on thin, conformal substrates. Different printing processes have been employed [27–29] and the reliability of the printed traces have been evaluated by observing formation and propagation of cracks under different types of mechanical stresses such as bending, stretching, and torsion [30]. Furthermore, several numerical models have been developed to analyze different failure modes of the printed traces [31]. But these studies might lack accuracy in assessing the reliability of a fully assembled and fabricated FHE system. As these studies evaluate the reliability of the printed traces only, they do not take into account the additional thermal stress caused by the solder reflow process while assembling the electronic components on the substrates [32].

Fabrication of FHE involves printing of the conductive traces, necessary interconnects and subsequent attachment of electronic components on solder pads printed on the substrate. The process of mounting and attaching rigid electronic components on flexible substrates exerts mechanical and thermal stress on the printed pad and the substrate [32]. As a result, cracks are formed in the printed conductors and solder joints. Recurrent application of stress leads to the propagation of those cracks which ultimately leads to the loss of electrical connection [33, 34]. Furthermore, due to the presence of the assembled components on the substrate, impact and distribution of stress on the substrate are different from that of a substrate containing only the printed components [35]. Hence, from a practical viewpoint, post-assembly assessment of the impact of mechanical stress on FHE is more insightful and judicious. Varun et al. [32] has performed a system-level study on a fully assembled FHE platform to assess and improve the mechanical reliability parameters. In that study, as illustrated in Fig. 1.5 (a), optical inspection has been utilized to observe and track the formation and propagation of cracks in the printed copper (Cu) circuitry

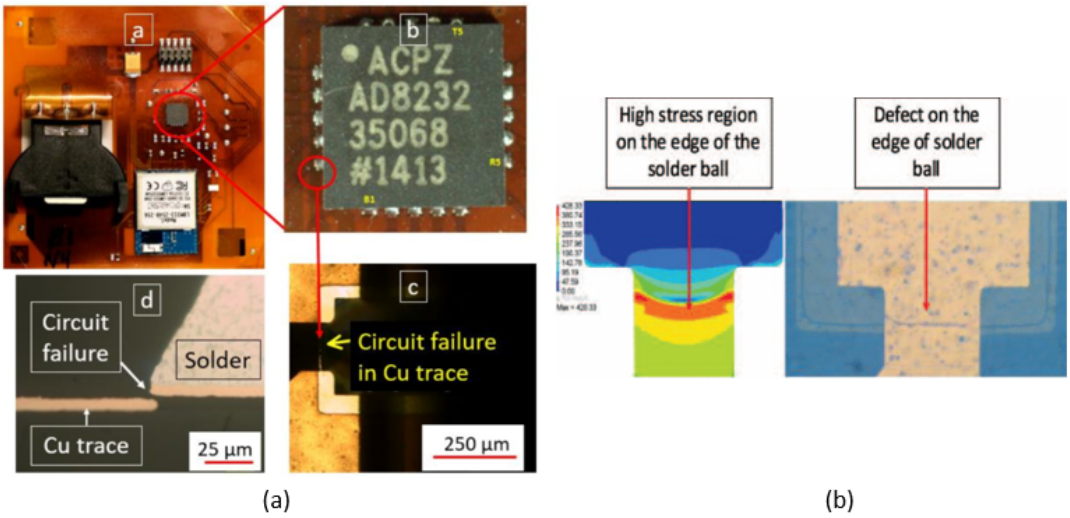


Fig. 1.5 Formation of solder joint defect due to bending.

and gradual loss of attachment of rigid components with printed traces. Although test vehicle array resistance has been measured after different manufacturing steps, points of attachments have not been assessed by any measurement technique individually. But a simulation carried out in this study identifies the solder joint or the point of contact of the electronic components with the substrate as the area under the highest amount of stress while bent, as shown in Fig. 1.5 (b). Hence, it is inferred that the solder joints are more prone to damage and critical to the proper functioning of the assembled FHE system which is why their susceptibility to the variation of the mechanical stress needs to be measured and assessed.

To quantify the effect of mechanical stress on printed traces using an electrical parameter, variation of the trace resistance is recorded and utilized. As ideally, traces are supposed to have zero resistance, this inherent resistance present in the traces can be termed as parasitic trace resistance. Additionally, due to attachment of electronic components on the substrate by means of soldering or applying adhesives, ancillary resistance forms named parasitic contact resistance. Several researches demonstrate that with repeated application of mechanical stress on printed traces, parasitic trace resistance shows an increasing trend which has been correlated with the formation and propagation of cracks in the traces under test. Hence, parasitic resistance can not only be used as an indicator of the mechanical

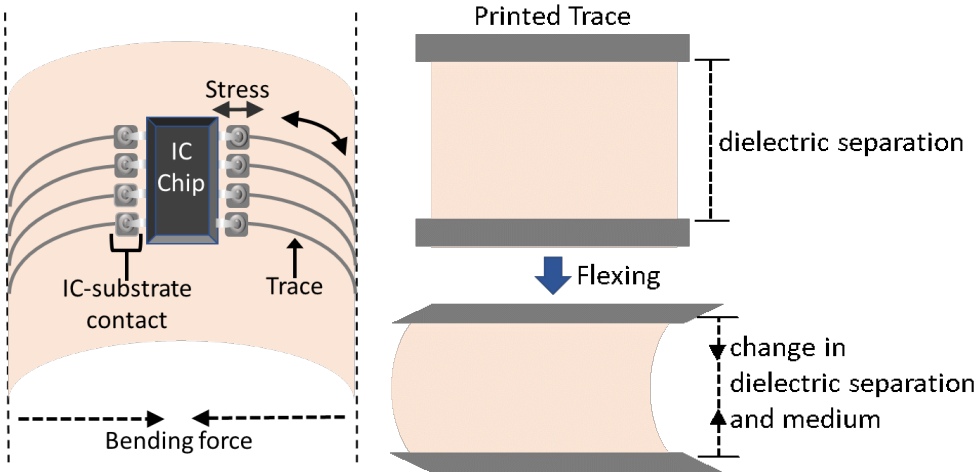


Fig. 1.6 Impact of flexing an FHE assembly: a) stress induced on printed conductors b) change in dielectric separation and medium between two printed conductors.

reliability but also be used to evaluate the electrical reliability of the circuit, which is fundamental towards the successful operation of the system designed. Hitherto, post-assembly variation of the parasitic contact resistance formed by the solder joint in between the IC package and the substrate has not been been studied, to the best of our knowledge. Besides parasitic resistances, parasitic inductance and capacitance are also inherent in every electronic system. No study is found to have reported the effect of mechanical stress on other inherent circuit parasitics such as parasitic inductance and capacitance, to the best of our knowledge. On-board parasitic inductance and capacitance is dominantly dependent on the dimension of the printed conductors and the dielectric separation in between. As mechanical stress alters the physical dimension of the substrate which in turn changes the dielectric separation, as illustrated in Fig. 1.6, variation of parasitic inductance and capacitance is highly likely. Although negligible at lower frequencies, high frequency applications accentuate their presence which causes concerns to the signal integrity of a system. So, the measurement of all three parasitic components- resistance, inductance, capacitance (RLC) inherent in the circuit and their susceptibility to the application of mechanical stress is critical. In conjunction, the study of the impact of their susceptibility on the performance of the designed system will result in a more accurate and all-round assessment of mechanical and electrical reliability of the assembled FHE system.

1.2 Research Scope

Circuit parasitics, although unavoidable, are very small quantities. As a result, their accurate measurement is challenging and more sensitive to external noise and probe parasitics. Two-port sensing, also known as Kelvin sensing, can eliminate the probe parasitics such as lead and contact resistance [36]. This is a huge advantage for precise measurement of small quantities, hence recommended and used in measuring circuit parasitics. However, at the post-assembly level, a two-port measurement of circuit parasitics is challenging to implement as this requires post-solder probing at the IC pins. This is difficult to accomplish as the IC pins are extremely small and often located underneath the IC package with no access. Even when the IC pins are accessible, repeated probing at the pins to track the parasitics from an FHE assembly can accumulate additional stress at the IC-substrate contact, thereby altering the measured quantity. Consequently, it is necessary to find a one-port, on-board measurement technique that eliminates the need for probing at the IC pins. Thereupon, a one-port measurement technique is needed to be devised and deployed to extract the parasitic elements. Then, the technique needs to be applied to record any change in the value of those respective elements when the assembly is subjected to mechanical stress. For that, a modular bending machine needs to be fashioned capable of subjecting the assembled prototype to controlled mechanical stress. Finally, if the parasitic elements vary, the varying parasitic elements are needed to be accounted for and incorporated in the circuit design.

In this research, at first, a detailed workflow of building FHE systems is provided along with the associated challenges. Then, the design of a new, in-lab built bending machine to perform bending test on the prototype is articulated. Next, a one-port, DC measurement-based method is presented for measuring the individual contact resistance between the pins of an IC package and a flexible substrate used in FHE systems. Afterwards, a one-port, AC measurement-based approach for post-assembly extraction of RLC parasitics from a flexible hybrid electronics prototype is presented. In both cases, on-chip ESD protection circuits inherent in ICs are exploited to perform one-port measurements at on-board test points. In their respective studies, the techniques are subsequently employed to investigate and reveal the susceptibility of these parasitic elements inherent in the assembled FHE prototypes to the variation of the form factor upon the application of mechanical stress.

Finally, to demonstrate the impact of varying parasitics on the circuit performance and the significance of including varying parasitics in the circuit design, the start-up of a second-order Wien Bridge oscillator circuit is investigated and the effect of variation of parasitic shunt capacitance present in between the signal forward path of each node and return path on the oscillation start-up is reported. So, the scope of this research can be laid out as follows:

- A review of the workflow and its associated challenges in building FHE systems.
- Design of the in-lab built, modular bending machine.
- Extraction of the inherent parasitic contact resistance between the IC pins and the board of an FHE system and the variation thereof due to mechanical stress in form of bending using a DC-based technique.
- Extraction of inherent parasitic resistance, inductance, and capacitance of an FHE assembly and the variation thereof due to mechanical stress in form of bending using an AC-based technique.
- Investigation of the impact of the presence and variation of parasitic shunt capacitance on the start-up of a second-order Wien Bridge oscillator circuit.

1.3 Thesis Outline

This thesis contains seven chapters. **Chapter 1** contains the necessary background, research motivation and its scopes. In **Chapter 2**, details of the workflow used to design, print, assemble, and test the FHE prototypes is discussed along with the associated challenges followed by the design of an in-lab built, modular bending machine built to perform Radius of Curvature (ROC) test on the assembled prototype in **Chapter 3**. **Chapter 4** discusses the extraction of the inherent and varying individual contact resistance between the pins of an IC package and the board of an FHE system by delineating the DC-based, one-port measurement technique. Moving on, **Chapter 5** discusses the extraction of the inherent and varying RLC parasitics from an FHE assembly using an AC-based, one-port

measurement method. Finally, **Chapter 6** investigates the steady stage oscillation of a second-order Wien Bridge oscillator and discusses the impact of varying parasitic capacitance on the start up of the oscillator. The thesis ends with the conclusion in **Chapter 7**.

Chapter 2

A Review of The Workflow And The Challenges Associated With Building FHE Systems

Creating functional FHE systems involves steps such as, circuit design, selection of materials, printing, assembly, and testing of the assembled system. In comparison to the workflow of conventional rigid PCBs, Flexible PCB (FPCB) workflow requires additional considerations at each of these stages and has supplementary challenges. This chapter chronologically delineates the steps involved and challenges associated with the workflow of realizing FHE systems.

2.1 Circuit Design And Challenges

2.1.1 Circuit Design

The first step of the workflow is the design of the system that involves preparing the schematic and layout of the circuit. These are designed by using standard PCB design software, e.g., Altium PCB Designer. At each level, the circuit can be simulated to observe

the ideal behavior of the circuit and later, can be used as a reference to compare the performance of the prepared prototype with. The PCB layout upon passing the design rule checks (DRC) is then converted into gerber files, which is the standard file format being used in the industry for printing patterns. In addition to generating gerber files for each layer of the FPCB, Numeric Control (NC) drill files are also generated to specify the location of sizes of the thru-holes and vias.

2.1.2 Challenges

Although there are no challenges in preparing the schematic of the circuit, the design of the layout of the respective schematic gets restricted by the limitations of the printing technology. Hence, the design rules of the circuit layout have to be set in accordance with the features attainable by the printing mechanisms. The design of the layout is challenged by, but not limited to, the following features:

- Minimum IC pin-to-pin clearance.
- Minimum trace width.
- Minimum trace separation.
- Minimum footprint dimension.
- Maximum dimension of the printable area.

2.2 Material Selection and Challenges

This step involves selection of substrate as well as material type for the ink and adhesives. Selection criteria of each of these along with the challenges associated with them are discussed below.

2.2.1 Substrate Selection And The Associated Challenges

The substrate provides the physical structure of the PCB. In the context of FHE, in addition to being flexible, for a substrate to be deemed suitable, it must fulfill several other criteria, ranging from physical and chemical properties to manufacturing cost [37]. It is to be considered that, the selection of a substrate often dictates the maximum fabrication temperature as well as the flexibility or stretchability of the circuit, among other features. The selection of a substrate is also strongly dependent on and challenged by factors such as, dimensional stability, thermal stability, curing temperature of the ink and the adhesives, solvent compatibility, and moisture absorption [38].

2.2.2 Ink Selection And Associated Challenges

Basing on the requirement, inks made up of either organic or inorganic material can be selected which can be conducting, semiconducting or nonconducting in nature. For example, in case of a conductive ink, the chosen ink must be suitable for use as a conductor and must also be compatible with the printing method employed, as well with the substrate chosen. The size of the particles must be much smaller than the nozzle used to dispense the ink. Should they be too large, there is a risk of clogging a nozzle, whose replacement can be costly and time-consuming. The selection of ink is also challenged by its curing temperature as prolonged exposure of the substrate to a heightened temperature beyond its compatibility can cause critical damage. Additionally, flexibility of the cured ink is another important criterion to consider as inability to maintain conductivity when flexed can critically impair the circuit performance.

2.2.3 Adhesive Selection And Associated Challenges

The adhesives in form of solder paste or epoxy are applied at the contact point of the electronic component and the substrate and then sintered by applying heat. The basic purpose of using adhesives is to keep the electronic components attached to the substrate and maintain conductivity. Additionally, in its application in FPCB realization, adhesives

have to also be able to withstand the mechanical stress applied to the assembly. The challenge of selecting appropriate adhesive material lies in the trade off between its flexibility, conductivity, sintering temperature, and adhesion.

2.3 Circuit Printing And Challenges

This stage involves printing of the desired patterns according to the layout prepared. In this step, the substrate is cleaned and placed on the printing area of the machine. Then upon performing necessary steps such as, calibration, alignment, and height profile calculation to ensure appropriate and uniform deposition of the ink as per requirement, the pattern is laid out. Afterwards, the printed pattern is sintered by applying heat. If vias and thru-holes are required to be drilled, they are drilled after sintering the pattern. Later, the vias are filled with ink and cured to ensure conductivity among the different layers of the FPCB.

The printing process can be either additive or subtractive. In the additive process of printing, materials are printed onto the substrate as needed, yielding the final pattern in a single step. Whereas in subtractive process, layers of materials are deposited onto the substrate and etched away during subsequent steps. For the purpose of this thesis, both additive and subtractive printing processes have been used to lay out the pattern, as per requirement. The following discussion delineates the additive printing technology employed to print on FPCBs and the challenges associated. As subtractive process is a well-established technology and its challenges have been studied extensively, this topic has not been included in this discussion.

The recent surge in the additive printing research has resulted in development of different types of additive printing mechanisms such as, Gravure, Flexography, Aerosol Jet, and Inkjet printing. As for the purpose of this thesis, desktop-inkjet based additive printing mechanism has been used to additively print the prototypes with the help of Voltera V-One printing machine, this technology is delineated below.

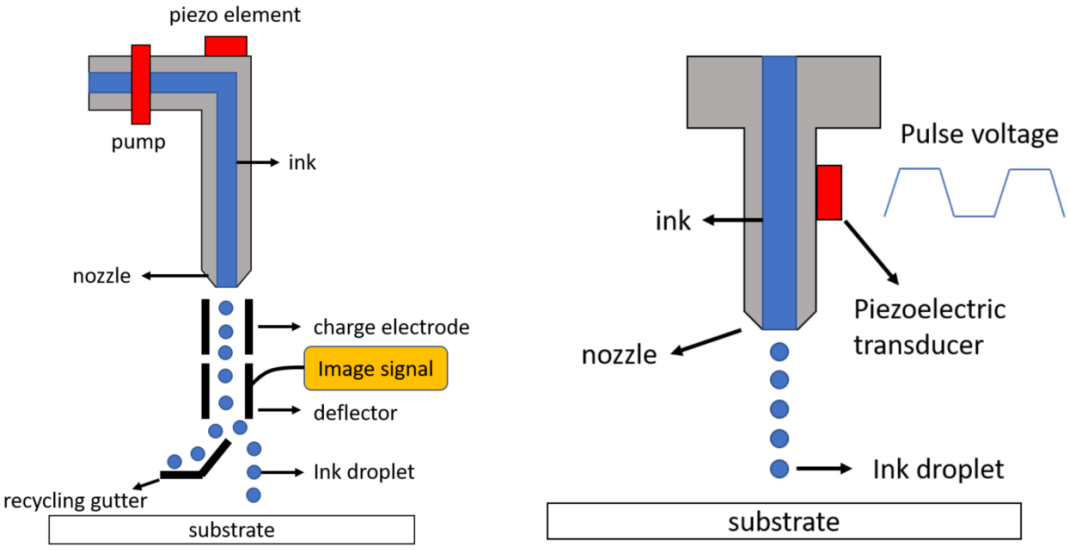


Fig. 2.1 (a) Continuous inkjet printing (CIJ) and (b) drop-on-demand (DOD) printing.

2.3.1 Desktop-Inkjet Based Additive Printing Mechanism

In this printing mechanism, the prepared circuit layout is interpreted by converting it into a monochrome bitmap format. The pixels in that file then represent the areas where the ink is to be deposited. Ink deposition can be continuous or on demand. As both the techniques can deposit ink without coming in contact with the printing area, both of them can be used to generate patterns on rigid and flexible substrates [39]. Figure 2.1 illustrates the mechanisms behind these two inkjet printing techniques [40]. In case of Continuous Inkjet Printing (CIJ), the ink keeps on flowing continuously and the ink droplets are charged by an electrode to get deflected by a deflector. The image signal is applied to the deflector which enables it to deflect the unwanted droplets to the recycling gutter for reuse. On the other hand, in Drop on Demand (DOD) method, used by the Voltera V-One printing machine, the ink is deposited on the substrate only if the nozzle is switched on. A pulse voltage is applied on the piezoelectric transducer to convert the electrical signal to mechanical on-and-off signal. As a result, ink is deposited on appropriate locations based on the bitmap generated and the desired pattern is obtained.

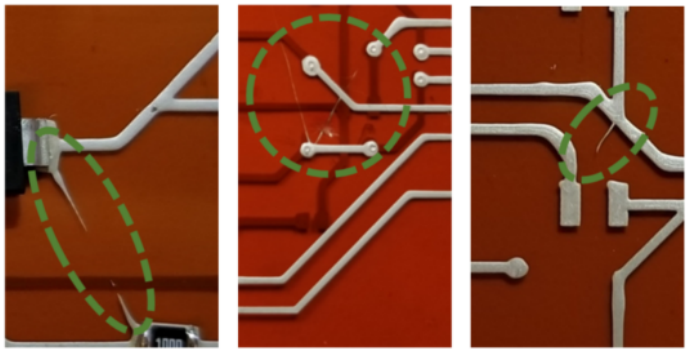


Fig. 2.2 Stringing effect.

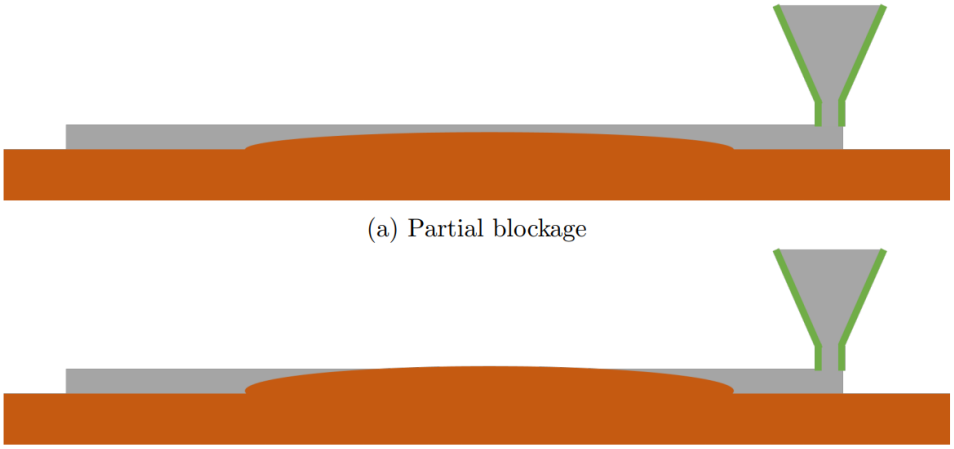
2.3.2 Challenges

Stringing Effect

Variation in the flow rate of the ink causes nonuniformity to the pattern printed using inkjet printing. As a result, the conductivity gets affected. For example, higher flow rate of conductive traces results in better conductivity. But it needs to be considered that this phenomenon can also lead to undesired shorts among closely spaced conductive traces due to the Stringing Effect, as illustrated in Fig. 2.2.

Misalignment

Before printing begins, the substrate is placed manually on the printing area of the machine and attached to it using adhesives. The alignment step is required to be performed with a view to determining the position of the substrate on the printing area. It is done by holding the substrate down using clamps and then the measurement is taken by locating the diagonally separated fiducials. In case of double layer printing using this technology, the removal of the clamps and subsequent re-placement of the substrate to print on different layers is done manually. Accuracy of manual alignment with the position of the fiducials in the printing system is constrained by the limitation of visual inspection and step size in the movement of the probe. Furthermore, before moving ahead with printing on additional



(a) Partial blockage

(b) Full blockage

Fig. 2.3 Effect of partial and full blockages of the print nozzle caused by the curvature of the substrate.

layers, the first printed layer needs to be sintered. During sintering, the thermal expansion of substrate causes shift in alignment. To avoid this, a substrate with low CTE needs to be used, which is another challenge involved in the process.

Miscalculation of The Height Profile

Immediately after the alignment step is performed, a probe is used to measure the height of multiple points on the substrate in order to create a height profile to ensure uniform deposition of the ink. Miscalculation in the height profile measurement can happen due to the presence of air bubbles underneath the substrate upon placing it on the printing area. If air bubble is trapped between the substrate and the platform underneath it, the bubble may be compressed by the probe until the height switch is triggered. The resulting measured height will be that of the compressed bubble, and not of its undisturbed height. During printing, this situation can lead to partial or full blockages of traces. An illustration of the phenomenon is provided in Fig. 2.3.

2.4 Circuit Assembly And Challenges

2.4.1 Circuit Assembly

After printing and sintering the desired layout, the components are assembled on the substrate. In the circuit design stage, the necessary footprints were designed which includes solder pads of appropriate dimensions onto which the electronic components are placed. In attaching the components, either metal epoxy or solder paste can be used. If solder paste is used, then the component is at first placed on the solder pad and then heat is applied locally using soldering iron to assemble the components. On the other hand, if metal epoxy is chosen to be applied, upon placing the components on the pad, epoxy is applied at appropriate places and the substrate is heated by placing it inside a heating chamber such as convection oven.

2.4.2 Challenges

Thermal Treatment

While attaching the components by applying localized heat to the solder joints, the flexible substrate, materials, and electronic components undergo fast temperature transitions. Fast change of temperature increases the degradation of integrity of the component connection because of the high thermal gradient and mechanical stress imposed on the component-solder paste interface. This also has the potential to damage the substrate by forming undesired creases. On the other hand, if metal epoxy is used and subsequently cured by thermal reflow in a convection oven, then the substrate and the printed inks go through multiple thermal cycles. This might cause undesired variation to their structural integrity and also exerts additional thermal stress mostly along the solder-component interface. Moreover, the selection of the adhesive material should be made in such a way that the temperature required for the thermal reflow of the solder paste remains below the glass transition temperature, T_g of the substrate used. Also, depending upon the substrate used, mismatch of Coefficient of Temperature Expansion (CTE) among the adhesive, conductive ink, component, and substrate affects the respective interconnect interfaces, which is

(a) Top view (b) Side view

Fig. 2.4 Test interface used to test printed circuits.

another challenge to be considered in this stage.

2.5 Electrical Testing of The Assembled Prototype And The Challenges

2.5.1 Post-Assembly Electrical Testing

In this stage, the assembled prototypes are tested to ascertain proper attachment of the components and measure critical circuit parameters such as circuit parasitics. Tests are needed to be performed both before and after the application of the mechanical stress for FPCBs. Post-assembly testing by means of electrical measurement allows for the verification of complex designs and offers a way to verify performance that is more reliable than mere visual or optical inspection.

In testing the assembled prototypes, electrical measurements are performed to identity any undesired shorts or opens, among other tests that might be required depending upon the application. One way to do this is by manually performing a short-circuit test on each node using a multimeter or source-meter. The resistant measured should be very close to the resistance of the printed trace. Another approach can be performing the tests using special test interfaces, as shown in Fig. 2.4 [38].

In this approach, a customized, modular test interface is built to create a bridge between the test equipment and the FPCB. Such interfaces use spring-loaded contacts to establish connection with the printed test pads on the circuit. An important feature of this type of test interface is the facility of the modular placement of the spring-loaded contacts which allows this interface to be used with a wide range of circuit designs. Using test interfaces also allows to perform all the measurements in just one step which is a tremendous advantage over performing manual measurements.

Another important post-assembly measurement criterion to assess the electrical reliability of the FHE system is that of measuring circuit parasitics. The details of their measurement methodologies along with their advantages and challenges will be delineated in chapters 3 and 4.

2.5.2 Challenges

One of the challenges associated with taking post-assembly electrical measurements is that the measurement probes exert pressure on the pads while establishing connections. Repeated exertion of pressure might damage the printed pads and open the circuit. Furthermore, if the probes are required to be placed on the IC pins to measure parameters such as solder joint resistance, that puts pressure on the solder joint which might cause damage to its integrity.

In addition to that, if post-solder probing is required at the IC pins, that can sometimes be very challenging to achieve for small-sized surface mount packages as their minute dimension limits the accessibility of the measurement probes. It can be even impossible to achieve for packages like QFN due to having pinouts underneath the structure.

As FPCBs are required to operate in bent conditions, their electrical performance has to be tested in such conditions as well. In these kinds of situations using test interfaces built to perform above-mentioned tests cannot be utilized because of their rigid and flat form factor which leads to assorting to manual testing of the desired electrical parameters.

Table 2.1 Summary of bending tests of interest from IPC-9204.

Name of the test	Description
Variable radius bending	Specimen is bent in a U-shape between two plates that are then raised and compressed to cyclically change the radius of the specimen
Variable angle bending	Maintained under a specific tensile load, the specimen is flexed back and forth to a specific angle about a mandrel
Free arc bending	Specimen is fixed horizontally to two fixtures. One fixture moves back and forth, thus changing the bending radius cyclically.
Loop Bending	Specimen is held in a looped fixture with fixed lateral tension while a probe applies a strain on the center of the specimen.

2.6 Post-Assembly Mechanical Testing And The Challenges

2.6.1 Post-Assembly Mechanical Testing

Post-assembly mechanical testing is required to be performed to evaluate the structural or mechanical integrity of the prototype. For FPCB, it is done by exerting desired mechanical stress, as demanded by the application, using a controlled setup in a controlled environment. It is done with a view to obtaining insight into the mechanical behavior of the assembled prototype under deformation for assessing its mechanical reliability and limitations.

Although there are no concrete standards that outline the mechanical testing of FHE systems, Institute of Printed Circuits (IPC) has compiled some "suggested test methods deemed appropriate for consideration in materials and properties testing" in a document titled "IPC-9204: A Guideline on Flexibility and Stretchability Test Methods for Printed Electronics". The mechanical parameters included in that document describes procedures for testing bending and stretchability among other types of tests [41]. Table 2.1 includes some of the bending tests that are relevant to the scope of this thesis.

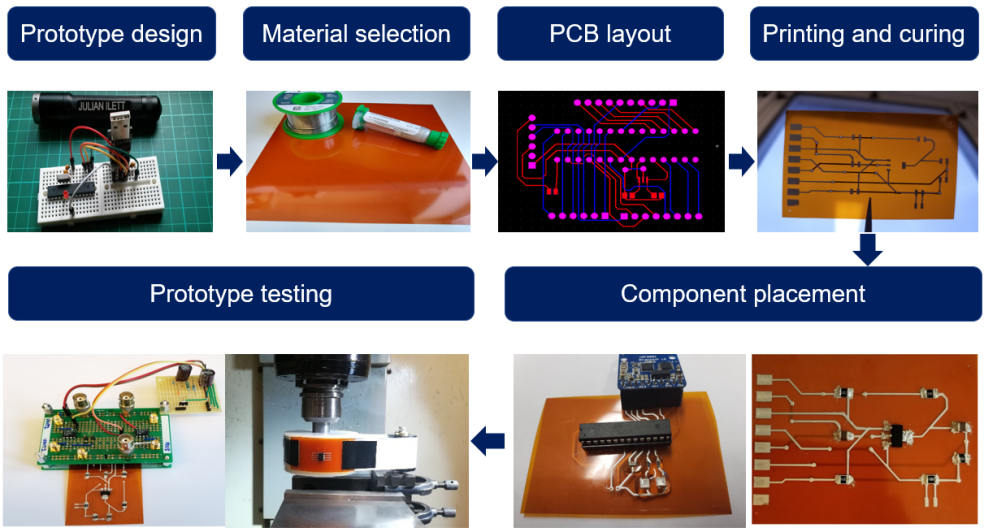


Fig. 2.5 Workflow of fabricating and testing FHE prototypes using additive manufacturing technology.

2.6.2 Challenges

A major challenge in performing mechanical tests on FHE systems is the appropriate mimicking of the mechanical stress that will be imposed on the system in real-life applications. Furthermore, there are limitations and challenges with regards to limiting the application of undesired stress on the FHE assembly while testing them in a controlled lab environment. Further review of the challenges of different types of tests and machines built to perform those tests have been provided in the following chapter while introducing the design of a bending machine capable of performing a modified version of variable radius bending test called ROC test, as required for the purpose of this thesis.

2.7 Chapter Summary

In this chapter, the workflow of building FHE systems is discussed. Moreover, the challenges associated with each of the stages have been mentioned. The summary of the workflow is illustrated in Fig. 2.5 which contains the sequential arrangement of each stages in the workflow from the beginning (prototype design) to the end (prototype testing).

Chapter 3

The Design of The Bending Machine

When designed to function in a bent condition such as in wearable devices and foldable display applications, it is necessary to test the performance and reliability of the fabricated prototype in such scenarios. That requires designing a setup which will be able to mimic the appropriate mechanical deformation and enable the researchers to observe and analyze the prototype's behavior. In this chapter, the design of a machine built and used to perform a type of bending test called the radius of curvature test, denoted in this thesis as the ROC test, is discussed. In this test, mechanical stress is applied to the assembled FHE prototype so that its contour takes the shape of the circumference of a circle with a certain radius. Then, that radius, i.e., radius of curvature is used as a metric that can be correlated to the stress applied. Moreover, this chapter contains a short literature review of the relevant bending setups that have been designed and implemented to achieve similar goals.

3.1 Literature Review

Several studies have been carried out to design devices which can apply one-time or repetitive mechanical stress on the prototypes in a controlled manner. The designs can broadly be categorized into two categories, namely, static bending setups and dynamic bending setups. Dynamic bending setups are designed to apply stress on the substrate to bend and

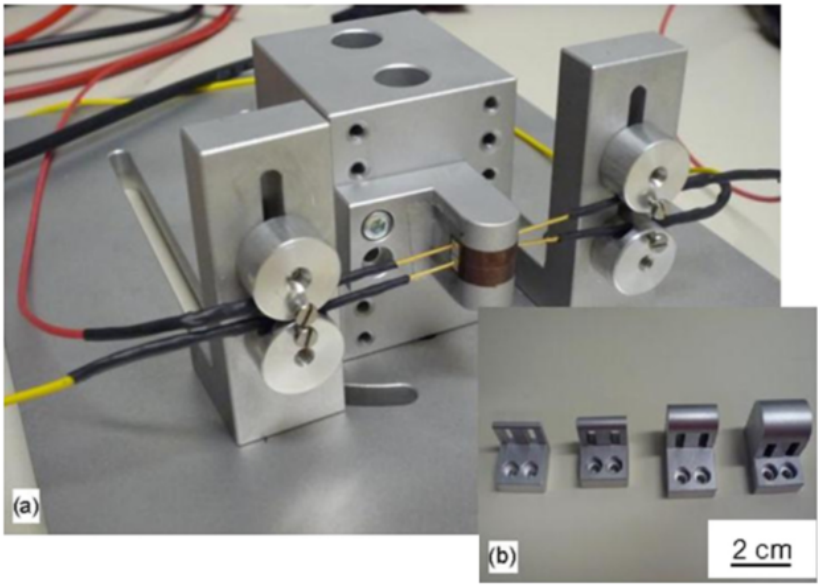


Fig. 3.1 (a) Bending setup containing Kelvin test measurement feature, (b) Bending accessories used for bending at different radii of curvature.

flatten it in a repeatable manner whereas static bending setups are designed to bend the substrates once and hold it in that position.

A static bending setup is most importantly comprised of a rigid structure having a desired contour. an FHE prototype is placed on and pushed against that structure to bend it accordingly. A static bending setup also contains arrangements in form of clamps or adhesives to hold the prototype in the bent shape. It might also have measurement probes built in the setup to enable performing electrical and optical measurements to assess the required parameters. Molina-Lopez et al. [42] built a static bending setup to measure the trace resistances, as shown in Fig. 3.1 . This setup has modular curved surfaces which enables bending the flexible substrate to different radii of curvature. Moreover, the setup contains measurement probes to enable Kelvin test measurements on the bent substrate. Figure 3.2 illustrates the static bending mechanism used by Heger et al. [38] where mandrels were used to wrap the substrate around and apply mechanical stress; electrical measurements were taken after detaching the substrate from the mandrel and re-flattening it.

(a) Side-view (b) Top-view

Fig. 3.2 The mandrel-based setup used to measure bent trace conductivity.

Although static bending setups have their utilities, most of the studies are found to be around designing dynamic or cyclic bending setups. T. Happonen [43] fashioned an in-house built machine using a LabView-controlled stepper motor which rotates the arms of the machinery resulting in a horizontally moving holder, while the other holder remains fixed to bend the substrate attached to these holders. An illustration of the concept is shown in Fig. 3.3 (a). H Gao et al. [44] designed a similar setup and established a relation between the linear displacement with the radius of curvature formed. One caveat of this kind of setup is that the stress due to the deformation is higher towards the end of the clamps, which is usually undesired. A slight modification of this approach has also been implemented where, to make the distribution of stress more uniform, both ends of the substrate are kept free without any clamps, whose concept is illustrated in Fig. 3.3 (b). This approach, however, has lesser control over the positional stability of the substrate due to the absence of the clamps. V. V. Soman et al. [32] designed a structure that uses weight in its mechanism to apply force and conform the substrate to a bent surface. Hitherto, the kinds of setups discussed are capable of bending the substrate in one direction only, resulting in the application of either compressive or tensile force. M. M. Hamasha et al. [45] used a setup that can bend the substrate in both the direction, adding more versatility. Apart from ROC tests, depending on the application, fatigue tests in the form of twisting and stretching have also been developed. Twisting tests are implemented by rotating one [46]

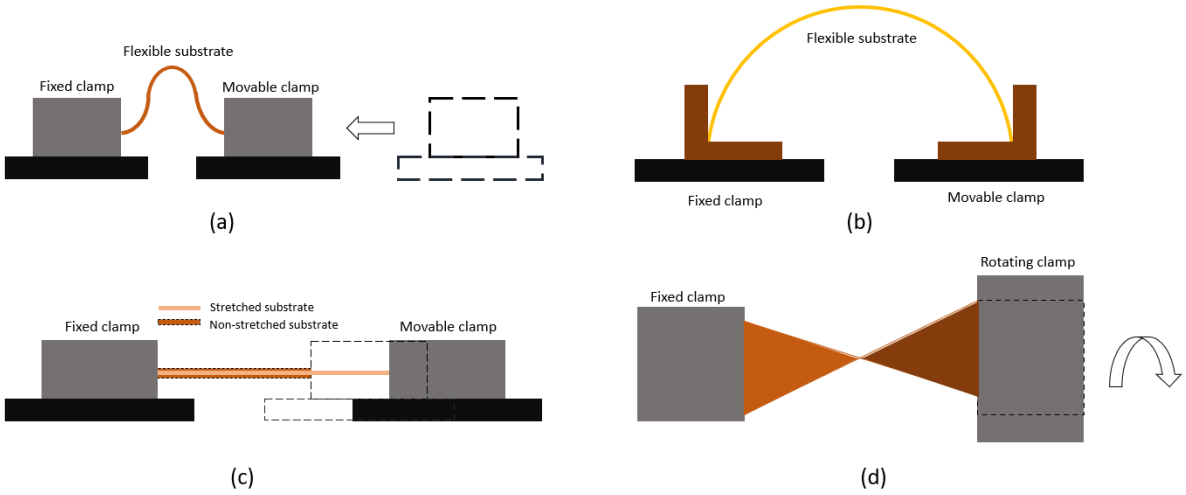


Fig. 3.3 Illustrations of the concept of the reviewed bending test methods for flexible electronic devices: (a) linear bending test setup using clamped ends, (b) linear bending test setup using free ends, (c) stretch test setup, (d) twisting test setup.

or both of the clamps [47] in the opposite direction by using setups similar to the one in Fig. 3.3 (d). On the other hand, stretching tests are performed by moving one [48], as shown in Fig. 3.3 (c) or both the clamps [49] in the opposite direction. C. Kim et al. [50] have designed a complex yet a very versatile universal test apparatus which is capable of performing all kinds of tests discussed above.

3.2 The Design

The design of the bending machine is dictated by the requirement from the application field because each application field has its own specifications. For example, a device to be worn on the wrist has different stress requirement than a device to be worn around chest. The design also depends on the number of different types of tests that a machine is required to perform. In all cases, bending machine designed should not exert undesired stress on any part of the substrate, for example, on the components. For the purpose of this thesis, for investigating the effect of bending on the parasitic components of the FHE prototype, a mechanism is designed with the following objectives in mind:

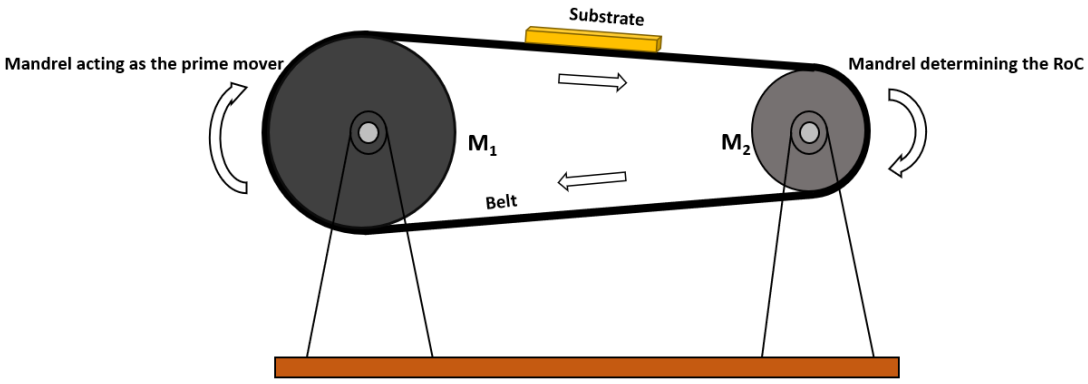


Fig. 3.4 Concept art of the bending setup.

- The machine has to be capable of performing the ROC test, both static and dynamic.
- The design has to be simple enough to be built in-lab.
- The design should minimize undesired stress on any part of the FHE prototype.
- The device should be versatile enough to accommodate more than one prototype to be tested at a time.

With these objectives in mind, a one-directional bending setup is designed to apply tensile force on the prototype. A bi-directional design is not suitable for bending FHE prototype because subjecting it to concave bending will press the components assembled on the lop layer of the substrate against the bent surface of the machine, which is an impractical application scenario in this case. Hence, one-directional bending is deemed to be sufficient.

3.2.1 The Concept and Calculations

The concept of the bending machine is illustrated in Fig. 3.4. The conveyor belt like mechanism consists mainly of two wheels or mandrels, a belt, a motor, and other auxiliary parts to erect the setup. One mandrel, M_1 upon coupling with the motor, serves as the prime mover whereas the other mandrel, M_2 dictates the radius of curvature for bending

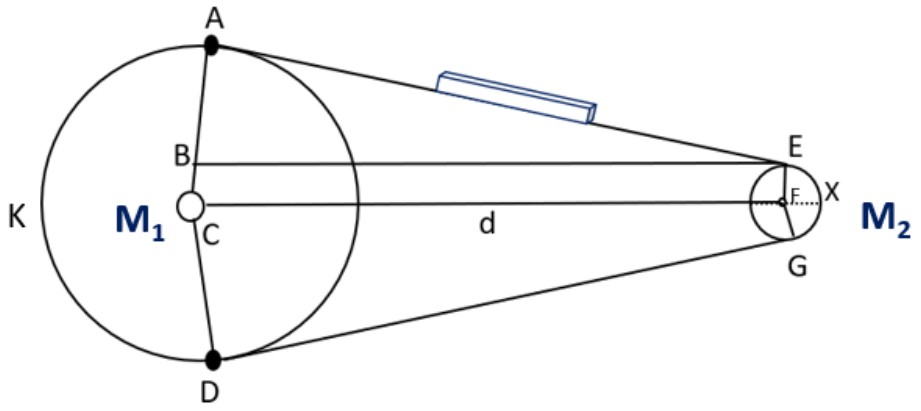


Fig. 3.5 A geometric drawing of the bending machine.

the substrate. Each cycle consists of bending the substrate to a required radius from its flat form by moving it over M_2 and then reinstating it back to that flat contour.The belt is used to place one or more prototypes over the setup. Upon placing the prototype on the belt, it is attached to the belt using adhesive or double-sided tape. The configuration mechanism of M_2 is modular in nature so that it can be replaced basing on the requirement of the radius of curvature to bend the substrate. So, depending on the radius of M_2, the length of the belt has to be readjusted. The calculation is discussed below:

Referring to Fig. 3.5, the length of the belt, L can be written as

$$L = AE + DG + S_1 + S_2 \tag{3.1}$$

where, S_1 and S_2 are the length of arcs AKD and EXG of M_1 and M_2 respectively. So, S_1 and S_2 are needed to be calculated to compute L, which can be done by determining $\angle ACD$ and $\angle EXG$. Here, $\angle ACD = \angle EXG = 2\angle ABE = 2\angle ACF = 2\angle EFX$. Now, $\angle ABE$ can be obtained from the following equation

$$\angle ABE = \arctan(AE/AB) \times \frac{\pi}{180} \tag{3.2}$$

where, $AE = \sqrt{CF^2 - AB^2)}$ and $AB = r_1 - r_2$. Here, r_1, r_2, and CF are the radius of M_1, radius of M_2, and the center-to-center distance between M_1 and M_2 respectively. For a particular setup, r_1, r_2, and CF are user dependent and known variables. Finally, S_1 and

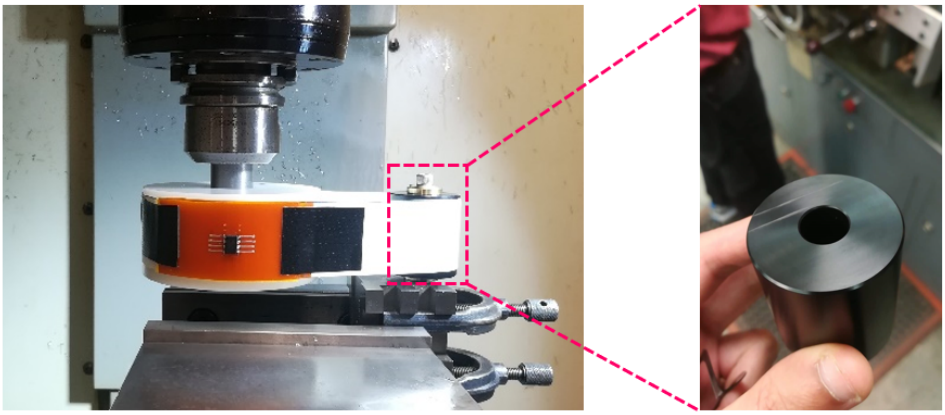


Fig. 3.6 (a) Realized version of the bending machine, (b) A close-up of the mandrel fashioned.

S_2 can be obtained from the following equations

$$S_1 = 2\pi r_1 - r_1\theta \tag{3.3}$$

$$S_2 = r_2\theta \tag{3.4}$$

Thus, after obtaining the values of S_1 and S_2, the length of the belt can be calculated for a particular set of radii of M_1 and M_2 separated by a fixed center-to-center distance, CF.

3.2.2 The Realized Design

The actual working version of the bending machine is shown in Fig. 3.6. At first, the mandrels of required radii are placed at a predetermined center-to-center distance. Then, a belt made up of paper-like material and of calculated length is wrapped around the two mandrels onto which the prototype is attached using a double-sided tape. The material of the belt is chosen to have sufficient grip on the surface of the mandrels which is made up of plastic material. Afterwards, the mandrel on the left in Fig. 3.6 (a) is coupled with the shaft of the motor to work as the prime mover. A close-up view of the modular mandrel dictating the radius of curvature is shown in Fig. 3.6 (b). The height of both of the cylindrical mandrels as well as the width of the belt should be more than the width of the

substrate of the prototype so that it can be rested properly on the belt. The substrate is first attached to the belt on the flat portion. Then, the motor is turned on and as a result, the flexible prototype is subjected to cycles of bending in a controlled setup each time it goes over M_2, i.e., the mandrel dictating the radius of curvature.

3.3 Chapter Summary

This chapter articulates the design of a bending machine capable of performing ROC test on the assembled FHE system in a controlled manner, preceded by a review of the existing machines.

Chapter 4

Extraction of Inherent Parasitic Contact Resistance and Variation Thereof Due to Bending of an FHE Assembly

In this chapter, the post-assembly parasitic contact resistance present in between the individual pins of an IC package and the substrate is extracted and its variation due to bending is recorded by means of a DC measurement-based technique. The one-port measurement technique exploits the Electrostatic Discharge (ESD) protection circuitry in an IC chip to extract the contact resistance by probing at on-board test pads. The accuracy of the extracted parameter is verified with a prototype developed on a rigid FR4 substrate. Then, ultimately, the technique is applied to observe and evaluate the variation in the contact resistances when the post-assembly FHE prototype developed on flexible Kapton Polyimide substrate is subjected to mechanical stress due to bending.

4.1 Measurement Methodology

This section discusses at length the propounded methodology used to extract the parasitic contact resistance. The contact resistance for a particular pin, for the purpose of this chapter, is defined as the resistance between the corresponding IC pin and contact pad on the substrate. The measurement technique exploits the built-in ESD protection circuitry inside the IC chip packages to create a circuit loop involving the contact resistance and the series incremental resistance of the ESD circuit via two IC pins, one of them being the power supply pin, i.e., GND or VDD pin. The measurement technique utilizes *a priori* information about these on-chip ESD protection circuits to isolate the contact resistance.

4.1.1 Modelling On-chip ESD Protection Circuit

Electrostatic discharge is the sudden release of electricity from one charged object to another when the two objects come into contact. On-chip ESD protection circuits are present in the commercial IC packages to protect each input and output of an IC from electrostatic discharge and other excessive voltage conditions [36]. These ESD protection circuits can be modelled as diodes and the ESD diode model of an IC with two I/O pins and power supply pins is illustrated in Fig. 4.1.

To substantiate the ESD diode model, I-V characteristics of the internal signal paths present between the pin pairs of an IC can be evaluated. To do so, 8-pin microcontroller IC ATTINY85 package manufactured by Microchip Technology is chosen. Although the diode paths might be non-identical for different IC packages, the diode model of the ESD protection circuit is also applicable for other commercially available ICs [36] and therefore, any other IC package can be chosen as well. The measured I-V characteristics of the internal signal paths between GND and I/O pins, I/O and VCC pins, and GND and VCC pins of ATTINY85 IC are shown in Fig. 4.2. The shape of the I-V curves clearly substantiates the diode model. The curves are not identical on the account of non-identical ESD diodes and arrangement of the diodes in each signal path.

Now, the measurement technique requires the diode incremental resistance, r_D between

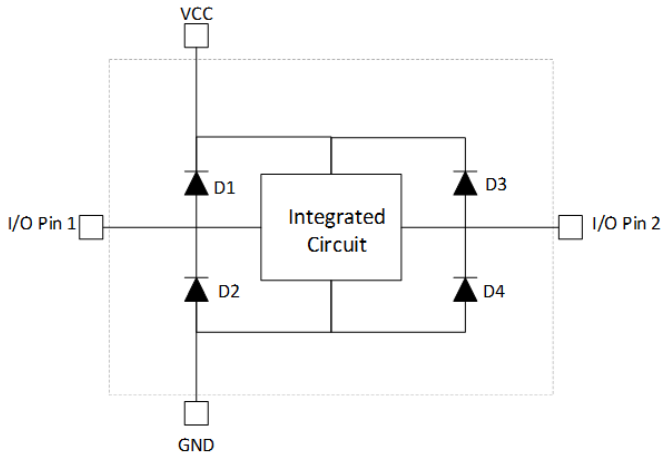


Fig. 4.1 Diode model for ESD protection circuit.

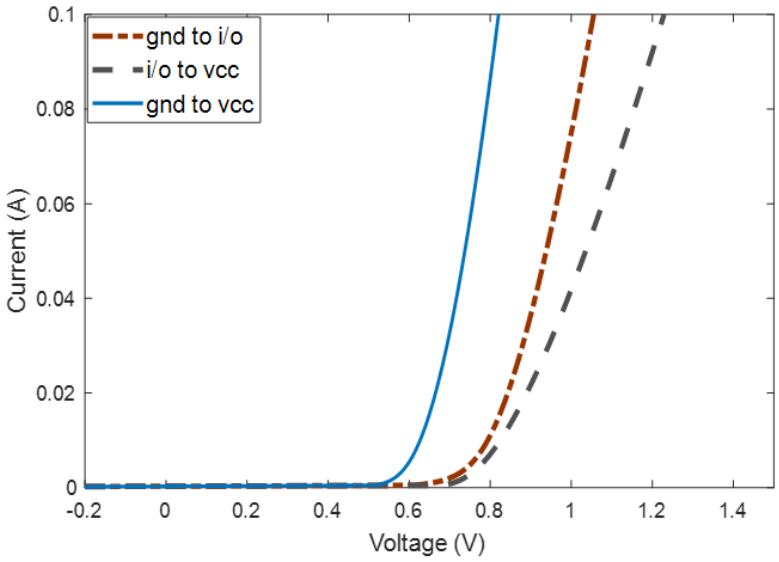


Fig. 4.2 I vs V Plot: (a) from GND pin to I/O pin, (b) I/O pin to VCC pin, (c) GND pin to VCC pin.

the corresponding IC pins. Here, r_D is calculated by measuring a change in voltage, ΔV for a change in bias current, ΔI. The nominal bias current, I is set to 10 mA and the step change ΔI will be set to 50% of that for the results reported in this work. The choice of bias current is elaborated in Section 4.3. The incremental diode resistances measured between the appropriate IC pins incorporate existing IC package resistances between the

Table 4.1 Normal distribution parameters of incremental diode resistances between particular pins for 33 samples of attiny85.

Incremental Diode Resistances	Mean (Ω)	Relative Standard Deviation (%)
$r_{D,pinGND-pin2}$	5.4514	0.5447
$r_{D,pinGND-pin5}$	5.5360	0.3842
$r_{D,pinGND-pin6}$	5.5106	0.6555
$r_{D,pinGND-pin7}$	5.5752	0.4714
$r_{D,pin5-pinVCC}$	5.5662	0.9014
$r_{D,pin6-pinVCC}$	6.9724	0.9483
$r_{D,pinGND-pinVCC}$	4.2042	0.5051

corresponding pins.

Then, to check whether similar diode paths exist between different pin pairs, the diode incremental resistances between different pairs of I/O and power supply pins of the ATTINY85 IC chip are measured. For that, r_D between each I/O and power supply pin pair is measured for 33 samples of ATTINY85 IC chip. The results show that r_D between different pairs of I/O and power supply pins of the ATTINY85 IC chip constitute a distribution with a large relative standard deviation of 16%. Therefore, the diodes' paths between different pairs of I/O and power supply pins are concluded to be non-identical.

In contrast, incremental diode resistances between a particular pair of I/O and power supply pin across different samples of the particular IC model show a normal distribution with small relative standard deviation. This is evident from Table 4.1 which lists the distribution parameters of the incremental diode resistances between particular I/O and power supply pin pairs for 33 samples of an ATTINY85 IC chip. That is why, the diode paths' between the same pairs of I/O and power supply pins are concluded to be identical. The other incremental diode resistances in the chip for different samples of the IC show a similar range of parameters.

4.1.2 Measuring The Contact Resistance of a Single Pin

Figure 4.3 depicts a circuit representation of an IC device with a single input and single output pin, together with VCC and GND pins mounted on a substrate. The figure also

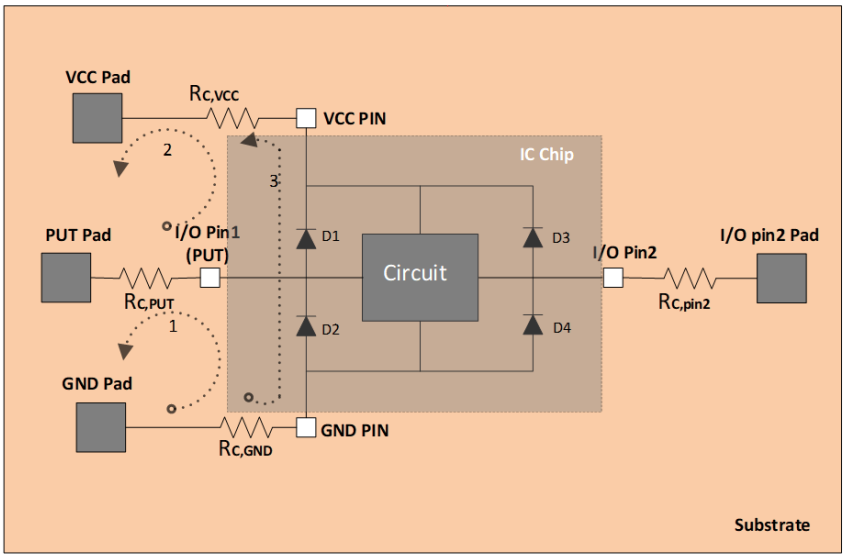


Fig. 4.3 Measurement of contact resistances of PUT after mounting an IC onto a substrate.

shows the contact resistance made between the substrate and IC pins. To identify the contact resistance of a specific I/O pin, let's call this pin the Pin-Under-Test (PUT) as visible on the left-hand side of the schematic. As each pin of the device has a series contact resistance component, it is impossible to identify these resistances with a single measurement. Instead, if the resistance seen between the PUT pad and the VCC pad is measured, then this resistance can be identified as follows

$$R_{padPUT-padVCC} = R_{c,PUT} + R_{c,VCC} + r_{D,1} \tag{4.1}$$

where $R_{c,PUT}$ and $R_{c,VCC}$ are the contact resistance and $r_{D,1}$ represents the incremental resistance of diode D_1. The incremental resistances of each diode can be assumed to be known from separate measurements, as discussed in the previous section.

Likewise, the resistance seen between the PUT and GND pads is

$$R_{padPUT-padGND} = R_{c,PUT} + R_{c,GND} + r_{D,2} \tag{4.2}$$

where, $R_{c,GND}$ and $r_{D,2}$ represents the contact resistance associated with the GND pin and the incremental resistance of D_2, respectively. As there are three unknowns listed in

the above two equations, a third equation is needed to be identified. This is found by recognizing that the resistance between the VCC and GND pads as follows:

$$R_{padGND-padVCC} = R_{c,GND} + R_{c,VCC} + r_{D,eq} \tag{4.3}$$

where,

$$r_{D,eq} = r_{D,1}||r_{D,2} + r_{D,3}||r_{D,4} \tag{4.4}$$

Solving for the three unknown contact resistances results in the following equations.

$$R_{c,PUT} = \frac{1}{2}(R_{padPUT,padGND} + R_{padPUT,padVCC} - R_{padGND,padVCC} - r_{D,1} - r_{D,2} + r_{D,eq}) \tag{4.5}$$

$$R_{c,GND} = \frac{1}{2}(R_{padPUT,padGND} - R_{padPUT,padVCC} + R_{padGND,padVCC} - r_{D,1} + r_{D,2} - r_{D,eq}) \tag{4.6}$$

$$R_{c,VCC} = \frac{1}{2}(-R_{padPUT,padGND} + R_{padPUT,padVCC} + R_{padGND,padVCC} + r_{D,1} - r_{D,2} - r_{D,eq}) \tag{4.7}$$

Combining the direct measurements of the resistances seen external to the IC with the incremental resistances of the diodes, the contact resistance of any pin can be found using the above three equations.

4.2 Experimental Setup

In this section, two experiments are discussed. The first experiment is conducted to evaluate the accuracy and to validate the proposed measurement technique. Then, the second experiment is conducted to detect and track the variation in IC-substrate contact resistance due to repeated bending of the substrate. In both experiments, Voltera V-one PCB printer is used to additively print the conductive traces on the substrate. In the developed prototypes used in these experiments, Silver (Ag) nanoparticle ink manufactured by Voltera, with 65% weight concentration of Ag is used for conductive traces and pads. Moreover, Lead-free solder with 57% Bismuth at a localized heat of $180°C$ is used for soldering the IC pins to the pads on the flexible and rigid substrates.

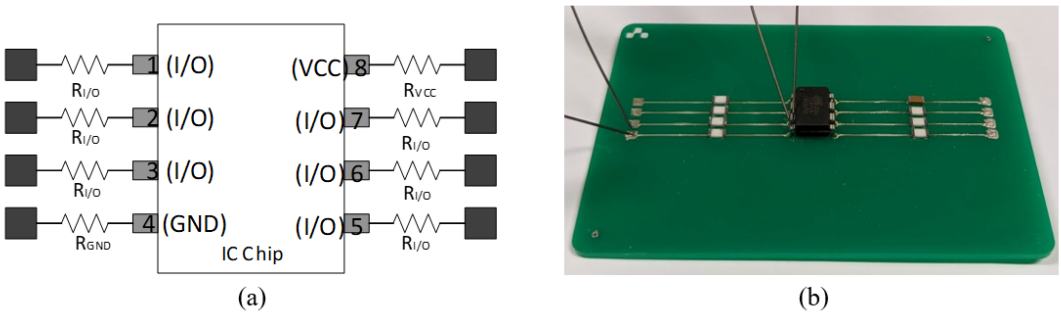


Fig. 4.4 Prototype for validating the measurement of the contact resistance associated with single IC pin: (a)electrical schematic (b) prototype under Kelvin test.

4.2.1 Validating The Measurement Technique

A prototype has been developed by mounting the ATTINY85 IC onto a FR4 PCB substrate with known values of resistances between the IC pins and the test pads. These known surface mount resistances are put here as reference values for validating the measurement technique. Their values are kept on the order of 1 Ω, within a range of 0.5 Ω to 2 Ω, similar to the values of the contact resistances. The measurements are carried out using a Keithley 2450 Source-Measure Meter. Figure 4.4 depicts the electrical schematic of the prototype and a photo of the prototype assembly under Kelvin test. In Fig. 4.4(a) the resistors $R_{I/O}$, R_{GND}, and R_{VCC} are assumed to be unknown resistances. At first, a Kelvin test is performed between the respective IC pins and test pads and $R_{I/O}$, R_{GND}, and R_{VCC} are measured, as shown in Fig. 4.4(b). Then, the proposed technique is employed and the contact resistances are measured using the mean values of diode incremental resistances for the ATTINY85 IC from Table 4.1. While measuring the contact resistance using the proposed technique, the one-port measurement is taken by placing the probes at the designated test pads as shown in Fig.4.5. Finally, the measured values of contact resistances using the proposed technique are compared with the known values of corresponding resistances found using the Kelvin test.

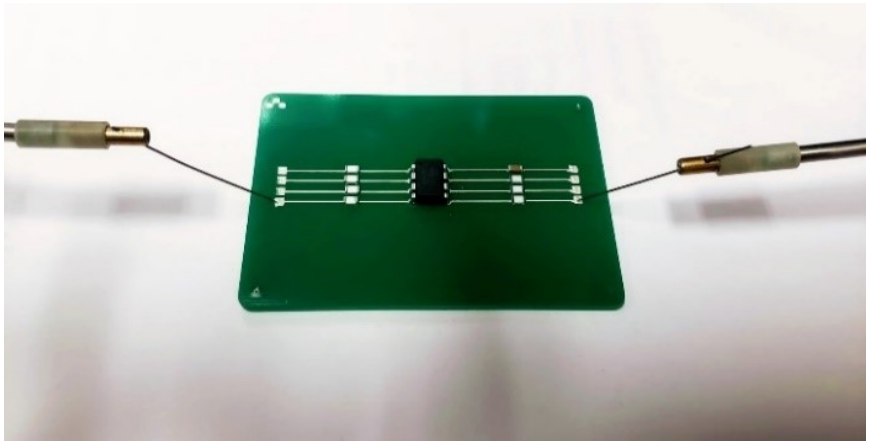


Fig. 4.5 Prototype under one-port measurement setup using the proposed technique.

4.2.2 Determining The Variation of Contact Resistances as a Function of Bending Cycle

For determining the variation of contact resistance as a function of bending cycles, the prototype is fabricated on the Kapton Polyimide substrate of thickness 125 μm as shown in Fig. 4.6. The developed flexible prototype is subjected to multiple cycles of bending in a controlled mechanical setup, as shown in Fig. 4.7. Each cycle consists of bending the substrate at a 1.5 cm radius from its original flat form and then reinstating it back to that flat contour. The radius of bending is controlled by placing appropriate mandrels on the bending machine. Contact resistances are measured at an interval of 200 bending cycles for a total number of 1600 bending cycles. The experiment is conducted at standard room temperature of 25°C.

4.3 Results

The results of the experiments described in the previous section are discussed here.

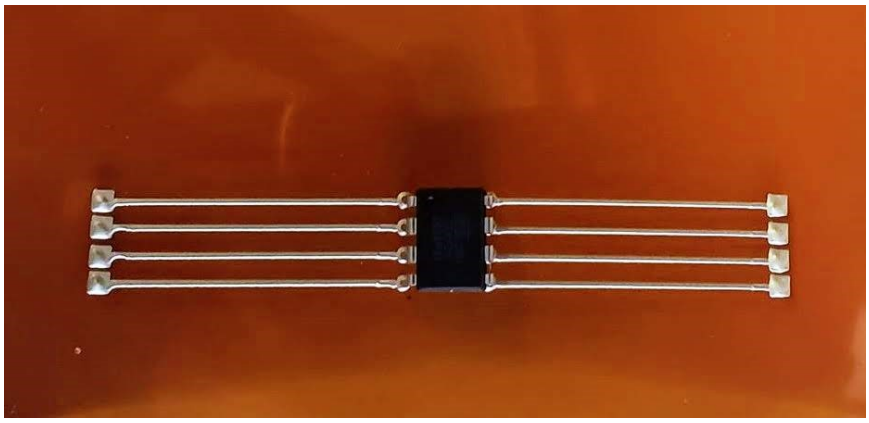


Fig. 4.6 Photo of the prototype on Kapton polyimide.

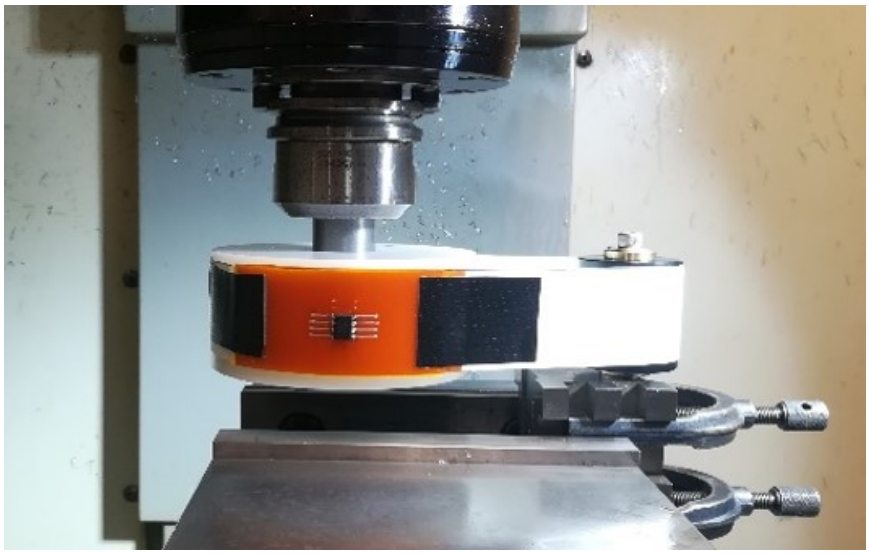


Fig. 4.7 Mechanical setup for bending the prototype.

4.3.1 Extraction of Contact Resistance

Table 4.2 reports the relative error in the measurement of contact resistances using the proposed technique with respect to known values of corresponding resistances found with the Kelvin test. In this table, PUT1, PUT2, PUT3, and PUT4 represents different I/O pins. It is found that the relative error is below 1% for measuring a contact resistance of the order of 1 Ω. Thus, we can infer the proposed measurement technique to be accurate for measuring contact resistance of the order of 1 Ω and higher.

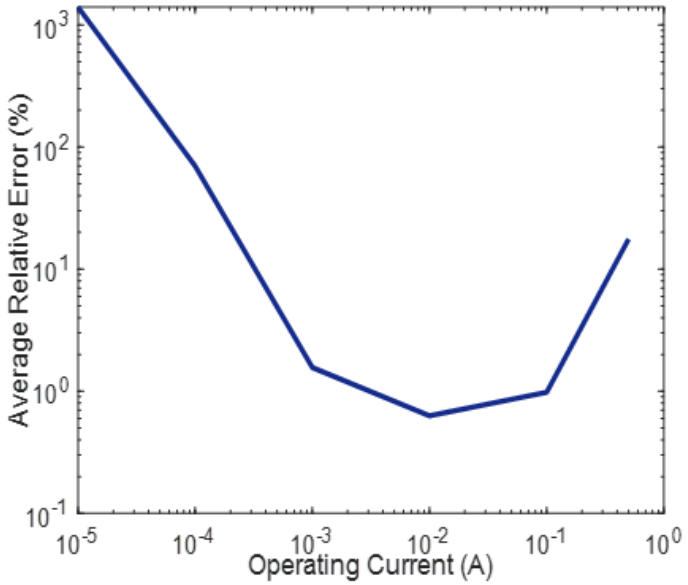


Fig. 4.8 Average relative error (%) vs operating current (A).

However, the relative error varies with respect to the order of operating currents. The proposed technique is employed to measure the contact resistance for different magnitudes of operating current, I assuming the current step change, ΔI will be 50% of this operating current. The average relative error (%) in measurement of contact resistance is plotted against the order of the operating current in Fig. 4.8. It is observed that the average relative error is quite high for very small and very large currents. For very small current, the incremental diode resistance, the resistance from which series contact resistances are extracted, is orders of magnitude larger than the contact resistances. Thus, a small relative

Table 4.2 Relative error in the measurement of contact resistances using the proposed technique.

Contact Resistances	Relative Error (%)
$R_{contact-PUT1}$	0.55%
$R_{contact-PUT2}$	0.99%
$R_{contact-PUT3}$	0.73%
$R_{contact-PUT4}$	0.69%
$R_{contact-GND}$	0.65%
$R_{contact-VCC}$	0.33%

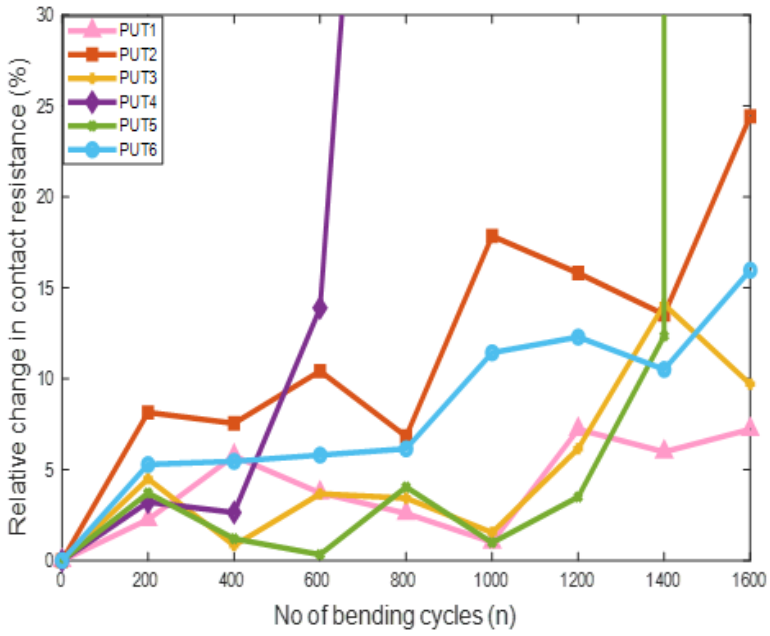


Fig. 4.9 Contact resistance variation with the number of bending cycles.

variability in estimating the incremental diode resistance can cause large relative error in the extracted contact resistances. For very high current, the voltage response to step current showed gradual rise with time within the measurement period, during which multiple readings are taken. This non-stationary effect can potentially cause the extracted contact resistance to deviate away from the actual value resulting higher relative error. That is why, an operating current of the order of 10 mA, where the average relative error is 0.63%, is chosen for the measurements presented in this work.

4.3.2 Variation of Contact Resistance as a Function of Bending Cycle

Figure 4.9 illustrates the relative percentage change in contact resistance as a function of number of bending cycles. The contact resistances prior to bending were of the order of 1 Ω. Due to repeated application of mechanical stress in the form of successive bending, an increasing trend in the contact resistance is evident for all the pins. However, the increasing pattern for the contact resistances associated with different pins are not similar, which can be attributed to inconsistencies in fabrication of hybrid electronics through

additive printing [7], [34] as well as to subtle non-uniformity in distribution of mechanical stress across different contact resistances. During the bending process, contact resistance of two of the pins, PUT 4 and PUT 5 increases abruptly at certain point and loses the electrical continuity. Regardless of that, the proposed technique is used successfully to find the progressive increase of contact resistances towards the ultimate failure of conductivity.

4.4 Chapter Summary

In this chapter, at first, a technique for the extraction of IC pin to flexible board contact resistance exploiting on-chip ESD protection circuit is articulated and substantiated. The method discussed is shown to determine the contact resistance with a relative error of less than 1%. The proposed technique is then employed effectively to observe and track the variation of the contact resistance due to stress induced by bending of a prototype fabricated on Kapton Polyimide substrate. Upon doing so, the results deduce that the application of mechanical stress on the FHE assembly causes a progressive increase of the the parasitic contact resistance which ultimately leads to the failure of conductivity.

Chapter 5

Extraction of The Inherent RLC Parasitics And Variation Thereof Due to Bending of an FHE Assembly

This chapter discusses the extraction of the RLC parasitics and the variation thereof from an FHE assembly by propounding an AC measurement-based technique. This proposed method also exploits on-chip ESD protection circuits, like the method presented in the previous chapter, to extract the RLC parameters of printed conductors bonded to an IC chip by one-port access to on-board test points. Employing AC-based measurement facilitates the extraction of all three parasitic components in comparison to the DC-based measurement deployed to measure only the parasitic contact resistance in the previous chapter. The accuracy of the extracted RLC parameters with the proposed method are verified with a prototype developed on a rigid FR4 substrate. Then, finally, the proposed technique is utilized to track the variation of RLC parasitics for prototypes developed on flexible Kapton Polyimide substrate subjected to different forms of bending.

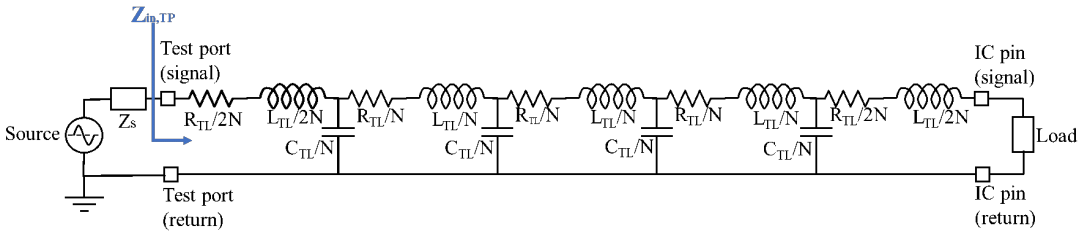


Fig. 5.1 Equivalent RLC Model with N number of T segments for a uniform transmission line on PCB (shown for N=4).

5.1 Transmission Line Modelling

The transmission line extending from the test port to the IC pins on a PCB can be represented by a lumped equivalent circuit model with N number of T segments as depicted in Fig. 5.1 [51]. In the model, total series resistance, R_{TL}, series inductance, L_{TL}, and shunt capacitance, C_{TL} between the test port and the IC pin are distributed among the N segments. As N becomes larger, the lumped equivalent circuit model approximates the distributed behavior of the transmission line over larger bandwidth. In the Fig. 5.1 , Z_s represents the source impedance.

When the load impedance Z_{load} becomes very small, the effect of C_{TL} can be neglected up to a certain bandwidth as long as the impedance due to C_{TL} is orders of magnitude larger than the sum of the impedance due to R_{TL}, L_{TL}, and the load. Hence, for a small Z_{load}, the transmission line from the test port to the IC pins on a PCB can be approximated within a certain bandwidth with R_{TL} and L_{TL} only. We refer to this approximation as a series

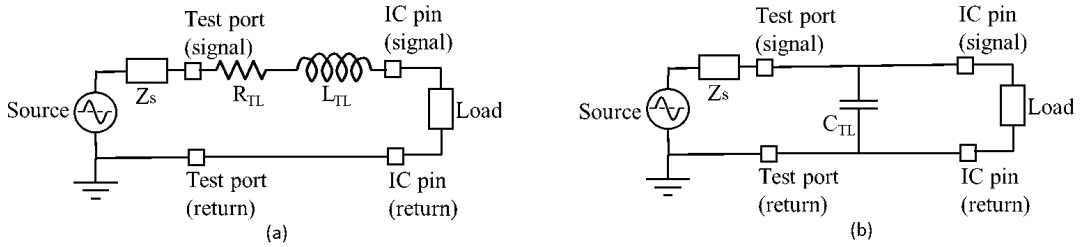


Fig. 5.2 Low frequency lumped equivalent models for transmission line: (a) Series RL model for small Z_{load}, (b) shunt C model for large Z_{load}.

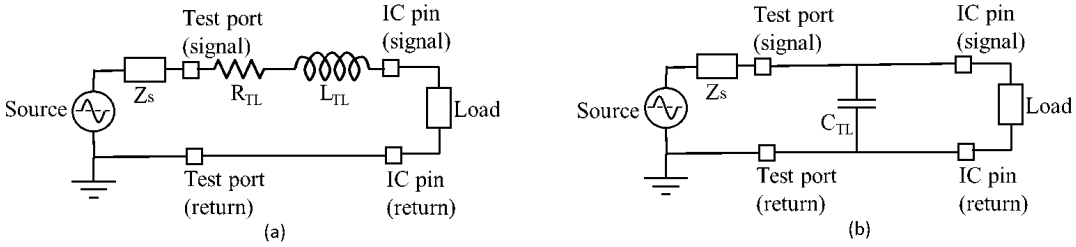


Fig. 5.3 Normalized plot of extracted R_{TL} and L_{TL} as function of frequency from a transmission line terminated with small load impedance.

RL model as depicted in Fig. 5.2(a). Conversely, as Z_{load} becomes very large, the effect of R_{TL} and L_{TL} can be neglected within a certain bandwidth as long as the admittance due to C_{TL} is orders of magnitude larger compared to sum of admittance due to R_{TL}, L_{TL} and, the load. Hence, for a very large Z_{load}, the transmission line from the test port to the IC pins can be approximated within a certain bandwidth with C_{TL} only, which we refer to this as the shunt C model depicted in Fig. 5.2(b).

The bandwidth, up to which series RL and Shunt C models are accurate under appropriate Z_{load}, is dependent on L_{TL} and C_{TL} of the transmission line. To demonstrate this bandwidth dependency for the series RL model, the input impedance $Z_{in,TP}$ of the RLC transmission line model of Fig. 5.1 is simulated as a function of frequency using the Keysight Advance Design System (ADS) platform for varying the orders of L_{TL} and C_{TL}. The characteristic impedance is held constant at 50 Ω and parameters $R_{TL} = 1\ \Omega$, $Z_{load} = 1\ \Omega$ and $N = 100$. From the simulation, R_{TL} is extracted as the real part of $Z_{in,TP}$ minus Z_{load}. Also, L_{TL} is extracted as the slope of the imaginary part of $Z_{in,TP}$ with respect to frequency. The extracted R_{TL} and L_{TL} are normalized by the corresponding known values inserted in the RLC model and plotted against frequency as shown in Fig. 5.3. It is observed that the extracted R_{TL} and L_{TL} remains constant and equal to their known values well below the resonant frequency. In other words, the series RL model is valid for at least one order of magnitude below the fundamental resonance, f_r [52], given by the following expression

$$f_r = \frac{1}{4\sqrt{L_{TL}C_{TL}}} = \frac{1}{4T_D} \tag{5.1}$$

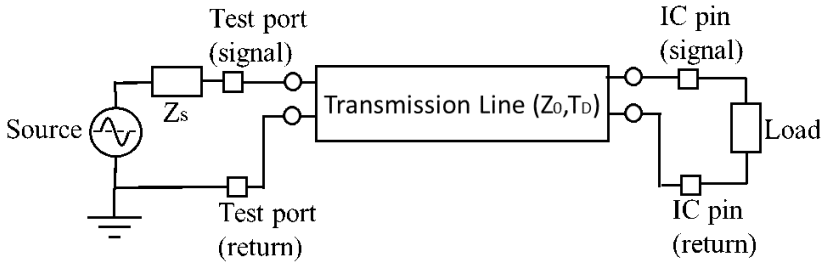


Fig. 5.4 Transmission line lossless model.

Here, T_D is the end-to-end time delay for the wave propagation in the transmission line. The parameter T_D can be expressed in terms of line length, l, velocity factor, v_f, and velocity of light, c as follows:

$$T_D = \frac{l}{v_f c} \tag{5.2}$$

Isolating the lumped equivalent parameters of a transmission line is practically challenging at high frequency, due to distributed behavior of the transmission line [51]. One way to describe a transmission line at high frequencies is by using the two-port lossless transmission line model depicted in Fig. 5.4. This model makes use of the characteristic impedance, Z_0 and end-to-end time delay parameter, T_D. Considering the lossless approximation ($R_{TL} << j\omega L_{TL}$) and ($G_{TL} << j\omega C_{TL}$) high frequency, the series incremental inductance L_{TL} for a uniform transmission line [53] can be described in terms of Z_0 and T_D as

$$L_{TL} = Z_0 \cdot T_D \tag{5.3}$$

Also, under the lossless approximation, C_{TL} for a uniform transmission can be expressed in terms of Z_0 and T_D as

$$C_{TL} = \frac{Z_0}{T_D} \tag{5.4}$$

This latter model provides a second method to extract the reactive elements of the transmission line. These will be used to compare the corresponding elements extracted by the series-RL and shunt-C models. In principle, they should be the same.

5.2 Measurement Methodology

This section discusses the measurement methodology employed to extract the RLC parasitics of a transmission line bonded to an IC and isolate the parasitic resistance associated with individual printed conductors bonded to a single IC pin. The method presented in this work utilizes the measured data from the on-chip ESD protection circuit before and after bonding the IC chip to the flexible substrate.The presence of ESD protection circuit between I/O and power supply pins as well as its diode model for an ATTINY85 IC have already been delineated in the previous chapter.

5.2.1 Modelling On-chip ESD Protection Circuit

The small-signal equivalent circuit for an ESD diode is depicted in Fig. 5.5 (a). In the figure, r_D represents diode incremental resistance given by

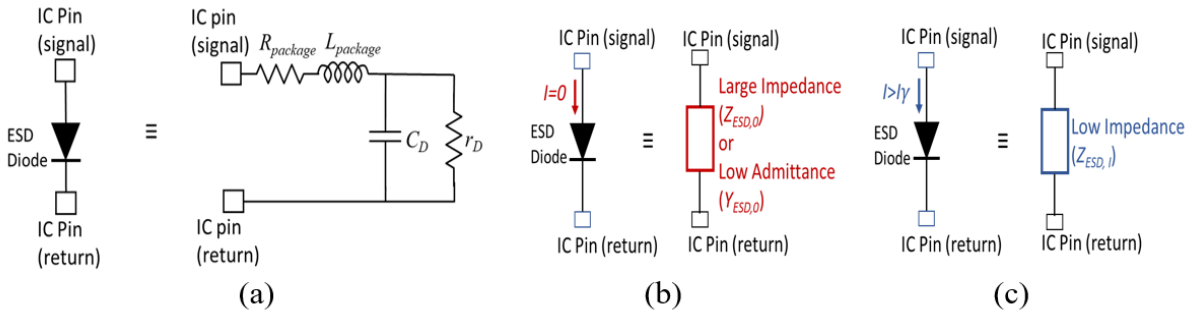


Fig. 5.5 Small signal representation of an ESD :(a) Equivalent circuit (b) Reverse Biased model c) forward biased model.

$$r_D = \frac{\eta V_T}{I} \tag{5.5}$$

where, η is diode ideality factor, V_T is thermal voltage and I is diode forward current. Also, in Fig. 5.5(a) C_D represents the diode capacitance given by

$$C_D = \frac{\tau_T I}{\eta V_T} + C_j \tag{5.6}$$

where τ_T is diode transit time. C_j is junction capacitance, which can be considered as negligible in a forward biased diode.

When the ESD diode is reverse biased at $I = 0$, the diode presents a large impedance or equivalently a small admittance as shown in Fig. 5.5 (b). Conversely, when the ESD diode is forward biased at $I > I_\gamma$, the diode presents a small impedance as shown in Fig. 5.5(c). In this work, I_γ is defined as the current above which r_D decreases to the order of 1 Ω.

The measurement technique requires prior knowledge of the impedance of the ESD diode, $Z_{ESD,I}$ at a chosen frequency, ω under a chosen forward bias current, $I > I_\gamma$. Also, prior knowledge of the admittance of the ESD diode, $Y_{ESD,0}$ at the same frequency under $I = 0$ is required. In the case of the Attiny85 IC made by Microchip Technology, it was observed experimentally that the impedance and admittance of different ESD diodes, present between different I/O and power supply pin pairs, across the same IC varies by more than 20%. In addition, the impedance and admittance of the same ESD diode, for a particular pin pair, varies very little (less than 1%) across 33 different samples of the same ICs. Hence, the $Z_{ESD,I}$ and $Y_{ESD,0}$ of a particular ESD diode in different samples of a given IC chip are considered to be same.

5.2.2 Extracting RLC Parameters of a Transmission Line Bonded to an IC Chip

In this subsection, we will utilize the prior knowledge of the impedance and admittance parameters of an ESD diode in a given IC chip to extract the RLC parameters of a pair

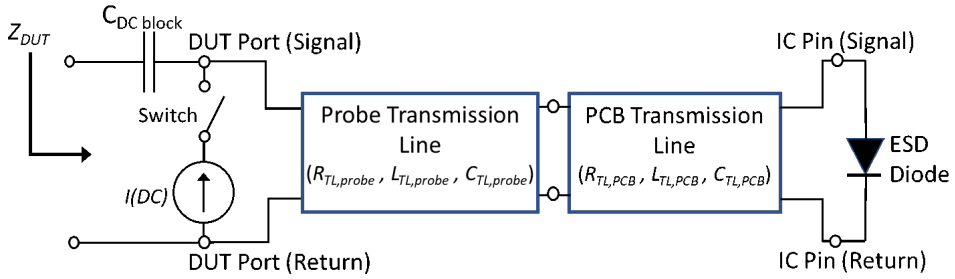


Fig. 5.6 Measurement Setup for extracting the RLC parameters of a PCB transmission Line bonded to a commercial IC chip.

of conductors acting as a transmission line bonded to the IC chip. Fig. 5.6 shows the measurement setup for extraction of the RLC parameters of a PCB transmission line bonded to an ESD diode in a commercial IC chip. The proposed method requires identifying the input impedance Z_{DUT} of the DUT at a particular frequency under a specific DC bias condition of the ESD diode. The DC bias point of the ESD diode is established with a current source connected to DUT through a switch. The rationale behind using a current instead of a voltage source is to force the ESD diode into desired DC bias point regardless of the unknown parasitic resistance in series with the source and ESD diode. The capacitor C_{DC} block prevents any DC current from going into the impedance measuring instrument, while acting as a short circuit to the AC signals above a certain frequency.

From the discussions in the previous section, a transmission line terminated with small load impedance can be approximated with series RL model and for a large load impedance the transmission line can be approximated with shunt C model, up to a certain bandwidth. In the proposed measurement, small and large load impedances for the PCB transmission line are achieved by forward or reverse biasing the ESD diode as illustrated by Fig. 5.7(a)

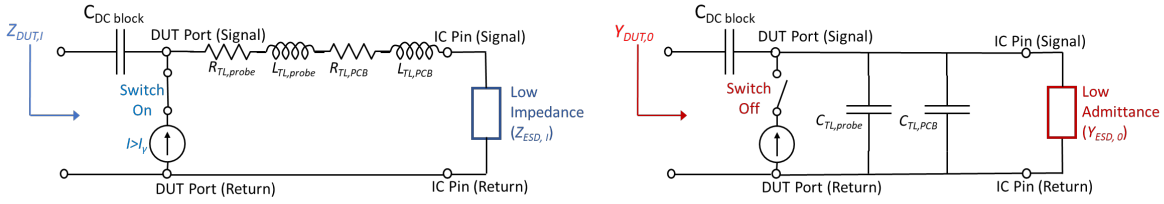


Fig. 5.7 The equivalent circuit of DUT for: (a) Forward biased ESD diode (b) Reverse biased ESD diode.

and (b) respectively.

From Fig. 5.7(a), the resistance of the PCB transmission line, $R_{TL,PCB}$ can be found as follows:

$$R_{TL,PCB} = Real(Z_{DUT,I}) - Real(Z_{ESD,I} - R_{TL,probe}) \tag{5.7}$$

Also, from Fig. 5.7(a), the inductance of the PCB transmission line, $L_{TL,PCB}$ can be found as

$$L_{TL,PCB} = \frac{1}{\omega}[Imag(Z_{DUT,I}) - Imag(Z_{ESD,I})] - L_{TL,probe} \tag{5.8}$$

Here, the real and imaginary parts of $Z_{DUT,I}$ is directly measured at a frequency, ω with some chosen bias current, I. The real and imaginary parts of $Z_{ESD,I}$ are found through a separate measurement of the ESD diode at the same ω and bias current level, I. Also, the probe parasitics $R_{TL,probe}$ and $L_{TL,probe}$ are known from a separate measurement.

From Fig.5.7(b), the capacitance of the PCB transmission line, $C_{TL,PCB}$ can be found using

$$C_{TL,PCB} = \frac{1}{\omega}[Imag(Y_{DUT,I}) - Imag(Y_{ESD,I})] - C_{TL,probe} \tag{5.9}$$

Here, the imaginary part of $Y_{DUT,0} = (1/Z_{DUT,0})$ is directly measured at frequency ω and the imaginary part of $Y_{ESD,0}$ is known from a separate measurement of the ESD diode at the same ω. Additionally, the probe capacitance $C_{TL,probe}$ is also known through separate measurement.

5.2.3 Isolating The Parasitic Resistance of an Individual Printed Conductor Bonded to an IC pin

This subsection delineates the decomposition of extracted $R_{TL,PCB}$ from the PCB transmission line into the constituent parasitic resistances of two printed conductors forming

the transmission line. That is, the parasitic resistance associated with individual printed conductors bonded to a single IC pin at the post-assembly level is isolated here. Each constituent resistance incorporates both the parasitic trace and contact resistance. Taking the measurement from the vicinity of the solder pad will allow to look at the contact resistance only, if necessary.

The circuit representation of an IC device with two I/O and power supply pins assembled on a substrate is illustrated in Fig. 4.3. To isolate $R_{p,PUT}$ from the power supply parasitic resistances $R_{p,GND}$ and $R_{p,VCC}$, one needs to find the transmission line resistances $R_{TL1,PCB}$, $R_{TL2,PCB}$ and $R_{TL3,PCB}$ from the transmission lines 1, 2 and 3, respectively. The extracted transmission line resistances can be expressed in matrix form:

$$\begin{bmatrix} R_{TL1,PCB} \\ R_{TL2,PCB} \\ R_{TL3,PCB} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} R_{p,PUT} \\ R_{p,GND} \\ R_{p,VCC} \end{bmatrix} \tag{5.10}$$

or, more succinctly:

$$R_{TL,PCB} = C \cdot R_p \tag{5.11}$$

From the measured transmission line resistance vector $R_{TL,PCB}$, the unknown parasitic resistance associated with the given pins, designated by vector R_P, can be found by inverting the matrix equation as follows:

$$R_p = C^{-1} \cdot R_{TL,PCB} \tag{5.12}$$

Thus, the parasitic resistance associated with any IC pin can be isolated with the presented method.

5.3 Experimental Setup

This section describes three experiments. The first experiment is conducted to validate the extraction of RLC parameters of a PCB transmission line bonded to an IC chip using the

proposed measurement technique. The second experiment is for validating the technique to isolate parasitic resistance associated with individual printed conductor bonded to an IC pin. Finally, to show the usefulness of the proposed technique in tracking the variation of RLC parasitics on an FHE assembly subjected to flexing, the third experiment is carried out. All the experiments are conducted under standard temperature and ambient conditions in a controlled lab environment.

5.3.1 Experimental Setup to Validate Extracted RLC Parameters of a Transmission Line

To validate the method of extracting the parasitic inductance and capacitance from a uniform PCB transmission line on an FR4 substrate, time-domain reflectometry (TDR) is employed to determine its characteristic impedance $Z_{0,PCB}$ and time delay $T_{D,PCB}$. From the values of $Z_{0,PCB}$ and $T_{D,PCB}$, the $L_{TL,PCB}$ and $C_{TL,PCB}$ are found using Eqns. (5.3) and (5.4). $R_{TL,PCB}$ is found by conducting Kelvin test separately on the two constituent printed conductors. Figure 5.8 shows the setup for the TDR measurement. In the setup, a voltage step signal from 0 to -250 mV with a rise time of approximately 32 ps is applied using a Picotest J2151A signal generator. The sourced signal is transmitted by a Picotest P2100A 50 Ω transmission line probe to the PCB transmission line terminated with an open-circuit. The voltage waveform V_m at the input port of the probe is monitored with an Agilent DSA80000B oscilloscope.

Next, the proposed measurement method is employed to extract $L_{TL,PCB}$, $C_{TL,PCB}$

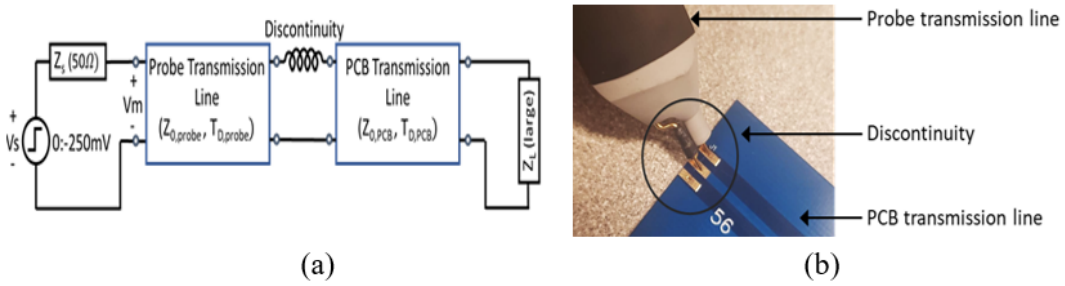


Fig. 5.8 (a) Setup for TDR measurement, b) Discontinuity at the interface.

and $R_{TL,PCB}$ of the same PCB transmission line. The measurement setup of Fig. 5.6 is implemented with a one-port of the PCB transmission line bonded to an I/O pin (pin 2) and Gnd pin (pin 4) of the ATTINY85 IC chip. The DC current source in the setup is established with the Keithley 2450 Source Measure Meter. For blocking the DC current from entering the impedance measuring instrument, the Picotest P2130A 500 Hz - 8 GHz DC blocker is used. Using the proposed measurement method, $L_{TL,PCB}$, $C_{TL,PCB}$ and $R_{TL,PCB}$ are found over a frequency range from 100 kHz to 10 MHz. Measurements over a bandwidth of 100 kHz to 1 MHz are taken with Keysight E4980A LCR Meter and measurements from 1 MHz to 10 MHz are taken with Keysight E4982A LCR meter. Upon ensuring the measured parameters at 1 MHz with the two LCR meters are in agreement, the parameters measured with E4980A meter at all the frequencies are scaled such that its measured parameters at 1 MHz are exactly the same as those from the E4982A meter. The extracted $L_{TL,PCB}$ and $C_{TL,PCB}$ with the proposed technique are compared against those found with TDR measurement and the extracted $R_{TL,PCB}$ is compared against that found from the Kelvin test.

5.3.2 Experimental Setup to Validate The Isolation of Parasitic Resistance of an Individual Printed Conductor Bonded to a Single IC Pin

For validating the isolation of resistance, a prototype similar to the one discussed in 4.2.1 is developed as illustrated in Fig.4.4. Here, The resistances introduced between IC pins and test pads range from 0.5 Ω to 2 Ω. Their exact values are found by performing a 4-wire Kelvin test on the prototype at 100 kHz as shown in Fig. 4.5. The chosen IC package for this purpose possess leads spacious enough for probing as required by a Kelvin test. The proposed measurement is employed to isolate R associated with each pin at 100 kHz using Keysight E4980A LCR Meter and the extracted values are compared against the known values from the Kelvin test, measured as illustrated in Fig. 4.4(b), to ascertain the validity and quantify the accuracy of the proposed method.

5.3.3 Experimental Setup to Track Variation of RLC Parasitics Due to Bending

To track the variation of the RLC parasitics due to flexing, two separate bending experiments are conducted using separate prototypes and experimental setups. The first experiment is implemented to track the variation of parasitic R due to stress introduced by repeated bending. Whereas, the second experiment is conducted to track the variation of parasitic L and C due to change in dielectric separation between the conductive traces. All the parasitics are tracked at 1 MHz frequency with the Keysight E4980A LCR Meter.

For the first experiment, the prototype is fabricated by following the recipe discussed in Section 3.2. Moreover, a similar mechanical setup as discussed in Section 3.2.1 is used to exert mechanical force in form of controlled bending, as illustrated in Fig. 4.7. There, the the prototype is attached to the mandrel of the bending machine in such a way that the bending exerts mechanical force perpendicular to the printed conductors and maximizes the effect of bending on them. In each cycle, the substrate is bend up to a radius of 1.5 cm and then reinstated back to its flat contour. Parasitic R is measured at an interval of 200 bending cycles for a total of 1600 bending cycles.

For the second experiment, another prototype is fabricated on a Kapton Polyimide substrate of 100 μm thickness. Here, 1 oz finished copper (Cu) is used to print the conductive traces and the pads with a redesigned layout pattern of the traces. These modifications have been made to avoid causing catastrophic damage to the traces while changing the dielectric separation in between them. A custom-made bending setup with a stationary and a moving arm is used to apply the necessary stress to change the dielectric separation. Here, the layout of the traces and the subsequent attachment of the prototype on the bending setup are designed to exert the mechanical force lateral to the printed traces. Due to that, the force can be used alter the dielectric separation while minimizing damage caused to the printed traces. After attaching the prototype with the machine as illustrated in Fig. 5.9 (a), the moving arm is brought closer to the static arm to reduce the dielectric separation. As a result, the substrate bends along an axis that lies at the middle of the dielectric separation which results in the formation of a curvature. A circle can be fit to the curvature and the diameter, d, of that circle is used as a measure of dielectric separation

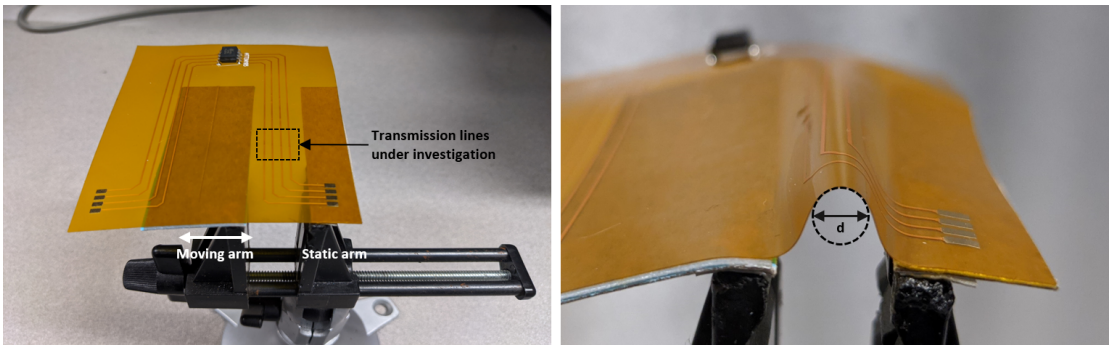


Fig. 5.9 Experiment to track the parasitic LC variation: (a) Prototype lying flat on the bending machine, (b) Bent prototype.

under stress as shown in Fig. 5.9(b). The prototype is bent at diameters of 160 mil, 130 mil, and 100 mil and the corresponding L and C are measured.

5.4 Results

The results of the three experiments described in the previous section are discussed here in successive order.

5.4.1 Validity of Extracted RLC Parameters of a Transmission Line

From the TDR measurement, the recorded waveforms for sourced voltage, $V_s(t)$ and DUT voltage, $V_m(t)$ are shown in the same plot in the Fig. 5.10. The part of the waveform $V_m(t)$ that is located between the interface discontinuity and open circuit discontinuity is the resultant waveform across the PCB transmission line, $V_{m,PCB}(t)$. The characteristic impedance profile of the PCB, $Z_{0,PCB}(t)$ is computed from the following

$$Z_{0,PCB}(t) = \frac{V_{m,PCB}(t)}{V_s(t) - V_{m,PCB}(t)} \cdot Z_s \tag{5.13}$$

Here the source impedance $Z_s = 50\ \Omega$. The characteristic impedance of the PCB transmission line, $Z_{0,PCB}$ is determined as the mean of the PCB impedance profile, $\overline{Z_{0,PCB}(t)}$, as

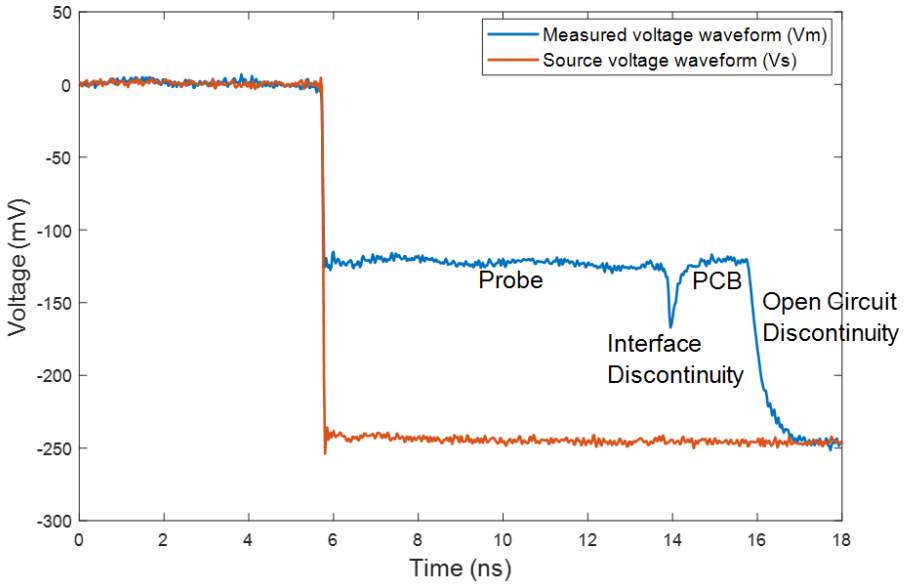


Fig. 5.10 Voltage waveform recorded from TDR measurement.

reflected waveform includes some noise. The bar over $Z_{0,PCB}$ represents the sample mean of the distribution. The time delay of the PCB transmission line, $T_{D,PCB}$ is found from

$$T_{D,PCB} = (T_{far} - T_{near})/2 \tag{5.14}$$

where T_{far} represents the time instance at the 50% of the open circuit discontinuity at the far end of the PCB transmission line and T_{near} represents the time instance at peak of the interface discontinuity at the near end of the PCB transmission line. Table 5.1 lists the computed values of $Z_{0,PCB}$ and $T_{D,PCB}$ with the corresponding uncertainty. The uncertainty in $Z_{0,PCB}$ is estimated from the 95% confidence interval of the computed mean, $\overline{Z_{0,PCB}(t)}$. Also, the uncertainty of $T_{D,PCB}$ is estimated from the rise/fall time at the discontinuities. From the determined $Z_{0,PCB}$ and $T_{D,PCB}$, the $L_{TL,PCB}$ and $C_{TL,PCB}$ are found using Eqns. (5.3) and (5.4) and also appears in Table 5.1. The lumped equivalent resistance $R_{TL,PCB}$ for the PCB transmission line is known to be 304 $m\Omega$ at 1 MHz from separate measurements of the two constituent printed conductors using the 4-wire Kelvin test.

Table 5.1 Computed transmission line parameters from TDR measurement.

	$Z_{0,PCB}(\Omega)$	$T_{D,PCB}(ns)$	$L_{TL,PCB}(nH)$	$C_{TL,PCB}(pF)$
Value	49.858	1.075	53.597	21.561
Uncertainty	±0.412	±0.035	±2.174	±0.53

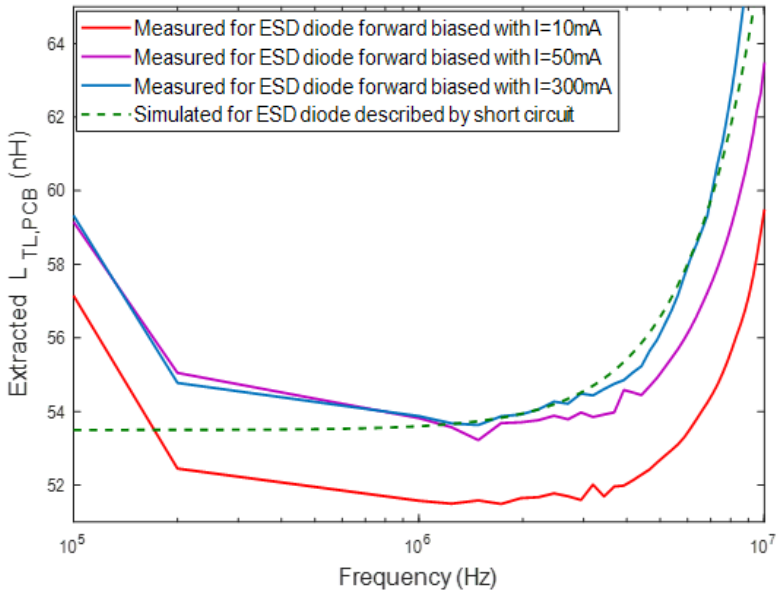


Fig. 5.11 Extracted $L_{TL,PCB}$ with the proposed measurement method.

The extracted $L_{TL,PCB}$, $C_{TL,PCB}$ and $R_{TL,PCB}$ employing the proposed measurement method in the experiment are shown in Fig. 17, 18 and 19 respectively. Also seen in each figure is the extracted values of the corresponding parameters found with the ADS software platform. The transmission line simulated in ADS is described by the model shown in Fig. 5.1 with N=100. The ESD diode is described by a short and open circuit under forward and reverse biased conditions, respectively. The simulated model is comprised of both the PCB and probe transmission lines. The RLC parameters used in describing transmission lines in ADS are found from TDR and Kelvin test of the practical transmission lines.

In the Fig. 5.11, the values of $L_{TL,PCB}$ extracted with the proposed technique agrees with those from TDR measurement within a certain bandwidth of approximately 200 kHz to 4 MHz. The high frequency error in the extracted $L_{TL,PCB}$ is due to series-RL ap-

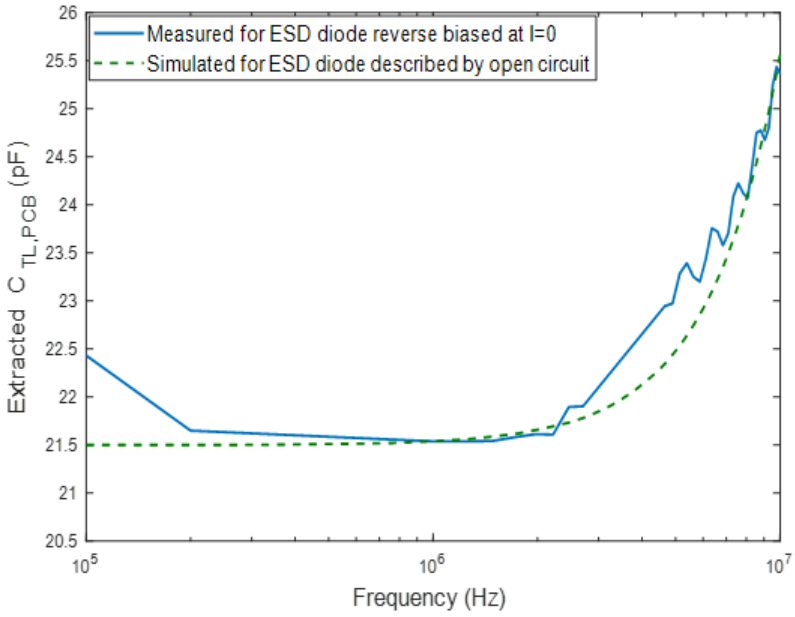


Fig. 5.12 Extracted $C_{TL,PCB}$ with the proposed measurement method.

proximation becoming invalid as the frequency approaches closer towards the fundamental resonance, f_r of the entire transmission line. Here, the f_r of the entire transmission line is found as 46.7 MHz using Eqns. (3.1) and (3.2) from the known lengths and velocity factors of the PCB and probe transmission lines. Implementing the extraction well below (at least one order of magnitude) 46.7 MHz provides reasonable accuracy over the measurement as observed in Fig. 5.11. Also, at the low end of the frequency plot of $L_{TL,PCB}$ it is masked by the instrument phase noise. Within a bandwidth of approximately 200 kHz to 4 MHz the accuracy of the measurement of $L_{TL,PCB}$ seems to improve with increasing ESD diode forward bias current, as shown in Fig. 5.11. This is because the increase in forward bias current makes the series RL parameters of the transmission line more detectable to the impedance measuring instrument by lowering the magnitude of the load impedance presented by the ESD diode. With biasing current above 50 mA, the accuracy enhancement in measuring $L_{TL,PCB}$ saturates as the impedance of the ESD diode saturates.

In the Fig. 5.12, the values of $C_{TL,PCB}$ extracted with the proposed technique agrees with those from TDR measurement within the same bandwidth as stated above, for much the same reasons as for $L_{TL,PCB}$; phase noise and transmission line resonance.

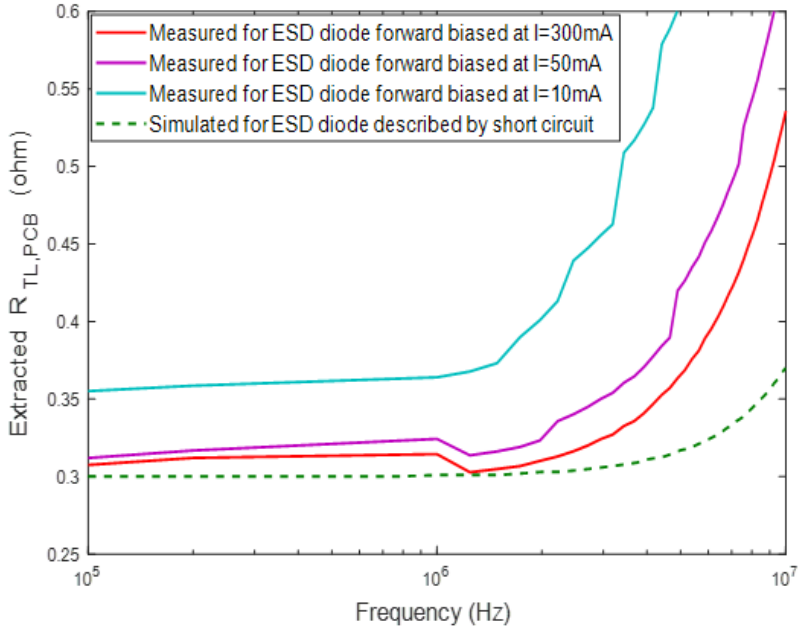


Fig. 5.13 Extracted $R_{TL,PCB}$ with the proposed measurement method.

In the Fig. 5.13, the extracted $R_{TL,PCB}$ with the proposed technique agrees with that measured by Kelvin test up to an upper frequency of approximately 2 MHz. The error at higher frequencies than 2 MHz is partly due to the series RL approximation becoming invalid as the frequency approaches towards the fundamental resonance of the entire transmission line. Also, there is discrepancy of the extracted $R_{TL,PCB}$ at high frequency between the practical measurement and simulation, which is due to modelling differences, such as skin effect. The accuracy of the measured $R_{TL,PCB}$ enhances with the increase of ESD diode forward bias current due to the same reason as explained for extracted $L_{TL,PCB}$. Also, the accuracy enhancement in measuring $R_{TL,PCB}$ saturates at around 50 mA, which is similar to the observation made from the plot of the measured $L_{TL,PCB}$.

For the extracted $L_{TL,PCB}$, $C_{TL,PCB}$ and $R_{TL,PCB}$ the measurement bandwidth is bounded by the f_r of the entire transmission line (comprised of both probe and PCB). Certainly, this measurement bandwidth is expandable by minimizing the propagation delay due to the probe transmission line. This will shift f_r of the entire transmission line to a higher frequency, thereby providing a higher bandwidth for accurate measurement.

Table 5.2 Summary of extracted RLC parameters with proposed method with respect to other methods.

Parameters	TDR	Kelvin Test	Proposed Method	Relative Error (%)
$L_{TL,PCB}$	53.59 nH	-	53.88 nH	0.5
$C_{TL,PCB}$	21.54 pF	-	21.54 pF	0.1
$R_{TL,PCB}$	-	304 $m\Omega$	323 $m\Omega$	6.3

Table 5.2 summarizes the extracted RLC parameters of the PCB transmission line with proposed measurement at 1 MHz in contrast to the corresponding parameters measured with TDR and Kelvin test. Here, the extracted series RL parameters with proposed measurement are reported for the ESD diode forward bias current of 50 mA. From this table, it is observed that the extracted parameters with the proposed method is consistent with those found with either the TDR or Kelvin measurement methods.

5.4.2 Validity of The Isolated Parasitic Resistance of an Individual Printed Conductor Bonded to a Single IC Pin

Table 5.3 compares parasitic resistances associated with four of the IC pins extracted with the proposed method (for ESD diode forward biased with $I = 50\ mA$) at 1 MHz to their corresponding known values from Kelvin test at the same frequency. The relative errors in the measured parasitic resistances for all the pins are within 5% under the chosen DC operating current.

Table 5.3 Comparison of the resistance of individual printed conductors extracted by using proposed method and Kelvin test.

Measured resistance	Kelvin test (Ω)	Proposed method (Ω)	Relative error (%)
$R_{p,GND}$	2.015	2.037	1.1
$R_{p,I/O1}$	1.006	1.024	1.8
$R_{p,VCC}$	0.675	0.692	2.5
$R_{p,I/O2}$	0.507	0.525	3.6

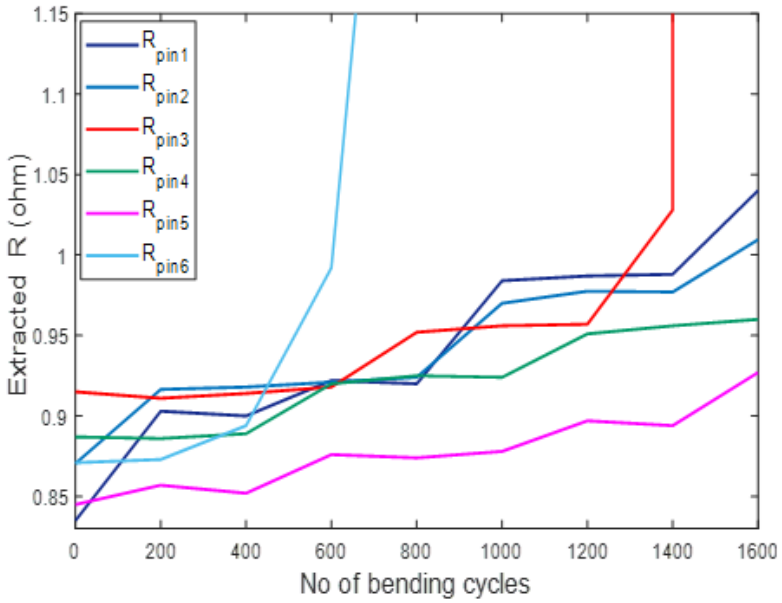


Fig. 5.14 Variation of extracted contact parasitic resistance with the number of bending cycles.

5.4.3 Variation of RLC Parasitics Due to Bending

Figure 5.14 shows the extracted R associated with six different IC pins as a function of the number of bending cycles. In the figure, all the parasitic R follow an increasing trend with respect to the number of bending cycles. The increase in R is caused by the accumulation of stress due to repeated bending. The dissimilarity in the increasing pattern for the different parasitic resistance is mainly due to the non-uniformity in the fabrication using additive printing. The resistance associated with two of the pins (pin 3 and pin 6) increase drastically after 500 bends in one case, and 1200 in another. Here, the signal path is lost. Thus, the change in trace resistance due to repeated bending can be catastrophic at some point.

Figures 5.15 and 5.16 shows the extracted inductance and capacitance for two uniform transmission lines with respect to the bending diameter of curvature formed by the substrate. The two transmission lines are designated by TL1 and TL2. The dielectric separation between the signal and return paths of TL1 and TL2 are 200 mil and 300 mil,

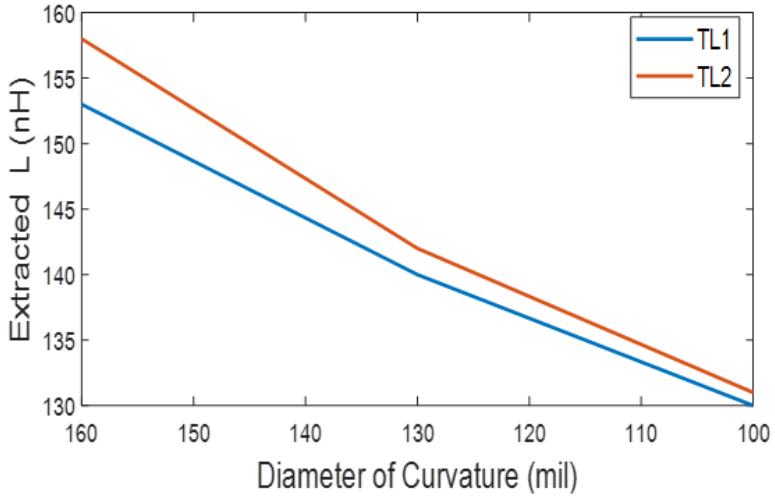


Fig. 5.15 Variation of extracted parasitic L with the number of bending cycles.

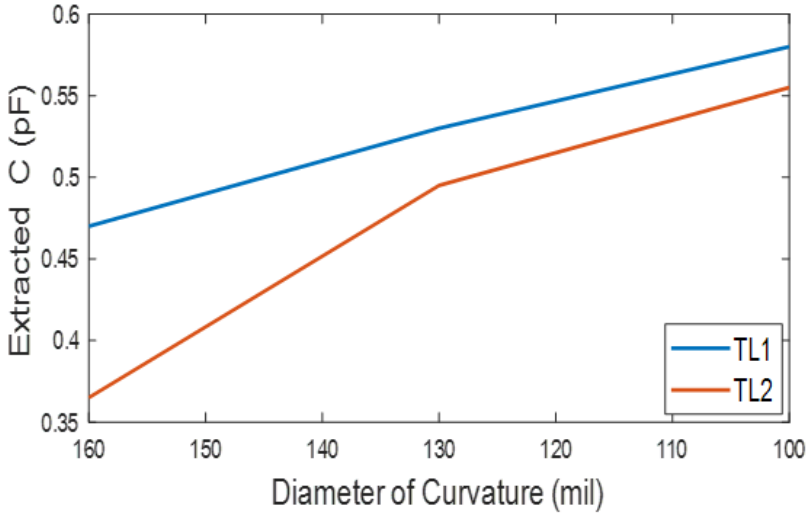


Fig. 5.16 Variation of extracted parasitic C with the number of bending cycles.

respectively. Under flat condition measured inductance and capacitance for TL1 are 160 nH and 0.45 pF, respectively, and those of TL2 are 170 nH and 0.32 pF, respectively. For both TL1 and TL2, the inductance decreases, and the capacitance increases as the diameter of curvature is reduced. The variation of inductance and capacitance is attributed to alteration of dielectric separation.

5.5 Chapter Summary

In this chapter, firstly, the RLC parasitics from an FHE assembly are extracted using a methodology which exploits on-chip ESD protection circuitry. The results infer that the technique is capable of extracting $L_{TL,PCB}$, $C_{TL,PCB}$ and $R_{TL,PCB}$ with relative errors of 0.5%, 0.1% and 6.3% respectively. Also, a method to isolate the parasitic resistance associated with individual printed conductors bonded to a single IC pin is demonstrated. The relative errors in the measured parasitic resistances for all the pins are found to be within 5% under the chosen DC operating current. Finally, the variation of RLC parasitics from an FHE assembly subjected to bending is tracked using the proposed method. The recorded data evinces that variation of the form factor of the substrate due to the application of mechanical stress alters the parasitic resistance, capacitance, and inductance of the FHE assembly.

Chapter 6

Investigation of The Effect of Parasitic Shunt Capacitance Variation on The Start-up of a Wien Bridge Oscillator Circuit

In the previous chapter, using the proposed AC measurement-based technique, it is shown that the parasitic shunt capacitance formed in between signal forward and return path vary due to bending of the flexible substrate. This chapter delineates the impact of the parasitic shunt capacitance variation on the start-up a second-order autonomous oscillator circuit.

6.1 Introduction

Oscillator circuits have a ubiquitous presence in electronic systems as timing reference circuits. Autonomous electronic oscillators are man-made, non-linear circuits which show steady-state oscillation when impelled by a constant energy source like DC power supply. In designing an oscillator circuit, it has long been touted that Barkhausen Criterion is the *necessary and sufficient* condition, while referring to oscillators as steady-state linear

circuits. In saying so, it is assumed that the linear oscillators in the steady state act like an ideal linear mathematical harmonic lossless LC oscillator with a pair of complex conjugate poles on the imaginary axis. This is misleading as a linear oscillator is in fact a mathematical fiction which can only be utilized as a starting point for the design of a real oscillator based on the Barkhausen Criterion [54].

While designing oscillator circuits based on Barkhausen Criterion, the loop of the circuit is broken and Nyquist and Bode plots are checked to see whether the loop gain satisfies the Barkhausen Criterion. The limitation of this open loop approach is that in spite of satisfying the criterion, it can very well be the case that upon closing the loop, the bias point of the amplifier gets altered, hence there is no certainty that the oscillation will build up. So, it is crucial that the oscillator design is based on the characteristic polynomial of the closed-loop circuit, which can be obtained from the closed-loop transfer function of the system.

It also needs to be addressed that the realization of a linear oscillator having poles on the imaginary axis for all times is an impossible act of balance and is quite impractical. In reality, an autonomous oscillator circuit rather relies on transitions between oscillation build up and decay stages having right half plane (RHP) and left half plane (LHP) complex conjugate poles respectively for its operation. Real, practical oscillators must rely on non-linearities for the transition to take place. In the absence of either of these two states, oscillation fails to sustain.

For the oscillation to build up, an autonomous oscillator circuit should have a pair of RHP complex conjugate poles. Presence of parasitic components in the physical implementation of the circuit designed can influence the position of these poles. Moreover, it has already been established in the previous chapter that FHE circuits are susceptible to the variation of the parasitic elements inherent in the circuit due to the variation of its form factor under mechanical stress. So, for FHE implementation of the circuit, investigating the effect of the presence of a single value of a particular parasitic component is not adequate. Rather, variable parasitics should be factored in, a potential range of values of each parasitic component type needs to be accounted for, and their impact on the oscillation build up needs to be investigated.

This chapter investigates the effect of varying parasitic shunt capacitance present at each node between the signal forward and return path on the start up of the Wien Bridge (WB) oscillator circuit. In doing so, firstly, the steady state oscillation behavior using piecewise linear model approach is discussed where the WB oscillator, a non-linear circuit, is treated as a time-varying linear circuit. It is shown that a sustaining oscillation in an autonomous oscillator circuit is the resultant effect of repeated transitions between oscillation build up and decay stages. Then, the start-up condition for the ideal oscillator circuit is analyzed from the perspective of a closed-loop transfer function. Subsequently, the start-up condition for the oscillator circuit in the presence of parasitic capacitance is discussed. Finally, the effect of varying parasitic capacitance on the oscillation start-up is examined and it is shown that an increment in the parasitic capacitance value can prevent the oscillation from building up.

6.2 Investigation of The Steady State Oscillation Behavior Using Piecewise Linear Model Approach

In this section, steady-state oscillation of a second-order autonomous oscillator, i.e., WB oscillator will be investigated using a time varying linear approach, i.e., piecewise linear modelling of the gain of the oscillator system. This approach is also called frozen eigenvalues approach [54] where a non-linear oscillator circuit is treated as a time-varying linear circuit to study the eigenvalues or the poles as a function of time. In doing so, the system action is broken down into two linear stages namely, oscillation build up stage and oscillation decay stage. The oscillation build-up stage is configured to have large gain for small signals and the oscillation decay stage is designed to have small gain for large signals. And, it is shown that the salient process responsible for the steady state oscillation of the oscillator is the balance of oscillation build up (when the oscillation determining poles are on the RHP) with oscillation decay (when the oscillation determining poles are on the LHP).

The oscillator topology illustrated in Fig. 6.1 is a WB oscillator having an amplifier with positive feedback path composed of a series RC and a parallel RC tank. The series and parallel RC tanks designed using R_1, C_1 and R_2, C_2 respectively form the frequency determining part of the circuit. The resonant frequency formed by the tanks can be written

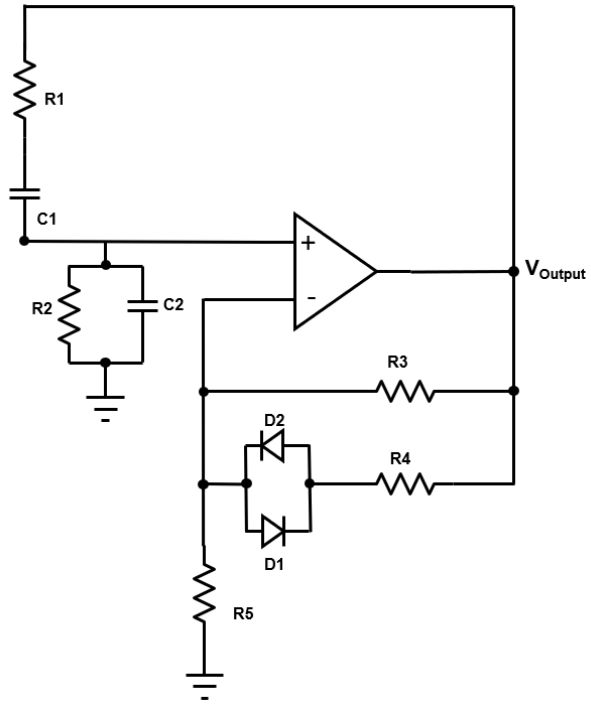


Fig. 6.1 A Wien Bridge oscillator circuit.

as

$$\omega_r = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \tag{6.1}$$

R_3, R_4, R_5 and the anti-parallel diode arrangement are responsible for setting up the non-inverting gain of the amplifier. The anti-parallel diode arrangement or the diode limiter in the feedback path in series with R_3 around the operational amplifier (opamp) is the mechanism to control the movement of the poles between RHP and LHP, i.e., oscillation build up stage and oscillation decay stage. If the opamp is replaced with an ideal voltage-controlled voltage source (VCVS), as shown in Fig. 6.2, then the diode limiter acts as the only means of transition in between the two stages while avoiding the use of non-linear gain of opamp.

The characteristic polynomial of the linearized differential equation describing the second-order oscillator circuit can be obtained from its closed loop transfer function. The charac-

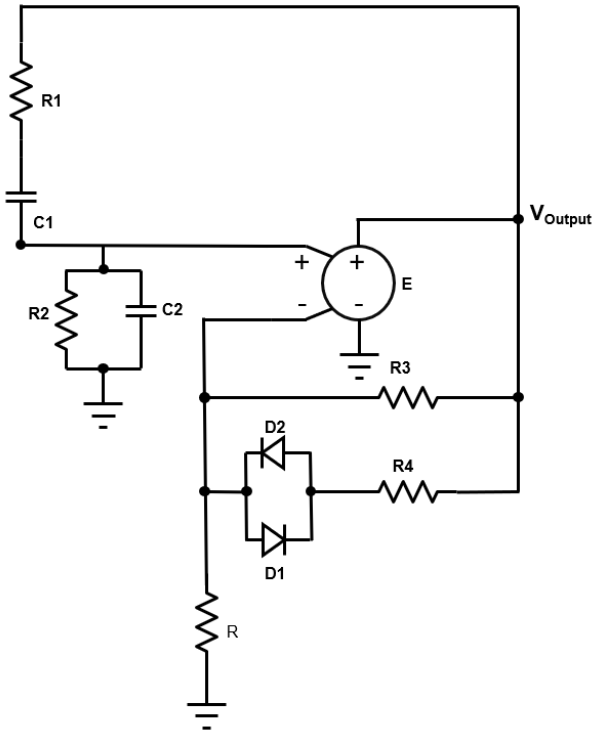


Fig. 6.2 Wien Bridge oscillator implementation using a VCVS.

teristic polynomial can be written in general form as,

$$s^2 + 2\alpha s + \omega_r^2 \tag{6.2}$$

where the roots of this characteristic polynomial are the poles of the circuit.

When the signal amplitude is less than diode threshold voltage, the diode limiter act as open circuit and the gain of the feedforward path is set by R_3 and R_5. Then, the circuit in Fig. 6.2 transforms into the circuit shown in Fig. 6.3 (a). Under such condition, by configuring R_1 and R_5 appropriately, the pole of the closed loop transfer function of the system can be placed on the RHP, i.e.,

$$p_{1,2} = \alpha \pm j\sqrt{\omega_r^2 - \alpha^2} \tag{6.3}$$

which makes the circuit unstable and oscillation begins to build up, i.e., the circuit is

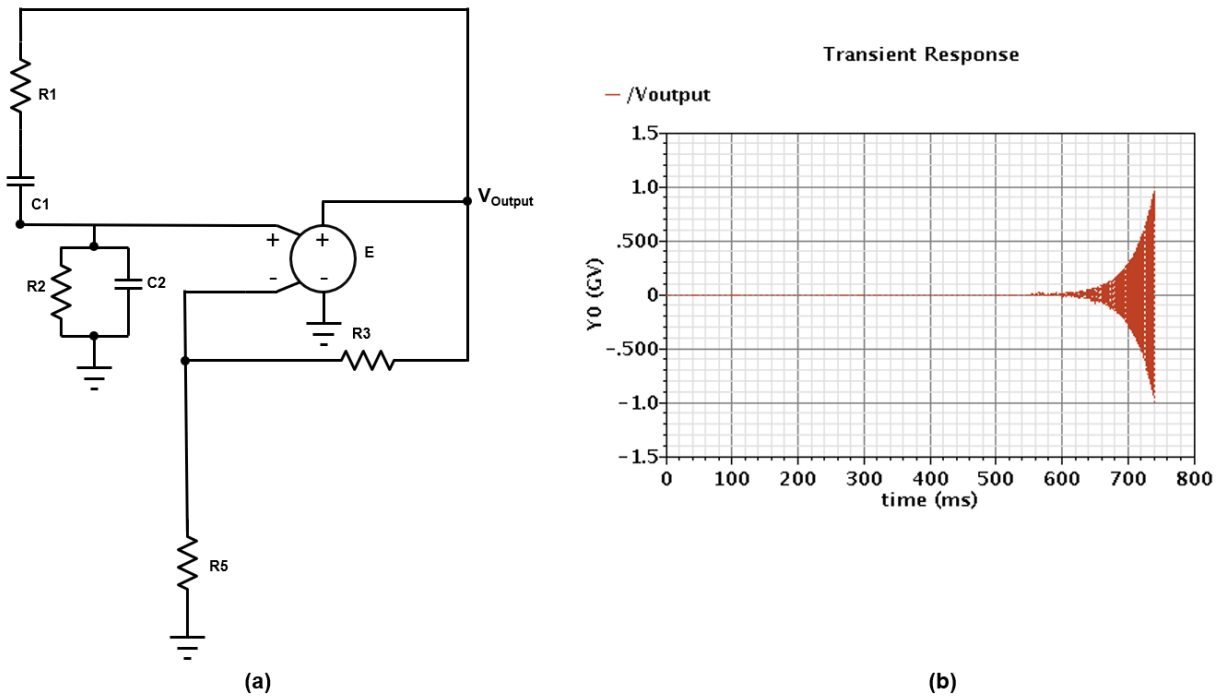


Fig. 6.3 (a) Small signal linear representation in the oscillation build up stage, (b) the transient response.

in the oscillation build up stage. Figure 6.3 (b) illustrates the transient response of the phenomenon.

Figure 6.4 shows the large signal linear representation or the oscillation decay stage. The diode limiter limits the gain of the feed-forward path when the signal amplitude is greater than the threshold voltage of the diode. When the signal amplitude is greater than the threshold voltage, the diode limiter acts as a short and the parallel equivalence of R_1 and R_4 acts to reduce the gain in the feed-forward path. By choosing appropriate value of R4 for a particular value of R_1 and R_5, the system pole can be placed on the LHP , i.e., the oscillation decay stage can be configured, i.e.,

$$p_{1,2} = -\alpha \pm j\sqrt{\omega_r^2 - \alpha^2} \tag{6.4}$$

The circuit remains in this stage until the diode threshold voltage is crossed due to the decaying oscillation, which then shifts the system back to the oscillation build up stage.

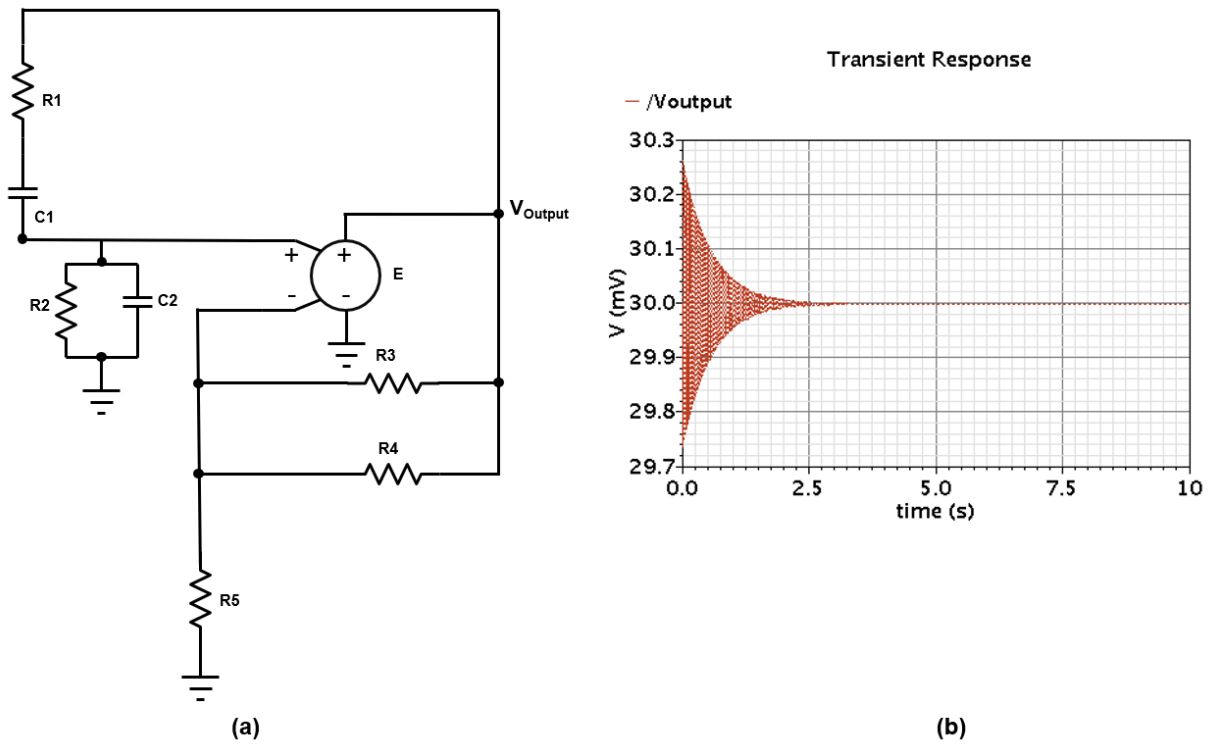


Fig. 6.4 (a) Large signal linear representation in the oscillation decay stage, (b) the transient response.

When the overall circuit is designed to have both the stages, upon providing excitation, due to the continuous and fast transition between these two stages, caused by the diode limiter, a sustaining oscillation is obtained as shown in Fig. 6.5. As a result of this continuous transition at play, the instantaneous frequency changes over time but the average frequency lies in the proximity of the resonant frequency found from Eqn. (4.1).

Conversely, in the absence of either of the stages, the sustaining oscillation cannot be obtained. An oscillation build-up stage must be complemented properly by an oscillation decay stage. Figures 6.6 and 6.7 illustrate the transient responses of two WB oscillator configurations representing two such scenarios. In Fig. 6.6, the small signal stage is setup to have RHP poles and the large signal stage is designed to have pole on the imaginary axis. This results in an ever-increasing oscillating signal, which will be capped by the dynamic range of a practical opamp. On the other hand, the circuit responsible for the transient response shown in Fig. 6.7 is configured to have the poles for the small signal stage on

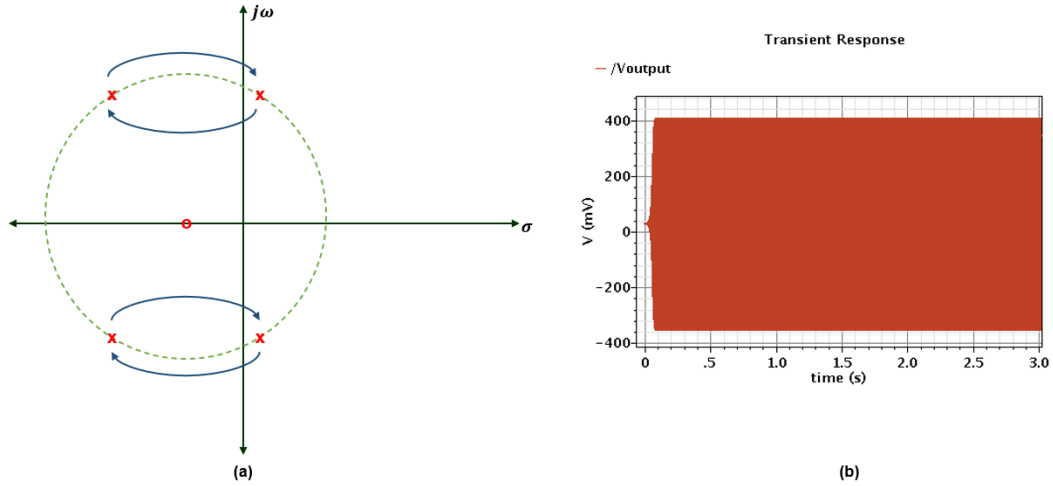


Fig. 6.5 (a) An illustration of complex pole transfer between LHP and RHP, (b) Corresponding sustaining oscillation.

the imaginary axis while having LHP poles for the large signal stage. This duly causes the oscillation to decay as shown. These two instances can be attributed to the absence of oscillation decay and oscillation build-up stage respectively.

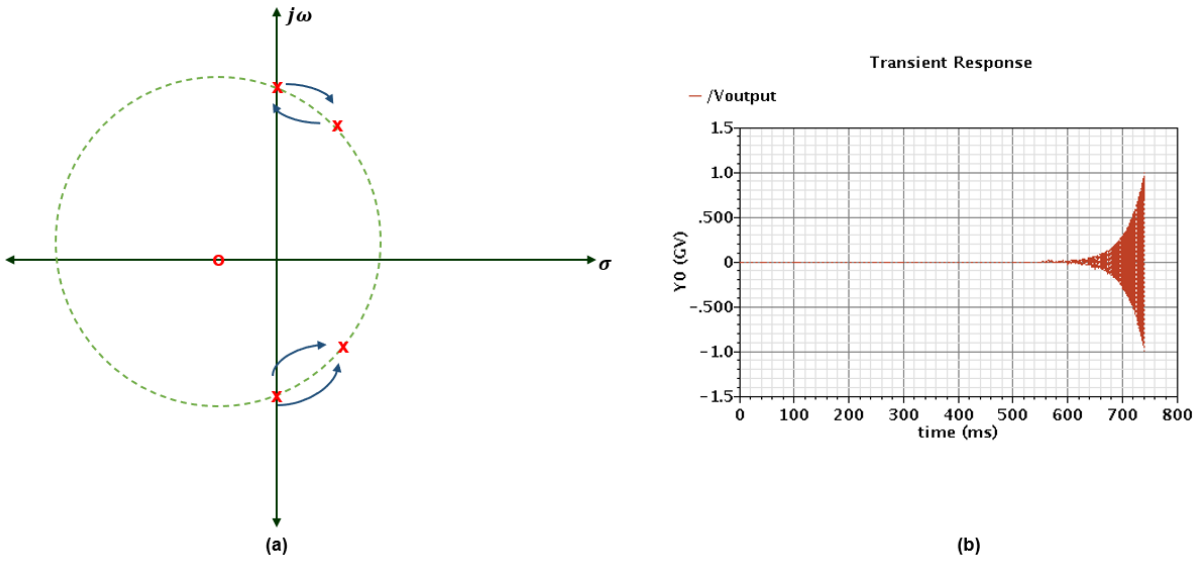


Fig. 6.6 (a) Pole arrangement in the absence of oscillation decay stage, (b) corresponding transient response.

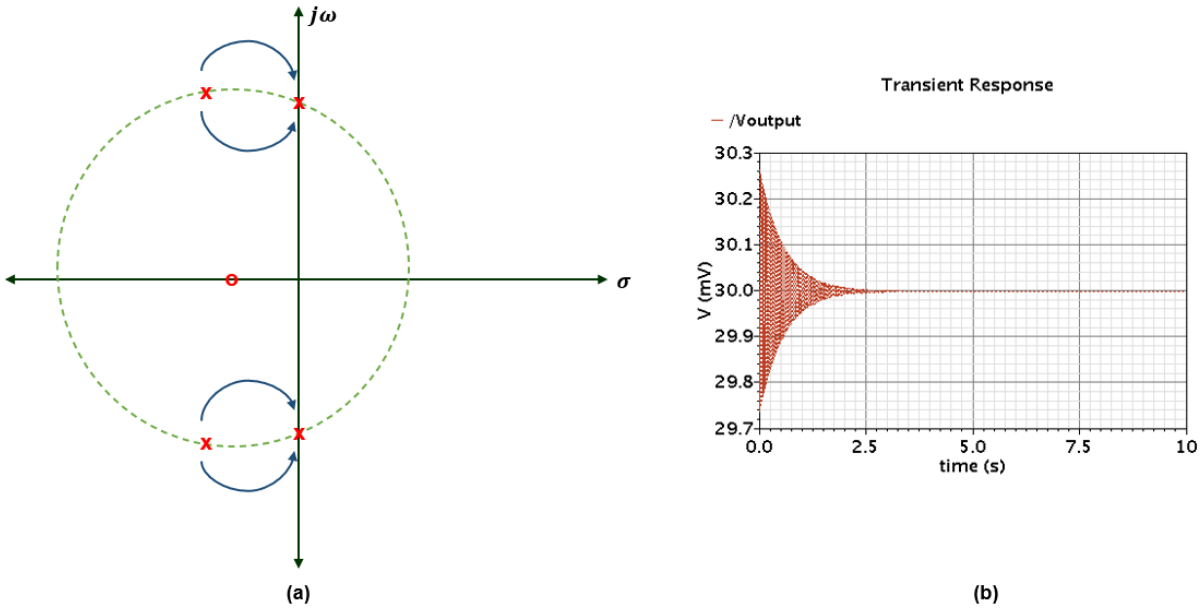


Fig. 6.7 (a) Pole arrangement in the absence of oscillation build up stage, (b) corresponding transient response.

6.3 Investigation of The Start-up of Wien Bridge Oscillator

In this section, the start-up of oscillation of a WB oscillator with and without the presence of parasitic capacitance is analyzed. At first, the start-up of the ideal WB oscillator circuit will be discussed in the absence of parasitic element. Then, parasitic element in form of shunt capacitance formed in between the signal forwarding path and the signal return path at each node is introduced and its effect on the start-up behavior of the circuit is studied. Finally, variable parasitic capacitance is introduced and the susceptibility of complex conjugate pole pairs responsible for the oscillation build up to the varying parasitic capacitance is examined.

6.3.1 Start-up of Wien Bridge Oscillator Without Parasitics

In the absence of parasitics, an ideal WB oscillator is a second-order circuit.Upon solving for the denominator of its close loop transfer function, i.e., the characteristic equation of

the closed loop system, two poles can be obtained whereas a system zero can be obtained by solving for the numerator. So, the ideal closed loop WB oscillator is a two pole, one zero system. Due to the presence of zero, the root locus of the system is not parallel to the imaginary axis, which makes it possible to drive the two poles of the system from LHP to RHP and vice versa by changing the gain of the system. As the root locus of the second-order oscillator revolves around the zero, while designing an oscillator, the zero needs to be positioned in such a way that the root locus can cross the imaginary axis. Mathematically, the condition can be expressed as,

$$\sqrt{|p_1 - z||p_2 - z|} > |z| \tag{6.5}$$

That is, the radius of the root locus circle must be larger than the distance from the zero to the origin [55]. Under such condition, the gain control mechanism will be able to move the pole in between LHP and RHP. As it has been stated earlier, in order to build up oscillation, the circuit has to be designed to have a pair of complex conjugate poles on the RHP. The following mathematical condition has to be satisfied to place the pole on the RHP-

$$EC_1R_1R_3 > EC_1R_2R_5 + EC_2R_1R_5 + C_1R_1R_3 + C_1R_1R_5 + C_1R_2R_3 + C_1R_2R_5 + C_2R_1R_3 + C_2R_1R_5 \tag{6.6}$$

Here, R_3 can be used as the degree of freedom and can be varied to place the pole on the RHP. Little research has been conducted on how far out on RHP this start-up pole pair can be placed and its subsequent effect on the steady state oscillation. Due to the presence of zero, and the subsequent nature of the root locus, changing the positions of the poles changes both its real and imaginary part. That is, the rate of energy transfer as well as the frequency change simultaneously which results in the loss of orthogonality of the control of these two parameters, which needs to be considered while designing an oscillator of this kind. Figure 6.8 illustrates the sensitivity of the real and imaginary part of the complex conjugate poles to the variation of the non-inverting gain of the opamp in the system.

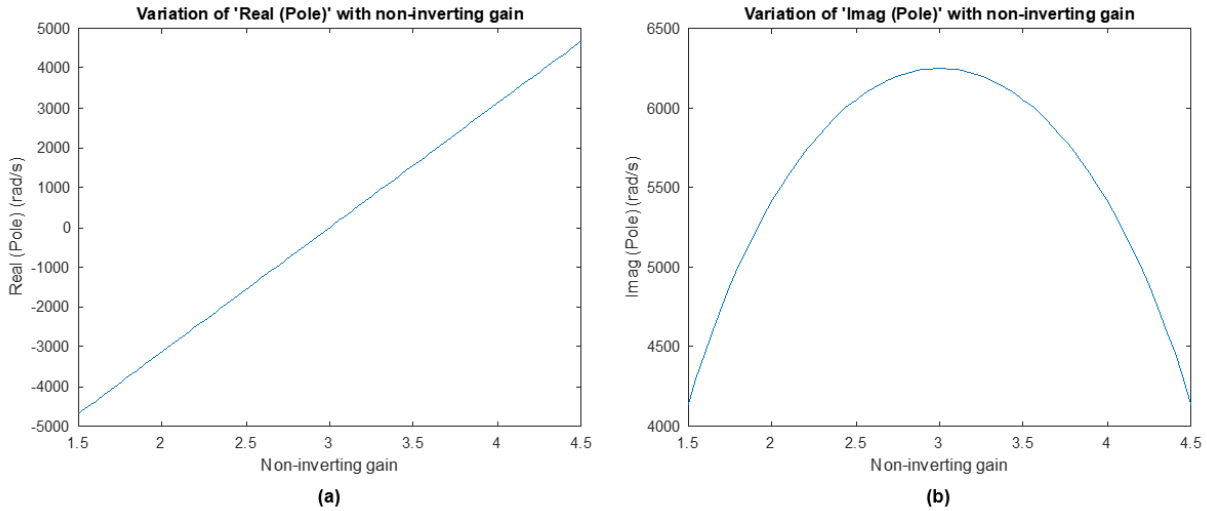


Fig. 6.8 Variation of the real and imaginary part of the pole with respect to the non-inverting gain.

6.3.2 Start-up of Wien Bridge Oscillator With Parasitics

Figure 6.9 shows a WB oscillator start-up circuit with parasitic shunt capacitance, C_p formed between the node's signal forwarding path and return path to ground. When parasitic shunt capacitance is considered, the closed loop transfer function describing the system contains three poles and two zeros. An unscaled plot of the relative positions of the poles and zeros is demonstrated in Fig. 6.10.

Similar to the circuit in Fig. 6.2, the complex conjugate pole pairs of this circuit are responsible for the oscillation of the system and when placed on the RHP, builds up the oscillation. But, due to the introduction of the additional parameter, C_p, both the real and imaginary part of the complex conjugate poles get affected. As a result, their variability with respect to the change in the non-inverting gain of the opamp is not the same as that of the ideal scenario. Figure 6.11 presents the variation of the real and imaginary parts of the complex conjugate poles due to a change in the non-inverting gain for both the ideal and parasitic cases.

As it is apparent from Fig. 6.11 that parasitic capacitance changes the sensitivity of the real and imaginary part of the complex pole pairs, the root locus of the pole due to the

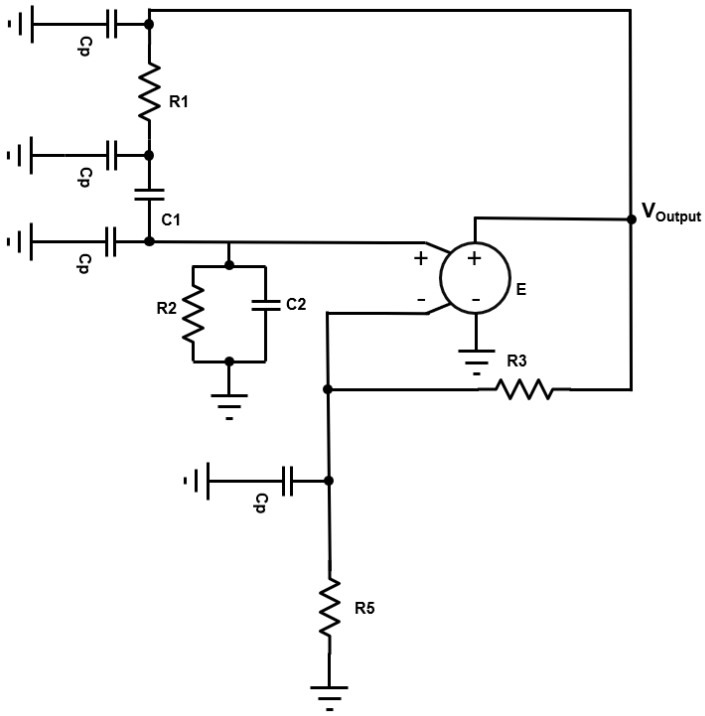


Fig. 6.9 Wien Bridge oscillator start-up circuit with parasitic shunt capacitance.

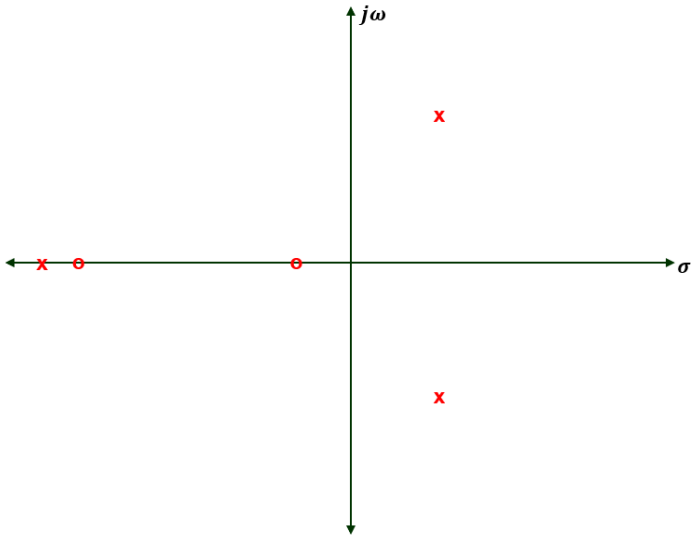


Fig. 6.10 Unscaled pole-zero plot of the third order system with three poles and two zeros.

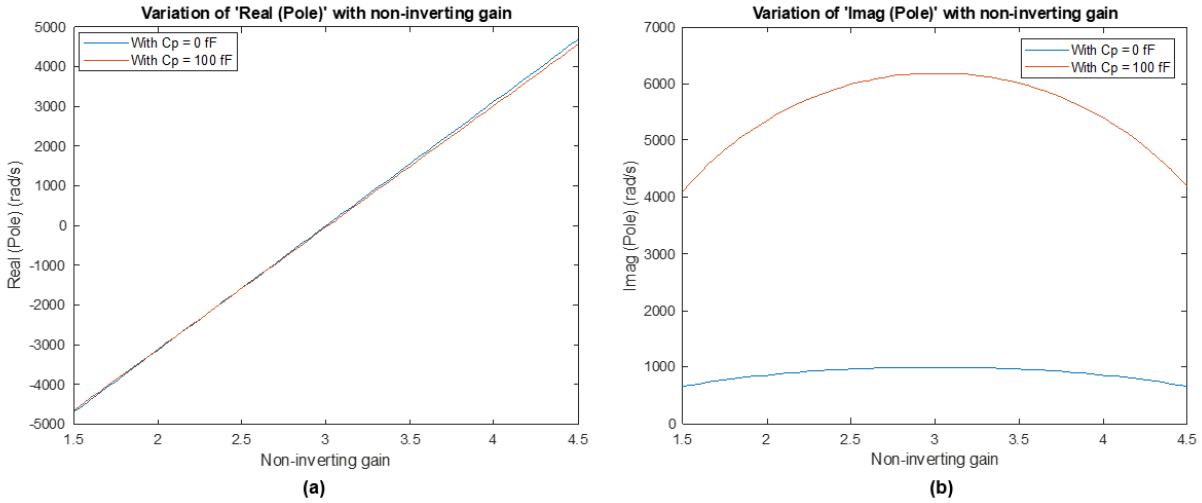


Fig. 6.11 Comparison of the variation of (a) real and (b) imaginary part of the poles with and without parasitic capacitance to the non-inverting gain.

variation of the non-inverting gain of the opamp is also dissimilar from that of an ideal WB oscillator circuit. Figure 6.12 illustrates the root locus of the positive complex conjugate pole due to the variation of the non-inverting gain for an ideal oscillator and an oscillator

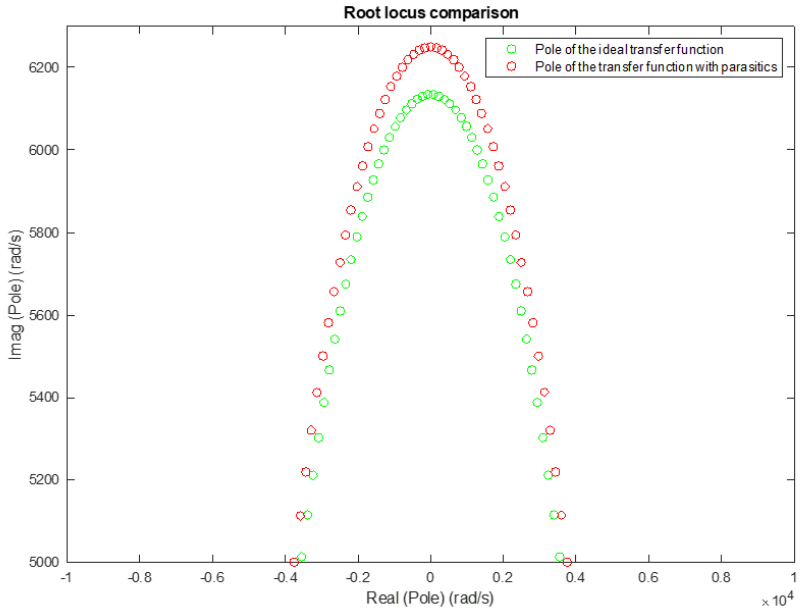


Fig. 6.12 Root locus comparison in the presence and absence of parasitic capacitance.

with parasitic capacitance from which the difference is evident.

Now, to realize the effect of increasing parasitic capacitance, ΔC_p on the pole position, the variation of real and imaginary parts of the complex pole pairs are examined with respect to increased parasitic capacitance, $C_{p(final)} = C_p + \Delta C_p$. Figure 6.13 incorporates the increasing parasitic capacitance in the start-up circuit of the WB oscillator.

Now, for a particular arrangement of values of the circuit's components, resulting in the RHP complex conjugate pole pairs, ΔC_p can be increased and the resultant change in the real and imaginary part of the poles for corresponding values of $C_{p(final)}$ can be examined.

As seen in Fig. 6.14, there is a inverse dependence of both the real and imaginary parts of the pole on the parasitic capacitance variation. Due to the increment of the parasitic capacitance, $C_{p(final)}$, imaginary part of the pole decreases, i.e., the oscillation will build up with a smaller frequency. Moreover, as the real part of the pole is also inversely proportional to $C_{p(final)}$, increased parasitic capacitance can make the pole travel to the LHP which will not allow the oscillation to build up. This is an important factor to consider while designing

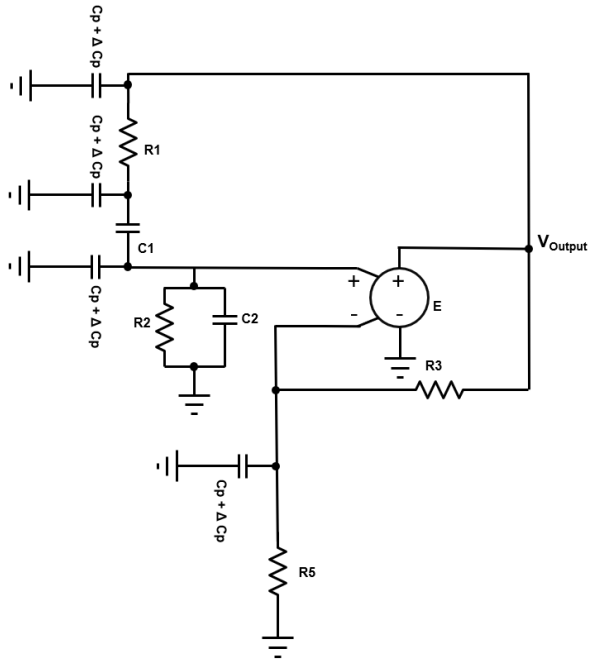


Fig. 6.13 Wien Bridge oscillator start-up circuit with increased parasitic shunt capacitance.

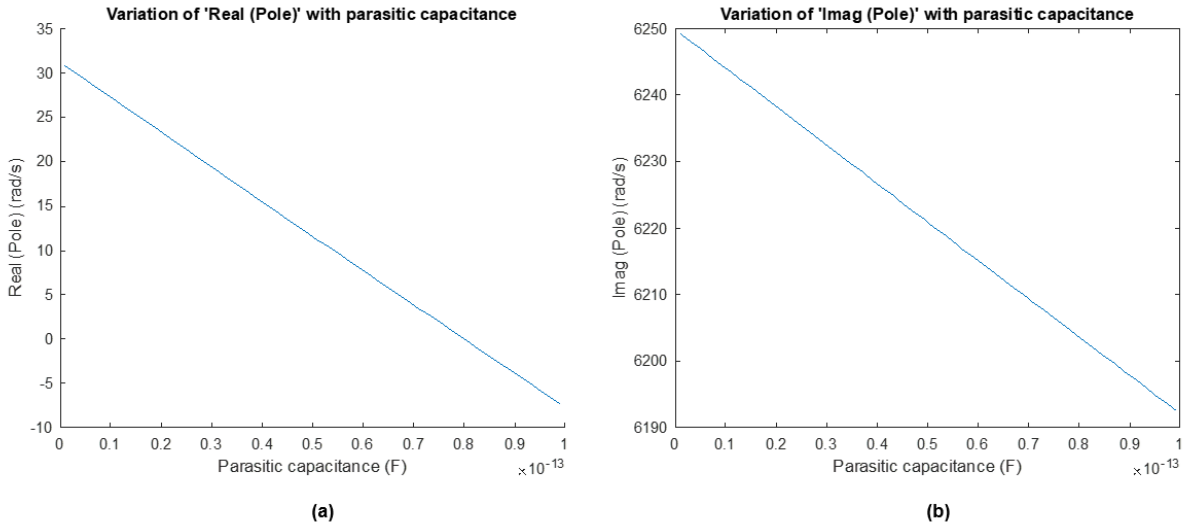


Fig. 6.14 Comparison of the variation of (a) real and (b) imaginary part of the poles due to variation of parasitic capacitance.

WB oscillator circuit on flexible substrate. It has already been demonstrated in the previous chapter that when the dielectric separation changes between the signal forward and return path, an increment in the value of the shunt parasitic capacitance takes place. Although start up can take place when the substrate is flat, in the absence of sufficient headroom for the increased capacitance while bent, it will fail to do so leaving the circuit inutile.

6.4 Simulation Test Benches

In order to test oscillation build up at the design level, pole-zero and transient analyses are performed using Cadence Virtuoso platform. At first, the pole-zero analysis has to be performed to check whether the complex conjugate pole pair is on the RHP. To do that, test bench illustrated in Fig. 6.15 (a) is used. In this test bench, the ideal current source is configured to provide AC signal necessary to perform the pole-zero analysis. Then, the system pole is checked at the V_{output} node.

After performing the pole-zero analysis, the transient analysis is performed using the test bench shown in Fig. 6.15 (b). Here, to provide the initial excitation to the oscillator

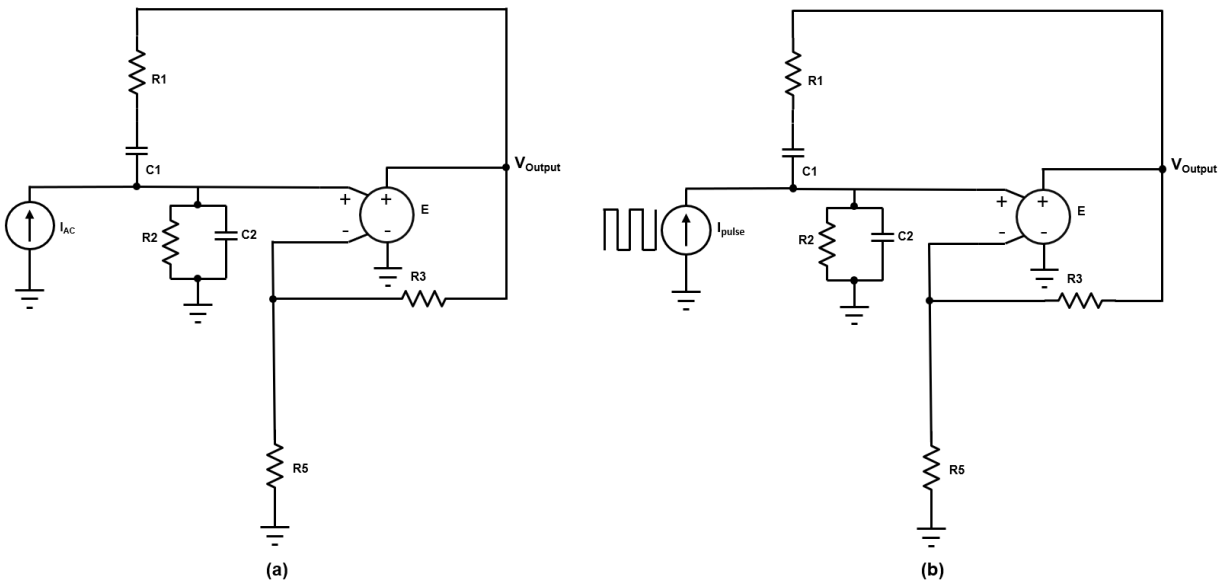


Fig. 6.15 Test bench: (a) to perform the pole-zero analysis, (b) to perform the transient analysis.

circuit, a single fast and sharp current pulse is provided for the entirety of the simulation run-time. As after the duration of the pulse width the ideal current source provides zero current to the system, i.e., the current source acts as an open circuit, the system remains unaltered and can mimic the transient behavior of an autonomous oscillator according to the circuit configured.

6.5 Simulation Configuration And Results

A WB circuit is configured to have a resonant frequency of 994.718 Hz. Using Eqn. (6.1), R_1 and R_2 are chosen to have a value of 10 $M\Omega$ for $C_1 = C_2 = 16\ pF$. Then, R_3 and R_5 are chosen to have values 20.02 $k\Omega$ and 10 $k\Omega$ respectively whereas the gain of the voltage-controlled voltage source is set to be 10^6 V/V. For providing the excitation in the transient analysis of the system, I_{pulse} is configured to provide a sharp pulse of 1 μA for a duration of 1 μs with 1 ns rise and fall time for the whole duration of the transient simulation, which in this case is 10 s. At first, pole analysis is performed in the absence of the parasitic shunt capacitance using the test bench shown in Fig. 6.15 (a). Then, Parasitic shunt capacitance

Table 6.1 Pole location corresponding to a parasitic capacitance value

Parasitic capacitance, $C_{p(final)}$ (fF)	**Pole location (rad/s)**
0	$+2.173 \pm 994.685$
2	$+1.723 \pm 994.592$
4	$+0.869 \pm 994.634$
6	$+0.01 \pm 994.2$
8	-0.8476 ± 994.034
10	-1.705 ± 993.983

is introduced and increased in steps of $\Delta C_p = 2\ fF$ and the corresponding pole locations are recorded. Table 6.1 lists the location of the complex conjugate pole pairs corresponding to respective $C_{p(final)}$ values.

As predicted, an increase in the $C_{p(final)}$ value shifts the pole gradually to the LHP and prevents the build up of the oscillation. Figure 6.16 illustrates the build up of the oscillation when $C_{p,(final)} = 0\ fF$ and the absence of it when $C_{p,(final)} = 8\ fF$. That means, in the FHE implementation of this oscillator circuit designed, if the parasitic shunt capacitance increases to 8 fF or more while bent, oscillation start up will not take place.

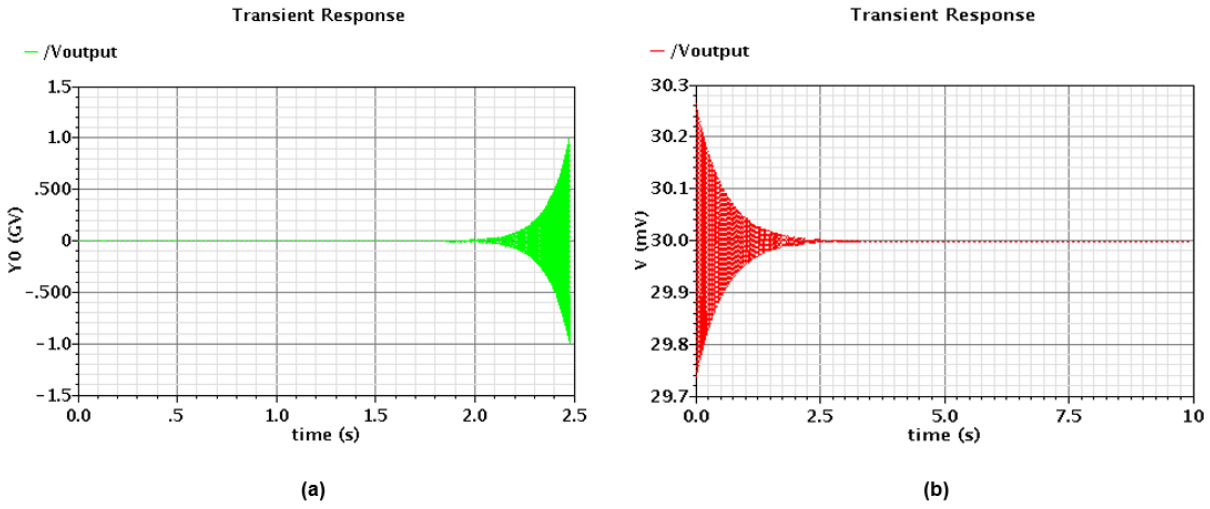


Fig. 6.16 Transient response of corresponding to pole placement in (a) RHP, (b) LHP.

6.6 Chapter Summary

In this chapter, impact of parasitic shunt capacitance variation on the start-up of a WB oscillator circuit is investigated. At first, it is shown that the steady-state oscillation is the result of continuous transitions between the oscillation build up and decay stages. It is also shown that, in the absence of one of these stages, oscillation does not sustain. Next, the start-up condition of an ideal WB oscillator from the perspective of a closed loop transfer function is analyzed which is then modified to accommodate the parasitic shunt capacitance present at each node between the signal forward and return path. Then, the effect of increasing parasitic capacitance value on the complex conjugate pole pairs and in turn on oscillation build-up is analyzed. Bending of the substrate in FHE implementation of the system lessens the dielectric separation between conducting traces. Consequently, it is shown that due to the increase of the parasitic capacitance value, the poles responsible for oscillation can shift to the LHP, restricting the oscillation from building up. Hence, for an FHE implementation of the oscillator circuit, assessment of the parasitic capacitance variation is required and the system has to be designed to have sufficient headroom in the pole position so that the varying capacitance cannot shift the poles to the LHP to ensure oscillator build-up.

Chapter 7

Conclusion

7.1 Thesis Contribution

In this thesis, the parasitic elements present in the FHE system were investigated. A bending machine was fashioned to exert mechanical stress on the assembled prototypes in a controlled manner. Measurement techniques were introduced to extract parasitic resistance, inductance, and capacitance from the post-assembly FHE prototypes. Furthermore, upon recording the variation of these parasitic components due to the application of the mechanical stress, it was shown that the parasitic elements vary due to the effect of the mechanical stress applied. Then, the significance of considering and including the effect of varying parasitics on the design of a functional circuit was demonstrated by studying its effect on the start-up of a ubiquitous electronic system like oscillator circuit. **Chapter 2** provided a chronological and detailed workflow of building FHE prototypes and also discussed the associated challenges in each step. In **chapter 3**, the design of the bending machine used to perform ROC test was delineated. **Chapter 4** articulated a DC measurement-based approach to measure the individual parasitic resistances present between the individual pins of an IC package and the substrate of the post-assembly FHE system. Subsequently, using the measurement technique, variation of the contact resistance due to bending of the substrate was tracked. Afterwards, **chapter 5** presented an AC measurement-based approach to extract all three parasitic components- resistance, capacitance, and inductance

present in the post-assembly FHE system. Using the technique it was shown that due to the variation of the form factor of the substrate under stress, all three parasitic elements vary. In **chapter 6**, at first, the steady state oscillation of a second-order WB oscillator circuit was investigated using a piecewise linear approach which demonstrated that a pair of RHP complex conjugate poles is necessary for the oscillation to build up. Later, the effect of the presence of parasitic shunt capacitance in between the signal forward path at each node and the return path on these pole positions and subsequently, on the start-up of the oscillation was examined. Simulation results inferred that the position of the complex conjugate pole pair is sensitive to the variation of the parasitic shunt capacitance. Consequently, an increase in the parasitic capacitance, caused by the change in the form factor due to bending, can lead to the failure of the oscillation build-up. Therefore, it is evident that the variation of the parasitic elements is critical for systems designed for implementation in flexible, hybrid domain and that is why it should be included and accounted for in the design of systems for such applications.

7.2 Future Work

This thesis evinced the variation of the parasitic elements when the assembled prototype is subjected to ROC tests. Further experiments can be and are needed to be performed for the quantitative assessment of the variation of these parasitic elements under other types of mechanical tests such as stretch and twisting tests.

As mentioned before, variation in the form factor of the FHE assembly and the amount of mechanical stress applied are dictated by the requirement of the application domain. The impact of the variation of these aforementioned parameters on all three parasitic elements should be considered at the design-level of any system. Hence, from this perspective, the effect of variation of parasitic elements on the start-up of the WB oscillator circuit when subjected to different types of mechanical stress such as bending, stretching, and twisting can be investigated in the future. Furthermore, the variation of the parasitic resistance, inductance, and capacitance on other second and higher order autonomous oscillator circuits needs to be investigated to ensure proper functioning of these systems in their FHE implementation.

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