Design of Modular Multilevel Converter-based Solid State Transformers

Ali Shojaei

Department of Electrical and Computer Engineering

McGill University, Montreal, Canada

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Abstract

A Solid State Transformer (SST) performs the tasks of a conventional transformer by means of power electronic converters and high-frequency transformers. In addition to voltage level transformation, some SST topologies are able to provide ancillary services to the AC grid.

In a three-stage SST, the first-stage is an AC/DC converter. In most designs, this stage employs a multilevel converter topology rather than a two-level converter. The reason for this is that a multilevel converter provides such advantages as capability to interface with a medium voltage AC grid.

Among all multilevel converter topologies, a new generation of multilevel converters called Modular Multilevel Converter (MMC) has been considered to be a promising topology for medium/high voltage converters in back to back and High-Voltage DC (HVDC) applications.

This thesis first studies the design, modulation, and control of an MMC. In this context, a modulation and control strategy is proposed which decreases the level of harmonics in the output voltage and current of the converter. Further, the proposed strategy pushes the harmonics towards higher frequencies and, hence, allows the converter to be switched at lower frequencies.

Next, this thesis proposes a number of three-stage SST configurations employing an MMC in their first stage. An advantage of the proposed SST configurations is that they are readily scalable to higher voltage levels and power ratings; this enables the application of an SST in higher levels of electrical grids. Further, the proposed SSTs feature a high-voltage DC terminal in addition to the commonly provided terminals to enable connection of the SST to a DC distribution grid.

Résumé

Un Transformateur à Semi-Conducteurs (TSC) effectue les tâches d'un transformateur conventionnel en utilisant des convertisseurs électroniques et transformateurs de haute-fréquences. En plus des conversions reliées aux niveaux de voltages, certaines topologies de TSC ont la capacité de fournir des services auxiliaires sur le réseau CA.

Dans un TSC à trois stades, le premier stade est un convertisseur CA/CC. Pour la majorité des conceptions, ce stade utilise une topologie d'un convertisseur à multi-niveaux au lieu d'un convertisseur à deux niveaux. La raison pour ceci est que le convertisseur à multi-niveaux offre des avantages tels que la capacité de se relier à un réseau CA de moyenne tension.

Parmi toutes les topologies de convertisseurs à multi-niveaux, une nouvelle génération de convertisseurs à multi-niveaux dénommés Convertisseurs Modulaires à Multi-niveaux (CMM) fut démontrée d'être une topologie prometteuse pour convertisseurs à moyenne/haute tension dans applications directes et de CC à Haute Tension (CCHT).

Cette thèse fait premièrement référence à la conception, la modulation et le contrôle d'un CMM. Dans ce contexte, une stratégie de modulation et de contrôle est proposée, notamment qui réduit le niveau d'harmoniques au voltage et au courant de sortie du convertisseur. De plus, la stratégie proposée comprend la conversion de ces harmoniques à des fréquences plus élevées et, par conséquent, permet la commutation du convertisseur à des fréquences plus basses.

Par la suite, cette thèse propose quelques configurations de TSC à trois stades utilisant un CMM au premier stade. Un avantage de ces topologies TSC proposées est qu'elles sont évolutives/adaptables à des niveaux de tensions et puissances plus élevées; ce qui permet

l'application d'un TSC sur réseaux électriques à niveaux plus élevés. De plus, les TSC proposés comprennent une borne CC à haute tension en plus des terminaux normalement fournis afin de permettre le branchement du TSC à un réseau de distribution CC.

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Chapter 1 - Introduction

1.1 Introduction

The smart-grid vision has attracted widespread research attention. It refers to evolution of a partially-automated human-assisted electric power system to a fully-automated system. Mitigation of environmental impacts, improvement of performance, better asset management and enablement of real-time interactions are among the main objectives of the smart-grid [1, 2]. Implementation of a smart-grid employs state-of-the-art monitoring, control, protection, and operation strategies such as power-electronic devices and systems, information and communications technologies, signal processing and automatic control and sensing, monitoring and metering.

As shown in Fig. 1-1, three key elements of a smart-grid are the Intelligent Energy Management (IEM) units, the Intelligent Fault Management (IFM) units, and Reliable and Secure Communication (RSC). The IEM unit manages the power flow among sources and consumers and thereby enables flexible energy sharing. The IEM unit embodies a Solid State Transformer (SST), the Distributed Grid Intelligence (DGI) software, and the communication interface [3]. The SST performs physical power routing and voltage step-down functions, and it consists of power electronic converters, high-frequency transformers, and auxiliary and control circuits. The high-frequency transformer performs the step-up/down function and the isolation

task, whereas the power electronic converters provide extra features to the SST. These features include voltage regulation, power flow regulation, non-standard customer voltages (DC or 400 Hz AC), voltage sag compensation, power factor correction, and harmonic and fault isolation [4-6]. Further, the weight and volume of an SST can be up to three times less than those of a Line-Frequency Transformer (LFT) with the same power rating, owing to the use of high frequency transformers [7].

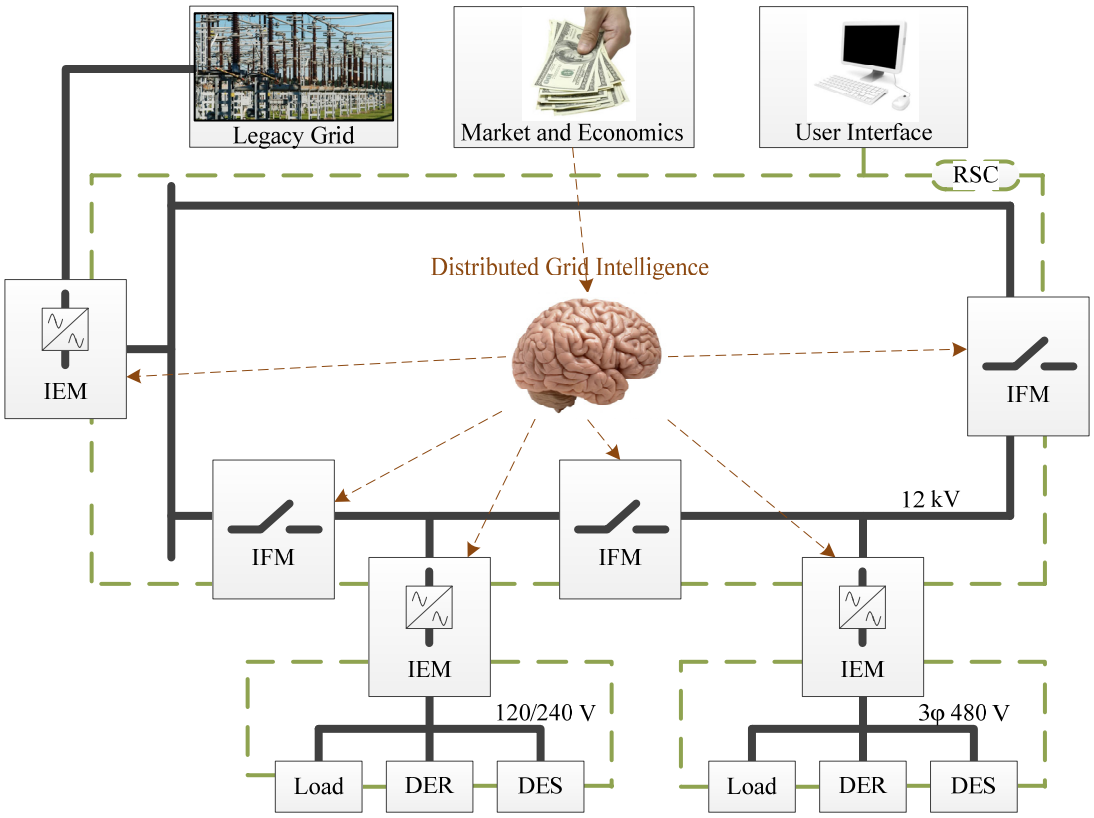


Fig. 1-1. Key elements of a Smart-grid

Unlike an LFT, an SST can provide both the AC and DC terminals. A commonly adopted SST configuration has three ports which enable it to connect and route the electric energy among High Voltage AC (HVAC) distribution network, Low-Voltage AC (LVAC) consumers and Low-

Voltage DC (LVDC) sources and storage devices. Fig. 1-2 shows a functional diagram of such an SST.

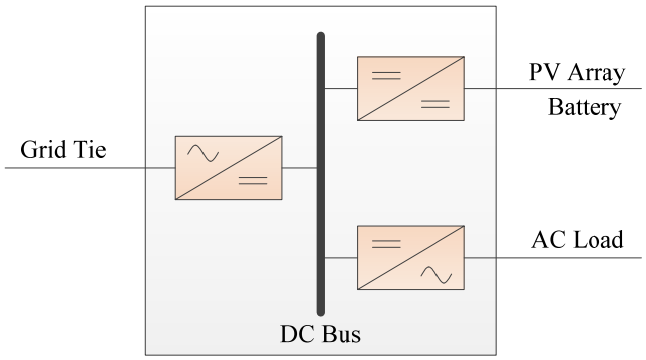


Fig. 1-2. Functional diagram of the SST

The SST interfaces Distributed Renewable Energy Resources (DRER), Distributed Energy Storage Devices (DESD), loads, and the distribution grid and is able to manage the power routing among all the connected devices [8].

Since an SST is interfaced to a medium voltage network, multilevel converters, typically cascaded multilevel converter, are used at the input stage of an SST. A new multilevel converter topology, called Modular Multilevel Converter (MMC), has been proposed in [9, 10]. The MMC is a potential candidate for back-to-back applications [11]. Although all multilevel converters can reach high power and medium voltage levels [12], MMC has become more attractive in these applications because of its advantages over other types. Some of those advantages include [13]: the scalability, inherent redundancy for failure management, increased efficiency, elimination of capacitors at the DC-bus, and fast dynamic control of AC- and DC-side under transient and fault conditions.

1.2 Problem Statement

A problem with common SST configurations is the lack of scalability to higher voltage levels. As mentioned before, today's SST topologies use multilevel converters at the input stage of the SST, which brings a good level of modularity to these topologies. The cascaded H-bridge multilevel converter is well adopted in this application, while use of diode clamped multilevel converter is also reported [14]. Nevertheless, one major problem of these multilevel converters is that the number of the achievable voltage levels is quite limited. This is because of the voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints [15]. This limitation on number of levels prevents the application of an SST in a high voltage grid. Therefore, it is required to investigate the application of modular high-voltage converters in the structure of an SST. This is an essential step to realize medium-voltage smart-grids, which interface a high-voltage grid through an SST.

The other deficiency of the most of common SST configurations is the lack of a High-Voltage DC (HVDC) terminal, which prevents use of SSTs in future DC distribution networks. Note that a Medium-Voltage DC (MVDC) link in common SST topologies typically has a voltage level of 4 kV or less, and is unable to interface a DC distribution network. Therefore, it is necessary to investigate new SST topologies with the ability to interface a DC distribution network. An SST topology that has both HVAC and HVDC terminals could be employed in either AC or DC distribution networks, or even it can simultaneously connect to both networks and performs power routing between them. If both LVDC and LVAC terminals are provided, this topology can universally be employed for any type of distribution network/load/storage configuration.

In this work, a Modular Multilevel Converter is adopted to design an SST. This converter is highly modular and by employing it as the input stage, it makes the SST topology readily scalable to higher voltage levels. MMCs have a good overall efficiency and are proved to be a potential solution for medium and high voltage applications. This type of converter provides an HVDC terminal as well as an HVAC terminal. Therefore the designed SST, based on an MMC, can be employed in both AC and DC distribution networks. The proposed configuration provides also LVAC and LVDC terminals which enables it to interface different types of load and storage units.

1.3 Scope of Work

The scope of this thesis is to develop solid state transformers which are flexible, modular, and scalable, and therefore, applicable to medium- and high-voltage grids. Moreover, the proposed SSTs will provide both high-voltage AC and DC terminals, and therefore, they can be employed in both AC and DC networks. The proposed SSTs are assumed to provide low-voltage AC and DC terminals in order to offer a good level of flexibility in interfacing different types of loads, generation and storage units.

1.4 Literature Review

In this section we present a literature review on modular multilevel converters and solid state transformers.

1.4.1 Modular Multilevel Converter

An MMC is a multilevel converter, presented by Marquardt *et al.* [16], which has attracted lots of research interest. The most important features of MMCs compared to other multilevel converters are their high level of modularity and scalability, their high efficiency which is especially important in high power applications, and finally, their superior harmonic performance [17].

This type of multilevel converters is expected to be the next-generation power converter for medium- and high-voltage applications such as motor drives, back-to-back systems, and HVDC applications [18]. Siemens has been using this converter in its latest HVDC system, with the trade name "HVDC-plus". This converter is ideal for connecting remote offshore platforms and wind farms to onshore grids [19]. The first practical application of this system is an HVDC transmission link between city of San Francisco and a Pacific Gas & Electric substation near Pittsburg, California [20].

The back-to-back MMCs configuration for interfacing high power renewable energy sources (RES), such as wind turbines, to grids has attracted interest as one of the most cost effective ways to generate electricity [21]. Application of multilevel converters permits the direct connection of wind turbines to the medium voltage electric grids without using expensive, bulky, and heavy 50/60-Hz transformers [22].

1.4.1.1 MMC Structure

A basic structure of a three-phase MMC is shown in Fig. 1-3. Each arm of the MMC has *N* sub-modules (SM), and a leg consists of the upper and lower arms of a phase. In each arm, there

is an inductor which suppresses the curling current inside the two arms of a leg. The coupling inductors between the converter and the grid are not necessary due to presence of the inductors in the legs; however, these coupling inductors are required if coupled or center-tapped inductors are used inside the MMC [18].

A number of circuit configurations are proposed in the literature to be used as an SM circuit [17, 23, 24]. Traditionally, each SM in an MMC is either a full- or half-bridge converter. In the case of a half-bridge converter, the SM consists of two IGBT switches, *S1* and *S2*, two anti-parallel diodes, *D1* and *D2* and a capacitor, *C*. The output voltage of each SM is either the voltage of its capacitor or zero. MMCs with half-bridge SMs are also called the Double-Star Chopper-Cells (DSCC) converters [16]. A Double-Star Bridge-Cells (DSBC) converter is an MMC with full-bridge SMs, and it has buck/boost functions of the DC-link voltage [25]. Therefore, DSBC converters are suitable for power conditioning systems for renewable resources such as solar and wind power. An SM of this converter can repurpose its capacitor to suppress a short-circuit fault current on the DC link. This converter, however, has shortcomings such as higher losses and higher cost due to the use of twice as many IGBTs as in a conventional half-bridge structure [26]. DSCCs, on the contrary, are easier to be built up and control. They also have higher efficiency and have more practical applications [16].

Recently other SM configurations for MMCs have been proposed in the literature. In some of these configurations, a three level Flying Capacitor (FC) or a three level Neutral Point Clamped (NPC) converter is used as an SM of an MMC [27, 28]. These configurations are not very attractive from manufacturing and control perspective [17]. A clamp-double SM consists of two half-bridge converters connected at the DC side through two diodes and one IGBT switch. This

SM has a higher semiconductor loss compared to a half-bridge SM and a lower loss compared to a full-bridge SM [17]. A number of recently proposed configurations for the SM circuit are presented in [24].

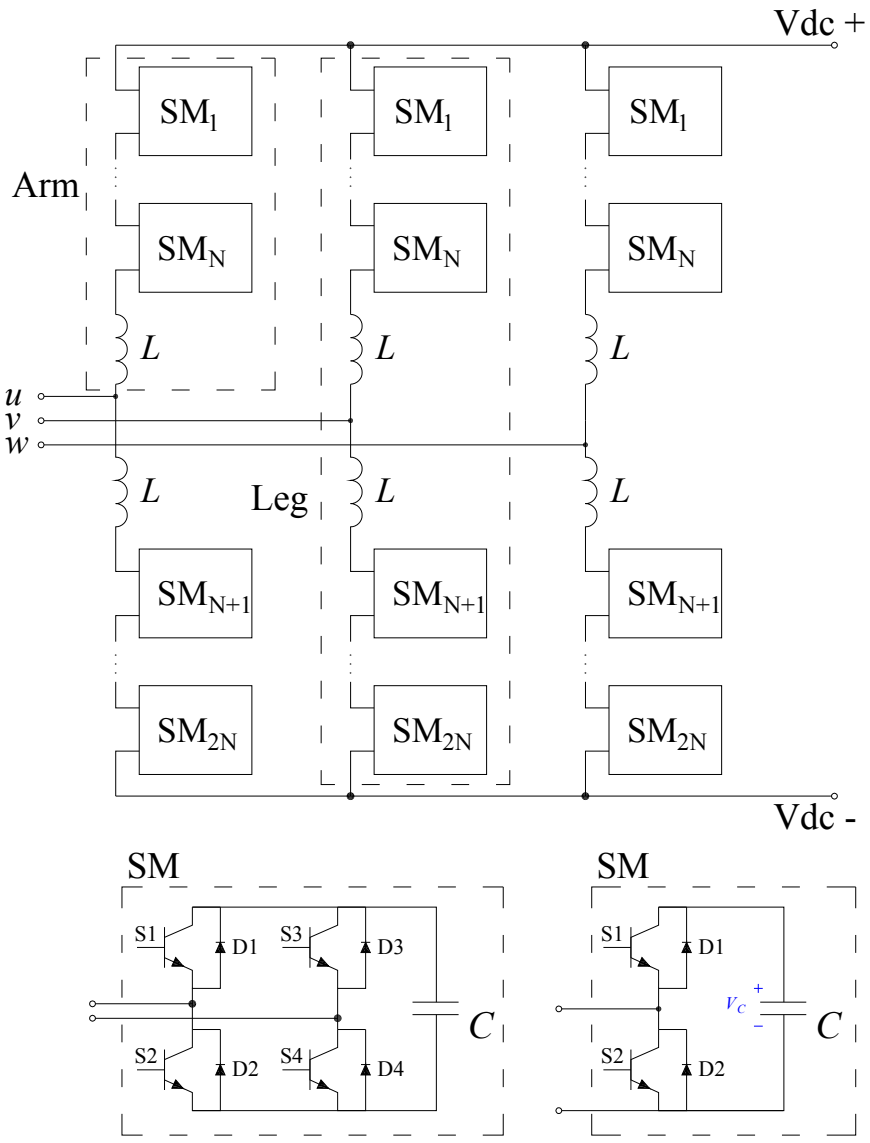


Fig. 1-3. Circuit Diagram of an MMC

The half-bridge (chopper cell) configuration is the most popular SM for MMCs, due to its lowest number of switches, compared with other configurations, which yields the lowest switch

loss, the lowest cost and an easier control and manufacturing process [17]. Therefore, MMCs comprising half-bridge SMs have found more industrial applications[16]. This thesis first focuses on control and modulation of MMCs with half-bridge converters. Later, the applications of this type of MMC as the input stage of solid state transformers is investigated.

1.4.1.2 Modulation Strategies

Fundamental frequency switching techniques are well developed for multilevel converters [29]. These modulation techniques are adopted to MMCs as well [30-32]. The Selective Harmonic Elimination (SHE) PWM has a mathematical approach to eliminate selected low order harmonics from the output line voltage of the converter [33, 34]. By employing this technique, a set of equations should be solved to find the required switching angles. This process could be time consuming if the number of switching angles is high. To make this process feasible for high number of switching angles, these switching angles are calculated in advance for each modulation index and then they are stored in a look-up table [34]. A simpler fundamental switching modulation technique, called the Nearest Level Control (NLC) modulation technique is proposed in literature [35-37]. In this modulation technique the nearest level to the reference voltage is chosen as the output level of the converter voltage. This modulation technique is easy to implement and requires low level of computational power.

Several multilevel PWM techniques are proposed for multilevel converters. These techniques are also applicable to MMCs. Carrier-Disposition PWM techniques (CD-PWM) [38] are well known among these modulation techniques. In this group of modulation techniques, several identical triangular waveforms are used. Each of these triangular waveforms has a different shift from the zero voltage level. The CD-PWM includes Phase Disposition (PD), Phase Opposition

Disposition (POD), and Alternative Phase Opposition Disposition (APOD) modulation techniques. The carrier waveforms in these modulation techniques are shown in Fig. 1-4.

The CD-PWM techniques are applied to the MMC in [39]. A performance comparison of these CD-PWM techniques, including the total harmonic distortion (THD) of the output voltage, is then presented. It is subsequently concluded that "the carrier disposition methods are not suited for the control of the MMC, resulting in significant levels of THD both in the output voltage and current waveforms, creating low order harmonics due to capacitor voltage unbalance, and large currents flowing through the phase-legs" [39]. The capacitor voltage balancing is not easily achieved with the aforementioned modulation techniques due to the fact that in these modulation techniques each carrier signal corresponds to one of the SMs of a multilevel converter. Since the characteristics and states of SMs are different, the problem of dynamic voltage balancing among the SMs' DC capacitors arises.

In the Phase-Shifted Carriers (PSC) PWM technique the triangular waveforms are shifted in time. Compared to other CD-PWM techniques, this technique has found more research interest in modulating multilevel converters due to its symmetry. A modified PSC-PWM technique is proposed in [35] which tries to balance the capacitor voltages. We will discuss this technique in the next section. This research focuses on application of the modified PSC-PWM technique. Moreover, in the proposed modulation technique, the PSC modulator can be replaced by other CD modulators without any performance degradation.

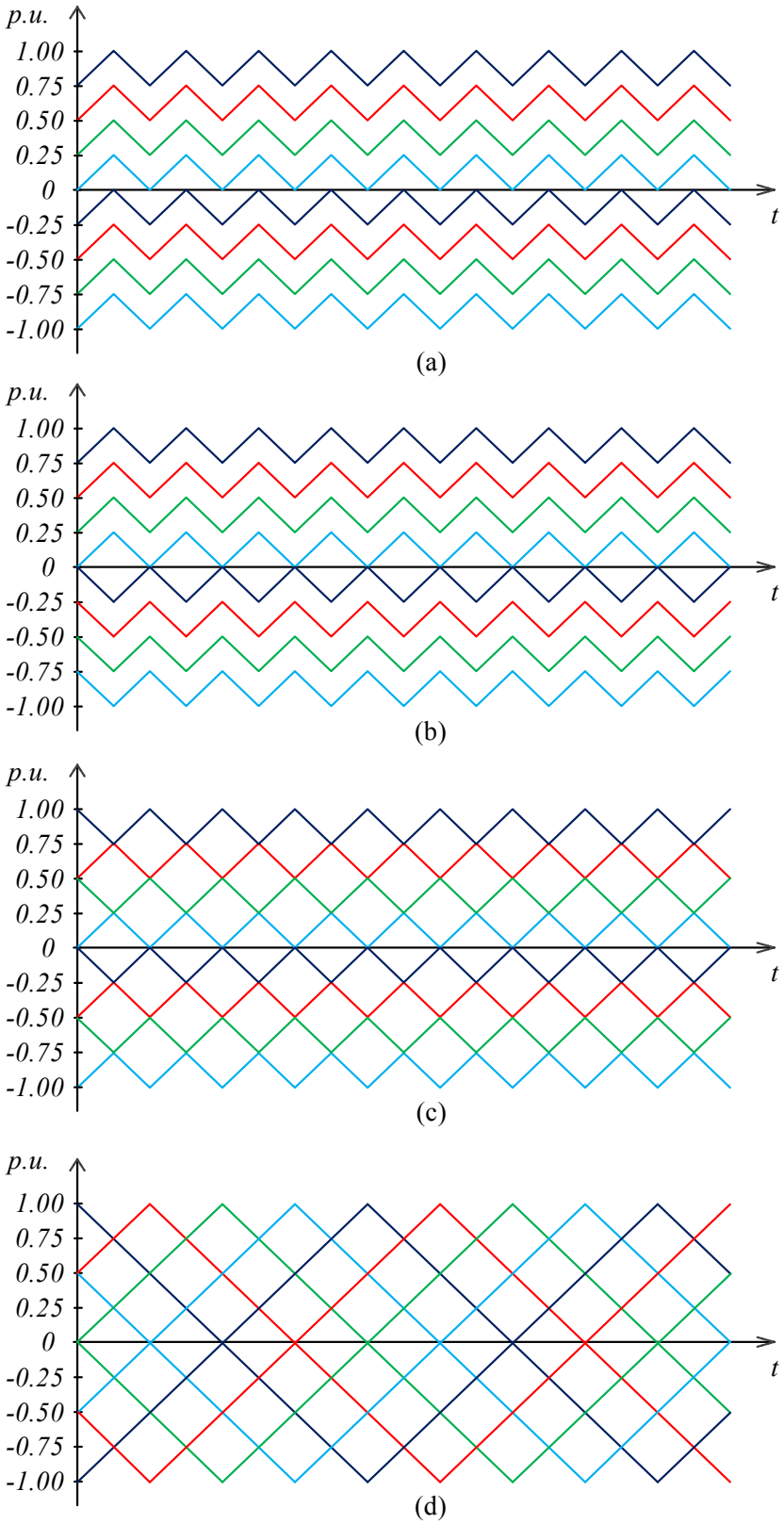


Fig. 1-4. Multilevel Carrier Waveforms a) PD, b) POD, c) APOD, d) PSC

1.4.1.3 Capacitor Voltages Balancing

MMCs, like any other multilevel converters, require additional controllers to balance the capacitors' voltages. Different voltage balancing techniques are proposed in literature [27, 32, 40-42].

A solution to the capacitor voltage balancing issue in an MMC modulated by PSC-PWM technique is presented in [18, 43]. In this technique a minor and a major voltage control loops are used to produce individual voltage references for each capacitor. These papers, however, do not provide documented results to justify the validity of the proposed method under the transients.

To tackle the problem of capacitor voltage balancing, a modified PSC-PWM technique with a voltage balancing algorithm is proposed in [35]. In this method, the carrier signals do not correspond to individual SMs; instead, they are used to assign the number of SMs in the on-state in each arm. Afterward, a capacitor balancing algorithm determines the modules to be turned on. This algorithm is discussed in [35]. A similar approach is proposed in [11], where PD-PWM is used as the modulation scheme.

1.4.2 Solid State Transformer

As mentioned before, a Solid State Transformer, also known as a Power Electronic Transformer (PET), an Electronic Power Transformer (EPT), and an Intelligent Universal Transformer (IUT) is an alternative to the Line-Frequency Transformer (LFT), and is able to convert electric power. It is actually a smart plug-and-play interface for exchanging electric power among its various terminals [3].

An LFT, working at low frequency of 50 or 60 Hz, has a bulky and heavy magnetic core. Operating at medium frequency is an approach to decrease the size and weight of a transformer. SSTs have first been introduced to decrease the size and weight of transformers through high operating frequency [44]. In 1970, GE introduced the concept of a high frequency link converter called as electronic transformer [45]. This became the basis for SSTs based on direct AC/AC converters. This initial work was followed by the United States Navy in 1980 with an AC/AC buck converter [46] and in 1995 by the Electric Power Research Institute (EPRI) with a similar SST concept [47, 48]. A solid state transformer called Intelligent Transformer (ITR) was proposed in 1996 [49]. The overall efficiency of this transformer was reported to be about 80% and this low efficiency is viewed as a major disadvantage of this transformer. In 1999, ABB Power proposed a solid state transformer which consists of input modules in series at HV side, isolation modules, and a converter at LV side. Each input module comprises an uncontrolled rectifier which lacks the bi-directional power flow feature. The number of series input modules depends on the input voltage level and the voltage ratings of the semiconductors and the capacitor. An extensive research on Intelligent Universal Transformer (IUT) has been conducted by EPRI since 2002 [50-53].

An SST consists of power electronic converters, High-Frequency (HF) transformer(s) and auxiliary and control circuits. SSTs perform physical power routing and voltage step-down functions. The HF transformer performs the step-up/down function and the isolation task, whereas the power electronic converters provide extra features to SSTs. Such features include voltage and power flow regulation, DC voltage provision, power factor compensation, and fault and harmonic isolation [4-6]. Further, the weight and volume of an SST can be up to three times

less than those of an LFT with same power rating, owing to the use of high frequency transformer [7].

All of the SST configurations provide HVAC and LVAC terminals which can interface AC grids. Besides, some of the proposed topologies provide an LVDC terminal to interface DC sources, loads and storage devices. However, most of the current SSTs lack an HVDC terminal and, therefore, they are not applicable to DC distribution grids.

1.4.2.1 Solid State Transformer Topologies

Many configurations are proposed for SSTs in the literature [4, 14, 54]. Approaches to classify current SST topologies and comparing them according to their application and features are introduced in [7, 14, 55]. According to these classifications, four basic topologies can be distinguished:

a. Single-stage topology with direct AC-to-AC conversion,
b. Two-stage topology with an LVDC link,
c. Two-stage topology with an MVDC link,
d. Three-stage topology with both LVDC and MVDC links.

These topologies are shown in Fig. 1-5 and are described below.

The single stage topology is the earliest SST topology introduced in [45]. This topology includes a direct AC/AC or a matrix converter, [56], and does not provide any DC link. Lack of providing DC links is viewed as a drawback since a DC link makes an SST capable of providing ancillary services such as reactive power compensation to the grid. Moreover, with the consideration of DC nature of many key components in a smart-grid, such as photovoltaic

panels, storage devices, fuel cell and DC-type loads, SST topologies with LVDC link have received more attention recently. Despite their limited functionalities, single-stage SSTs require simple control, and the switch count and the switch losses are low compared to other topologies [57].

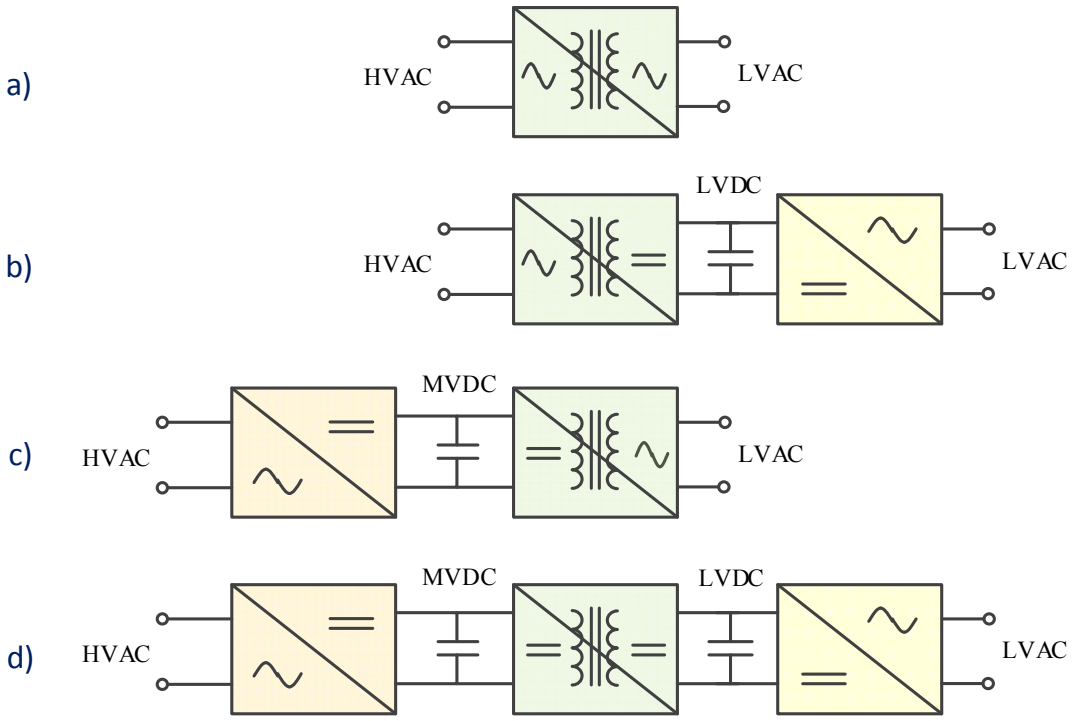


Fig. 1-5. SST configurations: a) single-stage AC-AC, b) two-stage with LVDC link, c) two-stage with MVDC link and d) three-stage with LVDC and MVDC links.

The SST topologies that provide an LVDC link include two-stage topology with LVDC link and three-stage topology with both MVDC and LVDC links.

The two-stage SST with an LVDC link facilitates the integration of DC sources and storage devices. It can also provide additional functionalities such as power factor correction. However, due to the lack of an MVDC link, the LVDC link has large 120 Hz (or 100 Hz) ripples. Use of a larger capacitor narrows the bandwidth of the voltage control loop [57].

While LVDC link in an SST provides the possibility of supplying ancillary services to an LVAC network and interactions with low-voltage DC generators, storage equipment, and load, the application of the MVDC link is limited to providing the ancillary services to the HVAC grid.

Nowadays, the three-stage SST topology is considered as the best solution for the requirements of future networks [14]. A three-stage SST topology has two DC links and hence can provide ancillary services to the both LVAC and HVAC grids [7, 14]. This type of SST provides all of the functions that are desirable for an SST [57]. However, the main drawback of this SST topology is its large number of components [57].

Fig. 1-6 shows the power circuit design of a three-stage SST. It is obvious that the voltage level of the MVAC port and MVDC link are limited to the voltage withstand of the switches. Assuming the state-of-the-art IGBTs, which have a voltage withstand of 6.5 kV, the MVDC and MVAC voltage levels are usually limited to 4 kV and 3 kV, respectively. These voltage levels are not high enough to allow connection to a typical AC and/or DC distribution networks. Although [3] claims that by using 15 kV SiC MOSFETs, the SST topology of Fig. 1-6 can be used in the existing distribution systems, this type of MOSFET is yet under development.

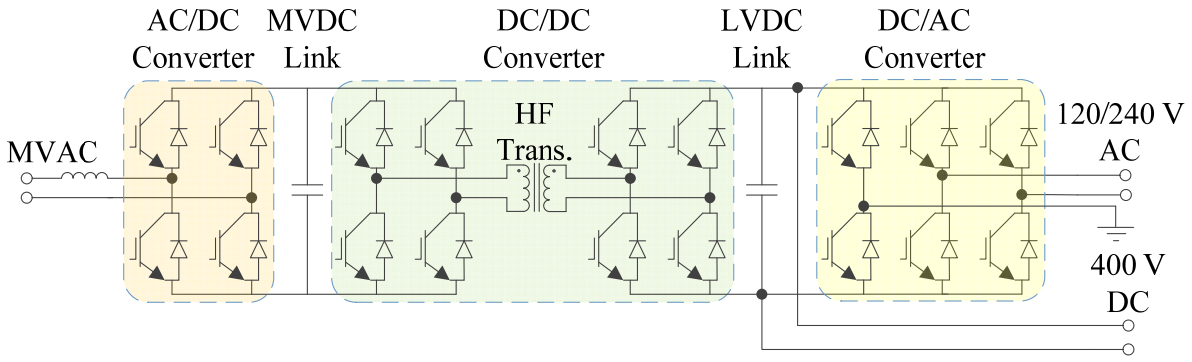


Fig. 1-6. Power circuit of a three-stage SST

Fig. 1-7 shows a series-connected input SST [7] as a potential solution for enabling an SST to interface to a distribution grid. Nevertheless, the MVDC voltage level limit in this configuration is the same as that in the single-module input SST topology, shown in Fig. 1-6, assuming the same switching devices. The first-stage converter in Fig. 1-7 is a cascaded H-bridge multilevel converter.

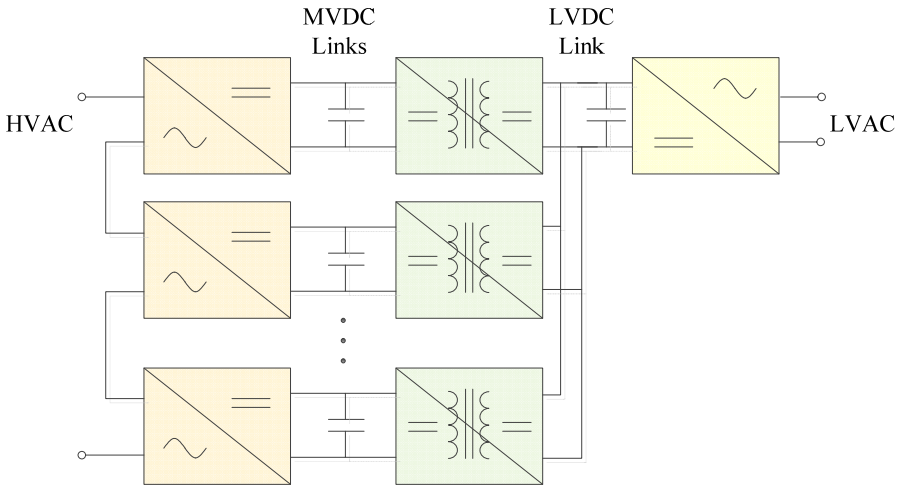


Fig. 1-7. A modular three-stage design of the SST with a common inverter

As mentioned before, this configuration is unable to provide an HVDC terminal. Other types of multilevel converters may as well be utilized as the input stage of an SST [14, 58, 59]. Using a diode-clamped multilevel converter as the input stage of an SST, as reported in [14], could provide an HVDC terminal. However, this type of SST suffers from the drawbacks of a diode-clamped converter, among which are the difficulty to expand to higher voltage levels and to balance the capacitors' voltages [60].

1.5 Original Contributions

The main contribution of this thesis to the field of power engineering is proposal of application of an MMC at the first (and second) stage(s) of an SST.

In the first part of this research, MMCs are investigated and as an original contribution, a modulation and control scheme is proposed, which uses the traditional PSC modulation with 2N carriers along with the capacitor voltage sorting control. This will result in a control scheme which presents output voltage and current with lower harmonic contents, while the capacitors voltages sorting technique keeps the capacitors voltages balanced. Since the proposed modulation offers a better harmonic distortion level with shifted harmonics, a lower switching frequency can be used with this modulation which will result in lower switching losses.

In the second part of this thesis, as original contributions, three SST configurations are proposed in which the MMC is used as the first (and second) stage converter. Compared to the existing SSTs, use of MMCs in the proposed SSTs provides high level of modularity and scalability to these configurations. Therefore, the configurations can be used in medium- and high-voltage applications. Furthermore, the proposed schemes provide HVDC terminal which can interface to an HVDC grid. This enables the proposed SSTs to be used in both AC and DC grids. These SSTs can even be interconnected to both DC and AC grids at the same time.

1.6 Methodology

To demonstrate the effectiveness of the control scheme proposed in Chapter 2, and the SST configurations proposed in Chapter 3, time-domain simulations have been conducted on detailed switched models of an MMC and SSTs using MATLAB/Simulink software package.

To compare the THD and harmonic spectrum of the proposed control scheme in Chapter 2 to that of the conventional controls, FFT analysis has been utilized.

To calculate the loss and efficiency of the proposed modulation scheme in Chapter 2, the equations describing the switching and conduction losses have been implemented in MATLAB. The specifications of IGBT switches obtained from manufacturers' datasheets are then used to calculate the loss distribution inside the converter in different modulation schemes.

To provide external validation of the results obtained in Chapter 2, the results have been reproduced using a real-time simulator. The real-time simulator used is an RT-LAB system from Opal-RT Technologies. RT-LAB is an integrated hardware and software system with multi-core processors. The real-time kernel of the RT-LAB simulator used for this study is Red Hat.

1.7 Thesis Summary

Chapter 2: Modular Multilevel Converter

This Chapter presents a background on the principles of operation and control of MMCs. A modulation scheme is further proposed which increases the number of the levels in the output voltage of an MMC and reduces the harmonic content in the output voltage and current, while maintaining the balance of the capacitors' voltages. Then, the effect of the proposed modulation

scheme on the converter efficiency is evaluated. The conventional and proposed modulation schemes are simulated in MATLAB/Simulink. The results are validated through Real-time simulation studies.

Chapter 3: Design of MMC-based Solid State Transformers

In this Chapter, three SST configurations are proposed in which an MMC is employed in the first (and second) stage(s). These SSTs are scalable to high voltage levels and provide DC terminals in addition to the commonly provided terminals. The performances of the proposed configurations are evaluated using simulation studies.

Chapter 4: Summary and Future Work

This chapter concludes the thesis and summarizes the main achievements of this thesis. Also, future possible research directions are outlined.

Chapter 2 - Modular Multilevel Converter

In this chapter, we first provide a short background on MMC operation principle, its circuit analysis and design, and its control loops. Then, we elaborate on the proposed scheme and present the results of simulations. Finally, we provide a validation for the proposed scheme using a real-time simulator.

2.1 Background

2.1.1 MMC Operating Principle

Fig. 1-3 shows the configuration of an MMC comprising half-bridge SMs. The operation principle of MMCs is as follows. At any moment only one of the switches in any of the MMC SMs is on. Therefore, depending on the switches state and the current direction, the SM is in one of the four possible states indicated in Fig. 2-1. If the upper switch *S1* in this figure is on, the SM is either in states 1 or 2 depending on the direction of the corresponding arm current. The current in state 1 charges the capacitor of the SM, while it discharges this capacitor in state 2. The SM output voltage in either of these two states is the same as the voltage of its capacitor. If the SM is in either state 1 or 2, it is called to be in the "on" state. Likewise, if *S2* is on, the SM is either in state 3 or 4. The capacitor voltage in these states remains constant and the SM output voltage is almost zero. If none of the switches are turned on, the SM would be in state 1 or 4 depending on

the direction of the current. In this case, the output voltage of the SM depends on the direction of the current. Therefore, this mode of switching is avoided. If an SM is in either state 3 or 4, it is called to be in the “off” state, or “bypassed”.

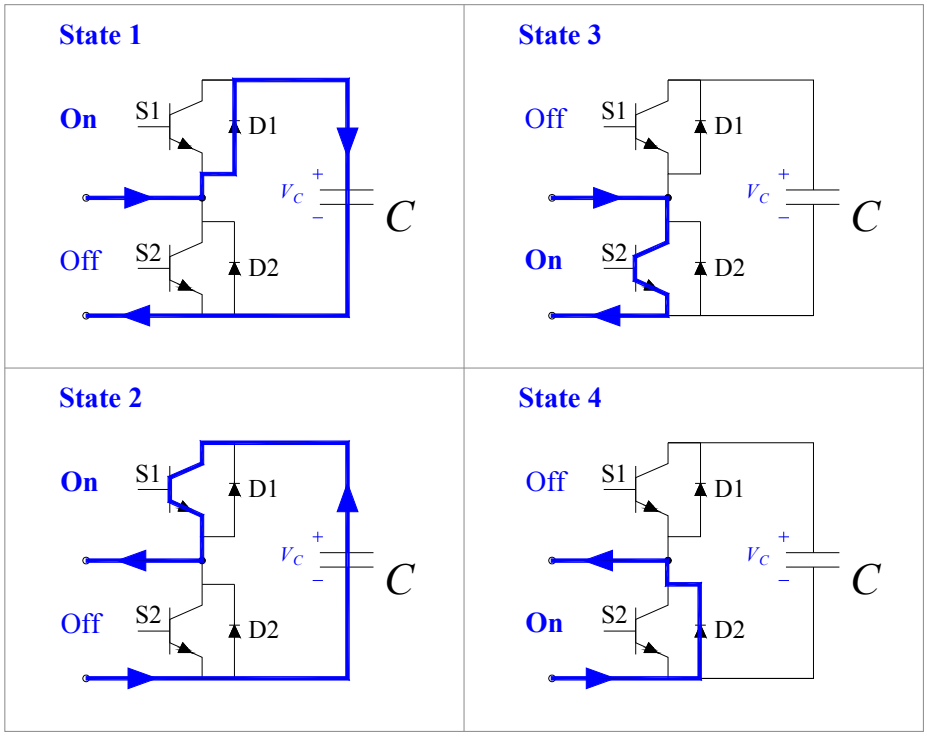


Fig. 2-1. States and the current distribution inside the SM

The reference voltage of the capacitors of the SMs is the overall DC voltage divided by the number of SMs in one arm. Assuming two SMs in each arm of a single-phase MMC, as shown in Fig. 2-2, the reference voltage of each capacitor is $V_{DC}/2$.

In basic operation of an MMC, the number of SMs that are in the on state in each leg at any moment is equal to number of SMs of one arm (i.e. half of the $2N$ SMs of a phase leg). In the MMC of Fig. 2-2, if two SMs in the lower arm are in the on state and the two SMs in the upper arm are in the off state, the output voltage is $+V_{DC}/2$. On the contrary, if the two SMs in the

upper arm are in the on state and the two SMs in the lower arm are in the off state, the output voltage is $-V_{DC}/2$. If one SM in each arm is in the on state and the other one is in the off state, the output voltage would be zero. Therefore, this converter can produce three voltage levels at the output. These voltage levels are shown in Fig. 2-3. Generally, an MMC with N SMs in each arm can generate a phase voltage waveform which has $N+1$ levels.

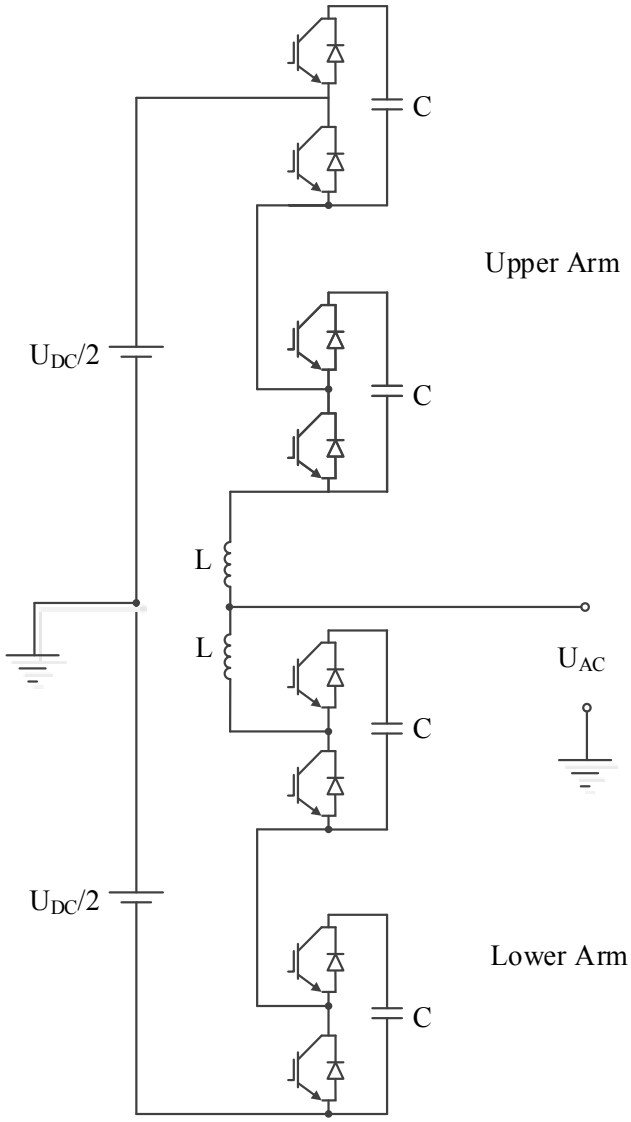


Fig. 2-2. A single-phase MMC with two SMs in each arm

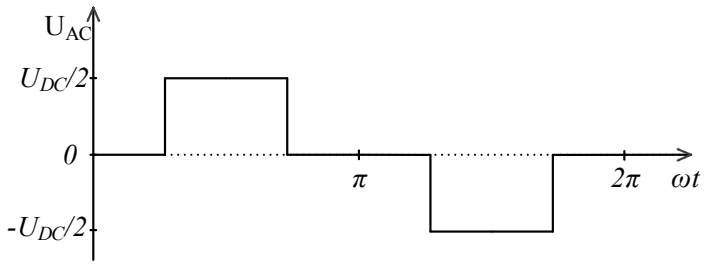


Fig. 2-3. A 3-level output of a single-phase MMC (*N=2*)

This principle of operation can be extended to MMCs with more SMs. As the number of SMs increases, there are more redundant switching patterns for each output voltage level. To clarify, assume that in a moment only one SM in an arm is supposed to be at the on state and the rest are off. In this situation, the number of choices for the SM in the on state is equal to the number of SMs in that arm. The only voltage levels with unique switching patterns are the highest and the lowest voltage levels, i.e. $+U_{DC}/2$, $-U_{DC}/2$. The redundant switching patterns can be used to balance the voltages of the capacitors in the converter, which will be discussed later.

2.1.2 General Modeling

A single-phase equivalent circuit of an MMC is shown in Fig. 2-4. Subscript u denotes the phase u of a three-phase converter and all the discussions conducted on this phase are valid for the other phases. U_{dc} represents the DC bus voltage, and the arms voltages generated by the cascaded SMs are expressed as u_{Uu} and u_{Lu}, where the subscripts U and L denote the upper and lower arms, respectively. The arm inductance and equivalent resistance are presented by L and R, respectively.

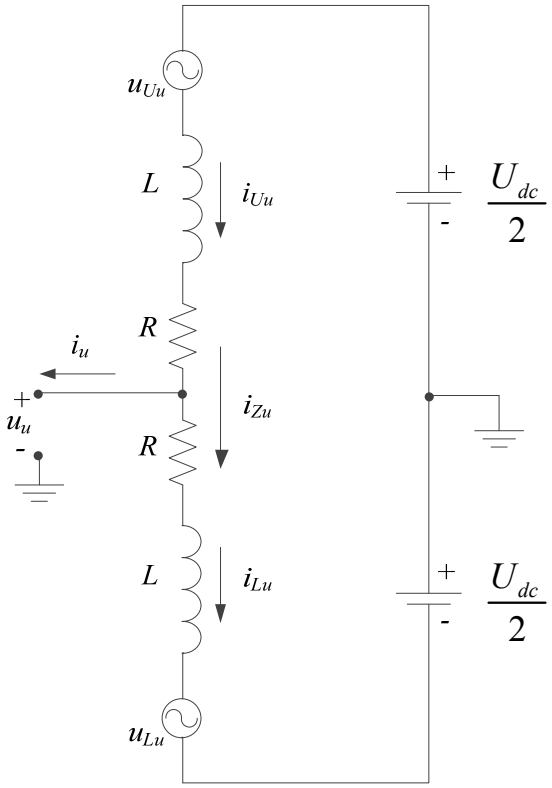


Fig. 2-4. Single-phase equivalent circuit of the MMC

The principles of the operation of an MMC are given in [35, 61]. The upper and lower arms currents, i.e. i_{Uu} and i_{Lu}, can be expressed as

$$i_{Uu} = i_{Zu} + \frac{i_u}{2} \tag{2-1}$$

$$i_{Lu} = i_{Zu} - \frac{i_u}{2} \tag{2-2}$$

where i_u is the AC side current and i_{Zu} is regarded as the inner difference current of phase u, which flows through both the upper and lower arms and is given as

$$i_{Zu} = \frac{i_{Uu} + i_{Lu}}{2} \tag{2-3}$$

According to [35], the MMC can be characterized by the following equations:

$$u_{Zu} = \frac{1}{2}[U_{dc} - (u_{Uu} + u_{Lu})] = \frac{Ldi_{Zu}}{dt} + Ri_{Zu} \quad (2\text{-}4)$$

$$u_u = e_u - \frac{R}{2}.i_u - \frac{L}{2}.\frac{di_u}{dt} \quad (2\text{-}5)$$

where u_{Zu} is the inner unbalance voltage and e_u indicates the inner emf generated in phase *u,* which is expressed as

$$e_u = \frac{u_{Lu} - u_{Uu}}{2} \quad (2\text{-}6)$$

2.1.3 MMC Design Criteria

Reference [62] presents the procedure of an MMC converter's dimensioning, including the voltage rating, the required size of the capacitors in the cell, and the inductance of the arm choke.

By knowing the voltage rating of the distribution grid, the DC bus voltage level for an MMC can be chosen. In order to prevent over-modulation, the HVDC bus voltage should be higher than the peak of the HVAC voltage; however, the DC bus voltage should not be much higher than the peak of the HVAC voltage, since it will decrease the modulation index, and therefore, introduces higher harmonic content in the converter's output voltage and current.

Additionally, by knowing the blocking voltage of an IGBT, a safety factor can be used to determine the capacitor voltage. IGBT manufactures suggest that the highest voltage an IGBT has to block should not exceed 80% of the collector-to-emitter voltage (V_{CES}) rated voltage, and the DC voltage should not exceed 50 to 60% of the V_{CES} rated voltage [63]. The common voltage ratings of an IGBT are 1200V, 1400V, 1700V, 3300V and 6500V. Using the nominal voltage of

the DC bus in an MMC, the number of modules in each arm can be calculated by selecting one of the IGBT modules and applying the required safety factor as follows:

$$n \geq \frac{U_{dc}}{\eta V_{CES}} \tag{2-7}$$

2.1.3.1 SM capacitance

Reference [64] elaborates the power calculations in an MMC using the assumption that the arms' voltages and currents are purely sinusoidal, and the arm capacitors are always kept balanced. It is then concluded that for an acceptable level of voltage ripple ε, the required SM capacitance can be obtained from (2-8).

$$C \geq \frac{\Delta W_{SM}}{2.\epsilon.\overline{U_c}^2} \tag{2-8}$$

where $\overline{U_C}$ is the average voltage across each capacitor and is equal to the average voltage of the DC bus divided by the number of modules in each arm ($\overline{U}_c = \frac{U_d}{n}$). Parameter ΔW_{SM} presents the energy difference in each capacitor during one period of the fundamental frequency and is calculated as [64]

$$\Delta W_{SM} = \frac{2}{3}.\frac{P_S}{k.n.\omega}.\left(1 - \left(\frac{k.cos(\phi)}{2}\right)^2\right)^{3/2} \tag{2-9}$$

where P_S and φ denote the load apparent power and angle respectively. ω is the nominal angular velocity and *k* is the ratio of the output phase voltage peak to the half of the DC bus voltage, as expressed in (2-10).

$$k = \frac{\hat{u}_a}{U_{dc}/2} \tag{2-10}$$

Eq. (2-9) is rewritten in [62] as

$$\Delta W_{SM} = \frac{\hat{\imath}_a}{\omega}.\frac{U_{dc}}{2n}.\left(1 - \left(\frac{\hat{u}_a.\cos(\phi)}{U_{dc}}\right)^2\right)^{3/2} \tag{2-11}$$

Considering that the voltage variations of SMs in the upper and the lower arms of an MMC are not "synchronous", an accurate model for calculating the voltage variation waveform in each arm's SM is presented in [65]:

$$\begin{aligned} u_C(t) = \sqrt{\frac{2W_q(t)}{N.C}} = \sqrt{\frac{2\left(\overline{W_q} + \Delta W_q(t)\right)}{N.C}} = \sqrt{\frac{2\overline{W_q}}{N.C}}\left(1 + \frac{\Delta W_q(t)}{\overline{W_q}}\right)^{0.5} \\ \cong \sqrt{\frac{2\overline{W_q}}{N.C}}\left(1 + \frac{0.5\,\Delta W_q(t)}{\overline{W_q}}\right) \end{aligned} \tag{2-12}$$

where,

$$\overline{W_q} = N\frac{C.U_c^2}{2} = N\frac{C.\left(\frac{U_{dc}}{N}\right)^2}{2} \tag{2-13}$$

$$\Delta W_q(t) = \frac{P_{dc}}{6\omega}\left[\frac{sin(2\omega t + \phi)}{2\,cos\,\phi} - \frac{2\,cos\,\omega t}{mcos\phi} + m\,cos(\omega t + \phi)\right] \tag{2-14}$$

$$m = \frac{3}{2}\frac{i_m}{I_{dc}} \tag{2-15}$$

In the above equations $W_q(t)$ is the energy stored in the capacitors of one arm. U_{dc}, I_{dc} and P_{dc} are the values of the DC voltage, current and power, respectively. i_m denotes the peak of the output AC current. ϕ is the load angle, and N is the number of SMs in each arm. Using the above

equations, the voltage ripple in each phase of the converter is derived. It is concluded that the voltage ripples obtained by the approximate model of [64] is smaller than the results by the accurate model.

2.1.3.2 Arm Inductance

Reference [66] describes two distinctive functions of the arm inductors of an MMC: suppressing the circulating current and limiting the fault current rise rate. For each of the functions, the required arms' inductance is calculated.

The positive arm current is presented as:

$$i_{pa}(t) = \frac{1}{3} I_{dc}(1 + m.sin(\omega t + \phi)) + I_{2f} cos(2\omega t + \phi) \quad (2\text{-}16)$$

where I_{2f} is the peak value of the double-fundamental-frequency circulating current. The equation to design the arm inductance for a given maximum circulating current peak value is derived as [66]:

$$L \geq \frac{1}{8\omega^2 . C . \bar{U}_C} \left(\frac{U_{dc} . I_{dc}}{3 I_{2f} . cos\phi} + U_{dc}\right) \quad (2\text{-}17)$$

Reference [62] presents another equation for required amount of arm inductance based on a maximum ripple current in the circulating current:

$$L \geq \frac{0.25 U_{c,max}}{n . f_c . \Delta i_{L,max}} \quad (2\text{-}18)$$

In this equation, $U_{c,max}$ is the maximum voltage of an SM capacitor; $\Delta i_{L,max}$ is the maximum voltage ripple of the circulating current; and f_c is the switching frequency of each SM.

Reference [66] elaborates that the other function of the arm inductor is limiting the fault current rise rate. For a given fault current rise rate α, the required arm inductance can be calculated as

$$L \geq \frac{U_{dc}}{2\alpha} \tag{2-19}$$

The required value for the arm inductance is the maximum of the values calculated by (2-17), (2-18) and (2-19).

2.1.4 AC side and DC side Control of an MMC

According to (2-5), the AC current i_u can be controlled directly by regulating the control variable e_u. As a result, the widely used current vector control scheme based on *dq* coordinates [67] can also be adopted in MMCs. In addition to this control, due to the floating capacitors in MMCs, some capacitor voltage control strategies should be utilized.

The purpose of averaging control is to keep the average voltage of the capacitors of one leg of an MMC at the reference value, and it does not guarantee balanced capacitors voltages. According to (2-4), the inner difference current $\boldsymbol{i_{Zu}}$ can be directly controlled by regulating the unbalance voltage $\boldsymbol{u_{Zu}}$. $\boldsymbol{i_{Zu}}$ conveys the power from the DC bus to SMs. Controlling the average voltage of the capacitors of phase *u* can be achieved by controlling the unbalance voltage $\boldsymbol{u_{Zu}}$ as illustrated in Fig. 2-5. The parameters of PI controllers may be set by trial and error or by using a simplified linear model of the converter.

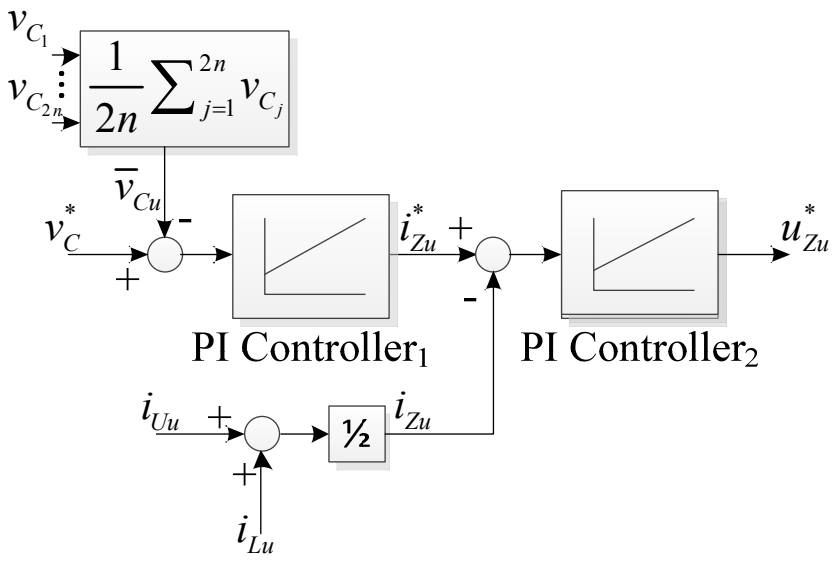


Fig. 2-5. Block diagram of averaging control unit

2.1.4.1 Phase-Shifted Carriers Pulse Width Modulation and Capacitors' Voltages Balancing

As described in chapter 1 several modular modulation schemes are proposed in literature. The Phase-Shifted Carriers Pulse Width Modulation (PSC-PWM) scheme showed better performance compared with other carrier disposal PWM schemes. The PSC-PWM technique is employed on an MMC in [18, 43]. Since every triangular waveform in the PSC-PWM technique is assigned to one of the SMs in the MMC, *2N* triangular waveforms are needed. By using a single reference voltage for one leg of the converter, there is no freedom to balance the capacitors voltages. This will result in unbalanced voltages across capacitors in a leg of the converter, which will effects the converter performance. In order to balance the capacitors voltages, each capacitor will be assigned an individual reference voltage. These reference waveforms are regulated by individual controllers which try to keep the corresponding capacitors' voltages at a reference level. This technique, however, is not fast enough to recover a capacitor voltage after a fault in the corresponding SM. Further, it requires *2N* controllers and *2N* reference signals for controlling one leg of the converter, which complicates the control scheme.

Reference [35] proposes a modified PSC-PWM scheme. In this modulation scheme, as shown in Fig. 2-6, *N* triangular waveforms and one reference voltage are used to modulate an MMC. The triangular carriers are each phase shifted by an angle of *360/N*. The main difference of this modulation scheme with the common PSC-PWM is that in the proposed modulation scheme triangular carriers are not assigned to individual SMs. The modulator in this scheme only provides the number of SMs in an arm in on state. This number, N_U, for an MMC with four SMs in each arm is shown in Fig. 2-6. If one modulator is employed for a phase of an MMC, the number of SMs in the on state in the upper (lower) arm is defined by the modulator; while, the number of SMs in the on state in the lower (upper) arm is equal to N - N_U. In other words, the total number of SMs in the on state in one leg is always *N*. Using the modified PSC-PWM technique, the specific SMs to be turned on are not specified by the modulator, but by another control scheme which tries to balance the capacitors' voltages.

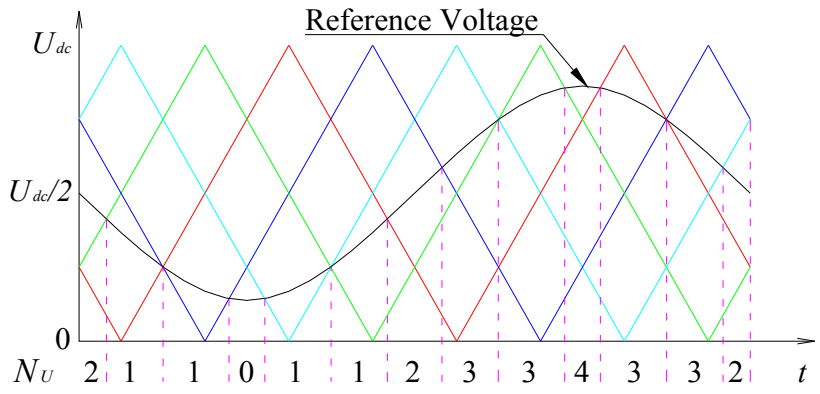


Fig. 2-6. PSC-PWM method

As discussed in chapter 1, the capacitors' voltages balancing is one the issues in controlling an MMC. In the modified PSC-PWM modulation of [35], the modulator specifies the number of the SMs in the ON state. A capacitors' voltages sorting algorithm defines the specific modules to

be turned on. In order to explain this sorting algorithm, we first explain the SM states. Each SM in an MMC, as shown in Fig. 1-3, has an output voltage that is either equal to its capacitor voltage or zero. The SM states are illustrated in Fig. 2-1. It can be seen that when *S2* is in the on state, *i.e.* states 3 and 4, both the output voltage and the current passing through the capacitor are zero. Therefore, the capacitor voltage would be constant in these states. However, if *S1* is in the on state, the capacitor voltage will change due to the current passing through it. The capacitor voltage will increase in state 1, where the module current charges the capacitor, while decrease in state 2.

The voltage balancing algorithm proposed in [35, 68] works as follows:

- When the arm current has a direction that charges the capacitors in the SMs of an arm, the algorithm switches on SMs with the lowest capacitors' voltages and put them in state 1. The algorithm switches off those SMs with the highest capacitors' voltages and put them in state 3.
- When the arm current has a direction that discharges the capacitors in the SMs of an arm, the algorithm switches on SMs with the highest capacitors' voltages and put them in state 2. The algorithm switches off those SMs with the lowest capacitors' voltages and put them in state 4.

The overall switching algorithm, proposed in [35], is as follows:

1. The number of SMs to be in the on state in each of the arms is specified by the modulation scheme.

2. A sorting algorithm generates a list of the SMs of each arm in the ascending order with respect to their capacitor' voltages.
3. If the arm current is in a direction that charges the capacitors in an arm, the SMs of that arm to be switched on are selected from the top of the lists; While, If the arm current is in a direction that discharges the capacitors in an arm, the SMs of that arm to be switched on are selected from the bottom of the lists. The rest of the SMs in the arm are switched off.

2.2 Proposed Modulation and Control Scheme

The conventional PSC-PWM scheme with *2N* carriers, where each carrier signal corresponds to a predetermined SM in an MMC, as proposed in [18, 43] will generate a *2N+1* level output voltage waveform. However, since each triangular carrier corresponds to an individual SM, the capacitor voltage sorting algorithm cannot be employed. Therefore, the reference signal for each SM should be individually regulated by its corresponding controller to keep the capacitors voltages balanced. One can expect that this scheme is slower in balancing the capacitors voltages compared to the sorting algorithm, since no comparison is done among the capacitors voltages.

The modified PSC-PWM scheme proposed in [35], has a better performance in balancing the capacitors' voltages. However, since only *N* carrier signals are used in the modulator, the output phase voltage of the MMC has an *N+1* level waveform, although the converter has *2N* SMs in each phase. It is expected that since the output voltage in this modulation scheme has less number of levels compared to the PSC-PWM scheme with *2N* carriers, the harmonic content in the modified PSC-PWM scheme is higher.

In this work a modified control and modulation scheme is proposed which has a low level of harmonic content in the output voltage and current, while it offers an efficient capacitors' voltages balancing technique.

The modified PSC-PWM of [35] offers a good balancing technique by sorting the capacitors' voltages. However, it has only *N* triangular carriers. If two modulators each with *N* triangular carriers are used for the two arms in one phase of an MMC, it is possible to have *2N+1* levels in the output voltage. Therefore, in this work, two modified PSC-PWM modulators are employed for each phase of an MMC. Each modulator has *N* carrier signals phase shifted from each other by *360/N* degree. The carrier signals of one of the modulators must be shifted by *360/2N* degree with respect to the carrier signals in the other modulator. Each modulator specifies the number of SMs in the on state in the corresponding arm. Afterward, two capacitors' voltages balancing algorithms specify the individual SMs to be turned on in each arm of a phase.

Details of the proposed control scheme, which generates a *2N+1* level output voltage, while maintains the capacitors' voltages balanced, are shown in Fig. 2-7. The averaging control in this scheme generates a reference to keep the average voltage of the capacitors in each arm at the reference value. The voltage balancing blocks keep the voltages of the capacitors in each arm balanced by using the aforementioned sorting algorithm. The modulators' carrier signals and reference voltages are depicted in Fig. 2-8.

It is to be noted that in the proposed control and modulation scheme, the number of modules in the on-state in each leg is no longer constant and varies among the values of *N-1, N*, and *N+1,* as depicted in Fig. 2-8. This affects the circulating current, the consequence of which is discussed later.

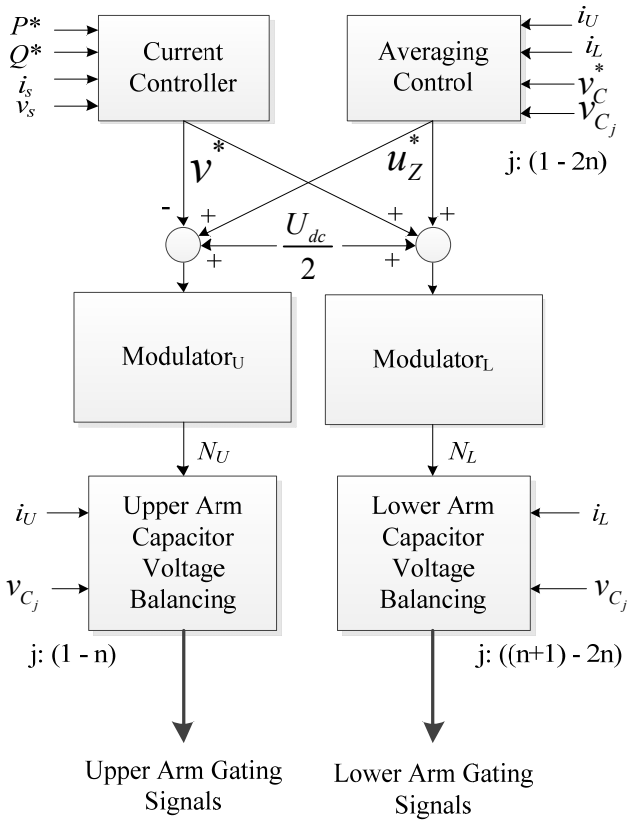


Fig. 2-7. Schematic diagram of the proposed control scheme

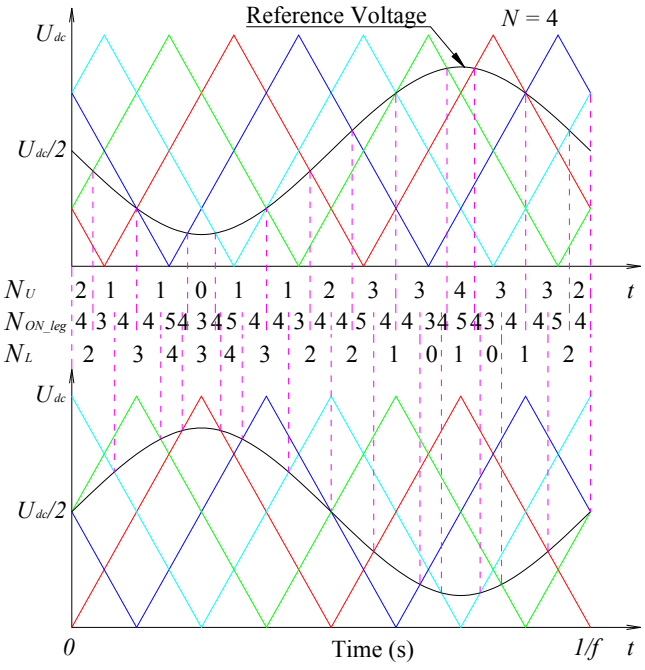


Fig. 2-8. The proposed modulation scheme

Table 2-1 shows the possible output voltages in a phase of an MMC with four SMs in each arm. It is assumed that all the capacitors are at v_c voltage level. This table shows that the modified PSC-PWM of [35] can only generate five output voltage levels (Inner EMF).

Table 2-1 The switching states, inner EMF, and inner unbalance voltage levels generated in an MMC employing proposed modulation scheme

Number of SMs in on-state in upper arm	**Number of SMs in on-state in lower arm**	**Number of SMs in on-state in the leg**	**Inner EMF**	**Inner unbalance voltage u_{zu}**	**Available in modified PSC-PWM scheme of [35]**
0	4	4	+2.v_c	0	√
0	3	3	+1.5.v_c	+0.5.v_c	--
1	4	5	+1.5.v_c	-0.5.v_c	--
1	3	4	+1.v_c	0	√
1	2	3	+0.5.v_c	+0.5.v_c	--
2	3	5	+0.5.v_c	-0.5.v_c	--
2	2	4	0	0	√
2	1	3	-0.5.v_c	+0.5.v_c	--
3	2	5	-0.5.v_c	-0.5.v_c	--
3	1	4	-1.v_c	0	√
3	0	3	-1.5.v_c	+0.5.v_c	--
4	1	5	-1.5.v_c	-0.5.v_c	--
4	0	4	-2.v_c	0	√

The averaging control block shown in Fig. 2-7 employs PI controllers which are tuned based on the controllers of [18, 43] . In this chapter, the controller design procedure is not presented as we are only studying steady-state behavior of the converter.

2.3 Simulation Results

In order to validate the effectiveness of the proposed modulation and control scheme simulation studies are performed on MATLAB/Simulink software package. The modulation scheme of [35] and the proposed modulation in this thesis are implemented on a three-phase MMC with four modules in each arm.

Table 2-2 summarize the circuit parameters used for simulation using MATLAB/Simulink software.

Table 2-2 Circuit Parameters for modeled MMC

Parameter	Symbol	Quantity
Rated RMS voltage	V	4.16 kV
Rated active power	P	1 MW
Rated RMS current	I	142 A
Rated frequency	f	60 Hz
Common DC voltage	E	7 kV
SM capacitance	C	2400 μF
Rated capacitors voltage	V_C	1.75 KV (= 7 kV/4)
Unit capacitance constant [43]	H	88 ms
Buffer inductance	L	2.4 mH (5.2%)
Load inductance	l	8.9 mH (19.4%)
Carrier frequency	f_C	300 Hz
Output switching frequency	$N.f_C$	1200 Hz

Fig. 2-9 shows the output voltages and currents of the MMC in the inverter mode of operation, when the modulation scheme of [35] is used.

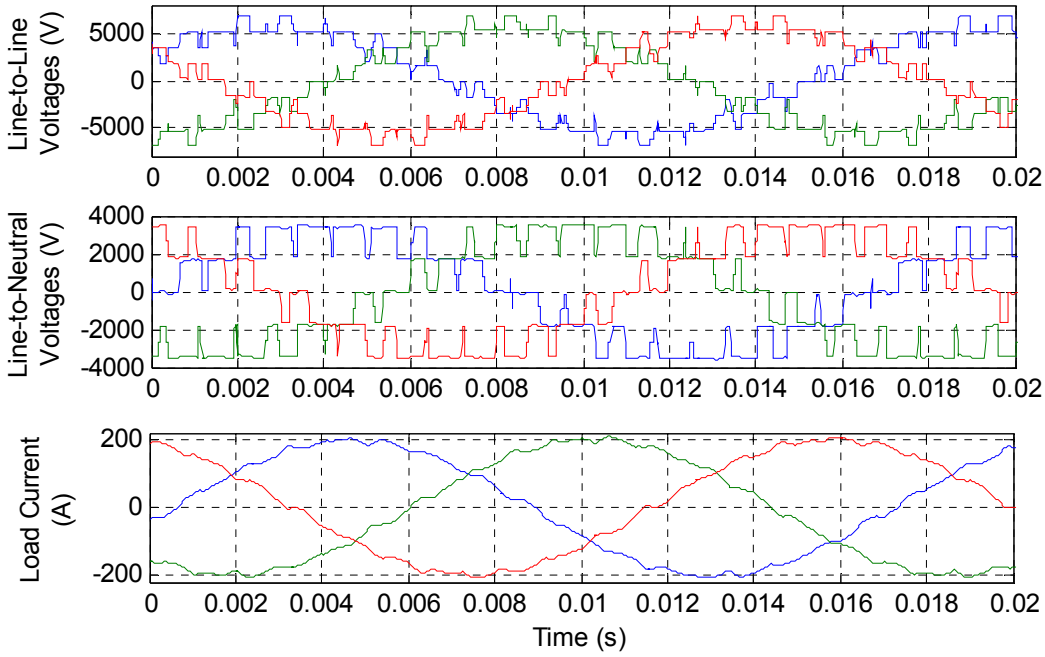


Fig. 2-9. MMC line-to-line voltages, line-to-neutral voltages, and currents with conventional control scheme

Although the modeled MMC has 8 SMs per leg, the output line-to-neutral voltage of the converter has only 5 levels as shown in Fig. 2-9. As explained before, this is due to the fact that in modified PSC-PWM scheme, two SMs of a leg are switched simultaneously to keep the number of SMs in the on state constant. These voltage levels were given in Table 2-2.

In order to evaluate the harmonic content of the waveforms in Fig. 2-9, a Fast Fourier Transform (FFT) analysis is conducted in MATLAB/Simulink.

The results of the FFT analysis show that the THD level of the line-to-line voltage, line-to-neutral voltage, and line current waveforms in Fig. 2-9 are 18.05%, 25.25%, and 4.14%, respectively.

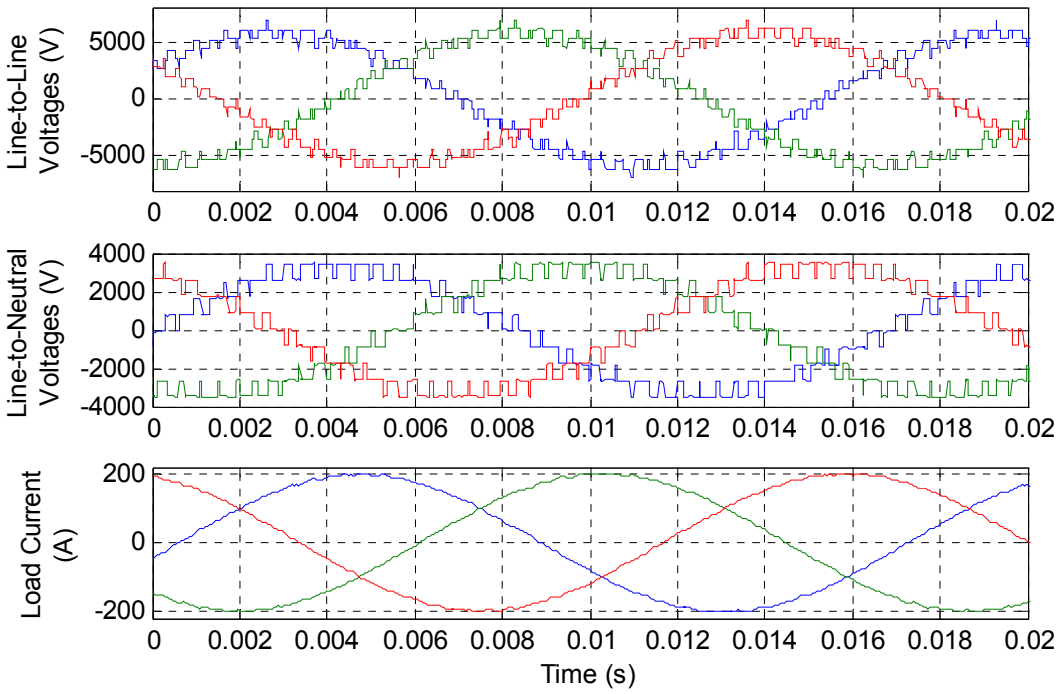


Fig. 2-10. MMC line-to-line voltages, line-to-neutral voltages, and currents with proposed control scheme

Fig. 2-10 demonstrates the output voltage and current waveforms of the MMC applying the proposed control scheme. The number of levels in line-to-neutral voltage of the converter increases to nine. It can be seen that the current waveforms have less distortion compared to those in Fig. 2-9. By performing an FFT analysis, the calculated THD levels of the line-to-line voltage, line-to-neutral voltage, and current are 10.48%, 13.82%, and 1.32%, respectively. This confirms that the proposed scheme has a better performance from the AC side view. Moreover the dominant switching harmonics are shifted to $2.N.f_c\ (Hz)$ in the proposed scheme, compared to those of the conventional scheme, which are around $N.f_c\ (Hz)$ as demonstrated in Fig. 2-11 and Fig. 2-12. The output current harmonic content of the proposed and conventional modulation schemes are shown in Fig. 2-13 and Fig. 2-14, respectively.

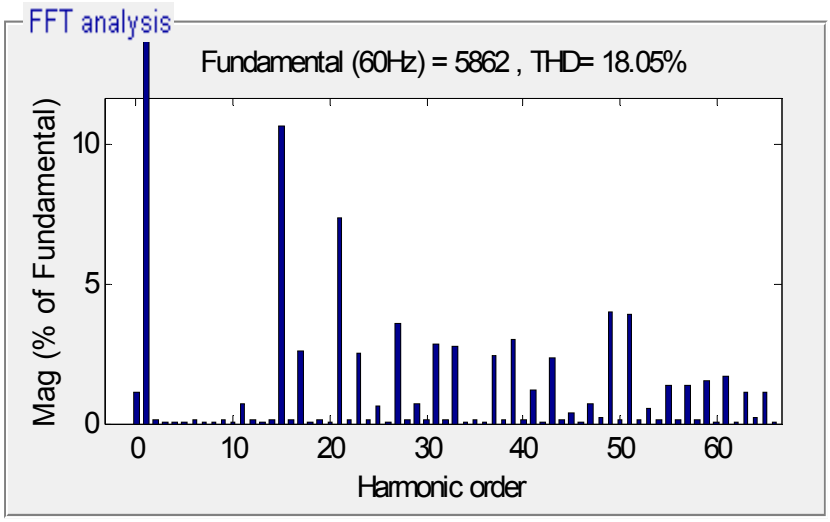


Fig. 2-11. MMC output line-to-line voltage harmonic content in the modified PSC-PWM scheme

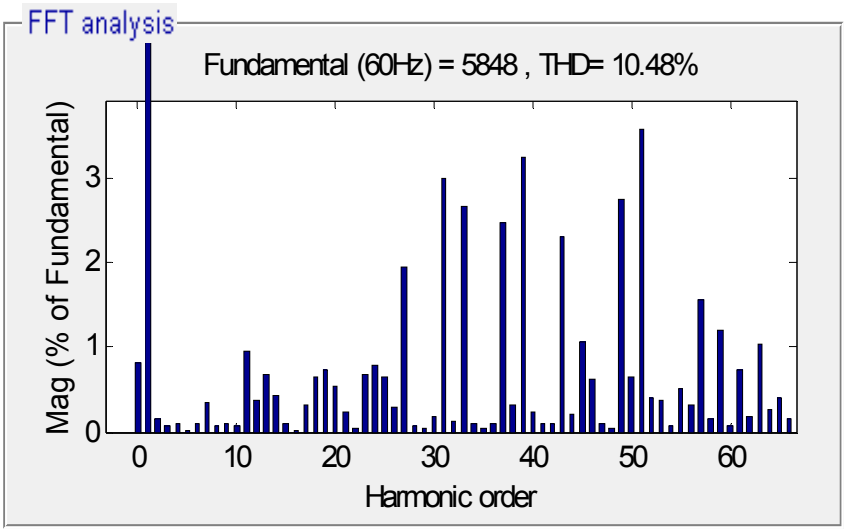


Fig. 2-12. MMC output line-to-line voltage harmonic content in the proposed modulation scheme

The zero order harmonic in these figures is due to the instantaneous voltage unbalance of the capacitors. The level of this harmonic is less than 1% of the fundamental harmonic.

In the Fourier transform plots, the level of fundamental harmonic is 100% and it is plotted out of the frame.

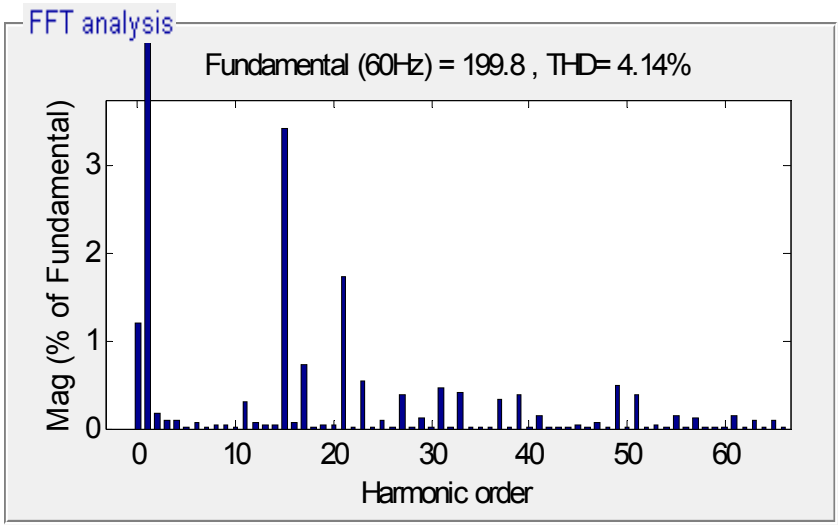


Fig. 2-13. MMC output current harmonic content in the modified PSC-PWM scheme

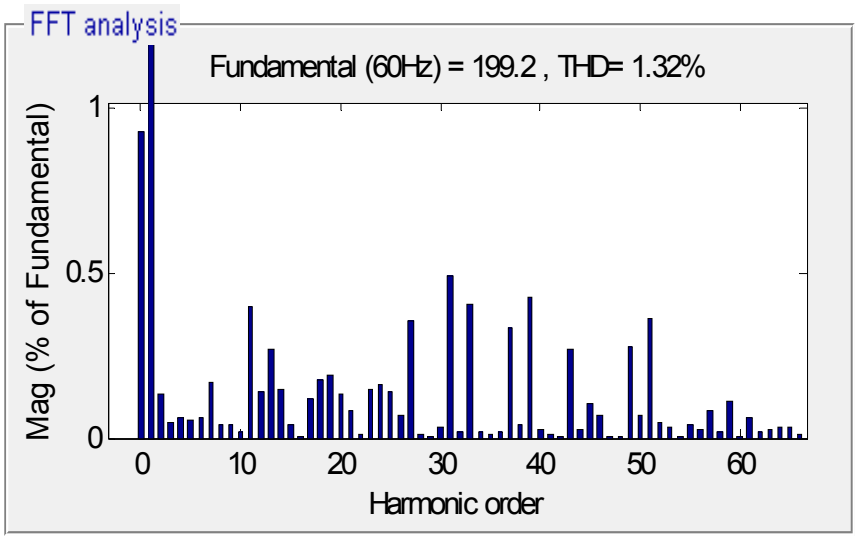


Fig. 2-14. MMC output current harmonic content in the proposed modulation scheme

Since the voltage balancing algorithm is used in the proposed control scheme, the capacitors voltages are properly balanced and kept at reference value of *1750 V* as shown in Fig. 2-15.

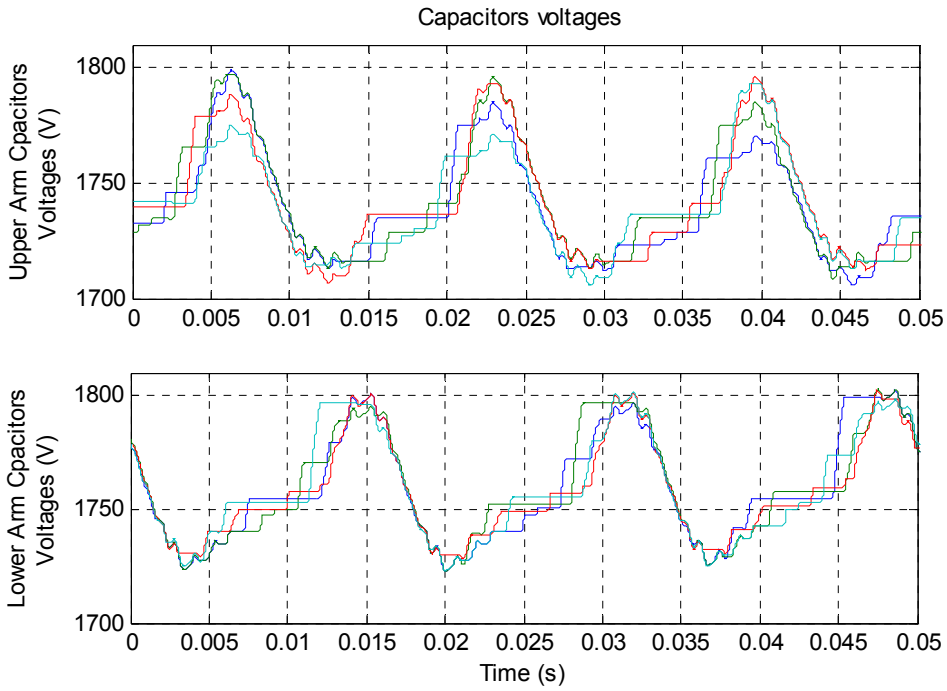


Fig. 2-15. Voltages of capacitors of one leg of an MMC in the proposed control scheme.

2.4 Inner Difference Current and Loss Calculation

In an MMC, the difference currents are used to negotiate the power between the DC source and the SMs' capacitors and are regulated by the averaging controls mentioned before. Assuming that all the capacitors are at the reference capacitor voltage v_c^* ($= {U_{dc}}/{N}$), (2-4) indicates that the inner unbalance voltage u_{Zu}, in the conventional control scheme, is equal to zero. Hence the difference current is attenuated. However, in the proposed control scheme, the inner unbalance voltage in each instance would be ${U_{dc}}/{N}$, 0, or $-{U_{dc}}/{N}$. This is due to the fact that the number of SMs in the on state in each instance can be equal to *N-1, N,* or *N+1*. Equation (2-4) indicates that this inner unbalance voltage imposes difference current in the legs, which may increase the converter loss.

In order to evaluate the effect of distortion in the difference current on the converter efficiency, the converter's conduction and switching losses in both control schemes are evaluated. Fig. 2-16 demonstrates the upper and lower arms currents of phase *u*, when conventional and proposed control schemes are applied to the MMC. The arms currents are more distorted in the case of the proposed modulation scheme as expected. Regarding (2-1) and (2-2) and given that the AC current has less distortion in the proposed scheme, the distortion in the arm current is due to the distortion in the difference current.

Using the simulated current waveforms, the semiconductor specifications from the manufacturer can be used to approximate semiconductor losses. Implementing the IGBT loss model [68] and using the required characteristic curves of the used IGBT module, CM600HB-90H, as described in [69], both conduction and switching losses are calculated for the switching devices in the SMs of an arm.

The IGBT and diode on-state voltages, $V_{CE/F,x}$, and the switching losses, $E_{sw,x}$, of a device *x,* given in the data sheet, are approximated by

$$V_{CE/F,x} = V_{0,x} + A_{cond,x}.\, i_x(t)^{B_{cond,x}} \tag{2-20}$$

$$E_{on,x} = A_{on,x}.\, i_x(t)^{B_{on,x}} \tag{2-21}$$

$$E_{off,x} = A_{off,x}.\, i_x(t)^{B_{off,x}} \tag{2-22}$$

where *i* is the instantaneous value of the device current, $V_{0,x}$, $A_{cond,x}$ and $B_{cond,x}$ are the fitting parameters for the V-I curve of the IGBT and its anti-parallel diode. $A_{on,x}$, $B_{on,x}$, $A_{off,x}$ and $B_{off,x}$ denote the fitting constants of the on and off switching losses [69]. The fitting parameters of the IGBT module used are presented in Table 2-3.

Table 2-3 Semiconductor Specifications for IGBT Module CM600HB-90H

Parameter	Quantity	Parameter	Quantity
$V_{0,T}$	1	$V_{0,D}$	0.5
$A_{on,T}$	0.00621	$B_{on,T}$	0.9501
$A_{off,T}$	0.06854	$B_{off,T}$	0.5112
$A_{off,D}$	0.01968	$B_{off,D}$	0.4705
$A_{cond,T}$	0.03168	$B_{cond,T}$	0.6648
$A_{cond,D}$	0.04501	$B_{cond,D}$	0.6605

Conduction and switching losses are calculated within one period of the output voltage by using the simulated currents and the characteristic curves of the IGBT module, by

$$P_{cond,x} = \frac{\omega}{2\pi}\int_{t}^{t+\frac{2\pi}{\omega}} i_x(\tau).\, v_{CE/F,x}\big(i_x(\tau)\big)d\tau \tag{2-23}$$

$$P_{on,T} = \frac{\omega}{2\pi}\sum_{\kappa_{T,on}=1}^{N_{T,on}}\left(\frac{v_{CE}\left(t_{\kappa_{T,on}}\right)}{v_{CE,ref}}.E_{on,T}\left(i_T\left(t_{\kappa_{T,on}}\right)\right)\right) \tag{2-24}$$

$$P_{off,x} = \frac{\omega}{2\pi}\sum_{\kappa_{x,off}=1}^{N_{x,off}}\left(\frac{v_{CE/F,x}\left(t_{\kappa_{x,off}}\right)}{v_{CE,ref}}.E_{off,x}\left(i_x\left(t_{\kappa_{x,off}}\right)\right)\right) \tag{2-25}$$

The switching-loss energies are scaled by the ratio of the occurring blocking voltage to the reference blocking voltage ($v_{CE,ref} = 2250\ V$) of the characteristic curves and are added together over the duration of a fundamental output time period. Blocking state losses and diode turn-on losses are considered negligible.

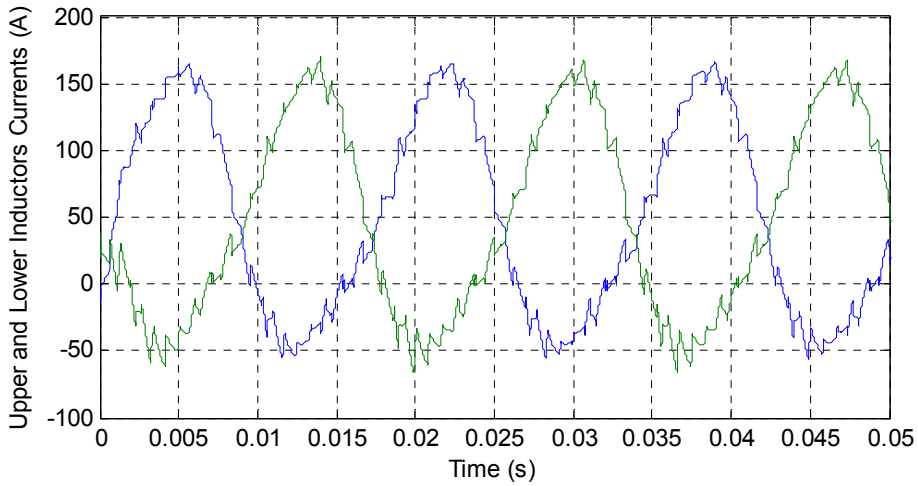
The loss values of all semiconductor devices in an arm are evaluated, and the conduction and switching losses of corresponding semiconductor devices in SMs are then averaged and

demonstrated in Table 2-4. This table corresponds to the parameter values given in Table 2-3, and compares the losses of the conventional control scheme with the ones in the proposed control scheme.

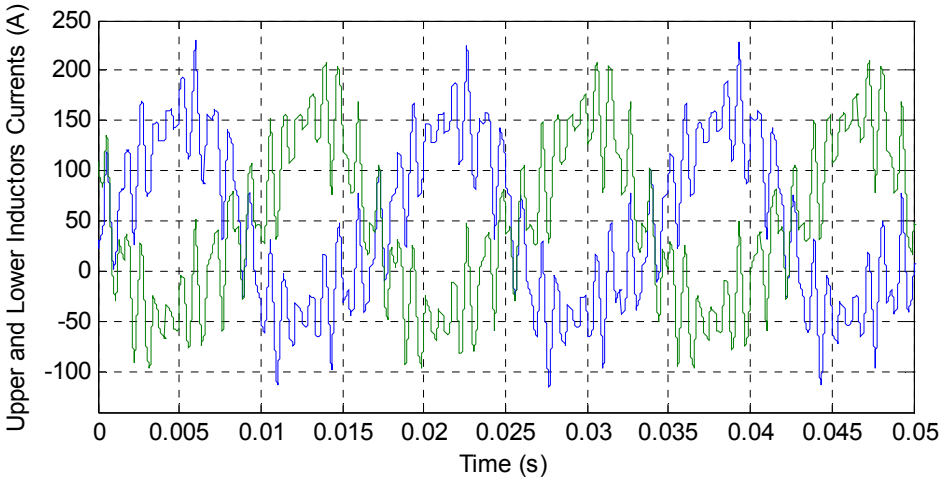
Note that when the converter is working in the inverter mode, the lower IGBT and the upper diode in an SM have more losses as compared to the upper IGBT and the lower diode, respectively. That is due to the fact that the difference current as shown in Fig. 2-4 is in positive direction, in order to convey the energy from the DC bus to the SMs.

Investigating the data of Table 2-4, it can be concluded that although the proposed scheme imposes a more distorted difference current, a semiconductor part within a SM may experience a higher or lower level of loss. That is due to the fact that regarding (2-24) and (2-25), the switching losses depend on the device voltage and current at the instance of switching.

Since the arms currents in the proposed scheme are more distorted, each switching action can impose more or less loss, comparing to its corresponding switching action in the conventional modulation scheme. The converter efficiency in the conventional scheme is 98.94% and reduces to 98.83% in the proposed scheme. Due to the fact that the line currents are less distorted in the proposed scheme, the difference in the overall efficiency between two schemes is even less, if the filter and AC line losses are being considered.



(a)



(b)

Fig. 2-16. The upper and lower arm currents in a) Conventional modulation b) Proposed modulation

If an acceptable THD level is assumed, by using the proposed control strategy, one can reduce the switching frequency, which will result in reducing the switching loss in the converter, and hence, increasing the efficiency of the converter. This is critical when it comes to application of a converter in high power applications.

Table 2-4 Averaged Loss Distribution of IGBT and Diode Parts in an SM

		S_1	D_1	S_2	D_2	SM
Proposed Method	**Conduction Loss**	18	16	87	2	490 W
	Switch-On Loss	11	0	72	0	
	Switch-Off Loss	75	27	176	6	
	Semiconductor Loss	104	43	335	8	
Conventional Method	**Conduction Loss**	14	14	86	1	443 W
	Switch-On Loss	10	0	86	0	
	Switch-Off Loss	38	34	155	5	
	Semiconductor Loss	62	48	327	6	

2.5 Validation

To validate the obtained results, a real-time simulation study is performed. For this purpose, the MMC model is simulated in real-time on an RT-LAB platform. The RT-LAB is an integrated hardware and software real-time simulator from Opal-RT Technologies. A discrete solver with a time step of 70 μs is used for the real-time simulations. This time step is less than one tenth of the period of the 1200 Hz equivalent switching frequency. The plant simulator sends the measurements to a controller simulator. The collected data is then plotted using MATLAB.

For the real-time simulation studies, an MMC model with data provided in Table 2-1 is used. Figures below show the results when the conventional control scheme and the proposed control scheme are implemented.

As it can be seen in these figures, the real-time simulation results validate the simulation results obtained from MATLAB/Simulink. The voltage and current waveforms are the same and the capacitor voltages are kept at the reference voltage.

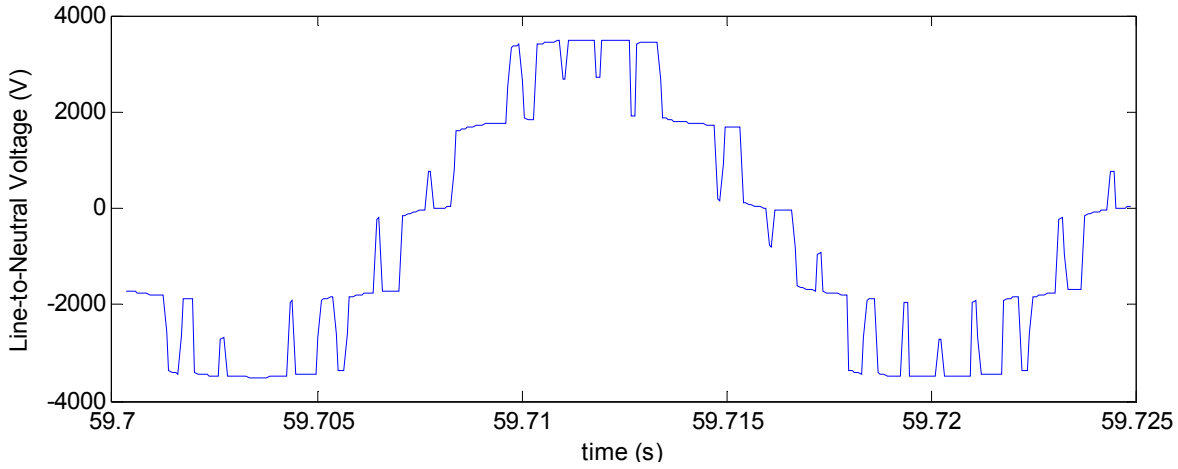


Fig. 2-17. Line-to-neutral voltage in conventional control scheme (Real-time)

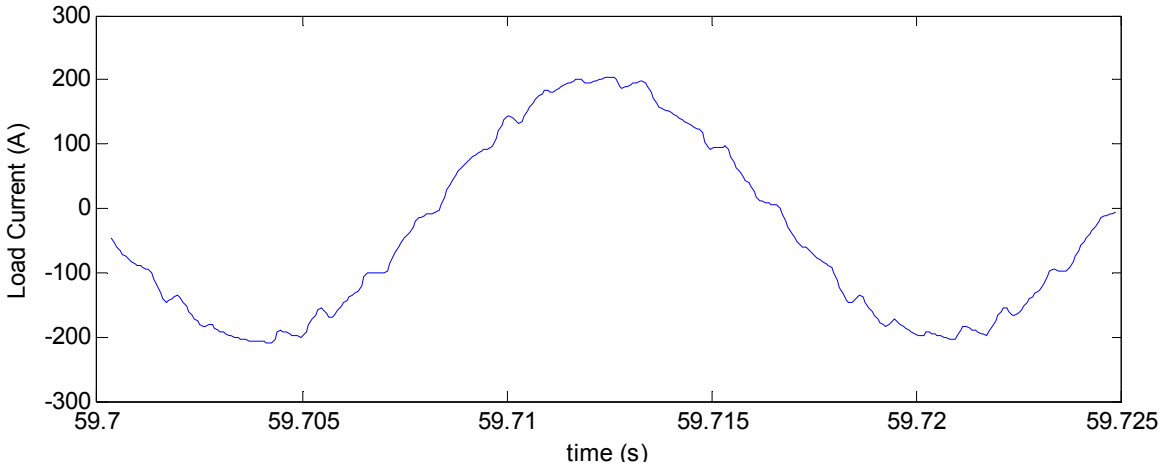


Fig. 2-18. Load current in conventional control scheme (Real-time)

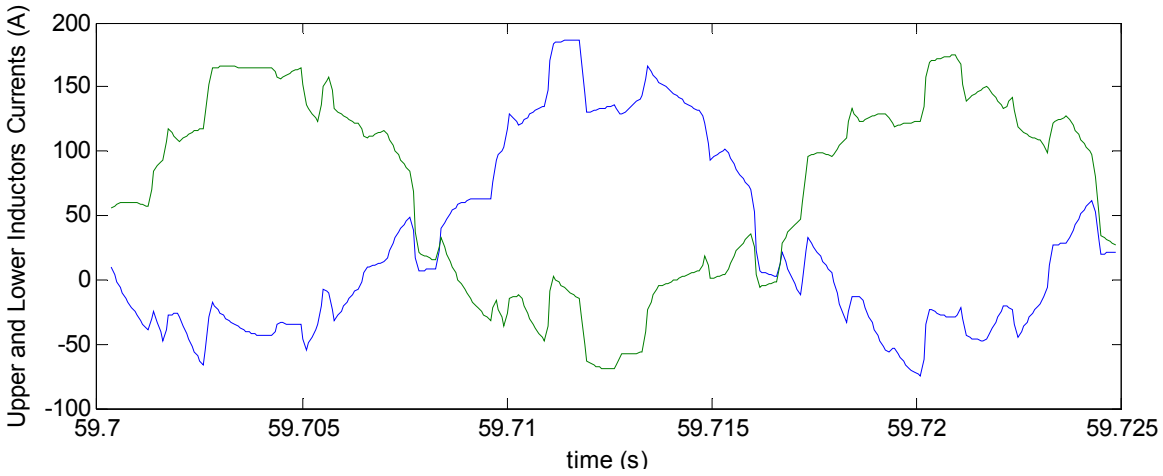


Fig. 2-19. Upper and lower inductors currents in conventional control scheme (Real-time)

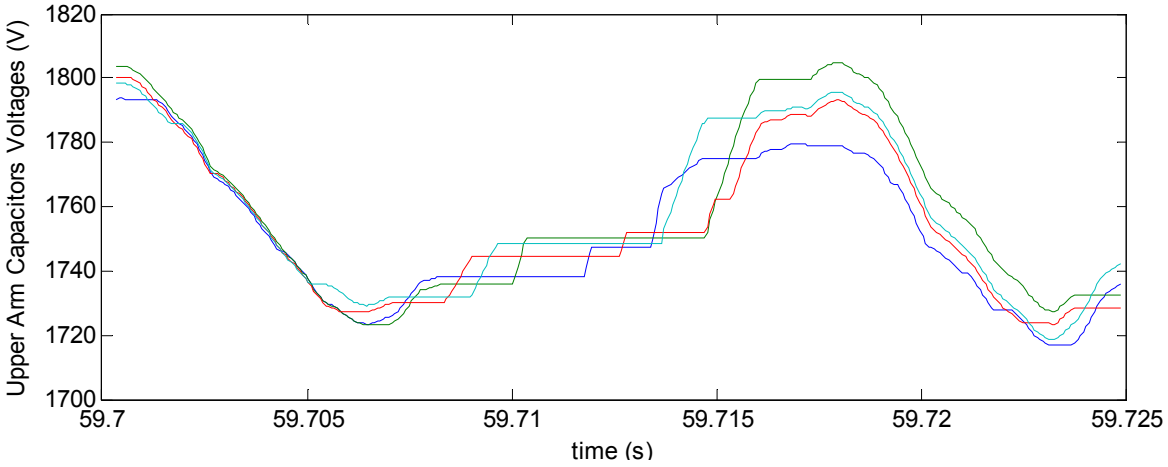


Fig. 2-20. Upper arm capacitors voltages in conventional control scheme (Real-time)

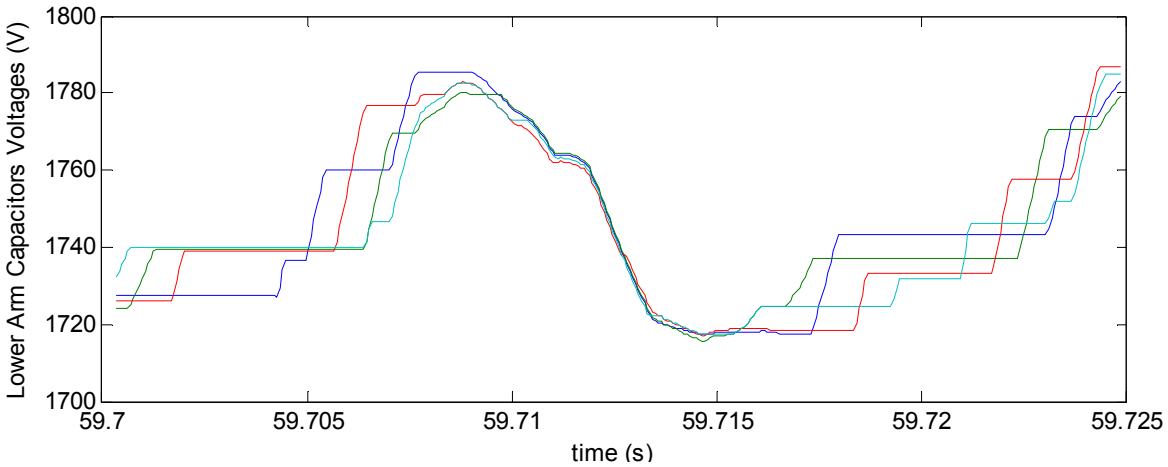


Fig. 2-21. Lower arm capacitors voltage in conventional control scheme (Real-time)

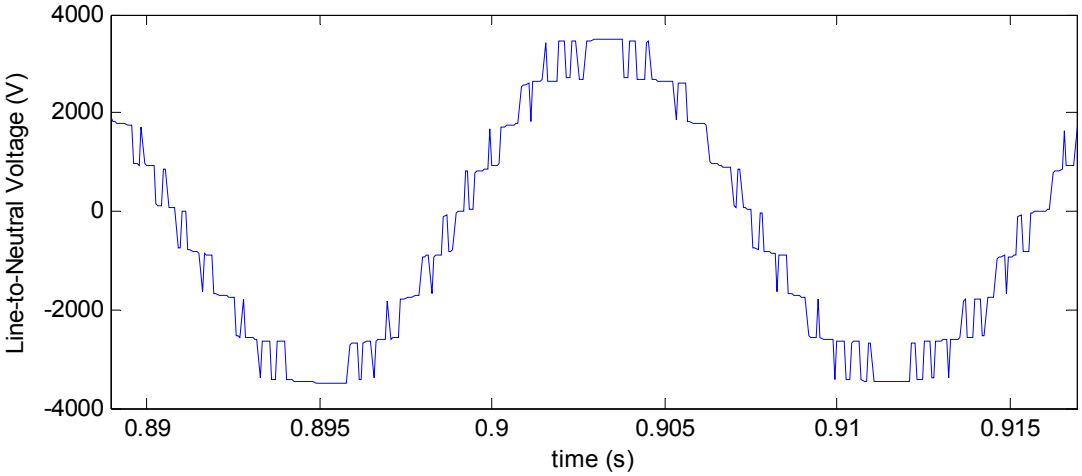


Fig. 2-22. Line-to-Neutral voltage in proposed control scheme (Real-time)

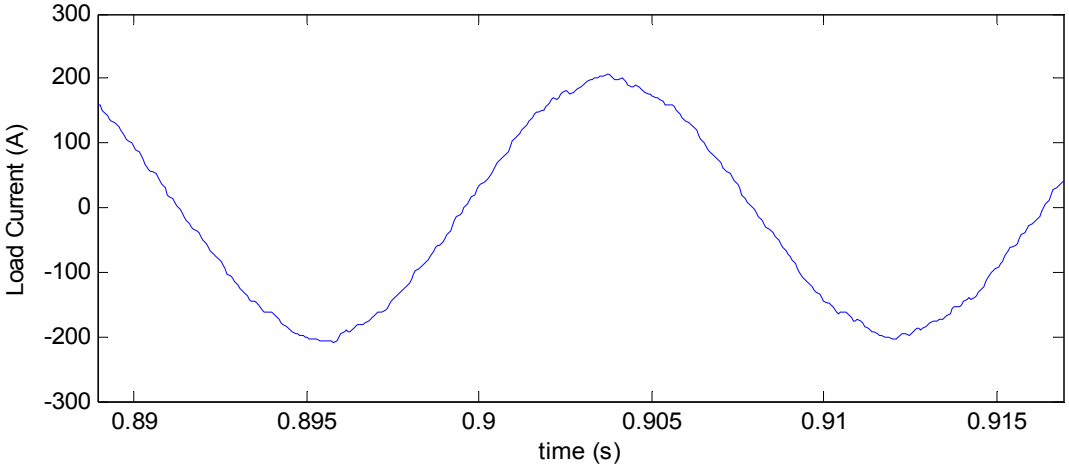


Fig. 2-23. Load current in proposed control scheme (Real-time)

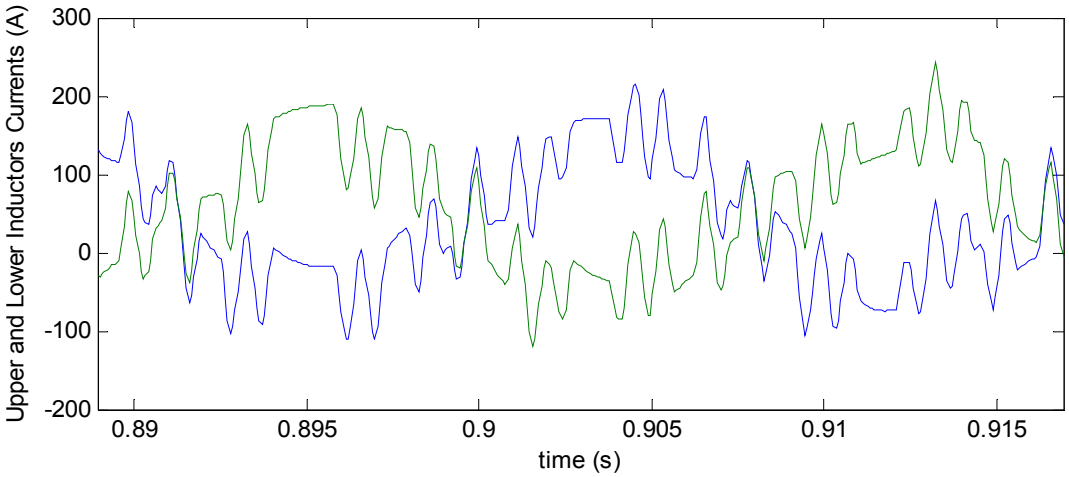


Fig. 2-24. Upper and lower inductors currents in proposed control scheme (Real-time)

The rate of change of the inductance current is high due to the fact that in the time intervals that the number of SMs in the circuit is *N+1* or *N-1*, the voltage across each inductor in that leg is almost equal to 1/2N of the DC bus voltage. This voltage changes the inductor current rapidly.

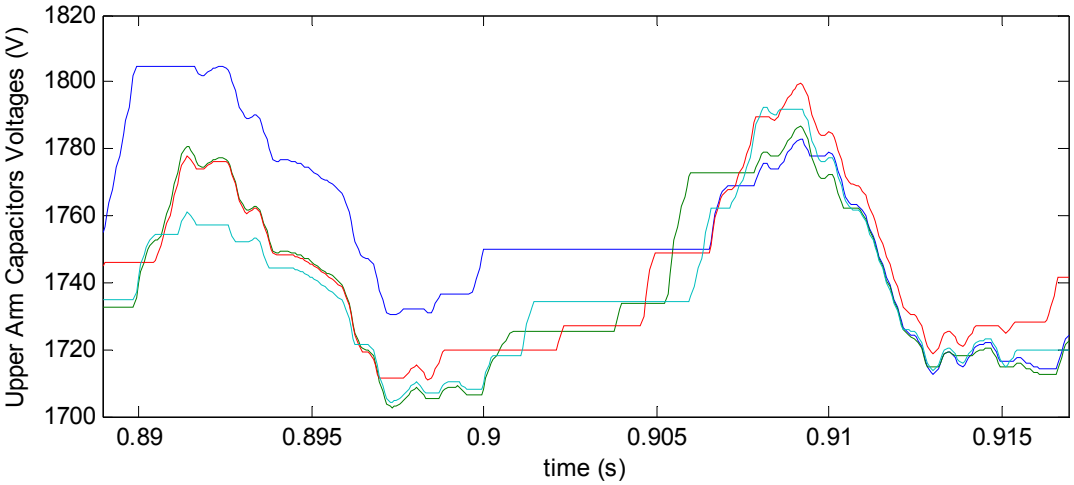


Fig. 2-25. Upper arm capacitors voltages in proposed control scheme (Real-time)

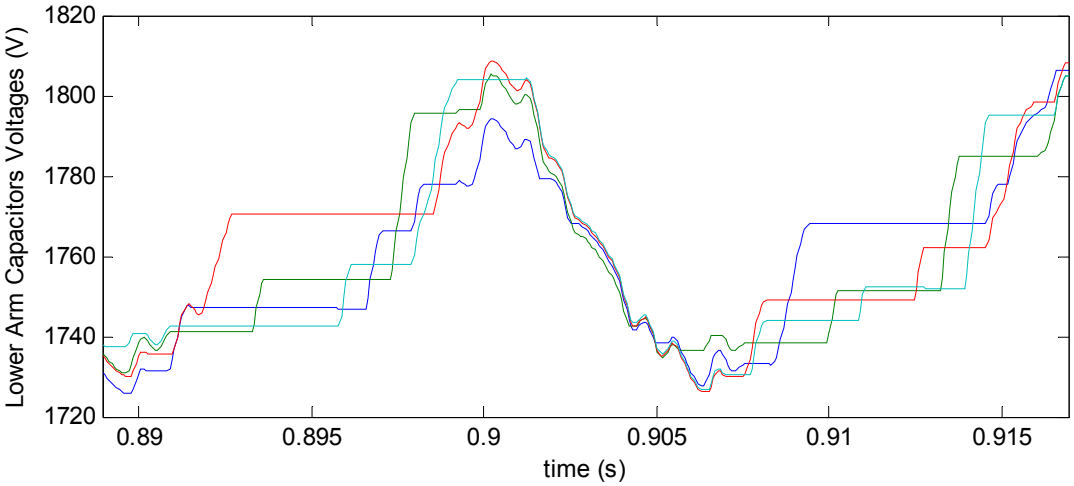


Fig. 2-26. Lower arm capacitors voltage in proposed control scheme (Real-time)

The voltages and currents waveforms obtained from the real-time simulation studies match the results obtained from the simulation studies on MATLAB/Simulink. This verifies the results provided in this chapter.

2.6 Summary

In this chapter a control and modulation scheme for the MMC is proposed. Employing this modulation scheme, the level of harmonics in the output voltage of an MMC is lower compared to the conventional modulation scheme. Further, the dominant harmonics are shifted to higher frequency which reduces the size of filter. The proposed control scheme uses the well-known sorting algorithm to balance the capacitors voltages of each arm.

The proposed control scheme is implemented on MATLAB/Simulink, and the results verify the effectiveness of the proposed scheme in lowering the harmonics levels, while maintaining the capacitors voltages balanced. Furthermore, in order to validate the simulation results, real-time simulation studies are conducted on Opal-RT real-time simulator. The acquired results from the real-time simulations validate the results obtained from offline simulation studies.

Chapter 3 - Design of MMC-based Solid State Transformers

3.1 Background

This section presents a short background on a three-stage SST configuration based on a cascaded H-bridge converter. The basic structure of this SST is then employed to build MMC-based SSTs. Fig. 3-1 shows a detailed model of a three-stage SST employing a 7-level cascaded H-bridge (CHB) multilevel converter [5].

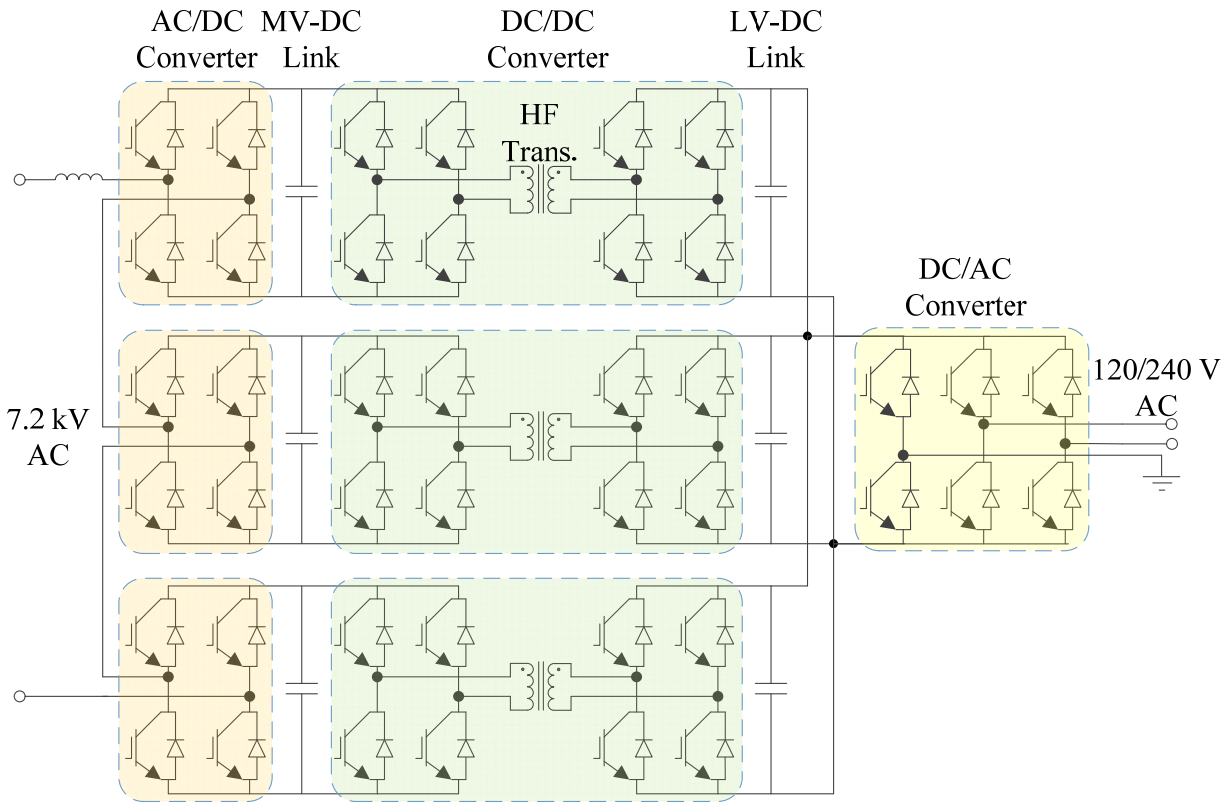


Fig. 3-1. Power circuit of a modular three-stage SST comprising a 7-level CHB

This SST configuration is used as the fundamental structure for the proposed SSTs in this research. The first stage converter is, however, substituted with an MMC. The MMC design criteria are described in chapter 1 under the background.

The second stage of this three-stage SST consists of Dual-Active-Bridge (DAB) converters [5], which are isolated bidirectional DC/DC converters. This converter consists of two single-phase full-bridge converters that are linked with a HF transformer. Each full-bridge converter has four IGBT switches. The IGBTs at high-voltage side of a DAB has the same voltage rating as of those used in multilevel converter. The IGBTs at low-voltage side withstand the LVDC voltage.

HF transformers in this stage perform the voltage level step-down and the isolation tasks. The leakage reactance of the HF transformers should be high enough to provide desired phase shift between the primary and secondary of the transformer at rated power. If the leakage reactance of the HF transformers is not high enough, series reactors may be added. If unidirectional power flow is required, an uncontrolled converter can be used at the low-voltage side of the second stage.

DAB converters are switched at a high frequency and are able to provide bidirectional power flow. The real power flows from the bridge with leading phase angle to the bridge with lagging phase angle. Assuming a modulation index of one for both bridges in a DAB, the voltages and current waveforms are presented in Fig. 3-2.

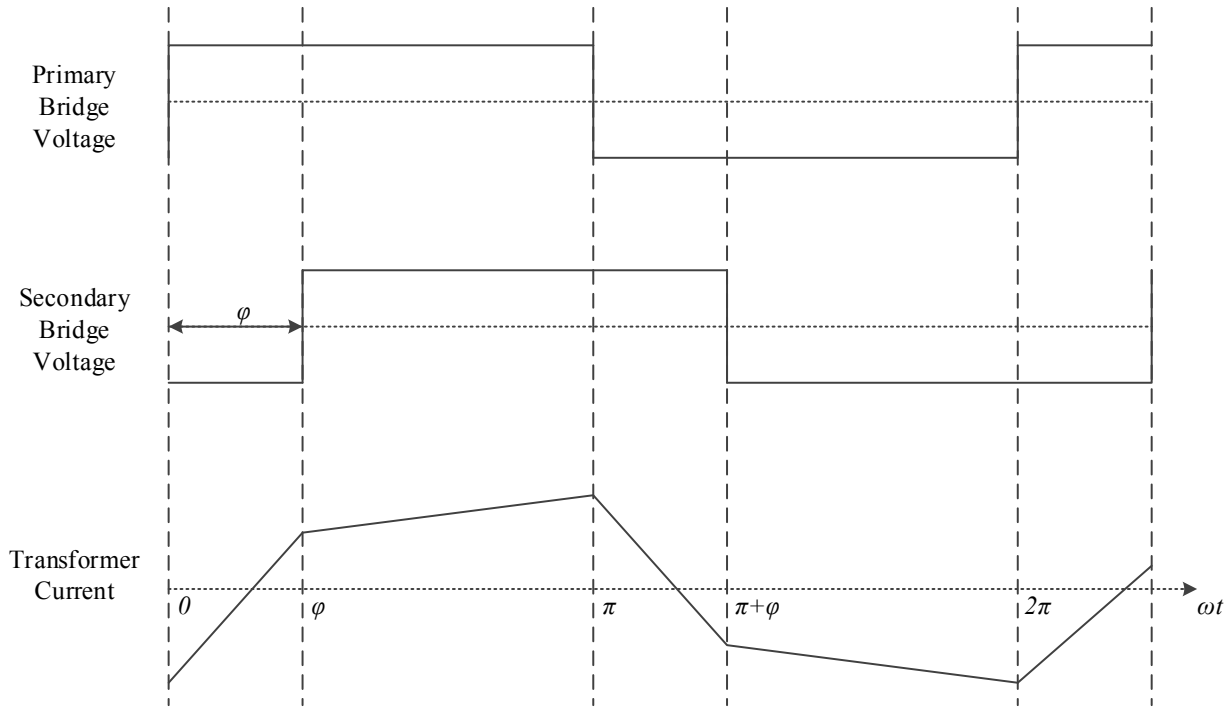


Fig. 3-2. Voltage and current waveforms in a DAB converter

The amount of transferred power in DAB converter with the aforementioned switching scheme is equal to [70]:

$$P = \frac{V_{dc_{MV}} \cdot V_{dc_{LV}}}{\omega n L_{leak}} \phi \left(1 - \frac{|\phi|}{\pi}\right) \tag{3-1}$$

Where $n = N_P/N_S$ is the turn ratio of the transformer; $V_{dc_{MV}}$ and $V_{dc_{LV}}$ are the voltages of the DC voltages at primary and secondary side of a DAB converter, respectively; ω is the angular velocity at switching frequency; L_{leak} is the inductance of the transformer seen from the secondary side; and ϕ is the phase-shift of the secondary voltage with respect to the primary voltage, and is controlled for the required amount of power.

If $d = nV_{dc_{LV}}/V_{dc_{MV}}$ is at one, by choosing the right transformer turn ratio, Zero Voltage Switching (ZVS) condition is well satisfied for both bridges for all values of ϕ [5, 70] . Hence,

the best transformer ratio would be the same as the voltage ratio between the MV and LV capacitors. The transformer design is addressed in [71, 72]. Knowing the rated power of the transformer, the switching frequency, DC voltages and the nominal phase shift, which would be around $\pi/6$, (3-1) can be employed to find the required amount of leakage reactance of the transformer, as in (3-2).

$$L_{leak} = \frac{V_{dc_{MV}} . V_{dc_{LV}}}{\omega N P} \phi \left(1 - \frac{|\phi|}{\pi}\right) \tag{3-2}$$

A power unbalance among the parallel DAB converters can occur because of transformer parameter mismatching and DC bus voltage differences. This problem can cause over-current issues. To overcome this problem, a control strategy is proposed in [73] which balances the real power through the parallel DAB modules.

The output inverter of Fig. 3-1 is a full-bridge converter that provides two 120 V terminals which are in opposite polarity. As a result a 240 V terminal is available for high power domestic loads. This inverter could be modulated in a way that it produces standard 3-phase output voltage in order to supply 3-phase loads.

In this chapter, an MMC is adopted to design SSTs with high/low voltage DC/AC terminals. This type of SST can be utilized in both AC and DC distribution systems. Besides, since an MMC is employed as the input stage, this SST is easily scalable to higher voltage levels.

3.2 Proposed SST, Type I

The MMC unlike other multilevel converters do not have a limitation on the number of series SMs. It also provides a HVDC terminal which is not provided in some of the multilevel

converters such as the CHB converter. Fig. 3-3 represents the power circuit diagram of a single-phase MMC consisting of half-bridge SMs.

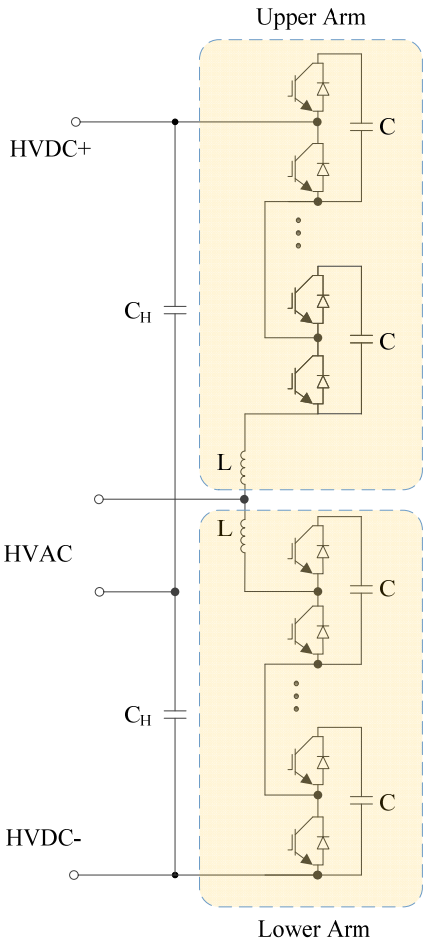


Fig. 3-3. Power Circuit of a single-phase MMC

The MMC has DC capacitors inside each SM. The energy stored in these capacitors can be transferred to a low voltage load or grid through isolated DC/AC converters. Hence, the DAB converters of Fig. 3-1 can be connected to the capacitors of the MMC of Fig. 3-3 to build up a SST that employs an MMC at the input stage. The proposed SST, which employs a single-phase MMC as its input stage converter, is shown in Fig. 3-4. The DAB converters are parallel at the

low-voltage side. The low-voltage capacitors can be distributed among the DAB cells or be lumped as a single capacitor module.

Since the MMC is modular and scalable to high voltage levels and this converter is used in the proposed SST, the proposed configuration is easily scalable to higher voltage levels.

The proposed SST provides LVDC, MVDC and HVDC ports in addition to LVAC and HVAC ports and, hence, can be employed in various network topologies. The LVDC port has a voltage level of 400V and can interface DC sources, loads and storage units. The presence of the HVDC link allows interfacing of the proposed SST to a DC distribution system.

The third stage converter in the proposed SST can be either three-phase or single-phase converter. The converter shown in Fig. 3-4 provides 120 V and 240 V output ports and interfaces a 3-wire, single-phase, midpoint neutral system.

As mentioned before, the DC/DC converters are DAB converters and they allow bidirectional power flow between HV and LV terminals. If a unidirectional power flow from HV terminals to LV terminals is sufficient, uncontrolled rectifiers can be employed at the low voltage side of the DC/DC converters. This will reduce the number of switches in the device and simplifies the control scheme.

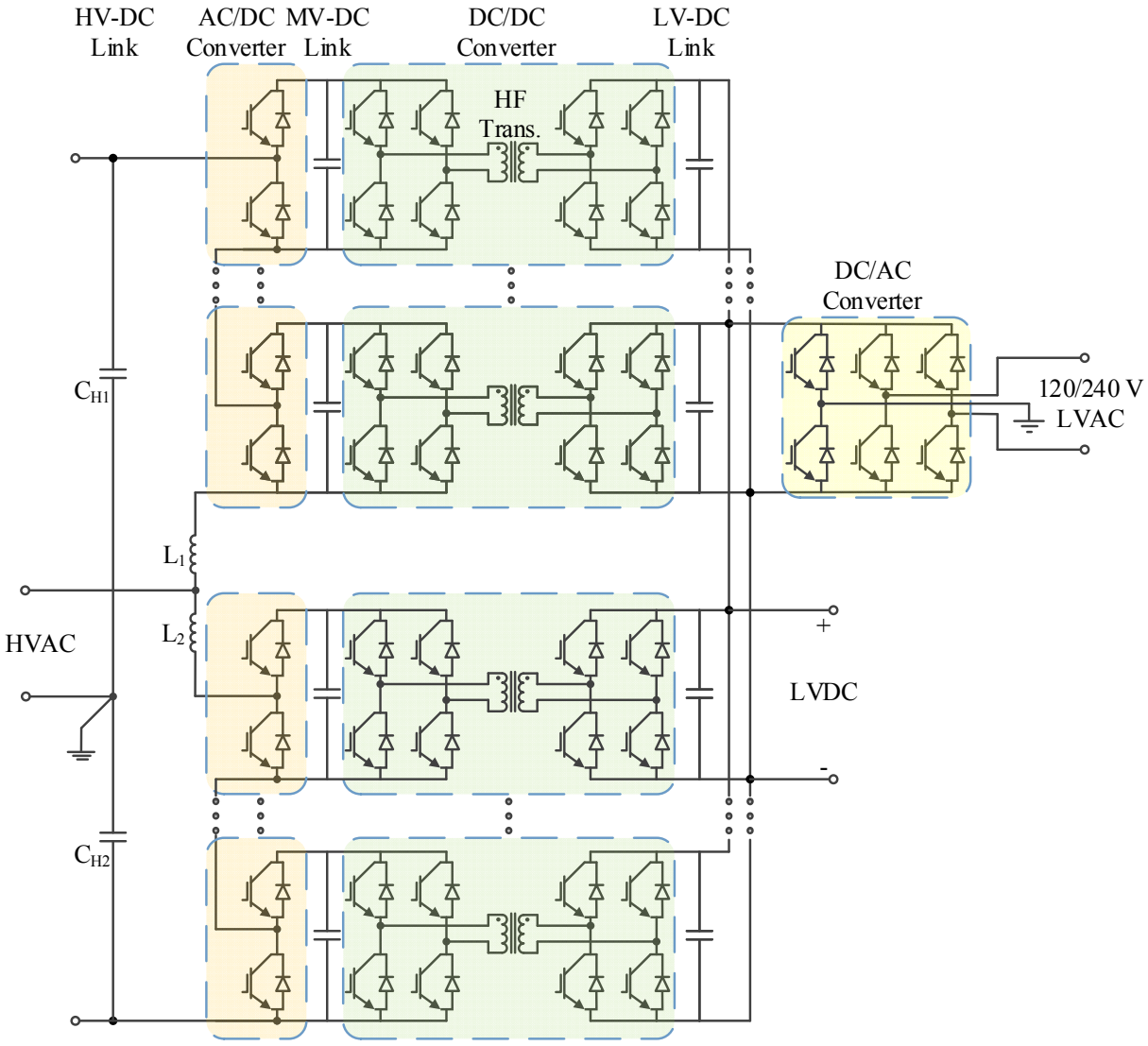


Fig. 3-4. Proposed modular three-stage SST, Type I

3.3 Simulation Results of SST Type I

In order to evaluate the validity of the proposed topology, a detailed model of a 50 kVA SST based on the proposed topology is implemented in MATLAB/Simulink. The model parameters are given in Table 3-1.

Table 3-1 Model Parameters, SST Type I and II

Parameter	Quantity	Unit
Nominal Power	50	*kVA*
HVAC voltage level	7.2	*kV*
LVAC voltage level	120/240	*V*
HVDC voltage level	22.8	*kV*
LVDC voltage level	400	*V*
MVDC capacitance	24	*μF*
Rated MVDC capacitor voltages	3.8 (=22.8/6)	*kV*
LVDC capacitance	100	*μF*
Arm inductance	16.2	*mH*
Rated frequency	60	*Hz*
HV converter switching frequency	360	*Hz*
HF transformer nominal frequency	3000	*Hz*
HF transformer nominal power	4.2 (=50/12)	*kVA*
HF transformer winding 1 parameters (V1, R1, L1)	3.8 0.0011 0.0048	*kV* *pu* *pu*
HF transformer winding 2 parameters (V2, R2, L2)	400 0.0011 0.0048	*kV* *pu* *pu*
LV converter switching frequency	1080	*Hz*
Load active power	2*23	*kW*
Load power factor	0.94	--

Fig. 3-5 shows the HVAC voltage and current waveforms of the SST. The THD level of the current is %4.41.

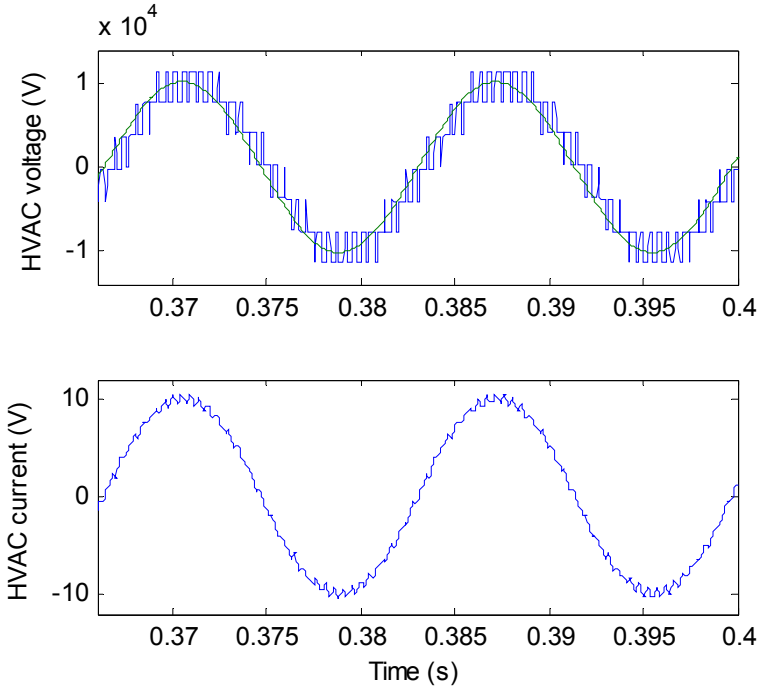


Fig. 3-5. HVAC voltage and current

Employing the aforementioned balancing controls, the voltages of the MVDC links are kept balanced as shown in Fig. 3-6. The upper part shows the voltages across the six capacitors in the upper arm of the MMC converter, and the lower part shows the capacitor voltages in the lower arm. The reference voltage for the MVDC links is 3800 V. The voltage variations across the MVDC capacitors are limited to %5 of the reference voltage.

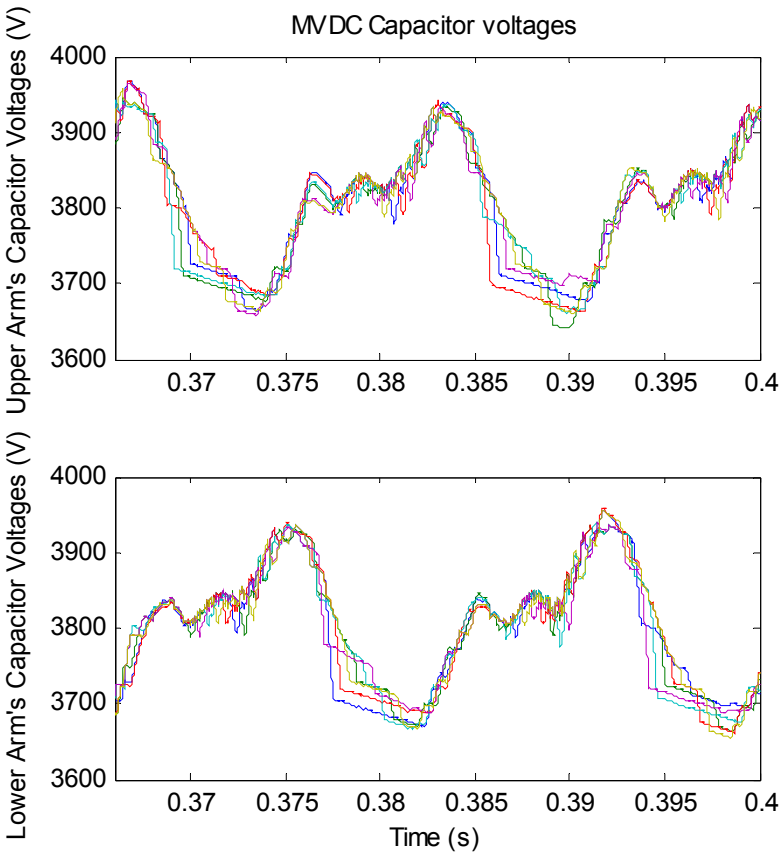


Fig. 3-6. MVDC capacitor voltages

Fig. 3-7 shows the LVDC voltage which is around the reference value of 400 V. Fig. 3-8 shows the 120 V and 240 V outputs of the LVAC converter. The voltage waveforms of the 120 V ports are offset by a half-cycle, or 180 degrees offset, measured against the neutral wire.

Fig. 3-9 shows the LVAC currents. Since two equal 23 kW single-phase loads are assumed at the output of the converter, the magnitudes of the two currents are the same. THD level of the LVAC current is %4.71.

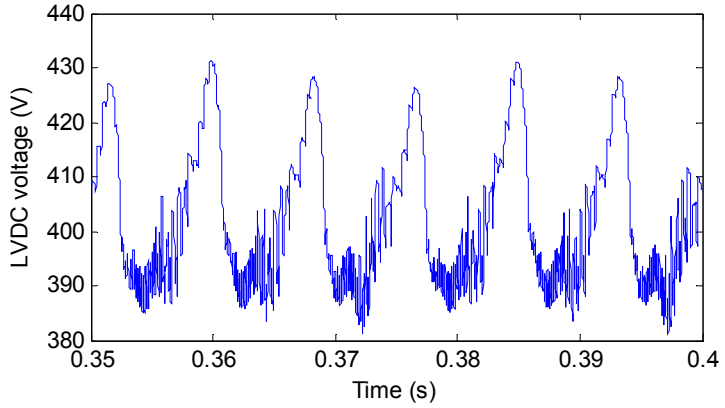


Fig. 3-7. LVDC voltage

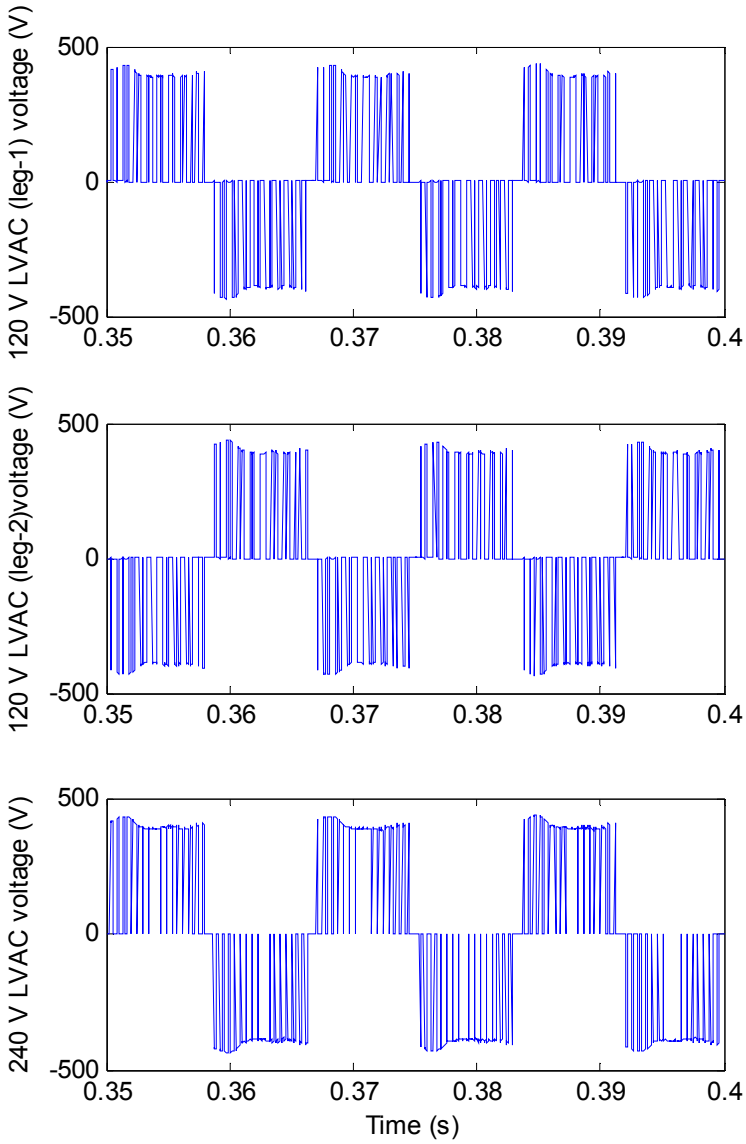


Fig. 3-8. LVAC output voltages

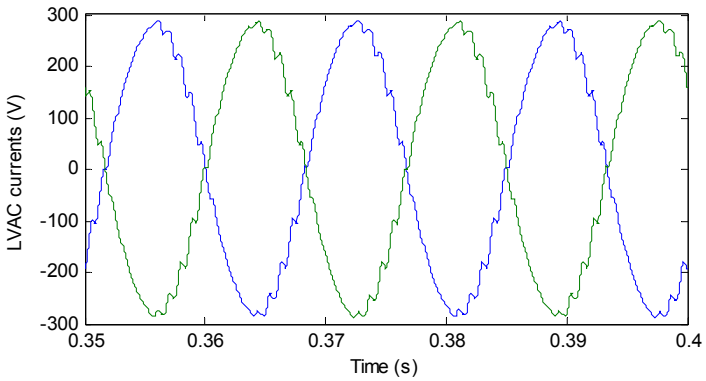


Fig. 3-9. LVAC output voltages

Simulation results indicate that SST exchanges the power among its ports while the controllers keep the voltages at the reference values.

3.4 Proposed SST, Type II

The number of SMs in the proposed SST type I is even. It is possible to have two groups of SMs each connected to one LVDC capacitor. Connecting two DC capacitors in series provides the neutral point of the output converter without employing the third leg in the converter. An alternate to the proposed SST in Fig. 3-4 is depicted in Fig. 3-10. In this SST two capacitors are employed at the LVDC bus, each connected to the SMs of one arm. The voltage across each capacitor is half of the voltage across the LVDC capacitor in Fig. 3-4. For the same voltage ripple in the LVDC bus as in type I SST, the capacitance of each capacitor must be two times higher.

In type II SST a neutral point is readily available and there is no need for the third leg in the output inverter. A simple single-phase sinusoidal-PWM technique is therefore sufficient for modulating the output inverter.

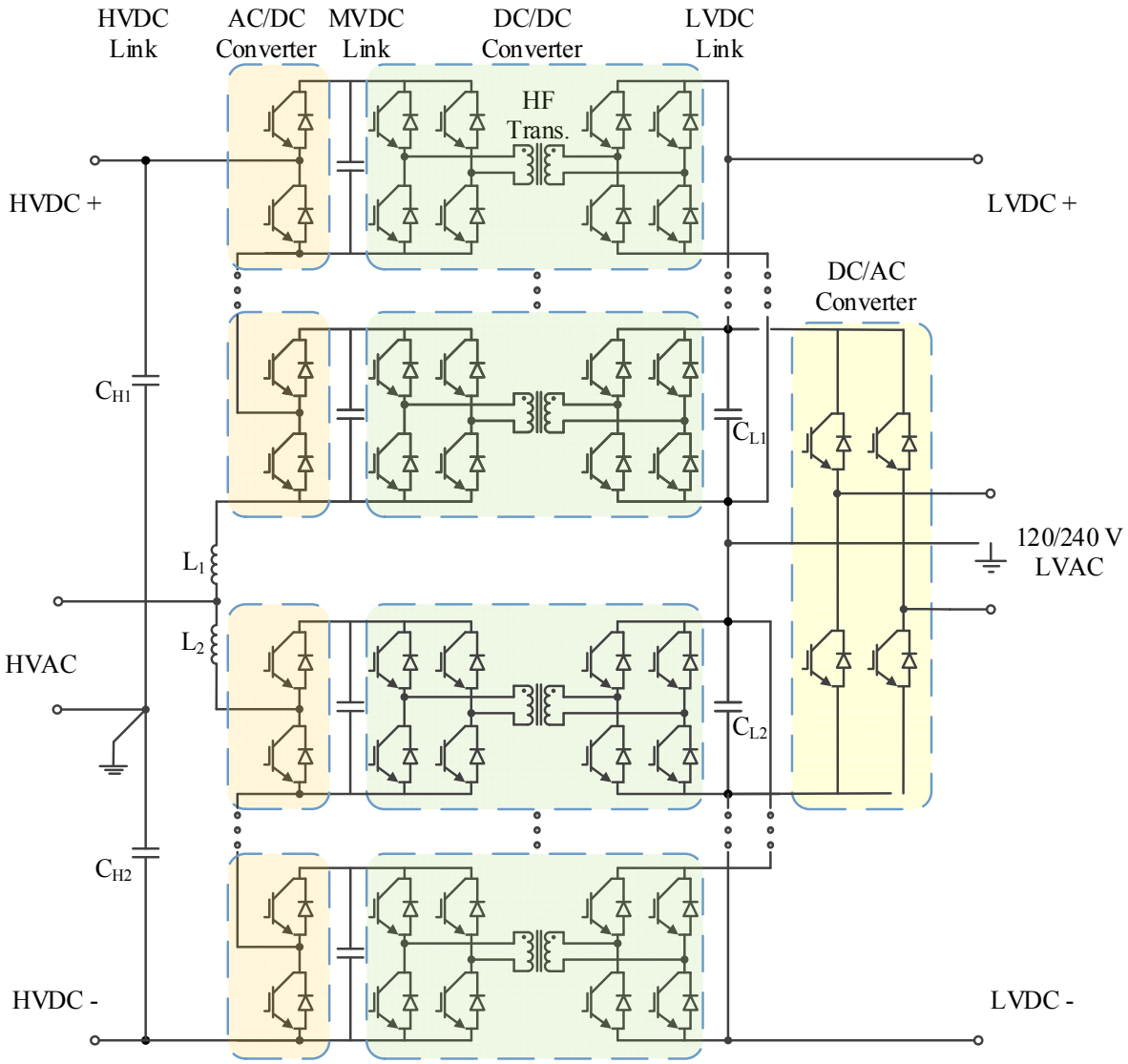


Fig. 3-10. Proposed modular three-stage SST, Type II

3.5 Simulation Results of SST Type II

A uni-directional power flow is assumed in the simulation studies, and hence, diode bridges are employed at the secondary side of the HF transformers. The model parameters are the same as the ones described in Table 3-1.

Fig. 3-11 shows the HVAC voltage and current waveforms. The generated voltage has seven levels. This voltage lags the grid voltage as it can be seen in the figure, which indicates an active power flow from the grid toward the SST. The THD level of the current is 4.39%.

The generated voltages by the SST at the low voltage side are shown in Fig. 3-12. This figure also shows the output currents of the SST measured after an output LC filter. These currents have the same magnitude since identical single-phase loads are connected to the LVAC terminals. The THD level of these currents is 1.61%.

The controllers on the MMC keep the capacitor voltages close to reference value. These voltages are shown in Fig. 3-13. The LVDC voltage is regulated by the converters in the second stage. This voltage is shown in Fig. 3-14. Both the MVDC and LVDC voltages are regulated in the ±10% of the reference value.

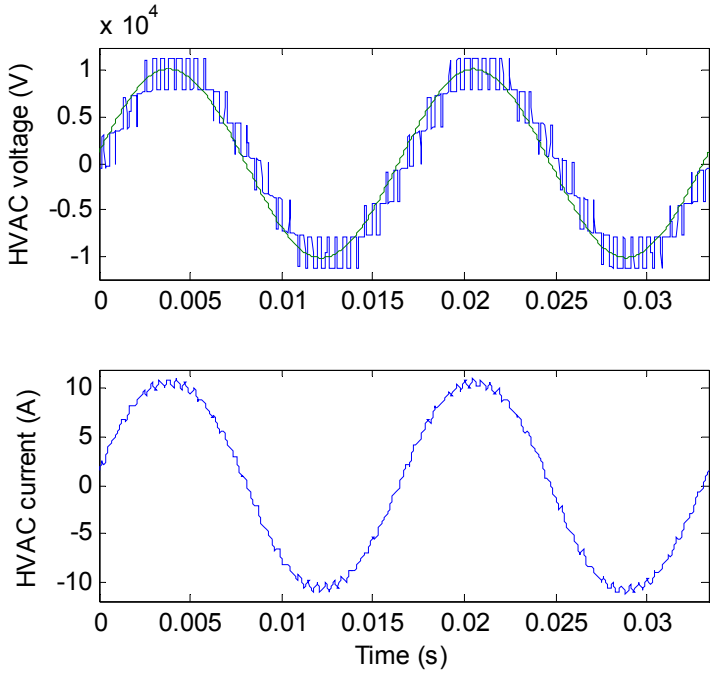


Fig. 3-11. HVAC voltage and current

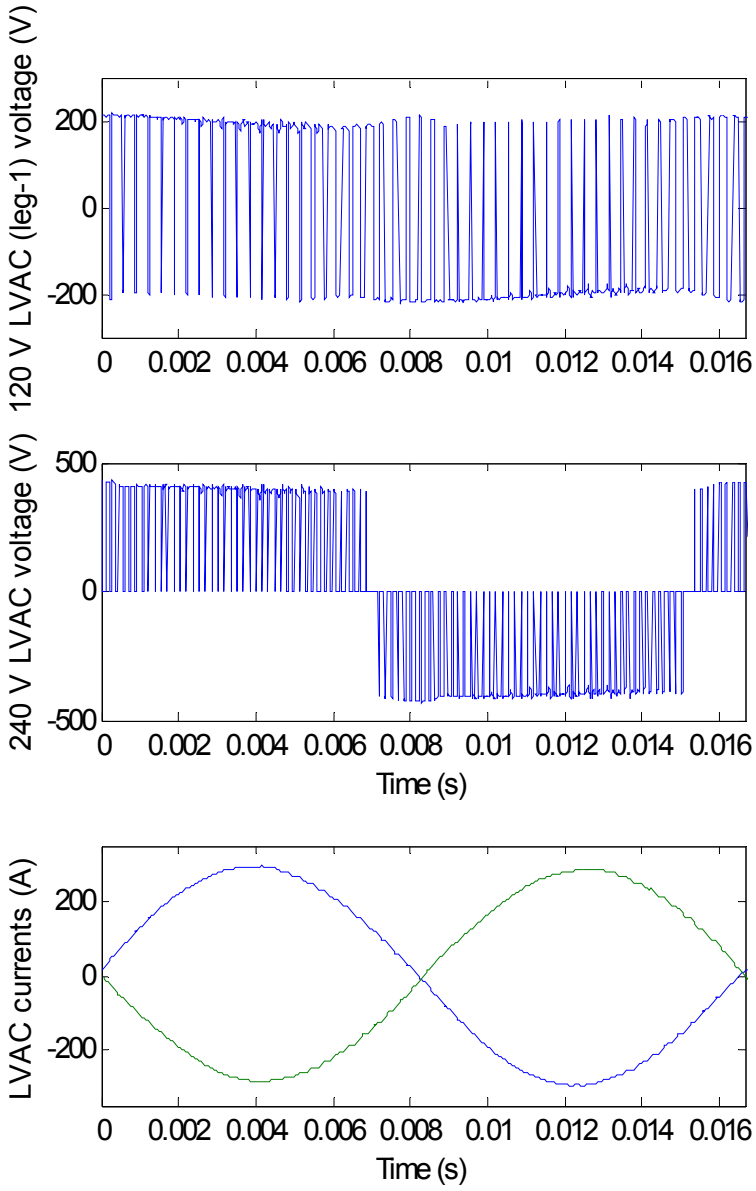


Fig. 3-12. LVAC output voltages and currents

As it can be seen, the 120v output has a two-level waveform, while the output voltage of the Type I SST has a 3-level waveform, as shown in Fig. 3-8.

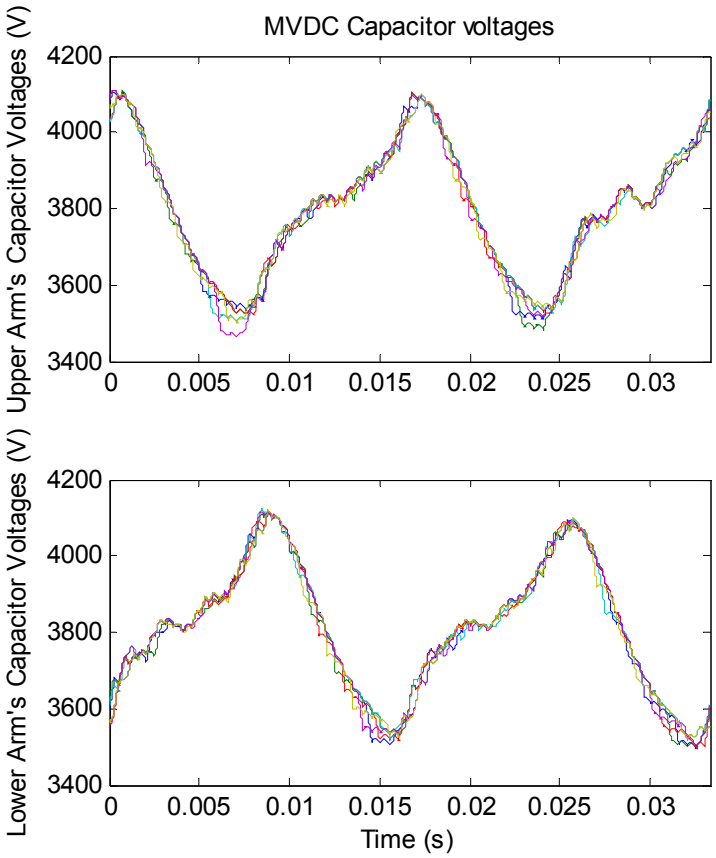


Fig. 3-13. MVDC capacitor voltages

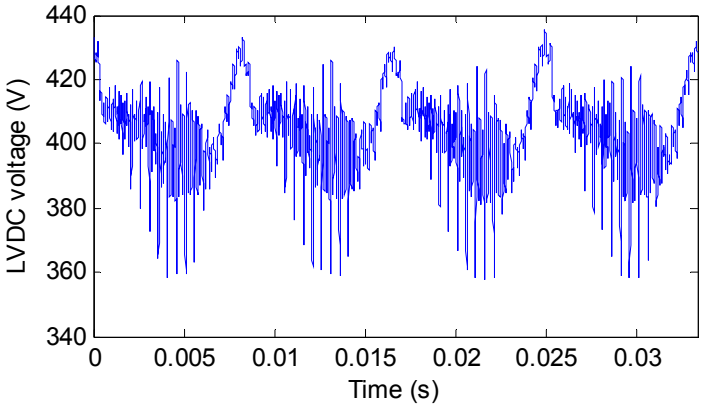


Fig. 3-14. LVDC voltage

Simulation results show that the proposed configuration effectively exchange the required amount of power among the terminals while all the voltages are kept at their reference values.

3.6 Proposed SST, Type III

Two back-to-back MMC converters results in a high-voltage AC/AC converter. In this configuration a common HVDC link is also available that can interface a DC source or grid. Note that since the MMC is easily scalable to high number of levels, this configuration is suitable for a wide range of input voltages.

In this work, the back-to-back MMC configuration is used to convert the low-frequency input voltage to a medium-frequency voltage. The converted voltage is then supplied to a HF transformer, which performs the step down and isolation tasks. A low-voltage bridge converter transfers the power from the output voltage of the transformer to a LVDC link. This LVDC link has a voltage level of 400V and is suitable for integration of DRERs, DESDs, and DC loads. The LVDC voltage is translated to a LVAC voltage through a three-leg converter. This converter provides 120 V and 240 V output terminals to supply residential customers. A three-phase converter may as well be employed at this stage. Fig. 3-15 illustrates the circuit diagram of the proposed SST configuration.

The proposed SST configuration provides all the required terminals, including a HVAC, a HVDC, a LVAC, and a LVDC terminal to interface all types of the distribution grids, loads, storage devices, and distributed generators.

Since the converters in the proposed configuration are bi-directional converters, the electric power can flow among all the AC and DC terminals. If a unidirectional power flow from HV terminals to LV terminals suffices, the full-bridge converter in the second stage can be replaced by an uncontrolled rectifier.

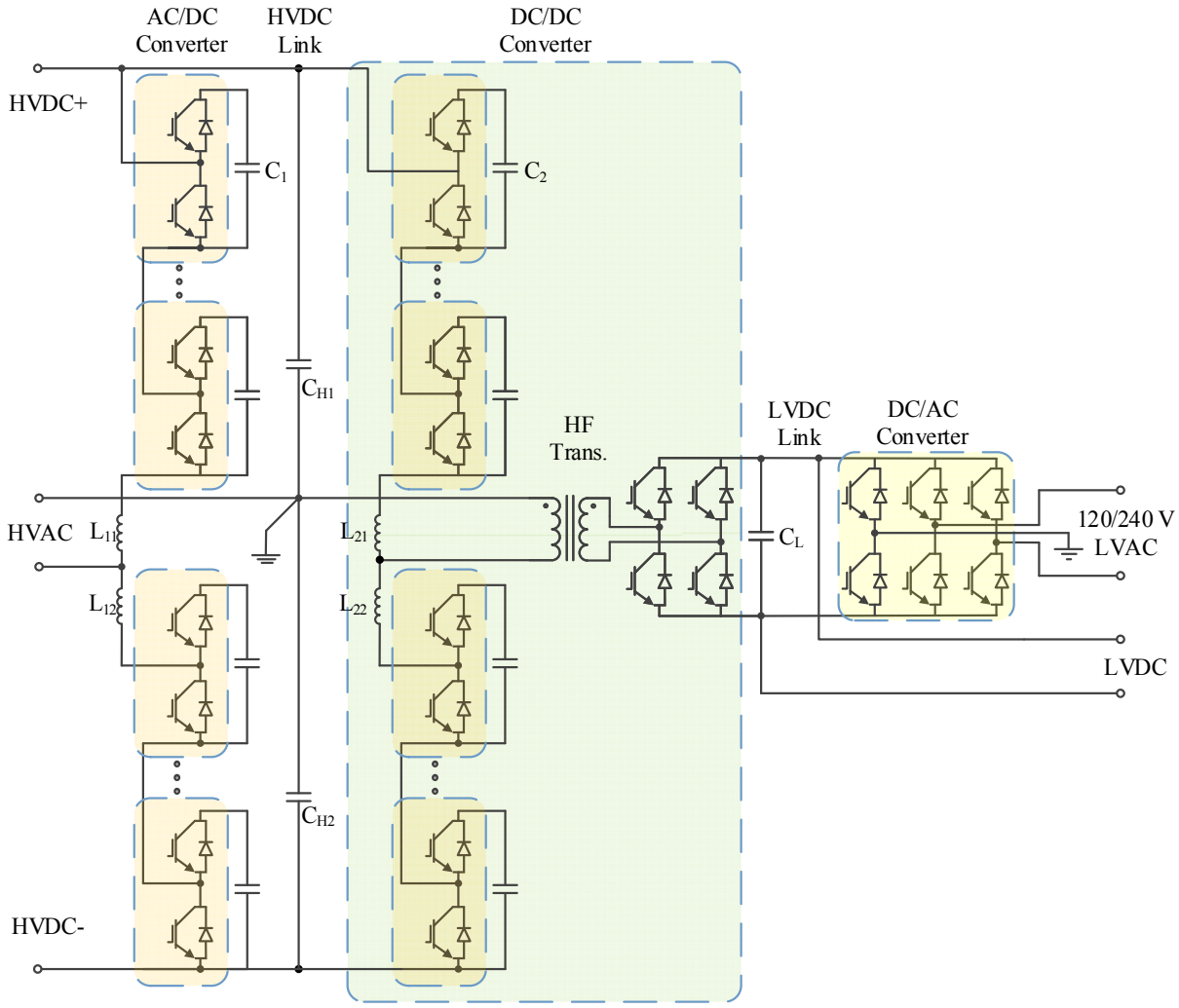


Fig. 3-15. Circuit diagram of the proposed three-stage SST, Type III

3.7 Simulation Results of SST Type III

In order to validate the expected performance of the proposed SST configuration in transferring the required amount of power among its terminals, a detailed model of the proposed SST is implemented in MATLAB/Simulink. The rated apparent power of this model is 50 kVA and the power flow is assumed to be unidirectional; hence an uncontrolled rectifier is employed in the second stage of the configuration. The HVDC terminal is connected to a DC grid.

Table 3-2 shows the model parameters.

Table 3-2. Model Parameters, SST Type III

Parameter		Quantity	Unit
Rated power		50	kVA
Grid rated frequency		60	Hz
HVAC phase voltage level		7.2	kV
HVDC voltage level		22.8	kV
HVDC capacitance (C_H)		12	μF
Number of modules per arm		6	--
SM capacitor rated voltage		3.8 (=22.8/6)	kV
Stage 1	SM switching frequency	360	Hz
	Arm inductance (L_1)	16.2	mH
	SM capacitance (C_1)	24	μF
Stage 2	SM switching frequency	3000	Hz
	Arm inductance (L_2)	2.0	mH
	SM capacitance (C_2)	3.0	μF
HF transformer rated frequency		3000	Hz
HF transformer turn ratio		11400/400	--
LVDC voltage level		400	V
LVDC capacitance (C_L)		1.2	mF
Output inverter switching frequency		1080	Hz
LVAC voltage level		120/240	V
Load active power		2*23	kW
Load power factor		0.94	--

Fig. 3-16 shows the input HVAC voltage and current of the SST. The grid voltage is also shown in this figure. Since the number of SMs in each arm is equal to six, the SST voltage has a seven level waveform. Fig. 3-17 shows the output voltages and current of the SST at the LVAC side. The current is measured after the output LC filter. Since the loads on 120 V terminals are the same, the LVAC currents have the same magnitude. The THD level of the HVAC and LVAC currents are 3.86% and 2.33%, respectively.

The medium-frequency output of the back-to-back converter is shown in Fig. 3-18. This voltage has a seven-level waveform and there is only one switching per level in every half-cycle. Note that this voltage has some fluctuation. The reason of this fluctuation is that the LVDC link has some variation due to existence of single-phase loads. The LVDC link voltage controller tries to compensate these variations by varying the modulation index of the second stage converter. Fig. 3-19 shows the LVDC voltage waveform. The average voltage of the LVDC terminal is 400 V and the voltage variation is limited to ±5%.

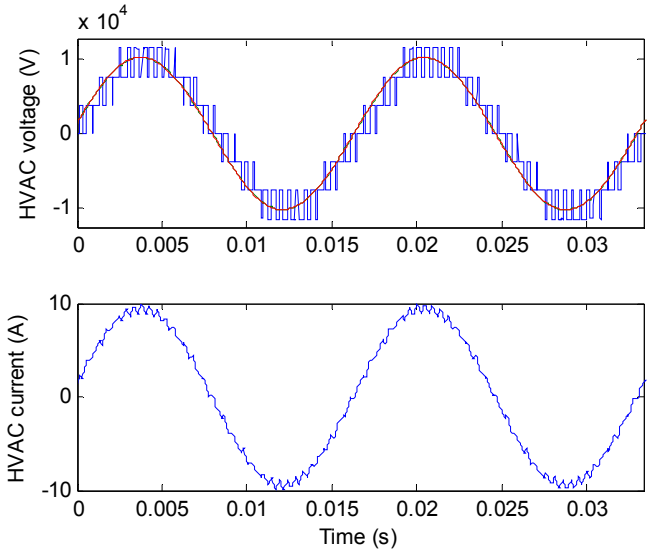


Fig. 3-16. HVAC voltage and current

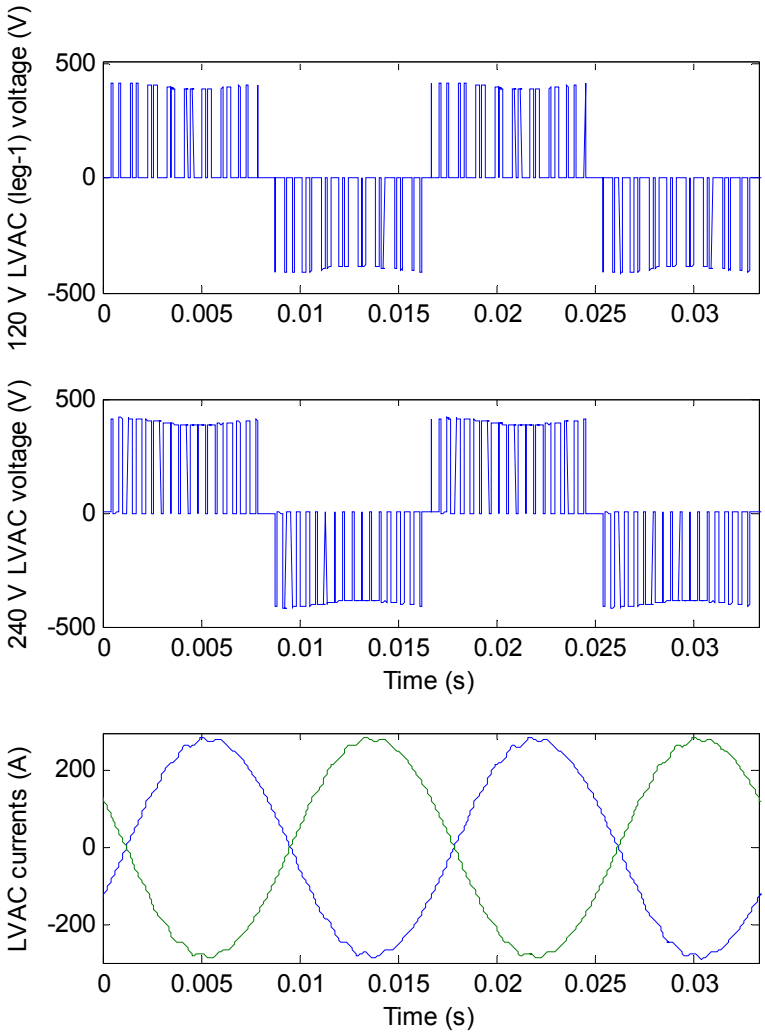


Fig. 3-17. LVAC output voltages and currents

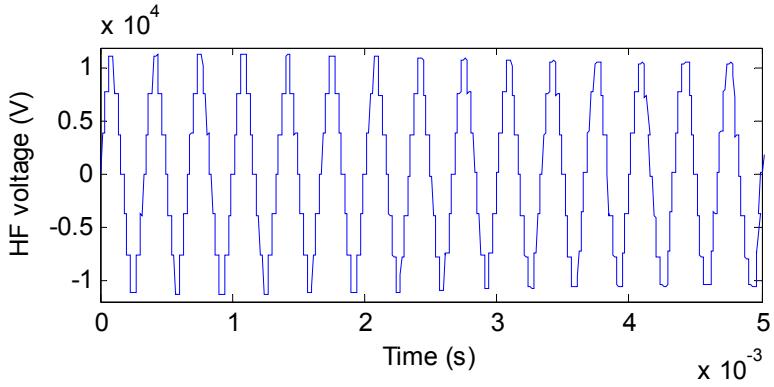


Fig. 3-18. Medium-frequency voltage

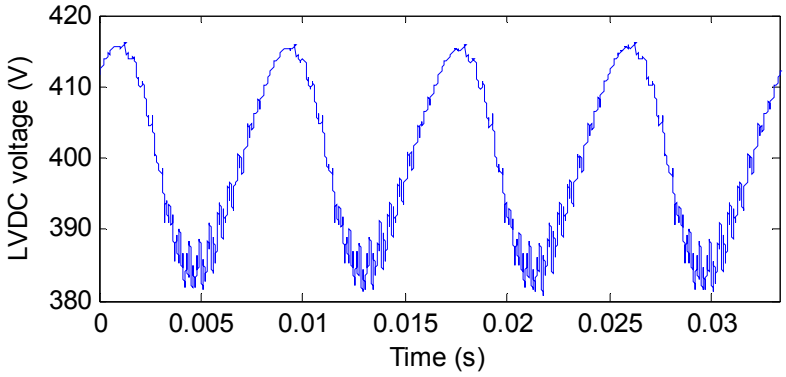


Fig. 3-19. LVDC terminal voltage

Simulation results prove that while the controllers keep the voltages at reference values, the required amount of power is exchanged among the SST terminals.

3.8 Comparison of the Common and the Proposed Topologies

One of the issues with solid state transformers is the device efficiency, which is lower than the efficiency of an LFT with the same capacity. The power loss and the efficiency of the CHB-based SST shown in Fig. 3-1 is reported in [5]. A summary of the data is provided in Table 3-3. The paper uses the DAB transformer loss reported in [71, 72].

Table 3-3. The loss contribution in each stage of the CHB-Based SST

Stage	**Loss**	**Efficiency**
First Stage: Rectifier Stage	2.892%	97.108%
Second Stage: DAB Stage	2.833%	97.166%
Third Stage: Inverter Stage	2.675%	97.325%
Total	8.40%	91.60%

The proposed SST type I is based on the CHB-based SST, while the first stage converter is replaced by an MMC. The MMC efficiency is calculated in this work and the losses in different parts are presented in Table 2-4. As this table shows the converter efficiency is 98.83%. This does not take into account the loss in the inductors. The input inductor loss as presented in [5] is about 0.75% of the converter nominal power, which brings the MMC converter efficiency to 98.08%. The second and third stages of the proposed SST are the same as in the CHB-based SST, which indicates that the same level of power loss is expected in these stages. That means the proposed SST has the loss distribution as indicated in Table 3-4. This table shows that the overall efficiency of the proposed SST Type I is almost 1% higher than a CHB-based SST at the same switching frequency. The Type II SST has the same efficiency as of Type I, as long as the loads connected to its LV terminals are equal. That is due to the fact that there would be no current in the third leg of Type I at this condition. A more detailed investigation into the devices efficiency is left as future research.

Table 3-4. The loss contribution in each stage of the SST Type I

Stage	**Loss**	**Efficiency**
First Stage: Rectifier Stage	1.92%	98.08%
Second Stage: DAB Stage	2.83%	97.17%
Third Stage: Inverter Stage	2.67%	97.32%
Total	7.42%	92.58%

Table 3-5 compares the proposed SSTs with the conventional CHB-based SST regarding the switching and passive components. The numbers in the table are provided for a single-phase 50kVA, 7200/240/120 V SST, assuming DAB converters at the second stage of the SST. The

CHB-based SST's data is extracted or calculated based on the presented data and equations in [5].

Table 3-5. Comparison among the structure of the proposed SSTs and the CHB-Based SST

Topology	**I**	**II**	**III**	**CHB-Based**
HV IGBT voltage level (kV)	6.5	6.5	6.5	6.5
Number of HV IGBTs (First and second stages)	72	72	48	24
LV IGBT voltage level (V)	600	600	600	600
Number of LV IGBT in the second stage	48	48	4	12
Number of LV IGBTs in the third stage	6	4	6	6
Number of HV capacitors	12	12	24	3
HV capacitor voltage level (kV)	3.8	3.8	3.8	3.8
HV capacitance (μF)	24	24	24 / 3	75
Number of HF transformers	12	12	1	3
KVA of each HF transformers	4.2	4.2	50.0	16.7
Voltage ratings of HF transformers (kV)	3.8/0.4	3.8/0.4	11.4/0.4	3.8/0.4
Operating frequency of HF transformers (kHz)	3	3	3	3
High Voltage Side inductor (H)	2*16.2	2*16.2	2*16.2	92

The switches voltage withstand is the same among all the configurations. However, an MMC requires four times higher the number of SMs compared to a CHB converter at the same grid voltage level. That makes the number of HV switches in the first stage of the proposed SSTs to be four times higher compared to the CHB-based converter. The number of low-voltage switches at the second stage of the Type I and Type II SSTs are also four-times the number of low-voltage

switches in the CHB-based SST. The number of high-voltage and/or low-voltage switches in the second stage can be reduced if half-bridge converters are employed.

The number of HV capacitors in the MMC-based configurations is higher than in the CHB-based SST. However, the required capacitance for each is lower. The output capacitor is the same for all the configurations.

The transformer frequency is the same among all the configurations. The Type I and Type II SST have more number of transformers compared to a CHB-based SST. However, the apparent power of these transformers is less in these two configurations. In type III SST only one HF transformer with the capacity equal to the SST capacity is required. The voltage level of this transformer at the primary side is higher compared to those in other configurations. The voltage level of the secondary side is the same in all the configurations.

3.9 Summary

In this chapter, three SST configurations are proposed for a three-stage SST. A modular multilevel converter is used in the first stage of the proposed configurations which enhances the modularity and scalability of the proposed configurations. This facilitates the design and employment of high voltage SSTs. Further, the proposed configurations provide an HVDC terminal which enables these SSTs to interface future DC distribution grids.

The proposed configurations are modeled on MATLAB/Simulink and the obtained results validate the effectiveness of the proposed SSTs in transferring the power among its AC and DC terminals. The capacitors voltages are kept balanced by the controllers.

Chapter 4 - Conclusion and Future Work

4.1 Summary of Work and Conclusion

This thesis investigated the solutions to application of an MMC as a first stage converter of an SST.

In chapter 2, a modified modulation and control scheme for the MMC is proposed which reduces the level of harmonics in the output voltage and current of the converter, while taking advantage of the well-known capacitor voltage balancing algorithm. The effectiveness of the proposed scheme in reducing the level of harmonics is evaluated by the simulation results on MATLAB/Simulink. The FFT analysis is employed to study the harmonic spectrum of the obtained simulation results. Further, the simulation results are validated by means of real-time simulation studies on an OPAL-RT simulator.

Employing the data obtained from the simulations, the loss equations, and the switches' characteristic data from the manufacturer's datasheet, the conduction and switching losses are evaluated and compared between the proposed control scheme and the conventional one. It is shown that assuming the same switching frequency, the proposed scheme proposes a small increase in conduction losses.

In chapter 3, three modular configurations for an SST, based on the application of an MMC as the input converter, have been proposed. The proposed SST configurations are modular and easy to implement and scale to higher voltage levels due to the modularity of the employed MMC. Hence they can be used in higher levels of an electrical grid. This enables the connection of a medium-voltage smart-grid to a high-voltage feeder through an SST.

In addition to the terminals in common SST topologies (i.e. HVAC, LVAC and LVDC), these configurations provide an HVDC terminal. This terminal enables the SST to interface a DC distribution network. The LVDC terminal in this configuration can interface distributed energy resources and storages.

The simulation studies on MATLAB/Simulink verify the performance of the proposed SSTs in delivering the power among their terminals, while maintaining the capacitors voltages balanced.

4.2 Future Work

The proposed SSTs have the feature of scalability to high voltage/ high power levels. These SSTs were simulated and tested to a medium-voltage grid. As future work, these SSTs should be tested on a high voltage grid that requires a higher number of levels in the model.

Since there is no limitation on the number of SMs in a MMC, the number of SMs in the proposed SSTs can be increased which results in higher number of switches and passive elements. However, low voltage switches can be then employed in the SMs. Besides, the switching frequency could be decreased for the same level of harmonic distortion at the output

voltage of the SST. A comparison between employing high and low voltage switches in the proposed SSTs regarding the overall efficiency is an extension to this research.

The simulation results of the proposed modulation in chapter 2 are validated by means of real-time simulation studies. The simulation step frequency (reverse of simulation step time) must be greater than 50 to 100 times of PWM carrier frequency and greater than 20 times the maximum transients or harmonics to be presented at the desired accuracy [74]. In practice, it is proved that the simulation time step should be around 0.25% to 0.5% of the PWM carrier period [74, 75]. This means for an SST with 3 kHz switching frequency a step time of smaller than 1.5 μs is required. This step time is beyond the capacity of high-end real-time simulators. However, a unique technology in RT-LAB simulation platform, called RT-Events, can increase the calculation step time, for the same accuracy in the results [74]. Testing the proposed SSTs on a RT-LAB simulation platform employing RT-Events technology or by means of prototyping is future work.

DAB converters are employed in the proposed configurations as isolated bi-directional DC/DC converters. The other type of converter that might be considered as DC/DC converters at the second stage of an SST is a Dual Active Half-Bridge (DAHB) converter. The number of switches in this converter is half of those in the DAB converter. However, the DAHB converter requires two capacitors at each side of the converter. A modified Type II SST employing DAHB converters at the second stage is illustrated in Fig. 4-1. Design, control and performance comparison of this SST with the proposed SSTs is among the future projects of this research.

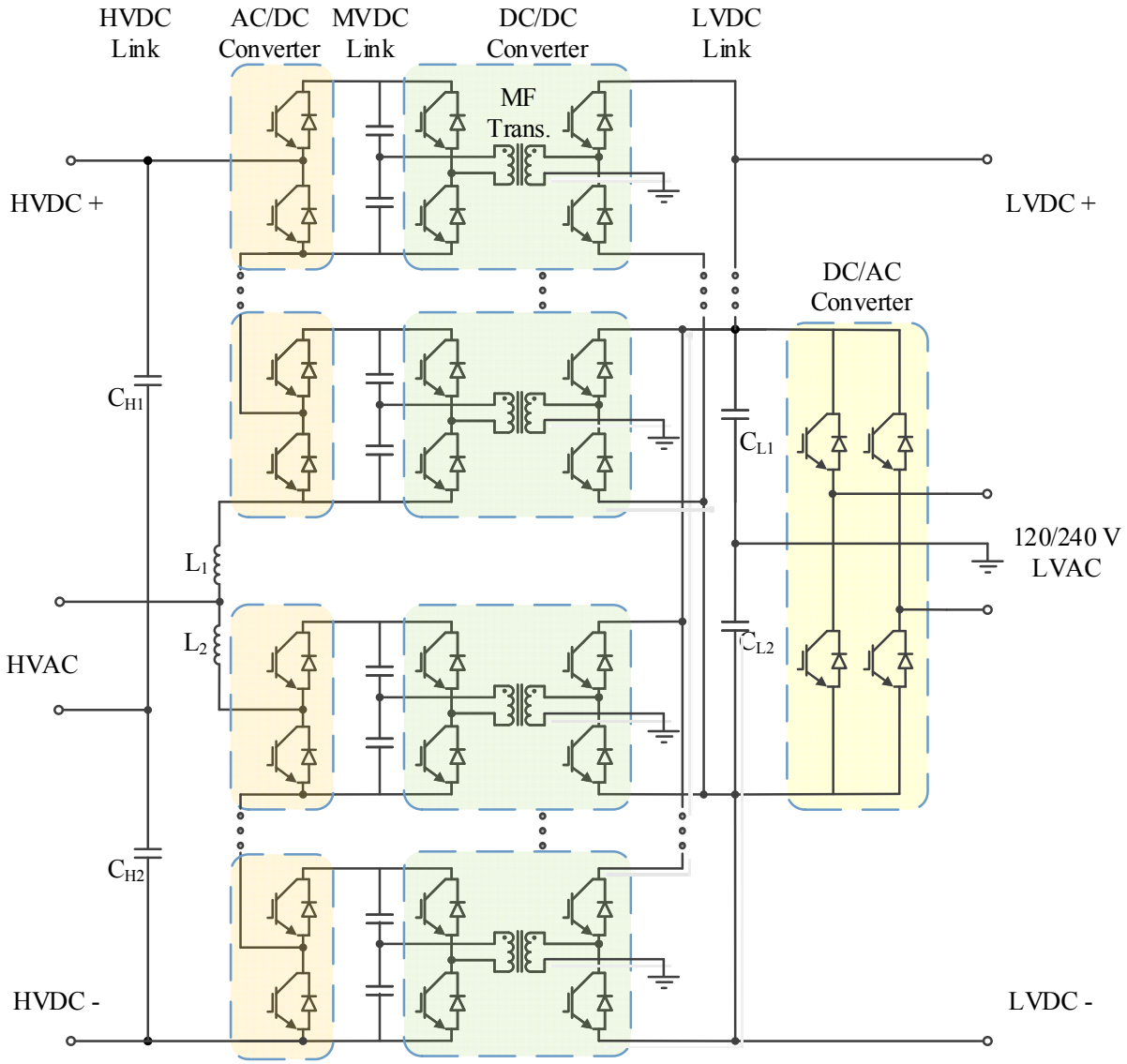


Fig. 4-1. SST Type II, employing DAHB converters at the second stage

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