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Transmitter for an Adaptive Redundant Optical Interconnect

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Table of Content

Abstract

The ever-increasing demand for bandwidth places a more stringent demand on the interconnections within electronic systems. Free space optical interconnection (FSOI) is a technology that satisfies the bandwidth requirements of newer systems. The development of the Vertical Cavity Surface Emitting Laser (VCSEL), which provides high yields and low cost makes FSOI possible. However, the packaging and alignment of opto-electronic components still dominate the manufacturing costs. A solution to the problem of alignment is to use spatial redundancy. One way to accomplish this is by increasing the number of possible optical links and using only a subset of those links to provide a collection of reliable high-speed channels.

This thesis presents the implementation of a transmitter specially developed for a redundant channels alignment FSOI. The implementation consists of a 1.25Gb/s transmitter chip driving one element of a 3x3 VCSEL array. The driver chip was designed and fabricated from a commercial 25-Ghz Silicon bipolar process. The design, construction and integration aspects covering the microelectronics, opto-electronics and packaging for the transmitter are summarized. Characterization results are presented for a transmission rate of 1 Gbit/s per channel.

Sommaire

La demande toujours grandissante pour la bande passante dans les circuits électroniques crée une forte pression sur les interconnexions. Les interconnexions optiques à l'air libre (IOAL) sont une technologie qui offre de satisfaire les besoins en bande passante des nouveaux systèmes. Vue le développement effectué sur les lasers de cavité verticale à émission de surface (VCSEL), ceux-ci ont maintenant de hauts rendements à moindre coût; ceci permet donc de faciliter la création des IOAL. Cependant, l'encapsulation et l'alignement des composants électroniques domine encore les coûts de fabrication. Une solution au problème de l'alignement est d'utiliser la redondance spatiale. Une façon d'accomplir ceci est d'augmenter le nombre de lien possibles et d'utiliser seulement un sous-ensemble de ces liens pour fournir des canaux de communication de haute qualité.

Cette thèse présente la réalisation d'un transmetteur spécialement développé pour une interconnexion optique à canaux redondants. Cette réalisation consiste en une puce de transmission de 1.25Gb/s actionnant un des VCSEL contenu dans une matrice de 3x3 VCSEL. La puce de transmission a été développée et fabriquée avec un procédé commercial de silicone bipolaire 25Ghz. Les aspects du développement, de la construction et de l'intégration couvrant la micro-électronique, l'optoélectronique et l'encapsulation du transmetteur sont résumés. Les résultats de la caractérisation pour une transmission de 1Gb/s sont présentés.

Acknowledgements

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Chapter 1- Introduction

1.1. Motivation

The Semiconductor Industry Association (SIA) road map [1,2], indicates an increasing chip size, density, output pins and aggregate input/output pins for next decades. Clock rate for new high performance processors are forecasted to be in the range of 1600Mhz by 2002 and to reach 3000Mhz by 2011. Interconnects have been represented as the technology with the largest potential technology gaps [1]. Although metallic interconnections are relatively cheap for short distances and are constantly being improved, it is not clear that they could support the required interconnection rates at competitive costs.

In parallel with the evolution toward faster and more powerful digital processors, the communication industry is undergoing a boom in the demand for increased communication capacity [3]. The 30% annual growth in data traffic worldwide has been fueled by the Internet [4]. For the future, Internet is key to the development of new services where the convergence of data, video, voice and wireless technology will provide more flexibility and cost reduction but will demand increasing bandwidth. In the network centric computing age we are entering, the most important resource will be a powerful datacom network [5].

The demand increase will lead to the need to develop ATM and IP routers and switching products with throughputs of 1 Tb/s and beyond. The interconnection needs targeted for a 5 years time frame are in the order of 1-5 Tb/s bi-directional interconnect capacity at the backplane, inter-shelf and inter-frame levels [4].

Current electrical technology used for interconnecting PCBs include coaxial cables, twisted pair and flex microstrip circuits. Metal wire is by far the cheapest medium within its bandwidth and distance limitations. However, the limitations are becoming apparent as the system speeds continue to increase. Those limitations are [6]:

- High power dissipation from line drivers due to the capacitive loading effect of electrical line.
- Difficult power management for the increased power dissipation that comes with higher interconnection density.
- Signal distortion that occurs due to reflection from improperly terminated line.
- Capacitive and inductive cross-talk.
- Attenuation of electromagnetic waves from the finite resistance of the metal conductor.
- Sensitivity to electromagnetic interference.
- Clock and signal skew resulting from delay variation in separate clock and signal path.
- Cost.

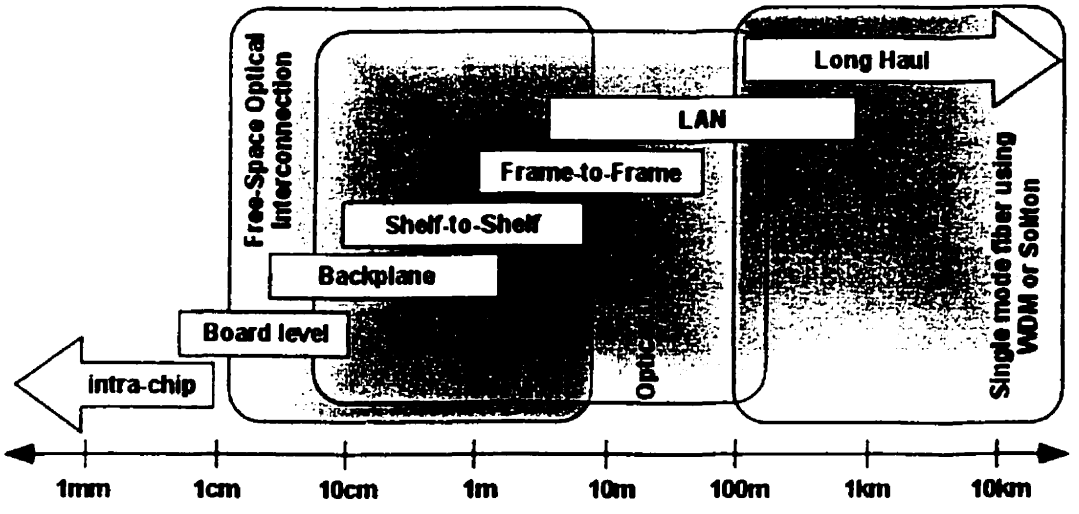

Figure 1.1 System packaging hierarchy vs. Optical interconnection technology

Traditionally, optical communication solutions have been successful in those areas that required longer unrepeated distances than can be provided by copper solutions. Figure 1.1 provides an overview of the conventional digital interconnection hierarchy and their typical lengths. Various optical interconnection alternatives are being researched, including free space optics, individual fiber based arrays, polymer waveguides, and fiber image guides. The cost for metal interconnect becomes a significant part of the

system cost as the bandwidth times distance factor increase. In comparison, the cost for optical interconnection as a function of distance is relatively flat with distance [7]. This explains why as increase in performance are needed, optical solutions become more attractive, the bandwidth time distance factor being higher for high performance systems. Optical interconnection do not only provide a way to reduce cost; they also provide higher interconnection density, less crosstalk, easier impedance matching, better skew performance and higher reliability [6].

1.2. Free space Optical Interconnection

This thesis is concerned with the design and characterization of a transmitter for a Free Space Optical Interconnection (FSOI). FSOI has been the subject of much research in

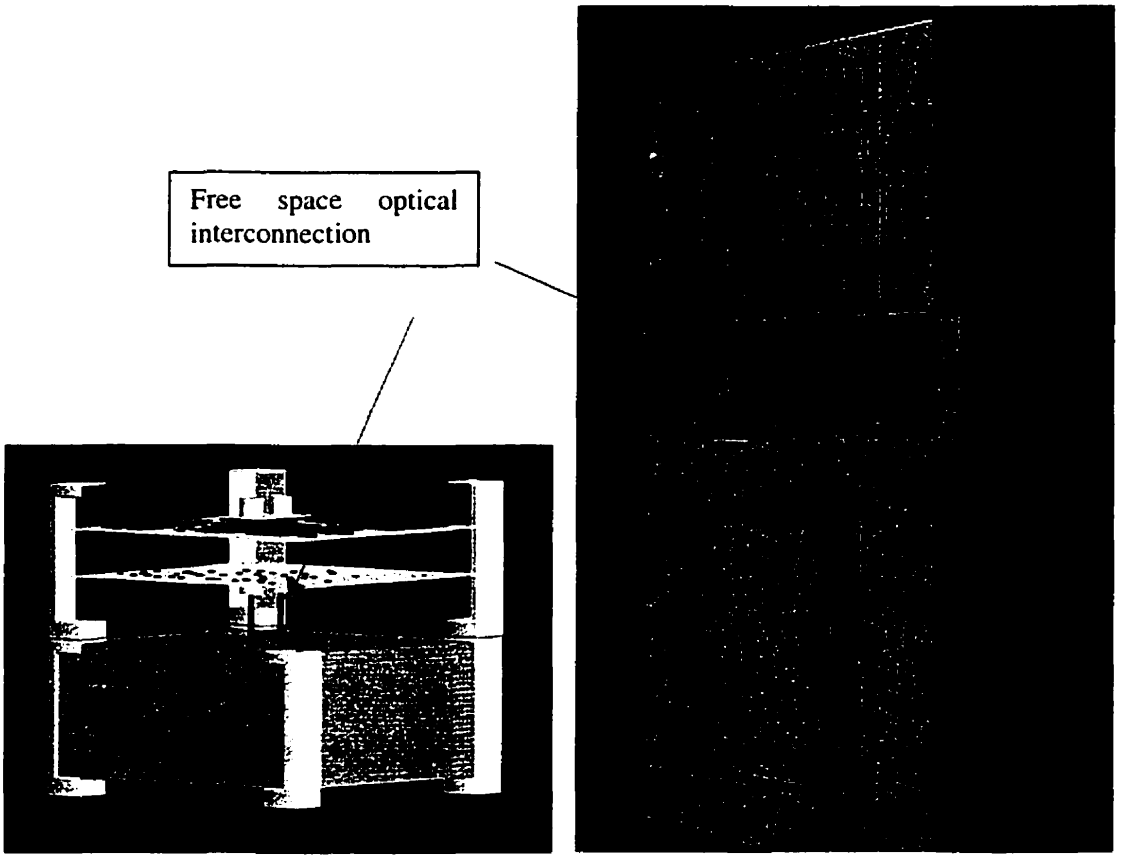

Figure 1.2 Example of usage of FSOI. Left: used in stackable modules type of systems. Allow for hot swap and "easy to install" high-speed interconnection between sub-systems. Right: FSOI used in between shelf of high performance system.

the past years; some of the best examples of interconnections systems can be found in the references [4,9-15]. FSOI offers evolutionary means of extending the performance of electronic technology. Rather than concentrating the light energy using waveguides, FSOI uses imaging systems and bulk material in order to allow for the propagation of the signal from the transmitter to the receiver. One advantage of FSOI is the use of three-dimensional propagation of information thus allowing the conception of very high density interconnections between the transmitter and receiver planes. Low crosstalk is present even for systems featuring thousands of multi-Gb/s I/O. It offers a scalability advantage since no cable or circuit board is needed between the transmitter and receiver; the same devices can be used for connecting system at the intra-shelf or inter-shelf level. FSOI systems do not use connectors and therefore no connector failure arises. In addition, FSOI can be used in order to retrofit existing product lines at low cost since the need for changing the principal back plane can be avoided.

However, FSOI systems present designs challenges in order to become a commercially viable solution. The most critical issues associated with free space optical interconnects are those of misalignment tolerance [8]. The packaging and alignment quality will affect the optical power loss along the optical path and can allow for optical crosstalk in between channels. Loss can compromise the low optical power and the density advantages of the FSOI. In order to increase the alignment quality, advanced manufacturing methods can be used. However, the optoelectronic transmitter and receiver cost might be adversely affected. Other methods of reducing misalignment sensitivity in free space optical interconnects will be introduced throughout this thesis.

FSOI interconnection length is limited principally by the unobstructed distance between the transmitter and the receiver, and the ease to which alignment can be established over the transmission distance. FSOI are best used in the medium-to-short distances as high performance interconnects in digital systems. The economical crossover point where FSOI can be used is principally in the inter-shelf PCB-to-PCB communication. Figure 1.2 shows applications in which FSOIs can be used. As an example, FSOI can become the principal communication trunk in a multi rack system,

the optical link being used principally to offer inter-rack and inter-shelf PCB communication. Another application is as a high-speed bus in between modules of a stackable system. The ease by which free space optical interconnection is established makes the technology attractive to this application. Optical Bus for communications between PCBs are also another application being looked into by many research groups. However, immediate bandwidth/distance needs of electronic systems do not call for the use of the FSOI technology at this level for the moment [4,7].

1.3. Competing optical technology

The following two sections present two selected optical technologies competing with Free space Interconnection. The major difference in interconnect solutions is the media used to propagate the light. This thesis is concerned with the transmitter section of a free space optical interconnection. Many sections of this thesis could also be used for competing technologies. As well, the development made in the competing technologies can help build better free space optical interconnections.

1.3.1. Parallel Fiber interconnection

Parallel fiber interconnection has attracted many research group through out the past years [16-19]. This type of interconnection involves combining several fiber links in a parallel fashion. Parallel fiber interconnection is presently being offered in commercial versions using newly developed VCSEL arrays and parallel fiber connectors. One commercial solution is offering up to 30 Gb/s unidirectional [20]. These solutions are still far from the 5Tb/s demanded for high end applications as an example one would need to use a 167 link of that type in order to provide enough bandwidth. As an attempt to increase the link density, 2D transmission channels are being examined [19]. However, fiber array systems will face some problems in increasing the channel density. One of those problems is that fibers themselves are expensive and inflexible. The second problem is the one of alignment of the fiber to the emitter and detector. This alignment will become remarkably difficult as the number of channels increases. Free space optical interconnections are not affected by these problems since they do not require alignment to a fiber for every individual channel.

1.3.2. Fiber image guides

One propagation medium that allows the desired density to be implemented is fiber image guides [21-23]. Fiber image guides were originally developed to be used as various imaging and sensing tools in medical diagnostics as well as in industrial inspection applications. A fiber image guide consists of a coherent bundle of individual step-index fibers. The core of the fibers can be as small as 3μm and can be separated by as little as 5μm [21]. This configuration allows fiber image guides to exactly copy the transmission pattern from the input end to the output end. By doing so, the alignment of dense link matrix could be eased; putting that technology in direct competition with free space interconnections.

1.4. Thesis Organization

This thesis deals with the design and test of a fully packaged transmitter chip. The transmitter design included the choice and cauterization of the light emitting technology, the design, test and cauterization of a high-performance silicon driver chip and the design and test of the packaging and control circuitry for the transmitter chip. Chapter 2 will give an overview of the methods used to overcome the alignment problems within a free space optical interconnection. Following this overview, the architecture of a system using extra transmitters and detectors in order to account for misalignment will be described. This section contains work provided by the other contributors to the project. This an overview of the optics, receiver, and algorithms used in the project to give the reader a more global context for the transmitter use. Chapter 3 will give an overview of the emitter technology, which is mainly a VCSEL. Parallel optical interconnections would have been a lot harder to conceive without this technology. This overview will be presented along with the characterization of the VCSELs used for the implementation of the interconnection. Chapter 4 will present the architecture and the design of the transmitter. Also, the packaging of the transmitter will be discussed. Chapter 5 is concerned with the testing of the transmitter section of the optical interconnection. Finally, the last chapter will conclude the thesis and suggest idea for future work.

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Chapter 2- The Adaptive Redundant Optical Interconnection

2.1. Introduction

One of the most important challenges preventing the acceptance of free space optics is the skepticism concerning the issue of alignment [1]. In order to have a reliable free space optical interconnect, the emitters, detectors and optical elements have to be aligned to each other within very tight tolerances (10μm). The ability of creating such an alignment will determine the success of the interconnection. Failure to meet the tolerance budget normally impact the system performance. Poor bit error performance (lower than BER than 10^{-9}) can be a sign of misalignment. An optical data link should be reliable, low cost, eye safe, easy to install, easy to maintain and compatible to existing systems.

The ability with which one can control the alignment will directly affect the power budget of the optical interconnection. In addition, if a parallel interconnection is to be implemented, optical crosstalk could occurs between optical links adding noise to the transmission system. Both problems would have a non-desirable effect on the bit error rate (BER) of the interconnection. Considering that the bit error rate for today's datacom systems easily attain 10^{-15} errors per transmitted bit [2], we do not have to stress how much the quality of alignment is important in a free space optical interconnection. The quality of this alignment does not only have to be achieved on the first time alignment of a system, but also has to be maintained during its lifetime despite vibration, shock, and environmental fluctuation.

The ease of the alignment is another factor that must be addressed. One cannot always have a team of highly trained researchers on hand to build and fix each systems one a time. The systems have to be simple to align to reduce installation and maintenance costs.

The goal of this chapter is to first review the techniques used in order to make free space optical interconnections tolerant to optical misalignment. The second part of the chapter will present a new free space optical interconnection architecture that proposes to make the alignment digitally adaptive using redundant optical links.

2.2. Static optical interconnection

One possible solution to produce an aligned system is to have a rigid mechanical structure that will not allow the beams to drift out of alignment. Most interconnect systems demonstrated to date uses this kind of approach [3-10]. Boisset et al. used precision machine base-plates in order to keep the optical elements in place. Some of the elements are mounted in precision-machined cells and every cell are deposited on precision-machined slots. Typically, the alignment precision required for rigid systems are on the order of 10um. This kind of system is usually difficult to align and will be very susceptible to environment changes and shock. Also, the alignment mechanisms are not simple and require highly trained personnel in order to achieve the predicted performance.

One solution to these problems is to make the optical system tolerant to misalignment at the design level. Robertson outlined this approach while describing the optical design of a free space optical interconnect [3]. However, even when ingenuity is used in order to increase the tolerances, the task of achieving the required alignments still poses many difficulties. Special alignment methods have to be put in place in order to make the system alignment realizable [4]. In order to realize the system described by Robertson; the optical system components have to be grouped into modules. Every module has to be assembled on an individual basis in specialized setups using interferometric methods [7]. The modularization process permits relaxed tolerances on the opto-mechanics and makes the assembly a more trivial task. The favored assembly method is to provide kinematic interfaces to every module. The complexity and the

difficulty of implementation of such a system can easily be appreciated just by looking at Figure 2.1.

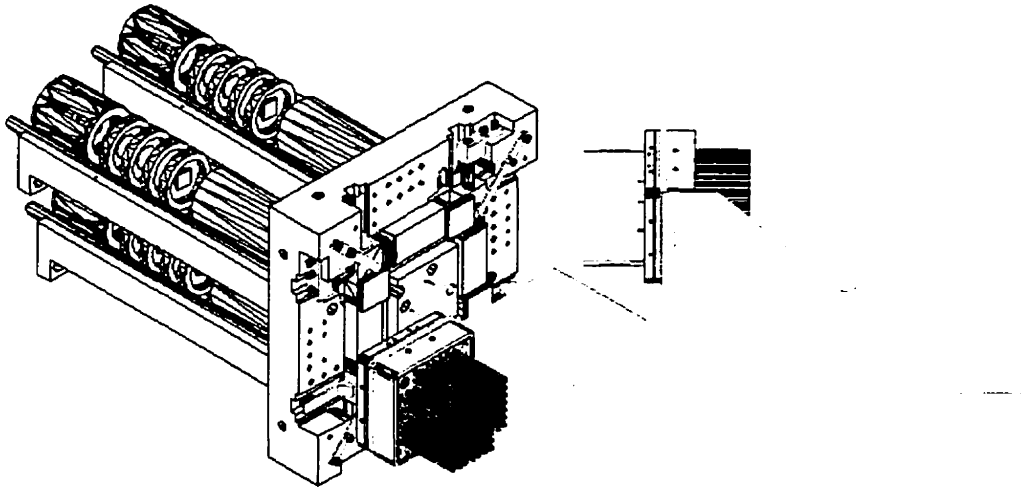

Figure 2.1 Final implementation for the interconnection presented in reference [3]

Even when using state of the art techniques in order to realize the alignment, rigid interconnection poses many problems to designers. The rigid interconnection technique becomes harder to implement as distances between stages increase. The manufacturing yield for the realization of mass produced systems might be problematic. Every part has to be perfect; any error in manufacturing makes the initial alignment many times harder to realize [4]. Rigid interconnection systems count on mechanical rigidity in order to provide reliable systems over time. Those systems have to be directed toward short distance interconnections like board-to-board or chip-to-chip applications. This is because alignment is easier to maintain on smaller distances since for the same mechanical defect the displacement of optical parts will be smaller on smaller distances.

Other types of static interconnections use a spread beam in order to create an alignment tolerance. By "spraying" the light from the transmitter to the receiver, they avoid complex imaging systems. This technique however wastes a lot of power which lead

to low receiver power limiting the possible speed. In the same way, the angle of divergence of the beam and the length of the link will limit the interconnection density. An example of this type of system is also the only product deployment of short-length FSOI to date. The diffuse link of the IRDA (Infra-red Data Association) permits links up to 4Mb/s. Another example of that type of interconnection using the techniques of spread beam is the interconnection presented by Goodwill [11]. This free space interconnection has a tolerance of ±1mm and ±1°. However, this technique is not extendable to dense arrays and does not possess the main advantages claimed by FSOI: high speeds and extremely high densities.

2.3. Dynamic optical interconnection

Another solution to the alignment problem is to have the system adapt the alignment to changes in the environment by using active steering elements [12-15]. Using this technique, the optical channels are positioned in alignment using optical MEMS (Micro Electro Mechanical Systems), liquid–crystals, adjustable liquid prisms, or any other beam steering devices. Normally, this type of interconnection will use a reference beam in parallel with the beam array of the optical link. The position of the reference beam is read by an xy-positioning sensor, and the output of the sensor is fed back to the controller of the optical beam deflector in order to optimize beam alignment. Results obtained by Hirabyashi [14] using an active realignment system look very promising. The system can correct for alignment error of the order of ±66μm. When the active alignment system is used, the alignment error is maintained to ±10μm. The alignment error is maintained minimal despite multiple card insertions and extractions, or shocks on the order of hundreds of G. This demonstration is the proof that misalignment tolerance can be increased by an active control system.

2.4. Redundant interconnection

Dynamic alignment free space optical interconnections are attractive because of their robustness. However, reliability is still of concern. Moving parts, like the one used in dynamic alignment interconnections, are usually many times less reliable than today's electronics. In order to gain acceptance within electronic systems, those devices will have to prove their reliability over time and environmental conditions. A solution exists to make the alignment dynamic without having to use active steering elements. The solution is to use redundant detectors and emitters. The concept of redundancy has been introduced only recently by various authors [1, 16-17] as a possible solution for making free space interconnections a viable solution to the alignment problem. However, no system and chip set has ever been developed in order to explore the possibility offered by the concept. The idea is quite simple: by adding extra detector and transmitters, one can increase the number of degrees of liberty the emitter and detector can have in order to be aligned. By routing the transmitted signals in an ordered fashion through the aligned subset, one can ensure a greater tolerance to angular and lateral misalignment. As an example, in the system presented by Plant [17], only a single active transmission channel was available at all time; however, the detectors and emitters were using 3x3 arrays of laser and detectors. Figure 2.2 depicts the channel configuration. This arrangement gave 81 possible combinations of emitter-detector pairs in order to achieve a working communication channel. The alignment between the boards was as large as $\pm 1°$ and ± 1mm across the combinations. If perfect alignment were to be realized, both the center elements of the emitter and detector arrays would be selected in order to produce the communication channel. The two arrays are allowed to drift out of alignment as long as one emitter-detector pair is available.

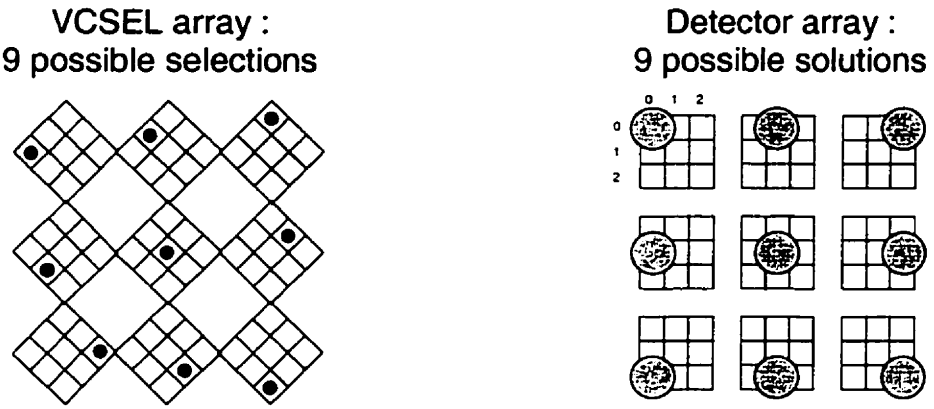

Figure 2.2 Emitter, detector redundancy concept

It is important to note that in the prefect alignment condition, the peripheral emitters and detectors in the array are not in alignment; the light from the edge of the emitter array falls outside the detector plane. In order to make the system as tolerant as possible, the optical system that is built in between the opto-electronic arrays is designed in such a way that the VCSEL light widely overfills the detector array area. This allows the detector switching to provide a fine alignment adjustment as the emitter switch corrects for larger displacement. The situation is depicted in Figure 2.3. The VCSEL array was at a 45° angle with respect to the detector array in the system. The available detector arrays and VCSEL arrays both had the same device pitch. By using an angled configuration, the horizontal pitch between the VCSEL and the detector was made different, which stabilized the channel coupling throughout displacement.

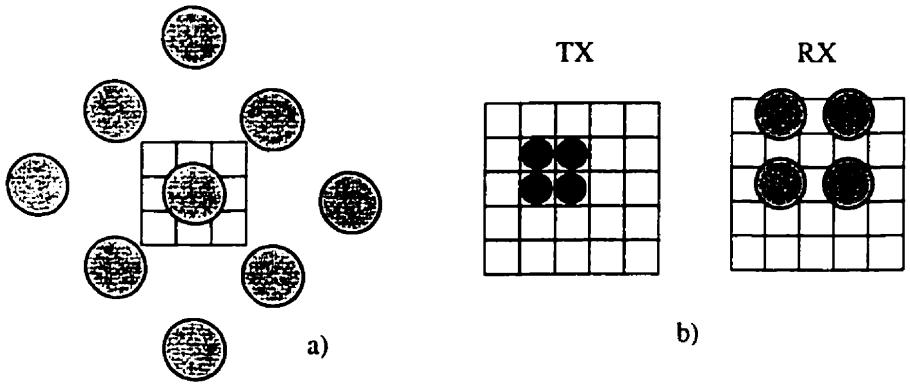

Figure 2.3 a) Image of the array of light from the VCSEL array with respect to the detector array when in perfect alignment. b) Example of a 2x2 interconnect.

Redundant interconnections were especially developed to increase the misalignment tolerances of dense optical interconnections. Scalability of redundant interconnection is therefore a subject that should be investigated. Figure 2.3 b) shows a method to scale to a redundant interconnection for a 2x2 interconnection. As can be seen in the figure, the optical beams do not fall on adjacent detectors. This architecture is necessary in order to take into account for crosstalk; enough space has to be maintained in between the optical beams in order to ensure that two optical channels will not fall on the same detector. The additional detectors ensure continuity in the signal coupling as the emitters and detectors fall out of alignment. Following this architecture, the number of extra emitter and detector that are needed for redundancy decrease as the array density increase. The number of emitter and detector needed for redundancy can easily be calculated using simple arithmetic.

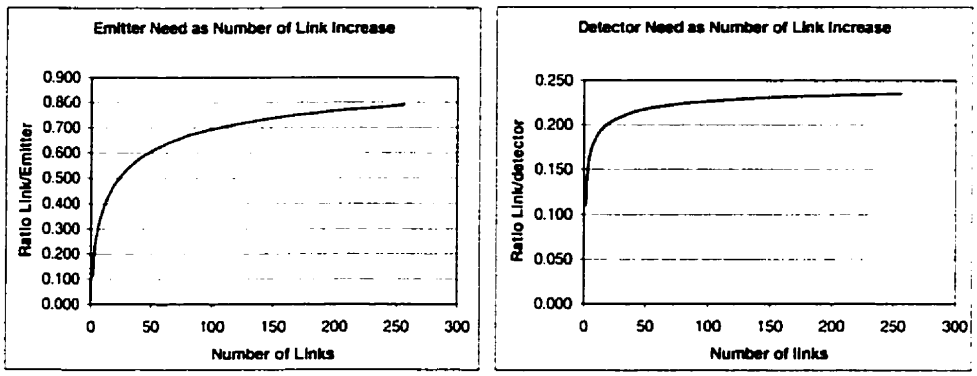

Figure 2.4 Emitter and detector need, as the interconnection is scaled

Figure 2.4 shows how the presented architecture scales as the number of links is increased. The link-to-emitter ratio needed for redundancy tends to 1 as the link density is increased. The link-to-detector ratio needed for redundancy tends to 0.25 as the link density is increased because of the extra detectors needed to minimize cross-talk. As the density of optical links is increased, the cost per link should decrease. This is because less detectors and emitters are needed in order to maintain the redundancy. In addition, the cost for adding intelligence to align the matrix is a fixed cost, therefore a lower cost as the density is increased.

Redundant interconnections provide a tradeoff between the static interconnections and the dynamic interconnections. By using only static electronic elements, they provide single elements reliability similar to the one provided by static interconnects. The channel redundancy and control systems allow for relaxed tolerances, making the alignment of the interconnect more easy to realize. Density is also preserved as dense interconnection can be achieved when using very large arrays. While providing a way to adjust the alignment dynamically, the redundant approach allows for the creation of a generic component that can be included in any system just like chips are included on a PCB board. By having very large misalignment tolerances, the redundant interconnection does not require a special rigid mechanical system to be developed in order to maintain the boards in a reasonable alignment. The standard methods used to

mount boards in systems can be used. This removes many or all of the problems that an engineer would face when including a free space interconnection in their system. The modules are self-contained and only their position has to be planned such as holes are made in the electronic enclosure when designing a PCB. In conclusion, adaptive redundant FSOI are easy to use dense, rapid, and misalignment friendly, making them one of the ideal FSOI one could design for use in an industrial environment.

2.5. System Implementation

This thesis is aimed at describing the design and test of an optical transmitter that was developed especially for a redundant FSOI. In this section, the full interconnection system will be introduced to give the context in which the transmitter is to be used. The system is designed to interconnect two boards with two bi-directional optical channels operating at 1.25Gb/s each over a distance of 5cm to 22 cm [17]. The two boards can have a lateral misalignment tolerance of ±1 mm and an angular tolerance of ±1°. The tolerance provided by the redundancy is loose enough to enable the use of the interconnection with standard board insertion tolerances normally available in between board in a rack system or between stackable modules. The system developed for this thesis employed a 3 X 3 array of VCSELs and 3 X 3 array of photo diodes for each channel. The selection of the transmitter-receiver pair in the array that gives the optimum performance is determined by a feed back control mechanism. In this implementation of the system, the control information is transmitted optically such that the system can operate with no electrical connections (except for the power connection). For the system development, a transmitter, an optical system, a receiver, and an alignment controller were developed. A graphical representation of the FSOI system is illustrated in Figure 2.5.

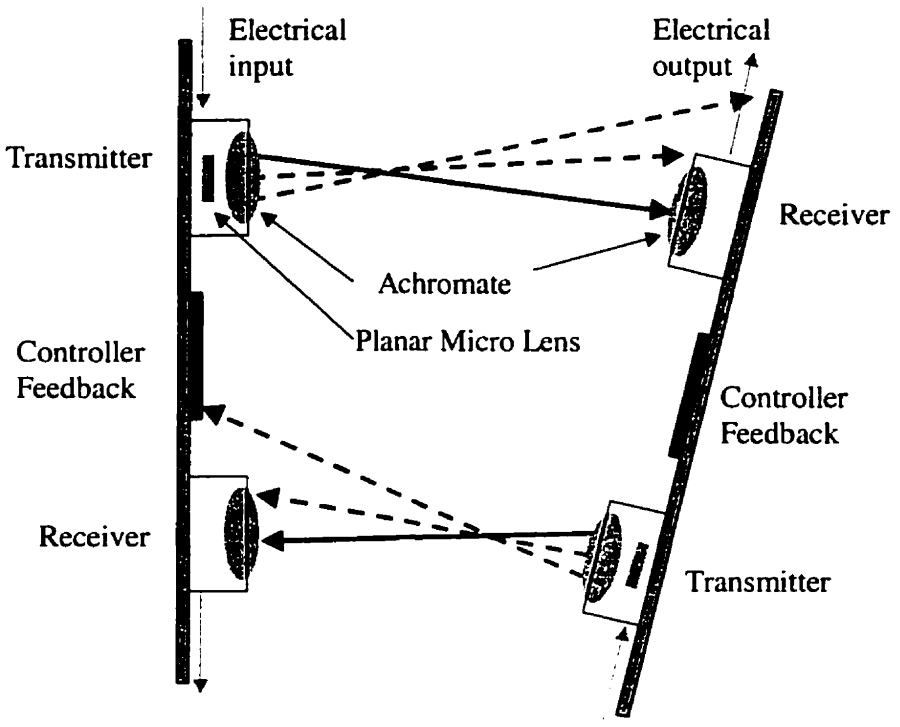

Figure 2.5 Bi-directional redundant interconnect

2.5.1. Transmitter

The transmitter Module consists of a 1 x 9 VCSEL driver, a 3x3 960nm VCSEL array, a ceramic carrier, a mount for a micro-lens array, and a bulk lens. The transmitter chip was designed using the NT25 technology. The transmitter takes two 1.25Gb/s PECL signals from two different sources and distributes them to nine VCSELs. This thesis gives a complete description of the transmitter.

2.5.2. Optical system

The design challenge addressed in developing the optical system for this free space optical interconnect based on redundancy was to provide the lateral misalignment of +/- 1mm and tilt tolerance of +/-1° over a distance of 5 to 22 cm. The optical system is shown in Figure 2.6. It consists of a planar micro-lens array (PML) and a 12.77mm

focal length achromatic lens with 6.25mm diameter on the transmitter. A 250μm glass spacer was inserted between the VCSELs and the PML in order to maintain the optical distance between these two components while increasing the physical distance. This allowed for the large PML substrate to be fixed at a slightly larger distance from the VCSEL array allocating more space for the electronic packaging, wirebonds, and air flow. On the receiver side, only one lens is used: a 14.22mm focal length achromatic lens with a 13.00mm diameter.

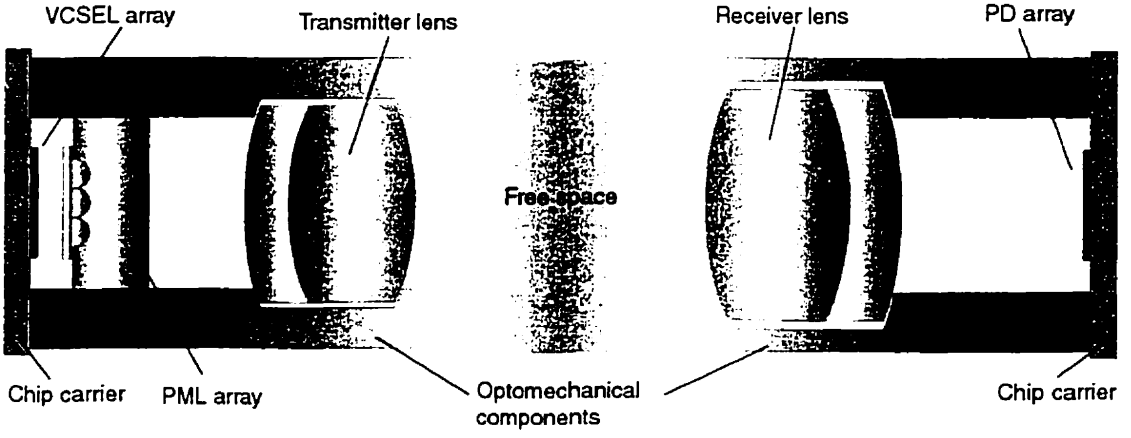

Figure 2.6 Optical system[19]

The optical beams from the VCSEL array are collimated by the PML array and then distributed angularly by the transmitter bulk lens. The beams then propagate in free space for a distance of 5cm to 21.5cm depending on the distance between the PCBs. The beams are then collected by the receiver lens and "focused" onto the detector array. Note that the spots do not have to be exactly focused on the detectors; only the spot size at the detector is important in this optical system. The distance between the different components has been optimized through mathematical simulations in order to provide the best coupling between the emitters (VCSEL) and the detectors (PD) across misalignment conditions, emitter-detector combinations, and distance between the modules.

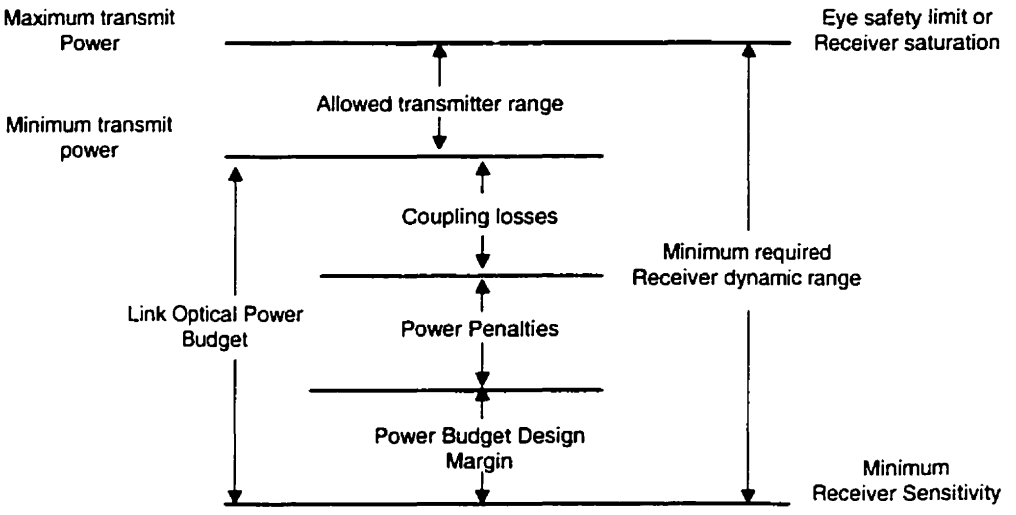

Figure 2.7 Power budget for an optical interconnection

The alignment tolerance for the optical system is tightly linked to the power budget for the optical link. Figure 2.7 shows a picture representing the power budget for an optical interconnection. The minimum receiver sensitivity for the interconnection was established to be –23dBm. The minimum transmitted power is –6dBm. This allows a power budget of 17dB. Unlike fiber interconnections, the major part of the power budget is consumed in the coupling between the transmitter and the receiver. The coupling was optimized such that it would be minimal over the different VCSEL/PD combinations. Figure 2.8 shows that the calculated coupling loss for the interconnection is never over 14dB across the interconnection alignment tolerance range VCSEL/PD combination. The power penalties such as the inter-symbol interference, the relative intensity noise, and jitter penalty, which account for the signal degradation over the interconnection, are evaluated to less than 1dB due to the very short distance crossed by the interconnect. The design margin for the interconnection is 2dB guarantying valid system performance over the target tolerance.

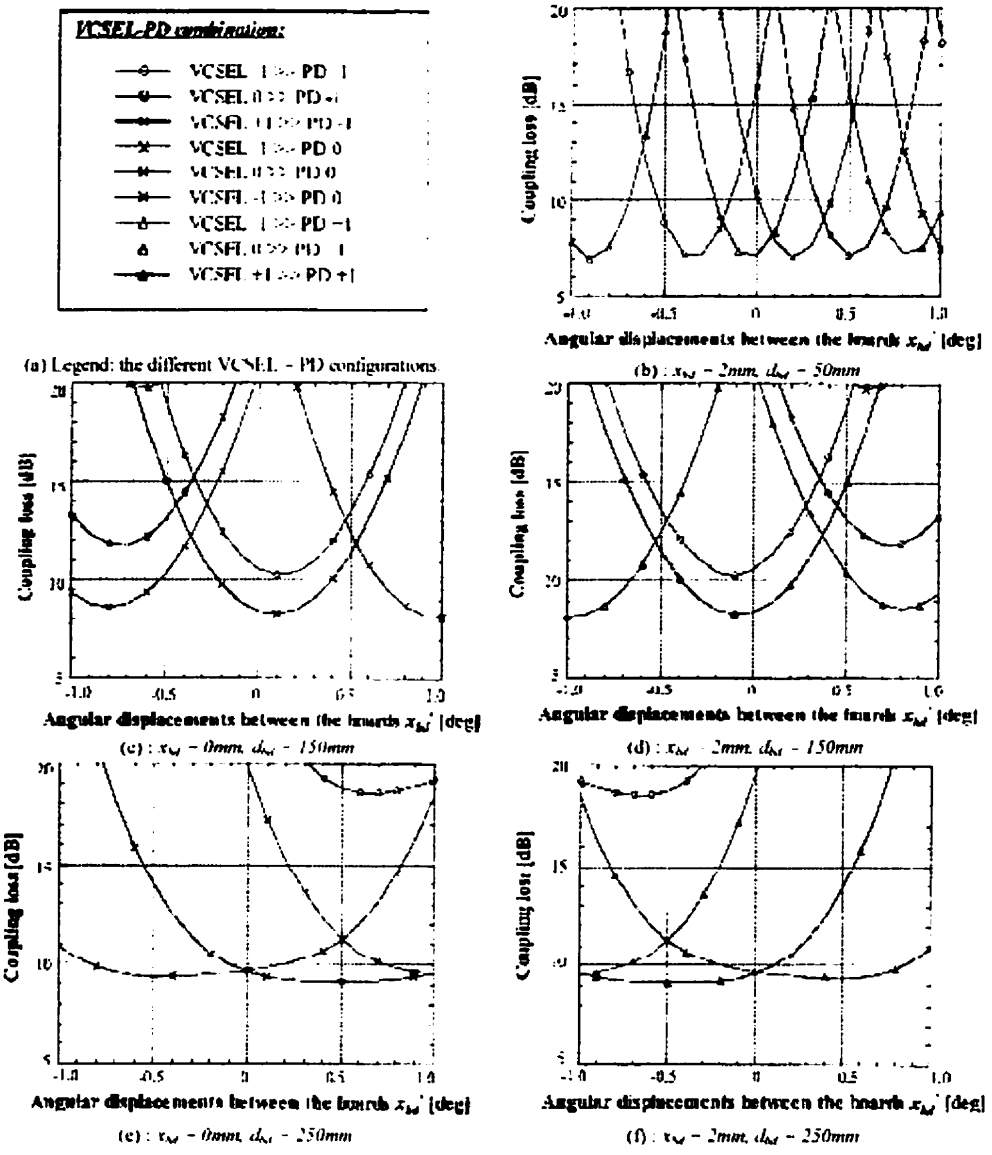

Figure 2.8 Coupling behavior of the optical system. The distance between the boards (d_{bd}) and the lateral misalignment (x_{bd}) are given for every plot. [27] (Calculated using Gaussian beam formalism using Mathematica[tm])

2.5.3. Receiver

The receiver module consists of a 9x1 receiver array, a 3x3 photo detector array, a ceramic carrier, and an optomechanical mount for a bulk lens. The module receives the optical data at 960nm. The photocurrents from the photodiodes are all preamplified to a suitable voltage swing using 9 transimpedance amplifier single-ended gain stages.

From these nine signals, one is selected through two stages of 3-to-1 analog switches. The signal is then converted in a differential PECL compatible format through a last stage of amplification. The receiver block diagram is shown in Figure 2.9. A more detailed description of the receiver along with test results was described by the receiver designer Mony [18].

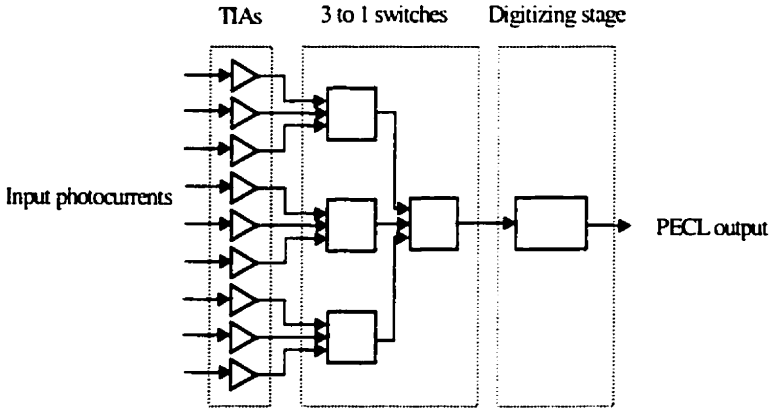

Figure 2.9 Receiver block diagram [18]

2.5.4. Optical Feedback (Hunt mechanism)

Optical feedback is an integral part of the redundant adaptive interconnection. It is possible to determine which detector receives the most light using a simple algorithm for which all decision and control mechanisms reside only on the receiver side. However, knowing which set of transmitters is aligned to the detectors is more difficult. Controlling the transmitter plane requires communication between the transmitter and the receiver in order to determine which combination of emitters and detectors will give the optimum performance. The feedback task has to be achieved by a communication channel parallel to the main transmission links.

This transmission channel can take different shapes: a very tolerant infrared link (IrDA like link), twisted pair, or it could also use the main communication channel. The system can use the high-speed data channel in order to communicate the feedback information given that no data is transmitted at the same time. Even if the interconnect

is not yet aligned, the signals can pass through by transmitting on all possible communication channels. This is done by modulating all VCSELs at the same time. In this case, the links will have to be operated at lower speeds in order to compensate for the power surge created by transmitting on all the lasers at the same time.

Figure 2.10 shows a simplified version of the algorithm used in the implementation of the interconnect system. The boards are first defined as master or slave by a hardware switch. This selection determines each boards state at the state of the algorighm. The first step is to synchronize the boards. To achieve the synchronization, the master board powers up all the VCSELs of the communication channel. As soon as the slave board detects the signal transmitted by the master board, it also powers up all available VCSELs. The master board detects the signal and as soon as the slave stops transmitting, both modules step into the second phase of the hunt algorithm. This movement will happen for both boards approximately at the same time; hence, the two boards are synchronized. Note here that the alignment will happen only if it is possible to align the two boards. Also, the synchronization tolerance will depend on the logic response time which is designed to be order of magnitudes faster than the circuit clock to make the synchronization inconsequential. If one link is too misaligned to produce at least one good communication channel, the algorithm will stop here since at least one board will never receive acknowledgement of the existence of a second board.

The next step involves finding the best VCSEL-PD pair by scanning through all the VCSELs on the master board and finding the receiver channel that received the highest power. The information about which VCSEL is providing the best transmission channel is known by the receiver plane since the scan pattern of the VCSEL plane and the time at which each VCSEL is exercised during the scan is predetermined. Based on the premises that both transmitters and receivers are synchronized, the information about the time at which the good transmission link occurred and therefore which VCSEL provides the best transmission media is sent back to the master board. At the end of a cycle, both the master and slave exchange roles to find the best VCSEL-PD pairs for the other direction. Once both VCSEL-PD pair have been found, the data is

transmitted across the two channels. If one of the receivers senses the power dropping on the channel used to sample the signal, all data transmission is stopped and the alignment algorithm begins again to find the new optimum value for transmission.

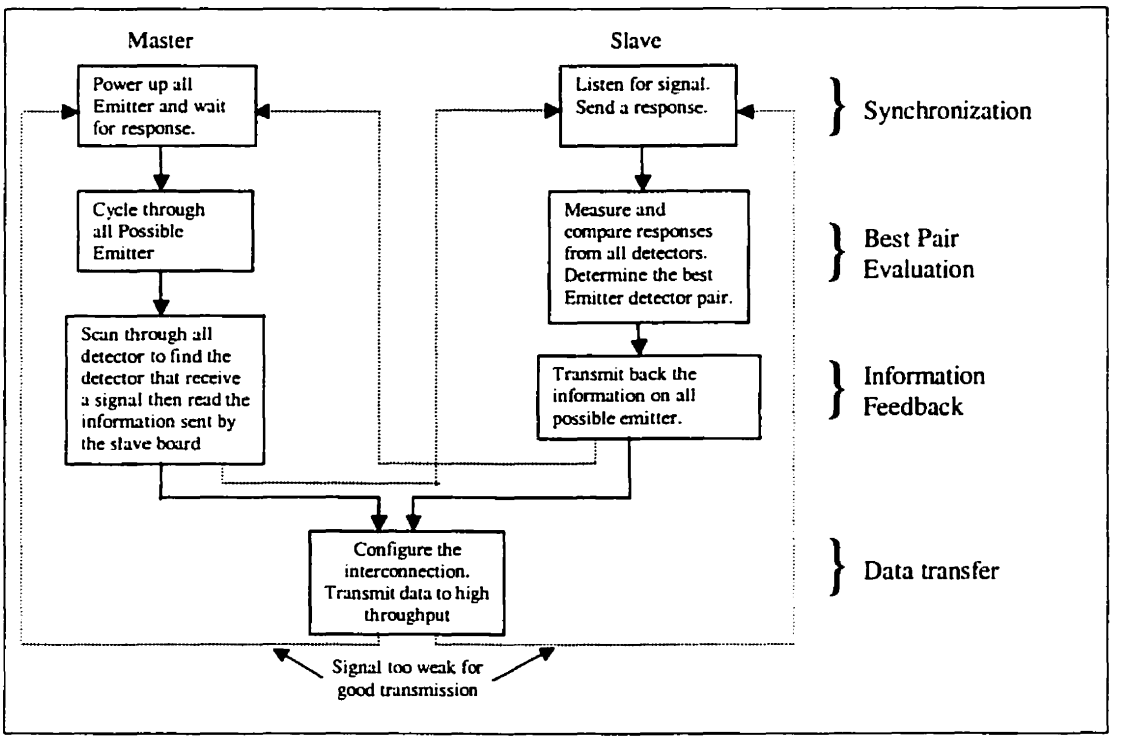

Figure 2.10 Flow diagram for the alignment algorithm [17]

The ability to adapt to changes in the interconnection alignment will greatly impact the robustness of the system. In the implementation presented here, the high-speed communication has to be stopped when the interconnection senses a misalignment. This occurs to allow the hunt algorithm to run again and calculate the new position of the emitter array with respect to the detector array. The communication channels used for the feedback only exist when no data is transmitted through the interconnection. There would be some advantages in using a permanent transmission medium for the feedback. If a permanent communication channel was used, a prediction algorithm could calculate the drift direction and allow for a seamless emitter-detector transition as the drift occurs, therefore causing no data disruption. In the case where the feed back information has to travel using the same communication link, a special communication

protocol would have to be used in order to allow for the coding of the drift information on top of the data. This would demand a considerable effort by itself and was therefore left for future investigations.

2.5.5. Speed and Communication protocol

The communication channel speed targeted for the system was 1.25 Gb/s. This transmission rate is the same as Gigabit Ethernet and is large enough to accommodate a fiber channel compliant signal. By choosing a transmission rate the same as an already available standard, the access to commercially available communication protocol chip sets is guaranteed. This allowed the design effort to be concentrated on the media and not to be disturbed by the development a special communication protocol. The transmission rate was also the fastest for which our research group was capable of testing.

Gigabit Ethernet protocol might not be the best solution for an adaptive free space optical interconnection. The ideal protocol would allow for channel maintaining information encoded on top of the transmitted data. As an example, the data could be framed in a special packet allowing the link status to be transmitted with the transmitted data. Other functions like error correction could be taking place with that header making the link more tolerant to loss of packets accruing from interruptions caused by channel reconfiguration. The availability of a working adaptive redundant optical interconnection will allow for the exploration of this hypothesis.

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Chapter 3- Single-mode VCSEL for FSOI

3.1. Introduction

Candidate transmitter technologies for free space optical interconnections have included both emitters and modulators: LEDs, PLZT modulators, VCSELs and electro-absorption (EA) modulators. Although many technologies are possible candidates to generate or modulate light in optical interconnections, not many have all the necessary qualities. The cutoff frequency of LED is much too low to be generating Gb/s data streams. Modulators require an external optical power supply which complicates alignment to the point where systems become very difficult to align. Arrayed single-mode high-speed VCSELs are a prerequisite for dependable, easy to align FSOI. VCSELs have some exceptional electrical and optical properties. As a result, they are quickly achieving market acceptance.

Some of the most attractive aspects of VCSEL versus edge emitter lasers lie in the elimination of the labor intensive fabrication steps such as wafer lapping, cleaving, dicing, and facet coating. The possibility to fabricate and test lasers on a wafer scale and perform non-intrusive testing is a differentiating factor of VCSELs over edge emitters. In addition, the possibility of making two-dimensional (2D) arrays from very small lasers makes VCSEL very attractive [1]. Optical interconnections, optical communication, optical recording, optical signal processing and sensor technology are only a small subset of all applications made possible by VCSELs.

This chapter will first give an overview of VCSEL structures and properties. Then, the VCSELs used for the redundant adaptive free space optical interconnection will be presented. Finally, the results from VCSEL evaluation will be commented.

3.2. VCSEL technology over view

Vertical-cavity emitting lasers were invented at the Tokyo Institute of Technology in 1978 [2] and achieved room-temperature continuous-wave operation for the first time in 1988 [3]. Since the mid 1990s, several companies have been launched in VCSEL manufacturing and many applications have penetrated the market place. The fundamental difference between VCSELs and conventional edge-emitting lasers is that the need to fabricate a facet mirror by either cleaving or dry etching is eliminated. Because of their perpendicular emission, VCSELs have several advantages over edge-emitting lasers such as low divergence, circular output beam, wafer-level device testing before packaging, and the feasibility of dense two-dimensional laser arrays. However, similar to the edge-emitting lasers, VCSELs need a mean to provide transverse confinement of photons and charge carriers within the cavity. Figure 3.1 shows schematically the primary VCSEL structures that are used to provide transverse optical and electrical confinement from which are based the VCSELs types: etched-air post, ion-implanted, etched/regrown, and selectively oxidized VCSELs.

Modern VCSEL consist of two highly reflective DBR (distributed brag reflector) mirrors separated by an optical cavity. The DBR surrounding the optical cavity are required for the longitudinal confinement of light. The mirror reflectivity has to be greater than 99% because of the low round trip gain typically found in VCSELs. The DBR consist of alternating pairs of quarter-wavelength thick high and low refractive index layers. By spacing multiple high-to-low index interfaces at a distance $\lambda/2$ apart, the reflectivity of each interface adds constructively to produce mirrors with a maximum reflectance greater than 99% [4]. The gain medium located between the mirrors is commonly composed of one or more very thin semiconductor layers that form quantum wells. The gain profile of the quantum well material and the cavity resonance wavelength determine the lasing wavelength of the VCSEL.

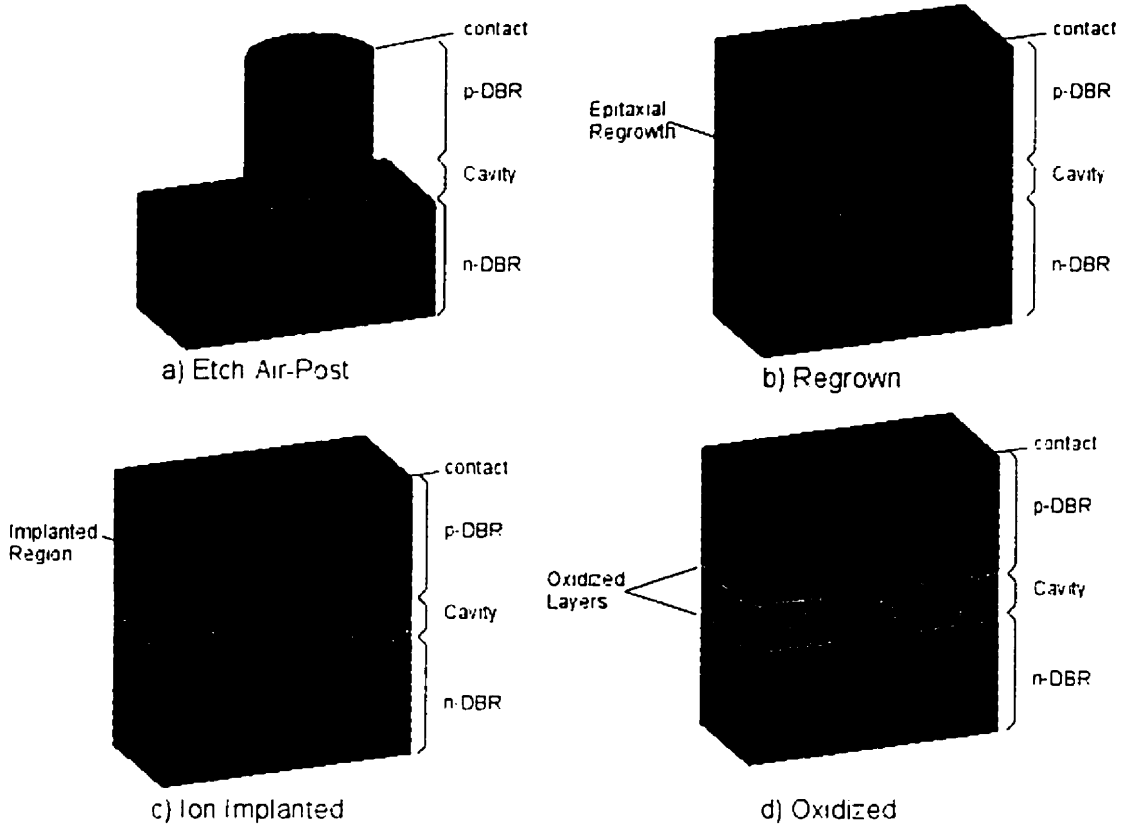

Figure 3.1 VCSEL Types (lateral confinement method)

Effectively limiting the cross-sectional areas of the electrical current and the optical mode near the gain region is important for achieving high efficiency or low threshold current. Figure 3.1 shows the four devices structure presently used for transverse electrical or optical confinement.

Shown in Figure 3.1 a), Etch Air-Post is the easiest structure elaborated for defining the lateral dimensions of the VCSEL. The pillar structures with small area and smooth vertical sidewalls are usually defined using dry etching techniques, such as chemically assisted ion beam etching or reactive ion etching [5]. Strong index and current guiding structures are present in air-post structures because of the large index at semiconductor-air interface. A disadvantage of the air-post structure is the high thermal impedance of the structure due to the absence of an effective heat sink in contact with the laser cavity. This problem accentuates the effect of temperature on the laser, which causes

pillar-etched type of VCSELs to perform poorly over ranging temperatures. Some etched air-post VCSEL implementations add a heat-spreading layer, which increases the thermal dissipation. These methods increase the maximum output power significantly [6]. In addition, the air-post VCSEL suffers from a high carrier loss due to recombination at the sidewall. The imperfections in sidewalls also increase the optical losses due to diffraction and scattering. These losses reduce the efficiency of the pillar-etched VCSEL when compared to the other types of VCSELs.

Planar VCSEL structures provide a better thermal dissipation [4]. The first planar structure is the regrown structure. Using similar a procedure as in the air post VCSEL case, the active region is first defined. The etched regions are then replaced by materials that have higher bandgap energies. The regrown regions provide both optical and electrical confinement, because of their higher bandgap and lower refractive indices. Regrowing techniques are usually very difficult to achieve and are not the preferred approach to VCSEL implementation. However, they allow for lateral current injection which greatly decreases VCSEL resistance allowing for easier laser driver design [4-5].

The two most popular planar VCSEL structures are the Ion-Implanted structure and the Oxide-Confined VCSEL. In Ion-Implanted VCSELs, ions are implanted at specific locations into the semiconductor material. This causes the implanted regions to be insulating and therefore controls the flow of the injected current [4-5]. The implantation does not provide an easy index guiding mechanism for the optical field like in the air-post, or regrown case. Instead, index guiding, to confine the optical modes is provided by the thermally induced index gradient creating a thermal lensing effect collecting the emitted light. Ion implanted VCSELs are limited to multilateral mode operation as the index guiding by thermal lensing is insufficient to allow single-mode operation. Also, the proximity to which the implanted regions can be positioned with respect to the active region is limited by the lateral scattering of the ions. These scattered ions could damage the active regions and reduce VCSEL reliability if the implantation is performed too close to the active region. Since small aperture

definition is limited, the Ion-Implanted VCSELs are unlikely to have optical characteristics superior to Etched Air-Post VCSELs. Oxide-Confined VCSELs provide index guiding and lateral electrical confinement through selective oxidation of the buried AlGaAs layer. Oxide-Confined VCSELs provide a significant improvement in laser performance. Current thresholds smaller than 150 μA, wall plug efficiencies greater than 50%, and high-speed modulation greater than 20Ghz have been achieved by oxide-confined VCSELs [7-9].

3.3. VCSEL used for the FSOI system

When developing transmitter circuitry, it is imperative to know the characteristics of the VCSELs being used. The different types of VCSELs will have a range of parameters for which the driver has to be specifically developed in order to provide the best performance both electrically and optically. The VCSELs used for the transmitter implementation were provided by CSEM, a commercial corporation specialized in laser fabrication. They were specifically developed and fabricated to be used in the adaptive redundant FSOI. The capability of the VCSEL manufacturer restricted the achievable VCSEL specifications. Working from our ideal specifications, the VCSELs characteristics were provided by the manufacturer. Table 3.1 summarizes the final specifications used for the laser design and the laser driver design. Once the manufacturing process was performed on the VCSELs, their characteristics were measured to confirm the laser performances. The reader will be able to appreciate later that the VCSELs were out of specifications, probably due to a lack of experience on the part of the manufacturing company with single mode VCSEL technology. The following sections in this chapter will review the measured characteristics of the VCSELs used in the transmitter implementation. From these measurements, the design of the driver electronics and packaging had to be corrected in order to improve the performance. Chapter 5 will review some of the corrections brought to the design based on the following measurements.

Table 3.1 VCSEL specifications (not actual VCSEL performance) [10]

Design Parameter	Minimum	Typical	Maximum
Thershold voltage (V)	2.0	2.1	2.5
Threshold current (mA)	3.0	4.0	6.0
Resistance (ohm)	83	200	250
Voltage for Maximum Power output (V)	2.5	3.0	3.5
Current for Maximum Power output (mA)	6.0	4.2	15.0
Maximum Optical Power output (mW)	0.3	0.5	NA
Capacitance (dominated by rooting) (pf)	-	-	1.0
VCSEL pitch (um)	-	250	-
Aperture size (μm)	3	-	4
Wavelength (nm)	-	960	-
$1/e^2$ Intensity half width (°)	-	15	-

3.4. Physical Characteristics

The VCSELs used for the FSOI were part of a 5x5 individually addressable array. The VCSELs in the array are of etched air-post type. Like the majority of the VCSELs to date, they are grown on an n-doped substrate with a lower n-type DBR and a p-type DBR on the top. The anode (p-contact) of every laser diode is electrically connected to the driving circuitry though the gold routing layer defined on the topside of the VCSEL array. The routing layer is designed to be connected through wire bonds onto a gold bonding pad located at the VCSEL die periphery. The current return path is provided though a broad-area ohmic contact created by a metal deposition on the backside of the wafer. This contact is designed to be fixed directly onto the bottom of the package cavity. The back contact is common to all VCSELs simplifying the routing for the array.

Figure 3.2 (a) shows the drawing describing the disposition of the VCSELs on the chip and the rouging layer. The resulting die shape can be seen on Figure 3.2 (b). The VCSEL die is square and measures 1800μm on the side. The VCSELs have a pitch of

250μm for which our FSOI optical system was specifically designed. The bonding pads are square, measure 90μm on a side and have a 200μm separation. These pad dimensions were made to be compatible with our wire-bonding equipment and to minimize the pad parasitic capacitance. The routing traces are 15μm in width and were disposed such as to allow for electrical access of a 3x3 sub-array from a unique die corner. The VCSEL array was designed to a 5x5 form factor in order to be able to develop a larger FSOI. The first step in the project realization was to build an FSOI using a 3x3 array and only 36% of the VCSELs on a die are to be used for the first phase of the project. Two more VCSELs out of the 3x3 sub-array are used as alignment targets for the opto-mechanic alignment; however, they are not to be used in normal FSOI operation.

Figure 3.2 (c) and (d) show a scanning electro-microscope picture of one VCSEL alone. On this picture, we can see the etched pillar and the annular ohmic contact to the top DBR VCSEL. We can also observe that the VCSEL top aperture is 4.7μm. since the larger aperture was 117% larger than specified, the divergence angle also differs from the specification. These variations can be corrected for by changing the distance between the micro lens and the VCSEL array in the opto-mechanics.

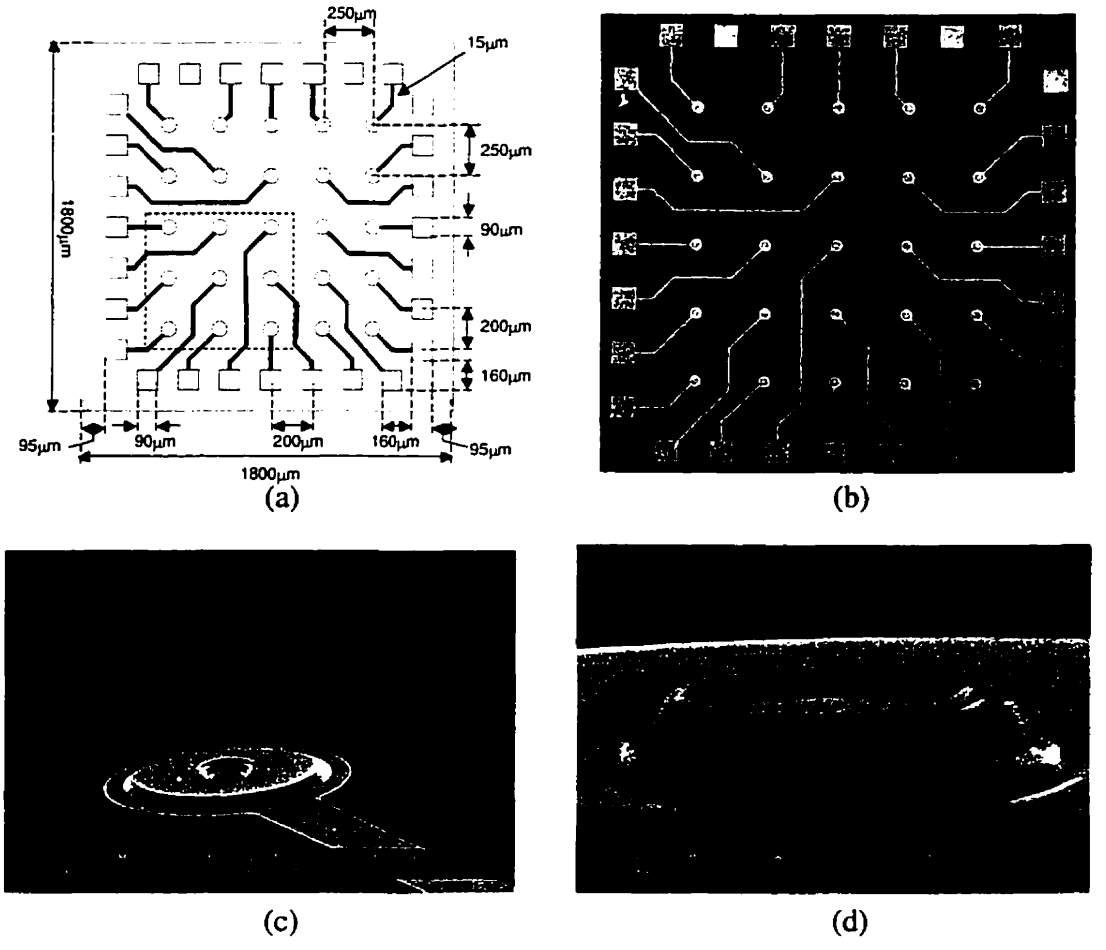

Figure 3.2 VCSEL array used for FSOI. (a) top routing specification and laser position drawing. (b) Top view of the 5x5 individually addressable array showing metal interconnect metal and bonding pad around the periphery (c) VCSEL mesa structure and interconnect view (d) 10,000x scanning electron microscope picture of one of the pillar structure forming one VCSEL on the array.

3.5. Electrical characteristics

The LI and IV curves are key parameters in the characterization of VCSELs. An LI curve plots the intensity of light with respect to the injected current. From the LI curves, it is possible to find the threshold current and the slope efficiency (ΔW of light produced/ Δ current injected). The voltage vs current curve (VI curve) helps determine

electrical characteristics of the laser diode such as the characteristic impedance. The third important curve calculates the electrical-to-optical power conversion efficiency of the diode with respect to the current.

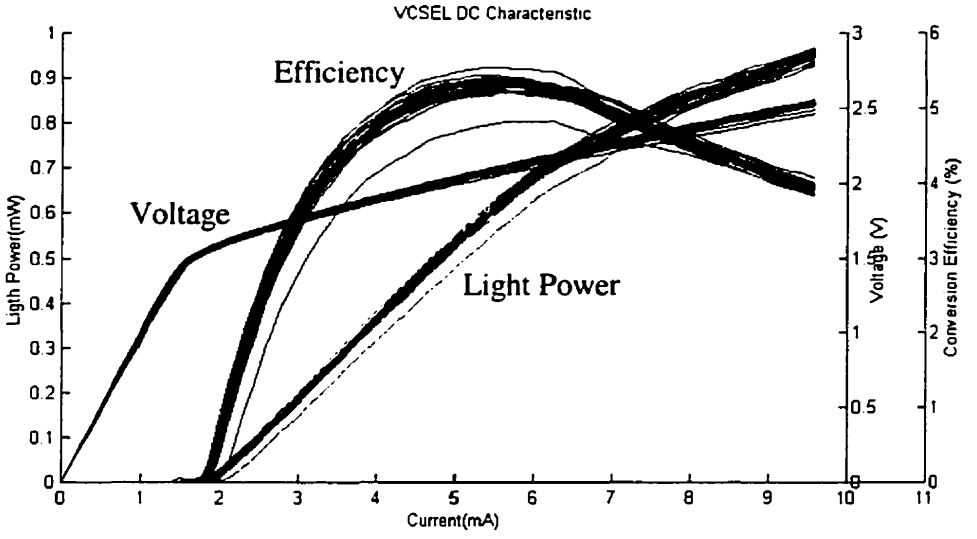

Figure 3.3 LI, VI and conversion efficiency curves for one VCSEL array

The characteristics for all laser arrays were measured using an automated measurement setup. For every VCSEL, a probe current was injected and the voltage and light intensity were recorded. A computer program was used to compile the information for every point measured on the LIV curve for each VCSLE. Figure 3.3 shows an example for the measurements of one VCSEL array. The VCSELs have an average threshold voltage of 1.58±0.07V. This is 0.4 Volts lower than the lowest voltage specified for the driver design. This lower voltage threshold caused some problems, as the silicon driver chip was not designed to drive such a low voltage laser. The threshold current is on average 1.7mA±0.6mA. The current characteristics of the VCSELs are 50% lower than the specifications. The resistance featured by the VCSELs is 130 ± 15 Ω. Lower resistance is beneficial for circuit performance as the discharge time for the circuit should be improved. Finally, the slope efficiency is measured to be 0.170±0.020 W/A. The laser featured a much larger maximum output power than anticipated although it

exhibits a maximum conversion efficiency of only 5.5%. Most of the electrical power is therefore thermally dissipated by the resistance of the DBRs.

3.6. Uniformity

VCSEL uniformity is an important factor to consider in designing an arrayed driver. As density of the transmitter array increases, it is essential to reduce the complexity of the driver circuitry. For instance, back facet monitoring with active adjustment of laser threshold and modulation levels have to be removed to make the driver more compact. Also, it is recommended that the laser array have a very good uniformity as this allows all drivers to use a common reference for modulation and threshold levels.

Investigation about VCSEL array uniformity was performed on the 50 arrays obtained for the realization of the projects. The voltage, current, light power curves were measured [11] for all VCSELs and the threshold current and voltage was extracted from the data. Figure 3.4 graphically shows the result from this study. For the case where the VCSEL driver development was concerned, the threshold voltage was most important since the driver developed for our FSOI was a voltage driver. The threshold voltage for the 1250 VCSELs measured had an average of 1.58V with a minimum voltage threshold of 1.5V and a maximum of 1.65V. This variation points that a driver development program has to include some way of adjusting the thresholds because of the non-negligible array-to-array variation in the threshold voltage. However, the per-array data Figure 3.4 d) shows that most of the arrays are very uniform in themselves as most of the arrays have a maximum of 0.03V variation in the threshold within an array. This allows all the driver levels to be set by a single reference source simplifying the driver design. The single source design would create a power non-uniformity of a maximum of 43μW across an array (6% of the modulated power).

VCSEL uniformity is mainly based on the quality of the epitaxial growth. With today's manufacturing methods, VCSEL arrays are being produced to exhibit increasingly uniform behavior across the array allowing for simpler driver designs in the future [1,4,10].

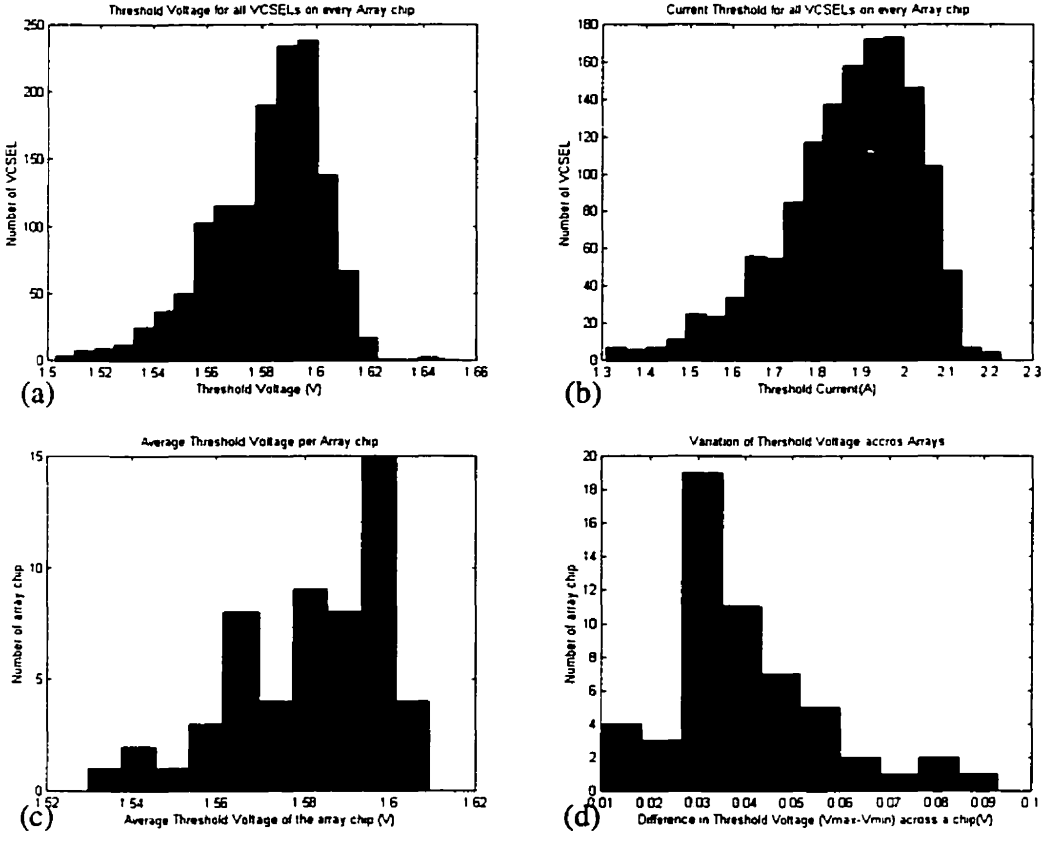

Figure 3.4 VCSEL electrical characteristic statistics (a) voltage threshold distribution for all VCSELs (b) current threshold for all VCSELs (c) average threshold voltage per VCSEL array chip (d) difference between the maximum and minimum voltage threshold on a per-array basis

3.7. Modulation Characteristics

The modulation properties of the VCSEL can be predicted by the relaxation resonance. For bias currents sufficiently above threshold to ensure sufficient carrier clamping, the frequency of the resonance is given by equation 3.1 [4]. The small active volume of

the VCSEL suggests that their potential modulation bandwidth might be quite high. In fact, if all the parameters in the equation were similar, aside for the volume, the VCSEL,s modulation frequency would be much higher than that of an edge-emitter. However, it is not possible to modulate a VCSEL nearly as much as an edge-emitter because of the VCSEL's high thermal impedance and series resistance. Nevertheless, the VCSELs exhibited a small-signal modulation response in excess of 4GHz even for very small currents just above threshold [8, 12].

$$f_R = \frac{1}{2\pi}\left[n_i \frac{\Gamma v_g}{qV}\frac{\partial g}{\partial N}(I - I_{th})\right]^{\frac{1}{2}} = \frac{1}{2\pi}\left[n_i \frac{\Gamma_{xy}\zeta v_g}{qL}\frac{\partial g}{\partial N}(J - J_{th})\right]^{\frac{1}{2}} \qquad \textbf{Equation 3.1}$$

The bandwidth of the VCSEL used for the FSOI was predominantly limited by routing parasitics and not by the resonance frequency of the cavity. The capacitance of the traces was in the order of 1.0pf with an average resistance of 130ohm. This limits the current drive frequency to the GHz range. By using a voltage driven scheme, the layout parasitic effect can be damped allowing for larger VCSEL bandwidth. In this scheme, the routing capacitance is charged through overshoot in the driving current induced by the voltage source and is therefore charged faster than is a current driving technique was used.

It is important to know the modulation characteristics of the VCSEL in order to achieve the optimum transmitter performance. At high-speed, the extinction ratio, the turn-on delay, and the jitter depend on VCSEL modulation capability and on VCSEL bias.

For experimental purposes, the VCSEL large signal modulation response was measured. The modulation voltage for the test was regenerated by a HP 8000 digital signal generator for which the voltage swing was set carefully so as to provide the same swing as presented by the FSOI driver circuitry. The VCSEL was directly mounted and wire-bonded to a female SMA connector to provide the best packaging performance possible. It is believed that the 3dB attenuation point for the signal was around 16GHz from the TDR measurement performed on the packaged device. The

bias at the device was provided through a 15Ghz bias-tee. The VCSEL resistance was matched to the 50Ω transmission line impedance using a 81-ohm resistance. Matching the impedance of the VCSEL is very important when driving the VCSEL through a long transmission line to reduce unwanted reflections which would add ringing on the VCSEL optical output not related to the VCSEL internal dynamics. However, when designing a driver chip to be used very close to the VCSEL, matching is not of much importance as the signal propagation time is much smaller than the rise/fall time, which makes the reflections negligible with respect to the driving signal. The optical signal was recorded by an ANTEL 2Ghz APD model ARX-SA. The resulting traces are shown in Figure 3.5. The source signal was modulated digitally to 1Gb/s. Note that the signal is inverted by the APD. The fall time is 380ps mainly due to the discontinuity in the edge caused by APD's the slow carrier response. The rising time was calculated to 590ps also due to a discontinuity in the edge. The discontinuity is most probably caused by VCSEL internal dynamics. Probing the electrical stimulus did not exhibit such discontinuities. Also, the discontinuity is dependent on the bias pointing to cavity dynamics as a probable cause. The rising edge kink is typical of single mode VCSELs or VCSELs with just a few modes. When the current attain a certain level in the cavity, it is diffused in the higher order mode even if these, mode do not laze due to high scattering. The stimulus signal was measured to have 87.4ps rise time and 127.8ps fall time at the VCSEL connection to the package.

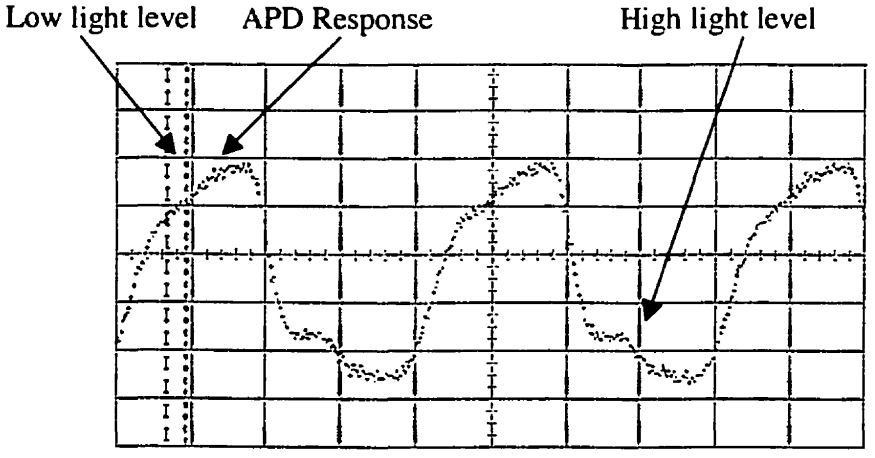

Figure 3.5 Modulated signal from a VCSEL measured with a non-amplified APD 400ps/div.

3.8. Temperature Dependence on VCSEL Characteristics

One requirement for the transmitter is that it must operate in environments having a maximum of 70°C ambient temperature. This temperature is a largely accepted value in telecommunications. As the temperature increases, the laser output power decreases. The cavity resonance/laser gain alignment dominates the temperature dependence of VCSEL operation. As the temperature increases, both the cavity resonance and the laser gain shift to longer wavelengths owing to refractive index and bandgap temperature dependence. However, the laser gain shifts to a longer wavelength faster than the cavity resonance causing spectral misalignment between the cavity resonance and the peak gain, leading to degradation of the laser performance as temperature increases [4].

It is necessary to understand the effect of an increase in temperature on the VCSEL since this dictates the cooling strategy. Experimental measurements were performed to measure the temperature dependence of the L-I characteristic and the results are shown in Figure 3.6. These measurements were performed using a precision programmable current source and a precision power meter, both attached to a control computer using a GPIB interface. A temperature controller was used to set the temperature in a ceramic test package. The VCSEL was placed into the package and probed to acquire the temperature dependency curves.

The threshold current at 85°C is 2.3mA and the maximum power is 0.72mW. The VCSELs will therefore operate over the minimum acceptable power for system operation (0.5mW). However, in order to accommodate the change in the threshold without incurring a penalty in VCSEL speed, the driver threshold current must be set to around 2.4mA. This then reduces the contrast ratio at lower temperatures. Implementation of the driver should include threshold and modulation level compensation mechanisms to maintain an even output power and contrast ratio as temperature increases.

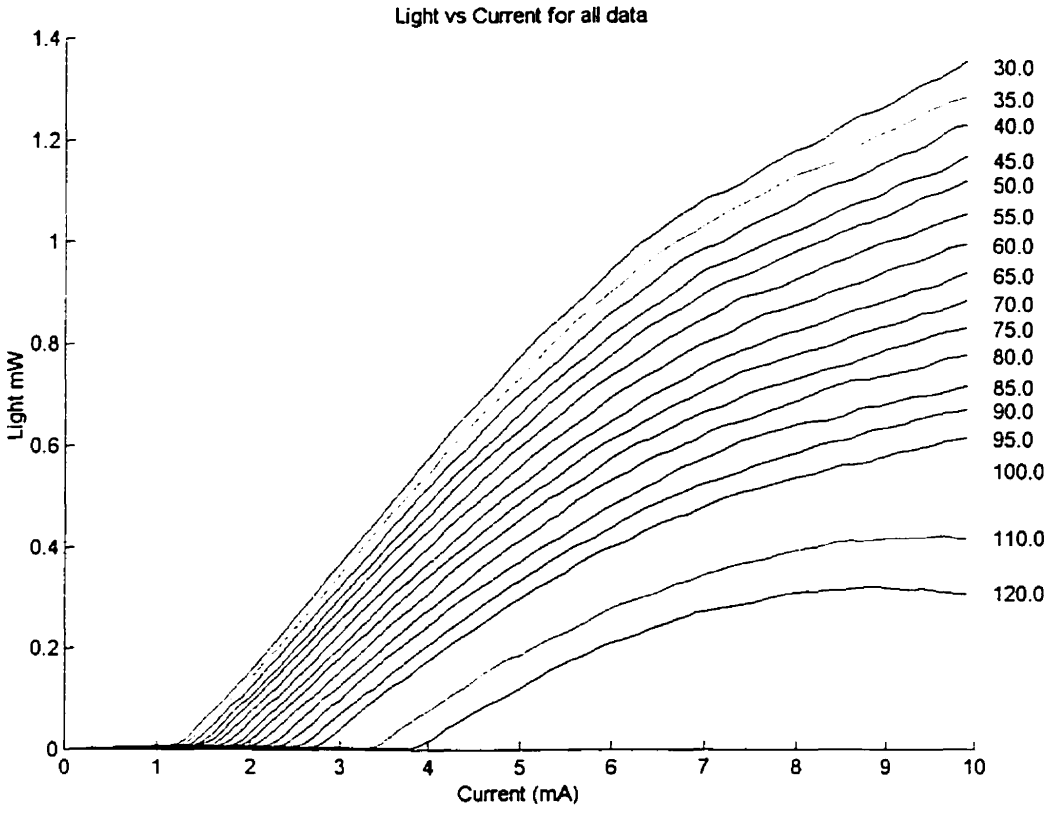

Figure 3.6 Effect of increasing the temperature on the L-I characteristics of the VCSEL. The number on the right of the graph represents the operating temperature in °C.

3.9. VCSEL Modal Characteristics

The single transverse mode VCSEL is an important component for the development of free space optical interconnections. The bit error rate (BER) can be adversely affected by the presence of multiple modes in the laser cavity. This tendency was noted in previous FSOI demonstrations [13] where strong correlation between the spatial mode opening and the mode quality was found. VCSELs that happen to be nearly single mode give markedly better error rate than lasers of more complex structures from the same manufacturing lot. Noise characteristics are also affected when using a multimode structured VCSEL. As current increases in the laser cavity, more modes can survive and therefore the power per mode gets redistributed as the current changes.

This dynamic effectively introduces switching noise in the interconnection when multimode VCSELs are used.

Multiple transverse mode structures are more difficult to model and the higher mode components produce a larger divergence than a single-mode beam. The impact on the FSOI optical design could have been disastrous as the power distribution with respect to switching was carefully calculated assuming a single Gaussian mode. By having multiple modes, the power distribution would have been much different than calculated possibly impacting the whole power budget in an unpredictable way.

The cavity of pillar etched VCSELs support multilateral modes for all but submicron diameter mesa. However, since the etch surface is not perfect, the higher modes tend to suffer higher losses than the fundamental mode. In consequences, the higher order modes do not typically laze and single lateral mode operation is observed for diameter up to about 8μm. We have to keep in mind that the mode filtering action is accompanied by unwanted loss for the fundamental mode. This increases the threshold current and decreases the differential quantum efficiency having a direct impact on the overall laser performance [4].

Measurement of the field emission from VCSELs can be performed in the far-field and in the near field. Near-field measurement provides more insight into the device's behavior giving a better picture of what is happening in the VCSEL cavity. Also, the optical system for the FSOI has a planar micro lens very close to the VCSEL making near-field modal behavior a much better metric for modeling the optical system. Measurement of modal characteristics in the single mode regime are traditionally performed with a lens relay and/or a microscope objective together with a CCD camera [14,15]. Other methods propose using a scanning near-field optical microscope (SNOM) to measure the mode profile [16]. Using this method, the light is collected from a very small aperture, scanning very close to the scanned surface. The SNOM usually uses a tapered optical fiber. The fiber tip is etched and covered by aluminum creating a tip from 100um to a few tenths of a nanometer. This very small tip allows

for the probing of the light power distribution to a very high precision across the laser mode at the surface.

The method used to measure the modal profile in our VCSEL was similar to the CCD method. The experimental setup is depicted in Figure 3.7. The image of the VCSEL surface (near-field) was magnified and projected on the image plane using an optical system made of a microscope objective and a lens. This optical system provided a 20x magnification. The image was read by moving a power measurement head into the image plane. The measurement head was obstructed using a 5μm pinhole. This method created an effective 5μm pixel. The 5μm pixel was scanned using a Klinger motorized translation stage with a resolution of 0.1μm. By using a centralized controller, the power was recorded along with the point coordinate, which permitted the reconstruction of the modal image using a computer program. Power-meter head offer a much greater dynamic range than that offered by a CCD camera. In addition, the uniformity of the measurements is ensured as the power head is well calibrated for the complete dynamic range. In contrast, power measurement uniformity problems (across spatial position) and power linearity problems are present in CCD methods.

One of the drawbacks of using a power meter as a power sensor is the speed at which the image can be acquired. As an example, if the image counts 10000 pixels (100x100pixels) and the scan takes 0.5 seconds per sample of the image, then the time required for a full scan is about 1 hour and 25 minutes long. This delay between the first sample and the last sample for a single modal image exclude any possible measurements on the mode dynamic that could happen as the laser power fluctuates. However, if the laser is single mode, the mode profile should not exhibit multimode behavior when driven by a rapidly changing current. Therefore, the method gives therefore a good measure of the VCSEL modal content.

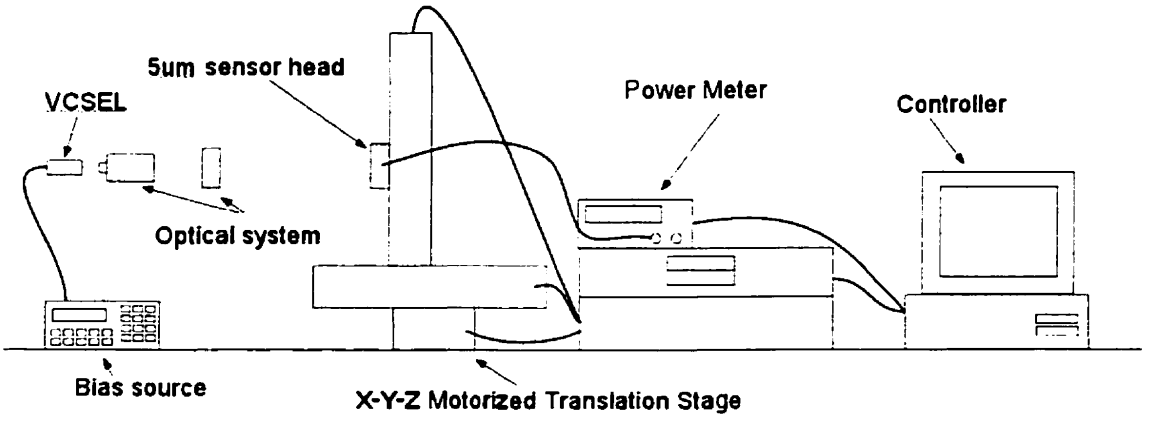

Figure 3.7 Near field mode measurement setup

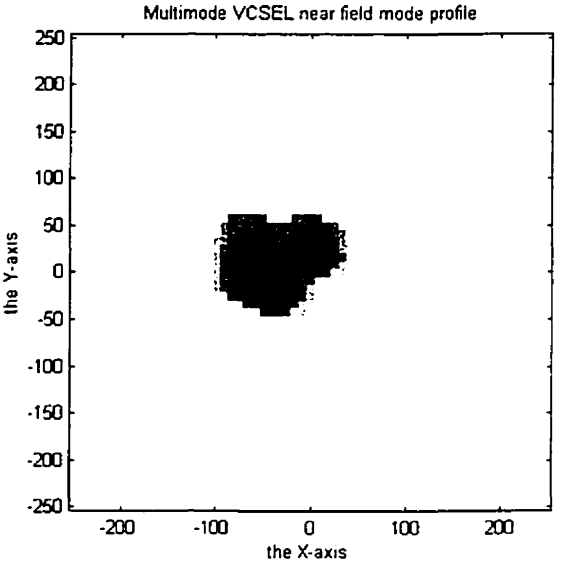

Figure 3.8 Test multimode VCSEL near field profile. The axis coordinates are in μm. Note that the modal image was magnified. (VCSEL provided by Honeywell)

The measurement method was validated using a test multimode laser. The multimode VCSEL had two dominant modes which were observed in the mode profile (Figure 3.8), confirming the capability of the setup to identify multiple modes in VCSELs.

The near-field mode for the VCSEL used in the FSOI demonstrated single mode operation. Measurements were performed at 2mA, 6mA and 10mA and are shown in

Figure 3.9. The profile for the worst case of these measurements was at the highest bias. A Gaussian intensity profile defined by Equation 3.2 was fit to the worst-case profile shown in Figure 3.10. The fit operation revealed that the intensity profile departed from the ideal Gaussian by only 17%, most of which can be explained by spontaneous emissions in the cavity and measurement uncertainty.

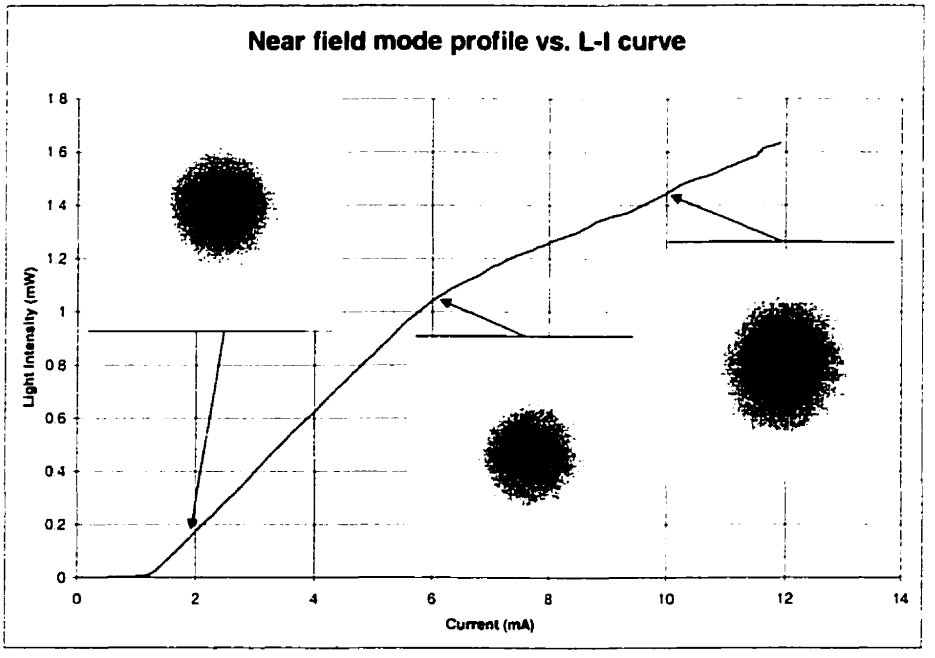

Figure 3.9 Mode profile for the VCSEL Referenced on he L-I Curve

$$I(x,y) = I_0 \exp\left[-\frac{2(x^2+y^2)}{W_0^2}\right] \qquad \textbf{Equation 3.2}$$

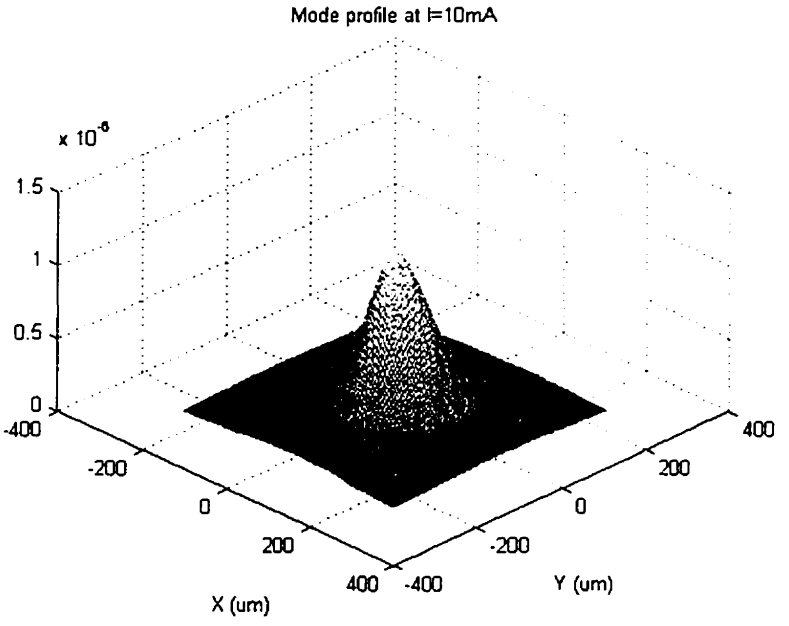

Figure 3.10 Mode profile for the VCSEL when the bias current=10mA

Due to the very small cavity, VCSELs usually have only one single longitudinal mode, especially if the laser exhibits only one transverse mode. The CSEM VCSEL does obey to this law. The spectrums of a few laser were observed to exhibit only one peak down to the noise floor of the spectrum analyzer at –80dBm. The peak wavelength is 959nm and the spectral width 40dB below the peak maximum is only 1 nm. The VCSELs have a very pure and narrow bandwidth, which will reduce noise in the interconnection and therefore allows a better BER to be achieved.

3.10. Beam divergence and Gaussian optics

One of the important parameters when simulating an optical system is the divergence angle. The divergence angle is the angle made by the beam radius expansion with respect to the propagation axis (θ_0 angle in Figure 3.11). This definition comes from the Gaussian beam propagation model that is often used when designing beam oriented optical systems.

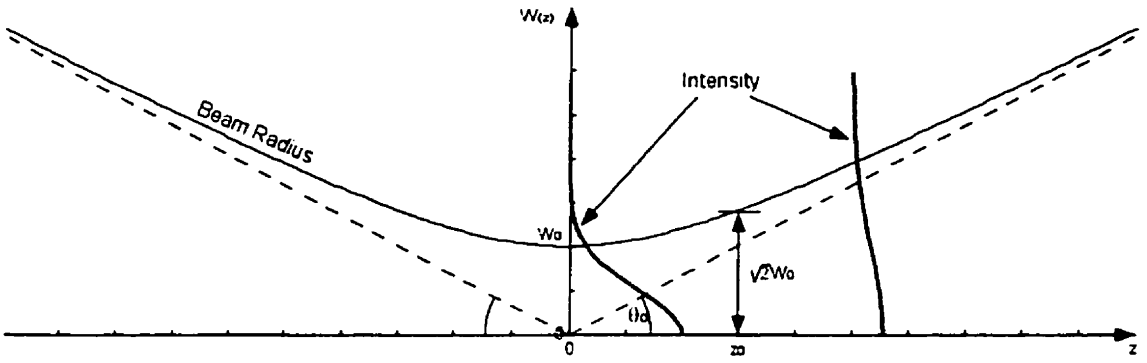

Figure 3.11 The Gaussian beam radius W(z) has its minimum value at the waist (z=0), where it reaches $\sqrt{2}W_0$ at the Rayleigh range. The beam increases linearly for large z following a divergence angle of θ_0. The bold line shows the beam intensity profile with respect to radial coordinates, and the lighter line shows the beam radius with respect to z.

Figure 3.11 shows a typical beam-spreading curve for a Gaussian beam. Within any transverse plane, the beam intensity assumes peak value on the beam axis (z axis). The point where the bean intensity drops by a factor $1/e^2$ is called the beam radius and represents 86% of the power carried by the Gaussian beam. The radius of the Gaussian beam is defined by the following equations along the beam axis [17].

$$W(z) = W_0\left[1+\left(\frac{z}{z_0}\right)^2\right]^{\frac{1}{2}} \qquad \textbf{Equation 3.3}$$

$$z_0 = \frac{W_0^2\pi}{\lambda} \qquad \textbf{Equation 3.4}$$

Z_0 is called the Rayleigh range. W_0 is called the beam waist. W_0 assumes its minimum value in the plane z = 0. As the beam propagates, the radius increases linearly for $z>>z_0$ from which the divergence angle θ_0 can be calculated from the following relationships:

$$W(z >> z_0) = W_0 \frac{z}{z_0} = \frac{z\lambda}{\pi W_0} \qquad \textbf{Equation 3.5}$$

$$\theta_0 = \frac{dW}{dz} = \frac{\lambda}{\pi W_0} \qquad \textbf{Equation 3.6}$$

The beam divergence for the VCSEL used in our FSOI was measured to be 17.48°, only 13% larger than specified. To obtain this measurement, a one-dimensional beam scanner, Beam Scan by Photon Inc., was used. The beam profile was measured at multiple points along the beam axis for a VCSEL bias of 4.0 mA, the average level of the modulation signal to be used when modulating the FSOI. The beam width was then obtained for every profile and fit to a linear equation to find the beam divergence slope for the beam with respect to the beam axis. The divergence angle was calculated from this slope. We have to note here that the VCSEL beam behaved very close to the ideal Gaussian beam, fitting the Gaussian intensity profile almost perfectly [18].

3.11. Conclusion

This chapter gave an overview of VCSELs and presented the four types of VCSELs currently being used. The electrical and optical properties of the VCSEL used for the interconnection were measured and described. The lasers that were received and measured were out of specifications. Out of specifications here does not mean that the lasers had undesirable characteristics. In fact, these lasers performed better than specified. The results presented here will serve for the tuning of the next generation driver for the adaptive redundant interconnect. Other properties could be measured to get an even better characterization of the VCSEL, like polarization, modal noise. These will be left for further studies as they did not impact the FSOI design in a great extend.

3.12. Reference

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Chapter 4- Driver Chip Design

4.1. Introduction

Each laser in an optical interconnection needs a driver circuit whose current drive capacity matches the characteristics of the VCSEL. The VCSEL characteristics for the adaptive free space optical interconnection were reviewed in Chapter 3. This chapter will focus on the microelectronic circuits permitting high-speed modulation of the VCSEL and the packaging strategies for the opto-electronics. Few driver designs for VCSEL-based interconnections have appeared in the literature. This is probably because similar receiver circuits are used in every type of interconnection independent of the emitter technology used. However, only VCSEL based interconnections need a VCSEL driver. A voltage mode driver is used in the chip to drive the VCSEL. The driver chip for adaptive free space optical interconnection has to provide more logical manipulation at the chip level than just the adequate voltage and current modulation for the lasers. The transmitter receives two PECL signals from two different sources and distributes them to nine VCSELs. Depending on the state of the interconnection, the transmitter has to transmit the information on one, some, or all the lasers. When lasers are deemed unnecessary for the communication, they are held at threshold; thereby reducing overall power dissipation. This interconnection system is a smaller prototype of a much denser system consisting of many more channels. Routing of the signals, although not necessary for this project, is demonstrated to show scalability of the system.

The purpose of the driving circuit is to provide electrical power to the optical source and to modulate the light in accordance with the signal that is to be transmitted [1]. Optical drivers range from very simple switches to very complicated feedback systems accounting for many variables. Lasers may be switched on and off, but their performance increases significantly if they are not turned off completely. Normally, the lasers are biased above threshold and the modulation current is added to a bias

current. The carrier populations dynamic in lasers are such that turn on delay is considerably longer if the lasers have to cross the threshold point. Figure 4.1 shows the implementation of a generic current mode laser driver; in this implementation, a controlled current is modulated onto the laser by a current switch the bias current is simply added to the modulation current through an electrical connection. Most implementations of laser drivers also use a feedback control loop to allow for an even average and modulation output power level of the light pulses. When current control is used, the pulse characteristics are typically measured through a photodiode fixed on the back facet of the laser.

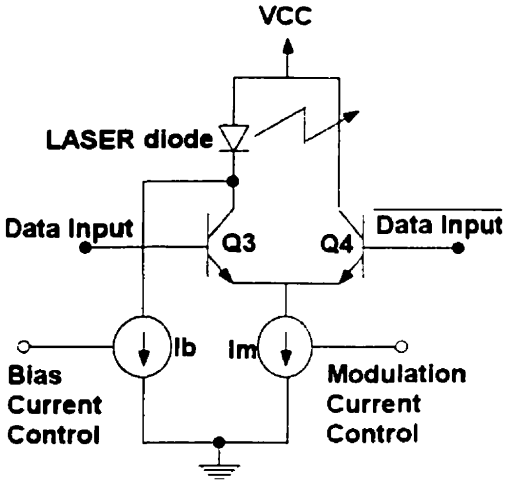

Figure 4.1 Typical Laser Driver [2]

The first part of this chapter will review the driver chip architecture and will introduce the circuits used for the transmitter chip implementation. The second part of the chapter will present the packaging concept used and will conclude by demonstrating a simulation of the full system.

4.2. Architecture

Figure 4.2 shows the driver circuit architecture. The chip features two differential high-speed inputs: the first input carries a probe signal used for the hunt algorithm, and the second input is for the data. Both signals are on-chip terminated by the "T" blocks before being recovered and transferred to chip logic levels by an input electrical receiver. The on-chip terminations are implemented by two 50Ω resistors placed between a termination voltage and the input lines. The termination also sets the correct input DC levels as the input is expected to be AC coupled. The input high-speed receiver is capable of recovering the high-speed signals after attenuation caused by the transmission line and packaging. The low-speed control signals are translated from single-ended TTL levels to the differential logic chip levels by an array of converters before routing onto the chip. This conversion was necessary as the routing conditions are provided by an FPGA featuring TTL output.

The control bus consists of 10 control signals and one test signal. The first nine signals control the state of the drivers, while the tenth signal is used to select the high-speed source. The first routing layer provided on the chip is achieved by a multiplexer, which selects one of the two input signals before transmitting it to the second routing layer. This multiplexer is controlled by control signal number 10. The second routing layer is controlled by inputs 1 to 9 and selects either to transmit the high-speed signals or to transmit the test signal. When the test signal is selected, driver output will be set to the threshold voltage. When the high-speed signal is selected, the driver transmits the data from the selected input. The test signal is normally set to zero; however, for testing purposes it can be set to one, sending all drivers but the selected drivers to a high output state. The VCSELs are not completely turned off during the modulation operation; instead, they are set to the threshold voltage. This allows the VCSELs to be ready for data modulation at all times if system realignment has to occur. The driver had to be independently controlled to allow the hunt algorithm to transmit the probe signal on all VCSELs. Since the alignment state is not known before the hunt has terminated, the probe signal has to be transmitted on all VCSELs to increase the

chances of finding a working transmission channel. Due to the wide variation of VCSEL specifications and uncertainty on the performance uniformity across all VCSELs, the drivers can be independently controlled for modulation and bias. External voltage and current references set the modulation and bias voltages through the Driver Bias Bus. The power lines (VCC and ground) used for the high power section of the VCSEL drivers were separated from the other power lines to allow isolation of the driver section from the rest of the chip using external decoupling capacitors. This procedure reduces power bounces through the chip, thereby reducing undesirable glitches in the driver output.

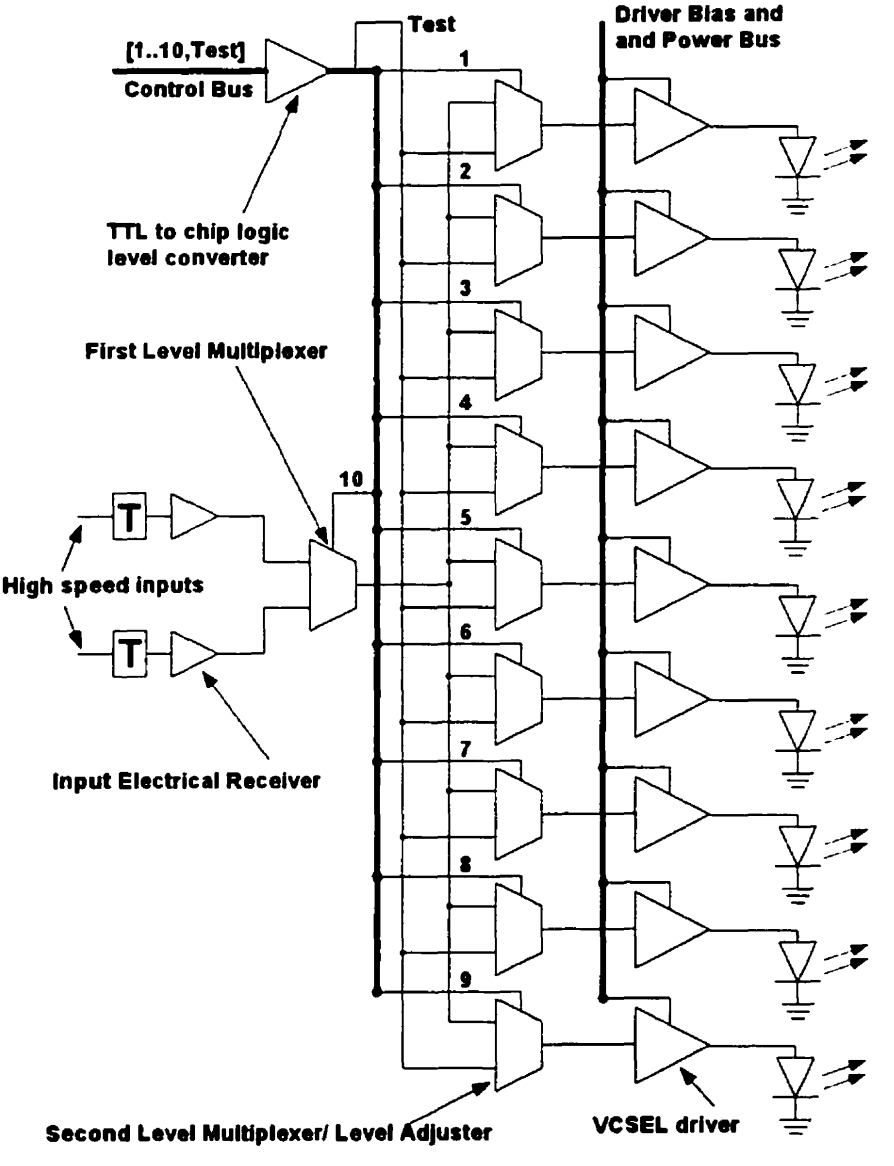

Figure 4.2 Architecture of the adaptive transmitter

The choice of a silicon process to develop the chip was mainly dictated by availability. The VCSEL driver was designed in the Nortel Semiconductor high performance bipolar process NT25. Using a commercial process was a requirement for the chip realization. The NT25 technology, made available through the Canadian Microelectronics Corporation, is a 0.5 μm 25GHz fT self-aligned double poly-silicon bipolar process [3]. This process features low parasitic interconnect capacitance of $0.7nF/cm^2$ for metal 3 to substrate and 5V linear metal-insulator-metal capacitor with $1fF/mm^2$. NT25 is well suited for applications operating in the 1-to-3 GHz range. Typical high-speed digital applications include multiplexers, demultiplexers, laser drivers, clock drivers, and buffers. This process is therefore well suited for an adaptive transmitter working at 1.25Gb/s.

Due to process variations in VCSEL and silicon technology, the driver circuit must be operated near the speed limit allowed by the technology. Therefore, aside from circuit resistances and currents, one must carefully optimize the size and configuration of the transistors provided with the technology.

4.3. Logic Routing Circuitry

The transmitter logic circuitry uses standard emitter coupled logic [4]. The simplest example of an ECL circuit is certainly the high-speed input buffer used for the driver chip design, which is shown in Figure 4.3. The base of an ECL circuit is the differential pair, a well known circuit from the analog circuit world [5-6]. The differential pair in an ECL circuit is used as a current steering circuit. When the voltage at the base of Q1 is higher than the base voltage of Q2, the current Id flows in R1. When the voltage at the base of Q2 is higher than the base voltage of Q1, the current Id flows in R2. By modulating the current in the resistors R1 and R2, the voltage at the output is also modulated. The input voltages to the input ECL are always complementary and separated by the voltage differential defined in the logic signal levels. By having complementary input, the noise margin of the logic circuit is more

than doubled. This noise margin relaxation allows for lower input swing levels which minimize the parasitic capacitances charging time. This in return minimize the gate delay.

The second most important stage in an ECL gate is the output driver. In Figure 4.3, the output driver is formed by transistors Q8 and Q10, and resistors R5 and R6. The differential pair could be used in a stand-alone configuration; however, this configuration is very sensitive to output loading. The main task of the output driver is to reduce the output impedance of the gate such that ample current drive is available for the next gate. At the same time, the output stage acts as a level shifter. It aligns all the signals in the circuit to pre-determined DC signal levels to avoid any transistor being placed in saturation. This theoretically increases the modulation speed and reduces the jitter. Without the output driver, the output voltage levels would be VCC and VCC-Id*R1. As an example, if the input to Q1 would be VCC, then the voltage at the collector of this transistor would be VCC-Id*R1 and the transistor would be in the saturation state. The output drivers prevent these kinds of situations. The resistors within the output buffers are simply there for current bias. Q7 and R7 in the circuit are a current source implemented as a current mirror [7]. The second part of the current mirror can be seen in Figure 4.4.

For the driver chip implementation, the current reference was shared for all logic on the chip. The resistor R7 is one of the emitter degeneration resistances. It minimizes the effect of a variation of V_{BE} on the current mirror resistance over temperature or mismatch in the V_{BE} on both sides of the current mirror. The bigger the degeneration resistance, the lower the effect of a V_{BE} change on the current Id. Improving the control of the current Id boils down to improving the control of the voltage swing with temperature.

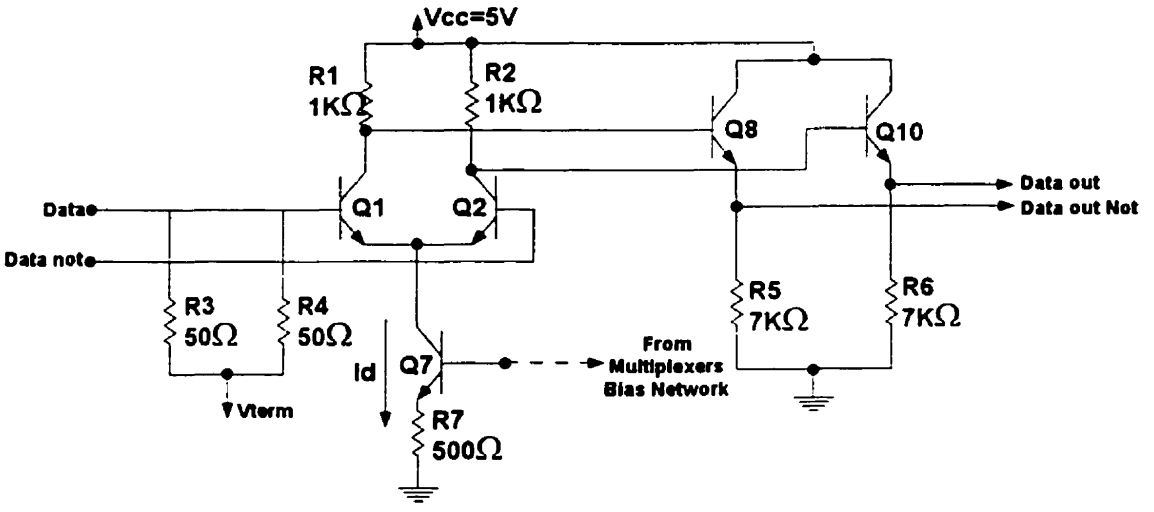

Figure 4.3 Input electrical receiver

The voltage swing for the driver chip logic was chosen to be 500mV. This voltage was judged the best when considering possible noisy conditions in the circuits and speed to which the driver was operated. The current Id was chosen to be 0.5mA which permitted the use of minimum size transistors. Rise and fall times of the internal circuitry were calculated to be faster than the driver circuitry; therefore, there was no need to optimize the circuit parameters for speed at the internal logic level. The input driver circuitry was optimized to recover input signal swings as small as 200mV. R3 and R4 are the internal 50ohm termination resistances whose function was described in the pervious section.

High-speed multiplexers circuits can be designed by adding two supplemental differential stages in the ECL circuit. Figure 4.4 shows an example of a multiplexer ECL circuit. In these circuits, the bottom differential stage steers the current in one of the two upper differential stages. The selected upper stage will be the one modulating the current in the resistors depending on its input signals, thereby creating a multiplexer function. The only departure from a standard ECL cell circuit in this multiplexer is the resistance R3. This resistance is added to the classical circuit to adjust the output voltages to provide the optimum DC levels to the transmitter. C0 in this circuit is also added to ensure low switching noise. The first multiplexer stage is

implemented with the same circuit without R3 because of less stringent input DC level requirements on the second multiplexer stage.

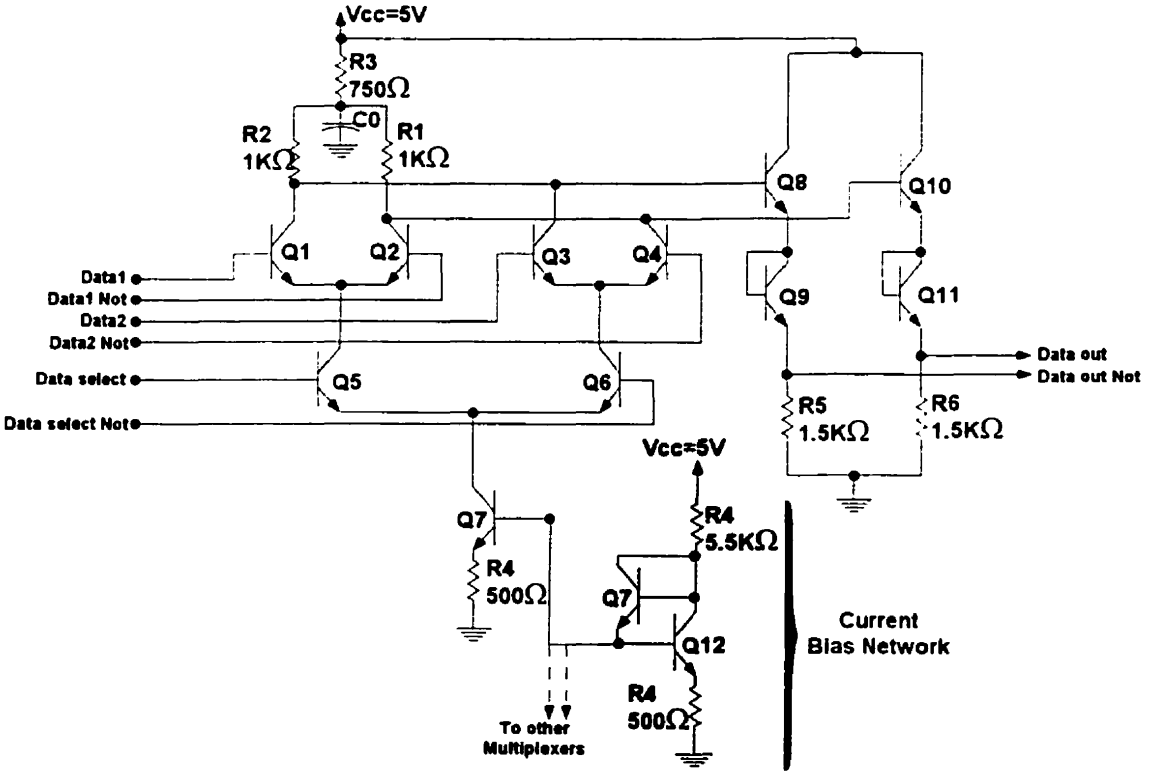

Figure 4.4 Routing multiplexer circuit

The internal logic circuitry was simulated (Using SPICE) over a range of temperature and input conditions to ensure the logic circuits were operating within the expected parameters. Results from the simulations indicated that the worst case rise and fall time came from the second multiplexer stage because of the higher loading imposed by the VCSEL drivers. The results indicated that the rise time was 156ps and the fall time was 178ps. These values were consistent with the 1.25Gb/s bit rate to be carried by the circuit. Noise margin simulation for this circuit indicated that the circuit could operate properly for differential swings as low as 178mV. This provided a 332mV margin removing any doubt about the logic functions being affected by a process parameter variation or noise.

4.4. *TTL Input Translator*

The TTL input translator converts the TTL inputs coming from the control circuitry to the internal logic levels. The TTL converters are implemented as a differential pair in which one of the control lines is tied to a 3.12V reference, creating a threshold condition compatible with the TTL input margin (V_{Lmax}=0.8V V_{Hmin}=2.0V). The TTL translator is developed in a four stage circuit consisting of an input stage, a differential stage, an output stage and a voltage bias network. The following section will explain how these stages work and present the results of simulations.

The input stage is a simple level shifter. The resistor provides the sink current for the connected TTL stage and the two diodes provide a 1.4V voltage shift in order to keep the differential stage current source transistors from saturating. The shift diodes are implemented as ESD protection device. The regular diode-connected NPN transistor could not sustain the high voltage difference experienced at the input. The ESD devices are large area diodes built from a p-doped region implanted into a large n-well. In this type of device, a reverse diode is also created between the n-side of the diode and the p-substrate. This parasitic diode protects the circuit against large input undershoots.

The differential stage is set up as a simple non-linear current switch like the one used for the high-speed routing logic. The output stage is also based on the high-speed routing circuitry design. The only differences between the simple current switch is the presence of two reverse biased diode-connected transistor and of the resistances R7 and R8. The resistors R7 and R8 reduce the gain of the differential pair and more importantly, they increase the base voltage that Q1 and Q2 can sustain. The resistors take a 200mV voltage drop that would otherwise have to occur on the transistors since the TTL voltage swings are very large, special steps have to be taken in order to protect the transistors. To this end, Q3 and Q4 are also there for protection. The base-emitter of the NPN is particularly susceptible to damage in reverse bias as it experiences hot

carrier damage at very low currents. It is recommended that a diode connected transistor be placed so as to shunt the current when a reverse bias condition is possible. In forward bias, much higher currents may be sustained with thermal damage being the limiting factor. The diodes for base-emitter protection should be connected when there is a possibility of forcing the base-emitter junction into reverse bias [8].

The Voltage bias network sets the voltage to which the input is compared in the decision circuit. It is a simple voltage reference composed of two transistors and two resistors. This circuit is inspired by the Motorola MECL II [9] voltage reference circuit differing only by the omission of one of the temperature-compensating transistors. The omitted temperature-compensating transistor was for compensating the input voltage DC point with temperature. In the case of the TTL input, the signal will not drift outside the switching limits over temperature, also, the signal were conveyed in a differential manner, making the second temperature compensation unnecessary. The DC analysis of such a network is quite simple. The voltage at the base of Q8 is provided by the voltage division network formed by R5, Q9, and R10. Q9 is introduced in the bias network in order to cancel the effect of V_{BE} Q8 diminishing with temperature. As temperature increases, V_{BE} for both transistors will decrease at the same rate and VBB will stay constant. VBB is given by the voltage at the base of Q8 less a V_{BE}, the final voltage being given by equation 4.1.

$$VBB = \left(\frac{VCC - V_{BE}}{R5 + R10} \right) R5 - V_{BE} \qquad \textbf{Equation 4.1}$$

The resistance R4 is there to introduce a voltage drop to reduce the V_{CE} experienced by Q8. The maximum voltage that a NPN transistor can support in the process technology is 3.5V; therefore, the transistor would risk breakdown without R4. The R9 resistance provides the necessary bias to transistor Q8. Note that transistor Q8 and Q9 are biased to similar current levels in order for both base emitter voltages to be similar.

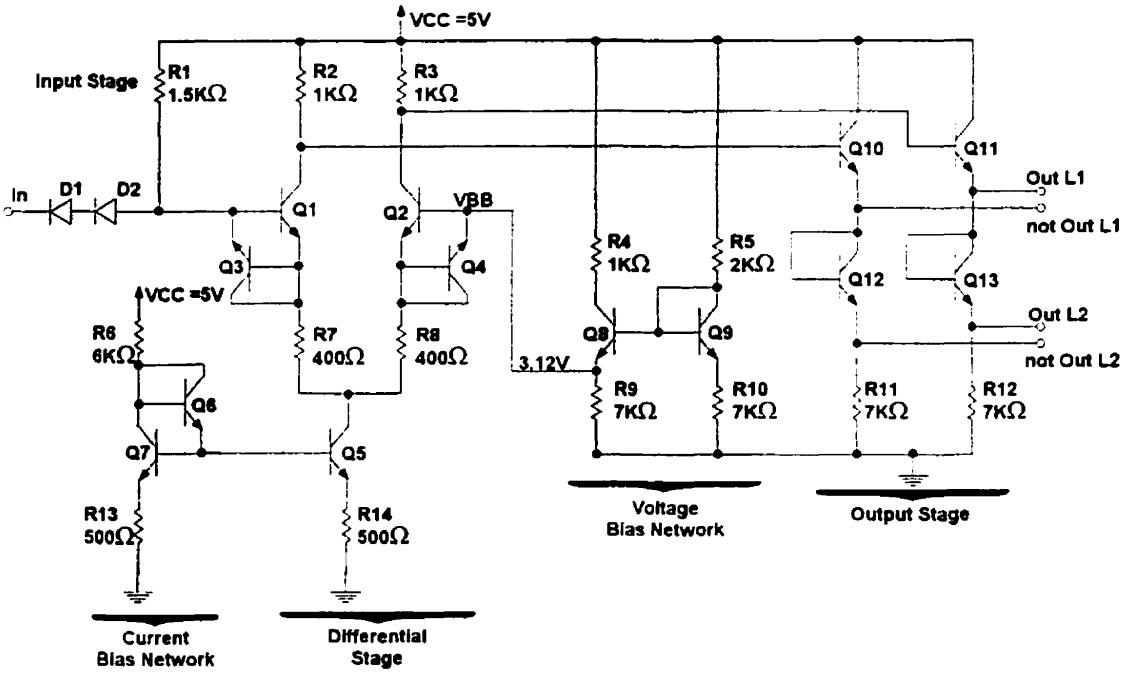

Figure 4.5 TTL-to-Chip-Logic Translation Circuit

In layout, special attention was taken to isolate the TTL translator from the rest of the sensitive circuitry. The TTL input translators are expected to be very noisy because of their single ended nature and large inputs. The isolation was created by a good ohmic contact to ground barrier placed around the translator cell. The barrier will collect unwanted noise and redirect it to a separate ground. The VCC and ground of the translator cells are on different pads from the ones used for the rest of the chip. This is to reduce the probability of noise propagating to critical and sensitive areas of the chip. The grounds are tied together through ESD devices to ensure ground level coherence across the chip. Note here that the noise protection steps used in the layout were not carried out only for the driver chip application. The translator was also used in the receiver circuit which is more sensitive to supply and ground noise by order of magnitude. This added justifications to the precautions taken for circuit isolation. In the layout architecture, the current bias network was shared by a bank of TTL translators thereby reducing the layout complexity.

Simulations performed on the TTL translator were mainly concerned with the DC voltage levels in the circuit. It was necessary to ensure that no transistor would be exposed to an excessive base-emitter or collector-emitter voltage. In addition, the switching characteristics were verified to ensure good functionality of the translation. Figure 4.6 shows the switching characteristics of the translator. It can be seen that for an input voltage over 2V, the output data level is high, while for voltages lower than 0.8V, the output is low. The output level is compatible with the internal switching noise margins and the circuit is tolerant to temperature variations over the 0°C to 100°C range. Translation speed was not of concern for this circuit. The initial implementation of the system would not allow a change of the interconnection state at speeds higher than a few mega hertz due to speed limitations in the alignment controller. However, simulations were performed to address the speed limitation. These simulations indicated that the translator would perform well up to 100Mhz. The input ESD device model was not characterized for speed simulation; therefore, it would be hard to evaluate the conversion repetition rate for higher than 100Mhz. These results were verified experimentally confirming conversion capability up to 40Mhz. The dominant limitation came from transmission line reflection off the input diodes.

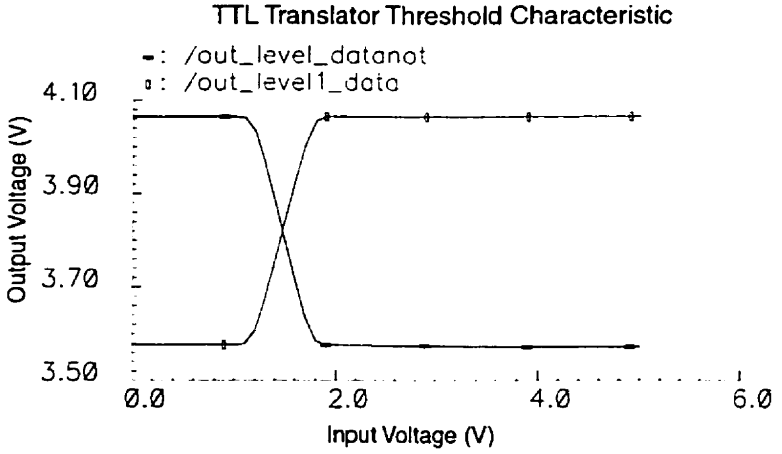

Figure 4.6 TTL Translator Switching Characteristics (SPICE simulation)

4.5. Laser Driver Section

VCSEL drivers are well known circuits that are commercially available. Parallel optical interconnections are already using VCSELs as their light sources at speeds of 1.25Gb/s and beyond [10]. However, VCSEL array drivers are required to be designed to match specific VCSEL characteristics in order to get the optimum performance from the transmitter. The VCSELs used for the adaptive FSOI are common n-substrate; that is, the n-contact of the diodes are connected through the substrate and the signals have to be injected on the p-side of the laser through a metal routing layer. The VCSEL target electrical characteristics are presented in Table 3.1. The driver was designed at an early stage in the interconnection project. At the time of design, only a vague specification was available for the VCSEL. Thus, the driver was designed to tolerate a very large range of possible VCSEL characteristics. The final characteristics were presented in chapter 3.

High-speed laser driver circuits are available from the literature [11-15]. However, most of these drivers are current drivers as their results are generally more uniform and predictable [11]. Because of the high impedance and trace capacitance of the VCSEL chip, a current driver may not be sufficient to achieve the required repetition rates. In addition, the current has to be sourced into the VCSEL chip to achieve modulation. Implementing a current driver would require high performance PNP transistors that are unavailable in the bipolar technology used to implement these circuits. Thus, the only type of driver capable of providing acceptable performances for this application is a voltage laser driver, given the silicon technology used.

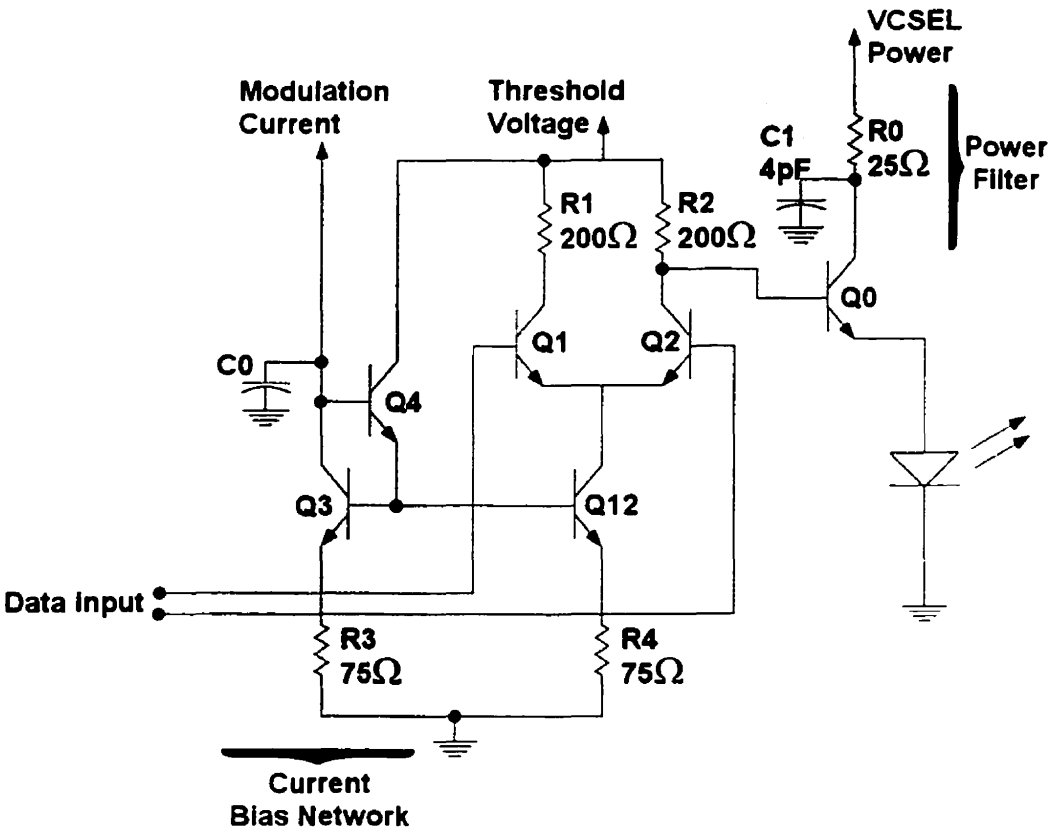

Figure 4.7 Circuit topology for the VCSEL driver section of the transmitter

The circuit topology for the VCSEL driver is shown in Figure 4.7. The VCSELs are driven from the emitter of a NPN transistor. This type of configuration is commonly used in ECL line drivers. Since the f_T of the transistors changes with the collector current, transistor sizing was important to achieve maximum circuit performance. The output transistor had to be at least 30 times larger than the smallest size transistor to allow for maximum performance when driving 15mA.

Due to the large variations in the design parameters, the VCSEL threshold and modulation is externally adjusted independently for each driver. The output voltage is set by the base of the output transistor Q0. Q1 and Q2 form a non-linear differential stage used as a current switch. By switching current in and out of R1, the output voltage is modulated. The current in the current switch is set by the current mirror formed by Q4, Q3, Q12, R3 and R4. It is controlled by an external resistor inserted

between the collector of Q3 and a precision voltage reference defining the voltages used for the VCSEL modulation. Resistors R1 and R2 are both connected to the threshold voltage reference. By changing this voltage, the control circuitry sets the high state of the transmitter and thus indirectly affects the threshold voltage. The threshold voltage is given by the expression $V_{th} - I_{mod} \cdot R2$

The capacitor C1 and resistor R0 behave as a low-pass filter reducing the electrical crosstalk in between drivers through the power lines. The resistor R0 is set to 25Ω causing a 0.4V drop on the power line sourcing the output transistor when using a worst case VCSEL. This resistor could not be made larger without risking the output transistor entering saturation when using a VCSEL with the highest voltage specified by threshold voltage and modulation current ranges. C1 was sized to be the largest possible (4pf) to push the 3dB bandwidth of the filter as low as possible. Simulations of laser driver crosstalk showed that the filter reduces crosstalk by at least 70%.

The size of the collector resistors in the current switch (R1 and R2) were determined by calculating the rise and fall times of the driver circuit. The rise and fall times of the driver circuit are directly affected by R1. Equations 4.2 and 4.3 [4] are the simplified equations used to estimate the rise and fall times in an emitter-coupled circuit. From Equation 4.2, the relation between R1 and the driver rise time can easily be seen. Reducing the value of R1 increases the rise time but also increases the power dissipation in the current switch. The rise time and power dissipation with respect to R1 was calculated for various value of resistance. The results are presented graphically in Figure 4.8. To maintain a constant maximum voltage swing on R1, the differential stage transistors have to be made larger as the current increases. Since the transistors are only available in discrete size, the resulting curve is dented. From this calculation, the value of R1 resistance was chosen to be 200 Ω allowing for a 228ps rise time if worst-case VCSEL parameters are used. The driver rise time is smaller than expected by gigabit ethernet (260ps [16]) providing a margin for process variations. The fall time, in the case of a driver like this one, is lower than the RC time constant. This is because the system does not discharge completely but only up to the threshold voltage.

The resulting fall time is therefore given by equation 4.2. The fall time was calculated to be much lower than the rise time. Therefore, the laser driver was not designed to have any type of active pull down circuitry to help the discharge of the VCSEL [17-19].

$$t_{rise} = 0.69\left(\frac{R_1}{\beta_F + 1} \| R_{VCSEL}\right)\left[C_c(\beta_F + 1) + C_{VCSEL}\right] \qquad \textbf{Equation 4.2}$$

$$t_{fall} = 0.5 C_{VCSEL} R_{VCSEL}\left(\frac{V_{swing}}{V_{CC} - V_{EE}}\right) \qquad \textbf{Equation 4.3}$$

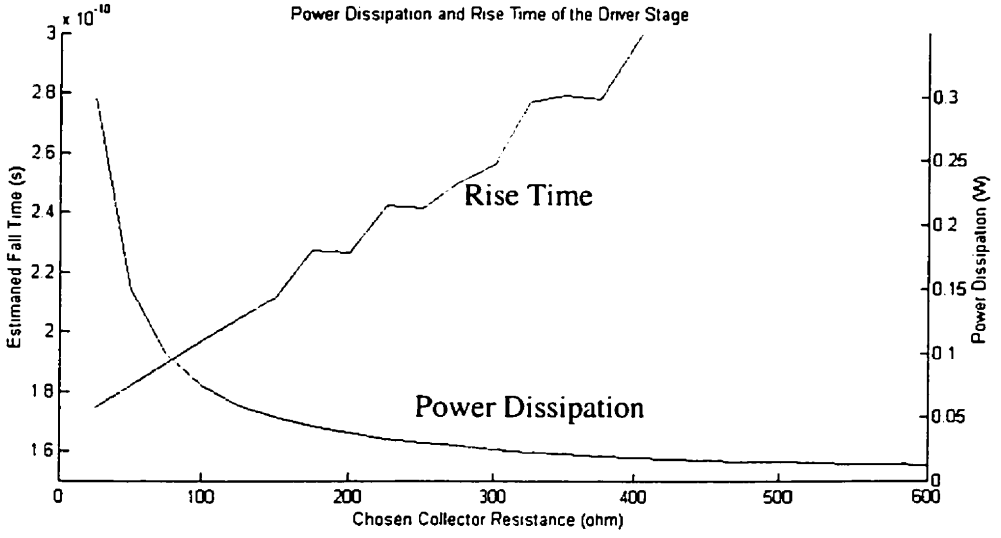

Figure 4.8 Power Dissipation and Rise Time with respect to R1 (Matlab Simulation)

Simulations were performed to verify the functional characteristics of the driver chip. Figure 4.9 shows the eye diagram using typical "specified" VCSEL parameters. In this image, the vertical axis shows the optical output power of the transmitter. For this simulation, the VCSEL model included a resistor, a voltage source, and a capacitor to simulate wiring capacitance. In addition, all the electronic stages before the driver were included in the simulation. The wide eye opening shows good functionality of the transmitter and features less than 25ps of jitter. The 10%-90% rise and fall times were measured to be 144ps and 92ps respectively. The rise time is lower than that

calculated as the simulation was performed on typical "specified" parameters and not on worst-case parameters. DC simulations were performed to evaluate the sensitivity of the driver to the input signal. The simulations indicated that the driver would meet the required output characteristics as long as the output signal from the second multiplexer stage has a swing larger than 140mV. The internal logic was developed for a 500mV swing. The driver should perform adequately over process variations.

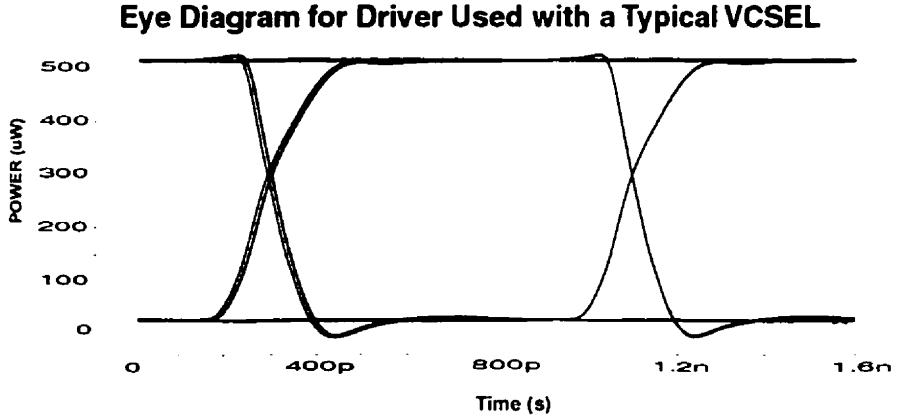

Figure 4.9 Simulated EYE given typical VCSEL characteristics. (SPICE simulation)

4.6. Layout and Floor Plan

Layout for the driver chip generally follows the layout design rules for NT25 [20]. These rules, being confidential, they will not be discussed here. Some additional guidelines were used when drawing the layout to maximize the chip performance. The resistances in the current sources and TTL input translators were matched using standard resistor matching techniques. Matching the resistors allowed canceling for imperfect lithography effects on the circuit output. The relative error incurred in one resistance value will be cancelled by an equivalent error in the matching resistor if:

- care is taken in positioning the matched resistors close to each other (by making an interleaved resistor structure),
- the resistors are made to span a wide area,
- the resistors are oriented in the same direction,
- the circuit is developed to take advantage of the matched resistance variation.

The top metal layer on the chip was avoided for high-speed signals in order to minimize the effects of parasitic capacitances on the circuit. The high-speed lines were made as narrow as permitted by the lithography rules. The narrow lines had an increased resistance; however, the longest line had a resistance <2Ω. The current expected in the high-speed lines was very small. Therefore, the voltage drop across the line was limited, permitting narrow interconnection lines. The bonding pads for all high-speed signals were made as small as possible (82μm on the side). This eliminated some of the pad parasitics.

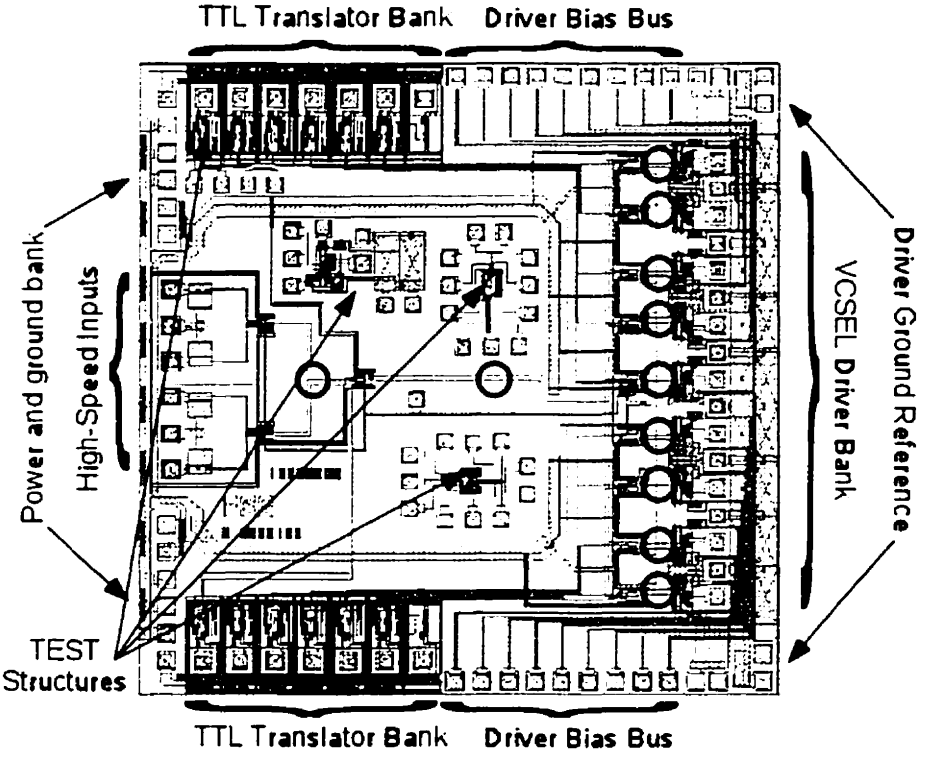

Figure 4.10 VCSEL Driver Chip Floor Plan. The circled areas define the 5um test pad locations.

The main objective in floor planning for the chip was to minimize wire-bond length for the high-speed signals. The layout and floor plan is shown in Figure 4.10. The VCSEL drivers are located on the right side of the chip. They were located the closest as possible to the VCSEL die to minimize the wire-bond length from the driver pad to the VCSEL pad. The grounds for the drivers were also located on the same side (close

to the VCSEL array) to minimize ground plane noise effects. The TTL translator and bias for the VCSEL driver were placed on top and bottom ends of the chip. This positioning created very long wire bonding lengths. However, since these signals were designed to be DC or very low speed, they could tolerate the higher inductance. Because of the large number of inputs to the chip, most of the chip is critical circuitry occupied the side areas of the chip, leaving the center of the chip empty. The center area was used for test structures. Test structures for every part of the chip were inserted in the empty space and not connected to the rest of the chip. In the eventuality that one of the parts was judged not performing within the expected parameters, this part could be investigated. This way, a redesign could be performed with knowledge of the exact cause of the error. In addition, 5um test pads were placed on the high-speed line. These pads would allow for the identification of the problematic area in testing by active probing.

4.7. Transmitter Packaging

4.7.1. Introduction

Packaging is in nature a multidiciplinary problem and perhaps one of the least developed aspects of free space optical interconnections. Micro-electronic pakaging must provide functionality for power distribution, signal distribution, heat dissipation and system protection. Packaging and alignment dominate the manufacturing costs of optical modules. Furthermore, packaging performance directly impacts the system performance. The following section will describe the package chosen for the interconnection and will discuss termal and electrical considerations for the package choice.

4.7.2. Package choice and modifications

The transmitter package choice was mainly driven by availability and by a few performance criteria. The package had to be available in small quantities, allow for the propagation of 1.25Gb/s signals, have good heat dissipation, and allow for the

attachment of the optomechanics on the package's top surface. In addition, the package had to be compatible with the receiver chip modules in order to reduce design and characterization time. The transmitter chip, VCSEL array, and two decoupling capacitors were packaged together in a 100-pin rectangular CERQUAD (also called ceramic quad flat pack) package; a rectangular ceramic package produced commercially by Kyocera Corporation of Japan [24]. We were able to acquire the package from a production surplus. The final assembly will look like that shown in Figure 4.11. It is usually uncommon to have a commercial rectangular package. This quality allows the wire bonds connecting the side of the chip to the package to have a much smaller length then if a common square package had been used.

The number of pins was also important in the choice of the package. Although only 54 connections are needed for the driver chip, only 50% of the package pins could be used. Half the package wire bond paths are inaccessible for chip connections, since they cross the VCSEL array. The high pin count of the chosen package is therefore just right when these variables are taken into consideration. As well, the ceramic package is made of alumina (Al_2O_3) whose thermal dissipation properties are among the best available in current package technology. In addition, the planarity of the package was important in order to position the VCSEL array precisely in tilt with respect to the printed circuit board. The planarity of ceramic packages is usually very well controlled compared with other package technologies. In the case of the Kyocera CERQUAD package, there was a $\pm 10\%$ maximum thickness variation over the length of the package.

The CERQUAD package was laser machined to electrically isolate the back of the VCSEL chip from the driver chip substrate contact and to create markers in the cavity for the alignment of the chips to the package. The electrical isolation was necessary to correct for the low voltage threshold of the VCSELs. Having the VCSEL substrate electrically isolated from the rest of the chips allowed for the insertion of a high-speed schottky diode in series with all the VCSELs in the chip. The two decoupling chip capacitors were then added to create a high frequency link between the VCSEL

substrate and the driver chip substrate. These capacitors are the two smallest chips shown in Figure 4.11. By linking the two chips at high frequency, transients at the VCSEL substrate plane were avoided, making a smoother transition between the on and off states. Figure 4.11 shows the four chips in the package, wire-bonded, before the insertion of the optical and mechanical parts.

The optomechanical component is a precisely machined aluminum part that is fixed on the CERQUAD package using a liquid adhesive [21]. First, the planar microlens is fixed on the aluminum part. Then, using two powered up VCSELs, the optomechanical component is laterally aligned onto the optoelectronic section using the planar microlens as the alignment target. Once this alignment is performed, the optics with mechanic is slowly lowered onto the top surface of the CERQUAD package while controlling for tilt misalignment. Adhesive is then introduced into special slots machined into contact points on the optomechanical component. The CERQUAD packages were soldered in place under microscope for a maximum precision. The CERQUAD, the VCSEL chip, and the optomechanics were therefore aligned to their ideal board position. This minimizing tolerance consumption from the alignment budget for inter-module displacement on the same board.

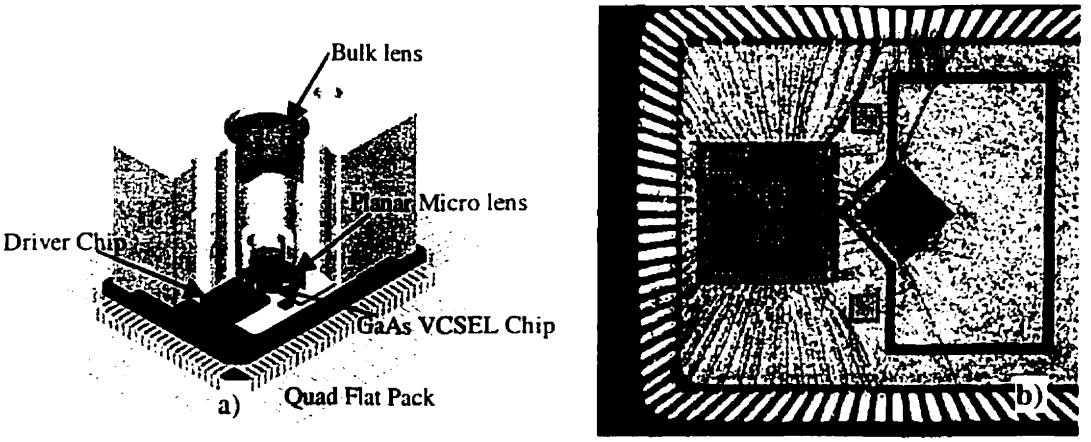

Figure 4.11 a) CAD view of the transmitter package, b) Transmitter mounted in a QFP Package

4.7.3. Electrical Modeling and Performance

When working with high bandwidth signals, the package parasitics become a dominant factor in the success of the design. Numerous papers already cover the considerations of modeling impedance and signal integrity through packages at Ghz speeds discussed in [22-23]. Simulations on the CERQUAD package were performed with HSPICE using a simple lumped RLC model as shown in Figure 4.12. The values used in this model were taken from the package characterizations performed by the manufacturer [24]. The modeling exercise included a wirebond model provided by the Canadian Microelectronics Corporation. When using this model, the lump parameters are calculated from the wire bond length, diameter and resistivity according to the equation developed by Bahl [25].

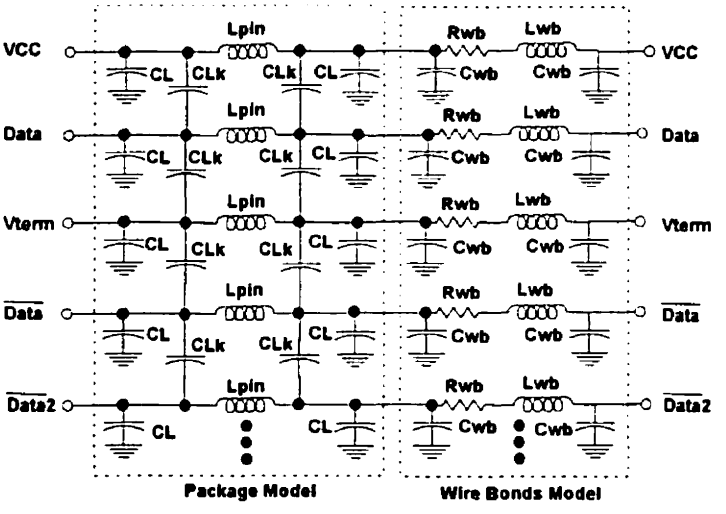

Figure 4.12 Package model used for driver simulation with package. CL=1.35pF, CLk=1.6pF Lpin=2.2nH, the other values were automatically calculated by the circuit simulator.

The simulation results indicated only a reduction in the rise time and some eye closure due to ringing and capacitive loading of the incoming transmission line at the imperfect interface of the package. However, the input voltage swing amplitude was not affected, thereby ensuring the recoverability of the signal by the chip front-end electrical receiver. Note that the package model was used in full only on the high-

speed pins and only one inductor and capacitor was used on the DC and TTL inputs of the chip. This simplification was acceptable since these signals were order of magnitudes slower than the high-speed input; in fact, and most of them were DC. In this case, package parasitics were less significant as they only partially affected switching noise in the chip, therefore a simple an over estimation of the lead inductance was sufficient to create a worst case situation.

Additionally, electrical tests were performed on the package using a vector network analyzer. The S[1,2] parameter, through one 1cm long 60Ω transmission line, one lead of the package, and one wire bond. The result is shown in Figure 4.13. This test shows that the 3dB attenuation point of the signal is around 2.1GHz demonstrating the package electrical compatibility with 1.25Gb/s applications.

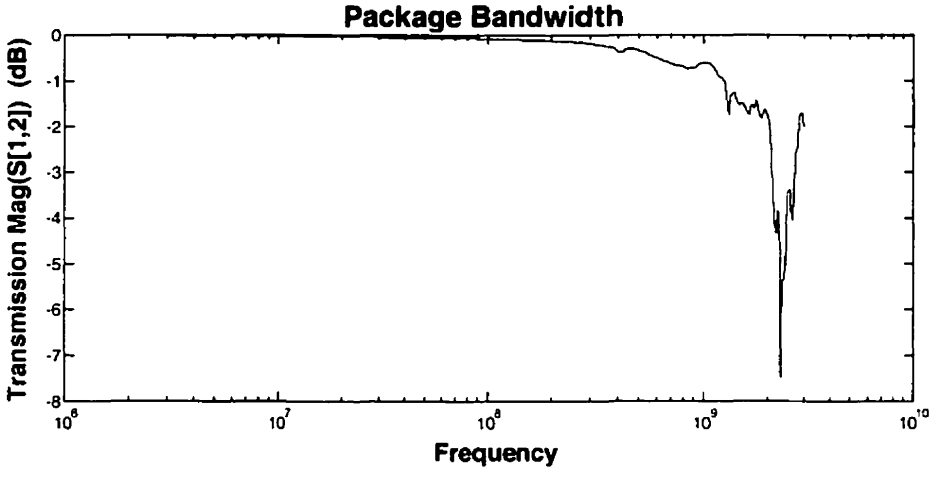

Figure 4.13 Measured Package Frequency Response.

4.7.4. Thermal considerations

VCSEL performance is very dependent on temperature. As introduced in Chapter 3, when the temperature increases, the VCSEL current threshold increases, the slope efficiency decreases and the overall conversion efficiency is negatively impacted. In the case of the redundant FSOI, the VCSELs had to be able to produce a maximum output power of at least -3dBm. This condition can only be achieved if the VCSELs

are maintained at a temperature of less than 95°C. This means that the transmitter package will not need to include any temperature control mechanisms if the temperature of the VCSEL array is maintained below 95°C using only natural convection as the cooling method. One of the requirements in the system implementation was that it could be operated in an environment of 70°C. This would give a 25°C maximum temperature differential between the ambient environment and the interior of the package. The rise in temperature at the interior of the package is due to the chip thermal dissipation and VCSEL inefficiency.

The effect of chip thermal dissipation on the package was evaluated experimentally. The chip was operated in a setup simulating worst thermal conditions:

- The top of the system was enclosed in an insulator permitting absolutely no thermal dissipation from the top of the package (in the real system, the top of the package will be mounted with the optomechanics which will sink a considerable amount of heat),
- All the parts in the VCSEL driver were operated over the specified voltage increasing the power dissipation, and the VCSELs were replaced with simple resistors to maximize the thermal dissipation.

When operated in these conditions, and for about one hour, the temperature difference was measured to be 15°C between ambient and the interior of the package. The power dissipation was measured to be 1.273W in this setup. From these measurements, it is concluded that the worst-case thermal resistance of the package would be 11.8°C/W imposing a VCSEL worst-case temperature of around 85°C. It is easy to conclude that no thermal control is needed for the interconnection, although the worst-case thermal resistance of the package was measured to be quite high. The low power dissipation of the chipsets can be properly handled by the package alone and the VCSELs will always be in an operable temperature range.

4.7.5. Package Assembly Process

The assembly process for optical components is always a hurdle that needs to be overcome towards the end of the design. The modules ultimately have to be mounted on a printed circuit board if it is to be used in a system; however, every component has different temperature tolerances. The assembly process needs to be performed in a specific order to ensure the integrity of the entire module by the end of the assembly process. This section will describe the steps used of the package assembly process.

The first step taken in the assembly was to fix the empty chip carrier on the PCB. The total interconnection tolerance to misalignment was dependent on the precision to which the modules were placed on the PCB. If the package had been placed 1mm outside its designated location, then none of the alignment budget would have been available for the interconnection alignment. In order to position the package very precisely at the designated position, a soldering reflow process had to be used. Through the reflow process, the solder and flux is deposited on the board solder pads and the package is precisely positioned on the pads. The entire board is then exposed to a temperature profile like the one shown in Figure 4.14. During this process, the package is positioned just in the center of the solder pads by virtue of the solder surface tension. This process is often called a self-alignment solder process for which the precision of the package position can be as good as a few tens of microns [27-28]. The high temperature to which the components are exposed during this process is incompatible with the opto-electronics' and optics' maximum temperature limitation. Therefore, the ceramic chip carrier was mounted on the board by a sub-contractor prior to the module assembly which avoided exposition of the opto-electronics to excessive temperatures.

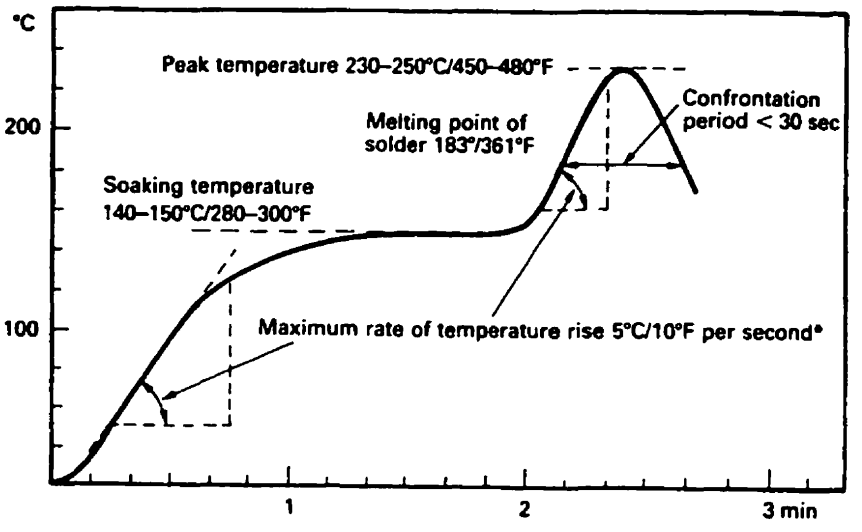

Figure 4.14 Typical soldering reflow process temperature curve [26]

Once fixed on the board, the package was populated by a driver chip, a VCSEL chip and by two decoupling capacitors. All chips but the VCSEL array were fixed using common electrically conductive epoxy. The VCSEL chip was precisely placed in the carrier by centering the array on laser machined markers in the carrier. The alignment was performed under a microscope and the position accuracy of the VCSEL chip is believed to be better than 25μm. Also, the VCSEL array was fixed to the chip carrier using an even bond line epoxy. This epoxy (Ablebond 826-1DS) was provided by Ablestick. The inclusion of special particle-size-controlled silver fillers in the adhesive permitted a tight control of the paralisim of the chip with respect to the cavity. By using lateral and tilt position control mechanisms, the VCSEL array could be positioned precisely in the cavity with high precision in all 6 degrees of freedom.

After this process, the dies were electrically connected to the package fingers using an ultrasonic wedge bonding process. The transmitter was tested for functionality and performance before the optical components were fixed onto the transmitter.

4.8. Transmitter Surrounding Electronics

The transmitter cannot be operated autonomously since the driver was designed to have bias and modulation references provided for each individual laser. In addition, the high-speed signals had to be provided to the transmitter in order to be able to retransmit the information optically. Finally, the VCSELs received from the manufacturer had a much smaller threshold voltage than specified which required some creative high-speed electronic design in order to solve the problem. The printed circuit board for the system holds two transmitter modules and two receiver modules for the two bi-directional links. The biasing circuitry for the transmitter modules, the power monitoring circuitry for the receiver modules, and the FPGA that handles all the control lines for the transceiver modules for the hunt algorithm were developed. This section will present the transmitter controlling circuitry. The full board implementation is out of the scope of this thesis and has already been presented by Plant [29].

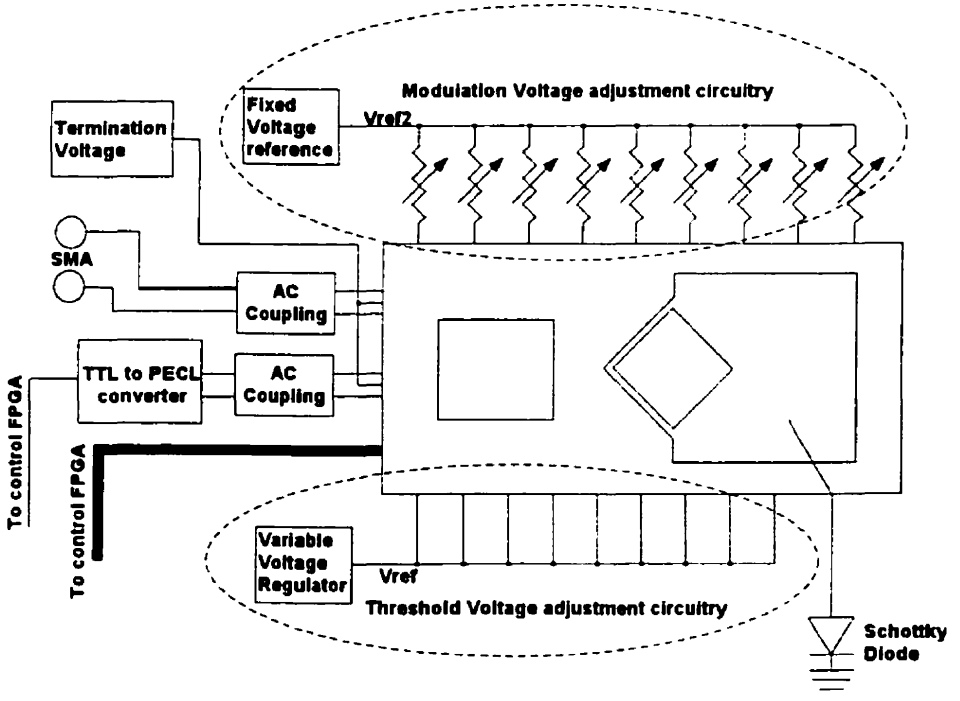

Figure 4.15 Tramsmitter board circuitry

Figure 4.15 shows a high level representation of the transmitter control circuitry. The first element of the surrounding circuitry (and perhaps the most important) is the power supply. The power supply to the transmitter chip was divided from the other power supply on the printed circuit board to provide a noiseless voltage to the driver. This ensures that any noise coming from the FPGA included on the board does not contaminate the high-speed transmitted signal. The voltage supply to the driver section of the circuit was very well decoupled through a double pole decoupling network formed by a 0.1μf and a 0.01μf capacitor placed near to the chip input.

The modulation voltage for the transmitter has to be provided by a reference current. The reference current is created by setting the resistance through a multi-turn variable resistor installed between the input to the chip and a precisely controlled voltage regulator. The voltage at the input of the chip is constant; in consequence, the change in the resistance will modify the current at the input as determined by Ohm's law. The reference voltage used here is implemented by a National Semiconductor LM1117MPX-3.3 voltage regulator. This circuit includes a zener trimmed bandgap reference to produce output voltage accuracy to within ±1% [30]. The precision of the voltage over temperature and load current was important. Since the drivers are adjusted for modulation voltage one after the other during the first power up process. As the modulation voltage is adjusted for the driver, the load current is slowly increased on the voltage reference. The voltage references are common to all driver inputs, it would have been difficult to adjust the drivers if the voltage had dropped as the load current was increased on the reference. The first driver would have been out of calibration as soon as a few drivers had been adjusted for their optimum voltage reference. The LM1117 offered a very good load regulation, which avoids the problem just described. More precise voltage references are available on the market; however, these voltage references are not usually capable of sourcing the current needed for the modulation voltage reference of nine drivers. Because of the DC nature of the reference current, a decoupling capacitor was added to the reference line just before the variable resistance. This is done to minimize the effect of switching noise on the

printed circuit board. The noise will be damped by the variable resistance/capacitor network and will not affect the modulation amplitude over time.

The voltage threshold reference circuit is designed such that the nine drivers in the driver circuitry are adjusted individually. However, the uniformity test on the VCSELs indicated that the VCSELs did not need individual set points. From this result, the eight threshold voltage references were not populated on the final board and the output of the remaining one was redirected to all chip threshold reference inputs. The threshold voltage reference is implemented by a National Semiconductor LP2986 chip. This device featured an ultra low dropout voltage and a Sleep Mode [31]. The ultra low dropout voltage is a feature that allows adjusting the reference voltage to values close to the input power supply. Due to the large input range of the of maximum drive voltage of the VCSEL, if the regulator had featured a typical drop out of more than one Volt, it would have been hard to adjust the output reference voltage to the right value. The sleep mode allowed the VCSEL driver to completely be turned off if needed by starving the driver section of threshold reference. Without a threshold reference, the VCSEL driver completely turns the laser off. This feature of the reference circuit is important for safety issues. When the driver is not being used, it is possible to turn off the lasers without powering off anything else on the board. This facilitated debugging and testing.

Two types of signals are directed to the transmitter circuit. The first kind of signal is provided by simple connections to the controlling FPGA. These signals are used to control the state of the driver circuit and are of TTL types. The second type of signal is of much higher speed in nature. These signals carry the high-speed information the transmitter need to retransmit optically. These signals travel to the transmitter chip through impedance-controlled lines. The high-speed signals are AC coupled by a 0.01μf 0603 capacitor. The AC coupling permits the DC level between the signal source connected to the board to be different from the DC level used by the electrical receiver of the transmitter chip. The hunt signal was considered a high-speed signal for the driver chip design and the input was designed as such. However, in the final

design, the hunt signal was decided to be sourced by the control FPGA and a Motorola MC100ELT20 chip [32] is used to provide the required TTL-to-PECL level conversion. The termination voltage required by the input electrical receiver on the driver chip is provided by the national semiconductor LM1117MPX-3.3 chip.

The VCSEL drivers are tuned to the average threshold specified by the manufacturer and have a minimum threshold capability of 1.8V. The driver was not designed to handle the actual 1.58V average voltage threshold of the received VCSEL arrays. As soon as the drive voltage has to be lower than 1.8V, the driver differential switch transistors are sent into saturation which increases the jitter by order of magnitudes. To find a solution for this problem was not an easy task. The fix has to work on the high-speed side of the circuit and has to be implemented using devices external to the driver chip. The solution retained to solve this problem was to separate the backside voltage by a few hundred of millivolts with respect to the driver chip ground. A Hewlett Packard surface mount RF schottky barrier diodes model number HSMS2813 is used for task. As explained in the package section of this chapter, the package was laser machined to generate two "ground planes". The laser ground plane was connected to ground through the schottky. As the laser drive current was discharged through the diode, a potential difference was created between both leads of the schottky. This ircuit allowed the voltage threshold to be effectively increased by 0.5V to 0.6V, and the driver could operate as if the laser diode was within specifications. In order to maintain a good DC coherence between both cavity planes, chip decoupling capacitors were used in the cavity to connect the two DC planes. These capacitors are California Micro Devices' thin film NMOS capacitors. Simulations indicated that the bigger the capacitance used, the better the DC linking of the signal. However, because of space constraints, the biggest capacitors that could be used in the cavity were two 100pf (760μm on a side) capacitors. Because these capacitors are located inside the cavity, the inductance imposed by larger devices is avoided and the best coupling is achieved.

4.9. Driver Chip Simulation and Results

The first step in the system verification was to use HSPICE to simulate the VCSEL small threshold voltage compensation method, as well as the packaging effects on the driver chip. In the same simulation, the measured VCSEL parameters, the packaging parasitics, the driver circuit with parasitics extracted from the layout, and the schottky diode model were included. The eye diagram resulting from this simulation is shown in Figure 4.16. The simulation shows an open eye at 1.25 Gb/s and less than 25ps of jitter. The rise and fall times are in the 175 ps range, which is better than specified by the Gigabit Ethernet standard for this type of signal. Overshoots and signal distortions are caused by multiple effects introduced by the addition of the schottky diode. Great care was taken to remove much of these undesirable effects by minimizing the inductance of the conduction path to the schottky diode, and by linking the two chip substrates through decoupling capacitors. The solution presented here is believed to be an optimized solution, considering that the design of the chip could not be modified. It should be noted that the VCSEL model used in the simulation might not be well adapted to a dynamic signal since it was modeled by a simple RC network.

This simulation only gives an approximation of what the eye would look like in the real system. Actual testing was finally performed from this point on to gain further information about the transmitter.

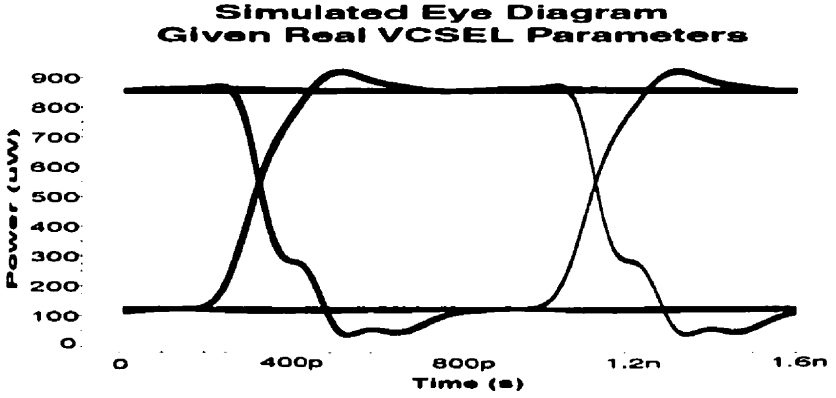

Figure 4.16 Simulated Eye Given Measured VCSEL characteristics. Input: PRBS Signal 27-1 at 1.25Gb/s

4.10. Conclusion

A driver matched to the VCSEL characteristics was developed to be used in an adaptive redundant optical interconnection. The driver was developed in the high-speed bipolar technology, NT25. The driver chip was designed such that the specific switching requirement of the free space interconnection could be achieved. The driver section of the chip was developed as a voltage driver partly due to the high-resistance of the VCSEL and partly due to the design limits imposed by the silicon technology being used. When simulated with the packaging and modifications necessary to correct for the out-of-specification parameters of the VCSELs, the driver shows a lot of promise for success. The remaining section of this thesis will focus on the physical performance of the driver and will conclude on ideas for the realization of better driver circuitry.

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Chapter 5- Testing and Performance

5.1. Introduction

The importance of proper tests and measurements of transmitter characteristics cannot be overemphasized. The design would have no value if it were not proven to work. It is important to know the characteristics of the transmitter in order to identify the limitations of the design, physical limitations of the current technology and improvements that need to be performed on the next generation design. The following sections will review the test procedures and test results for the transmitter design previously described in this thesis, beginning with a discussion of the test plan. The chapter will conclude with the high-speed test results that were performed on the transmitter. Note that the emitters used in the transmitter implementation were thoroughly characterized in parallel to the driver and these tests and results were reviewed in Chapter 3.

5.2. Test Plan

The test plan was developed early in the design phase so that the chip could be designed for testability. In order to design for testability, the following questions have to be answered [1]:

- Which test fixture is going to be used for the test?
- What is going to be the pad size, pad configuration?
- How will the chip be biased and powered up?
- What security protections have to be taken for the device under test (ESD) and for the persons performing the tests?
- Which test structures should be added to the chip?

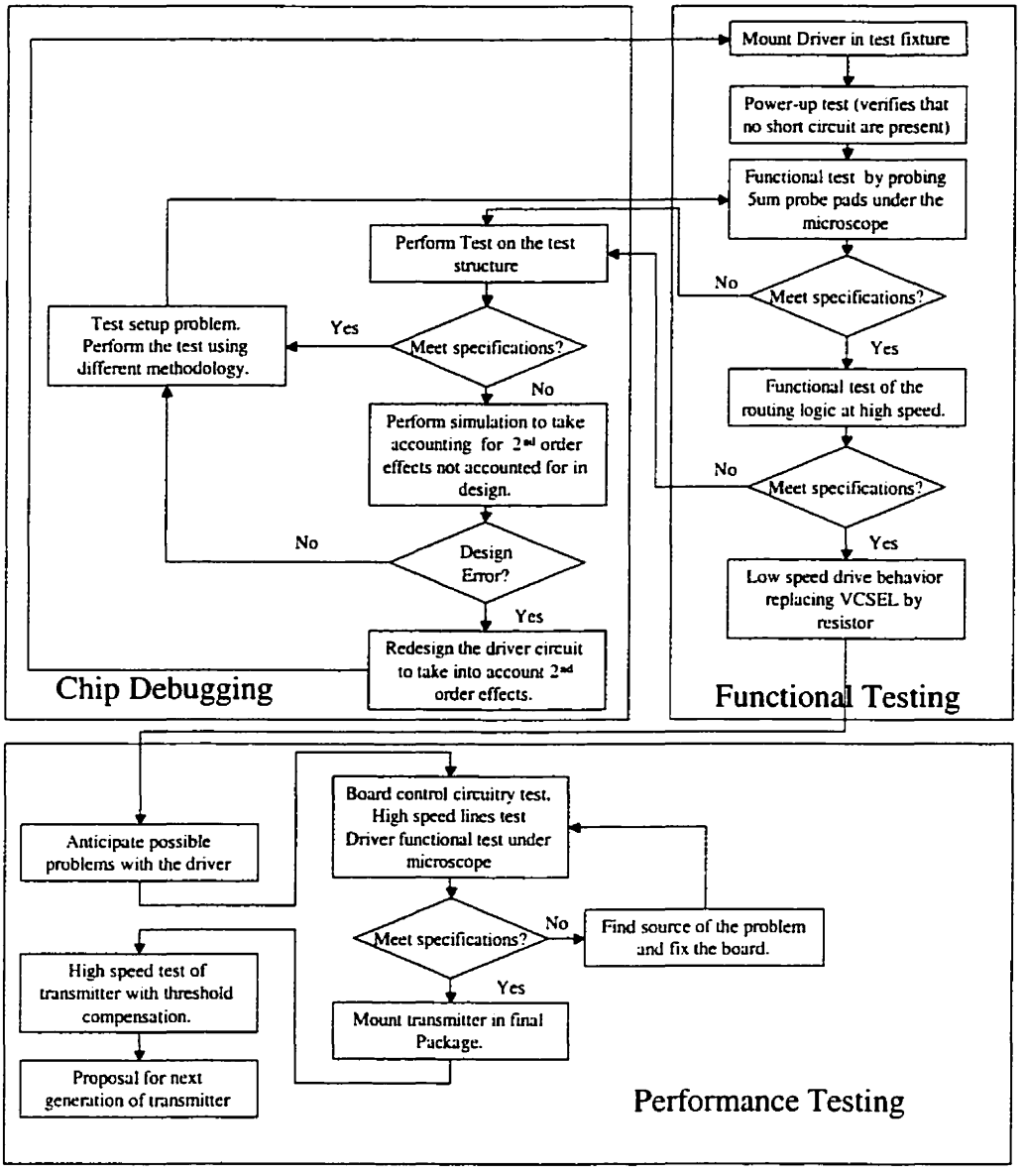

Figure 5.1 Simplified Test Plan Flow Chart

The test plan follows the flow diagram presented in Figure 5.1, it is sectioned in two major parts: the functional testing and the performance testing. In order to be tested thoroughly, the transmitter demanded a high-pin-count package, 18 voltage and current references, two termination voltages, adequate power distribution, and adequate signal distribution for both high and low speed signals. The final interconnection board was designed to include all the necessary biases for the transmitter. However, the final test board was scheduled to be available only 4 to 5 months after the arrival of the chip

from the foundry. A minimum had to be known about the chip functionality, since a chip redesign could have been the final answer to any eventual problem. Chip design re-spin would have had an important impact on the project schedule. Therefore, any functional test would indicate if the re-spin was necessary months before inclusion of the chip on the interconnection board. The performance test was developed for the final interconnection board. This test allowed for full functionality and characterization testing of the performance of the transmitter chip.

As described in the layout section of Chapter 4, test structures were added to the chip. These test structures were composed of one instance of each building block used in the chip. If one of the sections of the chip was suspected to be non-functional, it would have been possible to power up the test structure and verify the functionality of the building block independent of the rest of the chip. This would have been used in the chip debugging part of the test plan. Using this section would almost have meant failure of the chip. Not much could have been done if chip functionality was not met; most likely, a chip re-spin would have been the remedy to the problem. The chip debugging section of the test plan and the test structure inclusion on the die had to be done, since the failure of the chip was a possible outcome of the test procedure.

Probe pads for chip testing were added between every high-speed section of circuitry. These pads were square and 5μm on the side. This is the minimal size a test pad could be based on the lithography rules for the technology. Exact location of the pads was presented in Chapter 4. The test pads were made minimum size in order to reduce the loading on the high-speed track of the chip. Note that testing on the 5μm pads had to be performed using an active probe as they were the only probes small enough to reach the metal of the test pads. Active probing was also the only method that minimized the loading of the high-speed transmission lines. Limiting access of the small test points to active probes was important because the high speed line could not have supported a large probe loading; this would have destroyed the transistors on the chip. Other test pads were used on the test structures of the chip and test points for verification of the bias conditions of the chip. These were implemented as bond pads and could be

accessed by any type of probing or bonding method. In the case of the bias condition test point, these test points could be used to force the bias to the correct value if internal bias references were identified faulty.

Normal ESD procedures were used to ensure the security of the chip. As an example, the chips were kept in a desiccating cabinet. Their access was limited which minimized the risk of accident. When being manipulated, basic grounding rules were used which also minimize the risk of ESD problems. On the circuit side, ESD structures were added to the TTL translation buffer. These structures provided some protection against ESD discharges; however, loading of the ESD structures limited their use on DC and low-speed TTL signals, exposing the high-speed section of the chip to a higher risk of ESD related problems. With regards to safety issues, the lasers used were the biggest threat. The 960nm wavelength laser could have emitted a total of 9mW of optical power, classifying the assembly in the class 3b laser category. At any time that the lasers were on, only a camera was used to look at the chip surface. Using a microscope would have most certainly injured the person performing the test. In addition, normal laser security rules were used to minimize the risk of accident.

5.3. Functional Test

The functional tests were performed under an Alessi manual probing station. A photograph of the test setup used for functional testing is shown in Figure 5.2. For this test, a generic test board developed by the McGill Photonic system group [2] was used. This test board allowed for a limited high–speed test range on 32 lines connected to 32 SMA connectors. The limited number of test ports on this board limited the chip tests to two drivers and one high-speed section of the chip. Nevertheless, functional testing could be performed using this board. The majority of the high-speed lines on the test board were used for biasing and some minor modifications were performed on the board to ensure adequate decoupling of the driver chip. After one round of testing, the tests indicated poor chip functionality. The problem was traced to high frequency noise on the power and bias lines. This problem was solved by adding decoupling

capacitors in the DC line close to the chip; these were missing from the generic board. The chip was mounted using chip-on-board methods and wire bonded using long wire bonds, limiting the performance of the test. For these tests, none of the threshold voltage compensation mechanisms were available and no lasers were used. Instead, the VCSELs were replaced by 0603 surface-mount resistors. These resistors permited an emulation of the VCSELs at low speed. The various biases and powers to the chip were provided by commercial bench top low noise power supplies allowing for control of the biases to values lower and higher than the ones provided on the final board.

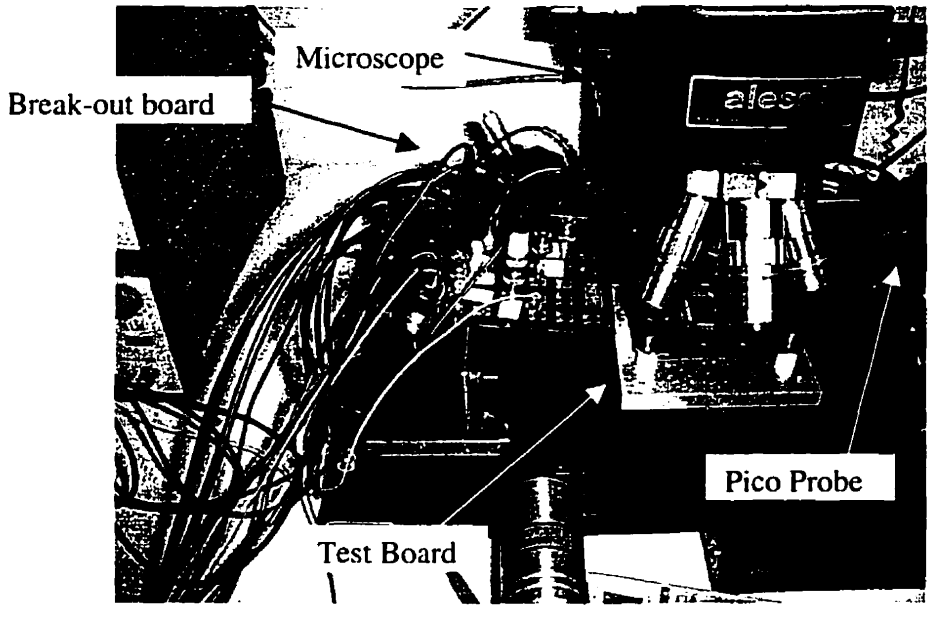

Figure 5.2 Functional test under process

The functional test starts with a power up test. During this test, power is gradually increased while the sink current is monitored. If the sink current reaches values much higher than predicted by simulation, then the possibility of a short circuit would have to be investigated. Fortunately, the test was conclusive and no problems were noted at this level. Following this functional testing was performed on the chip. In this test, a signal is injected into the input receiver of the chip and is followed on the traces after each circuit building block using probing techniques. Probing was performed with the Pico-Probe model 28 which was calculated to have a rise time of 338ps [3]. The

signals that were measured had rise times of the same order of magnitude and in general they had smaller ones. In order to have a better approximation of the rise time of the system under test, one has to remove the effect of the probe rise time on the measured signal. The rise time of the resulting signals, after passing through a probe, is equal to the square root of the sum of the squares of each rise time [4]. This is usually true for Gaussian pulse shape. Note that the rise time of the input to the oscilloscope is also a factor when de-embedding the rise-time. In the case of the Pico-probe measurements, however, the RF scope used had a rise time of 7ps and this variable was therefore negligible. The last point that has to be mentioned about probing the 5μm test pad is that the surface of the chip suffered organic contamination. This contamination created a greasy deposit on the test pad that was difficult to penetrate. For example, it was impossible to penetrate to some of the 5μm pads making it impossible to probe the signals after the second multiplexer stage. The functionality of the second multiplexer stage was investigated through the laser driver.

The signals were probed after the electrical input receiver of the chip. Functionally at this point demonstrated open eyes. The rise time at this point was 210ps and the fall time was 305ps. These measurements were 71% longer than those in simulations. The longer rise time was probably due to the input being distorted by long transmission lines >20cm and by loading caused by the chip package and wire bonds. The performance of the chip should not be affected by this discrepancy, as signals with responses around 260ps were good enough for gigabit Ethernet applications. The results after the second multiplexer indicated that the input signals were switched as expected by the multiplexer and therefore passed the functionality test. The rise time at this point was measured to be 204ps and the fall time was 150ps. After the multiplexer, the signal had recovered from the board distortion, was re-amplified, and partially reshaped.

The TTL input converter was tested using the on-chip test structure. In that case of the TTL buffer, the test structure was powered on at the same time as all other TTL translator making probing easier. It was simple to inject a TTL compatible signal into

the structure to verify functionality from the large output test pads. The driver had a measured 441ps rise time and an 820ps fall time. The eye was suitably open for switching speeds up to 200Mhz. The dominant effect limiting the switching speed was the ringing at the input of the chip. The results from the TTL input buffer were better than expected and better than it needed to be. Switching conditions of the translator were verified compatible with simulations results.

The laser driver was tested using a resistor in order to emulate the VCSEL. First, the second row of multiplexers was tested for functionality. It was determined that the device was switching the signals on and off as expected. The driver was then tested. The driver responded to input bias changes by changing output modulation as expected from simulations. The driver was tested up to 400Mb/s NRZ, a rise time of 1.7ns and fall time of 1.5ns were measured. The output signal had a 2.2V modulation output and the emulation resistor was 300Ω. These conditions were probably responsible for the poor driver performance. Since the driver will be driving a different load in the real system, performance tests were postponed to a later test, but driver functionality was deemed good.

5.4. Performance Tests

The performance test involved testing the transmitter at high speed with VCSELs and measuring the optical properties of the signal. In the previous tests, no problem was found other than noted performance degradations; therefore, no problems other than possible speed limitations were anticipated. The performance tests carried out on the final FSOI board since this board was equipped with all necessary voltage and current biases for the transmitter. In addition, the necessary low threshold voltage correction schottky diode was present on the final board allowing for full optical testing using the VCSEL as a load on the transmitter. The board functional circuitry was verified to be working as expected. The FPGA was programmed such that it controlled the TTL signals on the driver chip more easily to select a driver state. The laser states were selected using a dipswitch on the side of the board. The program made it such that the lasers were modulated one at a time by specifying the laser identification number on the dipswitch using binary code. The program also gave the possibility of modulating no laser and modulating all lasers by switching on and off a different set of dipswitches. The transmission line impedance was measured on the final board using a TDR (time domain reflectometry) method. It was established that the line had an impedance of 60Ω. This condition will probably affect the input of the high-speed signal to the chip as all the terminations were designed for 50Ω. Nevertheless, the test will still be performed as the transmissions lines were very short and this problem should have only a limited impact on the signal-to-noise ratio of the system.

The first step in testing the transmitter was to mount the transmitter on the board in the package as described in the previous chapter. The modulation and voltage threshold were then adjusted. The presence of the schottky diode made it hard to set the lasers to a known states. When one laser was adjusted, the current increased in the schottky diode, which in turn increase the voltage drop on the diode. Such an increase on the schottky involved an effectively reduced threshold voltage level. This meant that when adjusting the next laser, the laser previously adjusted was partially de-adjusted. In

order to minimize this effect, the threshold was adjusted by changing the modulation levels in cycling through the lasers in an iterative fashion until all VCSELs were set to the desired point. The biases were adjusted under the Alessi probing station while the VCSEL output power levels were monitored using an optical power meter.

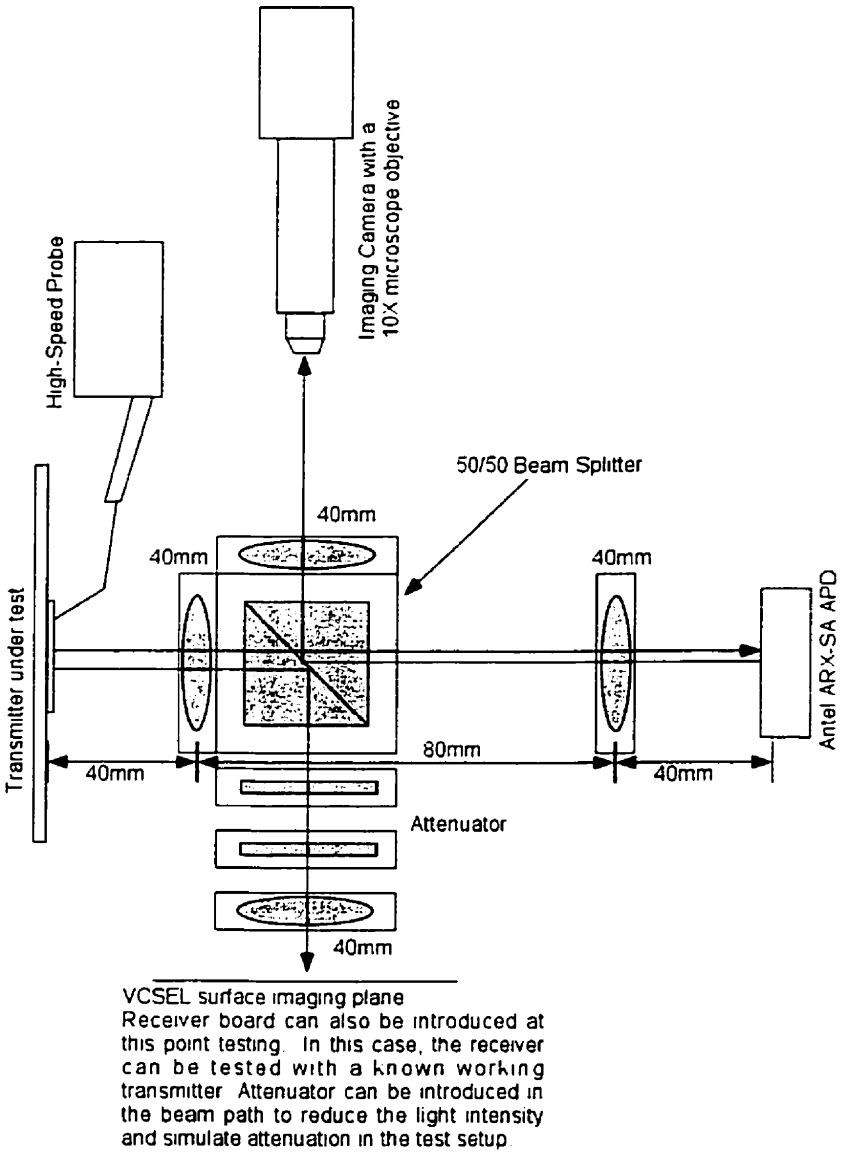

Figure 5.3 Optical test setup for performance tests

Once the board was adjusted for DC biases, the driver was ready for the optical performance tests. These tests were performed in the setup depicted by Figure 5.3. This setup is a simple imaging system that allows the beam to be optically relayed using two telecentric lenses configurations [5-6]. By using two 40mm focal length lens, separated by 80mm, the image at the focal point of the first lens is relayed to the focal point of the second lens. A beam-splitter was introduced in the path to allow for monitoring the signal position on the photo-receiver with a CCD camera. The beam-splitter was positioned in an unsymmetrical fashion in order to allow for the introduction of neutral density filters and power meter heads in the beam path. The beam splitter also allowed for relaying the beam from the transmitter onto a receiver under test.

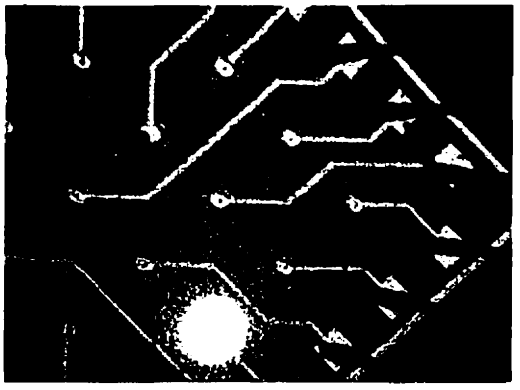

Figure 5.4 VCSEL stimulated during performance test

Figure 5.4 shows the image of a VCSEL being powered up and modulated during performance testing. It is also possible to see the other VCSELs being slightly above threshold, however, the powered up laser is much brighter which slightly masks the other VCSEL outputs. The chip logic was characterized in full during the functional test and was expected to also be working in the performance test since the conditions stayed the same for this part.

The first thing that was verified during the performance test was the inter-driver cross talk. The test consisted of measuring the voltage and the optical signal on a non-modulated driver adjacent to a modulated driver. No voltage or optical modulation was measured on the non-modulated driver and therefore no cross talk was measurable using our equipment. The next electrical parameter of interest was the VCSEL ground modulation. The schottky was sensitive to the modulated current despite the fact that great care was taken to stabilize the VCSEL ground plane voltage so that it would not be modulated at the same time as the VCSEL. When one VCSEL was modulated, no change was observed in the VCSEL ground plane. The voltage at this plane was stable 0.49V higher than the chip ground plane. The VCSEL low voltage threshold compensation circuitry was working as expected, as a stable voltage bias. When all VCSELs were modulated (which is the case when trying to find a good link during the hunt), a 0.2V modulation was measured. This modulation can be expected as the modulation current is not nine times higher than in the case where one VCSEL is used. The non-linear response of the schottky diode also accentuates this factor. In order to compensate for this issue, much bigger decoupling capacitors would need to be used in the package cavity. The VCSEL ground modulation in this case will increase the noise present on the links if all VCSELs are modulated at the same time. However, the hunt does not depend on a low BER and this noise hit should not be critical.

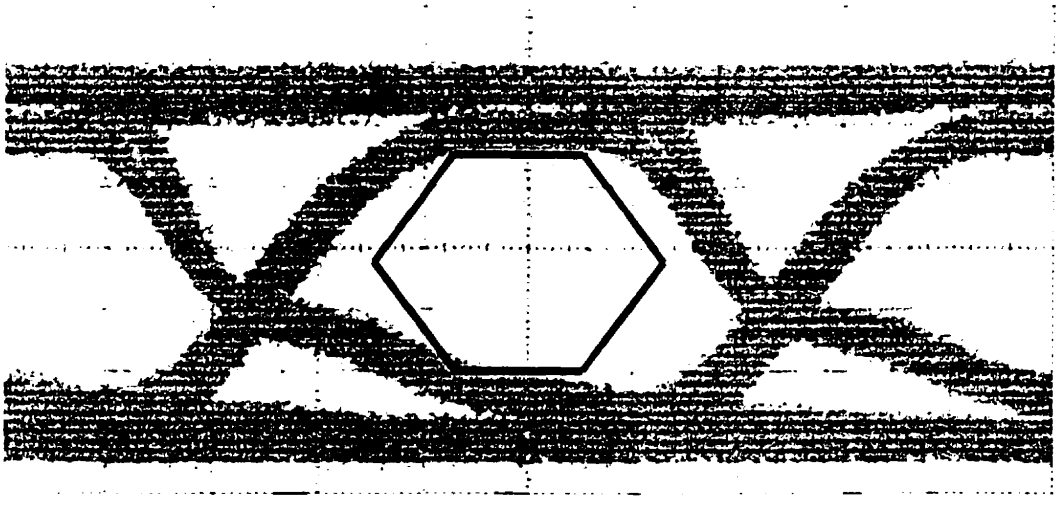

Figure 5.5 Optical Eye Mask results from performance test

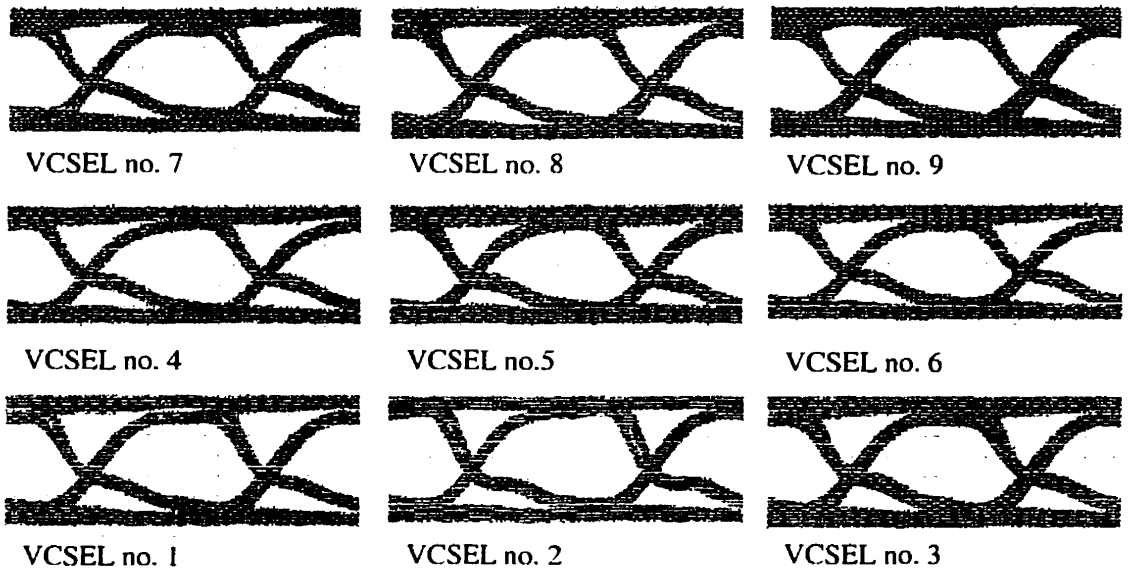

Figure 5.6 Results from the nine VCSEL being stimulated

The optical test consisted of measuring the output from the transmitter using an ANTEL 2Ghz APD model ARX-SA with a 210ps rise time [7]. The measured signal can be seen in Figure 5.5. Note that optical levels were inverted by the APD. This eye was modulated at 1Gb/s and a scaled gigabit Ethernet was overlaid on it. It is seen that the output is almost compliant with the gigabit Ethernet signal. The VCSEL response is the major limiting factor for optical signal compliance. At 1.25Gb/s, the VCSEL response have an even worst impact. However, if better VCSELs were used, the driver should be capable of sourcing at the full rate and still comply to the mask without any problems. When driven at speeds of 1.25Gb/s, the optical eye is still open but does not comply with the mask; the signal distortion comes into play. It could be concluded that at full speed, the transmitter has a limited performance due to the laser time response. The rise time of the optical signal was measured to be 430ps and the fall time was found to be 340ps. Rise and fall times were about double than that simulated. This is again due to signal distortions caused by the VCSEL time response. All eye diagrams

from all VCSELs can be viewed in Figure 5.6. This figure shows that all channels have similar responses, which is important in an arrayed transmitter.

The final test was to insert the receiver chip designed for the interconnection in the optical setup. Operations were proven to be working up to speeds of 400Mb/s and were limited by the receiver response. The receiver was limited to these speeds as measured independently before its integration in the transmitter test setup. This proved that a limited speed channel could be operated using the full FSOI chip set.

5.5. Conclusion

A test plan was developed to test the driver chip and the transmitter that were designed for the free space optical interconnection. The driver chip was proven to be functional and had the required performance to transmit the high-speed signals optically through the free space interconnection. However, the full transmitter was proven only to fully comply only with speed 20% lower than that of the original the design. Preliminary tests were performed on a TX-RX link proving operation speeds of 400Mb/s.

Further tests need to be performed in order to confirm full functionality of the transmitter when used in the system with the designed receiver chip. Bit error rate testing should be performed on the full link and the alignment tolerances of the system still needs to be verified. These tests will be performed as part of the optical link characterization work, which will not be presented in this thesis. It is the final system results that will judge the true quality of the transmitter design.

5.6. References

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Chapter 6- Conclusion and future work

This thesis has dealt with a broad range of topics concerning the development of a transmitter designed for an adaptive redundant free space interconnection. The first sections dealt with and explained the need for free space optical interconnections. The need to make these types of interconnections alignment friendly was then highlighted and today's proposed methods to render them simple to align were presented. Issues concerning alignment difficulty are preventing FSOI from obtaining wide-scale acceptance throughout the electronic industry. One of the most promising methods to make FSOI alignment friendly is to make them adapt to misalignments through adaptive methods. One of the most promising methods to date is to make the transmission channel redundant throughout the alignment possibility enabling very dense and high-speed free space interconnections without sacrificing the ease of interconnection. In this case a symbiotic relationship exists between optics, which relieves the interconnection bottleneck in the electronic systems; and electronics, which simplifies the alignment.

The first implementation of a redundant system for interconnection alignment was presented. The receiver, optical system and transmitter were presented to give a grasp of the system complexity even in the case of a one-channel interconnection. In the future, adaptive redundant FSOI will need to be scaled to very large array in order to compete in bandwidth with existing electrical interconnections. Several of the issues introduced by scaling the number of channels were introduced and further studies will need to be performed. Optical cross talk could introduce noise thereby limiting the error rate and reach of redundant interconnections. Very careful architecture engineering will be needed to make the FSOI reach their limit potential. In addition, the protocols used carry the data in the implementation introduced were not optimized to make full use of the link properties. Buffering would be needed to make the interconnect alignment phase transparent to the transmitting electronic systems. As well, out-of-band or even in-band signaling could be added to an eventual transmission protocol in order to signal the alignment state of the interconnection and predict the

next best transmission pairs. Such a prediction would minimize the down time for the interconnection as the alignment changes.

Essential to FSOI and optical interconnection in general, the VCSEL was introduced. A complete electrical and optical characterization of the VCSEL used for the optical interconnect implementation was presented. Unfortunately, the initial specifications of the VCSEL arrays were far from the actual laser characteristics. The development of future VCSEL drivers will have to take these new specifications into consideration as the driver needs to be tuned to the VCSEL in order to provide the best performance. In addition, the VCSELs will them selves continue to develop. New wavelengths like 1300nm and higher bandwidth VCSELs are already becoming available. As they become available, these new devices will likely impact free space interconnections by adding new applications in which they are not used.

Single modes VCSEL driver circuits do not have the same structure as drivers used for edge-emitters. Many differences exist between both of these structures. First, the series resistance of single mode VCSELs is a few time higher than that of edge-emitters. In addition, today's VCSELs are exhibiting much lower drive and threshold currents than edge emitters. These differences demand lead to very different drive characteristics; and therefore, very different drive circuitry. A special high-speed driver circuitry was developed to tailor the development of the adaptive free space optical interconnection. The circuit included all the necessary high-speed routing for the redundant interconnection as well as the driver circuitry. A future implementation of the driver should include on-chip digital-to-analog converters in order to set the bias and modulation levels. This exercise will minimize the complexity of the external references for the driver and make temperature compensation of these parameters possible. The high uniformity of the VCSEL arrays point to the fact that only two references are needed: one for modulation level, and one for threshold level. Since the reference circuits are very simple, their inclusion at the chip level is very attractive, as they would not take up any more board space and are easy to implement in silicon.

The transmitter packaging was introduced. In opto-electronics, packaging is even more important than for straight electronics. The package has to allow for electrical interconnections to the rest of the system and optical interconnections to the receiving module. The package chosen for the FSOI was a laser machined CERQUAD package. The package proved to behave better than that required for the FSOI. Every circuit implementation demands an original package solution. We can be confident that future FSOI implementations will have different packaging strategies in order to fulfill new interconnection requirements.

Tests on the driver circuitry demonstrated that the transmitter worked with characteristics inferior to the simulated behavior. However, the transmitter should still be capable of transmitting the required signal through the interconnection at the required bit rate. More investigations still need to be done on the interconnection in order to verify if the system works when all the parts are assembled together.

Although many technologies are competing with FSOI as a solution for the board-to-board, shelf-to-shelf, and rack-to-rack connections, FSOI still offer the lowest cost and simplest solutions. Once alignment is proven easily feasible for short reach free space optical interconnections, they should be rapidly coming to the market place. It is certain that as technology evolves, FSOI will have to be used in electronic systems. The future density requirement imposed by future electronic can only be addressed by optic; free space optic is the best of the optical solution when considering density. Free space links are presently being deployed for high-bandwidth connections linking the point of presence to end-users. These applications are involved in crossing the last-mile which fiber has not crossed yet for cost reasons. In the view of these developments, a bright future for FSOI is foreseen.