Extraction of RLC Parasitics from a Flexible Electronic Hybrid Assembly

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Abstract

This thesis presents a technique for extracting the RLC parasitics from a Flexible Hybrid Electronics assembly. The presence of RLC parasitics is a signal integrity concern and their progression can lead to a catastrophic failure of an electronic system. Therefore, tracking the variation of RLC parasitics from a flexible hybrid electronics assembly is fundamental to assessing the success of the technology.

While the parasitics LC are extractable through one port reflection-based techniques such as time domain reflectometry; the parasitic series resistance R requires 2 port measurement such as a Kelvin test, which is extremely difficult to perform for printed conductors bonded to small surface-mount IC package devices. The proposed method exploits on-chip ESD (Electro-Static-Discharge) protection circuits in order to extract the RLC parameters of the printed conductors bonded to an IC chip through an on-board one-port access point.

The accuracy of the extracted RLC parameters with the proposed method is validated with a prototype developed on rigid FR4. Then, the proposed technique is utilized to track the variation of RLC parasitics for prototypes developed on Kapton Polyimide substrate subjected different forms of bending.

Further, the practical challenges and corresponding measures for applying the proposed technique to In-Circuit-Testing are discussed.

Abrégé

Cette thèse présente une technique d'extraction des parasites RLC à partir d'un flexible hybride électronique assemblage. La présence de parasites RLC est un problème d'intégrité du signal et leur progression peut conduire à une défaillance catastrophique d'un système électronique. Par conséquent, le suivi de la variation des parasites RLC à partir d'un flexible hybride électronique assemblage est fondamental pour évaluer le succès de la technologie.

Alors que les parasites LC sont extractibles grâce à 1 port mesures basées sur la technique de réflexion, comme la réflectométrie du domaine du temps; le R parasite exige 2 port mesures telles que l'essai de Kelvin, qui est extrêmement difficile à exécuter pour les conducteurs imprimés collés aux petits dispositifs d'emballage IC de surface-montage. La méthode proposée exploite les circuits de protection ESD (Electro-Static-Discharge) sur puce afin d'extraire les paramètres RLC des conducteurs imprimés collés à une puce IC par un port d'accès aux points d'essai embarqués.

La précision des paramètres RLC extraits avec la méthode proposée est validée par un prototype développé sur FR4 rigide. Ensuite, la technique proposée est utilisée pour suivre la variation des parasites RLC pour les prototypes développés sur le substrat de Polyimide Kapton soumis à différentes formes de flexion.

En outre, les défis pratiques et les mesures correspondantes pour l'application de la technique proposée aux essais en circuit sont discutés.

Acknowledgements

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List of Acronyms

FHE	Flexible Hybrid Electronics
RLC	Resistance, Inductance, Capacitance
Si	Silicon
Cu	Copper
Ag	Silver
IC	Integrated Circuit
ESD	Electro-Static Discharge
PCB	Printed Circuit Board
AC	Alternating Current
DC	Direct Current
TDR	Time Domain Reflectometry
ICT	In-Circuit-Test

Chapter 1

Introduction

1.1 Motivation

Flexible electronics features low cost of manufacturability and unconventional form factor. It is rapidly finding various main-stream applications in healthcare [1-3], agriculture [4,5], and structural health monitoring [6,7]. A research from IDTechEx projects exponential growth of the market for healthcare products containing flexible electronics and prognosticates this market to exceed 8.3 billion USD in terms of annual revenue by 2030 as depicted in Fig. 1.1 [8]. Notably, the COVID-19 pandemic necessitates rapid deployment of the healthcare services in remote form. In this regard, flexible electronics can facilitate remote health monitoring by better interfacing of the health monitoring devices with human body and enhancing long term comfort of the patients to the medical interventions [8].

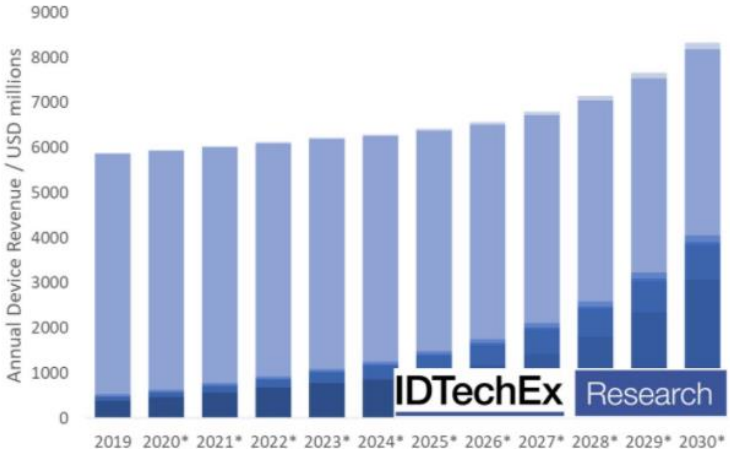


Fig. 1.1: Projection of annual revenue from healthcare devices containing flexible electronics [8].

Employing technologies such as printing allows for low cost manufacturing of flexible electronic devices. Despite manifold advantages of printed electronics, it is still inferior to state-of-the-art Si-based electronics in terms of data rate, scalability, signal integrity and reliability. Flexible Hybrid Electronics (FHE) on the other hand integrates the printed electronics and Si-based rigid electronics on a flexible substrate as illustrated in Fig. 1.2. The rationale behind the integration of the two technologies is to exploit the superior performance of Si-based electronics and flexible form factor of printed electronics in a complementary manner [9].

Structural conformation experienced by the printed conductors on an FHE assembly raises reliability and signal integrity concerns [10-14]. Flexing introduces stress in the printed conductors and connections as illustrated in Fig. 1.3(a). Recurrent stress causes formation and propagation of the cracks in the printed conductors [14]. The propagating cracks lead to increase in parasitic resistance R, which, in turn, culminate into ultimate loss of electrical connection [15,16]. Therefore, tracking these parasitic resistances is fundamental to the success of this technology. In addition, high frequency applications demand consideration of the parasitic inductance L and capacitance C associated with the printed conductors. These L and C on an FHE assembly can be subject to variation as well due to change in dielectric separation and medium as shown in Fig. 1.3(b).

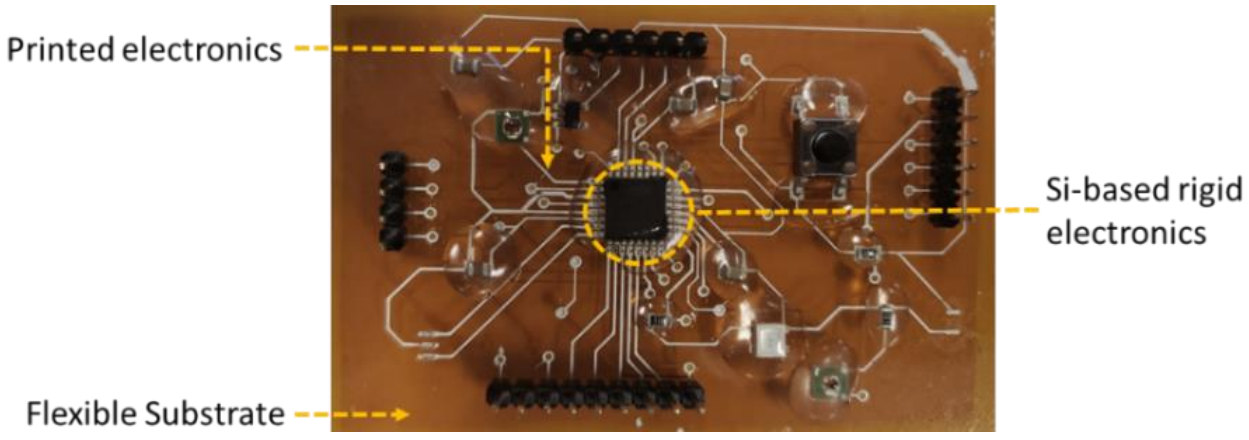
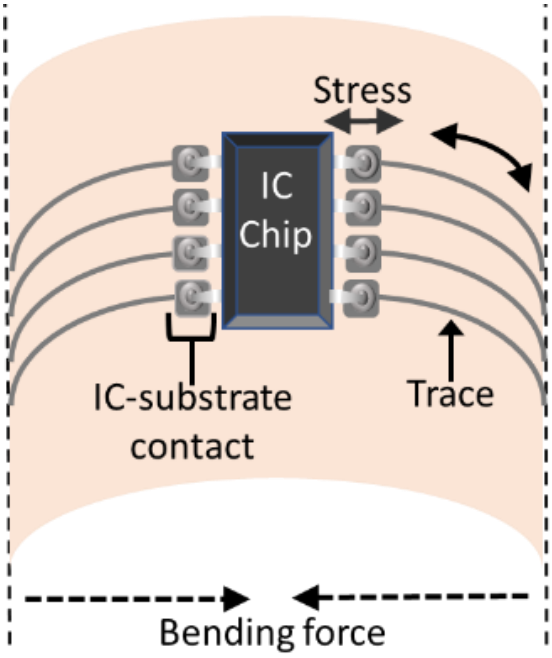


Fig. 1.2: Photograph of an FHE assembly.



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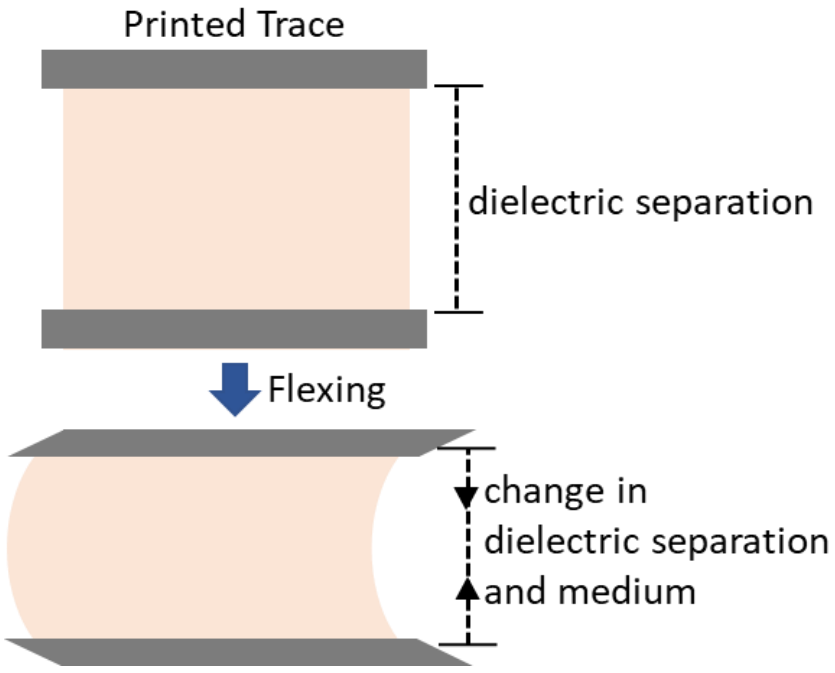

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Fig. 1.3: Impact of flexing an FHE assembly: a) stress induced on printed conductors b) change in dielectric separation and medium between two printed conductors.

1.2 Thesis Outline

This thesis aims to provide a means for extraction and tracking of the RLC parasitics from a flexible electronic hybrid assembly. In this work, printed conductors along with their return path is treated as transmission lines and the associated RLC parasitics are considered as the parameters of the transmission line model.

Chapter 2 reviews the research works on the modelling and extraction of PCB parasitics and the variation of the parasitics on flexible PCB. The necessity of the proposed extraction method in contrast to the existing ones is also discussed in this chapter.

Chapter 3 reviews the theory of transmission line modelling and delineates the approximations utilized in this work.

Next, in **Chapter 4**, a technique for extracting the RLC parameters of two printed conductors acting as a transmission line bonded to a commercial IC chip using the on-chip ESD protection circuit is proposed. Also, a way of isolating the parasitic R of an individual printed conductor bonded to a single IC pin is demonstrated. At the end of chapter, the verification of the proposed measurement method with simulations is presented.

In **Chapter 5**, the challenges and corresponding measures for applying the proposed technique to In-Circuit-Testing (test run on post assembled PCB) are discussed.

Chapter 6 introduces the techniques based on different measurement principles which are utilized to validate the extracted parameters with the proposed method. The details of the experimental setups for validating the proposed measurement method and demonstrating its usefulness are included in this chapter.

In **Chapter 7,** the results of the experiments described in the preceding chapter are demonstrated and discussed.

Finally, in **Chapter 8**, the conclusions are drawn. Also, the scopes for future work are discussed in this chapter.

1.3 Thesis Contribution

This thesis proposes a measurement technique for appropriate assessment of parasitic variation on an FHE assembly. It has following contributions to original knowledge.

• Transaction Submission:

“Extracting RLC Parasitics from a Flexible Electronic Hybrid Assembly Using On-Chip ESD Protection Circuits” Rafid Adnan Khan, Mohammad Muhtady Muhaisin, Gordon W. Roberts, IEEE Transactions on Circuits and Systems 1 (TCAS1), (under revision).

• Conference Submission:

“An In-Situ Technique for Measuring the Individual Contact Resistance Between the Pins of an IC Package and the Board of a Flexible Hybrid Electronic System” Rafid Adnan Khan, Mohammad Muhtady Muhaisin, Gordon W. Roberts, IEEE International Symposium on Circuits and Systems (ISCAS), 2020.

Chapter 2

Literature Review

This chapter is divided into two sections. The first section reviews the relevant research works on modelling and extraction of the PCB parasitics, and also focuses on the necessity of the proposed parasitic extraction method. The second section reports the research works on the variation of parasitics in a flexible PCB and discusses the scopes for further research works in this domain.

2.1 On Modelling and Extraction of PCB Parasitics

The parasitics associated with a printed conductor along with its return path are essentially the parameters of a transmission line model. As the spectral content of a signal approach higher frequencies, the treatment of printed conductors on a PCB as transmission lines is essential to consider the impact of parasitics on the signal integrity parameters (such as delay, reflection, attenuation, etc.) [17-19]. Transmission line models can be broadly classified into 2 types: lossy model and lossless model. A lossy transmission line model can be described in terms of a conductor series resistance R_{TL}, series inductance L_{TL}, shunt capacitance C_{TL} and a dielectric conductance G_{TL} (G_{TL} is negligible up to very high frequency). In contrast, a lossless transmission model ignores R_{TL} and G_{TL}, assuming they become negligible at high frequency compared to the series reactance ($j\omega L_{TL}$) and shunt susceptance ($j\omega C_{TL}$), respectively. The lossless model is a mathematical abstract, which is limited to certain high frequency applications only.

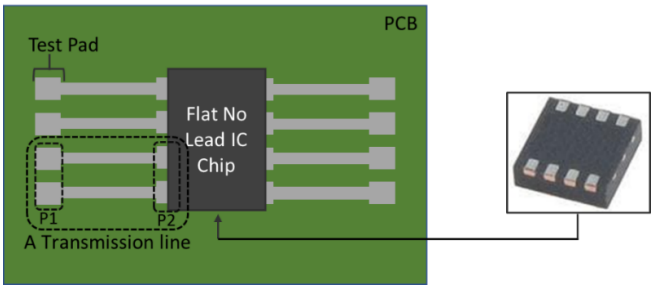
In order to extract transmission line parasitics on a PCB, majority of the efforts rely on high frequency reflection-based techniques. In this regard, Dascher demonstrated utilization of TDR (Time Domain Reflectometry) to find the PCB parasitics [20]. Here, characteristic impedance Z_0 and end to end time delay T_D of a uniformly distributed PCB transmission line is determined first using TDR and then the determined values of Z_0 and T_D are used to compute the L_{TL} and C_{TL} of the uniform PCB transmission line. Hashino et al. utilized TDR to determine parasitic L_{TL} and C_{TL} of a nonuniform transmission line on a power electronic PCB [21]. Lei et al. presented a built-in TDR test for monitoring discontinuity in the distribution of line parasitics on a flexible hybrid electronic system [22]. These TDR based approaches describe the parameters of the lossless transmission line model and their distribution exploiting reflection generated by a fast-edged signal. However, these methods cannot precisely describe the lossy parameters of the line.

Several research works stress on the importance of modelling and extraction of the lossy parameters of the line in addition to the lossless parameters for addressing important signal integrity concerns; such as signal attenuation at low frequency under small termination load [23], loss effect for long length [24], attenuation of the high frequency spectral contents [19], description of transmission line self-damping [25], determination of the electric and magnetic field variables [26] and determination of the chaotic circuit behavior [27]. Besides, in case of FHE assembly, the lossy parameter R_{TL} is subject to significant variations from the mechanical stress of flexing [28], and this variation can culminate into a catastrophic failure of electrical connection. Therefore, in case of an FHE assembly, the extraction of the lossy parameter R_{TL} is deemed essential for appropriate assessment of both the signal integrity and device reliability.

The lossy parameter R_{TL} can be extracted at low frequency using Four-Wire Kelvin Test [29] separately on the constituent printed conductors. This will require access to the two ports of a transmission line. While, at high frequency as the lossy parameter G_{TL} and frequency dependent increase of R_{TL} due to proximity effect (change in the conductor current distribution due to magnetic field resulting from the current in another conductor in proximity [30]) become considerable , the separate measurement of two constituent conductors do not completely account for the lossy behavior of the transmission line. The extraction of transmission line lossy parameters is achievable at high frequency using two-port S-parameter measurement [31,32].

However, a two-port measurement of transmission lines bonded to IC chips on an FHE assembly is challenging to implement as this requires post solder probing at the IC pins. This is difficult to accomplish as the IC pins are extremely small and often located underneath the IC package with no access as depicted in the Fig. 2.1. Even when the IC pins are accessible, repeated probing at the pins to track the parasitics from an FHE assembly can accumulate additional stress at the IC-substrate contact, thereby altering the measured quantity.

Consequently, in order to extract the parameters of a lossy transmission line on an FHE assembly, it is necessary to find a one-port measurement technique that eliminates the need for probing at the IC pins. In the proposed approach, we exploit on-chip ESD protection circuitry in commercial ICs to extract the parameters of the lossy transmission lines bonded to an IC chip on an FHE assembly. The extraction technique obviates the need for post solder probing at the IC pins and relies on direct computation of the data from one-port impedance measurements. Notably, the measurement method also allows for the isolation of the parasitic resistance of an individual printed conductor bonded to single IC pin. This feature bears critical importance for an FHE assembly, as parasitic resistance of different printed conductors on the same substrate can vary differently due to the nonuniformity of fabrication and stress distribution.



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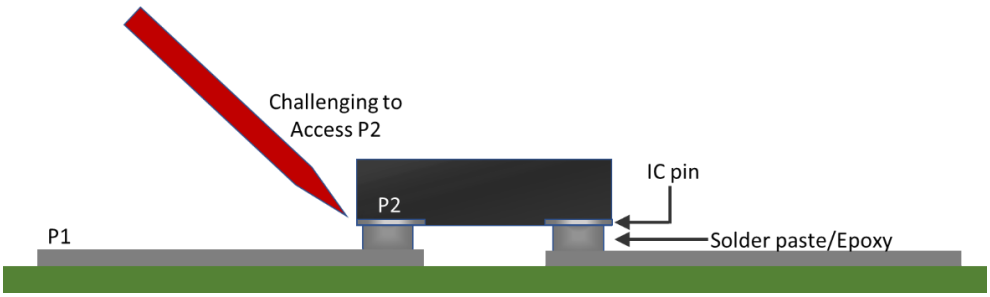


(b)

Fig. 2.1: a) a PCB transmission line with two ports marked as P1 and P2 b) challenge in conducting two port measurement of the transmission line bonded to flat no lead IC chip.

2.2 On Variation of Parasitics in Flexible PCB

To detect and analyze the variation of parasitics on a flexible PCB, several efforts have been made. Kim et al. reported gradual rise in the R of printed Cu (copper) traces on flexible substrate with the increase in the number of bending cycles [33]. They varied the bending strain on the traces by changing the bending radius and demonstrated the variation in the R increase with the increase of bending strain due to reduction of bending radius, as depicted by the Fig. 2.2. They observed cracks as shown in Fig. 2.3 in the parts of the printed conductor presenting increased R and attributed the increase of R with bending cycles to the propagation of the cracks resulting from the bending strain. They also observed when the bending radius is large, the strain is so small that no cracks are formed in the conductive trace. Therefore, there is no significant change in the R of the conductive trace with the increase of bending cycles, as observed for 0.7% bending strain in the Fig. 2.2.

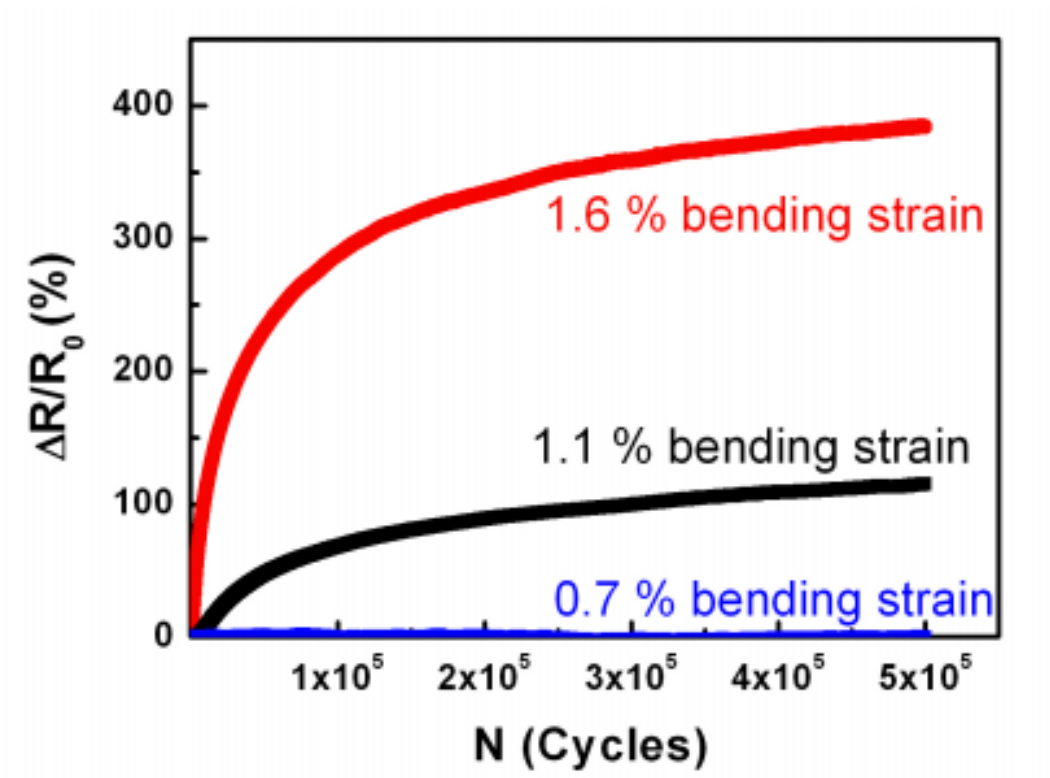


Fig. 2.2: Relative change in resistance of a Cu trace against the number of bending cycles for different levels of bending strain [33].

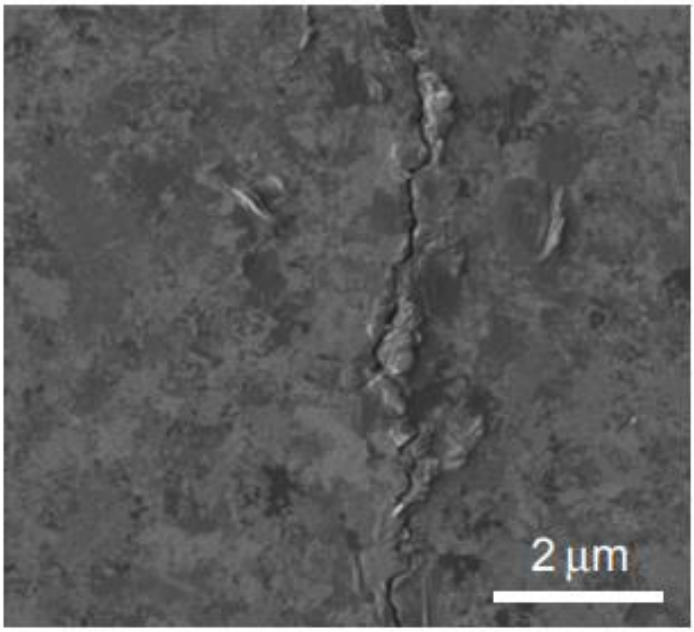
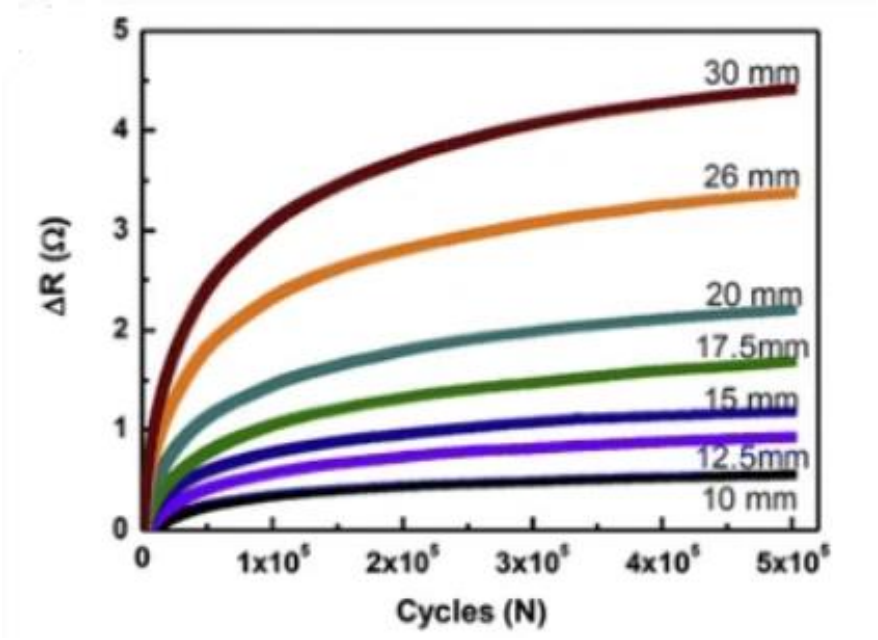


Fig. 2.3: Microscope image of a propagating crack on Cu trace [33].

Also, Yi et. al. reported increase in the R of printed copper traces due to evolution of cracks upon bending strain [10]. They further demonstrated the increase in the R of printed traces depend on the thickness of the trace and annealing level during its fabrication as depicted in the Fig. 2.4. Fig. 2.4(a) shows higher increase in the R for Cu traces upon bending as the thickness of the traces are increased. This is due to increase of bending strain with the increase in thickness of the film. Fig. 2.4(b) shows as the annealing temperature to evaporate the composite materials (materials mixed with metal particles to obtain printable ink) of inkjet printed Ag (silver) traces is increased over a certain level, the R of the printed conductor shows larger variations with the increasing bending cycles. While, the pure Ag film of same dimension deposited directly by evaporation shows highest degree of R variation with the increase of bending cycles. Although the metal traces become more conductive as more of composite materials from the ink are evaporated out by higher levels of annealing temperature, they become more brittle at the same time. Consequently, conductive traces annealed at higher temperature show increased R variation upon bending. Several other research works demonstrate the degradation of electrical R as well as catastrophic failure of electrical connection due to formation and propagation of cracks upon subjecting conductive traces on flexible substrate to bending [34,35]. Majority of these research works investigating variation of parasitics on a flexible PCB focus on characterizing parasitic resistance of standalone printed traces subjected to stress.



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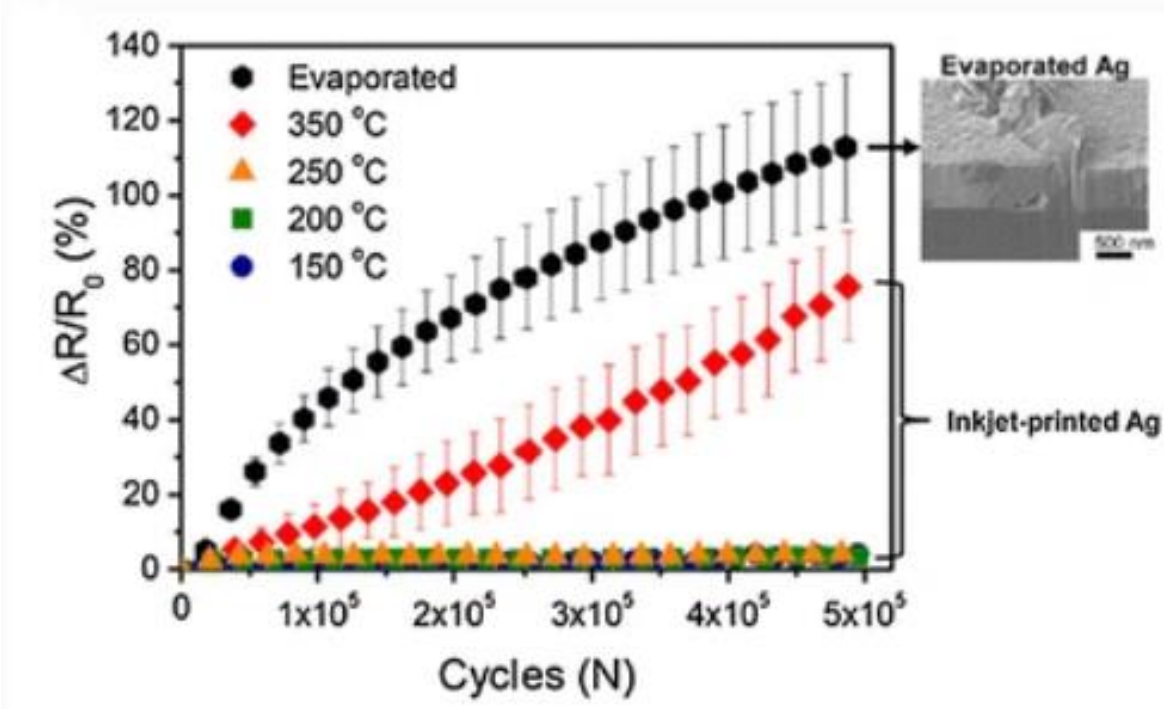


(b)

Fig. 2.4: (a) Change in the resistance of Cu traces against number of bending cycles for different trace thickness b) Relative change in the resistance of Ag traces against number of bending cycles for different annealing temperature [10].

A few studies involving Si-based rigid electronics on flexible substrates using optical techniques have inferred the variation in the stress distribution on the printed conductors due to the placement of the rigid parts [13,14]. As an impact of this, Soman et al. observes consistent cracking in flexible conductive traces close to solder joints of a rigid IC chip as shown in Fig. 2.5 [14]. Consequently, complex arrangements of commercial ICs on a flexible substrate is expected to have impact on the parasitic behavior, such as changes in R. Therefore, investigating the parasitic element variation of printed conductors bonded to an IC chip on an FHE assembly is essential for appropriate assessment of the reliability and signal integrity concerns of the technology.

In the available literature, no research work on electrical characterization of printed conductors bonded to IC chips on an FHE assembly has been reported. In addition, there has been no study investigating parasitic L and C and their variation on an FHE assembly. Thereby, this thesis aims to explore the variation of RLC parasitics of printed conductors bonded to IC chips on an FHE assembly employing the proposed measurement method.

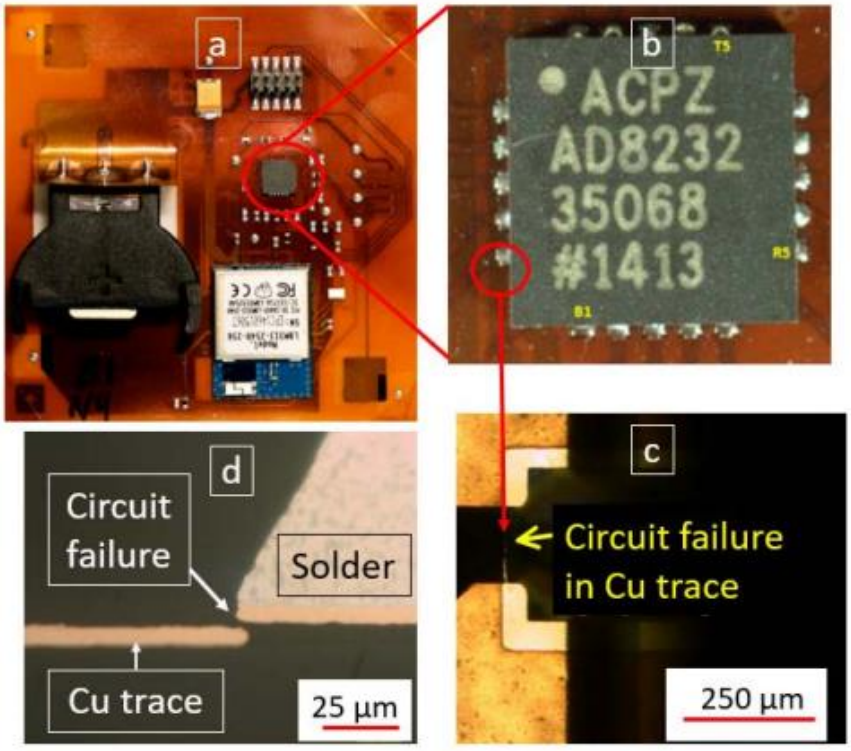


Fig. 2.5: a) component side of a double-sided FHE assembly b) closeup view of the 20 pin Si-based rigid IC chip c) crack in Cu trace d) cross section showing failure in Cu trace [14].

2.3 Chapter Summary

In this work, the PCB parasitics are treated transmission line parameters. Several issues such as signal attenuation and transmission line self-damping stress the importance of finding the lossy parameters (R_{TL} and G_{TL}) of a transmission line in addition to the lossless parameters (L_{TL} and C_{TL}). In case of FHE systems, the variation of the conductor resistance R_{TL} throughout the lifecycle of a device further accentuates the importance of its extraction. Several research works demonstrated extraction the PCB parasitics using one port TDR measurement. These TDR based measurements only extracts the lossless parameters of the line but do not extract the lossy parameters. The extraction of the lossy parameters is achievable with two port measurements such Kelvin test, S-parameter analysis. However, in case of an FHE system, two port access to a transmission line, which is bonded to an IC pin at one of its ports, is challenging to achieve. The proposed measurement circumvents the challenge, as it requires only one port access to the transmission line to extract both the lossy and lossless parameters.

On the other hand, research works on tracking the parasitics from an FHE assembly mostly focus on tracking parasitic R of standalone printed traces. In the available literature, no research work on tracking the variation of parasitic L and C has been reported. Also, as the placement of rigid ICs on a flexible substrate is expected impact the parasitic variation, tracking these parasitics for printed traces bonded to rigid ICs is essential for appropriate assessment of parasitic variation on an FHE assembly. In this regard, the proposed extraction method provides a scope to explore the parasitic variation of printed conductors bonded to IC chips.

Chapter 3

Transmission Line Modelling

A transmission line is a structure for guiding electromagnetic waves in a contained manner. In the simplest form, a transmission line is comprised of two conductors, one for propagation and the other for return of the electrical charges. As the length of the conductors becomes long enough such that it turns out to be comparable to the shortest wavelength of interest, the wave nature of the transmission needs to be considered. In this thesis, the PCB parasitics are treated as parameters of transmission line. The first section in the chapter reviews the transmission line analysis with Lumped Element Model. The next section focuses on the transmission line approximations, which are utilized in this work for extracting the line parameters and further validating the extracted parameters.

3.1 Review on Lumped Element Model Analysis

The nature of the electromagnetic wave is described by Maxwell's Equations [36]. To facilitate analysis, modelling and simulation the Lumped Element Model is derived from Maxwell's Equations. The Lumped Element Model links the distributed field theory and the circuit theory in describing the electromagnetic wave propagation through a transmission line. Fig. 3.1 depicts the Lumped Element Model for the propagation of electromagnetic waves through a small segment Δz of a 2-conductor transmission line.

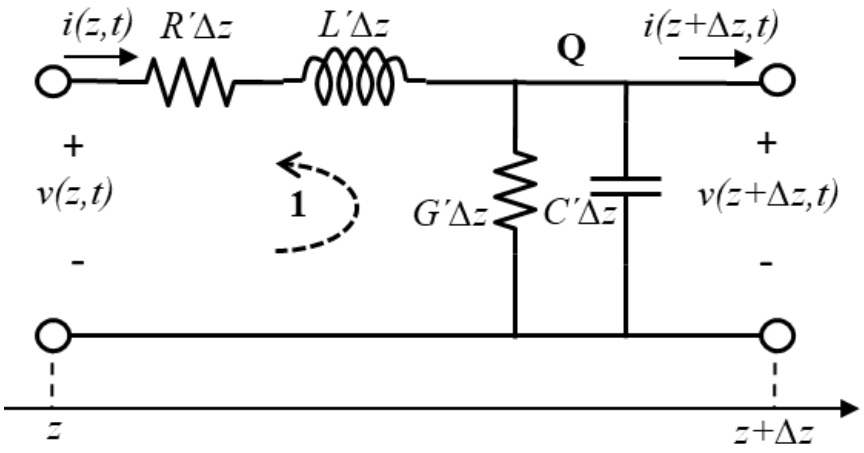


Fig. 3.1: Lumped Element Model of transmission line of length Δz.

In the Fig. 3.1, as the length of the transmission line segment, Δz→0, the Lumped Element Model approximates the distributed behavior of the transmission line. The descriptive parameters of the Lumped Element Model are discussed below:

- *R′* represent the combined resistance of the two constituent conductors per unit length of the transmission line. The series resistance accounts for the ohmic loss of energy resulting from the conductor current in the transmission line.
- *G′* represent the conductance of the dielectric medium separating the two conductors in a unit length of the transmission line. The shunt conductance accounts for the dielectric loss of energy resulting from the leakage current through the dielectric medium.
- *L′* represent the loop inductance per unit length of the transmission line. The series inductance accounts for the energy stored in the magnetic field around the transmission line.
- *C′* represent the capacitance between the two conductors per unit length of the transmission line. The shunt capacitance accounts for the energy stored in the electric field between the two conductors.

Next, we intend to describe other important transmission line parameters (such as characteristic impedance, propagation constant, time delay) in terms of the lumped parameters *R′*, *L′*, *G′* and *C′*.

First, by applying Kirchhoff's Voltage Law (KVL) in the loop 1 of Fig 3.1 and taking the limit as $\Delta z \to 0$, we obtain:

$$\frac{\partial v(z,t)}{\partial z} = -R' i(z,t) - L' \frac{\partial i(z,t)}{\partial t} \tag{3.1}$$

Similarly, by applying Kirchhoff's Current Law (KCL) in the node Q of Fig. 3.1 and taking the limit as $\Delta z \to 0$, we get:

$$\frac{\partial i(z,t)}{\partial z} = -G' v(z,t) - C' \frac{\partial v(z,t)}{\partial t} \tag{3.2}$$

The Eqns. (3.1) and (3.2) are known as Telegrapher's Equations. By setting $v(z,t) = Re[V(z)e^{j\omega t}]$ and $I(z,t) = Re[I(z)e^{j\omega t}]$, we obtain the time harmonic line equations as:

$$\frac{dV(z)}{dz} = -(R' + j\omega L')I(z) \tag{3.3}$$

and

$$\frac{dI(z)}{dz} = -(G' + j\omega C')V(z) \tag{3.4}$$

Combining the Eqns. (3.3) and (3.4), the line voltage and current can be expressed in terms of position *z* by the following differential equations:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{3.5}$$

and

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{3.6}$$

where γ is the propagation constant, given by

$$\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} = \alpha + i\beta \tag{3.7}$$

In the Eqn. (3.7), α is the attenuation constant describing the attenuation per unit length of transmission line and β is the phase constant describing phase change per unit length of the transmission line.

The solutions to the differential Eqns. of (3.5) and (3.6) are known as:

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{3.8}$$

and

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z} \tag{3.9}$$

V_0^+, V_0^-, I_0^+ and I_0^- are constants and their values are determined by the boundary conditions imposed on the transmission line. Substituting Eqn. (3.8) into (3.3) yields:

$$I(\mathrm{z}) = \frac{\gamma}{R' + j\omega L'}\left[V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}\right] \tag{3.10}$$

Comparing the Eqn. (3.9) and (3.10), we note:

$$I_0^+ = \frac{\gamma}{R' + j\omega L'} V_0^+ ; I_0^- = \frac{\gamma}{R' + j\omega L'}(-V_0^-) \tag{3.11}$$

Now the characteristic impedance Z_0 is defined as the ratio of the voltage and current waves propagating in a single direction at a certain point in the transmission line. Hence, we can express Z_0 as:

$$Z_0 = \frac{V_0^+}{I_0^+} = \frac{-V_0^-}{I_0^-} = \frac{R' + j\omega L'}{\gamma} = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \tag{3.12}$$

At high frequency it is plausible to take the lossless approximation by considering R'=0 and G'=0 as R' and G' turn out to be negligible with respect to ωL and ωC respectively. Under the lossless approximation, the Z_0 becomes

$$Z_0 = \sqrt{\frac{L'}{C'}} \tag{3.13}$$

Now, we aim to find simplified expressions for α and β. For this, γ from the Eqn. (3.7) is expressed as:

$$\gamma = j\omega\sqrt{L'C'}\left(1 + \frac{R'}{j\omega L'}\right)^{\frac{1}{2}}\left(1 + \frac{G'}{j\omega C'}\right)^{\frac{1}{2}} \tag{3.14}$$

Expanding the last two terms of the Eqn. (3.10) with Taylor series approximation and simplifying under the low loss approximation ($0<R'<<\omega L'$ and $0<G'<<\omega C'$) yields:

$$\gamma = \frac{1}{2}\left(R'\sqrt{\frac{C'}{L'}} + G'\sqrt{\frac{L'}{C'}} \right) + j\omega\sqrt{L'C'} \tag{3.15}$$

From the Eqn. (3.11), we obtain:

$$\alpha = \frac{1}{2}\left(\frac{R'}{Z_0} + G'Z_0 \right);\ \beta = \omega\sqrt{L'C'} \tag{3.16}$$

Whereas, under the lossless approximation ($R'=0$ and $G'=0$), the γ becomes:

$$\gamma = j\omega\sqrt{L'C'} \tag{3.17}$$

with

$$\alpha = 0;\ \beta = \omega\sqrt{L'C'} \tag{3.18}$$

So, the phase constant β remains same in case of both low loss and loss less approximations. The phase velocity v_p (the velocity of a single frequency wave) is expressed as:

$$v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{L'C'}} \tag{3.19}$$

Also, the group velocity v_g (the envelope velocity of a multiple frequency wave) is expressed as:

$$v_g = \frac{\partial\omega}{\partial\beta} = \frac{1}{\sqrt{L'C'}} \tag{3.20}$$

Thus, for any signal propagating through a low loss or loss less transmission line, the propagation velocity v can be expressed as:

$$v = v_p = v_g = \frac{1}{\sqrt{L'C'}} \tag{3.21}$$

The propagation delay or delay per unit length T_D' of the transmission line can be expressed as:

$$T_D' = \frac{1}{v} = \sqrt{L'C'} \tag{3.22}$$

So, the end-to-end delay T_D of a uniform transmission line of length l becomes:

$$T_D = l\sqrt{L'C'} \tag{3.23}$$

Another important parameter of the transmission line relevant to this work is fundamental resonance. At the frequency f_r, the reflected wave cancels out the incident wave at the front end of the transmission line, i.e., the incident and the reflected waves have a phase difference of 180˚ or half of a cycle. This implies, f_r is the frequency where the end to end time delay of the transmission line for a one-way travel is quarter of a cycle. Thus, we can express f_r of a uniform transmission line as:

$$f_r = \frac{1}{4T_D} = \frac{1}{4l\sqrt{L'C'}} \tag{3.24}$$

Table 3.1 summarizes the important descriptive parameters of the transmission line and compares these parameters for low loss and lossless lines:

Table 3.1: Summary of the transmission line descriptive parameters.

Parameters:	**Low loss** **($0<R'<<\omega L'$, $0<G'<\omega C'$)**	**Lossless** **($R'=0$, $G'=0$)**
Characteristic Impedance (Z_0)	$\sqrt{\frac{R'+j\omega L'}{G'+j\omega C'}}$	$\sqrt{\frac{L'}{C'}}$
Attenuation Constant (α)	$\frac{1}{2}\left(\frac{R'}{Z_0}+G'Z_0\right)$	0
Phase Constant (β)	$\omega\sqrt{L'C'}$	$\omega\sqrt{L'C'}$
Propagation Velocity (v)	$\frac{1}{\sqrt{L'C'}}$	$\frac{1}{\sqrt{L'C'}}$
End-to-End Delay (T_D)	$l\sqrt{L'C'}$	$l\sqrt{L'C'}$
Fundamental Resonance (f_r)	$\frac{1}{4l\sqrt{L'C'}}$	$\frac{1}{4l\sqrt{L'C'}}$

3.2 Approximations Utilized in this Work

The uniform transmission line extending from the test port to the IC pins on a PCB can be represented by a lumped equivalent circuit model [36] with N number of T segments as depicted in Fig. 3.2. In the model, total series resistance R_{TL}, total series inductance L_{TL} and total shunt capacitance C_{TL} between the test port and the IC pin are distributed among the N segments. As N becomes larger, the lumped equivalent circuit model approximates the distributed behavior of the transmission line over larger bandwidth. In the figure, Z_s is the source impedance. In the model of Fig 3.2, the total shunt conductance G_{TL} is neglected (as G_{TL} is insignificant within the bandwidth considered within the scope of this work). If the length of the uniform transmission model of Fig. 3.2 is assumed to be l, we can say $R_{TL}=R'l$, $L_{TL}=L'l$ and $C_{TL}=C'l$; where, R', L' and C' are the parameters per unit length of the line as defined in the previous section.

When the load impedance Z_{load} becomes very small, the effect of C_{TL} can be neglected up to a certain bandwidth as long as the impedance due to C_{TL} is orders of magnitude larger than the sum of the impedance due to R_{TL}, L_{TL} and the load. Hence, for a small Z_{load}, the transmission line from the test port to the IC pins on a PCB can be approximated within a certain bandwidth with R_{TL} and L_{TL} only. We refer to this approximation as a series RL model as depicted in Fig. 3.3(a). Conversely, as Z_{load} becomes very large, the effect of R_{TL} and L_{TL} can be neglected within a certain bandwidth as long as the admittance due to C_{TL} is orders of magnitude larger compared to sum of admittance due to R_{TL}, L_{TL} and the load. Hence, for a very large Z_{load}, the transmission line from the test port to the IC pins can be approximated within a certain bandwidth with C_{TL} only, which we refer to this as the shunt C model depicted in Fig. 3.3(b).

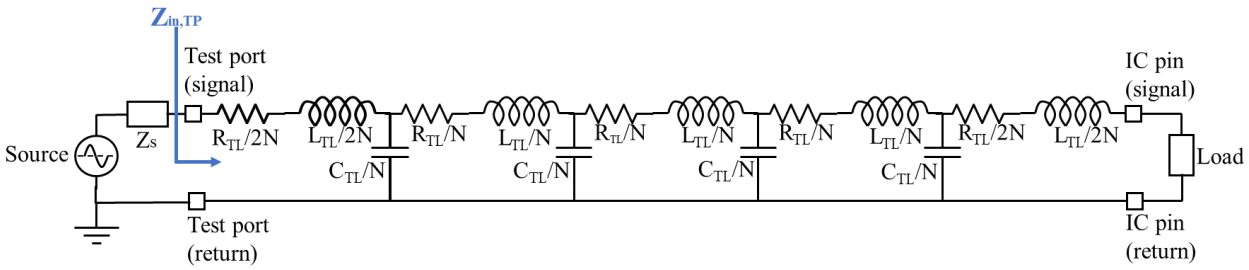


Fig. 3.2: Equivalent RLC model with N number of T segments for a uniform transmission line on PCB (shown for N=4).

The bandwidth, up to which series RL and shunt C models are accurate under appropriate Z_{load}, is dependent on L_{TL} and C_{TL} of the transmission line. To demonstrate this bandwidth dependency for the series RL model, the input impedance $Z_{in,TP}$ of the RLC transmission line model of Fig. 3.2 is simulated as a function of frequency using the Keysight Advance Design System (ADS) platform for varying the orders of L_{TL} and C_{TL}. The characteristic impedance is held constant at 50 Ω and parameters R_{TL}=1 Ω, Z_{load}=1 Ω and N=100. From the simulation, R_{TL} is extracted as the real part of $Z_{in,TP}$ minus Z_{load}. Also, L_{TL} is extracted as the slope of the imaginary part of $Z_{in,TP}$ with respect to frequency. The extracted R_{TL} and L_{TL} are normalized by the corresponding known values inserted in the RLC model and plotted against frequency as shown in Fig. 3.4. It is observed that the extracted R_{TL} and L_{TL} remains constant and equal to their known values well below the resonant frequency. In other words, the series RL model is valid for at least one order of magnitude below the fundamental resonance f_r, given by the following expression:

$$f_r = \frac{1}{4\sqrt{L_{TL}C_{TL}}} = \frac{1}{4T_D} \tag{3.25}$$

Here, T_D is the end-to-end time delay for the wave propagation in the transmission line. The parameter T_D can be expressed in terms of line length l, velocity factor v_f and velocity of light c as follows:

$$T_D = \frac{l}{v_f \cdot c} \tag{3.26}$$

Similarly, it can be shown for a large Z_{load}, description of a transmission line by its equivalent shunt C model, holds as a reasonable approximation well below (at least one order of magnitude) the fundamental resonance.

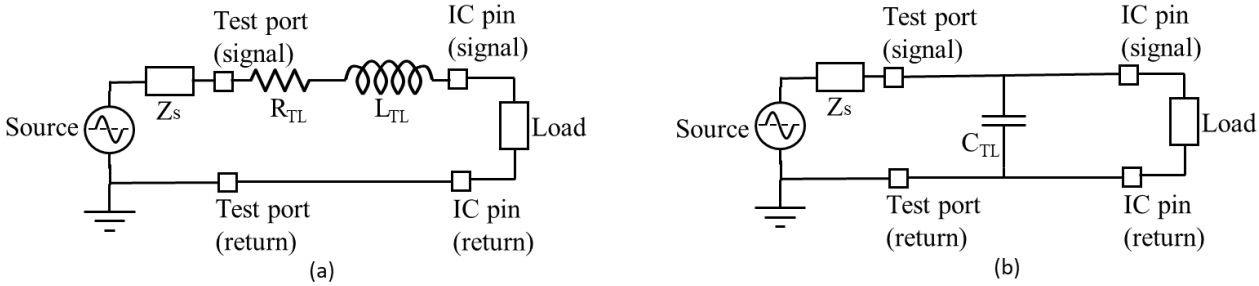


Fig. 3.3: Low frequency lumped equivalent models for transmission line: a) series RL model for small Z_{load} b) shunt C model for large Z_{load}.

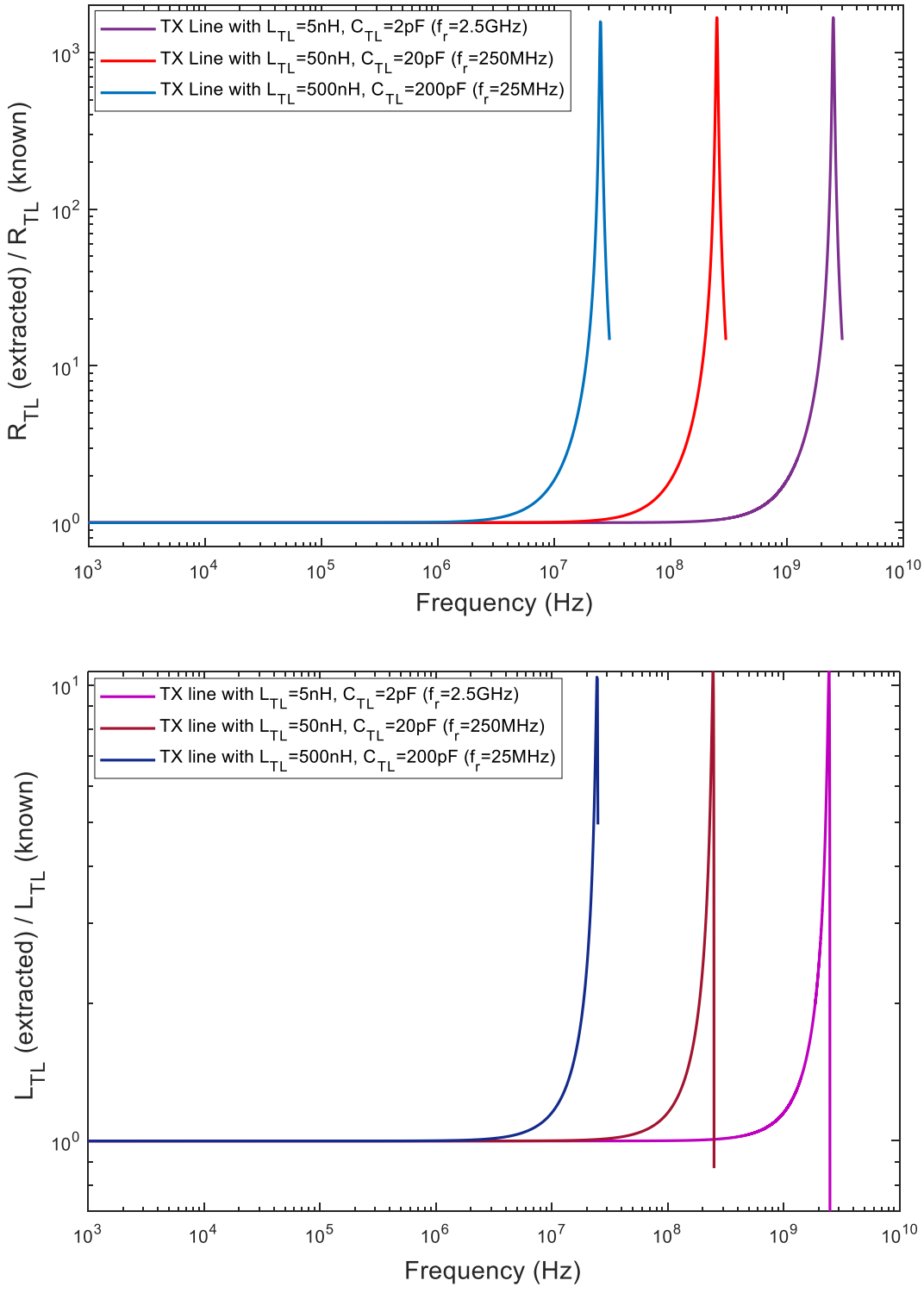


Fig. 3.4: Normalized plot of extracted R_{TL} and L_{TL} as function of frequency from a transmission line terminated with small load impedance of 1Ω.

Isolating the lumped equivalent parameters of a transmission line is practically challenging at high frequency, due to distributed behavior of the transmission line [36]. One way to describe a transmission line at high frequencies is by using the two-port lossless transmission line model depicted in Fig. 3.5. This model makes use of the characteristic impedance, Z_0 and end-to-end time delay parameter, T_D.

Considering the lossless approximation (R_{TL}=0 and G_{TL}=0) at high frequency, using the Eqns. (3.13) and (3.23) the total series inductance L_{TL} for a uniform transmission line can be described in terms of Z_0 and T_D as:

$$L_{TL} = Z_0 \cdot T_D \tag{3.27}$$

Similarly, under lossless approximation, total shunt capacitance C_{TL} for a uniform transmission can be expressed in terms of Z_0 and T_D as:

$$C_{TL} = Z_0 / T_D \tag{3.28}$$

This latter model provides a second method to extract the reactive elements of the transmission line. These will be used to compare the corresponding elements extracted by the series-RL and shunt-C models. In principle, they should be the same.

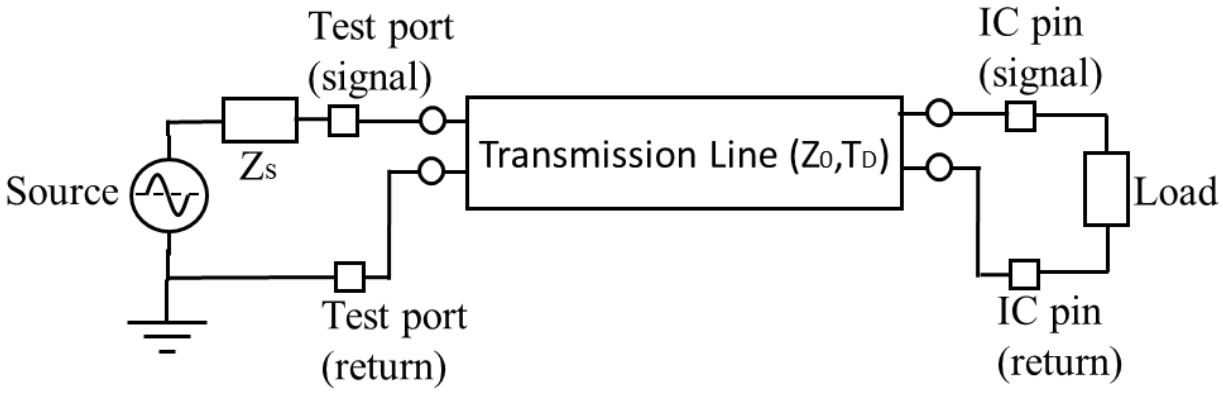


Fig. 3.5: Transmission line lossless model at high frequency.

3.3 Chapter Summary

First the Lumped Element Model of the transmission line is introduced. The derivations of the important descriptive parameters of the transmission line in terms of the lumped parameters are reviewed. Next, the Lumped Element Model is presented in a modified manner as the equivalent RLC model of the transmission line for utilization in the proposed extraction method. It is shown that the transmission line can be approximated by the series RL model and shunt C model up to a certain bandwidth for small and large load impedances, respectively. The bandwidth of the series RL and shunt C approximations is found to be well below (at least one order of magnitude) the fundamental resonance, which can be estimated with the length and velocity factor of the transmission line. The RLC parameters of the line are extractable within the appropriate bandwidth with these approximations and the proposed method will utilize them. Further, the high frequency lossless model of the transmission line is described. The lossless model provides another way of finding the LC parameters of the transmission line at high frequency through determination of the characteristic impedance and the end-to-end time delay. The extracted parameters from the lossless model will be utilized to validate the corresponding parameters extracted with the proposed method.

Chapter 4

Proposed Measurement Methodology

CMOS ICs include on-chip ESD protection circuitry in order to provide protection against large charge build up on high-impedance nodes [29]. The measurement method presented in this work utilizes the measured data from the on-chip ESD protection circuit before and after bonding the IC chip to a PCB transmission line in order to extract the RLC parasitics of the line. This chapter provides stepwise description of the proposed measurement method.

4.1 Modelling On-chip ESD Protection Circuit

The ESD protection circuit located between I/O and power supply pins (GND or VCC) can be modelled as diodes [29]. Fig. 4.1 illustrates the ESD diode model of an IC with two I/O pins, power and GND. As a point of reference, the ESD *i-v* behavior for an I/O pin between GND and VCC corresponding to the 8-bit microcontroller ATTINY85 made by Microchip Technology are shown in Fig. 4.2. The shape of the *i-v* curves substantiates the depicted diode model. These curves are different for different pin combinations, as the ESD structures are different for different pin types, i,e., I/O and power supply.

The small-signal equivalent circuit for an ESD diode is depicted in Fig. 4.3(a). In the figure, r_D represents diode incremental resistance given by

$$r_D = \frac{\eta V_T}{I} \tag{4.1}$$

where, η is diode ideality factor, V_T is thermal voltage and I is diode forward current [37].

Also, in Fig. 4.3(a) C_D represents the diode capacitance given by

$$C_D = \frac{\tau_T I}{\eta V_T} + C_j \tag{4.2}$$

where τ_T is diode transit time. C_j is junction capacitance, which can be considered as negligible in a forward biased diode [37].

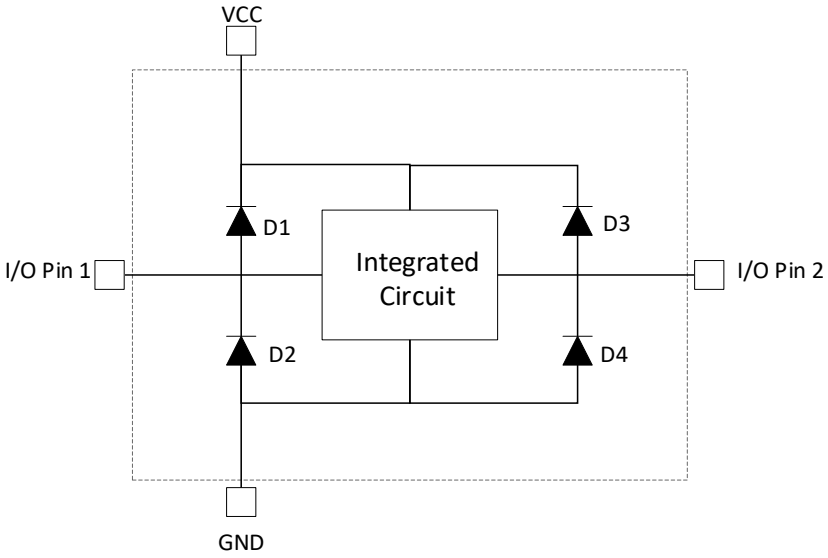


Fig. 4.1: Diode model for ESD protection circuit [29].

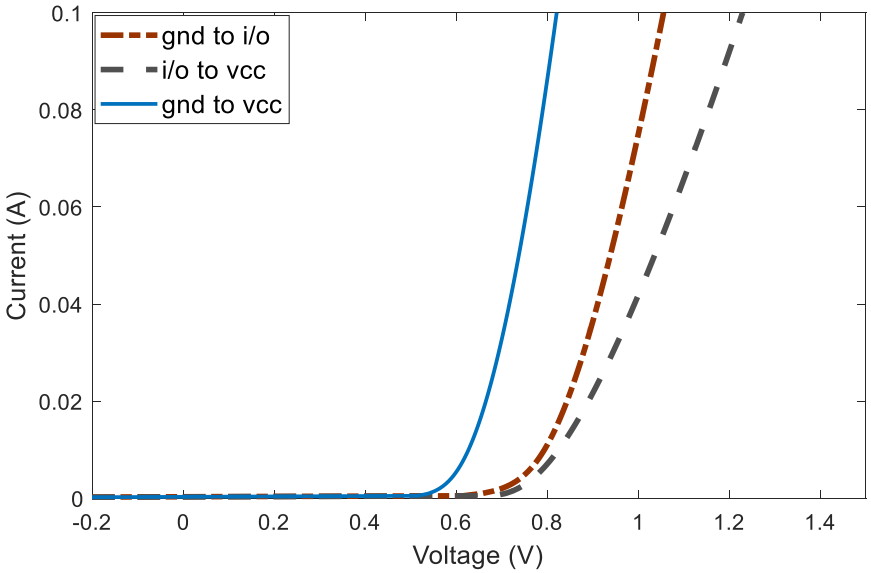


Fig. 4.2: I vs V plot (a) from GND (+) pin to I/O pin (-) (b) I/O pin (+) to VCC pin (-) (c) GND pin (+) to VCC pin (-) measured from Attiny85 chip.

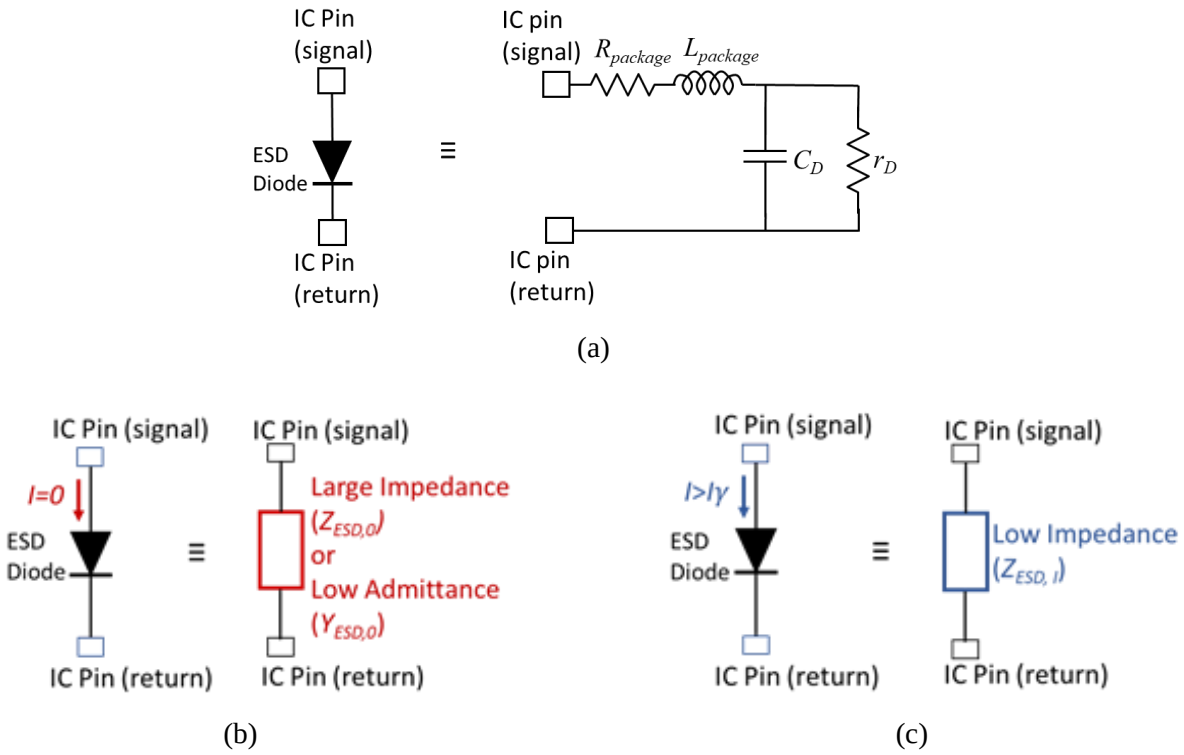


Fig. 4.3: Small signal representation of an ESD: (a) equivalent circuit (b) reverse Biased model c) forward biased model.

When the ESD diode is reverse biased (i.e., I=0), the diode presents a large impedance, or equivalently, a small admittance as shown in Fig. 4.3(b). Conversely, when the ESD diode is forward biased at $I > I_\gamma$, the diode presents a small impedance as shown in Fig. 4.3(c). In this work, I_γ is defined as the diode current where r_D is equal to 1 Ω.

The measurement technique presented in this paper requires prior knowledge of the impedance of the ESD diode (denoted here as $Z_{ESD,I}$) at a chosen frequency ω under a chosen forward bias current $I>I_\gamma$. Also prior knowledge of the admittance of the ESD diode ($Y_{ESD,0}$) at the same frequency under I=0 is required. In the case of the Attiny85 IC made by Microchip Technology, it was observed experimentally that the impedance and admittance of different ESD diodes across the same IC varied by more than 20%. In addition, the impedance and admittance of the same ESD diode varied very little (less than 1%) across 33 different samples of the same ICs. Hence, the ($Z_{ESD,I}$) and ($Y_{ESD,0}$) of a particular ESD diode in different samples of a given IC chip are assumed to be same.

4.2 Extracting RLC Parameters of a Transmission Line Bonded to an IC Chip

In this subsection, we will utilize the prior knowledge of the impedance and admittance parameters of an ESD diode in a given IC chip to extract the RLC parameters of a pair of conductors acting as a transmission line bonded to the IC chip. Fig. 4.4 shows the measurement setup for extraction of the RLC parameters of a PCB transmission line bonded to an ESD diode in a commercial IC chip. The proposed method requires identifying the input impedance Z_{DUT} of the DUT (Device-under-Test) at a particular frequency under a specific DC bias condition of the ESD diode. The DC bias point of the ESD diode is established with a current source connected to the DUT through a switch. The rationale behind using a current instead of a voltage source is to force the ESD diode into desired DC bias point regardless of the unknown parasitic resistance in series with the source and ESD diode. The capacitor $C_{DC\ block}$ prevents any DC current from going into the impedance measuring instrument, while acting as a short circuit to the AC signals above a certain frequency.

From the discussions in the previous section, a transmission line terminated with small load impedance can be approximated with series RL model and for a large load impedance the transmission line can be approximated with shunt C model, up to a certain bandwidth, of course. In the proposed measurement, small and large load impedances for the PCB transmission line are achieved by forward or reverse biasing the ESD diode as illustrated by Fig. 4.5(a) and 4.5(b), respectively.

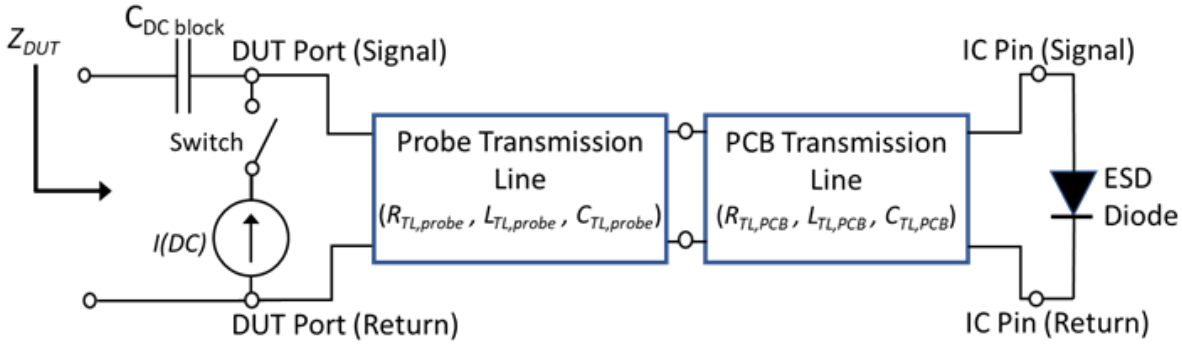
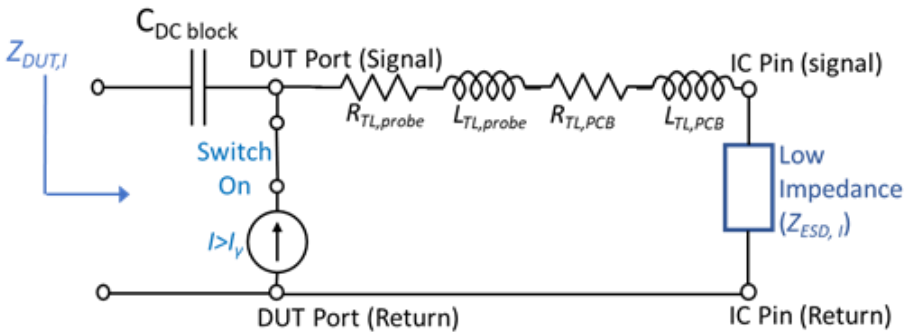
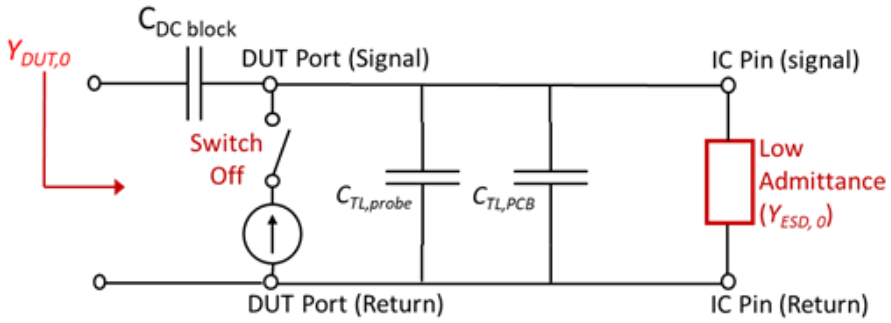


Fig. 4.4: Measurement setup for extracting the RLC parameters of a PCB transmission Line bonded to a commercial IC chip.



(a)



(b)

Fig. 4.5: The equivalent circuit of DUT for: (a) forward biased ESD diode (b) reverse biased ESD diode.

From Fig. 4.5(a), the resistance of the PCB transmission line, $R_{TL,PCB}$ can be found from:

$$R_{TL,PCB} = \text{Real}(Z_{DUT,I}) - \text{Real}(Z_{ESD,I}) - R_{TL,probe} \tag{4.3}$$

Also, from Fig. 4.5(a), the inductance of the PCB transmission line, $L_{TL,PCB}$ can be found as:

$$L_{TL,PCB} = \frac{1}{\omega}\left[\text{Imag}(Z_{DUT,I}) - \text{Imag}(Z_{ESD,I})\right] - L_{TL,probe} \tag{4.4}$$

Here, the real and imaginary parts of $Z_{DUT,I}$ is directly measured at a frequency ω under a chosen bias current I. The real and imaginary parts of the ESD protection circuit $Z_{ESD,I}$ is known by the separate measurement of the ESD diode at the same frequency ω and bias current level I. Also, the probe parasitics, $R_{TL,probe}$ and $L_{TL,probe,}$ are known from a separate measurement.

From Fig. 4.5(b), the capacitance of the PCB transmission line, $C_{TL,PCB}$ can be found from:

$$C_{TL,PCB} = \frac{1}{\omega}\left[\text{Imag}(Y_{DUT,0}) - \text{Imag}(Y_{ESD,0})\right] - C_{TL,probe} \tag{4.5}$$

Here the imaginary part of $Y_{DUT,0}=(1/Z_{DUT,0})$ is directly measured at frequency ω and the imaginary part of $Y_{ESD,0}$ is known by the separate measurement of the ESD diode at the same frequency ω. The probe capacitance $C_{TL,probe}$ is known from a separate measurement.

Thus, the direct input impedance measurement of a transmission line bonded to a commercial IC chip, augmented with the prior measurement of the on-chip ESD diode impedance under same frequency and DC bias current, allows one to extract the RLC parameters of the transmission line using the presented method.

4.3 Isolating the Parasitic Resistance of a Single IC Pin

This subsection delineates the decomposition of extracted $R_{TL,PCB}$ from the PCB transmission line into the constituent resistances of two printed conductors forming the transmission line. The parasitic resistance of an individual printed conductor bonded to a single IC pin can be isolated following the presented method within the same bandwidth constraint applicable for the extraction of $R_{TL,PCB}$.

The circuit representation of an IC device with two I/O and power supply pins assembled on a substrate is illustrated in Fig. 4.6. In the figure, the parasitic resistance associated with each IC pin are shown. The I/O pin under test is referred as PUT (pin-under-test). The total series resistance $R_{TL1,PCB}$ extracted from the transmission line 1 (between GND and PUT test pads) in the figure can be expressed as

$$R_{TL1,PCB} = R_{p,PUT} + R_{p,GND} \tag{4.6}$$

Likewise, the total series resistance $R_{TL2,PCB}$ extracted from the transmission line 2 (between PUT and VCC test pads) in the figure can be expressed as

$$R_{TL2,PCB} = R_{p,PUT} + R_{p,\text{VCC}} \tag{4.7}$$

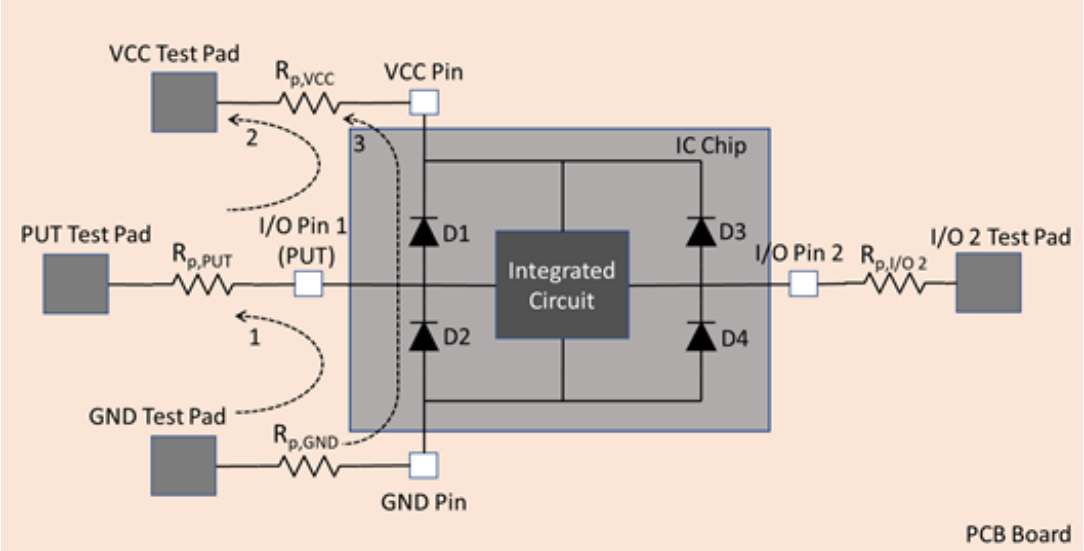


Fig. 4.6: Extraction of parasitic resistance of an individual printed conductor bonded to a single IC pin.

As there are three unknowns ($R_{p,PUT}$, $R_{p,GND}$ and $R_{p,VCC}$) listed in the above two equations, we need to identify a third equation. This is found by recognizing that the total series resistance $R_{TL3,PCB}$ extracted from transmission line 3 (between the GND and VCC pads) in the figure. $R_{TL3,PCB}$ can be expressed as

$$R_{TL3,PCB} = R_{p,GND} + R_{p,\mathrm{VCC}} \tag{4.8}$$

Therefore, to isolate $R_{p,PUT}$ from the power supply parasitic resistances $R_{p,GND}$ and $R_{p,VCC}$, one needs to extract the $R_{TL1,PCB}$, $R_{TL2,PCB}$ and $R_{TL3,PCB}$ from the transmission lines 1, 2 and 3, respectively. The extracted transmission line resistances can be expressed in matrix form as follows:

$$\begin{bmatrix} R_{TL1,PCB} \\ R_{TL2,PCB} \\ R_{TL3,PCB} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} R_{p,PUT} \\ R_{p,GND} \\ R_{p,VCC} \end{bmatrix}$$

or, more compactly as:

$$\mathbf{R}_{\mathbf{TL,PCB}} = \mathbf{C} \cdot \mathbf{R}_{\mathbf{p}} \tag{4.9}$$

From the measured transmission line resistance vector $\mathbf{R_{TL,PCB}}$, the unknown parasitic resistance associated with the given pins, designated by vector $\mathbf{R_P}$, can be found by inverting the matrix equation as follows:

$$\mathbf{R_P} = \mathbf{C^{-1}} \cdot \mathbf{R_{TL,PCB}} \tag{4.10}$$

Thus, the parasitic resistance associated with any IC pin can be isolated with the presented measurement method.

4.4 Verification of the Proposed Measurement Method

For simulating the proposed method to extract the RLC parameters from a transmission line bonded to an IC chip, the measurement setup of Fig. 4.4 is implemented in Keysight's Advanced Design System (ADS) platform. In the ADS implementation, the probe and PCB transmission lines are realized by separate equivalent RLC models as shown Fig. 3.2. The number of segments, *N* for both the models are chosen to be 100. The ESD diodes are realized with 1N914 model for silicon diode (as the exact simulation model for an ESD diode is unavailable). The chosen parameter values for the ADS implementation are listed in the Table 4.1. The LC parameters of the probe and the PCB are chosen such that the characteristic impedance of the probe and the PCB transmission lines are equal. The range of the chosen RLC parameters for the probe and PCB are comparable to practical cases.

Table 4.1: Chosen parameter values for implementation for simulating the measurement setup of Fig. 4.4.

Parameters	**Values**
$R_{TL,PCB}$	0.3 Ω
$L_{TL,PCB}$	50 nH
$C_{TL,PCB}$	20 pF
$R_{TL,probe}$	0.7 Ω
$L_{TL,probe}$	200 nH
$C_{TL,probe}$	80pF
I_{DC}	10 mA

The impedance and admittance of the DUT (Device-under-Test: comprised of probe, PCB and connected diode) are simulated from 10 kHz to 10 MHz under the forward and reverse biased conditions of the diode, respectively. From the simulated results, the $R_{TL,PCB}$, $L_{TL,PCB}$ and $C_{TL,PCB}$ are extracted following the proposed method. The extracted values of $R_{TL,PCB}$, $L_{TL,PCB}$ and $C_{TL,PCB}$ are shown in Fig. 4.7, 4.8 and 4.9, respectively.

In the Fig. 4.7, 4.8 and 4.9, the extracted values of $R_{TL,PCB}$, $L_{TL,PCB}$ and $C_{TL,PCB}$ agree with their known values up to a certain bandwidth. This bandwidth of the extraction depends on the bandwidth of the series RL and shunt C approximations. As discussed in the previous chapter, the series RL and shunt C approximations are valid well below the fundamental resonance f_r of a transmission line. As the probe and the PCB transmission lines are chosen to have the same characteristic impedance, we can assume they act as a single uniform transmission line. Hence, f_r of the entire uniform line can be found with the following expression (modified from Eqn. (3.25)):

$$f_r = \frac{1}{4(T_{D,probe} + T_{D,PCB})} = \frac{1}{4(\sqrt{L_{TL,probe}C_{TL,probe}} + \sqrt{L_{TL,PCB}C_{TL,PCB}})} \tag{4.11}$$

Where, $T_{D,probe}$ and $T_{D,PCB}$ are end-to-end delays for the probe and the PCB, respectively. The f_r found with Eqn. (4.11) is 50 MHz. From the simulated plots, the bandwidth for the accurate extraction of $R_{TL,PCB}$, $L_{TL,PCB}$ and $C_{TL,PCB}$ is well below (one order of magnitude) the f_r =50 MHz.

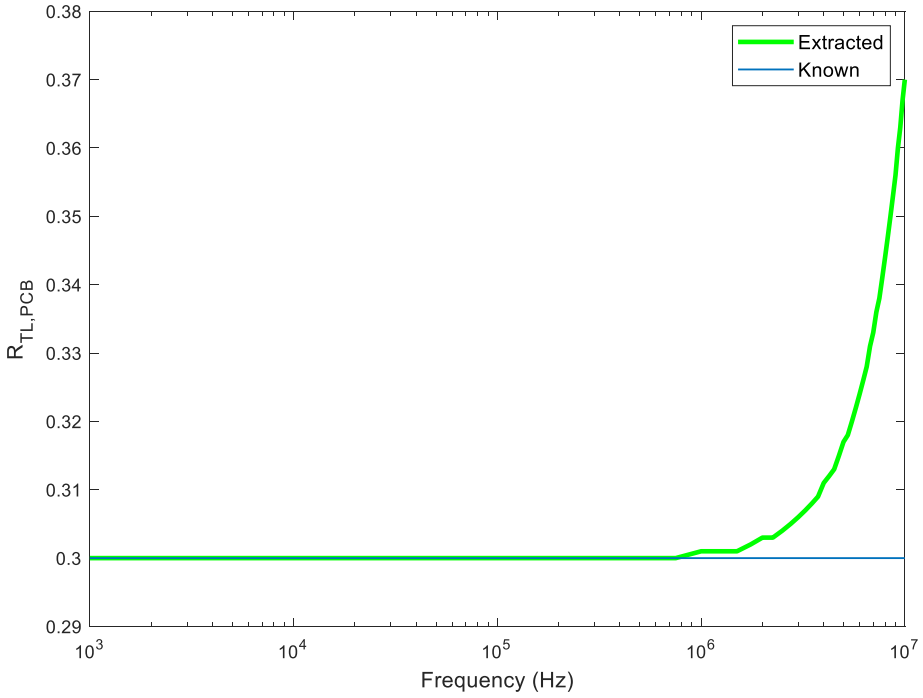


Fig. 4.7: Extracted $R_{TL,PCB}$ from simulation using the proposed method compared to its known value.

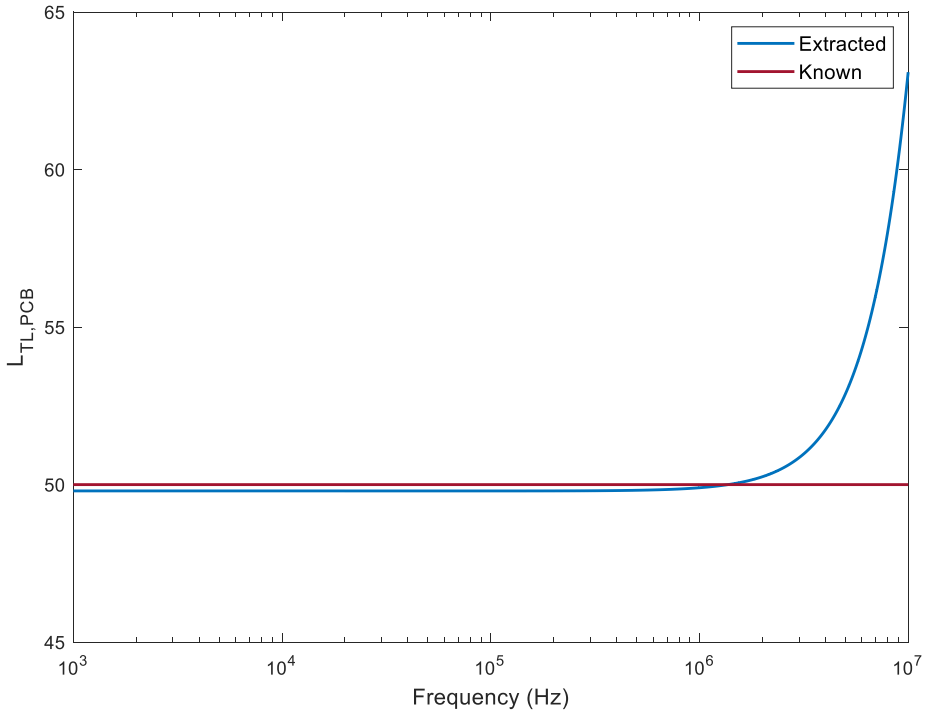


Fig. 4.8: Extracted $L_{TL,PCB}$ from simulation using the proposed method compared to its known value.

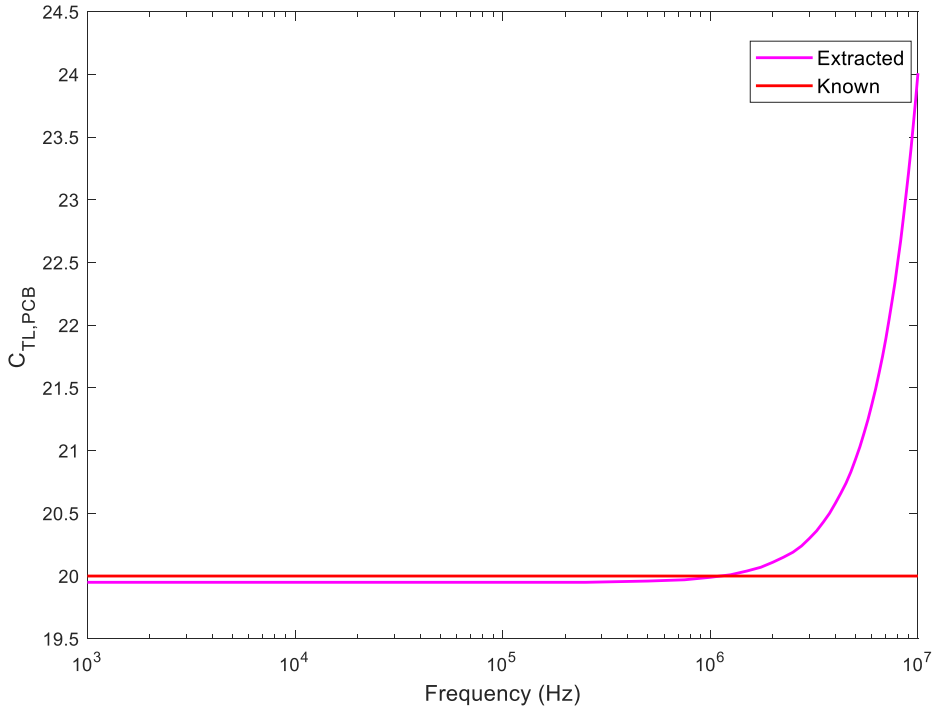


Fig. 4.9: Extracted $C_{TL,PCB}$ from simulation using the proposed method compared to its known value.

To verify the isolation of individual R of printed conductors bonded to a single IC pin, the circuit of Fig. 4.6 is simulated using SPICE. For the scope of this particular verification, the LC parameters associated with the printed conductors and the probe are neglected, as their impact in the bandwidth of the extracted R has already been discussed. It is assumed the extractions required for isolating R of a single IC pin are to be performed within the appropriate bandwidth. Here, the ESD diode is described with 1N914 SPICE model for silicon diode and the resistances associated to the IC pins are assigned different chosen values. An AC simulation is performed at 100 kHz. Applying the presented extraction method, the total R in series with each diode is extracted when the diode under test is forward biased at a 10 mA current level. Then, the extracted value is decomposed into R of individual printed conductors using the proposed technique of Section 4.3. Table 4.2 shows the chosen and the extracted values of the individual R for simulating circuit of Fig. 4.6. The table shows the values found in the simulation are same as their known values. Hence, the proposed method for isolating R of individual printed conductors bonded to a single IC pin is verified with simulation.

Table 4.2: The chosen (known) and the simulated values of the resistances in the circuit of Fig. 4.6.

Resistances	**Chosen (known) Values (Ω)**	**Extracted Values (Ω)**
$R_{p,GND}$	2	2
$R_{p,PUT}$	1	1
$R_{p,VCC}$	0.67	0.67
$R_{p,I/O2}$	.5	.5

4.5 Chapter Summary

In the proposed measurement method, the RLC parasitics associated with a transmission line bonded to an IC chip are extracted utilizing the on-chip ESD protection circuits. The on-chip ESD protection circuits can be modelled as diodes. First, for a given IC chip, the impedance and admittance of the ESD diodes under certain forward bias and reverse bias conditions need to be determined. Then, for having the IC chip bonded to printed conductors acting as a transmission line, the impedance and admittance parameters of the transmission line (loaded with a pre-measured on-chip ESD diode) are determined under the same biasing conditions as the

pre-measurement. From the determined impedance and admittance parameters of the ESD diode and the transmission line loaded the ESD diode, the RLC parameters of the line are extracted. Further, the extracted resistance of a transmission line can be decomposed into the resistances of the constituent printed conductors. This isolation of the resistance for a printed conductor connected to an arbitrary input/output pin is achieved using the extracted resistances from 3 transmission lines measurements involving the pin-under-test, Gnd pin and VCC pin. Finally, for verifying the proposed extraction method, ADS and SPICE simulations are performed with equivalent models for transmission line and diode. The simulation results show the extracted parameters with the proposed method agree with their corresponding known values well below the fundamental resonance of the measurand transmission line.

Chapter 5

In-Circuit-Test with the Proposed Method

This chapter introduces In-Circuit-Test with general challenges and measures in its application. Next, the practical challenges that may arise for applying the proposed measurement method to an In-Circuit-Test and the corresponding measures to circumvent these challenges are explored.

5.1 In-Circuit-Test: General Challenges and Measures

In-Circuit-Test (ICT) is run on a PCB after the components are assembled on the board. The objective is to identify defects as well as to address reliability, signal integrity and functionality of the assembled PCB. ICT is generally carried out using two different forms of test fixtures. One is Bed-of-Nail test fixture, where spring loaded pogo pins at customized locations on a rigid structure are pressed onto to test points in the board as shown in Fig. 5.1(a). Another is the Flying-Probe test fixture, where electromechanically controlled probes are programmed to access the test points on the board as shown in Fig. 5.1(b). Bed-of-Nail test fixture is relatively low cost and faster, but the fixture is customized for a particular PCB design. In contrast, the Flying-Probe test technique has a relatively higher cost and is slower, but it is adaptable to different PCB designs [40].

The general challenge in ICT is associated with access and isolation. Firstly, ICT requires additional test points at particular locations to be included in the design for allowing probe connection with the circuit. Secondly, when there are multiple parallel paths between two arbitrary test points, isolating an anomaly in an individual circuit path is challenging. Fig. 5.2 depicts the challenge in a simplified form, where we aim to measure the impedance of a particular element, Z_x between test point T1 and T2 in the circuit. In the figure, Z_a and Z_b are unknown impedances in

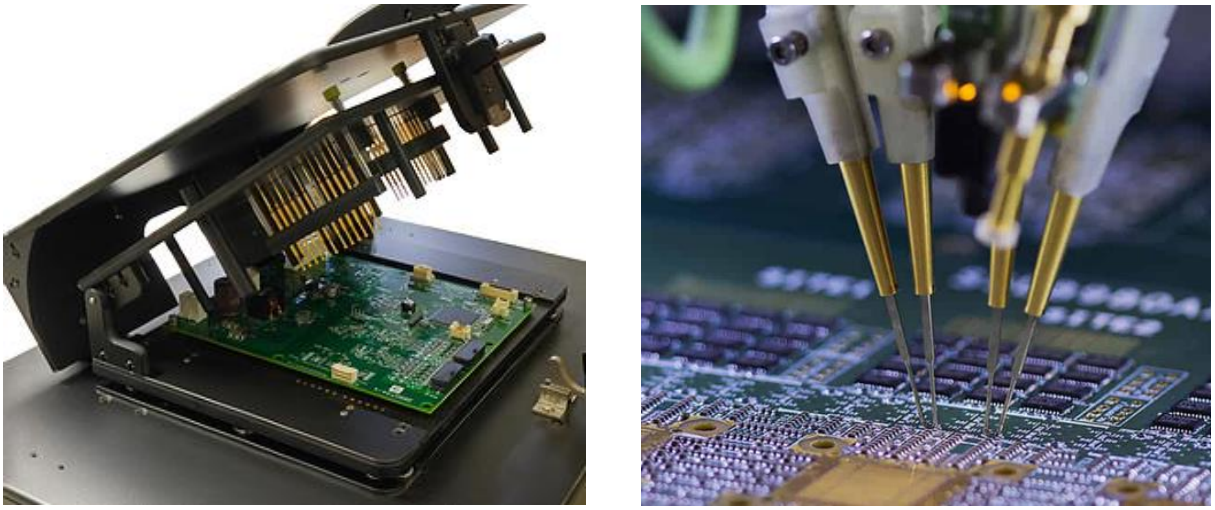


Fig. 5.1: In-Circuit-Testing with a) Bed-of-Nail fixture [38] and b) Flying-Probe fixture [39].

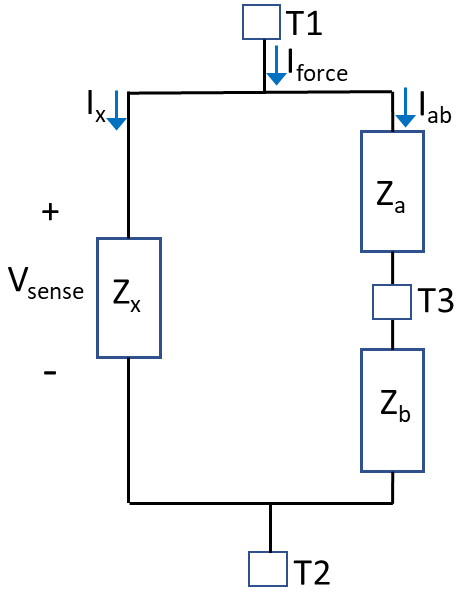


Fig. 5.2: Challenge in measuring impedance of an individual circuit element with In-Circuit-Test.

the path parallel to Z_x, and T3 is a test point in between them. V_{sense} is the voltage between the test points and I_{force} is the current forced through the test points. As the individual impedances of the parallel paths are unknown, I_x and I_{ab} are unknown as well. Hence, $Z_x=V_{sense}/I_x$ cannot be determined, and an anomaly associated with it is challenging to isolate.

One way to test the impedance of a circuit element in parallel with other circuit elements on a PCB is temporary isolation of the circuit element under test from the rest of the circuitry. The temporary isolation is achievable by incorporating jumper pads into the PCB design [41]. Jumper pad connections and isolations can be implemented by placement and removal of solder paste

between the pads. However, this soldering/desoldering process for jumper pads can pose inconvenience in testing large circuits. To facilitate jumper pad isolation for testing large circuits a programmable test setup providing synchronized connection and isolation through solid state relays has been developed [42]. Fig. 5.3 depicts the jumper pad isolation in order to measure the impedance Z_x from the circuit of Fig. 5.2.

Another way to isolate measurement of a circuit element in parallel with other circuit elements on a PCB is restraining the measurement current through the parallel circuit elements by analog guarding [43,44]. Fig. 5.4 depicts the analog guarding scheme in order to measure the impedance Z_x from the circuit introduced before. In the figure, T2 is considered to be the common reference Gnd of the circuit. Here, the virtual short between the two input terminals of the op-amp restrains current through Z_a. The current through Z_b is supplied by the op-amp. Consequently, the current I_{force} flows through Z_x only, allowing its isolated measurement. However, non-idealities of an op-amp such as finite gain, bandwidth, parasitics will impose constraint on the ranges of impedances that can be measured and guarded [44].

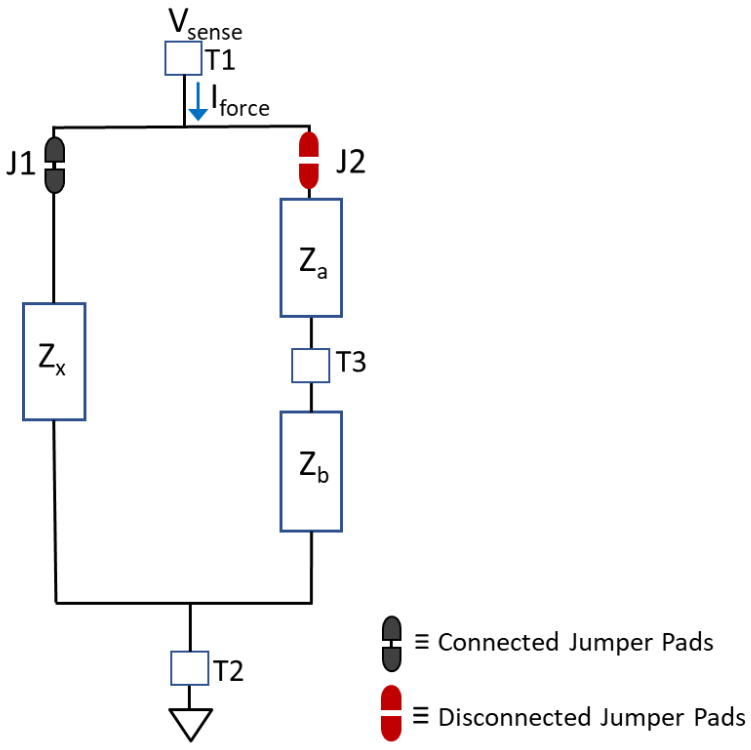


Fig. 5.3: Zumper pad isolation to measure imedance of an individual circuit element with In-Circuit-Test.

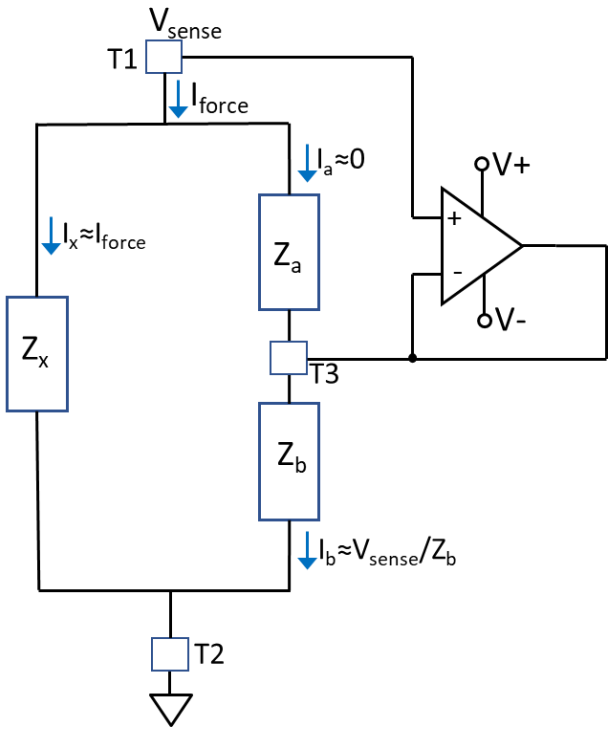
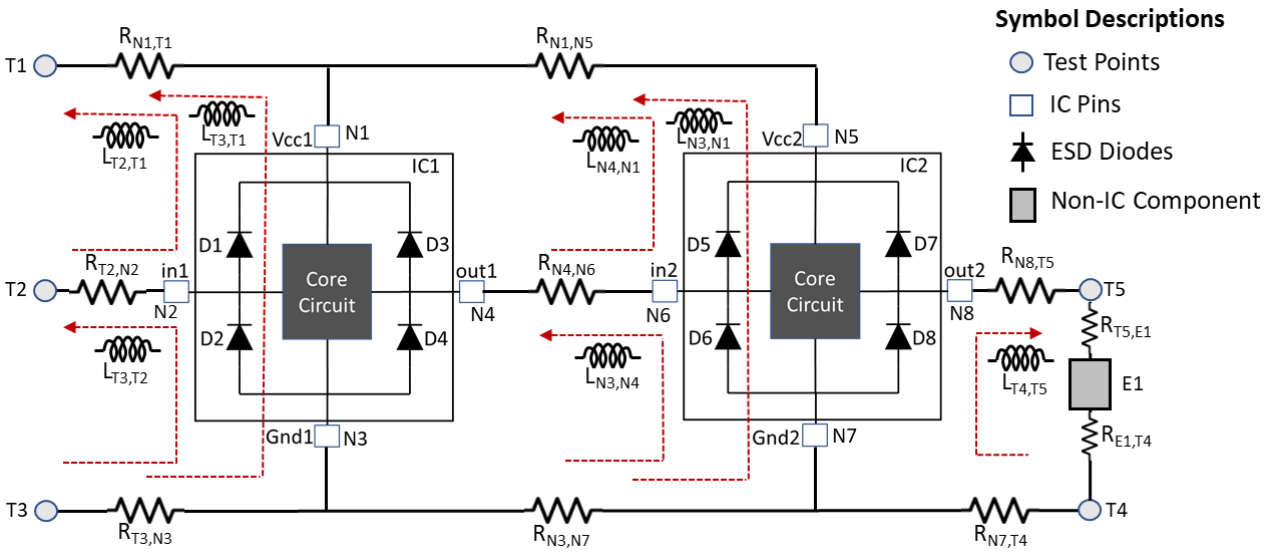


Fig. 5.4: Analog guarding to measure impedance of an individual circuit element with In-Circuit-Test.

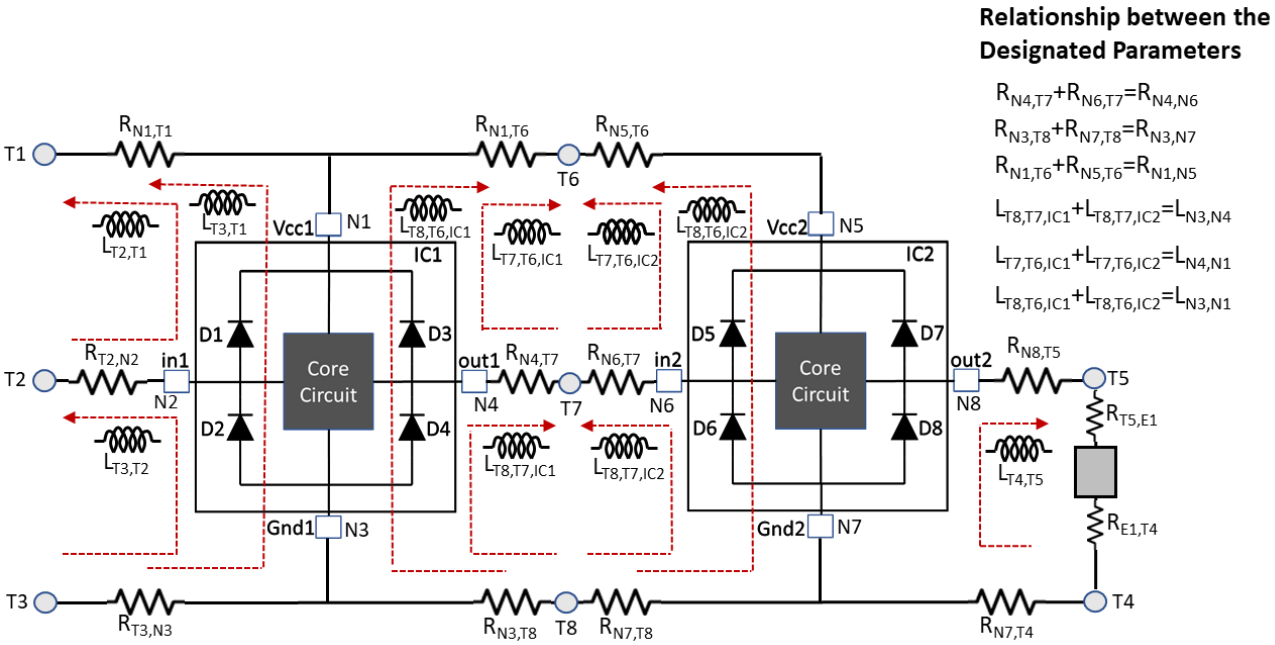
5.2 Application of the Proposed Measurement to In-Circuit-Test

The proposed method allows the post assembly extraction of the RLC parasitics of a transmission line, which is bonded to only a single IC chip at its one terminal. However, it is possible to have a transmission line with its two terminals bonded to two IC chips in an FHE circuit. In such cases, the in-circuit access to the transmission line under test and isolation of its series RL parameters is challenging to achieve.

The Fig. 5.5 depicts an FHE assembly with multiple IC chips in a simplified form. In the figure, the series RL parameters associated with the printed conductors are shown as well. In the Fig 5.5(a), the input, output, and power supply of the PCB are the only access points in the design. Alongside the figure, the descriptions of the employed symbols are provided. Firstly, the extraction of the parasitics from the internal loops such as the extraction of $R_{N4,N6}$, $L_{N3,N4}$ will require additional test points. Fig 5.5(b) shows the modification of the design with additional test points. Alongside the figure, the relationship between the designated parameters of Fig. 5.5(b) with those of Fig. 5.5(a) are listed.



(a)



(b)

Fig. 5.5: Simplified schematic of an FHE multi-IC environment with associated series RL parasitics: a) without any additional test point (other than input, output and power supply access) b) with additional test points.

Now, in the Fig. 5.5(b), let us consider the extraction of the series RL parasitics between the test points T7 and T8, by applying the proposed method. Here, the total current I_{force} (combining both the DC bias and the small signal AC) injected through test points by the measurement setup will divide among the two parallel paths as shown in Fig. 5.6. Considering the series parasitics in both the paths as unknown, the divided currents, I_{D4} and I_{D6} will be unknown as well. With the unknown values of current through the individual paths, isolation of their individual impedances is not possible. Hence in such a case, the extraction of the series RL parasitics in the individual paths is not directly achievable with the proposed method. This issue of measurement current leakage through a parallel path is also present for implementing the measurement between the test points T7 and T6, T3 and T1, T8 and T6 as well as T4 and T5 in Fig. 5.5(b).

The transmission lines connected to the IC chips also posses shunt parasitic C (not shown in the Fig. 5.5). The extraction of the shunt parasitic C of a transmission line connected to two ESD diodes at the terminals is straight forward using the presented method. Since for this extraction, the on-chip ESD diodes are reverse biased with zero DC current, the issue of measurement current division through the parallel ESD diodes is not present. For the isolation of the shunt parasitic C from a transmission line bonded to two ESD diodes at the terminals, the parallel C from the two ESD diodes need to be accounted and compensated in the measurement.

The aforementioned challenge for in-circuit extraction of the series RL parasitics using the proposed method can be circumvented by providing jumper pad isolation. Fig. 5.7 shows the jumper pad isolation for extracting the series RL parasitics connected to IC2. Likewise, the series parasitics connected to IC1 can be extracted by connecting the jumper pads J1 and J2 and disconnecting the rest.

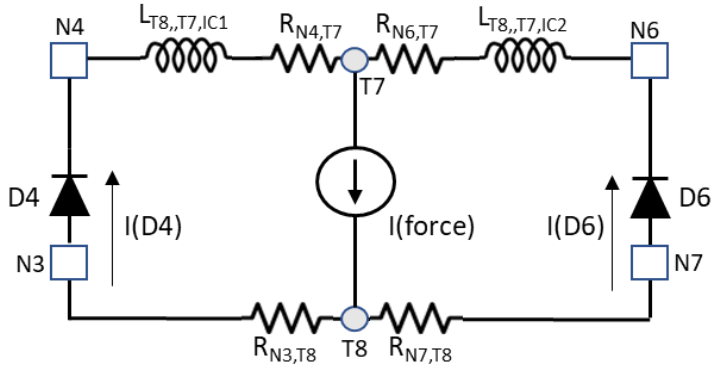


Fig. 5.6: Division of measurement current in the parallel paths formed by two ESD diodes.

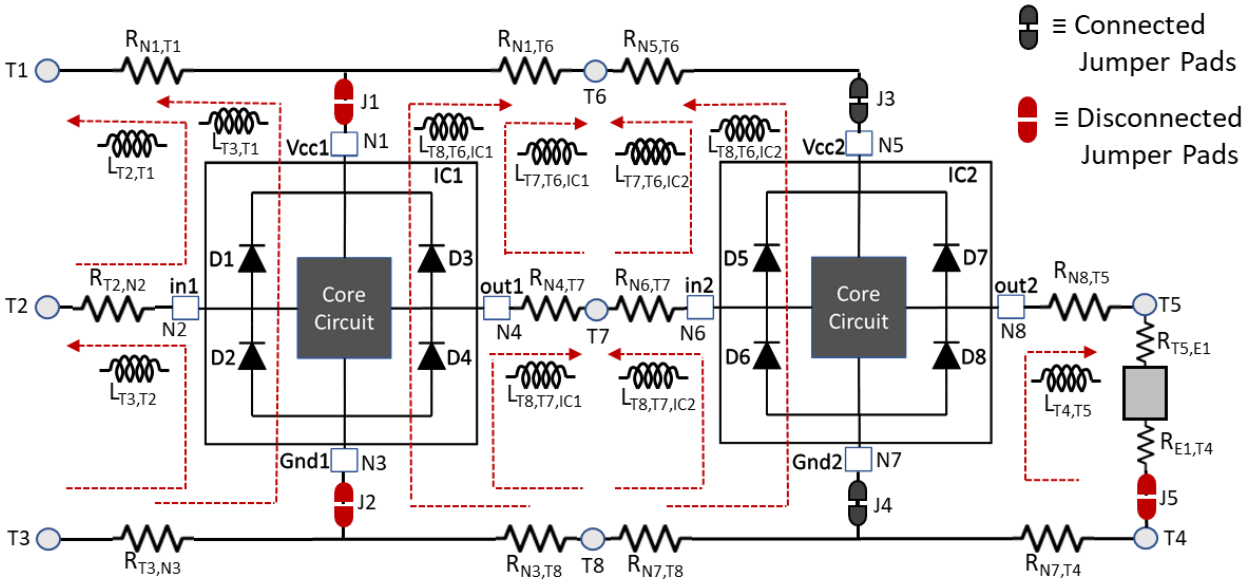
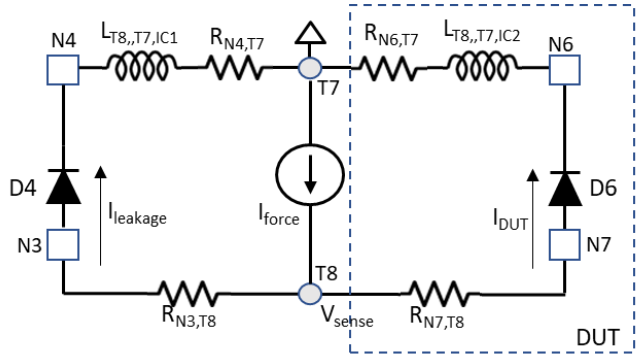
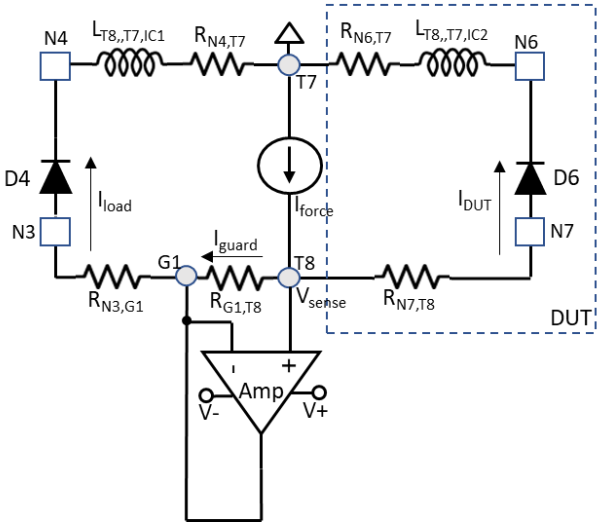


Fig. 5.7: Schematic of jumper pad isolation for extracting the series RL parasitics connected to IC2.

Another option for resolving the challenge can be analog guarding. Fig. 5.8(a) demonstrate the series parasitics connected to ESD diodes seen from the test points T7 and T8, where we aim to extract the parasitics connected to ESD diode D6. The measurand is designated by the block DUT (Device-under-Test). Fig. 5.8(b) shows a way to apply analog guarding for extracting series parasitics connected to D6 seen from the test points T7 and T8. A guard test point G1 is placed near the test point T8 on the path of ESD diode D4, though which we aim to block the measurement current. The guarding is provided by a non-inverting unity gain configuration of op-amp. Fig. 5.8(c) is a simplified circuit diagram of the Fig. 5.8(b). In the figure, the current I_{load} through the ESD diode D4 is supplied by the op-amp to make the voltage at G1 approximately equal to that of T8 such that, the current between G1 and T8, I_{guard} nullifies. For $I_{guard}\approx 0$, the total current forced by a measurement instrument, I_{force} will be flowing through the DUT only, that is $I_{DUT}\approx I_{force}$. Thus, the impedance of the DUT, $Z_{DUT}=V_{sense}/I_{force}$ can be found using the known values of I_{force} and V_{sense} and the series RL parameters of interest can be extracted using the known Z_{DUT}.



(a)



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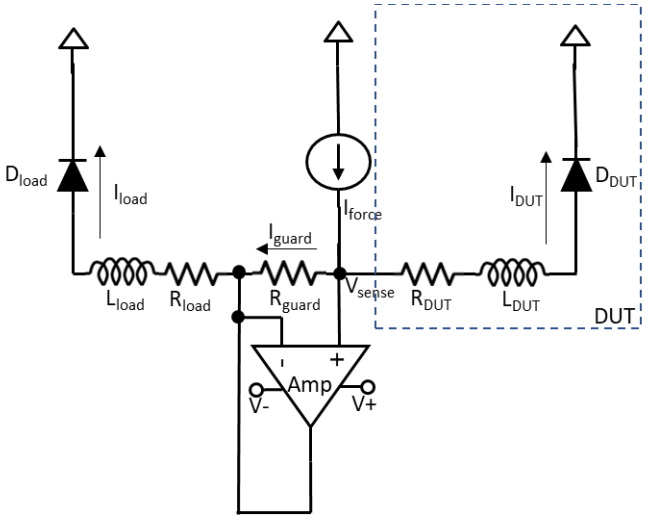


Here,
$R_{DUT}= R_{N7,T8}+R_{N6,T7}$
$L_{DUT}= L_{T8,T7,IC2}$
$R_{load}= R_{N4,T7}+R_{N3,G1}$
$L_{load}= L_{T8,T7}$
$R_{guard}= R_{G1,T8}$
D_{DUT}=D6
D_{load}=D4

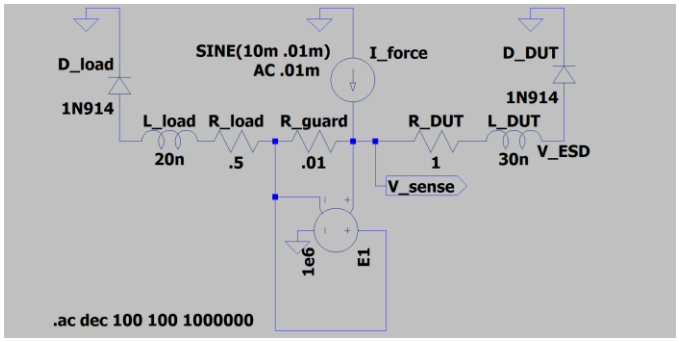
(c)

Fig. 5.8: Adaptation of analog guarding in the proposed extraction method: (a) DUT with its parallel circuit path (b) implementation of analog guarding in parallel circuit path (c) simplified schematic of the implemented analog guarding.

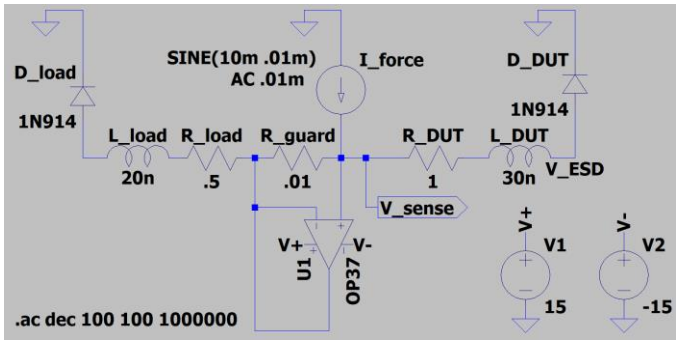
The circuit diagram of the Fig. 5.8(c) is implemented in SPICE for the parameter values listed in Table 5.1. For the scope of demonstrating analog guarding with the proposed method, the ESD diodes are realized with 1N914 SPICE model for silicon diode (as exact model of an ESD diode is unavailable). The op-amp is realized by an ideal model and a non-ideal model in two separate simulations. The ideal op-amp is realized by a Voltage Controlled Voltage Source (VCVS) having the gain of 10^6. As shown in the Fig. 5.9(a). The non-ideal op-amp is realized by OP37 SPICE model as shown in the Fig. 5.9(b). An AC simulation from 100 Hz to 1 MHz is performed for both the implementations.

Table 5.1: Chosen parameter values for SPICE implementation of Fig. 5.8(c).

Parameters	Values
R_{DUT}	1 Ω
R_{load}	0.5 Ω
R_{guard}	.01 Ω
L_{DUT}	30 nH
L_{load}	20 nH
I_{force}	10 mA(DC) +.01 mA(AC)



(a)



(b)

Fig. 5.9: SPICE Implementation of analog guarding: (a) using Voltage Controlled Voltage Source (VCVS) b) using OP37 op-amp model.

From the simulation R_{DUT} is found as follows:

$$R_{DUT} = \text{Real}\left[\frac{V_{sense} - V_{ESD}}{I_{force}}\right] \tag{5.1}$$

where, V_{sense} and I_{force} are the corresponding sensed voltage and forced current, V_{ESD} is the ESD diode voltage due to I_{force} at the intermediate node shown in Fig. 5.9. In the proposed method they are considered as the known parameters. Also, from the simulation the L_{DUT} is found as follows:

$$L_{DUT} = \text{Imag}\left[\frac{V_{sense} - V_{ESD}}{I_{force}}\right] \Big/ 2\pi f \tag{5.2}$$

where, f is the frequency of the AC current injected by I_{force}. Fig. 5.10 and 5.11 show the extracted values of R_{DUT} and L_{DUT} respectively with SPICE simulation from 100 Hz to 1 MHz.

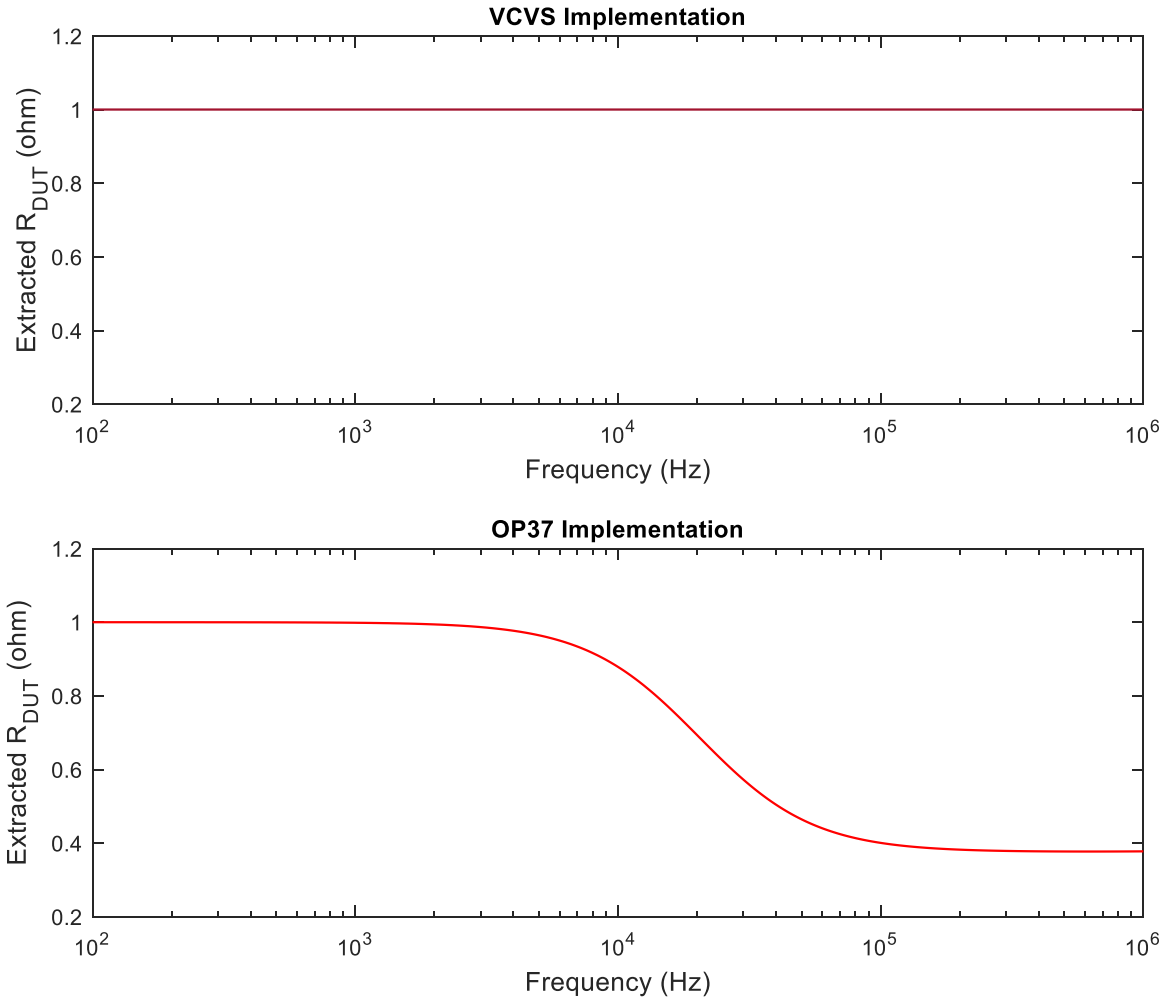


Fig. 5.10: Extracted values of R_{DUT} for implementation of analog guarding with proposed method in SPICE.

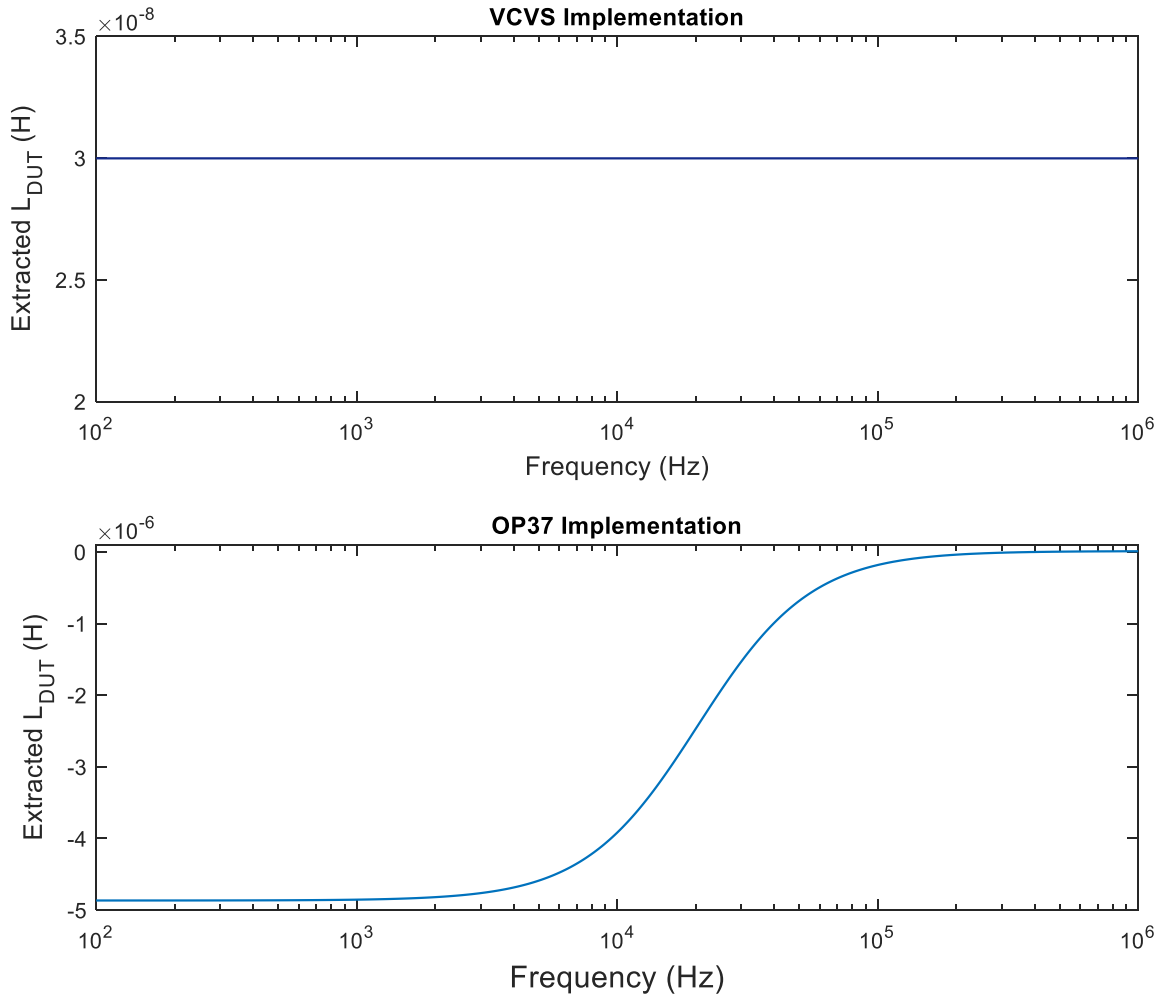


Fig. 5.11: Extracted values of L_{DUT} for implementation of analog guarding with proposed method in SPICE.

In the Fig. 5.10, R_{DUT} extracted with VCVS implementation agrees with the known value of 1 Ω at all frequencies over the simulated frequency range, while the extracted value of R_{DUT} with OP37 implementation agrees with the known value below a certain frequency (~5 kHz). As the frequency increases above the certain limit (~5KHz), the extracted R_{DUT} deviates away from its actual value. This is due to analog guarding becoming ineffective from significant drop in the gain of OP37 at higher frequencies. In the Fig. 5.11, L_{DUT} extracted with the VCVS implementation agrees with the known value of 30 nH at all frequencies within the simulated range. However, L_{DUT} extracted with OP37 implementation is negative at low frequencies where analog guarding is effective and it does not conform with its known value at any frequency over the simulated range. This can be attributed to nonideality of the amplifier such as op-amp parasitics.

Although, application of analog guarding with the proposed measurement poses challenge in the extraction of parasitic inductance, it can still have utility for low frequency extraction of parasitic resistance. When applying analog guarding for extraction of parasitic resistance with proposed method, several issues need to be considered. One is range of R_{guard} in the Fig. 5.8(c). In the figure, if R_{guard} is much smaller, the current I_{guard} leaking through R_{guard} will increase, resulting in the loss of accuracy over the measurement. For a given R_{guard}, I_{guard} can be reduced with higher gain of the op-amp. Another important issue is ranges of R_{DUT} and R_{load} in the Fig. 5.8(c). In the figure, if R_{DUT} increases or R_{load} decreases, the load current of the op-amp, I_{load} increases. A practical op-amp will have constraint in its load current driving capacity. If the op-amp cannot supply the required I_{load} in order to bring the voltage at G1 close to that of T8 in the Fig. 5.8(c), this will result in the loss accuracy over the intended measurement. Of course, it is possible to increase the load current driving capacity of the employed analog guard by having multiple op-amps in parallel.

5.3 Chapter Summary

A test or measurement on a post-assembled PCB is known as ICT (In-Circuit-Test). The practical challenges and measures for applying the proposed measurement to ICT are discussed in this chapter. Firstly, for application of the proposed method as an ICT requires inclusion of additional test points into the PCB design. Secondly, directing a measurement current in single direction through the measurand transmission line on a multi-IC environment can be challenging to achieve, when the transmission line is bonded to two ESD diodes from different IC chips. Therefore, in such cases the application of the proposed extraction method for finding the series RL parameters of a transmission line bonded to an IC chip requires isolation of the transmission line along with the connected IC chip from the parallel circuitry. The isolation can be achieved with jumper pads or analog guarding.

Jumper pads provides connections and isolation through placement and removal of solder dies between the pads. However, these soldering/desoldering process can turn out to be cumbersome in testing large circuits. Therefore, isolation method which do not require physical intervention to the PCB under test is of interest. In this regard, analog guarding mechanism can isolate a measurand from the parallel circuitry without any physical intervention to the PCB under test. Analog guarding entails non-inverting unity gain configuration of an op-amp to limit

measurement current flow in the parallel path of any measurand. However, the non-idealities of an op-amp (such as finite gain, finite bandwidth and parasitics) utilized in analog guarding make the extraction of L with the proposed method completely erroneous and impose constraints on the range and the bandwidth of the R extracted with the proposed method.

Chapter 6

Design of Experiments

First, the measurements which are utilized to experimentally validate the extracted parameters with the proposed method are briefly introduced. Following that the experimental setups for three experiments are discussed. The first experiment is conducted to validate the extraction of RLC parameters of a PCB transmission line bonded to an IC chip using the proposed measurement technique. The second experiment is for validating the technique to isolate parasitic resistance associated with individual printed conductor bonded to an IC pin. Finally, to show the usefulness of the proposed technique in tracking variations RLC parasitics on an FHE assembly subjected to flexing, a third experiment is carried out. All the experiments are conducted under standard temperature and ambient conditions in a controlled lab environment. The results are presented in the next section.

6.1 Measurements Utilized to Validate the Proposed Method

In this work, the extracted parameters by the proposed method are validated with respect to the corresponding parameters extracted by established techniques based on different measurement principles. Here, Time Domain Reflectometry (TDR) is utilized to verify the lump equivalent inductance and capacitance extracted with the proposed method and 4-Wire Kelvin Test is utilized for validating the lumped equivalent resistance extracted with the proposed method. This section discusses the measurement principles of TDR and Four-Wire Kelvin Test.

TDR is a technique used for characterizing a transmission line and localizing line faults [20]. In a TDR measurement, a high-speed edge produced by a step generator travels from beginning to end of a transmission line and then reflects back to the source where it is measured. Fig. 6.1 shows a simplified schematic of TDR measurement. In the figure, the discontinuity in characteristic impedance of the transmission line is described as the termination impedance, Z_T. A step voltage signal $Vs(t)=V_p*u(t)$ is applied as input. The resulting waveform $V_m(t)$ at the input port of the transmission line is a combination of both incident and reflected signals as shown in Fig. 6.2. In the figure, V_I and V_R represents the amplitude of incident and reflected voltage signals, respectively.

The time difference ΔT between the incidence and the reflection of the signal corresponds to the time taken by the signal for a round trip through the transmission line, so it can be expressed as

$$\Delta T = 2T_D \tag{6.1}$$

where T_D is the end-to-end propagation delay of the transmission line under test.

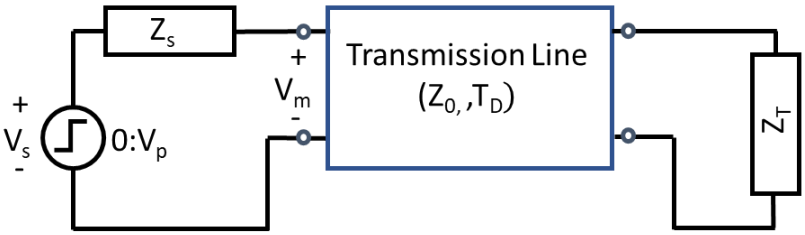


Fig. 6.1: Schematic for TDR measurement.

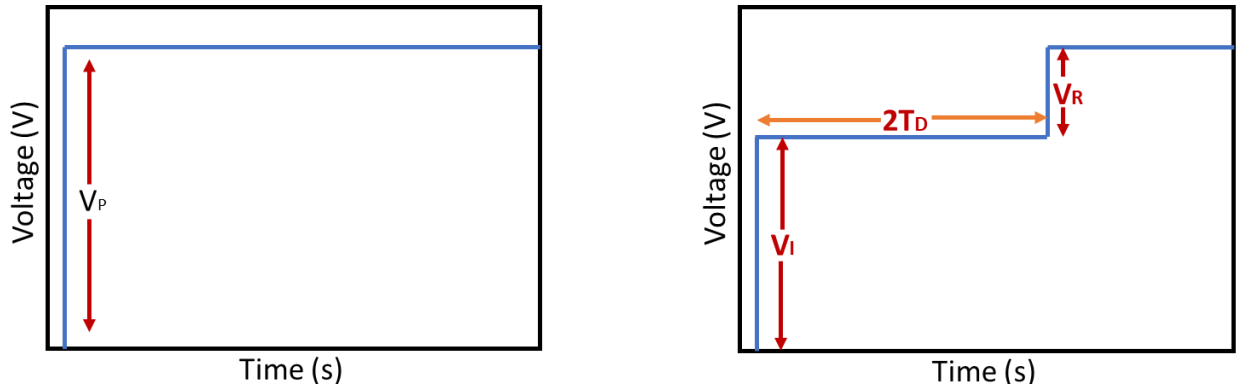


Fig. 6.2: The voltage waveform in a TDR measurement for (a) step input $V_s(t)$ and (b) measured step response $V_m(t)$.

The reflection coefficient ρ in the TDR measurement is defined as:

$$\rho = \frac{V_R}{V_I} = \frac{Z_T - Z_0}{Z_T + Z_0} \tag{6.2}$$

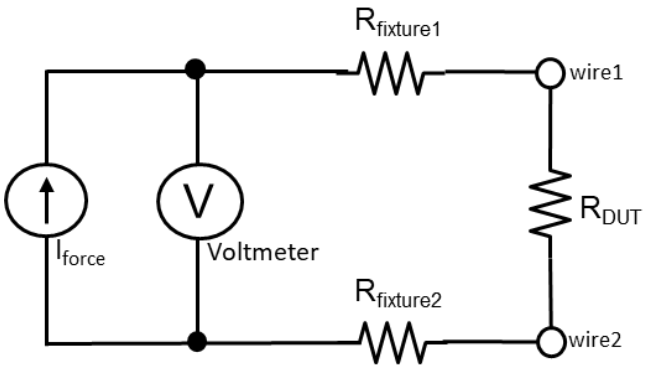
Hence, if Z_T at the terminal of a transmission line segment is known, the Z_0 of the segment can be determined and vice versa.

Further, the characteristic impedance profile, $Z_0(t)$ of the entire transmission medium of Fig. 6.1 can be expressed in terms of the source voltage waveform $V_s(t)$, measured waveform $V_m(t)$ and source impedance Z_s as:

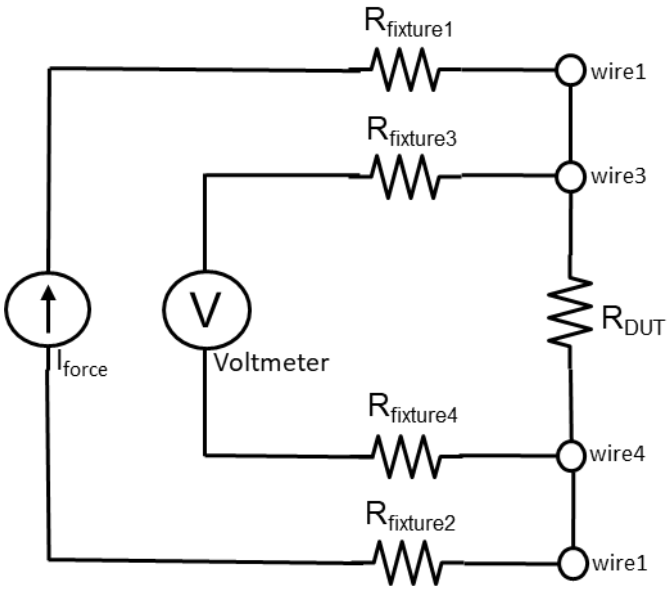
$$Z_0(t) = \frac{V_{\mathrm{m}}(t)}{V_s(t) - V_m(t)} \cdot Z_s \tag{6.3}$$

The values of Z_0 and T_D determined with TDR can be used to describe the lumped equivalent parameters of the transmission line, L_{TL} and C_{TL} using Eqns. (3.27) and (3.28).

The lumped equivalent parameter R_{TL} of a transmission line can be determined up to a certain bandwidth by measuring the two constituent printed conductors with Four-Wire Kelvin Test. Four-Wire Kelvin Test is a measurement technique for accurate measurement of low resistances invented by William Thomson, later Lord Kelvin [45]. The general measurement of moderate to high resistances are performed with a 2-wire setup as shown in Fig. 6.3(a). This involves connecting two probes to the resistance under test R_{DUT}, forcing a known current I_{force} through R_{DUT}, and measuring the resultant voltage V_{sense} with a voltmeter and calculating the resistance $R_{DUT}=V_{sense}/I_{force}$. However, when measuring very low resistances, the fixture resistances from the probe wiring and contacts contributes significant portion to the value of determined resistance, making the measurement inaccurate. To circumvent this issue, Four-Wire Kelvin Test is employed. This entails two separate pair of probes for forcing current and sensing voltage as shown in the Fig. 6.3(b). The high impedance of the voltmeter limits current through the sense probes. So the total current flows through the force probes which are excluded in the measurement. Thus, the impact of fixture resistances is eliminated, resulting in higher accuracy and sensitivity of the resistance measurement.



(a)



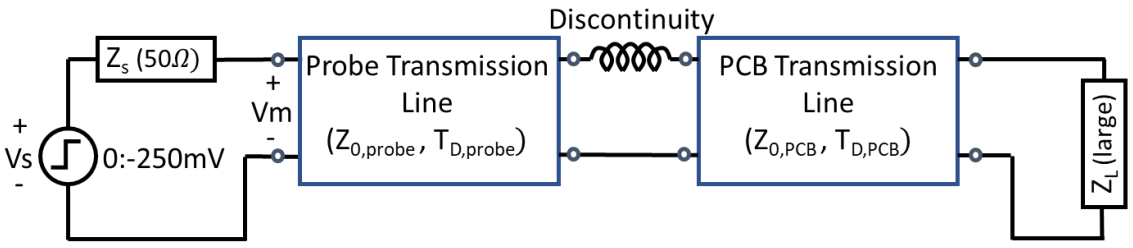
(b)

Fig. 6.3: Test setups for resistance measurement: a) 2-wire setup b) 4-wire setup.

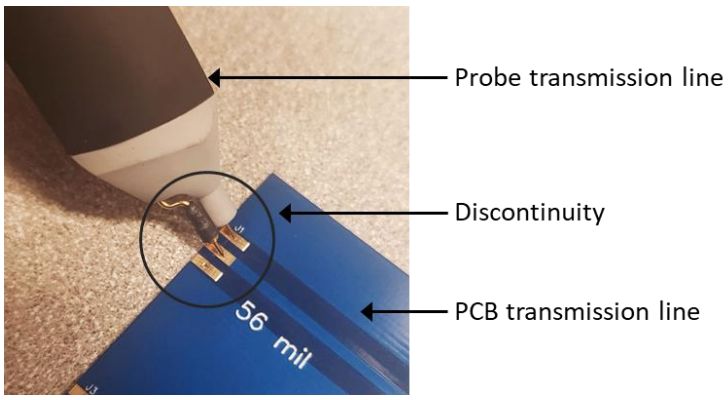
Of course, the fixture resistances can be separately measured and compensated in a 2-wire measurement. Still, this method is not as accurate and sensitive as a 4-wire measurement due to presence of the probe noise and the contact resistance variation at the probe-DUT interface (from the change in contact pressure) [46].

6.2 Experimental Setup to Validate Extracted RLC Parameters of a Transmission Line

To validate the method of extracting the RLC parameters of a transmission line, a uniform PCB transmission line on an FR4 substrate is fabricated. Time-domain reflectometry (TDR) is employed to determine its characteristic impedance $Z_{0,PCB}$ and time delay $T_{D,PCB}$, from which the $L_{TL,PCB}$ and $C_{TL,PCB}$ are found. $R_{TL,PCB}$ is found by conducting Kelvin test on the two constituent printed conductors. Fig. 6.4(a) shows the setup for the TDR measurement. In the setup, a voltage step signal from 0 to −250 mV with a rise time of ~32 ps is applied using a Picotest J2151A signal generator. The sourced signal is transmitted by a Picotest P2100A 50 Ω transmission line probe to the PCB transmission line. At the interface of the PCB and the probe transmission lines a discontinuity is formed as shown in the Fig. 6.4(b). The PCB transmission line is terminated with an open circuit, i.e., a large impedance designated by Z_L in the figure. The voltage waveform V_m at the input port of the probe is recorded with an Agilent DSA80000B oscilloscope.



(a)



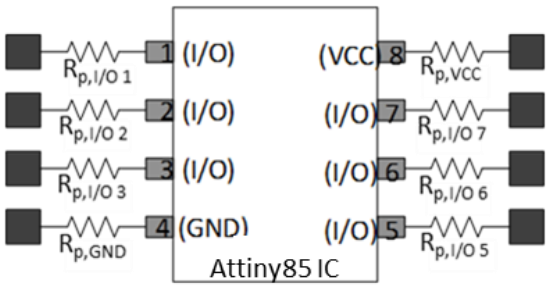
(b)

Fig. 6.4: (a) Setup for TDR measurement b) discontinuity at the interface.

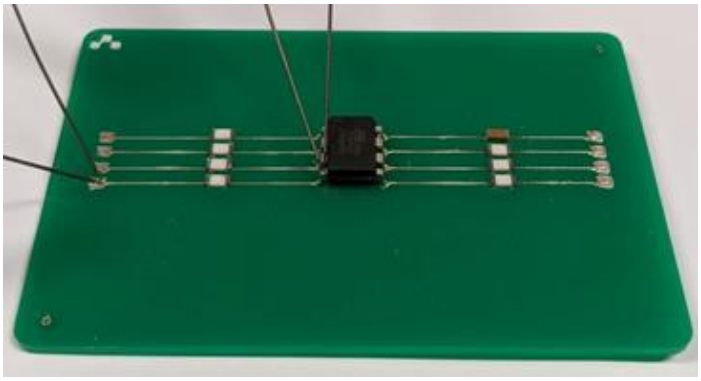
Next, the proposed measurement method is employed to extract $L_{TLPCB,}$ $C_{TL,PCB}$ and $R_{TL,PCB}$ of the same PCB transmission line. The measurement setup of Fig. 4.4 in Section 4.2 is implemented with one-port of the PCB transmission line bonded to an I/O pin (pin 2) and Gnd pin (pin 4) of the ATTINY85 IC chip. The DC current source in the setup is established with the Keithley 2450 Source Measure Meter. For blocking the DC current from entering the impedance measuring instrument, the Picotest P2130A 500 Hz-8 GHz DC blocker is used. Using the proposed measurement method, $L_{TLPCB,}$ $C_{TL,PCB}$ and $R_{TL,PCB}$ are found over a frequency range from 100 kHz to 10 MHz. Measurements over a bandwidth of 100 kHz to 1 MHz are taken with Keysight E4980A LCR Meter and measurements from 1 MHz to 10 MHz are taken with Keysight E4982A LCR meter. Upon ensuring the measured parameters at 1 MHz with the two LCR meters are in agreement, the parameters measured with E4980A meter at all the frequencies are scaled such that its measured parameters at 1 MHz are exactly the same as those from the E4982A meter. The extracted L_{TLPCB} and $C_{TL,PCB}$ with the proposed technique are compared against those found with TDR measurement and the extracted R_{TLPCB} is compared against that found from the Kelvin test.

6.3 Experimental Setup to Validate the Isolated Parasitic Resistance of a Single IC Pin

The ATTINY85 IC chip is bonded to a FR4 PCB with known R between the IC pins and the corresponding test pads. Fig. 6.5(a) depicts the electrical schematic of the setup. The resistances introduced between IC pins and test pads range from 0.5 Ω to 2 Ω. Their exact values are found by performing a 4-wire Kelvin test on the prototype at 1 MHz as shown in Fig. 6.5(b). The chosen IC package for this purpose possess leads spacious enough for probing as required by a Kelvin test. Also, the proposed measurement is employed to isolate R associated with each pin at 1 MHz. Results are obtained with Keysight E4980A LCR Meter for both of the measurement approaches. The extracted values with the proposed method are compared against the known values from the Kelvin test to ascertain the validity of the proposed method.



(a)



(b)

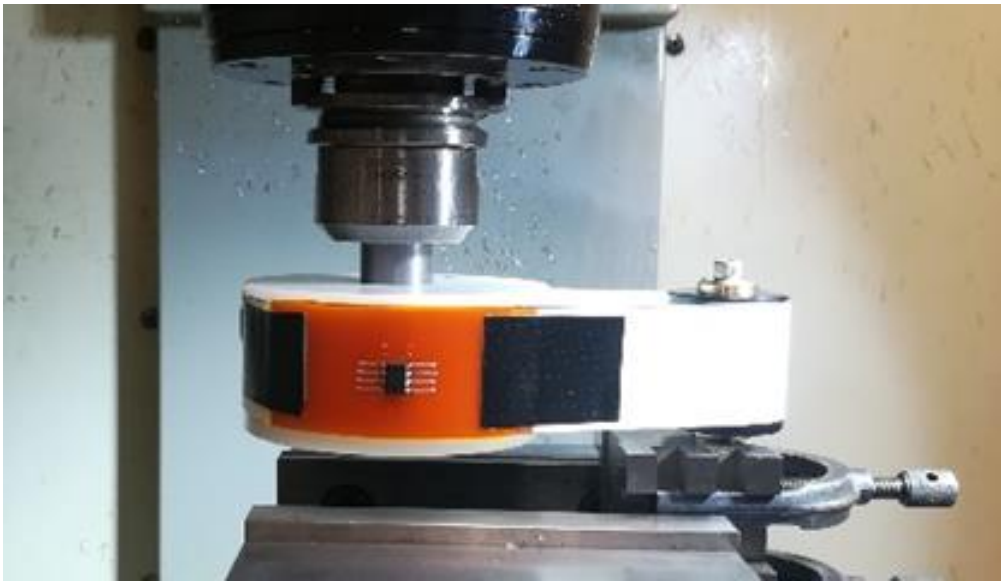
Fig. 6.5: Prototype for validating isolation of parasitic resistance associated with single IC pin: (a)electrical schematic (b) protype under Kelvin test.

6.4 Experimental Setup to Track Variation of RLC Parasitics due to Bending

To track the variation of the RLC parasitics due to flexing, two separate bending experiments are conducted using separate prototypes and experimental setups. The first experiment is implemented to track the variation of parasitic R due to stress introduced by repeated bending. Whereas the second experiment is conducted to track the variation of parasitic L and C due to change in dielectric separation between the conductive traces. All the parasitics are tracked at 1 MHz frequency with the Keysight E4980A LCR Meter.

For the first experiment, the prototype is fabricated by depositing Ag (silver) nanoparticle ink on the Kapton polyimide substrate as shown in Fig. 6.6(a). The prototype is subjected to multiple cycles of bending in a controlled mechanical setup by using the customized bending machine shown in Fig. 6.6(b). The details of the bending machine are presented in [47].

(a)

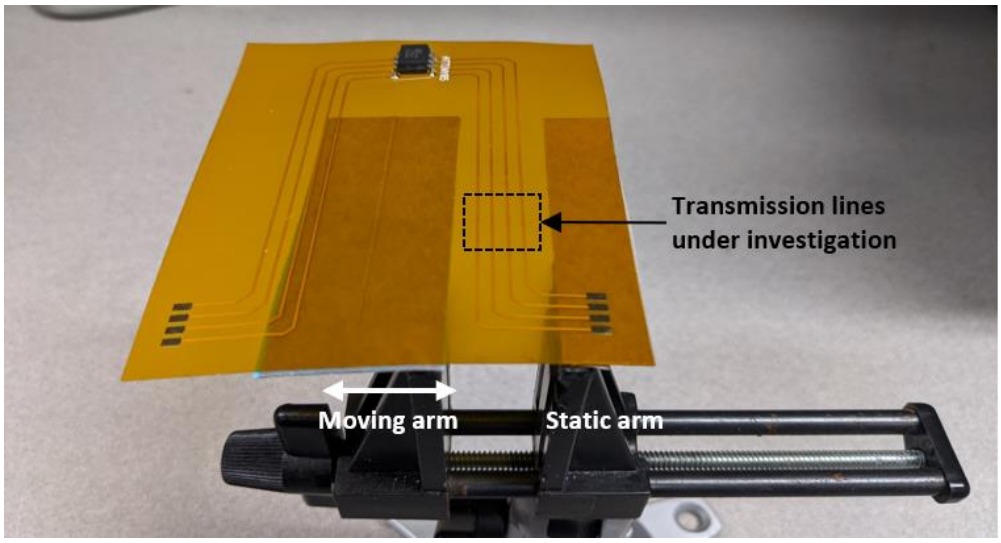


(b)

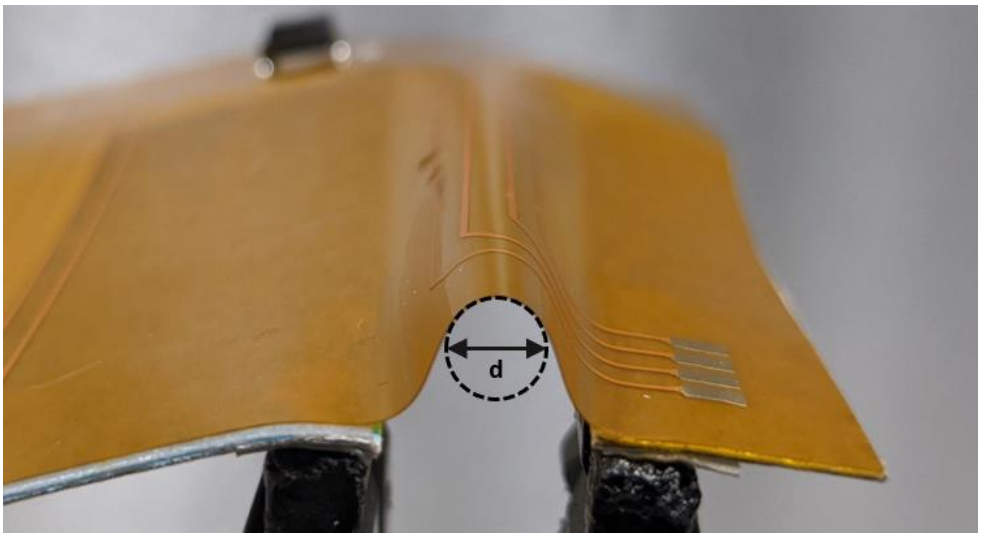
Fig. 6.6: Experiment to track the parasitic R variation: (a) prototype designed, (b) mechanical setup for bending the prototype.

Each bending cycle consists of bending the substrate at a 1.5 cm radius from its original flat form and then reinstating it back to that flat contour. Parasitic R is measured at an interval of 200 bending cycles for a total of 1600 bending cycles.

For the second experiment, another prototype is fabricated by depositing copper on Kapton polyimide substrate with some modifications in the trace layout of Fig. 6.6(a). The modifications in the conductive material and layout are made to avoid catastrophic failure of the measured conductors while bending at small diameters. A setup with a stationary and a moving arm is used to bend the substrate between the signal and return traces into small diameters and thereby reduce the dielectric separation between the traces as shown in Fig. 6.7(a). The substrate is bent such that



(a)



(b)

Fig. 6.7: Experiment to track the parasitic LC variation: (a) prototype lying flat on the bending machine (b) bent prototype.

axis of curvature formed lies at the middle of the two measured traces. A circle is fit to the curvature and the diameter *d* of the circle is recorded as shown in Fig 6.7(b). The prototype is bent at diameters of 160 mil, 130 mil, and 100 mil and the corresponding L and C are measured.

6.5 Chapter Summary

In this work, the TDR measurement and Four-Wire-Kelvin-Test are utilized to validate the extracted parameters with the proposed method. TDR sends a fast-edged signal through the transmission line and detects reflection. The characteristic impedance Z_0 and time delay T_D of the transmission line can be determined from the magnitude and time instance of the reflected signal. From the determined Z_0 and T_D, we can find the LC parameters of the line. On the other hand, the transmission line R can be determined up to a certain bandwidth by the Four-Wire-Kelvin-Test. The test method employs two wires to force current into the conductor under test and separate two wires for the sensing the resultant voltage in order to negate the effects of probe parasitics in the measurement.

Three experimental setups are delineated in this chapter. The first experiment involves the TDR measurement and Kelvin Test of a transmission line developed on rigid FR4 substrate for finding the RLC parameters of the line. The same parameters are then extracted by the proposed method with the transmission line bonded to an Attiny85 IC chip. The extracted parameters with the proposed method will be compared with those extracted by TDR and Kelvin test to ascertain the validity of the proposed method. In the second experiment, the pins of Attiny85 IC chip are bonded to printed conductors on a rigid FR4 substrate with a known value of resistance connected with each IC pin. The exact value of the resistance with each pin is known by performing the Kelvin Test. Then, the proposed method is employed to isolate the resistance associated with each pin and compared against the known values to quantify the accuracy of the proposed technique. In the third experiment, the proposed extraction technique is utilized to track the variations RLC parasitics on an FHE prototype developed on Kapton polyimide substrate. The protype is subjected to two different types of bending: cyclic and static bandings with two customized mechanical setups. In case of cyclic bending , the variation in the extracted parasitic R are tracked at definite interval of bending cycles. On the other hand, in case of static bending, the variation in extracted LC parasitics are tracked as a function of bending diameter of the substrate.

Chapter 7

Results and Discussions

The results of the three experiments described in the previous section are discussed here in the successive order.

7.1 Validity of Extracted RLC Parameters of a Transmission line

From the TDR measurement, the recorded waveforms for sourced voltage, $V_s(t)$ and DUT voltage, $V_m(t)$ are shown in the same plot in the Fig. 7.1. The part of the waveform $V_m(t)$ that is located between the interface discontinuity and open circuit discontinuity is the resultant waveform across the PCB transmission line, $V_{m,PCB}(t)$. The characteristic impedance profile of the PCB, $Z_{0,PCB}(t)$ is computed from the following

$$Z_{0,PCB}(t) = \frac{V_{\mathrm{m},PCB}(t)}{V_s(t) - V_{m,PCB}(t)} \cdot Z_s \tag{7.1}$$

Here the source impedance Z_s=50 Ω. The characteristic impedance of the PCB transmission line, $Z_{0,PCB}$ is determined as the mean of the PCB impedance profile, $\overline{Z_{0,PCB}(t)}$, as reflected waveform includes some noise. The time delay of the PCB transmission line, $T_{D,PCB}$ is found from

$$T_{D,PCB} = (T_{far} - T_{near}) / 2 \tag{7.2}$$

where T_{far} represents the time instance at the 50% of the open circuit discontinuity at the far end of the PCB transmission line and T_{near} represents the time instance at peak of the interface discontinuity at the near end of the PCB transmission line.

Table 7.1 lists the computed values of $Z_{0,PCB}$ and $T_{D,PCB}$ with the corresponding uncertainty. The uncertainty in $Z_{0,PCB}$ is estimated from the 95% confidence interval of the computed mean, $\overline{Z_{0,PCB}(t)}$. Also, the uncertainty of $T_{D,PCB}$ is estimated from the rise/fall time at the discontinuities. From the determined $Z_{0,PCB}$ and $T_{D,PCB}$, the $L_{TL,PCB}$ and $C_{TL,PCB}$ are found using Eqns. (3.27) and (3.28) and also appears in Table 7.1. The lumped equivalent resistance $R_{TL,PCB}$ for the PCB transmission line is known to be 304 mΩ at 1 MHz from separate measurements of the two constituent printed conductors using the Four-wire Kelvin test.

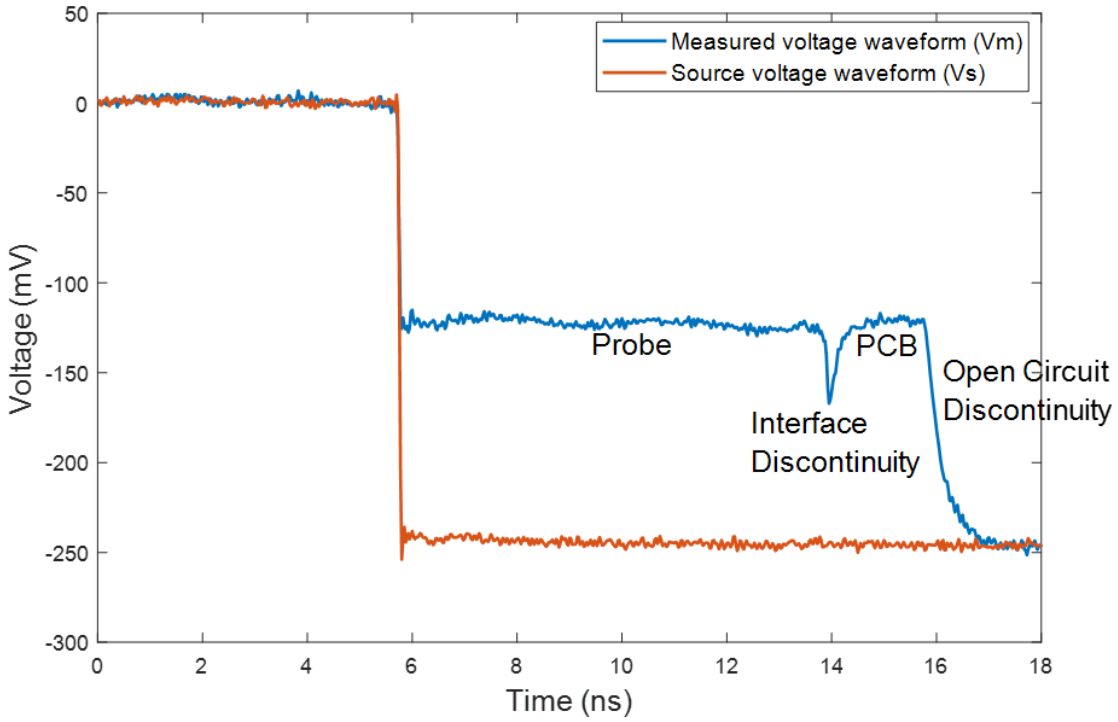


Fig. 7.1: Voltage waveform recorded from TDR measurement.

Table 7.1: Computed transmission line parameters from TDR measurement.

	$Z_{0,PCB}$ (Ω)	$T_{D,PCB}$ (ns)	$L_{TL,PCB}$ (nH)	$C_{TL,PCB}$ (pF)
Value	49.858	1.075	53.597	21.561
Uncertainty	±0.412	±0.035	±2.174	±0.530

The extracted $L_{TL,PCB}$, $C_{TL,PCB}$ and $R_{TL,PCB}$ employing the proposed measurement method in the experiment are shown in Figs. 7.2, 7.3, and 7.4, respectively. Also seen in each figure is the extracted values of the corresponding parameters found with the ADS software platform. The transmission line simulated in ADS is described by the model shown in Fig. 3.2 with N=100. The ESD diode is described by a short and open circuit under forward and reverse biased conditions, respectively. The simulated model is comprised of both the PCB and probe transmission lines. The RLC parameters used in describing transmission lines in ADS are found from TDR and Kelvin test of the practical transmission lines.

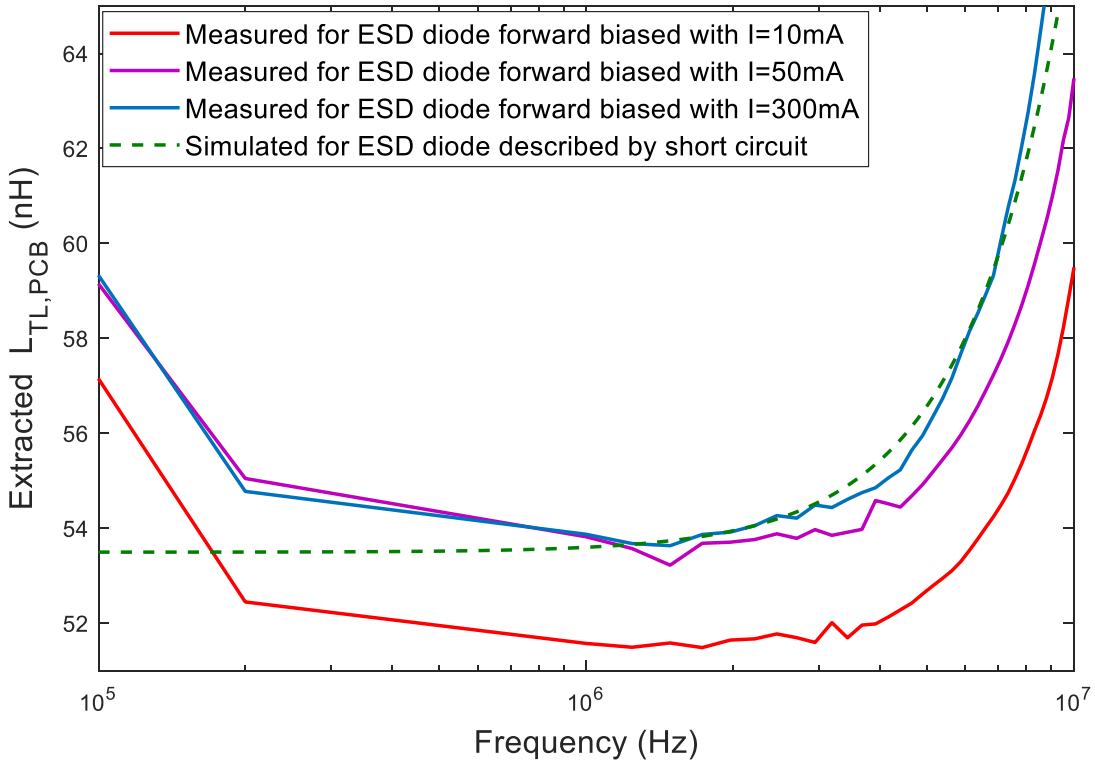


Fig. 7.2: Extracted $L_{TL,PCB}$ with the proposed measurement method.

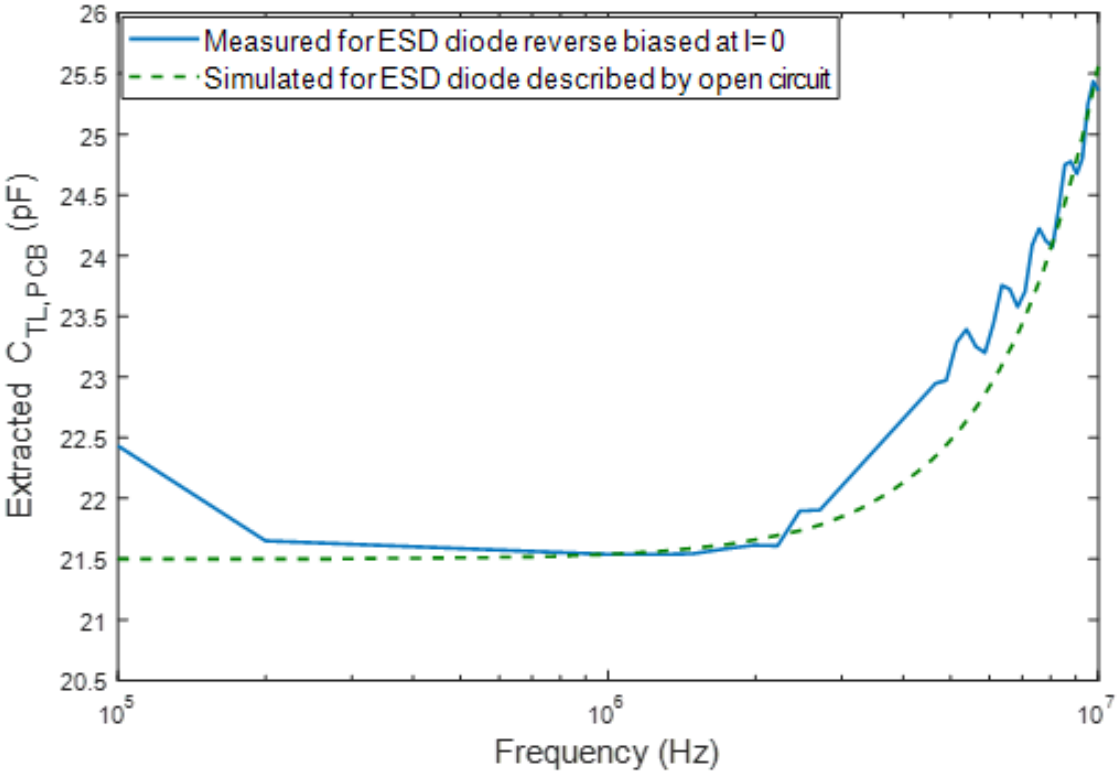


Fig. 7.3: Extracted $C_{TL,PCB}$ with the proposed measurement method.

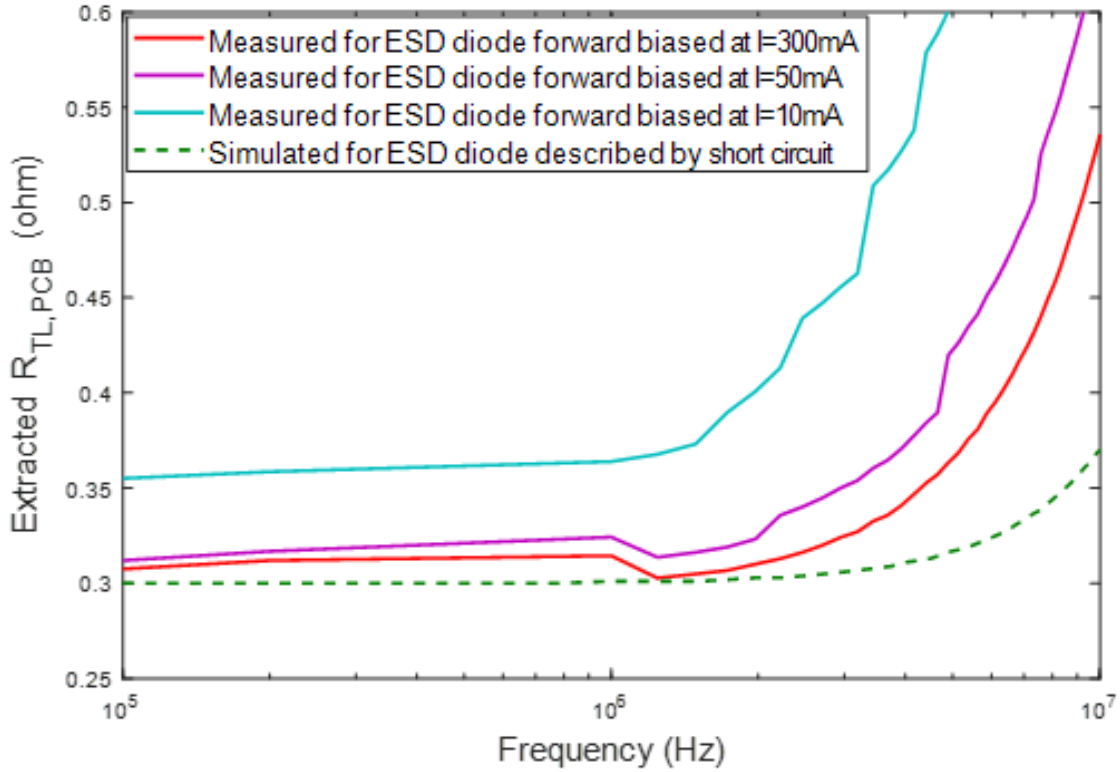


Fig. 7.4: Extracted $R_{TL,PCB}$ with the proposed measurement method.

In Fig. 7.2, the values of $L_{TL,PCB}$ extracted with the proposed technique agrees with those from TDR measurement within a certain bandwidth (~200 kHz - 4 MHz). The high frequency error in the extracted $L_{TL,PCB}$ is due to series-RL approximation becoming invalid as the frequency approaches closer towards the fundamental resonance, f_r of the entire transmission line (elaborated in the Chapter 3). Here, the f_r of the entire transmission line is found as 46.7 MHz using Eqns. (3.26) and (4.11) from the known lengths and velocity factors of the PCB and probe transmission lines. Implementing the extraction well below (at least one order of magnitude) 46.7 MHz provides reasonable accuracy over the measurement as observed in Fig. 7.2. Also, at the low end of the frequency plot of $L_{TL,PCB}$ it is masked by the instrument phase noise. Within a bandwidth of ~200 kHz to 4 MHz the accuracy of the measurement of $L_{TL,PCB}$ seems to improve with increasing ESD diode forward bias current, as shown in Fig.7.2. This is because the increase in forward bias current makes the series RL parameters of the transmission line more detectable to the impedance measuring instrument by lowering the magnitude of the load impedance presented by the ESD diode. With biasing current above 50 mA, the accuracy enhancement in measuring $L_{TL,PCB}$ saturates as the impedance of the ESD diode saturates.

In Fig. 7.3, the values of $C_{TL,PCB}$ extracted with the proposed technique agrees with those from TDR measurement within the bandwidth (~200 kHz - 4 MHz), for much the same reasons as for $L_{TL,PCB}$; phase noise and transmission line resonance limiting effects.

In Fig. 7.4, the extracted $R_{TL,PCB}$ with the proposed technique agrees with that measured by Kelvin test up to an upper frequency of ~2 MHz. The error at higher frequencies than 2 MHz is partly due to the series RL approximation becoming invalid as the frequency approaches towards the fundamental resonance of the entire transmission line. Also, there is discrepancy of the extracted $R_{TL,PCB}$ at high frequency between the practical measurement and simulation, which is due to modelling differences, such as skin effect. The accuracy of the measured $R_{TL,PCB}$ enhances with increase of ESD diode forward bias current due to the same reason as explained for extracted $L_{TL,PCB}$. Also, the accuracy enhancement in measuring $R_{TL,PCB}$ saturates at around 50 mA, which is similar to the observation made from the plot of the measured $L_{TL,PCB}$.

For the extracted $L_{TL,PCB}$, $C_{TL,PCB}$ and $R_{TL,PCB}$ the measurement bandwidth is bounded by the f_r of the entire transmission line (comprised of both probe and PCB). Of course, this measurement bandwidth is expandable by minimizing the propagation delay due to the probe transmission line.

This will shift f_r of the entire transmission line to a higher frequency, thereby providing a higher bandwidth for accurate measurement.

Table 7.2 summarizes the extracted RLC parameters of the PCB transmission line with proposed measurement at 1 MHz in contrast to the corresponding parameters measured with TDR and Kelvin test. Here, the extracted series RL parameters with proposed measurement are reported for the ESD diode forward bias current of 50 mA. From this table, it is observed that the extracted parameters with the proposed method is consistent with those found with either the TDR or Kelvin measurement methods.

Table 7.2: Summary of extracted RLC parameters with proposed method in contrast to other methods.

	TDR	**Kelvin Test**	**Proposed Method**	**Relative Error (%)**
$L_{TL,PCB}$	53.59 nH	-	53.88 nH	0.5
$C_{TL,PCB}$	21.56 pF	-	21.54 pF	0.1
$R_{TL,PCB}$	-	304 mΩ	323 mΩ	6.3

7.2 Validity of the Isolated Parasitic Resistance of a Single IC Pin

Table 7.3 compares parasitic resistances associated with four of the IC pins extracted with the proposed method (for ESD diode forward biased with I=50 mA) at 1 MHz to their corresponding known values from Kelvin test at the same frequency. The relative errors in the measured parasitic resistances for all the pins are within 5% under the chosen DC operating current.

Table 7.3: Comparison of the resistances of individual printed conductors extracted by proposed method and kelvin test.

Measurand Resistance	**Measured by Kelvin test (Ω)**	**Measured by Proposed method (Ω)**	**Relative Error (%)**
$R_{p,GND}$	2.015	2.037	1.1
$R_{p,I/O1}$	1.006	1.024	1.8
$R_{p,VCC}$	0.675	0.692	2.5
$R_{p,I/O2}$	0.507	0.525	3.6

7.3 Variation of RLC Parasitics due to Bending

Fig. 7.5 shows the extracted R associated with six different IC pins as a function of the number of bending cycles. In the figure, all the parasitic R follow an increasing trend with respect to number of bending cycles. The increase in R is caused by the accumulation of stress due to repeated bending. The dissimilarity in the increasing pattern for the different parasitic resistance is mainly due to nonuniformity in the fabrication with additive printing. The resistance associated with two of the pins (pin 3 and pin 6) increase drastically after 500 bends in one case, and 1200 in another. Here the signal path is lost. Thus, the change in trace resistance due to repeated bending can be catastrophic at some point.

Fig. 7.6 shows the extracted inductance and capacitance for two uniform transmission lines with respect to the bending diameter of curvature formed by the substrate. The two transmission lines are designated by TL1 and TL2. The dielectric separation between the signal and return paths of TL1 and TL2 are 200 mil and 300 mil, respectively. Under flat condition measured inductance and capacitance for TL1 are 160 nH and 0.45 pF, respectively, and those of TL2 are 170 nH and 0.32 pF, respectively. For both TL1 and TL2, the inductance decreases, and the capacitance increases as the diameter of curvature is reduced. The variation of inductance and capacitance is attributed to alteration of dielectric separation.

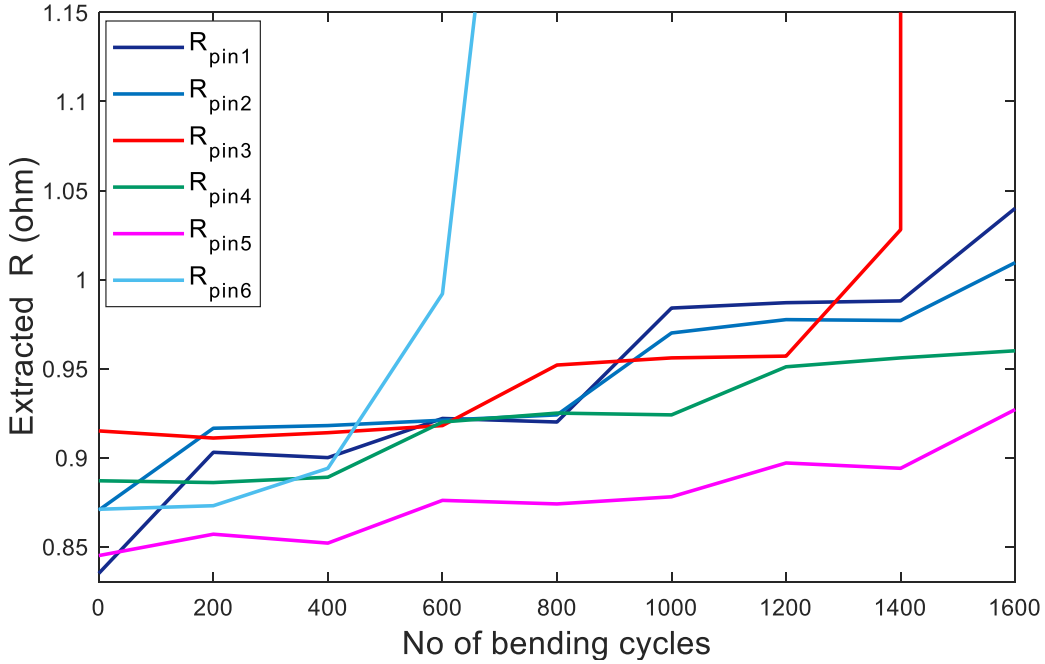


Fig. 7.5: Plot of R against no of bending cycles.

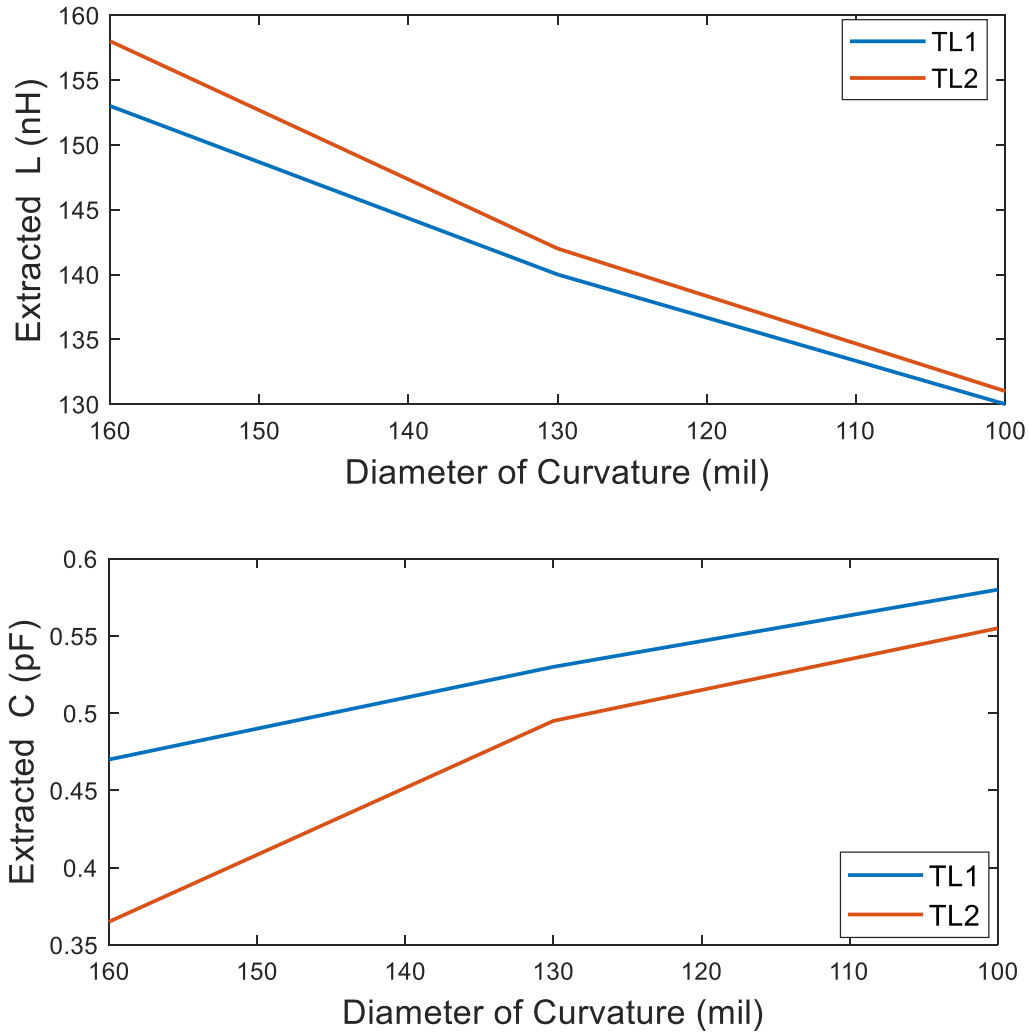


Fig. 7.6: Plot of L and C against curvature diameter.

7.4 Chapter Summary

The results of the three experiments introduced in the last chapter are discussed in this chapter. The first experiment demonstrates that the extracted RLC parameters with the proposed method agree with the corresponding parameters extracted by the TDR measurement and Kelvin Test within a certain bandwidth . For the proposed method, the bandwidth is constrained at the lower end of frequency by phase noise in extraction of the LC parameters and at the higher of frequency by fundamental resonance of the transmission line in extraction of all the RLC parameters. The second experiment demonstrates that the isolation of the R connected with a single pin with the proposed technique conforms to corresponding values of R measured with Kelvin Test. The third experiment shows that the proposed technique can be utilized to track the

variation of RLC parasitics on an FHE assembly subjected to bending. The experiment also reveals the extracted R of printed conductors bonded to an IC chip on an FHE assembly increase, at times catastrophically as the stress accumulation increases with the number bending cycles. It is also shown the extracted LC parameters of transmission lines bonded to an IC chip on a FHE assembly change as the dielectric separation between the constituent printed conductors alters from the change in bending diameter.

Chapter 8

Conclusion

8.1 Thesis Summary

First, **Chapter 1** discussed the motivation for this work. Flexible Hybrid Electronics (FHE) integrates Si-based rigid electronics and printed electronics on flexible substrate and thereby it simultaneously features the superior performance of Si-based electronics and mechanical flexibility of printed electronics. However, mechanical flexing of printed electronics causes variation in the RLC parasitics associated with the printed conductors. The presence of RLC parasitics concerns the signal integrity of a device. The progression of these parasitics can culminate into a catastrophic failure of the device and so it concerns the device reliability. Therefore, the extraction and tracking of these parasitics is fundamental to assessing success with FHE devices. In the case of FHE, the tracking of the RLC parasitics for printed conductors bonded to rigid IC chips is essential rather than tracking these parasitics for stand-alone printed conductors. This is because the complex arrangement of rigid IC chips is expected to impact the parasitic variation of the printed conductors. Thereby, this work aims to find a means for extracting the RLC parasitics associated with printed conductors bonded to a rigid IC chip.

Chapter 2 reviewed relevant research works on extraction of PCB parasitics and variation of these parasitics on a flexible PCB. Several research works employ Time Domain Reflectometry (TDR) to extract the LC parameters from a PCB transmission line through one-port access to the line. However, these TDR based measurement do not extract the lossy parameters (R and G) of a transmission line. While, in the case of FHE, the significant variation of the lossy parameter R

throughout the device lifecycle, makes its extraction essential. The lossy parameter R is extractable through measurements, such as Kelvin Test, S-parameter Analysis, which require two port access to the transmission line under test. However, it is extremely challenging to achieve two port access to a transmission lines when one of its port is bonded to a smaller package IC chip on an assembled FHE device. Therefore, a one-port measurement technique to extract the RLC parasitics from a transmission line bonded to an IC chip is essential, which is realized by the proposed method.

In this work, the RLC parasitics of PCB are treated as the parameters of transmission line. **Chapter 3** reviewed the theory of transmission line with Lumped Element Model. The description of the important of the transmission line parameters in terms of the lumped parameters are presented. Next, it is shown that the transmission line can be approximated by the series RL model and shunt C model up to a certain bandwidth for small and large load impedances, respectively. The bandwidth of the series RL and shunt C approximations is found to be well below (at least one order of magnitude) the fundamental resonance. The proposed measurement method will utilize the series RL and shunt C approximations to extract the RLC parameters from a PCB transmission line

Chapter 4 presented the proposed measurement methodology. The proposed technique utilizes on-chip ESD protection circuit in a commercial ICs to extract the RLC parameters associated with two printed conductors acting as a transmission line bonded to the IC chip. Here, the transmission line bonded to the IC pins sees the on-chip ESD diode between the pins as load. First, the impedance and the admittance parameters of the ESD diode under definite forward and reverse biased conditions needs to be modelled before the IC chip is bonded to a PCB transmission line. After bonding the IC chip to the PCB transmission line, when the ESD diode is forward biased, transmission line sees a small load at its termination. Thereby it can be approximated by series RL model. From the determined impedance of the transmission line loaded with forward biased ESD diode and known impedance of the ESD diode under the same biasing the RL parameters of the transmission line model are extracted. Likewise, for the reverse biased ESD diode transmission line load becomes large, thereby the line can be approximated by shunt C model. From the determined admittance of the transmission line loaded with reverse biased ESD diode and known admittance of the ESD diode under same biasing, the parameter C of the transmission line model is extracted. Further, the isolation of R of an individual printed conductor bonded to a single IC pin is achievable. For this, one need to utilize the extracted R from 3

transmission lines involving the I/O pin under test (the pin bonded to the printed conductor of interest), the Gnd pin and the Vcc pin of an IC.

Chapter 5 discussed the challenges and measures for applying the proposed measurement method to ICT are discussed. The application of the proposed measurement to ICT poses challenge in access and isolation. Firstly, it requires additional test point to be included in the PCB design to provide test access. Secondly, to prevent undesired leakage of measurement current through a circuit path parallel to the measurand (transmission line and the connected IC of interest), the measurand need to be isolated from any parallel circuit element. The isolation can be achieved with jumper pads or analog guarding. In this regard, the jumper pad connections and isolations are usually implemented through placement and removal of solder dies between the pads. Notably, to facilitate the jumper pad isolation in testing large circuits, a recent development of synchronized jumper pad connections and isolations through solid state relays embedded in a test structure is reported. On the other hand, analog guarding employs non-inverting unity gain configuration of op-amp to restrain the measurement current in the path parallel to the measurand and thereby isolates the parallel circuit elements from the measurand.

Next in **Chapter 6**, the TDR measurement and 4-Wire Kelvin Test, which are utilized to validate the extracted parameters with the proposed technique are described. The experimental setups for validating the proposed method and demonstrating its usefulness in tracking parasitic variation on an FHE assembly subjected to bending are presented.

In **Chapter 7**, the results of the conducted experiments are discussed. From the obtained results it is observed the extracted RLC parameters with the proposed method agree with the corresponding parameters extracted by the TDR measurement and Kelvin Test within a certain bandwidth . The bandwidth is constrained at the lower end of frequency by phase noise in extraction of the LC parameters and at the higher of frequency by fundamental resonance of the transmission line in extraction of all the RLC parameters. Also, successful utilization of the proposed method to track the variation of RLC parasitics is demonstrated through bending experiments conducted on an FHE assembly. The bending experiments reveal increase of R due to accumulation of stress and increase of LC parameters due to change in dielectric separation between the measurand printed conductors.

8.2 Future Work

The extraction of RLC parameters with the proposed technique has a bandwidth limitation both at lower and higher ends of frequency imposed by phase noise and transmission line resonance respectively. The extension of this bandwidth can be viewed as a scope for future work. The extended bandwidth will allow tracking the frequency dependent behavior of the transmission line parameters such as skin effect, dielectric loss.

Applying the proposed measurement method to In-Circuit-Testing requires isolating the measurand from the rest of the circuitry. The isolation with physical intervention to the circuit such as jumper pad isolation is challenging to implement in large circuit testing. The isolation without any physical intervention to the circuit can be achieved by analog guarding. However, nonidealities (such as finite gain, finite bandwidth, parasitics) of an op-amp used in analog guarding impose new challenges in the bandwidth and ranges of the measurement. Finding viable ways to address these challenges is an opportunity for further work.

Besides, characterizing the variation of RLC parameters on an FHE assembly based on material, dimensions, fabrication process and type of stressor are possibilities for future research.

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