Design of a Low Power, Low Area, Highly Linear Voltage-to-Current Converter for Biomedical Application

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Abstract

A voltage-to-current (VI) converter has been designed to allow a temperature sensor to be integrated into a wearable device with a pre-existing analog front-end. An already implemented Photoplethysmography (PPG) sensor in the wearable outputs current which is then processed by the analog front-end (AFE). The temperature sensor being integrated outputs data in voltage, thus rather than creating a new AFE which can process the voltage data from the temperature sensor, which would take up more silicon area and consume more power, it is wiser to design a VI converter that will create a proportional current that the existing AFE can read from. To get the output current to a level at which the AFE can process, the VI converter is split into two stages. The first stage consists of an OTA with an output voltage buffer in negative feedback configuration along with resistors in the feedback path to create a voltage subtractor topology. The input of the first stage is the voltage output of the temperature sensor (MCP9700) which based on core human body temperature ranges between $32°C\ -\ 42°C$ at extreme conditions. This temperature range as voltage from the sensor outputs $820mV\ -\ 920mV$. The output of the first stage is a voltage proportionally scaled to $0 - 100mV$.

The second stage is where the current conversion takes place with the use of a pseudo-resistor designed to replicate a $1M\Omega$ resistor. Using a second OTA in negative feedback with the pseudo-resistor allows for the output current branch to see $0 - 100nA$ of current exists within the readable range of the AFE. The output current is also independent of the load voltage within a certain error rate of $\pm 0.49\ nA$ of the expected current.

The design goals of the proposed VI converter are low power and area consumption and being independent of process variations while being extremely precise in the conversion of the voltage.

Résumé

Un convertisseur tension-courant (VI) a été conçu pour permettre l'intégration d'un capteur de température dans un dispositif portable avec une interface analogique préexistante. Un capteur PPG déjà implémenté dans le dispositif portable produit un courant qui est ensuite traité par l'interface analogique. Le capteur de température intégré produit des données en tension, donc plutôt que de créer une nouvelle interface analogique capable de traiter les données de voltage du capteur de température, ce qui nécessiterait plus d'espace silicium et consommerait plus d'énergie, il est plus judicieux de concevoir un convertisseur VI qui générera un courant proportionnel lisible par l'interface analogique existante. Pour ajuster le courant de sortie à un niveau que l'interface analogique peut traiter, le convertisseur VI est divisé en deux étapes. La première étape se compose d'un OTA avec un tampon de tension de sortie en configuration de rétroaction négative ainsi que des résistances dans le chemin de rétroaction pour créer une topologie de soustracteur de voltage. L'entrée de la première étape est la tension de sortie du capteur de température (MCP9700) qui, selon les températures corporelles humaines de base, varie entre 32°C et 42°C dans des conditions extrêmes. Cette plage de température en tant que tension de sortie du capteur est comprise entre 820 mV et 920 mV. La sortie de la première étape est un voltage proportionnellement échelonné de 0 à 100 mV.

La deuxième étape est où a lieu la conversion du courant en utilisant un pseudo-résistor conçu pour reproduire une résistance de 1 MΩ. En utilisant un deuxième OTA en rétroaction négative avec le pseudo-résistor, cela permet à la branche de courant de sortie de voir un courant de 0 à 100 nA qui existe dans la plage lisible de l'interface analogique. Le courant de sortie est également indépendant de la tension de charge dans une certaine marge d'erreur de ±0,49 nA du courant attendu.

Les objectifs de conception du convertisseur VI proposé sont une faible consommation d'énergie et d'espace et l'indépendance des variations de processus tout en étant extrêmement précis dans la conversion de la tension

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- L. F. Martínez Pantoja, A. D. Sánchez and J. M. Rocha Pérez, "A new Tunable Pseudo-Resistor for Extremely/Ultra Low Frequency applications," 2019 16th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE), Mexico City, Mexico, 2019, pp. 1-5, doi: 10.1109/ICEEE.2019.8884489.
- E. Raguvaran, N. Deepak Prasath, J. Alexander, N. Prithiviraj and M. Santhanalakshmi, "A very-high impedance current mirror for bio-medical applications," 2011 IEEE Recent Advances in Intelligent Computational Systems, Trivandrum, India, 2011, pp. 828-830, doi: 10.1109/RAICS.2011.6069425. keywords: {Mirrors;Impedance;Transistors;Low voltage;CMOS integrated circuits;CMOS technology;Leakage current;super-Wilson current mirror;high output impedance;Drain symmetry;Auxiliary current source},

Nomenclature

AFE	Analog Front-end
CMRR	Common Mode Rejection Ratio
CMOS	Complementary Metal-Oxide Semiconductor
PPG	Photoplethysmography
VI	Voltage-to-Current
THD	Total Harmonic Distortion
CM	Current Mirror
DC	Direct Current
OTA	Operational Transconductance Amplifier
Op-Amp	Operational Amplifier
P	Pole
z	Zero

Chapter 1 - Introduction

1.1 Motivation

As the progression of personal health monitoring technology advances, novel methods for monitoring various physiological parameters are being actively explored. Thanks to the widespread use of smartphones and the seamless connectivity facilitated by internet and Bluetooth protocols, it has led to a surge in the introduction of innovative devices that monitor different aspects of the human body. The devices are packed with sensors to measure the vital signs such as blood oxygen levels and heart rates. In conjunction with the sensors, it is equally important to have analog front ends to decipher the data from the sensors that convert and present it in a succinct and understandable manner for the user.

In healthcare settings, top-tier and costly technology is used for the meticulous monitoring of vital signs in patients, including parameters such as heart rate, blood pressure, and oxygen levels. Each vital sign is thoroughly observed using specialized machines known for their remarkable accuracy, enabling healthcare professionals to determine the optimal course of action for individual patients. However, the extremely high accuracy and abundant functions in such high-end technology also introduces a degree of inaccessibility due to its associated costs. Furthermore, this level of accuracy may extend beyond the essential requirements for the average consumer. In contrast to these high-priced medical apparatuses, more affordable alternatives such as wearables, exemplified by smartwatches, offer users access to the same vital sign information at a much lower cost. Over time, industry giants like Apple, Google, Samsung, and others have progressively incorporated an expanding array of sensors into their devices, in smartphones and smartwatches, facilitating the tracking of various bodily metrics. For instance, the photoplethysmography (PPG) sensor is employed to measure both the heartbeat and blood oxygen levels [1]. Another prevalent and important sensor integrated into many wearables is the temperature sensor.

The inclusion of a temperature sensor in wearables holds significant importance, as understanding body temperature is highly valuable for both users and healthcare professionals in gauging the user's overall health. Elevated body temperatures, indicative of a fever (temperatures exceeding 38 degrees Celsius), may result from various factors such as infections, medications, strokes, or certain cancers. Contrarily, abnormally low body temperatures, signaling hypothermia (below 35 degrees Celsius), can pose severe, and

potentially fatal, risks. Instances of low body temperatures may arise due to prolonged exposure to extremely cold temperatures, shock, or underlying metabolic disorders like diabetes or hyperthyroidism. Consequently, the integration of a temperature sensor into wearable devices designed for vital sign measurements emerges as a crucial component.

1.2 High Level System/Design Goals

In our lab a framework encompassing diverse sensors such as PPG, temperature, other signals, along with a low-power read-out analog front end (AFE) is being developed. The AFE is specifically engineered to directly interpret current values without necessitating voltage conversion. Consequently, our current focus involves designing a low-power voltage-to-current converter to facilitate the utilization of the same AFE for the temperature sensor that outputs voltage.

To implement a temperature sensor into the wearable, there were certain factors that needed to be looked at for example, size, ease of integration, power consumption, etc. Temperature sensors can be found in different forms, such as on chip, printed, however due to their larger dimensions and form factor, they were not chosen for this application. To design an on-chip temperature sensor for this application would require a lot more silicon space and power consumption than it would to simply implement a temperature sensor IC.

The temperature sensor chosen (MCP9700) has a voltage output the range of $0.2mV\ to\ 1.8V$ for the temperature range of $-40°C\ to\ 125°C$ with $0°C$ being at $500mV$.

The MCP9700 has a temperature coefficient of 10mV/°C. The core body temperatures of a healthy person on a normal basis float around 36.1°C to 37.2°C. As such, it was deemed more efficient to design a system to read the temperature between the range of 32°C and 42°C, allowing the system to operate in the extremes of the core human body temperature range. In this range of temperature, the output from the sensor is between 820mV to 920mV.

As a low power small area AFE has already been designed to read and process the PPG's sensor data, it would be beneficial to convert the temperature sensor data into a proportional current such that the AFE can read it. This can be done by designing a low power, low area, and highly precise voltage-to-current converter.

Wearables have very limited battery capacity as they need to fit on the user while not being overly bulky, as such one of the goals for the VI converter is to design it for low power

consumption. Silicon real estate is a crucial design aspect that the designer must take into consideration for chips that will be used in wearables, where space is highly limited. As such, another important design goal for the VI converter will be low area consumption to allow for compact integration in the overall system.

In terms of output specifications, the AFE can read a maximum of $100nA$ with the input node being of the AFE ranging anywhere between $400mV - 600mV$. This means that at the output node of the VI converter, the output current should be independent of the load voltage, or at least operational within the AFE node voltage range.

The VI converter is considered a vital building block in electronic circuits as it can serve various purposes in multiple applications. One of the applications being the conversion of voltage data from a sensor into current data which a system can read as used in this thesis. Other applications include the design of current sources which inherently uses some kind of bias voltage to produce a proportional output current that can be used for biasing transistors, diodes, LEDs, etc.

The design of the VI converter will be separated into two stages: voltage subtraction, and voltage to current conversion. A high-level system overview can be seen in figure 1.1.

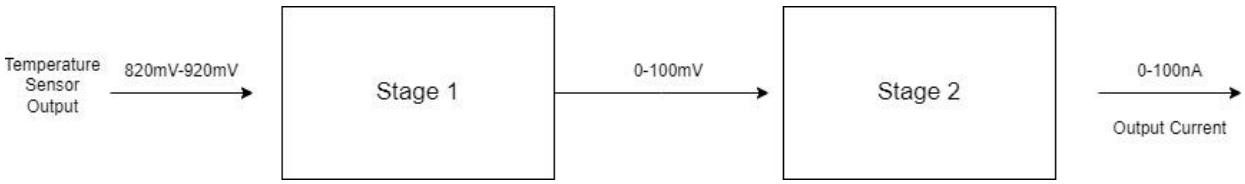


Figure 1.1 – High level VI converter overview

With the input of $820mV - 920mV$, stage 1 will subtract a reference voltage to give an output of $0 - 100mV$ where stage 2 can then convert that to an output current to $0 - 100nA$.

It is vital the output current can be read by the AFE, and that no data is lost during the conversion. As such, a margin of error is also set. Based on normal temperature readings done by wearables on the market, the body temperature is only taken to the first decimal point of accuracy. Thus, it is crucial that the VI converter is precise to the tenth of a Celsius within the temperature range determined.

As the output current can only be a maximum of $100nA$ with a total of $10°C$ to read, this means that there are 100 points of data to allow for the $0.1°C$ precision. This means that the precision for the VI converter is $0.1°C/nA$. With any analog design, system inaccuracies will cause deviations from the expected values and as such an error margin needs to be determined. As it would be very difficult to get the exact expected value at the output (i.e. 50.0nA), a $\pm 0.49nA$ error range of the expected value is set. As the precision of the VI converter is set to $1nA/0.1°C$ this would mean that in terms of temperature the tolerance would be $\pm 0.049°C$ of the measured temperature from the temperature sensor.

The proposed design of the VI converter provides a very precise representation of the temperature within the specification regarding the output current. In this design, the aim or low power and low area is what makes this design more appropriate for this specific application. With the use of a pseudo resistor in the second stage which is what is used for the conversion, a very large on chip resistance is achieved in a fraction of the area. Since the other VI converters designed which will be mentioned in chapter 2 don't have a specification for output current as low as this application in the nA, the use of large resistors is common. This in turn will also add to the deviations in output current observed due to process variations as on chip resistors are known for their process and temperature dependence. In this design, by choosing an alternate method to derive the large resistance, there is a large reduction in area which is a pivotal specification.

1.3 Thesis Organization

In Chapter 1, motivations behind the implementation of different sensors into wearable technology was discussed to provide context for the voltage-to-current converter requirements within the application. In Chapter 2, extensive literature review is provided on the different architectures of the Voltage-to-Current converter along with the theory behind the main circuit blocks used. In Chapter 3 and 4, the design of the OTA and the Pseudo-resistor will be presented. In each chapter, the design choices in terms of specifications, design process' presented with the simulation results from schematic as well as post-layout simulations. Chapter 5 will be a deeper dive into the proposed VI converter and its full design using simulation and post-layout simulation data. Finally, Chapter 6 provides a detailed conclusion with the summary of the work, with limitations of the design and how it can be improved upon in future iterations.

Chapter 2 – Literature Review

2.1 – Voltage to Current Converter

A voltage to current converter as the name suggests is a circuit that takes voltage as an input, and outputs a proportional current. A block diagram describing the definition is shown in figure 2.1.

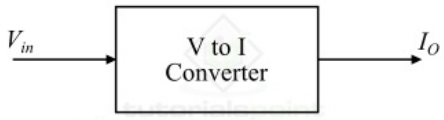


Figure 2.1 – Voltage to current converter block diagram

To understand the VI converter, the most basic relationship between voltage and current that is known as Ohm's Law must be known.

$$V = IR \tag{2.1.1}$$

Where the output current would then be represented as

$$I_o = V/R \tag{2.1.2}$$

This relationship shows that if a voltage is supplied with a resistor, a proportional current will flow through circuit. Through this relationship, it is clear that the resistance is the deciding factor for the current flow in a voltage source circuit and performs the current conversion in a linear circuit. The most basic VI converter circuit uses only an input voltage and a resistor to achieve a proportional current as shown in figure 2.2.

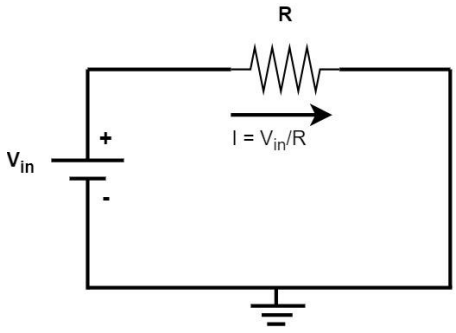


Figure 2.2 - Basic VI converter using only a resistor with the current flowing through the circuit being proportional

As the output current is based solely on the voltage drop across the load, it is considered a very crude and inaccurate passive implementation of the VI converter. In any form of application, the output current signal from this system will need to be processed and converted from analog signals to digital, making a passive implementation useless.

2.1.1 – VI Converter Implementations

A simple implementation of a VI converter using an OTA is by having it in negative feedback using an NMOS transistor as a buffer tied to a resistor as shown in figure 2.3.

In this figure, the OTA is in a negative feedback voltage follower configuration which allows the resistor R_S to convert the input voltage into a proportional current based on the resistance and equation (2.1.2). The current produced through R_S is then copied to another branch as the output current using a simple current mirror [2]. One aspect of this design that needs to be taken into consideration is that the output branch that is integrated into the AFE must operate at the voltage provided at that node by the next block. Hence, the current mirror must also be robust and operate within a large load voltage region which encompasses the voltage of the next circuit block.

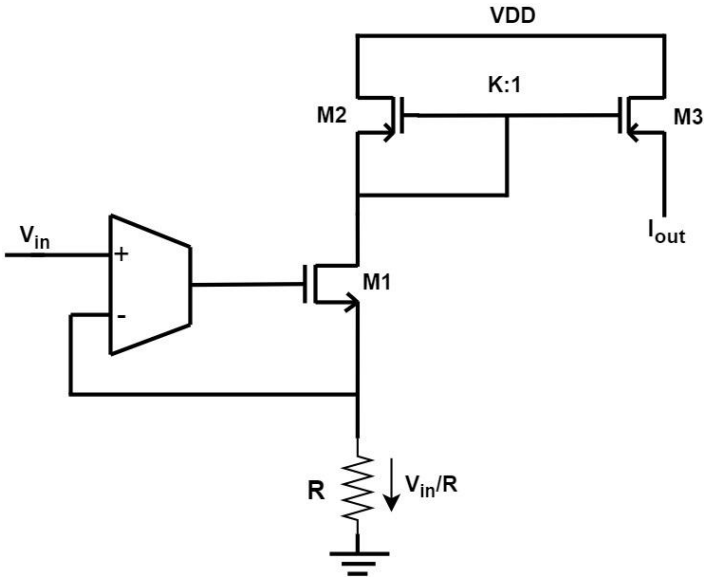


Figure 2.3 – Voltage to current converter using an OTA in negative feedback with an output current mirror where the conversion occurs at R_S

Another method of implementation is the feed-forward voltage attenuation (FFVA) proposed by [2] which can be seen in figure 2.4. This is an implementation of a rail-to-rail VI converter

that makes use of a voltage divider which is then used as the input to the OTA based VI converter.

By attenuating the voltage, this topology allows for a larger input voltage range. The input voltage is buffered by T_1 which allows for the rail-to-rail input-output operation and then fed into voltage divider formed by linear resistors R_1 and R_2. This outputs an attenuated voltage αV_{in} where

$$\alpha = \frac{R_2}{(R_1 + R_2)} \qquad 2.1.3$$

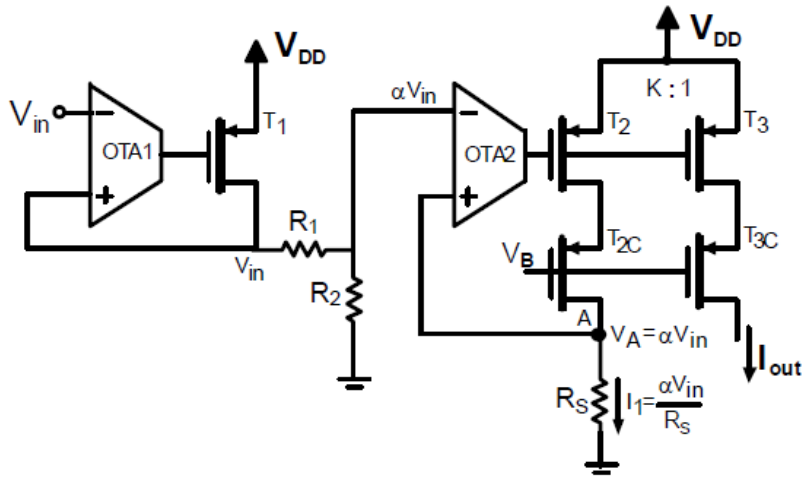


Figure 2.4 – Voltage attenuation VI converter implementation reprinted with permission from [2] (*Copyright © 2011, IEEE)*

This attenuated voltage is the new voltage that is fed into the main VI converter made up by OTA2 and transistors T_2 and T_{2C}. The output current I_{out} is driven by the cascode transistors T_3 and T_{3c} which improves the current copy over a larger load voltage range. This cascaded current mirror has a scaling factor of K. Therefore, the output current is

$$I_{out} = \frac{1}{K} \cdot \frac{\alpha V_{in}}{R_s} \qquad 2.1.4$$

[2] reported that with a supply voltage of $1.2\,V$ the FFVA has an input voltage range of $0 - 1.2\,V$ with a power consumption of $52.87\mu W$ with a 0.6% error rate. The total harmonic distortion (THD) was measured at $-41.2dB$ at $1\,V_{PP}$. Another design proposed by [2] called the feedback voltage-attenuated VI converter presented a $0 - 1.19\,V$ input range with an error

of 0.15%. The THD was measured to be better than FFVA at $-53.6dB$ with a power consumption to be very similar to that of the FFVA at $52.86\mu W$.

[3] proposed a fully differential output current mode VI converter with a supply voltage of $1.5\,V$. They were able to achieve a 0.5% THD value at the supply voltage with a very small power consumption of 1.5 μW. The output current displays high linearity with the input differential voltage range between $\pm 0.8\,V$. The conversion takes place by having current mirrors cross-coupled with the input NMOS differential pair. Cascoded with the input pair is a PMOS transistor externally biased, which if biased correctly would allow the converter to operate near VDD. Also cascoded with the input pair are current mirrors the copy the current to the differential output branch that if biased properly allows the converter to operate near VSS [3]. The output current range is dependent on the external bias voltage for the cascaded PMOS pair. A higher supply voltage increases the magnitude of the output current.

Highly linear implementations of the VI converter are presented in [4]-[5]. To increase linearity, [4] controls the mobility degradation factor by connecting the substrates of output current mirrors to an external voltage rather than V_{SS}. [5] increases linearity by reducing the threshold voltage variation.

To reduce the area of the design by replacing a resistor by implementing a transistor operating in the triode region was utilized by [6]. A simple differential amplifier is used in negative feedback configuration and allows for a high conversion range of the input voltage. The limitation of the maximum input voltage however is imposed by the operation of the transistor in the triode region.

2.1.2 – Current Mirror Topologies

In most cases, the output current of the VI converter are copies of the original output current using various methods of current mirrors. Not only are they used for outputs, but also for applications such as current sources, current amplifiers, active loads in OTAs, analog filters, etc. [8] – [11]. The core parameters for a CM include the percentage error ratio (PER), input/output resistance, load voltage range, and bandwidth [10]-[11]. The PER is indicative of how accurately the CM can copy a current. The load voltage range is also an important parameter as it expresses the voltage range where the output current behaves as a mirror of the input current.

Accuracy is highly important in applications such as the VI converter where depending on the input voltage range, and output current range, a small difference in current copy can completely change the operation of the circuit that follows. Applications that include parameters such as DC gain. Common-mode rejection ratio, power supply rejection ratio expects to have minimum loading effects [12]. Due to this, a high output resistance with low input resistance is expected [12],[13].

The simple current mirror that is most used and thoroughly developed in literature is depicted by figure 2.5. The working of this CM depends on the applied voltages as well as the aspect ratio. The gate-source voltage of M1 and M2 are equal hence the channel current would be equal. Saturation of both transistors is needed for proper operation and current mirroring.

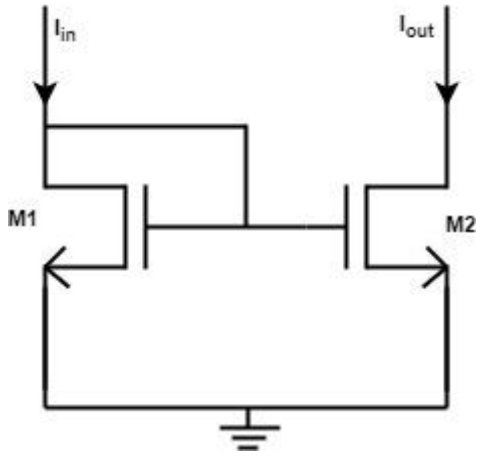


Figure 2.5 – Basic current mirror topology

The basic current mirror provides a good current copy however has a relatively small output resistance as compared to other topologies. To modify the performance of the basic current mirror, the Wilson current mirror consists of three transistors with one of them in a diode connected configuration on the output branch to maintain the gate-source voltage for mirroring. The diode-connected transistor is implemented in a way that produces a shunt-series negative feedback which provides a higher output resistance [11],[14]. Although the Wilson CM has a higher output resistance, the input and output voltages needed to keep all transistors in saturation are too high, reducing the voltage headroom for secondary circuits. To improve this performance an improved Wilson CM was proposed by [14] and depicted in figure 2.6. This topology has four transistors with the input transistors in diode-connected configuration while transistors M3 and M4 provide the accurate current copy by equalizing the V_{DS} of the base

transistors of M1 and M2. The output resistance of the improved current mirror can be calculated as

$$r_{out} = \frac{g_{m1} r_{01} g_{m3} r_{03}}{g_{m2}} \qquad 2.1.5$$

This topology provides a higher output resistance and a more accurate current copy than that of the normal Wilson CM [14].

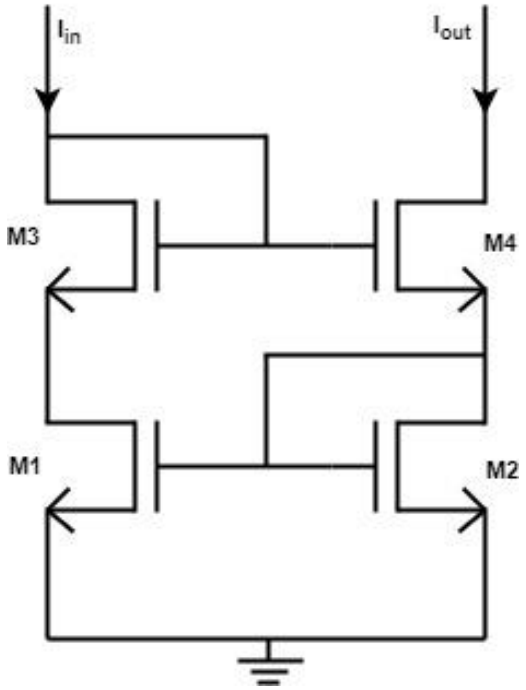


Figure 2.6 – Improved Wilson Current Mirror

The cascode CM is further designed to increase the output resistance and enhance the accuracy of the current copy. This method increased accuracy which is the result of a difference in output and input voltage. The V_{DS} of M1 and M2 are balanced by M3 and M4 which results in the output resistance as [11],[14]

$$r_{out} = r_{03} + r_{02}(1 + r_{03}(g_{m03} + g_{m02})) \qquad 2.1.6$$

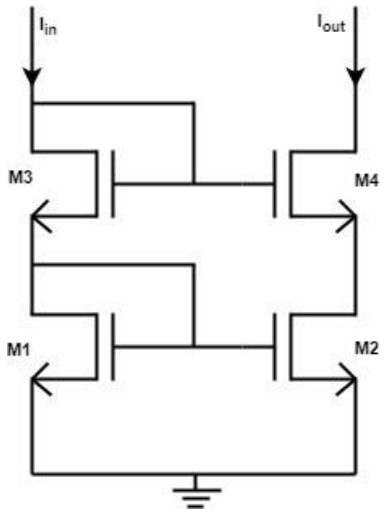


Figure 2.7 – Cascode Current Mirror

The cascode CM in figure 2.7 is the cascoded implementation of the basic CM. For a proper operation, the drain-source voltage of M2 should follow the V_{DS} of M1. M2 and M3 need to maintain saturation for this purpose and would occur only if $(W/L)_2/(W/L)_1 = (W/L)_3/(W/L)_4$ [14]. With proper biasing, highly accurate current copy can be achieved in the output branch while also being load voltage independent [14].

While the current mirror topologies mentioned thus far provide good performance, they are very fundamental designs. More recent designs show higher output resistance with very low error percentage at the output current node. They also present a high operating voltage range at the output node. Figure 2.8 shows the current mirror design from [15] which has an output resistance of

$$r_{out} = (g_{m1}||g_{m6})g_{m2}r_{01}r_{02}r_{05} \qquad 2.1.7$$

The current mirror proposed in [15] presents a very high output voltage range $(0.1V - 1.8V)$ at low input currents $(5\mu A)$ which would be ideal for the design in this thesis. Compared to other designs mentioned, the simulated output resistance is also very favourable. The proposed design in [15] clearly shows higher performance than that of the fundamental current mirrors, but it comes at the price of high-power consumption.

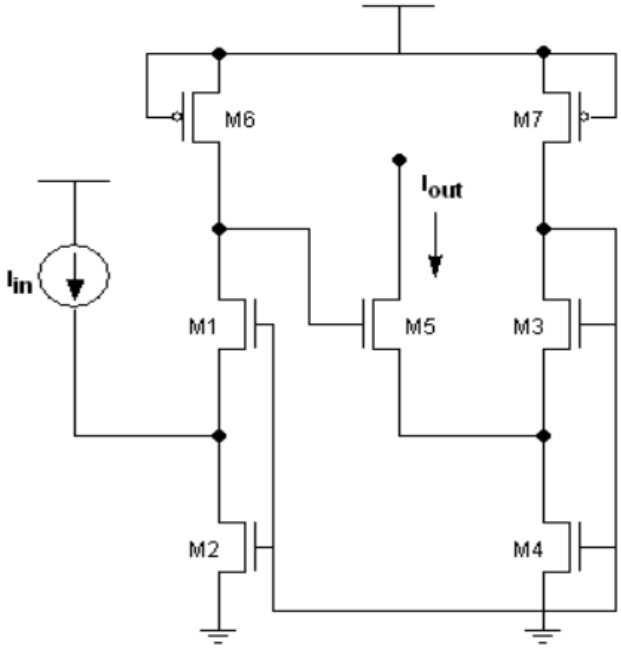


Figure 2.8 – Current mirror topology reprinted with permission from [15] (*Copyright © 2011, IEEE)*

2.2 – Operational Transconductance Amplifier (OTA) Review

The operational transconductance amplifier (OTA) stands out as a highly versatile and frequently utilized circuit block in analog circuit design [8]-[9]. Functioning as an amplifier, an OTA transforms differential input voltage into an output current, essentially serving as a voltage-controlled current source [16],[17]. Despite their similar operational nature, the OTA and op-amp differ in key parameters. For instance, unlike the op-amp, the OTA produces an output in the form of current rather than voltage [8]. An ideal OTA presents an output current resulting from the product of the OTA's transconductance and the differential input voltage [8].

$$I_{out} = (V_{in+} - V_{in-})g_m \qquad 2.2.1$$

The output voltage of the OTA is a product of the output current and the output resistance. As a result, the voltage gain (A_v) is a product of the output resistance (R_o) and the transconductance (g_m) of the OTA [9]. The transconductance is directly proportional to the bias current of the amplifier [9].

In this section, the focus will be on the operation and implementation of the common OTA topologies. There are many OTA topologies that get used in different stages: Single stage, Differential pair with common source amplifier, Folded Cascode amplifier, telescopic amplifier. Etc. The common denominator between all the topologies is the input method they use, the differential pair [3], as such we will dive deep into its operation.

2.2.1 - Differential Pair

Many circuits will have an input signal represented by taking the difference of two voltages thereby needing an important circuit called the differential pair shown in figure 2.9. Although single input OTAs exist, for purposes of higher stability and noise reduction though feedback methods, the most common input stage of an OTA is the differential pair [8].

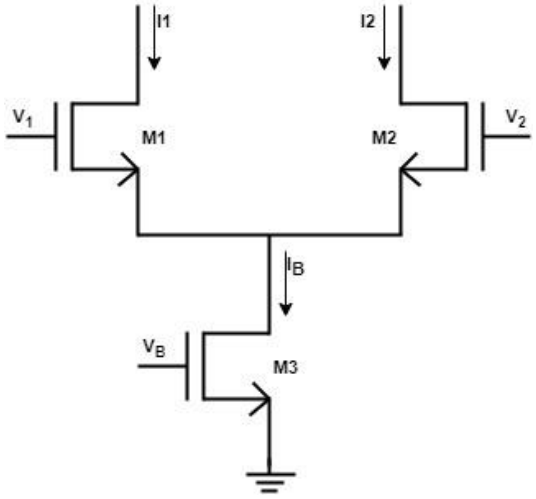


Figure 2.9 – Differential pair circuit

The gates of transistors M1 and M2 act as the input to the circuit for V_1 and V_2 respectively. The bias current I_b for the differential pair will be controlled by M3 and the bias voltage V_B.

The precise determination of the DC operating point for M1 plays a critical role in circuit biasing [9]. It must be calculated accurately to ensure that the current supplied by M2 matches that of M1 when both transistors are operating in the saturation region. The differential pair functions as the input for amplifiers, allowing for fluctuations in input voltages without influencing the gain stages. As M3 will act as the current source for the differential pair, the current through the circuit can be seen as thus:

$$I_B = I_1 + I_2 \qquad 2.2.2$$

To provide some analytical context to this amplifier let's say a differential voltage V_{I1} and V_{I2} is applied to M1 and M2 respectively with their DC and AC components as such:

$$V_{I1} = V_1 + v_1 \; and \; V_{I2} = V_2 + v_2 \tag{2.2.3}$$

Thus, the input difference between can be written as

$$V_{D1} = V_{I1} - V_{I2} = V_{GS1} - V_{GS2} \tag{2.2.4}$$

At equal gate potentials for M1 and M2 with the assumption that both transistors are operating in the saturation region

$$I_{D1} = I_{D2} = \frac{I_B}{2} \tag{2.2.5}$$

2.2.2 – Maximum and Minimum Differential Input Voltage

As we know, a MOSFET in saturation follows the relation of

$$I_D = \frac{\beta_n}{2}(v_{GS} - V_{TH})^2 \tag{2.2.6}$$

The differential voltage can be then described as

$$v_{D1} = \sqrt{\frac{2}{\beta_n}}\left(\sqrt{I_{D1}} - \sqrt{I_{D2}}\right) \tag{2.2.7}$$

The maximum difference input voltages v_{DIMax} can be found by setting I_{D1} to I_B and I_{D2} to 0 which is equivalent to having M2 turned off and having M1 conducting all of the tail bias current.

$$v_{DIMax} < v_{I1} - v_{I2} = \sqrt{\frac{2 \cdot L \cdot I_B}{KP_n \cdot W}} \tag{2.2.8}$$

The minimum differential input voltage v_{DIMin} can be then found by setting M1 to off and M2 conducting all the bias current, which is just the negative of the maximum differential voltage.

$$v_{DIMin} = -v_{DIMax} = -(v_{I1} - v_{I2}) = \sqrt{\frac{2 \cdot L \cdot I_B}{KP_n \cdot W}} \tag{2.2.9}$$

2.2.3 – Maximum and Minimum Common Mode Voltage

A common mode of operation for the differential amplifier is to have the inputs forced by using feedback (mainly negative). As circuit analysis dictates which will not be discussed in this

chapter, this allows both inputs to reach the same or very nearly the same voltages. This voltage which is more precisely the average of the two inputs is known as the common mode voltage. When designing the amplifier, it is important to know the minimum and maximum common voltages that will keep both M1 and M2 operating in the saturation region. When the common-mode voltage is too high, both input transistors will enter the triode region (behave like resistors) and when the common-mode voltage is too low, then the input transistors will shut off not allowing any current to pass through. Figure 2.10 shows the differential amplifier with both inputs tied to a common input.

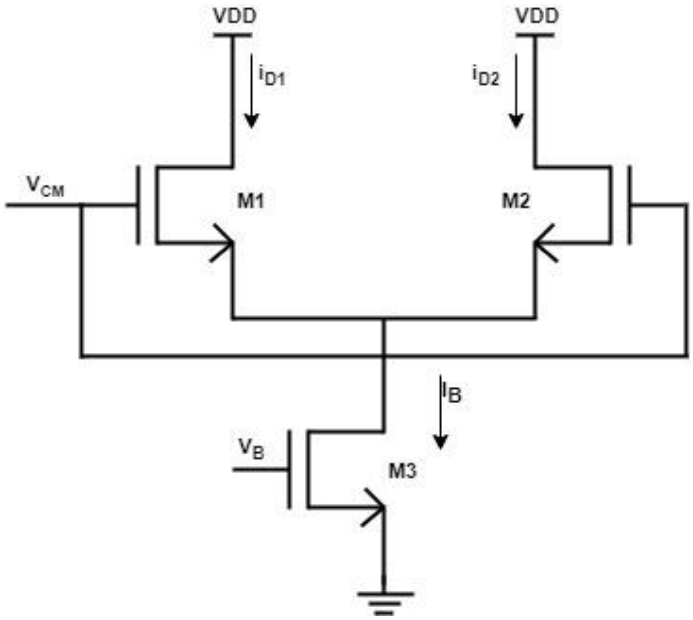


Figure 2.10 - Differential amplifier in a common-mode configuration

As discussed above, both M1 and M2 must remain in saturation for the operation of the amplifier in common mode configuration. The condition for that is as below

$$V_{DS} \geq V_{GS} - V_{TH} \rightarrow V_D \geq V_G - V_{TH} \quad 2.2.10$$

In this case since $V_D = VDD$, we can rewrite the above inequality to,

$$V_{CMMax} = VDD + V_{TH} \quad 2.2.11$$

where V_{CMMax} is the maximum common mode input voltage. According to equation 2.1.11, the differential pair will stay in saturation with a voltage even higher than VDD before M1 and M2 will move towards triode region operation. The minimum input voltage V_{CMMin} can be written as

$$V_{CMMin} = V_{GS1,2} + 2 \cdot V_{DS,sat} \quad 2.2.12$$

where $V_{DS,sat}$ is the minimum voltage across the current source transistor.

2.3 – Single Stage Differential Amplifier

The earlier section clarifies key operational characteristics of the differential pair, with a noteworthy emphasis on parameters such as the maximum and minimum common-mode input. An integral aspect for operational transconductance amplifiers (OTAs), specifically designed, is the differential gain of the amplifier. Let's delve into the single-stage amplifier illustrated in figure 2.11, featuring a differential pair as the input and a PMOS current mirror load. A significant attribute of this configuration is its ability to convert a differential input into a single-ended output, denoted as V_{out}.

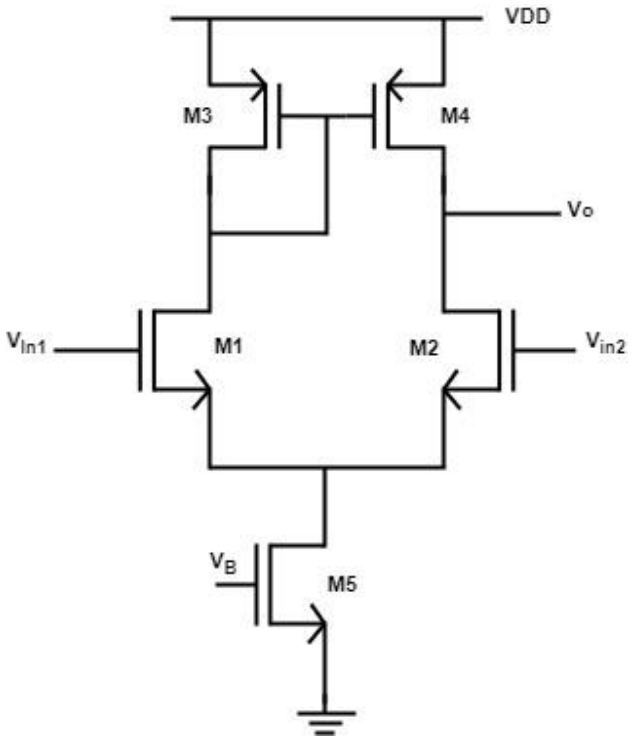


Figure 2.11 – Differential amplifier with current mirror load

2.3.1 – Large Signal Analysis

If V_{I1} is a lot more negative than V_{I2}, M1 will turn off which will cause M3 and M4 to turn off also. As current will not flow from VDD because of this, M2 and the bias current transistor M5 will operate in the triode region carrying zero current. This would mean V_{out} will be $0V$. As V_{I1} approaches V_{I2}, M1 will turn on and draw a part of the bias current. This will allow the PMOS current mirror to turn on. In this operating mode, the output voltage will depend on the

difference between I_{D4} and I_{D2}. When there is a small difference between V_{I1} and V_{I2}, M2 and M4 will both be saturated allowing the amplifier to operate in the high gain region (figure 2.12).

If V_{I1} becomes more positive than V_{I2}, the currents I_{D1} , I_{D3}, and I_{D4} will begin to rise, leading to a reduction in I_{D2}. Consequently, M4 will transition into the triode region. In the event that the voltage V_{I1} significantly exceeds V_{I2}, M2 will turn off, causing M4 to also turn off, resulting in zero current flow. As a result, V_{out} will be equal to V_{DD} .

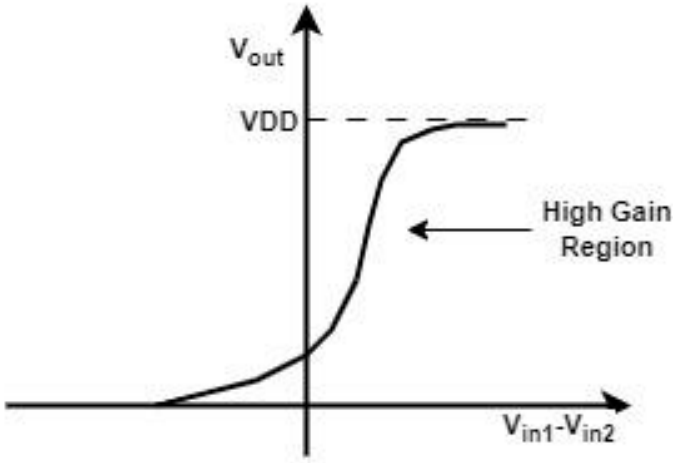


Figure 2.12 – Large signal input and output characteristics

The common-mode input voltage for the amplifier is also a crucial parameter that needs to be set in a precise manner. To allow for M2 to be saturated, the output voltage also cannot be less than $V_{IN,CM} - V_{TH}$. This means that to allow for the output swing (range of highest to lowest output voltage) to be as high as possible, the common-mode input voltage should be as low as possible. This is given by $V_{GS1,2} + V_{DS5,min}$. The main drawback of this circuit is the limitation that the input CM level has on the output swing.

2.3.2 – Small Signal Analysis

To determine the AC gain we must look at the small signal model of the differential amplifier as shown in figure 2.13. Notice the diode connected MOSFET M3 has been replaced with a $1/gm3$ resistor. This is because the voltage across M3 is $V_{sg3} = V_{sd3}$ and the AC current it is i_{d1} or

$$\frac{1}{g_m} = \frac{v_{sd}}{i_{d1}} = \frac{v_{sg}}{i_{d1}} \qquad 2.3.1$$

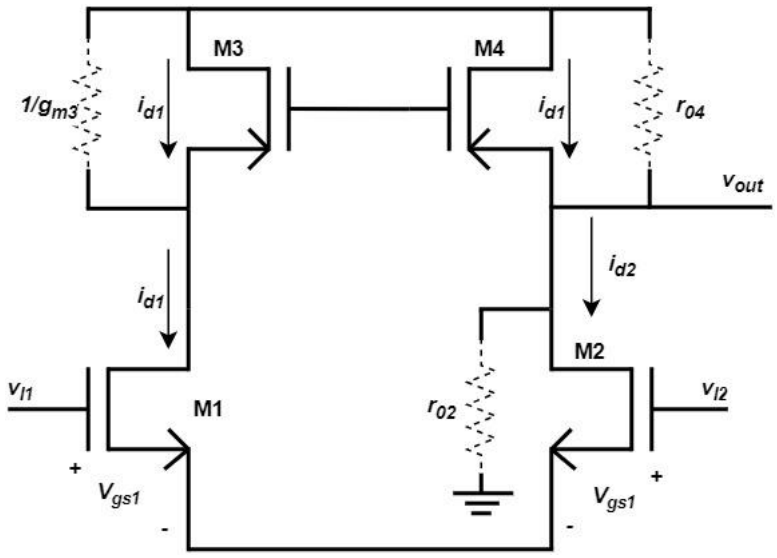


Figure 2.13 – Small Signal model of single stage differential amplifier with active current mirror load

A gate-drain tied MOSFET is always going to be in saturation when there's a current going through it, and the small signal resistance will always be represented as $1/g_m$. The resistance that is looking into the output node (drain of M4 and M2) and is represented by the r_{04} and r_{02} resistors respectively.

It's important to bear in mind that a negative AC current indicates a reduction in the total current, encompassing both its AC and DC components. Upon reviewing figure 2.13, it becomes evident that

$$i_{d1} = -i_{d2} = i_d \tag{2.3.2}$$

Due to the operating principles of the current mirror, the AC current flowing through M4 is i_{d1}. This is because current through M3 is mirrored to M4. Knowing this, the output voltage can be written as

$$v_{out} = (i_{d1} - i_{d2}) \cdot (r_{o2} || r_{04}) \tag{2.3.3}$$

Knowing equation (2.3.2), we can substitute it into equation 2.3.2 and get,

$$v_{out} = 2i_d \cdot (r_{02} || r_{04}) \tag{2.3.4}$$

Using the relationships derived above the differential mode gain A_d which in simple terms V_{out}/V_{in} can be expressed as,

$$A_d = \frac{v_{out}}{v_{di}} = \frac{v_{out}}{v_{i1} - v_{i2}} = -g_m \cdot (r_{02} || r_{04}) \tag{2.3.5}$$

An interesting behaviour of the circuit is that as the gate voltage of M1 increases, the current in M1 and thereby the current in M3 and M4 will also increase. This causes the output voltage to increase. When M2 gate voltage increases, so will its drain current which in turn will cause the output voltage to decrease [8]. This is one of the reasons why the gate input of M1 is known as the noninverting input and the gate voltage of M2 as the inverting input.

With a basic understanding of the differential amplifier being established, we can look at the different topologies of OTA that are most common in implementation along with their trade-offs.

2.4 – OTA Topologies

When designing an OTA, most designers will have more than one stage depending on the specifications that need to be met. Figure 2.14 shows the methodology behind multi-stage amplifiers.

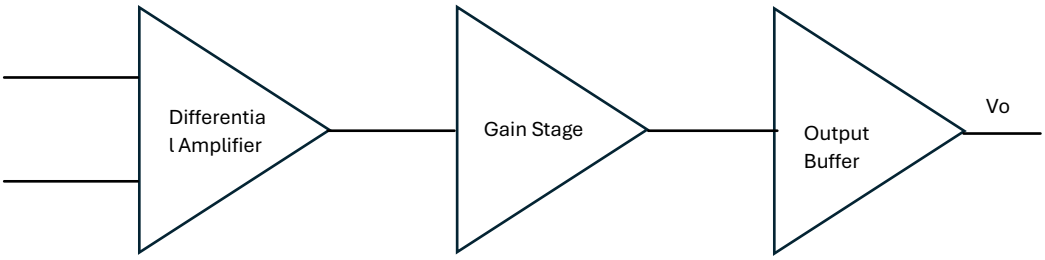


Figure 2.14 – Stages of an OTA

The differential amplifier is used as the input stage. This allows for the removal of any unwanted noise present within the signal that is common to both inputs. Since the OTA is mostly used in the feedback configuration, both terminals will carry the same voltage that may include noise artifacts being fed back into the system reducing the integrity of the signal being processed [5]. The first stage, however, won't provide the desired gain, so a second gain stage must be added. The second stage will provide that extra gain but will come with the trade-off of extra current consumption along with the extra area required [17]-[19]. The most common

topologies used for the gain stages are the common source, folded-cascode, telescopic, etc. [20] and each come with their advantages and disadvantages. The output buffer stage plays a crucial role in preventing the input impedance of one stage from loading into the output impedance of the next stage. This proactive measure helps avoid any unwanted signal loss. The output buffer, however, is only needed when the output load of the amplifier is resistive in nature. If the load is capacitive, the output buffer stage can be skipped. When looking at OTA topologies, several design parameters warrant careful consideration, as they significantly influence the overall operation of the amplifier. These design parameters along with a brief description are listed below.

- **Differential Gain**: Differential gain is the measure of an amplifier's ability to amplify the difference between the signals applied to its input terminals. The output can be observed either as single ended, or as differential. Measured in decibels, a high gain is essential in applications where only the differential signal needs to be amplified while rejecting any common signals present at both inputs. High differential gain for an amplifier is a very desirable parameter.
- **Common Mode Gain:** Common mode gain quantifies the amplifier's response to signals that are common to both input terminals. Ideally, the common mode gain should be as low as possible such that any common signal between the two inputs is amplified removed however in real amplifiers, common signals will be amplified to some extent. The amplification occurs as a result of discrepancies in tail current sources and variations between the transistors and resistors within the differential pair.
- **CMRR (Common Mode Rejection Ratio):** CMRR is parameter which quantifies the amplifier's ability to reject the common mode signals that are present at both input terminals. It represents the ratio of the differential gain to the common mode gain. A well-designed amplifier will have a high CMRR value indicating high differential gain and very low common mode gain. A higher CMRR value also is indicative of the amplifiers ability to reduce the noise that is amplified through the system keeping the signal clean. CMRR can be calculated by $CMRR = A_{DM}/A_{CM}$, in which A_{DM} is for the differential gain and A_{CM} is the common mode gain.
- **Slew Rate:** The maximum rate of change of the OTA's output is called the slew rate. It is specified by volts/microsecond $(V/\mu s)$ and is measured by applying a large step response to the input with the OTA in unity gain configuration. A high slew rate means that the OTA is very fast as it can reach the peak value very quickly.

- **Phase margin:** The phase difference between input and output will lead to oscillations if it becomes 180° in a closed loop configuration. High oscillations dictates that the amplifier is not stable. To understand the stability of the amplifier, the phase margin parameter is used. The phase margin is defined as the phase difference between 180° and the phase at the frequency at which the loop gain is $0dB$. This point is called the unity gain frequency. For phase margins above 60°, the step response of the feedback system shows very negligible ringing attaining a very fast settling time. Phase margins between $60° \; and \; 90°$ provide more stable systems, but the tradeoff with higher phase margins is slower settling times.
- **Bandwidth:** The OTA gain calculated at DC will not remain the same at higher frequencies as the operational frequency of the circuit increases as the gain decreases. The bandwidth is typically defined as the frequency range over which the output signal amplitude is within a certain level $(3dB)$ of the amplitude of the input signal.

2.4.1 – Differential Pair with a Common Source Amplifier

The two-stage OTA topology consists of a differential amplifier with a PMOS current mirror load as the first stage and a common source amplifier as the output gain stage as shown in figure 2.15. Transistors M5 and M2 act as the current sources for its own branch by copying the current for I_b.

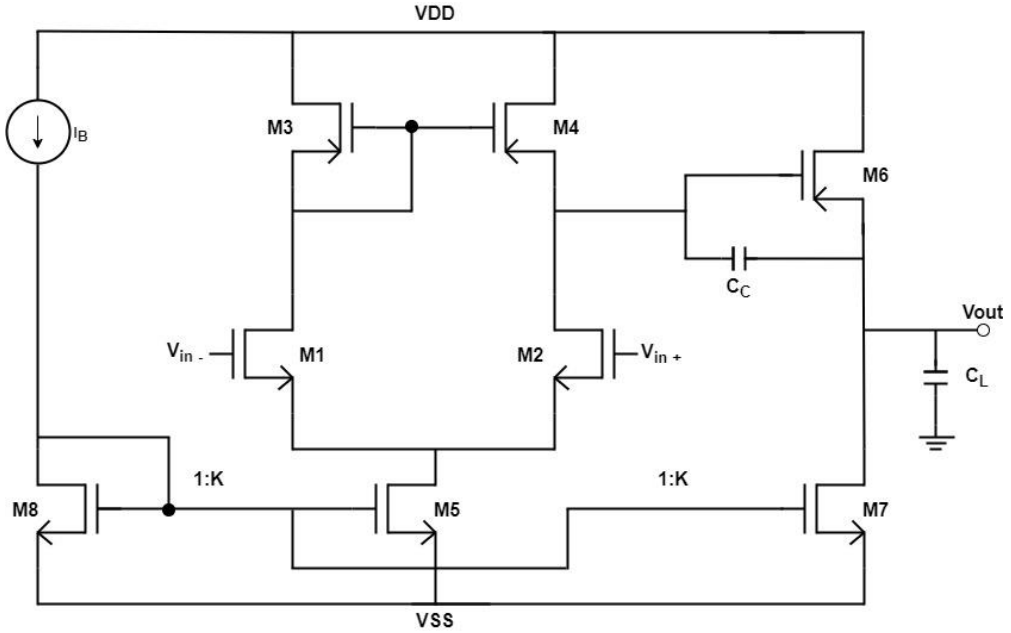


Figure 2.15 – Two – Stage OTA schematic

This topology has the advantage of providing high gain since the output gain stage only consists of 2 transistors. This means that the output swing can reach close to rail voltage as the maximum voltage is $V_{DD} - V_{TH,M6}$.

To determine the gain of the full two-stage OTA, it is known that

$$A_v = A_{d1} \cdot A_{d2} \tag{2.4.1}$$

Based on Eqn. (2.2.5) we know the differential gain of the first stage of the OTA is

$$A_{d1} = -g_{m4} \cdot (r_{02} || r_{04}) \tag{2.4.2}$$

The second stage differential follows the same method. The small signal model is shown in figure 2.16.

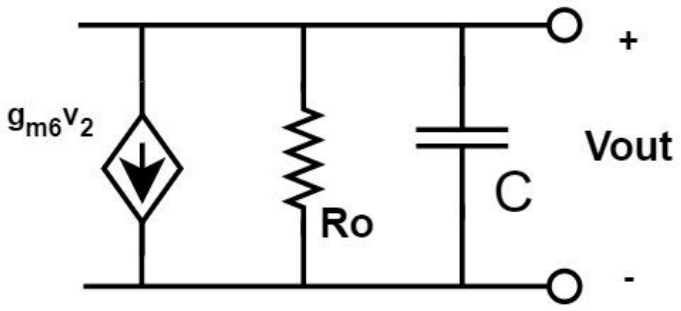


Figure 2.16 – Simplified small signal model of the second stage

In this case, R_{out} represents the total output resistance which is $r_{06}||r_{07}$. Therefore, by applying the principles used to calculate the first stage, the small signal gain of the second stage is,

$$\mathrm{A_{d2}} = -\mathrm{g}_{m6}(\mathrm{r_{06}}||\mathrm{r_{07}}) \tag{2.4.3}$$

Which makes the total AC gain of the two stage OTA

$$\mathrm{A_v} = -\mathrm{g_{m_4}g_{m_6}}(\mathrm{r_{02}}||\mathrm{r_{04}})(\mathrm{r_{06}}||\mathrm{r_{07}}) \tag{2.4.4}$$

Due to its elevated output resistance, the differential gain achievable with this topology can reach above 60dB [21] – [27]. Additionally, this configuration facilitates a high output swing, enabling it to operate near both power supply rails, often referred to as a rail-to-rail OTA [9]. An inherent drawback of this topology lies in its higher current consumption, which increases the overall power consumption [8], despite delivering high gain and near rail-to-rail operation. Nevertheless, reports indicate that similar gain can be achieved with low power consumption by biasing the transistors in the sub-threshold region [28],[29]. This mode of operation, though, presents several challenges, particularly in physical layout and manufacturing processes [8].

An alternative approach to mitigate power consumption involves implementing a bulk-driven input stage, where the input voltage is directed through the bulk of the transistor rather than the gate of the input differential pair [29]-[31]. These bulk driven OTAs find application in scenarios where the voltage supply is below $1V$ [30],[32], offering gains exceeding 50dB with minimal power consumption [32],[33]. However, this advantage comes with a trade-off, as accommodating different bulk potentials necessitates additional circuitry around the MOSFETs, significantly increasing the required area.

2.4.2 – Telescopic OTA

The single stage differential amplifier is a simple topology that exemplifies the operation of an OTA with some obvious limitations. One of the main limitations is the gain that comes from the single stage is not high enough while also showing large output noise [8]. These limitations can be overcome by increasing the number of transistors present in the stage by cascoding transistors on the input stage as well as the active current mirror as shown in figure 2.17.

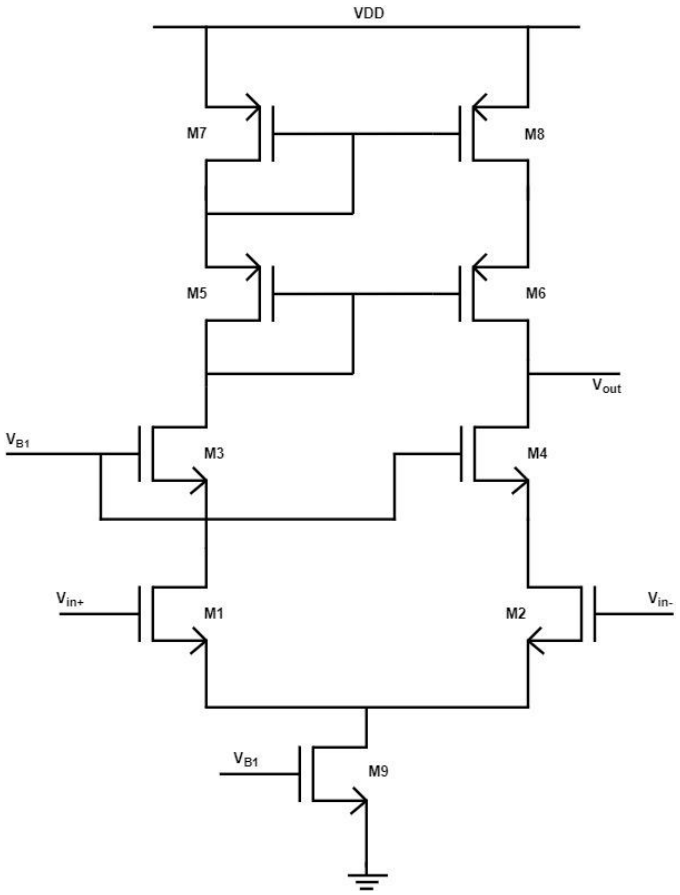


Figure 2.17 – Telescopic OTA schematic

Due to the cascading current mirrors, the output impedance increases which allows for a higher output differential gain [8],[9],[34] with upwards of 50dB having been reported [35]-[40]. Analysing the circuit above, the AC gain of the telescopic OTA can be written as

$$A_v = g_{m4}r_{04}r_{02}||g_{m6}r_{06}r_{08} \quad 2.4.5$$

The main drawback of adding cascading current mirrors is the reduction in the common mode range ultimately lowering the output swing [20]. The voltage headroom required to keep the cascaded current mirrors in saturation will limit the maximum common mode voltage hence it makes it a poor choice of amplifier for applications that need high voltage swing [35]. Another issue with this topology is that the linearity tends to decrease when it is operating in the feedback configuration [40].

This topology offers the advantage of typically having higher frequency capabilities while consuming less power [40]. Increasing gain is possible by adding multiple stages, but this comes at the expense of increased area and power consumption. Addressing the output swing issue, some designs incorporate body and gate connected PMOS transistors as the input differential pair [41]. This approach reduces the threshold voltage of the input pair, providing more voltage headroom for the output, while also ensuring that the transistors remain in saturation [41].

2.4.3 – Folded Cascode Amplifier

Figure 2.18 shows the typical structure of a folded cascode amplifier which is a single stage amplifier that contains a common source transistor in cascode with a common gate transistor with the opposite polarity. A differential pair is used as the input stage which acts as the common source of the cascode. The drains of the input pair are then connected to the opposite polarity common gate transistors which are then connected to the active current source [9]. This topology allows for the simplicity of a single stage amplifier while providing the gain of a multi-stage amplifier.

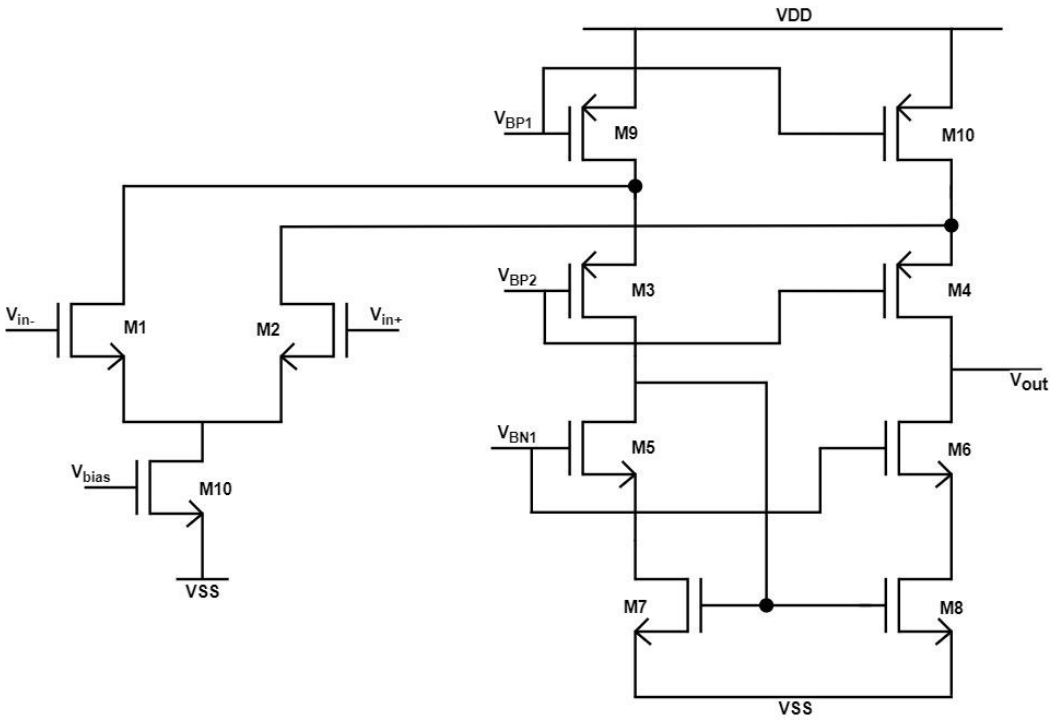


Figure 2.18 – Folded cascode amplifier circuit

The cascaded transistors are designed to give high output resistance which improves the overall gain of the amplifier higher than 60dB [42]-[48] Due to the folded cascode amplifier being a single stage OTA, it is inherently more stable than other multi-stage OTAs. While operating in saturation, the input common-mode voltage can be near the supply voltage while also providing a very high output swing [8],[42],[43] which is highly desirable.

Using our methodology from previous sections, we can see that the differential gain of the OTA presented in figure 2.11 is

$$A_v = g_{m04} r_{04} \cdot (r_{02} || r_{10}) || g_{m06} (r_{06} || r_{08}) \qquad 2.4.6$$

Due to the "folded" topology, an extra term is added to the output impedance thereby making it slightly smaller than that of the telescopic OTA. One drawback of this topology is that extra current consumption is required to keep the stages in saturation which accounts for higher power consumption [46]. This configuration also contributes to greater output noise which would make it harder to use to process signals with extremely small voltages [45].

Table 2.1 summarizes the properties of all the discussed OTA topologies and compares them to each other.

Table 2.1 – Comparison of OTA topologies

Topology	**Gain**	**Output Swing**	**Speed**	**Power Consumption**
Two – Stage	High	Highest	Low	Medium
Telescopic	Medium	Medium	Highest	Low
Folded Cascode	Medium	Medium	High	Medium

2.5 – Pseudo-Resistors

A resistor is a crucial passive element used in many ICs but comes with a huge disadvantage to the designer as it can take up significant but valuable silicon real estate if it is needed on chip. This is because the minimum doping level of silicon and polysilicon structures gives typical values of sheet resistance in the range from a few $\Omega/\square$ to a few $k\Omega/\square$ [49]. High value resistances would be then reached by very long resistors with many folds to allow for a more compact layout. Along with the large area, long resistors made with hundreds of squares introduce large parasitic capacitances that degrade their frequency operation and an increase in noise as frequency increases [49]. These disadvantages motivated the research of alternative solutions for high-value resistors based on circuit structures using transistors that exhibit the VI characteristics of a high value resistance while using a considerably smaller area than a resistor of equal value. This is now known as a pseudo-resistor.

To attain a pseudo-resistive element in a circuit, the resistors are replaced by a MOSFET transistor where the source and drain corresponds to the two terminals of the resistor and the drain current represents the current passing through the resistor [49-50]. A pseudo-resistor is a two terminal element whose current is a function of the differences in the pseudo-voltage across the two terminals. The pseudo-voltage is a non-linear function of the source and drain voltages at the terminals [49],[51].

A pseudo-resistance value is controlled by the gate voltage of the transistor as long as it is operating in the weak-inversion zone. Pseudo-resistors have demonstrated their effectiveness in many circuits such as Trans-impedance amplifier for high sensitivity current measurements down to fA [52]-[54].

Linear resistors are extremely area consuming in IC designs. Equivalent resistors can be implemented by using transistors however, the linearity range for this method is limited [52].

When $V_{GS} < V_{TH}$, a very small amount of drain current flows through the channel of the MOSFET. This current is called the subthreshold current and the region of operation is known as weak-inversion or the subthreshold region. [51]-[52] reported that a PMOS transistor in diode configuration can be used a pseudo-resistor with a very low current in the order of pA. The I-V characteristics of a PMOS device operating in the weak-inversion region is expressed as follows:

$$I_{SD} = I_{D0}\, e^{\frac{v_{BG}-v_{TH}}{nU_T}} \left(e^{-\frac{v_{BS}}{U_T}} - e^{-\frac{V_{BD}}{U_T}}\right) \quad 2.5.1$$

Where $I_{D0} = 2n\mu Cox\left(\frac{W}{Leff}\right)U_T$ (n is the subthreshold slope, Cox is the gate oxide capacitance per unit area, μ is the mobility, $U_T = \frac{kt}{q}$ is the thermal voltage, Leff is the effective length, W is width fo the transistor and V_{TH} is the threshold voltage of the transistor [51].

The equivalent resistance of the pseudo-resistor around $V_{AB} = 0V$ is then

$$r_{eq}|_{V_{AB=0}} = \left(\frac{\delta I_{SD}}{\delta V_{SD}}\right)^{-1} = \frac{V_{TH}}{I_{D0}} \quad 2.5.2$$

There are two types of pseudo-resistors that will be discussed in this section: tuneable pseudo-resistors, and non-tuneable pseudo-resistors. As the names suggests, the tuneable resistors are pseudo-resistors whose resistance can be controlled whereas non-tuneable pseudo-resistors are fixed in their resistances.

2.5.1 – Non-Tuneable Pseudo-Resistors

The most common way to implement a high value pseudo-resistor is to use a single PMOS transistor connected in a diode configuration as shown in figure 2.19. To use this as a pseudo-resistor with large bipolar signals, it is important to short the bulk and source/drain terminals of the MOSFET. This device will behave as a MOSFET for $V_{AB} = V_A - V_B < 0$ and as a diode for $V_{AB} > 0$ [52].

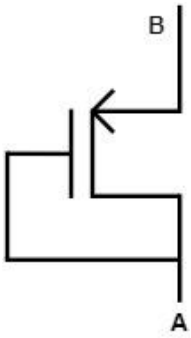


Figure 2.19 – PMOS in diode configuration

No conceptual difference would be present if an NMOS were to be used, however, due to the lower mobility of holes compared to electrons allowing for a higher effective resistance, the PMOS is preferred [50],[51]-[53]. This single cell pseudo-resistor is very compact but provides asymmetrical characteristics and shows linear behaviour only for very small signal ranges. To attain higher linearity while maintaining symmetry, multi cell implementations are more advantageous. Multi-cell implementation of the non-tuneable pseudo-resistors are shown in figure 2.20.

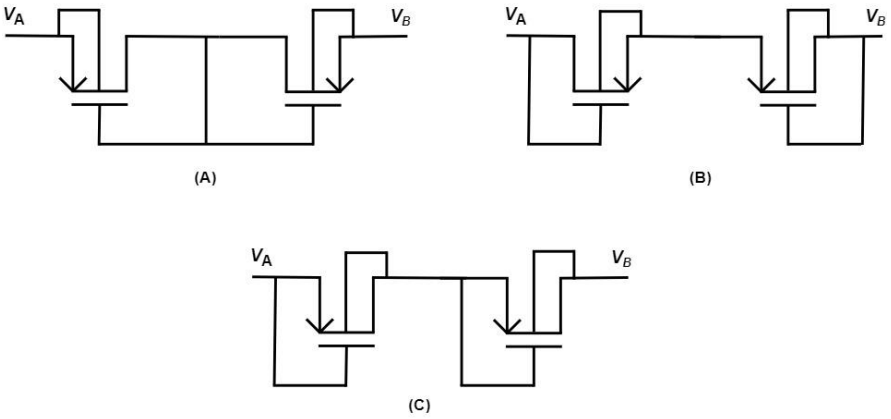


Figure 2.20 – Multi-cell non-tuneable pseudo-resistor structure: (a) Two series connected PMOS transistors in gate-drain connected diode configuration and source-connected bulks; (b) two series-connected PMOS transistors with a common source and gate-drain diode connection; (c) two regular series connected PMOS transistors

Due to the many drawbacks on the non-tuneable pseudo-resistor, it is uncommon for it to be implemented in many applications. They lack precision and accuracy compared to the other implementations. This can be a significant drawback with applications that require precise

resistance values. The more common implementations are of the tuneable pseudo-resistor as they provide more consistency in their resistance and a larger range of linearity [54],[55].

2.5.2 – Tuneable Pseudo-Resistor

Various structures can be employed for the implementation of tuneable pseudo-resistors. The first type involves using a voltage controlled MOSFET, illustrated in Figure 2.21 (a). This design is characterized by low parasitic capacitance and minimal added noise [54]. The equivalent resistance can be adjusted by varying the voltage V_{SG} of the transistor across positive and negative values. Achieving a high equivalent resistance with a suitable negative voltage result in very low leakage current, making the drain-bulk junction a dominant factor in the device and causing a resistance variation around the quiescent point [55]. To ensure symmetric resistance characteristics, the structure can be modified as depicted in Figure 2.21 (b).

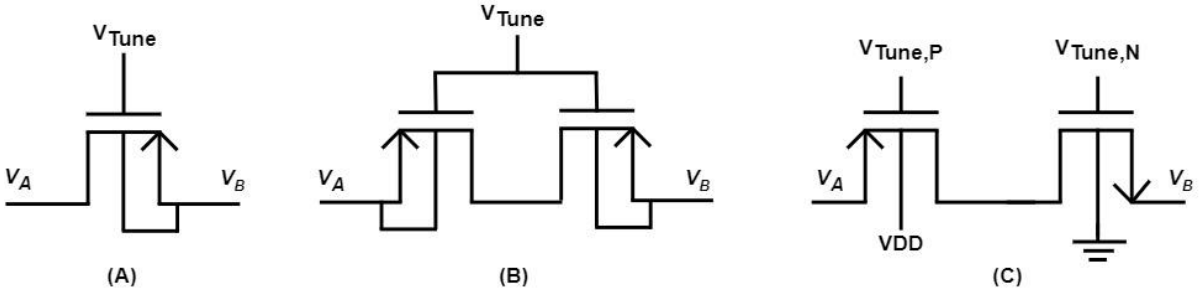


Figure 2.21 – Voltage controlled pseudo-resistor structures: (a) voltage controlled single MOS pseudo-resistor; (b) voltage-controlled series connected MOS pseudo-resistor structure; (c) CMOS voltage controlled pseudo-resistor structure

If the equivalent resistance is tuned to a moderate value by a small negative or slightly positive V_{SG}, the drain-source leakage current will affect the operation of the device resulting in asymmetrical resistance characteristics around the quiescent point [56]. Due to this, the resistance will experience large variations over the voltage swing range. The complementary scheme composed of a PMOS in series with an NMOS transistor is shown in figure 2.21 (c). It is more complicated than the other structures as each transistor needs to be separately tuned in order to achieve a symmetric variation around the quiescent point. This symmetry is also very sensitive to process variations. As such, even though resistors of this type have low parasitic capacitance, low added noise, and decent linearity, it would be difficult to use in applications where precise resistance values are necessary [56].

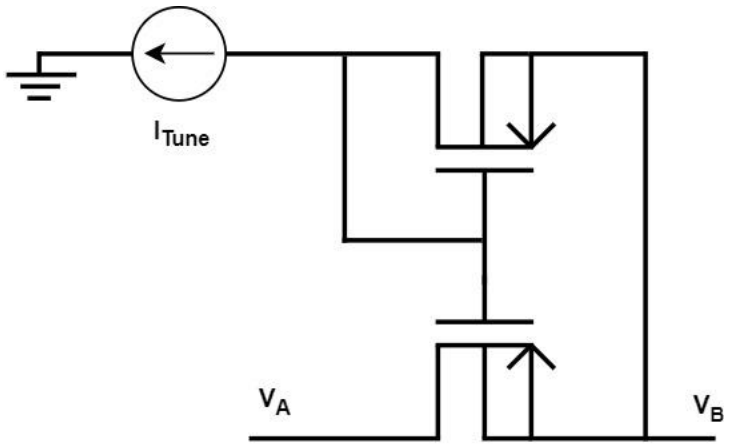


Figure 2.22 – Current Controlled Pseudo-Resistor

The next structure of tuneable pseudo-resistors is one that is current controlled rather than voltage controlled. The simplest implementation of this is shown in figure 2.22. This structure has low parasitic capacitance and low added noise. The resistance variations around the quiescent point, however, are not completely symmetric which leads to poor linearity. Linearity does improve for applied positive values of drain to source voltage [52].

In order to better control the operating point and provide a more linearly acting resistor [57] proposed the circuit in figure 2.23 in which uses a differential pair as an operating point control circuit for a standard voltage controlled pseudo-resistor circuit such as the one shown in figure 2.21 (b).

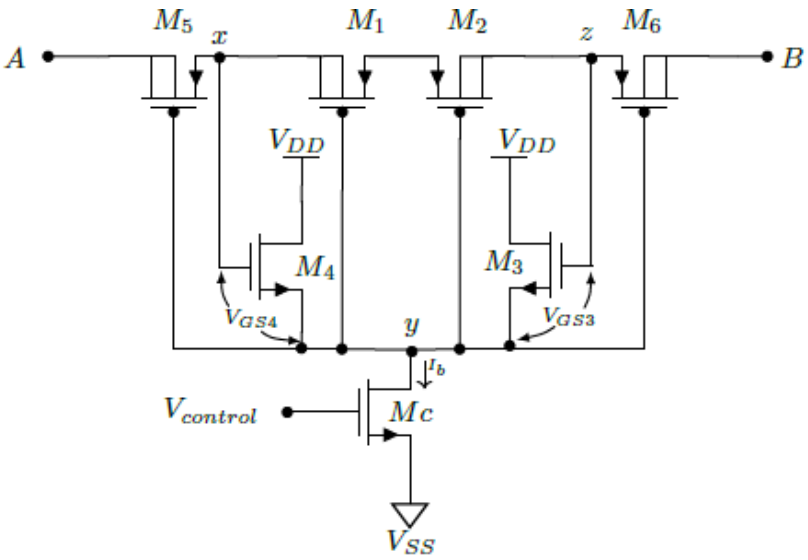


Figure 2.23 – Linear Current Controlled Pseudo-Resistor printed with permission from [57] (*Copyright © 2019, IEEE)*

Transistors M_5 and M_6 have been added to the ends of the resistor where in node y, the average of the voltages V_x and V_z minus the average of the differential pair voltages V_{GS} of M3 and M4.

$$V_y = \frac{V_x + V_z}{2} - \frac{V_{GS3} + V_{GS4}}{2} \quad 2.5.3$$

The M_C transistor acts as the current source which depends on the bias voltage at the gate. The closer the bias voltage is to the negative rail V_{SS} the lower the current through M_C and the voltages of $M_{GS3,4}$ will decrease. This will cause the resistances in transistors M1 and M2 will increase significantly [57]. This topology of the current controlled pseudo-resistor allows for a larger range of linear behaviour with high resistances but comes at the cost of having to use a negative supply rail which can be a trade-off worth taking in some applications.

Chapter 3 – OTA Design

3.1 – Design Requirements

The design of the OTA as well as all other circuit blocks were made using the TSMC 65nm technology node with power supply rails of $\pm 1.2V$. To make sure that the design of this OTA serves its purpose well in the larger system, it is important to know the overall structure of the VI converter. This allows us to better understand the inputs and outputs that can be expected from each stage of the VI converter, and what voltage and current ranges the OTA needs to be able to operate under. The design is based on figure 2.20 in which voltage attenuation occurs in the first stage, and the conversion occurs in the second. In the proposed VI converter, instead of attenuation, the voltage will be scaled such that the in the second stage the conversion will produce an output current that fits the desired output current range. Figure 3.1 shows the stages of the VI converter in which the OTA will be a major circuit component.

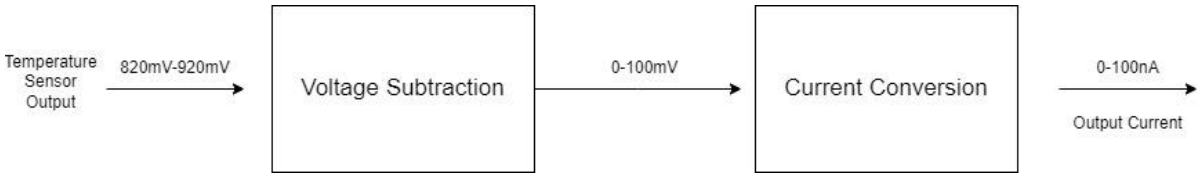


Figure 3.1 – VI converter block diagram

The temperature sensor output based on the expected body temperatures of 32°C to 42°C will produce a voltage of $820mV$ to $920mV$ as it has a $10mV/°C$ rating. The first stage of the VI converter which is the voltage subtractor will receive the output voltage of the temperature sensor as its input. The design specifications mentions that the AFE that follows the VI converter can read current from 0-$100nA$. As such, to make the conversion process simpler in the second stage, the temperature sensor voltage will be scaled to 0-$100mV$ via the voltage subtractor.

In the first stage, the OTA is required to facilitate the voltage scaling which will be done via voltage subtraction. The subtraction occurs with the use of four resistors in the feedback path of the OTA set in negative feedback. Based on the input and output required for the first stage, the OTA must have an operating range of up to $1V$ and down to $0V$. Using the first stage as a voltage subtractor was a crucial design decision. As discussed, since the output current range is from $0 - 100nA$, a very large resistance needs to be seen in the conversion stage. If the

voltage seen at the conversion stage is the same as the output voltage expected to be seen from the temperature sensor, the resistance needed to convert to the desired output current range would be $17.4M\Omega$ rather than the $1M\Omega$ needed with the voltage subtraction. Performing the voltage subtraction in stage 1 allows for a simpler design in stage 2 especially for the pseudo-resistor which will be discussed in the following chapter.

In the second stage, the OTA is required to process the signal from the first stage and act as a voltage follower circuit to allow for the voltage-to-current conversion.

Since the VI converter needs high precision conversion, the OTA must be able to operate at the higher voltage close to V_{DD} as well as the lower scaled voltage without being cutoff. This can only be achieved by designing a rail-to-rail OTA. In chapter 2, it is mentioned that rail-to-rail OTAs have very high swing and can reach very close to the power supply rails; although it is virtually impossible to reach the rails exactly as there will always be some cutoff due to device saturation. Under most cases, OTAs will operate with ground as V_{SS} and a positive voltage as V_{DD}. Since the first stage of the VI converter scales the voltage down to $0mV - 100mV$ it is important that the data close to $0mV$ does not get cutoff during the voltage subtraction. This portion of the data would represent temperature close to 32°C to 33°C. As such due to the expectation of slight voltage cutoff near the rails, it was decided that the power supply rails would be $\pm 1.2V$. The negative power supply is also needed for the pseudo-resistor in stage 2 and will be discussed further in Chapter 4.

One of the more important design specifications for the VI converter is that it must be low power. This means, since there will be two OTAs used in this design, the OTA power consumption must be kept as low as possible while also providing gain that is acceptable.

As discussed, the voltage ranges that the OTA must process span from close to V_{DD} and $0V$. This makes it crucial that the OTA can operate with very low distortion within those ranges. To achieve this, the OTA must have a very high output swing while also having very low total harmonic distortion (THD). With a low THD value, the distortion when the OTA is placed in unity gain configuration would allow for very precise and accurate voltage following.

Gain and THD are both functions of the frequency of operation of the OTA, so it is important to define the specifications regarding frequency. The VI converter is used to implement a temperature sensor used to track the core body temperature of the user. The core temperatures of the human body change gradually, so it's not essential for the OTA to perform optimally at

high frequencies. For this application, we will be operating at a frequency of 100Hz, allowing for temperature checks to be conducted a hundred times every second. This means that the required bandwidth for the designed OTA can remain low to help improve other parameters like power and area consumption.

3.2 – Proposed OTA Design

Based on the design requirements mentioned above, there are a few parameters that hold importance over others such as high output swing and very low power consumption. Based on table 2.1, the topology that best serves our purpose is the basic 2-stage OTA with a differential pair input stage and a common-source gain stage. The proposed OTA design can be seen in figure 3.2.

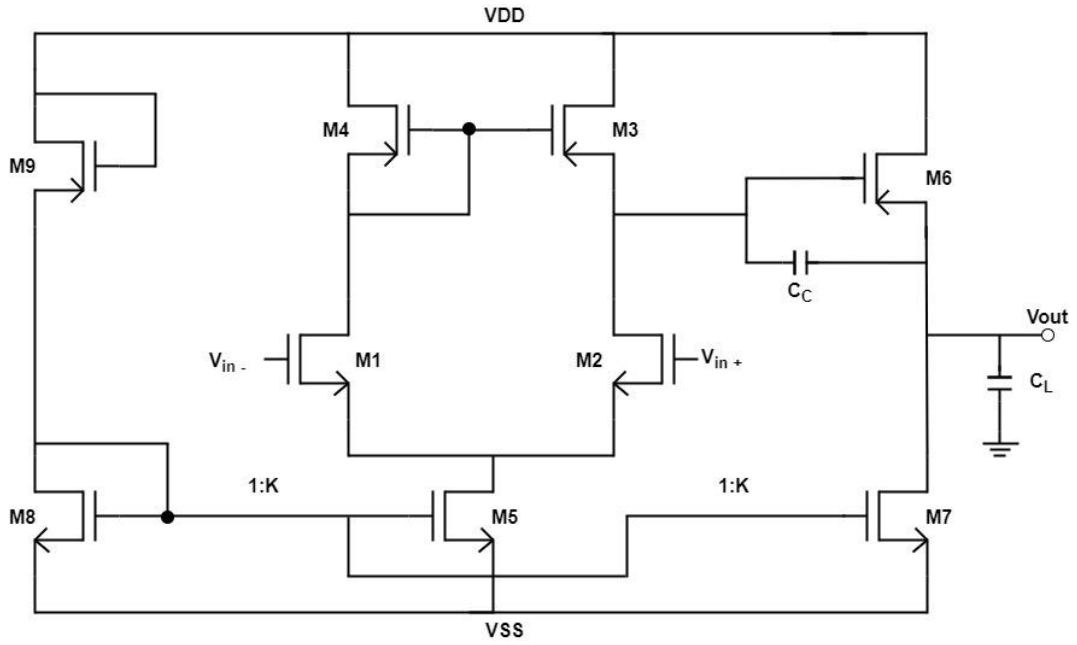


Figure 3.2 – Proposed 2-stage OTA design

To reduce overall power consumption of the OTA, it was decided to set the biasing points of the OTA such that each transistor operates in the subthreshold region. An NMOS will be in the subthreshold region when $V_{GS} < V_{TH}$, and a PMOS will be in the subthreshold region when $V_{SG} < V_{TH}$. Therefore, each biasing point needs to be carefully set to achieve this. In the proposed design the current for the OTA is sourced by M9 and mirrored to the different branches with its respective K value. Normally the current source is replaced by an NMOS in

diode configuration, but this comes with an issue of high bias currents. The only way to reduce the transistors drain current would be to increase the channel length significantly which increases the overall OTA area. This is due to the NMOS staying in the saturation region with higher W/L ratios which creates a larger drain to source current. To keep the OTA in the subthreshold region, a very low bias current is required. To implement this, as shown in figure 3.2, the current source is a PMOS in diode configuration while operating in the triode region which is given by $V_{DS} > (V_{GS} - V_{TH})$. Biased correctly, M9 will act as a very high value resistor and providing a bias current in the nA range which is suitable for subthreshold operation. The bias current was set as $115nA$, with the first and second stages of the OTA being biased at $1.25\mu A$ and $5\mu A$ respectively.

The first stage of this OTA determines parameters such as CMRR, slew rate, and other performance metrics. The second stage is an inverting amplifier whose purpose is to provide a very large voltage gain. Together, the input stage and the gain stage create two poles can create stability issues when the amplifier is in negative feedback. If unstable, the negative feedback turns positive, and the output can oscillate. As such, some form of compensation is required to keep the OTA stable at unity gain. The purpose is to reduce the gain magnitude to below unity at frequencies where instabilities may occur.

One way to check the amplifiers closed-loop stability is by way of the phase margin (PM) of the open loop response. The phase margin is determined by the phase shift perceived at the frequency where unity gain occurs (0dB). A low phase margin will cause oscillations in the step response which is undesirable. It is important for the stability of the OTA in closed loop performance to have an adequate phase margin, ideally above 60°. If the OTA is in unity gain configuration and a pulse wave is sent through as input, a low phase margin would create oscillations as the output tries to reach the peak value. A 60° phase margin effectively provides a dampening factor of 1 where there is no overshoot of the voltage.

A technique commonly used to increase the phase margin and provide more stability to the closed loop response is that of Miller compensation. In this technique, a capacitor is tied from the output to the input of the second gain stage. The small signal model with a compensation capacitor is shown below in figure 3.3.

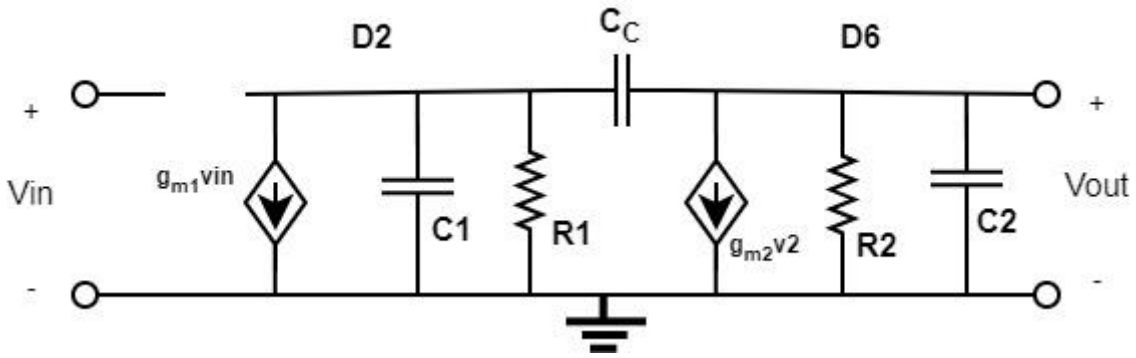


Figure 3.3 – Small signal model with compensation

The addition of the compensation capacitor (C_C) between the two stages produces two results. The first one being that the open loop pole location of p_1 is shifted closer to the origin of the complex frequency plane and p_2 is moved away from the complex frequency plane. A consequence of this, however, is that a zero appears in the RHP due to the feed-forward path through C_C. A well-known relationship that ensures the zero does no interfere with the stability of the system is $z = 10 * GBW$, where z is the frequency of the zero, and GBW is the gain bandwidth (unity gain frequency). Figure 3.4 shows the shifting of the dominant (p1) and non-dominant (p2) poles as well as the zero-placement due to the compensation capacitor. The resulting effect on the gain and phase bode plots is shown in figure 3.5.

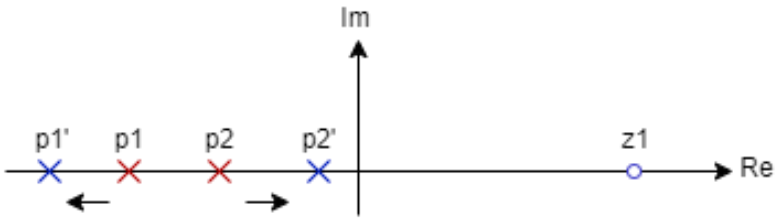


Figure 3.4 – Pole Splitting in the complex frequency plane

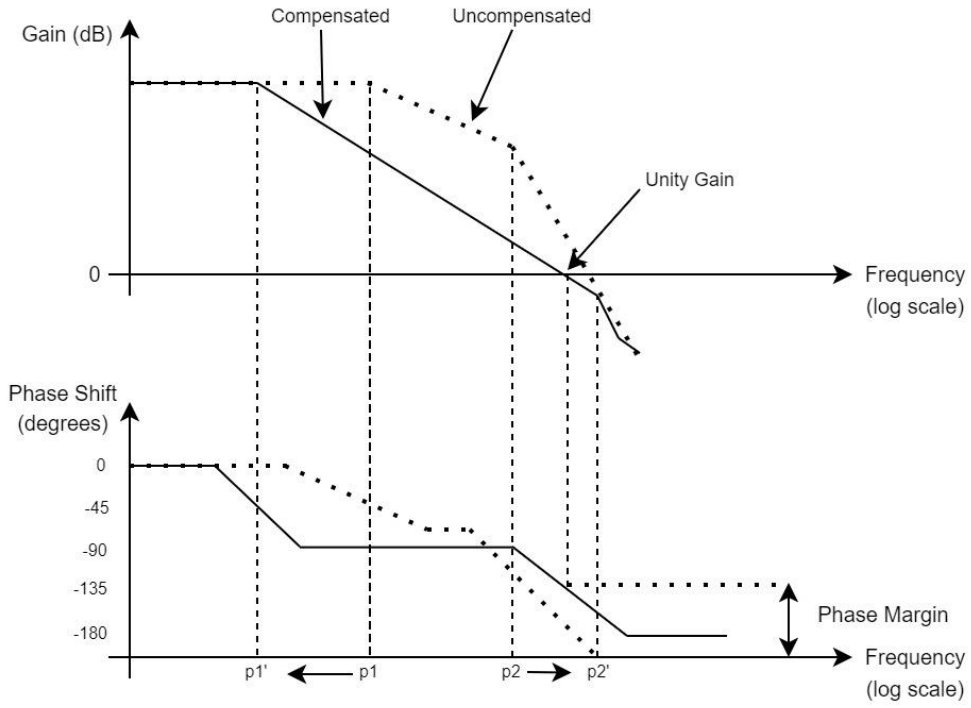


Figure 3.5 – Gain and phase plots with pole splitting

The dominant pole is moved to a lower frequency and the non-dominant pole is moved to a higher frequency which has a corresponding change in the phase shift plot. The general rule for deciding the C_C value is found by evaluating the transfer function of the OTA, but as it is widely known and documented it will not be derived in this chapter. To have a phase margin above 60°, it is commonly known that $C_C \geq 0.22C_L$. In this case, to achieve a high phase margin, the C_C needed to be much larger than C_L.

This OTA was designed specifically with the goal of the implementation of the VI converter in mind hence some of the specifications were deemed not as important as other. For example, the highest priorities were that of low power, high CMRR, V_{out} range and low area.

The transistors' aspect ratios were decided very carefully through the simulation of each parameter and carefully selecting the bias points required as per the specification. For the first stage, the transconductance of the input differential pair needs to be high enough. The PMOS active current mirror load also needs to provide a very high output impedance. This can be achieved by changing the W/L ratio of the input pair, as well as the PMOS current mirror pair. The gain achieved in the first stage output will not be very high, but it is crucial that the output signal is not distorted or cutoff near the power supply voltages. The second stage will provide the high gain with the common source amplifier. The current sourced by the NMOS current mirror determines where the output will be biased as well as provide high impedance to

improve gain. The PMOS amplifier would need to have a large aspect ratio to have a high enough transconductance value such that the desired gain can be achieved. The W/L values of the OTA are listed in table 3.1. Although the smallest length for the transistor can be 60nm in this technology node, it is common practice to use a channel length of at least $2 * L_{min}$. A large channel length also reduces the small channel lengths effects that causes distortion in the signal. As such a large channel length was selected for the transistors.

Table 3.1 – 2-stage OTA transistor sizes

Transistor	$\boldsymbol{W/L}$
M1	$3\mu/800n$
M2	$3\mu/800n$
M3	$5.5\mu/800n$
M4	$5.5\mu/800n$
M5	$1.6\mu/250n$
M6	$16.4\mu/800n$
M7	$6\mu/300n$
M8	$200\mu/800n$
M9	$4\mu/800n$

As discussed previously, it is very crucial for the stability of the OTA for it to have some form of compensation. Since the OTA will already have a load capacitor, adding a second capacitor for compensation can greatly increase the silicon area used up. As such, it was determined that very small capacitors will be used. The load capacitor was determined to be $100fF$. The selection of the compensation capacitor size will be discussed further in the next section.

The design requirements for the OTA are shown below in table 3.2.

Table 3.2 – OTA design specifications

Requirements	Specifications
Gain	$\geq 50dB$
Phase Margin	$\geq 60°$
C_L	100fF
CMRR	$\geq 85dB$
V_{out} Range	$\pm 1V$
THD Value	Minimum
Power Consumption	$\leq 20\ \mu W$

3.3 – Results

3.3.1– Simulation Results

The simulations performed for the OTA were done using Cadence software with the TSMC 65nm technology node. To measure the open loop gain, a $\pm 100\mu V$ sinusoidal differential input was given to the OTA and the AC response was measured at the output. The gain plot can be seen in figure 3.6. The gain measured at the frequency of operation of 100Hz is 49.9dB which effectively reaches the specification set. The trade-off between current consumption of the output branch and gain needed to be carefully managed. Since the second stage gain is heavily relied on the transconductance of the CS amplifier, we need to significantly increase the g_m value relative to that of the first stage amplifier. To accomplish this, the W/L of M6 already needs to be large enough to support that. However, since g_m is directly proportional to I_D, an increase in the transconductance would result in the increase of the drain current. Another trade-off with an increase in the gain would be that M6 would need to have a larger aspect ratio achieved by increasing the size of the transistor significantly which goes against the overall design specification of the VI converter. As such, to stay within the OTA, and VI converter specifications, the gain was not increased further.

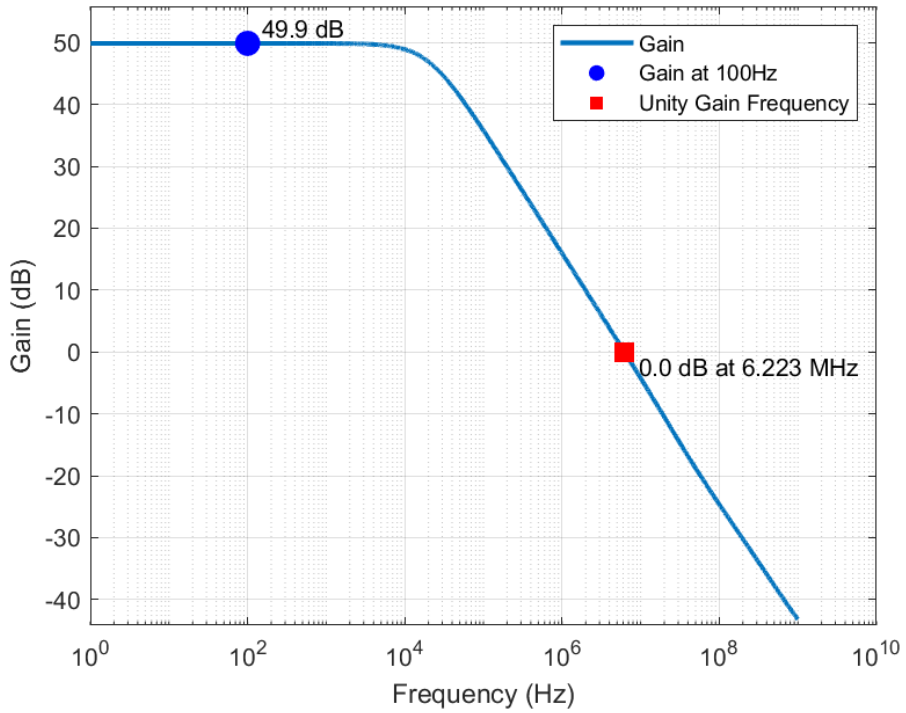


Figure 3.6 – Open-loop gain plot

The unity gain frequency which depicts the frequency at which the gain of the OTA is 0dB is found to be 6.223MHz. Based on the frequency response of the OTA, it is evident that the stability in closed-loop analysis will be good. After the dominant pole around 10KHz, the gain declines at a rate of 20dB/dec until after the unity gain frequency. This means that with compensation, a frequency response that resembles a single pole system has been achieved. This is further clarified through the phase margin plot shown in figure 3.7.

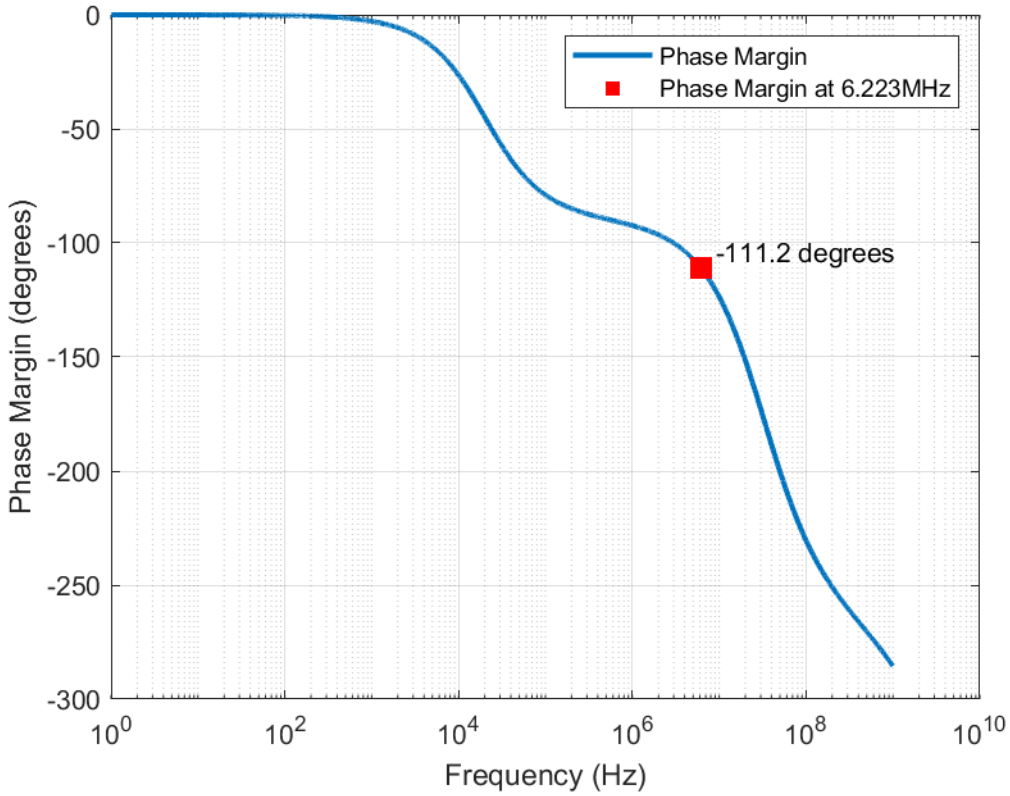


Figure 3.7 – Phase margin plot

The compensation capacitor chosen for the design was $400fF$. To have a properly damped system, the phase margin should be greater than 60°. To determine the phase margin from the plot above, the phase margin at the unity gain frequency (6.223MHz) must be subtracted from -180°. In this case, since the phase margin at unity gain is -111.2°, the phase margin of the OTA in open loop would be 68.8° which is very desirable.

Although the compensation capacitor value can be determined through relation mentioned previously $C_C > 0.22C_L$, to attain a favourable phase margin that would provide stability, different values of the compensation capacitor were tested. With lower values, the dominant pole moved further out and towards the non-dominant pole decreasing the phase margin. With values larger than the load capacitor, the dominant pole moved further away from the non-dominant pole and was able to stabilize the frequency response with higher phase margins. There is a clear trade-off between the phase margin and the compensation capacitor size which was managed as needed.

To test the common-mode gain, the same signal was passed into both input terminals and the response at the output was noted. In the log scale, since the gain can never be 0, the more

negative that gain, the better the OTA is at rejecting the common signals in both input terminals. As seen in figure 3.8, the common-mode gain is found to be -39.4dB.

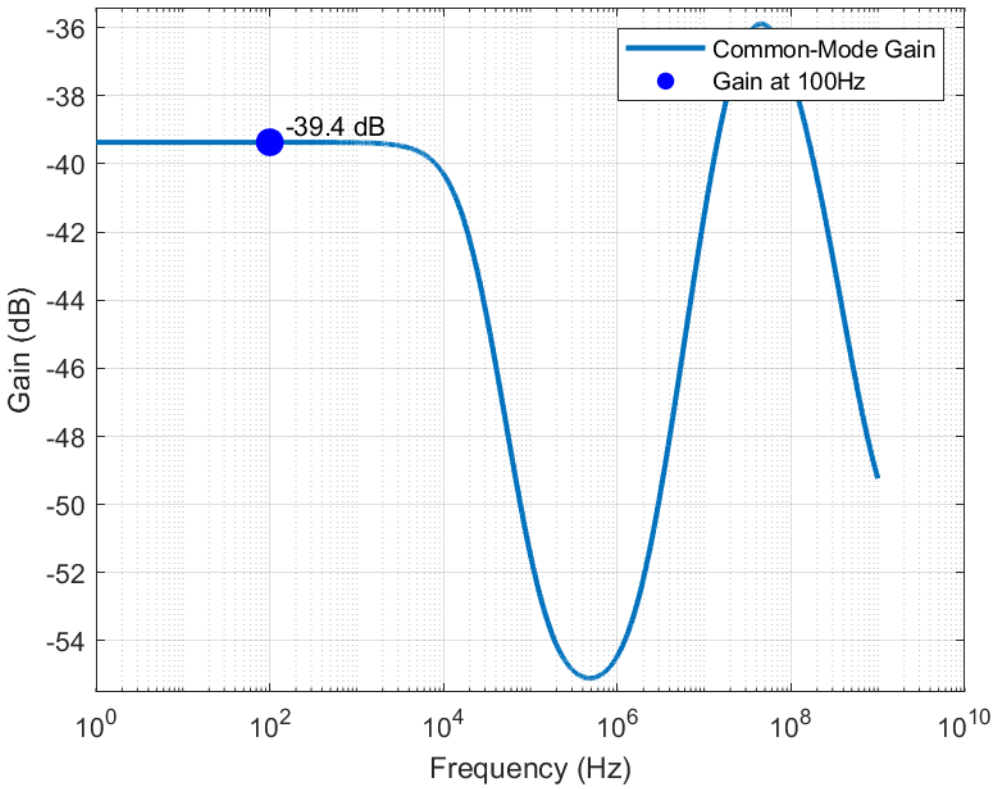


Figure 3.8 – Common-mode gain plot

The CMRR can be calculated by the equation $CMRR = A_d/A_{cm}$, where A_d and A_{cm} are the differential and common-mode gain in V/V. The calculated differential gain is 89dB which meets specification.

To measure the output swing, the OTA was placed in unity gain configuration with the output tied to the negative input terminal. The positive input terminal had a voltage varying from -1.2V to +1.2V. The results can be seen in figure 3.9. Notice that for much of the voltage range between the rails, the OTA can follow very well. There is some cutoff however near the negative and positive supply rail. The OTA performs well within the voltage range as required by the temperature sensor processing and the voltage subtractor.

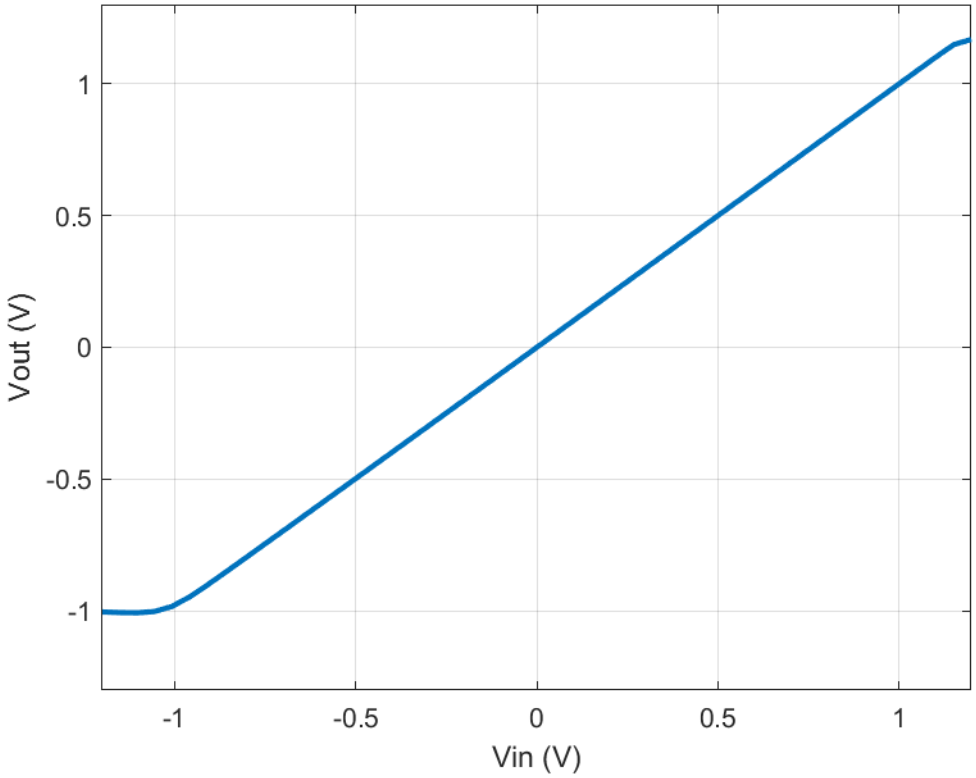


Figure 3.9 – Output voltage swing

Although in the overall VI converter design, the slew rate is not as important as other parameters, it can attest to the overall performance of the OTA. To test for the slew rate, an input pulse of 1.2V was given to the positive terminal while the OTA was in unity gain configuration and the output was observed as shown in figure 3.10. The slew rate was calculated to be 5.08V/μs. Notice the response when the voltage reaches its peak value. Due to the correctly placed poles and $> 60°$ phase margin, there is no overshoot or oscillation, and the response is stable.

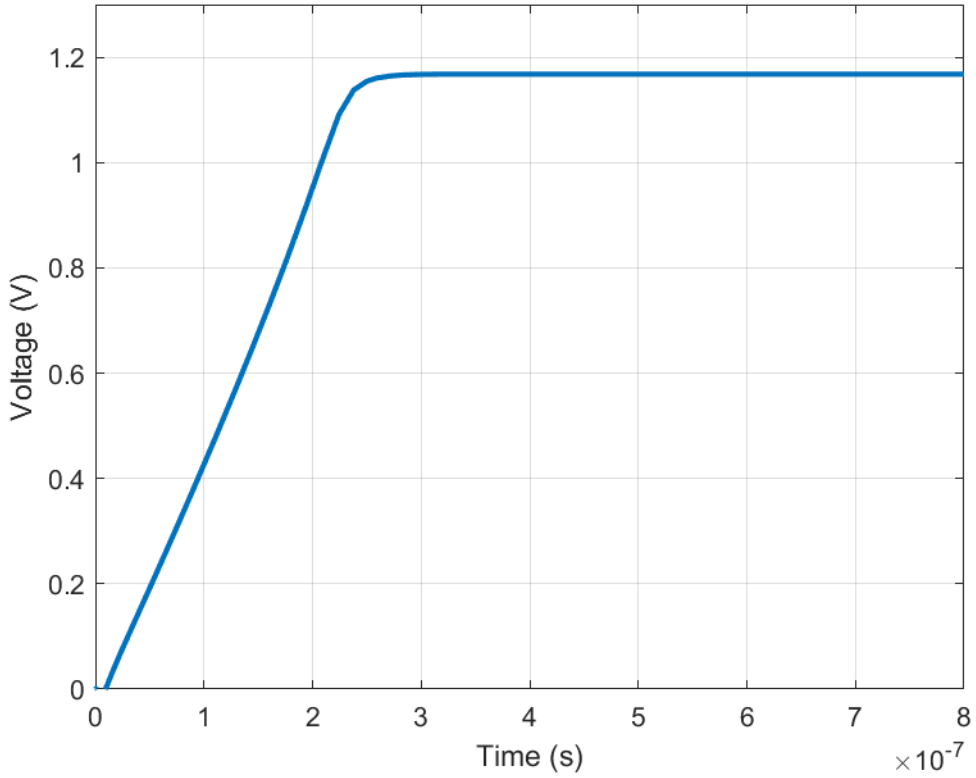


Figure 3-10 – Voltage response of input pulse

3.3.2 – Post-Layout Results

The layout of the OTA was accomplished using the Cadence tool with the TSMC65nm technology kit. After completing the layout, design rule checks (DRC) and layout vs schematics (LVS) checks were made such that all rules were followed as given by the foundry. Parasitic extraction was performed after which with no issues, the post layout performance of the OTA could be tested. The layout of the OTA can be seen in figure 3.11.

Notice the PMOS transistors are surrounded by an N-Well guard ring. This due to the subthreshold region operation of the transistors. It was found that if left without the guard rings, the leakage current from the PMOS transistors would cause performance degradation and cause a big difference between schematic and post-layout simulation results. This issue only seemed to affect the PMOS transistors which is why the NMOS transistors are without guard rings.

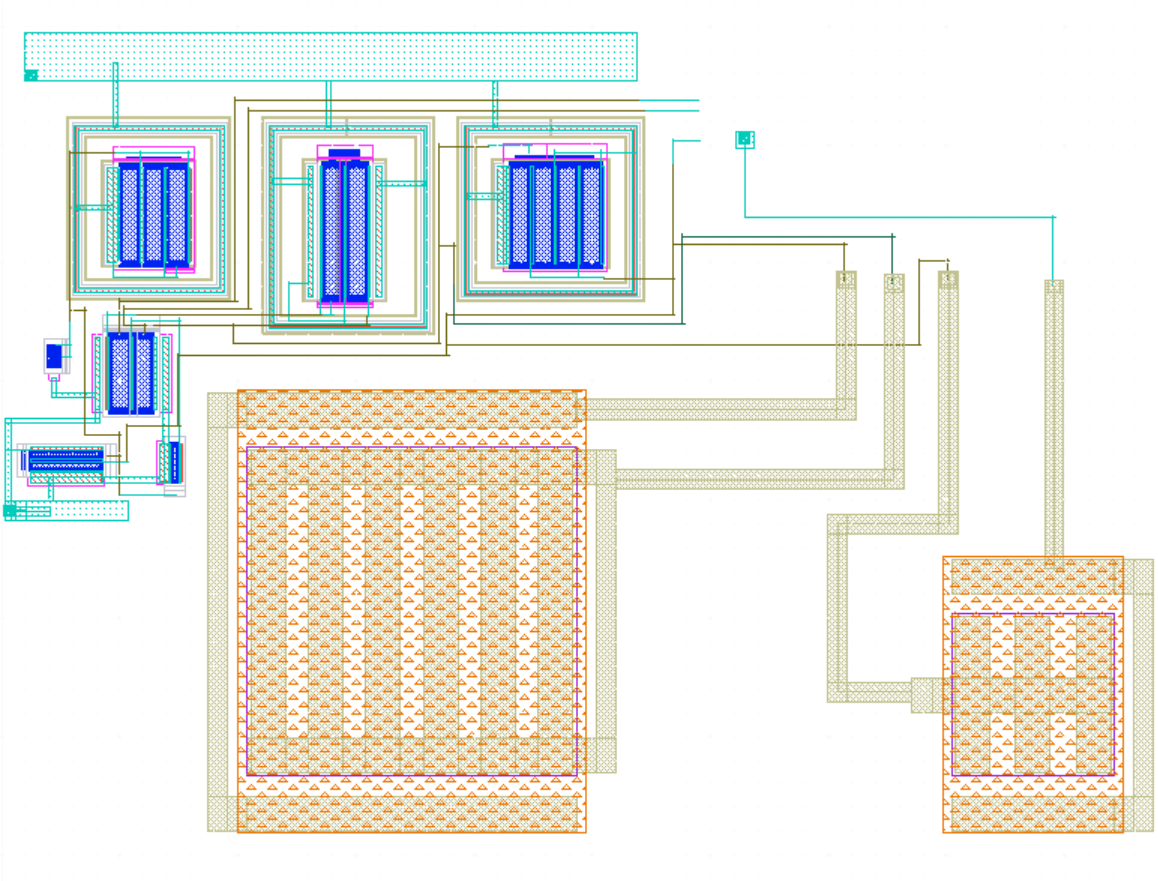


Figure 3.11 – 2-stage OTA layout

In post-layout simulations, the performance of the OTA matches quite well with that of the schematic simulations. Figure 3.12 shows the gain and phase plot of the OTA based on the layout. The gain is found to be 50.5dB and the unity gain frequency is 6.501MHz which are both higher than in the schematic simulations. The phase margin is found to be 66°, which is a little lower that schematic simulations but would not affect OTA performance in any significant way.

Figure 3.13 compares the step responses of the two simulations. The post-layout simulation shows that the step response arrives at the peak value earlier than that of the schematic simulation. Even though there was a decline in the phase margin, there is still no visible oscillations when approaching the peak value which was as expected. Since the post-layout pulse wave reaches the peak value sooner, the slew rate is slightly higher than that of the schematic simulation. The improved slew rate is 5.15$\mu V/s$.

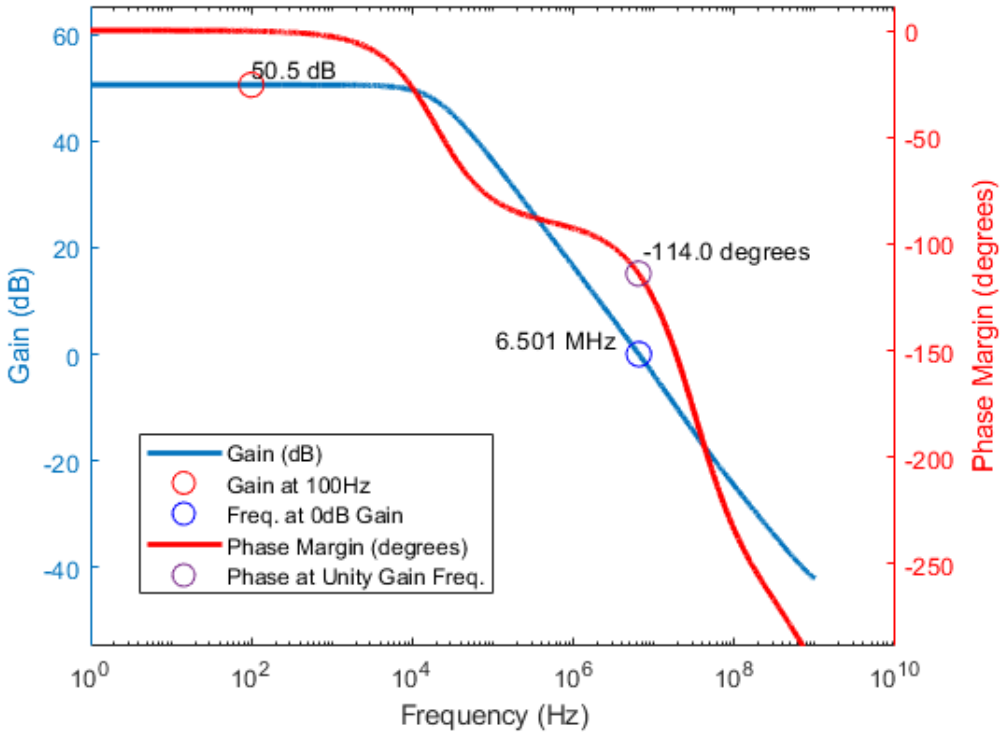


Figure 3.12 – Post-layout gain and phase plot

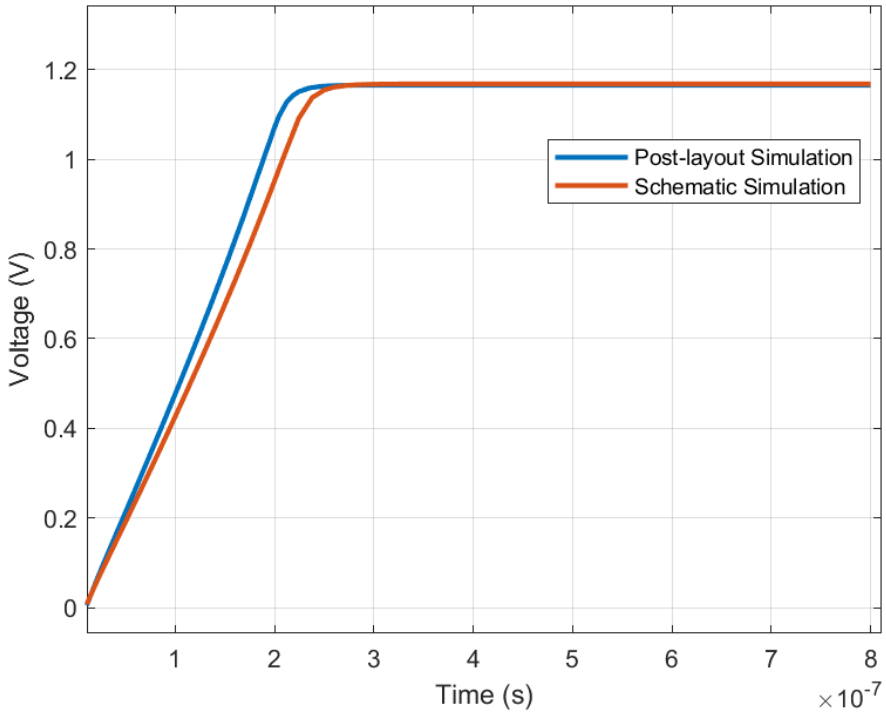


Figure 3.13 – Step response comparison of schematic and post-layout simulation

The output voltage range of the OTA post-layout follows the simulation results almost perfectly as seen in figure 3.14. The two curves fully overlap showing no significant performance loss after extraction.

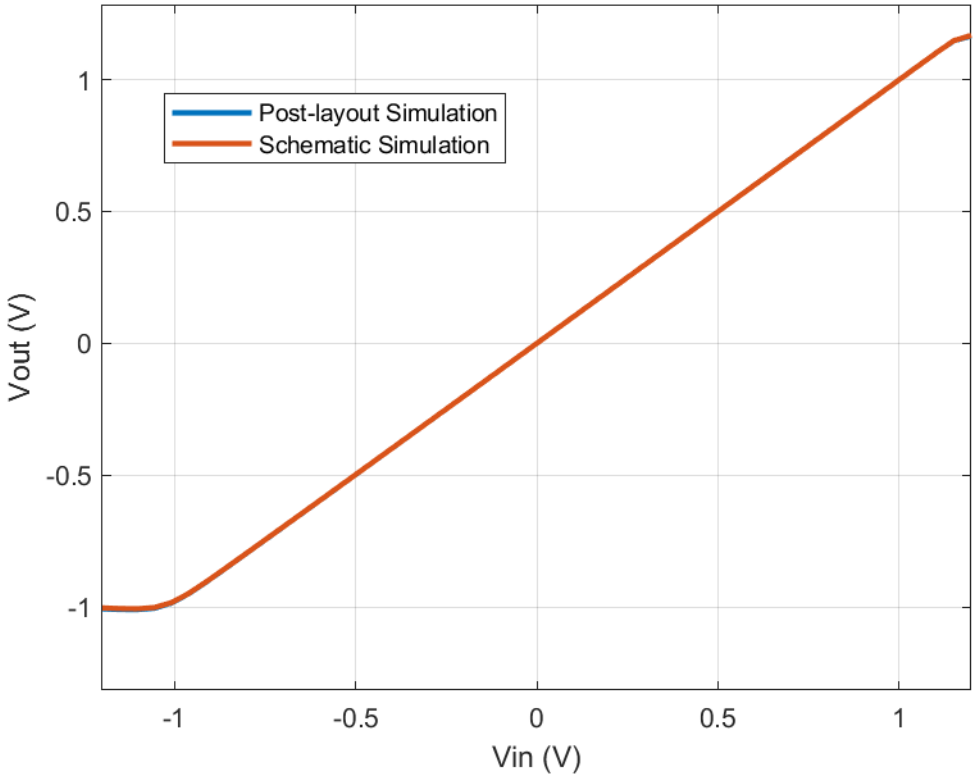


Figure 3.14 – Schematic vs post-layout of voltage output range

Another important aspect of IC design is to test the process corners to make sure that when fabricated, if the chip falls into any of the corners that is not typical, there is very minimal performance loss. Figure 3.15 shows the process corner testing of the OTA. Notice the overlap of all the corners at frequencies below 1KHz, meaning there is very minimal variation in the differential gain through the corners. The variations can be noticed in the unity gain frequencies, however slight variations as such offer no consequences to the overall performance of the OTA seeing as the unity gain frequency has no set specification.

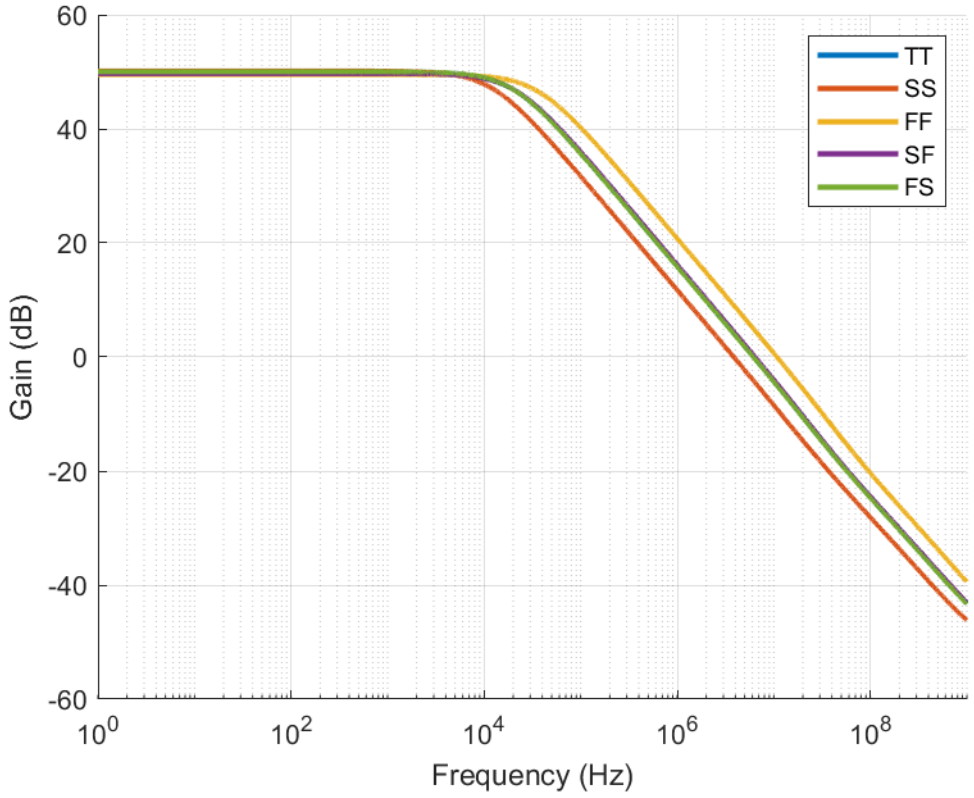


Figure 3.15 –Process corners testing

3.4 – Results Summary

The 2-stage OTA designed to be used in both stages of the VI converter reaches the specifications needed for the correct operation of each stage. It achieves the desired specifications for gain, phase margin, output range, etc. The area of the OTA is 48.76μm x 33.8μm. The summary of specifications can be seen in table 3.3. The power dissipation seems higher than originally expected, but this is due there be two power sources, the $\pm 1.2V$. The positive and negative rails were essential for the OTA and overall operation of the VI converter; hence the power dissipation is higher than desired but still low enough that the overall power dissipation of the VI converter would be very large.

Table 3.3 – Summary of results

Requirements	**Specifications**	**Schematic**	**Layout**
Gain	$50dB$	$49.8dB$	$50.5dB$
Phase	$\geq 60°$	68.8°	66°
CMRR	$\geq 85dB$	$89.3dB$	$90.1dB$
V_{out} Range	$\pm 1V$	$2.18V$	$2.18V$
GBW	$\geq 4MHz$	$6.223MHz$	$6.501MHz$
THD	Minimum	$-39dB$	$-39dB$
Power Consumption	$\leq 20\mu W$	$15.2\mu W$	$15.8\mu W$
Area	Minimum	-	$0.0249mm^2$

Chapter 4 – Pseudo-Resistor Design

4.1 – Design Specifications

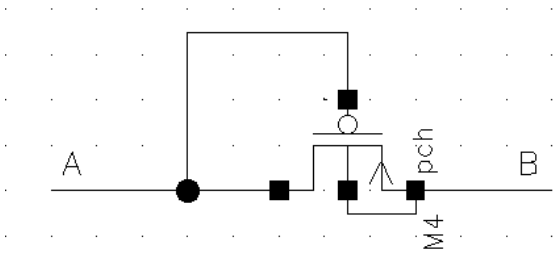
The pseudo-resistor is one of the most important blocks of the VI converter as it provides the precise voltage to current conversion for the design. The design specification is such that the pseudo-resistor needs to perform as a very specific high valued resistor for a small operating range. As a pseudo-resistor in nature is limited in its linearity, this may pose as a problem. The design specifications for the pseudo-resistor are as follows:

- High Linearity between $0mV - 100mV$
- Act as a $1M\Omega$ resistor for the entirety of the required range
- Low PVT Variations
- Low power consumption
- Low area

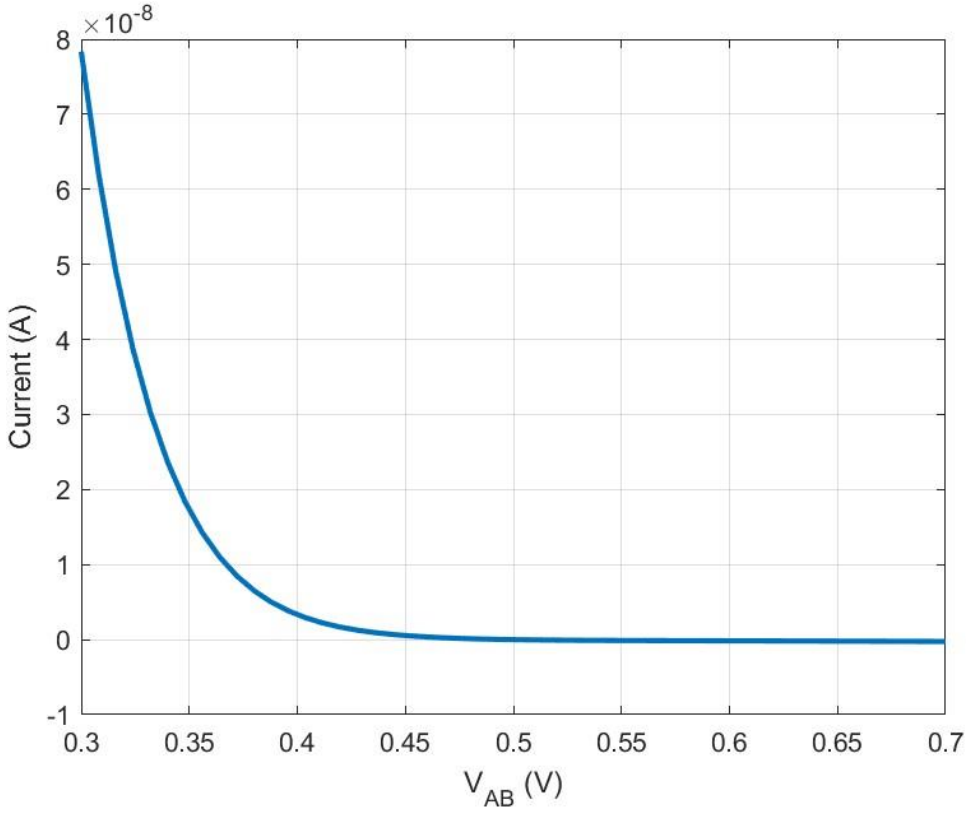
4.2 – Improving Linearity

In the pseudo-resistor designs, the transistors are operating in the sub-threshold region due to which exists a dependence of drain, source, and gate voltages with regards to the drain current. This relationship is shown in equation 2.4.1.

For small voltages of V_{SG} and V_{DG}, the transistor current can reach values in the pico-ampere and nano-ampere. This is due to the inversion layer in the channel not fully generating as the applied voltage to the transistor does not exceed the threshold voltage, thus not allowing it to reach saturation. The relationship with regards to the subthreshold operation is $V_{SG} \leq V_{TH}$ for the PMOS transistor. When the source-gate voltage is below the threshold voltage of the PMOS, there are not enough carriers to allow for proper current flow, only allowing leakage current. Due to the exponential dependence shown in equation 2.4.1, the channel resistance increases drastically as the potential difference between V_{SG} and V_{DG} decreases. As such, the channel can be considered highly resistive. A single cell PMOS pseudo-resistor is highly non-linear and due to the V_{SG} not being constant, cannot provide a behaviour that resembles that of a passive resistor in any range.



a)



b)

Figure 4.1 – a) Test circuit for a single cell PMOS pseudo-resistor, b) I-V characteristics with respect to a varying drain voltage

Figure 4.1 (a) shows the test circuit of a single-cell PMOS pseudo-resistor and (b) shows the $I-V$ characteristics where node A has a varying voltage from $300mV$ to $700mV$ and node B is set to $500mV$. The drain current curve starts decaying almost right away and then flattens when node A is at $500mV$. In this case, V_{AB} is 0, hence there is no current flowing through the circuit which can be seen in the $I-V$ curve. As previously discussed, there is no linear relationship between the potential difference of node A and B and the current passing through the single-cell pseudo-resistor. The W/L ratio was arbitrarily set to $1\mu m/200nm$.

Due to the high non-linearity, other topologies of pseudo-resistors have been tested, such as a common one shown in figure 4.2.

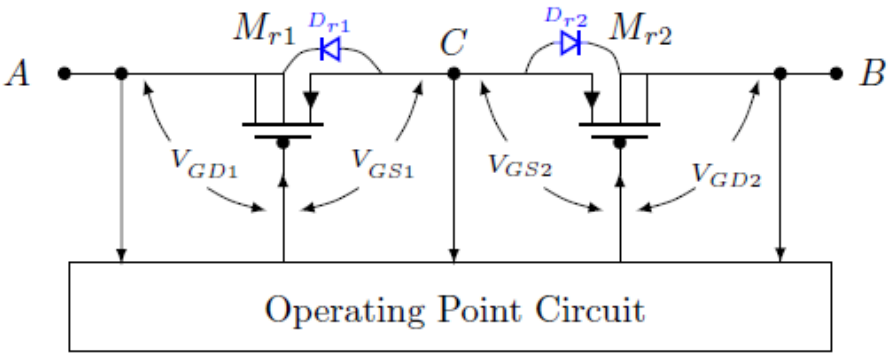
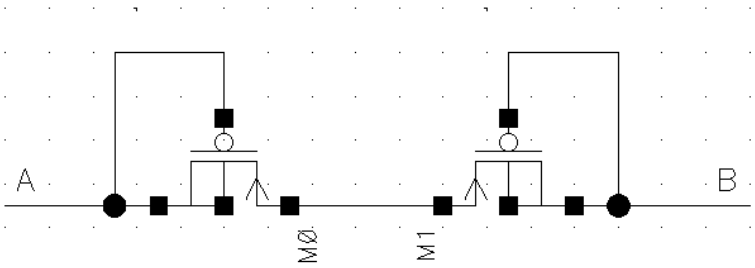


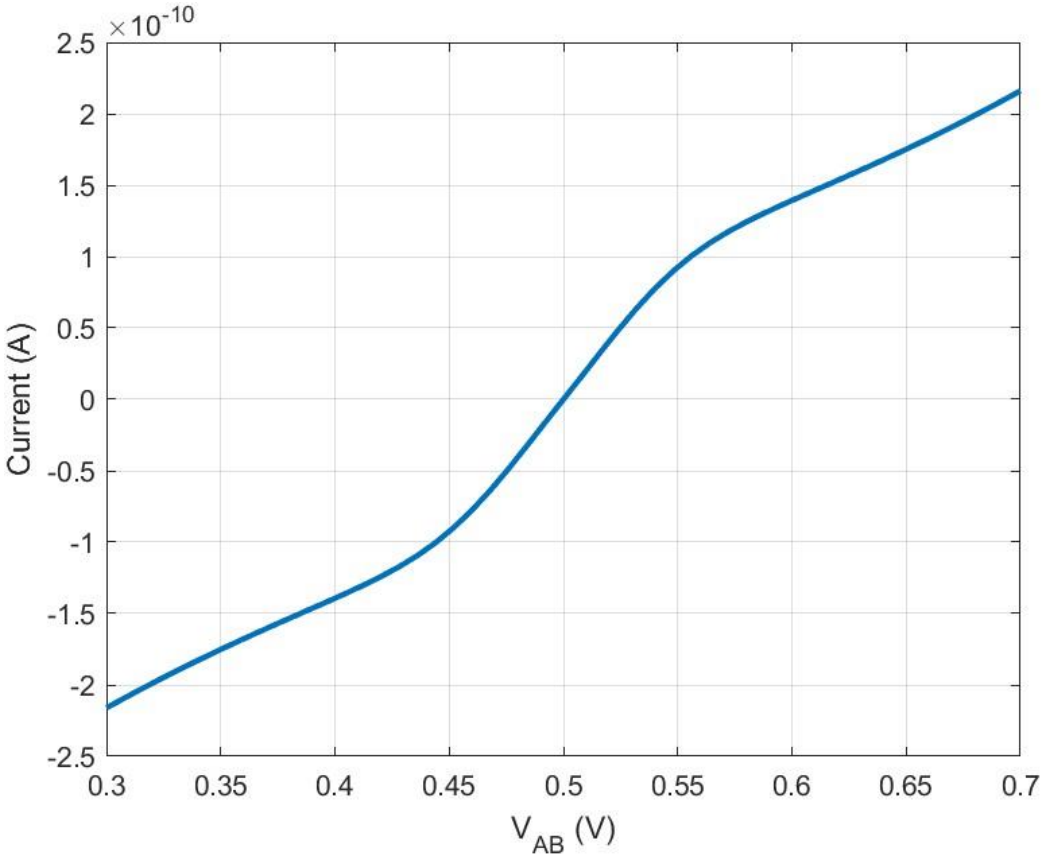
Figure 4.2 – Series pseudo-resistor with variable V_{GS}

In this topology, the two-diode connected PMOS transistors are connected in series with their N-Well connected to the output terminals (Node A and Node B). This gives symmetry to the pseudo-resistor allowing the resistance seen from A and B to be the same. Conversely, between the nodes C-A, and C-B, there exists two parasitic diodes D_{r1} *and* D_{r2} respectively. In the case when node A is very positive with respect to node B, D_{r2} is turned on, and D_{r1} is reverse biased and the reverse is true when node B is more positive than node A. In this manner, both diodes will never be turned on at the same time and only one diode will exhibit high resistance at a time.

To keep the transistors operating in the sub-threshold region and exhibiting a high resistance, an important aspect of the circuit is the supplementary circuit which sets the operating point of the resistive transistors. The supplementary circuit can be as simple as a diode connection to node A and B as shown in figure 4.3 a).



a)



b)

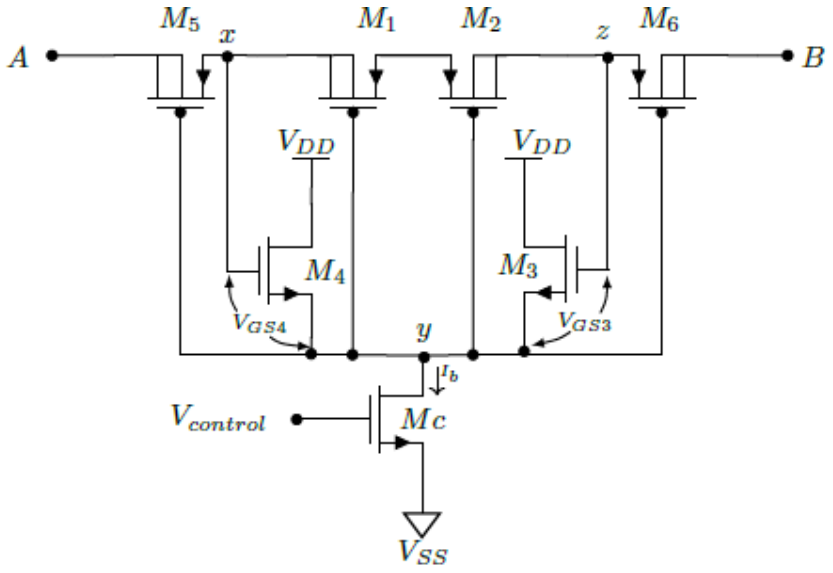
Figure 4.3 – a) multi-cell pseudo-resistor with symmetry and variable V_{GS}, b) I-V characteristics of a)

The $I-V$ characteristics of the simple multi-cell in diode-connected configuration and symmetry is able to provide higher linearity for a small potential difference between node A and B. This is seen in figure 4.3 b). In this case, although the V_{GS} is still variable, the added symmetry is the reason for the better performance in linearity. With B set to $500mV$ and A being varied from $300mV$ to $700mV$ the behaviour cantered around $500mV$

resembles that of a passive resistor. From $460mV$ to $540mV$ there is highly linear behaviour that would represent a high-value resistor in the tera-ohms.

4.3 – Proposed Pseudo-Resistor

The topologies mentioned thus far are able to achieve the high resistance values for small V_{AB} values as shown through testing. When it comes to larger V_{AB} ranges, the PMOS will start to acquire a significantly larger number of carriers thereby reducing the resistance and linearity. This is mainly due to the exponential behaviour of the transistor in sub-threshold region, as such, it was important to investigate the tuneable pseudo-resistors in which the operating point of the transistors can be controlled in a more effective manner. Based on literature, the topology shown in figure 2.16, which is the linear current controlled pseudo-resistor would be the most effective topology in this application. Let's take another look at the circuit mentioned.



With this topology, the differential pair are able to control the operating point of the PMOS pseudo-resistor elements. The operating point circuit allows the gate voltages of the resistive PMOS's to be controlled through equation 2.4.3 in which node Y is the PMOS gate voltage. Through the control of the PMOS V_{GS} by using the differential pair, the linearity of the pseudo-resistor will improve over a larger range, by mitigating the exponential behaviour presented in the sub-threshold equations. With this added control, the resistance of the pseudo-resistor can also be controlled to make it as close to the desirable resistance of $1M\Omega$.

The current source as we know is controlled by the bias gate voltage which in turn controls the overall resistance of the pseudo-resistor. As such the W/L of the NMOS current source was selected as $1\mu m/500nm$ arbitrarily. The larger channel length was chosen to avoid short challenge effects and reduce distortion. To get the desired $1M\Omega$ resistance, a $50mV$ input was sent into terminal A, and terminal B was grounded. The bias gate voltage was then varied until the current going through the resistor was at $50nA$ equating to a $1M\Omega$ resistor. The result is shown in Figure 4.4.

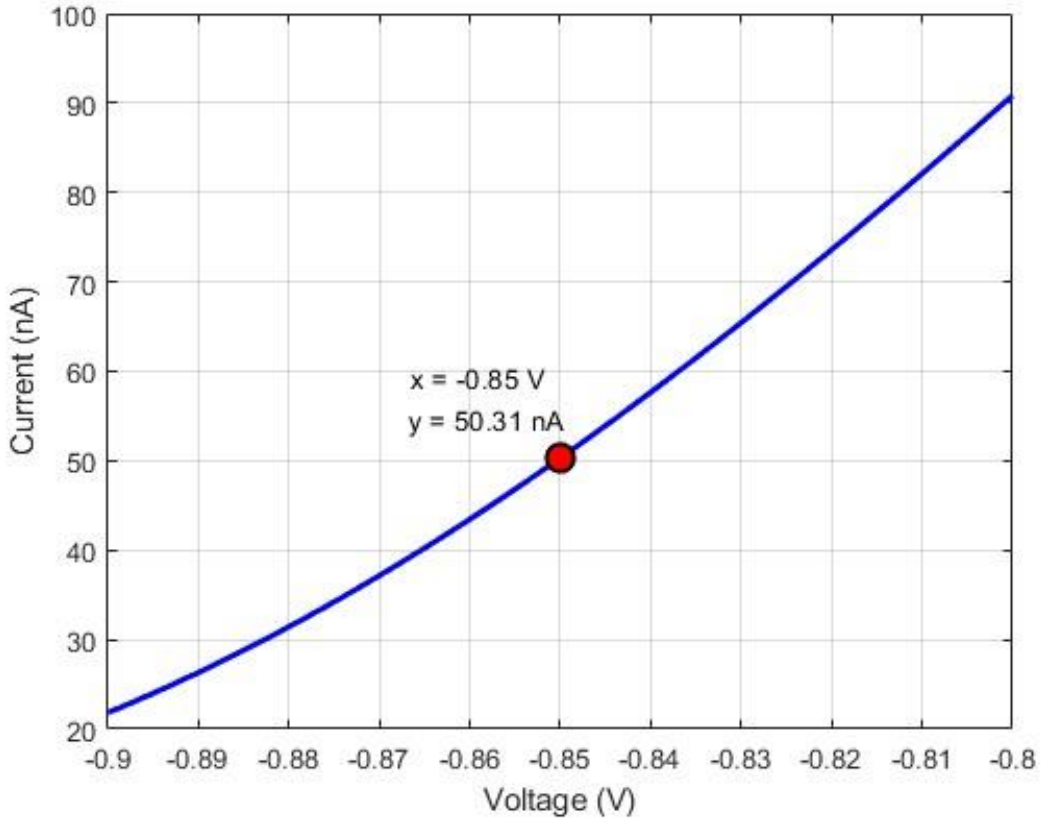


Figure 4.4 – Output current when bias voltage for current source is varied with a $50mV$ input to terminal A

4.4 – Results

4.4.1 – Simulation Results

Based on Figure 4.4, the resistance reaches about $1M\Omega$ when the bias voltage of the current source is $-850mV$. Since we know the pseudo-resistor acts as a $1M\Omega$ resistor when the bias voltage for the current source is $-850mV$, we can test the resistor as it would be used in the second stage of the VI converter. With an input range of $0mV - 100mV$ directly sent to terminal A, and terminal B being grounded, the output current through the resistor was measured and shown in Figure 4.5.

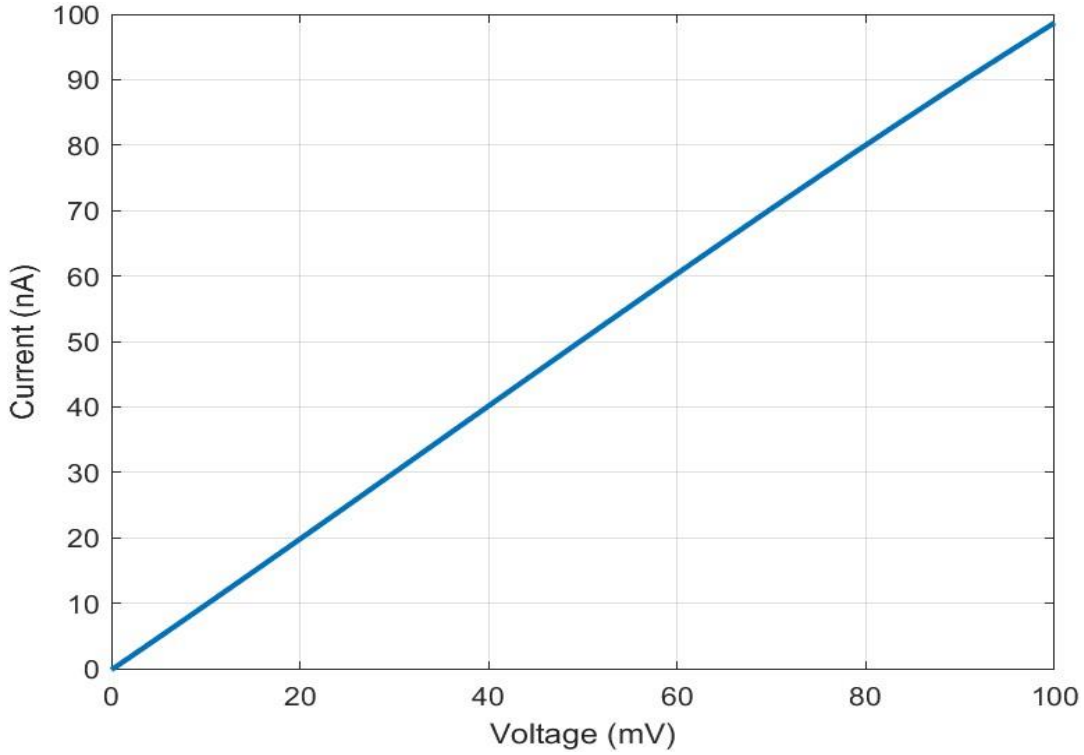


Figure 4.5 – Input voltage vs output current

If the current is taken at any point along the output, it can be found that the resistance stays extremely close to the desired value of $1M\Omega$. This is shown by figure 4.6 which takes the resistance at each point along the voltage range.

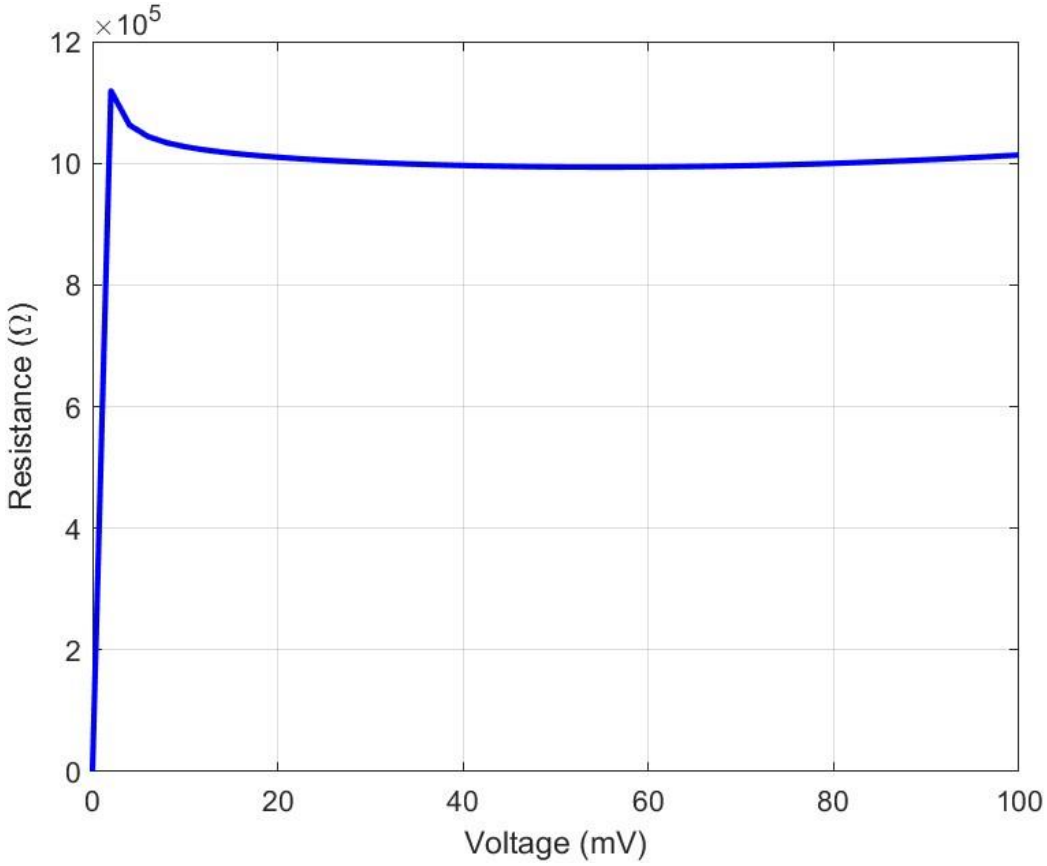


Figure 4.6 – Resistance taken along the voltage range

For the desired range of $0mV - 100mV$ the resistor works as expected, but it is important to test the linearity over a larger range of V_{AB} as well as for different current biases. Figure 4.7 shows the parametric analysis of a larger V_{AB}voltage with different gate bias voltages for the current source ranging from $-500mV\ to - 850mV$. It can be seen that as the bias voltage is more positive, the resistance is smaller but the linearity over a larger range increases. The opposite is true for gate bias voltages that are more negative.

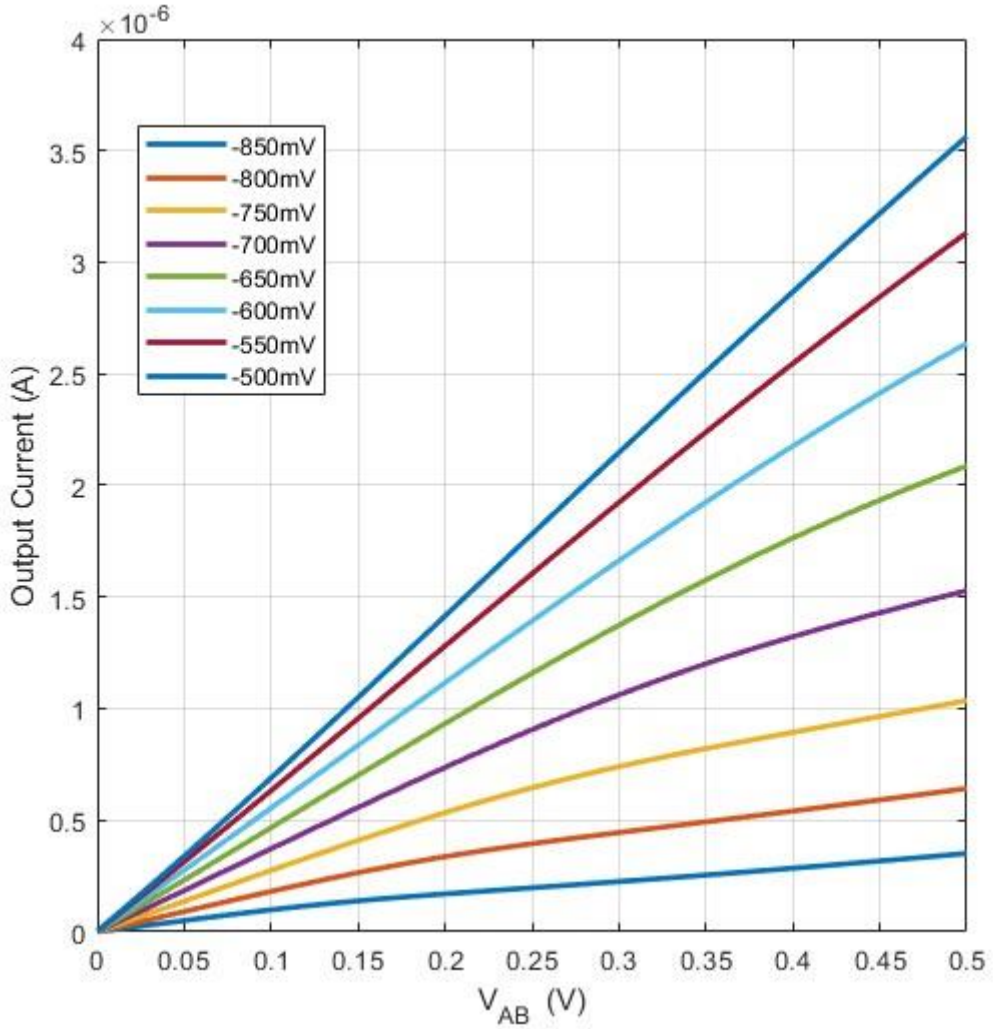


Figure 4.7 – Voltage V_{AB} with varied current biases for different resistances

To see the resistance range that the pseudo-resistor can exhibit, the bias voltage of the current source was varied over a large range of $-1V\ to\ 1V$. The resulting plot is shown in figure 4.8 depicting the resistance seen over that range. As expected, the resistance is highest when the bias voltage is closest to V_{SS} and then drastically decreases as it moves away from it. The resistance peaks at $26M\Omega$, while the lowest resistance value is $135K\Omega$ at around $-375mV$. From $-0.3V\ to\ 1V$ the resistance linearly increases to $610K\Omega$ versus the decaying exponential behaviour close to V_{SS}.

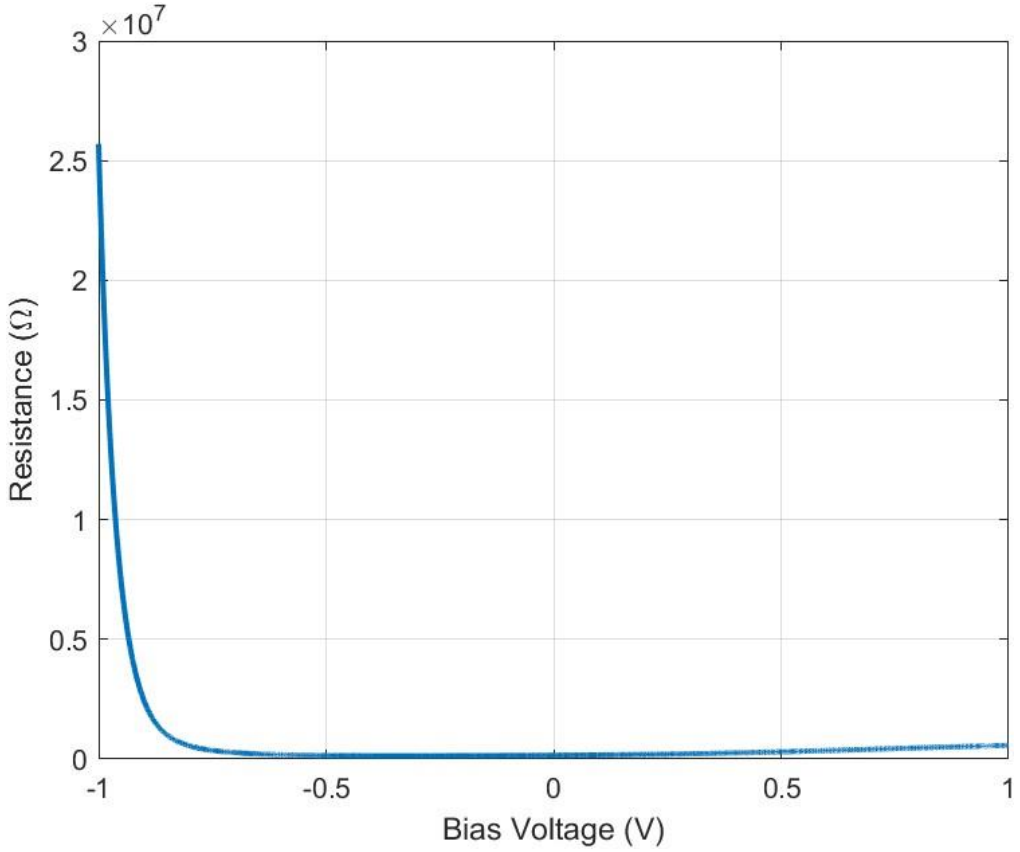


Figure 4.8 – Resistance seen from pseudo-resistor with varying bias voltage

4.4.2 – Reducing Process Variations

The sub-threshold equation for a PMOS transistor is expressed in Equation 2.5.1,

$$I_{SD} = I_{D0}\, e^{\frac{v_{BG}-v_{TH}}{nU_T}} \left(e^{-\frac{v_{BS}}{U_T}} - e^{-\frac{V_{BD}}{U_T}}\right)$$

where I_{D0} is expressed as $I_{D0} = 2n\mu Cox\left(\frac{W}{Leff}\right)U_T$. Notice that there is a strong dependence on process corners, temperature, and voltage. Due to this, there will be lots of variation in the results of the pseudo-resistor when testing for process corners, as well as temperature dependence. Since the pseudo-resistors need to operate in the sub-threshold region to attain the desired resistance, it would be difficult to fully implement a process variation robust pseudo-resistor that also can be highly linear in the voltage region required. To understand how the process variations affect the overall resistance of the pseudo-resistor, the current passing through the resistor was measured with an input of $0 - 100mV$ and the output current was observed at the different process corners as seen in figure 4.9.

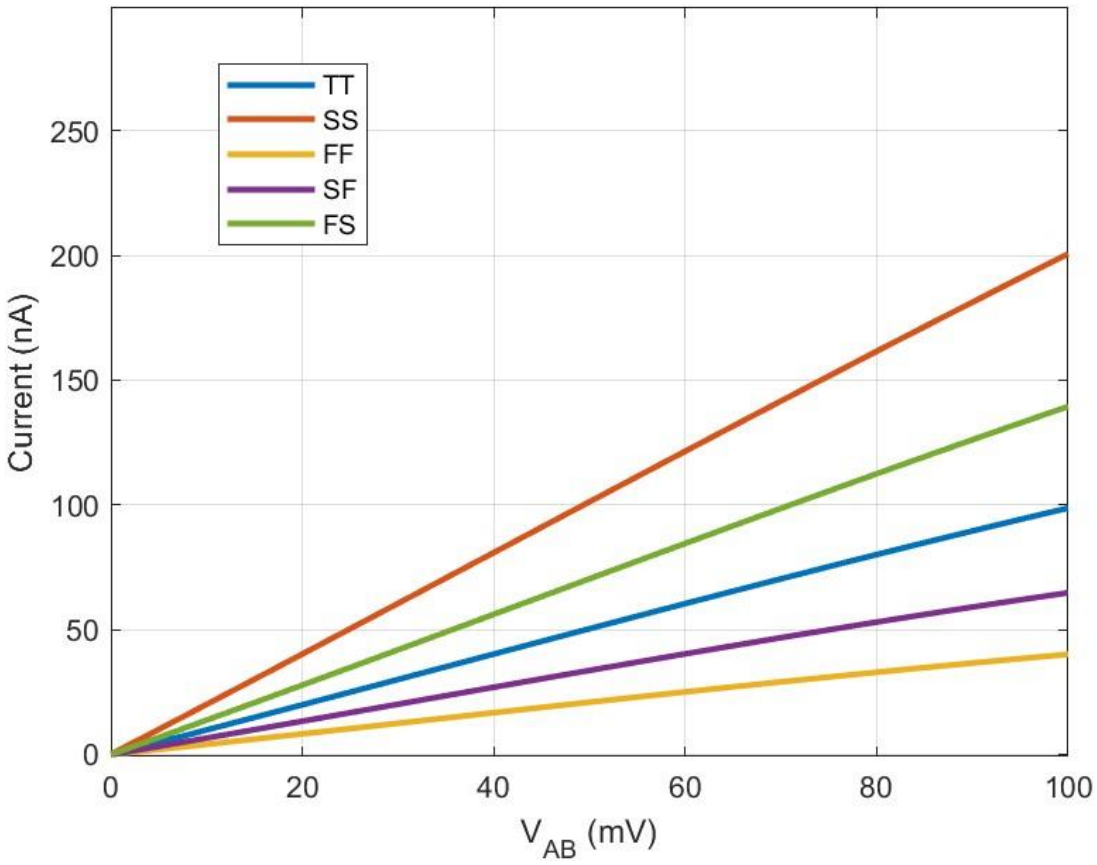


Figure 4.9 – Process corners testing

Notice that in the different corners, the output current response is still highly linear, but the output current levels are affected. Based on this test, it can be assumed that the overall resistance of the pseudo-resistor is being affected by the corners. This can only mean that there are variations in the drain current of the current source which we know to control the overall resistance of the pseudo-resistor. Since the gate bias voltage controls the drain current of the current source, to amend the process variations issue, it was deemed best to give the bias voltage off-chip as to allow for tunability based on the process corner. Table 4.1 shows the bias voltages needed for each process corner to achieve the desired output current of $0 - 100nA$.

Table 4.1 – Pseudo-resistor bias voltages needed for each process corner

Process Corner	**Bias Voltage**	**Drain Current**
TT	$-850mV$	$2.81\mu A$
SS	$-796mV$	$3.49\mu A$
SF	$-877mV$	$1.03\mu A$
FF	$-908mV$	$2.08\mu A$
FS	$-825mV$	$6.04\mu A$

The different bias voltages for the process corners allow the resistance of the pseudo-resistor to be extremely close to $1M\Omega$ for the entire range that it needs to operate within. As a result, when compared to the results obtained without altering the bias voltages off-chip, Figure 4.10 illustrates the improved current output from the pseudo-resistor compensating for the process corners.

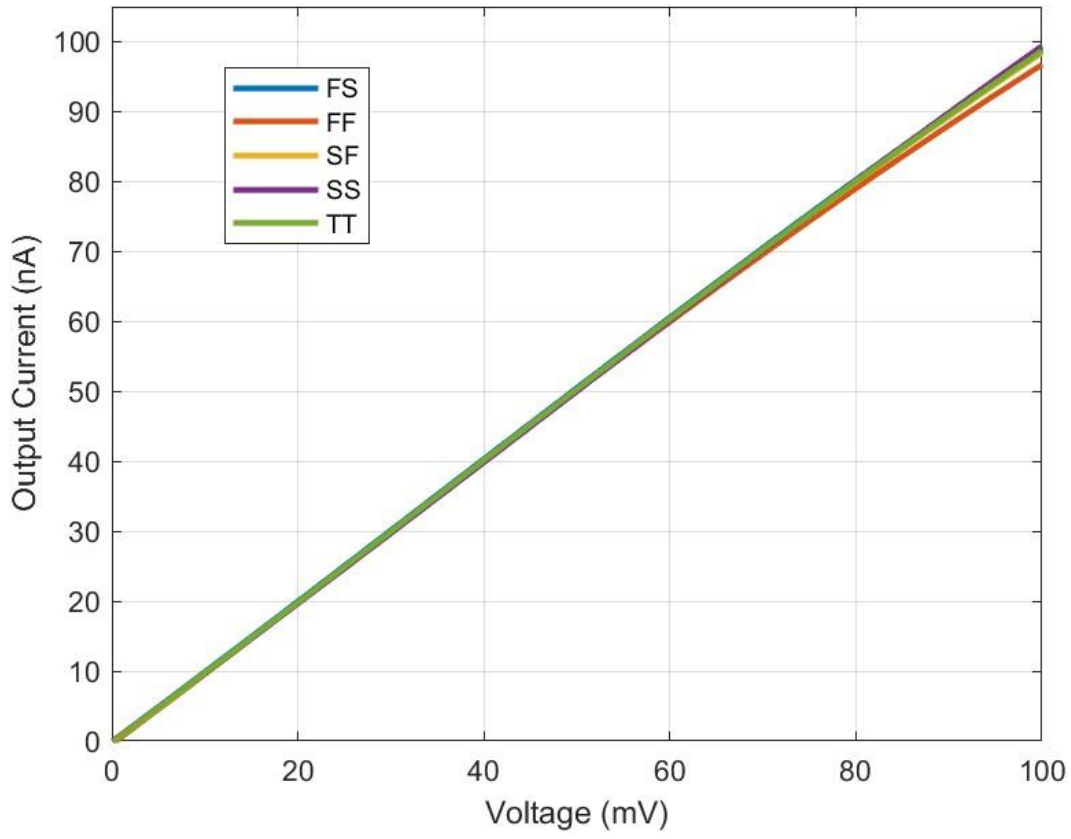


Figure 4.10 – Improved process corner

4.5 – Layout and Post-Layout Simulation

Before the layout for the pseudo-resistor could be completed, one important factor needed to be considered and that is of the body connections of the NMOS transistors. The NMOS bulks are meant to be attached to V_{SS}, which is the lowest potential given to the chip. The bulks of the NMOS transistors are then connected to the p-substrate which holds the V_{SS} potential. This means that for the circuit to properly function, there cannot be different bulk connections for different NMOS transistors as they share the same body of the p-substrate and would cause short circuits. However, in the case of the pseudo-resistor, the differential pair transistors' body connections are made to ground, whereas the current source body connection is made to V_{SS}. There is one way to implement this circuit with different body connections, however it would come at the cost of area and potential change in performance. The PMOS doesn't have this issue as it already has an n-well isolating the structure from the substrate. This means that its body can be connected to any potential without issues.

To be able to have the body connections tied to different potentials, they must be isolated from the substrate, which can be achieved by using a deep n-well. Figure 4.11 shows that the deep n-well completely encapsulates the NMOS allowing it to have its own isolated p-substrate which can be given a voltage potential that is different to that of the substrate.

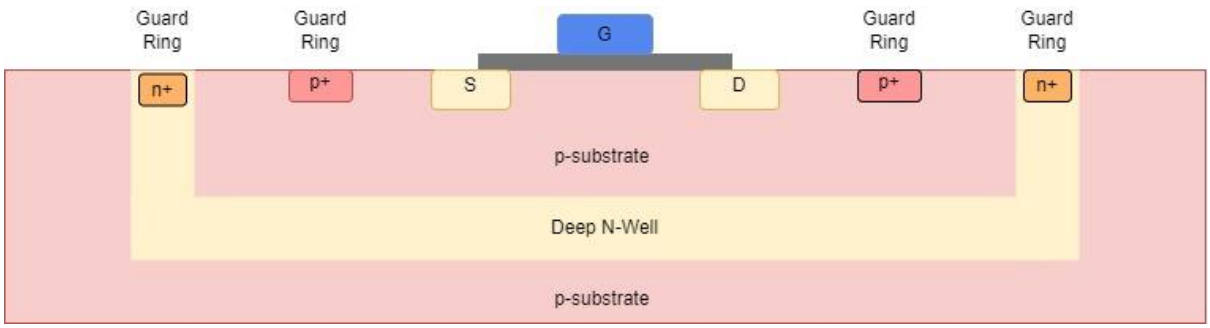


Figure 4.11 – Deep N-Well structure

To implement the deep n-well structure, the NMOS needs to be surrounded by a p+ guard ring as well as an n+ guard ring. The NMOS, with the two guard rings then need to be encompassed completely by the deep N-well which would completely isolate the P well from the P substrate.

Due to the PMOS transistors being operated in the subthreshold region, they will also require an n-well guard ring to protect it from leakage current and noise effects. This method was used

for the OTA and proved to be very effective. Figure 4.9 shows the layout for the pseudo-resistor with the deep n-well NMOS transistors outlined. Notice that the actual transistor is much smaller than the overall structure, but due to rules as prescribed by the foundry, the guard rings must be placed at specific distances from each other in order to clear DRC checks.

Once the layout was completed, DRC checks and LVS checks were performed to make sure that the layout followed all foundry specific design rules and that the layout design followed the schematic design perfectly. With proper structures for the deep n-well implemented, no errors occurred allowing for error free parasitic extraction. With the parasitic extraction complete, post-layout simulations produced the following results.

The resistor was given an input of $0 - 100mV$ to test the output current and see if the resistor can hold a $1M\Omega$ resistance for that range. Figure 4.12 shows the results, and it can be seen that the desired resistance is held very well through the input voltage range. The output current also stays within the error rate of $\pm 0.49nA$ at any given integer voltage value. In post layout simulation, at $-850mV$ bias voltage for the current source, the current increased which caused an increase in resistance. To offset that, the bias voltage was reduced by $8mV$ to bring the resistance back to $1M\Omega$ as seen in figure 4.13. Table 4.2 shows the bias voltage needed in each corner to keep the resistance at $1M\Omega$ for the input range as well as the resulting current sourced by that transistor.

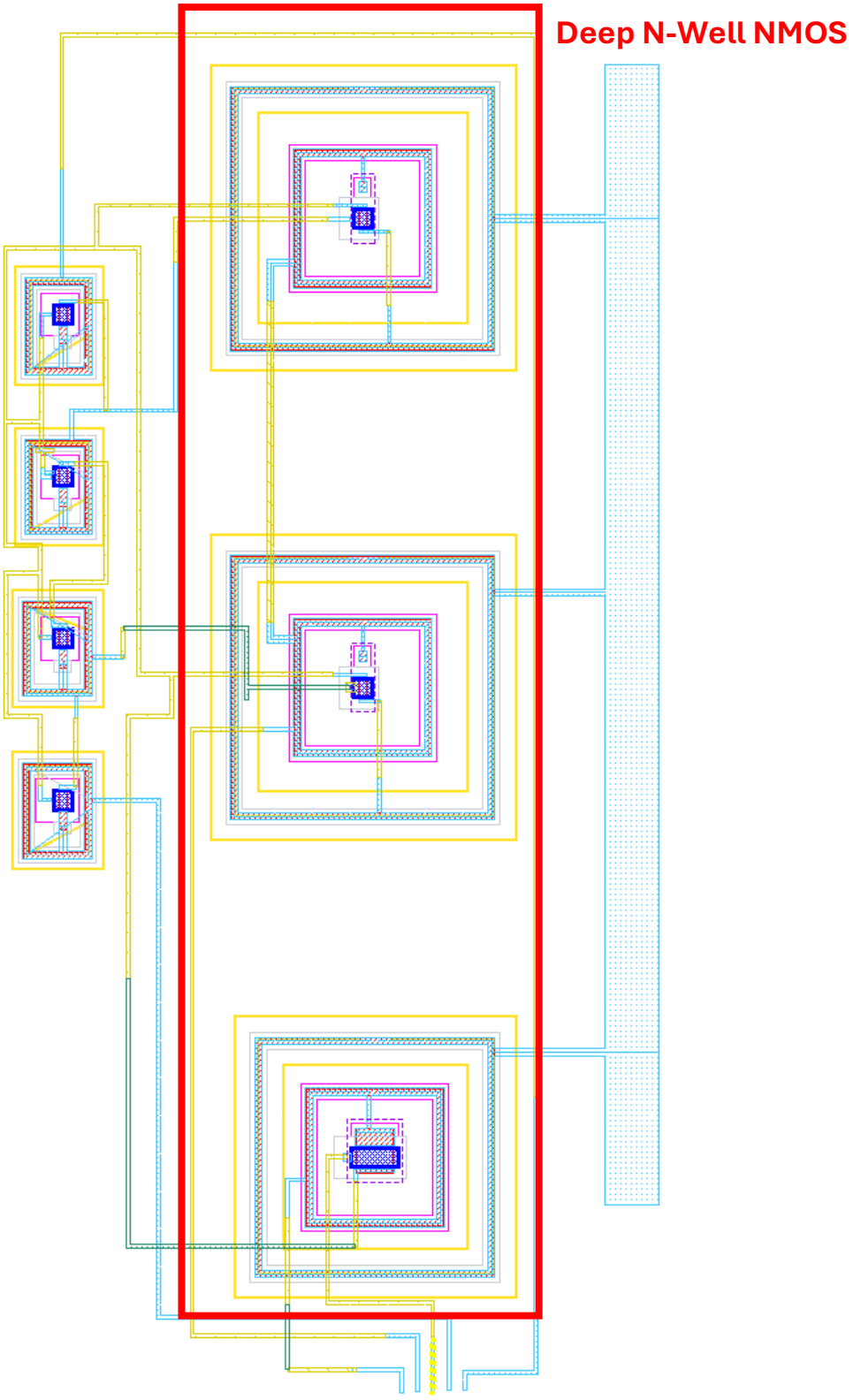


Figure 4.12 – Pseudo-resistor layout

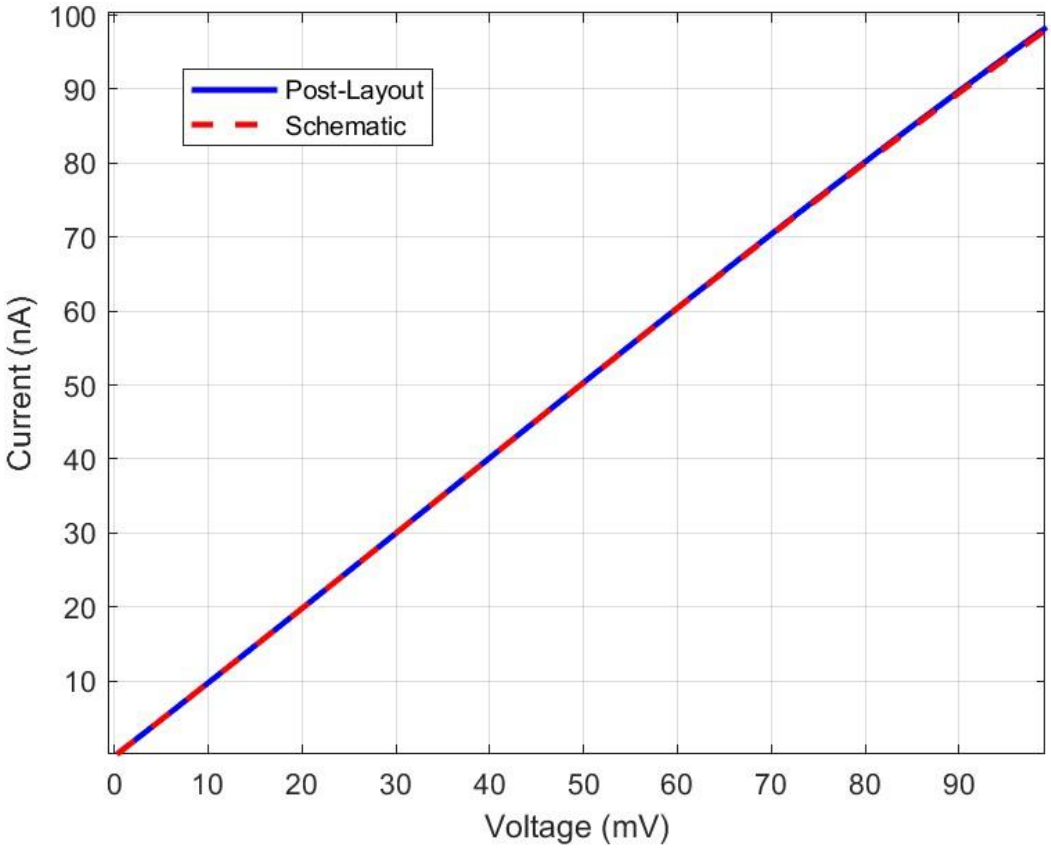


Figure 4.13- Output current vs Input voltage comparison for schematic and post-layout

Table 4.2 - Process bias voltage for ideal operation

Process Corner	**Bias Voltage**	**Current**
TT	-842m	$3.24\mu A$
SS	-788m	$3.98\mu A$
SF	-869m	$1.24\mu A$
FF	-900m	$2.42\mu A$
FS	-817m	$6.701\mu A$

Post-layout simulation of the process corners showed very similar results to the schematic simulations however, there is an increase in the bias current created by the current source. This is likely due to the leakage current caused by the deep n-well current source as well as the differential pair. The post-layout process variations are tested with one terminal seeing the expected voltage for the pseudo-resistor ($0 - 100mV$) while the second terminal is grounded, and the results are shown in figure 4.14.

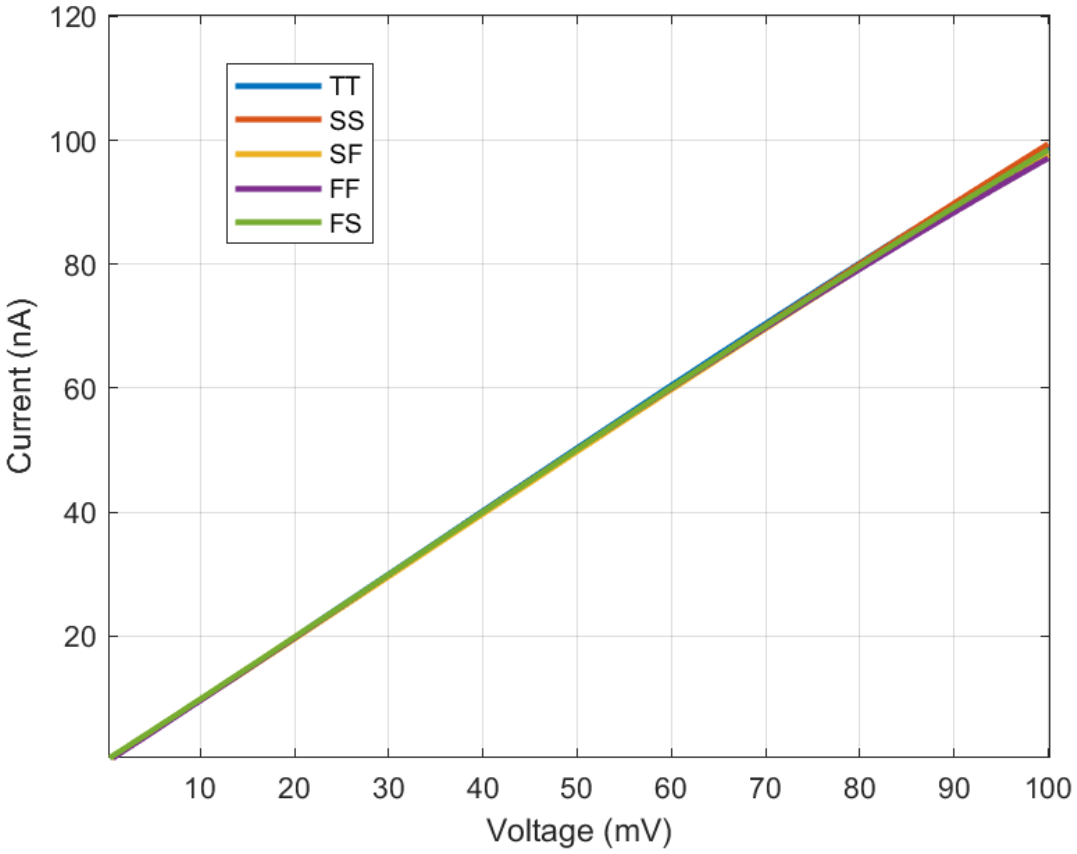


Figure 4.14 – Post-layout process variations

When the overall resistance range of the pseudo-resistor was tested, it was found that due to the increased current supplied by the current source, higher resistances were able to be reached as seen in figure 4.15 when compared to the schematic results. The resistance also steadily declines as the voltage moves away from V_{SS} past the initial rapid decrease. The highest resistance reached is around $34M\Omega$ whereas the smallest resistance value is reached furthest away from V_{SS} at $115K\Omega$.

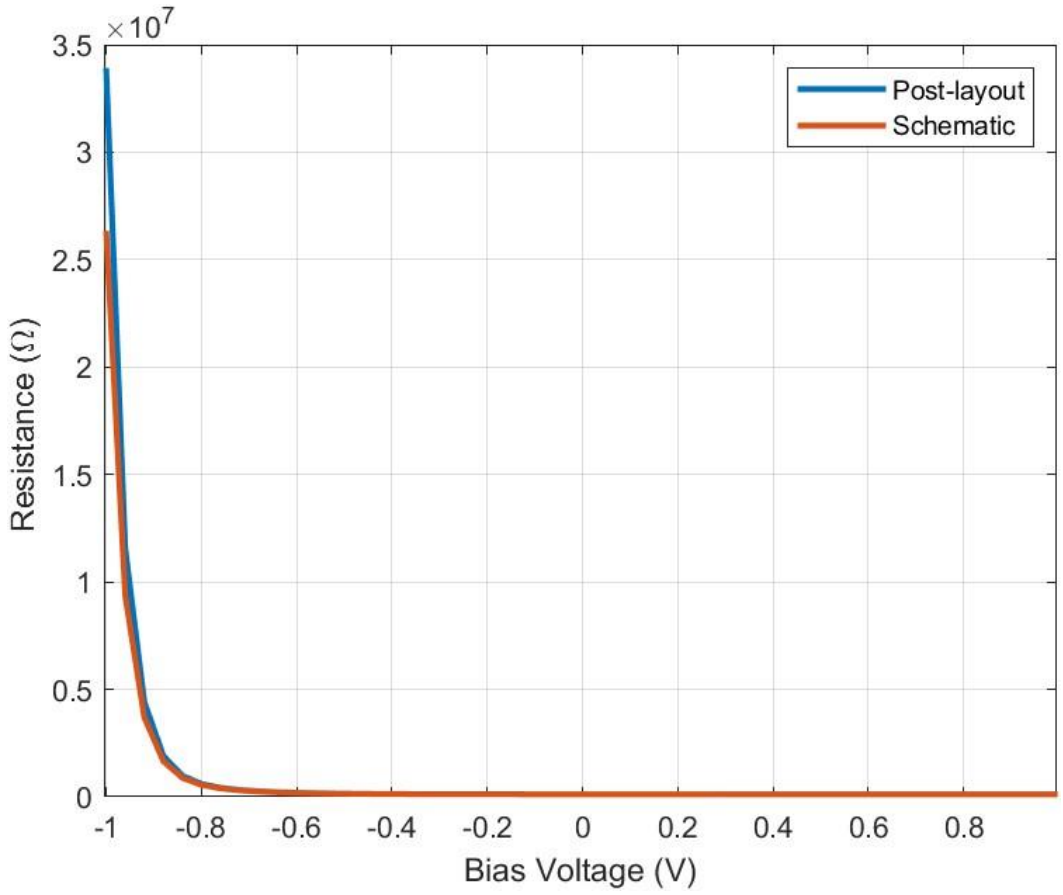


Figure 4.15 – Resistance Range for schematic and post-layout

When comparing the expected resistance of $1M\Omega$ over the entire $0 - 100mV$ input range, it is easy to see that the pseudo-resistor closely follows that in simulation, and post-layout as well, as seen in figure 4.16. There are large errors between $0 - 2mv$, but they then settle around $1M\Omega$ very quickly. The average resistance over the input range is calculated to be $1.006M\Omega$. With this level of accuracy in the design of the pseudo-resistor with very low process variations, the design of the VI converter can proceed without any issues.

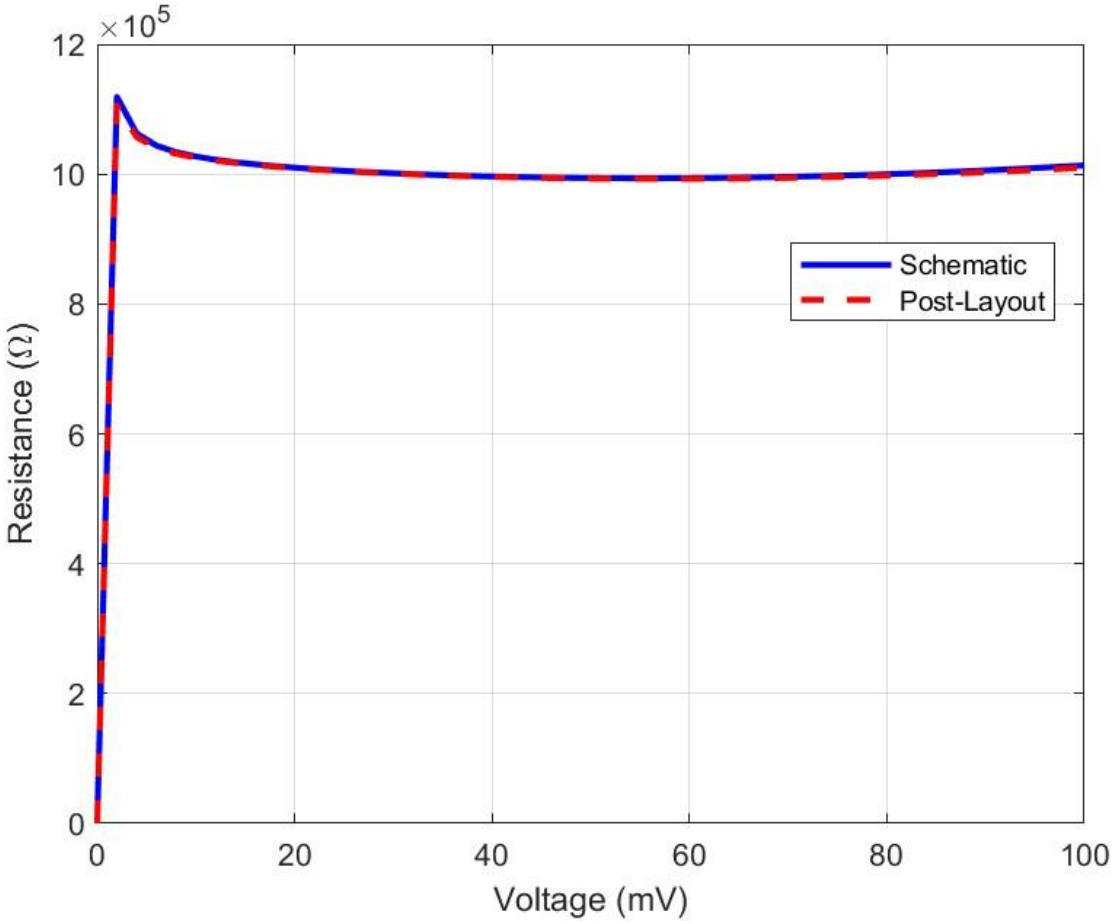


Figure 4.16 – Resistance over input range for schematic and post-layout

The pseudo-resistor designed meets all requirements set to allow it to function as a $1M\Omega$ resistor over the range of $0 - 100mV$. Although there is some variance in the resistance values, the variance in the output current is acceptable per the specifications set for the overall VI converter. As such, for the purposes of the second stage of the VI converter, this pseudo-resistor performs very well. The current consumption of the pseudo-resistor is $3.24\mu A$ for each power supply rail which equates to $7.78\mu W$ of power consumed by this block. The total area consumed by this block is $38.1\mu m\ x\ 19.6\mu m$ in comparison to the $114\mu m\ x\ 100\mu m$ that a normal $1M\Omega$ resistor would take. As such with this pseudo-resistor design, all specification set for this design have been met.

Chapter 5 – VI Converter Design

5.1 – Stage 1

To make the design process of the VI converter simpler, it was decided to modulate the system such that there are two stages that convert the input voltage to a output current. The first stage takes the voltage from the temperature sensor as input and scales it so that the output of stage 1 is within the voltage range of $0 - 100mV$ by using voltage subtraction.

5.1.1 – Output buffer

In chapter 2, the difference between the OTA and Op-amp is discussed briefly where one of the main differences is that the output of the OTA is current, and the op-amp outputs voltage. Another difference is the type of load that the OTA and op-amp can drive. Generally, if the load is capacitive in nature, an OTA is used, whereas if the load is resistive, an op-amp is used. Since an OTA is designed for high output impedance, it makes it more suitable to drive more capacitive loads as the high output impedance helps to stabilize the circuit and prevent oscillations. Along with that, if there is a resistive load attached, since the gain equation for an OTA is $A_V = g_m * R_O$, where R_O is the output resistance of the amplifier, if a resistive element is added to the output, R_O and R_L would form a parallel connection thereby decreasing the overall gain of the OTA. Hence, it is better to use an op-amp when the load is resistive in nature. To ensure precise voltage subtraction in stage 1, a simple voltage subtractor topology is to be used based on resistors in negative feedback. Since that would make the load of the OTA resistive, an output voltage buffer is required to effectively convert the OTA into an op-amp. The output buffer can be as simple as a single PMOS transistor however, for more precise voltage following, a more complex output buffer needs to be used. Since this voltage buffer needs to operate within the region of $0 - 1V$, it must have a high swing as to not lose any data when in voltage follower configuration.

The voltage buffer used in this design is shown in figure 5.1 and consists of the already designed OTA, and a super source follower circuit as shown in [58]. If the bias current source MB1 maintains a high output impedance, the input transistor for the voltage buffer M1 can follow the voltage accurately when the output voltage reaches near $0V$ and V_{DD}. The length of M2 must have a large W/L to ensure that when on, the gate voltage is not affected. If the width is not large enough, the operation of the current source MB1 may be affected and cannot work normally to allow for accurate voltage follow. If input voltage is close to$0V$, M2 would operate in the linear region, but as long as the gate voltage of M2 doesn't rise to force MB1 into the linear region, M1 can remain in saturation.

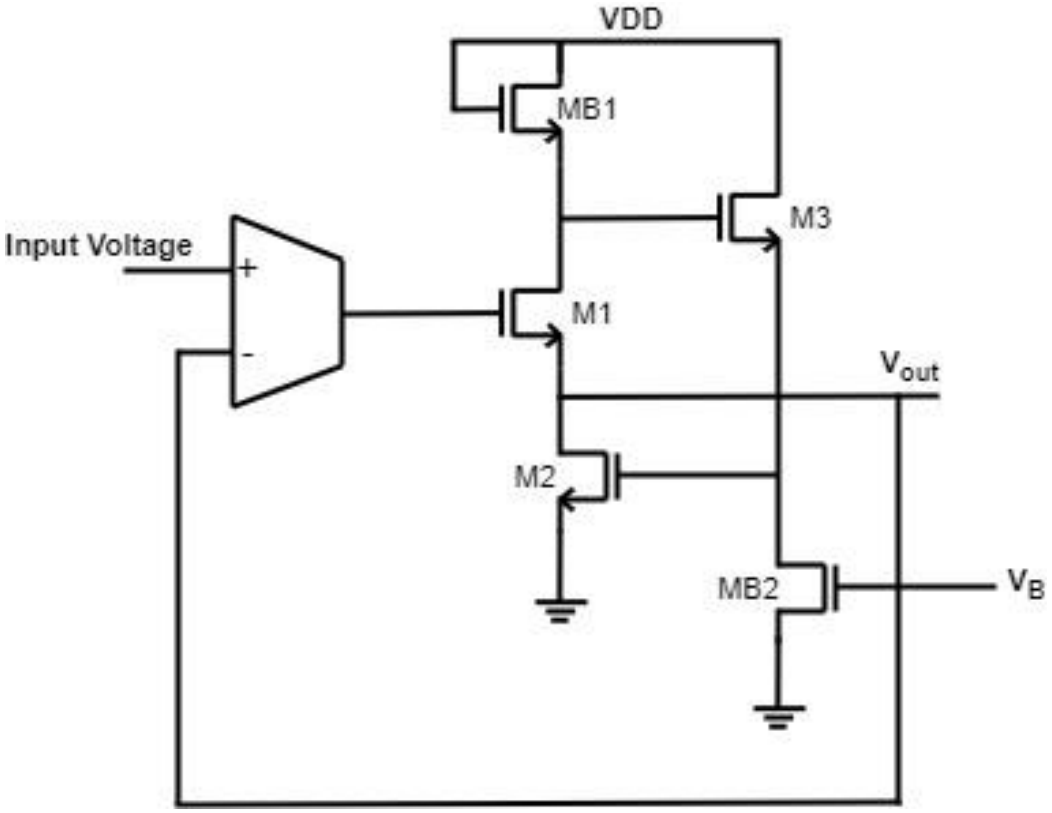


Figure 5.1 – Super source follower circuit

5.1.2 – Voltage Subtractor

There are many topologies of the voltage subtractor that can be used for the purpose of removing a specific DC voltage from a given range. Based on specifications, it is important that the voltage subtractor adheres to certain parameters such as keeping power consumption to a minimum and output voltage highly accurate to the desired output. Not only that, but an emphasis on keeping process variations low must be kept.

In order to simplify the design of stage 1, a very common and well-known circuit is used to perform the voltage subtraction. Figure 5.2 shows difference amplifier circuit used for this application. Note that the op-amp shown in the circuit is simply the designed OTA with the output voltage buffer stage discussed in the last section.

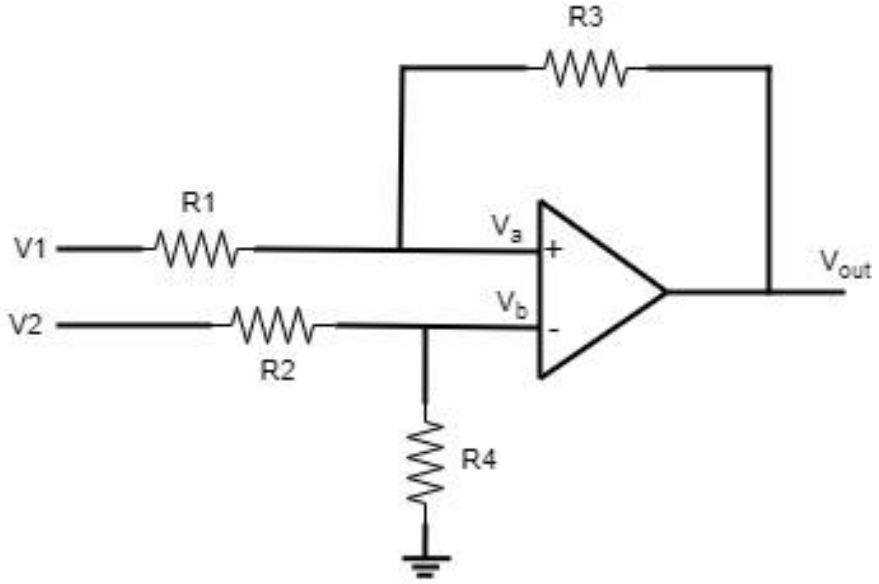


Figure 5.2 – Difference amplifier circuit

This circuit can be analysed using the super position principle by connecting each input to ground in turn. The transfer function for the above circuit can be given by:

$$I_1 = \frac{V_1 - V_a}{R1}, \qquad I_2 = \frac{V_2 - V_b}{R2}, \qquad I_f = \frac{V_a - V_{out}}{R3} \tag{5.1.1}$$

where based on op-amp principles we know that $V_A = V_b$.

Solving using superposition we can find V_{out} when each input takes turns being grounded and then combining them gives us,

$$V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right) \quad 5.1.2$$

If resistors $R_1 = R_2\ and\ R_3 = R_4$, the transfer function simplifies to

$$V_{out} = \frac{R_3}{R_1}(V_2 - V_1) \quad 5.1.3$$

Since in this application, no voltage gain needs to be applied, all the resistors can be kept at the same value. This also has the added benefit of resistor matching which allows for a design that will have very small process variations. Since the resistors will have the same nominal value, and will be matched in ratio, they will track each other closely through the manufacturing process. This means that if one resistor's value increases due to process variation, it is likely that the other will as well by a similar proportion. In fact, the ratio between these resistors is more constant than the actual values themselves, which maintains the accuracy of the transfer function and reduces process variations.

5.1.3 – Results (Simulation + Post Layout)

Even though the values of the resistors in the voltage subtractors will be the same allowing for very low process variations, it is important that the correct value is chosen such that there is no drop in accuracy while also keeping it to the lowest silicon area used as possible. To test this, the OTA with the output buffer were setup with the resistors as shown in figure 5.3, with the resistors given an arbitrary value of $10K\Omega$.

To simulate with values that were pertaining to the application an input DC signal sweep of $820mV\ to\ 920mV$ was used. Since the desired output voltage range is $0 - 100mV$ the voltage that would need to be subtracted is $820mV$. It was found that with $10K\Omega$ resistor, the voltage subtractor did operate well and as such a simple voltage divider output was displayed. Different values of resistors were tested from $10K\Omega\ to\ 100K\Omega$ with increments of $10K\Omega$. It was at $50K\Omega$ that the voltage subtraction operation presented highly accurate results. After that point, there was a very slight increase in the accuracy, however it was not enough such that it warranted the significant increase in area used by the resistors. In an effort to further reduce the area used, the voltage subtraction operation was tested with $45K\Omega$ resistors. Although there was a slight increase in the error percentage, it was not significant enough that would affect overall performance of the VI converter. As such it was decided to use $45K\Omega$ resistors for the voltage subtractor topology circuit. Though there is some cutoff near $0mV$ and an offset of a few mV, if the subtracted voltage of $820mV$ is lowered to $820mV - offset\ voltage$, the cutoff can be avoided, and the offset can be removed. This can be achieved by compensating the subtracted voltage by the offset voltage. The comparison of the output of stage 1 with the compensated and uncompensated reference voltage can be seen in figure 5.3.

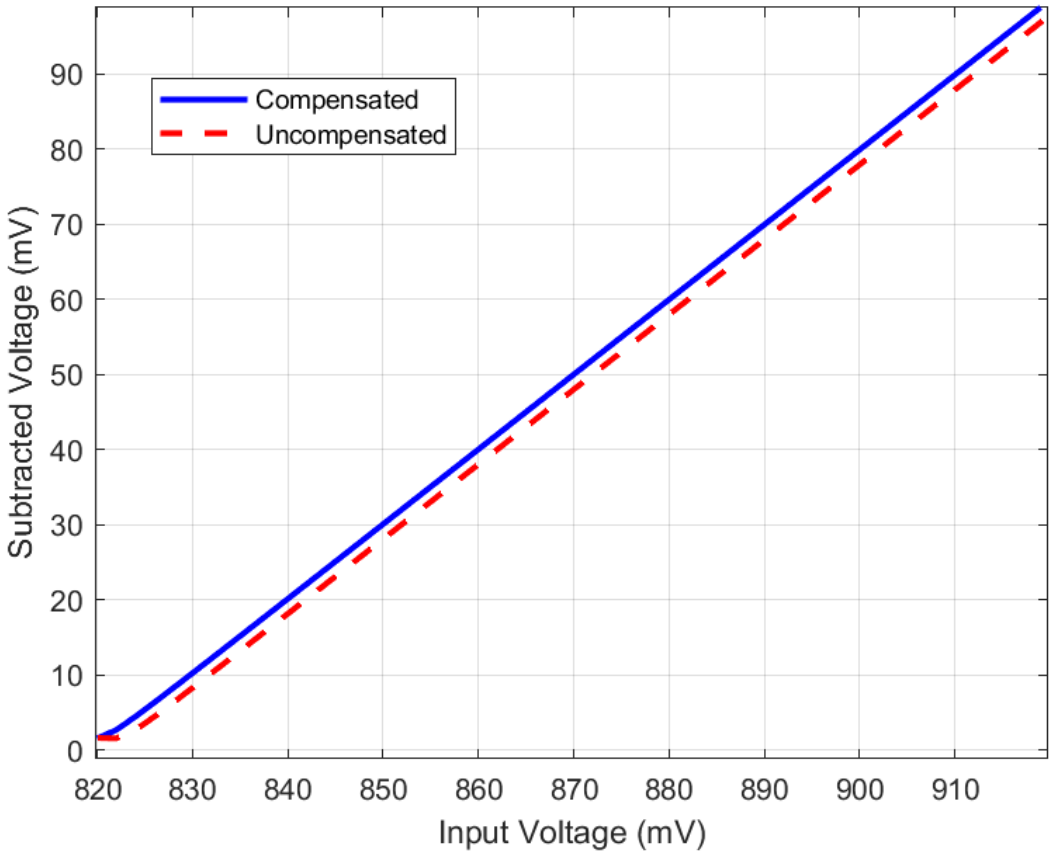


Figure 5.3 – Output of the voltage subtractor with and without compensated subtracted values

If the voltage is taken along any point in the compensated curve, the voltage would remain within the desired error range of $\pm 0.49mV$. Since the subtracted voltage is an off-chip controlled voltage, any variation we see in post-layout simulation can be adjusted accordingly.

To ensure that the resistors did not have an effect on the process variations, the subtracted voltage output was observed against the process corners and shown in figure 5.4.

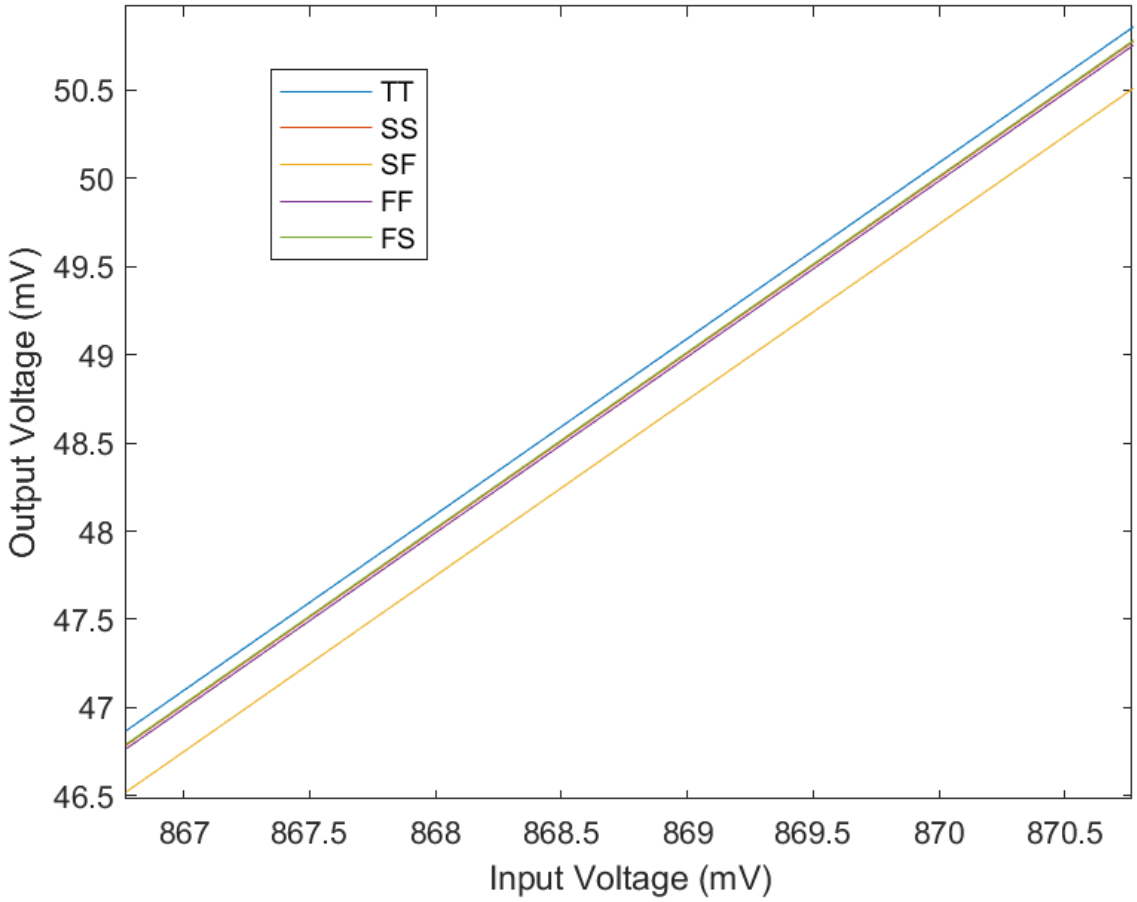


Figure 5.4 – Zoomed in plot of subtracted voltage tested against the process corners

As expected, there was very minimal variation due to the process corners for the entire testing range. Variations can only be seen when they are observed at a very small input voltage range. Even then, the variations are not large enough that it would cause issues in the voltage-to-current conversion process in stage 2 since the designed pseudo-resistor behaves very close to a $1M\Omega$ resistor.

One thing to note is that since the substrate voltage is V_{SS} at $-1.2V$, and the super source follower output buffer utilises NMOS transistors with body-to-source connections as well as ground connections, it was necessary to implement deep n-well transistors. Along with this, within the TSMC 65nm kit, the largest resistor has a value of $17.5K\Omega$ with a size of $2\mu m x 100\mu m$. To achieve the desired $45K\Omega$ resistor, four $11.25K\Omega$ resistors were connected in series which then had a total size of $22\mu m\ x\ 70\mu m$. Figure 5.5 shows the full layout of

stage 1 which includes the 2-stage OTA, the output voltage buffer and the four $11.25K\Omega$ resistors connected in series to form the $45K\Omega$ resistor needed.

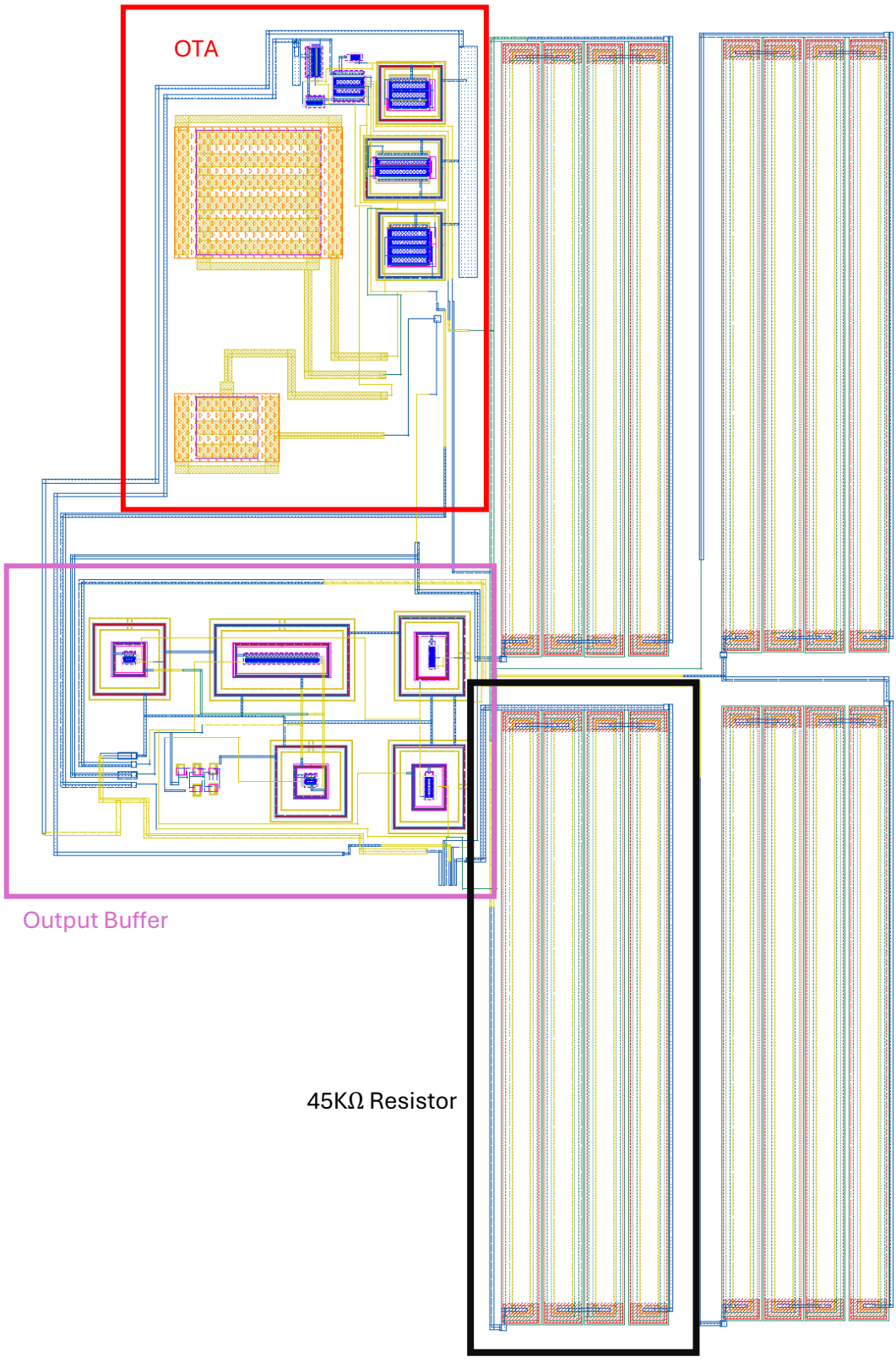


Figure 5.5 - Stage 1 full layout

Once the layout was complete, DRC and LVS checks were done to ensure that the design was done according to foundry specifications, while also making sure that the schematic and layout were matched perfectly.

To compare the results of the voltage subtractor between the schematic and post-layout, the same method was used as previously mentioned for post-layout simulations and then plotted alongside the schematic simulation results. This can be seen in figure 5.6. When looking at the results, it is evident that that there is almost no difference between the schematic and post layout simulations. Based on this fact, stage 1 of the VI converter can effectively transform the expected input voltage range of $820mV - 920mV$ to $0 - 100mV$ with high accuracy. The total area of the block is $149.6\mu m\ x\ 104.5\mu m$, although there is a block of $50\mu m\ x\ 53\mu m$ which is empty space, it will be used up in stage 2 to ensure no area is wasted. The total power consumed by stage 1 is $23.8\mu W$.

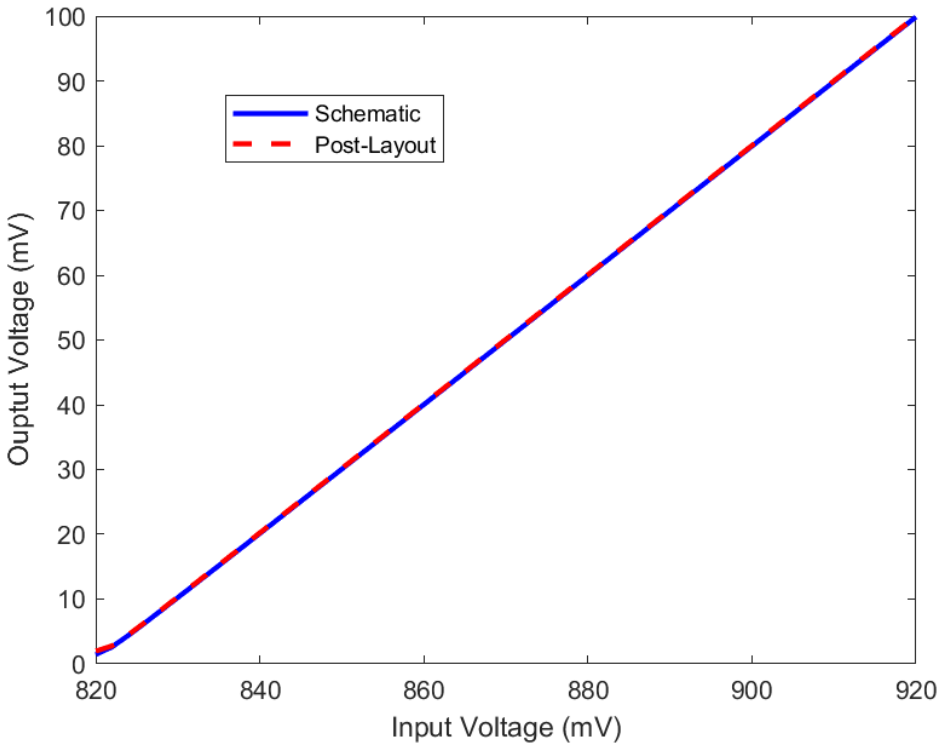


Figure 5.6 – Schematic vs post layout voltage subtractor output

5.2 – Stage 2

Stage 2 of the VI converter consists of three circuit blocks: the OTA in negative feedback, the pseudo-resistor and finally the output current mirror. Two of the three circuit blocks have already been designed to specifications, leaving only the current mirror. In this design, the current mirror is not only responsible for mirroring the current from the conversion branch to output branch, but also for the feedback path.

5.2.1 – Current Mirror

Among the discussed designs in chapter 2, such as the improved Wilson current mirror and the cascade current mirror, it is important that the one chosen for this application meets design requirements. The specifications for the current mirror as follows:

- Minimal power consumption
- Minimal area consumption
- Very precise current copy to the output branch
- Large output voltage range that is centred around $500mV$

One thing to note is that since the voltage of the node where the VI converter output node is to be connected is unknown, having a large output load voltage range ensures that there are no errors in reading the data post integration. To find the current mirror topology that best fits the needs of the VI converter, simulations need to be performed to make the decision. To test the precision of the current copy, an arbitrary DC current of $500nA$ is passed into the input branch and copied into the output branch with a load variable load voltage. Figure 5.7 compares the different current mirror topologies' ability to copy current precisely over a varied output load voltage range. The output load range is measured by taking the voltage at which the current is $499.51nA - 500.49nA$. The reason for this is that the error range of the VI converter is $\pm 0.49nA$ of the expected value.

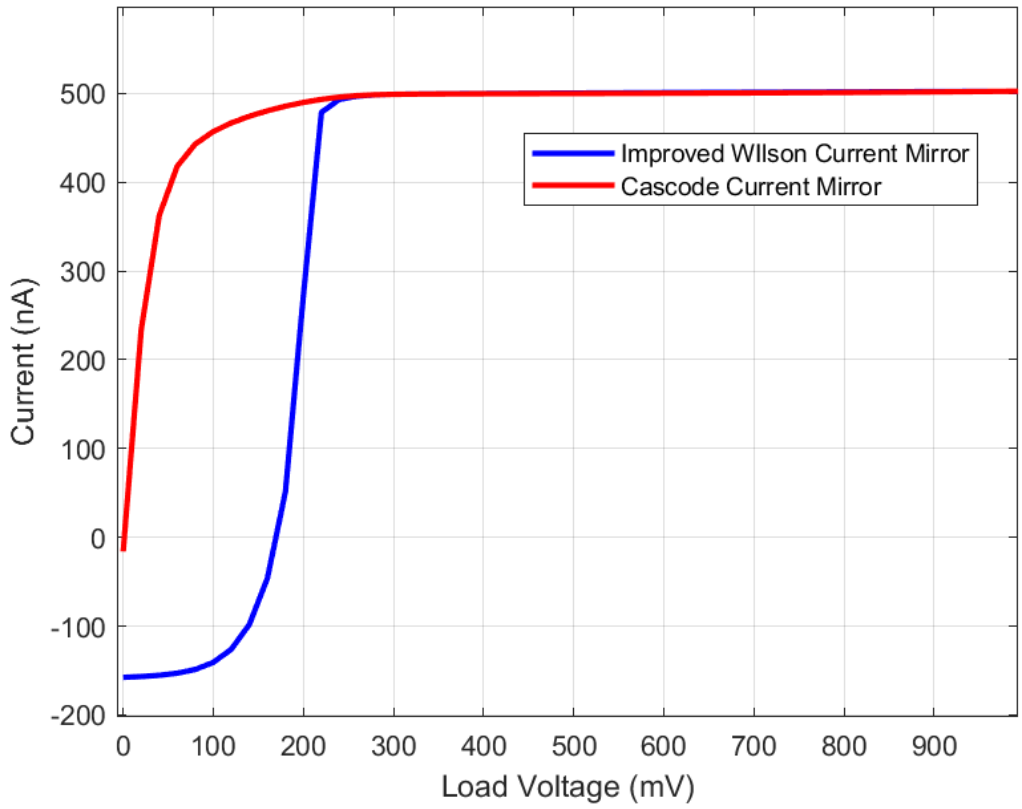


Figure 5.7 – Comparing the Improved Wilson current mirror vs cascode current mirror with a varied output load voltage

The output branch of the current mirror was connected to a voltage source that was varied from $0 - 1V$. The cascoded current mirror reaches the lower limit of the expected value at $380mV$ and the upper limit at $690mV$ with an output load voltage range of $310mV$. The improved Wilson current mirror reaches the lower limit at $350mV$ and the upper limit at $520mV$ with a total acceptable range of $170mV$. With a higher output load voltage rage, the cascoded current mirror seems to be the better option for this application.

5.2.2 – Voltage -to-Current Conversion

With the current mirror topology decided, the proposed stage 2 design is shown in figure 5.8.

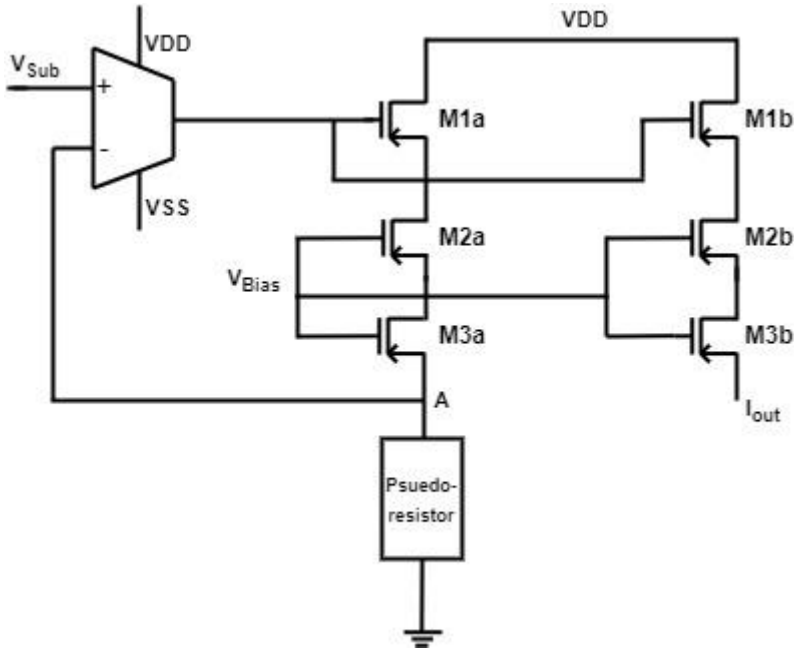


Figure 5.8 – Stage 2 design

The PMOS current cacoded current mirror takes the output from the OTA as input. In this configuration, the first branch also acts as a voltage buffer allowing Node A to be fed back into the negative feedback path. The cascoded transistors on the output branch will allow for a more precise current copy where the output current is not dependent on the load voltage. Transistors M1 and M1a were biased with the output voltage from the OTA while transistor M2, M2a, M3, and M3a were biased with $600mV$. This was to keep the biasing simple as it half of VDD which can be given with off chip voltage division. To keep the current copy from branch 1 to the output branch as exact as possible, a 1:1 ratio was kept which means all transistor sizing was kept the same at $200nm/2.5\mu m$. The widths and lengths were chosen by parametric analysis in which the sizing parameters were varied to see which transistor sizes gave the most desirable output.

The voltage to current conversion occurs in the input branch of the current mirror where the feedback voltage at node A, is converted to a proportional current by the pseudo-resistor acting as a $1M\Omega$ resistor. Based on OTA principle we know that $A = V_{sub}$. Therefore, the current that flows through the input branch is represented as $I_{out} = \frac{A}{R_{PR}}$.

With stage 2 fully designed, both the voltage subtractor of stage 1 and the current converter of stage 2 can be combined to form the full VI converter as shown in figure 5.9.

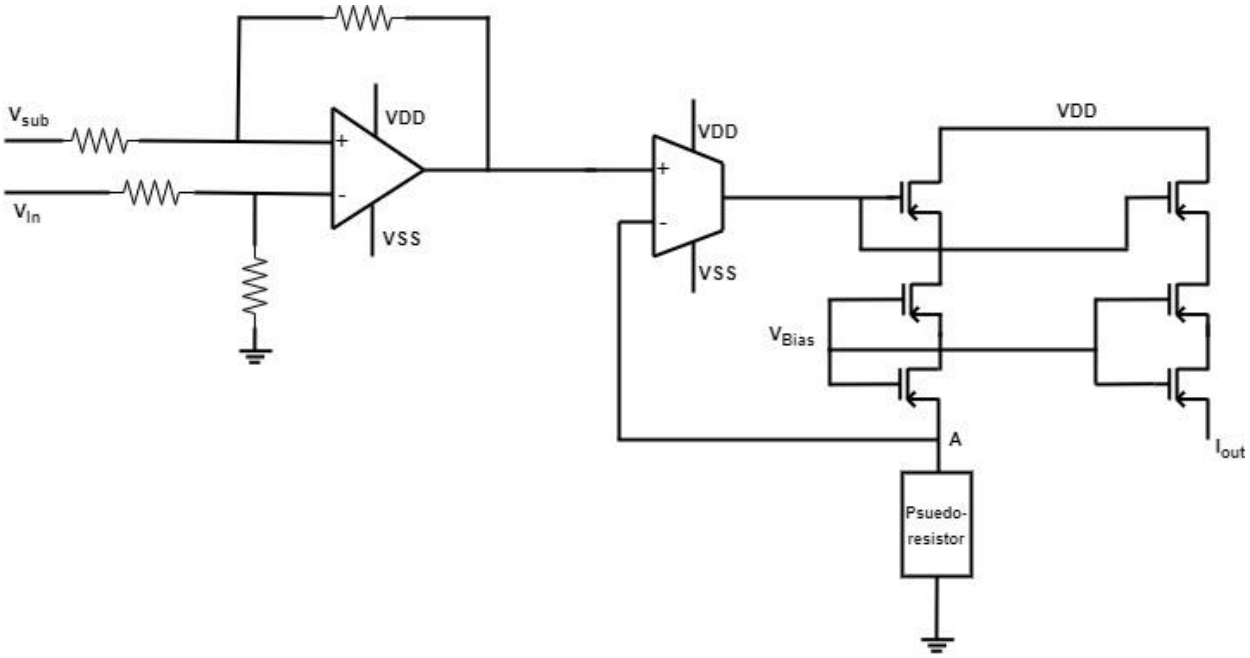


Figure 5.9 – Full VI converter design

The current conversion aspect of this design is heavily dependent on the fact that the subtracted voltage from stage 1 and the feedback voltage at node A in stage 2 match very well. A very precise voltage follow will allow for a conversion that is higher in precision. Figure 5.10 compares the two voltages.

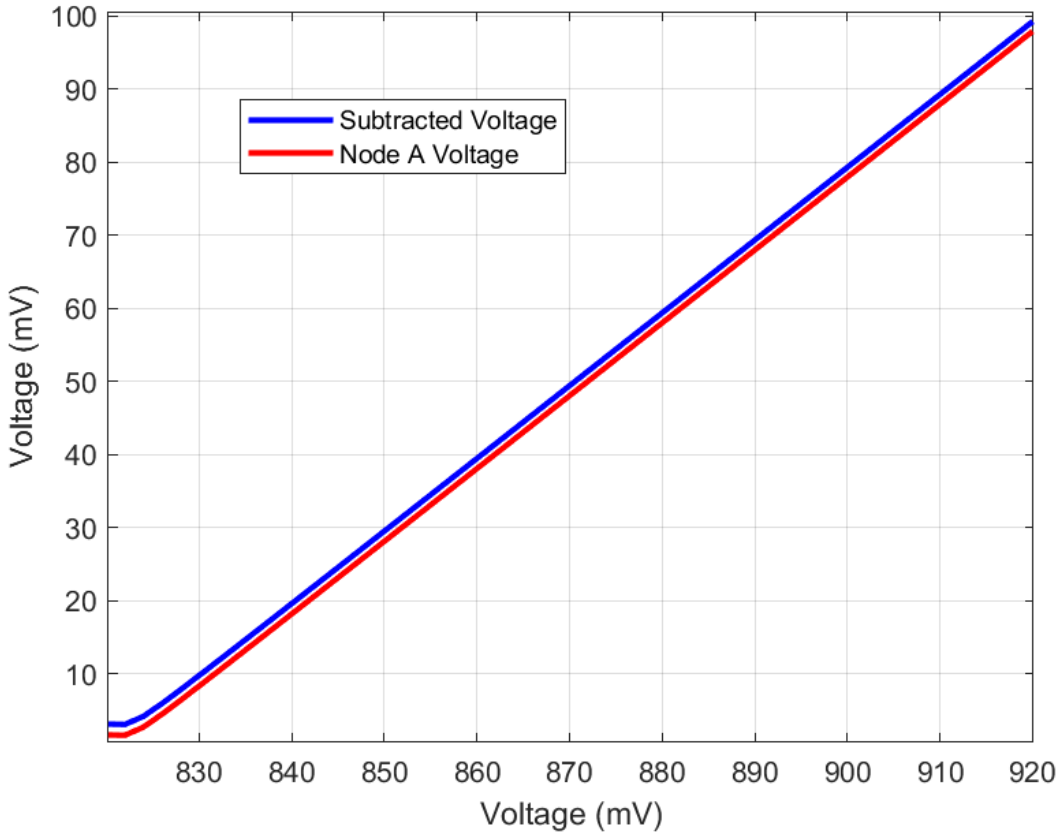


Figure 5.10 – Difference between subtracted voltage and feedback voltage at node A

The results show that the subtracted voltage and the feedback voltage at node A have a very slight difference between them of $1.3mV$. Although the voltages are not the same, this was expected as there is bound to be some difference between the two nodes. This is because no voltage follower circuit can replicate the input voltage exactly due to many factors such a leakage current, parasitic, etc. However, since the subtracted voltage and the feedback voltage are very close in value, it can be easily compensated by the current mirror and the conversion process.

5.2.3 – Results (Simulation + Post-Layout)

With the pseudo-resistor behaving as a $1M\Omega$ resistor and Node A following the subtracted voltage very closely, the current through that branch represents the desired output current that

would be the input to the AFE. To ensure that there is minimal difference between the first and second branches of the current mirror, a $500mV$ load voltage is added to the output branch and both branches are then observed and shown in figure 5.11.

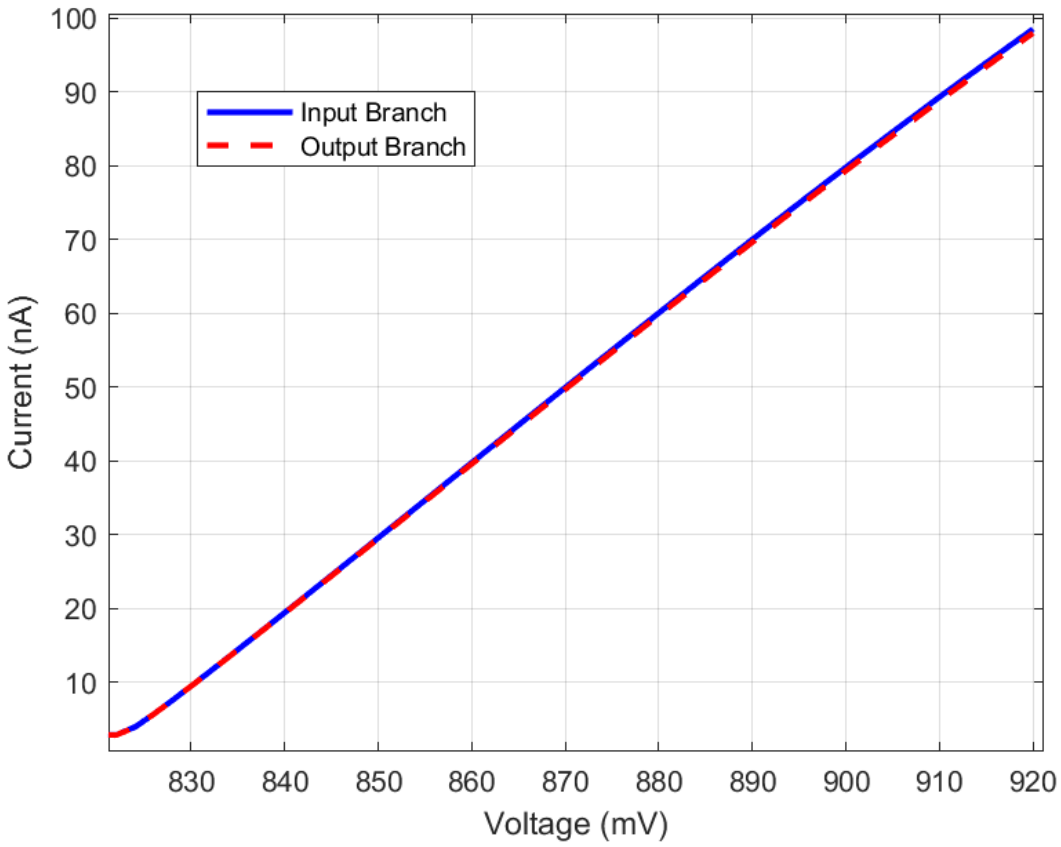


Figure 5.11 – Comparison between input and output branch of the current mirror

At $500mV$ load voltage, there is little to no difference in the current between the two branches which shows great current copy from the current mirror. Within figure 5.11, it is also evident that the current conversion process from the voltage input from the temperature sensor to the current conversion and the copy to the output branch shows very linear and highly precise current conversion.

With the full VI converter designed, all circuit blocks need to be assembled together in layout while ensuring that all previous empty space in block are used up so there is no waste in silicon area. All transistors in the current mirror are surrounded by guard rings to protect against

leakage current as even small leakages can alter the output. Figure 5.12 shows the full VI converter layout free from DRC and LVS errors.

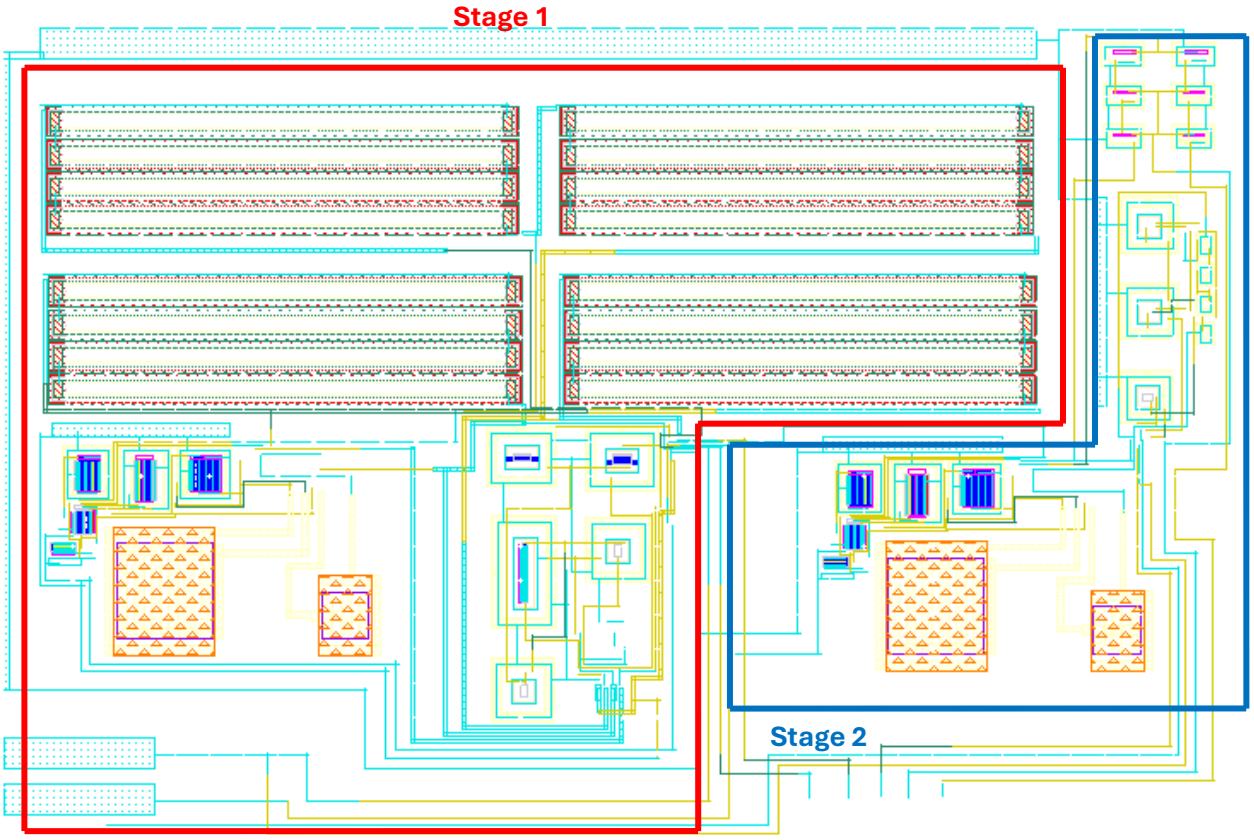


Figure 5.12 – Full VI Converter layout

The output current was simulated with a load voltage of $500mV$ post-layout and compared that with the results from schematic capture as shown in figure 5.13. In post-layout simulation, the pseudo-resistor bias voltage was changed to $-842mVC$ as opposed to the base $-850mV$ in schematic simulation to achieve the $1M\Omega$ resistor.

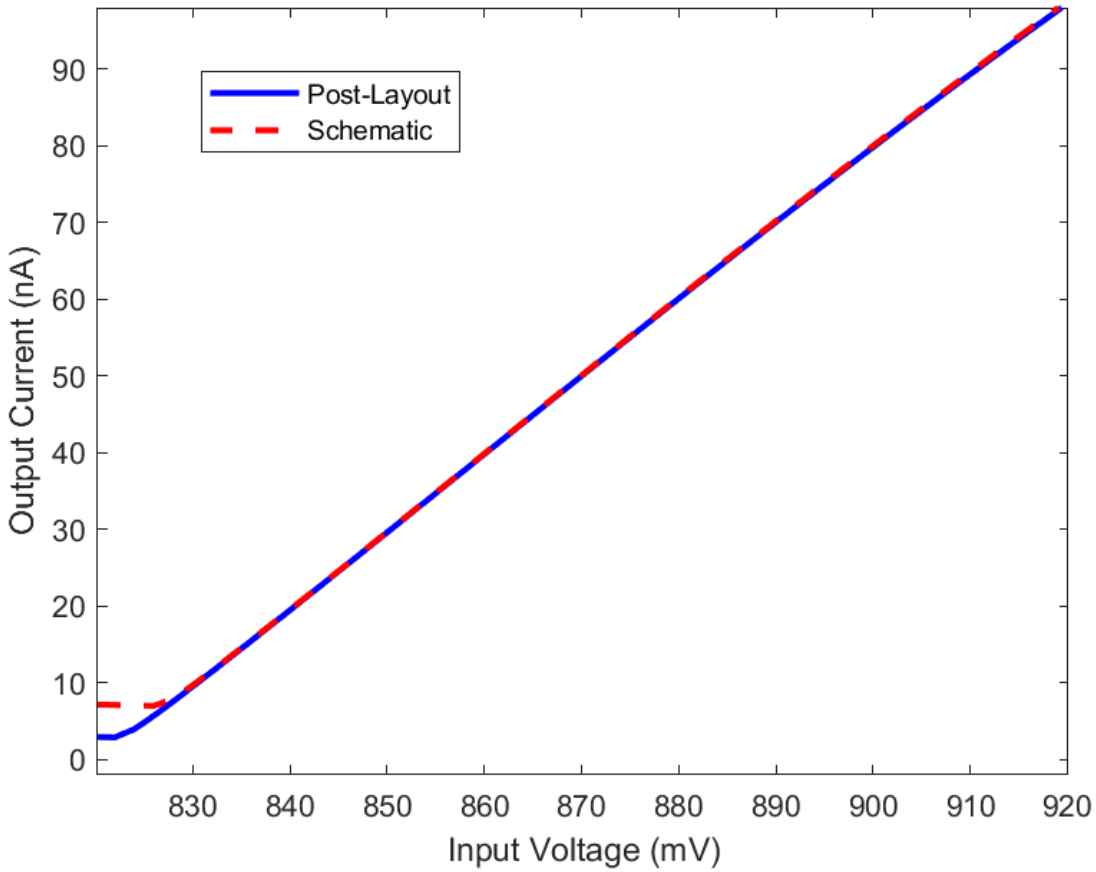


Figure 5.13 – Schematic vs post-layout comparison of output current with $500mV$ load voltage

In post-layout, there is larger cutoff that is observed at the range closer to $820mV$ which is seen as $0V$ at the conversion stage. The VI converter regains linearity at the converted $8mV$ and stays within the error rate of $\pm 0.49mV$ of the expected value for the remainder of the testing range. In terms of the data lost from the temperature sensor, the readings from $32°C - 32.7°C$ would be inaccurate. To measure the error rate of the output, the schematic and post-layout simulated results were compared to the ideal values over the expected input range, which is shown in figure 5.14.

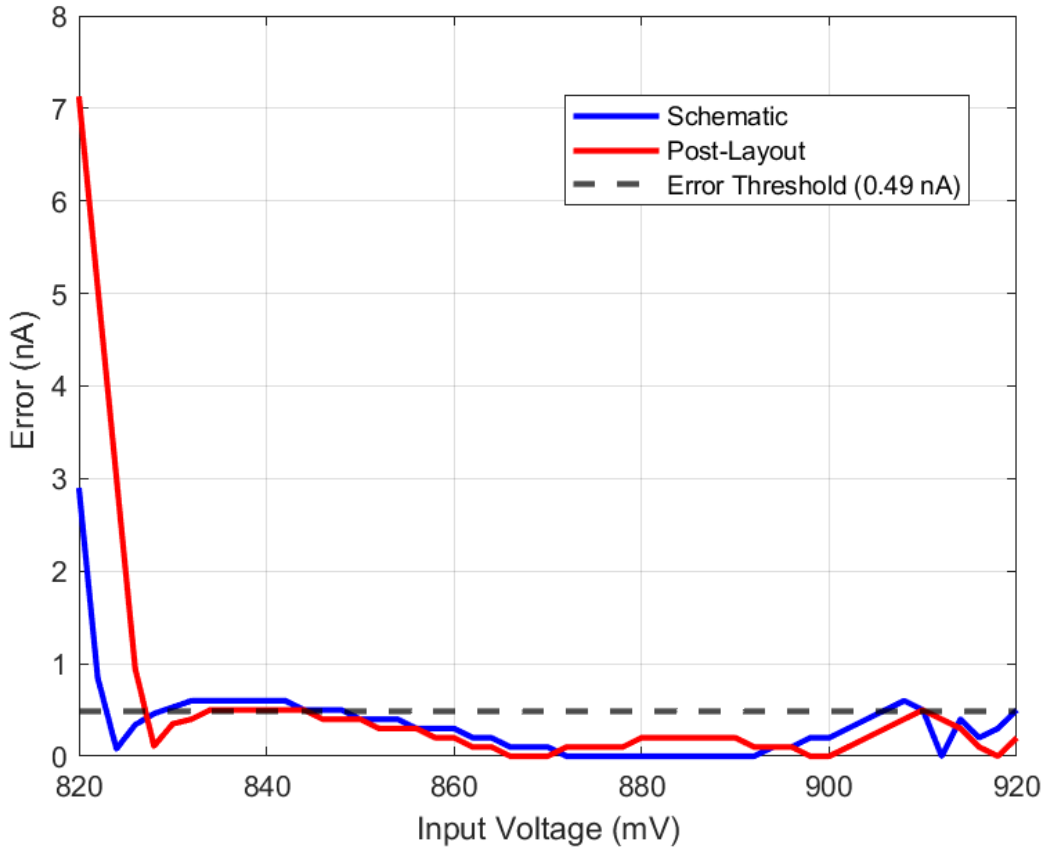


Figure 5.14 – Absolute error in nA vs input voltage for schematic and post-layout simulation

As seen in the figure above, the error is high for both the schematic and post-layout simulation until the $828mV$ point of the input voltage. After that point however, the error remains within the error threshold of the system for the remainder of the input range showing the high precision of the VI converter.

One of the important specifications for the VI converter was that it must have a high load voltage range where the output current will not be affected. This is so that the VI converter can be integrated into the pre-existing AFE for the wearable at any node voltage while operating as expected. The current mirror used was the cascode current mirror from figure 2.7, however it was modified to fit the needs of the stage 2 design. PMOS transistors were used instead of NMOS, and the aspect ratios of the transistors were varied until the desired output was achieved. Figure 5.15 shows the output current for an input of $870mV$ which equated to $50mV$

as the subtracted voltage for both the schematic and post-layout simulation. The load voltage was varied from $0 - 1V$ and the change in output current was observed.

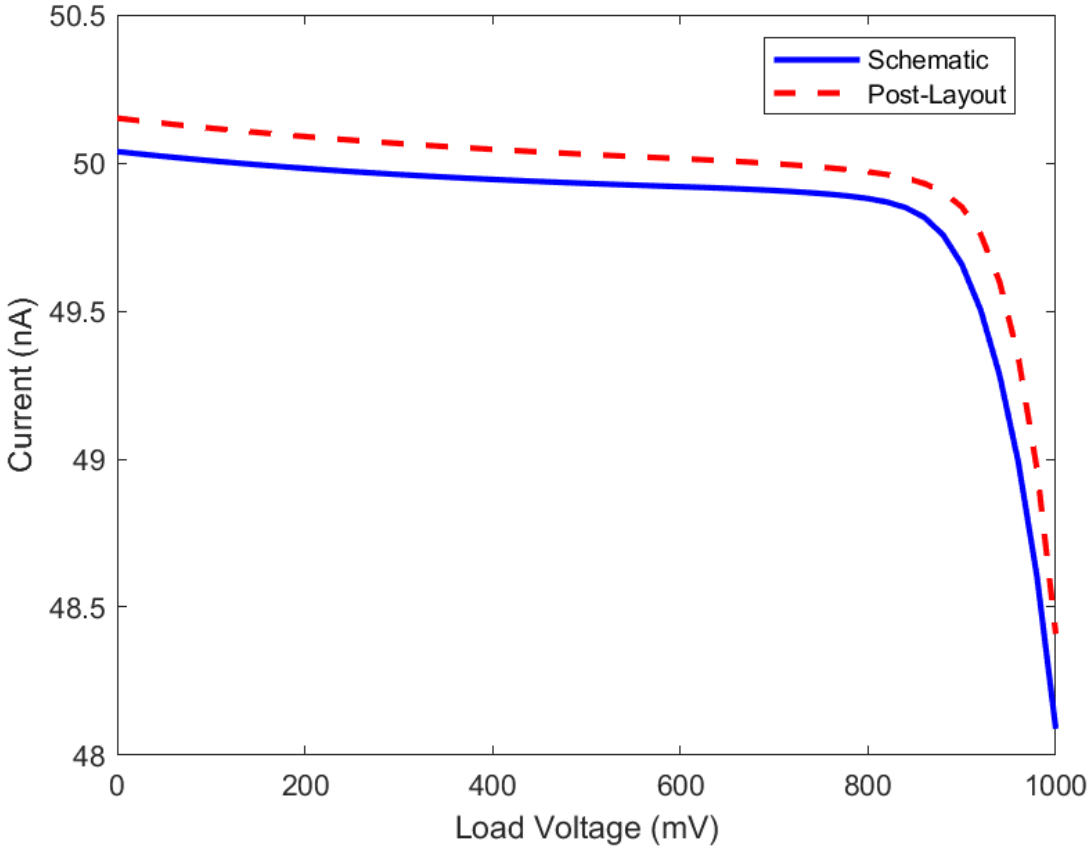


Figure 5.15 – Output current with varied load voltage

Throughout the load voltage range, going from $0V - 900mV$ the output current stays between the acceptable range of $\pm 0.49nA$ of the expected value which in this case would be $50nA$. Even with different input values, the output current behaves in the same manner as shown in figure 5.15. With this, we can say that the VI converter output current is independent of load voltage.

Another specification for the VI converter is that it must be independent of process variations. During the design of each circuit block, measures were taken place to reduce the effects of process variations at each stage. Therefore, it was expected that at the output node of the VI

converter, the process variations are highly controlled. This is further confirmed by figure 5.16 which shows the output current vs the expected input range over the different process corners.

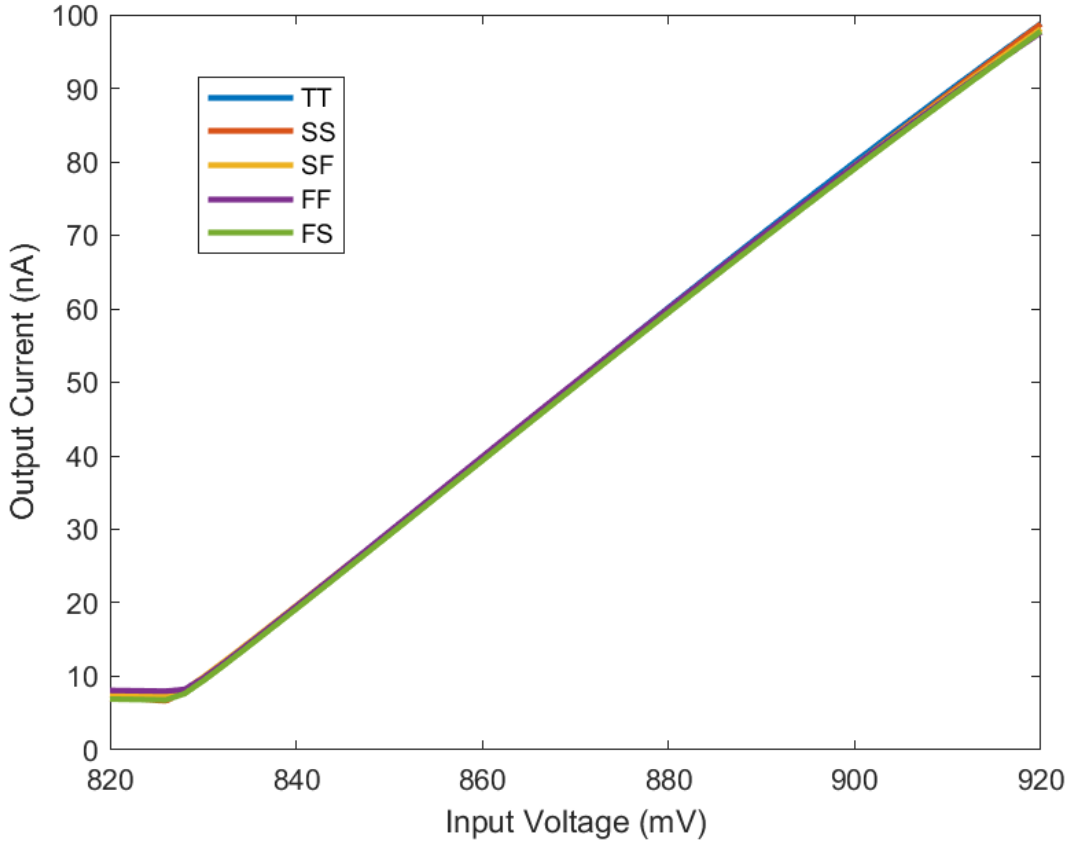


Figure 5.16 – Output current over the different process corners

Overall, the process variations are highly contained through the use of off-chip biasing of the pseudo-resistor which was the largest cause of the variations. Off chip biasing also adds the extra benefit of being able to save space on-chip while also removing elements that could cause variations and consume more power.

Based on the results observed through the simulations, the designed VI converter meets all required specifications that were set. The total power consumption of the VI converter is $61.1\mu W$ while the total area taken up is $122\mu m\ x\ 180.1\mu m$.

Chapter 6 – Conclusion

6.1 – Summary

The designed VI converter allows a temperature sensor to be integrated into the wearable device that our lab is developing. To ensure that the existing AFE can process the data from the temperature sensor, certain specifications were met such as the maximum input range for the current being $0 - 100nA$. Using this as a baseline, a range of $10°C$ was chosen as the temperature sensor MCP9700 has a temperature coefficient of $10mV/C$. This meant that at the output, each nA represents $0.1°C$. Since the core human body temperature fluctuates between $36°C - 37°C$, the temperature range the VI converter would be designed for was $32°C - 42°C$ allowing for lots of headroom in both directions. The output voltage from the temperature sensor for that temperature range is $820mV - 920mV$.

As the VI converter is meant to be implemented in a wearable device, it was vital that the power consumption was low as to not use up too much of the battery, as an important factor of any wearable device is battery life.

To achieve the desired results, the VI converter design was separated into two different stages: the voltage subtractor stage and the current converter stage. The voltage subtractor stage used a simple topology using a low power OTA, a super source following voltage buffer and four resistors in negative feedback. The voltage subtractor took an input of $820mV - 920mV$, and outputs $0 - 100mV$, by using $820mV$ as the reference voltage.

The current conversion stage utilized the same OTA designed in stage 1 in negative with a pseudo-resistor designed to achieve a $1M\Omega$ resistance value. The pseudo-resistor is a tuneable resistor which uses current to tune to the desired resistance value. The cascode current mirror then very accurately mirrors the current to the output branch.

It was vital that the load voltage range of the output branch be high as this ensures that wherever the VI converter is implemented in within the AFE, a change in the load voltage does not affect the output current. A full summary of the VI converter design specifications as well as a comparison to other VI converters found in literature is shown in table 6.1. During the extensive literature review process, current publications with designs of VI converters have normally been very general implementations. The design presented in this thesis was a very application specific design with very specified outputs required in which the output results were very difficult to match to literature. As such, the comparisons made in table 6.1 were based on the closest approximations available. Despite these challenges, the table demonstrates that the presented design exhibits better performance in several key metrics compared to the generalized designs.

6.2 – Future Works

Although the design of the VI converter works incredibly well for the application it was designed for, like any design, there is always room for improvements even in the smallest aspect.

As one of the main design goals of this VI converter was to consume as little power as possible, different methods of achieving that is worthy of further research. In this scenario, due to the pseudo-resistor design chosen to get as close to the $1M\Omega$ resistance value as possible, a secondary power supply rail was added which adds to the total power consumption. Along with that, the OTA was designed with the same negative supply rail such that when used in unity gain, the voltage can follow as close to $0V$ as possible as to not lose data. As such, other pseudo-resistor implementations can be evaluated further in order to remove the need for a secondary source.

By removing the secondary source, not only will it reduce the power consumption, the use of deep-nwell NMOS may not be necessary as well since all NMOS body connections can be

made to ground. This will thereby reduce the overall area of the VI converter as well. Further reductions in area consumption can also be made within the OTA design by using a MOSFET based capacitor for compensation.

Table 6.1 – Summary of results and comparison to literature

Parameter	**[2]FFVA, 2011**	**[4].2016**	**[6].2015**	**[7].2005**	**This work**
Technology	0.18 μm CMOS	0.18 μm CMOS	65nm CMOS	0.35 μm CMOS	65nm CMOS
Supply Voltage	1.2 V	3.3 V	2.8 V	3.3V	1.2 V
Input Voltage Range	$0 - 1.2V$	$1.3V - 3V$	$0.45V$ $- 1.75V$	$1.2V - 2.4V$	$0 - 1V$
Output Current Range	-	$0A - 3.3\mu A$	$30uA$ $- 100uA$	$120\mu A$ $- 260\mu A$	$0 - 100nA$
Power Consumption	$52.87\mu W$	$210\mu W$	$742\mu W$	$2.2mW$	$61.1\mu W$
Area	$0.0102\ mm^2$	$0.0022\ mm^2$	$0.000224\ mm$	$0.12\ mm^2$	$0.021\ mm^2$

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keywords: {Threshold voltage;CMOS integrated circuits;Transconductance;MOSFET;Degradation;Resistors;CMOS technology;voltage-to-current converter;mobility degradation;nonlinearity compensation;Mobility degradation;nonlinearity compensation;voltage-to-current converter (VCC)},

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