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ADVANCES IN PULSE WIDTH MODULATION TECHNIQUES

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A Thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfilment of the requirements for
the degree of Doctor of Philosophy

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ABSTRACT

The phase angle control of the Two-Level Sinusoidal Pulse Width Modulation (SPWM) strategy has been studied in Part I of this thesis, and applied to a new voltage-source type PWM High Voltage Direct Current (HVDC) transmission system. The PWM-HVDC station exercises direct control over the voltage phase angle, the amplitude and the frequency at the ac terminals using the phase angle lock loop (PLL) control of the SPWM. The parallel connection of multi-terminal PWM-HVDC stations can be achieved through simple local feedback control. The feasibility studies for the system, based on laboratory experiments and numerical analysis, are reported in the thesis.

In Part II of the thesis, the Three-Level SPWM technique has been studied and applied to the controls of a 3-phase, 6-valve, current-source PWM rectifier. A new Dynamic Three-Level SPWM strategy together with its Decoupler Pre-Processor has been proposed. The strategy enables each of three phase currents of the converter to be controlled independently and linearly, so that the dynamic feedback can be channelled. The Pole Placement control method has been implemented successfully, using a real-time digital control scheme. The scheme also succeeds in active filtering. The experimental results are obtained from a *1-KVA* size laboratory model with a real-time controller using three TMS320C25 DSPs. The three DSPs operating in parallel are necessary to compute the feedback algorithms with minimum delays so as to ensure sufficient frequency bandwidth.

RÉSUMÉ

La première partie de cette thèse fait l'étude de la commande du déphasage obtenu par la Modulation Par Largeur D'impulsion Sinusoïdale (SPWM) à Deux-Niveaux. Cette technique est implantée pour assurer l'asservissement d' HVDC de type source de tension. La station PWM Haute Tension Continu (HVDC), muni d'un contrôleur en boucle fermé du déphasage du SPWM, exerce un contrôle direct sur l'amplitude, le déphasage et la fréquence de la tension aux terminaux. On pourrait étendre ce type de commande à des stations PWM-HVDC multi-terminaux branchées en parallèle par un simple contrôle local en boucle fermée. Les études de faisabilité de ce système, basées sur des expériences de laboratoire et des analyses numériques, sont documentées dans cette thèse.

La Partie II décrit, la technique SPWM Trois-Niveaux, étudiée et appliquée a la commande d'une source de courant PWM rectificatrice 3-phases, 6-valves. On propose une nouvelle stratégie SPWM Trois-Niveaux dynamique et un Pré-Processeur Découpleur associé. Cette stratégie assure à chacun des courants triphasés du convertisseur une commande indépendante et linéaire, de façon à ce que la boucle fermée dynamique puisse être canalisée. La méthode du Placement de Pôles a été appliquée avec succès en utilisant d'ure part une stratégie de contrôle numérique en temps réel. Et d'autre part le filtrage actif. Les résultats expérimentaux sont obtenus d'un modèle de laboratoire d'ure puissance de *1-KVA* avec un contrôleur en temps réel utilisant trois DSP TMS320C25. Les trois DSP TMS320C25 opérant en parallèle sont nécessaires pour le calcul rapide des algorithmes en boucle fermée, assurant ainsi une largeur de bande suffisante.

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NOMENCLATURE

PART I (CHAPTERS 2, 3 and 4)

v_a, v_b, v_c	Instantaneous phase-to-neutral source voltages
i_a, i_b, i_c	Instantaneous ac line currents
L	Ac line inductance
C_{dc}	Dc link capacitance
V_{dc}	Dc link voltage
PWM	Pulse width modulation
HVDC	High voltage direct current
I_{dc1}	Output rectifier dc current before capacitor C_{dc}
I_{dc2}	Output dc link current after capacitor C_{dc}
v_{pa}, v_{pb}, v_{pc}	Instantaneous phase-to-neutral terminal voltages
$\overline{v}_{pa}$, $\overline{v}_{pb}$, $\overline{v}_{pc}$	Fourier Series fundamental components of voltages v_{pa}, v_{pb}, v_{pc}
$\overline{v}_{mREF}$	Amplitude reference of $\overline{v}_{pa}$, $\overline{v}_{pb}$, $\overline{v}_{pc}$
Δv_{mc}	Amplitude adjusting input of $\overline{v}_{pa}$, $\overline{v}_{pb}$, $\overline{v}_{pc}$
$\overline{v}_{mc}$	Amplitude control variable of $\overline{v}_{pa}$, $\overline{v}_{pb}$, $\overline{v}_{pc}$
ω	Angular frequency
ω_{cREF}	Frequency reference of $\overline{v}_{pa}$, $\overline{v}_{pb}$, $\overline{v}_{pc}$
$\Delta\omega_c$	Adjusting input of frequency
ω_c	Control variable of frequency
θ_m	Phase angle of voltage $\overline{v}_{pa}$
θ_{cREF}	Reference of phase angle θ_m
$\Delta\theta_c$	Adjustment input of phase angle θ_m
θ_c	Control variable of phase angle θ_m
PLL	Phase lock loop
VR	DC voltage regulator

DISP	Power dispatcher
v_{tr}	Peak value of triangular carrier
v_{ma}, v_{mb}, v_{mc}	Instantaneous modulating signals
S_j	Switching function
v_{Tn}	Thevenin equivalent voltage of ac utility system
i_n	Thevenin equivalent current of ac utility system
θ_{Tn}	Phase angle of voltage v_{Tn}
ω_{Tn}	Angular frequency of voltage v_{Tn}
R_{Tn}	Thevenin equivalent resistance of ac utility system
L_{Tn}	Thevenin equivalent line inductance of ac utility system
X_{Tn}	impedance of L_{Tn}
X_L	Local impedance at converter terminal
ϵ_{Vdc}	Error between V_{dcREF} and V_{dc}
P_n	Real power passing through the converter
P_{nREF}	Reference value of P_n
ϵ_{Pn}	Error between P_{nREF} and P_n
K_p	Gain of proportional feedback control
K_i	Gain of integral feedback control
X_{dc}	Impedance of dc link
R_{dc}	Resistance of dc link
X_{c1}	Capacitance at dc terminal
X_{c2}	Capacitance after dc link inductor
i_{n1}	Primary current of station transformer
i_{n2}	Secondary current of station transformer
v_{b1}	Primary fundamental voltage of station transformer
v_{b2}	Secondary fundamental voltage of station transformer
v_{pj}	*rms* value of $\overline{v}_{pa}$, $\overline{v}_{pb}$, $\overline{v}_{pc}$
θ_{n1}	Phase angle between v_{Tn} and v_{b1}
θ_{n2}	Phase angle between v_{b2} and v_{pj}
M	Modulating index

PART II (CHAPTERS 5 and 6)

C	Ac terminal capacitance
L	Ac line inductance
R	Resistance of ac line
L_{dc}	Inductance of dc link
R_{dc}	Resistance of dc link
I_{dc}	Dc link current
i_{pa}, i_{pb}, i_{pc}	Instantaneous terminal input currents
$\bar{i}_{pa}, \bar{i}_{pb}, \bar{i}_{pc}$	Fourier Series fundamental components of currents i_{pa}, i_{pb}, i_{pc}
S_{pa}, S_{pb}, S_{pc}	Control variables of currents $\bar{i}_{pa}, \bar{i}_{pb}, \bar{i}_{pc}$
S_{ma}, S_{mb}, S_{mc}	Modulating signals of Bi-Logic SPWM
$S_{tra}, S_{trb}, S_{trc}$	Triangular carriers of Bi-Logic SPWM
P_{Str}	Peak value of triangular carrier
Y_a, Y_b, Y_c	Tri-Logic PWM variables
X_a, X_b, X_c	Bi-Logic PWM variables
$\bar{X}_a, \bar{X}_b, \bar{X}_c$	Fourier Series fundamental components of signals X_a, X_b, X_c
i_u, i_v, i_w	Instantaneous phase currents in delta-connected voltage source
i_o	Zero sequence current
v_{sa}, v_{sb}, v_{sc}	Instantaneous ac phase-to-neutral supply voltages
v_{so}	Magnitude of v_{sa}, v_{sb}, v_{sc}
i_{sa}, i_{sb}, i_{sc}	Instantaneous ac line currents
$i_{sao}, i_{sbo}, i_{sco}$	Steady-state operating values of currents i_{sa}, i_{sb}, i_{sc}
$\Delta i_{sa}, \Delta i_{sb}, \Delta i_{sc}$	Small perturbation values of currents i_{sa}, i_{sb}, i_{sc}
v_{ca}, v_{cb}, v_{cc}	Instantaneous phase-to-neutral ac capacitor voltages
$v_{cao}, v_{cbo}, v_{cco}$	Steady-state operating values of voltages v_{ca}, v_{cb}, v_{cc}
$\Delta v_{ca}, \Delta v_{cb}, \Delta v_{cc}$	Small perturbation values of voltages v_{ca}, v_{cb}, v_{cc}
$\bar{i}_{pao}, \bar{i}_{pbo}, \bar{i}_{pco}$	Steady-state operating values of currents $\bar{i}_{pa}, \bar{i}_{pb}, \bar{i}_{pc}$
$\Delta\bar{i}_{pa}, \Delta\bar{i}_{pb}, \Delta\bar{i}_{pc}$	Small perturbation values of currents $\bar{i}_{pa}, \bar{i}_{pb}, \bar{i}_{pc}$
i_{so}	Magnitude command of currents i_{sa}, i_{sb}, i_{sc}

PAL	Programmable array logic
DSP	Digital signal processor
ΔT	Sampling period
f_o	Line frequency
f_{tr}	Frequency of triangular carrier
R_{load}	Resistance of dc load
$K_{P\text{-}dc}$	Proportional gain of dc current regulator
$K_{I\text{-}dc}$	Integral gain of dc current regulator

CHAPTER
ONE

INTRODUCTION

1.1 Historical Perspective

Power Electronics began with the vacuum tube diode which made ac to dc rectification possible [1]. The advent of thyratron [1], with the gate-turn-on capability, introduced an element of controllability. By delaying the gating pulse, it became possible to control the amount of the rectified power [2]. The turn-off of the thyratron depended on the negative half of the ac voltage cycle - or what is termed, line-commutation. An entire technology has developed around the line-commutation concept: the *Graetz* bridge [2], the line-commutated inverters [3], the *High Voltage Direct Current* (HVDC) Transmission System [2], the *Static VAR Controller* (SVC) [4,5], the cycloconverters [3].

By the mid-1960s, the solid-state thyristors, i.e., the *Silicon Controlled Rectifier* (SCR) [6] replaced the thyratrons and the mercury-arc rectifiers [1] in the line-commutated technology. Like the thyratrons, the thyristors have gate-turn-on capability but have to be turned OFF by the reversal of the anode-cathode voltage. Apart from line-commutation, this voltage reversal can also be achieved by a force-commutation circuit which turns-on an auxiliary thyristor to connect the reversed voltage from a previously charged capacitor to the principal thyristor [7, 8]. The force-commutated thyristors enable the dc-to-ac inversion to be carried out over a range of operating frequencies for variable speed ac motor drive [9, 10].

As the research in the variable speed ac motor drives progressed, it became clear that the ac voltage amplitude must be coordinated with the motor speed [11]. When the inverter source is a fixed dc voltage or dc current, the amplitude control can be achieved only by *Pulse Width Modulation* (PWM) [12], that is by controlling the relative durations of the ON and the OFF states of the force-commutated thyristors.

Originally the force-commutated thyristor circuits were slow, complex and costly. In the past 15 years, the solid-state industries have produced a range of power switches which have both gate-turn-on and gate-turn-off capabilities [13]. In this thesis, these power switches will be described under the generic term, "Valves". Some examples of these valves are: *Bipolar Power Transistors* (BJT)

[14], power *Metal Oxide Semiconductor Field Effect Transistors* (MOSFET) [15], *Insulated Gate Bipolar Transistors* (IGBT) [16], *Static Induction Transistors* (SIT) [14]. They have a broad range of switching speeds, voltage and current ratings. Tending to be slower but reaching to the higher voltage and current levels are the *Gate-Turn-off Thyristors* (GTO) [17], the *Static Induction Thyristors* (SITH) [18], the *MOS-Controlled Thyristors* (MCT) [19].

The availability of these valves has given a great impetus to the development of the PWM concepts. In addition to controlling the frequency and the amplitude of the modulating signal, the objectives have been broadened to include the control of the Fourier harmonics so as to reduce the motor torque pulsations [11,20,21]. In consequence, there is a rich literature on PWM methods [22], especially on what is described in this thesis as the Two-Level or Bi-Logic PWM [23].

Fig. 1-1 illustrates the Bi-Logic PWM. As the two logic levels are fixed at $+1$ and -1, the degrees of freedom in the specification of the Fourier series

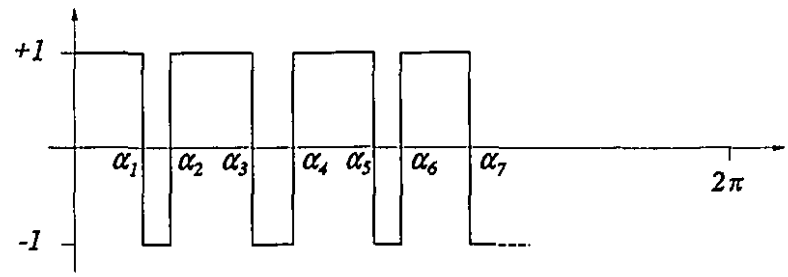


Figure 1-1 Two-Level or Bi-Logic PWM.

components are left to the choice of the switching angles α_1, α_2, $\cdots$ α_N. A good part of the literature is concerned with different algorithms for determining the switching angles. They can be classified as the Static Types and the Dynamic Types. In the Static Type, the switching angles have been determined by optimizing a chosen criterion function. The criterion function specifies the amplitudes of the fundamental and the critical harmonics of interest. The angles are solved by off-line computation in a optimization program and then stored in EPROMs and executed in real-time in the control module of the converter [24-27]. The description "Static" is applied to this class of PWM technique because the PWM waveforms are correct only for the periodic steady-state operating regime.

In contrast, the Dynamic Type of PWM strategies can cope with the transitions from one steady-state to another steady-static operating regime. The *Sinusoidal PWM* (SPWM) method [12], which is used in this thesis, is an example of the Dynamic Type. The modulating signal is sampled, and the algorithm produces a Bi-Logic output whose "local average" of the sampled period is proportional to the sample of the modulating signal. In many aspects, the converter under SPWM control is a sampled linear amplifier.

The research in the PWM strategies has been matched by research in bridge topologies. It is now recognized that the 3-phase, 6-valve bridge converter has two basic topologies: the Voltage-Source Type of Fig. 1-2 and the Current-

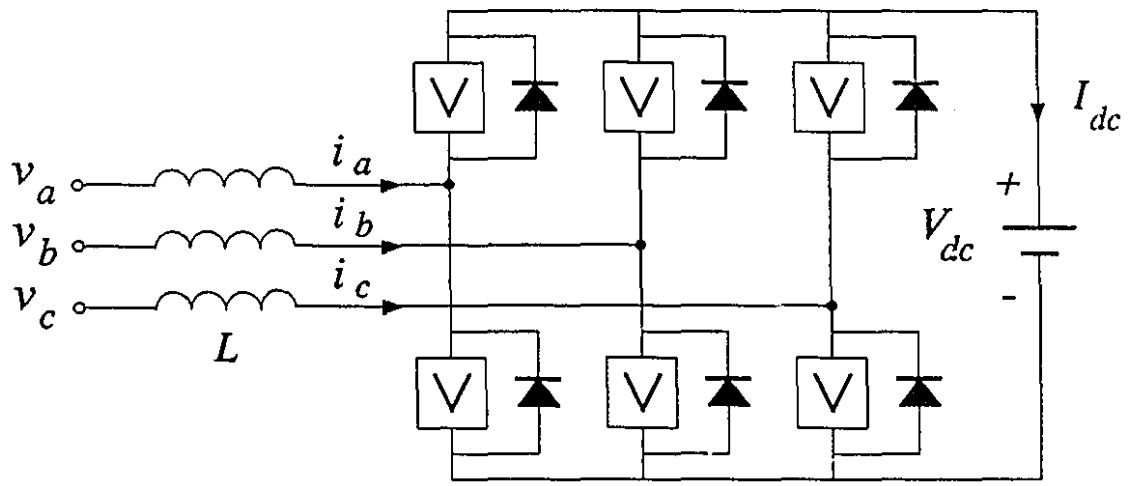


Figure 1-2 The 3-phase, voltage-source PWM power converter topology.

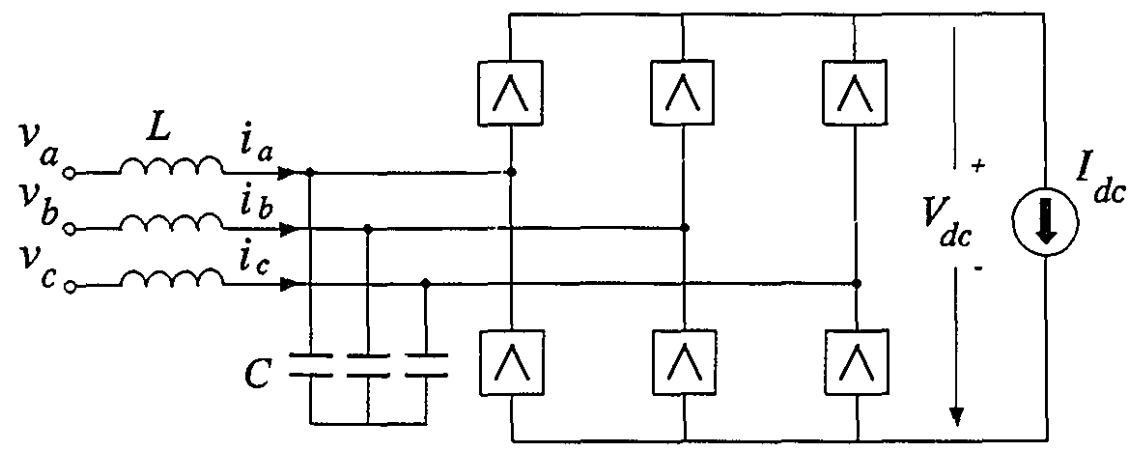


Figure 1-3 The 3-phase, current-source PWM power converter topology.

Source Type of Fig. 1-3, in which the boxed "V" represents the valve and with the arrow-head of the "V" indicating the direction of valve current flow. They are nearly (but not exactly) the circuit theory duals of each other. As such, they have almost complementary characteristics. For example power reversal on the dc side of the bridge is accomplished in the Voltage-Source Type of Fig. 1-2 by current-reversal (dc voltage unidirectional), and in the Current-Source Type of Fig. 1-3 by voltage reversal (dc current unidirectional).

In the past, the Bi-Logic PWM controls of Fig. 1-1 had been applied to control both the Voltage-Source Type (Fig. 1-2) and the Current-Source Type (Fig. 1-3) topologies. While the ac currents of the voltage-source converter came out as well-defined near sinusoidal waveforms [28-37], the valves of the current-source converter could not switch as intended [38-39]. Hombu, Ueda and Ueda [40,41] recognized the reason for the failure in the current-source topology and they have shown that instead of the Bi-Logic PWM, it is necessary to use the Three-Level or Tri-Logic PWM [23], as illustrated in Fig.1-4. The PWM Logic must have three levels: $+1$, 0 and -1. Since then, many research groups [42-46]

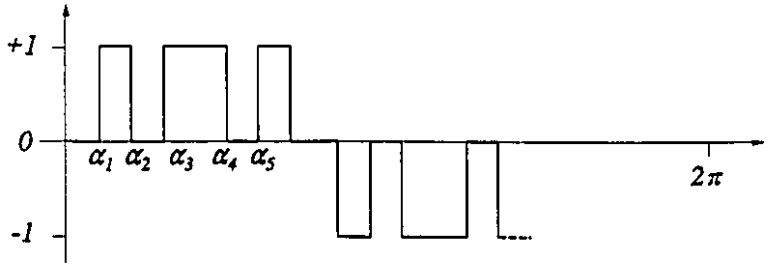


Figure 1-4 Three-Level or Tri-Logic PWM.

began researching on the Tri-Logic PWM. Up to this thesis, the Tri-Logic PWM strategies had been based on the Static Type. Because of the late start of the Tri-Logic PWM, the Current-Source Type PWM bridge converter is relatively backward with respect to its voltage-source dual.

In parallel with the research in modulation techniques and bridge topologies, there have been active interests in applying classical and modern control theories in the inverter-motor drive systems. An outstanding success here is the example of the induction motor which can now form part of a sophisticated machine tool drive because the attributes of fast controllability are conferred to it by vector control feedback [47,48].

All the historical development occurred in a period of transition from analogue to digital circuitry. To avoid the need for repeated component retuning because of their aging and thermal drifts, the trend is to digitize whenever possible. Many of the Static Type of PWM strategies have been implemented using EPROMs supervised by microprocessors [20,21,24-27]. But the early microprocessors had been too slow for the PWM converter applications and real-time digital feedback controls were reduced and limited to the "look-up table" approach. Recently, very fast Digital Signal Processors (DSPs) with facilities for parallel connection have appeared in the market. This offers the opportunity to use the computational power of the parallel DSPs to implement digital control in real-time.

The historical perspective has given a broad picture of the development of Power Electronics. The PWM principle is seen as the key element because it enables the valve to modulate the electric power while meeting harmonic constraints. For this reason, the thesis is focused on making contributions to the PWM Theory, its Applications and its Implementation.

1.2 Review of Previous Work on Pulse Width Modulation

The industrial success of PWM is found mainly in inverter applications in: (1) Variable Speed AC Motor Drives [49] and (2) *Uninterrupted Power Supplies* (UPS). The capability of the PWM inverter to produce variable-amplitude, variable-frequency, high quality voltage/current waveforms has been put to use in sophisticated drives, the notable example of which is the vector control [47,48]. The high quality UPS with closely regulated voltage and frequency is now indispensable for many critical loads such as computer systems and robotic systems [50-53].

Because most of the problems associated with the PWM inverter have been solved, researchers have recently turned their attention to PWM rectifiers. The early research on PWM rectifiers based on the Graetz bridge, began around the end of the 1970s [9,10,54-57]. As the gate-turn-off valves were then not available, the force-commutation of the thyristors were achieved by auxiliary commutation circuits.

Around the mid-1980s, German [28,29] and Chinese [30] researchers, and McGill University initiated research on the PWM rectifier based on the Voltage-Source Topology of Fig. 1-2.

The PWM rectifiers of McGill University were initially implemented using hysteresis-band control of the voltage-source bridge [31-37]. Both the 3-phase and the single-phase rectifiers were studied. These stand-alone rectifiers were capable of: (1) unity power factor operation, (2) near sinusoidal current waveforms, (3) regulated dc voltage, (4) fast response, and (5) bi-directional power transfer. The series of studies identified the design parameters with respect to: (i) waveform distortion limit, (ii) loss of waveform control limit and (iii) instability limit.

Recognizing that the well-known SPWM technique can produce the same quality of waveform at a lower switching rate than hysteresis current control, the research group at McGill University redesigned the rectifier based on the SPWM strategy. Incidentally, this redesign also brought a return in the form of the cost savings of the three high quality current sensors needed in hysteresis current control. In the absence of the information concerning the instantaneous line currents, the redesign needed a feedforward path so as to compute the converter ac terminal voltages required for the line current to be in phase with the ac voltages - so as to operate at unity power factor. The first iteration of the redesign [58] was not entirely successful because the stable operating region was found to be restrictive. The reason for the limited stability region was that the

dynamic term involving a Ldi/dt voltage was left out in the feedforward path. On restoring the missing term in the second iteration [59] of redesign, the stability region was equivalent to that of the hysteresis control.

This experience high lighted the importance that the PWM controller must be a virtual linear amplifier having the frequency bandwidth to channel control information signals, be it feedforward, feedback or active filtering signals.

In anticipation that higher voltage and current ratings will always be asked of the successful PWM rectifier, research towards meeting the higher ratings was pursued based on series and parallel connections of the bridge modules [52,53]. The initial studies based on hysteresis controlled PWM rectifiers have demonstrated, through simulations and experiments, that multi-module connections are feasible [60]. A later study based on the SPWM technique have shown that by phase shifting of the triangular carrier signals, harmonic elimination improves the waveform quality [61]. This is viewed as a significant finding because it will be possible to achieve high quality ac waveforms even when the very slow valves such as GTOs are used in the individual bridge module. By the technique of phase shifting in a large number of bridge modules, the harmonic cancellations remove the low order switching harmonics of the GTOs, while retaining the broad frequency bandwidth of the modulating signal. In fact, this important research conclusion crosses a hurdle giving justification for initiating the study of the PWM High Voltage Direct Current (HVDC) Transmission System in Part I of this thesis.

The existing HVDC Transmission System is based on the line-commutated thyristor technology [2,62,63]. After several decades of research and development, it has become a mature engineering science with applications in under-water transmission links, back-to-back asynchronous links and in very long distance transmission. Many researchers had been alert to the benefits which GTOs and force-commutation could bring to HVDC, especially the capability to operate at leading power factor [64-68]. Their bridge topology was based on the Graetz bridge which is the current-source topology of Fig. 1-3. Since the research pre-dated the work of Hombu, Ueda and Ueda [40,41], it would have failed in practice for want of the Tri-Logic PWM.

In fact, many of the PWM inverters for variable speed drives, which were claimed to be the Current-Source Type, also failed for the same reasons. After Hombu, Ueda and Ueda discovered that the Tri-Logic PWM of Fig. 1-4 had to be used, many Tri-Logic PWM schemes were synthesized [42-46]. These were of the Static Type and were obtained by the optimization of a criterion function which specifies the desired harmonic composition of the steady-state waveform.

In McGill University, following the successful research and development of the Voltage-Source Type PWM rectifiers, work was initiated with the objective of realizing a Current-Source Type PWM rectifier. The research followed a one-to-one equivalencing of Voltage-Source Type PWM rectifier to its circuit theory dual [69-72]. The three parallel legs of the six valves in the bridge of Fig. 1-2 have their equivalents in the form of three series-connected single-phase (4-valve)

bridges. As each single-phase bridge can operate with the Bi-Logic PWM strategy, no serious difficulty has been encountered. Following the successful implementation of the conceptual current-source PWM rectifier, the next challenge is to reduce the three series-connected single-phase bridges (involving 12 valves) to the more economical three parallel 6-valve bridge of Fig. 1-3 [73]. The PWM rectifier based on Fig. 1-3 requires a Tri-Logic PWM strategy. But it cannot be a Static Type. This is because it must be able to implement feedforward and feedback signals so as to operate at unity power factor and regulate the dc side current. Recognizing this challenge, Part II of this thesis is concerned with developing a Dynamic Type, Tri-Logic PWM to operate the 3-phase, 6-valve, current-source type PWM rectifier.

1.3 Scope and Contributions

The objectives of the research, reported in this thesis, are to make contributions to the PWM techniques as applied to Power Electronics in: (1) theory, (2) applications and (3) implementations. The contributions have been made against the background described in the **Historical Perspective** and the **Review of Previous Work.**

In describing the scope and the contributions, the thesis is organized in two parts:

Part I, Chapters 2, 3 and 4, Two-Level or Bi-Logic PWM,

Part II, Chapters 5 and 6, Three-Level or Tri-Logic PWM.

PART I CHAPTERS 2, 3 and 4

1.3.1 Bi-Logic PWM – Theory

In both the Historical Perspective and the Review of Previous Work, mention has been made that the Bi-Logic PWM and the Voltage-Source Type bridge have received considerable research attention especially in inverter drives which employ amplitude and frequency controls. For this reason, the Bi-Logic PWM theory is already at a mature level and this thesis adopts the Sinusoidal Pulse Width Modulation (SPWM) for its own use, because it is the Dynamic Type and it is easy to implement in the laboratory.

The unexplored avenue of research in this thesis is in the third control attribute of SPWM, namely the phase angle control. The phase angle control and the frequency control are not entirely independent because frequency is the time derivative of angle. In the highly inductive, electric power utility environment, the phase angle control is the lever for controlling the real ac power.

1.3.2 Bi-Logic PWM – Application

The application of the phase angle and frequency controls forms the bulk of Part I which is essentially a feasibility study [74-76] of a next generation HVDC Transmission System based on the Voltage-Source Type PWM converter of Fig. 1-2. The phase angle and the frequency controls play a pivotal role in the synchronization, the power dispatch through the converter stations and the voltage

regulation of the PWM-HVDC Transmission System.

As the existing thyristor HVDC Transmission System is based on the Current-Source Type topology, the contributions to the conceptual designs in **Chapter 2** are significant, since the Voltage-Source Topology is a revolutionary departure and there is a little in the way of precedents to follow. Tests using *1-KVA* size laboratory modules (reported in **Chapter 3**) have proven the soundness of the concepts. The experimental research is followed by the parametric studies [77] of **Chapter 4** which demonstrate that the sizes and ratings of the components of the PWM-HVDC station are comparable to those used in the existing thyristor station and therefore the voltage-source PWM-HVDC station is economically not infeasible.

The research has used laboratory-size modules to prove the superior performance characteristics of the Voltage-Source Type PWM-HVDC over that of the existing thyristor line-commutated HVDC. Its proven capability for multi-terminal operation with local controls only cannot be equalled by the thyristor HVDC which requires centralized control and, in consequence, vulnerable remote communication links.

1.3.3 Bi-Logic PWM – Implementation

The conceptual design at the system level (multi-terminal PWM-HVDC) can be successful only when the designs at the sub-system level and the hardware

implementations are successful in the first place. The innovative contribution at the hardware implementation level, in the form of the *Phase Lock Loop* (PLL) controller of Fig. 2-4 and **Appendix A**, is necessary to synchronize the PWM converter to the nominal standard frequency of the utility system. The Phase Lock Loop controller includes channels for introducing phase angle (proportional) feedback and frequency (integral) feedback. At the sub-system level, minor modifications based on the choice of the feedback error signals make the converter station into either the *DC Voltage Regulator* or the *Power Dispatcher*, which are the two building blocks of the Voltage-Source PWM-HVDC Transmission System.

PART II CHAPTERS 5 and 6

1.3.4 Tri-Logic PWM – Theory

The Tri-Logic PWM theory is at such an early stage of its development that the existing methods are the Static Type.

Chapter 5 presents the first definitive Dynamic Type [78]. It is based on a linear transformation of the Bi-Logic PWM signals. Since the specific Bi-Logic PWM is the Dynamic Type, Sinusoidal PWM, it follows that the Tri-Logic PWM is also a Dynamic Type. **Chapter 5** also presents a *Decoupler Pre-Processor* stage, which enables the output signals of the Tri-Logic PWM to be considered as three decoupled linear amplifier outputs, one for each of the three phases.

As all the transformations are linear operations, all the harmonic properties can be predicated from those of the Sinusoidal PWM.

1.3.5 Tri-Logic PWM – Application

The Dynamic Tri-Logic PWM is applied to the realization of the 3-phase, 6-valve, current-source PWM rectifier [73], in **Chapter 6.** The rectifier requires the "linear amplifier capability" of the Dynamic Tri-Logic PWM because it has a feedforward path to implement unity power factor operation, an outer feedback loop for dc current regulation and inner feedback loops for active filtering and fast response performance.

1.3.6 Tri-Logic PWM - Implementation

An important goal of the research is to implement digitally,

(a) the Dynamic Type Tri-Logic PWM strategy and the Decoupler Pre-Processor,

(b) the feedforward and the feedback controls of the Current-Source PWM rectifier.

The hardware components are the 6-valves (Bipolar transistors), their base drives, the associated snubbers, the ac capacitors, the dc inductor of the Current-Source PWM Bridge Converter.

The additional hardware of the controls are:

(i) Programmable Array Logic (PAL) chips, whose outputs are the logic

commands of the base drives and whose inputs come from a multi-DSP platform.

(ii) a multi-DSP platform consisting of three Digital Signal Processors (Texas Instrument TMS320C25s) capable of concurrent computation. This multi-DSP platform has been built by a colleague and Ph.D. candidate Ms. Y. Guo.

From the assembly of hardware components, the goal is to use software programming to realize a versatile range of performance characteristics.

The experiences sought in the research work are:

(1) programming of the PAL chips to implement the Dynamic Tri-Logic PWM and the Decoupler Pre-Processor. The details are described in **Appendix B.**

(2) real-time programming of the Multi-DSP platform to control the hardware as a Current-Source PWM Rectifier. (see **Chapter 6**)

(3) implementation of a "pole-placement" strategy in real time for fast response and active filtering. (see **Chapter 6**)

The implementation has also given opportunity for the exploration of an innovative feedback scheme which has been proved experimentally as very promising in **Chapter 6.**

CHAPTER
TWO

PWM-HVDC TRANSMISSION SYSTEM

2.1 Introduction

There are three attributes in the sinusoidal waveform:

(1) the frequency,

(2) the phase angle,

(3) the amplitude.

When the waveform consists pules of two levels ($+1$, -1), the three attributes are encoded in the pulse widths. So far, the *Pulse Width Modulation* (PWM) concepts, as exploited in Power Electronics, have been concentrated on only two of the three attributes, namely: frequency and amplitude. This is a reflection of the industrial interests in perfecting the variable frequency inverter for variable speed ac motor drives [11].

This chapter is concerned with the contributing to the advances of PWM methodology by demonstrating how all the three attributes can be brought to bear to solve significant engineering problems. The application example chosen here is the *High Voltage Direct Current* (HVDC) Transmission. In including the third attribute, namely: phase angle, into consideration, one needs to be reminded that it is not an entirely independent quantity. This is because the angle is the time integral of the frequency. Also, the phase angle has meaning only in the context of a reference sinusoidal waveform at a common frequency. Thus, the pulsed waveform must be synchronized to the common frequency so that the phase angle can be varied with respect to the reference.

The discussion of the three attributes of the sine wave brings to mind the turbo-generator stations which have to be synchronized to the utility system. Once in synchronism, the Governor-Frequency control shifts the voltage-angle in meeting the power demands [79]. The Field Exciter System adjusts the voltage amplitude in meeting the reactive power demands [79].

This reminder suggests that if the converter stations of the HVDC transmissions can operate with PWM and if PWM can control the frequency and the phase angle, then the real power can be controlled in the same manner as by the turbo-generator stations. As a matter of fact, the power electronic control response would be much faster than the sluggish Governor and Field Exciter controllers [80].

The generator voltage of the turbo-generator is an "active" voltage induced by the rotation of the magnetic flux from the field excitation. The ac voltage of the voltage-source PWM-HVDC converter station is likewise "active" in the sense that it is supported by the dc link voltage. The dc link voltage comes from the electric charge residing across the dc link capacitances. In fact, at least one of the voltage-source PWM-HVDC converter stations is assigned the function of regulating the dc voltage and is the DC Voltage Regulator of Section 2.4.2. Starting from the high quality regulated dc voltage source, the switching of the converter valves using the *Sinusoidal Pulse Width Modulation* (SPWM) strategy assures that the ac voltage is also a high quality ac active voltage.

Just as the field excitation control can be used to vary the ac voltage amplitude of the generator, the amplitude control of the SPWM strategy can be used by the PWM-HVDC converter station in its ac voltage amplitude control. In both situations, the amplitude controls the reactive power. As amplitude control in the SPWM strategy is already well known, this thesis focuses on the phase angle and the frequency control.

The PWM-HVDC converter station is capable of bi-directional power transfer. To complete the analogy, it is worth while mentioning that although in general, the turbo-generator stations are ac power sources only, in the pump-storage application they are also capable of bi-directional power transfer, using Kaplan turbines as reversible "prime-mover" power [79]. The "prime-mover"

power in the PWM-HVDC converter is the dc power. When the voltage-source PWM-HVDC converter station operates as a rectifier/inverter, the ac power is converted to/from the dc power.

The all important characteristic of the voltage-source converter is that the dc voltage is unidirectional so that the bi-directional power reversibility appears as the reversal in the direction of the dc current flow. This property makes the voltage-source PWM-HVDC converters ideally suited for multi-terminal connections as the converter stations can be connected in parallel at their dc sides.

This Chapter is organized as follows:

Section 2.2 describes the voltage-source converter and shows how the dc link voltage produces on the ac side terminals, pulsed voltage waveforms, whose fundamental Fourier Series harmonic are analogous to the generator voltages.

Section 2.3 describes the implementation of the controls of: (1) the frequency, (2) the phase angle and (3) the amplitude of the SPWM.

Section 2.4 describes the feedback control configurations required to make the voltage-source PWM-HVDC converter stations into two basic types of stations in a HVDC system. They are: (1) the DC Voltage Regulator and (2) the Power Dispatcher.

Section 2.5 describes the multi-terminal application in which the voltage-source topology has distinct advantage because each station requires local control only.

2.2 Force-Commutated Voltage-Source Converter Bridge

In the present HVDC transmission system, the converter station consisting of the Graetz bridge [2] mentioned in Chapter 1, depends on line-commutation principle which requires an external ac voltage source, typically the ac utility line, for the negative ac voltage to drive the commutation process. The thyristor valve, like its mercury-arc predecessor, can be turned on with a delay phase angle. It is properly turned off only after its current has fallen to zero with reverse bias voltage across its anode-cathode. Thus the valve switching frequency is constrained by the ac line supply. Near square waveform currents at the same line frequency are drawn from the ac line sources under lagging power factor. The improvement of line harmonics and power factor requires expensive filters. In weak ac systems, the back-to-back rectifier/inverter stations may have to be supplied with leading reactive power. The controls may require additional static VAR compensator [64-68].

The above inconveniences can be removed by employing force-commutation of the thyristors or semiconductor switch devices with gate turn-off capability, such as the GTO (*gate-turn-off thyristor*), which provides one more degree of freedom in control to overcome the limitations in the existing converter station. The force-commutation technique permits the valves of converter to be turned ON and OFF many times during each cycle of the ac line supply. The external ac source voltage is no longer necessary for the proper switching

operations.

Fig. 2-1 shows a simplified circuit diagram of the 3-phase, voltage-source (boost) type PWM converter bridge which is proposed here as the basic model of the new PWM-HVDC converter station in this thesis. In Fig. 2-1, the force-commutated semiconductor valve is represented by the boxed "V" with the arrow-head of "V" indicating the direction of valve current flow. Each valve has an anti-parallel diode. The inductances, L, on the ac side are important because they contribute to the "boost" action which enables rectification to take place. The

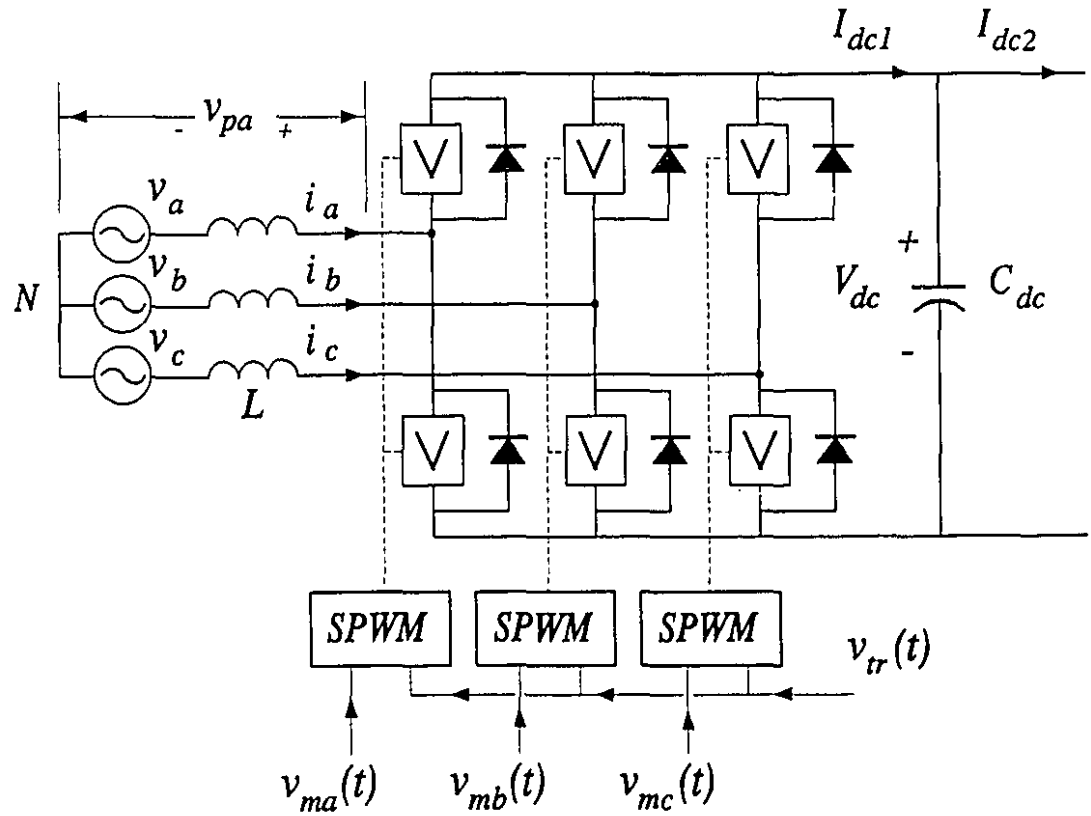


Figure 2-1 Simplified circuit topology of 3-phase, voltage-source, boost type PWM-HVDC converter bridge.

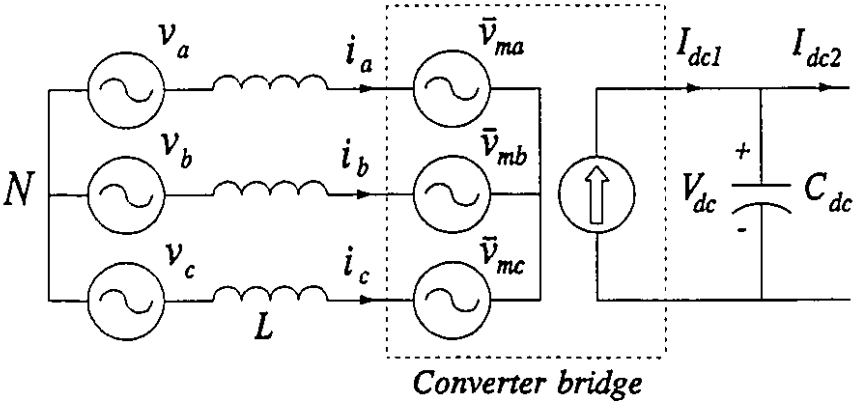


Figure 2-2 The equivalent circuit of voltage-source PWM converter.

power from the ac side is first converted to magnetic energy in the inductances during the ON states of the valves. When the valves are turned OFF, the *Ldi/dt* voltages of the inductances cause the anti-parallel diodes on the opposite side of the branches to conduct, thus admitting the stored magnetic energy to the dc side.

The converter operates with a unidirectional dc link voltage, V_{dc}, across on the dc capacitor, C_{dc}. For proper switching operation, the voltage V_{dc} should be kept large enough to ensure that all the anti-parallel diodes are normally reversed biased and conduction occurs only through the "boost" action [32,37]. The change of the direction of power flow is achieved by the reversal of the direction of the local average dc link current, I_{dcl}. The converter station is viewed as a current source from the dc side, shown by the equivalent circuit of Fig. 2-2.

Compared with the line-commutation technique, the following significant

features in the force-commutated voltage-source PWM converter station are worthy of note:

(i) The ac fundamental terminal voltage $\bar{v}_{pj}(t)$ is an active voltage supported by the dc link voltage. This contrasts sharply with the conventional HVDC which does not provide active ac voltage support at their terminals. Thus in the case where the ac transmission line is long, the voltage drop across the large line impedance results in severe voltage droop at the conventional HVDC terminal.

(ii) The power factor angle can be varied over the 360° range [32,35]. Operation with unity power factor, even leading power factor is not a problem.

(iii) The PWM technique suppresses low order harmonics ac currents. The residual harmonics are in the high frequency end of the spectrum where harmonic filters for them are relatively cheap. The dc output current, I_{dcl}, consists of high frequency pulses which can be filtered out efficiently by the dc link capacitor, C_{dc}. As the current pulses are at high frequencies the capacitor required for filters is relatively cheap. The problem regards to telephone interference of the dc transmission line may not be serious.

(iv) On the dc link side, the converter station operates with a unidirectional voltage, power reversal is accomplished by reversal in the direction of dc link current flow. This property favours parallel connection of several converter stations across a dc bus.

2.2.1 Switching Function S_j

By choosing the switching ON-OFF durations to follow some particular timing pattern, one can control the fundamental and the harmonic components of the ac terminal pulse waveform voltages. Many different kinds of switching control methods have been applied to generate the switching timing pattern [22]. As mentioned before, the Two-Level or Bi-Logic Sinusoidal PWM (SPWM) strategy [23] has been selected here. Fig. 2-3(a) shows the conventional technique of generating SPWM switching control signal using a triangular carrier waveform $v_{tr}(t)$ and a sinusoidal modulating signal $v_{mj}(t)$ ($j=a, b, c$ for the three phases). The intersection points of the two waveforms are used as the instants for sending the ON-OFF gating signals to the Upper and the Lower valves on one of the branches of the 3-phase bridge.

When the modulating signal is higher than the triangular carrier, the switching function S_j is defined as $S_j=+1$ in Fig. 2-3(b), and gating signal is sent to the Upper Valve so that the Upper Valve or Diode is conducting. Similarly, when the modulating signal is lower than the triangular carrier, corresponding to the switching function $S_j=-1$, the Lower valve or diode will be conducting. Each branch has only TWO possible conducting states. Fig. 2-3(c) shows the terminal voltage waveforms, $v_{pj}(t)$, with respect to the neutral point N. It can be expressed as a function of the dc link voltage, $V_{dc}(t)$, and the three phase switching functions, $S_j(t)$:

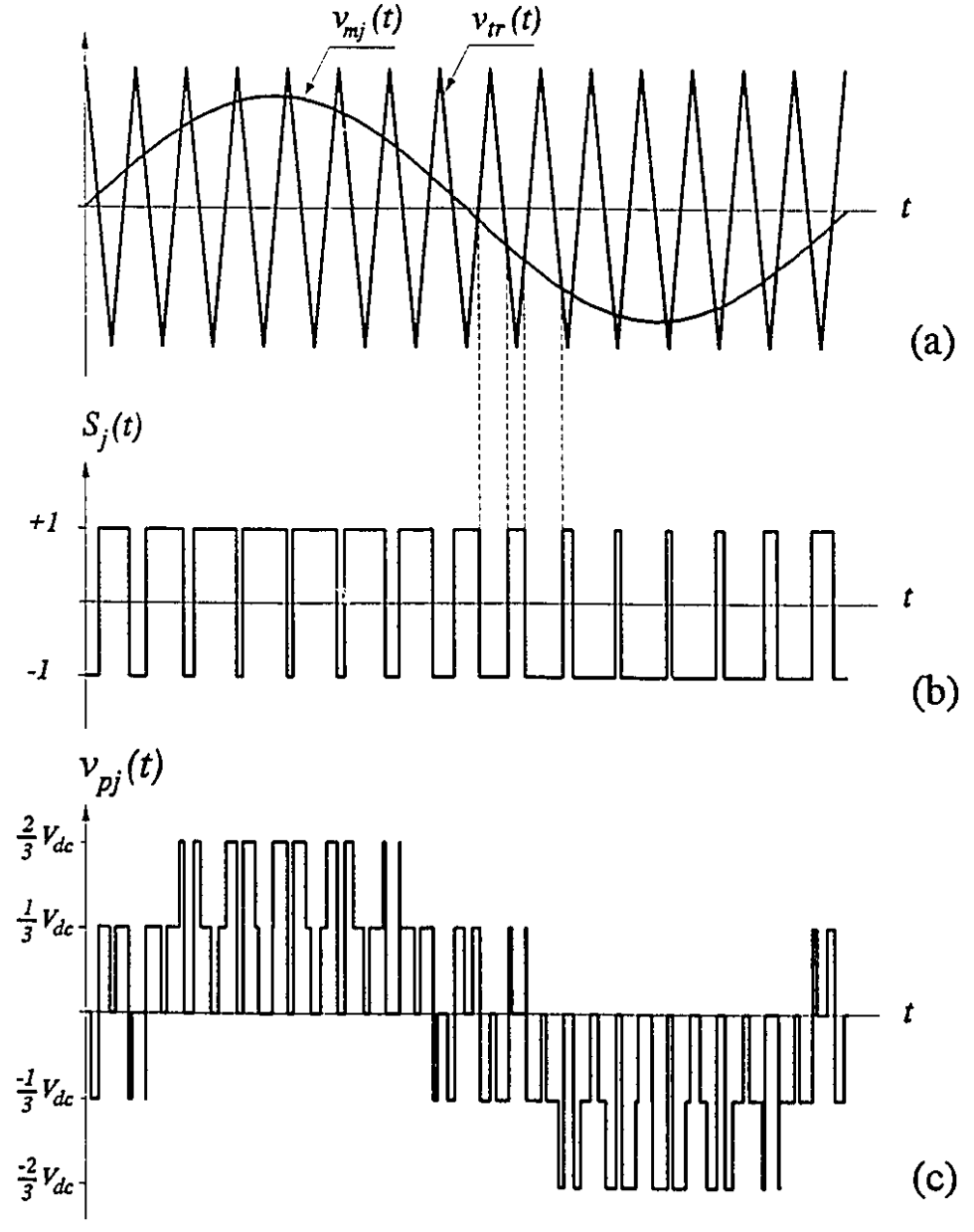


Figure 2-3 (a) Sinusoidal PWM strategy.

(b) Switching function.

(c) Line-to-neutral ac terminal pulse waveform voltage.

$$v_{pj}(t) = \frac{1}{6}\left(3\, S_j(t) - \sum_{k}^{a,b,c} S_k(t) \right) V_{dc}(t) \quad , \qquad j = a,\ b,\ c \qquad (2.1)$$

Note that S_k (k=a, b, c) describe the switching states of the other valves in the other branches. Since the dc link voltage can be normally considered as constant, the fundamental Fourier Series component of the ac terminal voltage $\bar{v}_{pj}(t)$ will be determined by the fundamental Fourier Series component of the switching functions, which is linearly proportional to the magnitude of the sinusoidal modulating signal waveform $v_{mj}(t)$. It is well known [81] that for the case of balanced three phase sinusoidal modulating signals, the fundamental Fourier Series component of the pulsed voltage of the *j*th phase will be:

$$\bar{v}_{pj}(t) = 0.5\, \frac{v_{mj}(t)}{V_{tr}}\, V_{dc} \quad , \qquad j = a,\ b,\ c \qquad (2.2)$$

V_{tr} is the peak value of the triangular carrier waveform. The important feature is that the ac fundamental terminal voltages, $\bar{v}_{pj}(t)$, have the same frequency and phase angle as the sinusoidal modulating signals $v_{mj}(t)$. Thus for constant V_{tr} and V_{dc} , the voltages $\bar{v}_{pj}(t)$ can be seen as the outputs of a 3-phase linear power amplifier with the modulating signals $v_{mj}(t)$ as input signals.

As shown in Fig. 2-1, the blocks labelled "SPWM" handle the gating functions for the valves of the converter bridge with the input modulating signals of $v_{ma}(t)$, $v_{mb}(t)$ and $v_{mc}(t)$.

2.3 Control of Voltage-Source Type PWM-HVDC Converter Station

Based on the voltage-source type PWM converter bridge Fig. 2-1, Fig. 2-4 adds the control schematic by which the voltage amplitude, the frequency and the phase angle of the fundamental component of the ac terminal pulse waveform voltages can be fully adjusted by the three command signals $\overline{v}_{mc}$, ω_c and θ_c, respectively.

In Fig. 2-4, the basic sinusoidal waveform templates of the three phases are stored in binary digits in the *A*, *B*, and *C Electronically Programmable Read Only Memories* (EPROM's). In the laboratory implementation, the angular period 0-2π is divided into $2^9=512$ segments. Corresponding to the binary address *K*, the *K*th memories of the *A*, *B*, and *C* EPROM's contain the values of $sin(2\pi[K/512])$, $sin(2\pi[(K/512)-(2/3)])$ and $sin(2\pi[(K/512)+(2/3)])$, respectively. As the counter number (modulo *512*) increases from $K=0$ to $K=511$, the contents of the EPROM's are passed through the *Digital-to-Analog* (D/A) converters. Their analog outputs generate fine stepped approximations of the basic balanced 3-phase sinusoidal waveforms.

2.3.1 Voltage Amplitude Control

Since the dc link voltage V_{dc} is regulated at its constant reference value in the PWM-HVDC transmission system, based on Eq. (2.2), the amplitudes of the ac terminal voltages are adjusted by varying of the amplitudes of the modulating

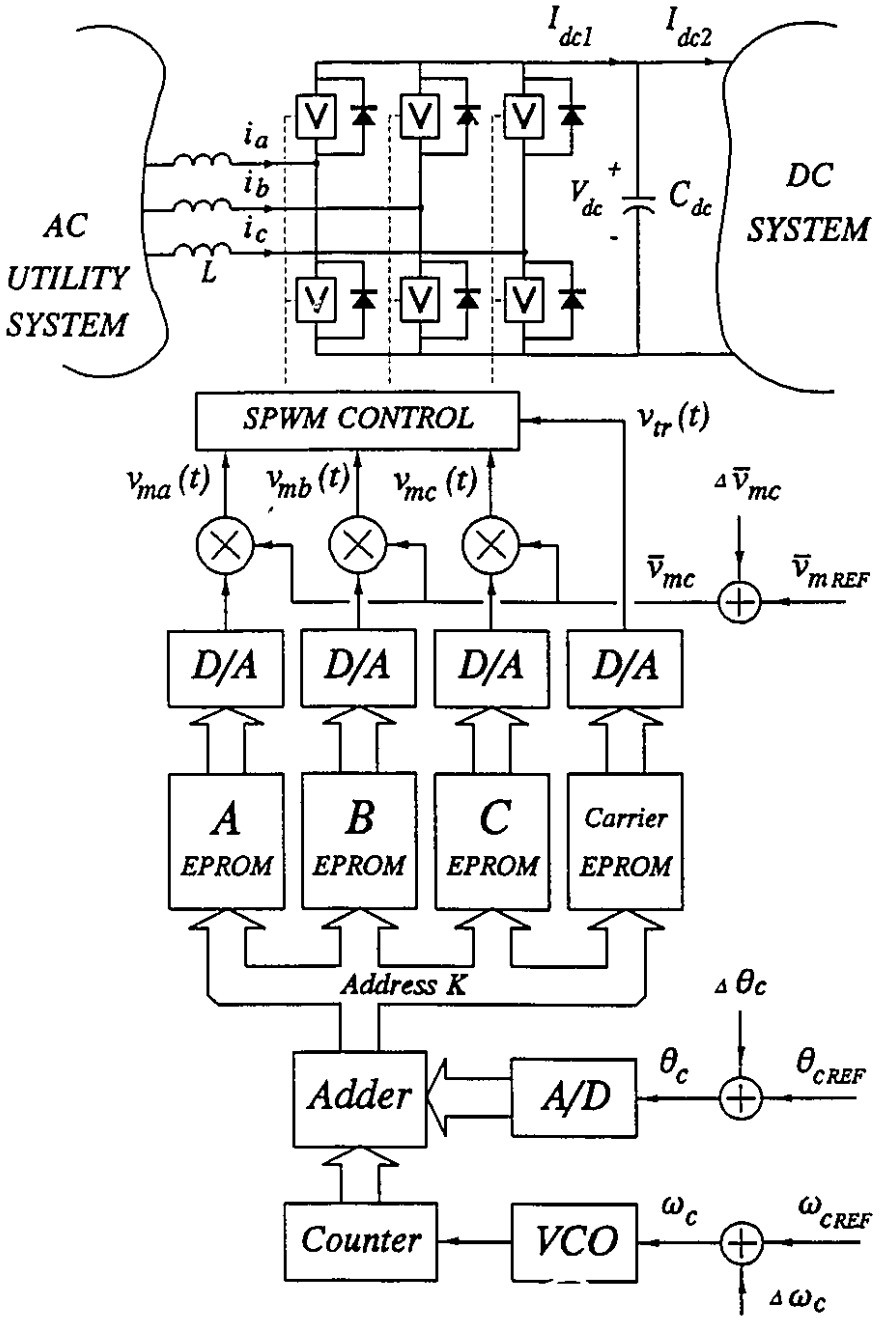


Figure 2-4 Schematic of voltage-source PWM-HVDC converter station with controls on voltage amplitude, frequency and phase angle.

signals in the SPWM functions. The amplitudes of the modulating sinusoidal signals are introduced by multiplying the outputs of the D/A converter from the *A*, *B*, and *C* EPROM's by the amplitude command signal, $\bar{v}_{mc}$, through the electronic multipliers. The modulating waveforms are compared with the triangular carrier waveform which is also generated by the D/A output of the triangular carrier EPROM with a constant peak value. In the laboratory implementation, the carrier EPROM contains the discretized form of *18* isosceles triangles in the same period of *512* counts.

2.3.2 Frequency Control

The four EPROM's are addressed simultaneously by the number *K*. As shown in Fig. 2-4, the number *K* is the sum of two binary numbers. The binary number contained in the binary counter (modulo *512*), receiving the pulse from the *Voltage Controlled Oscillator* (VCO), belongs to the channel in which the frequency is controlled. When the frequency command signal ω_c increases or lowers the pulsing rate of the VCO, the basic sinusoidal waveforms generated by the EPROM's will be cycled at a higher or a lower frequency.

The PWM-HVDC converter station should be able to generate the voltage whose frequency is identical to that of the ac utility system in Fig. 2-4. The frequency control signal ω_c provides this degree of independent control.

Since the address number $K=0, 1, 2 \cdots 511$, corresponding to the period

$\theta=0\text{-}2\pi$ of the sinusoidal modulating signals, the counting rate of the number K is associated with the angular frequency ω. The binary counter performs the function of an *integrator*. The phase angle θ_m of the waveforms generated by the EPROM's of Fig. 2-4 is related to signal ω_c by:

$$\theta_m(t) = \theta_m(0) + \int_0^t \omega_c(\tau)\, d\tau \tag{2.3}$$

To synchronize with the utility system, not only must the converter station have the same frequency, but it must also bear a constant voltage phase angle with respect to the Thevenin voltage equivalent representing the remainder of the utility. From Eq. (2.3), one sees that the frequency control ω_c is an indirect controller by which the constant phase angle can be secured.

Fig. 2-5 illustrates the situation when the converter station and the utility system are initially synchronized, i.e., both initially have the same frequency $\omega_c = \omega_{Tn}$ in Fig. 2-5(a) and the same voltage phase angle $\theta_m = \theta_{Tn}$ in Fig. 2-5(b). ω_{Tn} and θ_{Tn} are the frequency and phase angle of the voltages of the utility system. The voltage phase angle graphs of Fig. 2-5(b) are essentially the integral of the frequency graphs of Fig. 2-5(a). One sees that by momentarily increasing or decreasing the frequency of the VCO, the voltage phase angle can be advanced or retarded with respect of the utility's. At the end of the jogging, the frequencies are identical and the voltage phase angle remains constant.

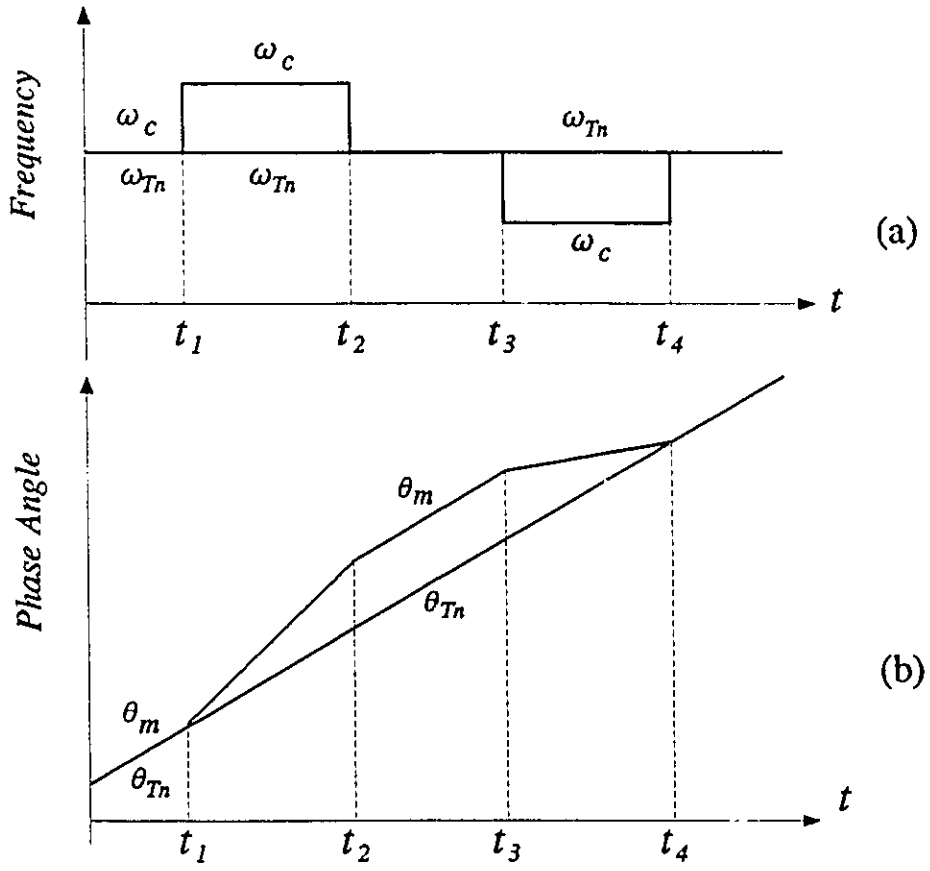


Figure 2-5 Illustration of integral voltage phase angle control by frequency jogging. (a) frequency versus time, (b) phase angle versus time.

2.3.3 Voltage Phase Angle Control

The other component of the binary address K in Fig. 2-4 comes from the direct phase angle shift control. The voltage phase angle shift command signal, θ_c, is translated into binary number by an *Analog-to-Digital* (A/D) converter, then added to the contents of the binary counter of the VCO. A change in the address number K can be made proportionally to the signal θ_c, thus providing a

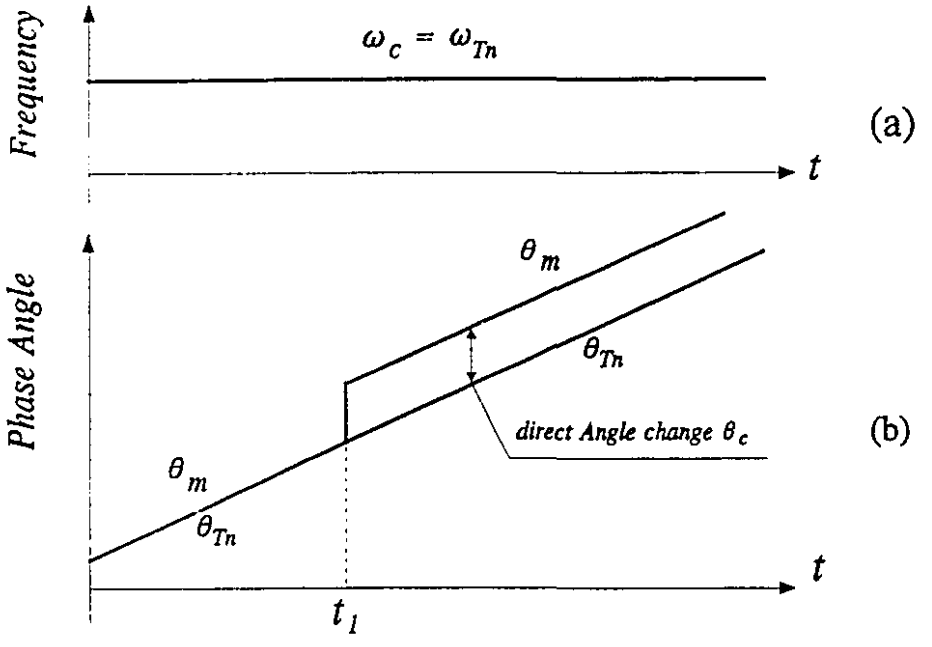


Figure 2-6 Illustration of proportional voltage phase angle control.
(a) frequency versus time, (b) phase angle versus time.

proportional control channel for the voltage phase angle regulation.

Fig. 2-6 illustrates the initial states of the converter station and the utility after synchronization. A step input θ_c is then introduced in the converter while keeping ω_c constant. The phase angle θ_m of the sinusoidal waveforms generated by the EPROM's is shifted instantly. Together with Fig. 2-5, one sees that the ω_c and θ_c are two independent channels of integral and proportional controls for the phase angle θ_m :

$$\theta_m(t) = \theta_c(t) + \theta_m(0) + \int_0^t \omega_c(\tau)\, d\tau \qquad (2.4)$$

2.3.4 Control Input Settings

As shown in Fig. 2-4, each of the signal inputs to the voltage amplitude, the frequency and the phase angle controls, consists of a reference value setting terminal and an additional terminal by which a feedback signal can be added. The reference signals are $\bar{v}_{mREF}$, θ_{cREF} and ω_{cREF} and the feedback signals are $\Delta\bar{v}_m$, $\Delta\theta_c$ and $\Delta\omega_c$ so that:

$$\begin{aligned} \bar{v}_{mc} &= \bar{v}_{mREF} + \Delta v_{mc} \\ \omega_c &= \omega_{cREF} + \Delta\omega_c \\ \theta_c &= \theta_{cREF} + \Delta\theta_c \end{aligned} \tag{2.5}$$

$\bar{v}_{mREF}$ is the reference setting by which the amplitude of the fundamental terminal voltage of the converter station is adjusted so as to be equal to the utility line voltage. ω_{cREF} is set at the nominal synchronizing frequency (*60* or *50 Hz*). Initially, the frequency difference is introduced through the terminal $\Delta\omega_c$ to synchronize the converter station to the utility prior to closing the circuit breakers. θ_{cREF} is initially set equal to zero. The synchronization condition is achieved through the amplitude and frequency adjustments. The circuit breakers are closed when the voltages across the breakers are zero. Once the circuit breakers are closed, the $\Delta\theta_c$ and $\Delta\omega_c$ terminals are used as the *Proportional* and *Integral* (P-I) feedback channels.

The 3 degrees of controllability over the ac terminal fundamental voltages provide the PWM-HVDC converter station with the same attributes of the

Generator station [79]. For example, the voltage phase angle can be used for real power control as is done by the *Automatic Governor System* [79]. The voltage amplitude can be used in reactive power control as is done by the *Field Excitation System* [80]. In addition, the duties of *Power System Stabilizer* [79] for dynamic enhancement can also be incorporated through the feedback terminals. In fact, the converter station should surpass the performance of the generation station because that it is not encumbered by the long time constants of the governor and field excitation systems.

2.4 Converter Station Regulation Scheme

Fig. 2-7 shows, on a single line diagram, the voltage-source PWM-HVDC converter station connected to an ac utility system which is represented by a

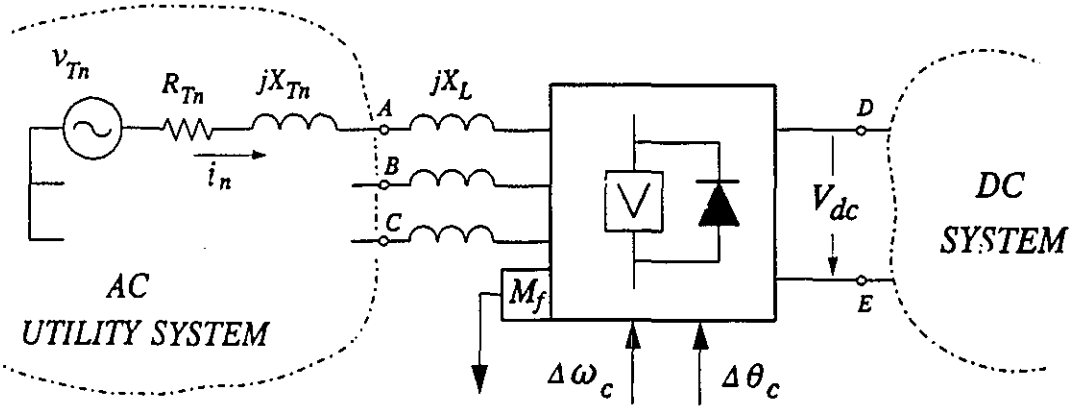


Figure 2-7 Voltage-source PWM-HVDC converter station connected to an ac utility system.

Thevenin equivalent voltage $v_{Tn} \angle \theta_{Tn}$ and the Thevenin equivalent impedance $R_{Tn}+jX_{Tn}$. A black box with the control inputs $\Delta\theta_c$ and $\Delta\omega_c$ and a feedback measurement box labelled M_f is now used to represent the more detailed schematic of the PWM-HVDC converter station of Fig. 2-4. The ac terminals are A, B and C, and the dc terminals are D and E. The impedance jX_L is the local inductance, i.e., the leakage inductances of transformer and some additional inductance, at the ac terminals of the PWM-HVDC converter station. As the R_{Tn} and the jX_L are usually very small compared to the jX_{Tn}, they are neglected to simplify the mathematical equations. It is assumed that the dc side has a sustained dc voltage V_{dc}, which as will be shown in Section 2.4.2, will be regulated.

Because of the large inductive reactance in the utility circuits, the real power transferred by the converter station is must effectively handled through varying the voltage phase angle $\theta_n=\theta_{Tn}-\theta_m$, while keeping the ac terminal voltage amplitude $\bar{v}_{pj}$ constant by simply fixing the reference setting $\bar{v}_{mREF}$. This is illustrated through the phasor diagram of Fig. 2-8, where the voltage amplitude of the PWM-HVDC converter station $\bar{v}_{pj}$ is made equal to the amplitude of the Thevenin voltage $|v_{Tn}|$. Assuming $R_{Tn}=0$ and $jX_L=0$, the voltage drop $jX_{Tn}|i_n|$ is the closing side of the voltage triangle subtended by the phase angle θ_n. The current i_n makes an angle $\theta_n/2$ between the two voltage phasors. It is well known that the power transferred and subsequently converted from ac to dc is:

$$P = \frac{3\,|v_{Tn}|\,|\bar{v}_{pj}|}{X_{Tn}} \sin(\theta_{Tn}-\theta_m) \tag{2.6}$$

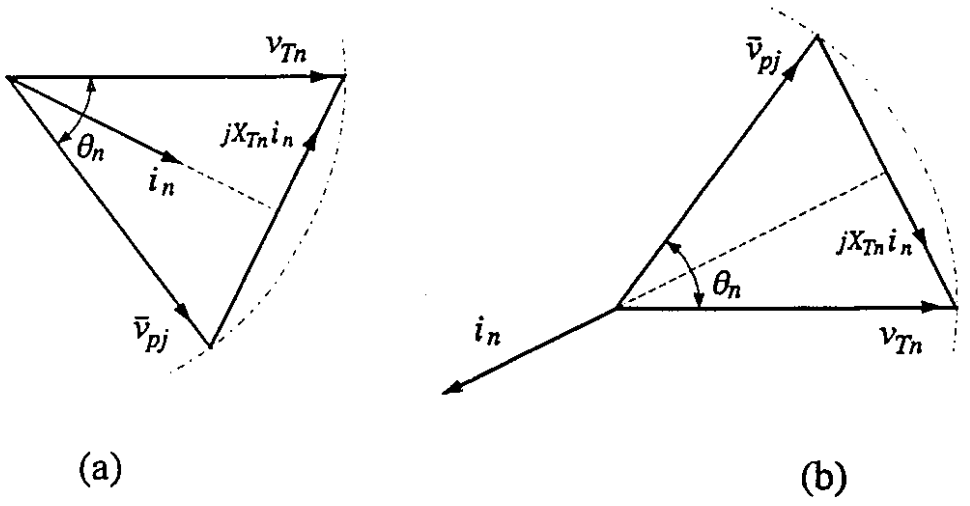


Figure 2-8 Phasor diagram of Fig.2-7. (a) rectifier operation, (b) inverter operation.

Thus the power can be simply regulated by varying the voltage phase angle θ_m. Figs. 2-8(a) and (b) show that for negative and positive values of $\theta_n = \theta_{Tn} - \theta_m$, the PWM-HVDC converter station is operating as a rectifier and an inverter respectively.

Because the ac utility system is an integrated pool of a large number of generator stations and loads which are changing dynamically, $v_{Tn} \angle \theta_{Tn}$ and the Thevenin equivalent impedance are fluctuating in time. Although the frequency reference setting is assigned at the standard *50* or *60 Hz*, there is a slow and very small but finite drift. In addition, the VCO characteristics and the tolerances in the circuit component parts in the schematic of Fig. 2-4 are also prone to drift.

2.4.1 Voltage Phase Angle Lock Loop

In order for the PWM-HVDC converter station to operate in a dynamic environment of fluctuating frequency and voltage phase angle of the utility system, it must have a *Voltage Phase Angle Lock Loop* (PLL) which ensure that the ac system and the dc system will hang together. Negative feedback is a classical method of designing against sub-system fluctuations and drifts. The design philosophy is based on using the voltage phase angle to control the real power. As has been mentioned previously, the voltage phase angle can be controlled directly through θ_c and indirectly after integration through ω_c. Thus the terminals $\Delta\theta_c$ and $\Delta\omega_c$ in Fig. 2-4 will be used for introducing the proportional feedback and integral feedback respectively. Based on the design objective, the feedback loops can be configured to make the converter station into either a power dispatcher or a dc voltage regulator.

2.4.2 DC Voltage Regulator

It has been tacitly assumed previously that the dc link voltage V_{dc} exists which is obtained by charging the dc capacitor, C_{dc}, connected on the dc link in Fig. 2-4. It is because the dc link voltage exists, that the active ac terminal voltage $v_{pj}(t)$ is supported and guaranteed. For this reason, at least one of the PWM-HVDC converter stations connected on the dc link has to be assigned to the function of *DC Voltage Regulator* (VR).

From Fig. 2-4. the capacitor charging current is:

$$C_{dc}\frac{d}{dt}V_{dc}(t) = I_{dc1}(t) - I_{dc2}(t) \tag{2.7}$$

where $I_{dc2}(t)$ is the dc load current and $I_{dc1}(t)$ is the dc pulse waveform output current of the PWM-HVDC converter station. Integrating this equation:

$$V_{dc}(t) = V_{dc}(0) + \frac{1}{C_{dc}}\int_0^t \left(I_{dc1}(\tau) - I_{dc2}(\tau) \right) d\tau \tag{2.8}$$

where $V_{dc}(0)$ is the voltage evaluated at $t=0$, due to charging from an earlier period:

$$V_{dc}(0) = \frac{1}{C_{dc}}\int_{-\infty}^0 \left(I_{dc1}(t) - I_{dc2}(t) \right) dt \tag{2.9}$$

The dc voltage regulation loop is shown in Fig. 2-9(a). It is based on measuring the dc link voltage $V_{dc}(t)$ and after comparing it with the voltage reference V_{dcREF}, the error:

$$\epsilon_{V_{dc}}(t) = V_{dcREF} - V_{dc}(t) \tag{2.10}$$

is used as a negative feedback signal to control the voltage phase angle directly and indirectly through the inputs $\Delta\theta_c$ and $\Delta\omega_c$ so as to null the error $\epsilon_{Vdc}(t)$.

In order to maintain the dc link voltage at the constant reference value V_{dcREF}, it is required that the DC Voltage Regulator has to be able to convert the same amount of real power to replace the power which has been drained by other converter stations placed across the dc link so as to ensure that the local average

current I_{dc1} is balanced with the load current I_{dc2} :

$$I_{dc1} = I_{dc2} \tag{2.11}$$

This means that the phase angle of the ac terminal voltage θ_m is adjusted by the negative feedback until the power from the ac utility satisfies the power demand $V_{dc}I_{dc2}$, so that the charge across the dc link capacitor is remains constant at the desired level. Otherwise the dc link capacitor would be overcharged or discharged. The ac power converted to dc power (or vice versa) is always just sufficient to make up for the dc output power leaving (or entering) the dc terminals. Thus when the PWM converter station is made into a DC Voltage

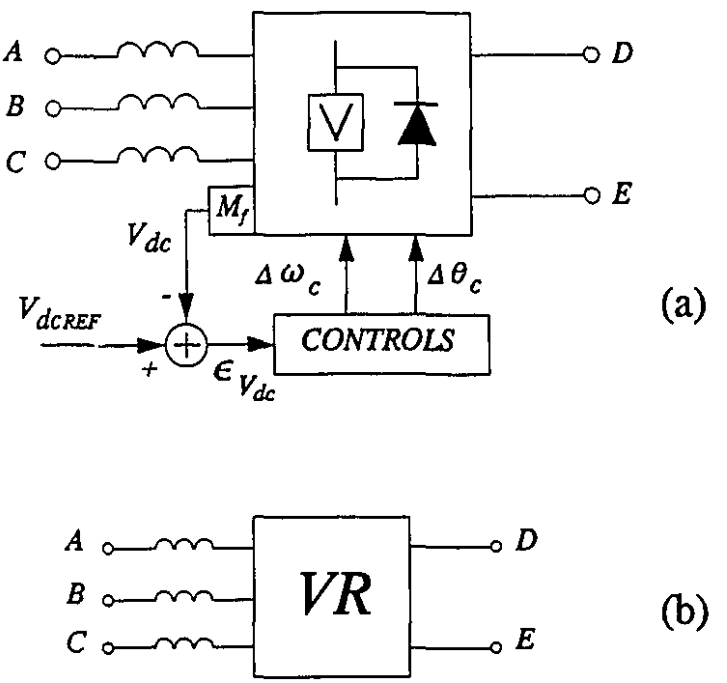


Figure 2-9 (a) Schematic of DC Voltage Regulator (VR), (b) block diagram representation of (a).

Regulator, it is automatically a power slack. The right amount of ac power is converted by the DC Voltage Regulator to satisfy the power requirements of other converter stations connected on the dc link. When all the other converter stations are assigned to rectifier function, the DC Voltage Regulator automatically assumes its role of an inverter.

2.4.3 Power Dispatcher

Fig. 2-10(a) shows the feedback loop configuration for the implementation of a *Power Dispatcher* (DISP). The converter station is assigned the duty of

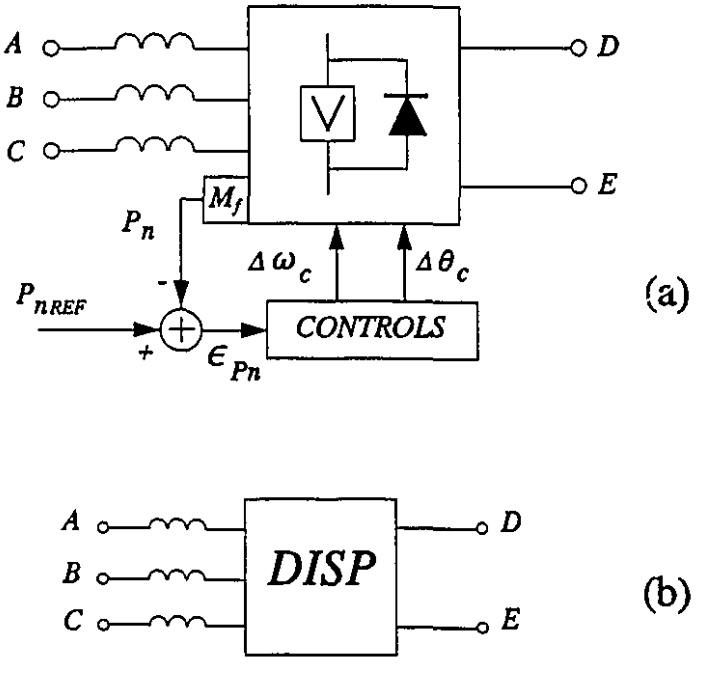


Figure 2-10 (a) Schematic of Power Dispatcher (DISP), (b) block diagram representation of (a).

converting a fixed amount of real power, P_{nREF}. Rectifier or inverter role is designated by the positive or negative sign in P_{nREF}. The real power P_n passing through the converter station is measured by the transducer of box M_f in Fig. 2-10(a) and after comparing it with the reference, the error:

$$\epsilon_{Pn} = P_{nREF} - P_n \tag{2.12}$$

is used as a negative feedback signal to the proportional input of $\Delta\theta_c$ and the integral input of $\Delta\omega_c$ to increase or to decrease the terminal voltage phase angle θ_m until the error ϵ_{Pn} is nulled.

During the power regulation, the dc link voltage is kept at desired level by the DC Voltage Regulator mentioned above. As in the DC Voltage Regulator. the Power Dispatcher is regulated by changing the voltage phase angle only while keeping the terminal voltage amplitude constant.

As the frequency reference setting ω_{cREF} is set near to the *60* or *50 Hz* of the ac utility system, the feedback loop in the Power Dispatcher of Fig. 2-10(a) or the DC Voltage Regulator of Fig. 2-9(a) automatically locks the frequency of the converter station to that of the ac system. This is because the VCO (*Voltage Controlled Oscillator*) in the feedback loop tracks the system frequency through the voltage phase angle lock loop (PLL) action.

2.5 Multi-Terminal PWM-HVDC Transmission System

Since the voltage-source type PWM converter stations maintain unidirectional voltage in the face of bidirectional power flow, their dc terminals can be connected in parallel to a pair of voltage buses to form a multi-terminal dc network. Based on the feedback control configurations of Sections 2.4.2 and 2.4.3, two building blocks:

(1) the DC Voltage Regulator (VR) in Fig. 2-9(b),

(2) the Power Dispatcher (DISP) in Fig. 2-10(b),

are used to construct a multi-terminal HVDC system, as in the example shown in Fig. 2-11. The *D* and *E* terminals of the PWM converter stations are connected in parallel to a dc grid. A number of ac utility system can be integrated through the dc grid. As illustrated in Fig. 2-11, four ac systems (which may be at different frequencies) are interconnected by the dc grid through five converter stations. The ac system ("*Z*") is integrated at two points through stations *#4* and *#5*.

The dc link voltage is regulated by the DC Voltage Regulator (*VR*), station *#1*. Since the dc link voltage is the sine-qua-non of the system, any short circuit fault across the dc lines must be isolated by the circuit breakers. The strong point in this multi-terminal system is that, in Fig. 2-11, each of the converter stations can invert or rectify power. The two building blocks, the Power Dispatcher and the DC Voltage Regulator, enable inter-system power exchanges, requiring only

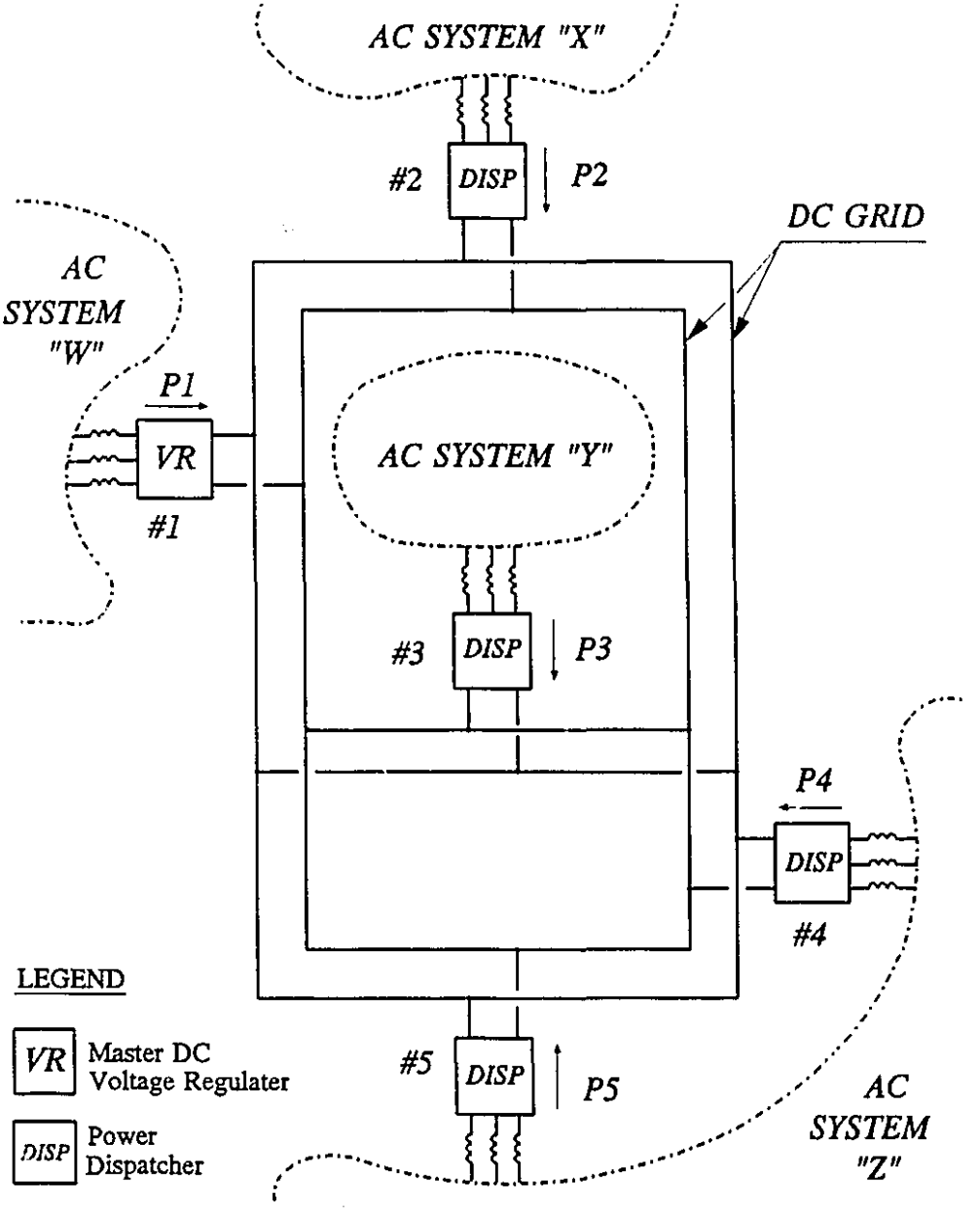


Figure 2-11 Multi-area ac system united by a dc grid through parallel connections of DISP and VR.

the local controls of the feedback loops discussed in Sections 2.4.2 and 2.4.3.

Converter stations *#2*, *#3*, *#4* and *#5* in the example of Fig. 2-11 are Power Dispatcher units. It is assumed that ac systems *"X"*, *"Y"*, and *"Z"* have decided to sell or purchase fixed schedules of power P_2, P_3, P_4 and P_5 at these converter stations. Rectification or inversion are respectively represented by the positive or negative sign in the power designation.

The four ac systems *"W"*, *"X"*, *"Y"* and *"Z"* can exchange power through the five converter stations through the dc grid. The power balance (neglecting ohmic losses) is always satisfied:

$$P_1 + P_2 + P_3 + P_4 + P_5 = 0 \tag{2.13}$$

As already mentioned, the DC Voltage Regulator is a power slack. In maintaining the assigned reference voltage, it delivers (as a rectifier) or absorbs (as an inverter) the left-over power of the other stations in the grid, so that Eq. (2.13) is satisfied at all times.

The dc voltages at the *D* and *E* terminals of the Power Dispatchers, differ from those of the DC Voltage Regulator by the voltage drops across the dc line resistances. The capacitors across the *D* and *E* terminals of each DISP station filter out the current ripples. The charge across the capacitor of each DISP station also supports the dc voltage which through the PWM switching of the valves becomes the active 3-phase voltages on the ac terminals of the converter station.

2.6 Summary

A new PWM-HVDC transmission system has been presented in this chapter. It is based on the voltage-source (boost) type PWM converter station with a control scheme which incorporates the voltage phase angle lock loop (PLL) technique.

On the ac side, the PWM-HVDC converter station has direct and independent control over the fundamental Fourier Series component of its ac line voltages as regards to the amplitude, the phase angle and the frequency. This enables the converter station to interact with the utility system in the same way as a generator station. On the dc side, the PWM converter stations are connected in parallel. Through simple local PLL feedback control, the converter station is made into one of two building blocks: either as a Power Dispatcher (DISP) or as a DC Voltage Regulator (VR). The local feedback is sufficient to co-ordinate HVDC power assignments.

The next chapter will present experimental results from *1-kVA* size laboratory models which show that the concepts of the PWM-HVDC transmission system are realizable and that the characteristics are worthy of attention.

It should be pointed out that this thesis has focused on the voltage phase angle control only. In consequence, Part I has been preoccupied with the management of the real power. In the power utility environment, the voltage

amplitude control is important for the management of the reactive power. While reactive power control is a subject for research, it has not been pursued because this thesis is concerned with Advances in PWM Techniques.

CHAPTER
THREE

EXPERIMENTAL TESTS OF PWM-HVDC

3.1 Introduction

In the previous chapter, the concepts of the multi-terminal HVDC transmission system based on the voltage-source type PWM converter station have been presented. This chapter describes the experimental work which have been pursued to demonstrate that these concepts of the PWM-HVDC transmission system are technically sound and that the voltage-source (boost) type PWM converters have certain operational characteristics which are impossible to achieve in the conventional line-commutated thyristor HVDC transmission system.

The tests were performed on two identical *1-kVA* size, bipolar transistor laboratory models of the voltage-source type PWM converter bridges, each of which was fitted with the controls of Fig. 2-4 in **Chapter 2.** One converter had

the feedback of Fig. 2-9 so that it operated as a DC Voltage Regulator (VR) and the other was made into a Power Dispatcher (DISP) of Fig. 2-10. The two units were connected as a back-to-back asynchronous tie at the mid-point of a transmission line between two 3-phase voltage sources as shown in Fig. 3-1. The transmission lines were represented by lumped impedances jX_{Tn}. The effect of the length of the transmission line was studied by varying the values of the inductive reactance jX_{Tn}. The dc link voltage was set at *110 Vdc* by the reference control V_{dcREF}, in the DC Voltage Regulator. The power was varied by changing the power reference setting, P_{nREF}, in the Power Dispatcher.

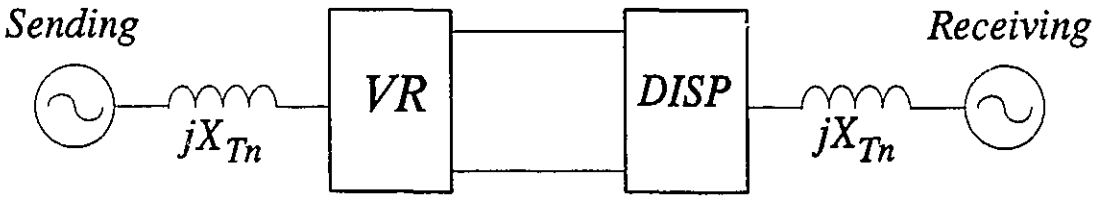


Figure 3-1 Single line diagram of back-to-back dc link consisting a DC Voltage Regulator (VR) and a Power Dispatcher (DISP) situated at mid-point of transmission line.

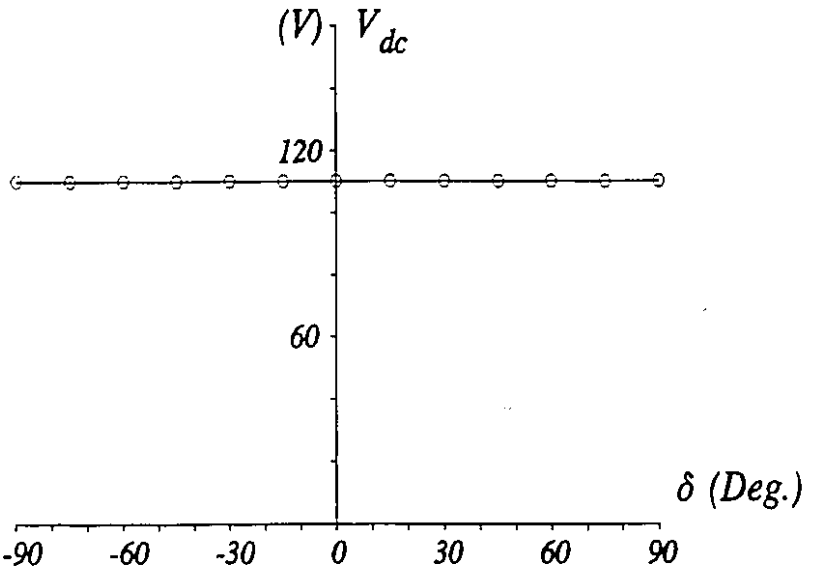
3.2 Synchronization Tests

The union of the converters in Fig. 3-1 to the ac sources is possible only when the voltage phase angle lock loop (involving VCO in Fig. 2-4) of each converter station makes its autonomous frequency synchronize with the frequency

of the ac utility system. The load and network topology changes in the ac utility system are modelled as variations in its Thevenin equivalent voltage and the Thevenin equivalent impedance at the ac terminals of the converter station. The voltage phase angle lock loops in Fig. 2-9 and Fig. 2-10 are intended to keep the converters synchronized in spite of the slow drifts in voltage phase angle and frequency.

The voltage phase angle drift of the ac utility system was simulated by interposing a 3-phase phase-shifting transformer between the ac voltage source and the transmission line impedance jX_{Tn} in Fig. 3-1. Measurements of dc link voltage across the Voltage Regulator were plotted, shown in Fig. 3-2, against the phase angle drift, δ, introduced by the phase shifting transformer. There was no change in V_{dc}. Similar results were obtained when the phase angle shifting transformer was transferred to the Power Dispatcher side. The power remained constant in spite of the voltage phase angle changes. Referring to Fig. 2-8, one concludes that when the phase angle of voltage v_{Tn} is changed the converter voltage v_{pj} will follow it in order to maintain a fixed phase angle θ_n. This insensitivity to the voltage phase angle drift of the ac utility system is a property of the feedback through the frequency ω_c channel which essentially is an integral feedback loop.

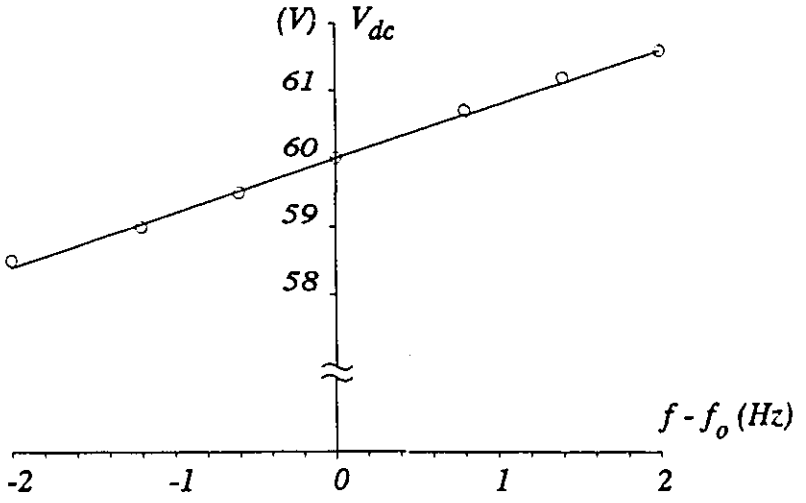
The effect of frequency deviation on the Power Dispatcher (DISP) and DC Voltage Regulator (VR) is depicted in Fig. 3-3 and Fig. 3-4 respectively. The



(V_{ac} =35 V_{rms}, V_{dcREF} =110 V, L_{Th}=0.01362 H, I_{dc}=3 A)

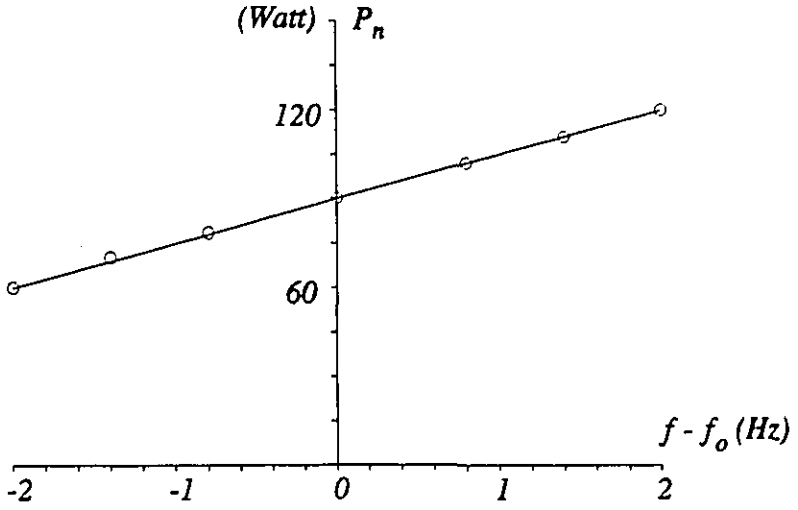
Figure 3-2 DC link voltage of DC Voltage Regulator (VR) as a function of voltage phase angle δ introduced by a phase shifting transformer between ac source and converter.

frequency deviation may arise from the gradual but minor drifts of the ac utility system or from the parameter changes with respect to temperature of the components in Fig. 2-4 itself. In the experimental tests, the utility's *60 Hz* was unaltered. The frequency deviation was introduced by adjustment of the frequency reference setting, ω_{cREF}, in Fig. 2-4. Fig. 3-3 and Fig. 3-4 show that when a frequency difference exists, the converter continues to remain synchronized by virtue of a non-zero feedback voltage $\Delta\omega_c$. This implies that the error in the regulator loop cannot be zero and this is confirmed by the sloped



(V_{ac} =20 V_{rms}, V_{dcREF}=60 V, L_{Th}=0.01362 H, I_{dc}=1.9 A, K_p=0.2, K_i=8.3)

Figure 3-3 DC link voltage of DC Voltage Regulator (VR) as a function of frequency deviation.



(V_{ac} =20 V_{rms}, V_{dcREF}=60 V, L_{Th}=0.01362 H, I_{dc}=1.5 A, K_p=0.1, K_i=25)

Figure 3-4 Power output of Power Dispatcher (DISP) as a function of frequency deviation.

straight lines in Fig. 3-3 and Fig. 3-4.

The K_p and K_i given in Fig. 3-3 and Fig. 3-4 are proportional and integral feedback gains in the $\Delta\theta_c$ and $\Delta\omega_c$ channels respectively.

3.3 Real Power Control

The DC Voltage Regulator was assigned a constant reference control voltage, $V_{dcREF}=110\ Vdc$. The power was varied through the reference setting, P_{nREF}, of the Power Dispatcher. The dc power and the voltage phase angle were measured experimentally. Fig. 3-5 shows the dc link power plotted against the voltage phase angle of the DC Voltage Regulator. The theoretical lines are based

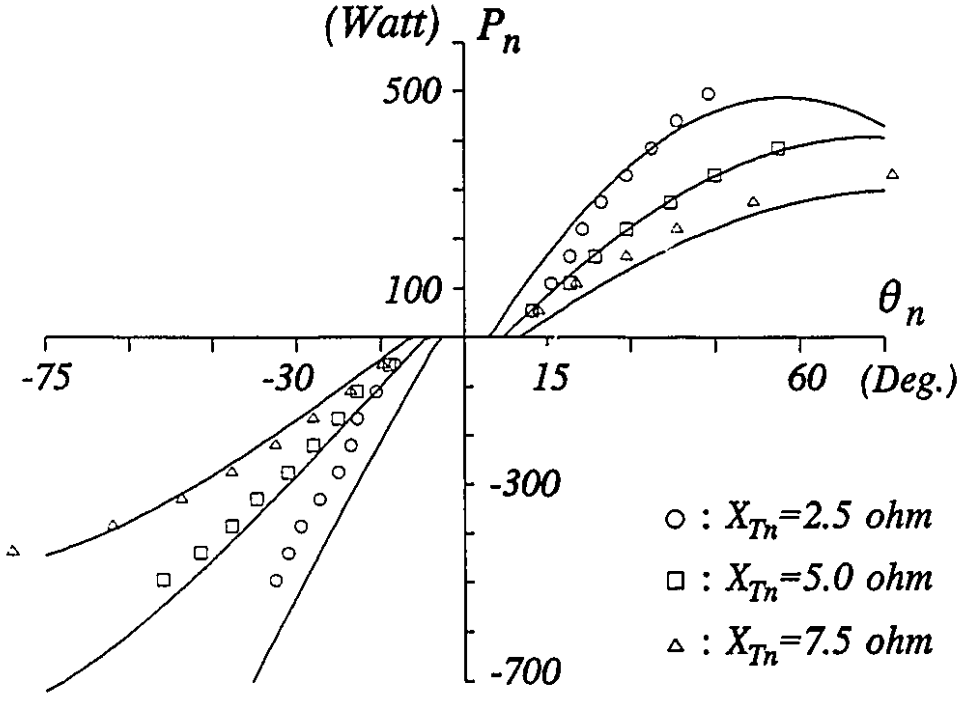


Figure 3-5 DC link power versus voltage phase angle characteristics.

on the well known formula of the real power, Eq. (2.6), when the transmission line impedance, the sending and receiving end voltage magnitudes and phase angle are known. The switching losses of the valves account for the zero power output between *-10* and *+10* degrees in Fig. 3-5. The estimated switching losses are deducted from the theoretical curves. The theoretical curves and the experimental points show reasonable agreement.

The following features have been demonstrated by the experimental results:

(1) Real power control is accomplished by the voltage phase angle control. (This follows the same practice as in the ac generator station.)

(2) The changeover from rectifier to inverter operation is achieved by changing the voltage phase angle from positive to negative value. On the dc side, the dc link voltage remains constant and it is the flow of the local average dc link current I_{dcl} that reverses direction.

(3) The Dc Voltage Regulator is a power slack. In order to ensure that the capacitor voltage is charged at the present reference voltage, the DC Voltage Regulator converts the power necessary to replace the amount taken by the Power Dispatcher.

(4) There are active ac voltages at the terminals of the converter which are supported by the dc link voltage from the capacitor charges, and therefore there is no voltage droop or collapse as in conventional HVDC.

(5) As the ac transmission distance increases, jX_{Tn} increases. From Fig. 3-5 one sees that in order to transmit same power it is necessary to increase the voltage phase angle. The steady-state stability limits are defined by the extremum points in the curves. For $jX_{Tn}=7.5$ ohm, one sees that ± 75 degrees have been recorded as experimental points which lie within the steady-state stability limit.

By situating the back-to-back PWM-HVDC link midway between the sending and receiving ends of a long weak ac transmission system, it is possible to double the power capability of the ac lines. The experimental points at ± 75 degrees for $jX_{Tn}=7.5$ ohm in Fig. 3-5 demonstrate this as a fact. The total transmission reactance is *15* ohm, with *7.5* ohm between the sending-end and DC Voltage Regulator and another *7.5* ohm between the Power Dispatcher and receiving-end. The total voltage phase angle between the sending-end and the receiving-end is $75^\circ + 75^\circ = 150^\circ$, which exceeds the stability limit of *90* degrees.

3.4 Transient Tests

A number of tests were conducted to prove that the Power Dispatcher (DISP) and DC Voltage Regulator (VR) coordinate their functions during transients using their local feedback controls only.

Fig. 3-6 is the photograph of the oscillogram taken at the DC Voltage Regulator, when a step reversal of demand from a negative (inverter) to a positive

(rectifier) value was applied to the power reference setting, P_{nREF}, of the Power Dispatcher. Initially the DC Voltage Regulator operated as an rectifier (positive dc link current I_{dc}) and then it changed to inverter operation (negative dc link current I_{dc}) in response to the power step change in the Power Dispatcher. Thus it operated as a power slack and ensured that the demands of the Power Dispatcher were satisfied promptly by the local voltage regulator feedback loop. Fig. 3-6(a) shows the fundamental harmonic voltage, and by comparison one sees that the line current in Fig. 3-6(b) is a very good sinusoidal current. Fig. 3-6(c) shows the voltage phase angle, θ_n, which controls the power change during the

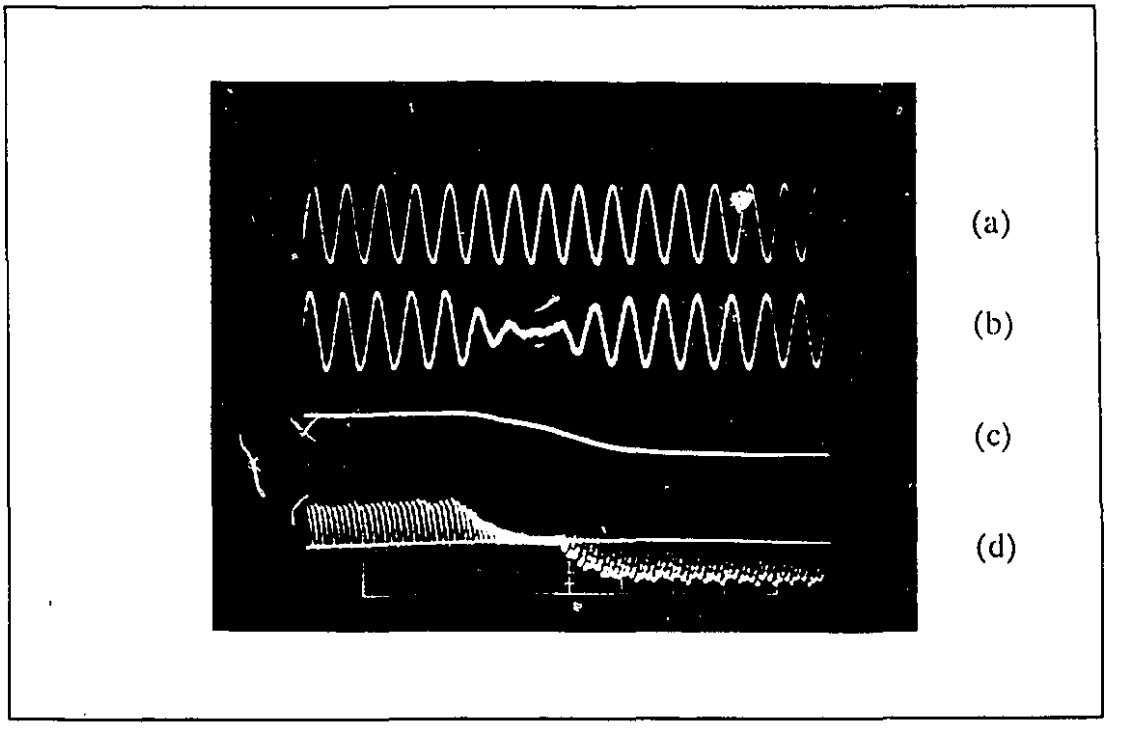


Figure 3-6 Transient waveforms in DC Voltage Regulator during power reversal: (a) fundamental harmonic voltage, (b) ac line current, (c) voltage phase angle, (d) dc link current.

transient (there is a slight delay in the voltage phase angle transducer). Fig. 3-6(d) shows the dc link current, I_{dc1}, immediately at the converter output terminal. The ripples of I_{dc1} have been filtered by the dc link capacitor so that the output dc current, I_{dc2}, would not cause communication channel interference. The dc link current is positive during rectification and negative during inversion as is evident in Fig. 3-6(d).

An experiment to simulate multi-terminal (3-station) HVDC operation was performed. Based on the circuit of Fig. 3-1, in the beginning, the Power Dispatcher (DISP) was assigned to deliver a fixed amount of inverter power. The DC Voltage Regulator (VR) automatically assumed the role of a rectifier. Fig. 3-7 shows the oscillogram of (a) the ac current, (b) the dc link current of the DC Voltage Regulator, (c) the ac current and (d) the dc link current of the Power Dispatcher (DISP). As shown in Fig. 3-7, the initial portions of the dc link currents of VR and DISP are respectively positive (rectifier) and negative (inverter). A step power demand of the third station in the dc link was simulated by connecting a resistance across the dc link. From Fig. 3-7(c) and (d) one observes that the Power Dispatcher fulfilled its assigned power in spite of disturbance from the third station. The additional power consumed by the simulated third station was taken up by the DC Voltage Regulator. From Fig. 3-7(a) and (b), it is apparent that the DC Voltage Regulator increased its rectified power so as to accommodate the step power demand of the third station.

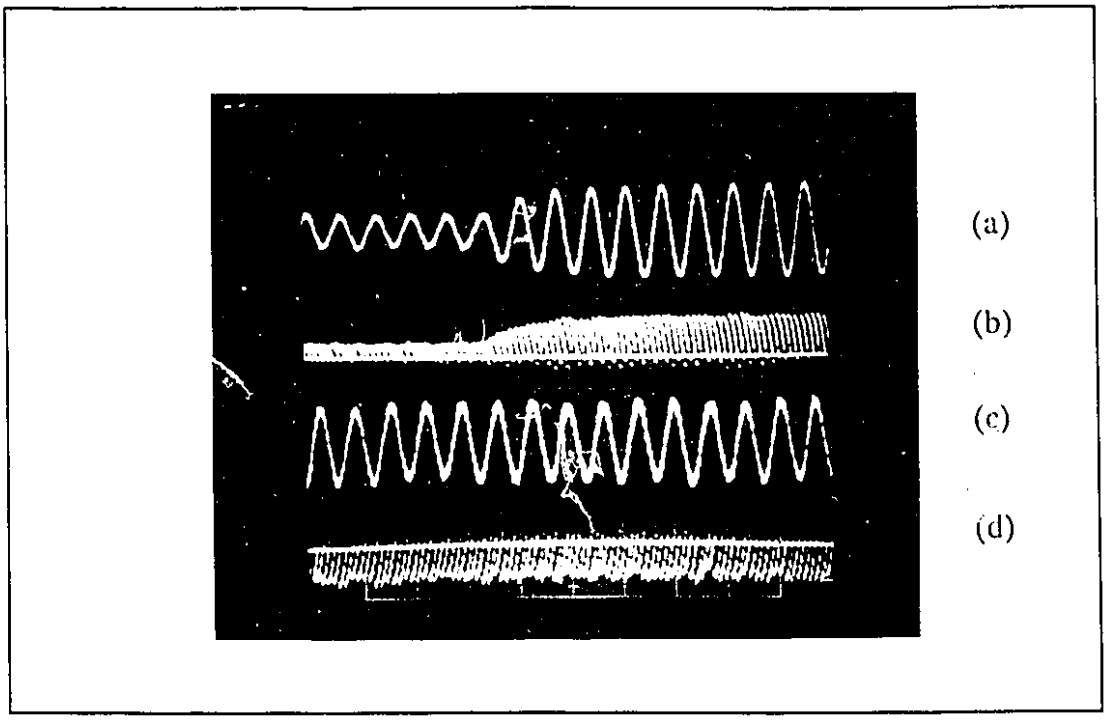


Figure 3-7 Transient waveforms in multi-terminal experiment: (a) ac line current and (b) dc link current in DC Voltage Regulator (VR); (c) ac line current and (d) dc link current in Power Dispatcher (DISP).

The HVDC converter station should be able to survive fault conditions. One kind of fault, the disconnection of one ac phase, has been tested successfully on the DC Voltage Regulator and on the Power Dispatcher. This occurs either through the accidental severance of one line or deliberately by opening the circuit breaker of the line which has a line-to-neutral fault.

Fig. 3-8 shows the line currents of the three ac phases in (a), (b) and (c) and the dc link current in (d) during such a fault which occured in the *B*-phase of

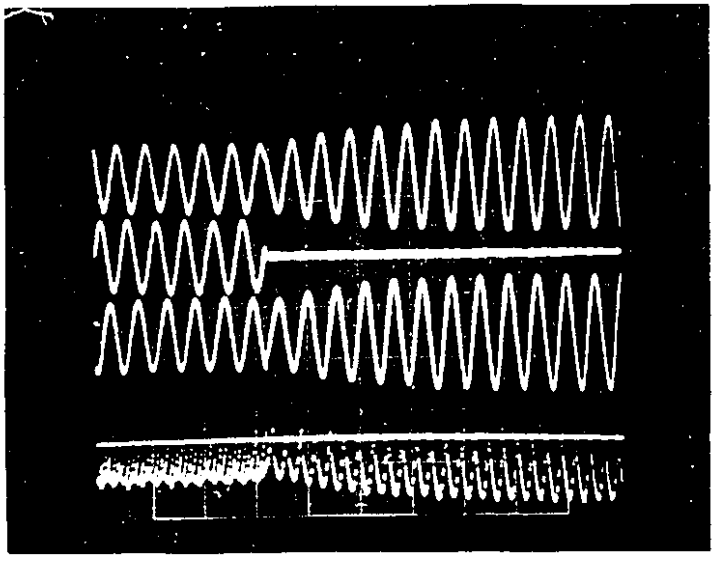


Figure 3-8 Transient in disconnection of *B*-phase of DC Voltage Regulator: (a), (b), (c) A, B, C phase line currents; (d) dc link current.

the DC Voltage Regulator. The currents in the remaining phases increased so as to make up for the same power as before the fault. The currents continued to have near sinusoidal waveforms.

3.5 Summary

Through the experimental tests under steady-state, transient, and faulted conditions, the significant advantages of voltage-source type PWM converter station in the HVDC applications have been demonstrated in this chapter. The next chapter continues the research on the system parameters and concludes that the voltage-source PWM-HVDC system is not economically unreasonable.

CHAPTER
FOUR

PARAMETRIC STUDY

4.1 Introduction

The realizability of the concepts of **Chapter 2** by the experiments described in **Chapter 3** leads the research to the next stage, which consists of sizing of the valves, the inductors, L, on the ac side and the capacitor, C_{dc}, on the dc side of the PWM-HVDC converter station in Fig. 2-1. Since the inductors and the capacitor form an integral part of the converter station, it is critical that they are of reasonable values compared to those presently used in conventional HVDC.

In addition, the parametric studies have been pursued to get an idea as to what carrier frequencies, f_{tr}, and modulation index, M [12], of the Sinusoidal Pulse Width Modulation (SPWM) should be used.

It is assumed in this study that there will be valves capable of switching at *1260 Hz* (21 pulse per *60 Hz* cycle) with acceptable losses for HVDC applications. It should be stressed that the GTO's used in present high power *Static VAR Compensation* (SVC) application switch only at *120 Hz* [4,5]. But given the fact that it takes an average time of 20 years for an innovation to go from the conceptual stage to the market place, it is not unreasonable to proceed with the expectation that when there is application for them, the valve manufacturers will invest in R & D to perfect the GTO's, the MCT's and the SITH's within the 20 year period.

In HVDC transmission systems, the dc voltage ratings are of the order of *±500 KV*. In the existing converter stations, the *5 KV* thyristors are strung in series to build up the voltage withstand [82]. Conceivably, the GTO's and the other gate-turn-off valves will also have to be connected in series to achieve the same high voltage rating. The mastery of the technology of increasing the voltage and the current rating will require extensive research by the manufacturers. In this chapter, the goal is to demonstrate that the "ball-park" figures required of the component sizes are not astronomically large so that the manufacturers will seriously consider the PWM-HVDC system as economically feasible.

4.2 System Model for Parametric Study

The voltage-source type PWM-HVDC converter station used for the

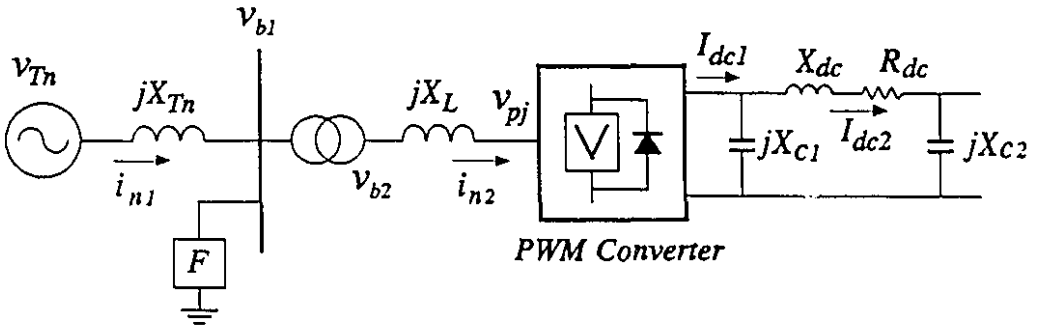


Figure 4-1 Converter station connected to ac utility system and dc system used for feasibility study.

parametric studies is illustrated in Fig. 4-1. In Fig. 4-1, the v_{Tn} and X_{Tn} are the Thevenin equivalent voltage and impedance representing the ac utility system. The reactance X_L includes the leakage reactance of the transformer with additional reactances which may have to be added. On the dc side, the X_{c1} and X_{c2} represent the capacitances directly connected across the converter stations. The dc transmission line is represented by the impedance $R_{dc}+jX_{dc}$.

The box "*F*" connected on the bus in Fig. 4-1 represents the ac filter bank which prevents the harmonic currents from being injected into the ac utility network. The ac filter can consist of the shunt *L-C* elements which are tuned to the switching harmonics so as to "short-circuit" the harmonic currents. It can be the same type of filter which is used in conventional HVDC [2,62,63] except that the harmonic currents are at a higher frequency so that the requisite *L-C* elements are smaller and hence cheaper.

The per unit system is used. The power base is chosen as:

$$\begin{aligned} P_{BASE} &= 3\ v_{b1\,BASE} \times i_{n1\,BASE} \\ &= 3\ v_{b2\,BASE} \times i_{n2\,BASE} \\ &= V_{dc\,BASE} \times I_{dc\,BASE} \end{aligned} \tag{4.1}$$

The ratings are defined under the condition that the PWM-HVDC station is operating with modulation index $M=1.0$ and the reactance $X_L=0.0$. Thus for the schematic of the converter station connected to the ac utility system as shown in Fig. 4-1:

$$\begin{aligned} v_{Tn} &= v_{b1} = 1.0 \quad p.u. \\ v_{b2} &= v_{pj} = 1.0 \quad p.u. \\ V_{dc} &= 1.0 \quad p.u. \end{aligned} \tag{4.2}$$

In Eq. (4.2), v_{b1} and v_{b2} are fundamental Fourier Series component of the voltages on the primary and the secondary side of the transformer, and v_{pj} is fundamental Fourier Series component of converter terminal voltage.

In the study, a weak ac utility system with a *Short Circuit Ratio* [63], $S.C.R.=3.0$ is assumed. The Thevenin equivalent impedance is then:

$$X_{Tn} = \frac{1}{S.C.R.} = 0.333 \quad p.u. \tag{4.3}$$

Fig. 4-2 shows the voltage phasor diagram in the general case when the modulation index M is not unity. It is assumed that *1.0 p.u.* power is transmitted to the converter station so that the voltage phase angle subtended by v_{Tn} and v_{b1}

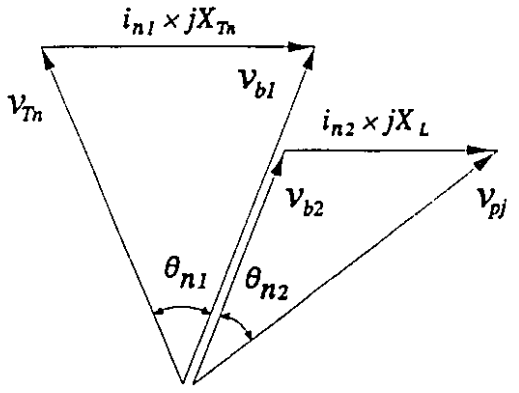


Figure 4-2 Phasor diagram of fundamental Fourier Series component of voltages.

will be:

$$\theta_{n1} = \sin^{-1}\left(\frac{X_{Tn}}{v_{Tn}v_{b1}}\right) = 19.74^{\circ} \tag{4.4}$$

As the v_{b1} and v_{b2} are not equal, it is necessary that the turns ratio of the transformer must be chosen such that:

$$n = \frac{v_{b2\,BASE}}{v_{b1\,BASE}} \tag{4.5}$$

The transformer secondary voltage, v_{b2}, and the fundamental Fourier Series voltage on the ac terminal of the converter station, $\bar{v}_{pj}$, are related as $v_{b2}=\bar{v}_{pj}=1$ *p.u.* under the condition of the modulation index $M=1.0$ and $X_L=0.0$. When $M\neq1.0$, $\bar{v}_{pj}$ can be presented as $\bar{v}_{pj}=M$ in per unit. Table 4-1 lists the per unit values used in the study.

Table 4-1 System parameters chosen for feasibility study.

Per Unit Values of Fig. 4-1		
$X_{Tn}=0.333$ *p.u.*	$X_{c1}=1.0$ *p.u.*	$X_{c2}=1.0$ *p.u.*
$X_{dc}=1.0$ *p.u.*	$R_{dc}=0.05$ *p.u.*	

4.3 Sizing X_L by AC RMS Current

The *rms* (root-mean-square) value of the ac line current is used for rating the bridge valves, the transformers and the reactance X_L. The ac line current can be obtained by using the superposition principle in which each harmonic component of the current is the line harmonic voltage divided by the line impedance at the harmonic frequency. The *rms* current is generally used for rating since it takes into account of the fundamental component and all the harmonics of the current in the computation of the heating of the component.

For meaningful comparisons, the results from the harmonic calculation will based on the same power rating condition. As the fundamental Fourier Series component of voltages and currents are the "useful" part of the power-transfer, their steady state values are adjusted to ensure *1.0 p.u.* power to be transferred to the converter station as the values of X_L and M are varied in the parametric study.

On the secondary side of the transformer, the power transmitted across X_L is:

$$\frac{v_{b2}\ M\ sin(\theta_{n2})}{X_L} = 1.0 \tag{4.6}$$

Referring to the height of the triangle in Fig. 4-2:

$$v_{b2}\ cos\frac{\theta_{n1}}{2} = M\ cos(\ \theta_{n2} + \frac{\theta_{n1}}{2}\ ) \tag{4.7}$$

The two equations (4.6) and (4.7) permit v_{b2} and θ_{n2} to be solved for a specification of M and X_L. The magnitude of the fundamental Fourier Series current of the transformer secondary, $\bar{i}_{n2}$, is:

$$\bar{i}_{n2} = \frac{v_{pj}\ sin(\ \theta_{n2} + \frac{\theta_{n1}}{2}\ ) - v_{b2}\ sin\frac{\theta_{n1}}{2}}{X_L} \tag{4.8}$$

The converter station is controlled by using the Bi-Logic SPWM scheme. The harmonics of the ac terminal voltages are determined by the choice of the M and f_{tr}. Apart from establishing that reasonable inductances and capacitance will enable the voltage-source PWM-HVDC converter station to operate, the study investigates their dependence on the modulation index M and the carrier frequency f_{tr}. It is desirable that f_{tr} is low as it reduces switching losses of the valves. It is also desirable that at the rated ac voltage, M should be less than 1.0. This allows the voltage amplitude to be raised and lowered for reactive power control. For instance, in choosing $M=0.8$ for the rated operation, an over-voltage capability up to $M=1.0$ is permitted.

Having used Eqs. (4.5) to (4.8) to solve for the fundamental Fourier Series component of voltages and currents which will transfer *1.0 p.u.* power through the converter, it is a straight forward exercise to evaluate the Fourier Series harmonic voltage based on the modulation index M and the triangular carrier frequency f_{tr}.

The inductive reactance X_L is used as a common abscissa in the study. The concern here is that X_L should not be excessively large. It should be stressed that X_L includes that transformer leakage reactance which lies in the *0.15-0.20 p.u.* range.

In the results presented graphically in Fig. 4-3, the attention is drawn first to the point of intersection of two axes which corresponds to the fundamental

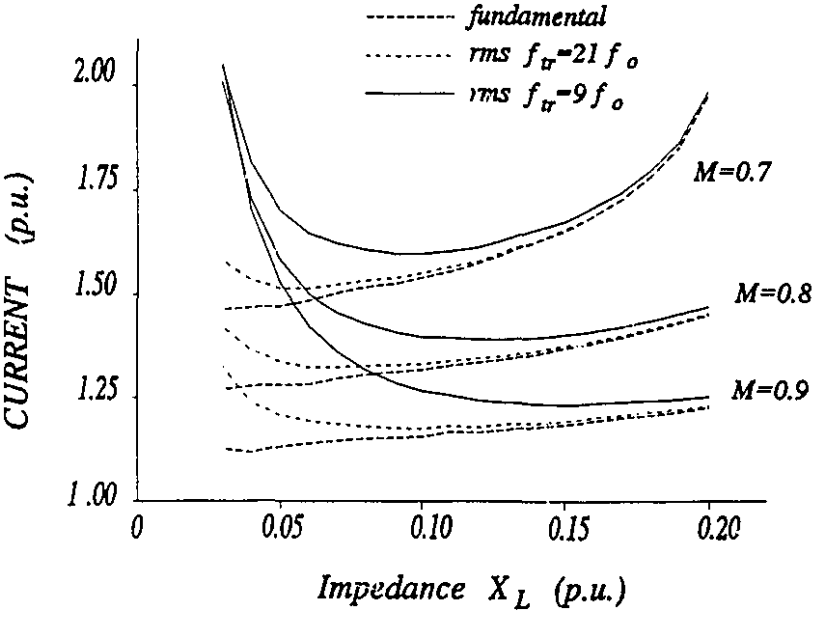


Figure 4-3 Fundamental and *rms* converter ac current as a function of X_L.

Fourier Series component of the converter ac phase current which is required to rectify *1.0 p.u.* power from the Thevenin equivalent voltage source, for $M=1.0$, $X_L=0.0$ and $\bar{i}_{n2}=1.0$ *p.u.* . In order that the same power is transferred for a lower converter voltage associated with the use of a smaller modulation index M, a bigger $\bar{i}_{n2}$ is required. Likewise, for the same M, a larger current is needed to deliver the same power when X_L is increased. The large current is required to compensate for the large voltage drop across X_L so as to be able to deliver the same power.

The *rms* values of the converter ac output current include all the switching harmonic components. As X_L increases, the filtering effect is apparent and the *rms* values converge towards the fundamental component. Fig. 4-3 also shows the difference between using a carrier of frequencies $f_{tr}=9\times f_o$ and $f_{tr}=21\times f_o$. Here f_o is the line frequency, *50* or *60 Hz*.

As a guide to the cost of X_L, Fig. 4-4 graphs the *VA* rating of X_L based on the formula $VA=0.5X_L\times i_{n2rms}^2$ and in Fig. 4-5 the cost reference factor based on the formula $Cost\text{-}Reference\text{-}Factor=X_L\times i_{n2rms}\times v_{max}$.

For PWM application, the Cost Reference Factor is likely to be more pertinent because the insulation of the reactance must be capable of withstanding the maximum voltage v_{max} during PWM switchings.

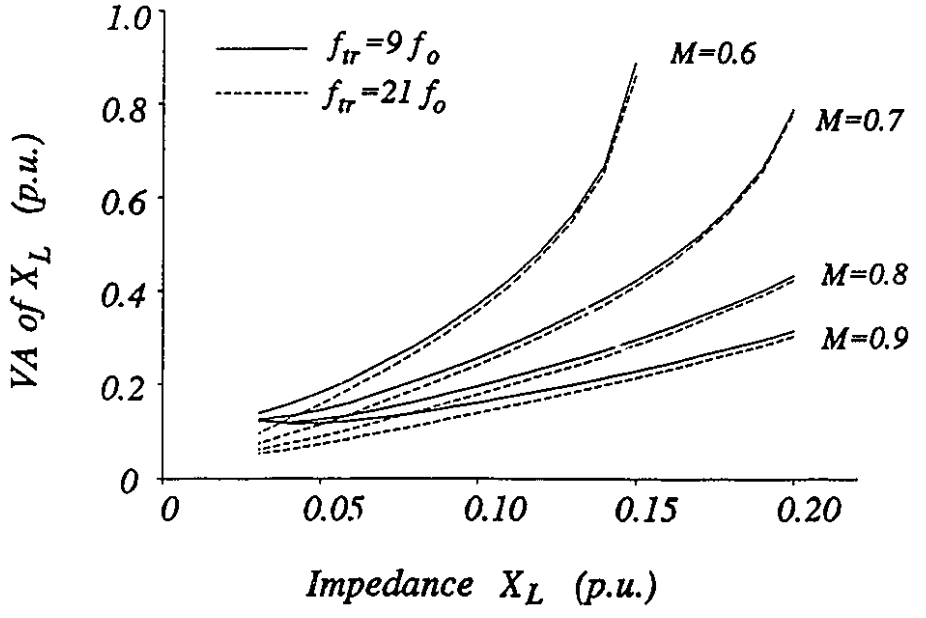


Figure 4-4 *VA* of X_L as a function of X_L.

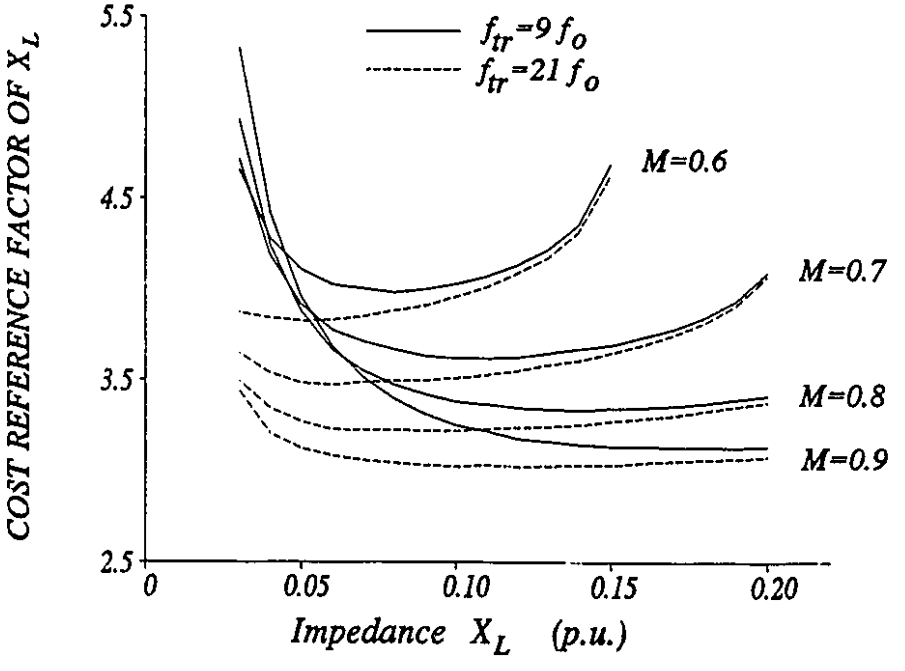


Figure 4-5 Cost Reference Factor ($X_L \times i_{n2rms} \times v_{max}$) vs X_L.

4.4 Total Harmonic Distortion

Based on the ac line currents, i_{n2}, and the SPWM switching functions, S_j, the current injected by the converter into the dc side of Fig. 4-1 can be calculated. A description of one method has appeared in [83,84]. The voltages and currents in the dc side are solved from circuit theory and Fourier Series analysis.

One measure for harmonic appraisal is the *Total Harmonic Distortion* factor. For the converter dc output voltage, the factor THD_{vdc} is defined as:

$$THD_{Vdc} = \left(\sum_{k=1}^{\infty} V_{dck}^2 \right)^{1/2} \times 100\% \tag{4.9}$$

where V_{dck} is the magnitude (per-unit) of the *kth* Fourier Series harmonic voltage across the capacitor X_{cl}. Also, the Total Harmonic Distortion factor for the converter dc output current, THD_{Idc}, is defined as:

$$THD_{Idc} = \left(\sum_{k=1}^{\infty} \left(\frac{V_{dck}}{kX_{dc}}\right)^2 \right)^{1/2} \times 100\% \tag{4.10}$$

It is important to keep the factor THD_{Idc} within certain limit to reduce the harmonic noise interference to the telephone communication system. The typical value is less than or equal to 5% [12,85].

Fig. 4-6 and Fig. 4-7 show the Total Harmonic Distortion factors of the dc voltage and current respectively. In Fig. 4-6, one sees that for $f_{tr}=9\times f_o$, one just misses complying with the required 5% in the practical range of $0.15<X_L$. At the

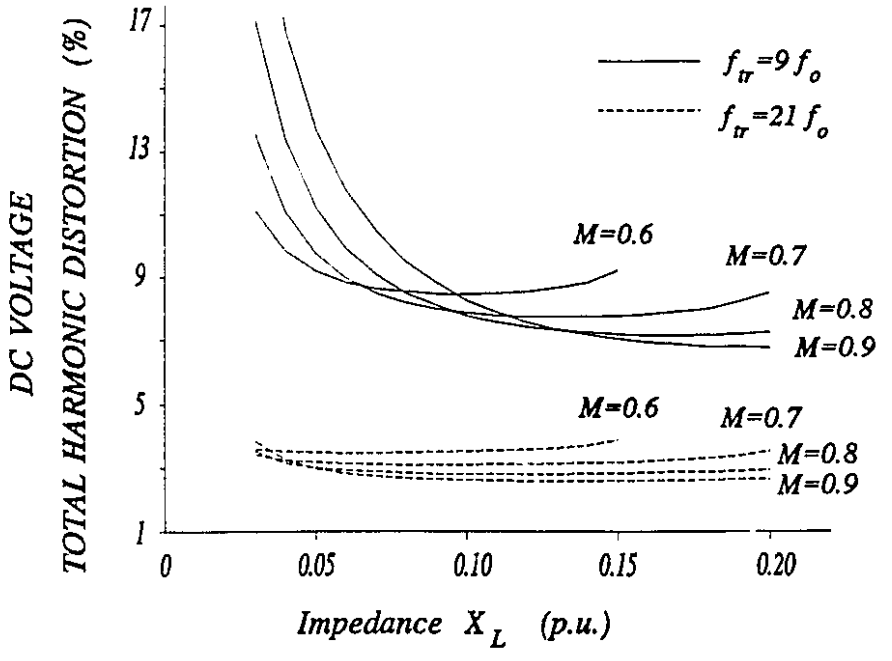


Figure 4-6 Total DC Voltage Harmonic Distortion factor vs X_L.

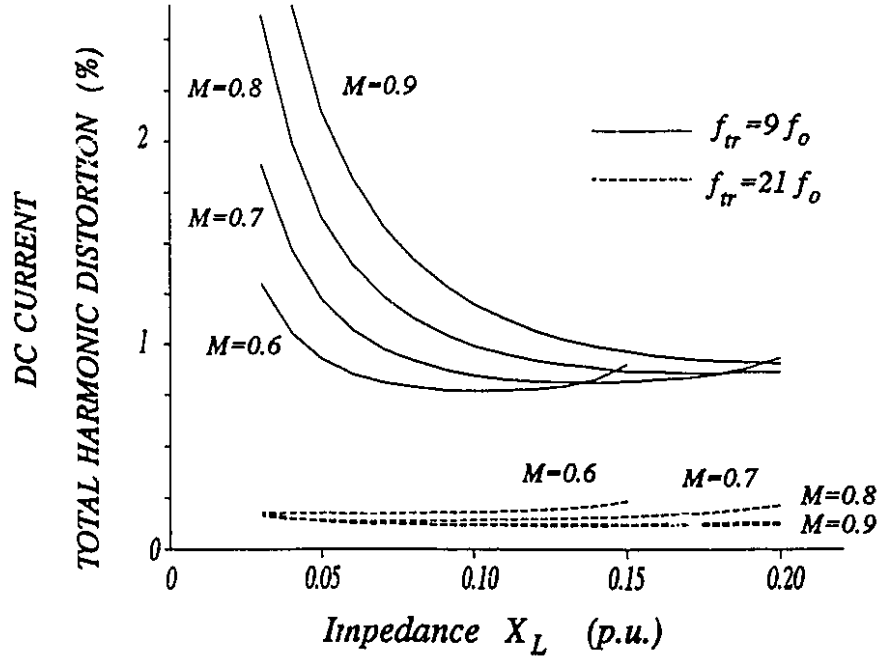


Figure 4-7 Total DC Current Harmonic Distortion factor vs X_L.

higher carrier frequency of $f_{tr}=21\times f_o$, the *5%* is easily satisfied. The Total Harmonic Distortion factor of the dc current is always below the allowed *5%*.

The above studies show conclusively that the fairly large transformer reactance, which is in the *0.15-0.20 p.u.* range, will contribute towards making the voltage-source PWM-HVDC a practical proposition.

With further refinement in the dc capacitor design, it should be possible to use a carrier frequency which is as low as $f_{tr}=9\times f_o$. For economic design M should be as high as possible. If the equipment is overrated to have excess *rms* current carrying capacity, M can be varied to have a range of voltage magnitude control.

4.5 VA Rating and Switching Losses

Any challenges to the conventional HVDC system must first address the problem of operation under the very high voltage and current ratings of the HVDC environment. Present HVDC systems, which are commonly in the thousands of *MVA* and hundreds of *KV* range, operate by connecting thyristors in series. Before PWM techniques can replace the line-commutated HVDC converter station, considerable expense and research will have to be devoted to mastering the technology of series and parallel connections of the force-commutated switching valves. Amongst the problems which have yet to be solved are: (1) reducing the switching losses associated with high frequency operation of

the valves, (2) increasing the voltage limit and the current carrying capacity of the valves or alternatively using series and parallel strings of valves (at reduced ratings) with protection to ensure that they are always stressed equally in steady-state and in transient conditions.

As mentioned in **Chapter 1**, many kinds of high power, force-commutated switching devices have been applied to the industrial power converters. The PWM technique using GTO's has already been operational at the *MVA* levels required in electrical traction, industrial drives, UPS and static VAR compensators, etc. Although there is still a leap from a few megawatts to the hundreds of megawatts range required of HVDC, it is not too early to pursue the conceptual and feasibility studies as have been done in this thesis.

Today, the GTO, the SITH and MCT have characteristics which are suitable for applications requiring high voltage and current ratings. Recently, Japanese researchers [68] have also proposed SITH valves for the PWM type of HVDC converter station which has the single pole capacity of *30 MW* (*150 kVdc/200 Adc*) using the SITH valves rated at *2500V/800A* with the switching frequency up to *20 kHz*.

In McGill University, preliminary feasibility studies have shown that the *MVA* ratings can be achieved by series and parallel connections of the dc terminals of the voltage-source (boost) type PWM converter modules of Fig. 2-1. It has been shown that the voltage and current stresses in steady-state and in

transients are fairly equitably distributed in the converter modules using acceptable tolerances in components [60]. Using the technique of phase shifting of the triangular carrier in SPWM [61], high quality PWM can be attained by reduced switching rates of the individual valves. This promises reduced switching losses and the ability to use slow switches, i.e., GTO thyristor. The reduction of switching losses through active and passive snubber circuits is again an extensive area for research.

4.6 Summary

This chapter has addressed the sizing of the ac inductances and the dc capacitor in the voltage-source PWM converter station for HVDC applications, as its proper functioning depends on the presence of fairly large inductances and capacitance. The study has shown that the sizes used in the present HVDC thyristor converter stations are comparable to those required by the voltage-source PWM-HVDC converter stations. Another finding is that fairly low carrier frequency can be used, so that switching losses can be low. These results add to support the practicality of the voltage-source type PWM-HVDC.

Part I of this thesis has been concerned with advancing the application of the Pulse Width Modulation technique to the Voltage-Source type bridge converter. As a research area, the field is well trodden, especially in amplitude and frequency control of Two-Level or Bi-Logic PWM techniques.

The advances made in **Chapters 2, 3 and 4** have been in the phase and the

frequency control of the PWM technique. Technically, the implementation is through a Voltage Controlled Oscillator, EPROMs to from a Phase Lock Loop described in **Chapter 2.**

The example of the application found for it in this thesis is in the form of a converter station of HVDC Transmission System. Elsewhere, not included in the thesis, the same concepts have been applied for the control of the Series-Type Static VAR Compensator [86]. The common denominator in all these applications is that the PWM converter interfaces with the power utility system which has its frequency to which the converter must be locked in synchronism through the Phase Lock Loop. Once in synchronism, the phase angle is advanced or retarded so that the converter operates as a rectifier or inverter. In the case of the Static VAR Compensator operation the power input is nulled.

The concepts had first been demonstrated by digital simulations and verified through the experimental tests reported in **Chapter 3.** As the test have shown the excellent characteristics predicted for the PWM-HVDC Transmission System are experimentally realizable, the parametric studies of **Chapter 4** have been conducted to demonstrate that the PWM-HVDC converter station is indeed not unrealistic in terms of cost.

The research on the phase angle and frequency control of PWM has opened up a large field of applications in the electric power utility environment.

Starting from the next chapter, the studies on the Tri-Logic SPWM technique and its applications will be described.

CHAPTER
FIVE

DYNAMIC TRI-LOGIC SPWM CONTROL OF 3-PHASE CURRENT-SOURCE CONVERTER

5.1 Introduction

Although many converters in the past had been labelled as PWM controlled Current-Source bridge converters, they had never lived up to the claims. After the definitive work of Hombu, Ueda and Ueda [40,41], one knows now that because the PWM strategy in use had been the Two-Level or Bi-Logic, the valves could not have switched in the manner as wished by their designers. A re-examination of their experimental results reveals very poor waveforms which have little resemblances to the intended sinusoids. Hombu, Ueda and Ueda [40,41] established that the Three-Level or Tri-Logic PWM should be used and indeed the experimental waveforms show remarkable improvements.

Unfortunately the syntheses of the Tri-Logic PWM signals by Hombu, Ueda and Ueda and other researchers [42-46] had been based on "ad-hoc" engineering design. Typically, the design begins with a decision as to the number of pulses to be used per cycle and choosing a waveform harmonic criterion. Then an optimization exercise follows by which the switching angles are determined for one discretized modulation index level. The information of the switching angles for all the modulation index levels are stored in EPROMs. These "ad-hoc" design methods are static methods because the optimization criterion is based on the steady-state sinusoidal waveform.

The research reported in this chapter is targeted towards a systematic synthesis of a Dynamic Tri-Logic PWM strategy. The term "Dynamic" is used to contrast it with the "Static" methods. The objective is ensure that the "local average" of the output signal is linearly proportional to the input modulating signal at the sampled period. The modulating waveform does not have to be a sine-wave.

It is stated in Part I that the Two-Level or Bi-Logic PWM techniques are in an advanced state of development so that the remaining area of research has been in the phase-angle control. In contrast, the Three-Level or Tri-Logic PWM concepts are at the infancy stage. For this reason, this chapter is devoted to a systematic mapping of its characteristics.

Section 5.2 discusses the peculiarities of the 3-phase current-source bridge

converter and why it is more difficult to operate than the voltage-source topology.

Section 5.3 describes the Dynamic Tri-Logic PWM. The truth table, Table 5-1, is essentially a proof that the proposed Dynamic Tri-Logic PWM will operate the valves of the bridge-converter in the manner prescribed by Hombu, Ueda and Ueda [40,41]. The truth table, Table 5-2 is another proof that the proposed Dynamic Tri-Logic PWM can be synthesized from Two-Level or Bi-Logic PWM by a linear transformation.

The rigorous mathematical foundation, with linear transformation as its corner-stone, ensures that the properties of Bi-Logic PWM carry over to the Tri-Logic PWM. In particular, the Sinusoidal PWM (SPWM) is chosen for the Bi-Logic PWM because it has the "Dynamic" properties sought for. Essentially, the "local average" of the Bi-Logic SPWM output is the linearly amplified signal of the modulation input signal. In fact, the amplification gain is constant and without phase-shift, for a frequency bandwidth of 1/3 of the triangle carrier frequency [87]. Since the translation from Bi-Logic to Tri-Logic is also linear, the Tri-Logic PWM outputs are also linear amplified signals of the inputs.

However, there is the problem that the translation formula in Eq. (5.2), "scrambles" the Bi-Logic signals. For this reason, it is necessary to prepare the inputs of the Bi-Logic SPWM signals in anticipation of the "scrambling". The Decoupler Pre-Processors in Section 5.3.5 compensate for the "scrambling" and accomplish the decoupled control of the 3-phase converter output currents by the

input signals.

There is another practical problem of deciding which one of the three legs of the bridge converter should have both the Upper Valve and the Lower Valve simultaneously ON, so as to implement the Zero or Shoot-Through State of the Tri-Logic signal. This problem is discussed in Section 5.3.3 and uses the "single switching action" as the criterion of choosing the Shoot-Through Valves. This is implemented by the PAL (Programmable Array Logic) Gating Circuit described in Appendix B.

5.2 Current-Source PWM Converter and Control Difficulties

The top part of Fig. 5-1 shows the 6-valve, 3-phase, current-source PWM converter bridge. It includes the ac line inductances L, the ac filter capacitors C and a smoothing inductance L_{dc} and its resistance R_{dc} in the dc side.

Comparing with the voltage-source PWM converter topology, Fig. 2-1 in **Chapter 2**, the current-source PWM converter bridge is a more difficult circuit to master. This is due to the fact that on both the ac and dc sides of the converter, the circuit components are originally all inductive elements. During switchings in the PWM mode of operation, it is not possible to meet the current continuity constraint, $i(t_-)=i(t_+)$, in each of the inductive elements, L and L_{dc}. Here t_- and t_+ are respectively the time instants just before and after the switching of a valve. For this reason, in Fig. 5-1 the capacitors, C, have to connected across the ac

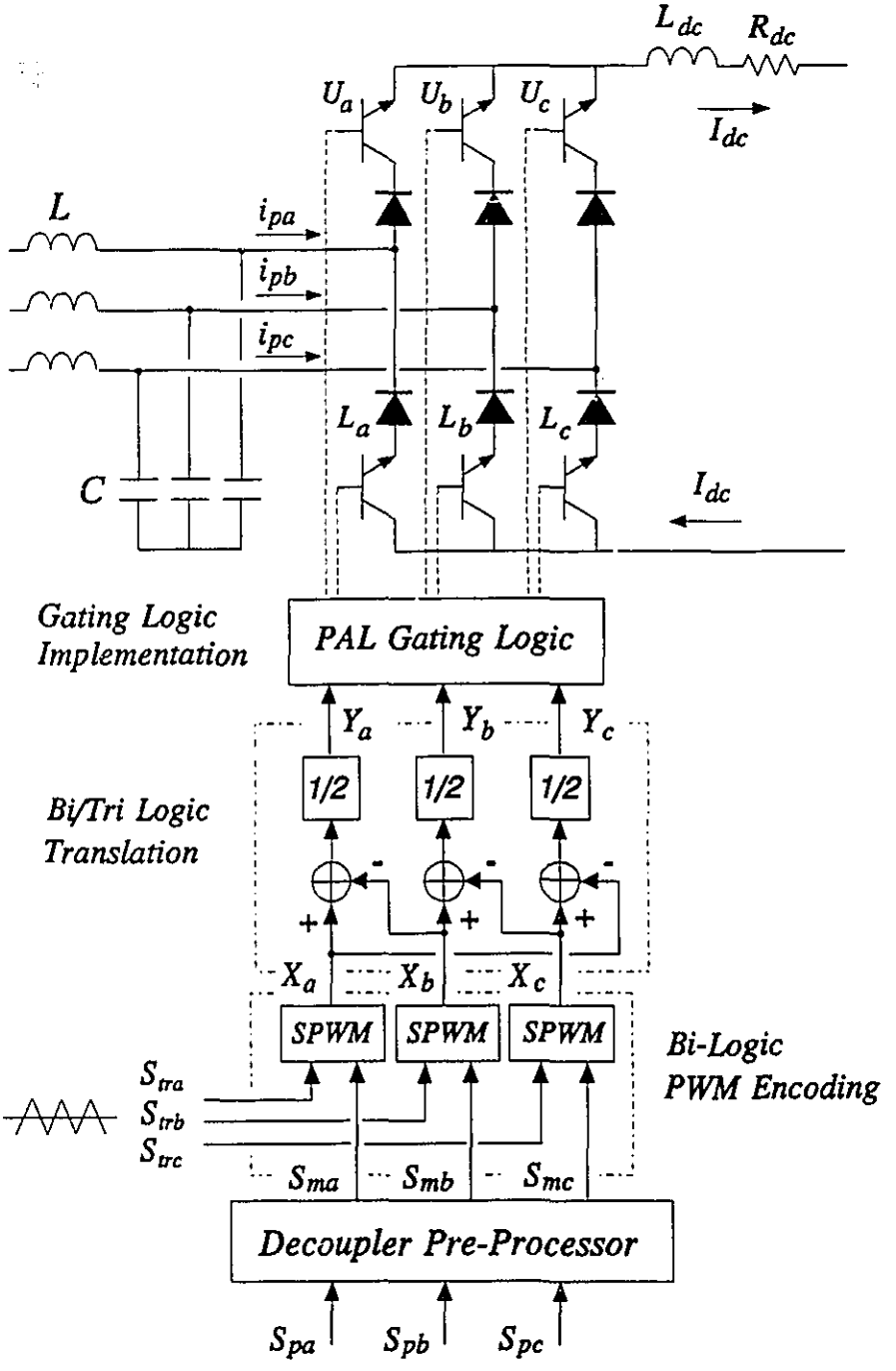


Figure 5-1 Current-source PWM converter with Dynamic Tri-Logic PWM trigger circuit and Decoupler Pre-Processor.

terminals of the converter to act as current buffers and harmonic filters. The presence of the capacitors brings out at least four difficulties which have to be recognized and surmounted.

The **first** difficulty arises from the capacitor voltages which allow only one of the three upper valves (U_a, U_b, U_c) and only one of the three lower valves (L_a, L_b, L_c) of the converter bridge to conduct at any time instant. As shown by Japanese researchers, Hombu et al. [40,41], the usual Two-Level or Bi-Logic PWM strategies, which have been developed for the voltage-source converter over the past 20 years, cannot be used. The converter input currents, $i_{pa}(t)$, $i_{pb}(t)$ and $i_{pc}(t)$, must be the three level ($+I_{dc}$, 0, $-I_{dc}$) type of waveforms. It is necessary to perfect a new Three-Level or Tri-Logic PWM logic.

The **second** difficulty is again due to the capacitor voltage which can apply a reversed anode-to-cathode voltage across on the valve which is receiving a Turn-ON gating signal. As this valve cannot conduct until the reversed voltage is removed by the proper Turning-OFF of the valve which has been ON, there is a brief non-conduction period. The resultant destructive $L_{dc}\, dI_{dc}(t)/dt$ voltage can be avoided only by the provision of a current snubber circuit. The current snubber circuit is not shown in Fig. 5-1 to reduce the complication in the presentation.

The **third** difficulty comes from the resonance between capacitor C and the inductance L in the ac lines. The resonance frequency must be chosen to avoid

forced-resonance from two sources: (i) the 5th, 7th and higher odd harmonics from the ferromagnetic nonlinearity of the ac source, (ii) the switching harmonics of the PWM converter. For high power applications, the switching rates of the valves have to be lowered so as to reduce switching losses. Thus the choice of the *L-C* resonance frequency is pushed towards the low frequency end.

The **fourth** difficulty arises from the fact that the additional energy storage elements in the form of the capacitor *C* increase the system equation dimensionality by one. By comparison with the voltage-source topology, the current-source topology is potentially more unstable. This is because in our design, which is based on using indirect ac current control, the unity power factor condition is obtained by a "*feed-forward*" loop which calculates the compensation required for the voltage drops across the inductive reactance, ωL, and the charging current through the capacitive reactance, $1/\omega C$, so that the converter injects the right amount of ac currents for unity power factor operation. However, this compensation is for the *60 Hz* steady-state operating condition only and results in poor stability [58,69-72]. For full compensation, it is necessary to implement the Ld/dt and Cd/dt operators in the "*feed-forward*" loop. In the indirect current control of the unity power factor voltage-source PWM converter [58], the Ld/dt operator can be implemented using analog components together with a filter which eliminates the high frequency noise introduced by the differentiator, to secure the same stable operating region as hysteresis control of the voltage-source PWM converter [59]. The addition of the capacitors in the

current-source PWM converter poses an impossible task because it requires a d^2/dt^2 operation to fulfil the Cd/dt operator to compute the current for charging the capacitor.

5.3 Dynamic Tri-Logic PWM

To overcome the first difficulty, this section develops the principles of the Dynamic Tri-Logic PWM strategy [78]. Since the capacitor voltages prevent more than one valve in the Upper and Lower valves of the converter to conduct at any one time instant, the current-source PWM converter has to operate with the currents based on the seven combinations of the Tri-Logic variables as shown in Table 5-1 in Section 5.3.1. Many "Static" Tri-Logic PWM methods [42-46] have been proposed for triggering the current-source PWM converter. But they cannot be used for dynamic control since they have been conceived exclusively for obtaining a good sinusoidal waveform in steady-state operation only.

A Dynamic Tri-Logic PWM strategy, whose converter output signal (after filtering) is the linearly amplified form of the modulating signal, is required for the proper operation of the current-source PWM converter if feedback signals are channelled through the converter for stabilization and active filtering. As the current-source PWM converter must be able to fulfil the multiple functions of unity power factor operation with near sinusoidal waveforms while maintaining close dc current regulation with stable and fast response, by necessity the PWM

strategy must be a dynamic one so that the power of linear system theory can be applied in the design of this fairly complex system. The Two-Level or Bi-Logic Sinusoidal PWM strategy, which has been used in the voltage-source PWM HVDC converter station of **Chapters 2, 3** and **4**, has the dynamic attributes. As will be shown, their qualities are passed onto the Tri-Logic PWM.

The implementation of the Dynamic Tri-Logic PWM strategy is shown in the functional blocks in Fig. 5-1. The stages of signal processing are added in order to make the local average values of the converter terminal currents, $i_{pa}(t)$, $i_{pb}(t)$ and $i_{pc}(t)$, to be the linearly amplified forms of the control input signals, $S_{pa}(t)$, $S_{pb}(t)$ and $S_{pc}(t)$.

In Fig. 5-1, the *Decoupler Pre-Processor* stage prepares the input modulating signals in anticipation that 3-phase ac circuit is one of two possibilities: (i) *wye* connection, (ii) *delta* connection (which will be shown later in Figs. 5-6 and 5-7 respectively). The aim is to ensure that each of three input modulating signals controls the ac current in the phase assigned to it.

The output signals of the Decoupler Pre-Processor, $S_{ma}(t)$, $S_{mb}(t)$ and $S_{mc}(t)$, are then encoded into Bi-Logic PWM signals, $X_a(t)$, $X_b(t)$ and $X_c(t)$ by the SPWM strategy, using triangular carrier signals, S_{tra}, S_{trb} and S_{trc}.

The Bi-Logic PWM signals, $X_a(t)$, $X_b(t)$ and $X_c(t)$, are next translated into Tri-Logic PWM signals, $Y_a(t)$, $Y_b(t)$ and $Y_c(t)$, which will be used finally to switch

the valves through the *PAL Gating Logic* circuit.

The details in each signal processing stages will be described in following sub-sections.

5.3.1 Tri-Logic PWM States, $Y_K(t)$

The Tri-Logic variable, $Y_k(t)$ (subscript $k=a, b, c$ for each of the 3 phases), is defined to have three possible values: $+1, 0, -1$. Thus the kth phase output current of the converter, $i_{pk}(t)$, is:

$$i_{pk}(t) = Y_k(t)\ I_{dc}(t)\ , \qquad (k = a, b, c) \tag{5.1}$$

where $I_{dc}(t)$ is the dc line current.

Table 5-1 lists all the possible Tri-Logic states of the 6-valve, 3-phase, current-source PWM converter and their realizations by the conduction states of the Upper valves, U_k, and the Lower valves, L_k. $U_k=1$ and $L_k=1$ denote that U_k and L_k are switched ON. $U_k=0$ and $L_k=0$ denote the OFF states. In the state designations $\#1, \#2, \cdots \#6$, $I_{dc}(t)$ flows through one of the three ac terminal lines and returns through another. In the state $\#0$ (which has three possible states: $\#D$, $\#E$ and $\#F$), all the three ac terminal lines do not carry any current. No current is admitted from the dc side to the ac side. The dc link current, $I_{dc}(t)$, flows through a "*shoot-through*" path constructed by the conduction of the Upper and the Lower valves of the same leg of one of the three phases.

Table 5-1 Current-Source PWM Converter States

State Designation	Tri-Logic			Upper Valve			Lower Valve		
	Y_a	Y_b	Y_c	U_a	U_b	U_c	L_a	L_b	L_c
#1	*0*	*+1*	*-1*	*0*	*1*	*0*	*0*	*0*	*1*
#2	*+1*	*-1*	*0*	*1*	*0*	*0*	*0*	*1*	*0*
#3	*+1*	*0*	*-1*	*1*	*0*	*0*	*0*	*0*	*1*
#4	*-1*	*0*	*+1*	*0*	*0*	*1*	*1*	*0*	*0*
#5	*-1*	*+1*	*0*	*0*	*1*	*0*	*1*	*0*	*0*
#6	*0*	*-1*	*+1*	*0*	*0*	*1*	*0*	*1*	*0*
#0, #D	*0*	*0*	*0*	*1*	*0*	*0*	*1*	*0*	*0*
#0, #E	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*1*	*0*
#0, #F	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*1*

5.3.2 Bi/Tri-Logic PWM Translation

As shown in Fig. 5-1, the Tri-Logic variables $Y_k(t)$ are obtained from the Bi-Logic variables, $X_j(t)$ ($j=a, b, c$ for each of three phases). Each Bi-Logic variable has two possible values: $X_j(t)=+1$ or $X_j(t)=-1$, which are generated from the Sinusoidal Pulse-Width-Modulation (*SPWM*) function blocks which accept as their inputs, the modulating signals, $S_{mj}(t)$, and the triangular carrier signals, S_{trj}.

The Bi-Logic PWM variables, $X_j(t)$, are translated into the Tri-Logic PWM

variables, $Y_k(t)$, through the block of *Bi/Tri-Logic Translation* which is based on the linear mapping:

$$\begin{bmatrix} Y_a(t) \\ Y_b(t) \\ Y_c(t) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} X_a(t) \\ X_b(t) \\ X_c(t) \end{bmatrix} \tag{5.2}$$

or $$\underline{Y_{abc}} = \frac{1}{2} [\, C \,] \, \underline{X_{abc}} \tag{5.3}$$

Table 5-2 lists all the $2^3=8$ combinations of the three Bi-Logic PWM variables, X_j ($j=a, b, c$), and their corresponding Tri-Logic PWM variables, Y_k ($k=a, b, c$), based on Eq. (5.2). The important fact emerging from Table 5-2 is

Table 5-2 Truth Table of Bi/Tri-Logic Translation

State Designation	Bi-Logic			Tri-Logic		
	X_a	X_b	X_c	Y_a	Y_b	Y_c
#0, #D, #E, #F	*+1*	*+1*	*+1*	*0*	*0*	*0*
#1	*+1*	*+1*	*-1*	*0*	*+1*	*-1*
#2	*+1*	*-1*	*+1*	*+1*	*-1*	*0*
#3	*+1*	*-1*	*-1*	*+1*	*0*	*-1*
#4	*-1*	*+1*	*+1*	*-1*	*0*	*+1*
#5	*-1*	*+1*	*-1*	*-1*	*+1*	*0*
#6	*-1*	*-1*	*+1*	*0*	*-1*	*+1*
#0, #E, #D, #F	*-1*	*-1*	*-1*	*0*	*0*	*0*

that the Tri-Logic PWM variables form the complete list in Table 5-1. When the valve switchings are based on Table 5-1, they fulfil the constraints of the current-source PWM converter operation, which is that only one Upper and only one Lower Valve can conduct simultaneously. Thus the translation based on Eq. (5.2) allows the current-source PWM converter to be driven by Bi-Logic PWM signals.

For the past two decades, there have been intensive research on Bi-Logic PWM. The translation algorithm of Eq. (5.2) allows this knowledge from Bi-Logic PWM research to be applied to Tri-Logic PWM.

Fig. 5-2 illustrates how the three Tri-Logic signals, $Y_k(t)$, are generated from the modulating signals, $S_{mj}(t)$ ($j=a, b, c$). In this example, the modulating signals are balanced 3-phase sinusoidal waveforms. Fig. 5-2(a) shows how the Bi-Logic PWM encoding is done by the SPWM strategy. The same triangular carrier is used for all the three phases to produce the Bi-Logic variables shown in Fig. 5-2(b), (c) and (d). The three sequences of Tri-Logic signals $Y_a(t)=[X_a(t)-X_b(t)]/2$, $Y_b(t)=[X_b(t)-X_c(t)]/2$, and $Y_c(t)=[X_c(t)-X_a(t)]/2$ are shown in Fig. 5-2(e), (f) and (g) respectively.

In the complete cycle of the modulating signal, the procession of the Tri-Logic states in the time dimension consists of six sub-periods. The sequence of the Tri-Logic states in Fig. 5-2(e), (f) and (g) is described by the six lines of Table 5-3 as a sequence of the state designation numbers from Table 5-1. Each of the sub-periods is identified by the number of the first state of the six lines.

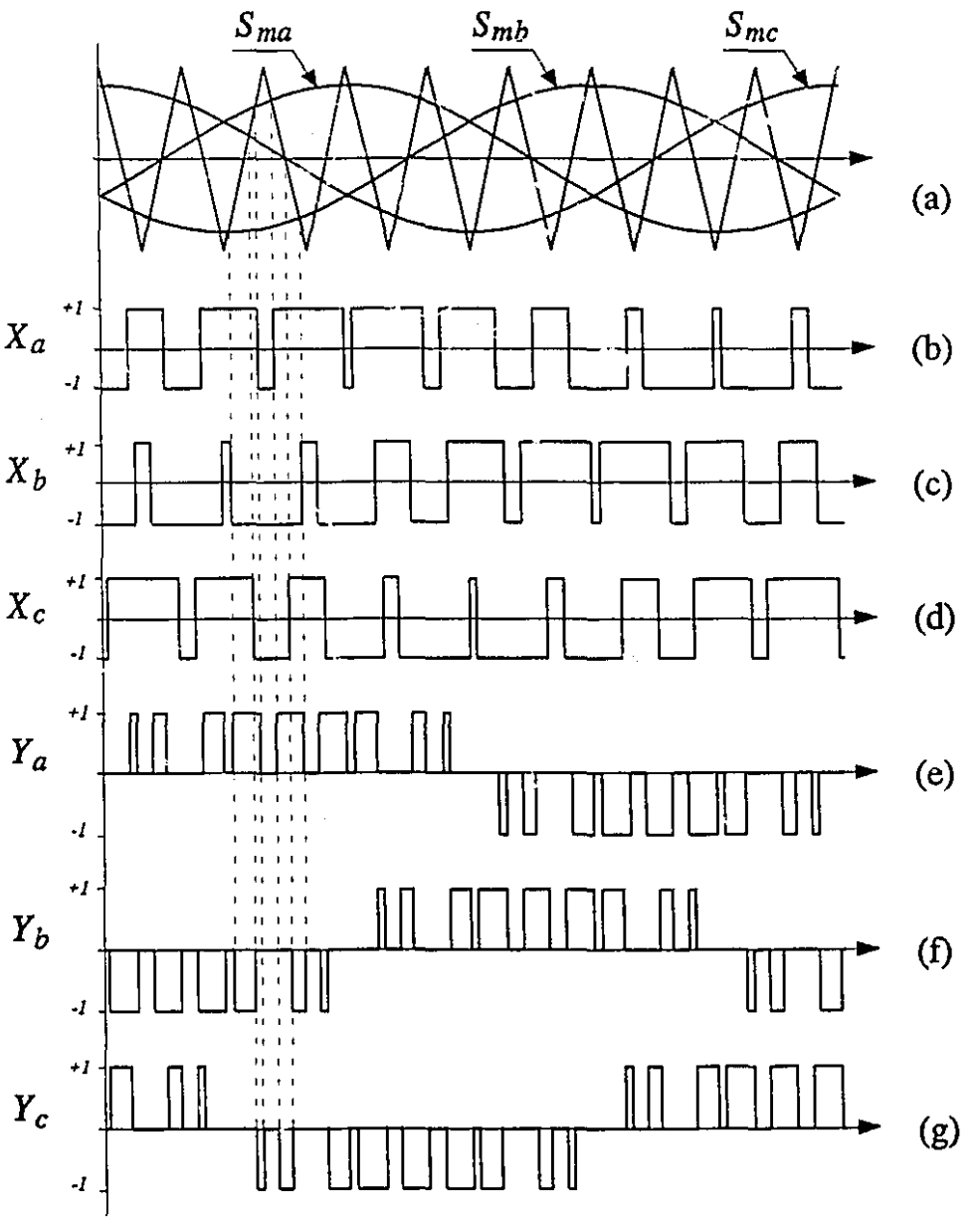


Figure 5-2 Generation of Tri-Logic PWM. (a) SPWM technique; (b),(c),(d) Bi-Logic PWM signals; (e),(f),(g) Tri-Logic PWM signals.

Table 5-3 Sequence of Tri-Logic States

Sub-Period Identification	Contiguity Interpretation (#0)	Sequence in Sub-Period
No.2	*#E*	*- 2 - 0 - 2 - 6 - 0 - 6 - 2 - 0 - 2 -*
No.3	*#D*	*- 3 - 0 - 3 - 2 - 0 - 2 - 3 - 0 - 3 -*
No.1	*#F*	*- 1 - 0 - 1 - 3 - 0 - 3 - 1 - 0 - 1 -*
No.5	*#E*	*- 5 - 0 - 5 - 1 - 0 - 1 - 5 - 0 - 5 -*
No.4	*#D*	*- 4 - 0 - 4 - 5 - 0 - 5 - 4 - 0 - 4 -*
No.6	*#F*	*- 6 - 0 - 6 - 4 - 0 - 4 - 6 - 0 - 6 -*

5.3.3 Single Switching Tri-Logic State Transition

It is apparent that the transition from one Tri-Logic state to the next Tri-Logic state must be executed by one "*single switching action*" which consists of turning OFF of one of the two valves which have been ON and turning ON of a new valve to form the next state.

Two Tri-Logic states are called "*contiguous*" when the transition from one state to the other can be effected by a *single switching action*. For example, the Tri-Logic state (*+1, -1, 0*) or *#2* as shown in Fig. 5-3 has four contiguous states. Two of them consist of keeping switch L_b unchanged and making the changes in the Upper valves as in the cases of *#6* and *#E*. The other two, consist of keeping

U_a fixed as for *#3* and *#D*.

By examining the contiguity of all the states in Table 5-1, it is found that they form a network as shown in Fig. 5-4.

Each sub-period, in Table 5-3, consists of oscillating transitions involving three Tri-Logic states, one of which is *#0* or *(0, 0, 0)*. The choice of which of the three *shoot-through* states (*#D, #E, #F*), is determined by the contiguity requirement embodied in Fig. 5-4.

Fig. 5-3 also shows the Tri-Logic states which come into play in the first

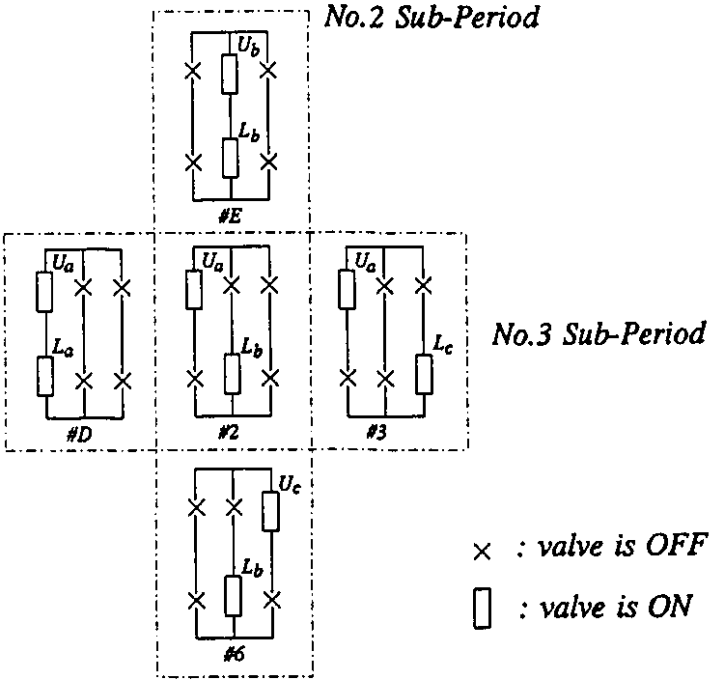


Figure 5-3 Switching state *#2* and four contiguous states in 6-valve current-source PWM converter bridge.

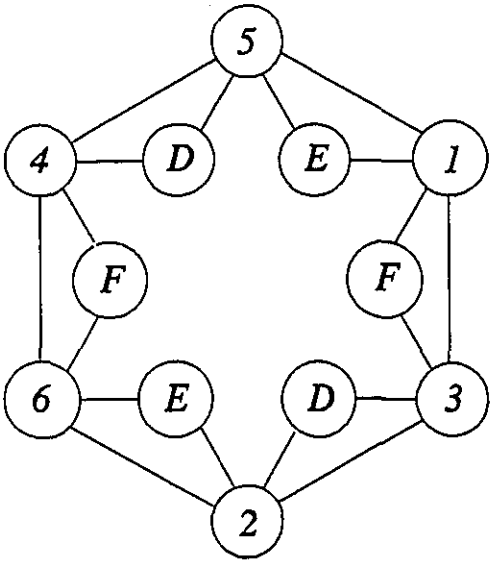


Figure 5-4 Contiguous state of 6-valve current-source converter.

and second lines of Table 5-3 which have been labelled as *No.2* and *No.3* sub-periods. The *#E shoot-through* state is used in connection with the *No.2* sub-period in the interpretation of the *#0* or *(0, 0, 0)* state. This interpretation allows L_a and L_c to be in the OFF states and L_b to be in the ON state all through this sub-period when the signals $Y_k(t)$ call for the stage transitions *-2-0-2-6-0-6-*$\cdots$. Only the Upper valves are switched. In the *No.3* sub-period, the states oscillate around *#2*, *#3* and *#0* (which is interpretated as *#D*). As Fig. 5-3 shows, this is efficiently handled by making U_a ON, U_b and U_c OFF throughout this sub-period.

The transition between sub-periods occurs when the state passes from the last member of one line to the first member of the next line in Table 5-3. From the network of contiguous states of Fig. 5-4, it is seen that the line-to-line

transitions in Table 5-3: *#2* to *#3*, *#3* to *#1*, *#1* to *#5* ··· are all contiguous transitions.

The block of *PAL Gating Logic* circuit in Fig. 5-1, receiving the procession of the Tri-Logic PWM signals, issue the switching instructions to the six valves of converter bridge. Its design has to take into account of the features embodied in Table 5-3 and Fig. 5-4. Essentially, it must be able resolve the ambiguity of the *#0* state, that is whether *#D*, *#E* or *#F* should be used. It must recognize the arrival of Sub-Period Identification state of Table 5-3 and use the Contiguity Interpretation of the *#0* state to implement the *shoot-through* gating signals. The details of the design for the *PAL Gating Logic* circuit will be described in **Appendix B.**

5.3.4 Linear Signal Amplification

Using the Bi/Tri Logic Transformation described above, the 6-valve, 3-phase, current-source PWM converter bridge can be made to function as three sampled linear signal amplifiers for the modulating signals $S_{mj}(t)$ ($j=a, b, c$). The property of the linear amplifier is derived from the stage of encoding the modulating signals to Bi-Logic PWM and from the linear mapping in the translation to Tri-Logic PWM.

In the Bi-Logic SPWM strategy, each triangular carrier signal, S_{trj}, samples the value of the modulating signal $S_{mj}(t)$ at the sampling period of the carrier

signal and embeds the information as the widths of the $+1$ and -1 pulses of $X_j(t)$. In practice, the modulating signal is usually a sinusoidal waveform but in actual fact it can be any arbitrary waveform provided that its frequency bandwidth is below *1/3* the carrier frequency [61,87]. In fact, the SPWM output signal $X_j(t)$ can be shown to be [81]:

$$X_j(t) = \frac{1}{P_{Str}} S_{mj}(t) + N_j(t) \qquad (j=a,b,c) \qquad (5.4)$$

where P_{Str} is the peak value of the triangular carrier S_{trj}, and $N_j(t)$ consists of the switching harmonics of the carrier and the sidebands. It is assumed that the carrier frequency of S_{trj} is sufficiently high so that the frequency spectrum of $N_j(t)$ is in the high frequency end of the spectrum so that it can be filtered by the inductances and the capacitances of the converter. Thus $N_j(t)$ in Eq. (5.4) can be omitted. Thus the $\bar{X}_j(t)$, defined as the local average values of the Bi-Logic SPWM signals $X_j(t)$, is:

$$\bar{X}_j(t) = \frac{1}{P_{Str}} S_{mj}(t) \qquad (j=a,b,c) \qquad (5.5)$$

Substituting Eq. (5.5) into Eq. (5.2) and thereafter Eq. (5.2) into Eq. (5.1), the local average values of the ac terminal input currents of converter, $\bar{i}_{pk}(t)$, will be:

$$\underline{\bar{i}_{Pabc}} = A \, [\, C \,] \, \underline{S_{Mabc}} \qquad (5.6)$$

where $A = \dfrac{I_{dc}(t)}{2\, P_{Str}}$,

$$\underline{\bar{i}_{Pabc}} = \left[\, \bar{i}_{pa}(t),\ \bar{i}_{pb}(t),\ \bar{i}_{pc}(t) \,\right]^T \ ,$$

$$\underline{S_{Mabc}} = [\ S_{ma}(t),\ S_{mb}(t),\ S_{mc}(t)\ ]^T \quad .$$

In the control design, the term A can be made to be constant through an auxiliary feedback loop, which makes the P_{Str} proportional to the $I_{dc}(t)$. This is to keep the gain of the Tri-Logic PWM converter function constant regardless of the variation of dc link current $I_{dc}(t)$. Thus the currents $\bar{i}_{pk}(t)$ ($k=a,\ b,\ c$) are the linearly amplified (constant gain without phase shift) outputs of the modulating signals, $S_{inj}(t)$.

The top parts of Figs. 5-6 and 5-7, in Section 5.3.5, show the equivalent circuits of the current-source PWM converter based on Eq. (5.6). From the [C] matrix in Eq. (5.2) the ideal current sources, $A\times S_{ma}(t)$, $A\times S_{mb}(t)$ and $A\times S_{mc}(t)$, are connected in *delta*.

5.3.4.1 Frequency Spectrum

Since Eq. (5.2) is a linear mapping, the spectrum of Tri-Logic PWM signal is a linear combination of the spectra from the Bi-Logic PWM signals. For example, the spectrum of the Tri-Logic PWM signal $Y_a(t)$ is based on applying Eq. (5.2) to the spectrum (complex numbers) of the signals $X_a(t)$ and $X_b(t)$. Fig. 5-5 (a) and (b) show respectively the spectrum (magnitudes) of the Bi-Logic PWM and Tri-Logic PWM for the case: SPWM modulating index $M=0.8$, triangular carrier frequency$=21\times60=1260$ *Hz*. In Fig. 5-5(b), all the harmonics at integral multiples ($n=1,3,\cdots$) of the carrier frequency (*1260 Hz*) are eliminated. One set

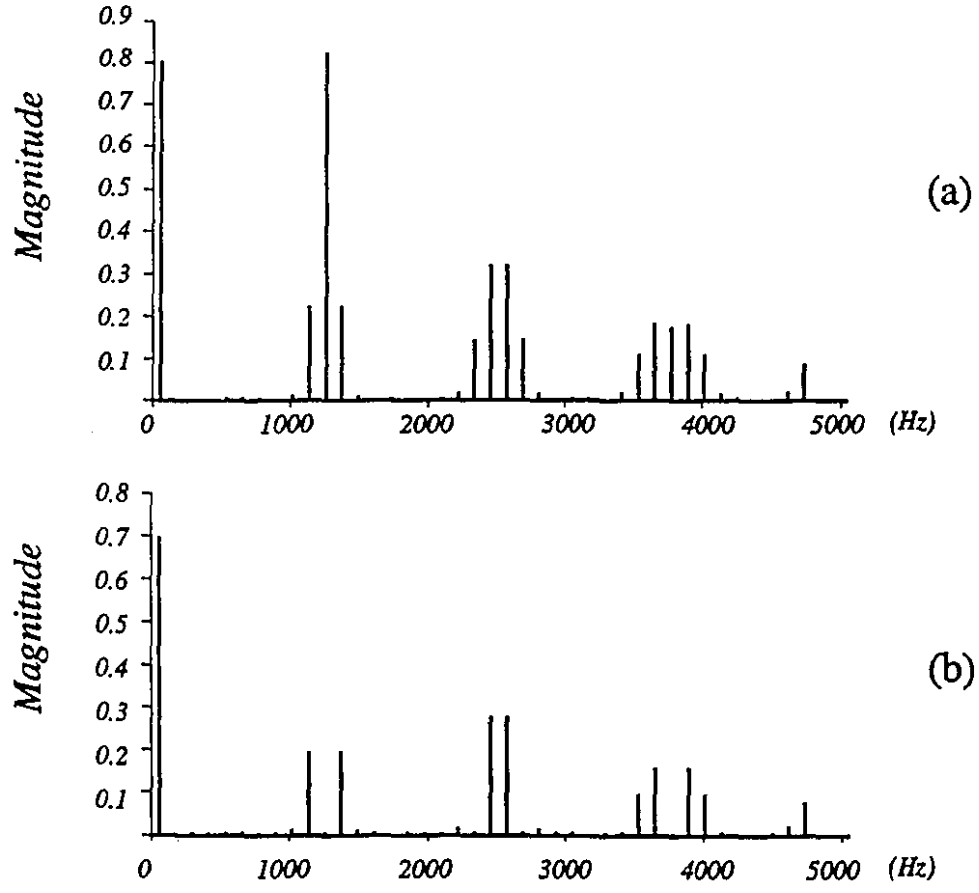


Figure 5-5 (a) Spectrum of Bi-Logic PWM signals X_j,

(b) Spectrum of Tri-Logic PWM signals Y_k.

of the sideband harmonics ($2\times1260\pm2\times60$ *Hz*) is also eliminated.

5.3.5 Decoupler Pre-Processing

Because of the form of the [C] matrix in Eq. (5.2) the ideal current-source amplifiers, $A\times S_{ma}(t)$, $A\times S_{mb}(t)$ and $A\times S_{mc}(t)$ are connected in *delta* as shown in

Figs. 5-6 and 5-7. Thus there is need for a *Decoupler Pre-Processor* block located as shown in Fig. 5-1, so that the input control signals, $S_{pa}(t)$, $S_{pb}(t)$ and $S_{pc}(t)$, can control the local average values of the converter ac terminal currents $\bar{i}_{pa}(t)$, $\bar{i}_{pb}(t)$, and $\bar{i}_{pc}(t)$ directly.

It is proposed that the Decoupler Pre-Processor consists of a transformation by a *3×3* constant matrix [*D*] which relates the input control signals $\underline{S_{Pabc}} = [S_{pa}(t),\ S_{pb}(t),\ S_{pc}(t)]^T$ to the modulating signals $\underline{S_{Mabc}}$ by the equation:

$$\underline{S_{Mabc}} = [\ D\ ]\ \underline{S_{Pabc}} \tag{5.7}$$

Substituting Eq. (5.7) into Eq. (5.6):

$$\underline{\bar{i}_{Pabc}} = A\ [\ C\ ]\ [\ D\ ]\ \underline{S_{Pabc}} \tag{5.8}$$

The desirable result is:

$$\underline{\bar{i}_{Pabc}} = A\ \underline{S_{Pabc}} \tag{5.9}$$

Thus, it is required that $[D] = [C]^{-1}$.

The determinant of matrix [*C*] in Eq. (5.3) is zero, meaning that the rank of the *3×3* matrix [*C*] is less than *3* and there is no inverse. The result of Eq. (5-9) can be achieved if the rank is increased. This is done by first defining:

$$[\ D\ ] = \frac{1}{3}\ [\ C\ ]^T \tag{5.10}$$

Substituting Eq (5.10) into Eq. (5.8), one has:

$$\underline{\bar{i}_{Pabc}} = A\ \underline{S_{Pabc}} - \underline{S_o} \tag{5.11}$$

where $\underline{S_o} = [S_o(t),\ S_o(t),\ S_o(t)]^T$ and $S_o(t) = (S_{pa}(t) + S_{pb}(t) + S_{pc}(t))/3$.

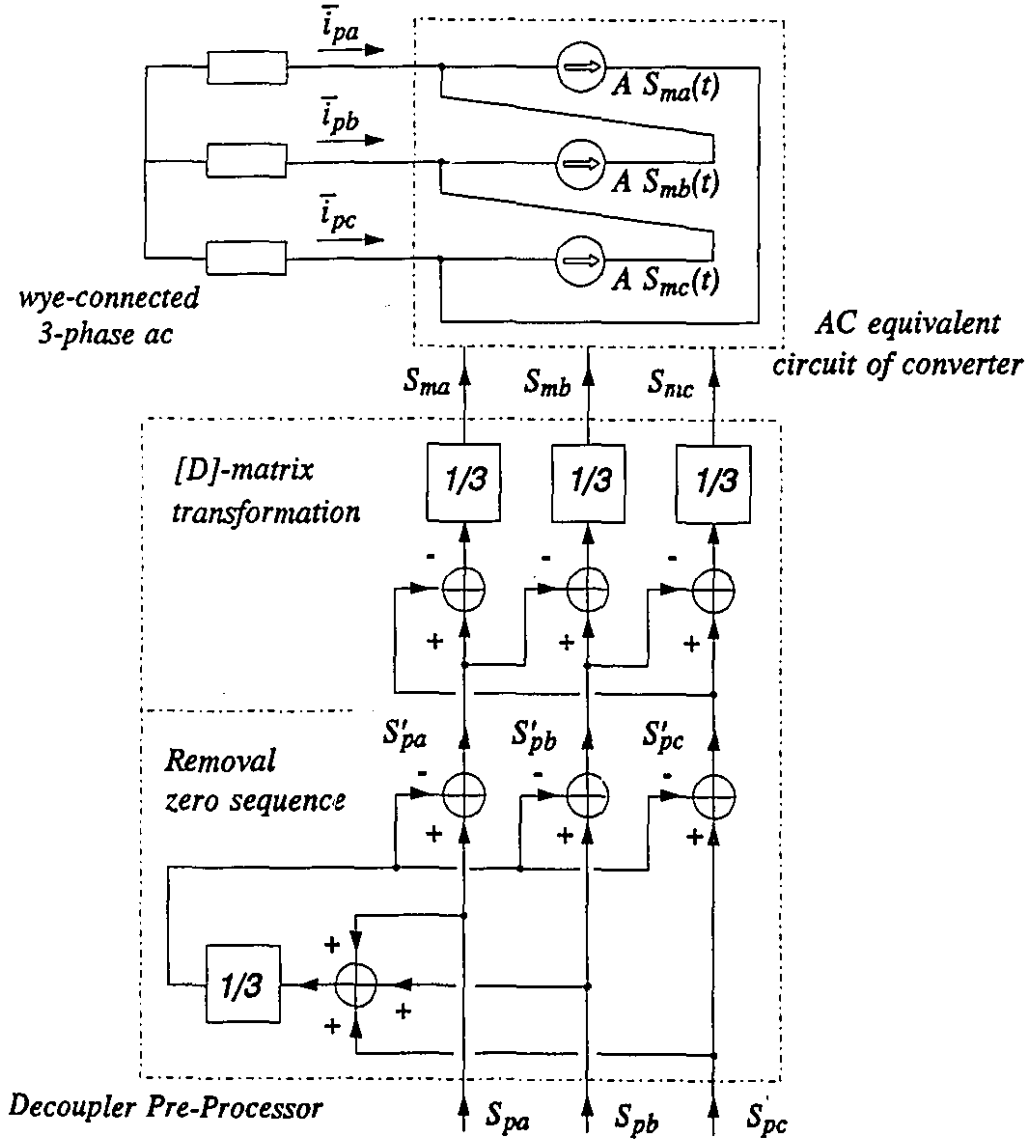


Figure 5-6 Decoupler Pre-Processor for *wye*-connected 3-phase ac.

5.3.5.1 WYE-Connected 3-Phase AC

The result of Eq. (5.9) is possible when $\underline{S_o} = \underline{0}$ in Eq. (5.11). In power engineering, this constraint is equivalent to requiring that the zero sequence does not exist.

Fig. 5-6 is the schematic of the Decoupler Pre-processor for the converter which has an isolated neutral, *wye*-connected 3-phase ac line circuits. The input control signals, $S_{pa}(t)$, $S_{pb}(t)$, $S_{pc}(t)$, pass through a first stage which removes the zero sequence component. The intermediate signals, bearing a prime, satisfy $S_o(t) = (S'_{pa}(t) + S'_{pb}(t) + S'_{pc}(t))/3 = 0$. The next stage consists of realizing Eq. (5.7) where the matrix [*D*] is given by Eq. (5.10). Thus each of three phase currents, $\bar{i}_{pk}(t)$, is completely controlled by the control input signals, $S_{pj}(t)$, independently.

Since there cannot be a zero sequence current flowing in this isolated neutral, *wye*-connected circuit, setting $S_o(t) = 0$ does not introduce any error.

5.3.5.2 DELTA-Connected 3-Phase AC

When the 3-phase ac sources and the *L-C* circuits are *delta*-connected, as shown in Fig. 5-7, the ac terminal currents, $\bar{i}_{pk}(t)$, are related to the three ac phase currents, $i_u(t)$, $i_v(t)$, $i_w(t)$, by the equation:

$$\underline{\bar{i}_{Pabc}} = [\ C\ ]\ \underline{i_{uvw}} \tag{5.12}$$

where $\underline{i_{uvw}} = [i_u(t),\ i_v(t),\ i_w(t)]^T$.

By subtracting Eq. (5.6) from Eq. (5.12), the result is:

$$[\ C\ ]\left(\ \underline{i_{uvw}} - A\ \underline{S_{Mabc}}\ \right) = 0 \tag{5.13}$$

As the *3×3* matrix [*C*] in Eq. (5.13) has a zero determinant, it is necessary that:

$$i_u(t) + i_v(t) + i_w(t) = 0 \tag{5.14}$$

$$S_{ma}(t) + S_{mb}(t) + S_{mc}(t) = 0 \tag{5.15}$$

before $i_u(t)$, $i_v(t)$, $i_w(t)$ can be controlled directly in the decoupled way.

As shown in Fig. 5-7, the Decoupler Pre-Processor removes the zero sequence components from the input signals $S_{pj}(t)$ so that Eq. (5.15) can be

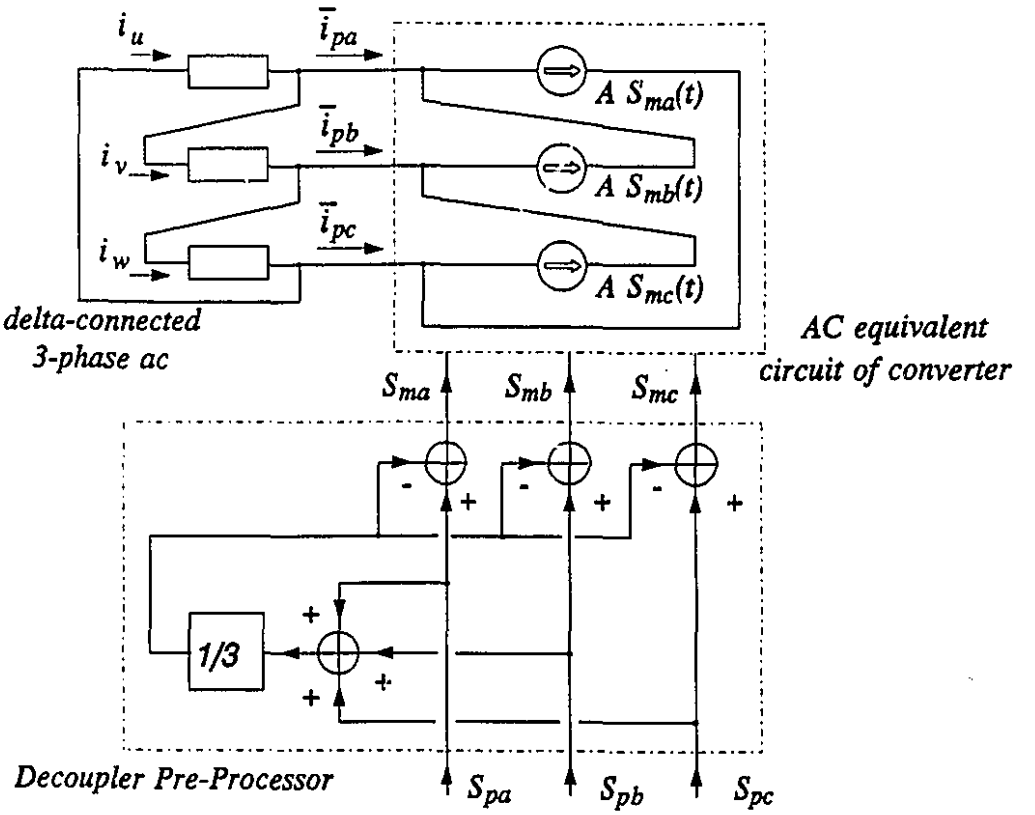


Figure 5-7 Decoupler Pre-Processor for *delta*-connected 3-phase ac.

satisfied. However, if there exists a zero sequence current, $i_o(t)$, which circulates around the *delta* loop of the 3-phase ac circuits, it cannot be controlled.

The extent of decoupled control attainable is:

$$\underline{i_{uvw}} = A\ \underline{S_{Pabc}} + \underline{i_o} \tag{5.16}$$

where $\underline{i_o}=[i_o(t), i_o(t), i_o(t)]^T$

5.4 Summary

This chapter has presented the Dynamic Tri-Logic PWM strategy which is translated from any 3-phase Bi-Logic SPWM signals. The Tri-Logic PWM fits the operational requirements of the 6-valve, 3-phase, current-source PWM converter. In the implementation of the switchings of the valves as controlled by the Dynamic Tri-Logic PWM, the state transition involving a single switching operation only is permitted. The Dynamic Tri-Logic PWM provides the converter with the characteristics of linear amplifiers, with the frequency bandwidth restricted by the frequency of the carrier frequency. The decoupled control over each of the three phases of the current-source PWM converter has been achieved by applying the Pre-Processing Stage to the inputs.

The next chapter will describe a design of the digital control for the current-source PWM converter using the proposed Dynamic Tri-Logic PWM strategy. The digital controller is based on multi-DSP in parallel for the computation of Pole-Placement algorithms.

CHAPTER
SIX

MULTI-DSP REAL-TIME CONTROL

6.1 Introduction

The previous chapter has identified four difficulties inherent in the 6-valve, 3-phase, current-source PWM converter. In order to overcome the main difficulties the converter has to operate under Tri-Logic PWM strategy. The Dynamic Tri-Logic SPWM strategy and the Decoupler Pre-Processor have been presented in **Chapter 5.**

The present chapter develops and describes a new digital control scheme based on the Pole Placement method to solve the remaining control difficulties caused by the ac capacitors. These are: (1) the stable operating region which is too limited, (2) the *L-C* resonance from the ac capacitors. The current-source converter is provided with a current snubber circuit as protection against

$L_{dc}dI_{dc}/dt$ voltage.

In applying the Pole-Placement method, the following innovative approaches have been followed:

(1) The mathematical equations are formulated in such a way that each of the three ac phases is treated independently and separately. This formulation is possible because the Decoupler Pre-Processor enables PWM converter to operate as three independent linear amplifiers.

(2) The entire control task has been implemented digitally. So far, the success of digital controls has been limited to relatively slow processes, such as in robotics and in chemical engineering. The challenge here is to realize a completely digital controller for the PWM converters and to find out what are the key parameters for the successful implementation. A very important conclusion from the research is that the frequency bandwidth needed for the pole-placement feedback is very intolerant of computational delays. To hasten the computation, the pole-placement algorithms were executed by two Texas Instrument TMS320C25 Digital Signal Processors in parallel with a clock frequency of *40 MHz*.

In proving the concepts of **Chapter 5** and the control methods of this chapter, a *1-KVA* size, 6-valve (Bipolar Transistor), 3-phase, Current-Source PWM Converter was constructed. The digital controller used, was a multi-DSP controller which had been designed and constructed in our laboratory.

The following functions were specified for the Current-Source PWM converter:

(1) operate as a stand-alone Rectifier,

(2) DC-side: Close regulation of dc link current. Fast response to dc link current reference setting.

(3) AC-side: Near sinusoidal current at unity power factor. Active filtering capability.

6.2 Mathematical Model

As Eq. (5.9) can be achieved by using the Dynamic Tri-Logic SPWM scheme with the Decoupler Pre-Processor stage, the ac side of the current-source PWM converter of Fig. 5-1 in previous chapter can be simply modelled as three separate, decoupled linear amplifiers of the control input signals, $S_{pj}(t)$ ($j=a, b, c$). Any one of the three phases of the converter can be separately represented by the

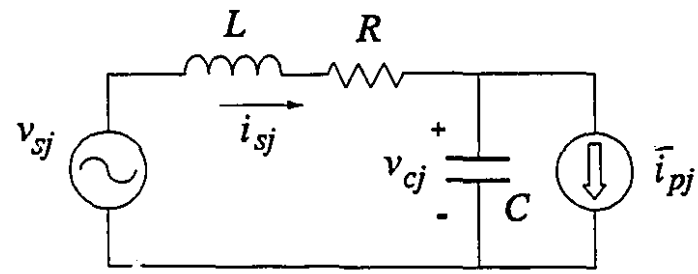


Figure 6-1 Single phase equivalent ac circuit of the current-source PWM converter. ($j=a, b, c$)

single phase equivalent circuit shown by Fig. 6-1.

In Fig. 6-1, $v_{sj}(t)$, $j=a, b, c$ for each of the three phases, is the phase-neutral ac voltage source. Each phase of the PWM converter is modelled as the equivalent current source with the value of $\bar{i}_{pj}(t)$. The switching harmonics in the converter terminal current, will be neglected. By judicious design they are filtered out sufficiently by the inductances and the capacitances of the converter.

Each ac phase circuit can be simply controlled by the equivalent linear amplifier, $\bar{i}_{pj}(t)=A\times S_{pj}(t)$, using a linear combination of the current and the voltage feedback signals of that phase. This approach has the distinct advantage in reducing the order of the system equations and in shortening the computational delays. Compared with other methods [47,48] which require the *Park*'s power invariant transformation [88] from the *a-b-c* frame to the *d-q* frame, to be followed by an inverse transformation back to the *a-b-c* frame again, the computation burden is less. Furthermore the *d-q* frame equations are not decoupled.

In the circuit of Fig. 6-1, by choosing the ac line current, $i_{sj}(t)$, and the capacitor voltage, $v_{cj}(t)$, as the system state variables, the state-space description of the circuit is:

$$\begin{bmatrix} \frac{d}{dt}i_{sj}(t) \\ \frac{d}{dt}v_{cj}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_{sj}(t) \\ v_{cj}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{C} \end{bmatrix} \bar{i}_{pj}(t) + \begin{bmatrix} \frac{v_{sj}(t)}{L} \\ 0 \end{bmatrix} \qquad (6.1)$$

The output is:

$$i_{sj}(t) = [\ 1\ \ 0\ ] \begin{bmatrix} i_{sj}(t) \\ v_{cj}(t) \end{bmatrix} \qquad (j = a, b, c)$$

Removing the input term $v_{sj}(t)$ by subtracting the steady-state operating values from Eq. (6.1), the small perturbation variable model is:

$$\begin{bmatrix} \frac{d}{dt}\Delta i_{sj}(t) \\ \frac{d}{dt}\Delta v_{cj}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \Delta i_{sj}(t) \\ \Delta v_{cj}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{C} \end{bmatrix} \Delta \bar{i}_{pj}(t) \tag{6.2}$$

$$\Delta i_{sj}(t) = [\ 1\ \ 0\ ] \begin{bmatrix} \Delta i_{sj}(t) \\ \Delta v_{cj}(t) \end{bmatrix} \qquad (j = a, b, c)$$

or

$$\frac{d}{dt}\Delta \underline{x}_j(t) = [A]\ \Delta \underline{x}_j(t) + [B]\ \Delta u_j(t)$$

$$\Delta y_j(t) = [C]\ \Delta \underline{x}_j(t)$$

$$(j = a, b, c)$$

where, the small perturbation variables are defined as:

$$\begin{aligned} \Delta i_{sj}(t) &= i_{sj}(t) - i_{sjo}(t) \\ \Delta v_{cj}(t) &= v_{cj}(t) - v_{cjo}(t) \quad , \qquad (j = a, b, c) \\ \Delta \bar{i}_{pj}(t) &= \bar{i}_{pj}(t) - \bar{i}_{pjo}(t) \end{aligned} \tag{6.3}$$

and, $i_{sjo}(t)$, $v_{cjo}(t)$ and $\bar{i}_{pjo}(t)$ are the steady-state operating values of the ac line current, the capacitor voltage and the equivalent current source respectively.

6.3 Control Difficulties

From Eq. (6.2), one sees that the first row element in the vector $[B]$ is zero so that the ac line currents, $\Delta i_{sj}(t)$, cannot be directly controlled by the input variables $\Delta \bar{i}_{pj}(t)$. The adjustment of the ac line current is delayed by one order compared with the control performance in the voltage-source topology [89]. Physically, this is a consequence of the capacitor C connected directly across the ac terminals of the converter. For adjusting the ac line current, the converter needs to inject the right amount of charging current to the ac capacitor so as to make the capacitor voltage correctly compensate for the voltage drops across the R and L of the line. During the transient period, in order to compensate for the $Ldi_{sj}(t)/dt$ voltage drop across the line inductance, the converter current $\bar{i}_{pj}(t)$ has to include the capacitor charging current component which must be contain the second derivative $Cd^2i_{sj}(t)/dt^2$. However, this task is difficult to implement as the d^2/dt^2 operator introduces noise and cannot be used in the control circuit.

Another control difficulty is shown by Fig. 6-2 which plots the open-loop frequency response of $\Delta y(s)/\Delta u(s)$ from Eq. (6.2) for the converter parameters listed in Table 6-1 of Section 6.6 . Since in high power applications the switching rates of the valves have to be lowered so as to reduce switching losses, the choice of L-C resonance frequency is pushed into the low frequency end. In the design example, there is a resonance peak close to 5th harmonic frequency in Fig. 6-2. Because of the 5th, 7th and other odd harmonics from the ferromagnetic

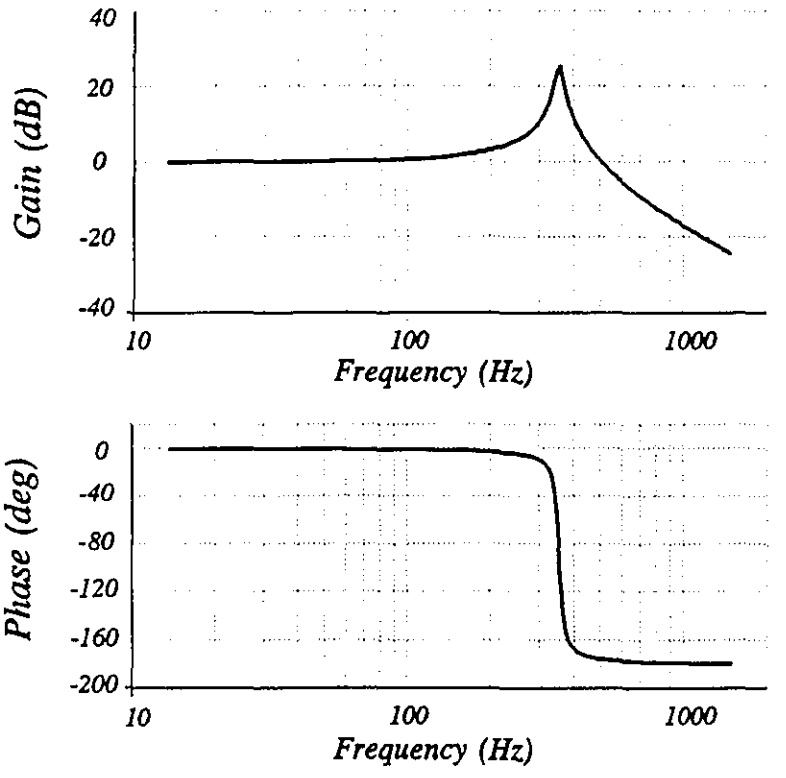


Figure 6-2 Open-loop frequency response of the system showing *L-C* resonance.

nonlinearity of the ac voltage source and the switching harmonics from the converter, the resonance will cause serious low order harmonic distortions on the ac line currents under steady-state operation condition.

During transients, the oscillations of the *L-C* resonance will persist unless there is adequate damping. From Eq. (6.2) the system poles are calculated as:

$$P_{1,2} = -\frac{R}{2L} \pm j\,\frac{\sqrt{4LC - R^2C^2}}{2LC} \tag{6.4}$$

It can be seen that on the *S*-plane, the resonance performance corresponds to one

pair of the low damping poles being located near the imaginary axis. The damping factor $\xi = R\sqrt{C}/2\sqrt{L}$ is low, as the ratio of R/L is small in most rectifier systems.

6.4 Control Strategy

To solve the above control difficulties, the *Pole Placement* control strategy from the modern control theory [90] is proposed to improve the dynamic performance characteristics of the circuit. By calculating the controllability of Eq. (6.2), it is known that the system of Eq. (6.2) is completely controllable for all possible steady-state operating points. Thus the low damping poles of the system can be moved to any desired locations by means of state feedback control. As defined by Eq. (6.3), the state vector $\Delta \underline{x}_i(t)$ in Eq. (6.2) is the "*error*" between the ac line current and the ac capacitor voltage and their desired steady-state waveforms. By using the state-feedback technique, the $\Delta \underline{x}_i(t)$ can be made converge to the origin at a faster rate determined by the Placement of the Poles. When the error $\Delta \underline{x}_i(t) = \underline{0}$, the ac line currents and the capacitor voltages are tracking their desired waveform templates. In maintaining $\Delta \underline{x}_i(t) = \underline{0}$, the harmonic distortions which arise from the interactions with the *L-C* resonance frequency are suppressed, and the converter operates virtually as an *Active Filter*.

Considering the requirement of the complex calculations in realizing the Pole Placement control strategy, the decision is made to built a system controller

based on multi-DSPs (*Digital Signal Processors*) and parallel processing techniques in real-time.

6.4.1 Discretization of System Model

In implementing the digital control design, the continuous time system model of Eq. (6.2) needs to be transformed into the discrete-time system formulation.

Considering the *Zero-Order-Hold Sampling* [91,92] of Eq. (6.2) with the sampling period ΔT, for the sampling instants $t_k = k\Delta T$ ($k=1, 2, 3\cdots$ denote the sampling sequence), the state at the next sampling time t_{k+1} is given by [91,92]:

$$\begin{aligned} \Delta \underline{X}_j(t_{k+1}) &= [G]\ \Delta \underline{X}_j(t_k) + [H]\ \Delta U_j(t_k) \\ \Delta Y_j(t_k) &= [C]\ \Delta \underline{X}_j(t_k) \end{aligned} \tag{6.5}$$

where $\Delta \underline{X}_j(t_k) = [\ \Delta i_{sj}(t_k),\ \Delta v_{cj}(t_k),\ \Delta \bar{i}_{pj}(t_{k-1})\ ]^T$, $\Delta U_j(t_k) = \Delta \bar{i}_{pj}(t_k)$, $(j = a, b, c)$,

$$G = \begin{bmatrix} e^{[A]\Delta T} & H_1 \\ 0 & 0 \end{bmatrix}_{3\times 3}, \qquad H = \begin{bmatrix} H_2 \\ 1 \end{bmatrix}_{3\times 1}, \qquad C = [\ 1\ \ 0\ \ 0\ ]_{1\times 3}$$

It is assumed that there is a delay between the sampling instants (t_k) of the feedback signal and the time needed to compute the control signal. This assumption is embedded in:

$$H_1 = e^{[A](1-m)\Delta T} \int_0^{m\Delta T} e^{[A]s} ds\ [B] \tag{6.5-a}$$

$$H_2 = \int_0^{(1-m)\Delta T} e^{[A]s} ds\,[B] \tag{6.5-b}$$

where $m\Delta T$, $(0 \le m \le 1)$, represents the computational delay. Because of this delay the discretized system model is increased by one order. This is necessary in the control design when the computational delay has a serious effect on the frequency bandwidth of the control system.

6.4.2 Pole Placement Feedback Control

Fig. 6-3 shows the block diagram of the detailed closed-loop control as implemented for phase-*a*. The inner state feedback loop, which is enclosed by the dotted line box of "*feedback*", is used to stabilize the ac *L-C* resonance circuit and to improve its transient response. It ensures that the measured values of the ac line current and the capacitor voltage will track their waveform templates provided by the dotted line box of "*feed-forward*".

At the kth sampling instant $(t=t_k)$, the ac line current, $i_{sa}(t_k)$, and the capacitor voltage, $v_{ca}(t_k)$, are measured, and the state variables $\Delta \underline{X}_a\,(t_k)$ are calculated, using Eq. (6.3). The control input variable $S_{pa}(t_k)$ consists of two components:

$$S_{pa}(t_k) = \bar{i}_{pao}(t_k) + \Delta \tilde{U}_a(t_k) \tag{6.6}$$

$\bar{i}_{pao}(t_k)$ is computed from the feed-forward loop in order to meet the unity power factor requirement of the line current $i_{sa}(t)$. The control will be described

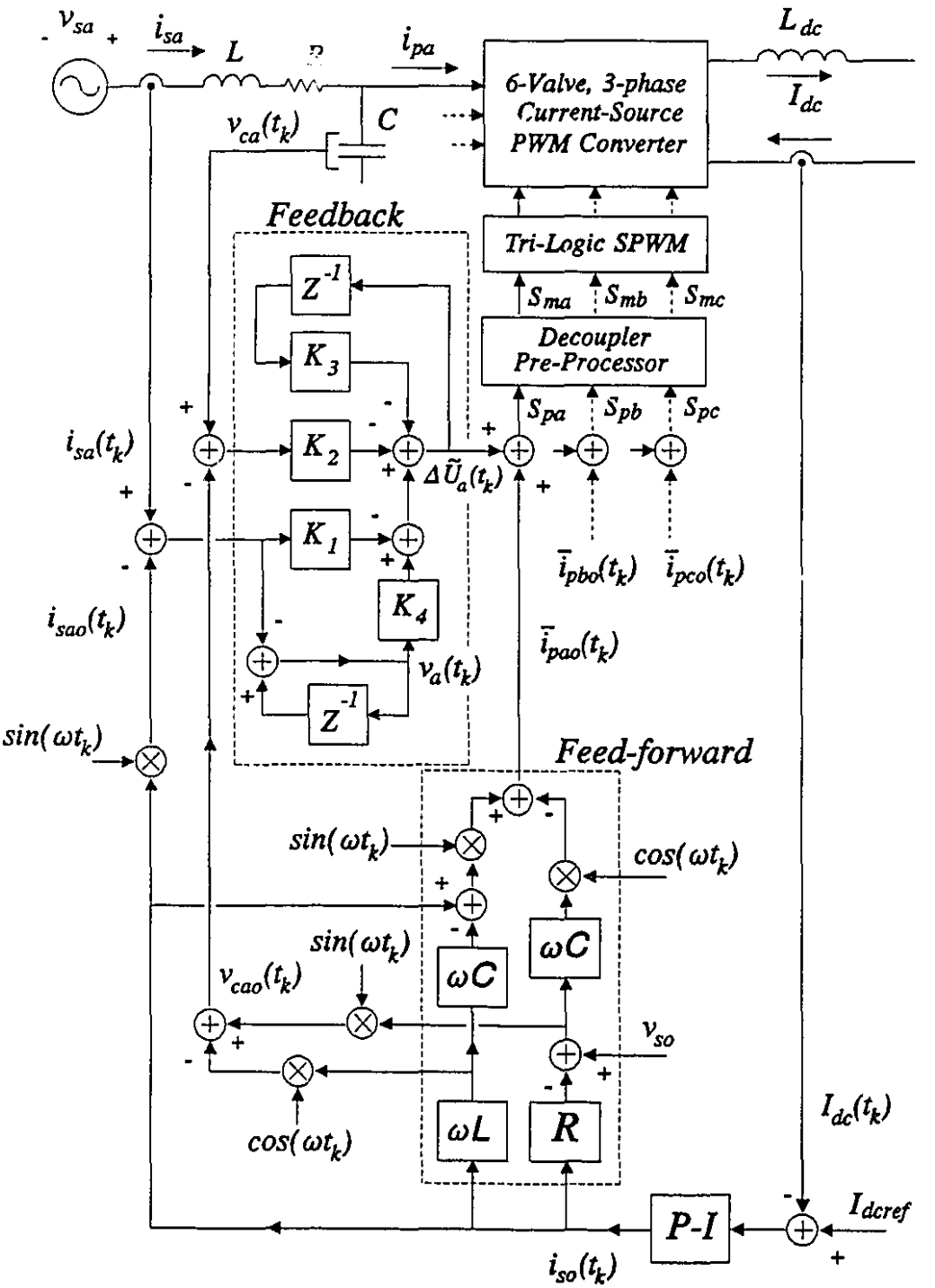


Figure 6-3 Pole Placement control scheme.

in the next section, Section 6.4.3.

$\Delta\tilde{U}_a(t_k)$ represents the state feedback control based on the Pole Placement control law:

$$\Delta\tilde{U}_a(t_k) = -\left[K_1, K_2, K_3\right]\Delta\underline{X}_a(t_k) + K_4 v_a(t_k) \tag{6.7}$$

where, the K_1, K_2 and K_3 are the gains of the state feedback loop which are designed to move the poles of the system of Eq. (6.5) to the desired positions. It can be proved that Eq. (6.5) is keeping the complete controllable characteristic after it has been discretized from Eq. (6.2) with the sampling period $\Delta T = 397\ \mu s$, which will be used later in the experiments described in Section 6.6, so that one can apply a pole placement technique. The additional term:

$$v_a(t_k) = v_a(t_{k-1}) - \Delta i_{sa}(t_k) \tag{6.8}$$

is an integral tracking control loop with the gain K_4, which is chosen to minimize the error between the ac line current, $i_{sa}(t)$, and its waveform template, $i_{sao}(t)$. This control is necessary when the system model parameters are not accurately known.

In the control implementation, the gain in the equivalent linear amplifier $\bar{i}_{pa}(t) = A \times S_{pa}(t)$, described in Section 5.3.4, is chosen as $A = 1$, so that the feedback control signal $\Delta\tilde{U}_a(t_k) \equiv \Delta U_a(t_k)$. Denoting t_k by k and $[K_1\ K_2\ K_3]$ by $K_{1\sim3}$, and substituting Eqs. (6.8) and (6.5) into Eq. (6.7), $\Delta U_a(k+1)$ (or $\Delta U_a(t_{k+1})$) can be solved as:

$$\begin{aligned}\Delta U_a(k+1) &= K_4\left[v_a(k) - [C]\left([G]\Delta\underline{X}_a(k) + [H]\Delta U_a(k)\right)\right] \\ &\quad - K_{1\text{-}3}\left([G]\Delta\underline{X}_a(k) + [H]\Delta U_a(k)\right) \\ &= \Delta U_a(k) + K_{1\text{-}3}\Delta\underline{X}_a(k) \\ &\quad - \left(K_4[C] + K_{1\text{-}3}\right)\left([G]\Delta\underline{X}_a(k) + [H]\Delta U_a(k)\right)\end{aligned} \tag{6.9}$$

Together with Eq. (6.5), the closed-loop system equations for each of the three phases are:

$$\begin{bmatrix}\Delta\underline{X}_j(k+1) \\ \Delta U_j(k+1)\end{bmatrix} = \begin{bmatrix} G & H \\ 0 & 0\end{bmatrix}\begin{bmatrix}\Delta\underline{X}_j(k) \\ \Delta U_j(k)\end{bmatrix} + \begin{bmatrix} 0 \\ 1\end{bmatrix} W_j \tag{6.10}$$

$$j = a, b, c$$

where, the state feedback input W_j is:

$$W_j = -K_s\begin{bmatrix}\Delta\underline{X}_j(k) \\ \Delta U_j(k)\end{bmatrix} = \begin{bmatrix} S_1 & S_2\end{bmatrix}\begin{bmatrix}\Delta\underline{X}_j(k) \\ \Delta U_j(k)\end{bmatrix} \tag{6.11}$$

$$j = a, b, c$$

and $\quad S_1 = K_{1\text{-}3}([I] - [G]) - K_4[C][G]$

$$S_2 = 1 - K_{1\text{-}3}[H] - K_4[C][H]$$

It can be shown that if Eq. (6.5) is completely controllable, Eq. (6.10) is also completely controllable. The gain vector $K_s = -[S_1\ S_2]$ can be solved by applying *Ackermann*'s formula [91,92]:

$$K_s = [\,0\ 0\ 0\ 1\,][C_t]^{-1}P([\bar{G}]) \tag{6.12}$$

where,

$$[\bar{G}] = \begin{bmatrix} G & H \\ 0 & 0 \end{bmatrix}$$

is the system matrix of Eq. (6.10), and $P(\bullet)$ is closed-loop system characteristic polynomial with desired pole locations, and $[C_t]$ is the controllability matrix of Eq. (6.10). Thus the state feedback gains K_4 and $K_{1\sim3}$ can be found from Eq. (6.11):

$$K_s = [\, K_{1\sim3} \;\; K_4 \,] \begin{bmatrix} [G]-[I] & [H] \\ [C][G] & [C][H] \end{bmatrix} - [\, 0\; 0\; 0\; 1 \,] \tag{6.13}$$

Therefore,

$$[\, K_1 \; K_2 \; K_3 \; K_4 \,] = \left(K_s + [\, 0\; 0\; 0\; 1 \,] \right) \begin{bmatrix} [G]-[I] & [H] \\ [C][G] & [C][H] \end{bmatrix}^{-1} \tag{6.14}$$

As the system model is completely controllable, in theory it is possible to assign the desired closed-loop system poles to any position on the Z-plane. The "*deadbeat*" control scheme [91,92], which is accomplished by placing all the poles at the zero of the Z-plane, is the desired way to achieve fast transient response. However, in practice this may not be realizable because of the "saturation" limits on the magnitudes of the control inputs. In particular in the SPWM function of Fig. 5-1 in previous chapter, the modulating signals, $S_{ma}(t)$, $S_{mb}(t)$ and $S_{mc}(t)$, must be less than the peak value of the triangular carrier signal $S_{tr}(t)$. From the laboratory experience, the assignment of the poles too close to the zero of the Z-plane has, in fact, led to instability.

Since the damping factors of poles of Eq. (6.5) are mainly determined by

the time constant L/R, in the control design, the desired closed-loop system poles have been chosen by substituting as large as possible the value of the resistance R into Eq. (6.5), and using corresponding eigenvalues as the ideal closed-loop system pole positions.

6.4.3 Unity Power Factor Feed-Forward Control

To achieve unity power factor control, the steady-state converter terminal current, $\bar{i}_{pao}(t_k)$, has been determined from the steady-state solutions of Eq. (6.1) when the ac source voltage v_{so} and the system parameters L and C are known. This is done in the dotted line box labelled "*feed-forward*" in Fig. 6-3.

Assuming the a-phase ac supply voltage is:

$$v_{sa}(t) = v_{so}\sin(\omega t - \theta_a) \tag{6.15}$$

for unity power factor operation the desired ac line current waveform template is:

$$i_{sao}(t_k) = i_{so}(t_k)\sin(\omega t_k - \theta_a) \tag{6.16}$$

where, θ_a is a phase angle and v_{so} is the peak value of ac voltage source. The quantity, $i_{so}(t_k)$, is the instantaneous peak value of the ac 3-phase line current templates. Substituting Eqs. (6.15) and (6.16) into Eq. (6.1), for constant value of $i_{so}(t_k)$, the steady-state solution of the capacitor voltage template, $v_{cao}(t_k)$, is given by:

$$\begin{aligned} v_{cao}(t_k) = &\left(v_{so} - R\,i_{so}(t_k)\right)\sin(\omega t_k - \theta_a) \\ &- \omega L\,i_{so}(t_k)\cos(\omega t_k - \theta_a) \end{aligned} \tag{6.17}$$

Therefore, the steady-state converter terminal current, $\bar{i}_{pao}(t_k)$, can be obtained through the equation:

$$\begin{aligned} \bar{i}_{pao}(t_k) &= i_{sao}(t_k) - C\frac{d}{dt}v_{cao}(t_k) \\ &= (1-\omega^2 LC)\, i_{so}(t_k)\sin(\omega t_k - \theta_a) \\ &\quad - \omega C\left(v_{so} - R\, i_{so}(t_k)\right)\cos(\omega t_k - \theta_a) \end{aligned} \tag{6.18}$$

As shown in Fig. 6-3, the current amplitude $i_{so}(t_k)$ comes from the current regulation *P-I* (Proportional and Integral) control block in the outer feedback control loop. The function of the outer dc current regulation loop is to null the error between the dc link current $I_{dc}(t)$ and its reference setting I_{dcref}. When this error appears, it is used to adjust the magnitude of the line current command $i_{so}(t_k)$. Through Eq. (6.18), $i_{so}(t_k)$ adjusts $\bar{i}_{pao}(t_k)$ in magnitude and in phase angle so as to make the converter increase or decrease the transmitted power while preserving unity power factor operation.

In the "feed-forward" control loop of Fig. 6-3, the in-phase and the in-quadrature references, $\sin(\omega t_k)$ and $\cos(\omega t_k)$, are from the sinusoidal waveform generators which are synchronized with the ac voltage sources.

Only the *a*-phase control implementation is shown. The *b* and *c*-phases are identical except that their in-phase and the in-quadrature references are shifted by $-120°$ and $-240°$ respectively.

6.4.4 Frequency Bandwidth

The above Pole Placement control design is realizable because the Dynamic Tri-Logic PWM scheme and the Decoupler Pre-Processor, introduced in pervious chapter, enable each modulating signal to control its ac phase as a linear amplifier. However, the frequency bandwidth of this equivalent linear amplifier needs to be considered to ensure that the feedback can be implemented successfully.

From the theory of Sinusoidal PWM, it is known that for the modulating index $M \leq 1$, the frequency bandwidth of linear amplification in the SPWM strategy is up to $1/3$ of the triangular carrier frequency [61,87]. Therefore, for active filtering of the low order harmonics in the ac circuits (up to the 7th harmonic in our design), the lowest triangular carrier frequency used to encode the bi-logic PWM signals in Fig. 5-1 of **Chapter 5** should satisfy with the formula $f_{tr} \geq (3 \times 7) f_o$ *Hz* (f_o is the line frequency).

In the adopted control design philosophy, the circuit *L-C* resonance frequency is chosen to be low enough with respect to the PWM triangular carrier frequency so that it falls within the frequency bandwidth of the equivalent linear amplifier. Although the *L-C* resonance frequency interacts with the low order harmonic sources, the state-feedback control loops can react fast enough so as to ensure $\Delta \underline{X}_j(t) = \underline{0}$. As such the *L-C* resonance is suppressed.

Another factor affecting the frequency bandwidth of the feedback control loop is related to the choice of the sampling frequency and the computational delays, $m\Delta t$ of Eqs. (6.5-a) and (6.5-b) [91,92] in the digital controller. In the digital control, the SPWM strategy is implemented by the "*four timer*" [93] method in which the control sampling instants are taken at each of the extremum points on the SPWM triangular carrier waveform. Thus the sampling frequency is fixed at twice the triangular carrier frequency. In high power applications where the switching losses of the valves can be considerable, it is necessary to maintain high efficiency by reducing the switching frequency. In such situations, one suffers a loss of control frequency bandwidth. For this reason it is critical that there should not be any further encroachment on the frequency bandwidth because of the computational delays. For example, from the experiments it was found that using the sampling time period as the delay (this corresponds to $m=1$ in Eqs. (6.5-a) and (6.5-b)) had led to system instability. Therefore, the control command was executed as soon as the numerical computations were completed. The computational delay was: $m=0.2$ in Eqs. (6.5-a) and (6.5-b). The following methods have been used to minimize the computational delays:

(1) The control feedback algorithm is chosen to minimize the computational time. By using the system model in the *a-b-c* frame, one avoids the calculations of the transformations from the *a-b-c* frame to the *d-q* frame and the inverse transformations back to the *a-b-c* frame. Because of the *wye* connection on ac side of converter, the feedback controls on only two

of the ac phases are calculated.

(2) The digital controller is implemented by using fast, parallel Digital Signal Processors. (see Section 6.5)

(3) Programmable Array Logic (PAL) is used to implement the Tri-Logic Gating. (see Appendix B).

6.5 Multi-DSP Control

High performance, fast Digital Signal Processors (DSPs) and parallel processing techniques provide the system controller with very powerful computational capabilities. In meeting the requirement to reduce computational delays so as to obtain a broad frequency bandwidth in the digital feedback control loop, a real-time multi-DSP controller is employed to implement the control schematic of Fig. 6-3. Fig. 6-4 shows the hardware design of the multi-DSP controller.

The *Multi-DSP Controller* of Fig. 6-4 has been designed and implemented in the Power Electronics Laboratory of McGill University, and has been used as a digital controller for PWM converters for a variety of applications [94-96]. As shown in Fig. 6-4, the Multi-DSP Controller consists of three high-speed DSPs (*Texas Instrument TMS320C25*s) operating independently in parallel. Each of DSPs has its own local program and data memories, and operates at *40 MHz* clock frequency. The operations of the three DSPs are synchronized by using the

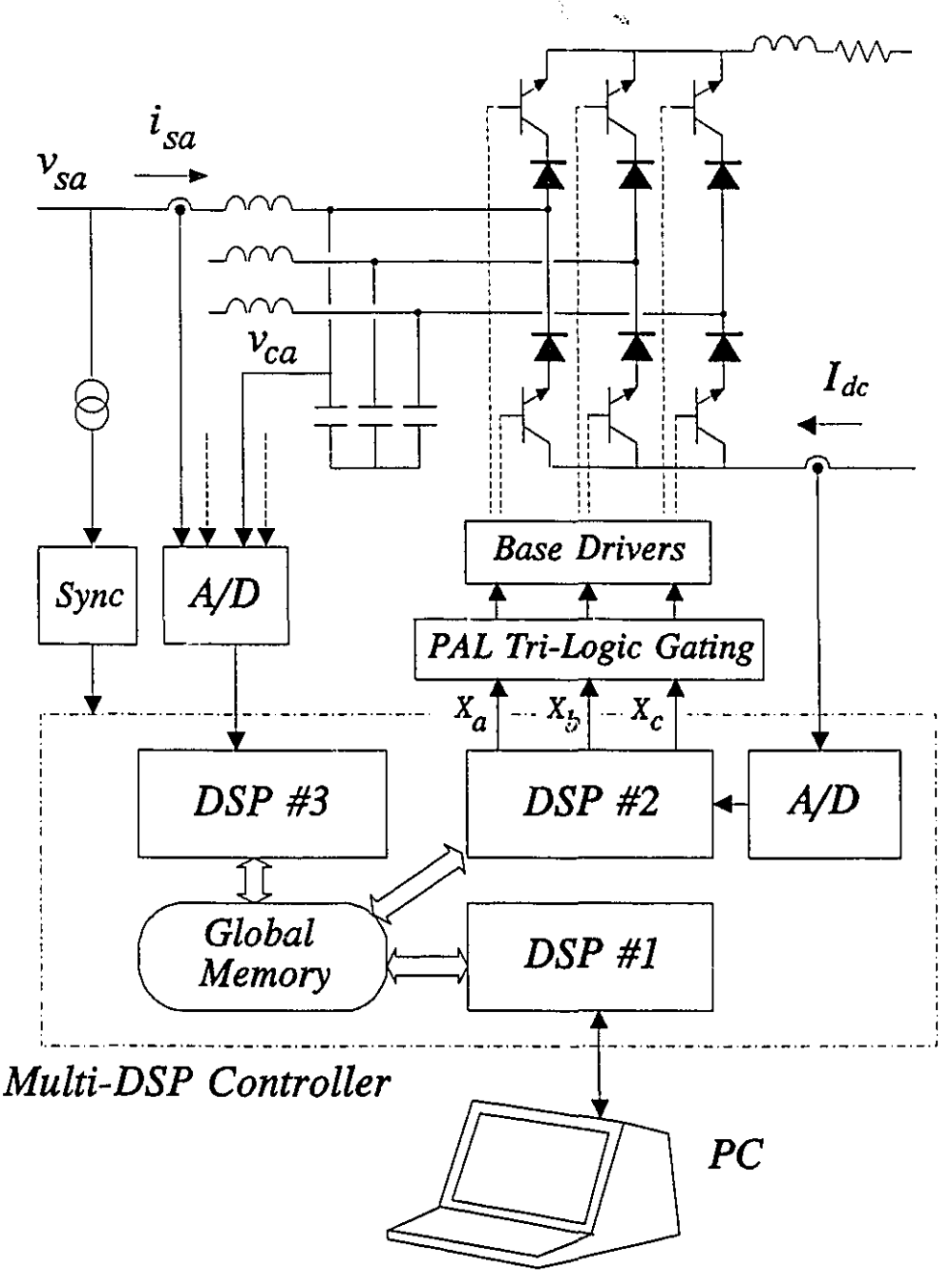


Figure 6-4 Hardware configuration of current-source PWM converter with multi-DSP controller.

interrupt signals and a hardware synchronization circuit (which is not shown in Fig. 6-4). During real-time operation, the parameters for the calculations and data are exchanged between the DSPs through a 3-port global memory.

The outputs of the Multi-DSP Controller have to be converted into base drive signals to activate the valves of the converter which operate under the Tri-Logic SPWM strategy described in Chapter 5. This is accomplished by the *PAL* (Programmable Array Logic) *Tri-Logic Gating* hardware circuit which is connected between the current-source PWM converter and the Multi-DSP Controller. It transforms the Bi-Logic SPWM signals, $X_a(t)$, $X_b(t)$ and $X_c(t)$, which are generated from the Multi-DSP Controller, into the Tri-Logic PWM signals based on Eq. (5.2). It has also the duty to store temporarily in the memory the Tri-Logic state sequence and then from its historical context to choose the *shoot-through* state (#D, #E or #F of Table 5-3) automatically. This depends on the programmed logic, which has been designed to fulfil the requirement of state contiguity embodied in Fig. 5-4 of Section 5.3.3. Its output trigger signals are sent to the converter valves through the *Base Drivers* circuit. The design details of the *PAL Tri-Logic Gating* circuit are described in **Appendix B.**

To access the feedback state signals of the new Pole Placement control strategy of Fig. 6-3, two current transducers and two voltage transducers measure the instantaneous ac line currents and capacitor voltages of two of *wye* connected ac phases. There is an additional current transducer to measure the dc current

for the outer current regulator loop.

The "Sync" block in Fig. 6-4 is a zero-crossing detection circuit for measuring the ac source voltage phase angle. Using it as a phase reference, a software implemented *Phase Lock Loop* (PLL) produces the in-phase and the in-quadrature sinusoidal reference waveforms, $sin(\omega t_k)$ and $cos(\omega t_k)$, in the "feed-forward" control block of Fig. 6-3. The sinusoidal reference waveforms are synchronized with the ac voltage source.

A *Personal Computer* (PC) is connected to the Multi-DSP Controller through a serial communication channel, by which the control program codes can be down-loaded to each of the DSPs and the control parameters can be modified and displayed during the real-time control.

In order to shorten the computational delay time $m\Delta T$ in Eq. (6.5), all the computation tasks to implement the feedback control shown in Fig. 6-3 have been evenly shared between DSP #2 and DSP #3, and executed in parallel. The DSP #1 has been mainly used to exchange the control parameters and the converter status signals with the PC during operation.

The control program of each DSP is divided into several computational stages in the duration of a sampling period. When all three DSP have completed the calculation of one stage, they exchange intermediate results through the global memory, and then continue the calculations of the next stage. The three DSPs

operate synchronously under the controls of the synchronization circuit which ensure that the stage-by-stage parallel calculations are kept in step.

The control programs have been written in the assembler language. 16-bit fixed-point arithmetic operations have been used. The details on the sharing of the control tasks and the programs by each DSP are described in **Appendix C.**

6.6 Experimental Results

A *1-kVA* size laboratory model of the bipolar transistor current-source PWM converter bridge using the multi-DSP controller, as shown in Fig. 6-4, has been constructed. Tests have been conducted for the verifications of the proposed Dynamic Tri-Logic PWM trigger method, the Decoupler Pre-Processor and the Pole Placement control schemes under the rectifier mode of operation.

The parameters of the current-source PWM rectifier used in the experiments are shown in Table 6-1. On the dc side, a resistance load is

Table 6-1 Current-Source PWM Converter Parameters.

Converter Bridge Parameters		
$v_s = 70\ V_{rms}$	$\omega L = 2.5\ ohm$	$L_{dc} = 200\ mH$
$C = 30\ \mu F$	$R = 0.8\ ohm$	$R_{dc} = 0.5\ ohm$

connected. On the ac side, the circuit *L-C* resonance frequency is chosen to be *357 Hz* which is close to the 5th harmonic.

In the experiment, the software of the "four timer" method [93] is used to implement the Bi-Logic SPWM function of Fig. 5-1. The number of carrier triangular is set as *21* per modulating signal period. In the multi-DSP controller, the sampling frequency is chosen to be twice of the triangular carrier frequency, $60\times21\times2=2520$ *Hz* (sampling period $\Delta T=397$ μs). In each sampling period, the control programs of the three DSPs are executed in parallel through *seven*

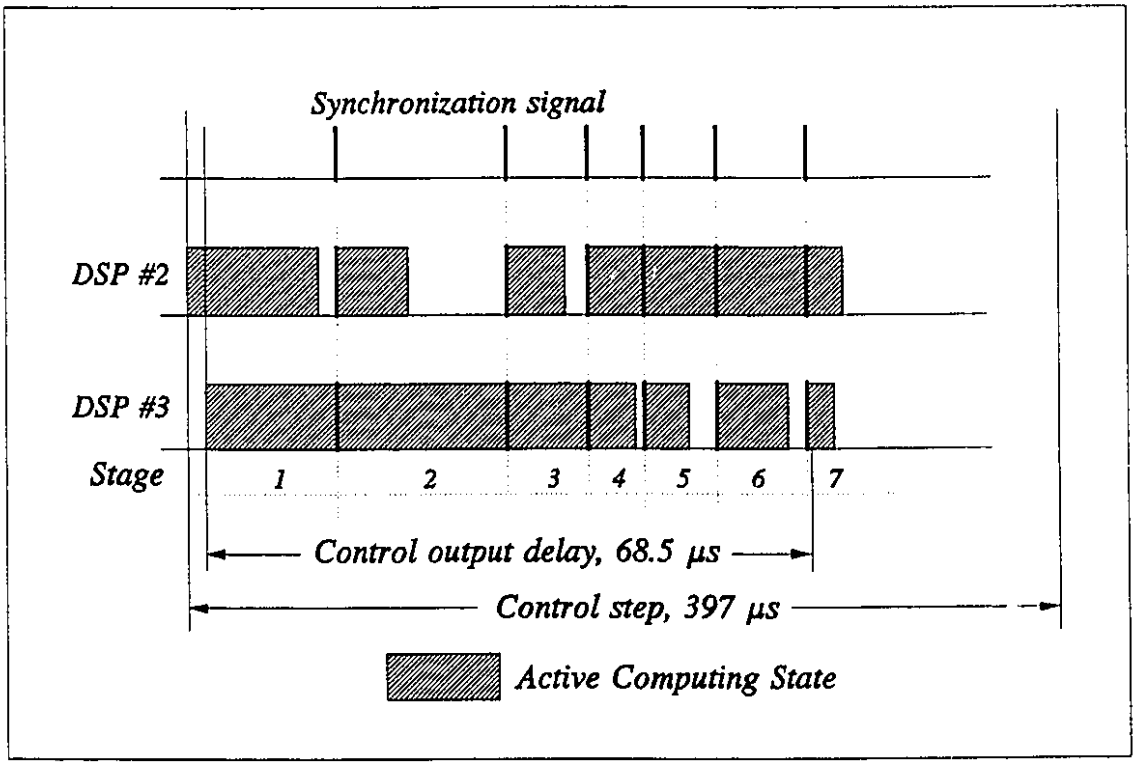


Figure 6-5 Active parallel computing times of the DSPs in each sampling period. (See Table 6-2 for details.)

Table 6-2 Length of active computing time for the DSPs.

Stages	*1*	*2*	*3*	*4*	*5*	*6*	*7*
DSP #2	*10.3 μs*	*7.0 μs*	*5.0 μs*	*6.6 μs*	*8.1 μs*	*10.0 μs*	*4.0 μs*
DSP #3	*14.6 μs*	*19.2 μs*	*9.0 μs*	*4.4 μs*	*3.5 μs*	*6.5 μs*	*3.0 μs*

calculation stages. The active computing times executed in experiments are shown in Fig. 6-5 and Table 6-2. The first row of pulse waveform in Fig. 6-5 is the synchronization signal which controls the beginning of each parallel calculation stages. It is seen that the control computational delay time $m\Delta T \leq 0.2 \times \Delta T$ is achieved.

6.6.1 Active Filtering Test

Fig.6-6 shows the steady-state operating waveforms of: (a) the ac line current, (b) the capacitor voltage and (c) the terminal PWM pulse current in the current-source PWM converter without the Pole Placement state feedback control. This corresponds to the case of the control variable $\Delta\tilde{U}_a(t_k)=0$ in Eq. (6.6). Typically the ac voltage source in the Power Electronics laboratory of McGill University contains the 3rd and the 5th harmonic. They cause the severe 5th harmonic distortions in the ac line current and the capacitor voltage waveforms

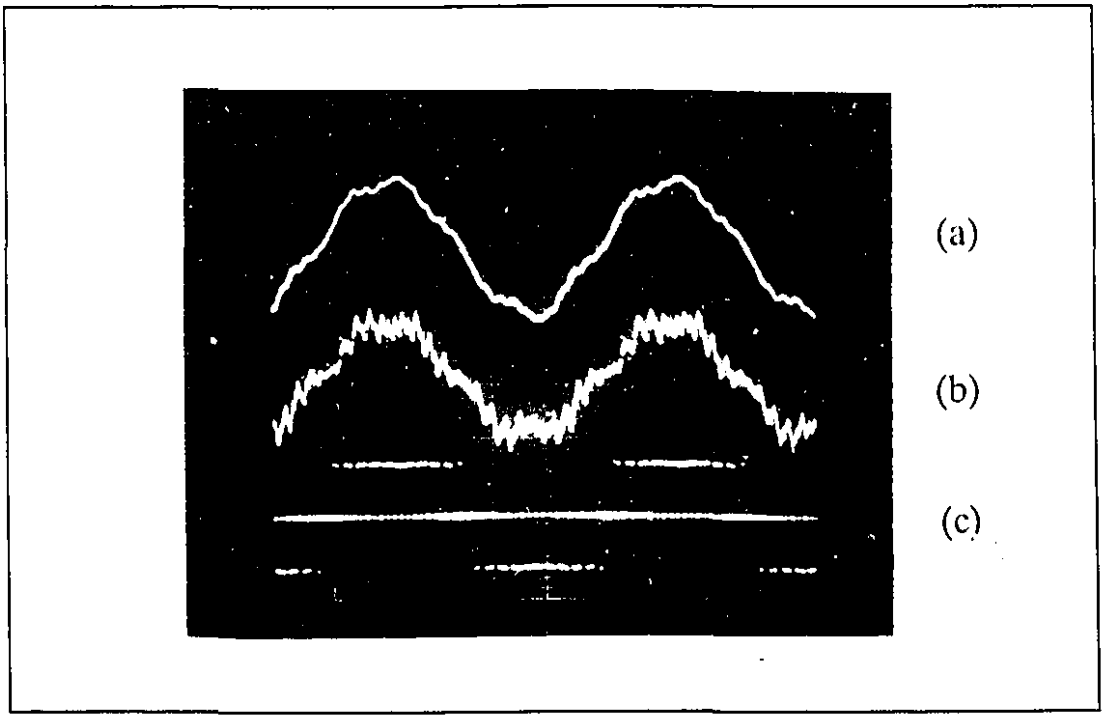


Figure 6-6 Waveforms without Pole Placement state feedback control: (a) ac line current, *5* A_{rms}; (b) capacitor voltage, *67* V_{rms}; (c) converter terminal pulse current, $i_{pj}(t)$.
(dc line current $I_{dc}=10\ A$, and load $R_{dc}+R_{load}=9\ ohm$)

because in this study the *L-C* resonance frequency has been chosen to be close to the 5th harmonic.

For comparison, Fig. 6-7 shows the same waveforms of the current-source PWM converter with the Pole Placement state feedback control under the same test condition. The state feedback gains shown in "feedback" block of Fig. 6-3, have been chosen as $K_1=-0.8289$, $K_2=0.0459$, $K_3=0.3876$ and $K_4=0.0$. These gains

assign the desired closed-loop system pole positions to be the same as the eigenvalues of Eq. (6.5) for a time constant of $\tau = 0.332\ ms$ (which corresponds to a equivalent system in which the line resistance has been increased to $R = 20\ ohm$). From Fig. 6-7, it is seen that the ac line current and the capacitor voltage are free of the lower order harmonics of Fig. 6-6, as they have been removed by the Pole Placement state feedback control.

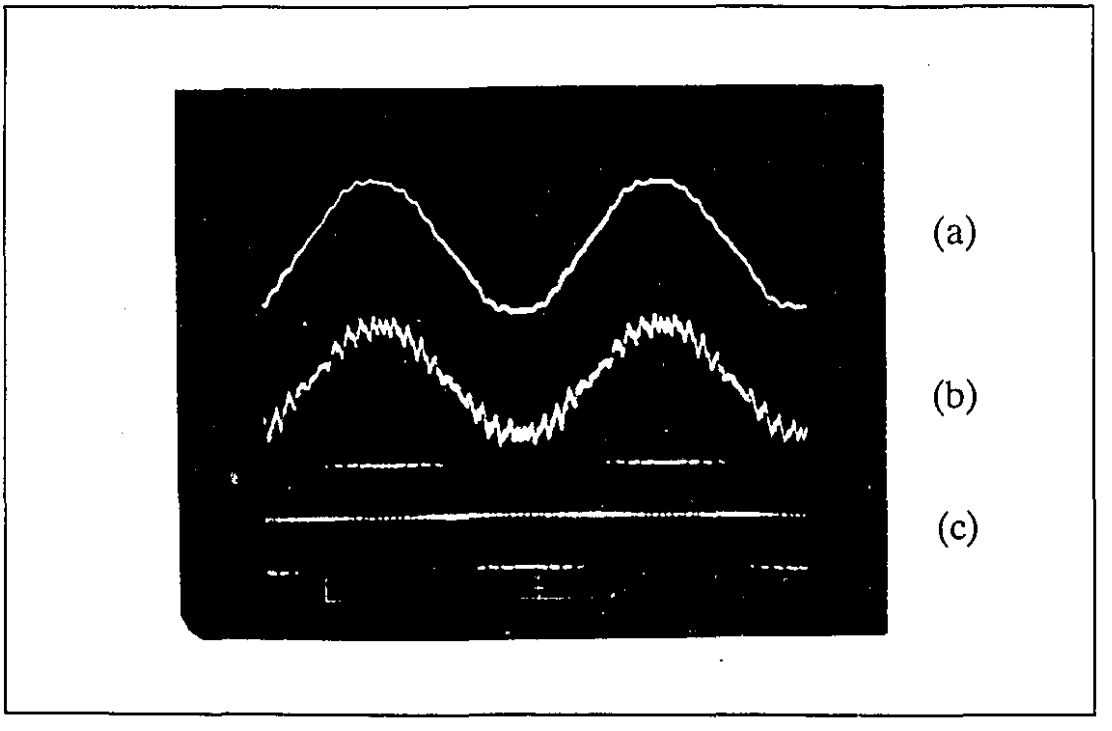


Figure 6-7 Waveforms with Pole Placement state feedback control: (a) ac line current, $5\ A_{rms}$; (b) capacitor voltage, $67\ V_{rms}$; (c) converter terminal pulse current, $i_{pj}(t)$.
(dc line current $I_{dc} = 10\ A$, and load $R_{dc} + R_{load} = 9\ ohm$)

6.6.2 Transient Test

Fig. 6-8 shows the oscillogram of: (a) the ac line current, (b) the capacitor voltage and (c) the dc link current, when the converter dc link current reference, I_{dcref}, has a step change from *8 A* to *11 A*. The dc link current regulator proportional gain $K_{P\text{-}dc}=0.19$ and integral gain $K_{I\text{-}dc}=0.02$. As can be seen, the

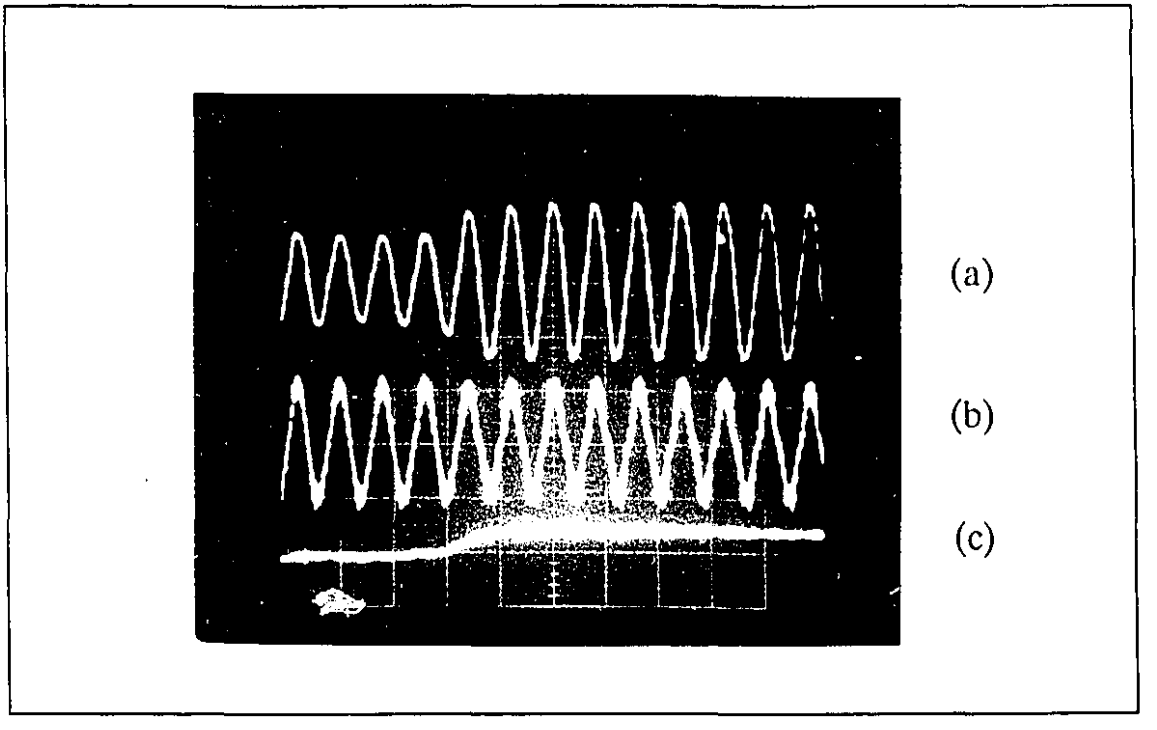


Figure 6-8 Transient response of a step change in the dc link current reference when the Pole Placement state feedback control method is used:
(a) ac line current, from *3.4* A_{rms} to *6.4* A_{rms}; (b) capacitor voltage; (c) dc link current, from *8 A* to *11 A*.
(dc resistance load $R_{dc}+R_{load}=9\ ohm$)

transient response is fast and the unity power factor ac line current is a good sine wave.

6.7 Summary

The incentive for the research of **Chapter 5** and the present chapter has been to bring to the perfection the 3-phase, 6-valve, current-source type PWM converter suitable for all power conditioning applications. The research has focused on a specific application. This is a high quality rectifier which is capable of: (i) generating almost sinusoidal current waveforms under unity power factor, (ii) actively filtering the ac line harmonics, and (iii) regulating the dc current.

The main difficulties have been identified in **Chapter 5**. The new control strategy: the Dynamic Tri-Logic Sinusoidal PWM method with the Decoupler Pre-Processor control scheme, has been proposed, analyzed and described in **Chapter 5**. This chapter has described the Pole Placement state feedback control which has been implemented by a high performance multi-DSP real-time controller. The predictions of its performance have been verified experimentally in a *1-kVA* laboratory converter.

The investigations of **Chapter 5** and the present chapter allow the following **conclusions** to be made:

(1) The high quality, unity power factor, 6-valve, 3-phase, current-source type,

PWM rectifier can be controlled entirely by software algorithm implemented by multi-DSPs. The key to the success consists of achieving a sufficiently broad frequency bandwidth channel to convey the control feedback information. This requires: (i) the use of high-speed DSPs to execute the algorithm concurrently to minimize the computational delay time in the real-time control, (ii) the use of a sufficiently high triangular carrier frequency in the SPWM strategy.

(2) The research has proposed and proven a new control design based on applying the Pole Placement state feedback technique to the inner ac line current control loop in each of the ac phases. The new design succeeds in: (i) improving the time response, (ii) actively filtering out the line harmonics.

(3) Pivotal to the success is the Dynamic Tri-Logic SPWM method and the Decoupler Pre-Processor which can be used in all 6-valve, 3-phase, current-source converter bridges. The ability of the PWM strategy to operate as a linear amplifier with respect to the control inputs is an important asset. This is because the current-source type of PWM converters are increasingly called upon to fulfil the duties of filtering, stabilization and dynamic performance enhancement.

Essentially, all the difficulties of the current-source PWM converter have been identified and removed.

CHAPTER
SEVEN

CONCLUSIONS

This thesis has contributed to the advances of the Pulse Width Modulation techniques as applied to Power Electronics. At every step, the advances have been proven, initially by digital computer simulations, then by analysis, and finally by laboratory experiments. The conclusions are reported here under the following headings:

1. Advances in Pulse Width Modulation Theory,
2. Advances in Engineering Applications.
3. Advances in the Implementation of Pulse Width Modulation Techniques.

7.1 Advances in Pulse Width Modulation Theory

7.1.1 Two-Level or Bi-Logic PWM (Part I: Chapters 2, 3 and 4)

The Two-Level or Bi-Logic PWM has existed for several decades and because of its mature state of development, there is little room for contributions.

1. Nevertheless, Part I of the thesis has uncovered the last frontier – Phase Angle Control. This completes the three control attributes of the sinusoidal waveform in PWM: the original two attributes being, Amplitude Control and Frequency Control.

2. Phase Angle Control and Frequency Control are not completely independent. If the feedback signal to the Phase Angle Controller is considered to be Proportional feedback, then the same signal to the Frequency Controller is the Integral feedback.

3. Using the Phase Angle and the Frequency Controls, the PWM converter can be synchronized to another system (such as the electric power utility system which has a nominal frequency of *50 Hz* or *60 Hz*) through phase lock principles. Depending on the feedback error, the Phase Lock Loop (PLL) enables the PWM converter to fulfil regulatory functions. The two regulatory functions, demonstrated experimentally in the research of this thesis, are:

    (i) dc voltage regulation,

(ii) dc power regulation.

4. In the electric power utility system, the Phase Angle and Frequency Controls affect the real power transmission whereas the Amplitude Control affects the reactive power.

7.1.2 Three-Level or Tri-Logic PWM (Part II: Chapters 5 and 6)

The contributions to the Three-Level or Tri-Logic PWM are extensive because it has only been recently recognized that the Current-Source, 6-Valve, 3-Phase PWM Bridge Converter must operate under Tri-Logic PWM.

5. A definitive method of generating Tri-Logic PWM from Bi-Logic PWM by the linear transformation of Eq. (5.2) in **Chapter 5** is proposed and proven by the truth table of Table 5-2.

6. Since the Tri-Logic PWM signals are generated by a linear transformation, then the preferred Bi-Logic PWM signals are those which have linear output-to-input relationship with respect to the modulating signals. An example of such a class of Bi-Logic PWM is the Sinusoidal PWM, in which the local averages of the Two-Level output pulse signals are the linearly amplified modulating signals. Thus the Tri-Logic PWM signals are also linear transformations of the modulating signals.

7. Using the Decoupler Pre-Processing Stage (Section 5.3.5), it is possible to compensate for the non-diagonal linear transformation equation of Eq.

(5.2), so that the local average of the Tri-Logic PWM signal of any of the three phases is linearly proportional to the modulating signal for that phase. The outputs and inputs of the three phases are decoupled. Essentially, the Tri-Logic PWM converter becomes three independent linear amplifiers (constant gain, without phase shift), one amplifier for each of the three phases.

8. All the linear properties of the Bi-Logic Sinusoidal PWM are conferred to the Tri-Logic PWM. For example, the ability to control (i) the Amplitude, (ii) the Frequency and (iii) the Phase Angle of the fundamental Fourier Component in the Bi-Logic PWM is also built into the Tri-Logic PWM. The linear amplifier property includes a broad frequency bandwidth channel (about 1/3 of the triangular carrier frequency) to convey non-sinusoidal signal transmission. The broad frequency bandwidth is necessary for the implementation of feedback and active filtering functions.

9. The linear transformation of Eq. 5.2 includes the switching harmonics. As the carrier and sideband harmonics of the Bi-Logic SPWM are known, the carriers and sideband harmonics of the Tri-Logic PWM are predictable, as shown in Fig. 5-5.

7.2 Advances in Engineering Applications

The applications chosen for the Bi-Logic PWM and the Tri-Logic PWM

are respectively the High Voltage Direct Current Transmission System and the Current-Source PWM Rectifier.

7.2.1 HVDC Transmission System (Part I: Chapters 2, 3 and 4)

1. The conceptual study in **Chapter 2** shows that the Voltage-Source PWM converter has performance characteristics which are superior to those of the existing line-commutated converters presently used in HVDC Transmission System. The ability to connect the dc sides of the converter stations directly in parallel, in the face of power reversals, is particularly attractive in multi-terminal application. The existing line-commutated HVDC system requires mechanical reversing switches for power reversals in multi-terminal connections.

2. The concepts are proven to be correct in **Chapter 3** in tests using *1-KVA* size converter modules. Of special interest, is the successful reversal of power in the multi-terminal connection while using local control in the individual converter station. The existing HVDC multi-terminal connections require centralized controls with remote communication links to the geographically separated stations.

3. The parametric studies of component sizes of the voltage-source PWM stations in **Chapter 4** demonstrate that they are within the "ball-park" figures of the line-commutated HVDC stations.

7.2.1.1 General Conclusion

The laboratory and the feasibility studies have shown that the concept of the Voltage-Source PWM-HVDC Transmission System is sound and merits follow-up, in-depth studies.

7.2.2 Current-Source PWM Rectifier (Part II: Chapters 5 and 6)

4. A stand-alone, 3-phase, 6-valve, current-source, PWM Rectifier has been built. Tests show that the demanding performance characteristics are all met:
   (i) Regulated dc link current,
   (ii) Unity power factor operation,
   (iii) Near sinusoidal ac current,
   (iv) Active Filtering to remove ac source harmonics,
   (v) fast response.

7.3 Advances In The Implementation of Pulse Width Modulation Techniques

The advances in the theory and the applications of Pulse Width Modulation techniques have been possible because of the advances in the methods of implementation: in hardware and in software, in analogue and in digital forms.

7.3.1 Phase Lock Loop Control (Part I: Chapters 2, 3 and 4)

Figs. A-2 and A-3 in **Appendix A** constitute a proven design of the Phase Lock Loop Control of the Voltage-Source Type Force-Commutated Converter Station. In the experimental results in **Chapter 3**, the same Phase Lock Loop Control has been used to make the Converter station into a DC Voltage Regulator and then as a Power Dispatcher simply by changing the feedback signals from Fig. 2-9 to Fig. 2-10.

To emphasize its versatility, in Ref. [86] the same controller is used to make the converter into a Static VAR Controller.

7.3.1.1 Real Power Controlled by Phase Lock Loop

Through the Phase Lock Loop Control, the PWM converter is synchronized to the nominal standard frequency of the electric utility system. The real power is controlled by the phase angle (which has the status of the proportional channel in feedback) and the frequency (which has the status of the integral channel in feedback). The reactive power is controlled through the amplitude of the PWM modulating signal.

7.3.2 Multi-DSP Controlled Current-Source PWM Rectifier (Part II: Chapters 5 and 6)

In Part I, the hardware implementation is hybrid: a mixture of analogue and digital methods. In the control of the current-source PWM converter in Part

II, the objective is to realize an entirely digital controller based on a multi-DSP platform and PAL (Programmable Array Logic) circuit. The multi-DSP platform has been designed and constructed by a fellow Ph.D. candidate, Ms. Y. Guo [94-96]. The feedforward, the feedback and regulatory controls of **Chapter 6** are realized by software programs (**Appendix C**) executed in real-time.

7.3.2.1 Frequency Bandwidth and Computational Delays

A very important conclusion of this research is the necessity to reduce computational delays by parallel processing so as to secure sufficient frequency bandwidth in the PWM controller to implement the Pole-Placement strategies. Laboratory experience shows that without the frequency bandwidth, the stability and the active filtering cannot be achieved.

7.3.2.2 Implementation of Dynamic Tri-Logic PWM

A very important contribution to reducing the computational delays is the use of Programmable Array Logic (PAL). The design of the PAL Gating Logic Circuit is shown in Fig. B-3 in **Appendix B.** The program lists of PAL chip designs are in Tables B-1 to B-6 of **Appendix B.** The PAL circuits implement the Tri-Logic SPWM described in **Chapter 5.**

7.3.2.3 Innovative Feedback Method

Another contribution to reducing the computational delay is the Innovative

Feedback Method in which the ac side equations remain in the *a-b-c* frame, thus avoiding the steps of transformations to the *o-d-q* frame and back.

The Innovative Feedback Method achieves Active Filtering from the Pole-Placement strategy which is originally intended for fast time response characteristics.

7.4 Suggestions For Future Work

The Bi-Logic PWM has an extensive literature and future advance in the theory is the range of diminishing returns. The Tri-Logic PWM is still in its infancy and there is scope for important contributions, especially in the Dynamic Type.

This thesis has opened up the application of PWM techniques in the utility environment. Because of switching losses, future research should concentrate on the lowest possible switching frequencies of the PWM technique. Beside HVDC, the future work will be on Static VAR Compensators (Shunt and Series Types), Phase Shifters, Power Conditioners for Storage Systems.

APPENDIX
A

IMPLEMENTATION OF VOLTAGE-SOURCE PWM CONVERTER

A.1 Introduction

The experimental work, in the research of the PWM-HVDC transmission system of **Chapters 2-4**, has been successfully carried out by using two *1-kVA* size bipolar transistor converter bridges to present two PWM-HVDC stations. The converter bridges have been built in our power electronics laboratory. A detail description of each converter can be found in Appendix-B of Ref.[89].

For demonstrating and verifying the concepts of the PWM-HVDC transmission system, a new design of the phase lock loop controller, described in **Chapter 2**, has been implemented. By configuring the feedback controls the converter is made to operate either as a DC Voltage Regulator (*VR*) or as a Power Dispatcher (*DISP*). A brief description of the hardware design and

practical implementation of this controller is given here. Figs. A-1, A-2 and A-3 show the circuit diagrams of the controller in detail.

A.2 Sinusoidal Modulating Signal

In the design, the 3-phase Sinusoidal PWM modulating signals, *Vm-A*, *Vm-B* and *Vm-C* as shown in Fig. A-1, are generated using the so-call "EPROM" method. Each of the 3-phase sinusoidal waveform templates in one complete period is sampled equally by $2^9=512$ points. The samples are then digitized (8-bit resolution) and stored in three EPROMs (2764s), one for each phase. When the EPROMs are addressed by a 9-bit number (*A0-A8*), the outputs from the EPROMs are converted into 3-phase analog sinusoidal waveforms, *Vm-A*, *Vm-B* and *Vm-C*, through the *D-to-A* converting circuits (consisting of the MC1408s and LM747s, shown in Fig. A-1). In the experiments, the amplitudes of the analog modulating signals are kept as constants which correspond to the modulating index $M=0.8$. The frequency of the modulating signals is determined by the rate at which the 9-bit address counter is increased by the VCO (*voltage controlled oscillator*).

A.3 The PLL Control

The PLL (*phase lock loop*) control, with the switch *S* turned to the position of *1* shown in Fig. A-2, is used to synchronize the output modulating signals, *Vm-A*, *Vm-B* and *Vm-C*, to the utility ac line voltages prior to the closing the circuit breaker. The utility has the nominal frequency of the *60* or *50 Hz* standards and

the autonomous frequency of the converter bridge has to be synchronized to the utility frequency. The chip CD4046 in Fig. A-2 plays a key role in the PLL control, which consists of a phase comparator and a VCO (*voltage controlled oscillator*). The output pulse signal from the VCO (*VCOUT* pin) is used as the clock of a 12-bit binary counter (74LS161s) shown in Fig. A-3. The most significant 9 bits of the counter (*Y3-Y11*) are chosen to address the EPROMs. In order to obtain the *60 Hz* sine-wave output, the central frequency of the VCO is set at $fo=60\times2^{12}=245760$ *Hz* by choosing the values of *R1*, *R2* and *CX* under the condition that the VCO input voltage $VCOIN=0.5Vdd=2.5$ *V*. The *2.5 V* can be obtained by adjusting the potentiometer *Rf*. The phase angle of the ac source voltage is measured using a *Zero-Crossing Detector* circuit (consisting of a second-order filter and two comparators, LM318 and LM319). The output phase signal, *SP*, with the duty ratio of *1:1*, is sent into the phase comparator on the chip CD4046 through the pin *SIN*, and compared with the MSB bit of the counter, *Y11*. The phase error, *PE*, between signals of *SP* and *Y11* is obtained by filtering the harmonics and removing the dc offset components contained in the output of phase comparator, *P1*, through a *R-C* low-Pass (*LP*) filter and an adder circuit. The error signal *PE* is used as a negative feedback signal, $\Delta\omega$, to adjust the VCO output frequency so as to vary the cycling rate of the counter to null the error of *PE*.

A phase angle control channel is inserted into the PLL control as shown in Fig. A-3. The analog phase angle control signal, $\Delta\delta$, is firstly digitalized into a 8-

bit binary number (*X0-X7*) through an *A-to-D* converter (ADC0804), then added onto the number contained in the address by a 9-bit binary adder circuit (74LS83s and 74LS373), so that the EPROM address (*A0-A8*) is equal to (*Y3-Y11*)+(*X0-X7,X7*). Thus an instantaneous change in the phase angle of modulating signal can be implemented. The phase angle control channel is effectively a proportional feedback channel because the modulating signal phase shift is proportional to the control signal $\Delta\delta$. Normally, during the procedure of closing circuit breaker, the $\Delta\delta$ is adjusted as zero as the converter is not loaded.

A.4 The VR/DISP Control

By turning the switch *S* to the position of *2* after the converter circuit breaker has been closed, the converter operates as either a voltage regulator (*VR*) or a power dispatcher (*DISP*). In the case of *VR*, the dc link voltage is measured using a Hall Effect (LEM) sensor circuit (with the frequency bandwidth *0-100 kHz*) shown in Fig. A-2. The error signal, *ER*, between *Vdc* and its reference setting is obtained from the *feedback comparator*, then amplified and fed to the VCO and the phase angle control circuits respectively to adjust the control signals $\Delta\omega$ and the $\Delta\delta$. For the case of *DISP*, the only change needed is the feedback signal, which is now the signal *Idc*, whose Hall Effect (LEM) feedback sensor circuit is shown in Fig. A-2 also.

All of the control circuits shown in Figs. A-1, A-2 and A-3 have been built on breadboards.

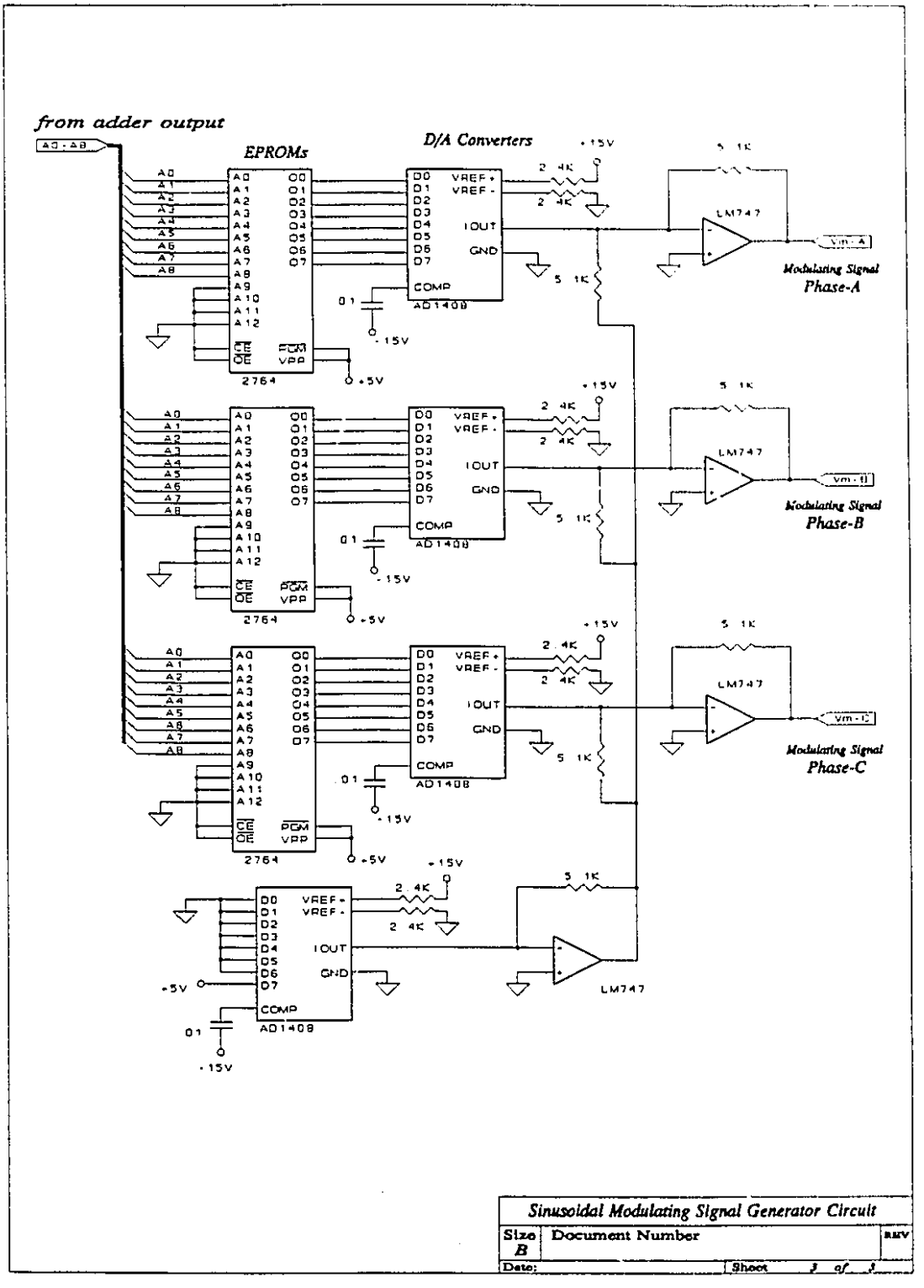


Figure A-1 Sinusoidal Modulating Signal Generator Circuit.

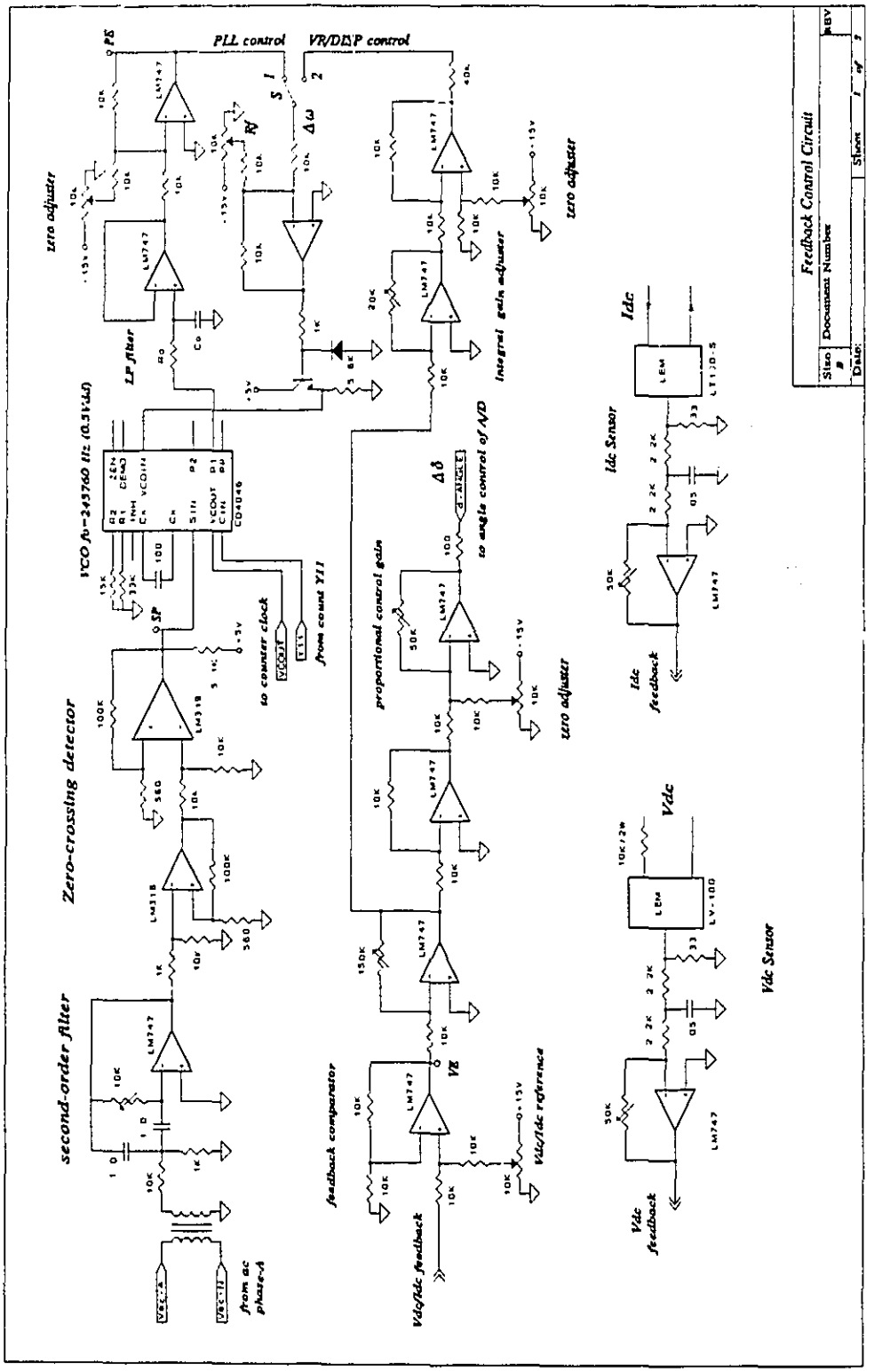


Figure A-2 Phase-Locked Loop Controller.

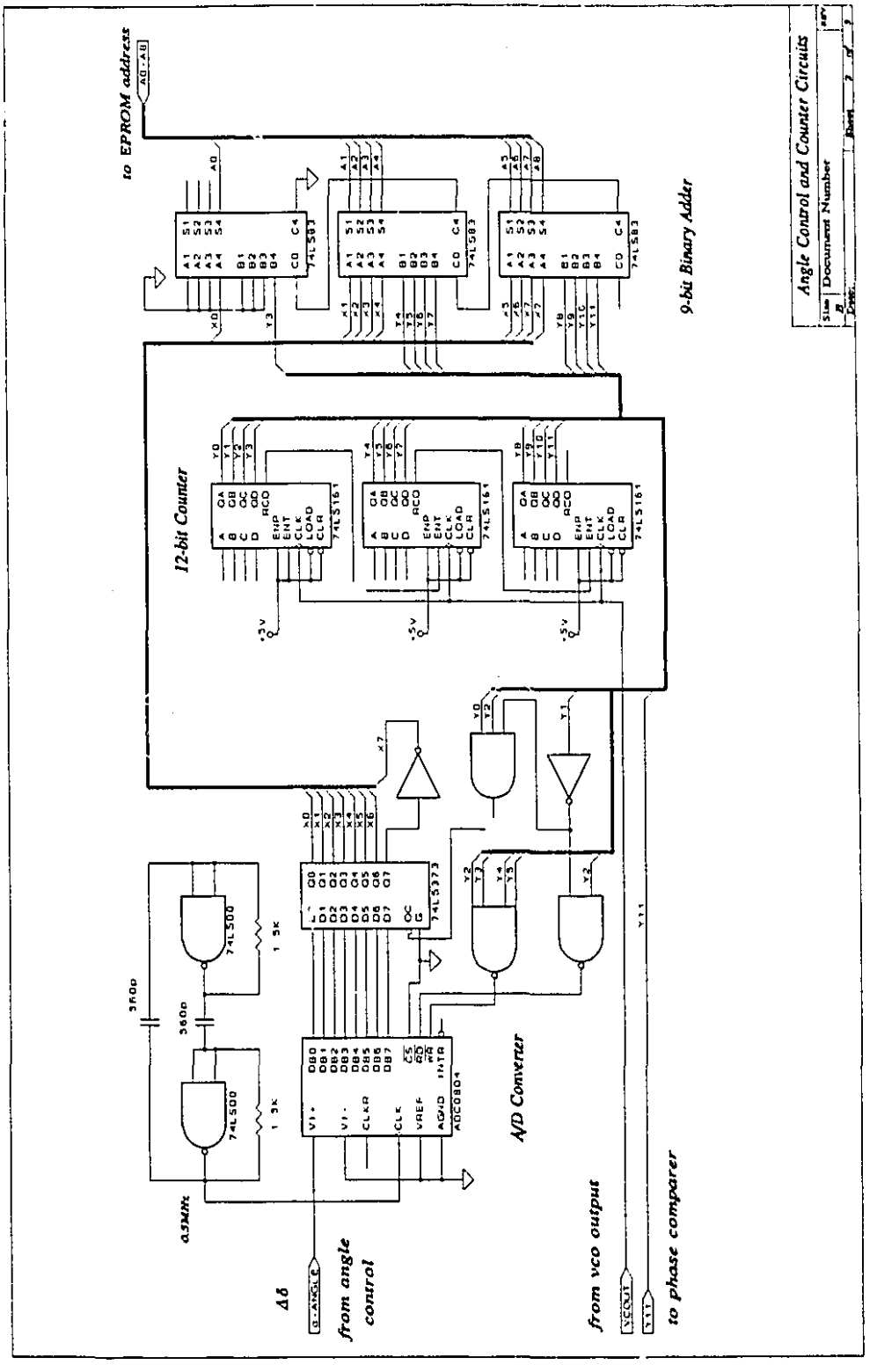


Figure A-3 EPROM Address Generator Circuit.

APPENDIX
B

IMPLEMENTATION OF DYNAMIC TRI-LOGIC PWM CONTROL

B.1 Introduction

Fig. B-1 shows a photograph of the experimental set-up of a multi-DSP controlled, *1-KVA* size of 3-phase, 6-valve, current-source PWM converter system, which has been implemented for demonstrating and verifying the concepts described in **Chapters 5** and **6**. The main converter, shown by the arrow *A*, has been inherited from previous researches [69-72] in our laboratory. Here, it has been reconnected into a 3-phase, 6-valve, current-source PWM converter bridge. A multi-DSP controller [94-96] and a PC XT computer have been employed to perform all the feedback control tasks described in **Chapter 6**. The controller consists of three high speed Texas Instrument TMS320C25 DSPs and execute the feedback calculations in parallel. The control programs are compiled and then

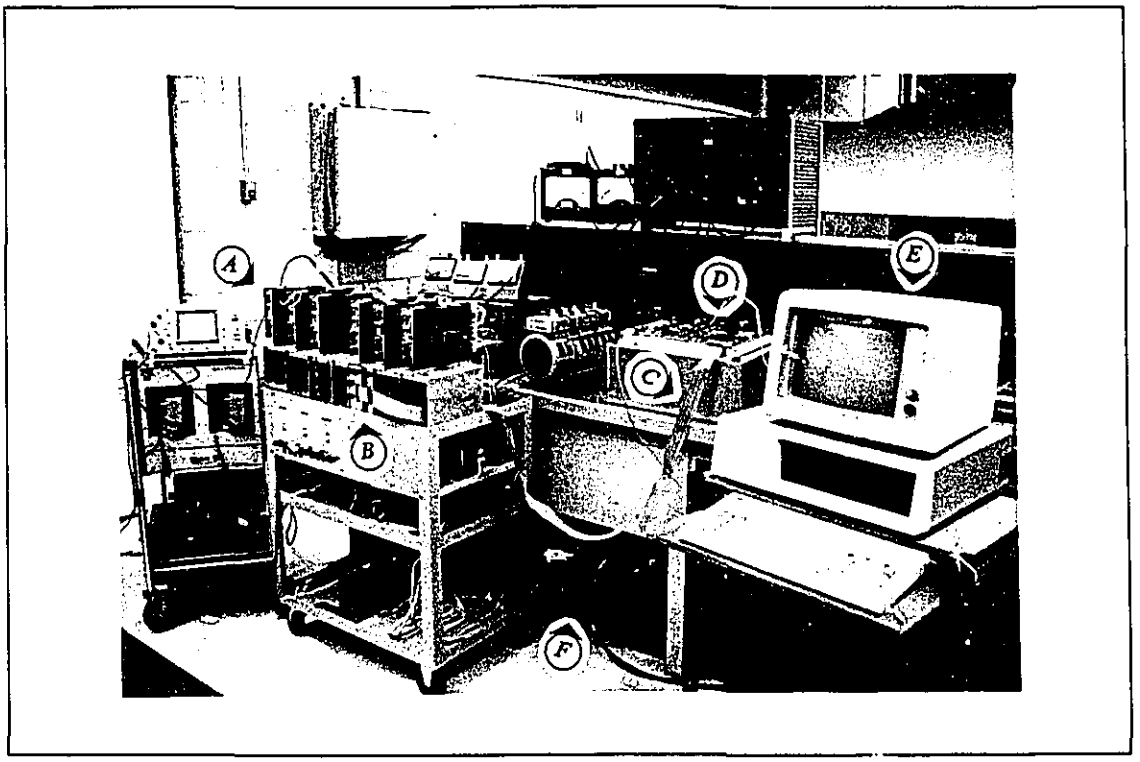


Figure B-1 Experimental set-up of the multi-DSP controlled 3-phase, current-source PWM converter system.
A) *1-KVA* size of bipolar transistor PWM converter bridge, B) PAL Gating Logic and A/D converter circuit boards, C) Data transmission cable, D) Multi-DSP controller board, E) PC-XT computer, F) inductor and capacitor boxes.

the machine codes are download to each DSP by using the PC XT computer. A new PAL Gating Logic circuit and a four channel A/D Converter circuit have been built and installed onto the converter, shown by the arrow *B*, to perform the functions or the Bi/Tri-Logic SPWM Translation (Section 5.3.2 of Chpater 5) and the feedback signal sampling. The data are transmitted between the multi-DSP

controller and the PAL circuits through a parallel cable shown by the arrow *C*.

B.2 Converter Bridge Circuit

Fig. B-2 shows the main converter bridge circuit of the 3-phase, 6-valve Current-source PWM converter. A detail description for each of the six switch units can be found in Ref.[72] (the component parameters in the Base Drive circuit have been modified here to improve the switching speed). A dc snubber circuit, consisting of R_s, C_s and D_s, is connected across the dc terminals for protection against $L_{dc}dI_{dc}/dt$ voltage. As mentioned in **Chapter 5**, because of the ac capacitors, a reverse biased capacitor voltage can appear directly across on a valve which is receiving a turning ON signal. This valve will be remain turned OFF until the reverse biased voltage is removed by the proper turning OFF of other valve. During this transient period both valves are OFF and the dc snubber circuit provides the dc link current with an alternate path so as to eliminate the large inductive voltage across the dc line inductance which can damage the switch device.

B.3 PAL Gating Logic Circuit

Fig. B-3 shows the circuit of PAL Gating Logic circuit. It receives the 3-phase Bi-Logic SPWM signals, *S-abc* (or X_a, X_b and X_c in Fig. 5-1), from the multi-DSP controller and translates them into the Tri-Logic SPWM signals

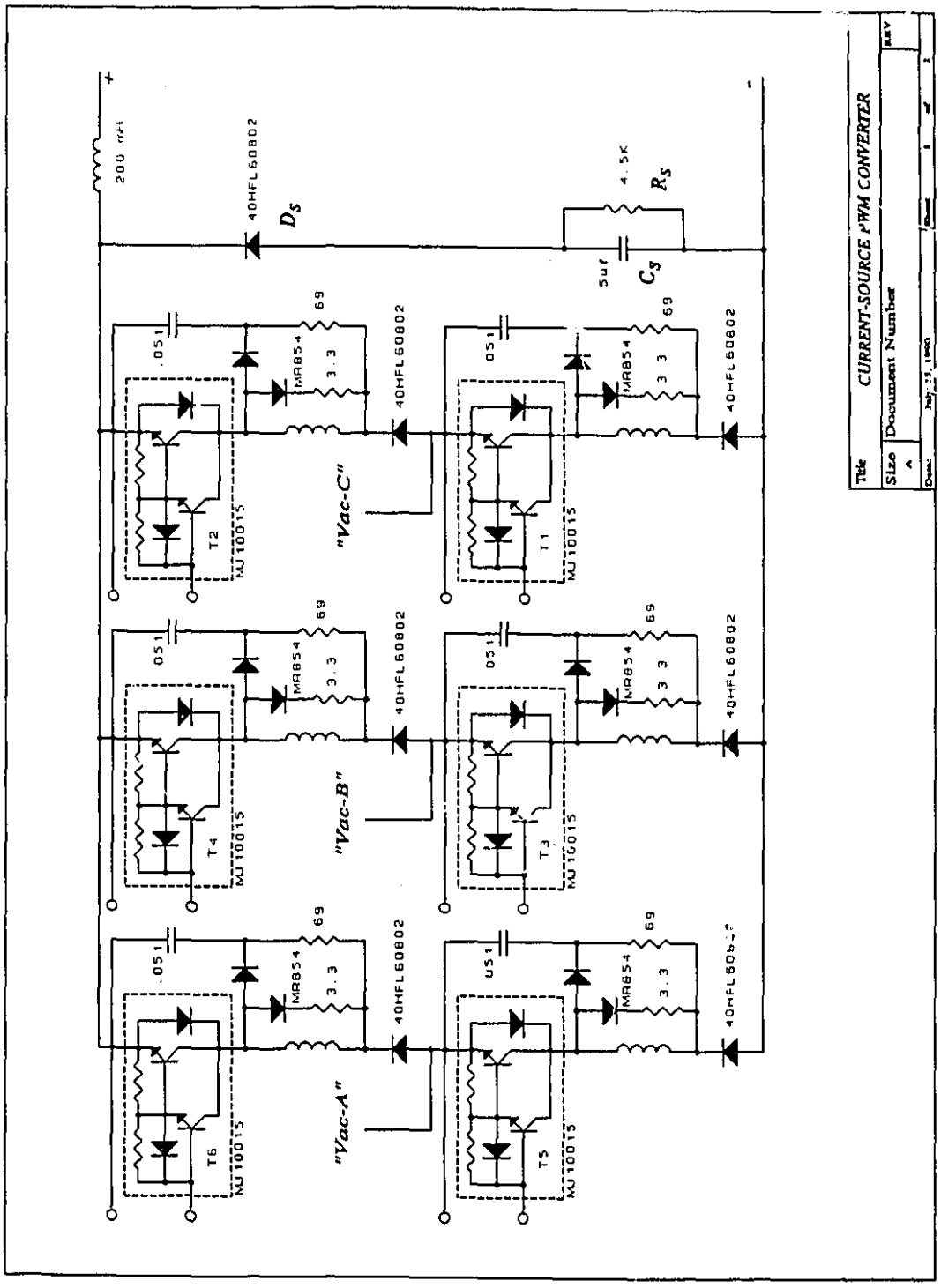


Figure B-2 The main switching circuit of 3-phase current-source PWM converter.

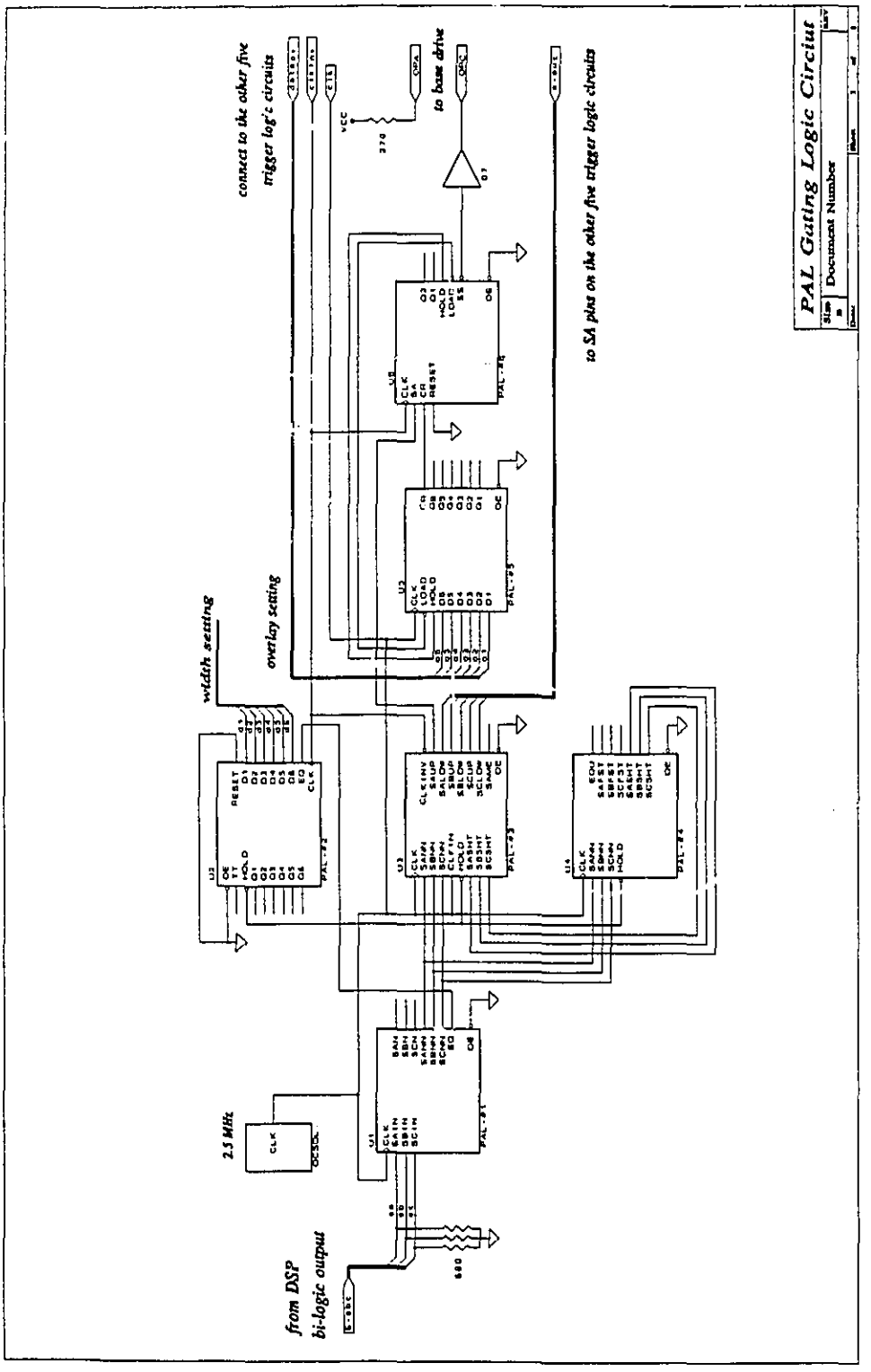


Figure B-3 PAL Gating Logic Circuit.

through the PAL chips *U1-U4*. The output Tri-Logic SPWM triggering signals are finally sent to each valve through the PAL chips *U5-U6*.

B.3.1 Bi/Tri-Logic Translation Circuit Programming

Table B-1 is the program list of the design for chip *U1*. Its function is to sample the Bi-Logic SPWM input signals *S-abc* at each rising edge of the circuit clock, and then output the signal *EQ* to indicate that a change has occurred in the signals *S-abc*.

Table B-2 shows the program list of the design for chip *U2*. Its function is to eliminate very narrow triggering pulses in the signals *S-abc* so as to protect the valve from unnecessary fast switching and from the effects of the noise in the signals *S-abc*. The data of *D1-D6* specify the width setting for the narrow pulse elimination.

The chip *U3* plays the function of The Bi/Tri-logic SPWM Translation and the *U4* determines the shoot-through signals based on the methods described in Section 5.3.3 of **Chapter 5.** The details of the designs for chips *U3* and *U4* are listed in Table B-3 and B-4, respectively.

B.3.2 Triggering Logic Circuit Programming

In Fig. B-3, chips *U5* and *U6* produce the trigger signal for one of the six valves of the converter bridge. The triggering logic circuits for the other five valves are exactly identical. The chip *U6* adds a short delay time to the turning

OFF edge of the triggering signal. Thus there is a short overlap time druing which both valves are ON as one valve is receiving the turning ON signal and other is being turned OFF. The object is to shorten the switching transent. The chip *U5* controls the width of this short overlap by choosing the date of *O1-O6*.

The output trigger signal at the terminals *OPA* and *OPC* is used directly to drive the optocoupler in the Base Drive circuit of valve (which is not shown in Fig. B-2).

All of the PAL circuit designs in Fig. B-3 are implemented by using the specialized chip GAL16V8-25ns [97], which can be programmed to assume different function by using '*OrCAD/PLD*' [98] as the CAD tools. The design has

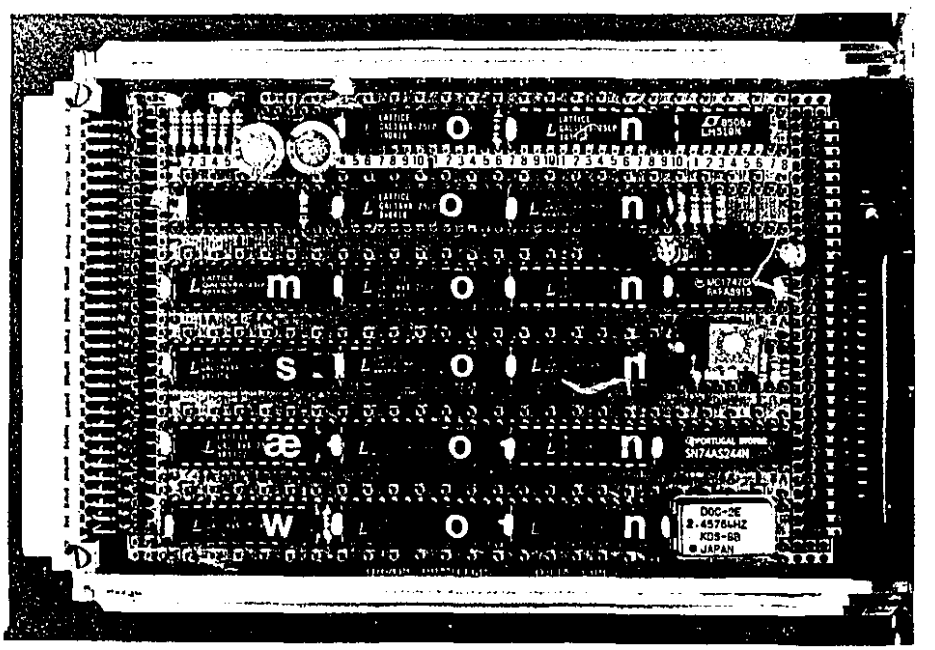


Figure B-4 The PAL Gating Logic circuit Implementation Using The Speedwire board.

been tested on a *speedwire circuit board* as shown in Fig. B-4. Table B-1 to B-6 show the logic designs

Table B-1 The Program List of PAL Chip #1 Design.

```
*************************************************************************
* CHIP NAME    : PAL-#1                                                 *
* FUNCTION     : latch the bi-logic SPWM input signals                  *
*************************************************************************

|PAL16RP8  indate, sbin, scin),
|          out: (san, sbn, scn, sann, sbnn, scnn, eq),
|          clock: clk
|
| active-high: "all"
|
| san = sain
| sbn  scn = scin
| sann  = san
| sbnn = sbn
| scnn = scn
| eq = (san' & sbn' & scn' & sann' & sbnn' & scnn')
|      # (san' & sbn' & scn  & sann' & sbnn' & scnn )
|      # (san' & sbn  & scn' & sann' & sbnn  & scnn')
|      # (san' & sbn  & scn  & sann' & sbnn  & scnn )
|      # (san  & sbn' & scn' & sann  & sbnn' & scnn')
|      # (san  & sbn' & scn  & sann  & sbnn' & scnn )
|      # (san  & sbn  & scn' & sann  & sbnn  & scnn')
|      # (san  & sbn  & scn  & sann  & sbnn  & scnn )
```

Table B-2 The Program List of PAL Chip #2 Design.

```
*************************************************************************
* CHIP NAME    : PAL-#2                                                 *
* FUNCTION     : counting the width of input pules                      *
*************************************************************************

|PAL16RP8  in: (eq, d[6~1], reset),
|          out: (q[6~1], ttr[2~1]),
|          clock: clk
|
| active-high: "all"
|
| procedure: reset, ttr[2~1]
| { states:   state1 = 00b,
|             state2 = 01b,
|             state3 = 10b
|
|  state1.    eq? -> state2
|             -> state1
|  state2.    eq'? -> state1
|             eq & q[6~1] = =0? -> state3
|             -> state2
|  state3.    eq'? -> state1
|             -> state3   }
|
```

```
| q1 = ((q1' & ttr[2~1] = =1 & eq)
|     # (d1 & (ttr[2~1] = =0 # ttr[2~1] = =2 # eq'))) & reset'
| q2 = ((((q1 & q2) # ( q1' & q2')) & ttr[2~1] = =1 & eq)
|     # (d2 & (ttr[2~1] = =0 # ttr[2~1] = =2 # eq'))) & reset'
| q3 = (((q[3~1] = =0 # q[3~1] = =7 # q[3~1] = =6 # q[3~1] = =5) & ttr[2~1] = =1 & eq)
|     # (d3 & (ttr[2~1] = =0 # ttr[2~1] = =2 # eq'))) & reset'
| q4 = (((q[4~1] = =0 # (q[4~1]/ =8 & q4)) & ttr[2~1] = =1 & eq)
|     # (d4 & (ttr[2~1] = =0 # ttr[2~1] = =2 # eq'))) & reset'
| q5 = (((q[5~1] = =0 # (q[5~1]/ =16 & q5)) & ttr[2~1] = =1 & eq)
|     # (d5 & (ttr[2~1] = =0 # ttr[2~1] = =2 # eq'))) & reset'
| q6 = ((q[6~1]/ =32 & q6 & ttr[2~1] = =1 & eq)
|     # (d6 & (ttr[2~1] = =0 # ttr[2~1] = =2 # eq'))) & reset'
```

Table B-3 The Program List of PAL Chip #3 Design.

```
*****************************************************************************
* CHIP NAME    : PAL-#3 (version 3)                                         *
* FUNCTION     : bi-logic to tri-logic transformation                       *
*****************************************************************************

|PAL16RP6  In: (sa, sb, sc, clkin, hold, sasht, sbsht, scsht),
|          Io: (clkinv, same),
|          out: q[6~1],
|          clock: clk
|
| active-low: hold
| registers: q[6~1]
|
| same = (sa & sb & sc) # (sa' & sb' & sc')
|
| q6 = (sa & sb' & hold')
|     # (same & sasht  & sbsht' & scsht' & hold')
|     # (same & sasht' & sbsht' & scsht' & q6 & hold')
|     # (same & sasht  & sbsht  & q6  & hold')
|     # (same & sasht  & scsht  & q6  & hold')
|     # (same & sbsht  & scsht  & q6  & hold')
|     # (same & q6  & q5  & q4' & q3' & q2' & q1' & hold')
|     # (q6 & hold)
| q5 = (sa' & sb & hold')
|     # (same & sasht  & sbsht' & scsht' & hold')
|     # (same & sasht' & sbsht' & scsht' & q6 & hold')
|     # (same & sasht  & sbsht  & q6  & hold')
|     # (same & sasht  & scsht  & q6  & hold')
|     # (same & sbsht  & scsht  & q6  & hold')
|     # (same & q6  & q5  & q4' & q3' & q2' & q1' & hold')
|     # (q5 & hold)
| q4 = (sb & sc' & hold')
|     # (same & sasht' & sbsht  & scsht' & hold')
|     # (same & sasht' & sbsht' & scsht' & q4 & hold')
|     # (same & sasht  & sbsht  & q4  & hold')
|     # (same & sasht  & scsht  & q4  & hold')
|     # (same & sbsht  & scsht  & q4  & hold')
|     # (same & q6' & q5' & q4  & q3  & q2' & q1' & hold')
|     # (q4 & hold)
| q3 = (sb' & sc  & hold')
|     # (same & sasht' & sbsht  & scsht' & hold')
|     # (same & sasht' & sbsht' & scsht' & q4 & hold')
|     # (same & sasht  & sbsht  & q4  & hold')
|     # (same & sasht  & scsht  & q4  & hold')
|     # (same & sbsht  & scsht  & q4  & hold')
|     # (same & q6' & q5' & q4  & q3  & q2' & q1' & hold')
|     # (q3 & hold)
| q2 = (sc & sa' & hold')
|     # (same & sasht' & sbsht' & scsht & hold')
|     # (same & sasht' & sbsht' & scsht' & q2 & hold')
|     # (same & sasht  & sbsht  & q2  & hold')
|     # (same & sasht  & scsht  & q2  & hold')
|     # (same & sbsht  & scsht  & q2  & hold')
```

```
|     # (same & q6' & q5' & q4' & q3' & q2  & q1  & hold')
|     # (q2 & hold)
| q1 = (sc' & sa  & hold')
|     # (same & sasht' & sbsht' & scsht & hold')
|     # (same & sasht' & sbsht' & scsht' & q2 & hold')
|     # (same & sasht  & sbsht  & q2  & hold')
|     # (same & sasht  & scsht  & q2  & hold')
|     # (same & sbsht  & scsht  & q2  & hold')
|     # (same & q6' & q5' & q4' & q3' & q2  & q1  & hold')
|     # (q1 & hold)
|
| clkinv = 1 ?? clkin'
```

Table B-4 The Program List of PAL Chip #4 Design.

```
*************************************************************************************************
* CHIP NAME     : PAL-#4                                                                        *
* FUNCTION      : store previous bi-logic input signals, produce shoot-through signal           *
*************************************************************************************************
|PAL16RP8  in: (sann, sbnn, scnn, hold),
|             out: (equ, safst, sbfst, scfst, sasht, sbsht, scsht),
|             clock: clk
|
| active-low: hold
|
| equ = (sann' & sbnn' & scnn' & hold')
|       # (sann  & sbnn  & scnn  & hold')
|       # (equ & hold)
|
| safst = (sann  & equ  & hold')
|       # (safst & equ' & hold')
|       # (safst & hold)
| sbfst = (sbnn  & equ  & hold')
|       # (sbfst & equ' & hold')
|       # (sbfst & hold)
| scfst = (scnn  & equ  & hold')
|       # (scfst & equ' & hold')
|       # (scfst & hold)
| sasht = (sann  & sbnn' & scnn  & safst  & sbfst' & scfst  & equ' & hold')
|         # (sann  & sbnn' & scnn  & safst  & sbfst' & scfst' & equ' & hold')
|         # (sann  & sbnn' & scnn' & safst  & sbfst' & scfst  & equ' & hold')
|         # (sann' & sbnn  & scnn' & safst' & sbfst  & scfst' & equ' & hold')
|         # (sann' & sbnn  & scnn  & safst' & sbfst  & scfst' & equ' & hold')
|         # (sann' & sbnn  & scnn' & safst' & sbfst  & scfst  & equ' & hold')
|         # (sasht & ((sann & sbnn & scnn) # (sann' & sbnn' & scnn') # equ # hold))
| sbsht = (sann  & sbnn  & scnn' & safst  & sbfst  & scfst' & equ' & hold')
|         # (sann  & sbnn  & scnn' & safst' & sbfst  & scfst' & equ' & hold')
|         # (sann' & sbnn  & scnn' & safst  & sbfst  & scfst' & equ' & hold')
|         # (sann' & sbnn' & scnn  & safst' & sbfst' & scfst  & equ' & hold')
|         # (sann  & sbnn' & scnn  & safst' & sbfst' & scfst  & equ' & hold')
|         # (sann' & sbnn' & scnn  & safst  & sbfst' & scfst  & equ' & hold')
|         # (sbsht & ((sann & sbnn & scnn) # (sann' & sbnn' & scnn') # equ # hold))
| scsht = (sann  & sbnn' & scnn' & safst  & sbfst' & scfst' & equ' & hold')
|         # (sann  & sbnn  & scnn' & safst  & sbfst' & scfst' & equ' & hold')
|         # (sann  & sbnn' & scnn' & safst  & sbfst  & scfst' & equ' & hold')
|         # (sann' & sbnn  & scnn  & safst' & sbfst  & scfst  & equ' & hold')
|         # (sann' & sbnn  & scnn  & safst' & sbfst' & scfst  & equ' & hold')
|         # (sann' & sbnn' & scnn  & safst' & sbfst  & scfst  & equ' & hold')
|         # (scsht & ((sann & sbnn & scnn) # (sann' & sbnn' & scnn') # equ # hold))
```

Table B-5 The Program List of PAL Chip #5 Design.

```
*************************************************************************************
* CHIP NAME     : PAL-#5                                                            *
* FUNCTION      : 6 bits down counter used with PAL-#8 to count the overlap width   *
*************************************************************************************

|PAL16RP6  in: (load, hold, d[6~1]),
|          io: cr,
|          out: q[6~1],
|          clock: clk
|
| active-low: load
|
| q1 = (q1' & load' & hold')
|    # (q1 & load' & hold)
|    # (d1 & load)
| q2 = (((q1 & q2) # ( q1' & q2')) & load' & hold')
|    # (q2 & load' & hold)
|    # (d2 & load)
| q3 = ((q[3~1] == 0 # q[3~1] == 7 # q[3~1] == 6 # q[3~1] == 5) & load' & hold')
|    # (q3 & load' & hold)
|    # (d3 & load)
| q4 = ((q[4~1] == 0 # (q[4~1]/ == 8 & q4)) & load' & hold')
|    # (q4 & load' & hold)
|    # (d4 & load)
| q5 = ((q[5~1] == 0 # (q[5~1]/ == 16 & q5)) & load' & hold')
|    # (q5 & load' & hold)
|    # (d5 & load)
| q6 = (q[6~1]/ == 32 & q6 & load' & hold')
|    # (q6 & load' & hold)
|    # (d6 & load)
|
| cr = 1 ?? q[6~1] == 0
```

Table B-6 The Program List of PAL Chip #6 Design.

```
*************************************************************************************
* CHIP NAME     : PAL-#6                                                            *
* FUNCTION      : add a overlap in falling edge                                     *
*************************************************************************************

|PAL16RP6  in: (sa, cr, reset),
|          out: (q[2~1], hold, ldi, ss),
|          clock: clk
|
| active-low: ss
| register: q[2~1], hold, ldi, ss
|
| procedure: reset, q[2~1]
| {  state:   state1 = 0,
|             state2 = 3,
|             state3 = 2
|
|  state1.    ss=0
|             hold=1
|             ldi=0
|             sa? -> state2
|             -> state1
|  state2.    ss=1
|             hold=1
|             ldi=0
|             sa'? -> state3
|             -> state2
|  state3.    ss=1
|             hold=0
|             ldi=1
|             cr? -> state1
|             -> state3     }
```

B.4 A/D Converter Circuit

A four-channel A/D converter circuit has been built. The design is shown in Fig. B-5. The device PCM-78P is a serial output type A/D converter with the conversion time of *6.2 μs* under *6 MHz* operating clock frequency. After receiving a "*start*" signal from the multi-DSP controller, the four channel input signals are sampled simultaneously and held by four S/H devices SHC-5320s. Then the four sampled signals are sent to the A/D converter sequentially through the multiplexer 4052. The four digital output data from the A/D are transmitted to the DSP #3 through a serial port. The whole A/D conversion procedure is controlled by the PAL control circuit consisting of the chips PAL-ADC-#1 and #2. A time of *33 μs* is needed for a complete conversion cycle. Fig. B-6 shows the implementation of the circuit. Tables B-7 and B-8 list the programs of the PAL control circuit designs.

B.5 Voltage Sensor Circuit

The broad bandwidth voltage sensor circuit shown in Fig. B-7 is used to measure the ac capacitor voltage waveform in the feedback control.

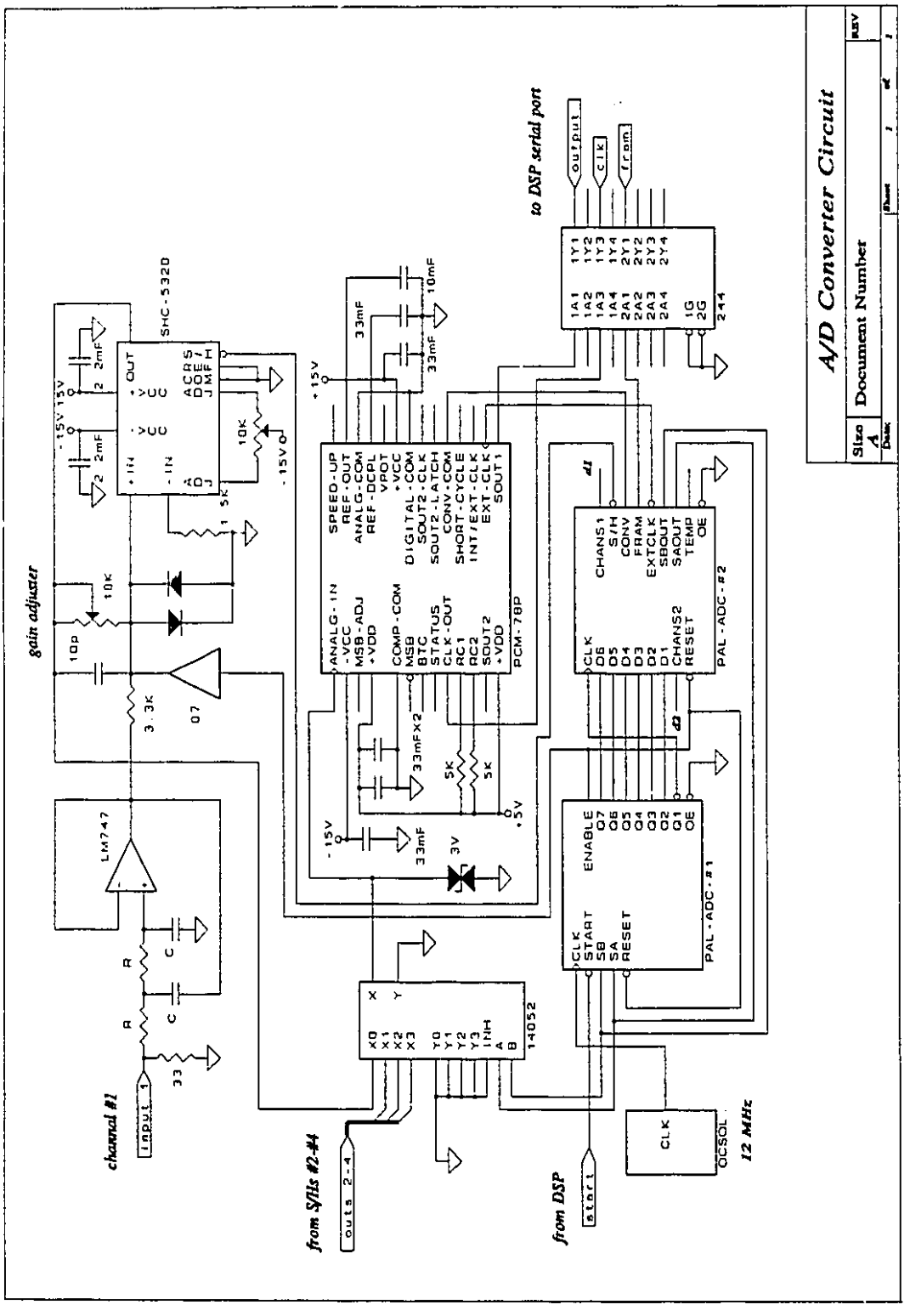


Figure B-5 The A/D converter circuit

Table B-7 The Program List of PAL Chip PAL-ADC-#2 Design.

```
*************************************************************************************
* CHIP NAME    : PAL-A/D#2                                                          *
* FUNCTION     : A/D control circuit (2), control analog-multiplexer, generate sampling, conv, ext.clock *
*                and frame pulses.                                                  *
*                clock is the LSB of the PAL-A/D#1                                  *
*************************************************************************************

| PAL16RP8  in: (d[8~1], chann2, reset),
|           lo: (chann1, temp),
|           out: (sh, conv, frm, extclk, sb, sa),
|           clock: clk
|
| active-low: sh, reset
|
| temp = 1 ?? d[8~1] = =0
|
| chann1 = 0 ?? 0                    | to be used as input pin
|
| sh = (d[8~1] = =62 # d[8~1] = =61 # d[8~1] = =60 # d[8~1] = =59 # d[8~1] = =58 # d[8~1] = =57
|    # d[8~1] = =56 # d[8~1] = =55 # d[8~1] = =54 # d[8~1] = =53 # d[8~1] = =52 # d[8~1] = =51
|    # d[8~1] = =50 # d[8~1] = =49 # d[8~1] = =48 # d[8~1] = =47 # d[8~1] = =46 # d[8~1] = =45)
|    & reset'
|
| conv = d[8~1] = =37 & reset'
|
| frm = (d[8~1] = =35
|     # d[8~1] = =34) & reset'
|
| extclk = (d[8~1] = =35 # d[8~1] = =33 # d[8~1] = =31 # d[8~1] = =29 # d[8~1] = =27
|        # d[8~1] = =25 # d[8~1] = =23 # d[8~1] = =21 # d[8~1] = =19 # d[8~1] = =17
|        # d[8~1] = =15 # d[8~1] = =13 # d[8~1] = =11 # d[8~1] = =09 # d[8~1] = =07
|        # d[8~1] = =05 #  d[8~1] = =03) & reset'
|
| sb = ((chann2 & chann1 & sb & sa' & d[8~1] = =0)
|    # (chann2 & sb' & sa & d[8~1] = =0)
|    # (sb & temp')) & reset'
| sa = ((chann2 & chann1 & sa' & d[8~1] = =0)
|    # (chann2 & sb' & sa' & d[8~1] = =0)
|    # (chann1 & sb' & sa' & d[8~1] = =0)
|    # (sa & temp')) & reset'
```

Table B-8 The Program List of PAL chip PAL-ADC-#1 Design.

```
*************************************************************************************
* CHIP NAME    : PAL-A/D#1                                                          *
* FUNCTION     : A/D converter control circuit (1),  control "enable" signal, record states *
*************************************************************************************

|PAL16RP8  in: (start, sb, sa, reset),
|          out: (enable, q[7~1]),
|          clock: clk
|
| active-low: start, q1, reset
|
| enable = start
|        # ((sb' & sa' & q[7~1] = =0)' & reset')
|
| map:  q[7~1] -> q[7~1]
| {  n -> n-1,    n/=0 & reset'
|    n -> 88,     n = =0 & (sb # sa) & reset'
|    n -> 127,    (n = =0 & sb' & sa' & reset') # reset }
```

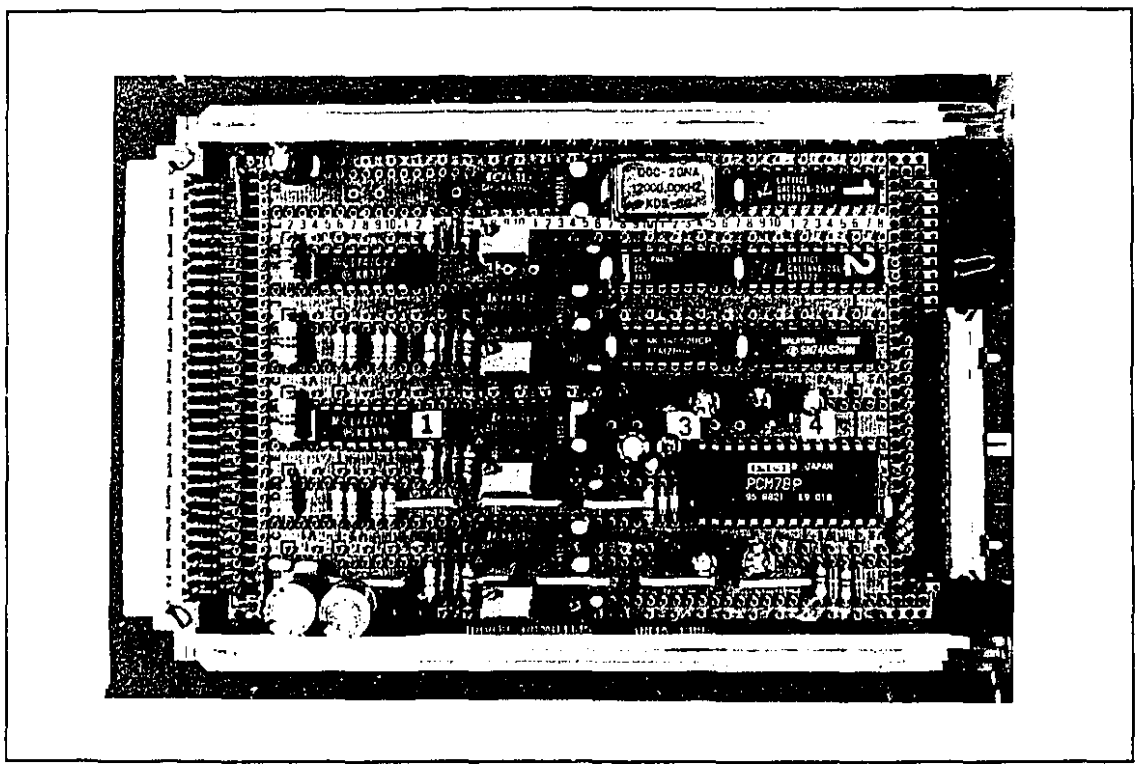


Figure B-6 The A/D converter circuit implementation using speedwire board.

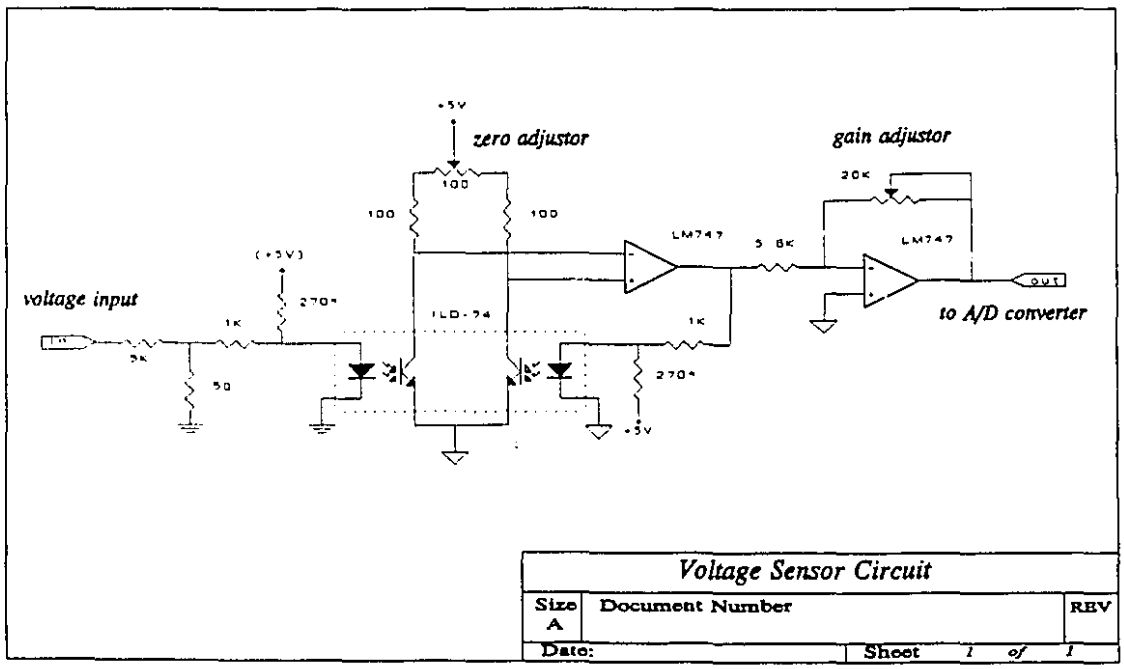


Figure B-7 The ac capacitor voltage sensor circuit.

APPENDIX
C

SOFTWARE DESIGN OF MULTI-DSP CONTROL

C.1 Introduction

The controls of the 6-valve, 3-phase, current-source PWM converter, using the Dynamic Tri-Logic SPWM and the Pole Placement control methods described in **Chapters 5** and **6**, have been implemented by a multi-DSP controller. The controller has been designed and constructed in our laboratory. A detailed description of the hardware design of the controller can be found in Refs. [94-96]. A brief descriptions of the software is given in here. The software is designed to be executed in parallel, in real-time.

C.2 Control Task Distribution

In the Pole-Placement feedback control design of Fig. 6-3 in **Chapter 6**, the computation tasks which implement the system feedback configuration of Fig. 6-4

are distributed as follows:

DSP #1: User interface through the serial communication with Personal Computer. It allows the user to change and display the control parameters and the converter status in real-time.

DSP #2: Sampling the dc link current $I_{dc}(t_k)$; calculating the 3-phase in-phase and in-quadrature reference waveforms $sin(t_k\text{-}\theta_j)$ and $cos(t_k\text{-}\theta_j)$ for $j=a$ and b; performing *phase lock loop* (PLL) control to synchronize the reference waveforms to the utility ac line voltages; calculating Eqs. (6.6) and (6.7) and the Bi-Logic SPWM timer settings for phases-a and b using the "four timer" method [93]; outputting the 3-phase Bi-Logic SPWM signals.

DSP #3: Sampling the ac line currents $i_{sj}(t_k)$ and the capacitor voltages $v_{cj}(t_k)$ for $j=a$ and b; getting $i_{so}(t_k)$ by doing the dc link current *P-I* regulation; calculating the steady-state waveform templates $i_{sjo}(t_k)$ and $v_{cjo}(t_k)$ for $j=a$ and b; calculating the SPWM timer setting for phase-c.

C.3 Program Flow Charts and Lists

Fig. C-1 shows the flow charts of three DSP's "main" programs, whose functions are to initialize the system and then control the flashing of the LEDs on the multi-DSP controller board to indicate the operating status of each DSP. In the experiments, the program of DSP #3 is started firstly, then DSP #2 and DSP #1. After the three DSPs have completed the initialization tasks, DSP #1 sends an interrupt signal to DSP #2 to start the parallel calculations. Then it jumps to

its system monitor program, which is stored in its EPROMs, to execute the interfacing function with the PC computer. Having received the interrupt signal from DSP #1, DSP #2 starts its on-chip timer to control the beginning instant of each sampling control period in the parallel calculations of three DSPs.

Once DSP #2 receives an interrupt signal from its on-chip timer, in the interrupt service subroutine "MTIMINT" it sends two interrupt signals to DSP #1 and DSP #3 respectively. Then the three DSPs start the sampling feedback control calculations in parallel. As shown in flow charts of Figs. C-2 and C-3, the interrupt service subroutines "MTIMINT" and "P3RP2IT" perform the main feedback control tasks. In order to keep the parallel calculations in-step, after finishing one stage of the calculation each DSP sends a "ready" signal to the synchronizing circuit on the controller board. When the synchronizing circuit has received three "ready" signals, it send a "all-ready" signal back to each of DSPs to allow them to continue the calculations in next stage.

Although the main task of DSP #1 is interfacing with the PC, it has to send out the "ready" signals to the synchronizing circuit in its interrupt service subroutine to keep the synchronizing circuit working properly. The flow chart of its interrupt service subroutine is not shown here.

The flow charts of the subroutines, which are used to initialize the A/D and D/A converters, to transmit the sampled data, to measure the ac voltage phase angle, etc., are not shown here. The reader can easily work out the details from the program lists shown in Tables C-1, C-2 and C-3.

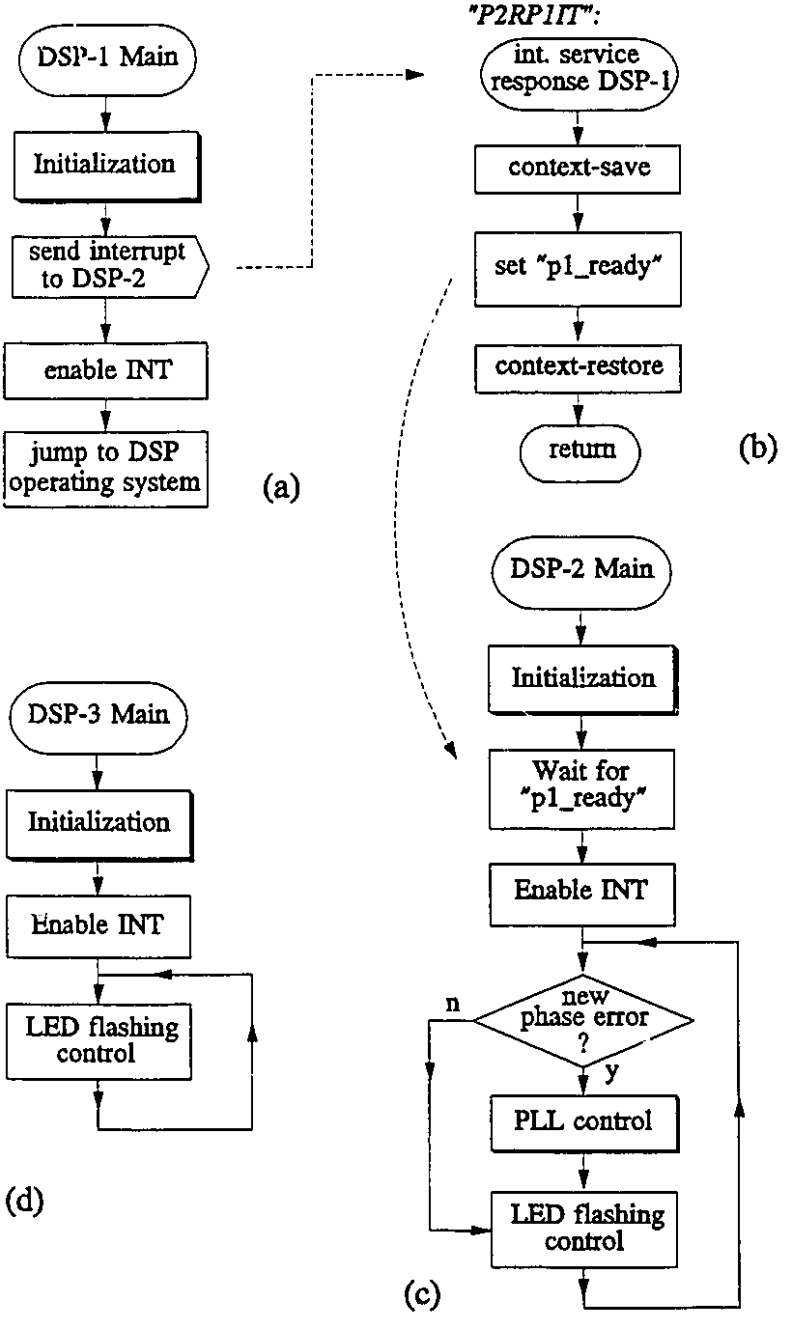


Figure C-1 Flow charts of DSP "main" programs. (a) DSP #1 The main program, (b) interrupt service subroutine "P1RP1IT" of DSP #2 , (c) DSP #2 main program, (d) DSP #3 main program.

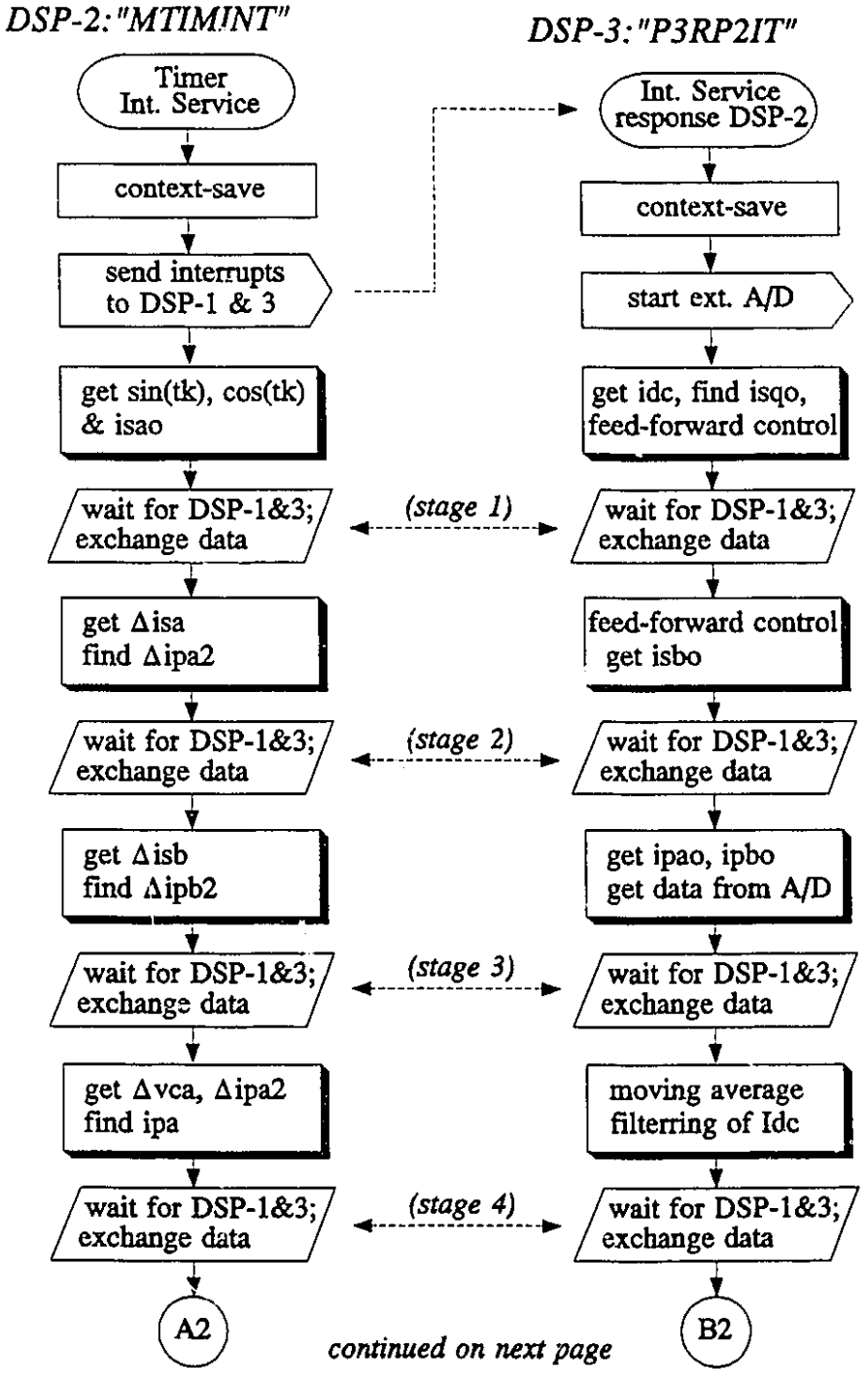


Figure C-2 The flow charts of interrupt service subroutines for parallel processing controls. (continued on Fig. C-3)

continued from last page

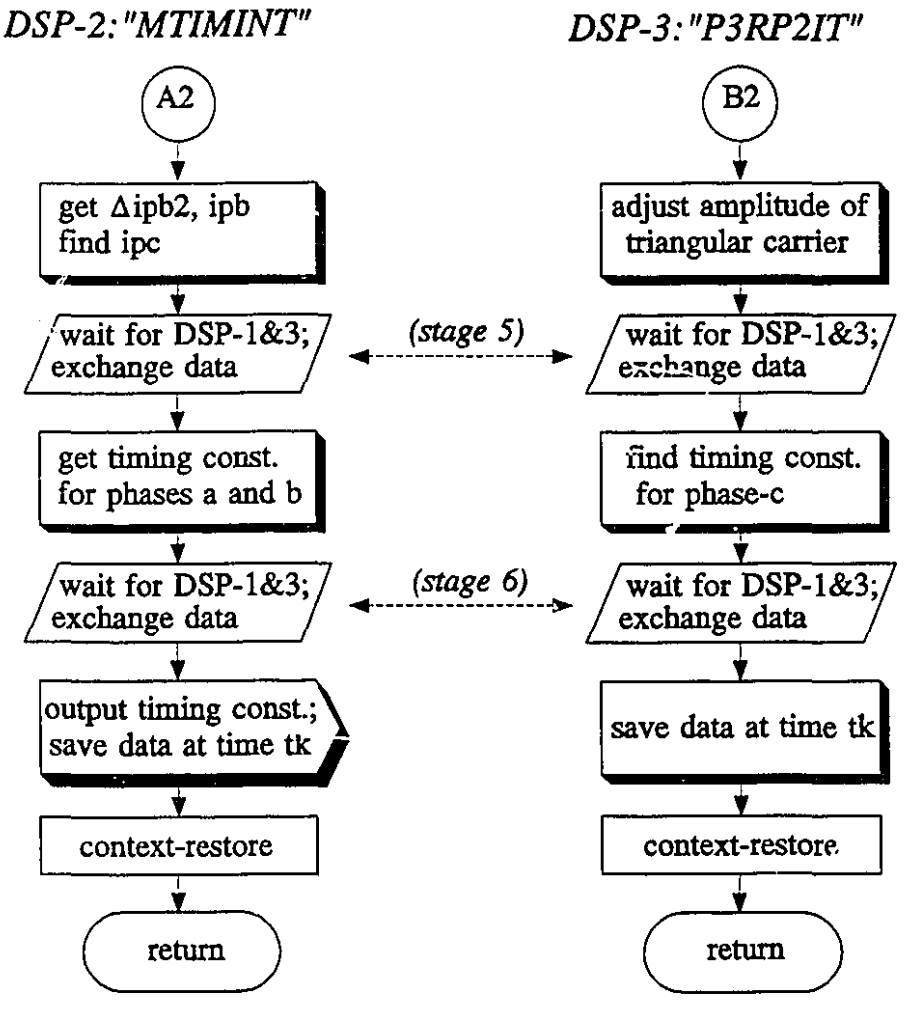


Figure C-3 The flow charts of interrupt service subroutines for parallel processing controls. (continued from Fig. C-2)

For more details about the compiling, linking, loading and executing procedures, please see the Refs. [99,100].

Table C-1 The List of DSP-2 Control Program.

```
*****************************************************************************
* Name     : DSP-2.ASM                                                      *
* Function : parallel processing with DSP-1.ASM and DSP-3.ASM.              *
*            start dsp1 and dsp3 at the beginning of each control period, measure Idc or Idcref
*            using the A/D on the DSP board.                                *
* Input    : interrupted by DSP #1 for starting parallel processing.        *
*            data from DSP #3 and PC passing through global memory.         *
* Output   : 3-phase Bi-Logic SPWM trigger signals to PAL circuit.          *
*            data required by DSP #3 to global memory.                      *
*****************************************************************************

        .title  'DSP2 PROGRAM'
                                        ; *- page 0 (00000h-0007Fh) -*
DRR     .equ    00000h
DXR     .equ    00001h
TIM     .equ    00002h
PRD     .equ    00003h
IMR     .equ    00004h
BCODE   .equ    00078h                  ; *- for initializing interrupt vectors -*
VINT0   .equ    0007Ah
VINT1   .equ    0007Bh
VINT2   .equ    0007Ch
VTINT   .equ    0007Dh
VRINT   .equ    0007Eh
VXINT   .equ    0007Fh
                                        ; *- page 4 (00200h-0027Fh) -*
SMARK   .equ    00200h                  ; control output
TRSIGN  .equ    00201h                  ; sign: triangle rising and falling
TRAMGN  .equ    00202h                  ; triangle carrier magnitude
FRQNC   .equ    00203h                  ; frequency reference
PHERR   .equ    00204h                  ; phase error in PLL at time kT
NEWPHE  .equ    00205h                  ; sign: new phase error is measured
KPSYNC  .equ    00206h                  ; proportional gain of PLL
DETFC   .equ    00207h                  ; frequency adjusting output
PRDBAK  .equ    00208h                  ; back-up of main timer constant
SCOUNT  .equ    00209H                  ; time-pointer: kT
INSIDE  .equ    0020Ah                  ; sign: time pointer has been increased
FCOUNT  .equ    0020Bh                  ; LED flashing time control
SWITCH  .equ    0020Ch                  ; control for closing inner loop
P1READY .equ    0020Dh                  ; sign: starting signal is sent from DSP-1
ADCIDC  .equ    0020Eh                  ; Idc(kT)
SIND    .equ    0020Fh                  ; sin(kT-dt)
COSD    .equ    00210H                  ; cos(kT-dt)
SIN120D .equ    00211h                  ; sin(kT-120-dt)
COS120D .equ    00212h                  ; cos(kT-120-dt)
SINA    .equ    00213h                  ; sin(kT+1.5dt)
COSA    .equ    00214h                  ; cos(kT+1.5dt)
SIN120A .equ    00215h                  ; sin(kT-120+1.5dt)
COS120A .equ    00216h                  ; cos(kT-120+1.5dt)
IACA_A  .equ    00217h                  ; Isa[(k-1)T]
IACB_B  .equ    00218h                  ; Isb[(k-1)T]
VCAPA_A .equ    00219h                  ; Vca[(k-1)T]
VCAPB_B .equ    0021Ah                  ; Vcb[(k-1)T]
AVGIACA .equ    0021Bh                  ; [isa[(k-1)T]+isa(kT)]/2
AVGIACB .equ    0021Ch                  ; [isb[(k-1)T]+isb(kT)]/2
AVGVCAPA .equ   0021Dh                  ; [Vca[(k-1)T]+Vca(kT)]/2
AVGVCAPB .equ   0021Eh                  ; [Vcb[(k-1)T]+Vcb(kT)]/2
IACAO   .equ    0021Fh                  ; isao(kT)
DETIACA .equ    00220h                  ; delta_isa(kT)
DETIACB .equ    00221h                  ; delta_isb(kT)
DETVCAPA .equ   00222h                  ; delta_Vca(kT)
DETVCAPB .equ   00223h                  ; delta_Vcb(kT)

ICTRLA  .equ    00224h                  ; va(kT)
ICTRLB  .equ    00225h                  ; vb(kT)
DETIPAI .equ    00226h                  ; ks_4*va
DETIPAP .equ    00227h                  ; ks_1*delta_Isa+ks_2*delta_Vca+ks_3*delta_Ua(k-1)
DETIPBI .equ    00228h                  ; ks_4*vb
DETIPBP .equ    00229h                  ; ks_1*delta_Isb+ks_2*delta_Vcb+ks_3*delta_Ub(k-1)
DETIPA  .equ    0022Ah                  ; Ua(kT)
DETIPB  .equ    0022Bh                  ; Ub(kT)
DETIPA_A .equ   0022Ch                  ; Ua[(k-1)T]
DETIPB_B .equ   0022Dh                  ; Ub[(k-1)T]
IPA     .equ    0022Eh                  ; isao+Ua
IPB     .equ    0022Fh                  ; isbo+Ub
IPC     .equ    00230h                  ; isco+Uc
IMPA    .equ    00231h                  ; Sma
IMPB    .equ    00232h                  ; Smb
IMPC    .equ    00233h                  ; Smc
CONSTA  .equ    00234h                  ; SPWM timing constant of phase a
CONSTB  .equ    00235h                  ; SPWM timing constant of phase b
CONSTC  .equ    00236h                  ; SPWM timing constant of phase c
KS_1    .equ    00237h                  ; state feedback gain K1
KS_2    .equ    00238h                  ; state feedback gain K2
KS_3    .equ    00239h                  ; state feedback gain K3
KS_4    .equ    0023Ah                  ; state feedback gain K4
SQR23   .equ    0023Bh                  ; constant
SYNCTT1 .equ    0023Ch                  ;
SYNCTT2 .equ    0023Dh                  ;
TEMP1   .equ    0023Eh                  ;
TEMP2   .equ    0023Fh                  ;
TEMP3   .equ    00240h                  ;
TEMP4   .equ    00241h                  ;
DADATA  .equ    00242h                  ; data for D/A output
DAOUT   .equ    00243h                  ; pointer of D/A output data
                                        ; *- global memory page #256, 08000h>) -*
GDATP3  .equ    08004h                  ; sign: display data in DSP-2 or DSP-3
GP2INDEX .equ   08005h                  ; index of DSP-2's data to be displayed
GP3INDEX .equ   08006h                  ; index of DSP-3's data to be displayed
GP3DA   .equ    08007h                  ; DSP-3's data to be displayed
                                        ; pc-controlled varibles
GKPIDC  .equ    08010h                  ; proportional gain of outer loop
GKIIDC  .equ    08011h                  ; integral gain of outer loop
GISTEP  .equ    08012h                  ; command for step change of Idcref
GSWITCH .equ    08014h                  ; command for closing inner loop
GIREF   .equ    08017h                  ; Idcref
                                        ; exchanged data: from DSP-3
GIACA   .equ    08018h
GIACB   .equ    08019h
GVCAPA  .equ    0801Ah
GVCAPB  .equ    0801Bh

GVSQO   .equ    08020h
GISQO   .equ    08021h
GIACAO  .equ    08022h
GIACBO  .equ    08023h
GVCAPAO .equ    08024h
GVCAPBO .equ    08025h
GIPAO   .equ    08026h
GIPBO   .equ    08027h
                                        ; exchanged date: to DSP-3
GSIND   .equ    08030h
GCOSD   .equ    08031h
GSIN120D .equ   08032h
GCOS120D .equ   08033h
GSINA   .equ    08034h
GCOSA   .equ    08035h
GSIN120A .equ   08036h
GCOS120A .equ   08037h
```

```
GADCIDC   .equ    08038h
GPRDBAK   .equ    08039h
GTRSIGN   .equ    0803Ah
GTRAMGN   .equ    0803Bh
GIMPC     .equ    0803Ch
GCONSTC   .equ    0803Dh
                                  ;*- constants -*
DEG30     .equ    00068h          ;DEG30 = 105
DEG60     .equ    000D2h          ;DEG60 = 210
DEG90     .equ    0013Bh          ;DEG90 = 315
DEG150    .equ    0020Dh          ;DEG150 = 525
TWOPI     .equ    004ECh          ;TWOPI = 1260
HALFDA    .equ    0000Fh          ;DA = 15
ONEHAFDA  .equ    00017h          ;1.5*DA
ICTRLMT   .equ    06800h          ;xxxx xxx.x xxxx xxxx
SINTABLE  .equ    00300h          ;pointer of sin-table
COEFF     .equ    05B48h          ;2*coeff (coefficient)
FCLIMT    .equ    09D00h          ;frequency limit

*****************************************************************************
*                          Initialization                                   *
*****************************************************************************

          .sect   "P2INITI"
START     DINT                    ;
          SSXM                    ;
          LDPK    00000h          ;point to date page 0
                                  ;*- initiallze interrupt vector -*
          LALK    P2RP1IT         ;interrupt vector for Int0
          SACL    VINT0           ;
          LALK    SYNCINT         ;interrupt vector for Int2.
          SACL    VINT2           ;
          LALK    MTIMINT         ;interrupt vector for on chip timer
          SACL    VTINT           ;
          LALK    ADININT         ;interrupt vector for A/D (serial port)
          SACL    VRINT           ;
          LALK    DAOUTIT         ;interrupt vector for D/A (serial port)
          SACL    VXINT           ;
          LALK    0FF80h          ;load "branch" operating code
          SACL    BCODE           ;
          LALK    03FF0h          ;point to vectors address set by EPROM
          TBLW    BCODE           ;load interrupt vectors
          ADDK    00001h          ;
          TBLW    VINT0           ;
          ADDK    00003h          ;
          TBLW    BCODE           ;
          ADDK    00001h          ;
          TBLW    VINT2           ;
          ADDK    00001h          ;
          TBLW    BCODE           ;
          ADDK    00001h          ;
          TBLW    VTINT           ;
          ADDK    00001h          ;
          TBLW    BCODE           ;
          ADDK    00001h          ;
          TBLW    VRINT           ;
          ADDK    00001h          ;
          TBLW    BCODE           ;
          ADDK    00001h          ;
          TBLW    VXINT           ;

          LACK    00001h          ;
          SACL    IMR             ;enable Int0 only
                                  ;
          LALK    00F7Fh          ;1/(60*42) = 3968x100ns
          SACL    PRD             ;start main timer
                                  ;*- initialize addressing register -*
          LRLK    AR0,00280h      ;AR0 is used for A/D initialization
          LRLK    AR1,002C0h      ;AR1 is used for SYNCINT stack
          LRLK    AR2,002E0h      ;AR2 is used for MTIMINT stack
          LRLK    AR3,00281h      ;AR3 is used for A/D initialization
          LRLK    AR4,00200h      ;
          LRLK    AR5,00300h      ;AR5 is used for DAOUTIT stack
          LRLK    AR6,00320h      ;AR6 is used for ADININT stack
          LRLK    AR7,00340h      ;AR7 is used for P2RP1IT stack
                                  ;*- clear registers -*
          LARP    00004h          ;using AR4
          LACK    00000h          ;clearing working area
          RPTK    255             ;
          SACL    *+              ;
          RPTK    255             ;
          SACL    *+              ;
                                  ;*- A/D Initialization -*
          LARP    00003h          ;using AR3 for load codes
          LALK    00000h          ;
          SACL    *+              ;
          LALK    0FFE3h          ;
          SACL    *+              ;
          LACK    00003h          ;
          SACL    *+              ;
          LALK    01E3Eh          ;
          SACL    *+              ;
          LACK    00003h          ;
          SACL    *+              ;
          LALK    00205h          ;
          SACL    *+              ;
          LACK    00003h          ;
          SACL    *+              ;
          LALK    02244h          ;
          SACL    *               ;load first D/A Initialization code
                                  ;
          LDPK    00004h          ;*- point to data page 4 -*
          LALK    0F207h          ;Initialize SMARK
          SACL    SMARK           ;
          OUT     SMARK,0Fh       ;turn on 3 LEDs  00000111(7-0)
          OUT     SMARK,08h       ;reset PWM timers  111100x0(15-8)
          OUT     SMARK,09h       ;switch A/D converter to channel 0
          ANDK    0AFFFFh         ;
          SACL    SMARK           ;prepared for starting PWM timers
                                  ;
          LACK    00001h          ;
          SACL    TRSIGN          ;initialize triangle edge sign
                                  ;
          LALK    05E3Fh          ;
          SACL    FRQNC           ;frequency reference = 60 Hz
                                  ;
          LALK    03800h          ;
          SACL    KPSYNC          ;set the gain of PLL
                                  ;
          LALK    00F7Fh          ;
          SACL    PRDBAK          ;backup PRD
                                  ;*- initialize state feedback gains -*
          LALK    06A1Bh          ;x.xxx xxxx xxxx xxxx
          SACL    KS_1            ;
          LALK    00641h          ;x.xxx xxxx xxxx xxxx
          SACL    KS_2            ;
          LALK    0319Bh          ;x.xxx xxxx xxxx xxxx
          SACL    KS_3            ;
          LALK    02BF1h          ;x.xxx xxxx xxxx xxxx
          SACL    KS_4            ;
                                  ;*- initialize coefficients -*
          LALK    07421h          ;
```

```
        SACL    SQR23           ; sqr23 = 65536x16368xsqrt(2)/14745/sqrt(3)
                                ; *- load PWM timing constants -*
        LALK    0330h           ;
        SACL    CONSTA          ;
        LALK    00202h          ;
        SACL    CONSTB          ;
        LALK    00F00h          ;
        SACL    CONSTC          ;
        LALK    00200h          ; set LED flashing time control counter
        SACL    FCOUNT          ;
                                ; *- initialize global memory -*
        LARP    00004h          ;
        LRLK    AR4,08000h      ; point to global memory
        LALK    00000h          ; clear working area in global memory
        RPTK    255             ;
        SACL    *+              ;
        RPTK    255             ;
        SACL    *+              ;
                                ;
        LRLK    AR4,GKPIDC      ;
        LALK    00300h          ; kpidc = xxxx x.xxx xxxx xxxx
        SACL    *+              ; gkpidc = kpidc
        LALK    00068h          ; klidc = xxx.x xxxx xxxx xxxx
        SACL    *               ; gkiidc = klidc
                                ;
        LRLK    AR4,GVSQC       ; *- set ac source voltage amplitude
        LALK    03C9Fh          ; 2*[sqrt(3)*70v] = xxxx xxxx xx.xx xxxx
        SACL    *               ;
                                ; *- set current reference -*
        LRLK    AR4,GIREF       ;
        LALK    02000h          ; idcref = xxxx xx.xx xxxx xxxx
        SACL    *               ;
                                ;
        LRLK    AR4,GPRDBAK     ;
        LAC     PRDBAK          ;
        SACL    *+              ; gprdbak = prdbak
        LAC     TRSIGN          ;
        SACL    *               ; gtrsign = trsign
                                ;
        EINT                    ; enable interrupt
                                ;
WAITP1  LAC     P1READY         ; wait for a starting sign
        BZ      WAITP1          ;
                                ;
        LACK    00020h          ;
        LDPK    00000h          ;
        SACL    IMR             ; enable xint only
                                ;
        LACK    00003h          ;
        SACL    DXR             ; start D/A initialization
                                ;
        LDPK    00004h          ;
        EINT                    ; enable interrupt
```

```
*                       Main Loop                                       *
* Function  : PLL regulation and LED flashing control                   *
* Input     : NEWPHE, PHERR                                             *
* Output    : FRQNC, PRD, PRDBAK, FCOUNT                                *
```

```
ADJFRQ  LAC     NEWPHE          ;
        BZ      FLASH           ;
                                ; *- new phase error has been tested -*
        DINT                    ; disenable interrupt
        LT      PHERR           ; load phase error to T register
        MPY     KPSYNC          ; gain*pherr
        SPM     00002h          ;
        SPH     DETFC           ;
                                ; *- output limit -*
        LAC     DETFC           ;
        BLZ     NEGFC           ; if detfc > 0 then
POSFC   SBLK    FCLIMT          ;   if |detfc| > fclimit then
        BLZ     ADDFO           ;     detfc = fclimit
        LALK    FCLIMT          ;
        SACL    DETFC           ;
        B       ADDFO           ;
NEGFC   ADLK    FCLIMT          ; elseif detfc < 0 then
        BGZ     ADDFO           ;   if |detfc| > fclimit then
        LALK    FCLIMT          ;     detfc = -fclimit
        NEG                     ;
        SACL    DETFC           ;
                                ;
ADDFO   LALK    05E3Fh          ; *- fc = 60Hz-detfc -*
        SUB     DETFC           ;
        SACL    FRQNC           ;
                                ;
        LALK    COEFF,0Fh       ; *- find 42x10/fc -*
        RPTK    12              ;
        SUBC    FRQNC           ;
        LDPK    00000h          ;
        SACL    PRD             ; load main timing data to PRD.
        LDPK    00004h          ;
        SACL    PRDBAK          ; backup PRD
                                ;
CLRSGN  LACK    00000h          ; clear NEWPHE sign
        SACL    NEWPHE          ;
        EINT                    ;
FLASH   LAC     FCOUNT          ; check flashing count
        BGZ     ADJEND          ;
        LAC     SMARK           ; if fcount = 0 then
        XORK    0003Fh          ;   change LEDs
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;
        LALK    00200h          ;   fcount = 200
        SACL    FCOUNT          ;
                                ;
ADJEND  B       ADJFRQ          ; do loop
```

```
* Subroutine  : MTIMINT response to the Main-timer interrupt call      *
* Function    : start DSP-3 and DSP-1 to do parallel calculation       *
*               sampling idc, state feedback control, get spwm timing data
* Output      : bi-logic spwm trigger signals                          *
* Call        : PWMRTN1                                                *
* Affect      : AR2 is used to save current registers                  *
*               AR4 is point to global memory.                         *
*               Temp1-8 are used.                                      *
```

```
        .sect   "MTIMINT"
                                ; *- save current registers -*
MTIMINT LARP    00022h          ; point to AR2
        ADRK    0C001h          ;
        SST1    *+              ;
        SST     *+              ;
        SACH    *+              ;
        SACL    *+              ;
        SPM     00000h          ;
        SPH     *+              ;
        SPL     *+              ;
        MPYK    00001h          ;
```

```
        SPL     *,4             ; point to AR4
;
FSTJOB  OUT     SMARK,0Eh       ; interrupt DSP-3
        OUT     SMARK,0Dh       ; interrupt DSP-1
;
        LDPK    00004h
PNEXT0  LAC     SCOUNT          *- kT = kT + dT -*
        ADDK    0001Eh
        SBLK    TWOPI
        BGEZ    NEXT0
        ADLK    TWOPI
NEXT0   SACL    SCOUNT
;
        LACK    00001h
        SACL    INSIDE          ; set INSIDE
;
        LAC     SMARK           *- set "busy" signal to sync. circuit -*
        ANDK    0FF7Fh
        SACL    SMARK
        OUT     SMARK,0Fh       ; reset bit7 of port F
;
        EINT
;
WWTT    LAC     SCOUNT          *- get phase angles -*
        SUBK    HALFDA
        BGEZ    NEXTWT0
        ADLK    TWOPI
NEXTWT0 SACL    SIND            ; save (kT-da)
        SUBK    DEG30
        BGEZ    NEXTWT1
        ADLK    TWOPI
NEXTWT1 SACL    COS120D         ; save (kT-120-da)+90
        SBLK    DEG90
        BGEZ    NEXTWT2
        ADLK    TWOPI
NEXTWT2 SACL    SIN120D         ; save (kT-120-da)
        SBLK    DEG150
        BGEZ    NEXTWT3
        ADLK    TWOPI
NEXTWT3 SACL    COSD            ; save (kT-da)+90
;
        LAC     SCOUNT
        ADDK    ONEHAFDA
        SBLK    TWOPI
        BGEZ    NEXTWT4
        ADLK    TWOPI
NEXTWT4 SACL    SINA            ; save (kT+1.5*da)
        SUBK    DEG30
        BGEZ    NEXTWT5
        ADLK    TWOPI
NEXTWT5 SACL    COS120A         ; save (kT-120+1.5*da)+90
        SBLK    DEG90
        BGEZ    NEXTWT6
        ADLK    TWOPI
NEXTWT6 SACL    SIN120A         ; save (kT-120+1.5*da)
        SBLK    DEG150
        BGEZ    NEXTWT7
        ADLK    TWOPI
NEXTWT7 SACL    COSA            ; save (kT+1.5*da)+90
                                *- look up sin(x) table -*
SINTAB  LAC     SIND
        ADLK    SINTABLE
        TBLR    SIND            ; get sin(wt-da)
        LAC     COSD
        ADLK    SINTABLE
        TBLR    COSD            ; get cos(wt-da)
;
        LAC     SIN120D
        ADLK    SINTABLE
        TBLR    SIN120D         ; get sin(wt-120-da)
        LAC     COS120D
        ADLK    SINTABLE
        TBLR    COS120D         ; get cos(wt-120-da)
        LAC     SINA
        ADLK    SINTABLE
        TBLR    SINA            ; get sin(wt+1.5da)
        LAC     COSA
        ADLK    SINTABLE
        TBLR    COSA            ; get cos(wt+1.5da)
        LAC     SIN120A
        ADLK    SINTABLE
        TBLR    SIN120A         ; get sin(wt-120+1.5da)
        LAC     COS120A
        ADLK    SINTABLE
        TBLR    COS120A         ; get cos(wt-120+1.5da)
;
SDATAD  LRLK    AR4,GSIND       *- transfer to global memory -*
        LAC     SIND
        SACL    *+
        LAC     COSD
        SACL    *+
        LAC     SIN120D
        SACL    *+
        LAC     COS120D
        SACL    *
                                *- get isao(kT) -*
FIACAO  LT      SQR23
        MPY     SIND
        LRLK    AR4,GISQO
        LTP     *
        SACH    SIND,1          ; xx.xx xxxx xxxx xxxx
        MPY     SIND
        LTP     KS_4            ; x.xxx xxxx xxxx xxxx
        NEG
        SACH    IACAO,4         ; xxxx x.xxx xxxx xxxx
                                *- set "ready" to sync. circuit -*
        RXF
        SXF                     ; clear BIO
        LAC     SMARK
        ORK     00080h
        SACL    SMARK
        OUT     SMARK,0Fh       ; set bit7 of port F for "ready"
WAIT_1  BIOZ    WAIT_1          *- wait for "all-ready" from sync. circuit -*
        LAC     SMARK
        ANDK    0FF7Fh
        SACL    SMARK
        OUT     SMARK,0Fh       ; reset bit7 of port F
;
FAVGIACA LRLK   AR4,GIACA       ; AR4 point to GIACA
        LAC     IACA_A,15
        ADD     *,15
        SACH    AVGIACA         ; avgiaca = (iaca + iaca_a)/2
        LAC     *
        SACL    IACA_A          ; iaca_a = iaca
;
FDETIACA LAC    AVGIACA,15      *- get delta-isa -*
        SUB     IACAO,15
        SACH    DETIACA         ; xxxx xx.xx xxxx xxxx
;
FICTRLA LAC     ICTRLA,15       ; yyyy yyyy.yyyy yyyy(31-16)
        SUB     DETIACA,14
        SACH    ICTRLA,1        ; xxxx xxx.x xxxx xxxx
```

```
LMT1     LAC     ICTRLA      ;*- output limit -*
         BLZ     CHKLOW1     ;
CHKUP1   SBLK    ICTRLMT     ;
         BLEZ    FDETIPAI    ;
         LALK    ICTRLMT     ;
         SACL    ICTRLA      ;
         B       FDETIPAI    ;
CHKLOW1  ADLK    ICTRLMT     ;
         BGEZ    FDETIPAI    ;
         LALK    ICTRLMT     ;
         NEG                 ;
         SACL    ICTRLA      ;

FDETIPAI MPY     ICTRLA      ;ictrla*ks_4
         LTP     KS_1        ;
         SACH    DETIPAI,2   ;xxxx xx.xx xxxx xxxx

FDETIPAP MPY     DETIACA     ;detiaca*ks_1
         LTP     KS_3        ;
         MPY     DETIPA_A    ;detipa_a*ks_3
         LTS     KS_4        ;
         SACL    TEMP1       ;
         SACH    TEMP2       ;yyyy yyy.y yyyy yyyy

         LRLK    AR4,GSWITCH ;
         LAC     *           ;
         SACL    SWITCH      ;load switch

SDATAA   LRLK    AR4,GSINA   ;transfer data to DSP-3
         LAC     SINA        ;
         SACL    *+          ;
         LAC     COSA        ;
         SACL    *+          ;
         LAC     SIN120A     ;
         SACL    *+          ;
         LAC     COS120A     ;
         SACL    *           ;

         RXF                 ;
         SXF                 ;
         LAC     SMARK       ;
         ORK     00080h      ;
         SACL    SMARK       ;
         OUT     SMARK,0Fh   ;
WAIT_2   BIOZ    WAIT_2      ;
         LAC     SMARK       ;
         ANDK    0FF7Fh      ;
         SACL    SMARK       ;
         OUT     SMARK,0Fh   ;

FAVGIACB LRLK    AR4,GIACB   ;
         LAC     IACB_B,15   ;
         ADD     *,15        ;
         SACH    AVGIACB     ;avgiacb = (iacb + iacb_b)/2
         LAC     *           ;
         SACL    IACB_B      ;iacb_b = iacb

FDETIACB LAC     AVGIACB,15  ;
         LRLK    AR4,GIACBO  ;
         SUB     *,15        ;
         SACH    DETIACB     ;xxxx xx.xx xxxx xxxx

FICTRLB  LAC     ICTRLB,15   ;yyyy yyyy.yyyy yyyy
         SUB     DETIACB,14  ;
         SACH    ICTRLB,1    ;xxxx xxx.x xxxx xxxx
```

```
LMT2     LAC     ICTRLB      ;
         BLZ     CHKLOW2     ;
CHKUP2   SBLK    ICTRLMT     ;
         BLEZ    FDETIPBI    ;
         LALK    ICTRLMT     ;
         SACL    ICTRLB      ;
         B       FDETIPBI    ;
CHKLOW2  ADLK    ICTRLMT     ;
         BGEZ    FDETIPBI    ;
         LALK    ICTRLMT     ;
         NEG                 ;
         SACL    ICTRLB      ;

FDETIPBI MPY     ICTRLB      ;
         LTP     KS_1        ;
         SACH    DETIPBI,2   ;xxxx xx.xx xxxx xxxx

FDETIPBP MPY     DETIACB     ;
         LTP     KS_3        ;
         MPY     DETIPB_B    ;
         LTS     KS_2        ;
         SACL    TEMP3       ;
         SACH    TEMP4       ;

         RXF                 ;
         SXF                 ;
         LAC     SMARK       ;
         ORK     00080h      ;
         SACL    SMARK       ;
         OUT     SMARK,0Fh   ;
WAIT_3   BIOZ    WAIT_3      ;
         LAC     SMARK       ;
         ANDK    0FF7Fh      ;
         SACL    SMARK       ;
         OUT     SMARK,0Fh   ;

FAVGVA   LRLK    AR4,GVCAPA  ;AR4 point back to gvcapa
         LAC     VCAPA_A,15  ;
         ADD     *,15        ;
         SACH    AVGVCAPA    ;avgvcapa = (vcapa + vcapa_a)/2
         LAC     *           ;
         SACL    VCAPA_A     ;vcapa_a = vcapa

FDETVA   LAC     AVGVCAPA    ;
         LRLK    AR4,GVCAPAO ;
         SUB     *           ;
         SACL    DETVCAPA    ;xxxx xxxx xx.xx xxxx

FDETIPA2 ZALS    TEMP1       ;
         ADDH    TEMP2       ;
         MPY     DETVCAPA    ;
         SPM     00002h      ;
         APAC                ;using add since ks_2<0
         SPM     00000h      ;
         SACH    DETIPAP,1   ;xxxx xx.xx xxxx xxxx

FIPA     LRLK    AR4,GIPAO   ;
         LAC     *           ;
         SACL    IPA         ;load ipa

         LACK    00000h      ;
         SACL    DETIPA      ;initialize detipa

TSIA     LAC     SWITCH      ;*- test integral control switch -*
         ANDK    0FF00h      ;
         BZ      TSPA        ;
```

```
ADDIPAI  LAC    DETIPA      *- adding integral control in -*
         ADD    DETIPAI
         SACL   DETIPA

TSPA     LAC    SWITCH      *- test proportional control switch -*
         ANDK   000FFh
         BZ     TOTIPA

ADDIPAP  LAC    DETIPA      *- adding proportional control in -*
         ADD    DETIPAP
         SACL   DETIPA

TOTIPA   LAC    IPA         *- get output of ipa -*
         ADD    DETIPA
         SACL   IPA

         RXF
         SXF
         LAC    SMARK
         ORK    00080h
         SACL   SMARK
         OUT    SMARK,0Fh
WAIT_4   BIOZ   WAIT_4
         LAC    SMARK
         ANDK   0FF7Fh
         SACL   SMARK
         OUT    SMARK,0Fh

FAVGVB   LRLK   AR4,GVCAPB  AR4 point back to GVCAPB
         LAC    VCAPB_B,15
         ADD    *,15
         SACH   AVGVCAPB    avgvcapb=(vcapb+vcapb_b)/2
         LAC    *
         SACL   VCAPB_B     vcapb_b=vcapb

FDETVB   LAC    AVGVCAPB    *- get detvcapb -*
         LRLK   AR4,GVCAPBO
         SUB    *
         SACL   DETVCAPB

FDETIPB2 ZALS   TEMP3
         ADDH   TEMP4
         MPY    DETVCAPB
         SPM    00002h
         APAC               using add since KS_2<0
         SPM    00000h
         SACH   DETIPBP,1

FIPB     LRLK   AR4,GIPBO
         LAC    *
         SACL   IPB         load ipb

         LACK   00000h
         SACL   DETIPB      initialize detipb

TSIB     LAC    SWITCH      *- test integral cotrol switch -*
         ANDK   0FF00h
         BZ     TSPB

ADDIPBI  LAC    DETIPB      *- adding integral control in -*
         ADD    DETIPBI
         SACL   DETIPB

TSPB     LAC    SWITCH      *- test proportional control switch -*
         ANDK   000FFh
         BZ     TOTIPB

ADDIPBP  LAC    DETIPB      *- adding proportional control in -*
         ADD    DETIPBP
         SACL   DETIPB

TOTIPB   LAC    IPB
         ADD    DETIPB
         SACL   IPB         *- get output of ipb -*

FIPM     LAC    IPA
         ADD    IPB
         NEG
         SACL   IPC         ipc=-ipa-ipb
                            *- decoupling processing -*
         SUB    IPB
         SACL   IMPC        impc=ipc-ipb

         LRLK   AR4,GIMPC
         SACL   *           send impc to global memory

         RXF
         SXF
         LAC    SMARK
         ORK    00080h
         SACL   SMARK
         OUT    SMARK,0Fh
WAIT_5   BIOZ   WAIT_5
         LAC    SMARK
         ANDK   0FF7Fh
         SACL   SMARK
         OUT    SMARK,0Fh

         LAC    IPB
         SUB    IPA
         SACL   IMPB        impb=ipb-ipa
         LAC    IPA
         SUB    IPC
         SACL   IMPA        impa=ipa-ipc
                            *- calculating spwm timing data -*
FDATA    LRLK   AR4,GTRAMGN
         LAC    *
         SACL   TRAMGN      load triangle magnitude
         LT     PRDBAK      load period variable
                            *- find timing constant for phase A -*
FDATAA   LAC    IMPA
         SACL   TEMP1       using temp1 to transfer data impa to 'subrtn1'
         CALL   SUBRTN1
         SACL   CONSTA      save timing data of timer A
                            *- find timing constant for phase B -*
FDATAB   LAC    IMPB
         SACL   TEMP1
         CALL   SUBRTN1
         SACL   CONSTB      save timing data of timer B.
                            *- wait for data of timer C -*
         RXF
         SXF
         LAC    SMARK
         ORK    00080h
         SACL   SMARK
         OUT    SMARK,0Fh
WAIT_6   BIOZ   WAIT_6
         LAC    SMARK
         ANDK   0FF7Fh
         SACL   SMARK
         OUT    SMARK,0Fh
```

```
        LRLK    AR4,GCONSTC     ;*- get timing constant of phase C from DSP-3 -*
        LAC     *               ;
        SACL    CONSTC          ;
                                ;*- output timing constants to PWM timer -*
LASTP   DINT                    ;disenable all interrupts
OUTTIM  OUT     CONSTA,0Ah      ;
        OUT     CONSTB,0Bh      ;
        OUT     CONSTC,0Ch      ;
        OUT     SMARK,08h       ;start the PWM timers,
        LAC     SMARK           ;and set/reset trigger register.
        ORK     0F000h          ;
        SACL    SMARK           ;
        OUT     SMARK,08h       ;release the trigger register.
                                ;*- preparing for next period calculations -*
        LAC     DETIPA          ;
        SACL    DETIPA_A        ;
        LAC     DETIPB          ;
        SACL    DETIPB_B        ;
        LRLK    AR4,GPRDBAK     ;AR4 point to global memory
        LAC     PRDBAK          ;
        SACL    *+              ;send prdbak to global memory
        LAC     TRSIGN          ;change the triangle edge sign.
        XORK    00001h          ;
        SACL    TRSIGN          ;
        SACL    *               ;send trsign to global memory
        BNZ     JUMP1           ;if present one is rising edge, then
        LAC     SMARK           ;  prepare for outputting falling edge
        ANDK    097FFh          ;
        SACL    SMARK           ;  (ready for Q=1\0)
        B       JUMP2           ;
JUMP1   LAC     SMARK           ;else prepare for outputting rising edge
        ANDK    0AFFFh          ;
        ORK     00800h          ;
        SACL    SMARK           ;  (ready for Q=0/1)
JUMP2   LAC     FCOUNT          ;fcount=fcount-1
        SUBK    00001h          ;
        SACL    FCOUNT          ;
                                ;*- output data to D/A, for debugging only -*
        LRLK    AR4,GDATP3      ;testing which DSP's data will be displayed
        LAC     *               ;
        BNZ     DATP3           ;
                                ;*- display DSP-2's data -*
DATP2   LRLK    AR4,GP2INDEX    ;point to index
        LALK    00200h          ;load beginning address of varibles
        ADD     *               ;
        SACL    DAOUT           ;save address
        LAR     AR4,DAOUT       ;
        LAC     *               ;load data to be displayed to
        SACL    DADATA          ;working register of D/A
        B       RECOVW          ;
                                ;*- display DSP-3's data -*
DATP3   LRLK    AR4,GP3DA       ;
        LAC     *               ;load data to be displayed from DSP-3
        SACL    DADATA          ;to working register of D/A
RECOVW  LACK    00000h          ;clear sign of inside
        SACL    INSIDE          ;
                                ;*- recover previous registers -*
        SPM     00000h          ;
        LARP    00002h          ;point to AR2
        MAR     *-              ;
        LT      *+              ;
        MPYK    00001h          ;
        LT      *-              ;
        MAR     *-              ;
        LPH     *-              ;
        ZALS    *-              ;
        ADDH    *-              ;
        LST     *-              ;
        LST1    *-              ;
        EINT                    ;
        RET                     ;

*****************************************************************
* Subroutine  : SUBRTN1 called by MTIMINT                       *
* Function    : calculate the timing constant using 'four timer method'.  *
* Input       : mudulating signal (vm) in 'temp1', period length in T register  *
* Output      : timing constant in ACC                          *
*****************************************************************

SUBRTN1 BLZ     NEGSGN          ;
        LACK    00000h          ;if vm>0 then
        SACL    TEMP2           ;  set TEMP2=0
        B       FRACT           ;
NEGSGN  ABS                     ;if vm<0 then
        SACL    TEMP1           ;  vm=|vm|, set TEMP2=1
        LACK    00001h          ;
        SACL    TEMP2           ;
FRACT   LAC     TEMP1           ;
        SUB     TRAMGN          ;
        BLZ     DIVID           ;
NFRACT  LAC     TRSIGN          ;if |vm|>tramgn then
        BZ      SIGN0           ;  if trsign=rising then
SIGN1   LAC     TEMP2           ;    if vm<0 then
        BZ      PRDMAX          ;
PRDMIN  LACK    00008h          ;      data=prdmin
        B       CORRECT         ;
PRDMAX  LAC     PRDBAK          ;    else data=prdmax
        B       CORRECT         ;
SIGN0   LAC     TEMP2           ;  elseif vm<0 then
        BZ      PRDMIN          ;      data=prdmin
        B       PRDMAX          ;  else data=prdmax
DIVID   ZALH    TEMP1           ;
        RPTK    10              ;
        SUBC    TRAMGN          ;
        SACL    TEMP1           ;quot=xxxx x.xxx xxxx xxxx
        LAC     TEMP2           ;
        BZ      ADDTRA          ;
        ZAC                     ;if vm<0 then
        SUB     TEMP1           ;  quot=-quot
        SACL    TEMP1           ;
ADDTRA  LAC     TRSIGN          ;fetch triangle edge sign
        BZ      MINUS           ;
        LALK    00800h          ;if trsign=rising then
        ADD     TEMP1           ;  acc=1+quot
        B       MPRDO2          ;
MINUS   LALK    00800h          ;else acc=1-quot
        SUB     TEMP1           ;
MPRDO2  SACL    TEMP1           ;save (1 +/- vm/tramgn)
        MPY     TEMP1           ;PRD*(1 +/- vm/tramgn)/2
        SPM     00002h          ;
        SPH     TEMP1           ;
        LAC     TEMP1           ;
CORRECT ADLK    00100h          ;add offset, since hardware design
        RET                     ;acc=timing constant
```

```
*****************************************************************************
* Subroutine    : SYNCINT response to INT2, the synchronizing interrupt call *
* Function      : measure phase error between ac source and sin-table pointer.*
* Affect        : SYNCTT1 and SYNCTT2 are used                                *
*****************************************************************************

        .sect   "SYNCINT"
                                        ; *- save current registers -*
SYNCINT LARP    00001h                  ; point AR1
        ADRK    00001h                  ;
        SST1    *+                      ;
        SST     *+                      ;
        SACH    *+                      ;
        SACL    *+                      ;
        SPM     00000h                  ;
        SPH     *+                      ;
        SPL     *+                      ;
        MPYK    00001h                  ;
        SPL     *                       ;
                                        ;
RESPON  LDPK    00000h                  ;
        LAC     TIM                     ; sampling TIM
        LDPK    00004h                  ;
        SACL    SYNCTT1                 ; save TIM to synctt1
        LAC     INSIDE                  ; if sampling after main timer interrupt
        BNZ     ADD00                   ;    then do not modify PHERR
        LAC     PRDBAK                  ; elseif PRD-TIM-20h>0, then
        SUB     SYNCTT1                 ;       do not modify PHERR
        SUBK    00020h                  ;
        BGEZ    ADD00                   ;
ADD30   LACK    0005Ah                  ; else do modify to PHERR
        SACL    SYNCTT2                 ;
        B       NORMAL                  ;
ADD00   LACK    00C3Ch                  ;
        SACL    SYNCTT2                 ;
NORMAL  LT      SYNCTT1                 ; load TIM to T
        MPYK    0001Eh                  ; TIM*30/PRD
        PAC                             ;
        RPTK    15                      ;
        SUBC    PRDBAK                  ;
        ANDK    0FFFFh                  ;
        NEG                             ;
        ADD     SYNCTT2                 ;
        ADD     SCOUNT                  ;
        SBLK    630                     ; normalize PHERR with pi/2
        BLZ     PLUS                    ;
        SBLK    630                     ;
        B       STORE                   ;
PLUS    ADLK    630                     ;
STORE   SACL    PHERR                   ; save phase error
        LACK    00001                   ; set new phase error sign
        SACL    NEWPHE                  ;
                                        ;
RECOVS  MAR     *-                      ; *- recover previous registers -*
        LT      *+                      ;
        MPYK    0C001h                  ;
        LT      *-                      ;
        MAR     *-                      ;
        LPH     *-                      ;
        ZALS    *-                      ;
        ADDH    *-                      ;
        LST     *-                      ;
        LST1    *-                      ;
        EINT                            ; enable interrupt
        RET                             ;
```

```
*****************************************************************************
* Subroutine    : DAOUTIT response to XINT, D/A DRX empty interrupt call      *
* Function      : Initializing A/D converter by sending data to DRX in the following sequence:
*                 02244h 00003h 00205h 00003h 01E3Eh 00003h 000E3h 00003h 00000h
*                   ^                                                   ^     *
*                  AR3                                                AR0=00280h
*****************************************************************************

        .sect   "DAOUTIT"
                                        ; *- save current registers -*
DAOUTIT LARP    00005h                  ; point to AR5
        ADRK    00001h                  ;
        SST1    *+                      ;
        SST     *+                      ;
        SACH    *+                      ;
        SACL    *                       ;
                                        ;
BBINITI LARP    00003h                  ; point to AR3
        LAC     *-                      ; (AR3)->DRX and AR3=AR3-1
        LDPK    00000h                  ;
        SACL    DXR                     ;
        CMPR    02h                     ; if AR3=AR0 then finish
        BBNZ    RECOVD                  ;
                                        ; *- to use D/A for debugging -*
        LALK    DA2OUT                  ; change interrupt vector for
        SACL    VXINT                   ; D/A output subroutine
        LALK    03FFBh                  ;
        TBLW    VXINT                   ;
                                        ;
FINISH  LACK    0003Ch                  ;
        SACL    IMR                     ; set enable for RINT TINT INT2
                                        ; *- recover previous registers -*
RECOVD  LARP    00005h                  ; point back to AR5
        ZALS    *-                      ;
        ADDH    *-                      ;
        LST     *-                      ;
        LST1    *-                      ;
        EINT                            ; enable interrupt
        RET                             ;
```

```
*****************************************************************************
* Subroutine    : DAOUT2 response to XINT, D/A DRX empty interrupt call       *
* Function      : after initialization of A/D, to send data to the DXR for debugging
* Input         : DADATA variable to be displayed                             *
*****************************************************************************

                                        ; *- save current registers -*
DA2OUT  LARP    00005h                  ; point to AR5
        ADRK    00001h                  ;
        SST1    *+                      ;
        SST     *+                      ;
        SACH    *+                      ;
        SACL    *                       ;
                                        ;
SENDDATA LAC    DADATA                  ; load dadata
        ANDK    0FFFCh                  ;
        LDPK    00000h                  ;
        SACL    DXR                     ; send data to DXR
                                        ; *- recover previous registers -*
RECOVDA LARP    00005h                  ;
        ZALS    *-                      ;
        ADDH    *-                      ;
        LST     *-                      ;
        LST1    *-                      ;
        EINT                            ;
        RET                             ;
```

```
*****************************************************************************
* Subroutine    : ADININ response to RINT, DRR full interrupt call.         *
* Function      : sample the Idc.                                           *
* Output        : ADCIDC and GADCIDC                                        *
*****************************************************************************

            .sect   "ADININT"
                                    ; *- save current registers -*
ADININT     LARP    00006h          ; point to AR6
            ADRK    00001h          ;
            SST1    *+              ;
            SST     *+              ;
            SACH    *+              ;
            SACL    *,0,7           ; point to AR7
                                    ; (Idc is connected to channel 1 of A/D)
LCH1        LDPK    00000h          ;
            LAC     DRR             ; load Idc
            LDPK    00004h          ;
            NEG                     ; considering there is a inverter circuit in A/D
            SACL    ADCIDC          ; send data to ADCIDC
            LRLK    AR7,GADCIDC     ; send to global memory
            SACL    *,0,6           ; point back to AR6
                                    ; *- recover previous registers -*
RECOVA      ZALS    *-              ;
            ADDH    *-              ;
            LST     *-              ;
            LST1    *-              ;
            EINT                    ; ***- enable interrupt -***
            RET                     ;

*****************************************************************************
* Subroutine    : P2RP1IT response to DSP-1 interrupt call from int0        *
* Function      : set the sign to ask DSP-2 to start the parallel processing.*
*****************************************************************************

            .sect   "P2RP1IT"
                                    ; *- save current registers -*
P2RP1IT     LARP    00007h          ; point to AR7
            ADRK    00001h          ;
            SST1    *+              ;
            SST     *+              ;
            SACH    *+              ;
            SACL    *               ;
                                    ;
            LACK    00001h          ;
            SACL    P1READY         ; set sign of P1READY
                                    ; *- recover previous registers -*
RECOVP      ZALS    *-              ;
            ADDH    *-              ;
            LST     *-              ;
            LST1    *-              ;
            RET                     ;
                                    ;
            .end                    ; *** enf of file ***
```

Table C-2 The List of DSP-3 Control Program.

```
*****************************************************************************
*Name       : DSP-3.ASM                                                     *
*Function   : Parallel processing with DSP-2.ASM and DSP-1.ASM              *
*            measure isa, Isb, vcapa and vcapb using the A/D in PAL circuits tox
*Input      : Interrupted by DSP #2 to start each sampling control calculation
*Output     : transfer inter-medium results and timing constant of phase-C to DSP #2
*****************************************************************************

            .title  "DSP-3 Program"
                                    ; *- page 0 (00000h-0007F) -*
DRR         .equ    00000h          ; (see dsp-2.asm)
DXR         .equ    00001h
TIM         .equ    00002h
PRD         .equ    00003h
IMR         .equ    00004h
BCODE       .equ    00079h
VINT0       .equ    0007Ah
VINT1       .equ    0007Bh
VINT2       .equ    0007Ch
VTINT       .equ    0007Dh
VRINT       .equ    0007Eh
VXINT       .equ    0007Fh
                                    ; *- page 4 (00200h-0027Fh) -*
SMARK       .equ    00200h
FCOUNT      .equ    00201h
ADINNO      .equ    00202h
ADINDAT1    .equ    00203h
ADINDAT2    .equ    00204h
ADINDAT3    .equ    00205h
ADINDAT4    .equ    00206h
IDCERR      .equ    00207h
INTERR      .equ    00208h
SIND        .equ    00209h
COSD        .equ    0020Ah
SIN120D     .equ    0020Bh
COS120D     .equ    0020Ch
SINA        .equ    0020Dh
COSA        .equ    0020Eh
SIN120A     .equ    0020Fh
COS120A     .equ    00210h
SQR23       .equ    00211h          ;
ISQO        .equ    00212h          ; Isqo(k) = xxxx xxx.x xxxx xxxx
IACBO       .equ    00213h          ; Iacbo(k) = xxxx x.xxx xxxx xxxx
VCDO        .equ    00214h          ; vcdo(k) = xxxx xxxx xx.xx xxxx
VCQO        .equ    00215h          ; vcqo(k) = xxxx xxxx xx.xx xxxx
VCAPAO      .equ    00216h          ; vcapao(k) = xxxx xxxx xx.xx xxxx
VCAPBO      .equ    00217h          ; vcapbo(k) = xxxx xxxx xx.xx xxxx
IPDO        .equ    00218h          ; Ipdo(k) = xxxx xx.xx xxxx xxxx
IPQO        .equ    00219h          ; Ipqo(k) = xxxx xx.xx xxxx xxxx
IPAO        .equ    0021Ah          ; Ipao(k) = xxxx xx.xx xxxx xxxx
IPBO        .equ    0021Bh          ; Ipbo(k) = xxxx xx.xx xxxx xxxx
ADCIDC      .equ    0021Ch          ; dc link current xxxx xx.xx xxxx xxxx
IDCREF      .equ    0021Dh          ; Idc reference xxxx xx.xx xxxx xxxx
INV42       .equ    00220h          ; save data of '1/42'
TRAMGN      .equ    00221h          ; trangle magnitude xxxx xx.xx xxxx xxxx
PRDBAK      .equ    00222h
TRSIGN      .equ    00223h
HIG1_1122   .equ    00224h          ; feedforward control parameters
HIG1_1221   .equ    00225h          ;
KIF1_1221   .equ    00226h          ;
TEMP1       .equ    00227h
TEMP2       .equ    00228h
```

```
TEMP3     .equ    00229h
TEMP4     .equ    0022Ah
DAOUT     .equ    0022Bh      ; saving data to be displayed
AVG2IDC   .equ    0022Eh      ; switching harmonic filter output of Idc
SUMIDCL   .equ    0022Fh      ;
SUMIDCH   .equ    00230h      ; 42 points sum of Idc
MAVGIDC   .equ    00231h      ; moving average filter output of Idc
SUMIAL    .equ    00232h      ;
SUMIAH    .equ    00233h      ; 42 points sum of Isa
AVGIA     .equ    00234h      ; moving average filter output of Isa
SUMIBL    .equ    00235h      ;
SUMIBH    .equ    00236h      ; 42 points sum of Isb
AVGIB     .equ    00237h      ; moving average filter output of Isb
SUMVCAL   .equ    00238h      ;
SUMVCAH   .equ    00239h      ; 42 points sum of vcapa
AVGVCA    .equ    0023Ah      ; moving average filter output of vcapa
SUMVCBL   .equ    0023Bh      ;
SUMVCBH   .equ    0023Ch      ; 42 points sum of vcapb
AVGVCB    .equ    0023Dh      ; moving average filter output of vcapb
SWAVG     .equ    0023Eh      ; sign: removing offset in sensor
                              ;
MIDC_1    .equ    002D6h      ; 42 points Idc
MIDC_42   .equ    002FFh      ;
IACA_1    .equ    00300h      ; 42 points Isa
IACA_42   .equ    00329h      ;
IACB_1    .equ    0032Ah      ; 42 points Isb
IACB_42   .equ    00353h      ;
VCA_1     .equ    00354h      ; 42 points vcapa
VCA_42    .equ    0037Dh      ;
VCB_1     .equ    0037Eh      ; 42 points vcapb
VCB_42    .equ    003A7h      ;
                              ; *- global  memory (page No.256, >08000h) -*
GDATP3    .equ    08004h
GP2INDEX  .equ    08005h
GP3INDEX  .equ    08006h
GP3DA     .equ    08007h

GKPIDC    .equ    08010h      ; p.i-controlled variables
GKIIDC    .equ    08011h
GISTEP    .equ    08012h
GSWITCH   .equ    08014h

GIREF     .equ    08017h

GIACA     .equ    08018h      ; exchanged data: to DSP-2
GIACB     .equ    08019h
GVCAPA    .equ    0801Ah
GVCAPB    .equ    0801Bh

GVSOO     .equ    08020h
GISOO     .equ    08021h
GIACAO    .equ    08022h
GIACBO    .equ    08023h
GVCAPAO   .equ    08024h
GVCAPBO   .equ    08025h
GIPAO     .equ    08026h
GIPBO     .equ    08027h

GSIND     .equ    08030h      ; exchanged data: from DSP-2
GCOSD     .equ    08031h
GSIN120D  .equ    08032h
GCOS120D  .equ    08033h
GSINA     .equ    08034h
GCOSA     .equ    08035h
GSIN120A  .equ    08036h
GCOS120A  .equ    08037h

GADCIDC   .equ    08038h
GPRDBAK   .equ    08039h
GTRSIGN   .equ    0803Ah
GTRAMGN   .equ    0803Bh
GIMPC     .equ    0803Ch
GCONSTC   .equ    0803Dh
                              ; *- constants -*
IDCINLMT  .equ    06000h      ; xxxx xxxx.xxxx xxxx
ISOOLMT   .equ    01A00h      ; xxxx xxx.x xxxx xxxx
TRAMIN    .equ    01400h      ; xxxx xx.xx xxxx xxxx

*****************************************************************
*                       initialization                          *
*****************************************************************

          .sect   "P3INIT"
START     DINT                ;
          SSXM                ;
          LDPK    00000h      ; point to date page 0
                              ; *- initial interrupt vectors -*
          LALK    P3RP2IT     ; interrupt vector for P3RP2IT
          SACL    VINT2       ;
          LALK    ADINtNT     ; interrupt vector for A/D
          SACL    VRINT       ;
          LALK    0FF80h      ; get branch operating code
          SACL    BCODE       ;
          LALK    03FF0h      ; get first vector address
          ADDK    00004h      ;
          TBLW    BCODE       ; load branch Instruction code
          ADDK    00001h      ; acc = 03EF5h
          TBLW    VINT2       ;
          ADDK    00003h      ;
          TBLW    BCODE       ;
          ADDK    00001h      ;
          TBLW    VRINT       ;
                              ;
          LACK    00014h      ; enable RINT INT2
          SACL    IMR         ;
                              ; *- initialize ARX -*
          LRLK    AR1,00280h  ; AR1 is used for P3RP2IT stack
          LRLK    AR2,002A0h  ; AR2 is used for ADINtNT stack
          LRLK    AR4,00200h  ;
                              ;
          LARP    00004h      ; point to AR4
          LACK    00000h      ; clear working area on chip
          RPTK    255         ;
          SACL    *+          ;
          RPTK    255         ;
          SACL    *+          ;
                              ;
          LDPK    00004h      ; *- point to page 4 -*
          LALK    00038h      ; initialize SMARK
          SACL    SMARK       ;
          OUT     SMARK,0Fh   ; turn on 3 LEDs -> 00111000(0-7)
                              ;
          LALK    00200h      ; set LED flashing time control counter
          SACL    FCOUNT      ;
                              ;
          LACK    00001h      ;
          SACL    SWAVG       ; set sign of
                              ; *- initialize system matrix -*
          LALK    01CCDh      ; hig1(2,2) = |-.9|(=tac) = xxx.x xxxx xxxx xxxx
          SACL    HIG1_1122   ;
          LALK    05000h      ; hig1(1,2) = 2.5(=xl)
          SACL    HIG1_1221   ;
          LALK    02E53h      ; kf1(1,2) = 0.0113(=wc) = .yyyy xxxx
```

```
        SACL    KIF1_1221       ;
                                ;
        LALK    07421h          ;
        SACL    SQR23           ; sqr23 = 65536x16368xsqrt(2)/14745/sqrt(3)
                                ;
        LALK    06187h          ;
        SACL    INV42           ; 1/42 = y.yyyy xxxx xxxx xxxx xxxx
                                ;
        LALK    02000h          ;
        SACL    IDCREF          ; idcref = xxxx xx.xx xxxx xxxx
        LALK    007D2h          ;
        SACL    ISQOO           ; just used for first step calculation
                                ;
        EINT                    ; *- enable interrupt -*

*****************************************************************************
*                       Main program                                        *
* Function  : control the LED lights flashing                               *
*****************************************************************************

                                ; *- LED light flashing control -*
FLASH   LAC     FCOUNT          ; load flashing time control count
        BGZ     ADJEND          ;
                                ; if fcount = 0 then
        LAC     SMARK           ;
        XORK    0003Fh          ;   interchange lights
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;
        LALK    00200h          ;   set fcount
        SACL    FCOUNT          ;   fcount = 200
ADJEND  B       FLASH           ; do loop

*****************************************************************************
* Subroutine    : P3RP2IT.ASM response to DSP-2 interrupt call              *
* Function      : parallel processing with DSP-2, sampling isa, isb, vcapa and vcapb *
*****************************************************************************

        .sect   "P3RP2IT"
                                ; *- save current registers -*
P3RP2IT LARP    00001h          ; point to AR1
        ADRK    00001h          ;
        SST1    *+              ;
        SST     *+              ;
        SACH    *+              ;
        SACL    *,0,4           ; point to AR4
                                ;
BBP3    OUT     SMARK,0Ch       ; start A/D on PAL circuit box
        LRLK    AR3,ADINDAT1    ; AR3 point to first A/D date_in address
        LACK    00000h          ;
        SACL    ADINNO          ; clear A/D input count
                                ;
        LAC     SMARK           ; *- set "busy" signal to sync. circuit -*
        ANDK    0FF7Fh          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;
                                ;
        EINT                    ;
                                ;
        LRLK    AR4,GADCIDC     ;
        LAC     *               ;
        SACL    ADCIDC          ; load idc
                                ; *- moving average filtering of idc -*
        LRLK    AR4,MIDC_1      ;
        LAC     *,15            ;
        ADD     ADCIDC,15       ;
        SACH    AVG2IDC         ; avg2idc = (idc(k) + idc(k-1))/2
                                ;
UREF    LRLK    AR4,GIREF       ;
        LAC     *               ;
        SACL    IDCREF          ; load idcref
                                ;
FERROR  LAC     IDCREF          ;
        SUB     AVG2IDC         ;
        SACL    IDCERR          ; idcerr = idcref-avg2idc
                                ; *- integral control -*
IIDC    ZALH    INTERR          ;
        SOVM                    ;
        ADD     IDCERR,14       ;
        ROVM                    ;
        SACH    INTERR          ; interr = interr + idcerr
                                ; *- proportional control -*
        LRLK    AR4,GKPIDC      ;
        LT      *               ;
FISQO   MPY     IDCERR          ; idcerrxKp
        LRLK    AR4,GKIIDC      ;
        LTP     *               ;
        MPY     INTERR          ; interrxKi
        LRLK    AR4,HIG1_1221   ;
        LTA     *               ;
        NEG                     ;
        SACH    ISQO,4          ; isqo = -(idcerrxKp + interrxKi)
                                ; *- limiter -*
        LAC     ISQO            ;
        BLZ     CHKLOW2         ;
CHKUP2  SBLK    ISQOLMT         ; if isqo < isqolmt (isqo > = 0) then
        BLEZ    SDISQO          ;   no change
        LALK    ISQOLMT         ; else isqo = isqolmt
        SACL    ISQO            ;
        B       SDISQO          ;
CHKLOW2 ADLK    ISQOLMT         ; if isqo > -isqolmt (isqo < 0) then
        BGEZ    SDISQO          ;   no change
        LALK    ISQOLMT         ; else isqo = -isqolmt
        NEG                     ;
        SACL    ISQO            ;
                                ;
SDISQO  LRLK    AR4,GISQO       ; *- send isqo to global memory -*
        LAC     ISQO            ;
        SACL    *               ;
                                ;
FVCDO   MPY     ISQO            ;
        LTP     HIG1_1122       ;
        SACH    VCDO            ; vcdo = hig1(1,2)*isqo
                                ;
FVCQO   MPY     ISQO            ;
        LTP     KIF1_1221       ;
        NEG                     ;
        LRLK    AR4,GVSQO       ;
        SUB     *,15            ;
        SACH    VCQO            ; vcqo = -|hig1(2,2)|*isqo-|2^vsoq|
                                ;
FIPDO   MPY     VCQO            ;
        PAC                     ;
        SACH    IPDO            ; ipdo = kif1(1,2)*vcqo
                                ;
FIPQO   MPY     VCDO            ;
        LTP     INV42           ;
        NEG                     ;
        SFR                     ;
        ADDH    ISQO            ;
        SACH    IPQO,1          ; ipqo = -|Kif1(2,1)|*vcdo + isqo
                                ;
TESTIA  LAC     ADINNO          ; waiting for A/D input iaca
```

```
        BZ      TESTIA
        LAC     ADINDAT1
        NEG
        SACL    ADINDAT1        ;considering there is a inverter in sensor
        LAC     SWAVG           ;*- test if need to remove sensor drift -*
        BZ      SIACA
                                ;*- 42 points moving average filtering -*
RMZIA   ZALS    SUMIAL
        ADDH    SUMIAH
        LRLK    AR4,IACA_42
        SUB     *,12
        ADD     ADINDAT1,12
        SACL    SUMIAL
        SACH    SUMIAH          ;sumiah=sumiah-iaca(k-42)+iaca(k)
        MPY     SUMIAH
        LTP     SQR23
        SACH    AVGIA           ;avgia=sumiah/42
SIACA   LRLK    AR4,GIACA
        LAC     ADINDAT1
        SUB     AVGIA
        SACL    *               ;iaca=iaca-avgia
                                ;*- set "ready" to sync. circuit -*
        RXF
        SXF                     ;clear BIO
        LAC     SMARK
        ORK     00080h
        SACL    SMARK
        OUT     SMARK,0Fh       ;set bit7 of port F for ready
WAIT_1  BIOZ    WAIT_1          ;*- wait for "all-ready" from sync. circuit -*
        LAC     SMARK
        ANDK    0FF7Fh
        SACL    SMARK
        OUT     SMARK,0Fh       ;reset bit7 of port F
FCOSD   LRLK    AR4,GCOSD
        MPY     *-              ;sqr23xcosd
        PAC
        SACH    COSD,1          ;xx.xx xxxx xxxx xxxx
FSIND   MPY     *
        LTP     VCOO
        SACH    SIND,1          ;sqr23xsind
FVCAPAO MPY     COSD
        LTP     VCOO
        MPY     SIND
        LTS     SQR23           ;vcapao=sqr23x(vcdoxcosd-vcqoxsind)
        SACH    VCAPAO,2        ;xxxx xxxx xx.xx xxxx
SVCAPAO LRLK    AR4,GVCAPAO
        SACH    *,2             ;send vcapao to global memory
FCOS120D LRLK   AR4,GCOS120D
        MPY     *-
        PAC
        SACH    COS120D,1       ;sqr23xcos120d
FSIN120D MPY    *
        LTP     VCDO
        SACH    SIN120D,1       ;sqr23xsin120d
FVCAPBO MPY     COS120D
        LTP     VCOO
        MPY     SIN120D
        LTS     ISOO
        SACH    VCAPBO,2        ;vcapbo=sqr23x(vcdoxcos120d-vcqoxsin120d)
SVCAPBO LRLK    AR4,GVCAPBO     ;send vcapbo to global memory
        SACH    *,2
FIBO    MPY     SIN120D
        LTP     INV42           ;*
        NEG                     ;iacbo=sqr23xsin120dxisqo
        SACH    IACBO,4         ;ACC*16 xxxx x.xxx xxxx xxxx
SIACBO  LRLK    AR4,GIACBO
        SACH    *,4             ;send iacbo to global memory
TESTIB  LAC     ADINNO          ;*- waiting for iacb -*
        SUBK    00002h
        BLZ     TESTIB
        LAC     ADINDAT2        ;load iacb
        NEG
        SACL    ADINDAT2        ;considering there is a inverter in sensor
        LAC     SWAVG           ;*- test if need to remove sensor drift -*
        BZ      SIACB
                                ;*- 42 points moving average filtering -*
RMZIB   ZALS    SUMIBL
        ADDH    SUMIBH
        LRLK    AR4,IACB_42
        SUB     *,12
        ADD     ADINDAT2,12
        SACL    SUMIBL
        SACH    SUMIBH          ;sumibh=sumibh-iacb(k-42)+iacb(k)
        MPY     SUMIBH
        LTP     SQR23
        SACH    AVGIB           ;avgib=sumibh/42
SIACB   LRLK    AR4,GIACB
        LAC     ADINDAT2
        SUB     AVGIB
        SACL    *               ;iacb=iacb-avgib
        RXF
        SXF
        LAC     SMARK
        ORK     00080h
        SACL    SMARK
        OUT     SMARK,0Fh
WAIT_2  BIOZ    WAIT_2
        LAC     SMARK
        ANDK    0FF7Fh
        SACL    SMARK
        OUT     SMARK,0Fh
FCOSA   LRLK    AR4,GCOSA
        MPY     *-
        PAC
        SACH    COSA,1          ;sqr23xcosa
FSINA   MPY     *
        LTP     IPDO
        SACH    SINA,1          ;sqr23xsina
FIPAO   MPY     COSA
```

```
        LTP     IPQO
        MPY     SINA
        LTS     SQR23           ; ipao = sqr23x(ipdoxcosa-ipqoxsina)
        SACH    IPAO,2          ; xxxx xx.xx xxxx xxxx
SIPAO   LRLK    AR4,GIPAO
        SACH    *,2             ; send ipao to global memory

FCOS120A LRLK   AR4,GCOS120A
        MPY     *-
        PAC
        SACH    COS120A,1       ; sqr23xcos120a

FSIN120A MPY    *
        LTP     IPDO
        SACH    SIN120A,1       ; sqr23xsin120a

FIPBO   MPY     COS120A
        LTP     IPQO
        MPY     SIN120A
        LTS     INV42
        SACH    IPBO,2          ; ipbo = sqr23x(ipdoxcos120a-ipqoxsin120a)
SIPBO   LRLK    AR4,GIPBO
        SACH    *,2             ; send ipbo to global memory

TESTVA  LAC     ADINNO          ; *- waiting for vcapa -*
        SUBK    00003h
        BLZ     TESTVA
                                ; *- test if need to remove sensor drift -*
        LAC     SWAVG
        BZ      SVCAPA
                                ; *- 42 points moving average filtering -*
RMZVA   ZALS    SUMVCAL
        ADDH    SUMVCAH
        LRLK    AR4,VCA_42
        SUB     *,12
        ADD     ADINDAT3,12
        SACL    SUMVCAL
        SACH    SUMVCAH         ; sumvcah = sumvcah-vcapa(k-42) + vcapa(k)

        MPY     SUMVCAH
        PAC
        SACH    AVGVCA          ; avgvca = sumvcah/42

SVCAPA  LRLK    AR4,GVCAPA
        LAC     ADINDAT3
        SUB     AVGVCA
        SACL    *               ; vcapa = vcapa-avgvca

        RXF
        SXF
        LAC     SMARK
        ORK     00080h
        SACL    SMARK
        OUT     SMARK,0Fh
WAIT_3  BIOZ    WAIT_3
        LAC     SMARK
        ANDK    0FF7Fh
        SACL    SMARK
        OUT     SMARK,0Fh
                                ; *- 42 points moving average filtering for idc -*
FMAVGIDC ZALS   SUMIDCL
        ADDH    SUMIDCH
        LRLK    AR4,MIDC_42
        SUB     *,12
        ADD     ADCIDC,12
        SACL    SUMIDCL         ; sumidch = sumidch-idc(k-42) + idc(k)
        SACH    SUMIDCH         ; xxxx xxxx xx.xx xxxx

        MPY     SUMIDCH
        PAC                     ; mavgidc = sumidch/42
        SACH    MAVGIDC         ; xxxx xx.xx xxxx xxxx

TESTVB  LAC     ADINNO          ; *- waiting for vcapb -*
        SUBK    00004h
        BLZ     TESTVB

        LAC     SWAVG           ; *- test if need to remove sensor drift -*
        BZ      SVCAPB
                                ; *- 42 point moving average filtering -*
RMZVB   ZALS    SUMVCBL
        ADDH    SUMVCBH
        LRLK    AR4,VCB_42
        SUB     *,12
        ADD     ADINDAT4,12
        SACL    SUMVCBL
        SACH    SUMVCBH         ; sumvcbh = sumvcbh-vcapb(k-42) + vcapb(k)

        MPY     SUMVCBH
        PAC
        SACH    AVGVCB          ; avgvcb = sumvcbh/42

SVCAPB  LRLK    AR4,GVCAPB
        LAC     ADINDAT4
        SUB     AVGVCB
        SACL    *               ; vcapb = vcapb-avgvcb

        RXF
        SXF
        LAC     SMARK
        ORK     00080h
        SACL    SMARK
        OUT     SMARK,0Fh
WAIT_4  BIOZ    WAIT_4
        LAC     SMARK
        ANDK    0FF7Fh
        SACL    SMARK
        OUT     SMARK,0Fh
                                ; *- get triangle magnitude -*
FTRA    LAC     MAVGIDC
        SBLK    TRAMIN          ; *- minimal limiter -*
        BGEZ    TIMES05
        LALK    TRAMIN,15
        ADLK    TRAMIN,14
        SACH    TRAMGN,1        ; tramgn = 1.5xtramin
        B       STRAMGN

TIMES05 LAC     MAVGIDC,15
        ADD     MAVGIDC,14
        SACH    TRAMGN,1        ; tramgn = 1.5xmavgidc

STRAMGN LRLK    AR4,GTRAMGN
        SACH    *,1             ; send tramgn to global memory

        LRLK    AR4,GPRDBAK
        LAC     *+              ; load PRDBAK
        SACL    PRDBAK
        LAC     *               ; load TRSIGN
        SACL    TRSIGN
        LT      PRDBAK

        RXF
```

```
        SXF
        LAC     SMARK
        ORK     00080h
        SACL    SMARK
        OUT     SMARK,0Fh
WAIT_5  BIOZ    WAIT_5
        LAC     SMARK
        ANDK    0FF7Fh
        SACL    SMARK
        OUT     SMARK,0Fh

        LRLK    AR4,GIMPC       ;*- get timing constant for phase C -*
        LAC     *               ; load impc
        SACL    TEMP1
FINDDATC BLZ    NEGSGN
        LACK    00000h          ; if impc>0 then
        SACL    TEMP2           ;   set temp2=0
        B       FRACT
NEGSGN  ABS                     ; if impc<0 then
        SACL    TEMP1           ;   impc=|impc|, set temp2=1
        LACK    00001h
        SACL    TEMP2
FRACT   LAC     TEMP1
        SUB     TRAMGN
        BLZ     DIVID
NFRACT  LAC     TRSIGN          ; if |impc|>tramgn then
        BZ      SIGN0           ;   if trsign=rising then
SIGN1   LAC     TEMP2           ;     if impc<0 then
        BZ      PRDMAX
PRDMIN  LACK    00008h          ;       data=prdmin
        B       CORRECT
PRDMAX  LAC     PRDBAK          ;     else data=prdmax
        B       CORRECT
SIGN0   LAC     TEMP2           ;   elseif impc<0 then
        BZ      PRDMIN          ;       data=prdmin
        B       PRDMAX          ;   else data=prdmax
DIVID   ZALH    TEMP1
        RPTK    10
        SUBC    TRAMGN
        SACL    TEMP1           ; quot=xxxx x.xxx xxxx xxxx
        LAC     TEMP2
        BZ      ADDTRA
        ZAC                     ; if impc<0 then
        SUB     TEMP1           ;   quot=-quot
        SACL    TEMP1
ADDTRA  LAC     TRSIGN          ; fetch triangle edge sign.
        BZ      MINUS
        LALK    00800h          ; if trsign=rising then
        ADD     TEMP1           ;   acc=1+temp1
        B       MPRDO2
MINUS   LALK    00800h          ; else acc=1-temp1
        SUB     TEMP1
MPRDO2  SACL    TEMP1           ; save (1 +/- impc/tramgn)
        MPY     TEMP1           ; PRD*(1 +/- impc/tramgn)/2
        SPM     00002h
        SPH     TEMP1
        LAC     TEMP1
CORRECT ADLK    00100h          ; add offset, since hardware design
                                ; acc=timing constant
SCONSTC LRLK    AR4,GCONSTC
        SACL    *               ; send consic to global memory

        RXF
        SXF
        LAC     SMARK
        ORK     00080h
        SACL    SMARK
        OUT     SMARK,0Fh
WAIT_6  BIOZ    WAIT_6
        LAC     SMARK
        ANDK    0FF7Fh
        SACL    SMARK
        OUT     SMARK,0Fh

                                ;*- data shifting -*
MOVIDC  LRLK    AR4,MIDC_41     ; for i=42 to 2
        RPTK    40              ; idc(i)=idc(i-1),
        DMOV    *-
        LRLK    AR4,MIDC_1
        LAC     ADCIDC
        SACL    *               ; idc(1)=adcidc

        LAC     SWAVG           ; if need to remove sensor drift then
        BZ      LASTP
                                ;*- do the same work like shifting idc on iac and vcap -*
MOVING  LRLK    AR4,VCB_41
        RPTK    168
        DMOV    *-              ; shift whole group of iac and vcap data
        LRLK    AR4,IACA_1
        LAC     ADINDAT1
        SACL    *               ; iaca(1)=iaca
        LRLK    AR4,IACB_1
        LAC     ADINDAT2
        SACL    *               ; iacb(1)=iacb
        LRLK    AR4,VCA_1
        LAC     ADINDAT3
        SACL    *               ; vcapa(1)=vcapa
        LRLK    AR4,VCB_1
        LAC     ADINDAT4
        SACL    *               ; vcapb(1)=vcapb

        LAC     SWAVG
        ADDK    00001h          ; swavg=swavg+1, until swavg=0
LASTP   LAC     FCOUNT          ; fcount=fcount-1
        SUBK    00001h
        SACL    FCOUNT
                                ;*- output to be displayed data to global memory -*
        LRLK    AR4,GP3INDEX    ; point to index
        LALK    00200h          ; load begin address of variables
        ADD     *
        SACL    DAOUT           ; save address
        LAR     AR4,DAOUT
        LAC     *               ; load the data to be displayed
        LRLK    AR4,GP3DA
        SACL    *               ; then send it to global memory

RECOVF  LARP    00001h          ;*- recover previous registers -*
        ZALS    *-
        ADDH    *-
        LST     *-
        LST1    *-
        EINT                    ; enable interrupt
        RET

*****************************************************************
* Subroutine  : ADINT.ASM  response to A/D data-in interrupt call *
* Function    : transferring 4 input data from DRR to global memory *
* Affect      : AR2 is used to save current field, AR3 is used to send data *
* Output      : ADINNO                                          *
*****************************************************************

        .sect   "ADINNT"
                                ;*- save current registers -*
```

```
ADINT   LARP    00002h          ; point to AR2
        ADRK    00001h          ;
        SST1    *+              ;
        SST     *+              ;
        SACH    *+              ;
        SACL    *,0,3           ;
                                ;
        LAC     ADINNO          ;
        ADDK    00001h          ;
        SACL    ADINNO          ; adinno = adinno + 1, indicate one more data in
        LDPK    00000h          ; point to page 0
        LAC     DRR             ;
        LDPK    00004h          ;
        SFR                     ; DDR = 00xx xxxx xx.xx xxxx
        SACL    *+,0,2          ; save data to global memory
                                ; *- recover previous registers -*
RECOVA  ZALS    *-              ;
        ADDH    *-              ;
        LST     *-              ;
        LST1    *-              ;
        EINT                    ; enable interrupt
        RET                     ;
                                ;
        .end                    ; *** end of file ***
```

Table C-3 The List of DSP-1 Control Program.

```
*****************************************************************************
* Name     : DSP-1.ASM                                                      *
* Function : interrupt (int0) service subroutine cooperates with DSP-2 and DSP-3, to send the *
*            "ready" signals to the sync. circuit all the time.             *
*            The main tasks of communication with PC are performed by using the utilities wrote in *
*            the EPROM monitor program.                                     *
*****************************************************************************

        .title  'DSP-1 program'
IMR     .equ    00004h          ; page 0 (00000h-0007Fh)
SMARK   .equ    00060h
BCODE   .equ    00079h
VINT0   .equ    0007Ah

*****************************************************************************
*                       initialization                                      *
*****************************************************************************

        .sect   "P1INIT"
START   DINT                    ;
        LDPK    00000h          ; point to date page 0
                                ; *- initialize interrupt vector -*
        LALK    P1RP2IT         ;
        SACL    VINT0           ;
        LALK    0FF80h          ; load branch operating code
        SACL    BCODE           ;
        LALK    03FF0h          ; load first vector address
        TBLW    BCODE           ; start to load interrupt vectors
        ADDK    00001h          ;
        TBLW    VINT0           ;
        LAC     IMR             ;
        ORK     00001h          ; set enable mark for int0
        SACL    IMR             ;
                                ;
        OUT     SMARK,0Eh       ; *- send a interrupt signal to DSP-2 asking -*
                                ;   for starting parallel processing
        LACK    00040h          ; EPROM enter address is pushed on the top of stack
        PUSH                    ;
        EINT                    ; enable interupt
        RET                     ; jump to the EPROM monitor programe

*****************************************************************************
* Subroutine    : P1RP2IT.ASM   response to the DSP-2 interrupt call.       *
*****************************************************************************

        .sect   "P1RP2IT"
                                ; *- save current registers -*
P1RP2IT LARP    00005h          ;
        LRLK    AR5,00300h      ;
        SST1    *+              ;
        SST     *+              ;
        SACH    *+              ;
        SACL    *+              ;
        LAC     SMARK           ;
        SACL    *               ;
                                ;
        LDPK    00000h          ; point to page 0
        LALK    00008h          ;
HHDD1   SUBK    00001h          ; *- do-loop waiting -*
        BGZ     HHDD1           ;
        RXF                     ;
```

```
        SXF                     ; clear BIO
        LAC     SMARK           ;
        ORK     00080h          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ; set "ready" signal to sync. circuit
WAIT_1  BIOZ    WAIT_1          ; wait for "all-ready" signal from sync. circuit
        LAC     SMARK           ;
        ANDK    0FF7Fh          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ; reset "ready" signal

        LALK    00008h          ;
HHDD2   SUBK    00001h          ;
        BGZ     HHDD2           ;
        RXF                     ;
        SXF                     ;
        LAC     SMARK           ;
        ORK     00080h          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;
WAIT_2  BIOZ    WAIT_2          ; *- second waiting -*
        LAC     SMARK           ;
        ANDK    0FF7Fh          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;

        LALK    00008h          ;
HHDD3   SUBK    00001h          ;
        BGZ     HHDD3           ;
        RXF                     ;
        SXF                     ;
        LAC     SMARK           ;
        ORK     00080h          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;
WAIT_3  BIOZ    WAIT_3          ; *- third waiting -*
        LAC     SMARK           ;
        ANDK    0FF7Fh          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;

        LALK    00008h          ;
HHDD4   SUBK    00001h          ;
        BGZ     HHDD4           ;
        RXF                     ;
        SXF                     ;
        LAC     SMARK           ;
        ORK     00080h          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;
WAIT_4  BIOZ    WAIT_4          ; *- fourth waiting -*
        LAC     SMARK           ;
        ANDK    0FF7Fh          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;

        LALK    00008h          ;
HHDD5   SUBK    00001h          ;
        BGZ     HHDD5           ;
        RXF                     ;
        SXF                     ;
        LAC     SMARK           ;
        ORK     00080h          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;
WAIT_5  BIOZ    WAIT_5          ; *- fifth waiting -*
        LAC     SMARK           ;
        ANDK    0FF7Fh          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;

        LALK    00008h          ;
HHDD6   SUBK    00001h          ;
        BGZ     HHDD6           ;
        RXF                     ;
        SXF                     ;
        LAC     SMARK           ;
        ORK     00080h          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;
WAIT_6  BIOZ    WAIT_6          ; *- sixth waiting -*
        LAC     SMARK           ;
        ANDK    0FF7Fh          ;
        SACL    SMARK           ;
        OUT     SMARK,0Fh       ;
                                ; *- recover previous registers -*
RECOVE  LAC     *-              ;
        SACL    SMARK           ;
        ZALS    *-              ;
        ADDH    *-              ;
        LST     *-              ;
        LST1    *               ;
        EINT                    ; enable interrupt
        RET                     ;

        .end                    ; *** end of file ***
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