Design and Fabrication of an Ion Sensitive Field Effect Transistor and Readout Circuit using a Commercial TSMC 65nm Process

Gueorgui Savadjiev

Department of Electrical and Computer Engineering

McGill University
Montreal, Quebec

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Abstract

This thesis presents the design considerations to building an implantable pH sensor for biomedical applications using solid-state ion-sensitive field effect transistors (ISFET), and the design and testing of an electronic readout circuit using the TSMC 65nm process. The use of ISFET-based pH sensors is motivated by the difficulty of achieving miniaturization with common pH glass electrodes. In this work, a floating gate ISFET structure had to be used instead of the traditional ISFET structure. This leads to design challenges related to loading effects and leakage currents on the floating gate. A systematic investigation of different readout circuit techniques to resolve the problems was conducted, and three main designs were proposed, analyzed and compared. Simulations investigated the correct operation of the designs. A model of the ISFET was implemented in verilog for simulation purposes. An IC was designed and fabricated, containing two identical op-amps and switches that could be used to implement the circuit in practice. Laboratory experiments were conducted simulating the pH and bulk potentials using a single power supply connected to a capacitance emulating the sensing dielectric. The experiments also investigated the implementation of a differential readout circuit. It was observed that the leakage and loading effects were significant, so that the simplest circuit could not work in practice. The differential configuration showed a significant reduction in common-mode sensitivity to bulk potential variation.

Résumé

Cette thèse présente la démarche de conception pour un capteur de pH implantable destiné à des fins biomédicales utilisant la technologie en état solide des transistors FET sensitifs aux ions (ISFET), ainsi que la conception d'un circuit électronique pour la lecture du signal basé sur le processus de fabrication de TSMC 65nm. L'utilisation des ISFET pour capteurs de pH est motivée par la difficulté d'achever la miniaturization des électrodes de verre habituellement utilisées en pH-métrie. Dans cet ouvrage, un ISFET à grille flottante a du être utilisé au lieu de la structure traditionnelle. Cela mène à des obstacles causés par l'effet de charge ainsi que des fuites de courant dans la grille flottante. Une étude systématique de différentes techniques de circuit de lecture destinés à surmonter ces obstacles a été effectuée, et trois concepts ont été proposés, analysés et comparés. Le bon fonctionnement en simulation de chacun de ces concepts a été étudié. Un modèle de l'ISFET a été réalisé en veriloga à des fins de simulation. Un CI a été conçu et fabriqué, celui-ci contenant deux amplificateurs opérationnels et commutateurs identiques pouvant être utilisés pour mettre en pratique le circuit. Des expériences en laboratoire ont été effectuées, imitant les signaux de pH et de potentiel de solution avec une source de tension connectée à un condensateur représentatif du matériel diélectrique sensitif. Les expériences ont aussi étudié la mise en oeuvre d'un circuit de lecture différentiel. Il a été observé que les fuites de courant et les effets de charge sont significatives, et que par conséquent le circuit le plus simple ne peut fonctionner en pratique. La configuration différentielle démontre une réduction significative de sensibilité au mode commun liée aux variations de potentiel de solution.

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Chapter 1

Introduction

1.1 Motivation

The measurement of pH is a basic tool in chemistry and biomedical disciplines. It can be used to study properties of acids and bases, as well as to observe the progression of various chemical reactions in a solution. In medicine, blood pH is an important indicator of a patient's condition. Monitoring its evolution can provide valuable information on the progression of an injury, and pH measurements can be the basis for critical decisions regarding surgical procedures. For this reason, it is highly desirable to have an implantable and biocompatible pH sensor. The most common pH measurement instrument today is the glass electrode. Glass electrodes provide very accurate and low noise measurements, but they are bulky and difficult to miniaturize. Hence research has been done on different sensing mechanisms for pH sensors that can be easily fabricated in small sizes.

As a reminder, the pH of a solution is defined by the equation

$$\mathrm{pH} = -\log_{10}(a_{\mathrm{H}^+}) \tag{1.1}$$

where a_{H^+} is the activity of the H^+ ions in the bulk of the solution (activity is closely related to molar concentration, and can in this case be reliably replaced by the molar concentration of H^+ ions in the bulk solution divided by the standard molar concentration of 1 mol/L). The pH of pure water is generally around 7, acids have a pH less than 7 and bases have a pH greater than 7. In biological settings, particularly in human blood, the pH of blood will typically remain between 6 and 7, and variations of blood pH can be an indication of the health of an individual.

The ion-sensitive field effect transistor (ISFET) is a promising pH sensor approach based on solid-state electronics. The fundamental mechanism

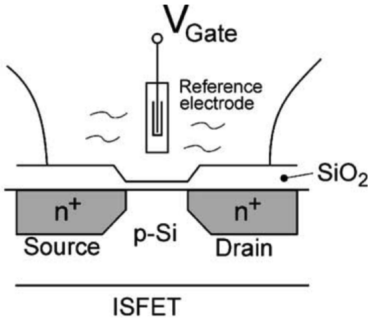


Figure 1.1 – Schematic of the ISFET. Image from [1]. Reprinted with permission from Elsevier. Copyright © 2002 Elsevier Science B.V. All rights reserved.

behind the ISFET is similar to that of an ordinary MOSFET, except that the gate structure is modified in order to be sensitive to pH. This is achieved by using a dielectric material that reacts chemically with the H^+ ions in the solution by the presence of dangling bonds on its surface. The concentration of H^+ ions in the solution affects the overall charge density on the surface of the dielectric, and this in turn produces an electric field across the gate. This electric field affects the channel conductivity in a way similar to the MOSFET. One can view its effect as a modification of the threshold voltage (V_T) by the pH. In addition, there is a reference electrode that must be placed in contact with the bulk of the solution in order to keep a stable reference potential. The basic structure of the ISFET is shown in Figure 1.1.

The ISFET is then very similar to the MOSFET devices already available in most commercial IC processes, so that few modifications are required to produce pH sensors (or other ionic sensors). However, it would be desirable to use a single unmodified process to produce the ISFET and electronic readout circuit, since custom IC fabrication procedures require access to expensive equipment and many development cycles to reach an acceptable performance.

The sensing gate should have a fairly large area to improve its sensitivity and reduce parasitic effects. Chip area on current microelectronics processes is expensive, so it would be preferable to avoid wasting precious area on the chip itself. In any case, a standard fabrication process such as TSMC 65nm does not support deposition of the dielectrics necessary for pH sensors. There has been some work by Milgrew [8] as well as Hu and Georgiou [7] to integrate the sensing element on chip by using the silicon nitride (Si_3N_4) passivation layer with the AMS 0.35μm process, which does not require any additional post-processing steps. Work has also been done to integrate the reference electrode. For example, the use of an on-chip gold electrode by

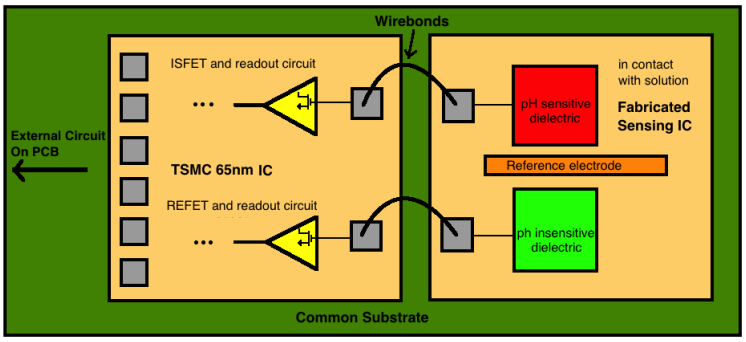


Figure 1.2 – High-level structure of pH sensor.

Liao *et al.* [2]. Again, in these cases the gate area is constrained by the chip size, and the TSMC 65nm process used in this thesis did not support such additions.

Therefore, it was decided that the design would include two separate components: 1) the transistor (ISFET) and electronic readout circuit implemented with the standard TSMC 65nm process and 2) a separate chip containing the sensing elements and reference electrodes fabricated using cheaper facilities available from the university. The two chips would later be combined on a common substrate by wirebonding as shown in Figure 1.2. Here a REFET and its readout circuit is added. The REFET has the same structure and readout circuit as the ISFET except that the REFET is connected a pH insensitive layer. The purpose of the REFET is to remove the noise of the reference electrode, as will be discussed in the next chapter. The resulting structure can still remain sufficiently small to be implantable. The benefits from such a design separation are that the expensive electronic IC does not waste area for the sensing elements and reference electrodes, and that the two parts can be designed and tested independently, to be combined only once both parts have been shown to work.

1.2 High-Level Structure of the System

To further clarify the structure of the pH sensing system, a high-level system block diagram is shown in Figure 1.3. The diagram shows the various components and signals present in the pH sensor. Each component will be discussed in more detail in Chapter 3. It is emphasized that the TSMC 65nm IC fabricated in this thesis corresponds to the ISFET and readout circuit block. However, the other blocks are essential to understand the operation of the sensor, and they should be modeled for analysis and simulation pur-

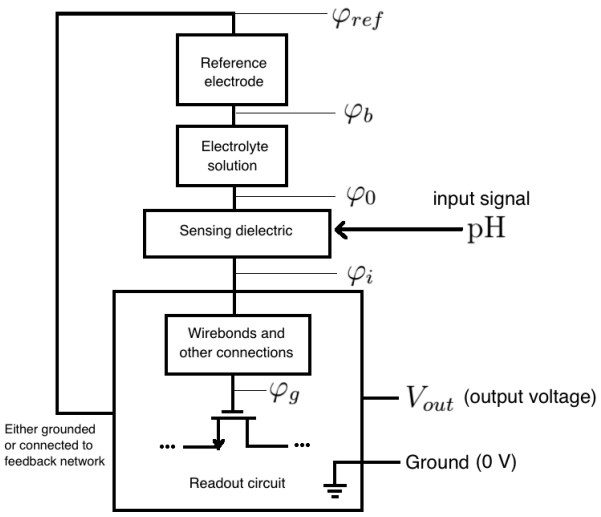


Figure 1.3 – High-level system block diagram.

poses. The reference electrode component has two terminals corresponding to potentials φ_{ref} and φ_b. The φ_{ref} terminal is connected to ground or to a feedback node coming out of the readout circuit. The terminal φ_b represents the bulk potential of the electrolyte solution. The potential of the electrolyte solution varies as a function of the distance to the sensing dielectric surface, and right at the surface, the potential is represented by the terminal φ_0. The sensing dielectric will, depending on the pH, lead to a potential φ_i on its other side, which connects to the readout circuit.

1.3 Main Challenges

Despite the possible advantages, many issues were encountered in this approach as well. The main drawbacks are that the structure of the ISFET becomes more complicated than that of the traditional ISFET. This structure becomes sensitive to new effects that make the readout more difficult. One of the main concerns during the design of the electronic readout circuit was the effect of input current leakage. In the current design, the ISFET actually consists of a complete MOSFET in the TSMC chip, whose gate dielectric uses the standard silicon dioxide (SiO_2) material and is connected to metal layers all the way up to an aluminum (Al) pad on the IC. This pad would then be wirebonded to another pad on the second chip, which is connected to the second dielectric material that is pH sensitive.The resulting structure does not really work the same way as the traditional ISFET.

It can be viewed as two dielectrics connected by a floating piece of metal, which is similar to a floating-gate MOS transistor. Any charge stored on this metal node affects the gate voltage of the MOSFET and hence the readout value. If there is any current leakage path, then this charge can vary over time due to the discharge process, and will cause the readings to drift. In addition, due to the large physical extent of the metal conductor, one has to consider the effect of parasitic capacitance to external sources of potential, which could couple into the readout circuit. One important source of leakage is the gate of the input MOS transistor itself. Even though the gate current is usually considered to be extremely small due to the gate being an isolator, there is in fact some current coming from the tunneling effect. This tunneling current depends on the gate area and thickness (see section 2.1.2). The application for which this pH sensor was designed requires the ability to continuously monitor pH for up to 48 hours, so the effect of the drift and other parasitic effects must be negligible over a long period of time. Even a very small leakage current on the order of picoamps (pA) is too large when its effect accumulates over such a long period of time. These considerations will be discussed further in the theory and simulation chapters. The main takeaway is that particular attention must be given to minimize the input current leakage, as well as the parasitic capacitance on the floating node.

A few approaches were considered for solving the current leakage problems, which will be discussed further in Chapters 4-8. The first idea was to use the MOSFETs having the thickest gate dielectric available from the TSMC 65nm process. Detailed information on the process models cannot be publicly divulged due to NDAs, but for such a process the maximal gate thickness is less than 10 nm. But for some applications, such a thickness can have a significant tunneling effect, and simulations should be made to evaluate its influence on the performance. The best way to reduce the tunneling effect is by using the thickest gate dielectrics available in the process. Based on the simulations, this should have been enough to make the input gate leakage current negligible in the current application.

However it was not very clear how accurate the simulation models for the gate input current would be, and how much these results could be relied upon. Therefore, additional ideas were proposed to further reduce leakage effects. The first idea is to use a differential measurement, where two identical FETs and their readout circuits are on the same chip, and the only difference is that one of them is connected to a pH sensitive element and the other is connected to a reference element insensitive to pH. This idea is shown in Figure 1.2 and has been proposed in other papers such as [9, 3, 10] in order to eliminate other common-mode sources of noise such as that coming from the reference electrode. The effect of leakage (and other common-mode sources of noise)

should be symmetric over the two circuits, and will cancel out partially after a differential measurement. Another idea that was considered is to use a feedback circuit involving the reference electrode, in a way that causes the reference potential to change over time in order to compensate for the drift. Finally the idea of placing a switch that disconnects the MOSFET gate from the sensing gate between measurements in order to reduce the effect of charge leakage of long periods of time was studied. All of these ideas will be detailed further in the next chapters. Based on the simulation results, the decision was made to test the most basic circuit in the lab, consisting of a voltage buffer using the thickest transistors available.

In summary, the work in this thesis provides novel insight on the design of ion-sensitive field effect transistors and their readout circuits using the TSMC 65nm process, which is a more modern fabrication process with new challenges caused by the small scale of the components.

1.4 Thesis Structure

This thesis is organized into chapters whose purpose will be outlined here. Chapter 1 provides an introductory overview of the thesis and its main subject. Chapter 2 is a review of the theory of the ISFET and its readout circuits. Chapter 3 presents an analysis of all components of the ISFET frontend system, abstracting away to readout circuit to find the common features of all such circuits. A model for the ISFET frontend is formulated and simulated in Cadence using `veriloga`. Chapter 4 discusses the specifications of the project for the thesis, and presents the proposed readout circuits. Chapters 5, 6, 7 and 8 treat the buffer, switch and buffer, reference electrode feedback and differential readout circuits, respectively. Each chapter contains the analysis followed by simulation results in Cadence using ideal op-amp models to verify the correctness of the analysis. Chapter 9 shows simulations of the leakage current and input resistance of the MOSFET gates and switches used in the TSMC 65nm process. Chapter 10 presents the design and simulation results of the op-amps implemented in TSMC 65nm for use in the readout circuits. Chapter 11 discusses the design, layout and simulation of the full IC and bondpads. Chapter 12 will present laboratory results with fabricated ICs, including results on the performance of the op-amps, switches and transistors, as well as results for the readout circuits. Finally, Chapter 13 will be the conclusion.

Chapter 2

Literature Review

2.1 Review of MOSFET Theory

The metal-oxide semiconductor field-effect transistor (MOSFET) is a basic component of integrated circuits. The basic structure of the MOSFET consists of a semiconductor substrate, typically made of a silicon crystal (Si), over which certain regions are doped with donor or acceptor atoms. The doping determines the majority carrier type of the region, either n-type or p-type. In a p-type region, the majority carriers are positively charged holes, while in an n-type region the majority carriers are negatively charged electrons. There are two main types of MOSFETs depending on the doping of source, drain and substrate, called the n-type MOSFET (NMOS) and p-type MOSFET (PMOS). The MOSFET consists of four regions called the source, the gate, the drain and the body, as shown in Figure 2.1 for the NMOS. The PMOS will instead have p-doped source and drain, inside an n-doped substrate (in common IC fabrication processes, the substrate is always p-doped,

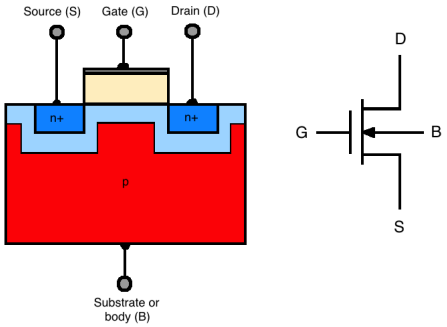


Figure 2.1 – Structure of n-type MOSFET.

but the PMOS have their own bodies isolated in n-wells). The gate terminal is separated from the substrate by an isolator which is usually silicon dioxide (SiO_2). The channel is the region in the substrate near the gate and between the source and the drain.

2.1.1 Basic model of operation

The theory of operation for the MOSFET has many intricacies in general, but the basic idea can be understood by the fact that an electrical field across the gate oxide will be able to control the conductivity of the channel. For an NMOS, a certain voltage applied between the gate and source will cause the substrate near the gate to become n-type and allow current to flow between the source and drain terminals in the channel. This voltage is called the *threshold voltage* or V_T, and is an important parameter for a MOSFET. It is possible to analyze the physics of the NMOS structure to derive equations for the current between the drain and source I_{DS} for various values of drain-to-source voltage V_{DS} and gate-to-source voltage V_{GS} [11]:

$$I_{DS} = \mu_n C'_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{ when } V_{GS} \geq V_T \text{ and } 0 \leq V_{DS} \leq V_{GS} - V_T \tag{2.1}$$

$$I_{DS} = \frac{1}{2} \mu_n C'_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \text{ when } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T \tag{2.2}$$

There are similar equations for the PMOS structure. In these equations, W is the channel width, L is the channel length, μ_n is the carrier mobility, C'_{ox} is the capacitance per area of the gate oxide and λ is the channel length modulation parameter. The first equation represents the operation of the MOSFET in the triode (or linear) region, and the second equation represents its operation in saturation. The transconductance of a MOSFET in saturation is defined by:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_n C'_{ox} \frac{W}{L} (V_{GS} - V_T)(1 + \lambda V_{DS}) \tag{2.3}$$

This is a useful parameter to model the MOSFET in small-signal analysis in order to estimate the gain of amplifier stages. Similarly one can define the output resistance r_o of a MOSFET, which in saturation is given by the equation:

$$r_o = \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right)^{-1} = \frac{1}{\mu_n C'_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \lambda} \tag{2.4}$$

In some applications, the MOSFET is biased with $V_{GS} < V_T$, in which case the device operates in the *subthreshold* region, or *weak inversion*. In this

case, the drain current follows an exponential relationship of the approximate form [12]:

$$I_{DS} = \frac{W}{L} I'_M e^{\frac{q(V_{GS}-V_T)}{nk_BT}} \left(1 - e^{-\frac{qV_{DS}}{k_BT}}\right) \tag{2.5}$$

where I'_M and n are process-dependent parameters with $n \approx 1$. The transconductance and output resistance are given by:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{q}{nk_BT} I_{DS} \tag{2.6}$$

$$r_o = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)^{-1} \approx \frac{k_BT}{qI_{DS}} e^{\frac{qV_{DS}}{k_BT}} \tag{2.7}$$

More accurate models will take into account effects such as drain-induced barrier lowering that cause the output resistance to be reduced, in a way analogous to channel length modulation.

2.1.2 Gate leakage current

The gate terminal is connected to an insulator, so the gate current is usually very small and can be neglected in most situations. However, as the thickness of the gate oxide decreases down to the nanometer scale, various effects can come into play to introduce small leakages through the gate. Such effects include the quantum mechanical tunneling of electrons across the oxide, which can happen through Fowler-Nordheim tunneling or direct tunneling [12]. It is intuitive that this gate current will increase with larger gate areas and with larger V_{GS}. Moreover, the gate current increases exponentially with decreasing oxide thickness, becoming significant below 4 nm. In the application where the MOSFET is used for this thesis, it was realized that the gate leakage current would be an important design constraint because the gate will be floating, and any charge on the gate contact will leak over time, causing voltage readings to drift. This particular issue will be discussed in more detail in Chapter 3.

2.1.3 Body effect

In an IC fabrication process using a p-substrate, all NMOS will generally have a common body connection to the substrate, which is usually grounded. If the source of an NMOS is not grounded, there will be a voltage V_{SB} between source and body terminals which can affect the threshold voltage V_T. The

dependence of V_T with V_{SB} is called the body effect, and can be modeled by the following equation [12]:

$$V_T = V_{T0} + \gamma \left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0} \right) \tag{2.8}$$

where V_{T0} is the threshold voltage when $V_{SB} = 0$ V, ϕ_0 is the surface potential (not related to φ_0 discussed later in the context of the electrolyte interface) and γ is the body effect coefficient which is process-dependent. Due to the body effect, if the source is not shorted to the body, the threshold voltage will not depend only on the pH of the electrolyte, so variations in the source voltage can affect pH readings.

2.1.4 Flicker noise

There are many sources of noise in a MOSFET, which will end up limiting the signal-to-noise ratio (SNR) of any readout circuit. Since most pH sensor applications deal with low-frequency phenomena, the dominant source of noise in this regime is the flicker noise, whose power spectral density (PSD) has a $1/f$ dependency with frequency. A common way to model the flicker noise is in terms of an input-referred gate noise voltage source which is added in series to any signal connected to the gate. In a simple empirical model, the PSD of this noise source is given by the equation [12]:

$$S_{vf}(f) = \frac{K_1}{C_{ox}'^2 W L} \frac{1}{f} \tag{2.9}$$

where K_1 is a process-dependant parameter. Intuitively, the model implies that it is desirable to increase the area of the MOSFET in order to reduce the flicker noise. It is also possible to increase the oxide capacitance per area C_{ox}' by reducing the oxide thickness. The total noise of the source will then be calculated as a root-mean-square (RMS) voltage value by integrating this expression over the frequency range of interest, and taking square roots. For low frequencies, the $1/f$ dependence will be dominant.

2.1.5 Practical models

In a practical IC fabrication process such as TSMC 65nm, the MOSFET behavior can be more complicated, notably due to the very small scale of the device. The models provided above should serve merely as a guideline for the designer, but the foundry generally provides more accurate and complete MOSFET models, usually based on BSIM4 [12, 13]. However, the specific parameters used for the model are unique to each process, and are kept confidential through the use of NDAs.

2.2 ISFET Theory

The ion-sensitive field effect transistor (ISFET) was invented by Piet Bergveld [14] in the 1970s. Its structure consists of a modified field effect transistor where the gate insulator has been replaced from the usual silicon dioxide (SiO_2) to an ion-sensitive dielectric in contact with the solution whose pH is to be measured, as well as a reference electrode in the bulk of the solution. The operation of the transistor itself is essentially the same as in a standard MOSFET, except that the pH of the solution affects the surface charge density on the dielectric gate. This surface charge density in turn affects the electric field across the insulator, causing a change in the channel conductivity in the same way as in the MOSFET. The effect of pH on the ISFET can also be understood in terms of the ISFET threshold voltage, which is given by the following equation [15]:

$$V_T = E_{ref} - \Psi + \chi^{sol} - \frac{\Phi_{\mathrm{Si}}}{q} - \frac{Q_{ox} + Q_{SS} + Q_B}{C_{ox}} + 2\phi_F \tag{2.10}$$

where E_{ref} is the reference electrode half-cell potential, Ψ is the potential drop across the electrolyte, χ^{sol} is the surface dipole potential and q is the elementary charge. The remaining terms are related to the MOSFET structure, with Φ_{Si} being the workfunction of silicon, with C_{ox} being the total oxide capacitance, with Q_{ox}, Q_{SS} and Q_B being trapped charges in the oxide, oxide/semiconductor interface and depletion layer respectively, and ϕ_F being the Fermi level of the body.

The importance of this equation lies in the fact that the Ψ term will be pH-dependent as explained in the following sections. Hence the threshold voltage of the ISFET can be modulated by changes in pH in the solution, and this can be measured with appropriate circuitry. Most of the theory regarding ISFETs relates to the basic structure proposed by Bergveld, and the threshold voltage V_T is a useful parameter in such cases, and is commonly referred to in the literature. However, as mentioned in the introduction, this thesis uses a somewhat different structure where the ISFET contains a floating metal layer between the sensing dielectric and the MOSFET gate. This introduces screening of the electric field from the surface charge on the sensing dielectric surface, and the MOSFET's threshold voltage is not really affected by pH in the same way. It becomes more important to have an expression for the voltage at the floating metal node, since this will be the input to all the electrical readout circuits.

The operation of the ISFET is explained by modeling the interface between the solution and the dielectric gate. The *site-binding model* was proposed by Yates *et al.* in 1974. A detailed discussion of the site-binding

model as well as the modeling of the electrolyte double-layer near the dielectric surface is presented in Appendix A. The main relationship that is obtained between Ψ and pH is summarized in the following equation:

$$\Psi = -2.303\frac{k_B T}{q}\alpha(\text{pH} - \text{pH}_{\text{pzc}}) \tag{2.11}$$

where k_B is Boltzmann's constant, T is the temperature (in K), q is the elementary electric charge, pH_{pzc} is the *point of zero charge*, and α is a sensitivity parameter depending on the properties of the dielectric material. The value of α is ideally 1, and materials such as tantalum pentoxide (Ta_2O_5) will have α close but slightly below 1. These provide a pH sensitivity close to the theoretical maximum which is around 59 mV/pH at 25° C.

2.3 Reference Electrode Theory

The reference electrode has been the cause of many difficulties regarding the use of ISFET and their miniaturization. In principle, the reference electrode's role is supposed to be to provide a well-controlled potential in the bulk solution, and to close the electrical loop formed by the electrolyte, the ISFET gate, and the readout circuit. Without a reference electrode, there is nothing in the system controlling the bulk potential, so its value might depend on unknown sources which could affect the voltage readings. Moreover, as remarked in the end of section A.0.4, the reference electrode could have a theoretical role in maintaining charge conservation by supplying small currents to compensate for effects of pH variation on the total charge in the bulk.

The theory of operation of an electrode involves many details and complications outside the scope of this work, which are treated in depth in electrochemistry textbooks such as Bard and Faulkner [22]. The main aspect of its operation is the electrochemical redox reaction happening at the surface of the electrode in contact with ions in the solution. During a redox reaction, there is a transfer of electrons between the electrode and the solution. The thermodynamics of such redox reactions are characterized by the half-cell potential, which indicates the electric potential drop across an electrode when the redox reactions are at equilibrium (so that there is no current flow). This half-cell potential is related to the standard electrode potential by the Nernst equation, which takes into account the effect of concentrations of ions and of the temperature on the half-cell potential. Outside of equilibrium, there will be some charge transfer between the solution and the electrode, in the form of a current that depends nonlinearly on the potential drop. The behavior

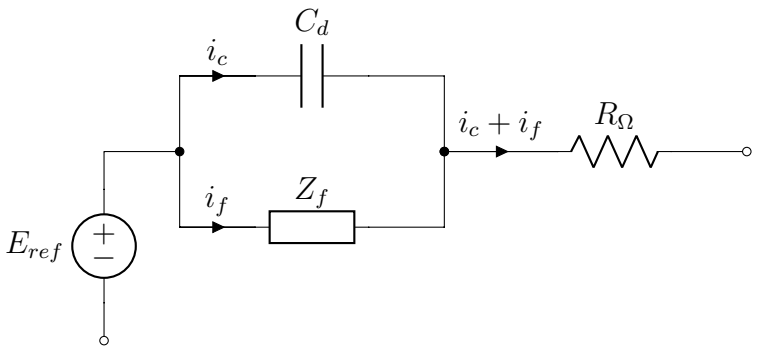


Figure 2.2 – Randles model of an electrode.

of this current depends on many factors and is generally complicated, but a simple model can be used in terms of an equivalent circuit involving a few impedance elements, called the Randles model [22], as shown in Figure 2.2.

The i_f current represents Faradaic current, caused by actual charge transfer between the electrode and the solution, where the Faradaic impedance Z_f combines effects such as the kinetics of the redox reaction, diffusion and mass transfer. The i_c current represents the transient current required to build up charges for an electrical double-layer of capacitance C_d at the surface of the electrode, similarly to the one discussed in section A.0.3. The electrolyte itself has a resistance R_Ω which is in series with the electrode. The half-cell potential would arise as an ideal voltage element placed in series with the Randles circuit, representing the offset required to achieve a zero current at equilibrium. We can gain some intuition about theoretical design constraints for a reference electrode. For example, in order to provide a fixed DC potential in the bulk, it is necessary that the series combination of the R_Ω and real part of Z_f be small enough so that the effect of other external sources of potential (with their own output impedances) is negligible. Thus there must be some resistive behavior in the electrode, which involves the transfer of ions between electrode and solution. This might be a concern for biocompatibility since the reference electrode would be in contact with blood, and should not contaminate it with foreign ions. On the other hand, an inert and purely capacitive electrode would not be able to maintain a fixed DC potential, but it could still affect higher frequency components of the bulk potential through the capacitive elements. It is worth noting that in a biological setting, there could be many external sources of biological potentials that cause the bulk potential of the blood to vary.

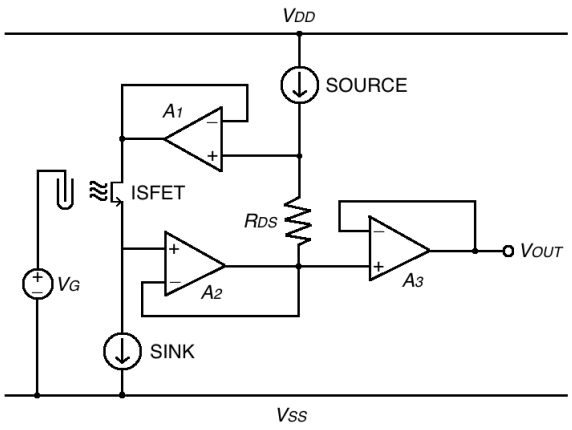


Figure 2.3 – Source-drain follower circuit, redrawn from [8].

2.4 Readout Circuits

The previous sections discussed the theory of operation for ISFETs. In this section, different readout circuits used to measure the electrolyte potential Ψ using electronic means will be discussed, such as source-drain followers, complementary ISFET/MOSFET pairs, floating gate structures, differential readout circuits and temperature-compensated readout circuits.

2.4.1 Source-drain follower

One common ISFET readout circuit is the source-drain follower, which uses constant current and constant voltage (CCCV) biasing of the ISFET through feedback. The basic structure is shown in Figure 2.3. There are two unity-gain opamps A_1 and A_2 that fix the drain-source voltage of the ISFET to be equal to the voltage drop across R_{DS}. The current through R_{DS} is fixed by the current source, and the current through the ISFET is fixed by the current sink. The output voltage will vary with variations of the threshold voltage V_T of the ISFET caused by pH variations.

2.4.2 Topologies avoiding the body effect

In a source-drain follower, the source terminal is connected to a feedback node and so it is generally not grounded. This can introduce problems involving the body effect discussed in section 2.1.3. Morgenshtein considered various readout circuits that avoid the body effect, by ensuring that the source terminal of n-type ISFETs is always grounded. One of the ideas was the use of a complementary ISFET/MOSFET pair (CIMP) together with an

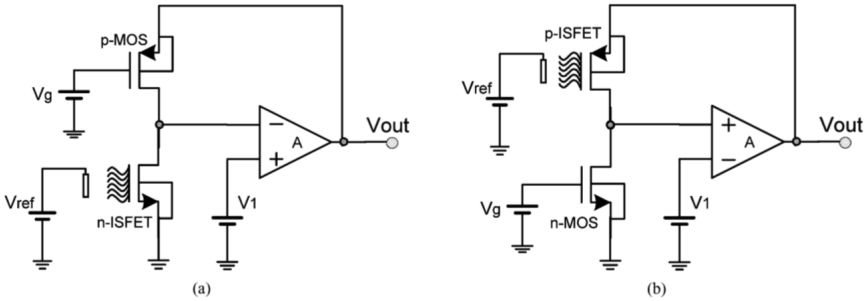


Figure 2.4 – Indirect (a) and direct (b) CIMP circuits from Morgenshtein *et al.* [6]. Reprinted with permission from Elsevier. Copyright © 2003 Elsevier B.V. All rights reserved.

op-amp in direct or indirect feedback configuration, where the feedback is applied either to the gate or source of the ISFET (direct feedback) or MOSFET (indirect feedback) [6]. The indirect and direct CIMP circuits with source feedback are shown in Figure 2.4. Based on Morgenshtein's analysis, assuming both transistors operate in saturation, the change in V_{out} tracks the change in threshold voltage V_T of the ISFET by the formula $\Delta V_{out} = -\Delta V_T$ (direct feedback) and $\Delta V_{out} = \Delta V_T/\sqrt{a}$ (indirect feedback) where a is a ratio of process-dependent quantities for the ISFET and MOSFET pair, that can be modified by sizing the transistors [6]. Morgenshtein also considered a readout circuit where the ISFET is part of a Wheatstone bridge, that can be used to double the sensitivity [33].

2.4.3 Using passivation layer and floating gate structures

Many research groups also worked on ISFET-based readout circuits where the floating gate structure is used and the sensing dielectric is part of the IC itself, using the passivation layer (see Figure 2.5). Most of these groups used the autriamicrosystems (AMS) 0.35 μm fabrication process, where the passivation layer is Si_3N_4, one of the common materials for pH sensing gates. Some examples include Milgrew [8] in 2007 and Hu and Georgiou [7] in 2014. The advantage of using the passivation layer as the sensing gate dielectric is that no additional processing steps are required, so that the design would be ready for large-scale production. However it was noted by Milgrew that the floating gate would contain some amount of trapped charge from the fabrication process which introduces a large random offset on the ISFET threshold voltage. The proposed solution was to expose the devices to ultraviolet (UV)

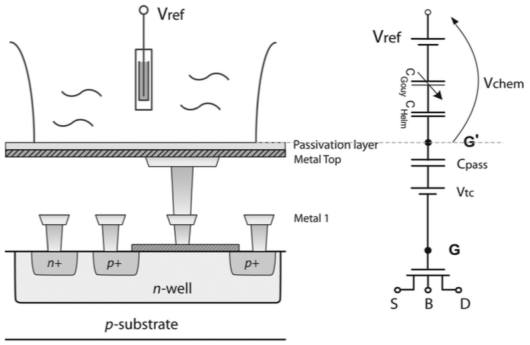


Figure 2.5 – Floating gate ISFET structure from Hu and Georgiou [7]. Reprinted with permission from IEEE. Copyright © 2014, IEEE.

light for 10 hours in order to remove the trapped charges [8]. In terms of the readout circuit, Hu and Georgiou also proposed a periodical resetting scheme which resets the gate voltage of the floating node to a fixed voltage in order to counter the effect of drift that caused it to increase over time. The measurements were then performed differentially, so that a voltage difference over the operating cycle is used to measure variations in pH [7].

2.4.4 Integration of reference electrode on chip

The most common implementation of a reference electrode is the Ag/AgCl glass electrode, which has a very stable potential over a large pH range. Another common option is a calomel (Hg_2Cl_2) electrode. However the main drawback of such electrodes is that they use an internal buffer solution separated by a glass membrane. The structure is very difficult to miniaturize, so it cannot be used for implantable devices. Various solutions to the problem have been proposed. One solution was proposed by Liao *et al.* involving on-chip gold deposition in the shape of octagonal rings to use as integrated reference electrodes [2]. They used a TSMC 0.35μm CMOS BioMEMS post-process with gold. The pH sensing gate was made from Al_2O_3 with a 250 μm diameter and was placed in the center of the octagonal gold reference electrodes, with the goal of providing a uniform electric field across the gate. Their sensor is shown in Figure 2.6. This design has the obvious advantage that it allows the entire pH sensor to be integrated in a small chip and be easily encapsulated. However it is not clear whether gold is a good material for the reference electrode, since it is a noble metal which implies very slow redox reactions and hence mostly capacitive behavior based on the theory of section 2.3. This solution could be more appropriate in the context of a

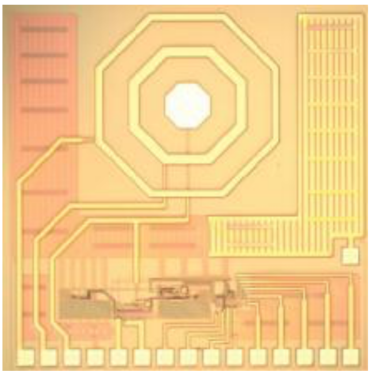


Figure 2.6 – Photograph of the ISFET and reference electrodes from Liao *et al.* [2]. Reprinted with permission from IEEE. Copyright © 2013, IEEE.

differential readout circuit as will be discussed next, because then the gold can be used as a pseudo-reference electrode instead.

2.4.5 Differential readout circuits and REFET

Another interesting solution involves the use of a differential readout circuit, where a second device similar to the ISFET is used whose gate material is insensitive to pH but is still sensitive to bulk potential. The resulting device provides a reference from which the pH-sensitive ISFET signal can be decoupled from the bulk potential to isolate the pH variation signal. Such devices have been called reference field-effect transistors (REFET). Although the ideal case would involve a completely pH-insensitive REFET, most gate materials will have some nonzero pH sensitivity anyways. It is possible to combine two ISFETs where the second ISFET has lower pH sensitivity, so that the net sensitivity in the differential readout is the difference in sensitivities between the two ISFETs. This idea was already proposed back in 1978 by Esashi and Matsuo in [9]. The bulk potential still needs to be controlled, but it can be done using a pseudo-reference electrode. A pseudo-reference electrode is usually made from a noble metal such as gold (Au) or platinum (Pt), and its potential is not necessarily constant with pH variations. However its variation is cancelled by the ISFET/REFET combination, so the effect is avoided. This allows an easier integration on a chip because small-scale deposition of gold is easier to achieve. Another attractive advantage of the REFET is that it can cancel out all common-mode sources of noise. Such sources might include bulk potential variations unrelated to pH, temperature variations, light intensity variation, or drift behavior that is identical in both ISFET and REFET.

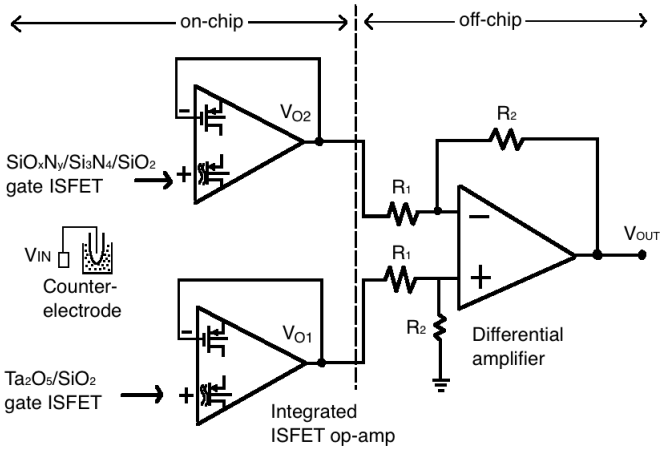


Figure 2.7 – Differential readout circuit from Wong and White, redrawn from [3].

This idea of combining two ISFETs with different sensitivities in a differential readout circuit was tried by Wong and White in 1989 [3]. They used two p-channel ISFETs with different pH sensitivity as parts of two separate operational amplifiers, and a gold counter electrode (or pseudo-reference electrode). The highly pH-sensitive ISFET used a Ta_2O_5/SiO_2 gate insulator structure, achieving a sensitivity of $58 - 59$ mV/pH. The pH-insensitive ISFET used a $SiO_xN_y/Si_3N_4/SiO_2$ gate with sensitivity of $18 - 20$ mV/pH. The two operational amplifiers were combined into an instrumentation amplifier to produce a difference reading as shown in Figure 2.7. The overall pH sensitivity of the circuit was $40 - 43$ mV/pH. They made use of careful matching of the ISFET/MOSFET pairs in the differential stage of each operational amplifier in order to improve common-mode rejection and reduce sensitivity to temperature and light.

In a different work in 1999, Errachid *et al.* [10] fabricated a REFET with a very low pH sensitivity of 1.8 mV/pH. To do this they used some post-processing techniques on an ISFET to reduce the number of reactive sites on the gate surface, and used non-blocking ion-insensitive membranes. They deposited PVC on a Si_3N_4 gate insulator that had undergone previous chemical processing to improve the adhesion of PVC and reduce the number of silanol (SiOH) sites on the gate surface. The PVC membrane acted as a diffusion barrier for protons to further reduce the pH sensitivity. Their readout circuit was similar to that of Wong and White [3], using two ISFET amplifiers followed by a differential amplifier. The overall pH sensitivity of their

system was 43.7 mV/pH. Sensitivity to other ions such as K^+ and Na^+ was less than 5 mV/pH. These results were obtained over a pH range of 2 to 9. This method has the advantage of maintaining a high pH sensitivity by avoiding too much subtraction from the differential readout circuit. However, additional processing steps to achieve the low pH sensitivity of the REFET, as well as the requirement for careful matching of devices to maintain identical transconductances, make the implementation difficult in practice for large-scale production.

2.4.6 Temperature compensation

If we recall equation (2.11), we observe that the relationship between electrolyte potential drop Ψ and bulk pH includes a linear temperature dependence, in addition to the temperature dependence of the sensitivity parameter α and $\mathrm{pH_{pzc}}$. For a nearly ideal material such as Ta_2O_5, the value of α remains approximately constant near 1. Ignoring also the temperature dependence of $\mathrm{pH_{pzc}}$, the temperature sensitivity can be expressed as

$$\frac{\partial \Psi}{\partial T} = -2.303 \frac{k_B}{q} (\mathrm{pH} - \mathrm{pH_{pzc}}) \tag{2.12}$$

The coefficient $-2.303\frac{k_B}{q}$ is approximately equal to -0.2 mV/°C $\cdot$ pH. If this is compared to the typical pH sensitivity of around 50 mV/pH, we see that a 1 °C increase in temperature with $\mathrm{pH} - \mathrm{pH_{pzc}} = 1$ corresponds to about 0.4% of the increase in Ψ due to pH. The effect is not very strong, particularly for environments where the temperature is well-regulated, such as in the human body. Nonetheless it is important to take into account its existence, and the fact that the temperature sensitivity may also increase due to the other neglected effects.

Temperature compensation may be achieved in different ways. One method is to bias the ISFET drain current in such a way as to minimize the temperature coefficient (the current for which the temperature coefficient is 0 is called the *athermal* or *isothermal* current). This biasing technique works if the pH does not vary too much, because the temperature coefficient is also pH-dependent in general. One example of this technique was proposed by Chin *et al.* [4]. In their analysis, they consider an ISFET in a constant current and constant voltage (CCCV) feedback configuration, where V_{DS} and I_{DS} are kept constant, and the ISFET operates in the triode (linear) region. In such a case, one can use equation (2.1) and differentiate with respect to T while keeping I_{DS} and V_{DS} constant. The implicit differentiation results

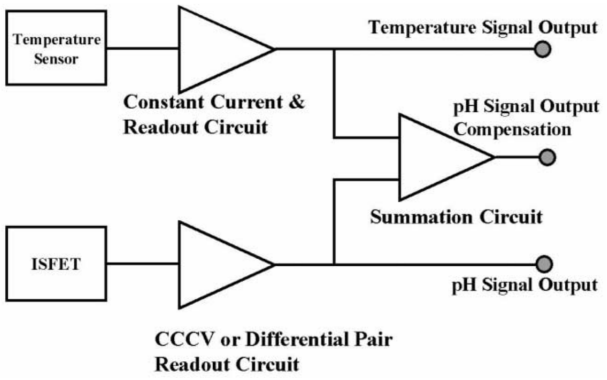


Figure 2.8 – Temperature compensation circuit from Chin *et al.* [4]. Reprinted with permission from Elsevier. Copyright © 2001 Elsevier Science B.V. All rights reserved.

in the relationship [4]:

$$\frac{\partial V_{GS}}{\partial T} = \frac{\partial V_T}{\partial T} + \frac{I_{DS}}{V_{DS}} \frac{\partial}{\partial T} \left(\mu_n C'_{ox} \frac{W}{L} \right)^{-1} \tag{2.13}$$

Hence given fixed process parameters for μ_n and C'_{ox} and fixed dimensions, it is possible to choose I_{DS} such that the sum of the two terms is zero, as long as it remains consistent with the requirement of biasing in the linear region (in particular the two terms on the right hand side must have opposite signs). However such a method will only work in a small pH range since the $\frac{\partial V_T}{\partial T}$ term depends on pH, so that different I_{DS} values are necessary for different pH values. In the same paper, Chin *et al.* also propose to combine this CCCV circuit with a temperature sensor obtained from a *pn* diode. The two circuit outputs are summed together (see Figure 2.8), resulting in a net output whose temperature coefficient is the sum of the two individual temperature coefficients. Due to the opposite signs of the temperature coefficients of the two circuits, it was possible to obtain a net reduced temperature dependence at the output. The ISFET had a temperature coefficient of 1.38 mV/°C and the diode had a temperature coefficient of −1.51 mV/°C, leading to a net temperature coefficient of 0.16 mV/°C [4].

It is also possible to eliminate or reduce the temperature dependence by using a differential readout circuit as mentioned in section 2.4.5. The ISFET will have to be electrically matched to a MOSFET, that is their transconductances will have to be close to each other. This was also discussed by Wong and White in [3].

2.4.7 Leakage in floating gate

One aspect that did not seem to be discussed in these works is the effect of leakage mentioned in section 2.1.2. Indeed, the trapped charge in the floating node is generally assumed to be constant, however the presence of leakage could cause it to slowly discharge and introduce another drift effect. It is possible that the process used in these works had sufficiently thick gate oxides for tunneling effects to be negligible, or that the time scales over which the pH measurements had to be performed were not large enough for the drift to manifest itself.

Chapter 3

System Components and Models

3.1 Introduction

In this chapter, the various components of the system diagram in Figure 1.3 will be described in more detail. The terminals of each block will be described, and models of the block's behavior will be provided. The discussion will be based on the theory provided in Chapter 2. The signal labels will be used consistently with the description of the readout circuits in Chapters 4-8.

3.2 Reference Electrode

Based on the theory of section 2.3 and Figure 2.2, the reference electrode can be modeled as an ideal voltage source E_{ref} in series with an impedance Z_{ref}. Knowledge of Z_{ref} requires details about the structure and materials of the reference electrode. However in this work the reference electrode is not yet fabricated and its properties remain unspecified. In order to simplify the

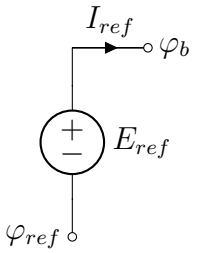


Figure 3.1 – Reference electrode circuit model.

following analysis, an idealized short-circuit model of the reference electrode will be considered as shown in Figure 3.1.

The short-circuit model neglects the impedance and connects φ_b directly to the ideal voltage source E_{ref}. This represents a reference electrode capable of maintaining a stable DC potential in the solution with all reactions and ion displacements occurring fast enough that they can be treated as instantaneous over the frequency range of interest. In the Randles model, we are setting $R_\Omega = 0$ and $Z_f = 0$. The resulting equation is given by:

$$\varphi_b = \varphi_{ref} + E_{ref} \tag{3.1}$$

In reality the behavior of the reference electrode will likely be nonlinear and more complex, and this model will only be valid for small-signal analysis at a specified operating point computed from a more general relationship between I_{ref}, φ_{ref} and φ_b. Moreover, if the reference electrode is made from an inert material such as gold, it is possible that the impedance Z_{ref} is not negligible.

The potential φ_{ref} represents the potential at the terminal of the reference electrode not in contact with the liquid. It will generally be grounded (so $\varphi_{ref} = 0$ V) but in the reference electrode feedback readout circuit, it will be connected to a feedback node. The potential φ_b represents the bulk potential of the solution. The voltage E_{ref} represents the potential drop of the electrode at equilibrium (i.e. when the chemical reactions lead to no net charge transfer so that $I_{ref} = 0$).

3.3 Electrolyte Solution

The electrolyte solution will introduce an electrical double-layer at the interface between the solution and the sensing dielectric, as discussed in section A.0.3. The double-layer is modeled by a series combination of a nonlinear capacitance C_d (diffuse layer) and linear capacitance C_h (Stern layer) as shown in Figure 3.2. The nonlinear capacitance C_d introduces a nonlinear relationship between the charge Q_d and the voltage $\varphi_h - \varphi_b$. The reader may refer to Figure A.2 for an illustration of the geometrical structure of this double-layer and the potentials. The Stern layer capacitance is given by multiplying equation (A.10) by the sensing area A:

$$C_h = AC'_h = A\frac{\varepsilon_0 \varepsilon_h}{x_h} \tag{3.2}$$

The model relates the various parameters as follows:

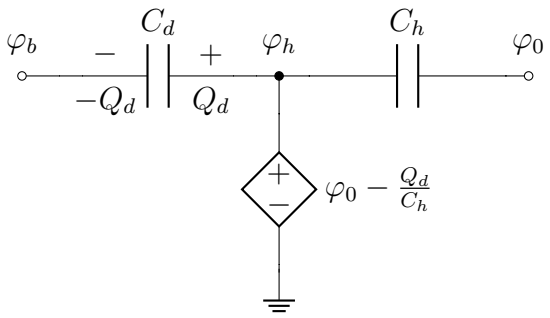


Figure 3.2 – Electrolyte double-layer circuit model.

$$Q_d = A\sqrt{8\varepsilon_0\varepsilon_b N_A k_B T c_0}\sinh\left[\frac{q(\varphi_h - \varphi_b)}{2k_B T}\right] \tag{3.3}$$

$$C_h(\varphi_h - \varphi_0) + Q_d = 0 \tag{3.4}$$

Equation (3.3) was obtained from equation (A.8) by multiplying by the sensing area A to convert surface charge densities to total charge (here $Q_d = -A\sigma_d$). This assumes that the geometry is sufficiently planar and that the charge density remains uniform across the sensing area. Equation (3.4) represents charge neutrality at the node φ_h (Helmholtz plane). The dependent voltage source ensures that $\varphi_h = \varphi_0 - \frac{Q_d}{C_h}$ to satisfy this neutrality condition. The terminals are φ_b (the bulk potential) and φ_0 (the potential at the surface of the sensing dielectric).

3.4 Sensing Dielectric

The sensing dielectric consists of a surface with dangling bonds that allows the accumulation of a surface charge density σ_0. The chemical reactions on the surface will depend on the material, and will cause the sensitivity to pH or to other ions. The theory of surface binding reactions was described in section A.0.1. Combining equations (A.5) and (A.7) we obtain the following relationship between the total surface charge $Q_0 = A\sigma_0$, the voltage $\varphi_0 - \varphi_b$ and the pH:

$$Q_0 = qN_s A\frac{\left[e^{-2.303\cdot\mathrm{pH}-\frac{q}{k_B T}(\varphi_0-\varphi_b)}\right]^2 - K_a K_b}{K_a K_b + K_b e^{-2.303\cdot\mathrm{pH}-\frac{q}{k_B T}(\varphi_0-\varphi_b)} + \left[e^{-2.303\cdot\mathrm{pH}-\frac{q}{k_B T}(\varphi_0-\varphi_b)}\right]^2} \tag{3.5}$$

In addition, the sensing dielectric will introduce a capacitance C_{sens} between the sensing surface and the ISFET floating gate. The circuit model of the sensing dielectric is therefore as shown in Figure 3.3.

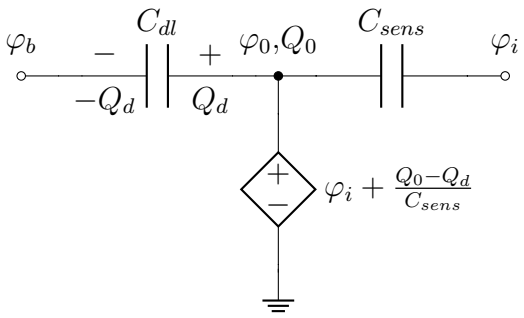


Figure 3.3 – Combined sensing dielectric and electrolyte circuit model.

It should be remarked that the electrolyte double-layer was also included because the surface charge Q_0 and the potential φ_0 depend on the voltage $\varphi_0 - \varphi_b$ and the charge Q_d. The nonlinear capacitance C_{dl} is the series combination of C_d and C_h from section 3.3. The linear capacitance C_{sens} represents the dielectric, and it satisfies

$$C_{sens} = A\frac{\varepsilon_0 \varepsilon_d}{x_d} \tag{3.6}$$

where ε_d is the relative dielectric permittivity and x_d is the thickness of the sensing dielectric. Finally, the dependent voltage source ensures that the total charge at the node φ_0 is equal to Q_0. This is achieved by forcing the relation $\varphi_0 = \varphi_i + \frac{Q_0 - Q_d}{C_{sens}}$ which may also be written in the charge conservation form:

$$Q_d + C_{sens}(\varphi_0 - \varphi_i) = Q_0 \tag{3.7}$$

The quantity Q_0 depends on $\varphi_0 - \varphi_b$ and pH by equation (3.5), and Q_d is given by equation (3.3). The terminal φ_i is the input to the ISFET (connected to the readout circuit) including the pad connections and wirebonds.

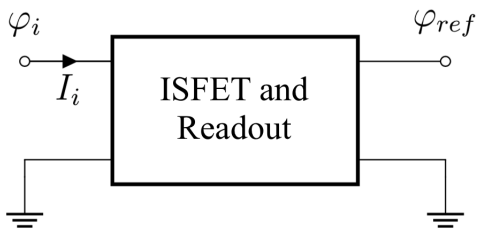


Figure 3.4 – Readout circuit model.

3.5 Readout Circuit

For the purposes of this chapter, the combination of ISFET and readout circuit will be represented as a two-port network with terminals φ_i and φ_{ref} as shown in Figure 3.4. The wirebonds, PCB connections, integrated circuit and ADC are all abstracted in the black box in order to focus on the interaction of the readout circuit with the ISFET frontend. Inside the readout circuit, the capacitors have very small area so it is expected that their size is negligible compared to the double-layer capacitance C_{dl} and the sensing dielectric capacitance C_{sens}. Therefore at the low frequencies of interest, the readout circuit can be assumed to contain only resistive components and to store negligible amounts of charge compared to the external solution.

The input φ_i of the ISFET and readout circuit is connected to switches or to the gate of an ISFET, so its input current I_i is expected to be very low, and any coupling of I_i to φ_{ref} will be neglected. The potential φ_{ref} will be used to control the reference electrode, and will either be grounded or depend on φ_i through a feedback network with low output resistance, much lower compared to that of the reference electrode's input resistance seen from terminal φ_{ref}. Therefore the readout circuit will be modeled as follows:

$$I_i = I_i(\varphi_i) \tag{3.8}$$

$$\varphi_{ref} = F(\varphi_i) \tag{3.9}$$

Here $I_i(\varphi_i)$ and $F(\varphi_i)$ are possibly nonlinear functions that depend only on the instantaneous value $\varphi_i(t)$. Ultimately, the digital reading of pH will be a function of the instantaneous value of $\varphi_i(t)$.

3.6 Complete Model of ISFET Frontend

The complete model of the ISFET frontend is shown in Figure 3.5. The external ports are φ_{ref} and φ_i which connect to the ISFET and readout

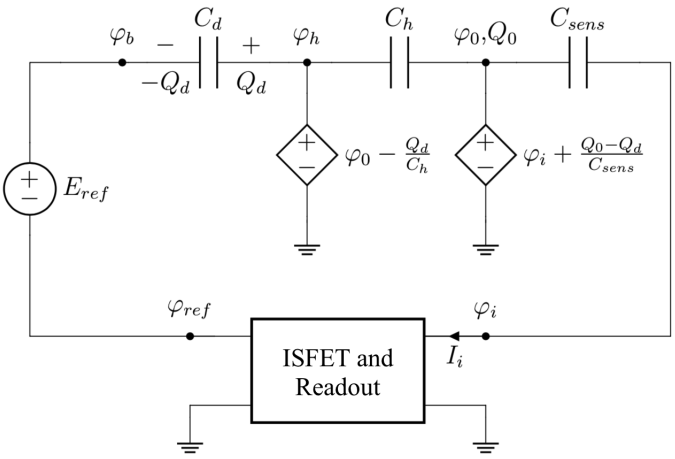


Figure 3.5 – ISFET frontend circuit model.

circuit. The potential φ_{ref} is provided by the readout circuit, either as ground or as a feedback output. The potential φ_i is the input to the ISFET and readout circuit. The following equations specify the mathematical model of the ISFET frontend:

$$\varphi_b = \varphi_{ref} + E_{ref} \tag{3.10}$$

$$Q_d = A\sqrt{8\varepsilon_0\varepsilon_b N_A k_B T c_0}\,\sinh\left[\frac{q(\varphi_h - \varphi_b)}{2k_B T}\right] \tag{3.11}$$

$$C_h(\varphi_h - \varphi_0) + Q_d = 0 \tag{3.12}$$

$$Q_d + C_{sens}(\varphi_0 - \varphi_i) = Q_0 \tag{3.13}$$

$$Q_0 = qN_s A \frac{\left[e^{-2.303\cdot\mathrm{pH} - \frac{q}{k_B T}(\varphi_0 - \varphi_b)}\right]^2 - K_a K_b}{K_a K_b + K_b e^{-2.303\cdot\mathrm{pH} - \frac{q}{k_B T}(\varphi_0 - \varphi_b)} + \left[e^{-2.303\cdot\mathrm{pH} - \frac{q}{k_B T}(\varphi_0 - \varphi_b)}\right]^2} \tag{3.14}$$

$$C_{sens}\frac{\mathrm{d}}{\mathrm{d}t}(\varphi_i - \varphi_0) + I_i(\varphi_i) = 0 \tag{3.15}$$

$$\varphi_{ref} = F(\varphi_i) \tag{3.16}$$

The capacitances C_h and C_{sens} are given by equations (3.2) and (3.6) respectively. There are seven equations involving the seven unknowns φ_b, φ_h, φ_0, φ_i, φ_{ref}, Q_d and Q_0, so the model is complete and every parameter may be calculated once I_i and F are substituted with explicit functions. The equation (3.15) will also require an arbitrary initial condition.

The model presented here allows the determination of the transient behavior for large signals. A small-signal model will be useful when designing the

readout circuits because the nonlinear equations are complicated and require numerical solutions. If the pH signal does not vary greatly, it is expected that the linearized equations will be sufficiently accurate. The small-signal model is developed in section 3.8.

The small-signal components will be defined relative to the initial values. Therefore, each signal φ will be decomposed in the form $\varphi(t) = \varphi^0 + \Delta\varphi(t)$, where $\varphi^0 = \varphi(0)$. The equations (3.10)-(3.16) can then be decomposed into initial conditions and small-signal components, which will be analyzed separately in the following sections.

3.7 Initial Conditions

The initial conditions satisfy the following equations:

$$\varphi_b^0 = \varphi_{ref}^0 + E_{ref} \tag{3.17}$$

$$Q_d^0 = A\sqrt{8\varepsilon_0\varepsilon_b N_A k_B T c_0}\sinh\left[\frac{q(\varphi_h^0 - \varphi_b^0)}{2k_B T}\right] \tag{3.18}$$

$$C_h(\varphi_h^0 - \varphi_0^0) + Q_d^0 = 0 \tag{3.19}$$

$$Q_d^0 + C_{sens}(\varphi_0^0 - \varphi_i^0) = Q_0^0 \tag{3.20}$$

$$Q_0^0 = qN_sA\frac{\left[e^{-2.303\cdot \mathrm{pH}^0 - \frac{q}{k_BT}\left(\varphi_0^0 - \varphi_b^0\right)}\right]^2 - K_aK_b}{K_aK_b + K_be^{-2.303\cdot \mathrm{pH}^0 - \frac{q}{k_BT}\left(\varphi_0^0 - \varphi_b^0\right)} + \left[e^{-2.303\cdot \mathrm{pH}^0 - \frac{q}{k_BT}\left(\varphi_0^0 - \varphi_b^0\right)}\right]^2} \tag{3.21}$$

$$\varphi_{ref}^0 = F(\varphi_i^0) \tag{3.22}$$

The value of φ_i^0 is arbitrary and will be set by the readout circuit to a known value chosen to properly bias the circuit. Once pH^0 and φ_i^0 are given, the remaining initial conditions can be calculated by solving the system of equations.

3.8 Small-Signal Model

By taking Taylor expansions around the initial values up to first order, and applying the equations from the previous section, we obtain the following linearization of equations (3.10)-(3.16):

$$\Delta\varphi_b = \Delta\varphi_{ref} \tag{3.23}$$

$$\Delta Q_d = C_d(\Delta\varphi_h - \Delta\varphi_b) \tag{3.24}$$

$$C_h(\Delta\varphi_h - \Delta\varphi_0) + \Delta Q_d = 0 \tag{3.25}$$

$$\Delta Q_d + C_{sens}(\Delta\varphi_0 - \Delta\varphi_i) = \Delta Q_0 \tag{3.26}$$

$$\Delta Q_0 = -qA\beta_{int}\left[\Delta\mathrm{pH} + \frac{q}{2.303k_BT}(\Delta\varphi_0 - \Delta\varphi_b)\right] \tag{3.27}$$

$$C_{sens}\frac{\mathrm{d}}{\mathrm{d}t}(\Delta\varphi_i - \Delta\varphi_0) + I_i^0 + \frac{\Delta\varphi_i}{R_i} = 0 \tag{3.28}$$

$$\Delta\varphi_{ref} = K\Delta\varphi_i \tag{3.29}$$

The linear capacitance C_d is given by multiplying equation (A.9) by the sensing area A:

$$C_d = qA\sqrt{\frac{2\varepsilon_0\varepsilon_b N_A c_0}{k_BT}}\cosh\left[\frac{q(\varphi_h^0 - \varphi_b^0)}{2k_BT}\right] \tag{3.30}$$

The intrinsic buffer capacity β_{int} was defined by equation (A.13) and can be calculated from the DC operating point using equation (A.14) combined with equation (A.7) using the initial values of pH^0, φ_b^0 and φ_0^0. The DC input current I_i^0 is given by $I_i^0 = I_i(\varphi_i^0)$ and the input resistance R_i is given by $R_i = [I_i'(\varphi_i^0)]^{-1}$. Similarly, the value of K is given by $K = F'(\varphi_i^0)$.

3.9 Time Evolution Equation for $\Delta\varphi_i$

After eliminating all variables except for $\Delta\varphi_i$ and $\Delta\mathrm{pH}$ in the linearized model, it is possible to obtain the following first order linear ODE for $\Delta\varphi_i$ and $\Delta\mathrm{pH}$:

$$\frac{\mathrm{d}\Delta\varphi_i}{\mathrm{d}t} + \frac{\Delta\varphi_i}{\tau} = -S_i\frac{\mathrm{d}\Delta\mathrm{pH}}{\mathrm{d}t} - \frac{R_iI_i^0}{\tau} \tag{3.31}$$

The time constant τ is given by:

$$\tau = \frac{(1-K)R_iC_{sens}}{1 + (1-\alpha)\frac{C_{sens}}{C_{dl}}} \approx (1-K)R_iC_{sens} \tag{3.32}$$

The pH-sensitivity S_i of φ_i is given by:

$$S_i = 2.303\frac{k_BT}{q}\frac{\alpha}{1-K} \tag{3.33}$$

In these equations, $C_{dl} = \frac{C_dC_h}{C_d+C_h}$ is the series combination of the diffuse and Stern layer capacitances, and α is the sensitivity parameter from equation (A.17).

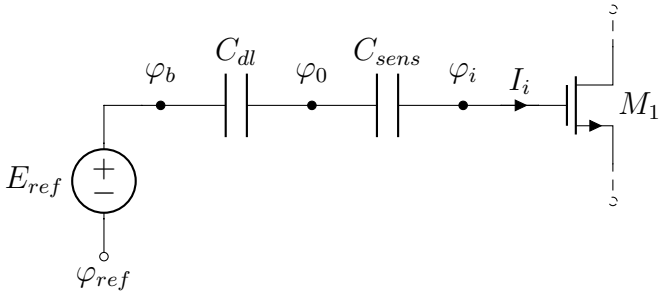


Figure 3.6 – Floating gate ISFET structure.

3.10 Analysis of Solutions

In order to investigate the evolution of $\Delta\varphi_i$ over time with ΔpH, we consider a sinusoidal pH input signal:

$$\Delta\mathrm{pH}(t) = A_{\mathrm{pH}} \sin(\omega t) \tag{3.34}$$

The solution of equation (3.31) for $\Delta\varphi_i(t)$ is given by:

$$\Delta\varphi_i(t) = -\frac{S_i}{\sqrt{1+\frac{1}{\omega^2\tau^2}}}\Delta\mathrm{pH}(t+t_d) + \frac{A_{\mathrm{pH}}S_i}{\omega\tau+\frac{1}{\omega\tau}}e^{-t/\tau} - \left(1-e^{-t/\tau}\right)R_i I_i^0 \tag{3.35}$$

where $t_d = \frac{1}{\omega}\arctan\left(\frac{1}{\omega\tau}\right)$ is a time shift (it can be positive without violating causality since the signal is periodic).

The solution involves a steady-state component that oscillates at the same frequency as the pH signal, with an amplitude scaled by a frequency-dependent factor which approaches S_i for $\omega\tau \gg 1$. There is also a frequency-dependent time shift t_d which approaches 0 for $\omega\tau \gg 1$, and the oscillation is inverted due to the presence of the negative sign. In order to minimize the time shift and amplitude distortion over the frequency range, it is desirable that $\omega\tau \gg 1$. The pH signal is known to oscillate as a superposition of frequencies bounded by $0 < \omega_{min} \leq \omega \leq \omega_{max}$, so that we should have $\tau \gg \frac{1}{\omega_{min}}$.

There is also a transient component caused by the initial conditions which decays exponentially with the time constant τ. In order to avoid noticeable drift over the time of operation t_{max}, it is also desirable that $\tau \gg t_{max}$, so that the transient term stays essentially constant. Finally, the last term is another transient component arising from the drift caused by having a nonzero input current I_i^0. This term will cause an approximately linear drift over time as long as $t \ll \tau$, after which it converges to an offset of $-R_i I_i^0$.

In order for the system to be stable, τ must be positive, so K must satisfy $K < 1$. In order to have τ as large as possible, we need to maximize $(1-K)R_iC_{sens}$. Different ways to achieve this will be considered in the readout circuits described in the next chapters. In the simplest case, the reference electrode is grounded and $K = 0$. The time constant is then R_iC_{sens}, and it is limited by the maximal achievable input resistance of the circuit. Since during sampling of the signal, the input must connect to the gate of a MOSFET, R_i will be limited by the tunneling current through the gate (see Figure 3.6). We see that the gate leakage introduces a loading effect, causing reduced pH sensitivity and increased phase shift at low frequencies, and causing drift from the exponentially decaying transient. The transient effect is intuitively caused by the leakage of charge stored in the floating node.

3.11 Limiting Behavior as $\tau \to \infty$

3.11.1 Fixing $K = 0$ and $R_i \to \infty$, $I_i^0 \to 0$

We will be interested in the limiting behavior of $\Delta\varphi_i$ as $R_i \to \infty$ and $I_i^0 \to 0$, representing the ideal case of a circuit with infinite input resistance and zero leakage current. The reference electrode is grounded so $K = 0$. We will use $S_i = 2.303\frac{k_BT}{q}\alpha$ from equation (3.33), and from equation (3.32) it also follows that $\tau \to \infty$. Then we analyze each component in equation (3.39) separately:

$$\lim_{R_i\to\infty} -\frac{S_i}{\sqrt{1+\frac{1}{\omega^2\tau^2}}}\Delta\mathrm{pH}(t+t_d) = -2.303\frac{k_BT}{q}\alpha\Delta\mathrm{pH}(t) \tag{3.36}$$

$$\lim_{R_i\to\infty} \frac{A_{\mathrm{pH}}S_i}{\omega\tau+\frac{1}{\omega\tau}}e^{-t/\tau} = 0 \tag{3.37}$$

$$\lim_{\substack{R_i\to\infty\\ I_i^0\to 0}} -\left(1-e^{-t/\tau}\right)R_iI_i^0 = \lim_{\substack{\tau\to\infty\\ I_i^0\to 0}} -\tau\left(1-e^{-t/\tau}\right)\frac{I_i^0}{C_{sens}} = 0 \tag{3.38}$$

We see that in the ideal case where $R_i \to \infty$ and $I_i^0 \to 0$, the input $\Delta\varphi_i$ varies according to:

$$\Delta\varphi_i(t) = -2.303\frac{k_BT}{q}\alpha\Delta\mathrm{pH}(t) \tag{3.39}$$

Therefore, if the process parameters can be improved sufficiently to have infinite input resistance and zero leakage current, the input φ_i tracks pH linearly with the sensitivity reported in equation (A.16) from the literature.

3.11.2 Fixing R_i and I_i^0 while $K \to -\infty$

When analyzing the reference electrode feedback readout circuit, it will be assumed that R_i and I_i^0 cannot be improved, so that the only way to increase τ is by letting $K \to -\infty$. Now we have $\tau \to \infty$ again, but since $S_i = 2.303\frac{k_B T}{q}\frac{\alpha}{1-K}$, the pH-sensitivity of $\Delta\varphi_i$ goes to 0. It will therefore be necessary to measure $\Delta\varphi_{ref} = K\Delta\varphi_i$ instead. We have $\lim\limits_{K\to-\infty} KS_i = -2.303\frac{k_B T}{q}\alpha$, so the pH-sensitivity of $\Delta\varphi_{ref}$ is nonzero. We analyze again each component in equation (3.39) separately, multiplied by K:

$$\lim_{K\to-\infty} -K\frac{S_i}{\sqrt{1+\frac{1}{\omega^2\tau^2}}}\Delta\text{pH}(t+t_d) = 2.303\frac{k_B T}{q}\alpha\Delta\text{pH}(t) \tag{3.40}$$

$$\lim_{K\to-\infty} K\frac{A_{\text{pH}}S_i}{\omega\tau+\frac{1}{\omega\tau}}e^{-t/\tau} = 0 \tag{3.41}$$

$$\lim_{K\to-\infty} -K\left(1-e^{-t/\tau}\right)R_i I_i^0 = \lim_{\tau\to\infty}\tau\left(1-e^{-t/\tau}\right)\frac{I_i^0}{C_{sens}} = \frac{I_i^0}{C_{sens}}t \tag{3.42}$$

We see that in the ideal case where $K \to -\infty$, the signal $\Delta\varphi_{ref}$ varies according to:

$$\Delta\varphi_{ref}(t) = 2.303\frac{k_B T}{q}\alpha\Delta\text{pH}(t) + \frac{I_i^0}{C_{sens}}t \tag{3.43}$$

It is important to observe the presence of the drift term with coefficient $\frac{I_i^0}{C_{sens}}$. Since it was assumed that the leakage current could not be reduced to zero by process improvements, the only way to reduce this coefficient will be to choose an initial value φ_i^0 such that $I_i(\varphi_i^0) = 0$, which requires precise biasing. This will be discussed further in section 7.1.1 when analyzing the reference electrode feedback readout circuit.

3.12 ISFET Model in Spectre

For simulation purposes, a model of the electrochemical interface involved in the ISFET had to be made. Work on ISFET models has been undergone by various researchers, one early example being the work of Grattarola *et al.* in 1992 [21]. They developed a built-in model of the ISFET in SPICE, however it required a modified version of SPICE called BIOSPICE. Martinoia and Massobrio later published an ISFET behavioral macromodel for SPICE in source code [34]. The model used in this thesis was adapted from this model, rewritten to be compatible with the `veriloga` syntax of the Spectre simulator

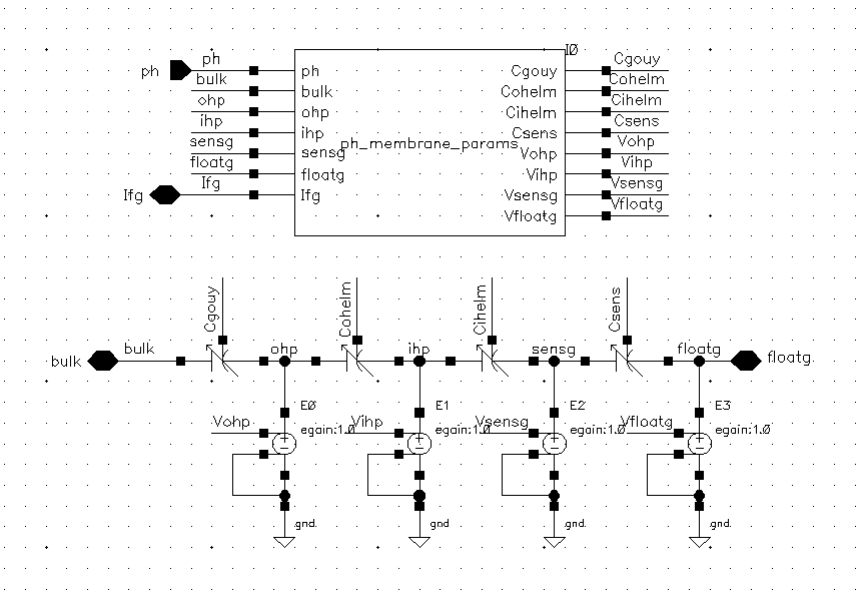


Figure 3.7 – Schematic of ISFET interface in Cadence. The `bulk` is φ_b, `sensg` is φ_0 and `floatg` is φ_i.

available in Cadence Virtuoso. The equations provided in section 3.6 were used. However equation (3.15) was rewritten in integral form as:

$$C_{sens}(\varphi_i - \varphi_0) = Q_i^0 - \int_0^t I_i(\varphi_i(t'))\mathrm{d}t' \tag{3.44}$$

The parameter $Q_i^0 = C_{sens}(\varphi_i^0 - \varphi_0^0)$ represents the initial charge stored in the capacitor C_{sens}. The current I_i appearing in equation (3.48) is given as an input to the Spectre macromodel, and is provided by a current-controlled voltage source (CCVS) at the schematic level. This component measures the current going into the input of the readout circuit, and converts it to a "voltage" value used in the Spectre model for numerical calculations. The capacitors modeling the electrochemical double layer and the sensing dielectric are included at the schematic level, and their capacitances are controlled by the calculations of the `veriloga` source code. Hence there is a tight interaction between the `veriloga` model and the schematic model which instantiates it, shown in Figure 3.7.

The source code for the ISFET model in Spectre is shown in Appendix C. The source code used values for a Si_3N_4 gate in order to compare with the results in [34]. Simple modifications can be made to obtain the model for Ta_2O_5. It should also be mentioned that the model uses a formulation where the Helmholtz plane is separated into the outer Helmholtz plane (OHP)

Parameter	Value	Description
N_A	$6.022 \cdot 10^{23}$ mol^{-1}	Avogadro's constant
k_B	$1.38 \cdot 10^{-23}$ J/K	Boltzmann's constant
ε_0	$8.85 \cdot 10^{-12}$ F/m	Permittivity of free space
q	$1.602 \cdot 10^{-19}$ C	Elementary charge
T	310 K	Temperature
c_0	0.1 mol/L	Ionic concentration in bulk
x_h	0.4 nm	Thickness of Helmholtz layer
x_d	10 nm	Thickness of sensing dielectric
A	400 μm $\times$ 400 μm	Area of sensing dielectric
Q_i^0	0 C	Initial charge stored in C_{sens}
ε_b	78.5	Relative permittivity of bulk
ε_h	32	Relative permittivity of Helmholtz layer
ε_d	7.5 / 22	Relative permittivity of dielectric (Si_3N_4 / Ta_2O_5)
N_s	$3.0 \cdot 10^{18}$ m^{-2} / 10^{19} m^{-2}	Number of silanol binding sites (Si_3N_4 / Ta_2O_5)
K_a	15.8 / 10^{-2}	Positive dissociation constant (Si_3N_4 / Ta_2O_5)
K_b	$63.1 \cdot 10^{-9}$ / 10^{-4}	Negative dissociation constant (Si_3N_4 / Ta_2O_5)

Table 3.1 – ISFET model parameters.

and inner Helmholtz plane (IHP) with their capacitances in series. Their permittivities are identical and the parameter x_h below is the sum of the thicknesses of the OHP and IHP. The equation (3.14) is also modified to include a term representing another type of binding sites mentioned at the end of section A.0.1.

The values of the various constants and parameters used in the models are shown in Table 3.1. The values for Si_3N_4 were obtained from [34] and the values for Ta_2O_5 were obtained from [35]. Using these values, we can provide estimates of the capacitances C_{dl} and C_{sens}. The value of $C_{dl} = AC'_{dl}$ is found from equations (A.9), (A.10) and (A.11), and the value of C_{sens} is found using $C_{sens} = A\frac{\varepsilon_0\varepsilon_d}{x_d}$. It is assumed that $\varphi_h = \varphi_b$, near the point-of-zero-charge. The obtained values are $C_{dl} = 56.6$ nF and $C_{sens} = 1.062$ nF for Si_3N_4, $C_{sens} = 3.12$ nF for Ta_2O_5. The thickness of 10 nm is already fairly small, and the dimensions of 400 μm $\times$ 400 μm are also close to the maximal size that can be used for implantable devices.

In the schematic above, the terminal `bulk` corresponds to node φ_b, `sensg` corresponds to φ_0 and `floatg` corresponds to φ_i. It should be noted that the reference electrode is not modeled explicitly, instead the model takes the bulk potential φ_b as a parameter, directly controlled by the simulations, which was set to 0 V. This can be seen as using the short-circuit model of the reference electrode and setting $E_{ref} = 0$ V while grounding φ_{ref}.

The ISFET model was verified by comparing it with the results shown in the plot of Fig. 4 in [34] for Si_3N_4, and the results agree closely with our

simulations. The plot in Figure 3.8 shows $\Psi = \varphi_0 - \varphi_b$ (or just φ_0 since $\varphi_b = 0$ V) with respect to pH values from 2 to 12. As in [34], the value of Ψ goes from 0.3 V at pH of 2 to -0.2 V at pH of 12. The slope is negative here while it is positive in [34] because they plotted $\varphi_b - \varphi_0$ instead. The potentials at the OHP and IHP are also shown as φ_{ohp} and φ_{ihp} respectively. The potential φ_i is also shown, but it is equal to φ_0 due to $Q_i^0 = 0$ C. The sensitivity of this Si_3N_4 is shown to be 54.9 mV/pH, which is typical. A simulation of the Ta_2O_5 sensing dielectric is shown in Figure 3.9. It is seen that the sensitivity is 58.8 mV/pH, again typical for this material.

Based on the simulations in Figures 3.9 and 3.8, it was decided that the sensing elements would use tantalum pentoxide (Ta_2O_5), due to its generally superior properties regarding sensitivity and linearity. The sensitivity of Ta_2O_5 is reported to go up to 58 mV/pH at room temperature, however a conservative estimate of 50 mV/pH was used during the design phase, since empirical data will not be available until the sensing elements are fabricated and tested. Note that the sensitivity here refers to that obtained with a grounded reference electrode, so that $K = 0$ in equations (3.33) and (3.37). It is a property of the material and temperature, given by $S = 2.303\frac{k_B T}{q}\alpha$.

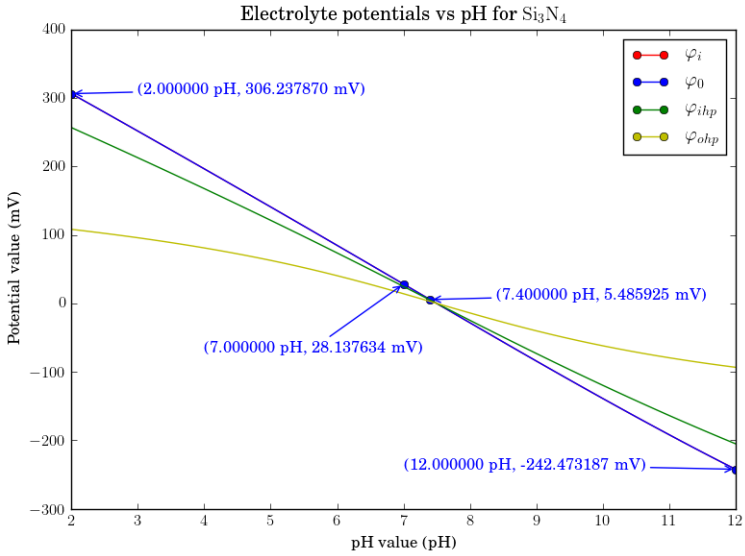


Figure 3.8 – DC sweep of pH from 2 to 12 with Si_3N_4, $N_{sil} = 3.0 \cdot 10^{18}$ m^{-2}, $N_{nit} = 2.0 \cdot 10^{18}$ m^{-2}.

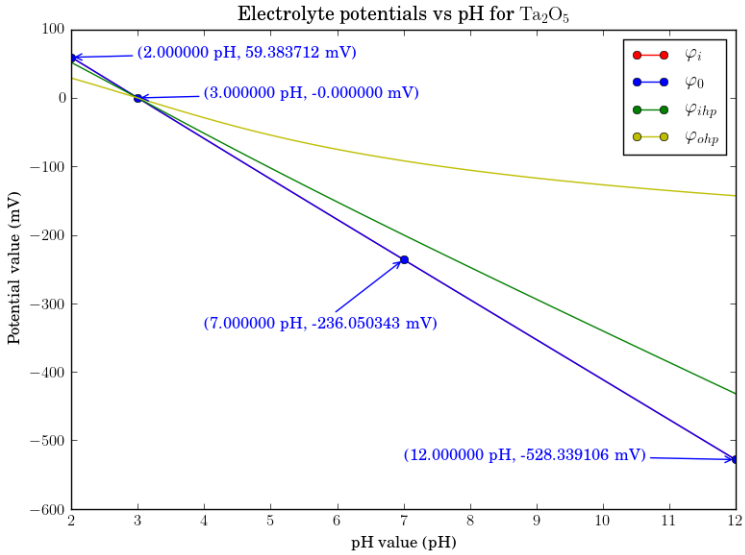


Figure 3.9 – DC sweep of pH from 2 to 12 with Ta_2O_5, $N_{sil} = 10 \cdot 10^{18}$ m^{-2}, $N_{nit} = 0$ m^{-2}.

Chapter 4

Specifications and Proposed Designs

4.1 Project Specification and Constraints

From this point and onwards in the thesis, the readout circuit is meant to refer both to the ISFET and the reader circuit to read the ISFET with the rest of the components on the IC. The ISFET-based pH sensor designed for this thesis is meant for a medical application where continuous pH monitoring over 48 hours is required. The device should be able to measure pH up to a resolution of 0.1 pH with a range between 6 and 8 pH, which is the normal range for human blood. In addition, its response time should be in the order of a second. Since the pH of the blood changes very slowly, it is not essential to track signal frequencies above 1 Hz. The sensor should operate at a body temperature of around 37 °C (310 K). Since the human body temperature is generally well-regulated, significant temperature variations are not expected. However the sensor would initially be stored at room temperature.

The readout circuitry for the sensor is designed with the commercial TSMC 65nm fabrication process available to the university through CMC, and has an allocated area of 1.5 mm $\times$ 1.5 mm. The TSMC 65nm process includes 9 metallization layers and aluminum pads on the BEOL. In particular, the ISFET structure must be of the floating gate type, since the MOSFET gates must be connected to metal stacks and vias to input pads. The sensing gate and reference electrode will be fabricated on a separate chip and connected to the MOSFET gates by wirebonding. This thesis only focuses on the readout circuit, and the design of the sensing elements and reference electrode will be completed in future work. To clarify, all the designs discussed in the following sections include op-amp building blocks, and the ISFET is

Resolution	0.1 pH
Range	6 - 8 pH
Signal frequency	1 μHz - 1 Hz
Operation time	48 hours
Input pH sensitivity	50 mV/pH
Temperature	37 °C
Fabrication process	TSMC 65nm
Chip area	1.5 mm × 1.5 mm

Table 4.1 – Design specifications and constraints.

part of the op-amps, as one of the transistors in the input differential pair (see section 10).

The design of the electronic circuit was done with the commercial Cadence Virtuoso program, and device models provided by the TSMC 65nm process design kit (PDK). Simulations used the Spectre circuit simulator provided as part of the Cadence design tools. It was decided that the first iteration of the circuit would only provide an analog output, so that no ADC integration is necessary.

In order to achieve a resolution of 0.1 pH, it is necessary that the measurement error for the input voltage does not exceed 2.5 mV over all operating conditions. The various design constraints and specifications are summarized in Table 4.1.

4.2 Proposed Readout Schematics

As discussed in section 3.5, the pH is measured by tracking the value of φ_i, which is proportional to pH (up to a constant offset) in the ideal case that $\omega\tau \to \infty$ according to equation (3.39). The output will then need to be sampled by an analog-to-digital converter (ADC) in order to compute the final pH values. The ADC is off-chip for the first iteration of the sensor.

The simplest circuit that can achieve a high input impedance and sufficiently low output impedance for external voltage measurements is a voltage buffer, where the gain is 1 V/V. It is possible to introduce a higher voltage gain, however this is not required unless there are specific constraints on the input range of the ADC. The signal-to-noise ratio (and pH resolution) do not improve with additional gain, since this depends mainly on the input-referred noise of the op-amp. Another possibility would be to use a transconductance amplifier where the output signal is a current instead of a voltage. However, such transconductances are generally process-dependent and more difficult to

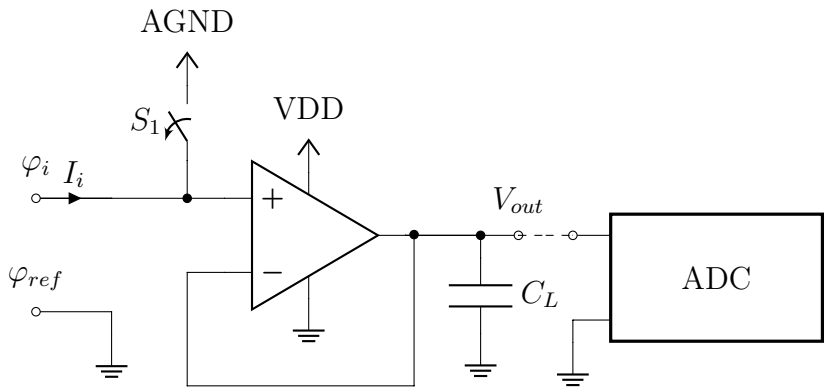


Figure 4.1 – Buffer readout circuit.

control. Moreover, the ADC would have to sample current instead of voltage. In any case, this would not help increase τ. The possibility of connecting φ_i directly to an ADC was also considered, and it could work provided that an ADC with an input resistance as high as estimated in section 10.1 is available. This would be the simplest possible readout circuit. But for the purposes of this research, no assumptions were made on the availability of such ADCs.

Based on these considerations, the most basic circuit that can be designed to achieve the desired operation is shown in Figure 4.1. The buffer output V_{out} will simply track φ_i with a lower output impedance. With this structure, the pH-sensitive surface is decoupled from the circuit through C_{sens}, and the transistor M_1 from Figure 3.6 is one of the transistors in the input differential pair of the op-amp, similarly to what was shown in Figure 2.7 from Wong and White's paper.

In this circuit as well as the following ones, the op-amps are not assumed ideal, so they may have a finite gain, nonzero voltage offset, finite input impedance and nonzero output impedance. In addition, the positive input of the op-amp is technically floating in these diagrams. In reality there needs to be some DC biasing, which could be set by initial conditions or by connecting a known voltage source to the node through the switch S_1 closed at time $t = 0$. This will be discussed in section 5.1.

The next idea that can be implemented is a simple modification of the circuit in Figure 4.1, where the positive input of the op-amp is connected to φ_i through a low-leakage switch S_2 as shown in Figure 4.2. The purpose of the S_2 switch will be to let the input impedance of the circuit be as large as possible most of the time. The switch will be closed for short amounts of time during measurements, and will remain open the rest of the time. The charge leakage effect will then only accumulate during the measurement periods, so

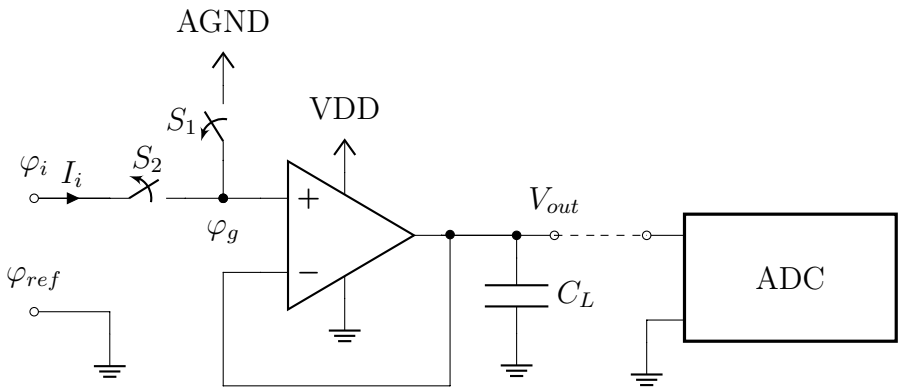


Figure 4.2 – Switch and buffer readout circuit.

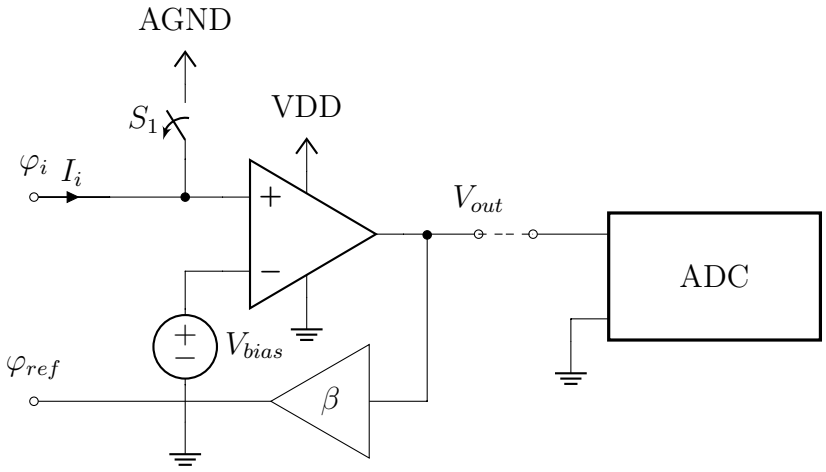


Figure 4.3 – Reference electrode feedback readout circuit.

the drift caused by this leakage can hopefully be reduced. The assumption is that the open switch will have much larger impedance than the op-amp's own input impedance.

Finally, a third design was considered under the hypothesis that neither the op-amp's nor the switch's input impedance can be ensured sufficiently high as to avoid loading effects at low frequencies. This design makes use of the reference electrode to provide feedback, instead of applying the feedback at the negative input of the op-amp. This design is shown in Figure 4.3. The feedback network includes an amplifier with gain β which can be used to tune the overall relationship between V_{out} and pH.

It is also possible to combine two identical readout circuits in a differential readout configuration using and ISFET/REFET pair in order to remove sen-

sitivity to the common mode noise of the reference electrode. The differential readout circuit will be discussed further in Chapter 8.

4.3 Motivation for Proposed Designs

The topologies discussed in section 4.2 are essentially the only ones that need to be considered. Indeed, the conclusions of section 3.10 apply to a fairly general class of readout circuits satisfying the assumptions stated in section 3.5. It was determined that the input to the readout circuit, namely φ_i, varies proportionally to the pH of the solution as long as the time constant τ satisfies $\tau \gg \frac{1}{\omega_{min}} = \frac{1}{2\pi f_{min}}$ and $\tau \gg t_{max}$. From the design constraints in Table 4.1, the values are $f_{min} = 1$ μHz and $t_{max} = 48$ hours. Hence the readout circuit must be designed to have $\tau > 48$ hours. It was determined that to maximize τ, one must maximize $(1-K)R_iC_{sens}$. The value of C_{sens} is limited by geometric constraints, and cannot be increased much. Therefore, it is necessary to tune the values of R_i and/or K.

If the MOSFET gate tunneling current and the leakage current through S_1 are both negligible, so that R_iC_{sens} is already large enough, then K can be set to 0 (grounding the reference electrode) and the buffer can be directly connected to φ_i. We then obtain the simplest possible topology which is the buffer readout circuit from Figure 4.1.

If either the tunneling current of the MOSFET or the leakage current through S_1 is non-negligible, we can try to increase R_i by adding another switch S_2 in series at the input φ_i. During most of the time, the switch will be open and R_i will be maximized. During measurements, the switch will be closed for short periods of time to connect the buffer's input node φ_g to φ_i and sample its value. It is assumed that S_2 will have a sufficiently large open resistance so that K can again be set to 0. The simplest topology achieving this is the switch and buffer readout circuit from Figure 4.2.

Finally, if R_iC_{sens} simply cannot be increased sufficiently, we can try to increase τ by modifying the value of the factor $1 - K$. This is achieved by connecting φ_{ref} to φ_i through a feedback network. Any point in the middle of the loop can be chosen as V_{out} to be sampled by the ADC, so in general we can have an amplifier with gain A between φ_i and V_{out}, and a feedback network with gain β between V_{out} and φ_{ref}. The value of K should be negative for this factor to be larger than 1, and it will be obtained as the product of the amplifier's gain A and the feedback network gain β, so that $K = A\beta$. The reference electrode feedback readout circuit from Figure 4.3 is the simplest topology that uses this idea. A summary of the considerations mentioned here is given in Table 4.2.

Buffer (Figure 4.1)	$\tau = R_i C_{sens}$	Input resistance of MOSFET and S_1 must be high.
Buffer and switch (Figure 4.2)	$\tau = R_i C_{sens}$	Improves R_i, but open resistance of S_2 must be high.
Reference electrode feedback (Figure 4.3)	$\tau = (1 - K) R_i C_{sens}$	Increases $1 - K$.
Differential with buffer (Figure 8.2)	$\tau = R_i C_{sens}$	Common mode noise reduction.

Table 4.2 – Comparison of proposed topologies.

The use of the op-amp building blocks can be justified by various reasons. First, they can eliminate most common-mode sources of noise such as temperature variation and power supply variation, assuming the differential pairs in the op-amps are sufficiently well matched. Second, they allow an easily controllable transfer function to be produced by the use of passive components in feedback networks. The parameters of passive components such as resistors and capacitors are usually better controlled than those of transistors. This also addresses the concerns regarding the body effect discussed in section 2.4, as the body effect affects transistors inside the op-amp but does not affect the passive devices in a feedback network. Finally, the linearity of op-amps in feedback networks is generally controlled by the passive feedback elements, and the op-amp design must mostly concern itself with maintaining a large gain over the desired frequency range, remaining stable in a closed-loop circuit and having low input-referred noise. A linear relationship between input and output reduces the number of degrees of freedom that must be accounted for during device calibration, so it is a desirable property.

4.4 The DC Biasing Problem

For any of the considered readout circuits, the node at φ_i is connected to a capacitor C_{sens} and to the high input impedance of the readout circuit. Therefore it is essentially floating, and its DC value is uncertain. In principle, the capacitors will have some initial conditions related to the stored charge at time $t = 0$. The voltage of node φ_i will also converge after some time to some value determined by process-dependent details of the input MOSFET, such that the input current I_i becomes zero. But this voltage will be difficult

to predict and control, and might not correspond to an acceptable DC bias for the op-amp.

Another alternative is to short the floating node φ_i to a known voltage source that will bias the circuit. The voltage should be selected for optimal performance of the op-amp. Implementing this solution requires the use of the switch S_1 which will have high resistance in the open configuration. The initial condition will be given by $\varphi_i^0 = \text{AGND}$, and this will also set the parameters R_i and K. Unfortunately the switch will cause additional leakage and worsen the loading effect because it acts as a resistor in parallel to the input resistance of the op-amp.

4.5 Remarks on Literature

As remarked in the end of section 2.4, the loading effect caused by the input resistance of readout circuits at low frequencies did not appear to be discussed in the literature. There are various reasons that could explain this. Firstly, the original ISFET structure did not have a floating gate between the sensing dielectric and the MOSFET channel. Therefore there is no additional stage that can introduce loading effects and screen the electric field from the surface charges at the electrolyte/insulator interface. In this case, the concerns discussed here are not relevant, and the ISFET response to pH can accurately be described through the variation of its threshold voltage V_T. For the papers where a floating gate ISFET structure was used, it is possible that the MOSFETs had sufficiently thick gate oxides that tunneling effects were negligible, or at least sufficiently small that the introduced low-frequency pole occurs below the frequencies of interest. However these effects were not negligible in the application of this thesis.

Chapter 5

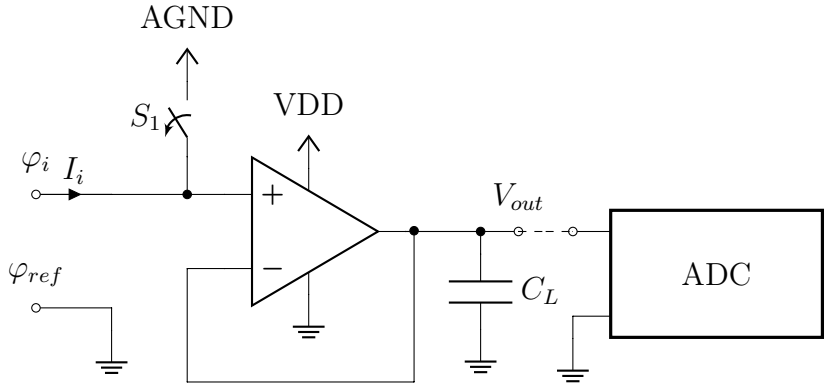
Buffer Readout Circuit

5.1 Mathematical Analysis

For this analysis, we assume that at its operating point, the op-amp has a transfer function $A(s)$ with DC gain A. The op-amp also has an output resistance R_{out}, and we assume that the op-amp is loaded by an equivalent load capacitance C_L coming from the ADC and from an external compensation capacitor that could be connected to V_{out}. Since the reference electrode is grounded, the value of K is zero. The reader is referred to Razavi's textbook [37] for a treatment of the general theory of op-amps, feedback circuits, as well as frequency compensation and stability.

In this circuit, the relationship between the Laplace transforms $\varphi_{\mathbf{i}}(s)$ and $\mathbf{V_{out}}(s)$ is:

$$\mathbf{V_{out}}(s) = \frac{1}{1 + \frac{1}{A(s)}\left[1 + sC_L R_{out}\right]}\varphi_{\mathbf{i}}(s) \tag{5.1}$$



5.1.1 Relationship between V_{out} and pH

At low frequencies, the load capacitor acts as an open-circuit. Therefore in the low frequency limit, the relationship between V_{out} and φ_i simplifies to:

$$V_{out}(t) = \frac{1}{1+\frac{1}{A}}\varphi_i(t) \approx \varphi_i(t) \tag{5.2}$$

Here the approximation comes from the fact that the DC gain of the op-amp is expected to be large. Therefore, the output of the op-amp simply tracks the input, as expected for the operation of a buffer. When the switch S_1 is closed, the input is fixed to some initial value connected to AGND, and this sets the bias of the op-amp. Hence the transfer function and impedances should be calculated at this operating point. The switch S_1 is then open for the remainder of the time, allowing the input to vary with the external pH signal.

In section 3.12, it was estimated that $C_{sens} \approx 3$ nF for Ta_2O_5 with the given dimensions of 400 μm $\times$ 400 μm (area) and 10 nm (thickness). In the buffer readout circuit, $K = 0$. Therefore, in order for τ to exceed 48 hours, it is necessary that R_i be larger than 10^{14} Ω, which is quite a large value. From the analysis of section 3.11, there is also a drift term with coefficient $\frac{I_i^0}{C_{sens}}$. In order for the drift to accumulate an error less than 2.5 mV, it is required that $|I_i^0| < \frac{C_{sens}}{t_{max}}2.5$ mV. Therefore I_i^0 must be below 40 aA, which is a very small value.

Assuming that R_i is sufficiently large and that the leakage current I_i^0 is sufficiently low, the input $\Delta\varphi_i$ will satisfy equation (3.43), so that the relationship between ΔV_{out} and ΔpH is:

$$\Delta V_{out}(t) = -\frac{A}{A+1}2.303\frac{k_B T}{q}\alpha\Delta\text{pH}(t) \tag{5.3}$$

5.1.2 Stability and noise

At high frequencies it is expected that $A(s)$ will eventually roll off due to poles introduced by the MOSFET input capacitances and other parasitic effects. The load capacitor C_L can be chosen to ensure stability using the dominant pole frequency compensation technique. This would be required if $A(s)$ does not have a sufficient phase margin to ensure stability in a unity-gain configuration. In fact, the poles of the system are determined by the roots of the equation:

$$\frac{A(s)}{1+sC_L R_{out}} = -1 \tag{5.4}$$

Let M be such that $-\frac{\pi}{2} < \angle A(s) < \frac{\pi}{2}$ as long as $|s| < M$. In fact, $\angle A(0) = \angle A_{DC} = 0$, so such an M exists by continuity. For $\Re(s) \geq 0$ we also have $-\frac{\pi}{2} < \angle(1 + sC_L R_{out}) < \frac{\pi}{2}$, so $-\pi < \angle\left(\frac{A(s)}{1+sC_L R_{out}}\right) < \pi$ as long as $|s| < M$ and $\Re(s) \geq 0$. Therefore if C_L is chosen large enough as:

$$C_L > \frac{A_{DC}}{M R_{out}} \tag{5.5}$$

it will be impossible to have roots of equation (5.4) with $\Re(s) \geq 0$ since whenever the phase is π, the absolute value will be less than 1. This will ensure stability of the system.

The op-amp will have an input-referred noise which can be modeled as a voltage source V_n in series with the positive input. Since φ_i varies proportionally to pH with a sensitivity $S_i = 50$ mV/pH (as per Table 4.1), the integrated RMS noise should not exceed 2.5 mV over the frequency range of 1 μHz to 1 Hz to achieve the desired resolution of 0.1 pH.

5.2 Simulation Results

The simulation sections for this and the other readout circuit chapters will serve to verify the mathematical models presented in the mathematical analysis sections. The op-amp will be replaced by an ideal voltage-controlled voltage source (VCVS) with gain A and input resistance R_i in parallel to its positive input. The input to the circuit will be provided by the ISFET model presented in section 3.12 using Ta_2O_5, and the simulations will directly control the pH and bulk potential φ_b through ideal voltage sources. Every simulation is done at a temperature of $T = 310$ K (37° C).

The Cadence schematic used for the simulation of the buffer readout circuit is shown in Figure 5.1. The component `ph_membrane` represents the model of the pH sensing dielectric. As mentioned previously, the model takes the input current I_i to the readout circuit as a parameter. This is achieved by placing a CCVS at the `Ifg` pin, whose voltage is controlled by the current going through the dummy voltage source between `floatg` and R_i.

The AC analysis of the circuit is shown in Figure 5.2 for $R_i = 10^9$ Ω and $A = 200$ V/V, and in Figure 5.3 for $R_i = 10^{14}$ Ω and $A = 200$ V/V. The plots show the magnitude of the transfer function in V/V. As expected, the response is that of a high-pass filter, and the cutoff frequencies are near 50 mHz and slightly below 1 μHz respectively. The cutoff frequency f_c is related to the time constant by $\tau = \frac{1}{2\pi f_c}$.

These results are consistent with the value of C_{sens} calculated in section 3.12 and the analysis in section 5.1. The high-frequency sensitivity is near

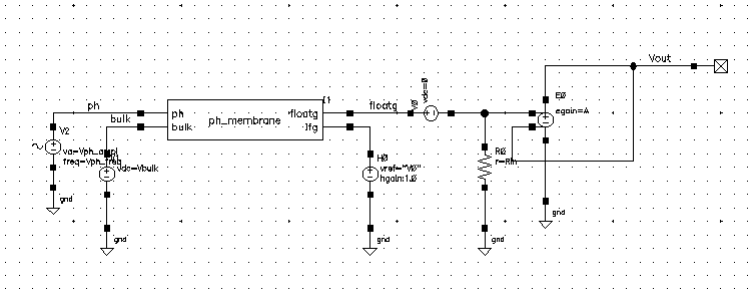


Figure 5.1 – Schematic of buffer readout circuit for simulations. The pin `bulk` is φ_b and `floatg` is φ_i.

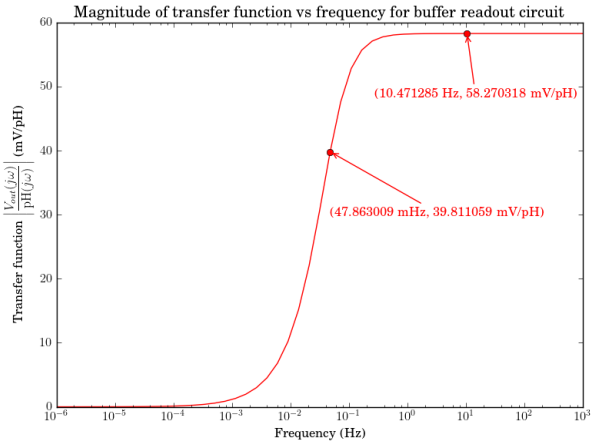


Figure 5.2 – AC analysis of buffer readout for $R_i = 10^9\ \Omega$ and $A = 200\ \text{V/V}$.

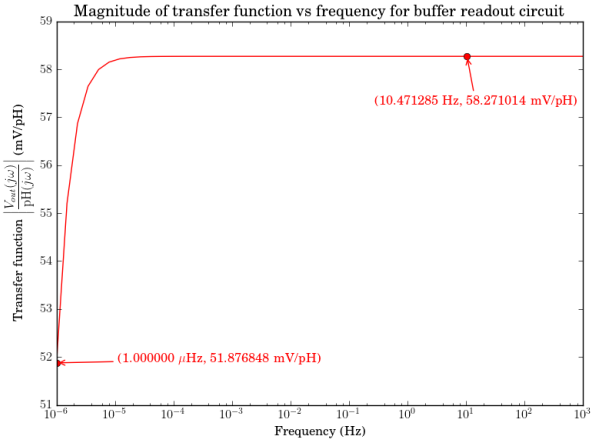


Figure 5.3 – AC analysis of buffer readout for $R_i = 10^{14}\ \Omega$ and $A = 200\ \text{V/V}$.

58.2 mV/pH, which is consistent with the simulated sensitivity of 58.8 mV/pH for Ta_2O_5 in section 3.12, taking into account the factor $\frac{A}{A+1}$ due to the finite gain. The AC analysis used pH = 7 for the operating point.

The value of 58.8 mV/pH is an average over the entire pH range, but between pH 6.5 and 7.5, the average sensitivity is 58.56 mV/pH, which explains the remaining discrepancy.

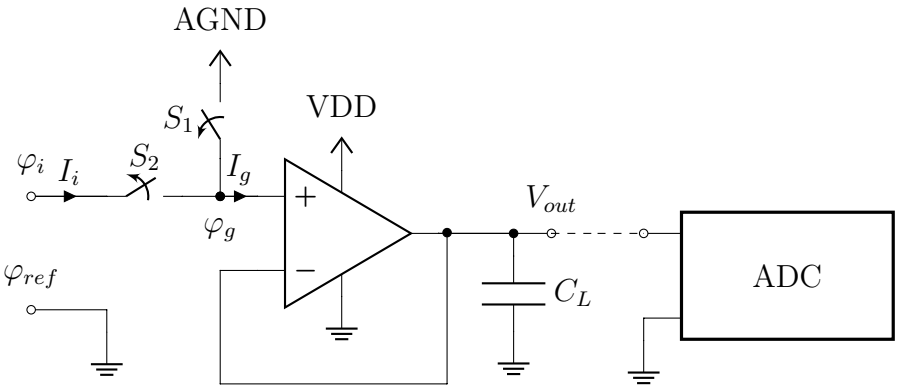
Chapter 6

Switch and Buffer Readout Circuit

6.1 Mathematical Analysis

For this analysis, the switches will be assumed ideal, so that when the switch S_2 is open we have $R_i = \infty$. We also have $K = 0$ since φ_{ref} is grounded. The switch S_1 will be open all the time except at $t = 0$ to set the initial condition for φ_i^0. The node φ_g represents the input to the op-amp buffer, and is directly connected to a MOSFET gate. The MOSFET gate has a capacitance C_g which is negligibly small compared to C_{sens} due to its small area, and it has a gate current given as $I_g = I_g(\varphi_g)$.

Suppose the switch S_2 closes at time $t = t_n$. During the short period of time where the switch transitions from the open to the closed configuration, the charges stored in nodes φ_i and φ_g will redistribute uniformly over the entire floating node shorting φ_i and φ_g. Since we assumed that the gate capacitance C_g is negligible compared to C_{sens}, the charge stored across C_{sens}



will not be affected and the value of φ_i will be the same right before and right after closing the switch, so the following continuity condition holds:

$$\lim_{t \to t_n^+} \varphi_i(t) = \lim_{t \to t_n^-} \varphi_i(t) = \varphi_i(t_n) \tag{6.1}$$

As long as the switch remains closed, the value of φ_i will evolve according to equation (3.39) with $R_i = R_g$, $I_i = I_g$ and $\tau = R_g C_{sens}$, where $R_g = \left[I_g'(\varphi_i(t_n))\right]^{-1}$. If the switch is only closed for a short time period Δt, then we can use a first-order Taylor expansion to calculate $\varphi_i(t_n + \Delta t)$:

$$\varphi_i(t_n + \Delta t) = \varphi_i(t_n) - \left[S_i \cdot \mathrm{pH}'(t_n) + \frac{I_g(\varphi_i(t_n))}{C_{sens}}\right] \Delta t \tag{6.2}$$

After this, the switch goes back to the open configuration until the next closing time t_{n+1}. Then $R_i = \infty$, $I_i^0 = 0$ and $\tau = \infty$. In this case, we can apply equation (3.43), using the starting time $t_n + \Delta t$ instead of 0:

$$\varphi_i(t_{n+1}) = \varphi_i(t_n + \Delta t) - S_i \left[\mathrm{pH}(t_{n+1}) - \mathrm{pH}(t_n + \Delta t)\right] \tag{6.3}$$

Combining equations (6.2) and (6.3) together with the continuity condition (6.1), we obtain the following recurrence relationship:

$$\varphi_i(t_{n+1}) = \varphi_i(t_n) - S_i \left[\mathrm{pH}(t_{n+1}) - \mathrm{pH}(t_n)\right] - \frac{I_g(\varphi_i(t_n))}{C_{sens}} \Delta t \tag{6.4}$$

The recurrence can be rewritten in the following form:

$$\varphi_i(t_n) = \varphi_i^0 - S_i \Delta\mathrm{pH}(t_n) - \Delta t \sum_{k=0}^{n-1} \frac{I_g(\varphi_i(t_k))}{C_{sens}} \tag{6.5}$$

Here φ_i^0 is the initial value, which can be set by closing switches S_1 and S_2 at time $t = 0$, setting $\varphi_i^0 = \mathrm{AGND}$. This allows proper biasing of the op-amp during measurements.

The ADC will sample the value of V_{out} measured right after closing the switch S_2. Assuming that the buffer is ideal, we have $V_{out}(t) = \varphi_g(t)$. Once the switch is closed, we have $\varphi_i(t) = \varphi_g(t)$, so right after closing the switch, we have $V_{out}(t_n^+) = \varphi_i(t_n)$. The samples will be denoted by $V_{out}[n] = V_{out}(t_n^+)$ and $\Delta\mathrm{pH}[n] = \Delta\mathrm{pH}(t_n)$. Then the samples are related by the equation:

$$V_{out}[n] = \mathrm{AGND} - S_i \Delta\mathrm{pH}[n] - \Delta t \sum_{k=0}^{n-1} \frac{I_g(\varphi_i[k])}{C_{sens}} \tag{6.6}$$

Note that during the open phase, node φ_g will converge to a value where the gate current becomes zero. The node φ_g sees a gate current I_g and gate capacitance C_g which is small compared to C_{sens}, and the equation for φ_g is:

$$C_g \frac{\mathrm{d}\varphi_g}{\mathrm{d}t} + I_g(\varphi_g(t)) = 0 \tag{6.7}$$

It is seen that φ_g will quickly converge to a constant value $\overline{\varphi_g}$ such that $I_g(\overline{\varphi_g}) = 0$. The buffer will then output a value of V_{out} that is not related to pH and should be discarded.

As can be seen from equation (6.6), V_{out} tracks ΔpH with sensitivity $S_i = 2.303\frac{k_B T}{q}\alpha$. The error term is due to the gate leakage current I_g accumulating during each closing phase of the switch. The overall error is minimized by reducing the closing time Δt.

The high-frequency limit of this circuit is determined by the sample rate $f_s = \frac{1}{T_s}$ where T_s is the period of one switching cycle. By the Nyquist criterion, the sample rate must be larger than twice the maximal signal frequency to be measured, so $f_s > 2f_{max}$. Over a maximal time of operation t_{max}, the total number of samples N will therefore have to satisfy $N = \frac{t_{max}}{T_s} > 2f_{max}t_{max}$. We can then give an upper bound for the error term for all $n \leq N$ by the formula:

$$\left| \Delta t \sum_{k=0}^{n-1} \frac{I_g(\varphi_i[k])}{C_{sens}} \right| \leq N\Delta t \frac{|I_g|_{max}}{C_{sens}} \tag{6.8}$$

where $|I_g|_{max}$ is the largest value of I_g expected over the time of operation. This provides a design criterion for Δt to guarantee that this error term is below a desired bound.

The main concern with this approach is once again the use of a switch with very high resistance in open configuration. The analysis provided above neglected the leakage currents present through the switches in open configuration, and these currents will introduce additional sources of error. This could be implemented using a mechanical switch, but it would be preferable to have electronic switches using MOSFET, particularly due to the fast switching times required. Unfortunately it is not clear whether MOSFET switches will be able to maintain sufficiently low leakage currents in the off state, especially in a small-scale process such as TSMC 65nm. For stability and noise, the same considerations apply as in section 5.1.2.

6.2 Simulation Results

Based on the preceding analysis, it is important to fix the number of samples N and the closing time Δt of the switch. In the current application,

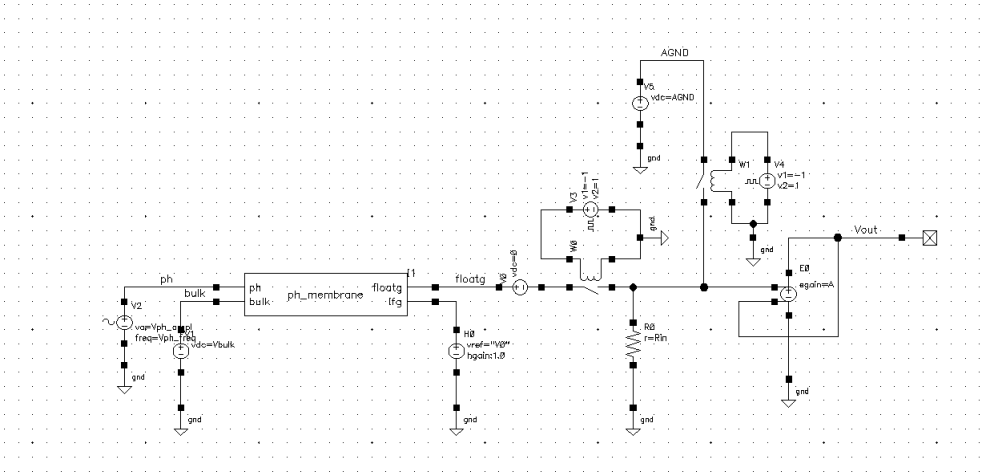


Figure 6.1 – Schematic of switch and buffer readout circuit for simulations. The pin `bulk` is φ_b, `floatg` is φ_i and the net connected to the `E0` VCVS is φ_g.

the pH signal frequency was assumed to be at most $f_{max} = 1$ Hz, and the time of operation is $t_{max} = 48$ hours $= 172800$ s. By the Nyquist criterion, the sampling period T_s will have to be less than 0.5 s, and the number of samples N will have to exceed 345600.

In the simulation, $R_i = 10^9\ \Omega$ and $I_i^0 = 0$. The bulk potential was set to $\varphi_b = 0$. The pH varies between 6 and 8, with $\text{pH}^0 = 7$. Since φ_i varies by around ± 60 mV in this case, it follows that the gate leakage current satisfies $|I_g|_{max} = 60$ pA. In that case, the criterion given by equation (6.8) requires Δt to be smaller than 0.3 μs to achieve an error below 2.5 mV, and this would require a fast sampling circuit. However the upper bound provided by this equation is very conservative due to the possibility of cancellation between terms in the summation. For the simulations, the switch is assumed to have a resistance $R_{s,closed} = 1\ \Omega$ when closed and $R_{s,open} = 10^{21}\ \Omega$ when open. These resistance values are used to provide an ideal switch model.

In order to set the DC operating point such that $I_i^0 = 0$, the value of AGND was set to 0 V. In practice, the resistance R_i is not necessarily connected to ground, so the potential for which $I_i^0 = 0$ may vary. This is due to offsets from Q_i^0 (see section 3.12) as well as due to the specific nonlinear current-voltage relationship of the MOSFET gate. Hence it might not be easy to set $I_i^0 = 0$. In such a case, $|I_g|_{max}$ will be larger and even shorter times Δt will be required.

The Cadence schematic used for the switch and buffer readout circuit is shown in Figure 6.1. There is a switch between the node `floatg` and R_i that

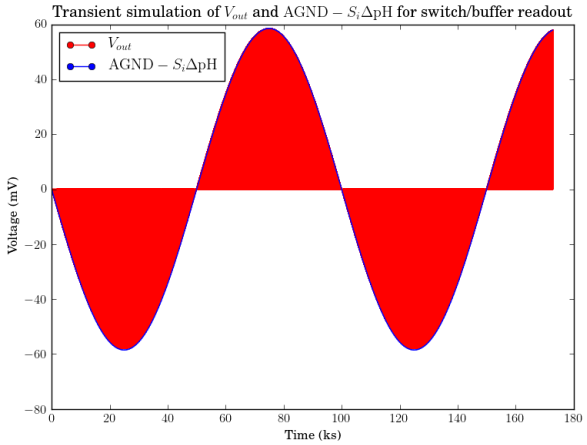


Figure 6.2 – Transient analysis of switch/buffer readout for $R_i = 10^9\ \Omega$, $A = 200$ V/V, $\Delta t = 0.3\ \mu$s.

represents switch S_2, and the switch connected to AGND represents switch S_1. The op-amp gain was set to 200 V/V as before. For this simulation, the pH was set as a sine wave with DC offset at 7 and amplitude of 1, at a frequency of 10 μHz. The switch S_1 is closed for the first 500 μs to set the initial value to AGND, and remains open for the rest of the simulation.

The plots of V_{out} and AGND − $S_i\Delta$pH are shown in Figure 6.2. As can be seen from the envelope, V_{out} closely follows the pH signal scaled by the sensitivity when the switch is closed. When the switch is open, V_{out} drops to 0 V. The error V_{out} − (AGND − $S_i\Delta$pH) is shown in Figure 6.3, where the error was multiplied by $\frac{V_{switch}+1}{2}$ in order to ignore the errors during the open phase of the switch. The switch voltage alternates between −1 V (open) and 1 V (closed), so this effectively multiplies the error by zero when open and by 1 when closed. As predicted, the error does not exceed 2.5 mV over the time range.

For comparison, the plots of V_{out} and AGND − $S_i\Delta$pH in the switch and buffer readout circuit using a value $\Delta t = 3\ \mu$s are shown in Figure 6.4. The error already becomes noticeable, exceeding 2.5 mV for long periods of time. The simulation results obtained in this section are consistent with equation (6.6), where the sensitivity is $S_i = 58.56$ mV/pH, taking into account the factor of $\frac{A}{A+1}$ coming from the finite op-amp gain, just as in section 5.2.

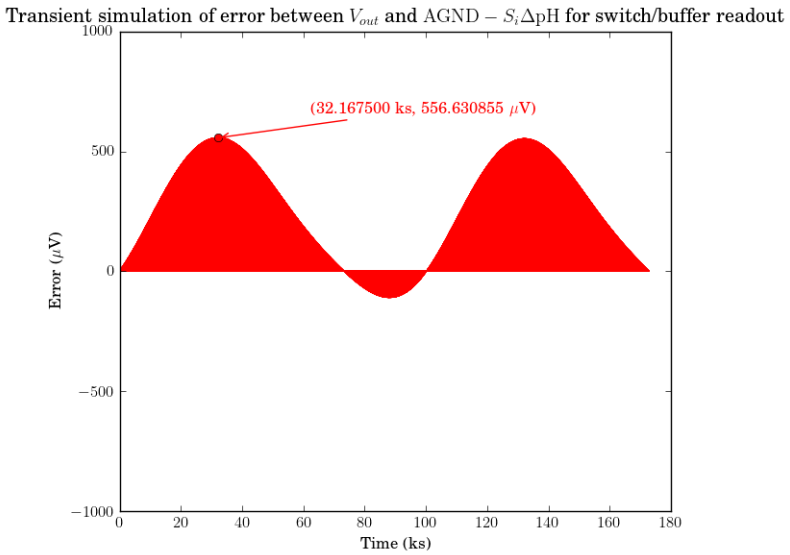


Figure 6.3 – Error in transient analysis of switch/buffer readout for $R_i = 10^9$ Ω, $A = 200$ V/V, $\Delta t = 0.3$ μs.

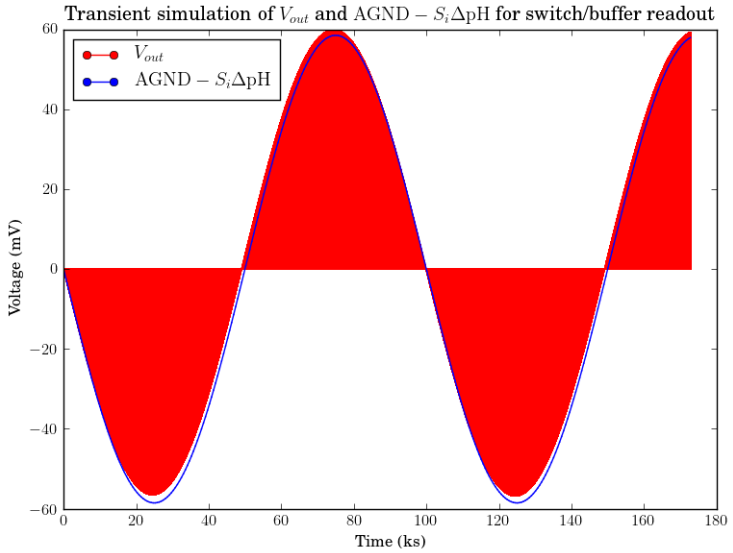


Figure 6.4 – Transient analysis of switch/buffer readout for $R_i = 10^9$ Ω, $A = 200$ V/V, $\Delta t = 3$ μs.

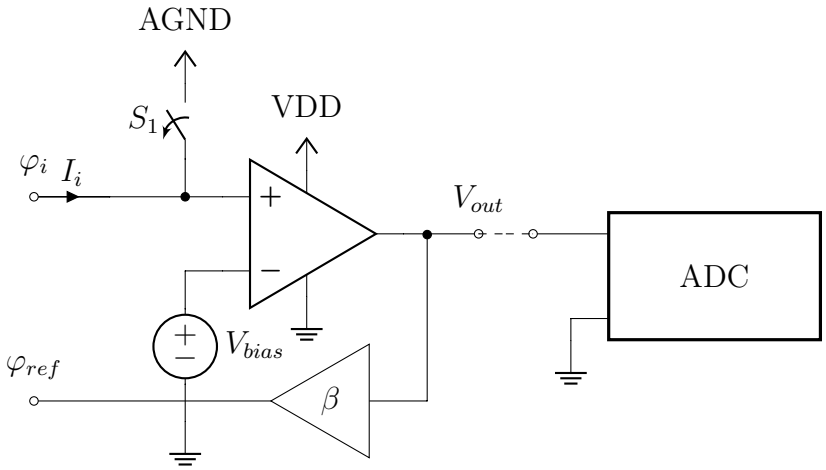
Chapter 7

Reference Electrode Feedback Readout Circuit

7.1 Mathematical Analysis

Assuming that the op-amp is properly biased with a DC gain A, then at low frequencies we have $\Delta V_{out}(t) = A\Delta\varphi_i(t)$. Moreover, assuming an ideal feedback network with DC gain β, the relationship between $\Delta\varphi_{ref}$ and ΔV_{out} is given by $\Delta\varphi_{ref} = \beta\Delta V_{out}$. Therefore, the value of K for this circuit is given by $K = A\beta$. The value of R_i is the parallel combination of the open resistance of switch S_1 and the gate resistance of the MOSFET directly connected to the op-amp's positive input.

According to equation (3.47) and the relationship between $\Delta\varphi_{ref}$ and ΔV_{out}, we see that if $|K|$ is sufficiently large, then ΔV_{out} evolves over time



and pH as follows:

$$\Delta V_{out}(t) = \frac{1}{\beta} 2.303 \frac{k_B T}{q} \alpha \Delta \text{pH}(t) + \frac{I_i^0}{\beta C_{sens}} t \tag{7.1}$$

In order for the system to be stable, $K < 1$ so we must have $\beta < 0$ (since A is already assumed positive). Therefore the feedback network must be inverting. We conclude that the circuit can be designed by choosing a negative value of β that controls the overall pH-sensitivity of V_{out} (the simplest choice would be $\beta = -1$). Then the gain of the op-amp is chosen so that $A\beta = K > \frac{t_{max}}{R_i C_{sens}}$.

7.1.1 Biasing and drift analysis

Just as in the previous readout circuits, the initial values are set by closing the switch S_1 at time $t = 0$, so that $\varphi_i^0 = \text{AGND}$. This sets the biasing of the op-amp. In this circuit, the value of AGND must also be set such that $I_i^0 = I_i(\text{AGND}) = 0$, otherwise there will be an additional drift error coming from the term $\frac{I_i^0}{\beta C_{sens}} t$ in equation (7.1). Intuitively, the drift comes from the fact that $\varphi_i(t) = \varphi_i^0 = \text{AGND} = V_{bias} + V_{os}$ at all times (virtual ground). This leads to a DC current $I_i^0 = I_i(\text{AGND})$, which must be supplied by a displacement current through C_{sens}, which leads to a gradual charge build up over time.

Therefore, it is essential to set I_i^0 as close as possible to 0 in order to avoid drift, and this must be done by choosing AGND such that $I_i(\text{AGND}) = 0$. However, it is possible that this constraint conflicts with the biasing requirements of the op-amp. Even though the drift coefficient is inversely proportional to β, increasing β will not help because the pH sensitivity is also inversely proportional to β, so the error relative to pH does not change.

Now we assume again that the op-amp has finite gain A in order to analyze the choice of V_{bias}. The op-amp will be assumed to have infinite common-mode rejection, so that the relationship between V_{out}, V_+ and V_- depends only on the difference, $V_{out} = f(V_+ - V_- - V_{os})$, where V_{os} is an offset voltage. The function $f(x)$ is nonlinear, with a generally sigmoid shape which saturates at V_{DD} for positive x and saturates at 0 for negative x. A high gain region is maintained over a small interval around $x = 0$. As a simplification, we may assume that $f(x) = Ax + \frac{V_{DD}}{2}$ for $-\frac{V_{DD}}{2A} \leq x \leq \frac{V_{DD}}{2A}$, $f(x) = 0$ for $x < -\frac{V_{DD}}{2A}$ and $f(x) = V_{DD}$ for $x > \frac{V_{DD}}{2A}$.

Then in order to take advantage of the high gain of the op-amp, it is required to bias the op-amp in such a way that

$$|\text{AGND} - V_{bias} - V_{os}| < \frac{V_{DD}}{2A} \tag{7.2}$$

where A is the maximal DC gain of the op-amp. This leaves little margin of error to set V_{bias} if the gain A is required to be large. Unfortunately, since V_{os} is generally process-dependent and unpredictable, it is not possible to simply short AGND and V_- because the op-amp could saturate in the presence of an internal offset.

7.1.2 Discussion

Using feedback on the reference electrode allows controlling the value of K, which as mentioned previously, allows increasing the time constant τ by a factor of $1 - K$. This could be helpful in the case that the MOSFET gate resistance and the S_1 switch resistance are not sufficiently high for $R_i C_{sens}$ to be as large as required. However, as noted in the previous section, there are practical problems related to the proper biasing of this circuit. In order to achieve a high gain, the voltage source V_{bias} must be precisely controlled according to equation (7.2). Moreover, the value of AGND must be precisely set to minimize the input bias current I_i^0 in order to eliminate the drift term from equation (7.1).

One more important problem can be found when thinking about the effect of the input-referred noise of the op-amp at φ_i in series with C_{sens}. Using the fact that φ_i should be a virtual ground, the series voltage V_n at the input of the op-amp would affect V_{out} while being scaled by the gain A. Hence the noise referred to pH would be scaled by $\frac{A}{|\beta|}$, meaning it would be very large unless the op-amp has very low V_n. Intuitively, we can also see that the noise V_n contributes a random value to the input offset voltage V_{os}, so that either the noise must be extremely small, or V_{bias} would have to change over time tracking this noise in order to maintain the op-amp in the high-gain region. Both possibilities seem infeasible in practice. The solution might still be useful if R_i is already very high so that the time constant only needs to be increased by a small factor. In that case a lower gain can be used, and might be achieved by replacing the op-amp with a non-inverting amplifier configuration having a small gain set through resistive feedback. Having a low A could resolve the DC biasing and noise problems.

The stability of the circuit is another concern. The analysis above was performed considering only low frequency operation. However, stability must be investigated at all frequencies to avoid spontaneous oscillations, and this requires a more complicated analysis of all the impedances and transfer functions in the circuit.

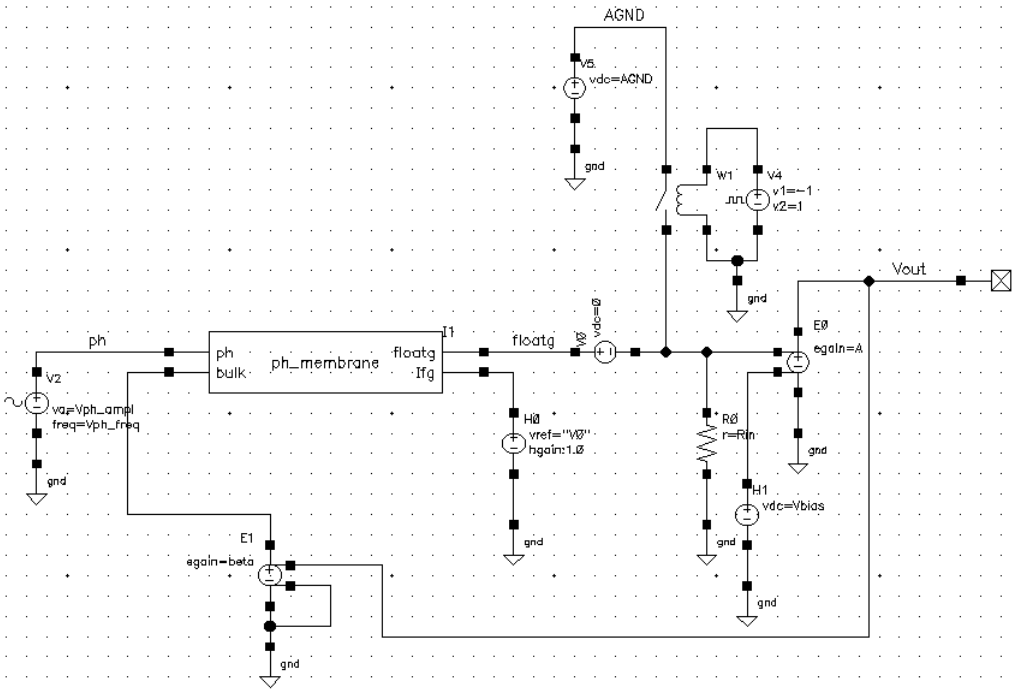


Figure 7.1 – Schematic of reference electrode feedback circuit for simulations. The pin `bulk` is φ_b, φ_{ref} is same as φ_b, and `floatg` is φ_i.

7.2 Simulation Results

The Cadence schematic for the reference electrode feedback readout circuit is shown in Figure 7.1. The structure is similar to that of the buffer readout circuit in Figure 5.1, except that V_{out} is fed back to the `bulk` input of the `ph_membrane` model through an ideal VCVS with gain β. This simulates the feedback through the reference electrode, where the reference electrode was assumed ideal with $Z_{ref} = 0\ \Omega$ and $E_{ref} = 0$ V. In Figure 7.2 is shown the AC analysis of this circuit using $A = 200$ V/V, $\beta = -0.5$ V/V and $R_i = 10^9\ \Omega$. As expected, the transfer function is again that of a high-pass filter, and the cutoff frequency f_c is around 570 μHz.

Using these values for A and β, we obtain $K = -100$. According to equation (3.32), the value of the time constant is $\tau = (1 - K)R_iC_{sens} \approx 300$ s. Therefore, the result for f_c agrees with this analysis, given that $\tau = \frac{1}{2\pi f_c}$. In addition, the high-frequency response shows that V_{out} has a pH-sensitivity of 116 mV/pH, which is about twice the sensitivity of Ta_2O_5, in agreement with the claim that the pH-sensitivity is scaled by a factor of $\frac{1}{\beta}$.

The same simulation with $A = 200$ kV/V is shown in Figure 7.3. This confirms the fact that increasing A allows reducing the cutoff frequency pro-

portionally, and making $R_i = 10^9\ \Omega$ being usable despite the loading effect. However, as mentioned in the preceding analysis, such high gains are unrealistically high and will suffer from the DC biasing issues that were overlooked in this simulation. It is still possible to use this method to reduce the cutoff frequency slightly if R_i is already close to the right value.

The transient simulation in Figure 7.4 shows the effect of a bad choice for AGND. In this simulation, AGND = V_{bias} = 10 μV. As predicted by equation (7.1), there is a drift caused by the fact that the DC value of node φ_i is not exactly 0 V, causing the leakage current I_i^0 to be nonzero. The plot shows that V_{out} drifts over time as expected from the analysis. In Figure 7.5, the values of AGND = V_{bias} = 0 V were used, eliminating the drift component. It is shown that V_{out} is approximately equal to AGND + $\frac{S}{\beta}\Delta$pH as predicted by equation (7.1), where $S = 58.56$ mV/pH (the sensitivity of Ta_2O_5 around a pH of 7, as mentioned in section 5.2. We also see that φ_i indeed behaves like a virtual ground.

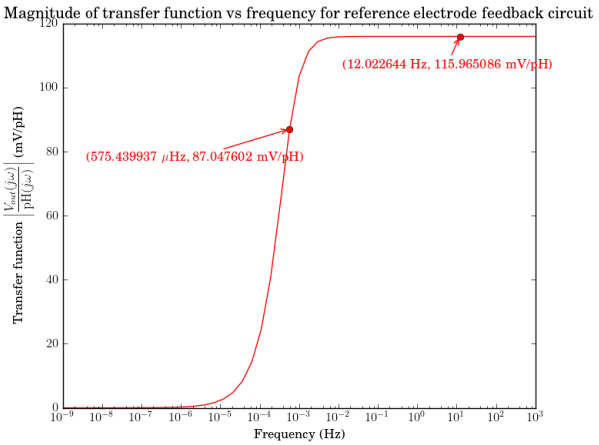


Figure 7.2 – AC analysis of reference electrode feedback circuit for $R_i = 10^9$ Ω, $A = 200$ V/V and $\beta = -0.5$ V/V.

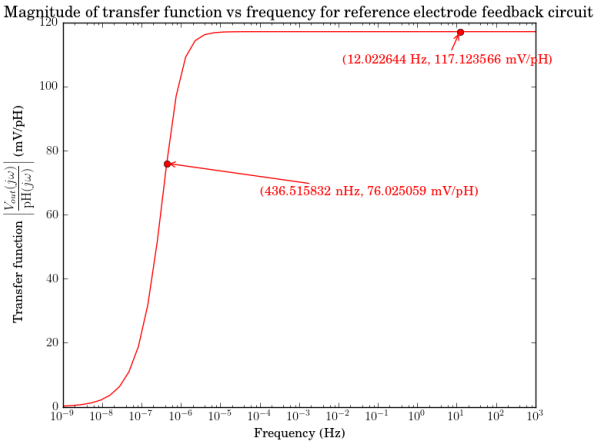


Figure 7.3 – AC analysis of reference electrode feedback circuit for $R_i = 10^9$ Ω, $A = 200$ kV/V and $\beta = -0.5$ V/V.

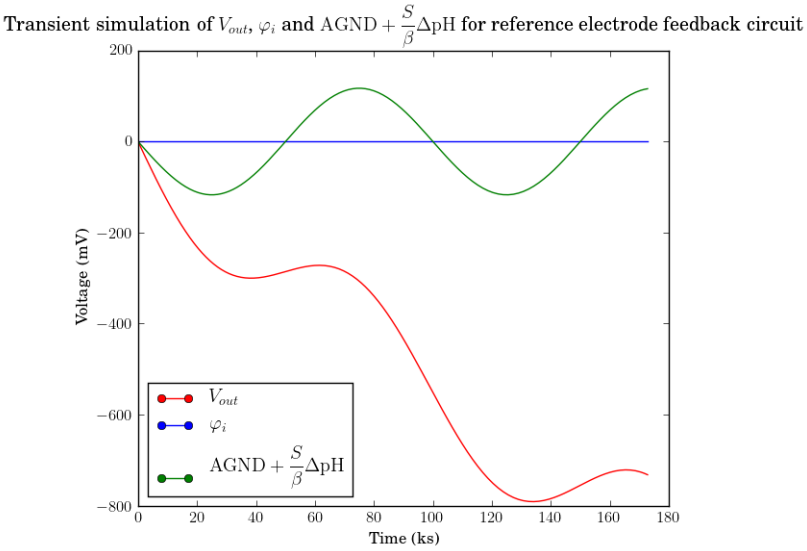


Figure 7.4 – Transient analysis of reference electrode feedback circuit for $R_i = 10^9\ \Omega$, $A = 200$ kV/V, $\beta = -0.5$ V/V and AGND $= 10\ \mu$V.

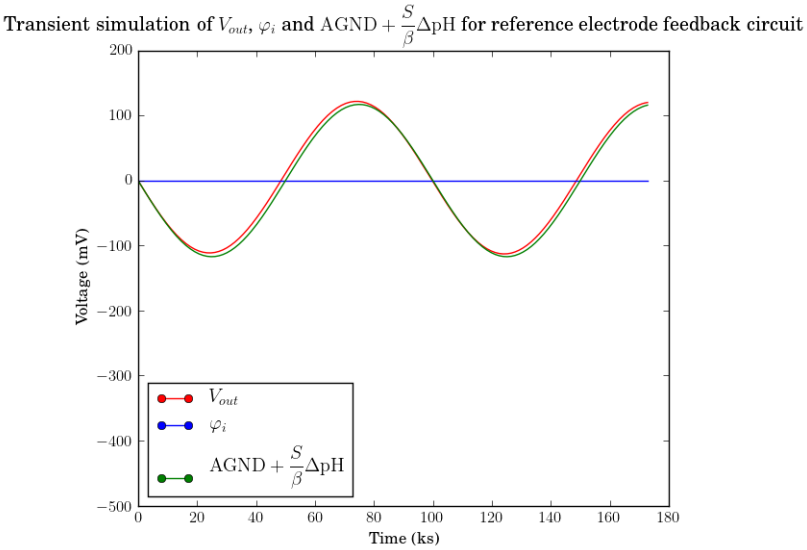


Figure 7.5 – Transient analysis of reference electrode feedback circuit for $R_i = 10^9\ \Omega$, $A = 200$ kV/V, $\beta = -0.5$ V/V and AGND $= 0$ V.

Chapter 8

Differential Readout Circuits

So far, the readout circuits presented used a single-ended configuration, where a single input φ_i is measured relative to its initial value $\varphi_i^0 = \text{AGND}$. As mentioned in section 2.4.5, the reference electrode might introduce a source of noise in the system. Similarly, there may be other phenomena occurring in the solution that could affect the value of φ_i without being related to pH. For this reason, it is desirable to use a differential configuration of the readout circuit, which can eliminate or reduce common-mode sources of noise.

A circuit model of the differential readout configuration is shown in Figure 8.1. Only the case where the reference electrode is grounded will be considered, since reference electrode feedback would require the ability to connect two distinct nodes to the same reference electrode. The dependent voltage sources were not labeled to avoid cluttering the diagram.

The idea behind this structure is that there are two different dielectrics on the surface of the sensor, with capacitances $C_{sens,1}$ and $C_{sens,2}$ respectively. They will be made from different materials with different chemical properties. In particular, the first material will be pH-sensitive while the second material will be pH-insensitive. The reference electrode will be common to both circuits. However, on the surface of the dielectrics, there will be different charges $Q_{0,1}$ and $Q_{0,2}$ accumulated. Finally, the readout circuit will have access to inputs $\varphi_{i,1}$ and $\varphi_{i,2}$.

In reality, it is not clear whether $\varphi_{h,1}$ and $\varphi_{h,2}$ should be uncoupled, because it is possible for ions to move across the solution between the two dielectric surfaces. This could perhaps be avoided by introducing an isolating barrier.

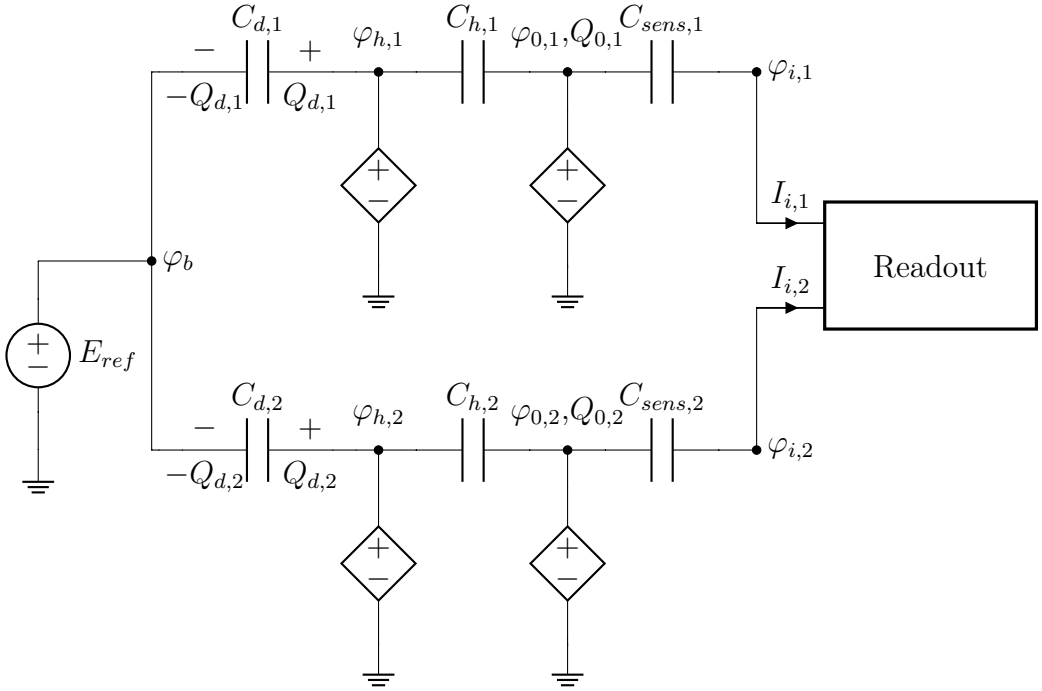


Figure 8.1 – ISFET differential frontend circuit model.

8.1 Analysis of Differential Frontend

The mathematical model of the differential frontend for branch 1 is as follows:

$$Q_{d,1} = A_1 \sqrt{8\varepsilon_0 \varepsilon_b N_A k_B T c_0} \sinh\left[\frac{q(\varphi_{h,1} - E_{ref})}{2k_B T}\right] \tag{8.1}$$

$$C_{h,1}(\varphi_{h,1} - \varphi_{0,1}) + Q_{d,1} = 0 \tag{8.2}$$

$$C_{h,1}(\varphi_{0,1} - \varphi_{h,1}) + C_{sens,1}(\varphi_{0,1} - \varphi_{i,1}) = Q_{0,1} \tag{8.3}$$

$$Q_{0,1} = qN_{s,1}A_1 \frac{\left[e^{-2.303\cdot \mathrm{pH} - \frac{q}{k_B T}(\varphi_{0,1} - E_{ref})}\right]^2 - K_{a,1}K_{b,1}}{K_{a,1}K_{b,1} + K_{b,1}e^{-2.303\cdot \mathrm{pH} - \frac{q}{k_B T}(\varphi_{0,1} - E_{ref})} + \left[e^{-2.303\cdot \mathrm{pH} - \frac{q}{k_B T}(\varphi_{0,1} - E_{ref})}\right]^2} \tag{8.4}$$

$$C_{sens,1}\frac{\mathrm{d}}{\mathrm{d}t}(\varphi_{i,1} - \varphi_{0,1}) + I_{i,1}(\varphi_{i,1}) = 0 \tag{8.5}$$

Just as in Chapter 3, the signals are decomposed into initial conditions and small variations relative to the initial conditions. The initial values of $\varphi_{i,1}^0$ and $\varphi_{i,2}^0$ are arbitrary and depend on the charge stored in the capacitors $C_{sens,1}$ and $C_{sens,2}$ initially.

The small-signal equations for branch 1 are obtained again by a first-order Taylor expansion around the initial values. This time, we will consider the

effect of noise in the reference electrode, so that $E_{ref} = E^0_{ref} + \Delta E_{ref}$:

$$\Delta Q_{d,1} = C_{d,1}(\Delta\varphi_{h,1} - \Delta E_{ref}) \tag{8.6}$$

$$C_{h,1}(\Delta\varphi_{h,1} - \Delta\varphi_{0,1}) + \Delta Q_{d,1} = 0 \tag{8.7}$$

$$C_{h,1}(\Delta\varphi_{0,1} - \Delta\varphi_{h,1}) + C_{sens,1}(\Delta\varphi_{0,1} - \Delta\varphi_{i,1}) = \Delta Q_{0,1} \tag{8.8}$$

$$\Delta Q_{0,1} = -qA_1\beta_{int,1}\left[\Delta\mathrm{pH} + \frac{q}{2.303k_BT}(\Delta\varphi_{0,1} - \Delta E_{ref})\right] \tag{8.9}$$

$$C_{sens,1}\frac{\mathrm{d}}{\mathrm{d}t}(\Delta\varphi_{i,1} - \Delta\varphi_{0,1}) + I^0_{i,1} + \frac{\Delta\varphi_{i,1}}{R_{i,1}} = 0 \tag{8.10}$$

The various quantities appearing here are defined similarly as in Chapter 3. After proceeding similarly as in section 3.8, one can obtain the following time evolution ODE for $\varphi_{i,1}$, including the effect of ΔE_{ref}:

$$\frac{\mathrm{d}\Delta\varphi_{i,1}}{\mathrm{d}t} + \frac{\Delta\varphi_{i,1}}{\tau_1} = -S_{i,1}\frac{\mathrm{d}\Delta\mathrm{pH}}{\mathrm{d}t} - \frac{R_{i,1}I^0_{i,1}}{\tau_1} + \frac{\mathrm{d}\Delta E_{ref}}{\mathrm{d}t} \tag{8.11}$$

The time constant τ_1 is given by:

$$\tau_1 = \frac{R_{i,1}C_{sens,1}}{1 + (1-\alpha_1)\frac{C_{sens,1}}{C_{dl,1}}} \approx R_{i,1}C_{sens,1} \tag{8.12}$$

The pH-sensitivity $S_{i,1}$ of $\varphi_{i,1}$ is given by:

$$S_{i,1} = 2.303\frac{k_BT}{q}\alpha_1 \tag{8.13}$$

Similar equations can be obtained for $\varphi_{i,2}$, τ_2 and $S_{i,2}$ replacing each subscript of 1 by 2. Finally, assuming that the two branches are sufficiently symmetric so that $\tau_1 = \tau_2 = \tau$, $R_{i,1} = R_{i,2} = R_i$ and $I^0_{i,1} = I^0_{i,2} = I^0_i$, we can substract the two differential equations to obtain the following:

$$\frac{\mathrm{d}\Delta\varphi_{i,12}}{\mathrm{d}t} + \frac{\Delta\varphi_{i,12}}{\tau} = -(S_{i,1} - S_{i,2})\frac{\mathrm{d}\Delta\mathrm{pH}}{\mathrm{d}t} \tag{8.14}$$

Here $\varphi_{i,12} = \varphi_{i,1} - \varphi_{i,2}$ is the differential input to the readout circuit.

This equation can be solved for a sinusoidal pH input just as in section 3.10, giving the result:

$$\Delta\varphi_{i,12}(t) = -\frac{S_{i,1} - S_{i,2}}{\sqrt{1 + \frac{1}{\omega^2\tau^2}}}\Delta\mathrm{pH}(t + t_d) + \frac{A_{\mathrm{pH}}(S_{i,1} - S_{i,2})}{\omega\tau + \frac{1}{\omega\tau}}e^{-t/\tau} \tag{8.15}$$

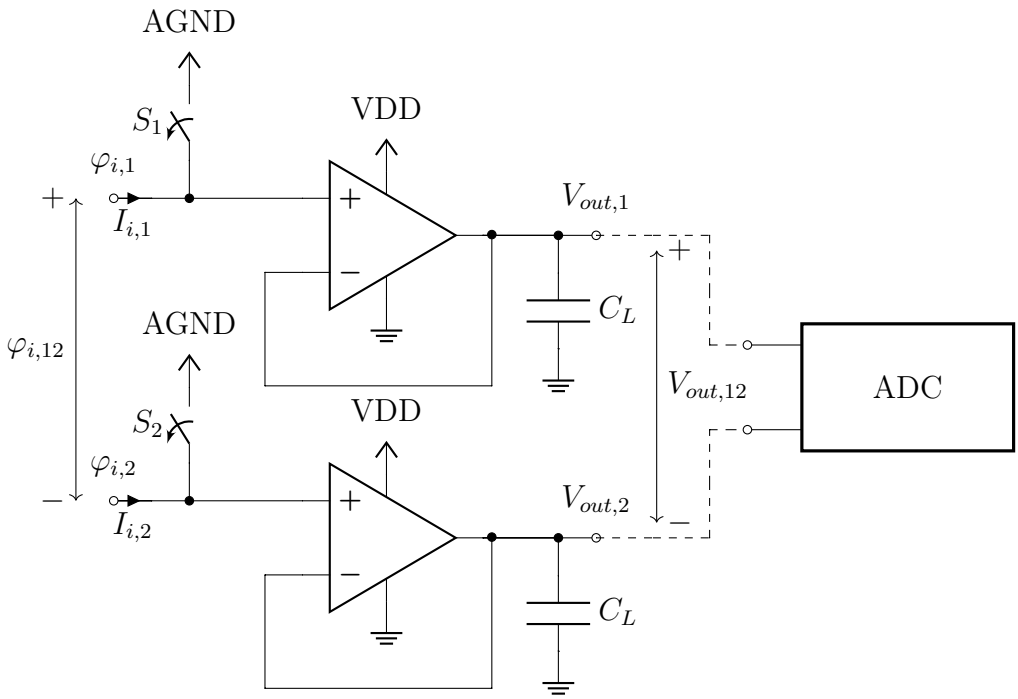


Figure 8.2 – Differential readout circuit.

where $t_d = \frac{1}{\omega} \arctan\left(\frac{1}{\omega\tau}\right)$ is the time shift.

Therefore, the pH-sensitivity of the differential input $\varphi_{i,12}$ is given by $S_{i,12} = S_{i,1} - S_{i,2}$ and the time constant is $\tau \approx R_i C_{sens}$. It can be seen that the leakage current drift terms as well as the reference electrode potential variation were cancelled so that the differential input is not sensitive to these error terms. However, in practice there will always be some mismatch so that perfect cancellation will not occur. Therefore it is necessary to make sure that the circuits are as close and identical as possible to reduce these errors. Even with the differential configuration, the effect of the time constant on the signal amplitude cannot be removed, so it is still important to keep R_i large.

In the case of the REFET discussed in section 2.4.5, the pH-sensitivity of the second dielectric will be close to zero, so $S_{i,2} = 0$ and $S_{i,12} = S_{i,1}$. This will allow not having a reduced pH sensitivity (if $S_{i,1}$ and $S_{i,2}$ were similar, their difference would be small).

8.2 Differential Readout Circuit

The differential frontend was analyzed in the previous section. It was shown that the differential input $\varphi_{i,12}$ varies proportionally to the pH and is insensitive to variations of reference electrode potential and current leakage drift, as long as the R_i is sufficiently large and the two branches are identical except for the pH sensitivity coefficients $S_{i,1}$ and $S_{i,2}$. The net pH-sensitivity of $\varphi_{i,12}$ will be $S_{i,1} - S_{i,2}$. One possible implementation of the differential readout circuit is shown in Figure 8.2.

In this circuit, two identical op-amp buffers are connected to inputs $\varphi_{i,1}$ and $\varphi_{i,2}$, and are biased at the same value of AGND through switches S_1 and S_2 that close simultaneously. Their outputs $V_{out,1}$ and $V_{out,2}$ will connect to the differential input of an ADC. The differential output is $V_{out,12} = V_{out,1} - V_{out,2}$ and the low-frequency relationship between $\Delta V_{out,12}$ and pH will be given by:

$$\Delta V_{out,12}(t) = -\frac{A}{A+1}(S_{i,1} - S_{i,2})\Delta\text{pH}(t) \tag{8.16}$$

where A is the op-amp gain. In the case of an ISFET/REFET pair, the sensitivities will be $S_{i,1} = 2.303\frac{k_B T}{q}\alpha$ and $S_{i,2} = 0$ so that the relationship becomes:

$$\Delta V_{out,12}(t) = -\frac{A}{A+1}2.303\frac{k_B T}{q}\alpha\Delta\text{pH}(t) \tag{8.17}$$

The load capacitor C_L is chosen according to the stability considerations of section 5.1.2. Even though the differential circuit can cancel common-mode sources of noise such as bulk potential variations and identical drift behavior, it will not cancel uncorrelated sources of noise coming from the op-amps, and in fact the flicker noise powers of the two op-amps will add up.

8.3 Simulation Results

The Cadence schematic for the differential readout circuit is shown in Figure 8.3. Two buffer circuits with ideal VCVS components were connected in parallel to two frontend models. The `ph_membrane_params` component is the ISFET `veriloga` model with Ta_2O_5 dielectric, as discussed in section 3.12. The `ref_membrane_params` component is the REFET `veriloga` model with identical parameters except for $N_s = 0$ m^{-2} to simulate a pH-insensitive material.

The op-amp gain was set to $A = 200$ V/V and the input resistance was set to $R_i = 10^{14}$ Ω. The value of AGND was set to 0.1 V, which gives a nonzero leakage current $I_i^0 \approx 1$ fA. This causes a drift coefficient of $\frac{I_i}{C_{sens}} \approx 0.3$ V/Ms

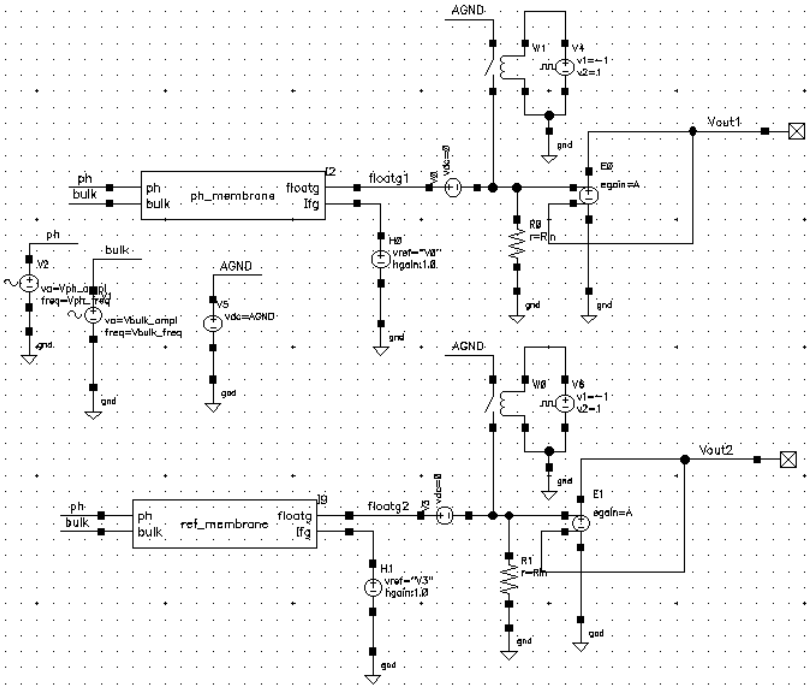


Figure 8.3 – Schematic of differential readout circuit for simulations. The net `bulk` is φ_b, `floatg1` is $\varphi_{i,1}$ and `floatg2` is $\varphi_{i,2}$.

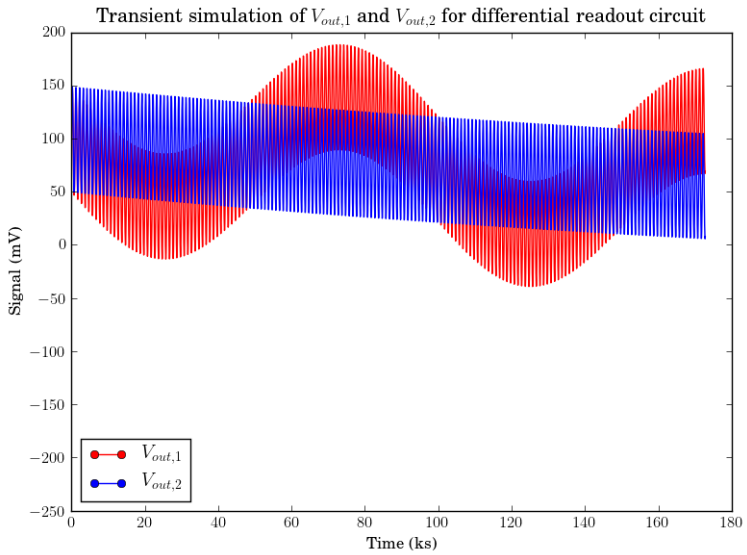


Figure 8.4 – Transient simulation of $V_{out,1}$ and $V_{out,2}$ for $R_i = 10^{14}$ Ω and AGND = 0.1 V.

or around 33 mV after 100 ks. The pH signal is a sine wave of DC offset 7 pH with amplitude of 1 pH, at a frequency of 10 μHz, and the bulk potential φ_b varies sinusoidally around 0 V with an amplitude of 50 mV and a frequency of 1 mHz.

The plots of the transient simulation for $V_{out,1}$ and $V_{out,2}$ are shown in Figure 8.4. It is seen that the bulk potential noise couples into both $V_{out,1}$ and $V_{out,2}$. However, only $V_{out,1}$ is coupled to the pH signal. Both signals also exhibit drift coming from the nonzero leakage current. After taking the differential output $V_{out,12} = V_{out,1} - V_{out,2}$, the plot in Figure 8.5 is obtained. It is seen that the bulk potential noise and the drift have been cancelled, leaving only the pH variation with sensitivity given by equation (8.17) with value 58.2 mV/pH (taking into account the finite op-amp gain).

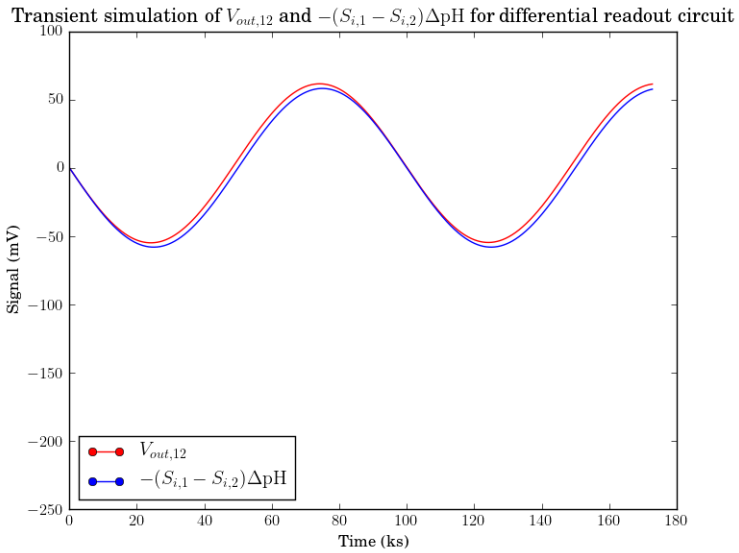


Figure 8.5 – Transient simulation of $V_{out,12}$ and $-(58.2\ \text{mV/pH})\Delta\text{pH}$ for $R_i = 10^{14}\ \Omega$ and AGND $= 0.1$ V.

Chapter 9

Simulations of MOSFETs and Switches

9.1 Gate Leakage Simulations

The TSMC 65nm PDK provides device models for different MOSFET types. For n-channel MOSFETs, the standard `nch` device uses a 1 V supply, while another `nch_25` device uses a 2.5 V supply. One important difference between the `nch` and `nch_25` devices is the larger oxide thickness of the 2.5 V devices. The oxide thickness of the `nch` is well below 5 nm, so its gate leakage currents are expected to be significant. The `nch_25` MOSFET has an oxide that is about twice as thick, above 5 nm. Its threshold voltage is also higher than for `nch`.

As discussed in section 5.1.1, the R_i of the readout circuit must be larger than 10^{14} Ω and the I_i^0 must be below 40 aA. The main contribution to R_i is the parallel combination of the MOSFET gate and switch input resistances. Similarly, I_i^0 is the sum of the MOSFET gate and switch leakage currents. Assuming an ideal switch, it is necessary for the input resistance of the MOSFET to be larger than 10^{14} Ω and for its gate leakage current to be below 40 aA. The gate leakage of `nch` devices was investigated in simulations to obtain an estimate on the gate input resistance R_g of these devices. The plot in Figure 9.1 shows the DC gate current I_g as a function of the gate-to-source voltage V_{GS} for an `nch` device with minimal gate area, using $W = 120$ nm and $L = 60$ nm, $V_{DS} = 1$ V and a temperature of 37 °C. It can be seen that the current is typically on the order of 100 pA, with the estimated value of R_g near $I_g = 0$ being $3 \cdot 10^9$ Ω, which is far from meeting the requirements.

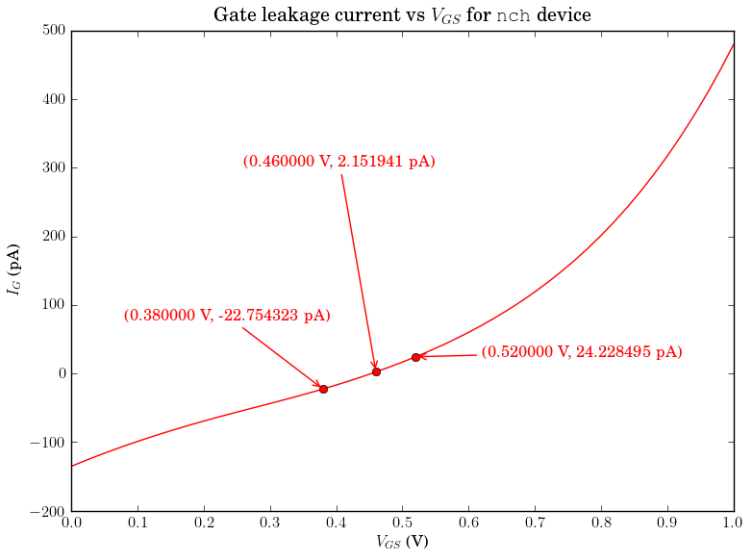


Figure 9.1 – DC sweep of V_{GS} for the `nch` device with $W = 120$ nm and $L = 60$ nm, $V_{DS} = 1$ V.

The simulation of the gate leakage for the `nch_25` devices is shown in Figure 9.2. Again, the size was chosen as small as possible with $W = 400$ nm and $L = 280$ nm, and $V_{DS} = 2.5$ V. It is clear that the current remains below 10 aA (or 10^{-17} A) over the entire range of V_{GS}, and that the gate input resistance remains larger than 10^{17} Ω. On the other hand, it is not clear how accurate the gate current model is for `nch_25` because the default models from the TSMC 65nm PDK had disabled the gate current simulations by setting the `igbmod` and `igcmod` selectors to 0 in the BSIM4 model card of `nch_25`, which control the ability to simulate gate currents. The selectors were modified to 1 for the purpose of simulations, but it is possible that additional inaccuracies are present in the model. Hence a good estimate for the R_g of the `nch_25` can only be obtained by experiment.

9.2 Switch Simulations

The switches to be used in the readout circuit for DC biasing and for the implementation of the switch and buffer readout circuit need to have very low leakage currents. As discussed in section 5.1.1, the R_i of the readout circuit must be larger than 10^{14} Ω and the I_i^0 of the readout circuit must be below 40 aA. The switches are not truly ideal so even when they are open, they will have some input resistance and leakage current, which are in parallel with

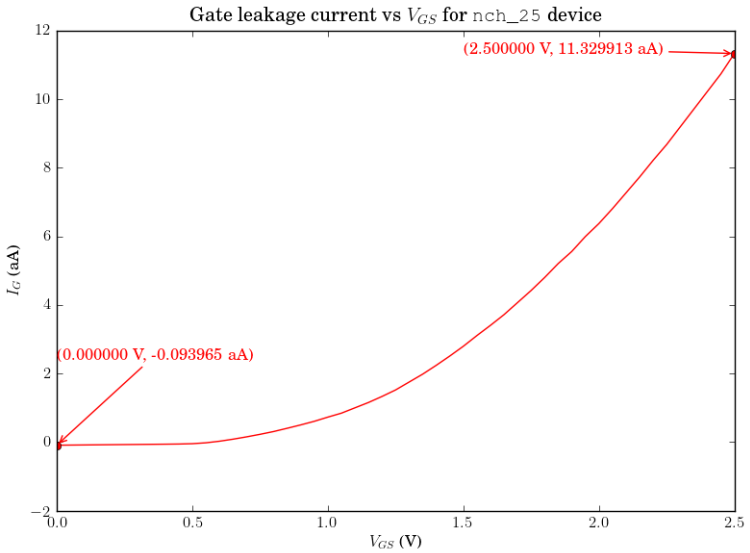


Figure 9.2 – DC sweep of V_{GS} for the `nch_25` device with $W = 400$ nm and $L = 280$ nm, $V_{DS} = 2.5$ V.

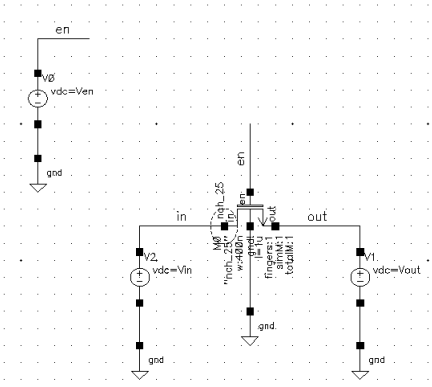


Figure 9.3 – Switch testbench schematic for simulations.

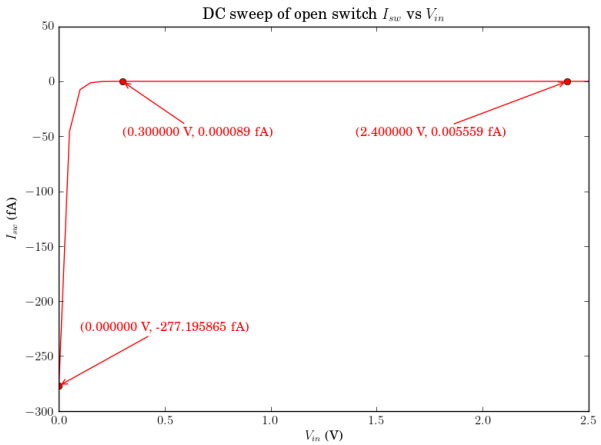


Figure 9.4 – DC sweep of switch current when open.

those of the MOSFET gate. Therefore it is necessary for the input resistance of the switches to be above 10^{14} Ω and for the leakage current of the switches to be below 40 aA.

The switches included in the IC are described in Table 11.1. Simulation results will be shown here regarding their open resistance and closed resistance. The Spectre simulator includes a parameter `gmin` which is used as a minimal conductance placed in parallel on certain high-impedance nodes to avoid DC convergence problems. It was necessary to reduce the value of `gmin` from 10^{-12} S to 10^{-24} S in order to avoid its interference with the simulation. Unfortunately, this simulation is probably not very reliable, because real devices will likely have leakage currents larger than those predicted here.

The testbench used for the simulations of the switch is shown in Figure 9.3. The switch is controlled by V_{en}, being open when $V_{en} = 0$ V and closed when $V_{en} = 2.5$ V. For the simulations, V_{out} was set to 1.3 V, and V_{in} was swept from 0 V to 2.5 V. The current I_D is plotted in Figure 9.4 when it is open, and in Figure 9.5 when it is closed. The open resistance is above 10^{17} Ω over a wide range of voltages, and the closed resistance is around 30 kΩ near 1.3 V. The closed resistance is not ideal, but since the switch is meant to be connected to a high-impedance node with low input capacitance, there was not too much concern in having a low closed resistance.

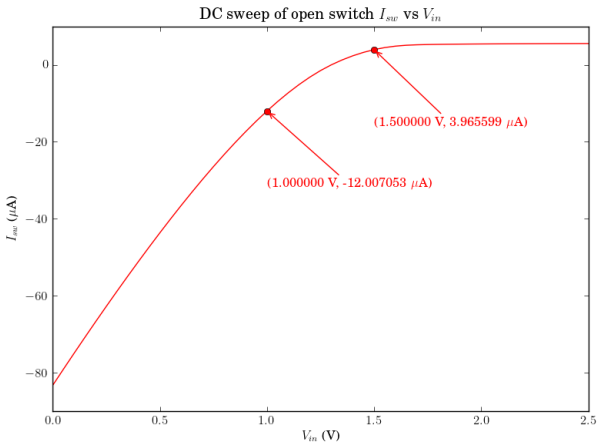


Figure 9.5 – DC sweep of switch current when closed.

Chapter 10

Op-Amp Design

10.1 Requirements

The main requirements for the op-amp are its low input-referred noise, high gain, low input offset voltage, high input resistance and low input leakage current. As shown in Table 4.1, the input pH is expected to vary between 6 and 8, centered at 7. With a pH-sensitivity of 50 mV/pH, φ_i could have variations up to $\pm$50 mV around the DC operating point. Therefore the closed-loop circuit should maintain its linearity for input swings of $\pm$50 mV. The total measurement error of the input should be less than 2.5 mV in order to achieve the resolution of 0.1 pH. Therefore the RMS input-referred noise integrated over the frequency range of 1 μHz and 1 Hz should be less than 2.5 mV.

Since there can be other sources of error coming from nonlinearity, temperature and power supply variation, as well as drift, it is preferable to make sure the input-referred noise falls far below this limit. A conservative design can be made for a resolution of 0.01 pH instead, requiring an input-referred noise below 250 μV. If the ideal transfer function $\frac{A}{A+1}$ is considered for the buffer, the error relative to 1 over a range of $\pm$50 mV is $\pm\frac{50}{A+1}$ mV, so A should be larger than 200 if this error is to be below 250 μV, conservatively.

As mentioned in the analysis of the buffer readout circuit, the R_i of the readout circuit must be above 10^{14} Ω and the I_i^0 of the readout circuit should be below 40 aA. If the switch is assumed ideal, the main contribution to these parameters will come from the op-amp positive input which connects to a MOSFET gate, so the op-amp must have an input resistance above 10^{14} Ω and an input leakage current below 40 aA. This is not a trivial requirement to achieve, especially with very thin oxides. The various design specifications for the op-amp block are summarized in Table 10.1. There was no specific

Power Supply	2.5 V
Input-referred noise (RMS over 1 μHz - 1 Hz)	below 250 μV
Output swing	above $\pm$50 mV
Gain	above 200 V/V
Input resistance (for buffer readout)	above 10^{14} Ω
Leakage current (for buffer readout)	below 40 aA

Table 10.1 – Design specifications for the op-amp block.

constraint on the load driven by this op-amp. Since the goal is to measure its output with an ADC or multimeter, the load should be mostly capacitive and will not pose problems given that the output impedance of op-amps is resistive and small.

The possibility of using a commercial op-amp instead of designing one from scratch was also considered. There already exist very good op-amp designs with low noise, high gain and other desirable properties. It was still decided that designing a custom op-amp could provide valuable information on the feasibility of the project as well as allow more flexibility for integration in implantable pH sensors. A commercial op-amp was used for some of the laboratory measurements described in section 12.9, as a comparison to the fabricated chips.

10.2 Choice of MOSFET Devices

Based on the results of Chapter 9, it was decided to use `nch_25` type MOSFETs for the design. The advantage in using `nch_25` in the current application is to increase the achievable input resistance. It was estimated based on the simulations in section 9.1 that the gate leakage current of the `nch` devices is on the order of 100 pA and their input resistance is on the order of 10^9 Ω. If `nch` had to be used, the buffer readout circuit would not be able to work at low frequencies. The method of reference electrode feedback could allow increasing the effective input resistance by a factor of $A\beta$, but it would require a loop gain $A\beta$ higher than 10^5 V/V, which is very large.

10.3 Choice of Topology

The topology of the op-amp is shown in Figure 10.1. In order to achieve a high gain, it was decided to use a four stage op-amp with three gain stages and one output stage. Each gain stage consists of identical differential pairs with

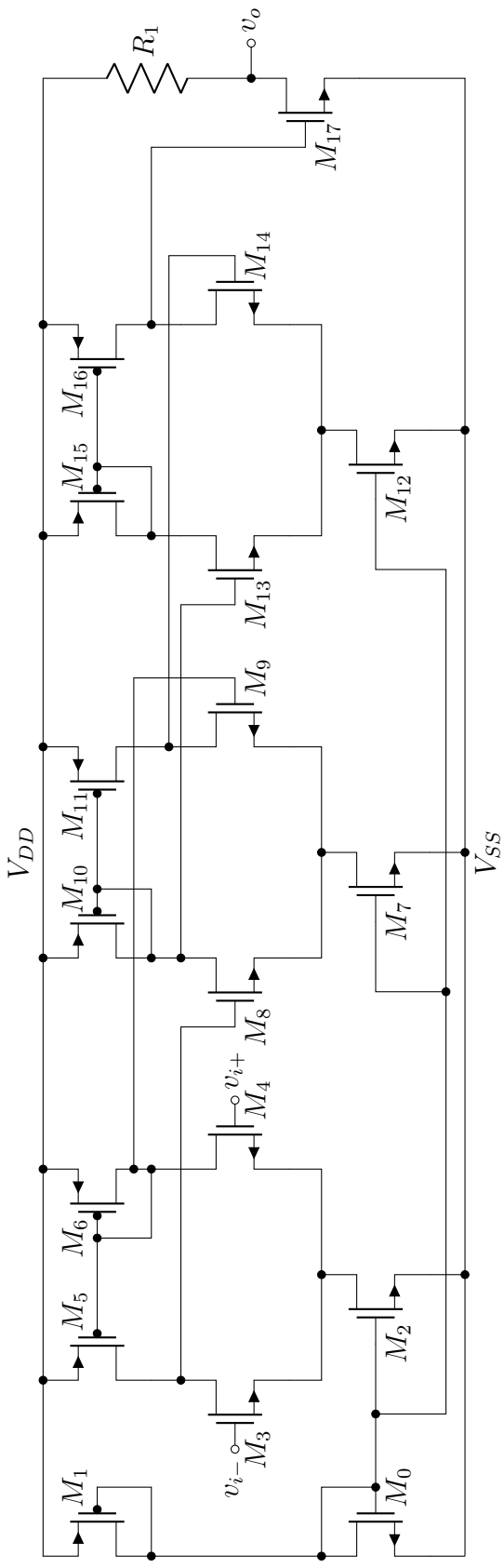


Figure 10.1 – Circuit topology of the op-amp.

active current mirror loads. The differential pair with active load is discussed in [37]. The decision to use three identical differential pairs for each stage was to remove common mode effects from each stage as much as possible, and to simplify the design so that once a single differential pair was designed and known to be working, the remaining stages would be ready as well. In order to reduce the output impedance and provide a single-ended output, an additional output stage was connected. Each stage is biased through current mirrors, and the current reference is built from a diode-connected PMOS and the NMOS current mirror input. The bias current was designed to be 50 μA, but due to the symmetry of the differential pairs, it was expected that some variation on the bias current could be tolerated due to the common-mode rejection.

The first differential stage was inverted in order to compensate for the gain inversion occurring at the output stage. The differential pairs can in principle be used without the diode-connected transistor in the active load (M_6, M_{10} and M_{15}), in which case the differential gain would be twice as high. However, this requires the implementation of a common-mode feedback to properly bias the floating node between the two PMOS gates. For simplicity, it was decided to use the diode-connected transistor structure for biasing purposes. In this case, the nodes connected to the drains of M_6, M_{10} and M_{15} vary little with input voltage, leaving most of the gain to the other branch.

There are many improvements that could be made in future designs. During the design phase, the problems related to the use of high gains discussed in the analysis of the reference electrode feedback circuit were not understood immediately, so the op-amp was designed with the goal of having as high a gain as possible. The decision turns out to be misguided, and future work could improve the op-amp design by choosing a simpler topology with fewer stages.

Another drawback from the use of four stages is that each stage adds a phase shift which causes the op-amp's phase margin to decrease. After four stages, the phase shift crosses 180° at frequencies where the gain A is still larger than 1, causing the op-amp to be unstable in unity-gain configurations unless frequency compensation is added. The decision was made to use an external 1 μF capacitor for this purpose. The capacitor is too large to implement on chip, and it also reduces greatly the bandwidth of the circuit for high frequencies. However the high-frequency range was not an important concern for this design because the device was expected to work with low frequencies up to 1 Hz.

Ideally the current reference should have been external or generated from a bandgap voltage reference discussed in [37] in order to avoid the effect

of process variations, and the ability to tune the current could have helped correcting for such effects on the fabricated devices. However this would increase the complexity of the design, and it was decided that the simpler biasing method would be used. This is another improvement that could be done in future designs. Simulation results of the op-amp will be shown in section 10.6.

10.4 Component Parameter Values

The transistors in the op-amp have the width W, length L and number of fingers as parameters controllable by the designer. For TSMC 65nm, the smallest L and W value allowed is 60 nm. The size of each transistor in the op-amp is shown in Table 10.2, where W represents the total width when there are multiple fingers. The value of the resistor R_1 is shown in Table 10.3. The choice of parameter values was done while considering the various constraints of flicker noise, gate input resistance, gain and output swing. Some design tradeoffs can be mentioned about the sizes of the input transistors M_3 and M_4. Larger areas for these transistors help reduce the flicker noise according to the intuition from equation (2.9). The larger area also allows better matching of the transistors [37]. On the other hand, increasing the gate area will also decrease the gate input resistance. But since the `nch_25` had very high gate input resistance based on the simulations, increasing the area was preferable. The biasing was chosen so that the DC operating point of each differential stage would be near 1.3 V, which is halfway between the power supplies at 0 V and 2.5 V. The number of fingers was selected mainly based on maintaining a reasonable aspect ratio for the layout.

10.5 Analysis of Op-Amp Design

10.5.1 Total DC gain

The gain of each differential stage can be estimated using AC analysis. In a differential pair, the node above the current source can be modeled as a virtual ground when the current source has high output resistance. In that case, the gain of the differential pair is given by [37]:

$$A_{v,diff} = g_m(r_o||R_L) \approx \frac{1}{2}g_m r_o \tag{10.1}$$

where g_m is the transconductance of either of the input MOSFETs, r_o is its output resistance and R_L is the load resistance. The factor of $\frac{1}{2}$ accounts for

Component	Type	W (μm)	L (μm)	Fingers
M_0	`nch_25`	5.6	2	4
M_1	`pch_25`	2.67	1	1
M_2	`nch_25`	0.4	2	1
M_3	`nch_25`	10	0.4	4
M_4	`nch_25`	10	0.4	4
M_5	`pch_25`	0.4	1.64	1
M_6	`pch_25`	0.4	1.64	1
M_7	`nch_25`	0.4	2	1
M_8	`nch_25`	10	0.4	4
M_9	`nch_25`	10	0.4	4
M_{10}	`pch_25`	0.4	1.64	1
M_{11}	`pch_25`	0.4	1.64	1
M_{12}	`nch_25`	0.4	2	1
M_{13}	`nch_25`	10	0.4	4
M_{14}	`nch_25`	10	0.4	4
M_{15}	`pch_25`	0.4	1.64	1
M_{16}	`pch_25`	0.4	1.64	1
M_{17}	`nch_25`	1	0.5	1

Table 10.2 – Transistor sizes used for op-amp.

Component	Type	Resistance
R_1	`rnwsti`	30 kΩ

Table 10.3 – Resistor values used for op-amp.

the fact that r_o is in parallel with the output resistance of the active load current mirror PMOS device, which is of the same order as r_o. The values of g_m and r_o can be substituted from the model equations (2.3) and (2.4), and we obtain an expression for the gain in terms of design parameters:

$$A_{v,diff} \approx \frac{1}{2} g_m r_o = \frac{V_{DS} + \frac{1}{\lambda}}{2(V_{GS} - V_T)} \tag{10.2}$$

In the subthreshold region where $V_{GS} < V_T$, different models for g_m and r_o apply as given in equations (2.6) and (2.7). In that case, the gain is given by:

$$A_{v,diff} \approx \frac{1}{2} g_m r_o \approx \frac{1}{2n} e^{\frac{qV_{DS}}{k_B T}} \tag{10.3}$$

From these equations, it appears that the highest gain is achieved when V_{GS} is close to the threshold voltage V_T, and that the gain becomes somewhat independent of V_{GS} in the subthreshold region, while increasing with V_{DS}. The MOSFETs were indeed biased with a value of V_{GS} somewhat below V_T to increase the gain and to leave more headroom for biasing the current sources.

The last stage is a common-source amplifier with a resistive load (a resistor was used instead of a MOSFET as the load in order to have a low output resistance). This stage has a gain $A_{v,cs} = g_{m,17} R_{out}$, and the total gain of the op-amp is given by:

$$A_{DC} = A_{v,diff}^3 A_{v,cs} \tag{10.4}$$

Unfortunately, the estimates coming from equations (10.2) and (10.3) require parameters for a simplified model, while the simulations use more complex models from which it is not easy to calculate values of the simplified model parameters. Therefore, the design relied on the simulation results, based on the assumption that the models provided in the simulator will be correct, but using intuition from the simplified models to guide the choices.

One could expect $A_{v,diff}$ to be around 50 V/V at best, and the last stage will have a low gain less than 10 V/V (because the transistor M_{17} is biased with a large V_{GS} in order to reduce its output resistance). Therefore, the total gain would be somewhere around 10^6 V/V. In reality the gain will likely be lower because simulation results may give unrealistically high gains assuming perfectly matched components and precise biasing.

10.5.2 Poles and frequency compensation

The dominant poles of the op-amp will most likely be introduced by the transistors at the input of each differential pair stage, that is M_3-M_4, M_8-M_9, M_{13}-M_{14}. These transistors have various parasitic capacitances, including

gate-source C_{gs} and gate-drain C_{gd} capacitances. These capacitances are increased with larger gate areas, so the bandwidth of each stage will decrease with larger gate areas. However, the noise will be reduced with larger gate areas according to equation (2.9), leading to a design tradeoff. Due to the high gain of each stage, it is expected that the Miller effect will lead to multiplying C_{gd} by the stage gain, leading to a total gate capacitance estimate of:

$$C_g = C_{gs} + A_{v,diff} C_{gd} \tag{10.5}$$

At each stage, an output resistance of r_o will be present from the previous stage, leading to a pole at frequency near $f_{p1} = \frac{1}{2\pi r_o C_g}$. With $r_o \approx 400$ kΩ and $C_{gd} \approx 2$ fF, $C_{gs} \approx 15$ fF (values obtained from simulations at the DC operating point of M_3), the estimate for C_g is 115 fF and the estimate for f_{p1} is 3.5 MHz. Of course there are multiple stages and calculating the actual location of poles will require taking into account coupling between stages. The pole values will be obtained in the simulation results. Only the first two poles will be considered as dominant, because the higher frequency poles will be located far enough for the gain to be below 0 dB at these frequencies.

According to this estimate, the op-amp open-loop gain will remain at its DC value for frequencies below f_{p1}, and will start to roll off at 20 dB/dec until the second pole is reached. The dominant pole frequency compensation method was described in section 5.1.2, and the simulations involving open-loop and frequency compensation are shown in section 10.6.2. For a single pole, the phase shift reaches 90° near f_{p1}, and tends to 180° for larger frequencies. However, the presence of a second pole at f_{p2} will lead to an additional phase shift of 90° before reaching f_{p2}. Based on an estimate of the gain being $A_{DC} = 10^6$ V/V and using equation (5.5) with $M = 2\pi \times 3.5$ MHz and $R_{out} = 30$ kΩ (from last stage of op-amp), the estimated value of C_L is $C_L > 1.5$ μF to allow the op-amp to be stable in a unity-gain configuration.

10.5.3 Output resistance and linearity

The last stage was used to reduce the output resistance of the op-amp to around 30 kΩ, and to improve the linearity by increasing the upper range of V_{out} without being limited by the saturation voltage of the PMOS devices in previous stages.

10.6 Simulation Results

The op-amp was simulated in Cadence in the open-loop configuration as shown in Figure 10.2. The `iref` block consists of transistor M_1 from Figure

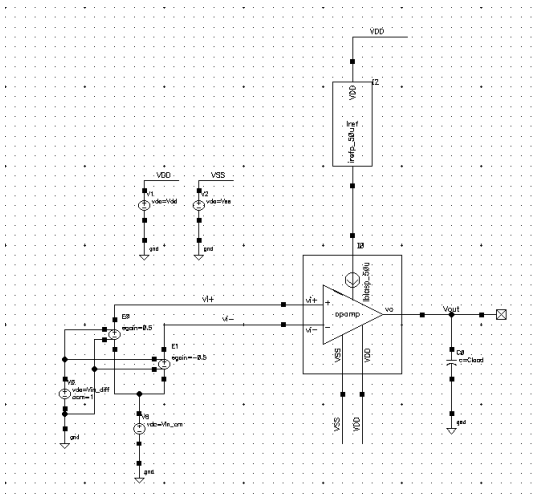


Figure 10.2 – Schematic of op-amp testbench for open-loop simulations.

10.1, and the `opamp` block contains the remaining transistors. The inputs of the op-amp are controlled through two dependent voltage sources that allow setting the common-mode $V_{in,CM}$ and the differential input $V_{in,diff}$ separately. The power supplies are $V_{DD} = 2.5$ V and $V_{SS} = 0$ V. The output is loaded with a capacitor C_L.

10.6.1 DC analysis

At DC, the bias current to the op-amp is 50 μA, and the differential pairs each have an output of around 1.4 V when $V_{in,CM} = 1.3$ V. Due to the common-mode rejection, this allows the differential pairs to be connected in sequence without affecting their DC bias noticeably. Each differential pair takes around 3.6 μA of current through its current tail, and the last stage has a DC bias current of 70 μA. The gates of the current sources are biased at 1 V, and their drains are biased at around 0.7 V. The plot in Figure 10.3 shows a DC sweep of $V_{in,diff}$ from -10 μV to 10 μV. From the figure it is shown that the input offset is around 1.7 μV, and that the output of the op-amp ranges from 150 mV to 2.3 V approximately. However it should be remembered that the real op-amp will suffer from mismatch and process variations that could affect these results.

10.6.2 AC analysis

The AC analysis of the op-amp was done while fixing the operating points $V_{in,CM} = 1.3$ V and $V_{in,diff} = 1.7$ μV to bias the op-amp in the high gain

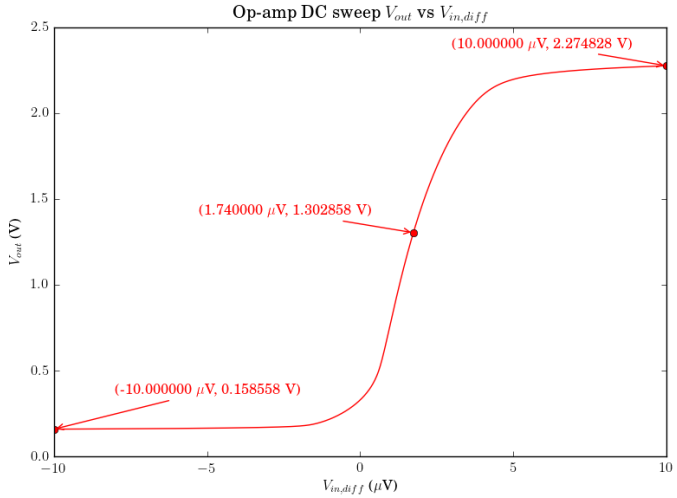


Figure 10.3 – DC sweep of op-amp $V_{in,diff}$.

region. The plot in Figure 10.4 shows the magnitude and phase of the transfer function $A(s)$ of the op-amp for frequencies between 0.1 Hz and 1 GHz, where the load capacitance was set to 0 F (open circuit). From the figure it is seen that the low-frequency gain is around 115 dB or about 10^5 V/V, which is around the estimate of section 10.5.1 with $A_{v,diff} \approx 50$ V/V and $A_{v,cs} \approx 4$ V/V.

The first pole occurs at around 300 kHz (which is lower than estimated in section 10.5.2 by a factor of 10), and the unity gain frequency is around 500 MHz. Unfortunately, the gain is still too high when the phase reaches 180°, which means that at this frequency the op-amp would be unstable in unity-gain feedback. The simplest way to resolve this problem is to introduce a large load capacitor C_L to introduce a low-frequency pole that lets the gain fall below 1 V/V before the phase has reached 180°. This is the dominant pole frequency compensation method. In order for the gain to become 1 V/V before the second pole (near 10 MHz), the dominant pole would need to be placed at around 10 Hz. The output impedance of the op-amp is around 30 kΩ, so the capacitance C_L should be larger than 1 μF, which cannot be fabricated on chip due to the limited area. This problem was mentioned in section 10.3. This bound for C_L is close to that estimated in section 10.5.2.

The AC analysis using a load capacitor of 2 μF is shown in Figure 10.5. The use of large load capacitors also has the effect of reducing the bandwidth, however the application does not require frequencies higher than 1 Hz so this was not a main concern. In closed-loop feedback, the bandwidth will be

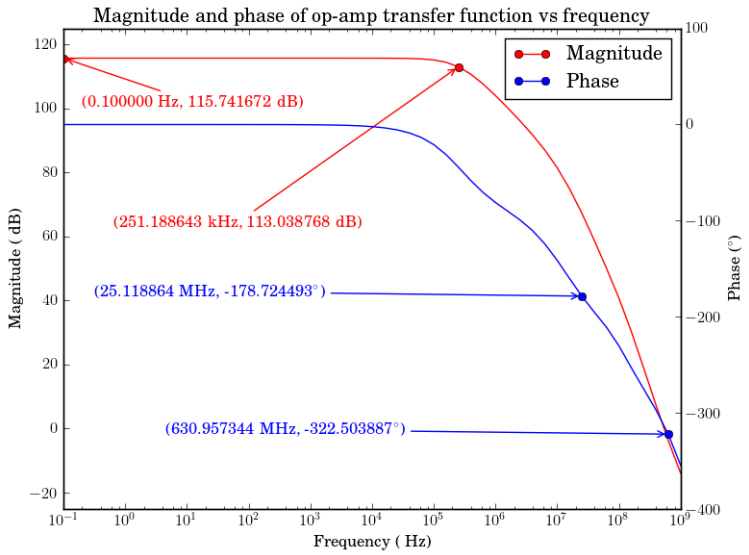


Figure 10.4 – AC magnitude and phase of op-amp transfer function for C_L = 0 F.

extended by the op-amp gain, however the op-amp has a maximal output current I_{max}, which limits the slew rate by $\left|\frac{\mathrm{d}V_{out}}{\mathrm{d}t}\right|_{max} = \frac{I_{max}}{C_L}$.

10.6.3 Unity-gain configuration

The op-amp was simulated in the unity-gain configuration to verify its linearity, noise, input resistance and step response. The Cadence schematic of this configuration is shown in Figure 10.6. The linearity of the op-amp was verified by a DC sweep of the input voltage V_{in}, as shown in Figure 10.7. The error between V_{in} and V_{out} is plotted in Figure 10.8. It is clear that the op-amp is sufficiently linear over the desired range of inputs, with its maximal error below 250 μV. The input current I_{in} was also plotted as a function of V_{in} in Figure 10.9. The input current does not vary by more than 40 aA over the entire range, which gives an estimate of R_i above $6 \cdot 10^{16}$ Ω.

The input-referred noise PSD is shown in Figure 10.10, and as expected it is dominated by $1/f$ noise at low frequencies. The integrated RMS noise between 1 μHz and 1 Hz was calculated to be 45 μV RMS.

Finally, the step response of the op-amp in unity-gain feedback was simulated and shown in Figure 10.11, using a step of V_{in} from 1.3 V to 1.5 V with a rise time of 1 μs and a delay of 10 s. The output follows the input closely, and no noticeable ringing or instability is present. A pole-zero analysis did not find poles with positive real components, so the system appears to be

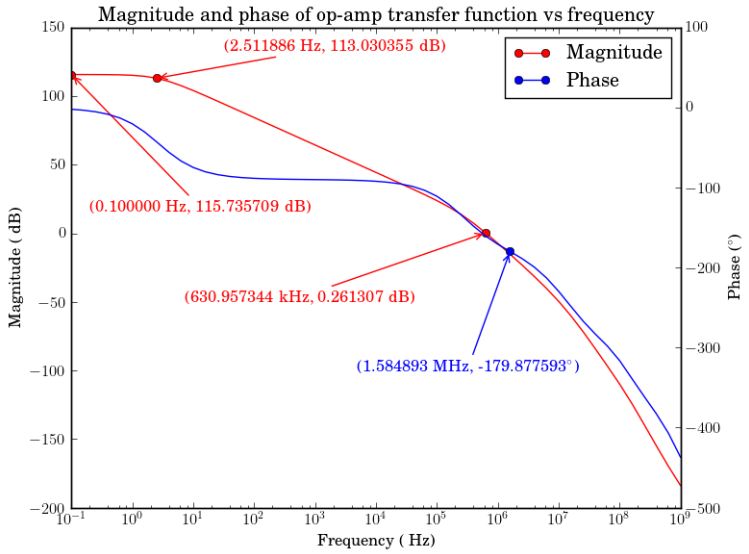


Figure 10.5 – AC magnitude and phase of op-amp transfer function for C_L = 2 μF.

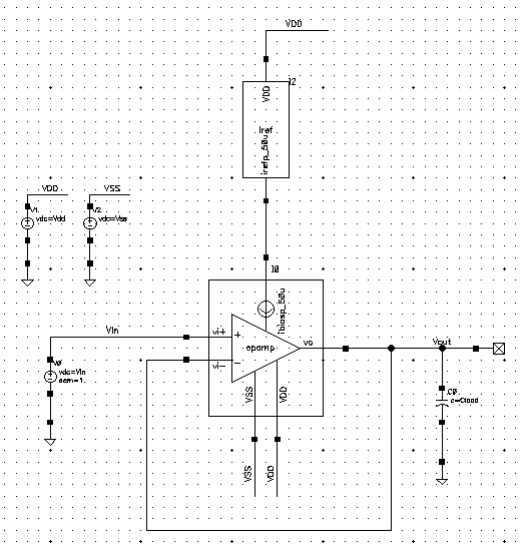


Figure 10.6 – Schematic of op-amp testbench for closed-loop simulations.

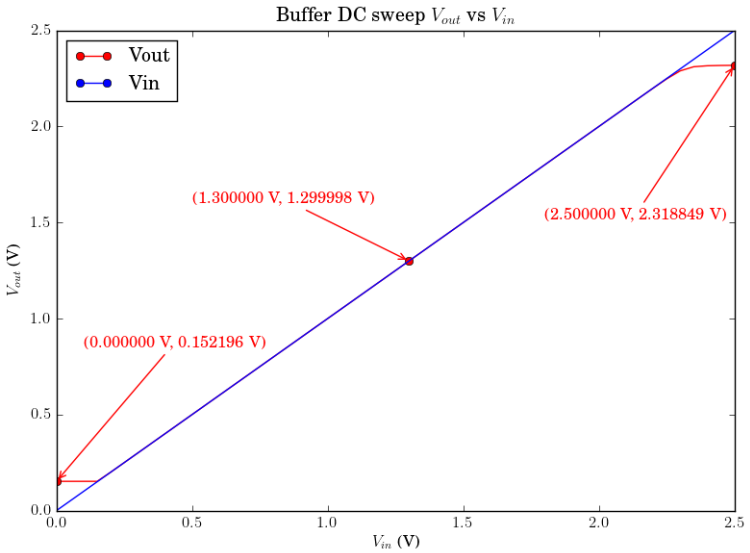


Figure 10.7 – DC sweep of V_{in} for op-amp in unity-gain configuration.

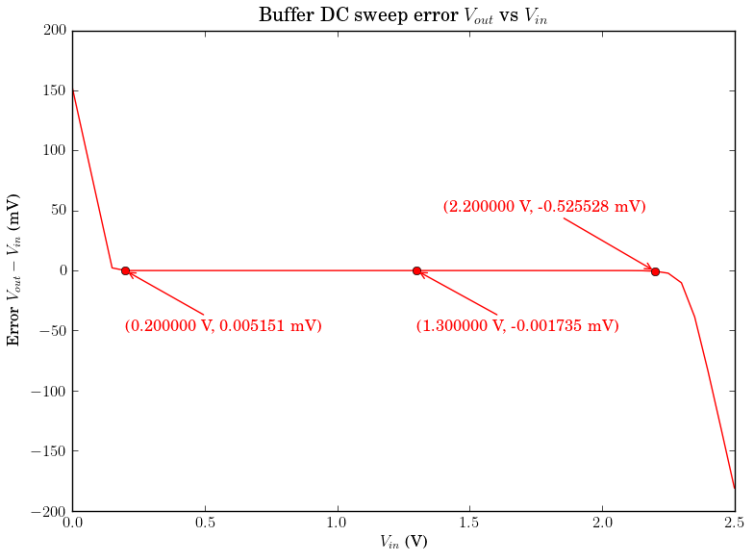


Figure 10.8 – Error in DC sweep of V_{in} for op-amp in unity-gain configuration.

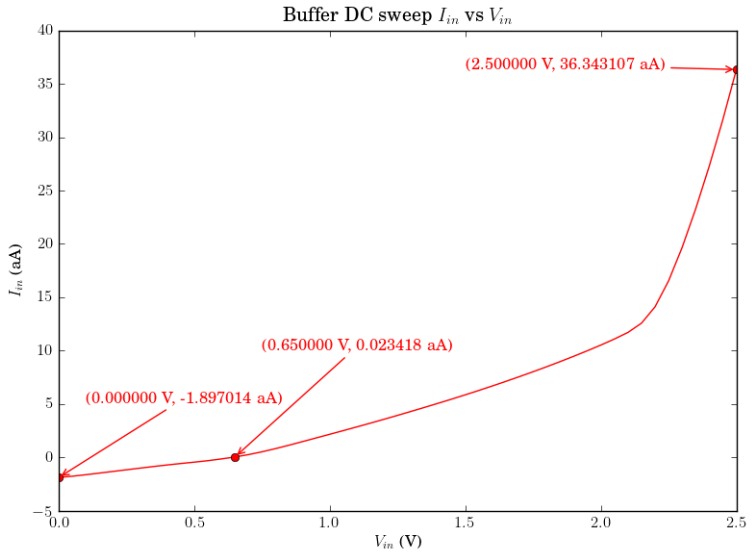


Figure 10.9 – Input current of op-amp in unity-gain configuration.

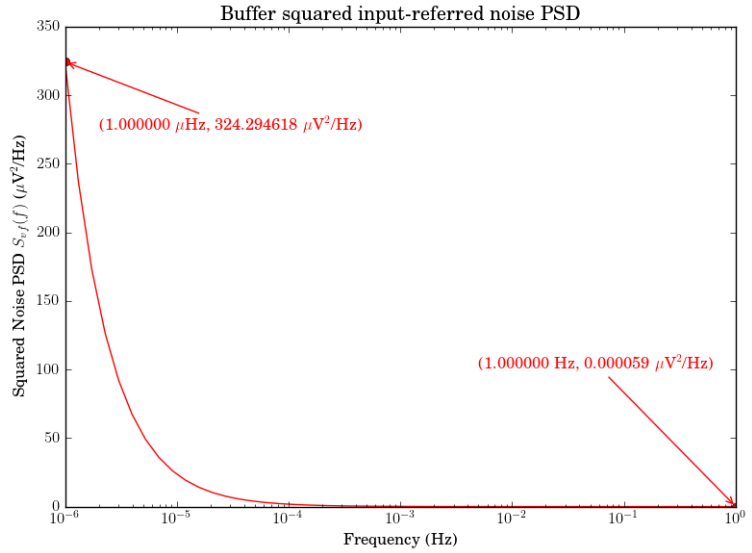


Figure 10.10 – Input-referred noise of op-amp in unity-gain configuration.

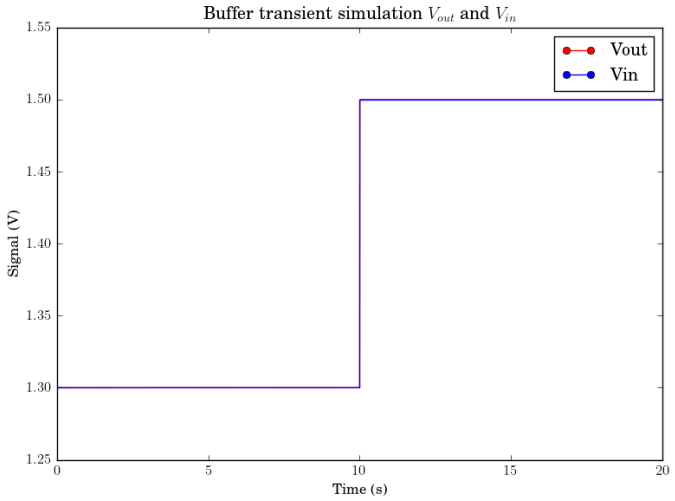


Figure 10.11 – Step response of op-amp in unity-gain configuration.

stable. The first pole occurs at 110 kHz, and the unity gain is maintained over the required bandwidth of 1 μHz to 1 Hz.

10.6.4 Mismatch and process variation

As mentioned in section 10.6.1, the simulation results obtained so far were done on ideal schematic models where the parameters of every transistor can be precisely controlled by the simulator. In reality, the fabrication of integrated circuits involves many sources of error due to process variation that can affect the parameters of identical devices on different chips or even on the same chip. In order to account for such parameter variation and to make sure that the design is robust, it is useful to run mismatch simulations over different process corners. This is typically achieved by using statistical models of parameter variation provided by the foundry, in combination with Monte-Carlo simulations.

The TSMC 65nm PDK provides the `nch_25_mac` device that is meant to be used for mismatch simulations. A copy of the op-amp block was made replacing every transistor from the `nch_25` to the `nch_25_mac` models, and the `stat_mis_25` section of the device models provides the statistical parameters. In addition, process corners labeled `TT` (typical), `FF`, `SS`, `FS` and `SF` include global variation effects across all devices on the same chip. The Monte-Carlo simulations were run with 200 trials over each process corner, resulting in a total of 1000 trials, using the op-amp in unity-gain configuration.

The DC offset, gain and input-referred noise (RMS integrated over 1 μHz to 1 Hz) were calculated for each trial. The DC offset is the difference between V_{out} and V_{in} when $V_{in} = 1.3$ V, and the gain should be ideally 1. The results are summarized in Table 10.4, which shows the variation of each output over all process corners and mismatch trials. Gains larger than 1 may appear strange, but they can arise in presence of asymmetries between the positive and negative inputs of the op-amp, leading to a relation $V_{out} = AV_{in+} - BV_{in-}$. Such asymmetries can be introduced by mismatch. The table also shows the variation of V_{out} with a temperature sweep from 0 °C to 100 °C, where the variation is calculated by $\max_{0 \leq T \leq 100} |V_{out} - V_{in} - V_{os}|$ with V_{os} being the DC offset at $T = 37$ °C. Similarly, the power supply variation is shown where V_{DD} was swept from 2.3 V to 2.7 V.

Based on these results, it was concluded that the op-amp could meet all design specifications from Table 10.1, while remaining robust under different conditions.

Output	Max	Mean	Median	Min	Stddev
DC offset	15 mV	360.9 μV	-109.7 μV	-14.92 mV	4.831 mV
Gain	1.002 V/V	1 V/V	1 V/V	998.9 V/V	481.6 μV/V
Noise (RMS 1 μHz to 1 Hz)	50.4 μV	45.36 μV	45.22 μV	41.01 μV	2.638 μV
Temperature variation (0 °C to 100 °C)	268.7 μV	56.69 μV	42.37 μV	1.358 μV	45.19 μV
V_{DD} variation (2.3 V to 2.7 V)	624.7 μV	151.4 μV	122.2 μV	1.956 μV	119.7 μV

Table 10.4 – Monte-Carlo simulation results for op-amp.

Chapter 11

Full IC Design

11.1 IC Layout and Pad Design

In order to be able to test the op-amp as well as the differential configuration discussed in Chapter 8, the IC contains two identical op-amps of the type designed in section 10. One of the op-amps is intended to be connected to a pH-sensitive dielectric, and the other op-amp is meant to be connected to a pH-insensitive material that only senses variations of the bulk electrolyte potential φ_b. It was decided that the differential configuration would be used for the IC design because of its advantage in common-mode noise reduction, and the option of testing the individual buffers separately as well.

In addition to the op-amps, the IC also includes two identical MOSFET switches made from a single `nch_25` with parameters shown in Table 11.1. The goal was to see how much leakage would be obtained from electronic switches using TSMC 65nm, and to see whether they could be used for the purpose of the DC biasing and switching with acceptable performance. Also, three single MOSFETs were included with their terminals directly connected to bondpads. The parameters of these MOSFETs are given in Table 11.2. These MOSFETs were included in case the op-amp circuits would not work on the fabricated ICs due to unforeseen problems, and they would allow a backup plan for testing. Among these three MOSFETs, there are two identical NMOS transistors (`nisfet`, `nrefet`) and one PMOS transistor (`pisfet`). The `nisfet` and `pisfet` transistors would connect to pH-sensitive dielectrics while `nrefet` would connect to a pH-insensitive dielectric. The size of `pisfet` was chosen so that its transconductance matches that of the NMOS devices. The reason for the scaling is due to the mobility of holes being lower than that of electrons, which comes into play in equation (2.3). In order to have a possibility to test resistive feedback circuits, two identical sets of resistor di-

Component	Type	W (μm)	L (μm)	Fingers
`switch_ph`	`nch_25`	0.4	1	1
`switch_ref`	`nch_25`	0.4	1	1

Table 11.1 – Switch transistor parameters.

Component	Type	W (μm)	L (μm)	Fingers
`nisfet`	`nch_25`	20	10	2
`nrefet`	`nch_25`	20	10	2
`pisfet`	`pch_25`	83	10	2

Table 11.2 – Parameters of the isolated transistors.

viders were also included, where each divider uses 100 kΩ and 20 kΩ `rnwsti` resistors for a ratio of 5:1.

Finally, the IC must also include the pad ring consisting of all the bondpads that will provide the interface between the chip and the exterior. Most bondpads come with electrostatic discharge (ESD) protection circuitry using reverse-biased diodes, whose purpose is to provide discharge paths for ESD events where the pad voltage may rise above V_{DD} or below V_{SS}, thus protecting the more sensitive components in the chip. However it was decided that these diodes would not be placed on the bondpads connected to the gates of the positive op-amp inputs, as well as the gates of the three isolated transistors. The reason was to avoid problems where the diodes add their own impedance in parallel to the input resistance of the gates, thus contributing to the leakage and loading effects discussed previously. This decision comes at the risk of increased device sensitivity to ESD events, so care would have to be taken during testing. In order to be able to wirebond the devices using the machine available in the lab, the bondpads had to be sufficiently large and spaced out. Their size is 80 μm $\times$ 90 μm, and the spacing is 40 μm for most pads. The five pads connected to the two op-amp positive inputs and three transistor gates were placed together on one side of the IC with a spacing of 70 μm, in order to facilitate future connections with the sensing elements through wirebonding. There is a total of 28 pads on the IC, in addition to a dummy pad which had to be added to meet design rule checks (DRC). The final layout of the IC (not including the dummy fills) is shown in Figure 11.1, and the layout of the op-amp (without M_1) is shown in Figure 11.2. The list of pins is shown in Table 11.3. The pin numbers are related to the wire-bonding on the DIP-40 sockets used to test the fabricated ICs.

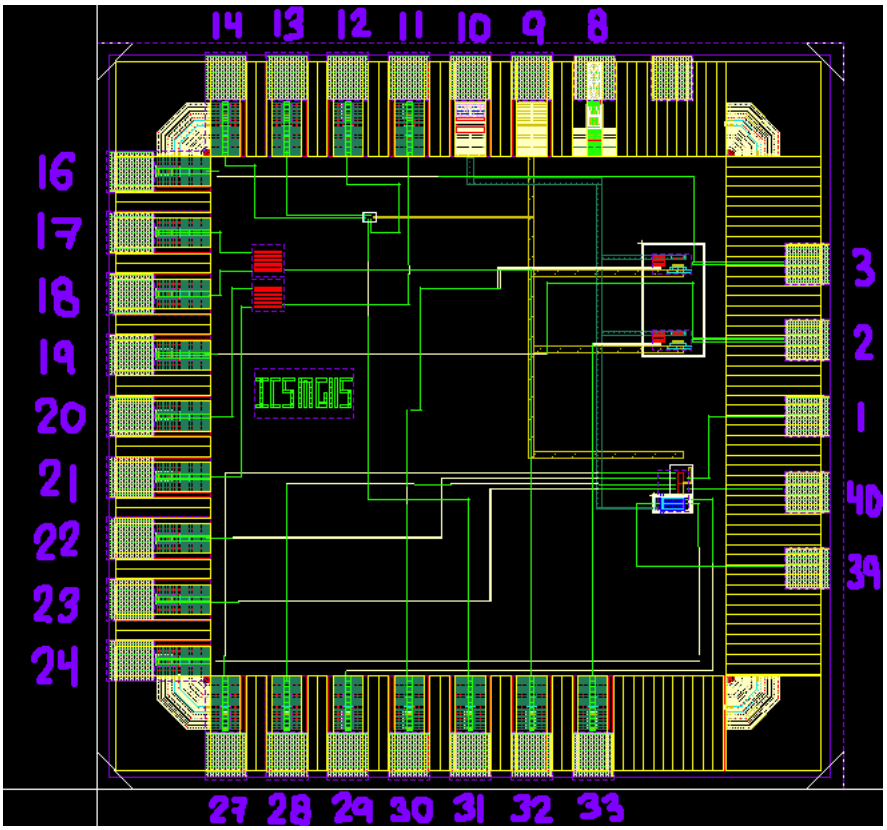


Figure 11.1 – Layout of the IC.

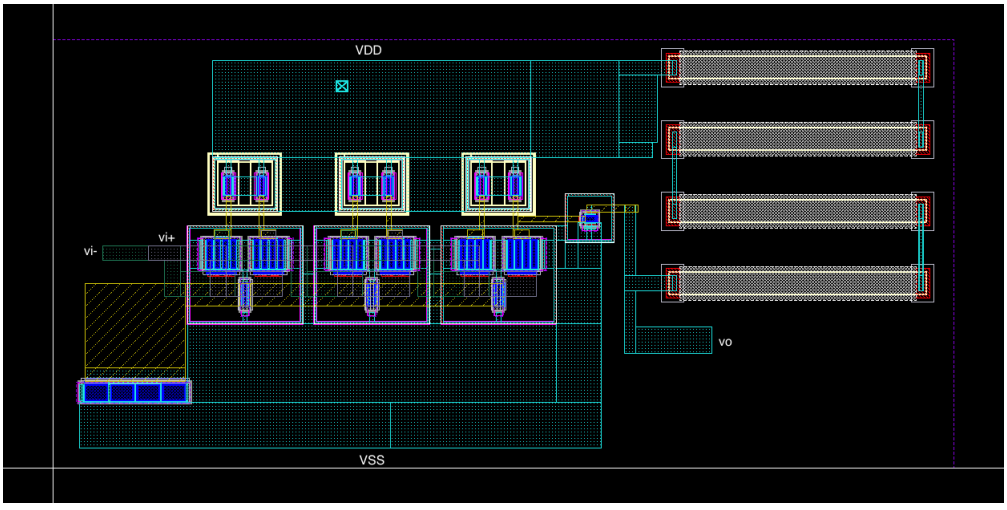


Figure 11.2 – Layout of the op-amp.

Pin #	Name	Description
1	nisfet_g	Gate of isolated NMOS for ISFET
2	vref_in+	Positive input of reference op-amp
3	vph_in+	Positive input of pH op-amp
8	VSS!	Global VSS net
9	AVSS	VSS net for analog blocks
10	TACVDD	Global VDD net
11	fb_out_ref	Output of resistor divider for reference op-amp
12	sw_out_ref	Output of switch for reference op-amp
13	reset	Reset input for switches
14	AGND	DC bias voltage for switches and resistor feedback
16	vph_in-	Negative input of pH op-amp
17	fb_in_ph	Input of resistor divider for pH op-amp
18	fb_ref_ph	DC reference of resistor divider for pH op-amp
19	vref_in-	Negative input of reference op-amp
20	fb_in_ref	Input of resistor divider for reference op-amp
21	fb_ref_ref	DC reference of resistor divider for reference op-amp
22	nisfet_d	Drain of isolated NMOS for ISFET
23	nrefet_d	Drain of isolated NMOS for REFET
24	pisfet_d	Drain of isolated PMOS for ISFET
27	nisfet_s	Source of isolated NMOS for ISFET
28	nrefet_s	Source of isolated NMOS for REFET
29	pisfet_s	Source of isolated PMOS for ISFET
30	vph_out	Output of pH op-amp
31	sw_out_ph	Output of switch for pH op-amp
32	fb_out_ph	Output of resistor divider for pH op-amp
33	vref_out	Output of reference op-amp
39	pisfet_g	Gate of isolated PMOS for ISFET
40	nrefet_g	Gate of isolated NMOS for REFET

Table 11.3 – Pin list of the IC.

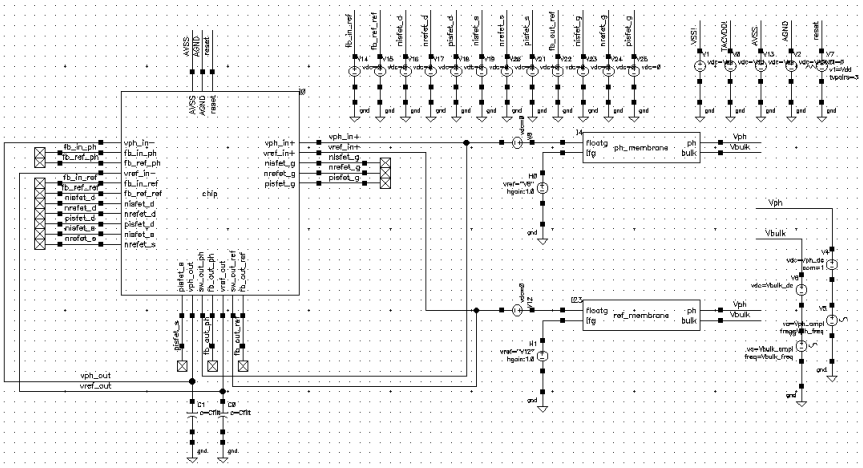


Figure 11.3 – Schematic of full IC testbench.

11.2 Simulation Results

Simulations of the full chip were performed, using the differential configuration with the two op-amps in unity-gain configuration as in the buffer readout circuit. One op-amp was connected to the ISFET model discussed in section 3.12, and the other op-amp was connected to the REFET model, which was made ideal by setting `Nsil = 0` and `Nnit = 0` in the `veriloga` model. This causes the model to simulate a complete lack of surface binding sites, leading to zero pH sensitivity. The schematic of the chip testbench is shown in Figure 11.3. The pH signal and bulk potential φ_b are controlled directly by ideal voltage sources as before. The output of the pH-sensitive circuit is `vph_out` and the output of the pH-insensitive circuit is `vref_out`. Both outputs are loaded with 2 μF capacitors for frequency compensation.

The power supplies were set to $V_{DD} = 2.5$ V, $V_{SS} = 0$ V and AGND = 1.3 V. The voltage AGND connects to the MOSFET switches in the chip, which set the initial value of the inputs `vph_in+` and `vref_in+` to 1.3 V. The switches are controlled by the `reset` input of the chip, which closes the switches at 2.5 V and opens them at 0 V. The switch outputs are `sw_out_ph` and `sw_out_ref`, and they connect to `vph_in+` and `vref_in+` respectively. The switches are closed for 1 second at the beginning, and are then open for the rest of the simulation. The remaining pins of the chip were grounded to ensure DC convergence in simulations.

The transient simulation was run for 10^6 seconds (11 days) to see how much error accumulates over long periods of time according to the simulation. The pH signal was set as a sine wave centered at pH = 7, with amplitude ± 0.5 pH and a frequency of 1 μHz. The bulk potential φ_b was a sine wave

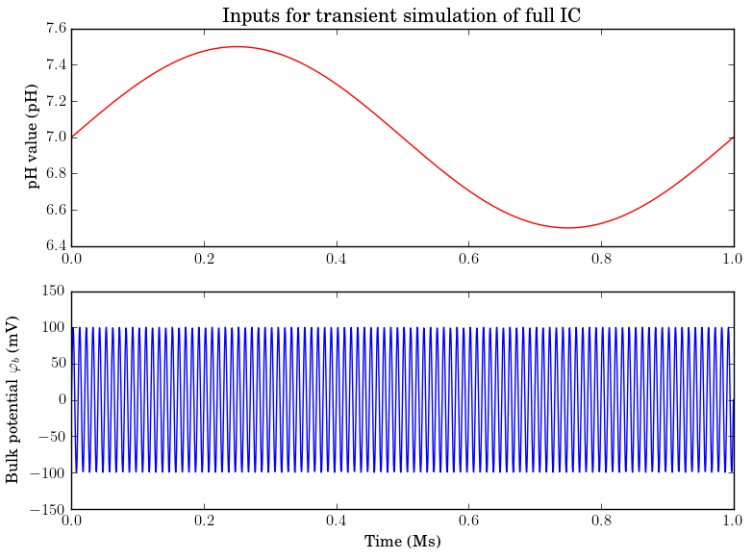


Figure 11.4 – Inputs for transient simulation of full IC.

centered at 0 V with an amplitude of 0.1 V and a frequency of 10 μHz, which is meant to represent noise from the reference electrode. The plots of the input signals are shown in Figure 11.4. The plots of the output signals are shown in Figure 11.5. The differential output $V_{out,ph} - V_{out,ref}$ is plotted in Figure 11.6 and compared to the expected value of $-S_i\Delta\text{pH}$ with $S_i = 58.5$ mV/pH. Finally, the error relative to pH is shown in Figure 11.7. The error is calculated as $\frac{V_{ph,out}-V_{ref,out}}{-58.5\text{ mV/pH}} - \Delta\text{pH}$. This uses the pH sensitivity of -58.5 mV/pH estimated previously for Ta_2O_5. As seen, the error stays below 0.005 pH over the entire period, and a pH resolution of 0.1 pH can therefore be maintained over 2 days. It is also clear that the differential configuration can help reduce the sensitivity to bulk potential variations. There is a slight drift caused by the fact that when the switch closes, charge flows into the floating gate node, leading to some initial charge Q_i^0. After the switch is opened, this charge will slowly leak through the MOSFET gate and the switches. However, since the two op-amp buffer circuits for the ISFET and REFET are identical, the drift components cancel out.

Based on the simulation results, it was determined that the chip design is worthy of fabrication for further laboratory testing, since the simulations showed acceptable performance. It is expected that the simulation results will not be entirely accurate due to the ideal conditions of simulation, such as having perfectly matched components and precise biasing through ideal power supplies. The next chapter discusses laboratory results of the fabricated ICs.

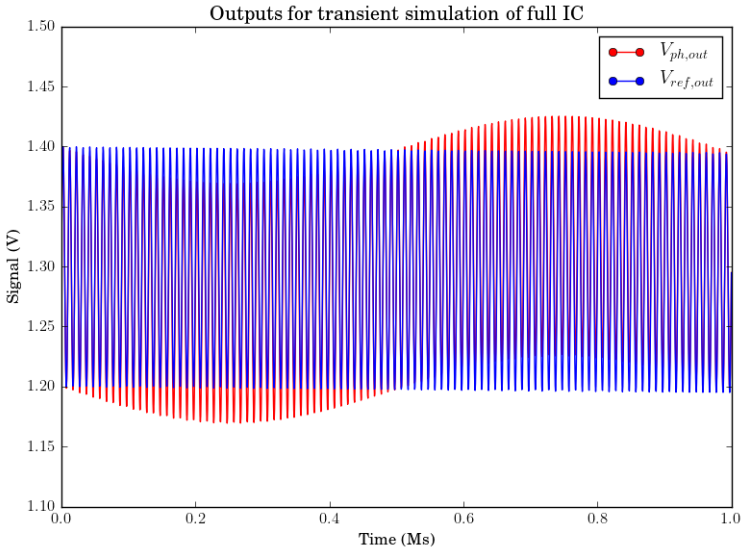


Figure 11.5 – Outputs for transient simulation of full IC.

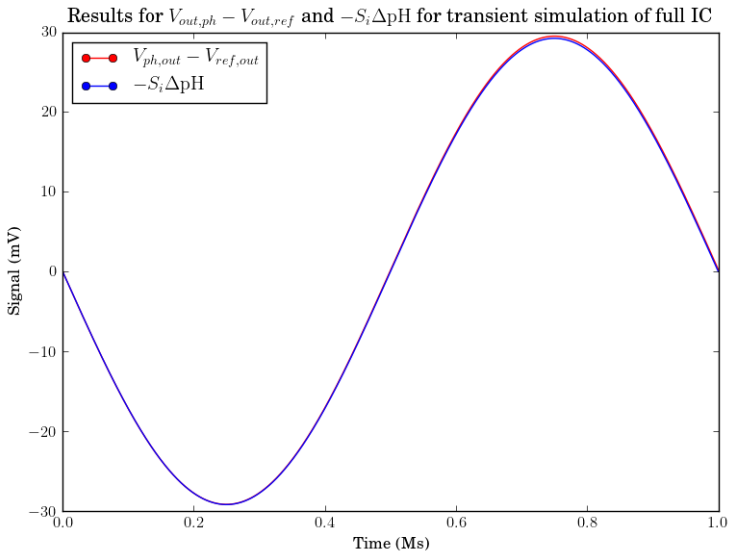


Figure 11.6 – Differential output $V_{out,ph} - V_{out,ref}$ and $-(58.8\ \text{mV/pH})\Delta\text{pH}$ in transient simulation of full IC.

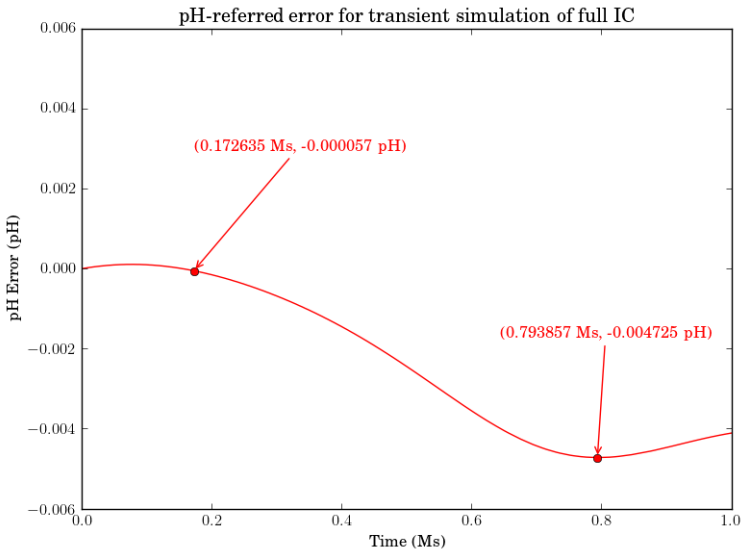


Figure 11.7 – Error in transient simulation of full IC.

Chapter 12

Laboratory Testing

12.1 Device Fabrication

The IC designed in Chapter 11 was submitted to CMC for fabrication, under the design name `ICSMG11S`. A total of 100 chips were produced, with 95 bare die and 5 chips wirebonded to a DIP-40 package for testing purposes. The DIP-40 packaged chip is shown in Figure 12.1, and the wirebonding with pin numbers (corresponding to those of section 11.1) is shown in Figure 12.2. The laboratory tests described in the following sections used the packaged chips due to the ease of handling and integration on the PCB test board. However this could introduce undesirable parasitic capacitances due to the DIP-40 pads and longer traces connecting to the PCB. Moreover, there could be additional leakage resistances along the PCB or the wirebonding close to the lid.

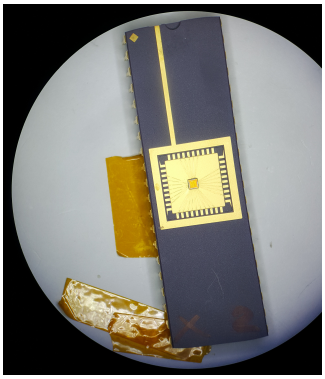


Figure 12.1 – DIP-40 package used for testing.

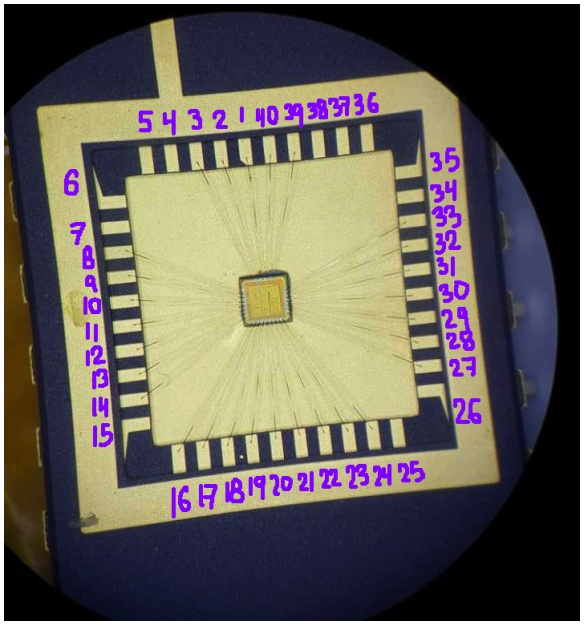


Figure 12.2 – Picture of the wirebonding with pin numbers.

12.2 Test Circuit Board and Laboratory Setup

For the laboratory testing, a PCB test board was designed using Altium Designer. The layout of the PCB is shown in Figure 12.3, and a photograph of the test PCB in the lab is shown in Figure 12.4. The PCB contains a DIP-40 socket of the zero-insertion force (ZIF) type which allows different ICs to be replaced on the same PCB without re-soldering. Every pin on the chip is exposed to a header on the PCB allowing connections with jumper wires for different circuit configurations. In addition, five 1 nF capacitors of the ceramic SMD type ($C_1, \ldots, C_5$ in Figure 12.3) were connected in series to each of the five gate inputs (two op-amp positive inputs and three transistor gates). These capacitors simulate the sensing dielectric capacitance C_{sens}. It is therefore possible to connect an input signal either directly to the readout circuit, or indirectly through the capacitors. This allows to verify the operation of the circuit without being affected by the leakage and loading effects. The PCB also contains a mechanical switch (S_1 in Figure 12.3) connected to both `vph_in+` and `vref_in+`. This allows the option of using either the on-chip MOSFET switches or an off-chip mechanical switch and compare their performance. Finally, capacitors C_8 and C_9 are 1 μF capacitors connected to `vref_out` and `vph_out` respectively for frequency compensation.

During testing, it was found that the op-amps were very sensitive and could quickly stop working, with signs of damage including unusually high

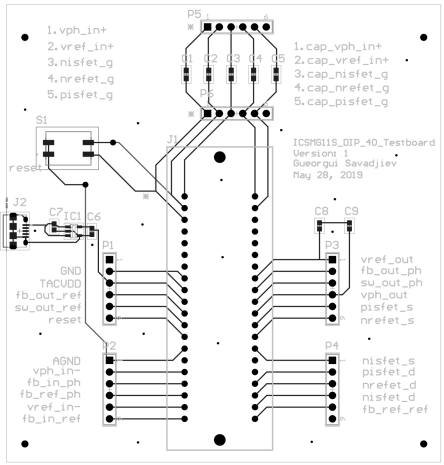


Figure 12.3 – Layout of the test PCB in Altium.

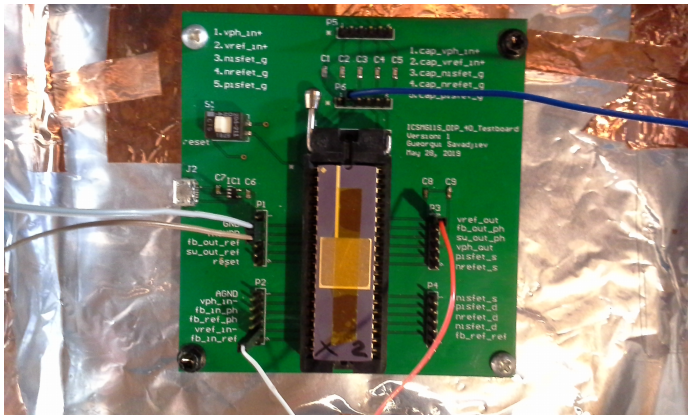


Figure 12.4 – Test PCB in the lab.

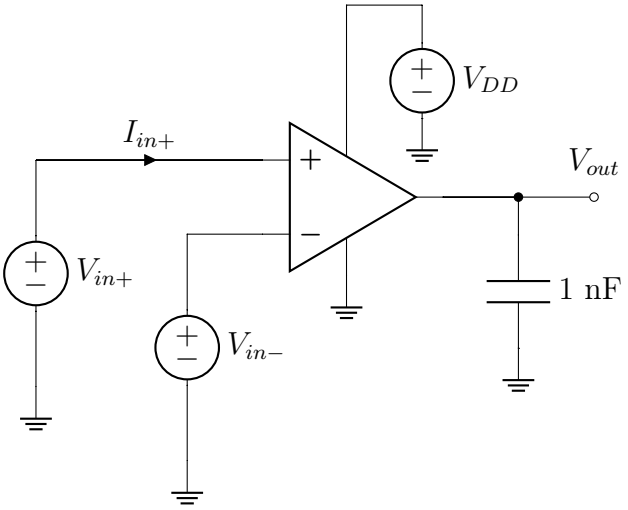


Figure 12.5 – Op-amp test circuit in open-loop configuration.

gate currents or power supply shorts. It was suspected that this could be due to ESD events, particularly since the ESD diodes were not used at the five gate inputs. Therefore precautions were taken such as using grounded wrist straps and storing the PCB inside a shielded box. Nonetheless each device would stop working after a few weeks of testing, so all tests could not be run on all devices.

12.3 Op-Amp Characterization in Open-Loop

The op-amps on the chips were characterized initially in the open-loop configuration, as shown in Figure 12.5. The V_{in+} and V_{in-} sources were swept independently from 0 V to 2.5 V, and the output V_{out} was measured with a multimeter. The V_{in+} input was connected to a Keithley 2410 Source Meter, and the V_{in-} input was connected to an Agilent E3631A Triple Output DC Power Supply, on the `P6V` output. The V_{out} output voltage was measured using a GwInstek GDM-8255A Multimeter. The chip was powered by 2.5 V through the `TACVDD` pin, connected to the Agilent power supply on the `P25V` output. The V_{in+} input was swept from 0 V to 2.5 V in steps of 10 mV. The V_{in-} input was swept from 0 V to 2.5 V in steps of 100 mV.

The plots in Figure 12.6 show the results for the two op-amps on one device, labeled `IC2_ph` and `IC2_ref`. The op-amps behaved qualitatively as expected, with a high gain region that shifts with V_{in-}. However, as shown in Figure 12.7, it was observed that there was a large input offset (V_{os}) and lower gain than expected. The figure shows a higher resolution sweep of V_{in+} with

steps of 1 mV, where there is an offset of around 320 mV and a gain of around 200 V/V. Clearly the fabricated devices suffered from greater mismatch errors than had been predicted in the Monte-Carlo simulations of section 10.6.4. Moreover, the gain is far below the gain predicted in section 10.6.2. Similarly high offsets above 150 mV and gains below 300 V/V were observed on the other devices. The simulation results are also shown in the same figure. In the simulation results, the gain is much higher than in the measurements, and the offset is near 0 V. This discrepancy between simulation and laboratory results could be due to some systematic cause during chip fabrication, which might not have been accounted for in the mismatch models. It could also be due to layout problems, because the transistors in the op-amp layout shown in Figure 11.2 were not placed in completely symmetric environments. Since the offsets were always of the same sign, it is possible that the layout introduced some systematic asymmetry in the differential pairs.

The input current I_{in+} of the op-amps was also measured using the Keithley 2410 Source Meter, and the plots are shown in Figure 12.8*a*. Based on the plots, there is a slight slope of around 10 pA/V leading to an input resistance of around 10^{11} Ω, which is far below what was expected from the simulations which are shown in Figure 12.8*b*. In the simulations, the current stays below 70 aA in the whole range, and the resistance exceeds $7 \cdot 10^{15}$ Ω. This discrepancy could be due to the inaccuracies in gate input current models mentioned in section 9.1. It is also possible that additional sources of leakage were present on the PCB, such as the mechanical switch and the soldering. Unfortunately, the source meter was slightly out of calibration and had a current offset of a few nA, in addition to noisy current spikes. The highest resolution of the source meter allowed measuring currents down to around 1 pA, so it was not possible to accurately measure lower currents.

12.4 Op-Amp in Unity-Gain Feedback

The op-amps were tested in the unity-gain feedback configuration as shown in Figure 12.9. Again, the chip was powered with 2.5 V through the `TACVDD` pin using the Agilent E3631A power supply's `P25V` output. The input voltage V_{in+} was swept from 0 V to 2.5 V in steps of 1 mV, using the Keithley 2410 Source Meter. The output voltage was measured with the digital multimeter GDM-8255A. The plots in Figure 12.10 show the sweep results for V_{out} against V_{in+}. It can be seen from the plots that the region with V_{in+} above 1 V is linear with a gain close to 1 V/V. Below 1 V, the gain is slightly reduced, and there is an initial offset of around 150 mV. The simulation results are shown in the same figure. Again the slope is near 1 V/V,

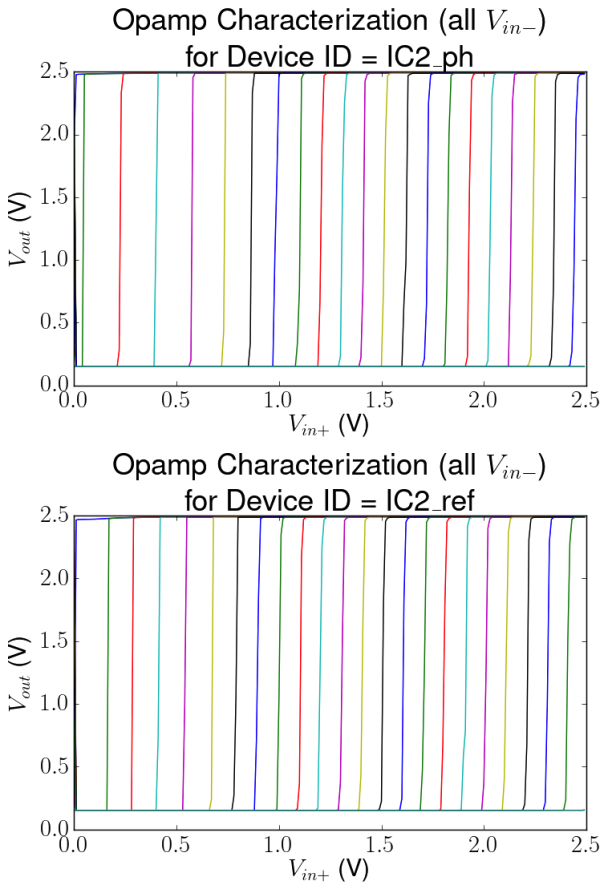


Figure 12.6 – Op-amp characterization open-loop sweep results. The different colors represent different constant values for V_{in-}.

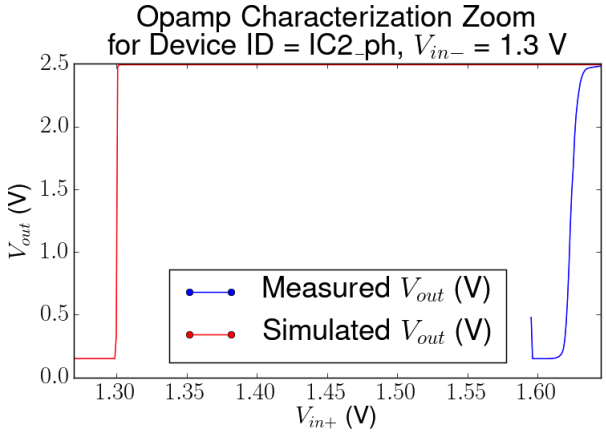
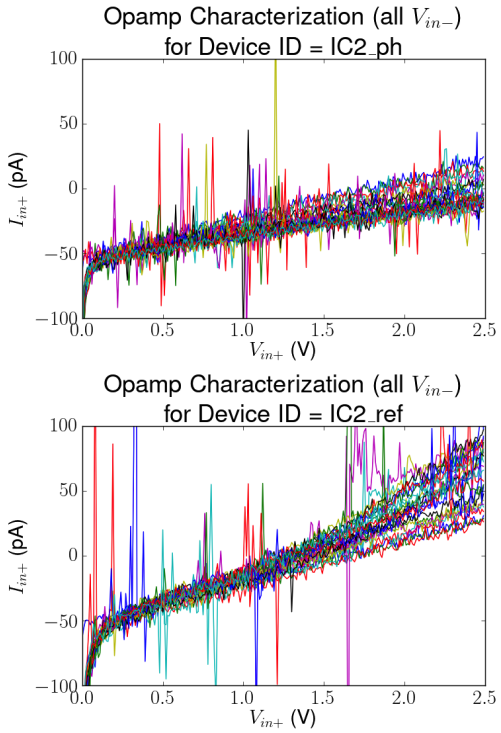
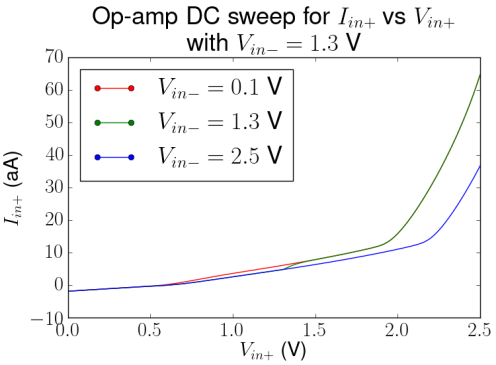


Figure 12.7 – Op-amp sweep zoom in high gain region with $V_{in-} = 1.3$ V.



(a) Lab results



(b) Simulation results

Figure 12.8 – Op-amp input current sweep. The different colors represent different constant values for V_{in-}.

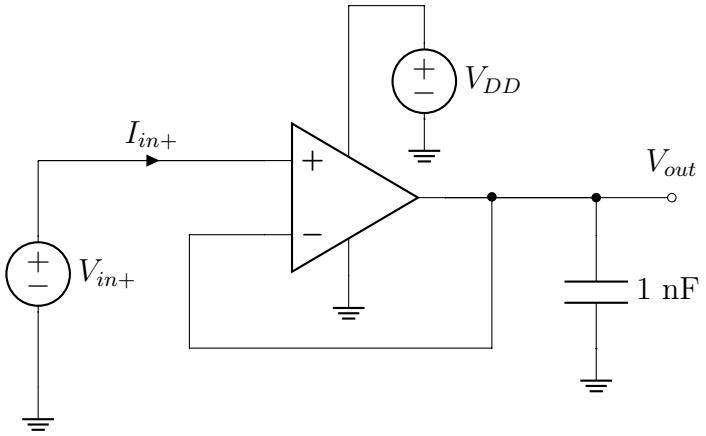


Figure 12.9 – Op-amp test circuit in unity-gain feedback.

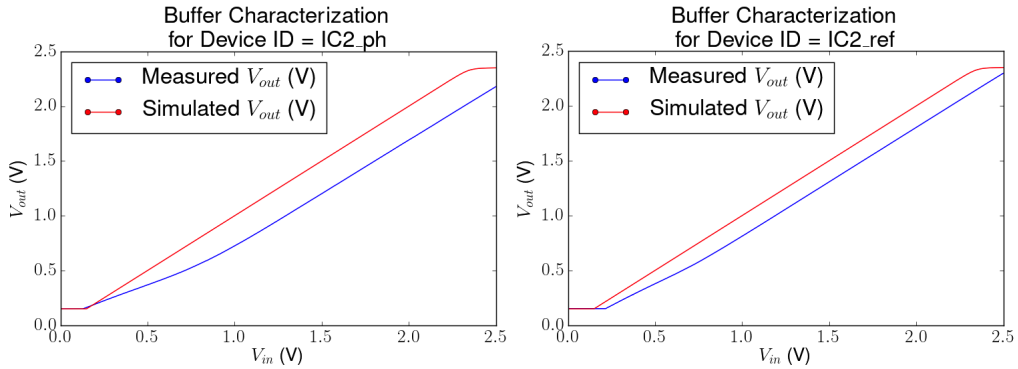


Figure 12.10 – Op-amp unity-gain input sweep results.

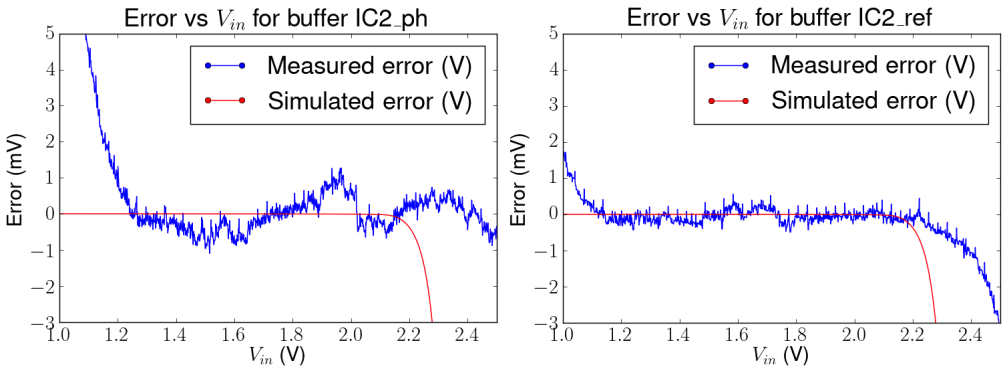


Figure 12.11 – Op-amp unity-gain input sweep error results.

however the linearity is much higher as there is no kink near $V_{in+} = 1$ V. The difference can be accounted by the lower open-loop gain of the opamp, which causes nonlinearities to be more pronounced in feedback operation, as the op-amp's behavior becomes less ideal.

The error plots are shown in Figure 12.11, where the error is calculated using the following equation:

$$V_{error} = \frac{V_{out} - V_{os}}{A} - V_{in} \tag{12.1}$$

where V_{os} is the input offset and A is the overall loop gain, estimated from the data points. For `IC2_ph`, the parameters were $V_{os} = -0.2634$ V and $A = 0.977$ V/V. For `IC2_ref`, the parameters were $V_{os} = -0.1826$ V and $A = 0.9934$ V/V. The error generally stays between ± 1 mV over a wide range around 1.3 V, which is still below the minimal error of 2.5 mV specified to achieve a pH resolution of 0.1 pH. The observed noise can be due to nonlinearity, flicker noise from the transistors or external sources including

the instruments and connections. The simulation results are shown the same figure, and again it can be seen that the error is much lower over a wide range of V_{in}, which can be explained by the more ideal behavior of the op-amp and the higher linearity.

The repeatability of the measurement was also investigated by keeping all inputs constant for the op-amp in unity-gain configuration. The input V_{in+} was kept at 1.5 V for this test, and 2000 measurements were performed on V_{out}, where each measurement takes around 1 second. The plot in Figure 12.12 shows the variation of V_{out} over time. It is clear that there is some initial transient effect which appears as a decaying exponential behavior with a time constant on the order of 100 seconds, followed by a slower linear drift of V_{out}. Unfortunately the drift is sufficiently high to cause V_{out} to change substantially over less than an hour. The cause of the behavior is not understood, as it does not occur in simulations. It must be noted that the input voltage source is directly connected to the op-amp, so loading effects coming from the series capacitor C_{sens} are not present. Therefore this variation of V_{out} indicates a time dependence of properties of the transistors on the chip, possibly caused by aging or by some reversible mechanism. Drift coming from the measurement instruments themselves was also considered, but tests where the device was replaced by simple resistors or shorts did not exhibit similar behavior, so it was concluded that the drift comes from the devices themselves.

12.5 Switch Characterization

The circuit used to test the switches on the ICs is shown in Figure 12.13. The gates of the two MOSFET switches are both connected to the `reset` pin on the IC, which is connected to a voltage source at 0 V in the off state. The sources of the two MOSFET switches are both connected to the `AGND` pin on the IC, which was grounded for this test. The drains are connected individually to either `sw_out_ph` or `sw_out_ref`. The drain voltage was swept from 0 V to 2.5 V in steps of 100 mV, and the gate voltage was swept independently from 0 V to 1.0 V in steps of 10 mV. The results of the switch current I_{DS} in the off state with $V_{GS} = 0$ V are shown in Figure 12.14*a*. On average it appears that there is a net slope of around 20 pA/V, which corresponds to a resistance of $5 \cdot 10^{10}$ Ω. The simulation results are shown in Figure 12.14*b*. The slope is around 6 pA/V, giving a resistance of $1.7 \cdot 10^{11}$ Ω. The measured resistance is about 3 times lower than the simulated resistance. However the resolution of the source meter is not sufficient to accurately measure such small currents.

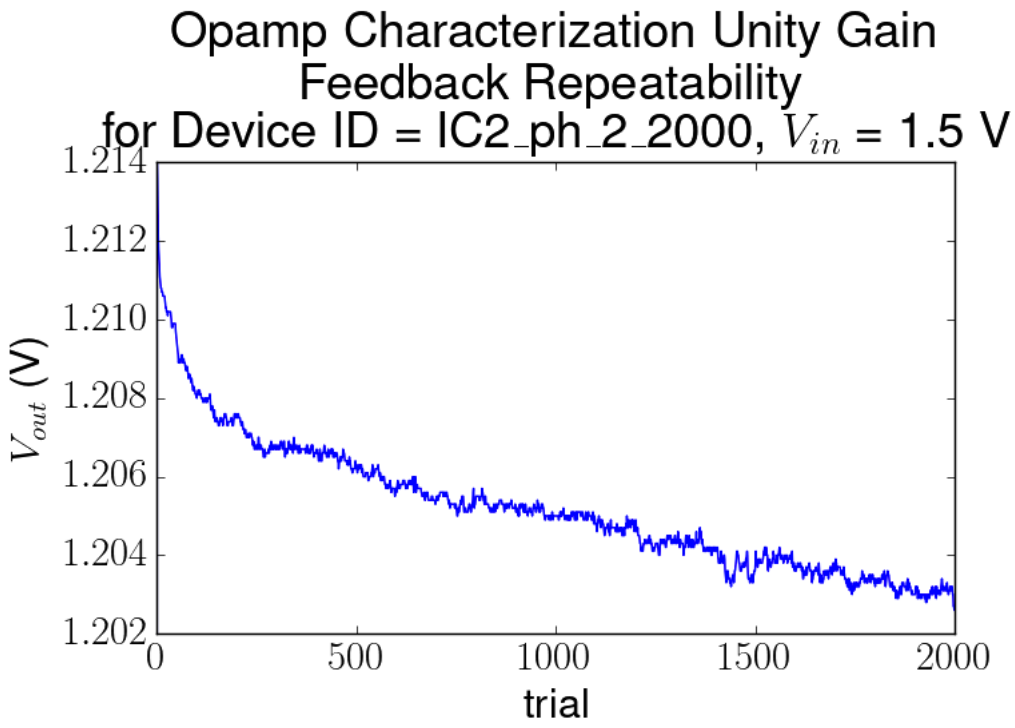


Figure 12.12 – Op-amp unity-gain repeatability test results.

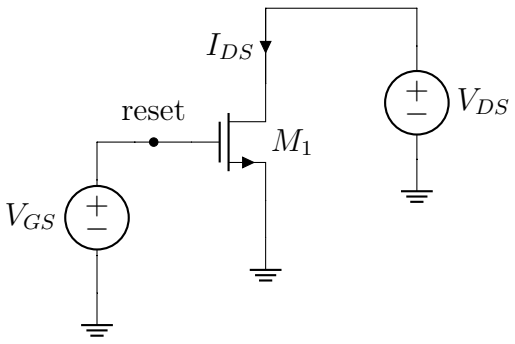
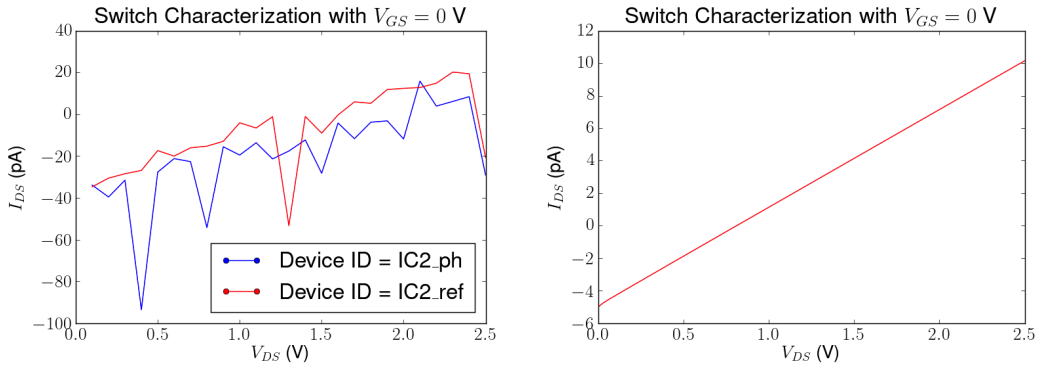


Figure 12.13 – Test circuit for the MOSFET switch characterization.



(a) Lab results (b) Simulation results

Figure 12.14 – Switch current in off-state ($V_{GS} = 0$ V) across all devices. Different colors represent different devices.

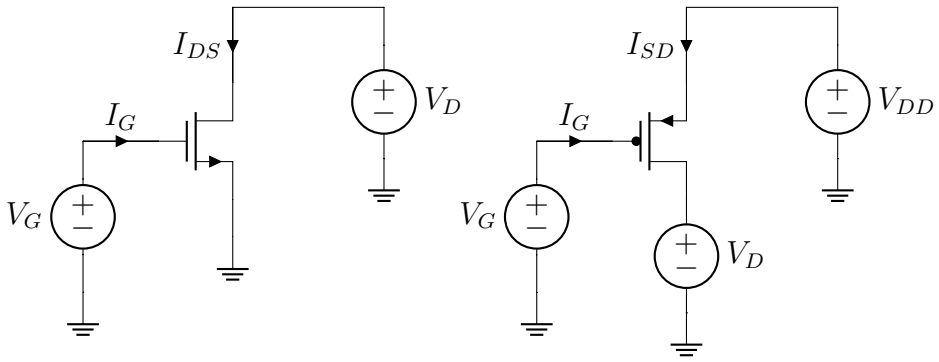
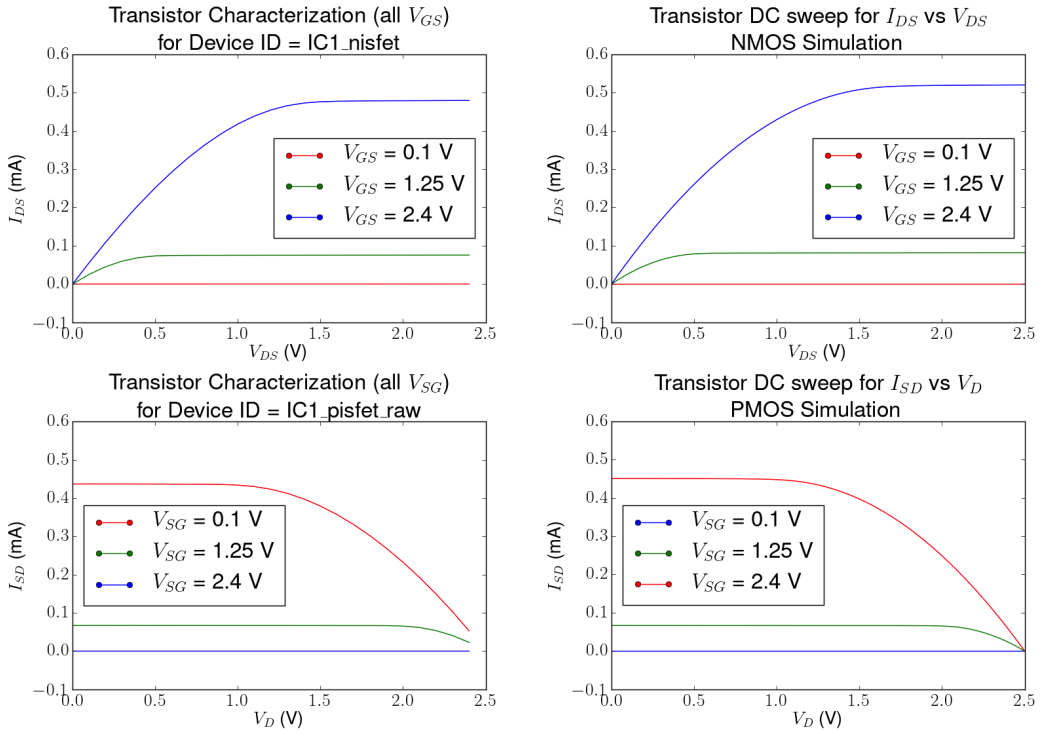


Figure 12.15 – Test circuits for the NMOS and PMOS characterization.

12.6 Transistor Characterization

The chip contains three unconnected transistors, two identical NMOS and one PMOS transistor. The PMOS size has been scaled so that its transconductance is approximately equal to the transconductance of the NMOS. The NMOS transistors were characterized by connecting power supplies on the gate and drain terminals, and measuring the I_{DS} current while sweeping V_{GS} and V_{DS} independently. The source terminal was grounded. Similarly, the PMOS source was connected to V_{DD} and the V_{SG} and V_{SD} voltages were swept independently. The sweep results for the two NMOS (`nisfet` and `nrefet`) and the PMOS (`pisfet`) devices are shown in Figure 12.16*a*. For the PMOS, $V_{SD} = V_{DD} - V_D$ and $V_{SG} = V_{DD} - V_G$. The transistors appear to be fairly well matched, the PMOS having been scaled to have the same transconductance as the NMOS as mentioned in section 11.1. The simula-



(a) Lab results

(b) Simulation results

Figure 12.16 – Transistor characterization $|I_{DS}|$ vs $|V_{DS}|$ with $|V_{GS}|$ fixed.

tion results are shown in Figure 12.16*b*, and the results are close to what was obtained in the measurements.

The gate currents I_G were also measured as functions of V_G while keeping V_{DS} fixed, as shown in Figure 12.17. It can be seen that there is a noticeable current dependence, on the order of 50 pA/V, leading to an estimated input gate resistance $R_g = 2 \cdot 10^{10}\ \Omega$. This is again far below what would be expected from the simulations, likely because the transistor gate leakage models did not take into account other possible sources of leakage on the PCB or the chip, such as through cables, through solder bridges or through the wirebonds. For comparison, the same test was performed with an empty socket to see how much of the measured current could have come from leakage on the PCB or cables, with results shown in Figure 12.18. There was indeed some leakage present with empty sockets as well, however its magnitude was not as large, so it cannot account for the observed values of the gate input resistance.

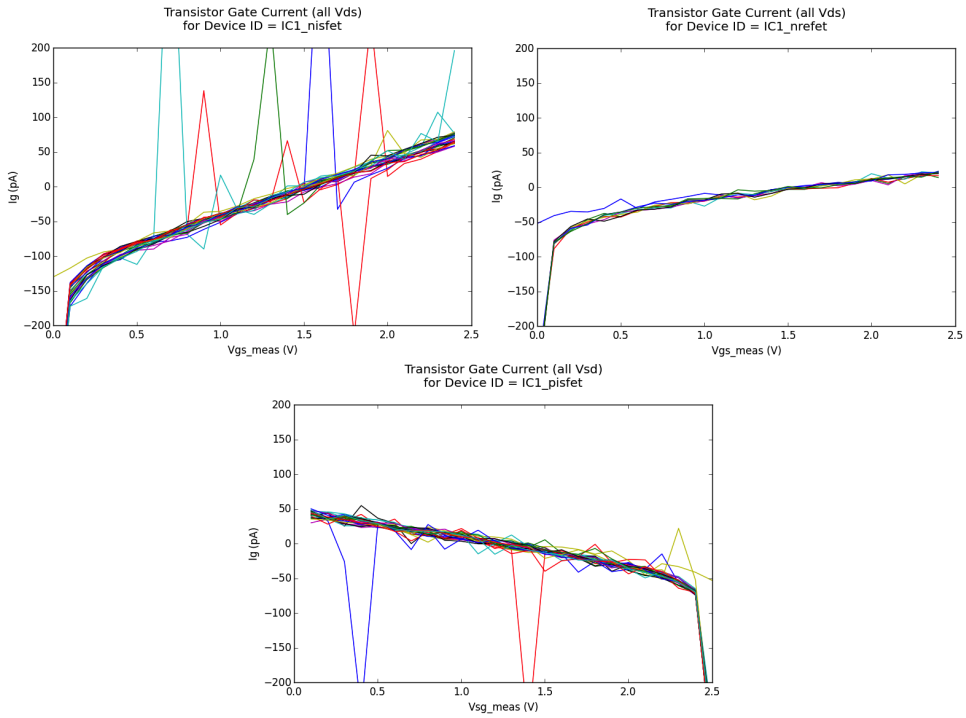


Figure 12.17 – Transistor gate current I_G vs V_G with $|V_{DS}|$ fixed (in simulation, the current remains below 60 fA). Different colors represent different constant values for V_{DS} or V_{SD}.

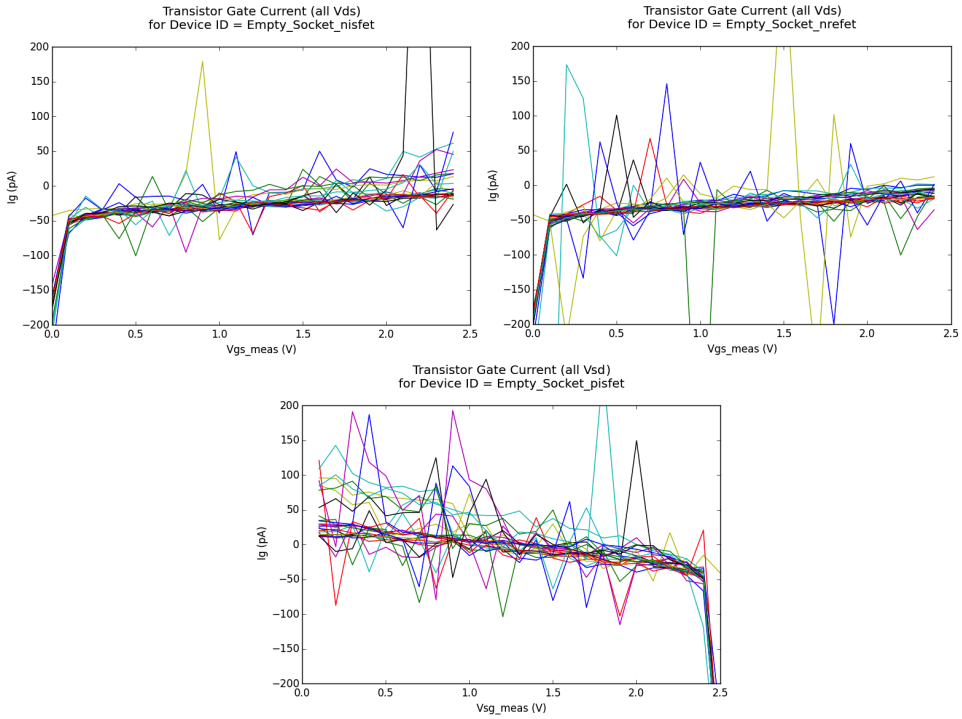


Figure 12.18 – Measured current I_G vs V_G with $|V_{DS}|$ fixed with empty socket. Different colors represent different constant values for V_{DS} or V_{SD}.

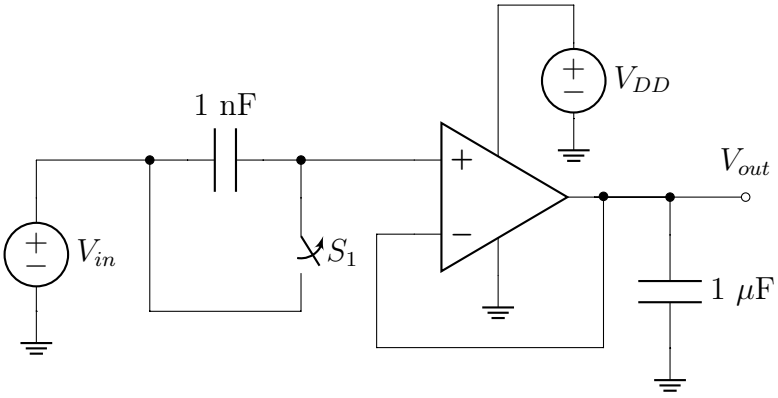


Figure 12.19 – Test schematic for buffer readout circuit.

12.7 Test Results of Buffer Readout Circuit

The configuration of the buffer readout circuit was tested in the laboratory using the PCB testboard and connecting the op-amps according to the schematic of Figure 12.19. The switch S_1 was the mechanical switch on the PCB. Due to the leakages measured for the MOSFET switches in section 12.5, it was decided that the mechanical switch would be a better choice in terms of minimizing the leakage. The input voltage V_{in} simulates the potential φ_0 at the side of the sensing dielectric in contact with the solution. Therefore controlling V_{in} is a way to verify the operation of the readout circuit under variations of pH and bulk potential.

For the tests conducted, the input voltage was controlled as a series of steps alternating between two voltage values. This allows to see the step response of the readout circuit, and estimate time constants arising from the loading effect at the input capacitor. The switch S_1 was initially closed for a few seconds in order to set the initial condition of the floating node to V_{AGND}. The input V_{in} was set to alternate between 1.5 V and 1.6 V, while staying constant for 15 minutes each time. The results for one device are shown in Figure 12.20*a*.

It was originally expected that the mechanical switches would have negligible current leakage when open, so V_{AGND} was actually provided by the same supply as V_{in} due to laboratory limitations. There is a possibility that the switch introduces a parallel resistance which would couple V_{out} and V_{in} and affect the measured time constant and DC offset. Indeed, if $V_{AGND} = V_{in}$ then the switch resistance becomes effectively in parallel with $C_{sens} = 1$ nF. Based on the results shown, it appears that the switch resistance may indeed be low enough for V_{in} to couple directly to the floating node, since V_{out} does not converge to the same value when V_{in} changes. It would normally be

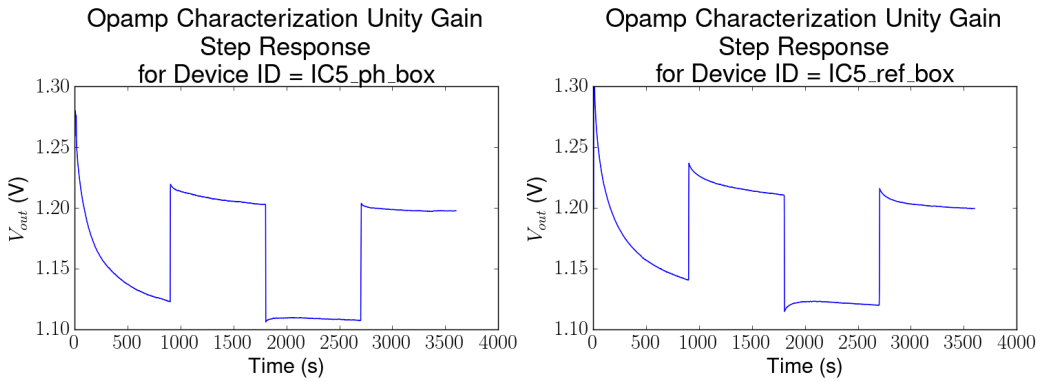
expected for V_{out} to converge to a fixed value independent of V_{in} if there was no switch resistance R_{switch} in parallel with C_{sens}, since the readout circuit would be DC-decoupled from the input V_{in}.

The test still provides information on the time constant of the circuit while V_{in} is fixed however. The time constant appears to be on the order of 100 seconds. Using the relationship $\tau = RC$, the estimate for the input resistance is around 10^{11} Ω which is consistent with the DC current measurements of section 12.3. It is still clear from the plots that there is a noticeable transient effect which causes the output voltage to drift over time with an increased error relative to V_{in}. This transient effect was discussed in the analysis section 3.10. Unfortunately the drift is large enough for V_{out} to vary by a few mV over 15 minutes, which is already too large to maintain the desired pH resolution. The simulation results for the same test are shown in Figure 12.20*b*. There is no drift or visible decay in the pulses over time, indicating that the time constant is very large. This is because the simulation predicts a much larger input resistance compared to what was measured in the lab, and therefore it shows the ideal behavior of the circuit.

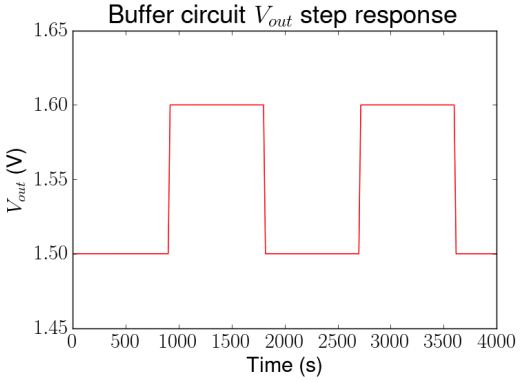
An overnight test was performed where V_{in} alternated between 1.5 V and 1.6 V, with an initial delay of 3 hours, followed by intervals of 1 hour, with an overall time length of 12 hours. The results are shown in Figure 12.21. As seen, each pulse has some noise and transient spikes, but there is also an overall slow drift that accumulates over each pulse. This drift could be caused by the same phenomenon observed in the repeatability test of section 12.4, in addition to the current leakage effect.

12.8 Buffer Readout Circuit in Differential Configuration

The differential configuration of the buffer readout circuit, discussed in Chapter 8, is shown in Figure 12.22. In this test, the input V_{in} is provided as a common-mode input to the two identical circuits, where one circuit represents the pH-sensitive part and the other circuit represents the reference part. The measurement is a differential reading of $V_{out,diff} = V_{out,ph} - V_{out,ref}$. The switches S_1 and S_2 are physically parts of a double-pole single-throw (DPST) mechanical switch on the PCB. They are initially closed for a few seconds, and then opened for the rest of the test. As mentioned in section 12.7, the switches should ideally have been connected to a separate fixed voltage source. Otherwise they can introduce a parallel resistance that arti-



(a) Lab results



(b) Simulation results

Figure 12.20 – Test results for buffer readout circuit while pulsing V_{in} between 1.5 V and 1.6 V in 15 min intervals.

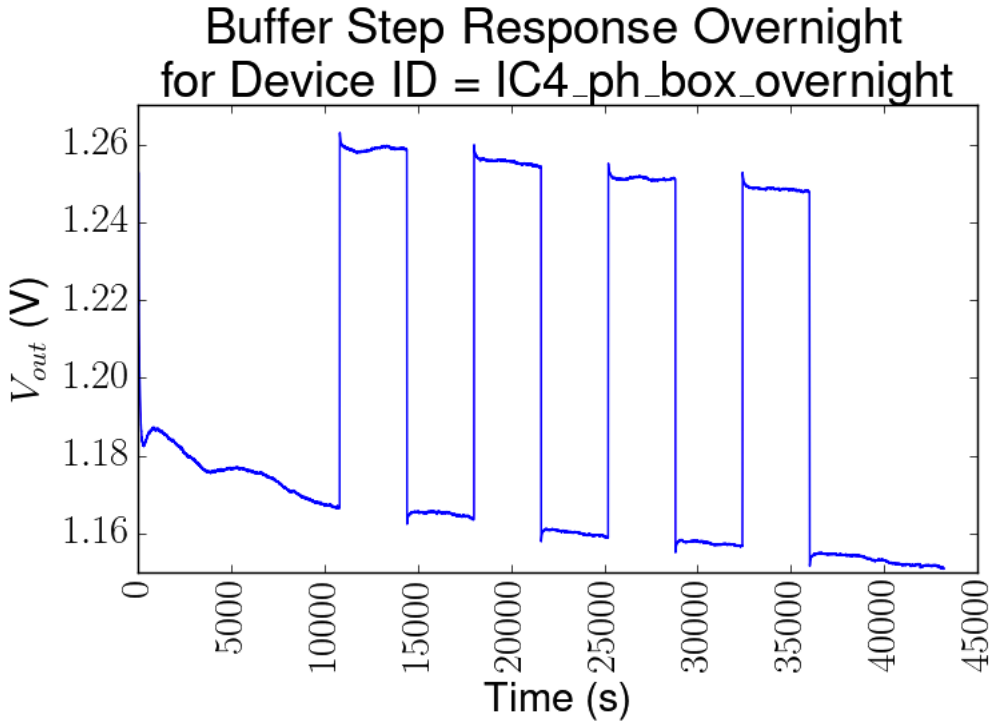


Figure 12.21 – Overnight test results for buffer readout circuit while pulsing V_{in} between 1.5 V and 1.6 V in 1h intervals.

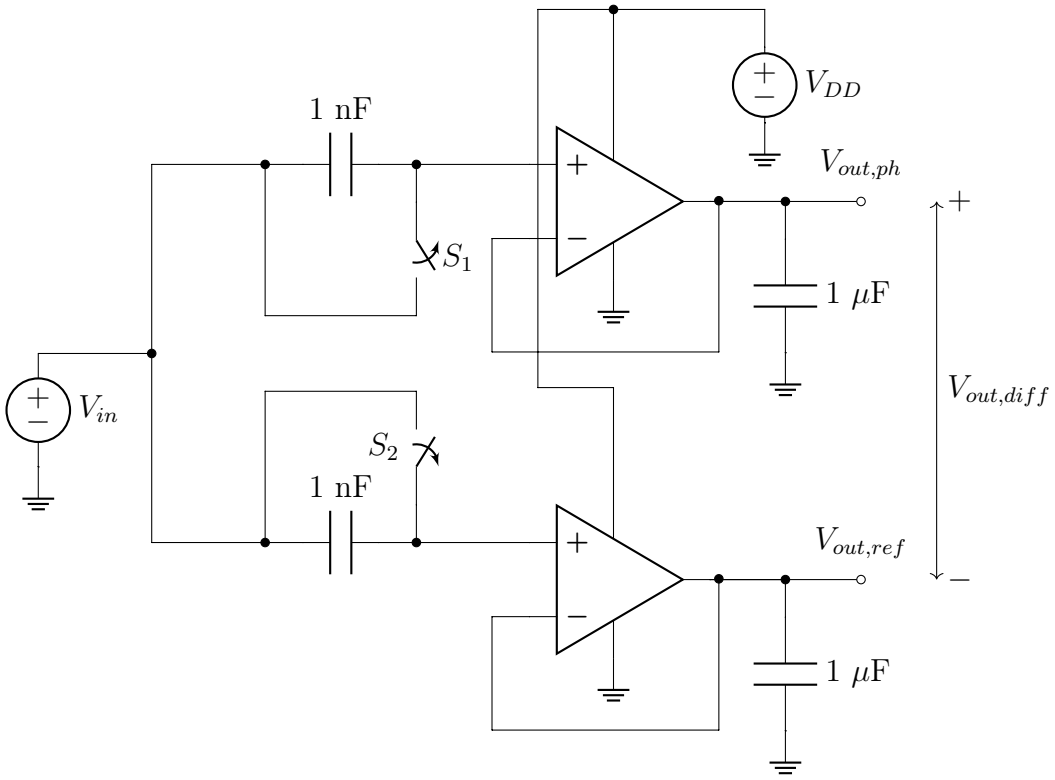
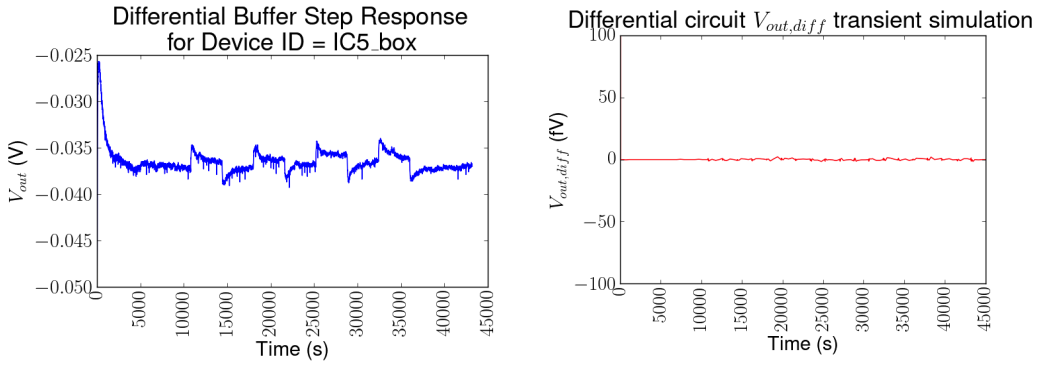


Figure 12.22 – Test schematic for buffer readout circuit in differential configuration.



(a) Lab results

(b) Simulation results

Figure 12.23 – Overnight test results for buffer readout circuit in differential configuration.

ficially improves the readings by reducing the loading effect from the input capacitors.

An overnight test for 12 h was done with the same input waveform V_{in} as described in section 12.7. The result for one device is shown in Figure 12.23*a*. The differential configuration seems to reduce greatly the drift that was observed in Figure 12.21, showing that this method can indeed help improving the readout. In addition, the response of V_{out} to the common-mode variation of V_{in} (which involved steps of 100 mV) appears to be reduced as well, with V_{out} varying by less than 5 mV in comparison. This is a good verification of the common-mode rejection behavior, and the ability to cancel out variations from the bulk potential of the electrolyte. There is an overall DC offset of around -35 mV between $V_{out,ph}$ and $V_{out,ref}$, which could be due to the slightly different DC operating points of each op-amp because of their different V_{os}. The simulation results for the same test are shown in Figure 12.23*b*. In the simulations, the error is extremely small, and this is due to the ideal behavior of the op-amp with very little input mismatch. In reality there will always be some component mismatch which is reflected in the higher sensitivity to common-mode variations.

12.9 Commercial Op-Amp Tests

As was mentioned in section 10.1, the possibility of using a commercial op-amp for the readout circuit was also considered. In this section will be presented test results using one particular commercial op-amp, the LMC6442IN from Texas Instruments. The op-amp was selected due to its very low input

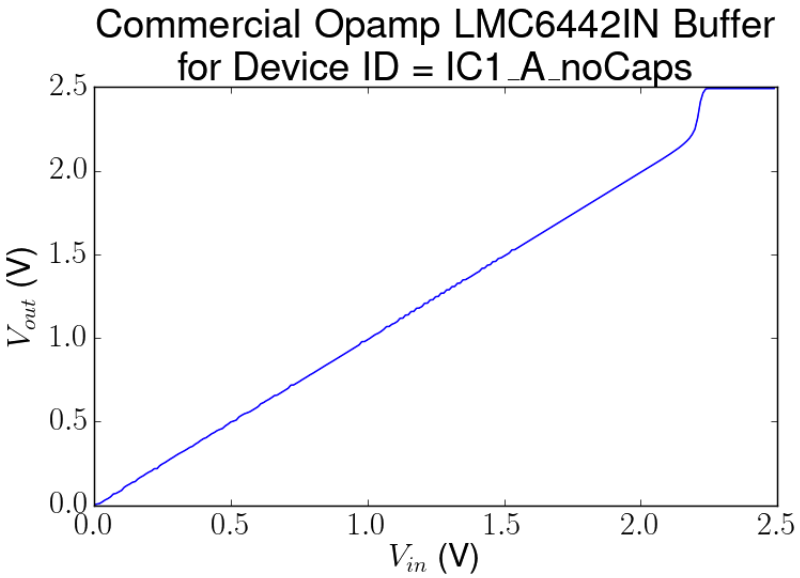


Figure 12.24 – DC sweep test of LMC6442IN op-amp in unity-gain feedback.

current leakage advertised to be below 5 fA. The LMC6442IN chip contains two identical op-amps labeled `A` and `B`. The op-amp was first characterized with a DC sweep in the unity-gain configuration just as in section 12.4. The resulting plot is shown in Figure 12.24. The error was calculated in the same way as in section 12.4 and the result is shown in Figure 12.25. The parameters used were $V_{os} = -1.75$ mV and $A = 0.99965$ V/V. Thus clearly the DC offset is much lower than that of the fabricated op-amps, and the loop gain is much closer to the ideal unity gain, as expected from a high-gain op-amp. The error stays below 500 μV for most of the input range. For the commercial op-amp, the PCB testboard was not used, instead it was placed in a breadboard. No output capacitor was placed at V_{out}. The power supply was again set at 2.5 V.

The input current of the commercial op-amp was also measured using the Keithley 2410 Source Meter. The plot is shown in Figure 12.26. It was not possible to detect a noticeable current dependence on input voltage due to the limited resolution of the source meter, however the input resistance is definitely higher than the one in the fabricated op-amps shown in Figure 12.8*a*. This is consistent with the advertised input current below 5 fA.

Based on these results, it was decided to also test the commercial op-amp in the buffer readout circuit configuration. The input waveform V_{in} was fixed at 1.5 V for 24 h initially, and was then alternated between 1.5 V and 1.6 V in 1 h intervals, with the whole test lasting 48 hours. The resulting plot

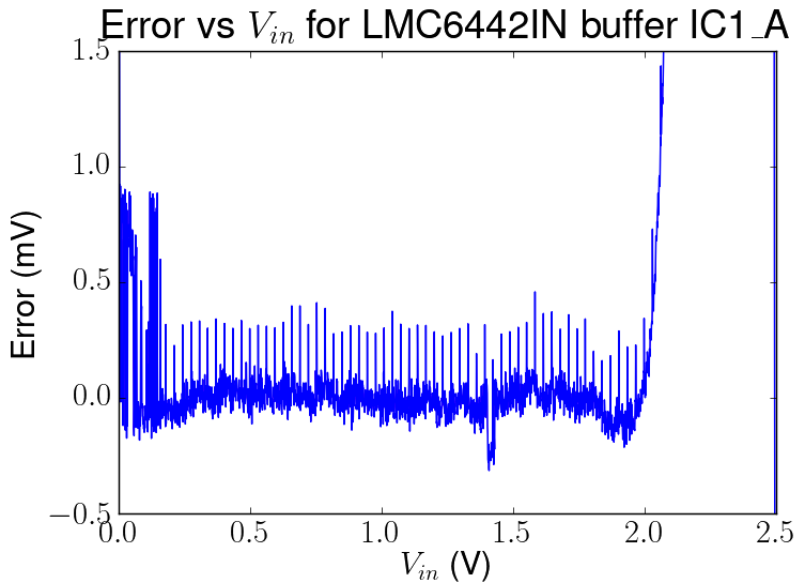


Figure 12.25 – Error in DC sweep test of LMC6442IN op-amp in unity-gain feedback.

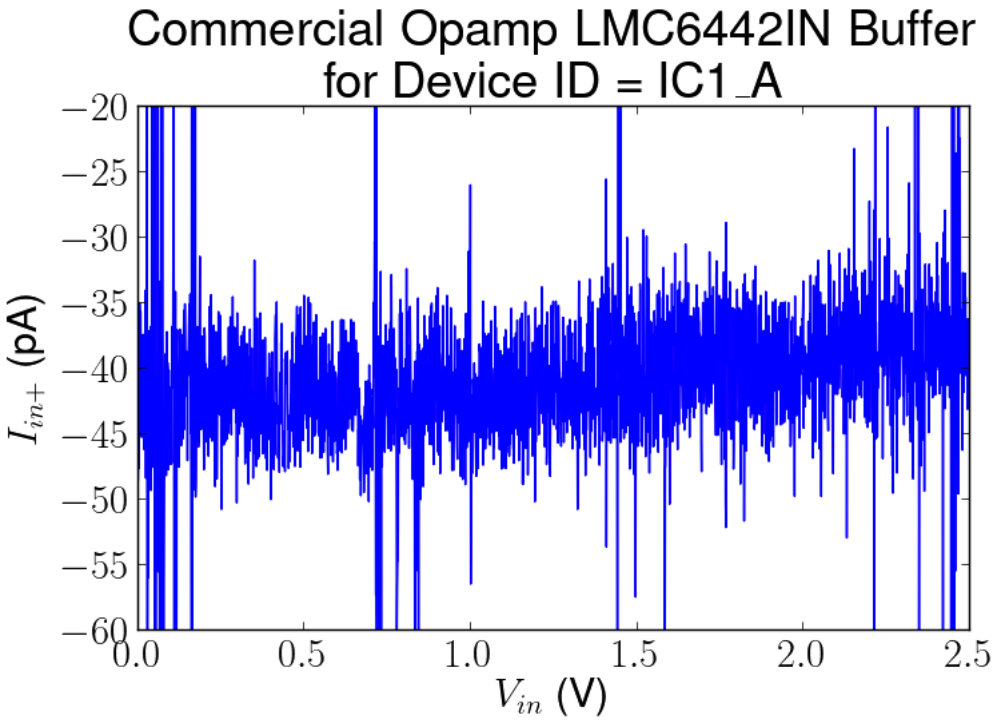


Figure 12.26 – Input current of LMC6442IN op-amp in unity-gain feedback.

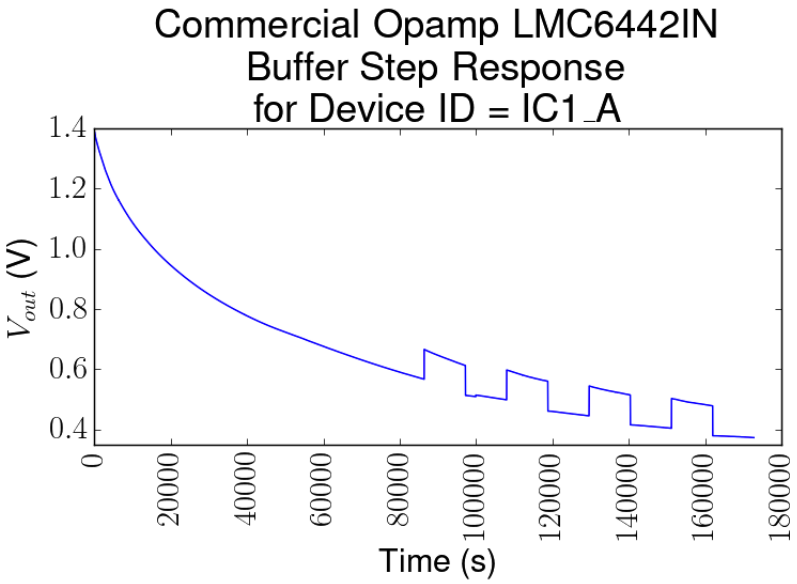


Figure 12.27 – Overnight test results for LMC6442IN in buffer readout circuit while pulsing V_{in} between 1.5 V and 1.6 V in 1h intervals.

is shown in Figure 12.27. As mentioned earlier, the op-amp was connected directly on a breadboard with a 1 nF capacitor, and no switch. Therefore it is expected that the switch leakage would not affect the results. The capacitor was manually shorted prior to the start of the test in order to provide a zero DC offset across C_{sens}.

From the plot it is seen that there is again a transient effect, but its time constant is close to 20000 seconds (5 hours), which is around 100 times higher than with the fabricated op-amp. The estimated value of input resistance is around $2 \cdot 10^{13}$ Ω, which is still not as high as desired despite the much better performance.

In order to verify the claim that the transient behavior is caused by the $R_i C_{sens}$ time constant, another test was performed where the input capacitor C_{sens} was increased from $C_{sens} = 1$ nF to $C_{sens} = 1$ μF. This is not realistic in practice due to the large sensing area required to achieve such a high capacitance, but it allows confirming that the behavior is related to this parameter as expected from the time constant equation (3.32). A 12 h test was performed similar to the previous one, with V_{in} fixed at 0.3 V for 6 h initially, followed by alternating between 0.3 V and 0.4 V in 2 h intervals. The result is shown in Figure 12.28. Indeed it was found that the transient behavior is greatly reduced, with little observable drift after the first 6 hours. This result suggests that increasing C_{sens} as much as possible will be an

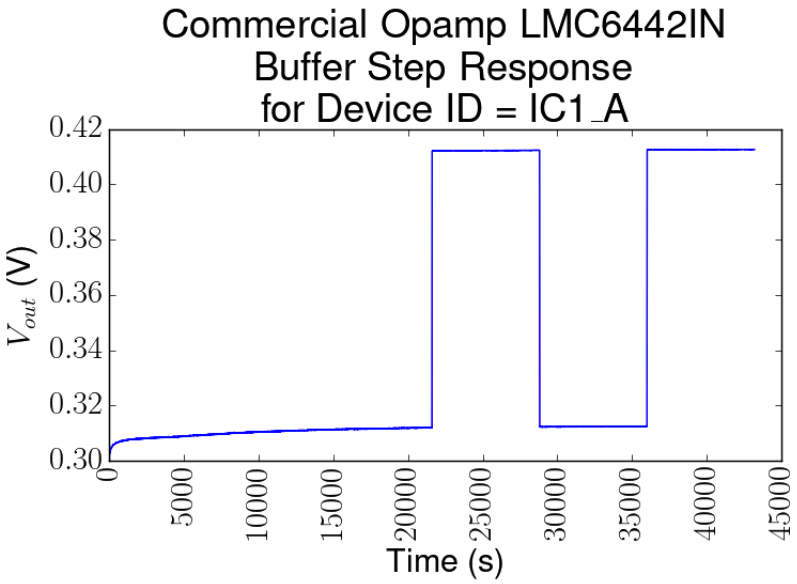


Figure 12.28 – Overnight test results for LMC6442IN in buffer readout circuit while pulsing V_{in} between 0.3 V and 0.4 V in 2h intervals with $C_{sens} = 1$ μF.

important design goal in future implementations, as well as a proper choice of DC biasing for the floating node. Indeed, the DC bias may also affect the observed input leakage current and therefore affect the transient behavior.

Chapter 13

Conclusion

13.1 Summary of Thesis

In this thesis, the possibility of designing a readout circuit for an ISFET-based pH-sensor using TSMC 65nm was investigated. Based on the theory from the literature, a model of the ISFET was formulated to use in simulations, using Ta_2O_5 as the sensing material. The choice of gate material was based on the superior sensitivity and linearity of Ta_2O_5. Due to the small scale of the devices in this process, the issue of current leakage and loading effects at the floating gate of the ISFET had to be considered. Some circuit solutions were proposed and analyzed, and each of their advantages and drawbacks were compared.

The simplest circuit used an op-amp in buffer configuration in series with the sensing dielectric capacitance. It was determined that the input resistance of the op-amp had to be larger than 10^{14} Ω to avoid the loading effect. The standard `nch` transistors did not have sufficiently high gate input resistance based on simulations, but the `nch_25` transistors with thicker gate oxide seemed to be acceptable. With this knowledge, an IC was designed containing two identical op-amps and switches that could be used to implement the buffer readout circuit in practice. However, laboratory experiments showed that such high values of R_i were hard to achieve in practice, with both the fabricated ICs and the low-leakage commercial op-amps having lower input resistance than acceptable. Therefore it can be concluded that implementing the buffer readout circuit is not feasible in practice with the given constraints.

The alternative solutions of the switch and buffer readout circuit and the reference electrode feedback readout circuit were also analyzed and simulated with ideal models. The solution proposed in the switch/buffer readout circuit was to disconnect the readout circuit from the sensing capacitor with a

low-leakage switch in between readings, thus avoiding the loading effect and leakage drift to accumulate too much over time. The simulations showed that such an approach is theoretically possible. The reference electrode feedback readout circuit instead used the reference electrode as a feedback node in the circuit, allowing measurement of the electrolyte potential with the ability to decrease the low-frequency cutoff. This method was also verified in simulations, however it was found to be very sensitive to biasing voltages.

The laboratory experiments also investigated the implementation of the differential readout circuit. The differential configuration of the buffer readout circuit was found to sufficiently reduce sensitivity to common-mode variations in bulk potential and drift.

13.2 Limitations

The laboratory experiments investigated the leakage currents of the fabricated op-amps and the switches, as well as implementations of the readout circuit. Some limitations in the laboratory setup were encountered. First, the measurement of the small currents was difficult due to the source meter's resolution being limited. Second, there were various additional sources of leakage that could have been introduced with the PCB and laboratory setup, such as leakage through the mechanical switch and soldering bridges, as well as leakage through BNC cables. Third, the measurements of time constants for the op-amps connected the input voltage directly to the switch for DC biasing purposes. In reality the DC bias voltage at the switch should be fixed and independent of the input voltage, and the presence of a switch leakage resistance can affect the measurements due to the switch being in parallel to the sensing capacitors.

13.3 Future Work

It may be possible to implement different op-amp topologies implementing feedback on the MOSFET drain or source terminals in a way that exploits knowledge of the relationship $I_G(V_G, V_D, V_S)$ to increase the input resistance R_i. This would require controlling one of the other terminals besides V_G in such a way that when V_G changes, the other terminal changes in such a way that I_G remains constant near zero. However this would require precise knowledge of the MOSFET physical model and more extensive testing. Also it could be possible to characterize the device response and reconstruct the distorted signal after the measurement in order to compensate for drift and

loading effects. These solutions were not investigated in this work but could be in future efforts.

The possibility of increasing C_{sens} and having some parallel resistance R_{sens} in order to allow DC coupling between the input φ_i and the solution could also be investigated. A different choice of geometry and materials could perhaps allow these solutions to be feasible. The DC biasing problem discussed in section 4.4 was resolved here using switches, however the use of a control gate for capacitive biasing could be a promising approach that avoids switch leakage problems. Finally, the sensing elements should be fabricated to obtain empirical data on their properties, and verify the correctness of the ISFET model used in this work.

Bibliography

[1] P. Bergveld. Thirty years of isfetology: What happened in the past 30 years and what may happen in the next 30 years. *Sensors and Actuators B: Chemical*, 88(1):1–20, 2003.

[2] H. H. Liao, H. H. Tsai, Y. Z. Juang, R. L. Wang, C. C. Fu, and C. Yu. Isfet with built-in gold electrode and readout circuit with frequency-adjustable pulse output. In *2013 Seventh International Conference on Sensing Technology (ICST)*, pages 457–460, 2013.

[3] H. S. Wong and M. H. White. A cmos-integrated 'isfet-operational amplifier' chemical sensor employing differential sensing. *IEEE Transactions on Electron Devices*, 36(3):479–487, 1989.

[4] Yuan-Lung Chin, Jung-Chuan Chou, Tai-Ping Sun, Wen-Yaw Chung, and Shen-Kan Hsiung. A novel ph sensitive isfet with on chip temperature sensing using cmos standard process. *Sensors and Actuators B: Chemical*, 76(1):582–593, 2001.

[5] Shahriar Jamasb, Scott Collins, and Rosemary L. Smith. A physical model for drift in ph isfets. *Sensors and Actuators B: Chemical*, 49(1):146–155, 1998.

[6] Arkadiy Morgenshtein, Liby Sudakov-Boreysha, Uri Dinnar, Claudio G. Jakobson, and Yael Nemirovsky. Cmos readout circuitry for isfet microsystems. *Sensors and Actuators B: Chemical*, 97(1):122–131, 2004.

[7] Y. Hu and P. Georgiou. A robust isfet ph-measuring front-end for chemical reaction monitoring. *IEEE Transactions on Biomedical Circuits and Systems*, 8(2):177–185, 2014.

[8] Mark James Milgrew. *An integrated CMOS sensor array technology for direct extracellular ion imaging.* Ph.d. thesis, University of Glasgow (United Kingdom), 2007.

[9] M. Esashi and T. Matsuo. Integrated micro multi ion sensor using field effect of semiconductor. *IEEE Transactions on Biomedical Engineering*, BME-25(2):184–192, 1978.

[10] A. Errachid, J. Bausells, and N. Jaffrezic-Renault. A simple refet for ph detection in differential mode. *Sensors and Actuators B: Chemical*, 60(1):43–48, 1999.

[11] Donald A. Neamen. *Semiconductor Physics and Devices - Basic Principles, 4th Edition.* The McGraw-Hill companies. New York, N.Y : McGraw-Hill, 2012., 2012.

[12] Y. Tsividis and C. McAndrew. *Operation and Modeling of the MOS Transistor.* Oxford Series in Electrical and Computer Engineering. Oxford University Press, 2011.

[13] BSIM Group. Bsim4 model, 2017. [Online; accessed 02-October-2019].

[14] P. Bergveld. Development of an ion-sensitive solid-state device for neurophysiological measurements. *IEEE Transactions on Biomedical Engineering*, BME-17(1):70–71, 1970.

[15] P. Bergveld. Isfet, theory and practice. *Proc. IEEE Sensor Conference, Toronto*, pages 1–26, 2003.

[16] David E. Yates, Samuel Levine, and Thomas W. Healy. Site-binding model of the electrical double layer at the oxide/water interface. *Journal of the Chemical Society, Faraday Transactions 1: Physical Chemistry in Condensed Phases*, 70(0):1807–1818, 1974.

[17] L. Bousse, N. F. De Rooij, and P. Bergveld. Operation of chemically sensitive field-effect sensors as a function of the insulator-electrolyte interface. *IEEE Transactions on Electron Devices*, 30(10):1263–1270, 1983.

[18] P. Bergveld, R. E. G. van Hal, and J. C. T. Eijkel. The remarkable similarity between the acid-base properties of isfets and proteins and the consequences for the design of isfet biosensors. *Biosensors and Bioelectronics*, 10(5):405–414, 1995.

[19] R. E. G. van Hal, J. C. T. Eijkel, and P. Bergveld. A novel description of isfet sensitivity with the buffer capacity and double-layer capacitance as key parameters. *Sensors and Actuators B: Chemical*, 24(1):201–205, 1995.

[20] R. E. G. van Hal, J. C. T. Eijkel, and P. Bergveld. A general model to describe the electrostatic potential at electrolyte oxide interfaces. *Advances in Colloid and Interface Science*, 69(1):31–62, 1996.

[21] Massimo Grattarola, Giuseppe Massobrio, and Sergio Martinoia. Modeling h+-sensitive fets with spice. *Electron Devices, IEEE Transactions on*, 39(4):813–819, 1992.

[22] A.J. Bard and L.R. Faulkner. *Electrochemical Methods: Fundamentals and Applications, 2nd Edition.* Wiley Textbooks, 2000.

[23] S. J. Schepel, N. F. de Rooij, G. Koning, B. Oeseburg, and W. G. Zijlstra. In vivo experiments with a ph-isfet electrode. *Medical and Biological Engineering and Computing*, 22(1):6–11, 1984.

[24] S. Alegret, J. Bartrolí, C. Jiménez, M. del Valle, C. Domínguez, E. Cabruja, and A. Merlos. ph-isfet with nmos technology. *Electroanalysis*, 3(4-5):355–360, 1991.

[25] Dae-Hyuk Kwon, Byung-Woog Cho, Chang-Soo Kim, and Byung-Ki Sohn. Effects of heat treatment on ta2o5 sensing membrane for low drift and high sensitivity ph-isfet. *Sensors and Actuators B: Chemical*, 34(1):441–445, 1996.

[26] Yuan-Lung Chin, Jung-Chuan Chou, Tai-Ping Sun, Hung-Kwei Liao, Wen-Yaw Chung, and Shen-Kan Hsiung. A novel sno2/al discrete gate isfet ph sensor with cmos standard process. *Sensors and Actuators B: Chemical*, 75(1):36–42, 2001.

[27] Jung-Chuan Chou and Chen-Yu Weng. Sensitivity and hysteresis effect in al2o3 gate ph-isfet. *Materials Chemistry and Physics*, 71(2):120–124, 2001.

[28] Jung-Chuan Chou, Chen-Yu Weng, and Hsjian-Ming Tsai. Study on the temperature effects of al2o3 gate ph-isfet. *Sensors and Actuators B: Chemical*, 81(2):152–157, 2002.

[29] Kow-Ming Chang, Chih-Tien Chang, Kuo-Yi Chao, and Chia-Hung Lin. A novel ph-dependent drift improvement method for zirconium dioxide gated ph-ion sensitive field effect transistors. *Sensors (Basel, Switzerland)*, 10(5):4643–4654, 2010.

[30] S. Jamasb. An analytical technique for counteracting drift in ion-selective field effect transistors (isfets). *IEEE Sensors Journal*, 4(6):795–801, 2004.

[31] A. K. Vijayan, S. Sreenivasan, D. R. Nair, and M. R. Reddy. Drift compensation using bulk feedback in a neural recording system based on open-gate fet. In *2015 International Conference on Smart Sensors and Application (ICSSA)*, pages 98–101, 2015.

[32] S. Shah and J. B. Christen. Pulse width modulation circuit for isfet drift reset. In *2013 IEEE SENSORS*, pages 1–4, 2013.

[33] A. Morgenshtein. *Design and Methodology of Isfet (ion Sensitive Field Effect Transistor) Microsystems for Bio-telemetry.* Technion - Israel Institute of Technology, Department of Biomedical Engineering, 2003.

[34] Sergio Martinoia and Giuseppe Massobrio. A behavioral macromodel of the isfet in spice. *Sensors and Actuators B: Chemical*, 62(3):182 – 189, 2000.

[35] R. Narang, M. Saxena, and M. Gupta. Analytical model of ph sensing characteristics of junctionless silicon on insulator isfet. *IEEE Transactions on Electron Devices*, 64(4):1742–1750, April 2017.

[36] K. B. Parizi, A. J. Yeh, A. S. Y. Poon, and H. S. P. Wong. Exceeding nernst limit (59mv/ph): Cmos-based ph sensor for autonomous applications. In *2012 International Electron Devices Meeting*, pages 24.7.1–24.7.4, 2012.

[37] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, first edition, 2001.

Appendix A

ISFET Site-Binding Model

A.0.1 Site-binding model

In order to understand the operation of the ISFET, it is important to study the interface between the solution and the dielectric gate. A model of the interface between the solution and the pH-sensitive dielectric surface was proposed by Yates *et al.* in 1974, called the *site-binding model* [16]. Various improvements of the model have been proposed later by Bousse *et al.* [17], Bergveld *et al.* [18] and van Hal *et al.* [19, 20]. The main idea is illustrated in Fig. A.1. The dielectric consists of a large lattice of atoms or molecules chemically bound together, but the atoms near the surface of the material will have some unpaired electrons in their valence shells, leading to the presence of dangling bonds at the surface. These dangling bonds will generally interact with hydroxyl (OH^-) ions present in the solution and produce neutral sites. However, some hydroxyl ions might act as proton donors and lose their H^+ ions, leaving a negatively charged site. Similarly, some OH^- ions will act as proton acceptors and bind with additional H^+ ions, leading to a positively charged site. If the symbol A is used to represent some specific element of the dielectric lattice, the resulting structures at the surface can be of the form AOH (neutral), AO^- (negative) or $AOH_2{}^+$ (positive). This behavior is called amphoteric, because the bonds can both act as acids or bases. As a result, the surface of the dielectric will have a net surface charge density depending on the relative density of positively and negatively charged sites on the surface. The surface charge density will arise as a chemical equilibrium of various chemical reactions at the surface. The reactions are written as:

$$AOH \longleftrightarrow AO^- + H_s^+ \text{ (with equilibrium constant } K_a)$$

$$AOH_2{}^+ \longleftrightarrow AOH + H_s^+ \text{ (with equilibrium constant } K_b)$$

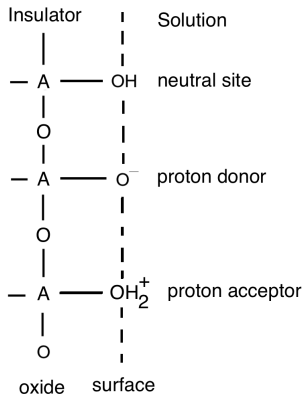


Figure A.1 – Site-binding model.

Here the subscript s in H_s^+ means that the ions are near the surface. The chemical equilibrium relations can be written in terms of the activities of the ions near the surface and the equilibrium constants:

$$\frac{a_{\mathrm{AO}^-} a_{\mathrm{H}_s^+}}{a_{\mathrm{AOH}}} = K_a \tag{A.1}$$

$$\frac{a_{\mathrm{AOH}} a_{\mathrm{H}_s^+}}{a_{\mathrm{AOH_2}^+}} = K_b \tag{A.2}$$

The activity of the surface elements can be reliably replaced with their fractional surface density. We then obtain the following two equations representing the total number of sites, and the total surface charge density σ_0 on the surface:

$$a_{\mathrm{AO}^-} + a_{\mathrm{AOH}} + a_{\mathrm{AOH_2}^+} = 1 \tag{A.3}$$

$$\sigma_0 = qN_s(a_{\mathrm{AOH_2}^+} - a_{\mathrm{AO}^-}) \tag{A.4}$$

Here q is the elementary charge and N_s is the surface density of binding sites. We can eliminate the activities of every component except $a_{H_s^+}$ from the system of four equations given by (A.1), (A.2), (A.3) and (A.4), allowing us to write σ_0 as a function of $a_{H_s^+}$ [15, 19]:

$$\sigma_0 = qN_s \left(\frac{a_{\mathrm{H}_s^+}^2 - K_a K_b}{K_a K_b + K_b a_{\mathrm{H}_s^+} + a_{\mathrm{H}_s^+}^2} \right) \tag{A.5}$$

It is also possible to consider additional reactions at the surface, leading to more complex models for the relationship between surface charge density and pH. For example, Yates *et al.* considered, in addition to the H^+ absorption/dissociation reactions, other reactions including Na^+ and Cl^-

absorption/dissociation [16]. Similarly, there may be more than one type of binding site for H^+ ions, such as in Si_3N_4 where one can have both $SiOH_2{}^+ \longleftrightarrow SiOH + H^+$ and $SiNH_3{}^+ \longleftrightarrow SiNH_2 + H^+$ reactions with different equilibrium constants [21].

A.0.2 Boltzmann equation

It is important to remember that $a_{H_s^+}$ is the activity of H^+ ions at the surface of the dielectric, but pH uses the activity in the bulk solution. These two activities are generally not identical, due to the presence of electric fields near the surface that introduce variations in the chemical potential of ions near the surface. This will be explained further in the section on the double-layer theory. In the presence of an electrical potential φ at point P, the activity of an ionic species X at point P in a system in thermodynamic equilibrium satisfies the Boltzmann equation [15]:

$$a_X\big|_P = a_X\big|_{\text{bulk}} e^{-\frac{qz(\varphi-\varphi_b)}{k_B T}} \tag{A.6}$$

Here q is the elementary charge, z is the valence of the species X, φ_b is the electrical potential in the bulk solution, k_B is Boltzmann's constant and T is the temperature. Applying this equation to the H^+ ions and combining with equation (1.1), we obtain the following relationship between $a_{H_s^+}$, pH and electrical potential:

$$a_{H_s^+} = e^{-2.303\cdot \text{pH} - \frac{q}{k_B T}(\varphi_0 - \varphi_b)} \tag{A.7}$$

where we used $z = 1$ for H^+ ions, the surface potential is φ_0 and 2.303 is an approximation to $\ln(10)$. Note that the potential difference $\varphi_0 - \varphi_b$ corresponds to the potential across the electrolyte, which was denoted by Ψ in equation (2.10).

Equations (A.5) and (A.7) together provide a relationship between the total surface charge density σ_0 at the surface of the dielectric, the pH of the solution and the electrical potential difference $\Psi = \varphi_0 - \varphi_b$ between surface and bulk.

A.0.3 Electrical double-layer

Another relation between the electrical potential difference and the surface charge density is needed in order to eliminate σ_0 and obtain a direct relationship between Ψ and pH. This relation is found by studying the electrical double-layer in the solution near the surface of the dielectric. The

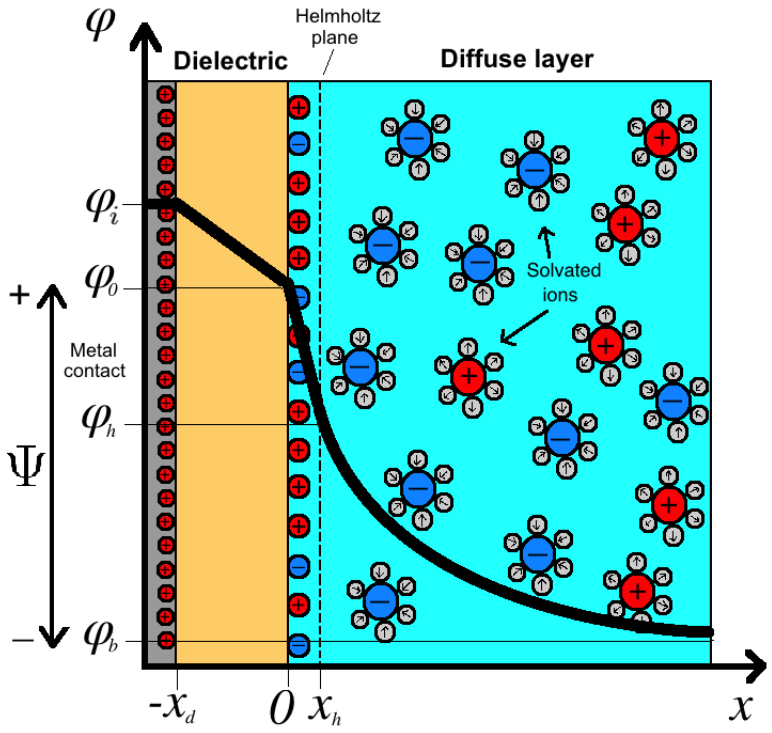


Figure A.2 – Electrical double-layer and potential distribution.

Gouy-Chapman-Stern theory [22, 20] can be used to provide a model of this electrical double-layer in terms of capacitances between two different regions in the electrolyte, the diffuse layer and the Stern layer. In the diffuse region, the ions can be assumed to follow a continuous distribution, and the charge distribution can be obtained by solving the Poisson-Boltzmann equation. The ions will also commonly be surrounded by a shell of water molecules polarized by the ionic charge. Due to their size, these solvated ions cannot come closer than a finite distance to the surface of the dielectric, and this distance defines the Helmholtz plane. The Stern layer is the region between the Helmholtz plane and the dielectric surface. Therefore there are mostly only polarized solvent molecules in the Stern layer. By solving the Poisson-Boltzmann equation, it can be shown that the diffuse layer will contain an effective surface charge density σ_d given by:

$$\sigma_d = -\sqrt{8\varepsilon_0\varepsilon_b N_A k_B T c_0}\,\sinh\left[\frac{q(\varphi_h - \varphi_b)}{2k_B T}\right] \tag{A.8}$$

where φ_h is the potential at the Helmholtz plane, ε_0 is the permittivity of free space, ε_b is the relative permittivity of the bulk, N_A is Avogadro's constant and c_0 is the molar concentration (in mol/m^3) of positively or negatively

charged ions in the bulk. This result is derived under the assumption that the bulk solution is neutral, that ions in the solution are all of valence ± 1, and that the geometry is planar. A detailed derivation is provided in Appendix *B*. Taking the derivative of (A.8) with respect to potential difference gives the nonlinear capacitance per area (in $\mathrm{F/m^2}$) of the diffuse layer:

$$C'_d = -\frac{\partial \sigma_d}{\partial(\varphi_h - \varphi_b)} = q\sqrt{\frac{2\varepsilon_0 \varepsilon_b N_A c_0}{k_B T}} \cosh\left[\frac{q(\varphi_h - \varphi_b)}{2k_B T}\right] \tag{A.9}$$

In the Stern layer, the volume charge density is assumed to be zero, so that Poisson's equation implies a constant electric field and a linear potential increase within this region. The region will therefore have a capacitance per area given by the simple relation:

$$C'_h = \frac{\varepsilon_0 \varepsilon_h}{x_h} \tag{A.10}$$

where x_h is the distance between the Helmholtz plane and the dielectric surface, and ε_h is the relative permittivity of the electrolyte in the Stern layer [22, 20].

The double-layer can thus be modeled as a series combination of two capacitors, where the diffuse layer capacitance is nonlinear and the Stern capacitance is linear. The total capacitance per area of the electrolyte double-layer C'_{dl} will then be given by:

$$C'_{dl} = \frac{1}{\frac{1}{C'_d} + \frac{1}{C'_h}} \tag{A.11}$$

This capacitance provides the desired relationship between the surface charge density σ_0 and the potential difference $\Psi = \varphi_0 - \varphi_b$, expressible in the form:

$$\frac{\partial \sigma_0}{\partial \Psi} = C'_{dl} \tag{A.12}$$

Note that C'_{dl} is generally a function of Ψ so that it is not constant. Nonetheless it can be approximately constant if the variation of Ψ is small.

If there were no additional capacitances connected to the dielectric surface (for example if the dielectric was replaced by a conductor at a fixed potential, with no parasitic capacitances anywhere else) then we could integrate this equation over the small range of potentials to find σ_0. However, the sensing dielectric will have a capacitance that couples to another potential at the channel or floating gate of the MOSFET (depending on the structure used for the ISFET). There may also be parasitic capacitances to other sources of

potential. Taking such effects into account, σ_0 will in general be a weighted sum of different terms $C_i'(\varphi_0 - \varphi_i)$ where the C_i' represent various capacitances per area in the circuit, and φ_i represent the potentials fixed at the other side of these capacitances. The effect of the sensing dielectric capacitance is considered in Chapter 3.

It is also interesting to note that in such cases, the total charge in the electrolyte appears to not be preserved during changes of pH (the electrolyte is assumed neutral in the absence of any electric field) since the diffuse region will consist of dominantly positive or negative ions near the surface that are not cancelled completely by σ_0. This must be compensated by the presence of some current flow, which could be provided by the reference electrode or other sources of potential. If the change in pH is very slow, these currents should be negligibly small, however.

A.0.4 Intrinsic buffer capacity and pH sensitivity

It is ultimately of interest to know the sensitivity of Ψ with respect to changes in the bulk pH. In order to do so, it is useful to first define the intrinsic buffer capacity β_{int} of the sensitive dielectric by [20]:

$$\frac{\partial \sigma_0}{\partial \mathrm{pH_s}} = -q\beta_{int} \tag{A.13}$$

where $\mathrm{pH_s}$ is the pH near the surface of the dielectric, and β_{int} is the intrinsic buffer capacity. It represents the number of surface binding sites per area that are affected by a small change in electrolyte potential. An explicit formula for β_{int} in terms of material properties can be obtained by using the equation (A.5) and $a_{\mathrm{H}_s^+} = 10^{-\mathrm{pH_s}}$:

$$\beta_{int} = 2.303 N_s \frac{K_a K_b + 4K_a a_{\mathrm{H}_s^+} + a_{\mathrm{H}_s^+}^2}{\left(K_a K_b + K_b a_{\mathrm{H}_s^+} + a_{\mathrm{H}_s^+}^2\right)^2} K_b a_{\mathrm{H}_s^+} \tag{A.14}$$

Combining (A.13) with (A.12) through the chain rule, we obtain the result for the sensitivity of Ψ to local changes in $\mathrm{pH_s}$:

$$\frac{\partial \Psi}{\partial \mathrm{pH_s}} = -\frac{q\beta_{int}}{C_{dl}'} \tag{A.15}$$

Using the chain-rule and the relation $\mathrm{pH_s} = \mathrm{pH} + \frac{q\Psi}{2.303 k_B T}$ obtained by taking logarithms in (A.6), we obtain the pH-sensitivity, after some rearranging, as:

$$\frac{\partial \Psi}{\partial \mathrm{pH}} = -2.303 \frac{k_B T}{q} \alpha \tag{A.16}$$

where α is the sensitivity parameter

$$\alpha = \frac{1}{2.303\frac{k_B T C'_{dl}}{q^2 \beta_{int}} + 1} \tag{A.17}$$

It is clear from (A.17) that the sensitivity parameter must be between 0 and 1, and that the theoretical maximal value of 1 is approached by maximizing β_{int} and minimizing C'_{dl}. Since C'_{dl} is a nonlinear function of the potential and bulk ion concentrations, it is desirable to reduce its influence on Ψ by having $\beta_{int} \gg \frac{k_B T}{q^2} C'_{dl}$. This provides the theoretical maximum for the pH sensitivity, which at $T = 293$ K (or 20 °C) is 58.2 mV/pH. This is also the theoretical pH sensitivity of the glass electrode. So in general ISFET sensors are limited in their sensitivity by this upper bound. It is of course possible to increase the sensitivity further by electronic amplification, however the signal-to-noise ratio will not be improved since this amplification will also affect the noise coming from the electrolyte and add its own sources of noise as noted in section 2.1.4.

Assuming α to be constant with pH, equation (A.16) can be integrated to obtain a direct relationship between Ψ and pH as

$$\Psi = -2.303\frac{k_B T}{q}\alpha(\mathrm{pH} - \mathrm{pH_{pzc}}) \tag{A.18}$$

where $\mathrm{pH_{pzc}}$ is the *point of zero charge*. The parameter $\mathrm{pH_{pzc}}$ acts as an integration constant, and its value depends on other factors than those considered here. The complete analysis of the ISFET frontend is presented in Chapter 3.

The pH sensitivity is maximized by increasing the intrinsic buffer capacity β_{int}. This has the additional benefit of improving the linearity, since the sensitivity parameter α remains close to 1 and becomes less sensitive to changes in C'_{dl}. From (A.14), it is clear that β_{int} is larger for materials that have a large density of surface binding sites N_s. The dielectric commonly used for MOSFET gate oxides is silicon dioxide (SiO_2). However SiO_2 is not the best material for pH sensing applications. It was found that materials such as silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3) and tantalum pentoxide (Ta_2O_5) have larger sensitivities and better linearity. In fact Ta_2O_5 has a sensitivity very close to the theoretical maximum. This is due to the much larger amount of dangling bonds present in such materials.

Appendix B

Derivation of Gouy-Chapman Model

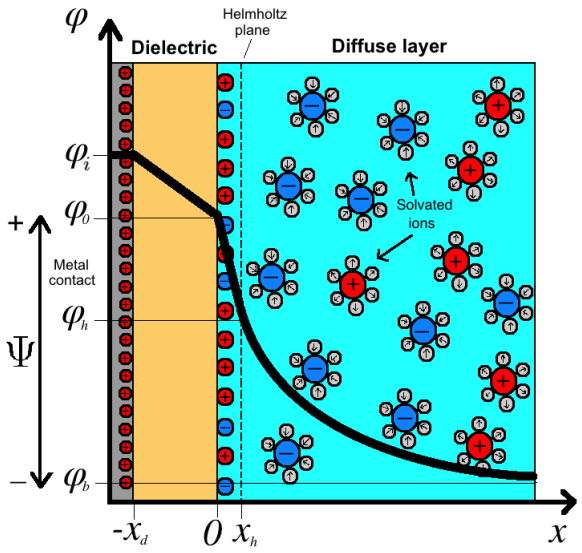
In this Appendix will be presented a more detailed analysis of the electrolyte interface and the derivation of the Gouy-Chapman model for the electrolyte-double layer capacitance. Consider a material surface placed in an aqueous electrolyte at thermal equilibrium. We assume the geometry is planar and the system is translation-invariant in the y and z directions. The material surface interfacing with the electrolyte is placed on the plane $x = 0$, and increasing values of x go toward the bulk at infinity. In addition, we assume a physical system with a constant potential at infinity (the bulk) given by $\lim_{x\to\infty} \varphi(x) = \varphi_b$, and we assume charge neutrality in the bulk (the total sum of all charges in the bulk is zero).

As mentioned in section A.0.2, in thermodynamic equilibrium the distribution of ions in the solution satisfies the Boltzmann equation (A.6). As formulated previously, this equation uses the activity of the ions, but at low concentrations, the activities can be replaced with the molar concentrations. Therefore in equilibrium, the ions in the solution are distributed according to the Boltzmann distribution:

$$c_i = c_{i0} e^{-\frac{q z_i (\varphi - \varphi_b)}{k_B T}} \tag{B.1}$$

where c_i is the concentration of the i-th ionic species at a given point (in mol / m^3), c_{i0} is the bulk concentration of the i-th ionic species, q is the elementary charge (in C), φ is the potential at a given point (in V), z_i is the valence of the i-th ionic species (unitless), k_B is Boltzmann's constant (in J / K) and T is the absolute temperature (in K). The condition of charge neutrality in the bulk can be written as

$$\sum_i c_{i0} z_i = 0 \tag{B.2}$$



The potential φ satisfies Poisson's equation, which in one dimension is given by:

$$\frac{\mathrm{d}^2\varphi}{\mathrm{d}x^2} = \frac{\rho}{\varepsilon_0 \varepsilon} \tag{B.3}$$

Here ε_0 is the dielectric permittivity of vacuum (in F / m), ε is the relative permittivity of the material (unitless) and ρ is the volume charge density (in C / m^3). The charge density of the i-th ionic species is $\rho_i = qN_A c_i z_i$, where N_A is Avogadro's constant (in mol^{-1}). Using (B.1) we find that the volume charge density in the electrolyte is given by

$$\rho = \sum_i \rho_i = qN_A \sum_i c_{i0} z_i e^{-\frac{qz_i(\varphi-\varphi_b)}{k_B T}} \tag{B.4}$$

Using this expression for ρ in the Poisson equation, we obtain what is called the one-dimensional Poisson-Boltzmann equation for the potential in the electrolyte:

$$\frac{\mathrm{d}^2\varphi}{\mathrm{d}x^2} = \frac{qN_A}{\varepsilon_0 \varepsilon_b} \sum_i c_{i0} z_i e^{-\frac{qz_i(\varphi-\varphi_b)}{k_B T}} \tag{B.5}$$

We use ε_b for the relative permittivity of the bulk. We now multiply (B.5) by $\frac{\mathrm{d}\varphi}{\mathrm{d}x}$ and integrate from x to x' to obtain

$$\tfrac{1}{2}\left(\tfrac{\mathrm{d}\varphi}{\mathrm{d}x}\right)^2\Big|_x - \tfrac{1}{2}\left(\tfrac{\mathrm{d}\varphi}{\mathrm{d}x}\right)^2\Big|_{x'} = \tfrac{N_A k_B T}{\varepsilon_0 \varepsilon_b} \sum_i c_{i0} \left(e^{-\frac{qz_i(\varphi-\varphi_b)}{k_B T}} - e^{-\frac{qz_i(\varphi'-\varphi_b)}{k_B T}} \right) \tag{B.6}$$

We used $\varphi = \varphi(x)$ and $\varphi' = \varphi(x')$. Due to the boundary condition $\lim_{x\to\infty} \varphi(x) = \varphi_b$ we see that as $x' \to \infty$, the right hand side of this equation converges.

Therefore the left-hand side must also converge, and so $\lim_{x\to\infty}\left(\frac{\mathrm{d}\varphi}{\mathrm{d}x}\right)^2$ exists. Since φ was assumed twice-differentiable by the use of Poisson's equation, its derivative must be continuous so the sign of $\frac{\mathrm{d}\varphi}{\mathrm{d}x}$ cannot change, and hence $\frac{\mathrm{d}\varphi}{\mathrm{d}x}$ must also converge to some limit. But if the limit exists, it must be that $\lim_{x\to\infty}\frac{\mathrm{d}\varphi}{\mathrm{d}x}=0$, otherwise the function φ would not be bounded. We can therefore take the limit as $x'\to\infty$ and rearrange to find that

$$\frac{\mathrm{d}\varphi}{\mathrm{d}x}=\pm\sqrt{\frac{2N_Ak_BT}{\varepsilon_0\varepsilon_b}\sum_i c_{i0}\left(e^{-\frac{qz_i(\varphi-\varphi_b)}{k_BT}}-1\right)} \tag{B.7}$$

We now add the assumption that all ions have valence $+1$ or -1. Let $S_+=\{i:z_i=+1\}$ and $S_-=\{i:z_i=-1\}$. The sum in equation (B.7) can be partitioned into sums over the sets S_+ and S_-:

$$\tfrac{\mathrm{d}\varphi}{\mathrm{d}x}=\pm\sqrt{\tfrac{2N_Ak_BT}{\varepsilon_0\varepsilon_b}\left[\left(\sum_{i\in S_+}c_{i0}\right)\left(e^{-\frac{q(\varphi-\varphi_b)}{k_BT}}-1\right)+\left(\sum_{i\in S_-}c_{i0}\right)\left(e^{\frac{q(\varphi-\varphi_b)}{k_BT}}-1\right)\right]} \tag{B.8}$$

We also note that charge neutrality becomes $\sum_{i\in S_+}c_{i0}-\sum_{i\in S_-}c_{i0}=0$, and we can therefore introduce a new symbol $c_0=\sum_{i\in S_+}c_{i0}=\sum_{i\in S_-}c_{i0}$, which represents the total concentration of positive (or negative) ions in the bulk. We can now write:

$$\frac{\mathrm{d}\varphi}{\mathrm{d}x}=\pm\sqrt{\frac{2N_Ak_BTc_0}{\varepsilon_0\varepsilon_b}\left(e^{\frac{q(\varphi-\varphi_b)}{k_BT}}+e^{-\frac{q(\varphi-\varphi_b)}{k_BT}}-2\right)} \tag{B.9}$$

We use the identity $e^x+e^{-x}-2=\left(e^x-e^{-x}\right)^2=4\sinh^2(x)$ to obtain:

$$\frac{\mathrm{d}\varphi}{\mathrm{d}x}=-\sqrt{\frac{8N_Ak_BTc_0}{\varepsilon_0\varepsilon_b}}\sinh\left[\frac{q(\varphi-\varphi_b)}{k_BT}\right] \tag{B.10}$$

Note that we have now made a choice in the negative sign. This follows from physical considerations. When $\varphi>\varphi_b$, the derivative of φ should be negative in order to keep φ bounded as $x\to\infty$. Similarly when $\varphi<\varphi_b$, the derivative should be positive in order for φ to converge to φ_b as $x\to\infty$.

We remark that (B.10) is only valid as long as the ions follow the Boltzmann distribution. At some distance x_h to the surface, the solvated ions are unable to move any closer due to their finite radius including the surrounding shell of polarized water molecules. This distance defines the Helmholtz plane, in which the volume charge density is zero. The relative permittivity of the

solution between the interface and the Helmholtz plane is denoted by ε_h. Hence within the Helmholtz plane we obtain the Poisson equation $\frac{\mathrm{d}^2\varphi}{\mathrm{d}x^2} = 0$ instead. Therefore the slope of φ is constant in this region and we can use the Gauss boundary condition at x_h (assuming no surface charge density at x_h):

$$\varepsilon_0\varepsilon_h \frac{\mathrm{d}\varphi}{\mathrm{d}x}\bigg|_{x=x_h^-} = \varepsilon_0\varepsilon_b \frac{\mathrm{d}\varphi}{\mathrm{d}x}\bigg|_{x=x_h^+} = \sigma_d \tag{B.11}$$

where the effective surface charge density σ_d is given by:

$$\sigma_d = -\sqrt{8\varepsilon_0\varepsilon_b N_A k_B T c_0}\,\sinh\left[\frac{q(\varphi_h - \varphi_b)}{2k_B T}\right] \tag{B.12}$$

This equation corresponds to equation (A.8) which was presented in the Gouy-Chapman model. But it should be clear that σ_d is not an actual surface charge density since the ions are distributed continuously in the volume. Instead it should be thought of as an equivalent surface charge that produces the net electrical displacement field at the Helmholtz plane.

Appendix C

Spectre Model of ISFET

```
// VerilogA for pHSensor, ph_membrane_params, veriloga_Si3N4

`include "constants.vams"
`include "disciplines.vams"

module ph_membrane_params(ph, bulk, ohp, ihp, sensg, floatg, Ifg, Vohp, Vihp, Vsensg,
Vfloatg, Cgouy, Cohelm, Cihelm, Csens);
  input ph, bulk, ohp, ihp, sensg, floatg, Ifg;
  output Vohp, Vihp, Vsensg, Vfloatg, Cgouy, Cohelm, Cihelm, Csens;
  electrical ph, bulk, ohp, ihp, sensg, floatg, Ifg, Vohp, Vihp, Vsensg, Vfloatg, Cgouy,
  Cohelm, Cihelm, Csens;

  // Physical constants
  localparam real NAv = 6.022e23; // Avogadro's constant [1/mol]

  // ISFET geometrical parameters
  localparam real sens_w = 400u; // sensing gate width [m]
  localparam real sens_l = 400u; // sensing gate length [m]
  localparam real sens_t = 10n; // thickness of sensing gate dielectric [m]

  // ISFET electrochemical parameters at 25 C
  // Source: Grattarola et al. "Modeling H+-Sensitive FET's with SPICE" for Si3N4
  //  Ajay et. al. "Analytical Model of pH sensing Characteristics of Junctionless Silicon
  on Insulator ISFET" for Ta2O5
  localparam real dohp = 0.3n; // thickness of outer Helmholtz plane [m]
  localparam real dihp = 0.1n; // thickness of inner Helmholtz plane [m]
  localparam real Ka = 15.8; // positive dissociation constant (use 1.0e-2 for Ta2O5)
  localparam real Kb = 63.1e-9; // negative dissociation constant (use 1.0e-4 for Ta2O5)
  localparam real Kn = 1e-10; // dissociation constant for amine sites
  localparam real Nsil = 3.0e18; // silanol (or oxide) surface site density [1/m^2] (use
  1.0e19 for Ta2O5)
  localparam real Nnit = 2.0e18; // amine surface site density [1/m^2] (use 0 for Ta2O5)
  localparam real cbulk = 0.1; // electrolyte concentration [mol/L]
  localparam real epsw = 78.5; // relative permittivity of the bulk electrolyte solution
  localparam real epsohp = 32; // relative permittivity of the Outer Helmholtz layer
  localparam real epsihp = 32; // relative permittivity of the Inner Helmholtz layer
  localparam real epssg = 7.5; // relative permittivity of the sensing gate dielectric (use
   22 for Ta2O5)
  localparam real Qtcfg0 = 0; // initial trapped charge in the floating gate [C]

  real T; // temperature [K]
  real Vt; // thermal voltage [V]
```

```
real pKa, pKb, pKn; // -log10(Ka), -log10(Kb), -log10(Kn) used to get better scaling in
log-domain for numerical solution
real z1, z2, z3; // ln(10)*(pKa + pKb - 2*pH), ln(10)*(pKb - pH) and ln(10)*(pKn - pH)
real fa, fb; // components of the expression for surface charge density (sigma0)
real sq; // sqrt(8*e0*eb*NA*k*T*c0) [C/m^2]
real sigma0; // surface charge stored on the sensing gate dielectric due to surface-
binding and trapped charge [C/m^2]
real A; // sensing membrane area [m^2]
real CCgouy, CCohelm, CCihelm, CCsens; // capacitances [F]

real Qs, Qfg; // total charge on sensing gate and on floating gate nodes [C]
real vNsil, vNnit;

// We assume quasistatic equilibrium, i.e. at all times the ion concentrations follow the
 Boltzmann distribution and the site-binding reactions at the surface are at equilibrium.
 This holds if pH and ref vary sufficiently slow compared to the rate of the thermal
settling and the chemical reaction rate.

analog begin
  vNsil = Nsil;
  vNnit = Nnit;

  T = $temperature;
  Vt = $vt;

  A = sens_w * sens_l;
  sq = sqrt(8 * `P_EPS0 * epsw * NAv * `P_K * T * 1000 * cbulk); // The factor of 1000
  comes from converting m^3 to L

  pKa = -log(Ka);
  pKb = -log(Kb);
  pKn = -log(Kn);

  z1 = ln(10) * (pKa + pKb - 2 * V(ph));
  z2 = ln(10) * (pKa - V(ph));
  z3 = ln(10) * (pKn - V(ph));

  fa = (1 - limexp(2 * V(sensg, bulk) / Vt - z1)) / (1 + limexp(V(sensg, bulk) / Vt - z2)
  + limexp(2 * V(sensg, bulk) / Vt - z1));
  fb = 1 / (1 + limexp(V(sensg, bulk) / Vt - z3));
  sigma0 = (`P_Q * Nsil) * fa + (`P_Q * Nnit) * fb;

  // Compute the capacitance values, where Cgouy is linearized at the operating point
  CCgouy = A * (sq / (2 * Vt)) * cosh(V(ohp, bulk) / (2 * Vt));
  CCohelm = A * `P_EPS0 * epsohp / dohp;
  CCihelm = A * `P_EPS0 * epsihp / dihp;
  CCsens = A * `P_EPS0 * epssg / sens_t;

  Qs = A * sigma0;
  Qfg = Qtcfg0 - idt(V(Ifg), 0);

  // Interface with the schematic, these values are used to set the capacitances of the
  varcaps
  V(Cgouy) <+ CCgouy;
  V(Cohelm) <+ CCohelm;
  V(Cihelm) <+ CCihelm;
  V(Csens) <+ CCsens;

  // Gaussian surface with faces on floating gate and ohp.
  // We know from the Poisson-Boltzmann equation that the electric field on the ohp
  // is given by D = sq * sinh(V(ohp, bulk) / (2 * Vt)) (where D is displacement field).
```

```
    // But the surface encloses total charge Qfg + Qs so we can use Gauss law to find the
    electric field.
    // This gives Qfg + Qs = A * sq * sinh(V(ohp, bulk) / (2 * Vt)).
    V(Vohp) <+ V(bulk) + 2 * Vt * asinh((Qfg + Qs) / (A * sq));

    // The electric field at the floating gate is 0, so we can take a box that encloses fg,
    sensg and the node of interest is at the other surface
    // We assume no coupling to the MOSFET capacitances, which is reasonable since they are
    much smaller than Csens, so all charge is on the other surface.
    // Then we use Gauss's law to find the electric field at the surface of interest, and
    evaluate the potential.
    V(Vihp) <+ V(ohp) + (Qfg + Qs) / CCohelm;
    V(Vsensg) <+ V(ihp) + (Qfg + Qs) / CCihelm;
    V(Vfloatg) <+ V(sensg) + Qfg / CCsens;
  end
endmodule
```