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MONOCRYSTALLINE $CuInSe_2$ PHOTOVOLTAIC CELLS WITH A CdO WINDOW LAYER

by

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ABSTRACT

Photovoltaic cells having the structures $CuInSe_2$-CdO and $CuInSe_2$-CdS-CdO have been fabricated on a cut or cleaved p-type Bridgman-grown $CuInSe_2$ ingot. The CdO window layer in both cases was deposited by dc reactive sputtering. In the $CuInSe_2$-CdS-CdO structures, the CdS interlayer was deposited by a solution growth method and these cells, incorporating the CdS interlayer, yielded a conversion efficiency of about 6.9%. By comparison, the cell with the structure $CuInSe_2$-CdO, where the lattice mismatch between the $CuInSe_2$ and the CdO is some 23%, showed a surprising efficiency of 6.8%. This result, indicating that the defect centers at the $CuInSe_2$-CdO interface arising from the large lattice mismatch, play a smaller role than expected, suggests that the seat of photovoltaic action may lie away from the substrate-window layer interface as a buried homojunction within the $CuInSe_2$. While the conversion efficiencies of the two kinds of cells were similar, there were slight differences in their other characteristics whereby the device without the CdS interlayer had a higher illuminated open circuit voltage, lower short circuit current density, higher forward ideality factor above 2 and higher internal series resistance. The acceptor concentration of the stoichiometrically-prepared $CuInSe_2$ was estimated to be about 10^{17} cm^{-3} in the bulk of the wafers but almost an order of magnitude smaller than this near the surface after annealing in argon. Using the photocurrent-capacitance method, minority electron diffusion lengths in the $CuInSe_2$ were estimated to be about 3 μm for the devices made with cleaved substrates and about half this value for the cells made with abrasively-polished substrates.

RÉSUMÉ

Des cellules photovoltaïques comportant des structures $CuInSe_2$-CdO et $CuInSe_2$-CdS-CdO ont été fabriquées sur un lingot de $CuInSe_2$ de type-p coupé ou clivé produit par la méthode de Bridgman. Dans les deux cas, la couche-fenêtre de CdO a été déposée par le procédé de pulvérisation réactive en courant continu (c.c.). Dans les structures $CuInSe_2$-CdS-CdO, la couche intermédiaire de CdS est déposée par la méthode du bain chimique, et ces cellules, qui comportent une couche intermédiaire de CdS ont produit un rendement de conversion de ~6.9%. Par comparaison, la cellule de $CuInSe_2$-CdO où l'erreur d'adaptation cristalline entre les couches de $CuInSe_2$ et de CdO est d'environ 23%, a produit un rendement de conversion surprenant de 6.8%. Ce résultat imprévu indique que les centres de défaut que l'importante erreur d'adaptation crée à l'interface $CuInSe_2$-CdO jouent un rôle moins important qu'on ne l'avait cru. Il semble donc que l'action photovoltaïque s'exerce à distance de la jonction couche fenêtre/substrat sous la forme d'une homojonction enfouie dans le $CuInSe_2$. Bien que le rendement de conversion de ces deux genres de cellules soit similaire, on a observé de légères différences en ce qui a trait aux autres caractéristiques: le dispositif dépourvu de couche intermédiaire de CdS a produit une tension en circuit ouvert plus élevée et une densité de court-circuit plus faible, en plus de présenter un facteur d'idéalité supérieur à 2 et une resistance de série interne plus forte que la cellule comportant une couche intermédiare de CdS. On a estimé à 10^{17} cm^{-3} la concentration d'accepteur du substrat $CuInSe_2$ stoechiometrique dans la masse des pastilles, alors qu'elle était inférieure de près d'un ordre de grandeur à la surface après recuite en présence d'argon. En utilisant la méthode du photocourant-capacité on a aussi estimé que les longueurs de diffusion des porteurs minoritaires dans le $CuInSe_2$ étaient d'environ 3 μm pour les cellules fabriquées sur les substrats clivés et d'environ la moitié de cette valeur pour les cellules fabriquées à partir de substrats polis par abrasion.

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CHAPTER 1

INTRODUCTION

As world energy consumption and demand increases, there are growing concerns of exhausting conventional non-renewable energy resources such as coal, oil and wood. This, combined with the increasing pressure from international environmental agencies who call for "clean" or "pollution-free" energy resources, raises interest in alternative "clean" energy resources. Photovoltaic energy is one of several promising renewable energy resources. With continuous decrease of cost and increase of conversion efficiencies, large-scale photovoltaic systems may soon be in use as supplementary alternative energy sources.

The chalcopyrite semiconductor $CuInSe_2$ is a serious candidate material for the absorber layer of a thin film solar cell. This is because of its exceptionally high optical absorption coefficient over the solar spectrum wavelengths, as shown in Figure 1.1. Other contender materials for thin film cells are hydrogenated amorphous silicon and cadmium telluride. However, $CuInSe_2$, in a structure of the form $Cu(In,Ga)Se_2/CdS/ZnO$, has given a higher solar conversion efficiency in laboratory samples than the other two materials and has exhibited excellent performance stability over long periods of time under continuous illumination [1.1][1.2].

Polycrystalline material has been used in the best solar cells because in this form,

layer control is easier and lower temperatures are used during the fabrication process than for the fabrication with monocrystalline material. Despite this, much of the progress in increasing the photovoltaic performance in $CuInSe_2$ - based cells has come about through empirical methods without knowing exactly the action involved. Therefore, much work needs to be done to understand more precisely the factors that control the photovoltaic action in devices using $CuInSe_2$. It is for this reason that work on single crystal $CuInSe_2$ photovoltaic cells was done and is now reported in this thesis by the author.

The study described herewith follows on from the work of Z.A. Shukri [1.3], who pioneered a unique method of preparing monocrystals of $CuInSe_2$, involving a one-ampoule process with a boron nitride inner ampoule coating to prevent adhesion of the grown ingot to the ampoule wall [1.4], thus avoiding ingot cracking and voids. Some preliminary photovoltaic devices using monocrystalline $CuInSe_2$ substrates were also fabricated by Shukri and Champness [1.5]. The main purpose of the present work was to determine whether a small lattice mismatch between the absorber layer of $CuInSe_2$ and the traditional CdS window layer was really necessary. If a structure of the form $CuInSe_2$/CdS is considered to involve a pn heterojunction in its photovoltaic action, then there should be a minimum of defects at the $CuInSe_2$ - CdS interface, since these can act as recombination centers, which can consume much of the photogenerated current, leaving less current at the output terminals. Thus, since the lattice mismatch between CdS and the chalcopyrite is only about 1% ($\sqrt{2}\, a_{CdS}$ [1.6] - $a_{CuInSe2}$ = 5.850 - 5.782 Å = 0.068 Å), the former material has been the optimum choice as the n-type partner in the junction for $CuInSe_2$ cells. The work reported

here, however, uses cells with a different window material, CdO and raises questions about the nature and location of the seat of photovoltaic action. By using single crystal substrate cells, there are no grain boundaries in the absorber layer to confuse the process. With a rocksalt structure, CdO has an a-parameter of 4.689 Å, while $CuInSe_2$, with a chalcopyrite structure (c/a = 2.008 [1.7]), has an a-parameter of 5.782 Å. The difference of these values constitutes a lattice mismatch between the two materials of some 23 %. Thus, CdO as a window layer, constitutes a junction with a very large lattice mismatch, even though the energy gap of CdO (2.4 eV) [1.8] is similar to that of CdS (2.42 eV) [1.9].

Two kinds of photovoltaic cells were fabricated and studied in this work and these are indicated schematically in Figures 1.2 (a) and (b). The device in Figure 1.2 (a) was made essentially by reactive sputtering a layer of cadmium oxide on a wafer of p-type $CuInSe_2$, obtained from an ingot grown by a Bridgman method. The cell in Figure 1.2 (b) was made in the same way but, prior to the sputtering of the CdO, a thin layer of CdS was deposited on the $CuInSe_2$ substrate by a chemical bath method. The work in this thesis consists of the fabrication of these two kinds of cells and the determination of their characteristics from measurements made on them. The measurements were current as a function of voltage, both under solar irradiation and in darkness, capacitance as a function of voltage and frequency, spectral photovoltaic response over the wavelength range 400 to 1300 nm and photocurrent-capacitance variation with bias under monochromatic light to estimate minority diffusion lengths, where possible.

A comprehensive review of the progress made on photovoltaic cells using $CuInSe_2$ - based cells is beyond the scope of the present thesis because of the enormous number of papers involved, especially in thin film polycrystalline devices. However, since the present work involved only *monocrystalline* substrate cells, it is helpful to review briefly the history of just those photovoltaic cells using single crystal $CuInSe_2$ as the absorber layer. The first cell reported with a significant performance was in 1974 when Wagner, Shay, Migliorato and Kasper [1.10] of the Bell Telephone Laboratories obtained a solar conversion efficiency of about 5 % in a device where CdS was evaporated, from separate Cd and S sources, on a substrate of melt-grown $CuInSe_2$. The substrate was previously made p-type by a 24 hour heat-treatment in a selenium atmosphere. About a year later, workers from the same laboratories reported [1.11] fabrication of a $CuInSe_2$/CdS cell with a conversion efficiency of 12 %. This was obtained using an antireflection coating of SiO, without which the efficiency was estimated to be about 10.6 %. The {112} B face of the $CuInSe_2$ was employed for the deposition of the CdS, which was 5-10 μm thick. Because of microcracks in the $CuInSe_2$, the cell area was only 0.79 mm^2 . The contact metal to the CdS was a Ga-In eutechtic and that to the p-type $CuInSe_2$ substrate was gold [1.12]. Following this spectacular result, many papers were published on cells using thin film polycrystalline substrates of $CuInSe_2$ because of the lower cost of fabrication of such devices. Eventually the 12 % efficiency value was exceeded and at the present time about 18 % has been reported in polycrystalline devices [1.1][1.2]. For monocrystalline cells, however, very few papers were published in the years following the Bell Laboratories' results. In 1978, Kazmerski and Sheldon [1.13] reported a conversion efficiency of 8.5 % on a cell with a window layer of

indium tin oxide [ITO], instead of CdS, which was evaporated on Bridgman-grown $CuInSe_2$. In 1980, a cell was reported where $CuInSe_2$ was deposited by molecular beam epitaxy (MBE) on the (001) B face of monocrystalline CdS by Grindle, Clark, Rezaie-Serej, Falconer, McNeily and Kazmerski [1.14]. They obtained a conversion efficiency of 4.7 % under simulated solar irradiation of 100 mW/cm^2. In 1983, Arya, Warminsky, Beaulieu, Kwietniak, Loferski and Giriat [1.15] reported an efficiency of 5.9 % on a cell of area 4.5 mm^2, where CdS was evaporated on to a wafer of large multi-grain $CuInSe_2$. However, on reducing the cell area to 0.8 mm^2, they obtained an efficiency of 10.6 %, which equalled, but did not exceed, the Bell workers' result [1.11] of 1975. In the period since 1975, there have been papers on homojunctions in $CuInSe_2$ produced by introducing Cd [1.16][1.17] or In [1.18] into monocrystalline material; these devices showed photovoltaic behaviour, but no conversion efficiencies were reported. The next significant result came from our own laboratory at McGill where L.S. Yip and I. Shih [1.19] reported in 1994 a cell with the structure $CuInSe_2$/CdS/ZnO, which yielded an efficiency of 11 % without an antireflection coating. While the efficiency was greater than that of Shay et al [1.11], the most significant feature was the cell area of 8 mm^2, which was an order of magnitude greater than that of the previous devices of Shay et al [1.11] and of Arya et al [1.15]. Since 1994, no further increases in efficiency have been announced but it is believed that the use of a quaternary monocrystalline chalcopyrite substrate will lead to still improved photovoltaic cell performance.

The structure of the thesis is as follows. Firstly chapter 2 presents the equivalent

circuit model of a photovoltaic cell with a formal method of extracting series and shunt resistances from gradients in the illuminated current-voltage characteristics. Chapter 3 describes the fabrication process of the cells and the method of the measurements made on them is described in chapter 4. The experimental results are presented in chapters 5 and 6 and are analyzed and discussed comprehensively in chapter 7 along with a summary and ideas for future work.

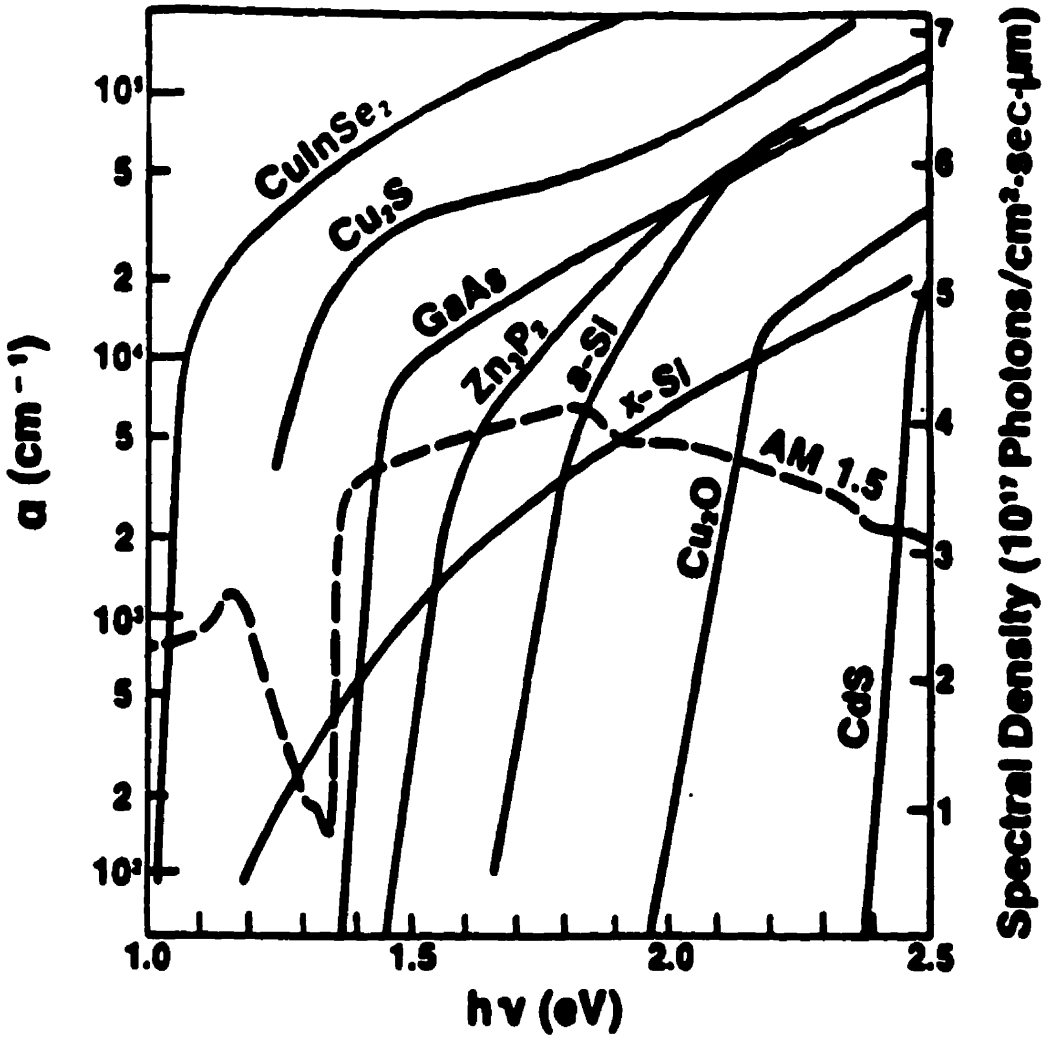
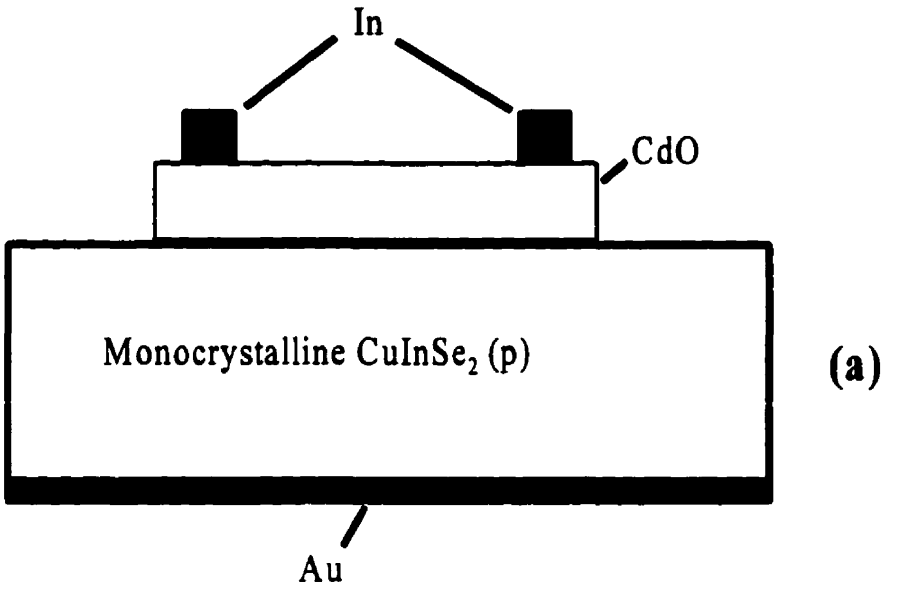


Figure 1.1 Plot of optical absorption coefficient against incident photon energy for selected semiconductor materials (After K. Mitchell and S. Wagner, Tutorial Notebook, 20th IEEE Photovoltaic Specialists Conf., 1988).



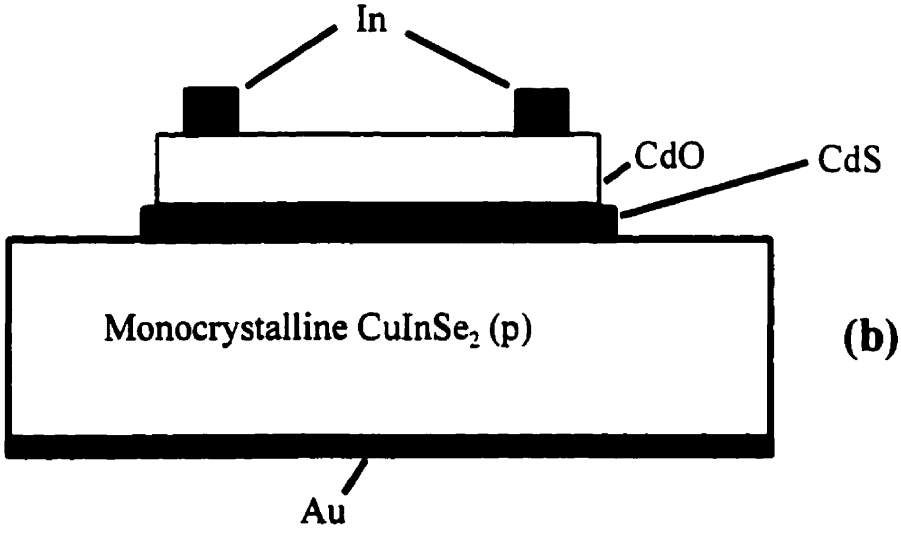


Figure 1.2 Schematic diagram of the photovoltaic cell structures used in this study (a) without the CdS interlayer and (b) with the CdS interlayer present.

CHAPTER 2

THEORETICAL CONSIDERATIONS

2.1 INTRODUCTION

While most of the theory of photovoltaic cells is to be found conveniently in text books, such as M.A. Green [2.1], it is helpful to review certain basic ideas before the fabrication of the cells, the measurements made on them and the results are presented in chapters 3, 4, 5 and 6. Thus, in the present chapter, the equivalent circuit model of a cell is considered, both ideally and with equivalent series and shunt resistances. Then the basic energy band diagram of a heterojunction $CuInSe_2$ - CdS cell is presented.

2.2 CIRCUIT MODEL OF PHOTOVOLTAIC CELL

(a) Ideal Diode Model

An ideal photovoltaic cell can be modeled simply as a current generator supplying a photoinduced current I_{ph} in parallel with an ideal diode as shown in Figure 2.1.

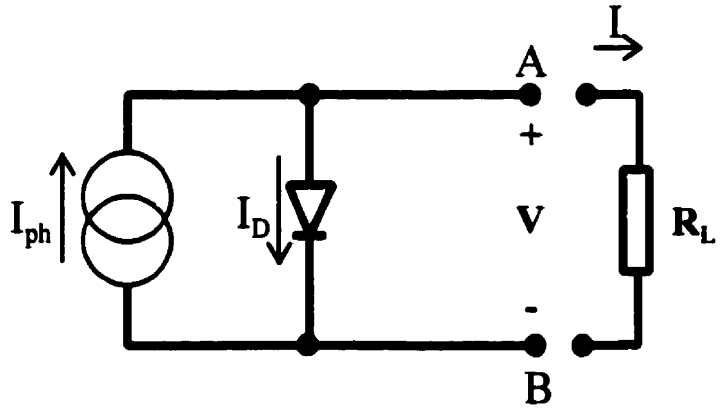


Figure 2.1 Ideal photovoltaic cell circuit model.

If the current through the diode is I_D, then the output current I from the terminals AB into the load R_L is given by:

$$I = I_{ph} - I_D = I_{ph} - I_o(e^{(\frac{qV}{nkT})} - 1) \quad , \tag{2.1}$$

where V is the voltage across terminals AB, I_o is the diode reverse saturation current, q is the electronic charge, k is Boltzmann's constant, T is the absolute temperature and n is the diode ideality factor.

For a short circuit at terminals AB (ie $R_L = 0$), V=0, the current I_{sc} is simply:

$$I = I_{sc} = I_{ph} \quad . \tag{2.2}$$

For an open circuit at terminals AB (ie $R_L = \infty$), I=0, so that equation (2.1) gives

$$I_{ph} = I_o \exp^{(\frac{qV_{oc}}{nkT})} \qquad if \quad \frac{nkT}{q} \ll V_{oc}$$

and the open circuit voltage is given by

$$V_{oc} = (\frac{nkT}{q}) \ln(\frac{I_{ph}}{I_o}) \quad . \tag{2.3}$$

(b) Model with Series and Shunt Resistances

A more realistic circuit model of an actual photovoltaic cell is shown in Figure 2.2. Here R_s represents an internal series resistance arising from resistances, such as those originating from the absorber semiconductor, the window layer and the metal contacts. The

quantity R_{sh} represents an equivalent shunt resistance arising from currents bypassing the junction through surface leakage, imperfections and tunnelling.

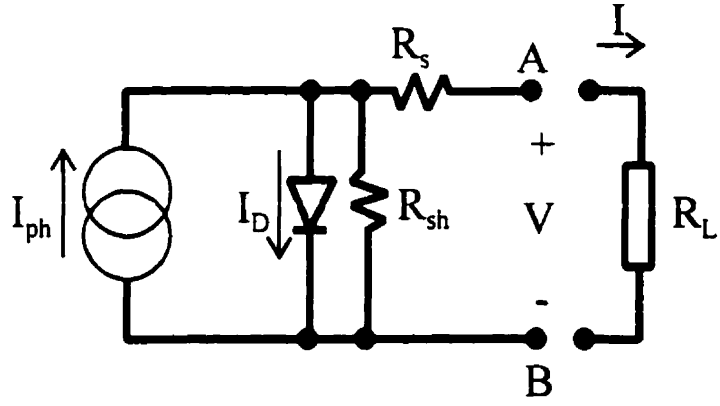


Figure 2.2 Real photovoltaic circuit model.

The current I at the output terminals AB, in this case, is given by:

$$I = I_{ph} - I_o(e^{\frac{q(V+IR_s)}{nkT}} - 1) - \frac{V+IR_s}{R_{sh}} \quad . \tag{2.4}$$

For short circuit conditions V=0, the current is:

$$I = I_{sc} = I_{ph} - I_o(e^{\frac{qIR_s}{nkT}} - 1) - \frac{IR_s}{R_{sh}} \quad . \tag{2.5}$$

For open circuit conditions I=0 and equation (2.4) with $V=V_{oc}$ yields:

$$0 = I_{ph} - I_o(e^{\frac{qV_{oc}}{nkT}} - 1) - \frac{V_{oc}}{R_{sh}} \quad . \tag{2.6}$$

so that

$$I_{ph} = I_o(e^{\frac{qV_{oc}}{nkT}} - 1) + \frac{V_{oc}}{R_{sh}} \qquad (2.6A)$$

and hence, if $V_{oc} >> nkT/q$ (~ 0.05 if n=2), then

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{(I_{ph} - V_{oc}/R_{sh})}{I_o}\right) \qquad (2.6B)$$

(c) Gradients of j-V Characteristics

In imperfect cells, the magnitudes of R_s and R_{sh} can sometimes be estimated from the gradients dV/dI, evaluated at the short circuit or open circuit conditions as shown in Figure 2.3.

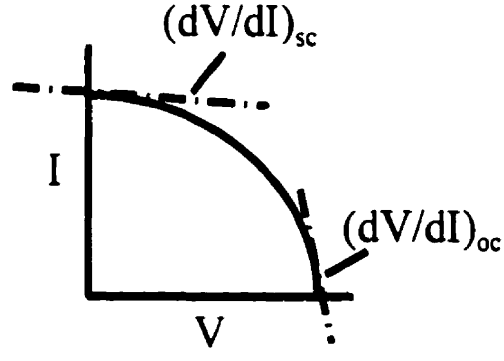


Figure 2.3 Gradients at short circuit and open circuit conditions.

Differentiating equation (2.4) yields:

$$\frac{dI}{dV} = -I_o\, e^{\frac{q(V+IR_s)}{nkT}} \cdot \frac{q}{nkT}\left(1 + R_s\frac{dI}{dV}\right) - \frac{1}{R_{sh}}\left(1 + R_s\frac{dI}{dV}\right) \qquad (2.7)$$

For short circuit, V=0, equation (2.7) gives:

$$\frac{dI_{sc}}{dV} + I_o\, e^{\frac{q(I_{sc}R_s)}{nkT}} \frac{q}{nkT}\left(1 + R_s\frac{dI_{sc}}{dV}\right) = -\frac{1}{R_{sh}}\left(1 + R_s\frac{dI_{sc}}{dV}\right)$$

Therefore:

$$R_{sh} = -\frac{1 + R_s\dfrac{dI_{sc}}{dV}}{\dfrac{dI_{sc}}{dV} + I_o\dfrac{q}{nkT}\, e^{\frac{q(I_{sc}R_s)}{nkT}}\left(1 + R_s\dfrac{dI_{sc}}{dV}\right)} \tag{2.8}$$

$$= -\frac{1}{\dfrac{dI_{sc}/dV}{1 + R_s\dfrac{dI_{sc}}{dV}} + I_o\dfrac{q}{nkT}\, e^{\frac{q(I_{sc}R_s)}{nkT}}} \tag{2.8A}$$

For open circuit conditions I=0, equation (2.7) gives:

$$\left(\frac{dI}{dV}\right)_{oc} = -I_o\, e^{\frac{qV_{oc}}{nkT}} \frac{q}{nkT}\left(1 + R_s\left(\frac{dI}{dV}\right)_{oc}\right) - \frac{1}{R_{sh}}\left(1 + R_s\left(\frac{dI}{dV}\right)_{oc}\right)$$

so that

$$\left(\frac{dI}{dV}\right)_{oc} + I_o\frac{q}{nkT}\, e^{\frac{qV_{oc}}{nkT}} + \frac{1}{R_{sh}} = -\frac{qI_o}{nkT}R_s\left(\frac{dI}{dV}\right)_{oc} e^{\frac{qV_{oc}}{nkT}} - \frac{R_s}{R_{sh}}\left(\frac{dI}{dV}\right)_{oc} = -R_s\left(\frac{dI}{dV}\right)_{oc}\left(\frac{qI_o}{nkT}e^{\frac{qV_{oc}}{nkT}} + \frac{1}{R_{sh}}\right)$$

Therefore:

$$R_s = -\frac{(\frac{dI}{dV})_{oc} + I_o \frac{q}{nkT} e^{\frac{qV_{oc}}{nkT}} + \frac{1}{R_{sh}}}{(\frac{dI}{dV})_{oc}(\frac{1}{R_{sh}} + \frac{qI_o}{nkT} e^{\frac{qV_{oc}}{nkT}})} \quad ,$$

and hence

$$R_s = -[\frac{1}{\frac{qI_o}{nkT} e^{\frac{qV_{oc}}{nkT}} + \frac{1}{R_{sh}}} + (\frac{dV}{dI})_{oc}] \quad . \qquad (2.9)$$

(d) Check for Ideal Cell

It is worthwhile checking equations (2.8) and (2.9) for an ideal cell with $R_s = 0$ and $R_{sh} = \infty$.

For V = 0, equation (2.8) gives:

$$R_{sh} = -\frac{1}{(\frac{dI}{dV})_{sc} + \frac{qI_o}{nkT}} = \infty \quad .$$

and hence $-(\frac{dI}{dV})_{sc} = \frac{qI_o}{nkT}$ = *dynamic conductance of diode at zero bias .*

For I = 0, equation (2.9) gives:

$$R_s = -\left[\frac{1}{\frac{qI_o}{nkT}e^{\frac{qV_{oc}}{nkT}}} + \left(\frac{dV}{dI}\right)_{oc}\right] = 0 \quad ,$$

$$\text{so that } -\left(\frac{dV}{dI}\right)_{oc} = \frac{nkT}{qI_o}e^{-\frac{qV_{oc}}{nkT}} = \text{dynamic resistance of diode cell at } V=V_{oc} .$$

Thus, in principle, values of R_{sh} and R_s can be estimated using equations (2.8A) and (2.9). However, this assumes that the equivalent circuit model of Figure 2.2 is a sufficiently good representation of an actual photovoltaic cell. In fact, the gradients are likely to give good estimates of R_s and R_{sh} only for a cell with a low fill factor, where the slopes at short circuit and open circuit conditions are sufficiently well-defined.

2.3 ENERGY BAND DIAGRAM FOR $CuInSe_2$ - CdS HETEROJUNCTION

(a) $CuInSe_2$ - CdS Junction

The simplified band diagrams for n-type CdS and p-type $CuInSe_2$ are given as separate semiconductors in Figure 2.4 (a). While accurate values for the electron affinities (χ) and donor (δ_n) and acceptor (δ_p) levels with respect to the band edges are not known, the values: $\chi_n = 4.5$, $\chi_p = 4.3$, $\delta_n = 0.2$ and $\delta_p = 0.1$ eV [1.12] are sufficient for descriptive purposes. Since the Fermi level in n-type CdS is higher than that in p-type $CuInSe_2$, electrons will eventually flow into the p-type material until equilibrium is established. With

the Fermi levels lined up, Figure 2.4 (b) shows that the built-in potential difference is given by:

$$qV_{bi} = [\chi_p + (E_{Gp} - \delta_p)] - (\chi_n + \delta_n) \quad ,$$

where E_{Gp} is the energy gap of the $CuInSe_2$, so that

$$V_{bi} = \frac{1}{q}[\chi_p - \chi_n + E_{Gp} - \delta_n - \delta_p] \quad , \qquad (2.10)$$

which with the values given above yields:

$$V_{bi} = 4.3 - 4.5 + 1 - 0.2 - 0.1 = 0.5 \ volt \quad .$$

It is noted that V_{bi} is increased if δ_n and χ_n are reduced. The difference in the levels of the conduction bands (Figure 2.4 (b)) is seen to be:

$$V_{CB} = \frac{1}{q}(E_{Gp} - \delta_n - \delta_p) = 1 - 0.2 - 0.1 = 0.7 \ volt \quad .$$

Hence $V_{CB} - V_{bi} = \Delta E_c/q = 0.2$ volt, so there is no "spike" in the transition of the conduction band from one semiconductor to the other. There is also no spike in the valence band offset ΔE_v, since the difference in the valence band levels is

$$V_{VB} = \frac{1}{q}(E_{Gn} - \delta_n - \delta_p) = 2.4 - 0.2 - 0.1 = 2.1 \ volt \quad ,$$

so that

$$V_{VB} - V_{bi} = \Delta E_v = 2.1 - 0.5 = 1.6 \ volt \quad .$$

(b) $CuInSe_2$-CdO Junction

Values of χ_n and δ_n for CdO have not been found in the literature by the author but maybe similar to those of CdS. Since the energy gap of CdO [1.8] is similar to that of CdS, it is possible therefore that the values of V_{bi}, V_{CB}, ΔE_c, and ΔE_v are also similar.

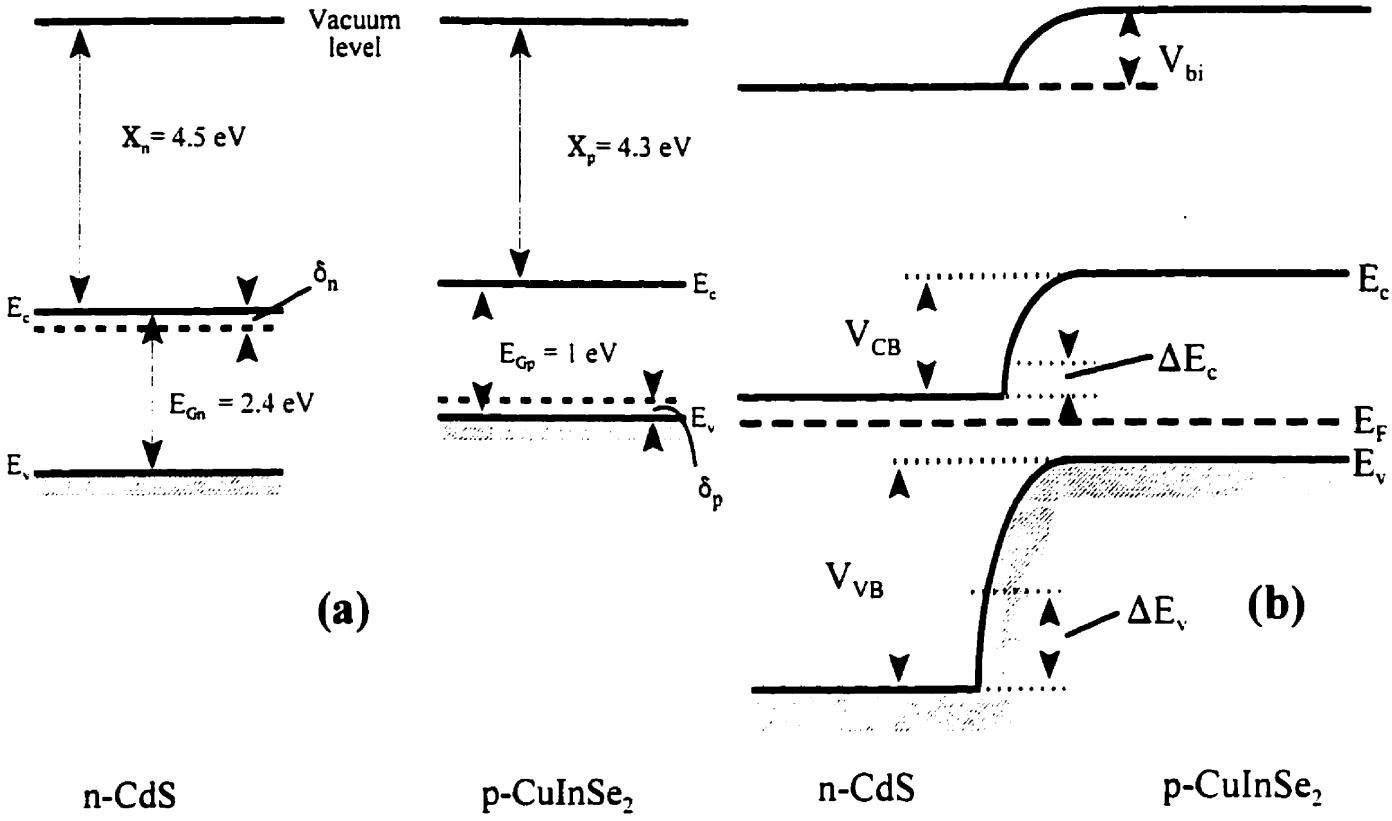


Figure 2.4 Equilibrium energy band diagram of a $CuInSe_2$/CdS heterojunction with (a) the $CuInSe_2$ and the CdS separated and (b) the $CuInSe_2$ and the CdS brought together.

CHAPTER 3

Fabrication of Monocrystalline Photovoltaic Cells

3.1 INTRODUCTION

As indicated in chapter 1, the studies in this work were on photovoltaic cells using p-type Bridgman-grown $CuInSe_2$ substrates with a CdO window layer which was deposited by dc reactive sputtering. Two kinds of cell were fabricated, one with the structure $CuInSe_2$-CdO and the other with the structure $CuInSe_2$-CdS-CdO. In the latter case, the CdS interlayer was deposited by a dipping method. In all, some 12 cells were fabricated but the results on only 9 of these are reported in this thesis, as indicated in Table I. The details of fabrication are now specifically described in this chapter. A single ingot of p-type monocrystalline $CuInSe_2$ was grown by the author with stoichiometric starting proportions of the high purity elements copper, indium and selenium. All the photovoltaic cells reported in this thesis were made using substrates from this ingot. However, since the Bridgman growth was not the main focus of this study, its description is displaced to Appendix I.

3.2 CELLS FABRICATED

As mentioned above, a total of 12 cells were fabricated, three of which were found

to have short circuits and thus were not further investigated. The characteristics of the remaining 9 photovoltaic cells are given in Table I. Of these, 3 had the basic layer structure $CuInSe_2$-CdO, namely cells AB-2, 5 and 12, while 6 cells had the structure $CuInSe_2$-CdS-CdO, namely cells AB-1, 4, 6, 7, 8, and 10. The devices, without the CdS interlayer had substrates cleaved in either the {101} or {112} plane, as indicated in column 2 of Table I. By contrast, the 6 devices with the CdS interlayer present, had substrates which were abrasively polished without any specific crystallographic orientation. The CdO window layer thicknesses are given in column 3 and ranged from about 0.6 to 0.8 μm, while the active areas are given in column 4 and ranged from about 3 to 10 mm^2. Details of the fabrication steps to make these cells are now given.

3.3 SUBSTRATE TREATMENT

(a) Surface Preparation

In each case, the substrate was cut or cleaved from the Bridgman-grown $CuInSe_2$ ingot. The cleaving was carried out by applying gentle pressure at room temperature on opposite ends of the grown ingot, without a particular orientation, using a sharp cutting blade. This process of cleaving, while somewhat primitive, yielded cleavage planes ranging from 5 to 100 mm^2 in area. The principal cleavage planes were identified under a stereo-zoom microscope. The {101} plane, exhibits some terracing and is less planar than the {112} surface. These observations and cleavage features are discussed in detail by Shukri and Champness [3.1]. The non-cleaved material from the shattered ingot was used for the fabrication of the polished devices.

An important first step in the fabrication procedure was the verification of the conductivity type. The conductivity type of the cleaved (or cut) substrate was determined using the well-known hot point probe method, as depicted in Figure 3.1. Then, using abrasive polishing in order to obtain a flat surface suitable for device fabrication, the substrate, with an original thickness of 4 to 5 mm, was thinned down to about 1 to 2 mm. In the case of the cleaved substrate(s), this grinding process was done on the non-cleaved face, while the top cleaved surface was protected by a layer of Apeizon wax. The polishing was performed on a rotating mechnical wheel with kerosene-lubricated coarse sand paper (silicon carbide 400A). One surface was then polished with 1 μm powdered alumina for approximately 20 minutes using water as the lubricant on a rotating wheel covered with felt cloth. Next, this surface was lapped for another 20-25 minutes with 0.3 μm alumina powder and finally finer polishing (0.05 μm alumina) was done for an additional 20-25 minutes. The resulting surface was highly specular and scratches could only be observed under the microscope. Once the polishing was completed, the cell was immersed in trichloroethylene and placed in an ultrasonic bath for approximately 5 minutes to remove any residual granular alumina from the lapped surface. The sample was then immersed in acetone for another 5 minutes to dissolve away any remaining tricholoroethylene. Finally, the sample was rinsed with deionized (DI) water.

(b) Surface Etching

It was reported by Galaly [3.2] that ohmic contacts to $CuInSe_2$ could be obtained by evaporation of gold after application of a strong etch, such as aqua regia. Aqua regia

(3 HCl: 1 HNO_3) was used to etch the back surface of the $CuInSe_2$ in order to obtain an ohmic contact, as shown in Figure 3.2. It was also found in this work that the use of aqua regia causes the subsequent gold metal (section (d)) to adhere very well to the $CuInSe_2$.The Wood's alloy, used for soldering to the back contact was found to wet the back surface and did not peel off the gold layer as it solidified. In runs where the back surface was not etched (earlier work, not discussed in this thesis), the soldering to the gold back surface was not always successful. In many cases the gold peeled off after the Wood's alloy solidified or was poorly adherent, so that high series resistance on these cells was often observed. The aqua regia was maintained at a temperature of approximately 60 °C and the etching was done with the top surface (fine polished) protected with Apeizon wax. The back surface was etched for approximately 1 minute, as prolonged etching caused the formation of etch pits. The aqua regia did not change color and remained reddish orange throughout the reaction. The reaction was arrested by flooding the sample with DI water.

(c) Substrate Annealing

Arising from the work of L.S. Yip and I. Shih [1.19] of this laboratory, on $CuInSe_2$/CdS/ZnO cells, annealing the $CuInSe_2$ in argon prior to cell fabrication was carried out, since this was crucial to obtain cells with higher overall performance. It is believed that the annealing tends to heal the mechanical damage that is caused by the abrasive lapping (polishing) of the substrate surface as well as having other actions. The substrate annealing was carried out for all the cells (cleaved and non-cleaved) in this work and annealing was done in a furnace, shown schematically in Figure 3.3 containing an open-ended quartz tube

some 30 cm in length, one end of which was connected to an argon gas cylinder. The substrate was inserted in the other end of the tube, followed by a thermometer, which was placed close to the sample to get a good estimate of its temperature. The quartz tube, along with the sample and thermometer, were placed inside a metal block having a cylindrical hole with the same diameter as the quartz tube to provide thermal stability. The gas flow rate was set at about 150-200 ml/min and the temperature was slowly ramped up to 320-360 °C. With the temperature stabilized and a steady flow of argon, annealing was proceeded with for 2 to 3 hours. Annealing for longer periods was found by L.S. Yip and I. Shih [1.19] not to be particularly beneficial. Once completed, the furnace was turned off and the sample was allowed to cool down under the flow of argon. Once room temperature was reached, the sample was removed from the tube.

(d) Back Contact Deposition (Au Deposition)

The metal deposited as a back contact for this work was gold. The deposition was carried out by evaporation in an Edwards model E306A high vacuum system as depicted in Figure 3.4. The annealed and etched $CuInSe_2$ substrate was mounted with its top surface down on a glass slide, containing a patch of molten Apiezon wax. The wax provided support for the sample, thus holding it in place and also protected the top surface from any unwanted scratches and other damage. This method of mounting also provided a mask against any gold deposition onto the top surface, while keeping the back abrasively-polished and etched surface exposed. The glass slide supporting the sample was then mounted approximately 10 cm above the Mo (molybdenum) boat containing several pieces of thin gold metal wire. The

system was then allowed to pump down to a pressure of roughly $5x10^{-7}$ Torr (approx. 1 hour), when evaporation was commenced. The current through the Mo boat was slowly raised until the gold wire started to melt (at approximately the 80 Amp setting). The current was maintained at that level for 2 to 3 minutes, thus allowing all the gold wire to evaporate at a rate of about 20 Å/second. This gave a film thickness of approximately 0.2 μm on the sample. The sample was then allowed to cool down for approximately 1 hour before its removal from the vacuum system. After removing the sample, it was first immersed in both trichloroethylene, in order to dissolve away the Apeizon wax, and then in acetone to dissolve away any remaining tricholoroethylene.

3.4 CdS INTERLAYER DEPOSITION

The solution growth of CdS [3.3] was carried out using the following laboratory prepared stock solutions: 0.01M $(NH_2)_2CS$ (thiourea), 0.1M $(NH_4)Cl$ (ammonium chloride), 0.01M $CdCl_2$ (cadmium chloride) , 0.01M NH_4 OH (ammonium hydroxide). The correct proportions of the salts were weighed out using a balance. Each weighed salt was dissolved in DI water to give an aqueous solution and was stored in a glass bottle. The ammonium chloride was used as a buffer solution, the thiourea was employed as a source of sulphur ions and the ammonium hydroxide was the complexing agent. The experimental setup for the solution growth of the CdS layer is shown in Figure 3.5. About 300 ml of experimental solution was prepared by adding equal amounts of preheated stock solutions of cadmium chloride and ammonium chloride in continuously stirred DI water at a temperature of

approximately 90°C. The pH of the solution was set at approximately 10-11 and was controlled with the ammonium hydroxide. The beaker containing the solution was covered with a plastic wrap in order to prevent the excessive loss of ammonia. Pre-heated thiourea (at approximately 90 °C) was then added to the solution, whose temperature was allowed to stablize to 90 °C for approximately 5 minutes before the substrate was immersed. The deposition was proceeded with for approximately 15 minutes. Stirring the solution during the deposition promoted heterogeneous growth on the substrates. This gave CdS layers typically violet or blue in color with thicknesses between 500 and 750 Å. The CdS generally adhered very well to abrasively polished $CuInSe_2$ substrate surfaces and the layers that were formed were usually uniform. This uniformity and adherence, however, was not particularly true in the case of cleaved $CuInSe_2$, where the CdS layers were generally patchy. This is probably due to the fact that the cleaved $CuInSe_2$ surface was too smooth.

3.5 SAMPLE MOUNTING AND MASKING

Once the sample was withdrawn from the CdS solution, it was rinsed in DI water and then the unnecessary CdS was etched away using HCl. Before mounting the sample on an aluminum stud, a thin gold wire was soldered to its back using Wood's alloy. The sample was then mounted on the aluminum stud using Quickmount™ epoxy. After this stage, the sample, mounted on the stud, was placed inside a holder with a metal shadow mask defining the CdO area, as shown in Figure 3.6 (a). This entire unit was then positioned within a vacuum chamber.

3.6 CdO LAYER DEPOSITION

(a) Sputtering Process

The window layer used in the cells of this work was CdO. A solid cadmium target, obtained form Kurt J. Lesker Company of Clairton, Pennsylvania using high purity 99.999% (or 5-9's) cadmium, was used as the cadmium source. It consisted of a disc 7.6 cm in diameter and some 0.6 cm in thickness. This disc was placed in a cylindrical aluminum block 10.2 cm in diameter and 4 cm thick. The cadmium target was always kept 1 mm above the aluminum surface in order to minimize unwanted aluminum sputtering. The CdO layer was deposited directly onto the CdS coated surface (or directly on $CuInSe_2$ for $CuInSe_2$ -CdO cells). The masked sample was loaded (along with a glass slide to monitor the CdO thickness) into a special vacuum system and placed some 3-4 cm above the high purity cadmium metal target. The target was negatively biased, with respect to the sample, which was maintained at zero bias (grounded). Figure 3.7 shows a schematic of the set up for the CdO deposition. The vacuum system was then pumped down to approximately 10^{-6} Torr, after which the pressure was raised up to roughly 75 mTorr by admitting a gas mixture consisting of 99% argon and 1% oxygen. The total flow rate of this gas was maintained at approximately 25 ml/min. The system pressure was then allowed to stabilize and the deposition process was begun with the sputtering current adjusted to about 15-20 mA. The negative potential of the cadmium target was approximately 700 volts, depending on the pressure. The deposition was performed in a continuous manner for a period of between 2 - 3 ½ hours until the desired thickness of CdO was achieved. The sample was allowed to cool down for approximately 1 hour. The holder was then unloaded from the vacuum system, with

the sample kept in place. Finally, the CdO mask was replaced with another mask (Figure 3.6 (b)) for the front metal contacts.

(b) CdO Film Thickness and Resistivity Measurements

The thickness of the CdO film on each cell was estimated by counting the order of interference fringes at the edge of the deposited area and noting its central color under a microscope. This was verified from the corresponding fringes on a glass slide (inserted along with sample in the sputtering system). The thickness was then calculated using the following relationship:

$$2nd = (N - ½)\lambda \ .$$

where n is the refractive index for CdO (n = 2.5), d is the thickness of the CdO film, N is the diffraction order of the central color and λ is its corresponding wavelength.

The resistivity of the CdO film was estimated using the four point probe method on different regions of the film on the glass slide to ensure a constant film resistivity. The conductivity type of the CdO film on the glass slide was also verified to be n-type using the hot-point probe.

3.7 CONTACT STRIPES

(a) Deposition of indium

Conducting stripes are needed on the CdO film to make electrical contacts on the

illuminated side of the photovoltaic solar cell. These must be sufficiently large to minimize series resistance but not so large that they obscure the illuminated area. After the CdO layer was sputtered onto the substrate, two indium contacts were evaporated onto the CdO. This was done in the following way. In this process, the sample holder was removed from the vacuum system and the mask was changed to a new mask containing pairs of thin rectangular openings, as shown in Figure 3.6 (b). In this mask these stripe-openings correspond in position to the mask defining the CdO area (Figure 3.6 (a)). The sample holder was then mounted inside a vacuum coater (Cooke Vacuum Products CV301FR) above a molybdenum boat containing two pellets of indium. A metal shutter was rotated to a position between the boat and the sample, and the system was allowed to pump down to a pressure in the range of 10^{-5} Torr for approximately 1 hour. Next, current was passed through the molybdenum boat and increased slowly to 40 amps. After about 30 seconds with this current maintained, the shutter was opened to allow the start of the indium deposition, which was continued for another 2-3 minutes at a rate of approximately 25 Å/second. Following this, the current was turned down to zero and the sample was allowed to cool in the system for 1 hour to avoid air-oxidation of the indium surface as well as the molybdenum boat.

(b) Attachment of Leads

The cell (mounted on the aluminum stud), now complete with indium contact stripes, was next inserted into a circular Teflon plate containing brass screws to act as terminals, as shown schematically in Figure 3.8. These screws were longer than the thickness of the Teflon plate so that the connection to the measuring instruments could be made on the other end of

the screws. Fine copper wires were soldered to the indium stripes on the CdO area with Wood's alloy (50% Bi, 25% Pb, 12.5% Sn and 12.5 Cd, m.p. approx. 71 °C) as the solder material, using a small low-heated soldering iron. The other end of these fine copper wires was soldered to each of the brass screw heads using normal electronic solder and a regularly heated soldering iron. The technique of the Wood's metal soldering to the stripes required some extra skill and patience, otherwise the cell would be damaged by the heat or even scratched by the tip of the soldering iron. For this reason, this step was performed under a microscope or magnifying glass in all cases.

Table I
$CuInSe_2$-CdO and $CuInSe_2$-CdS-CdO Cells Fabricated

Cell Number	Cleavage[1] plane	CdO Layer[2]		Dark Characteristics		Illuminated Characteristics[5] (Simulator)				Electron[6] Diffusion Length
		thickness[3] (μm)	area[4] (mm^2)	R_s (Ω-cm^2)	Ideality factor n	j_{sc} (mA/cm^2)	V_{oc} (volt)	F.F.	η (%)	(μm)
$CuInSe_2$-CdO Cells										
AB-2	{101}	0.55	9.0	7.2	N/A	17	0.36	0.30	2.1	-
AB-5	{101}	0.66	8.1	4.8	2.8	29	0.42	0.45	5.0	-
AB-12	{112}	0.78	3.4	1.2	2.4	30	0.41	0.55	6.8	3.0
$CuInSe_2$-CdS-CdO Cells										
AB-1	-	0.55	9.5	3.7	N/A	6.6	0.25	0.33	0.5	-
AB-4	-	0.66	6.0	1.0	2.2	26	0.34	0.52	4.6	-
AB-6	-	0.66	5.0	4.0	1.7	24	0.40	0.54	5.3	1.0
AB-7	-	0.78	6.0	2.1	2.2	34	0.40	0.50	6.5	-
AB-8	-	0.78	6.2	1.5	1.7	30	0.38	0.42	5.0	1.9
AB-10	-	0.78	4.0	0.9	1.8	33	0.38	0.56	6.9	1.2

1. Cells with CdS interlayer were abrasively polished and not cleaved.
2. Sputtering conditions Cd target, gas (1% Ar 99% O_2) flow rate 12.5 ml/min, 750V, 20 mA, 70-75 millitorr.
3. Thickness from interference color and order.
4. Active area of CdO.
5. Irradiance of 100 mW/cm^2 from Xe arc lamp simulator.
6. Obtained from photocurrent-capacitance method.

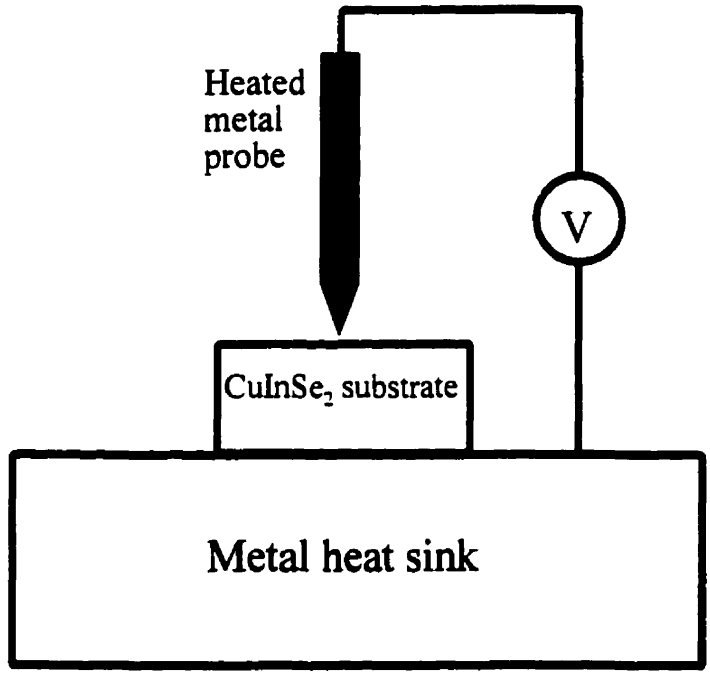


Figure 3.1 Schematic diagram showing the setup used for the conductivity type determination using the hot point probe.

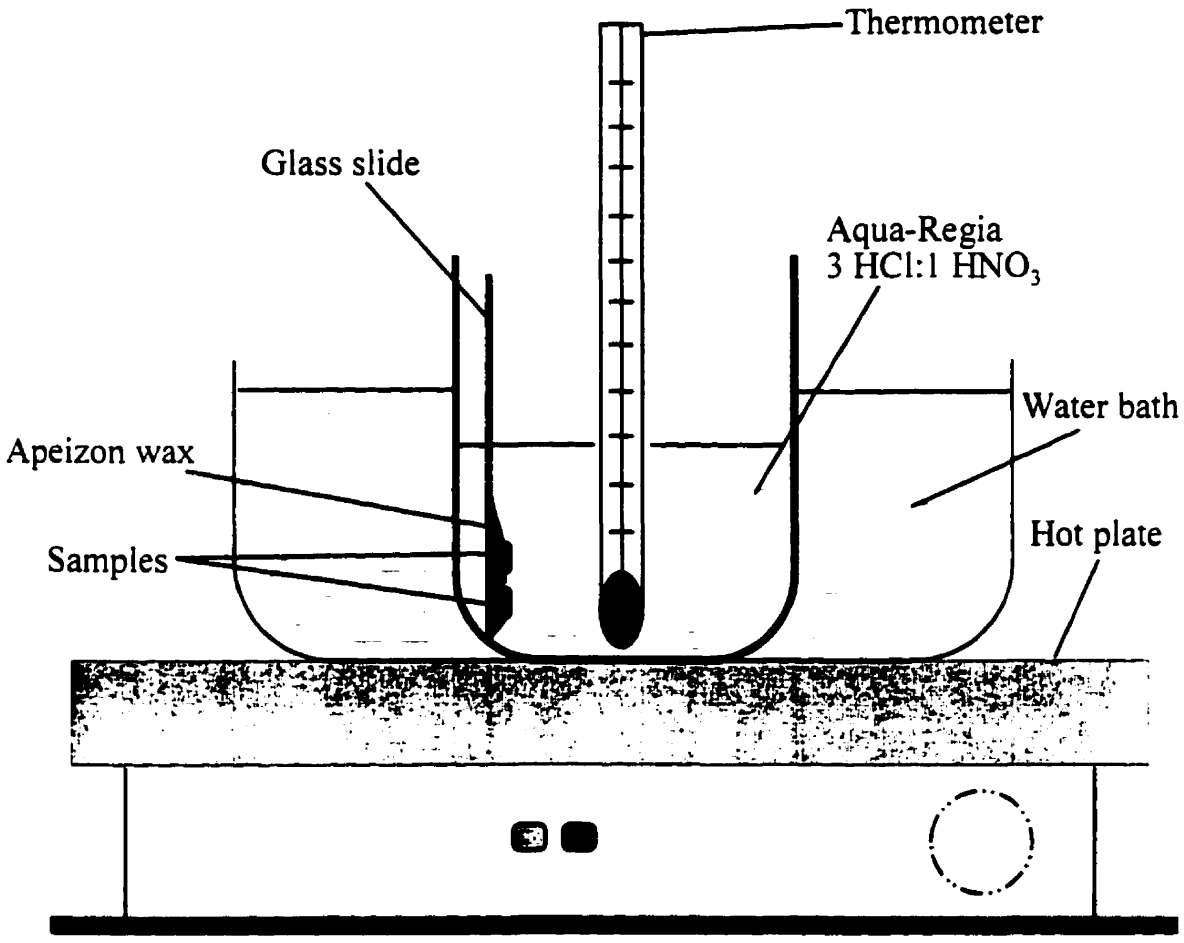


Figure 3.2 Schematic diagram showing the setup used for etching the back surface of the $CuInSe_2$ substrates.

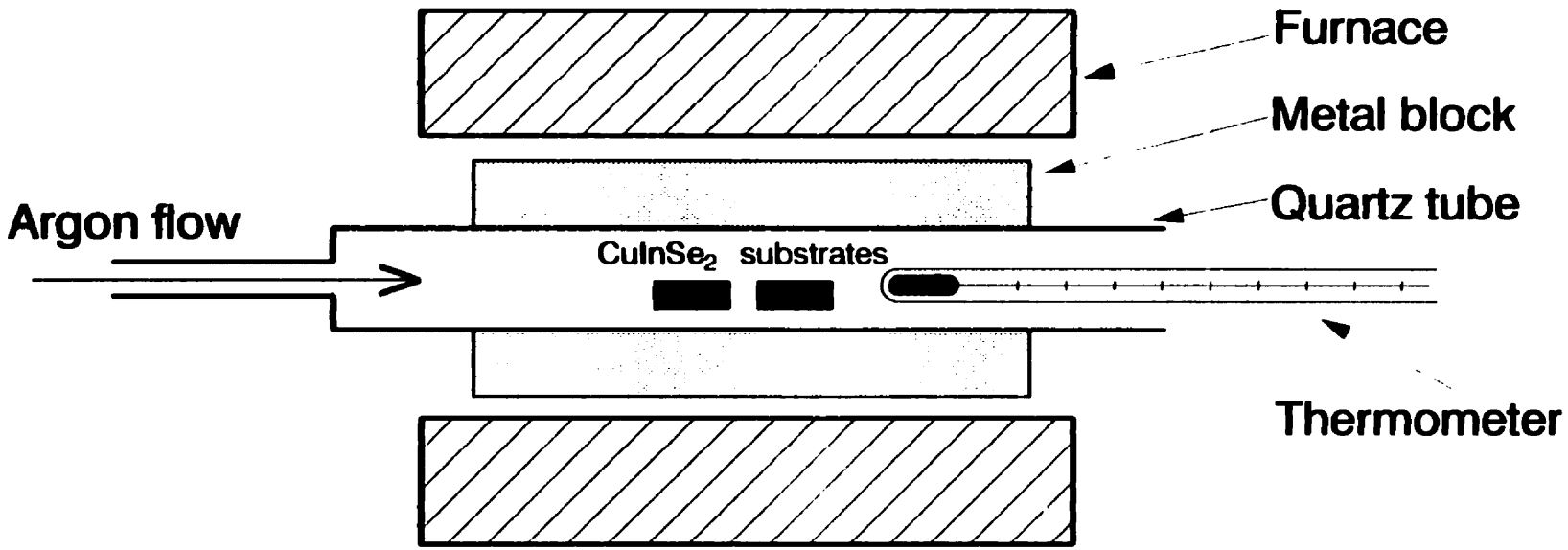


Figure 3.3 Schematic of furnace used to anneal the $CuInSe_2$ substrates in argon.

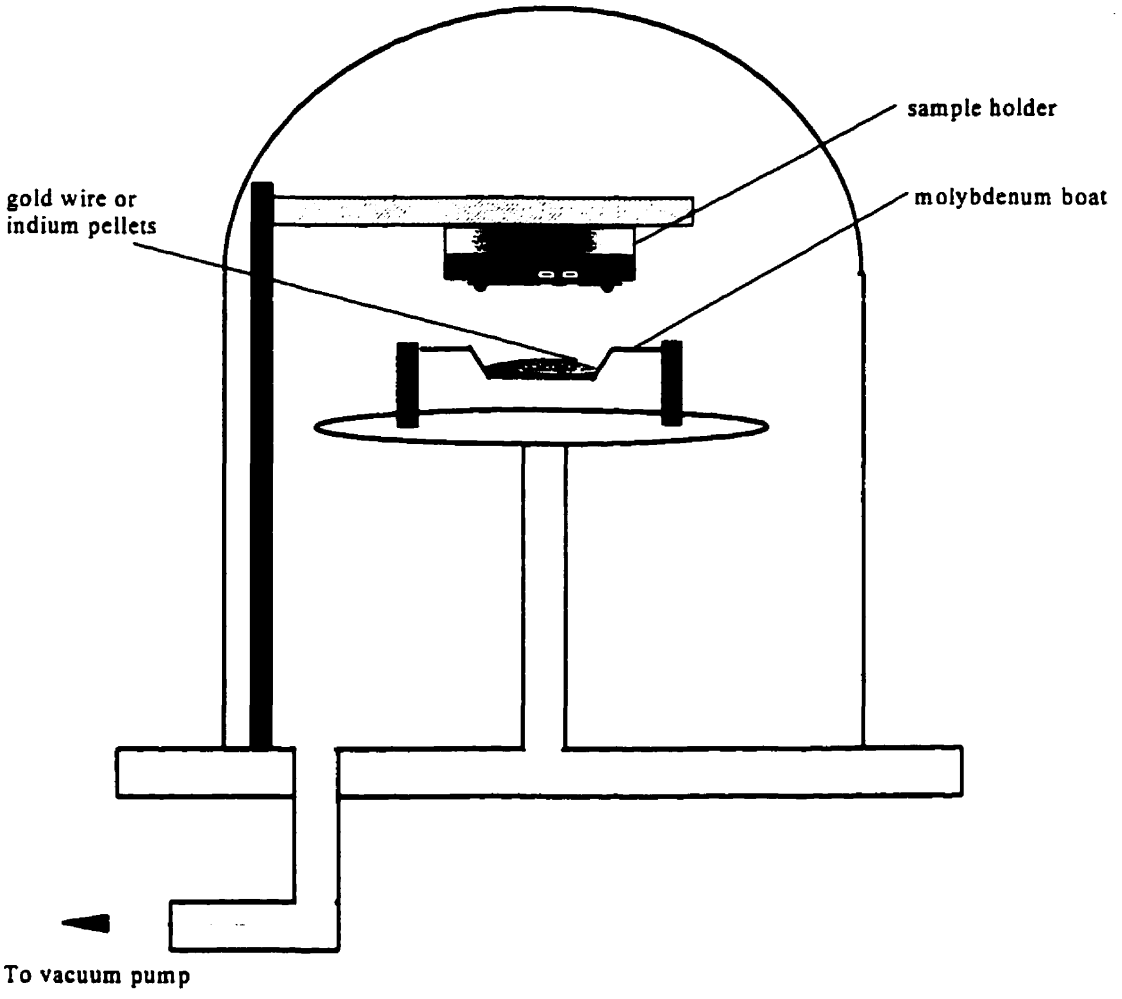


Figure 3.4 Schematic diagram of the vacuum system used for the deposition of the gold / indium contacts by thermal evaporation.

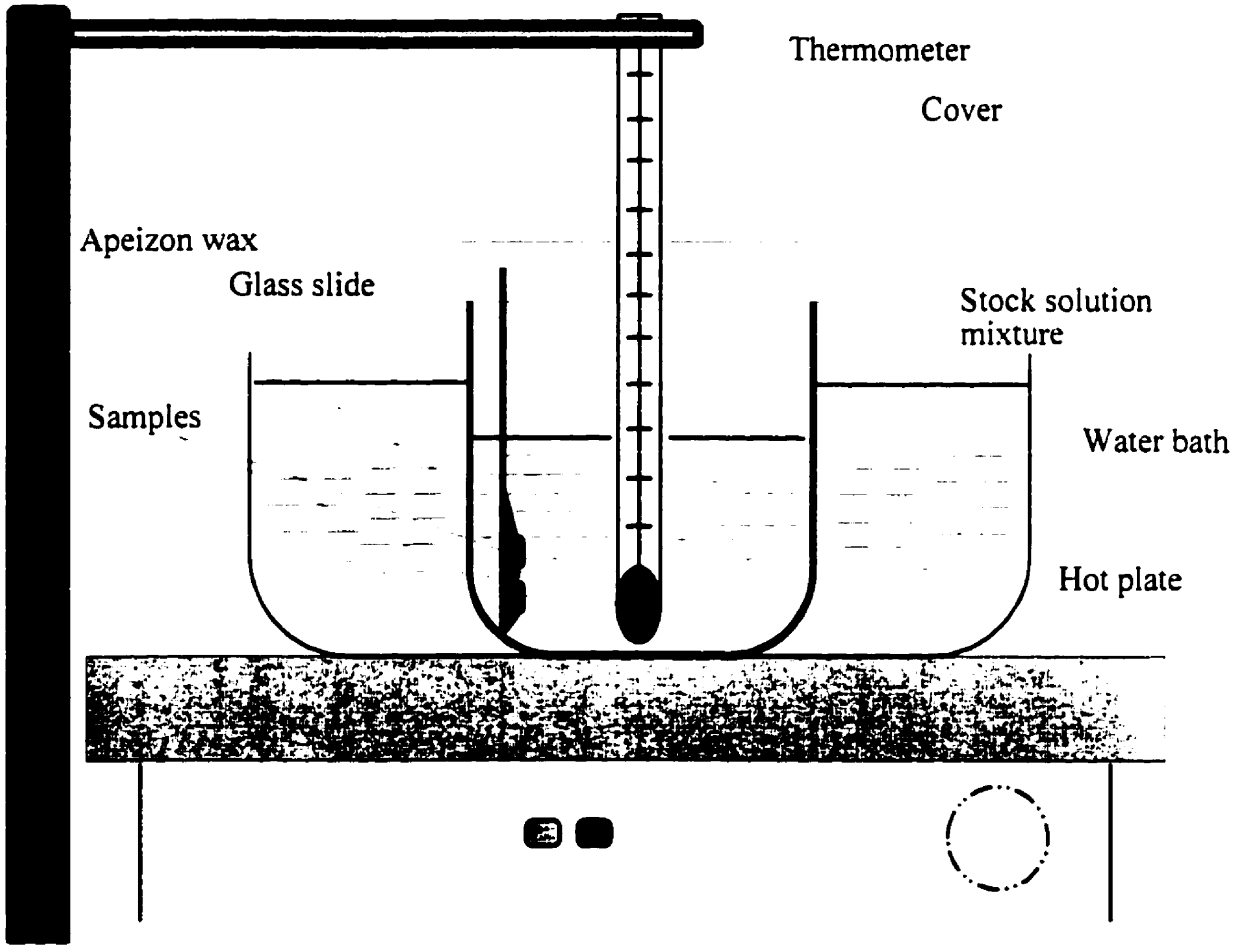
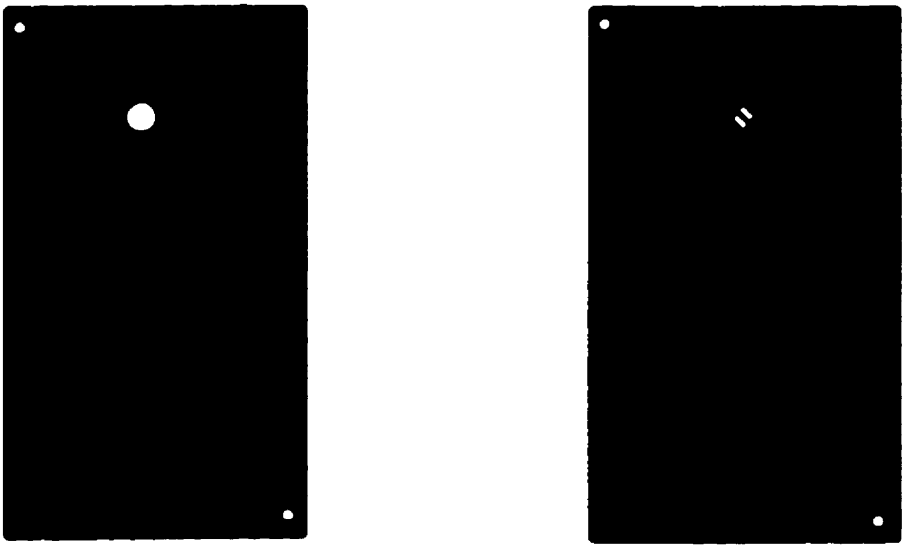


Figure 3.5 Schematic diagram of the setup used for the CdS thin film deposition by the dipping/solution growth method.



(a) (b)

Figure 3.6 Schematic diagram of the metal shadow masks used for (a) the CdO thin film deposition and (b) the indium contact stripes deposition (not to scale).

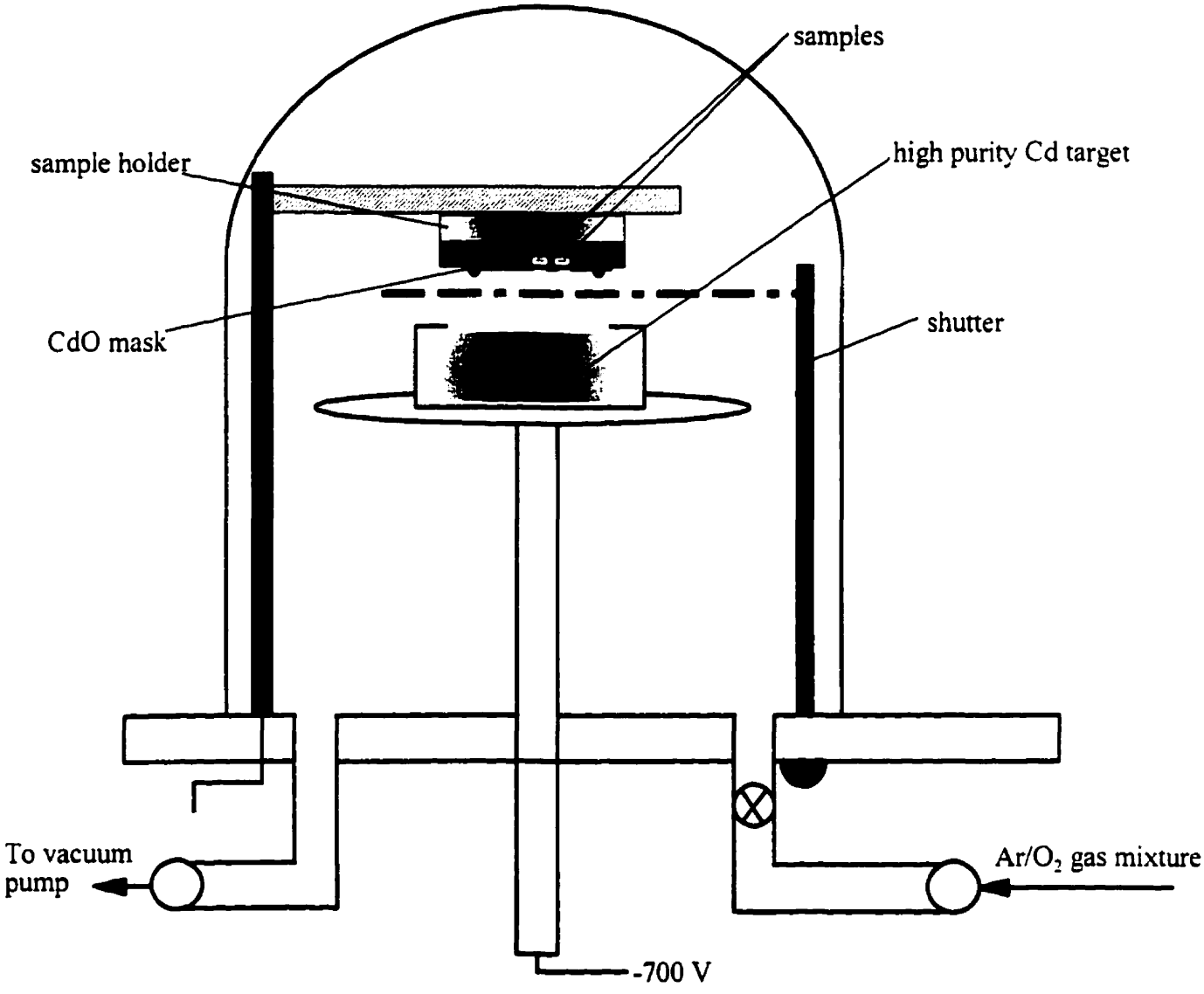


Figure 3.7 Schematic diagram of the vacuum system used for the deposition of CdO thin films by dc reactive sputtering.

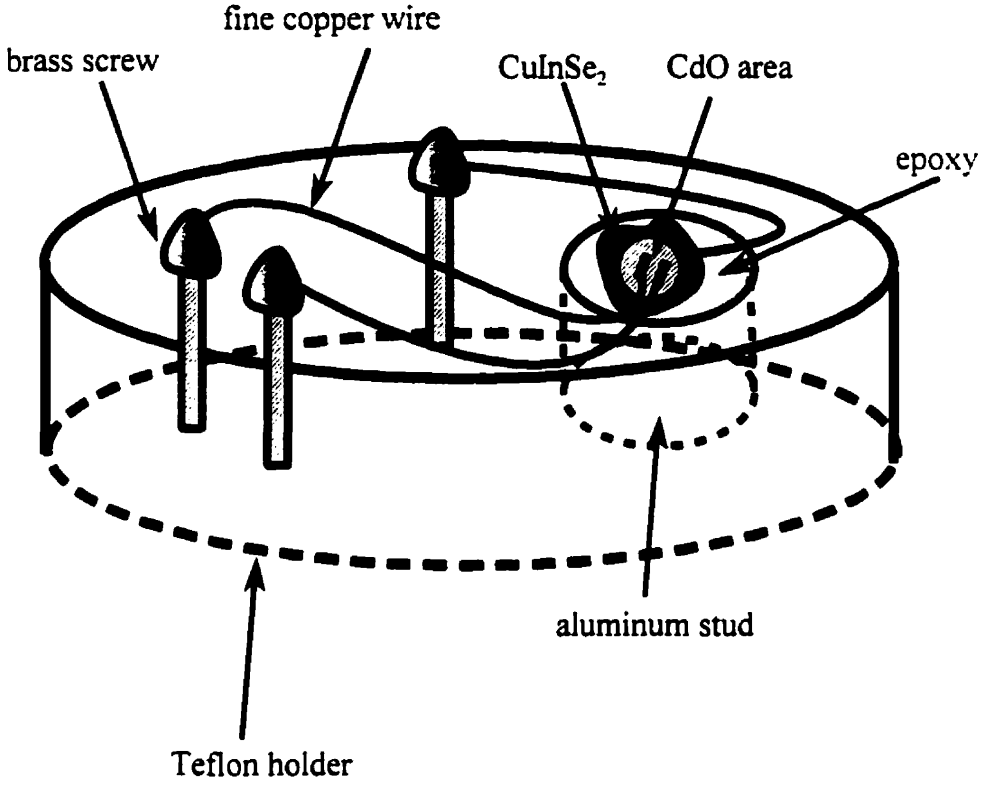


Figure 3.8 Schematic diagram of the mounting of the fabricated device in a Teflon holder.

CHAPTER 4

Measurement Techniques

4.1 INTRODUCTION

Following the fabrication of each of the cells, various measurements were made on them to assess photovoltaic performance and other characteristics. Each cell was characterized based on illuminated and dark current density-voltage (j-V) measurements under simulated sunlight, capacitance-voltage characteristics, photoresponse, estimation of minority carrier diffusion length and finally, in most cases, current density-voltage measurements under actual sunlight.

4.2 CURRENT-VOLTAGE MEASUREMENTS

(a) Illuminated Current Density-Voltage Characteristics under Solar Simulator

Measurements of illuminated and dark current density-voltage (j-V) characteristics reveal important solar cell parameters. The illuminated j-V measurements were obtained under a solar simulator using a xenon arc lamp (characteristics given in Appendix III) fitted with an AM1 filter, calibrated to give an irradiation of approximately 100 mW/cm^2. The calibration was done using a Solarex silicon reference cell having a reduced area of 0.125 cm^2. The calibration procedure was as follows. The reference cell, which was connected to a Fluke multimeter model 37, was placed under the beam of light centered over the active area. Its vertical position was adjusted such that the reading it gave on the Fluke meter was

3.1 mV, corresponding to an incident radiant power density of 100 mW/cm^2, which in turn corresponds to AM1.5G. The vertical position of the reference cell was then recorded and replaced with the actual test device whose specific location was adjusted to be the same as that of the reference cell. The circuit arrangement used for these illuminated current-voltage (I-V) measurements is shown in Figure. 4.1. The bias voltage was swept (using a power supply and a poteniometer) from 1.2 volts in the reverse to approximately 0.8 volts in the forward direction in increments of 0.05 volt.

(b) Dark Current Density-Voltage Characteristics

Dark I-V characteristics were obtained in much the same manner, as described in section (a) above except that the incident beam of light was blocked from impinging upon the cell. In this case, the cell was covered with a black cloth to ensure complete darkness. In this measurement, it was important to obtain readings at small currents because of the logarithmic plots made of this quantity shown in chapter 5. For this reason, a Keithley picoammeter (Model 485) replaced the Fluke multimeter (ammeter A) shown in Figure 4.1 for very small currents. The voltage across the cell was measured with a high impedance Keithley 610C electrometer. To obtain the current density, j, each of the current (I) readings was divided by the "active" area of the CdO layer, which was determined by measuring the total area A directly under a stereo-zoom microscope having a built-in scale.

(c) Illuminated I-V Characteristics under Actual Sunlight

In order to gain some confidence in the measurements done using the solar simulator,

illuminated characteristics of some cells were repeated under actual sunlight. The measurement circuit used in this case was slightly different from that used with the solar simulator and is shown in Figure 4.2. The difference was that no external bias was applied to the cell and the I-V characteristics were obtained by connecting a variable load resistor R_L, as well as a fixed series sensing resistor (R_{sen}) across the cell. The load resistor was varied in order to get as many points as possible between the "short circuit" (R_L=20 Ω) and "open circuit" (R_L=25 kΩ) conditions. The voltage across the sensing resistor (chosen to be 10 Ω) was measured using a Fluke multimeter (model 37) and the value was divided by the sensing resistance to get the current through the cell. The measurements were carried out on the roof of the McConnell Engineering Building at McGill University between about 11:30am and 12:30pm on selected sunny days between mid-April and early October, 1997. The intensity of the solar irradiation in this location was measured using three different devices namely: a pyroelectric detector (Molectron model PR 200), a pyranometer (Eppley model PSP) and finally a calibrated Solarex silicon cell. The readings taken from the three instruments were averaged to give the mean solar irradiation.

4.3 CAPACITANCE-VOLTAGE MEASUREMENTS

The parallel mode capacitance, C_p, was measured on the cells with the bias voltage swept from 2 volts in the reverse direction to 1 volt in the forward direction in increments of 0.05 volt. This measurement was done using a Hewlet Packard model 4192 LF Impedance Analyzer as well as a GenRad Digibridge (Model 1689) at three different frequencies 1, 10 and 100 kHz with a test signal of approximately 20 mV. The voltage across the sample was

verified for every bias point using a Keithley electrometer model 610C. However, the electrometer was disconnected prior to recording the value of the capacitance in order to ensure that the capacitance recording was that of the photovoltaic cell. Figure 4.3 shows the experimental circuit used for measuring the capacitance of the photovoltaic cells. The capacitance-voltage measurement provided data for two characteristics. Firstly, it gave the actual capacitance voltage characteristics of the cell and secondly, it provided Mott-Schottky plots. The Mott-Schottky plot is a plot of $(A/C_p)^2$ versus bias, where A is the cell total area. Such plots are important in that they can give an estimate of the acceptor concentration profile on the p-side of the cell (the $CuInSe_2$) and also the junction built-in potential. For a pn^- junction (ie. a "one sided" junction), the acceptor concentration N_A on the p-side is given by:

$$N_A = \left(\frac{2}{q\epsilon_o\epsilon_r}\right) \times \left(\frac{1}{\frac{d[(A/C_p)^2]}{dV_R}}\right) \quad ,$$

where ϵ_o is the permittivity of free space (vacuum), ϵ_r is the relative dielectric constant of the p-side ($CuInSe_2$) and V_R is the reverse voltage. The majority carrier concentration can therefore be estimated by determining the slope of the $(A/C_p)^2$ curve.

4.4 SPECTRAL RESPONSE MEASUREMENTS

The spectral response of the cells was carried out between a wavelength (λ) of 400 and 1300 nm. Each sample was illuminated using a monochromator from Photon Technology International model L1. The exit slit was set at 5 mm and the sample was positioned some

6 cm from the exit slit. The monochromator beam was chopped at a frequency of approximately 150 Hz using a Stanford Research Systems light chopper (model SR 540). The photogenerated current signal from the cell was converted into a voltage signal using a 10 Ω sensing resistor. This value was found to yield the short circuit current with small error, since tests with a lower value of sensing resistance (1Ω) indicated no significant change of current. The voltage across the resistor was measured using a lock-in amplifier (EG&G model 5302), with the reference frequency set by that of the light chopper. All measurements were taken at wavelength increments of 25 nm. In the range between 600 and 1075 nm, a long pass filter (610 nm cutoff) was placed in the path of the incident light beam to suppress any second and higher order harmonics arising from the monochromator diffration grating. For wavelengths of 1100, 1200, and 1300 nm, corresponding wavelength band pass filters (all with $\Delta\lambda \approx 50$ nm) were placed in the path of the incident light beam. Figure 4.4 shows a schematic diagram of the experimental setup used for the spectral response measurement. Once the measurements were completed on the sample under investigation, it was replaced with a pyroelectric radiometer (Molectron model PR 200) in order to measure the light intensity ($M(\lambda)$ in mW/cm^2) at each wavelength. The photoresponse of the cell ($P(\lambda)$ in amps/watt) was then calculated at each wavelength using the following relation:

$$P(\lambda) = I(\lambda)/(A_e \times M(\lambda)) \quad ,$$

where $I(\lambda)$ is the photogenerated current in mA, A_e is the effective CdO area (CdO area less the area of the contacts of the cell) and $M(\lambda)$ is the Molectron detector reading in mW/cm^2.

The quantum efficiency, $\eta(\lambda)$, for the sample was calculated at the respective wavelengths using the following relationship:

$$\eta(\lambda) = \frac{1}{q} P(\lambda) \times (\frac{hc}{\lambda}) ,$$

where h is Planck's constant and c is the speed of light.

For confirmation of the results in the wavelength range up to about 1 μm, the procedure was repeated using a calibrated silicon Schottky detector (from United Detector Technology) in the place of the Molectron detector.

In this work using the Photon Technology model L1 monochromator, a grating blazed at a wavelength of 1200 nm was employed. This has the transmission characteristics shown in Figure 4.5.

4.5 DIFFUSION LENGTH ESTIMATION MEASUREMENT

The method employed to estimate the diffusion length of the minority carriers in the monocrystalline $CuInSe_2$ was the photocurrent-capacitance technique. The theoretical considerations of this method are discussed in detail by Chan [4.1] and a brief treatment of the theory behind this method is contained in Appendix II.

The actual experimental procedure consisted of two steps. First, a measurement of the illuminated-to-dark change in the short circuit current (ΔI) of the cell at different reverse bias voltages and under long monochromatic wavelength illumination was carried out. This was followed by the measurement of the junction parallel capacitance, C_p, for the same reverse bias values and illumination. The measurement procedure itself was as follows. The

sample was placed about 6 cm from the exit slit of the monochromator, such that the entire sample was illuminated. The wavelengths used were 1.1, 1.2 and 1.3 μm with a fixed exit slit width, which was successively changed with the values 2, 4 and 5 mm. At these three wavelengths, corresponding bandpass filters (1.1, 1.2 and 1.3 μm), all having a $\Delta\lambda$ = 50 nm, were placed in the path of the incident light beam, which was chopped at a frequency of approximately 150 Hz using an SRS light chopper model SR 540. The cell was connected to a Farnell model TSV 30/5CL stablized power supply, biased in the reverse direction and the voltage across the cell was verified with a Keithley electrometer (model 610C). The cell was also connected in series with a sensing resistor of 10 Ω. The signal voltage across this resistor was measured using a lock-in amplifier (EG&G model 5302) from which the photocurrent change (ΔI) was obtained by dividing the signal voltage by the 10 Ω sensing resistance. The bias was varied between 0 and 5 volts in the reverse direction in increments of 0.2 volt.

The second phase of this experiment involved a measurement of the parallel mode capacitance versus reverse bias. The sample was kept in place but was connected directly to the inputs of a Digibridge or Hewlet Packard LF Impedance Analyser (model 4192A) and the incident light was unchopped. The voltage was again swept from 0 to 5 volts in the reverse direction in increments of 0.2 volt. The measurements were carried out at a frequency of 10 kHz and a test signal of 20 mV. This frequency of 10 kHz was chosen in order to avoid any anomalous capacitance contributions often observed at lower (typically below 10 kHz) and higher (100 kHz and above) frequencies. In order to gain confidence in the capacitance values, the readings from the Digibridge (GenRad Model 1689) and the HP 4192A

impedance analyser were averaged. Finally, the values of ΔI and C_p at each respective reverse bias value were used to plot ΔI vs. $1/C_p$. Figures 4.6 and 4.7 show the experiemtal setups for these measurements. A condition of using the photocurrent-capacitance method is that the αW product (α = absorption coefficient, W = depletion width) [4.2] [4.3] must be much smaller than unity, which in practice means using monochromatic light of bandgap edge wavelength. In the case of $CuInSe_2$, this would correspond to a wavelength of 1.2 to 1.3 μm (since the energy gap of $CuInSe_2$ is approximately 1 eV) . Therefore, if the wavelength is too short, the αW condition is violated, while if it is too long, the photocurrent is too small to measure accurately. Thus, although the ΔI measurements were made between 1.1 and 1.3 μm, only those values at longer wavelengths should be accepted, since they comply with the $\alpha W << 1$ inequality. Therefore, the most suitable ΔI values for estimating L_n selected were those obtained at a wavelength of 1.2 μm.

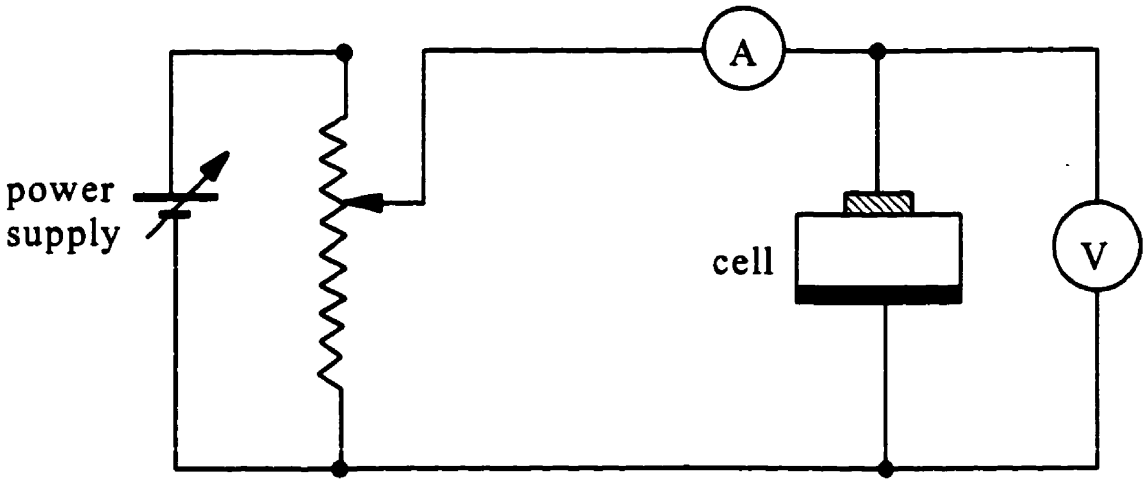


Figure 4.1 Electrical circuit diagram of the arrangement used for the indoor measurement of the current density-voltage (j-V) characteristics of the cells, under simulated light.

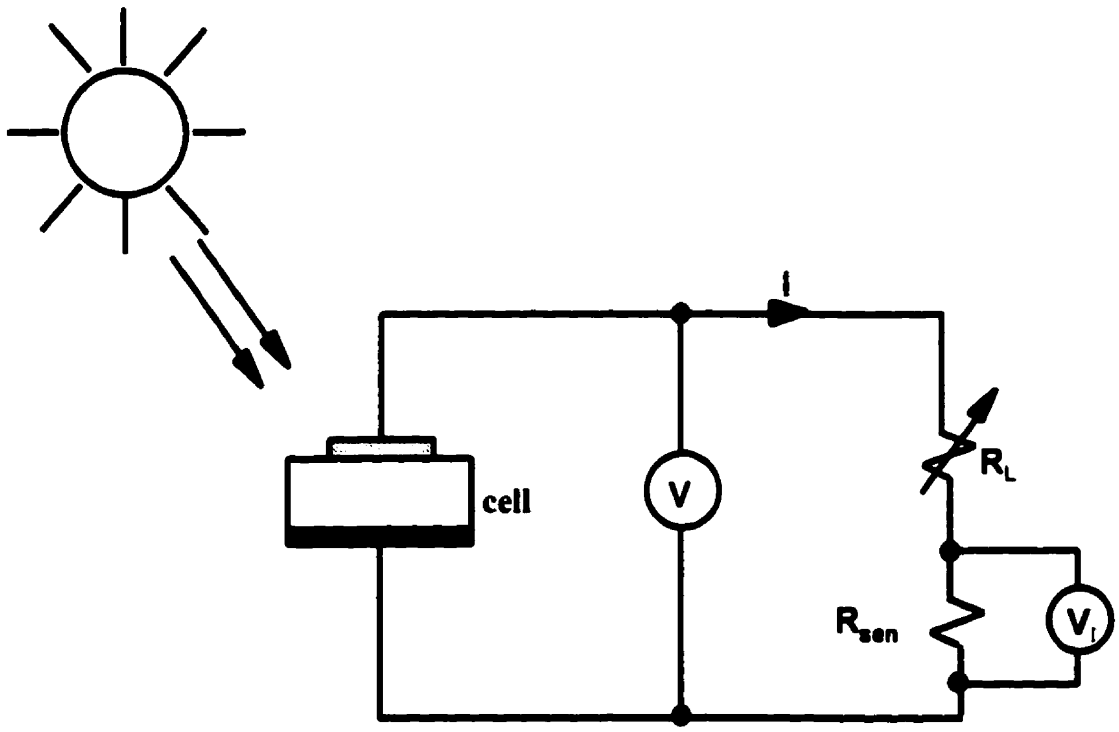


Figure 4.2 Electrical circuit diagram of the arrangement used for the outdoor measurement of the current density-voltage (j-V) characteristics of the cells, under actual sunlight.

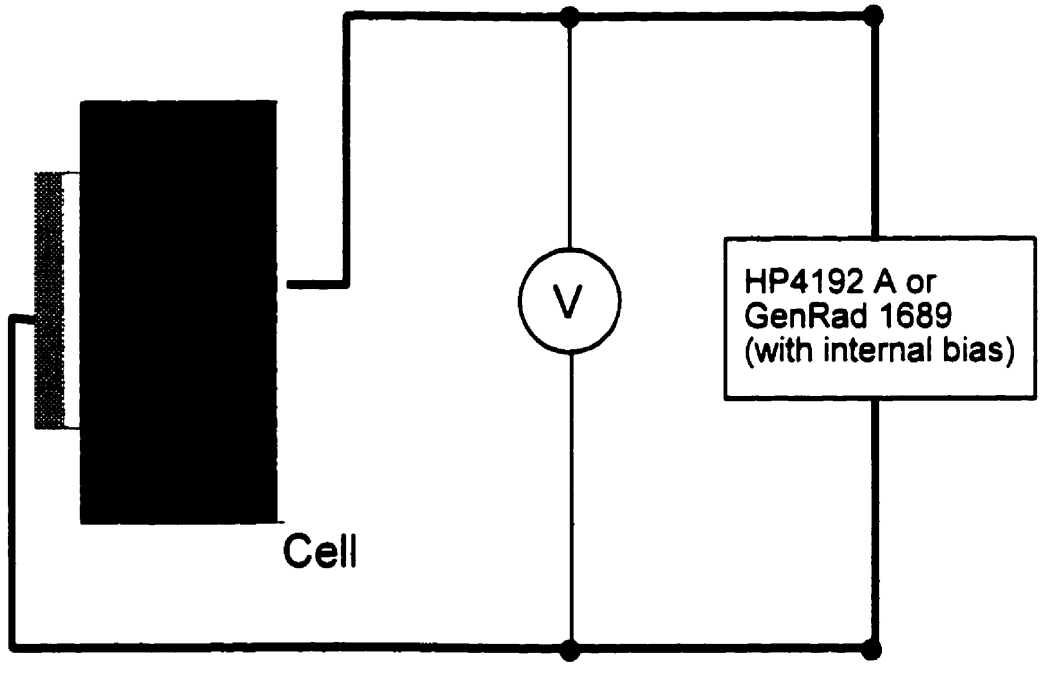


Figure 4.3 Electrical circuit diagram of the arrangement used for the capacitance-voltage measurements of the cells.

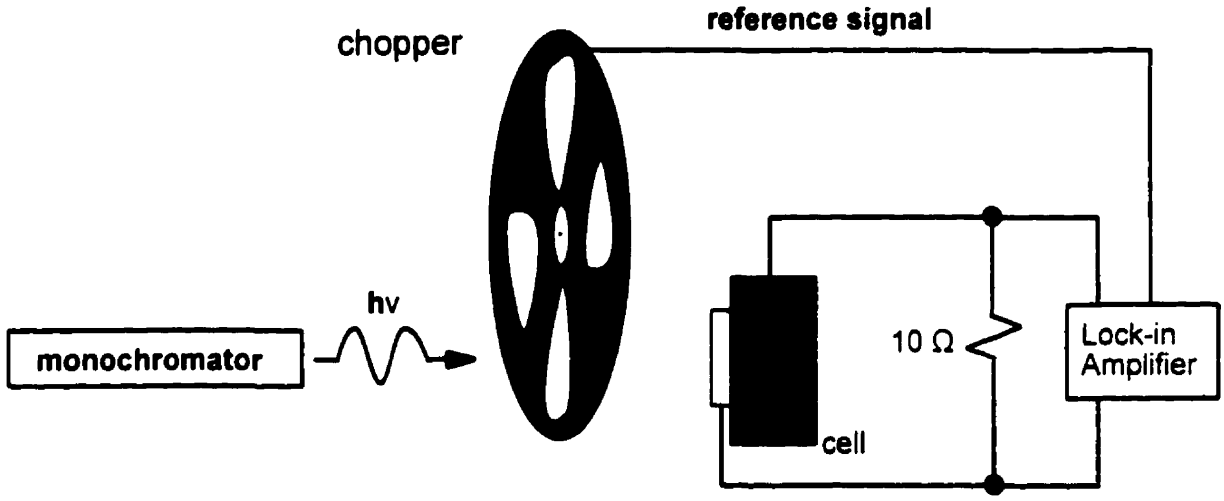


Figure 4.4 Schematic diagram of the experimental setup used for the spectral response measurement of the cells.

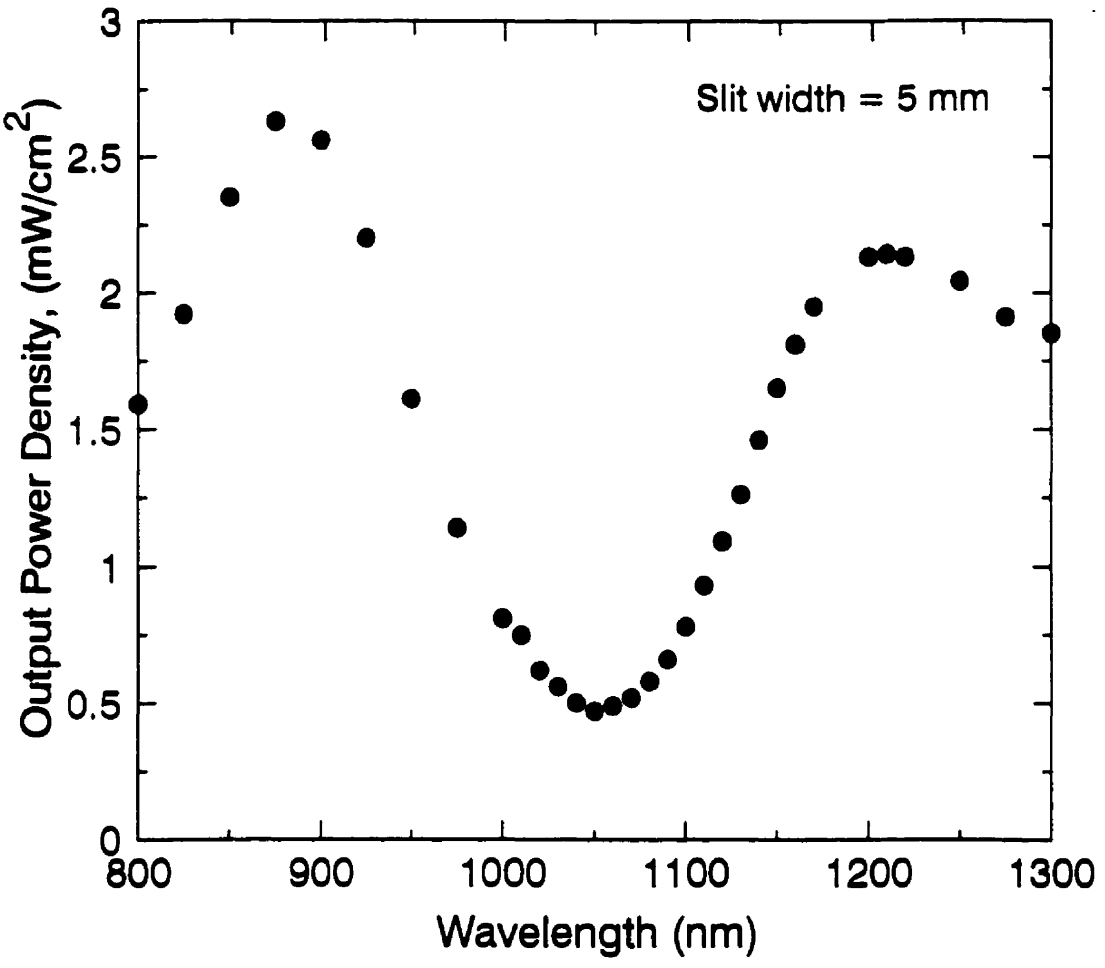


Figure 4.5 Plot of output power density measured from Photon Technology International model L1 monochromator, with a diffration grating blazed at 1200 nm.

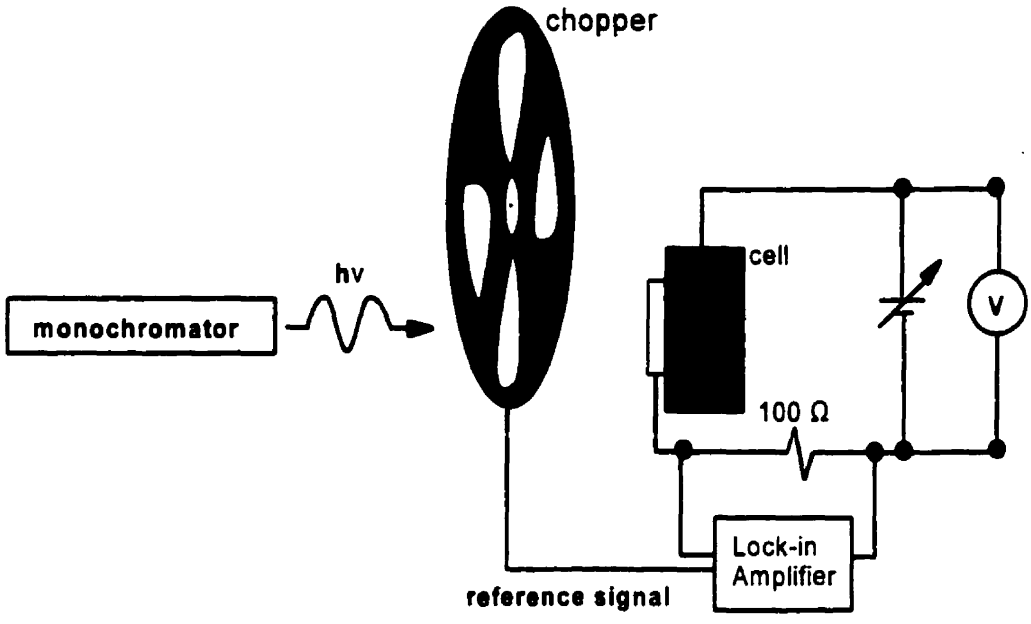


Figure 4.6 Schematic diagram of the experimental setup used for the measurement of the illuminated-to-dark change in current, ΔI, in the photocurrent-capacitance method.

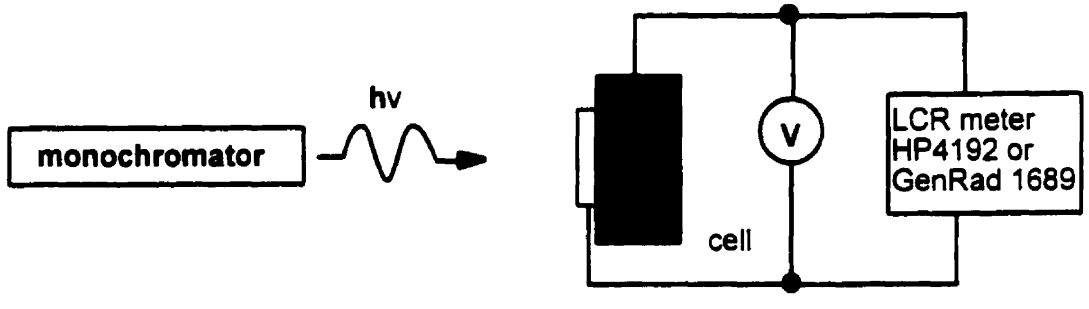


Figure 4.7 Schematic diagram of the experimental setup used for the measurement of the parallel mode capacitance, C_p, in the photocurrent-capacitance method.

CHAPTER 5

Photovoltaic Results

5.1 INTRODUCTION

Using the techniques described in sections 4.2 and 4.4 of the previous chapter. measurements were carried out on the $CuInSe_2$-CdO and $CuInSe_2$-CdS-CdO cells, consisting of current-voltage (j-V) characteristics and spectral response. The j-V measurements were carried out under solar irradiation and in darkness. The results of these measurements, all of which were determined at room temperature (20-24 °C), are presented in this chapter.

5.2 ILLUMINATED CURRENT DENSITY-VOLTAGE CHARACTERISTICS

(a) Characteristics Measured Under Solar Simulator

Plots of current density-voltage (j-V) were made on all of the cells listed in Table I under 100 mW/cm^2 of simulated solar irradiation, as described in chapter 4. Except for cells AB-1 and AB-2, which were fabricated early in this work, all the j_{sc} values listed in column 7 of Table I are seen to exceed 20 mA/cm^2 and all the conversion efficiencies (η) in column 10 exceed 4%. A comparison of the illuminated j-V characteristics between $CuInSe_2$-CdO cells and $CuInSe_2$-CdS-CdO cells is shown in Figures 5.1, 5.2, and 5.3, while Figure 5.4 shows characteristics for 3 $CuInSe_2$-CdS-CdO cells alone. It should be noted that in the early

fabricated cells AB-1 and AB-2, etching the back surface of the $CuInSe_2$ substrate, as described in chapter 3, was not optimized. Furthermore, in the case of device AB-1, the use of a different gas mixture during the CdO deposition resulted in a fairly resistive film yielding a low photovoltaic current density. In comparing the j-V results in Figure 5.4 of cells AB-6 with AB-8, it is seen that, while these two devices show similar performance characteristics, the latter cell shows a steeper rise of current density at higher voltage. This is reflected in the lower series resistance value given in column 5 of Table I, which may be partially due to the larger CdO thickness for this cell given in column 3. From the plots in Figures 5.1, 5.2, and 5.3, one can infer that, in general, the cells having the CdS interlayer, exhibited higher fill factors than those without it. Again with the exception of cells AB-1 (with CdS) and AB-2 (without CdS), cells containing the CdS interlayer generally exhibited higher short circuit current densities (j_{sc}) but had lower open circuit voltages (V_{oc}). However, columns 9 and 10 of Table I (showing F.F. and η) for cells AB-10 and AB-12 in Figure 5.3, show that the overall performances of the cells with and without the CdS interlayer were fairly comparable. While cell AB-10 had a higher short circuit current density than cell AB-12, the latter cell had a higher open circuit voltage, compensating for the slight loss of the j_{sc}, resulting in similar efficiency performance for the two cells. It is also noted in Figures 5.2 and 5.3 for voltages beyond V_{oc}, that the cells with the CdS interlayer present show a steeper increase of current with voltage than those with no CdS. In other words, series resistance, which tends to be dominant in this voltage region, was smaller in the $CuInSe_2$-CdS-CdO cells than in the $CuInSe_2$-CdO cells.

(b) Characteristics Measured Directly Under The Sun

In order to gain confidence in the accuracy of the current density-voltage measurements made indoors under the solar simulator, j-V characteristics of a representative number of cells listed in Table I were also measured outdoors, as described in chapter 4. Depending on the weather conditions, the average solar irradiance was found to be generally in the vicinity of 100 mW/cm^2 during the period mid-April to early October in Montréal, when the measurements were made. Figures 5.5 through 5.10 show plots of these solar measurements, where the cell parameters j_{sc}, V_{oc}, F.F., and η are listed within each figure. As a basis for comparison, the indoor measurements (square symbols) are also plotted with the measurements made outdoors (circular solid symbols). In general, it is noted that there was reasonable agreement between measurements made under the sun and those made under the solar simulator, considering that the error in the latter measurement is limited to about ±10%. However, cell AB-4 (Figure 5.5) showed significant improvement in performance under the sun, consisting of approximately a 60 mV increase in the open circuit voltage, yielding a 0.7% difference between the efficiencies. The only other cell which showed a small increase of V_{oc} under the sun was AB-5 (Figure 5.6), which was measured on the same day. The V_{oc} values on the other cells under the sun were essentially the same as those under the simulator. In respect of j_{sc}, the values were again essentially the same, except for cells AB-6 and AB-10 (Figures 5.7 and 5.9 respectively), where the sun-values were respectively somewhat below and above the simulator values.

5.3 DARK CURRENT DENSITY-VOLTAGE CHARACTERISTICS

Plots of dark current density (j) versus bias voltage (V) are shown in Figures 5.11 through 5.14 for both polarities on semilogarithmic scales. Plots of the dark j-V characteristics on linear scales were already shown in Figures 5.1 through 5.4. The plots in Figures 5.11 through 5.14 compare samples made with and without the CdS interlayer. Figure 5.11 shows the results on cells AB-2 and AB-4, where in the former device, the effects of high series and low shunt resistance are again evident. By contrast, cell AB-4 shows a relatively high rectification ratio of more than 3 orders of magnitude near 0.6 volt, as a result of higher shunt and lower series resistances, yielding an ideality factor of approximately 2.2. Figure 5.12 compares cells AB-5 and AB-7, where both cells show significant shunt current at low voltages (below 0.2 volt). Apart from this, the ideality factor n for cell AB-7 was 2.2, while that of AB-5 was approximately 2.8. The rectification ratio of cell AB-7 however was lower than that of AB-5, amounting to approximately 2.5 orders of magnitude near 0.6 volt. Figure 5.13 compares devices AB-10 and AB-12, where again the cell with CdS shows the steeper slope. This is reflected in an ideality factor for cell AB-10 of 1.8, less than that of cell AB-12 with a value of 2.4. The rectification ratio for cell AB-10 was approximately 4 orders of magnitude, while that for cell AB-12 was about 3 orders near 0.6 volt.

Figure 5.14 shows plots for cells AB-1, AB-6 and AB-8, all of which incorporated the CdS interlayer. Cells AB-6 and AB-8 show similar slopes giving equal ideality factor values of 1.7 as listed in column 6 of Table I. Plotted also for comparison are the characteristics of cell AB-1, which was fabricated early in this work, as mentioned in section

5.2 (a). The dark j-V curves for this cell clearly reflect the detrimental effect of excessive shunt current and series resistance, where the rectification ratio was only about two orders of magnitude, compared with cell AB-8 where it was some four orders near 0.6 volt. It is thus noted, from column 6 in Table I, that n was on the average less than 2 for the cells with the CdS interlayer present but greater than 2 for those with it absent.

5.4 SPECTRAL RESPONSE AND QUANTUM EFFICIENCY

Photoresponse measurements were carried out on two $CuInSe_2$-CdS-CdO cells (AB-7 and AB-10) and one $CuInSe_2$-CdO cell (AB-12). The photoresponse (PR) plots for all three cells are shown in Figure 5.15. It is noted that the peak lies in the wavelength region of about 1100 nm, with a slow rise on the short wavelength side of the maximum and a sharper fall-off on the long wavelength side. Figure 5.16 shows the corresponding plots of quantum efficiency (QE) against wavelength, obtained by multiplying the PR values by $hc/(q\lambda)$. Here, it is seen that the QE maxima are generally broader in wavelength than those of the P.R., ranging between 600 and 1000 nm, with an average QE-value of some 60%. This rather low quantum efficiency may be attributed to reflection and collecting electrode losses. The quantum efficiencies at the short wavelength end are seen to be slightly higher for the two cells with the CdS interlayer present than for those for the cell without it. For comparison, a curve is included in Figure 5.16 of a $CuInSe_2$/CdS thin film polycrystalline cell obtained from the earlier work of Kazmerski [5.1]. Here, it is noted that the fall-off with decreasing wavelength at the violet end is much sharper than that observed in the present results, possibly due to the use, at that time, of evaporated rather than chemically deposited

CdS.

The short circuit current density for the cells AB-7, AB-10 and AB-12 was calculated from the photoresponse curves in Figure 5.15 using the AM1.5 global irradiance spectrum shown in Figure 5.17 obtained from the Tutorial Manual of the 23rd IEEE PVSC. These cells yielded calculated short circuit current densities of 26, 25 and 24 mA/cm^2 respectively compared to the actual measured j_{sc} values of 34, 33, and 30 mA/cm^2 for the cells AB-7, 10 and 12. Thus, the calculated and measured values are in the same sequence; the lower difference of average magnitude, however, may be due to the low light levels used in the monochromator measurements, compared to the 100 mW/cm^2 irradiation used for the j_{sc} determinations. Nevertheless, this is contrary to what is usually observed in other cells.

5.5 DISCUSSION

The results of the current-voltage characteristics, illuminated and dark, and spectral response are now discussed.

Firstly, the question of accuracy should be raised in respect of the solar irradiation on the cells. Comparison of the illuminated j-V characteristics under the laboratory simulator and under the sun showed sufficient agreement to give confidence in the indoor irradiation measurements. Here, the accuracy would appear to be some ±10%, which is enough to determine the photovoltaic effects of specific changes in the fabrication processes.

The most important result in this chapter is the fact that the conversion efficiency of the $CuInSe_2$-CdO cell was not significantly lower than that of the $CuInSe_2$-CdS-CdO device, which contained a CdS interlayer. This is despite the fact that the lattice mismatch between

$CuInSe_2$ and CdO is some 23 %, whereas that between $CuInSe_2$ and CdS is only about 1%. There was indeed evidence of greater recombination current in the cells without CdS as indicated by their larger j-values at low forward current, leading to the higher ideality factors above 2. The question, therefore, is why did this increased recombination current not lead to lower conversion efficiency. It is speculated that the active photovoltaic junction may lie some distance away from the interface of the $CuInSe_2$ with CdO, where there would be many interface states. In other words, there may be a buried homojunction in the $CuInSe_2$. This could be formed by the diffusion of cadmium into the chalcopyrite from the CdO, since Cd is reported to be a donor in $CuInSe_2$ [1.16][5.2]. There were other differences between the two kinds of cell. In general, the devices with the CdS interlayer present yielded slightly lower V_{oc}-values but higher j_{sc} -values than those of the cells without the interlayer. The higher j_{sc}-values are consistent with the observation of slightly higher quantum efficiencies at the shorter wavelengths for these cells. The smaller V_{oc}-values could be due to the smaller ideality factors less than 2 according to equation (2.6B) (chapter 2) in the cells with CdS. However, it is more likely that the higher V_{oc} in the cells without CdS is due to a smaller electron affinity in CdO than in CdS and/or a donor level closer to the conduction band in the CdO (equation (2.10), chapter 2).

The rather low values of quantum efficiency (Figure 5.16) of around 60 % are predominantly due to the absence of an antireflection coating and to the series resistance arising from the simple type of current collecting grid, consisting of just two stripes of indium on the illuminated CdO area. The maximum conversion efficiency observed on the cells was 6.8% but, with an antireflection coating and an optimized current collecting grid,

this quantity is likely to rise above 8%, which is a remarkable figure for a semiconductor window material with an apparent 23% lattice mismatch to the absorber layer.

Calculations from the illuminated j-V characteristics of illuminated series resistance R_s and shunt resistance R_{sh} will be given in section 7.4.

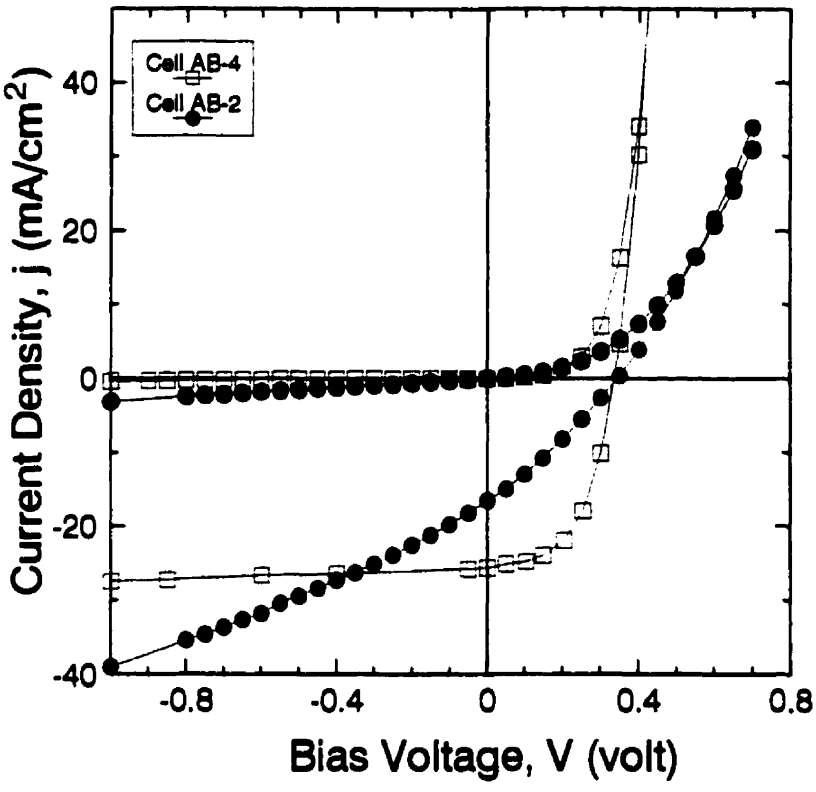


Figure 5.1 Illuminated (solar simulator, 100 mW/cm^2) and dark j-V characteristics of cells AB-2 (without CdS interlayer) and AB-4 (with CdS interlayer).

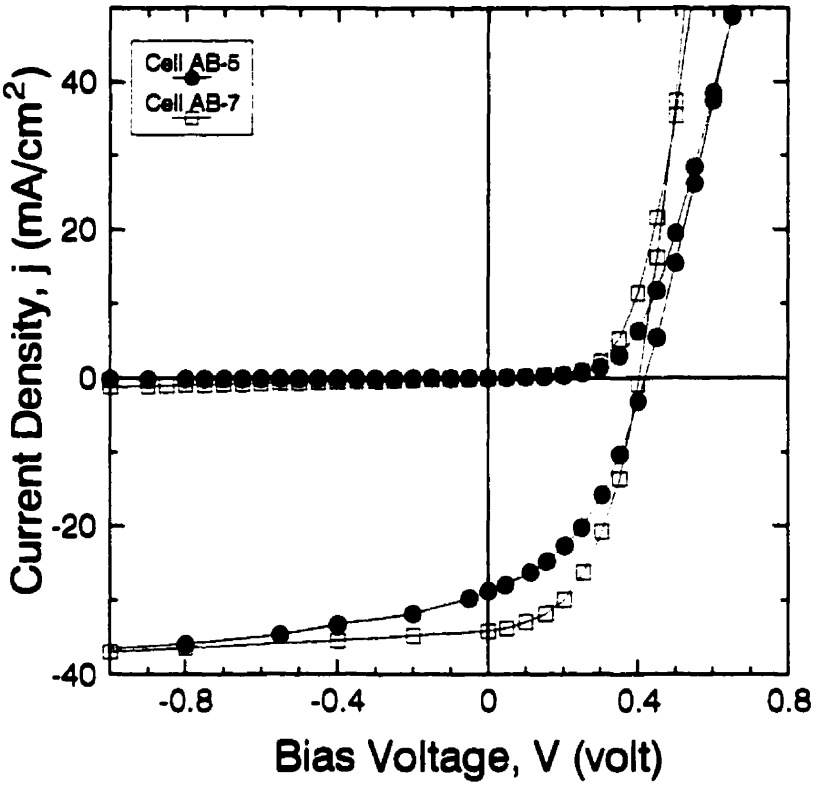


Figure 5.2 Illuminated (solar simulator, 100 mW/cm^2) and dark j-V characteristics of cells AB-5 (without CdS interlayer) and AB-7 (with CdS interlayer).

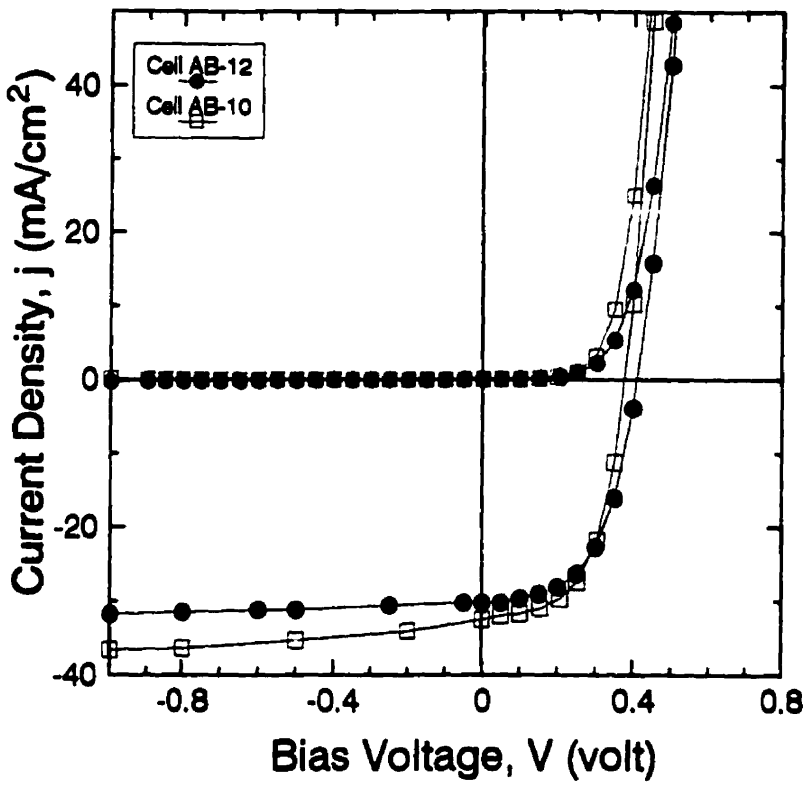


Figure 5.3 Illuminated (solar simulator, 100 mW/cm^2) and dark j-V characteristics of cells AB-10 (with CdS interlayer) and AB-12 (without CdS interlayer).

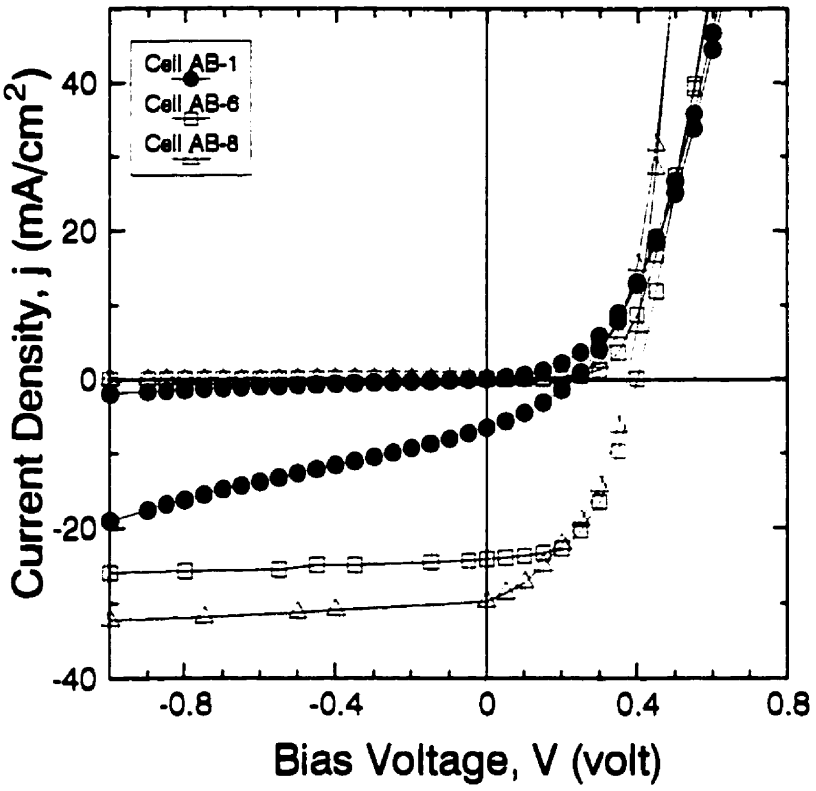


Figure 5.4 Illuminated (solar simulator, 100 mW/cm^2) and dark j-V characteristics of cells AB-1, AB-6 and AB-8 (all with CdS interlayer).

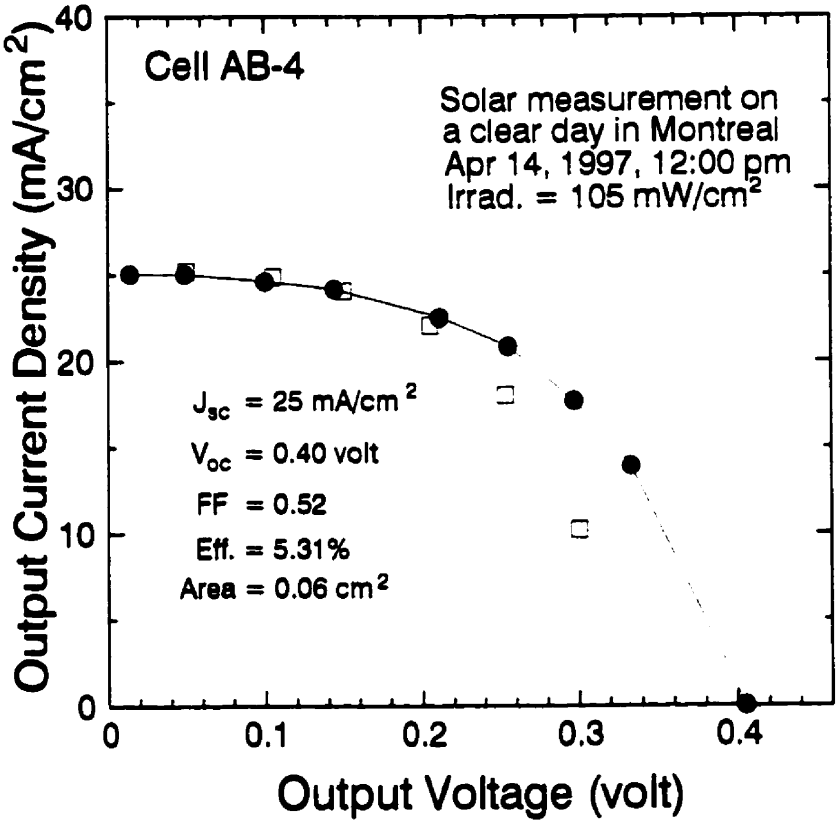


Figure 5.5 Current density-voltage (j-V) characteristics of cell AB-4, as measured under actual solar irradiation under the conditions indicated. The dotted lines (square symbols) show the j-V characteristics as measured under the solar simulator with 100 mW/cm^2 solar irradiation.

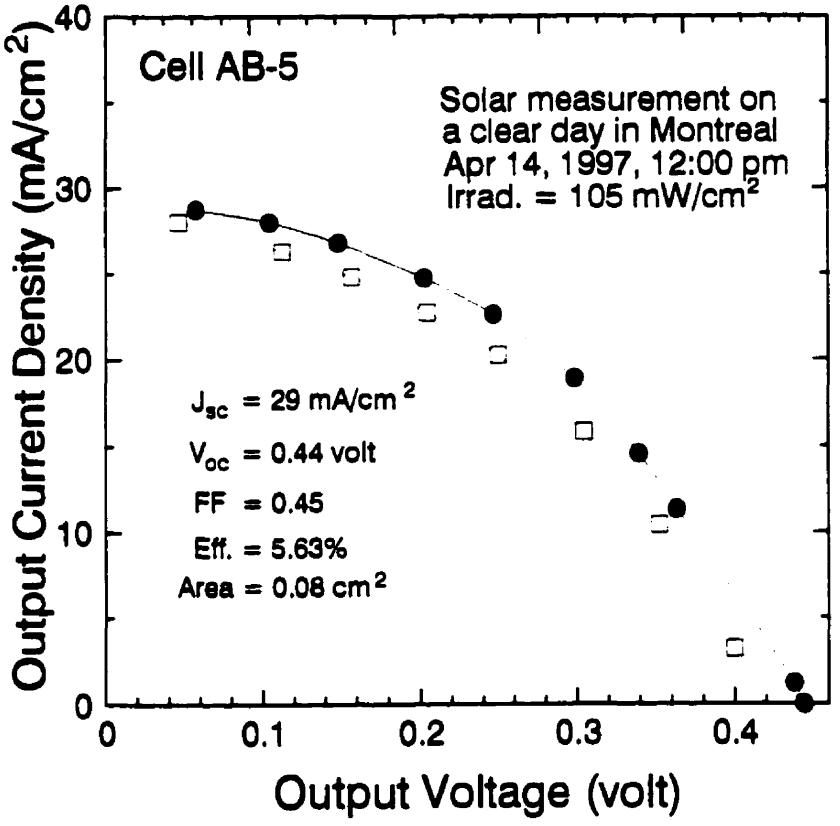


Figure 5.6 Current density-voltage (j-V) characteristics of cell AB-5, as measured under actual solar irradiation under the conditions indicated. The dotted lines (square symbols) show the j-V characteristics as measured under the solar simulator with 100 mW/cm^2 solar irradiation.

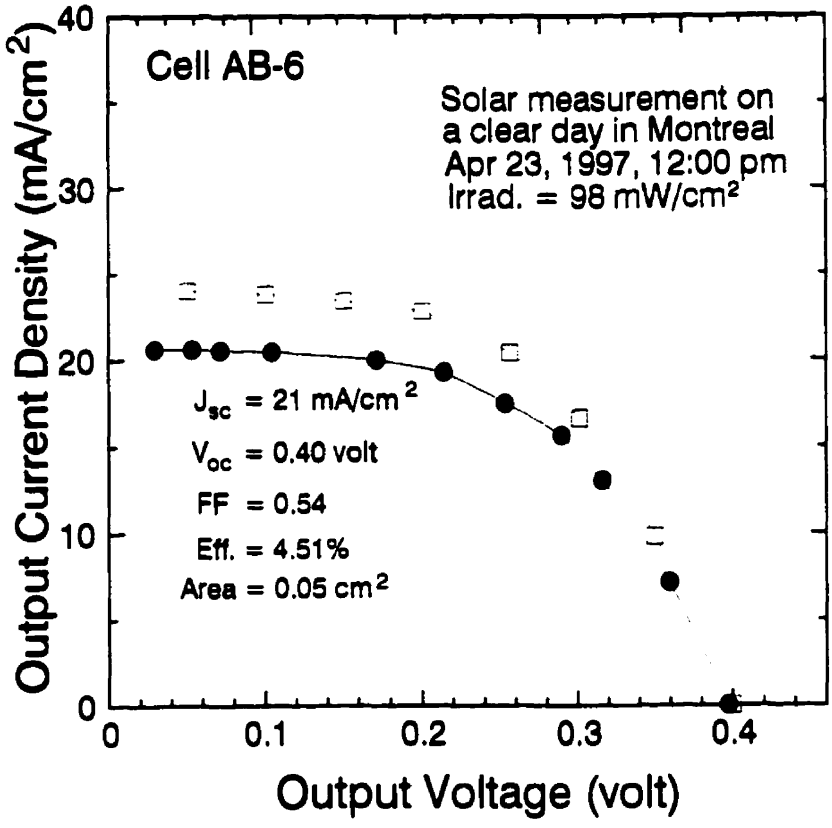


Figure 5.7 Current density-voltage (j-V) characteristics of cell AB-6, as measured under actual solar irradiation under the conditions indicated. The dotted lines (square symbols) show the j-V characteristics as measured under the solar simulator with 100 mW/cm^2 solar irradiation.

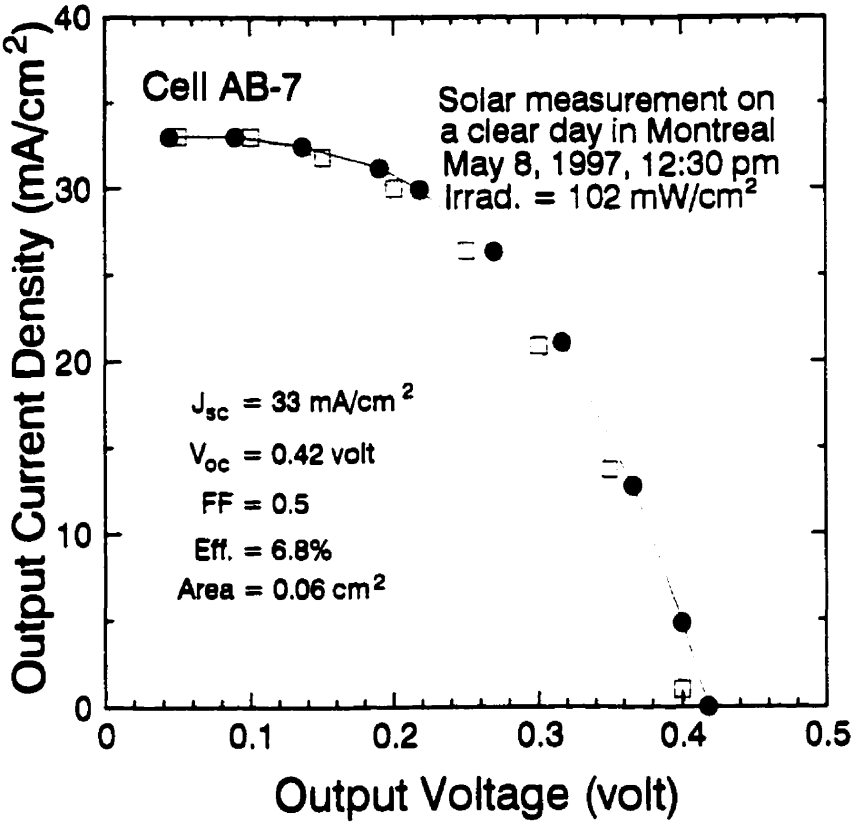


Figure 5.8 Current density-voltage (j-V) characteristics of cell AB-7, as measured under actual solar irradiation under the conditions indicated. The dotted lines (square symbols) show the j-V characteristics as measured under the solar simulator with 100 mW/cm^2 solar irradiation.

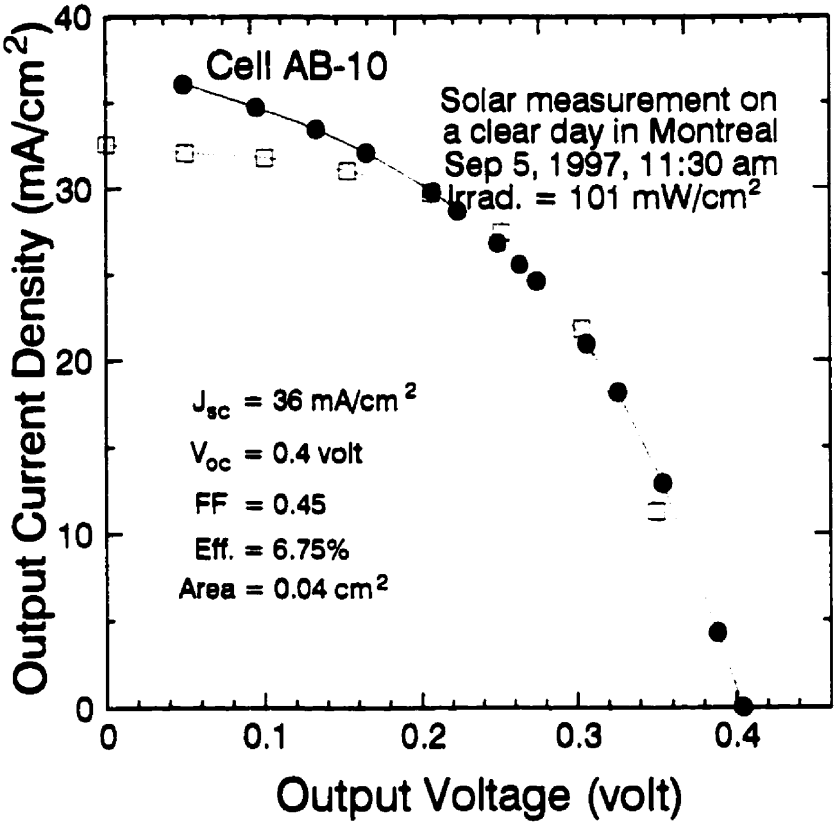


Figure 5.9 Current density-voltage (j-V) characteristics of cell AB-10, as measured under actual solar irradiation under the conditions indicated. The dotted lines (square symbols) show the j-V characteristics as measured under the solar simulator with 100 mW/cm^2 solar irradiation.

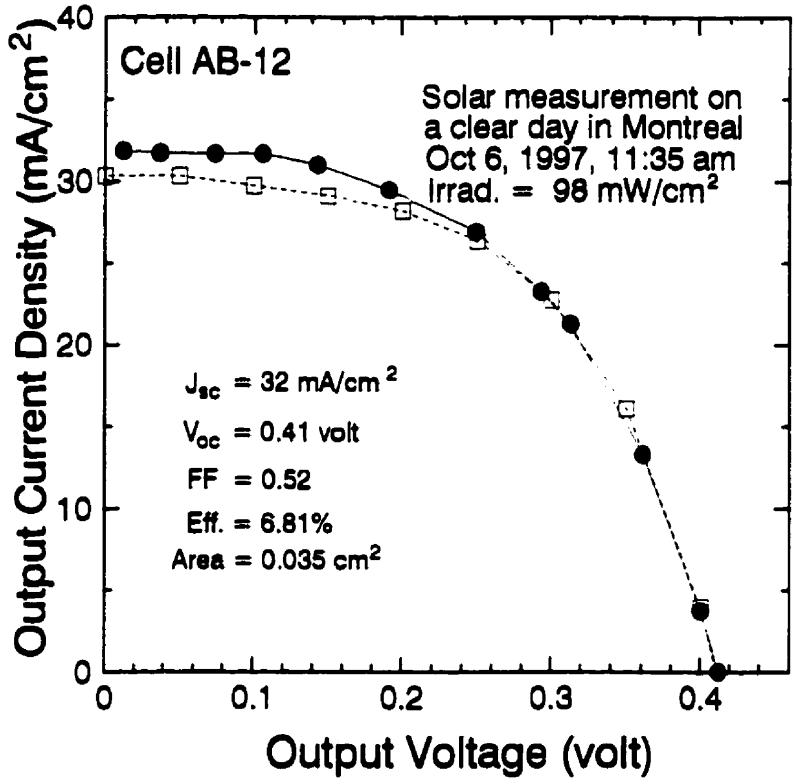


Figure 5.10 Current density-voltage (j-V) characteristics of cell AB-12, as measured under actual solar irradiation under the conditions indicated. The dotted lines (square symbols) show the j-V characteristics as measured under the solar simulator with 100 mW/cm^2 solar irradiation.

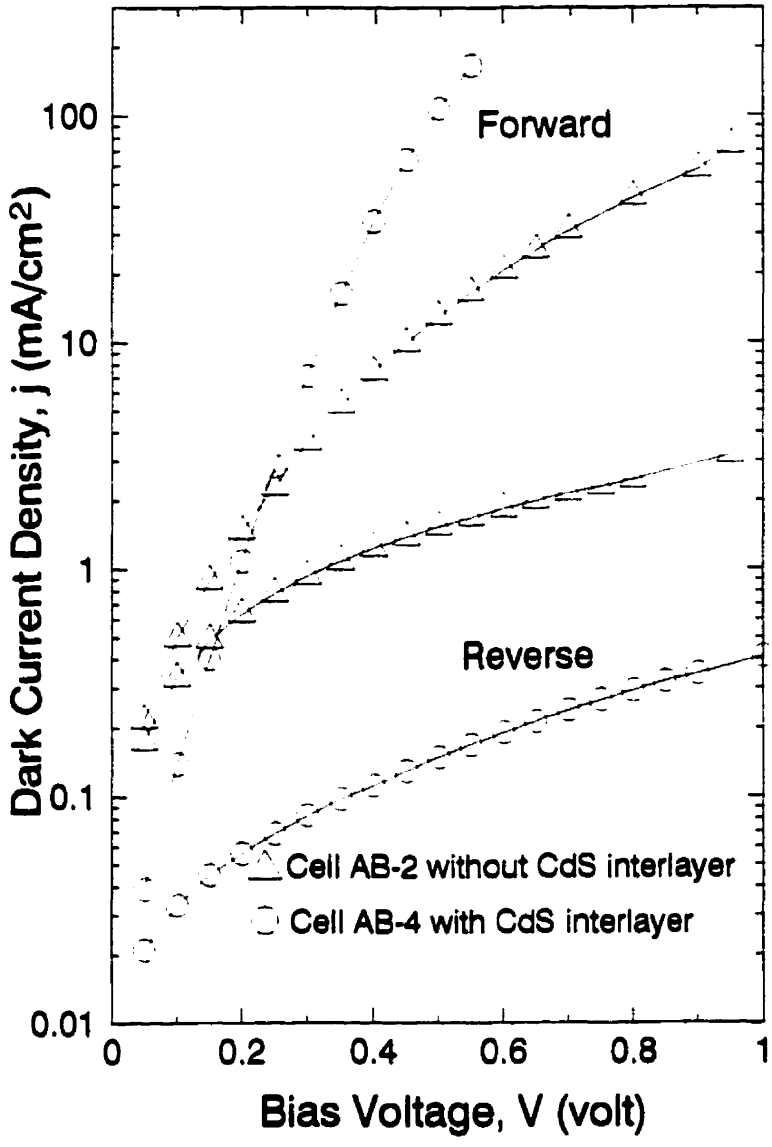


Figure 5.11 Dark j-V plots of cells AB-2 and AB-4 on semilogarithmic scales.

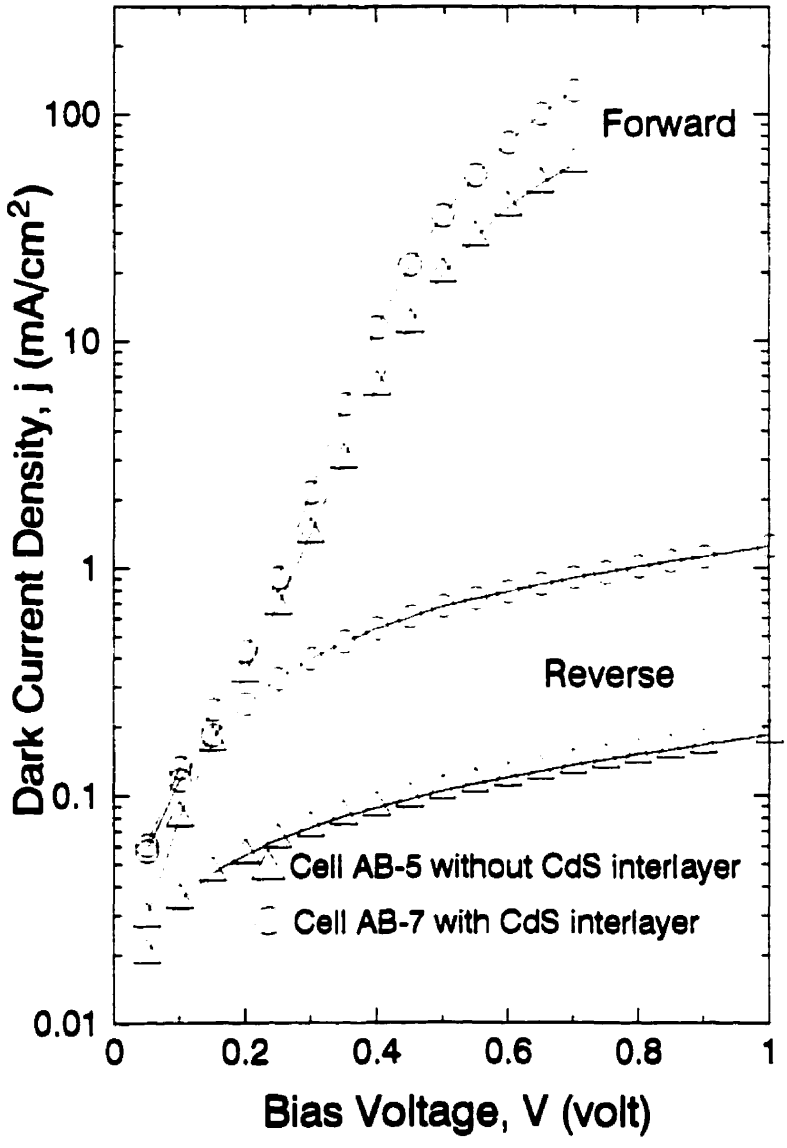


Figure 5.12 Dark j-V plots of cells AB-5 and AB-7 on semilogarithmic scales.

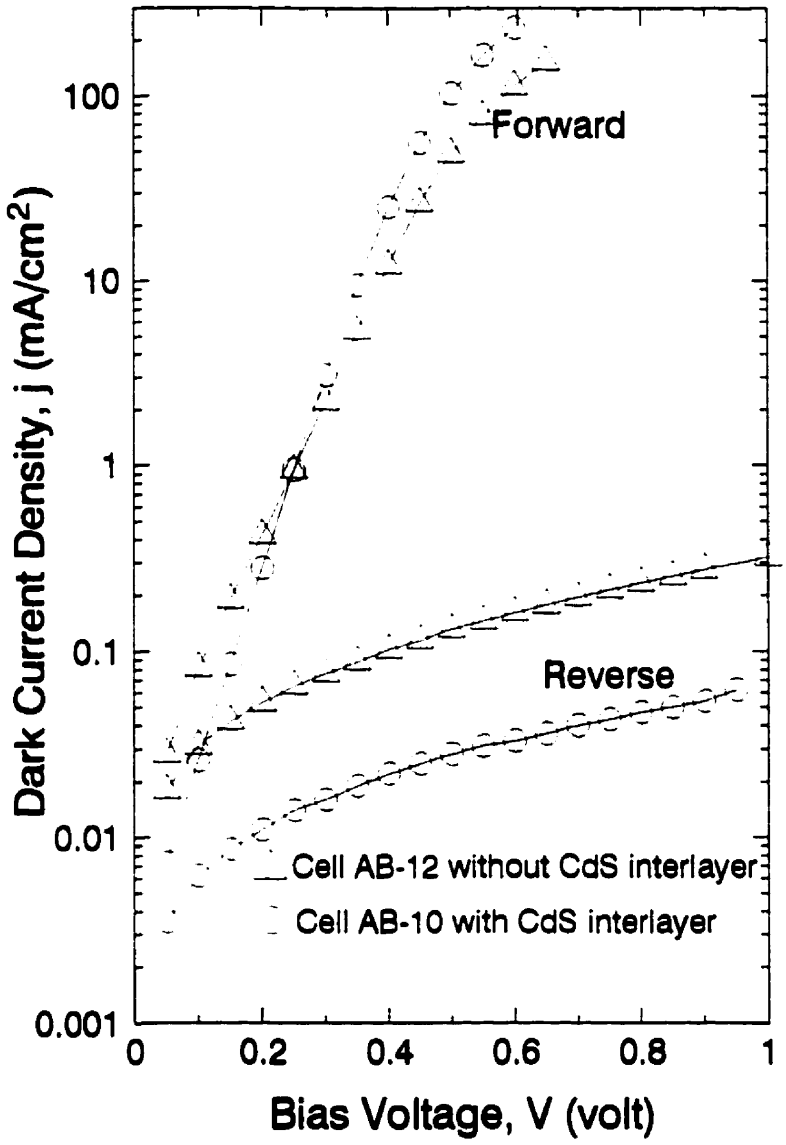


Figure 5.13 Dark j-V plots of cells AB-10 and AB-12 on semilogarithmic scales.

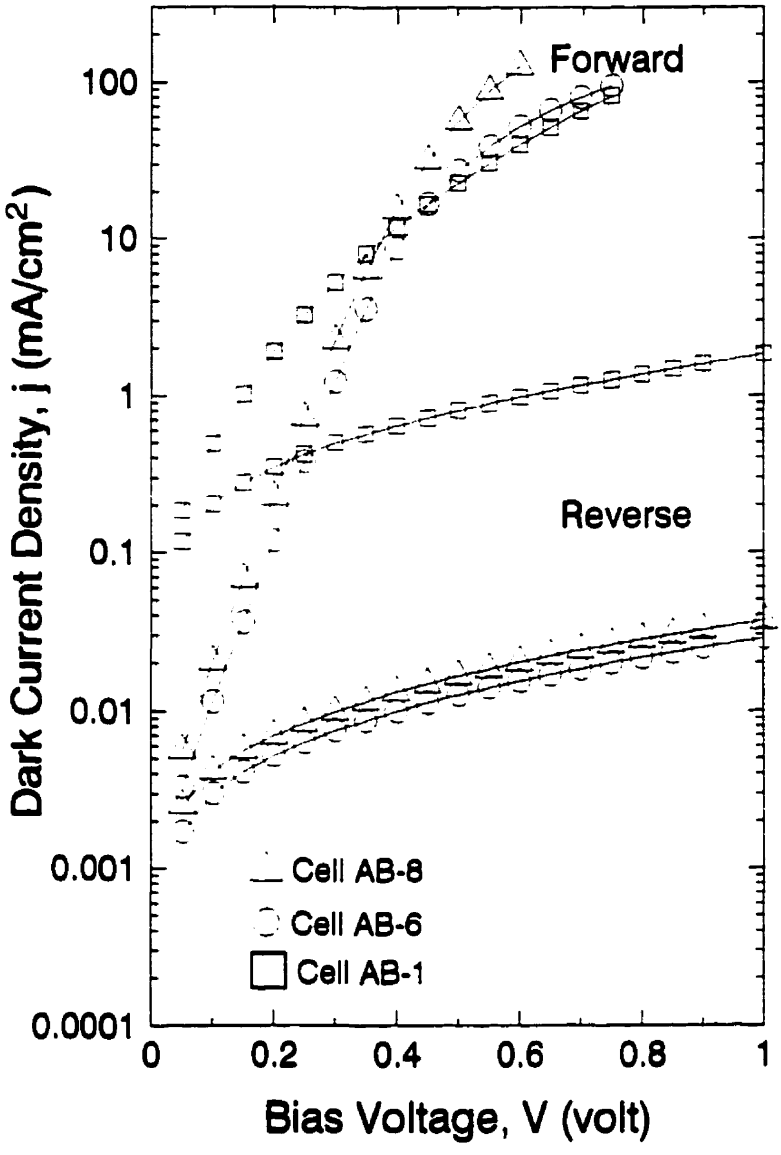


Figure 5.14 Dark j-V plots of cells AB-1, AB-6 and AB-8 on semilogarithmic scales.

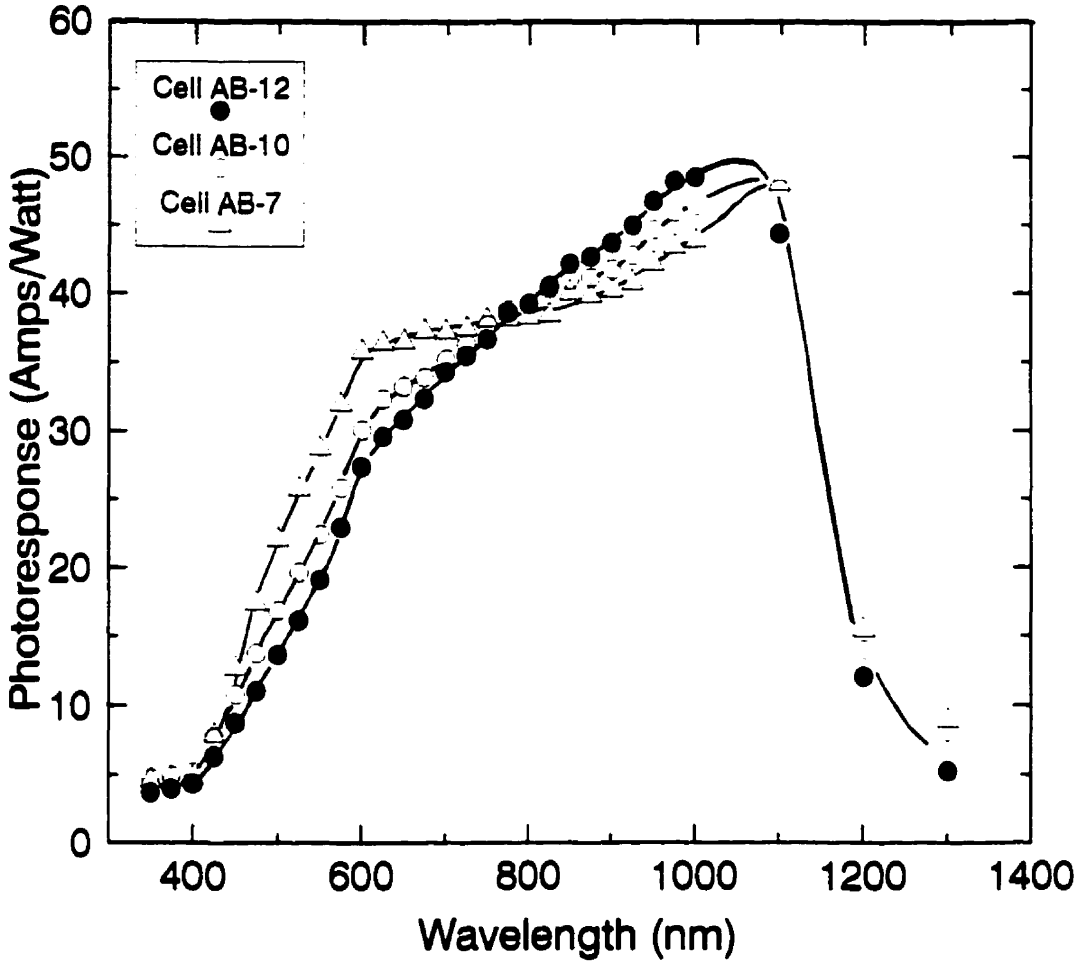


Figure 5.15 Plot of photoresponse against wavelength for three representative cells AB-7, AB-10 and AB-12 measured at zero bias.

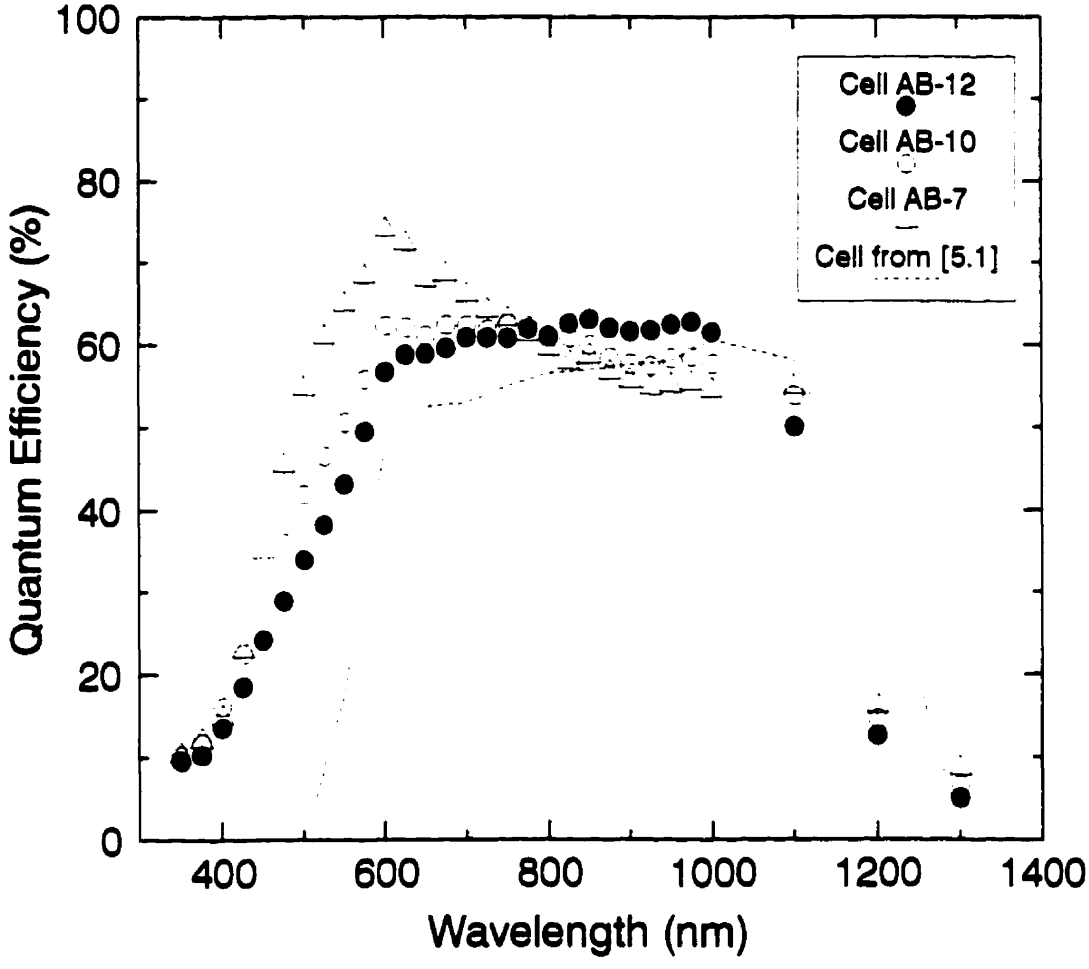


Figure 5.16 Plot of quantum efficiency against wavelength for the three representative cells AB-7, AB-10 and AB-12 (from the measurements in Figure 5.15), together with a curve for a $CuInSe_2$/CdS cell from reference [5.1].

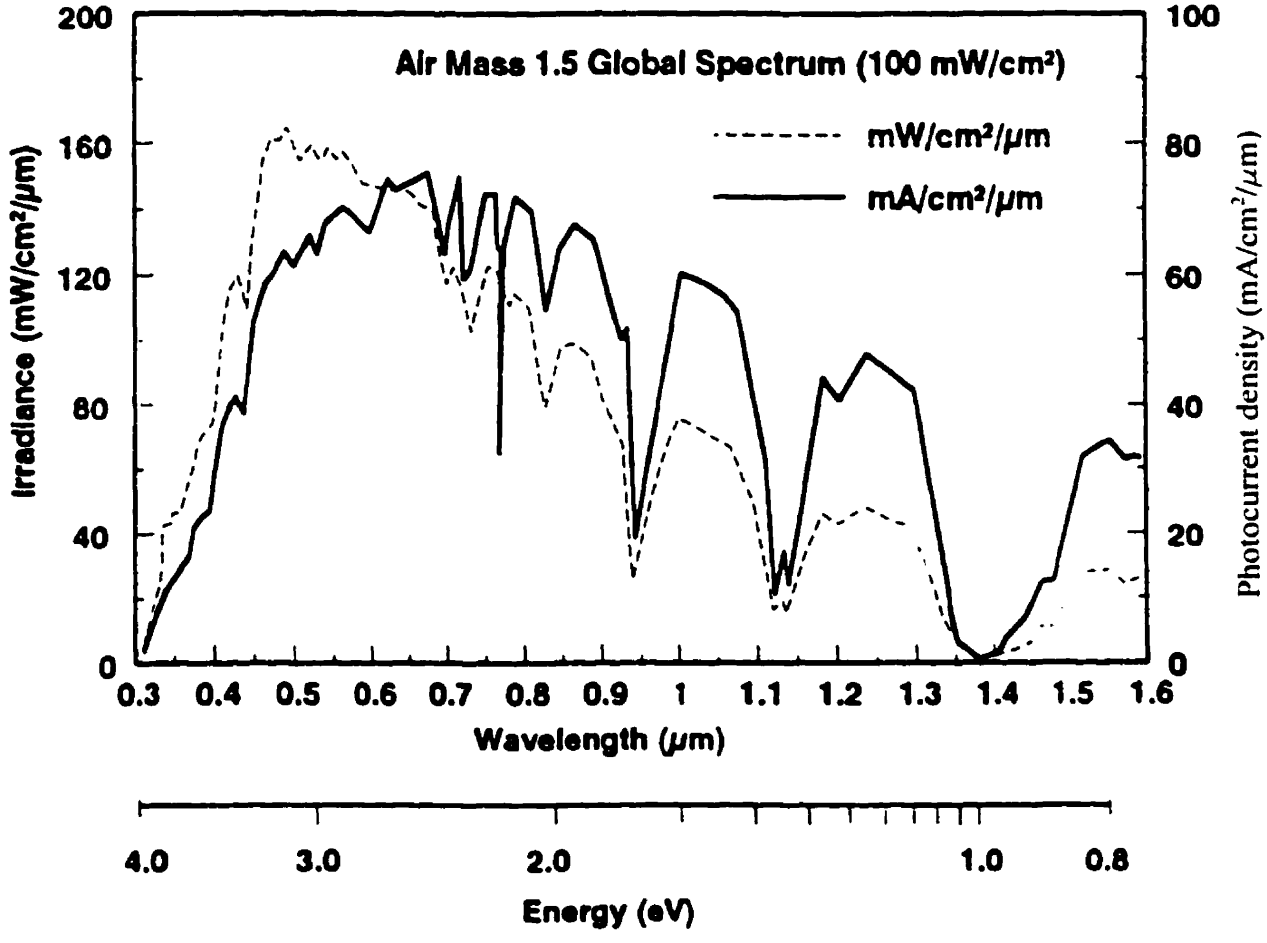


Figure 5.17 AM1.5 global irradiance spectrum (broken line) and photovoltaic response assuming 100% quantum efficiency (solid line). (After K. Mitchell and H. Schock, Tutorial Notebook, 23rd IEEE PVSC Conf., 1993).

CHAPTER 6

Capacitance and Other Results

6.1 INTRODUCTION

Besides the important measurements of current-voltage characteristics and spectral response reported in chapter 5 , other measurements were made on the cells to help in their further characterization. These measurements were capacitance as a function of bias and frequency and estimations of the electron diffusion length by the photocurrent-capacitance method. The results of these measurements are presented in this chapter. Some preliminary electron beam induced current (EBIC) investigations are also reported, along with results on the deposition of CdO.

6.2 CAPACITANCE-VOLTAGE MEASUREMENTS

(a) Capacitance-Voltage Characteristics

Plots of capacitance (C_p) against voltage, as described in section 4.3, were made on all the cells listed in Table I and the characteristics of four representative cells AB-5, AB-6, AB-10 and AB-12 are shown in Figures 6.1 and 6.2. All the cells are seen to exhibit similar general profiles at reverse bias voltage, with maxima at forward bias voltages in the range

between 0.25 and 0.35 volt. Comparing the characteristics of cells AB-5 and AB-12 (Figures 6.1 (a) and 6.2 (b)), devices without CdS, with cells AB-6 and AB-10 (Figures 6.1 (b) and 6.2 (a)), devices with CdS, the only apparent difference appears to be a slightly larger drop of C_p with voltage following the maximum in each case for the former cells. Capacitance values beyond a forward bias of approximately 0.5 volt are not shown, since these were usually unsatisfactory, possibly due to heavy loading on the instrument (Digibridge or HP Impedance Analyzer). Furthermore, capacitance values at frequency settings below 1 kHz are also not shown because these yielded unstable readings from the measuring instruments.

(b) Mott-Schottky Characteristics

As discussed in chapter 4, Mott-Schottky plots can reveal two useful pieces of information, firstly, the acceptor concentration profile of the cell substrate material ($CuInSe_2$) and secondly it can give an estimate of the built-in voltage for the junction. It is helpful first to show results which confirm the experimental trends observed by Shukri [1.3]. Figure 6.3 shows the Mott-Schottky plots measured on cell AB-5 and a similar earlier-made cell (cell AC-2, not listed in Table I), which was fabricated without the substrate annealing step (section 3.2 (c)). The variation for the cell with the annealed substrate (AB-5) clearly shows a steeper slope with increasing forward voltage near zero bias, whereas the cell made without this heat-treatment shows a straighter characteristic (with even a slight tendency to curve upwards) in this voltage region. Despite this, the two curves have about the same slope at the relatively large reverse bias near 2 volts. This is the same trend as that observed by Shukri [1.3] . The present Mott-Schottky results on the cells mentioned in section 6.1(a) are

presented in Figures 6.4 through 6.7. From these results, it can be seen, that in the reverse direction, the slopes of the characteristics of all the cells are not very different from one another, yielding a corresponding slope-determined acceptor concentration in the $CuInSe_2$ substrate in the range of 3.5×10^{16} to about 1×10^{17} cm^{-3}. It is apparent that near zero bias, the trend of the points exhibits a downward curvature for all the devices, which, as mentioned above, is characteristic of substrate-annealed cells. This suggests that the acceptor concentration in the $CuInSe_2$ absorber material decreases with distance from the metallurgical junction. In this region near the junction, the slope-determined acceptor concentration is typically in the range of 2×10^{16} (cells AB-5 and AB-6) to about 3.5×10^{16} cm^{-3} (cells AB-10 and AB-12). If the approximately linear region between about 1 and 2 volts in the reverse direction, is extrapolated to the abscissa, it would yield an intercept on the voltage axis greater than 2.5 volts, which is rather large and thus difficult to interpret. However, extrapolation from the region near zero bias, for small forward voltages, yields much lower intercepts of about 0.3 to 0.5 volt for the 10 kHz measurements. Ideally, the intercept on the voltage axis in such plots would, as mentioned earlier, yield the value of the built-in potential for the junction.

6.3 ESTIMATION OF ELECTRON DIFFUSION LENGTH L_n

Photocurrent-capacitance measurements, as described in section 4.5 to estimate the diffusion length L_n for electrons, were carried out on 4 samples (AB-6, AB-8, AB-10 and AB-12) and the results for L_n are shown in column 11 of Table I. Meaningful measurements were not made on the other 5 cells of Table I for reasons to be discussed below. Figures 6.8

through 6.11 show plots of illuminated-to-dark photocurrent change (ΔI) as a function of reciprocal parallel mode capacitance ($1/C_p$). In part (a) of these figures the variation of ΔI with $1/C_p$ is given for the wavelengths (λ) of 1.1, 1.2, and 1.3 μm, for a fixed monochromator slit width of 5 mm. The linear portions through the experimental points are extrapolated to the $1/C_p$ axis, where the intercepts for the different wavelengths are seen to be not particularly coincident. For reasons discussed in chapter 4, therefore, the wavelength of 1.2 μm was chosen as the most suitable value for estimating L_n. Accordingly, in the (b) parts of figures 6.8 through 6.11, ΔI is plotted against $1/C_p$ for different monochromator slit widths, for the single wavelength of 1.2 μm. It is noted that, in this case, the extrapolated intercepts on the negative $1/C_p$ axis are closer together and thus the average values of these were used to calculate L_n as given in column 11 of Table I. For the cells without the CdS interlayer, only one L_n value of 3 μm was obtained (cell AB-12). This value is in the same range as that observed by Shukri [1.3] on this type of cell. For the cells with CdS present, the L_n values were smaller, with an average value from Table I of about 1.4 μm.

A dark j-V curve is shown for cell AB-7 in Figure 6.12 (a), exhibiting somewhat excessive shunt current, seen as a slight bulge in the forward curve at low voltages. Figure 6.12 (b) shows the detrimental effect of this excessive shunt current on the photocurrent-capacitance measurement, whereby extrapolations here would lead to very high intercepts for this cell, which cannot be interpreted in a simple way. While the photocurrent-capacitance method is very tolerant to series resistance as reported by Chan in his work with Se/CdO structures [4.1][4.2][4.3][4.4], it is highly intolerant to shunt current because the method depends on the reverse current arising from carriers generated from the depletion and

diffusion regions and not from current driven through an undesired parallel shunt path. For this reason, L_n - measurements were not possible on cells AB-1, 2, 4, 5 and 7.

6.4 PRELIMINARY EBIC INVESTIGATIONS

Some preliminary attempts were made to obtain an electron beam induced current (EBIC) scan across a cell. An EBIC measurement involves scanning an electron beam across the width of a sectioned device having a charge-collecting junction. The electron beam generates electron-hole pairs in a volume surrounding it inside the semiconductor. For the electron pairs generated close enough to diffuse to the space charge region of the p-n junction, the electron-hole pairs will be separated by the electric field and contribute to an external short-circuited current (EBIC signal). This current is measured and recorded for the particular position of the electron beam. By scanning the electron beam across the junction and plotting the measured EBIC signal against the beam position, an EBIC scan of the junction can be obtained. Ideally, the EBIC signal should peak at the position with the maximum electric field (metallurgical junction of a p-n junction). Therefore, the position of the EBIC peak is a good indicator of the approximate position of the p-n junction.

Figure 6.13 (a) shows such a scan across a section of device AB-9 (not listed in Table I), a cell with a CdS interlayer. Here the peak appears to lie about a micrometer below the $CuInSe_2$/CdS interface, which would appear to indicate the existence of a buried layer. However, there is some uncertainty whether the edges visible in the micrograph really correspond to the interfaces within the structure. Figure 6.13 (b) shows an EBIC scan on the same sample after the CdS and CdO layers were removed by carefully etching with a pipette

using diluted hydrochloric acid ($HCl:H_2O$ 1:5 by volume) . In this case, the peak again occurs slightly within the $CuInSe_2$, but the distance is less than one micrometer. Thus, because of these small shifts and the preliminary nature of this study, these EBIC investigations must be regarded as rather inconclusive. Furthermore, no EBIC scan was successful on a sectioned cell without the CdS interlayer, where the postulated buried junction would have a greater effect.

6.5 INVESTIGATION OF REACTIVELY SPUTTERED CdO FILMS ON GLASS

In the early stages of this research work, CdO films were reactively sputtered on glass slides in order to determine optimum deposition conditions using different gas compositions and sputtering currents. The structure of the samples was rather simple, consisting of a single layer of a CdO film sputtered on a thin glass substrate (slide). The thickness and resistivity (ρ) were then measured as described in section 3.5 (a). The objective, more specifically, of this study was to investigate the possibility of obtaining high resistivity CdO films as a substitute for the CdS interlayer used later in the photovoltaic cells of this work.

Figure 6.14 (a) shows a plot of thickness vs. time for a 50% O_2, 50% Ar gas mixture and a 5 mA sputtering current (solid circular points). It is seen that there is essentially a linear relation between film thickness and sputtering time. The triangular symbols correspond to results on two films deposited using a 10% O_2 in Ar gas mixture and a 10 mA sputtering current. Assuming a linear dependence on sputtering time in this case, one can draw a straight line through these points to the origin. The larger slope indicates that, as expected, the deposition rate increases with higher sputtering current. In addition, in agreement with

Champness and Chan [6.1], the lower the oxygen content in the gas mixture, the higher is the deposition rate. Figure 6.14 (b) shows a plot of resistivity vs. film thickness. The solid circle points are again for the 50% O_2 in Ar gas mixture and 5 mA sputtering current, where it is seen that there is an increase in resistivity with increasing film thickness. The two triangular points are for a 10% O_2 in Ar gas mixture and a 10 mA sputtering current and correspond to a lower resistivity, which again is consistent with the observation of Champness and Chan [6.1] that ρ decreases with decrease of oxygen content and increase of sputtering current.

6.6 DISCUSSION

The capacitance results reported in this chapter do not seem to show a significant difference between the two kinds of cell. Since the devices without the CdS interlayer showed a slightly higher V_{oc} (section 5.2), one might have expected a larger extrapolated intercept on the voltage axis from the Mott-Schottky plots for these cells. However, such a difference was not apparent, at least for the frequency of 10 kHz. The average slope of these plots gave an apparent acceptor concentration of the order of 10^{17} cm^{-3} in the bulk and a value of about a half or a third of this near zero bias, corresponding to a location closer to the junction. Some confidence that the hole concentration was about $10^{17}cm^{-3}$ was also obtained from the results of Hall effect measurements made on similar material by G. Ahmad [3.2].

The estimates of the electron diffusion length L_n averaged to about 1.4 μm for the $CuInSe_2$-CdS-CdO cells using the photocurrent-capacitance method. While only one estimate was possible for L_n for the $CuInSe_2$-CdO cells, its higher value of 3 μm may be significant,

since this magnitude was also reported by Shukri [1.3] in his measurements on this kind of device. The higher L_n value probably reflects the fact that the surfaces of the cells without the CdS interlayer were cleaved {112}, while abrasive polishing was used for the $CuInSe_2$ substrates for the cells with the CdS interlayer. If this is so, it indicates that the annealing process does not eliminate all the surface imperfections that reduce the lifetime and mobility of the carriers in the $CuInSe_2$. The selection of the wavelength of 1.2 μm for the L_n estimates was made because of the need to satisfy the relation $\alpha W << 1$, where α is the optical absorption coefficient, which at this wavelength is about 2×10^3 cm^{-1} [6.2] and W is the depletion width, estimated at about 0.2 μm. Hence, αW at λ=1.2 μm amounts to 0.04, which satisfies the required inequality.

The EBIC experiments mentioned in section 6.4 must be regarded as very preliminary but they are generally supportive of the idea that there is a buried homojunction in the cells fabricated in this work. A junction lying less than a micrometer below the interface with the CdS, however, is hardly sufficient to explain the apparent insensitivity of the photovoltaic performance to interface imperfections arising from lattice mismatch. This is especially so, since it was not possible to obtain an EBIC scan successfully for a $CuInSe_2$/CdO cell, where the effect of a buried junction would be greater.

The experiments with sputtering CdO were carried out in an attempt to obtain a high electrical resistivity film of this oxide by using a sputtering gas rich in oxygen deposited at a slow rate. It was observed that, indeed, the film resistivity (ρ) increased on raising the oxygen content from 10 to 50% (with the remainder gas being argon) and on reducing the sputtering current from 10 to 5 mA, thus reducing the deposition rate. However, the increase

of ρ was less than an order of magnitude, which is insufficient to obtain a high resistivity film. It was also confirmed that the thickness of the CdO increased linearly with sputtering time. In addition, an increase of resistivity with sputtering time was found, which may be due to a change in the target surface as sputtering proceeds.

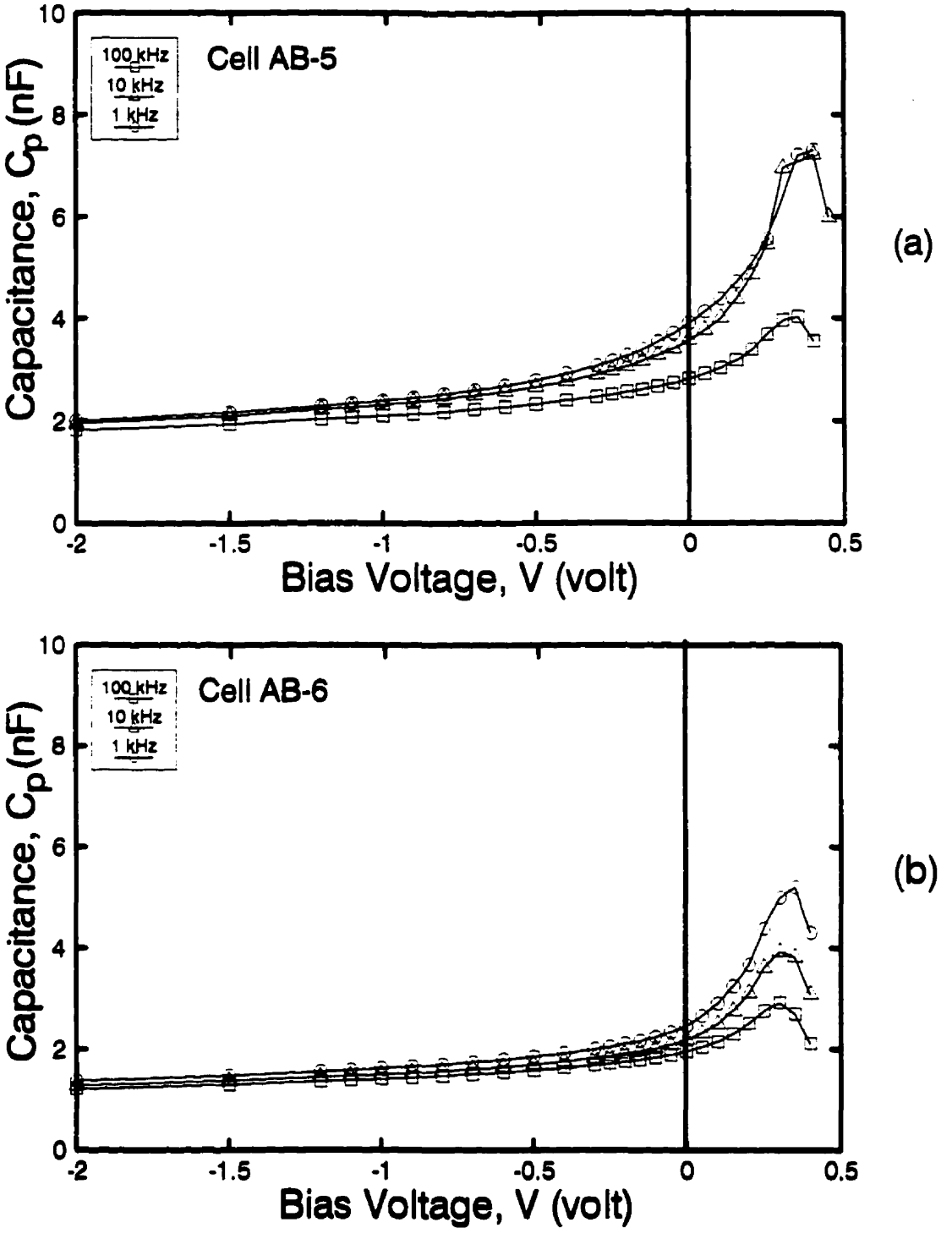


Figure 6.1 Plot of equivalent parallel capacitance, C_p, against bias voltage (V) at three different frequencies for (a) cell AB-5 and (b) cell AB-6.

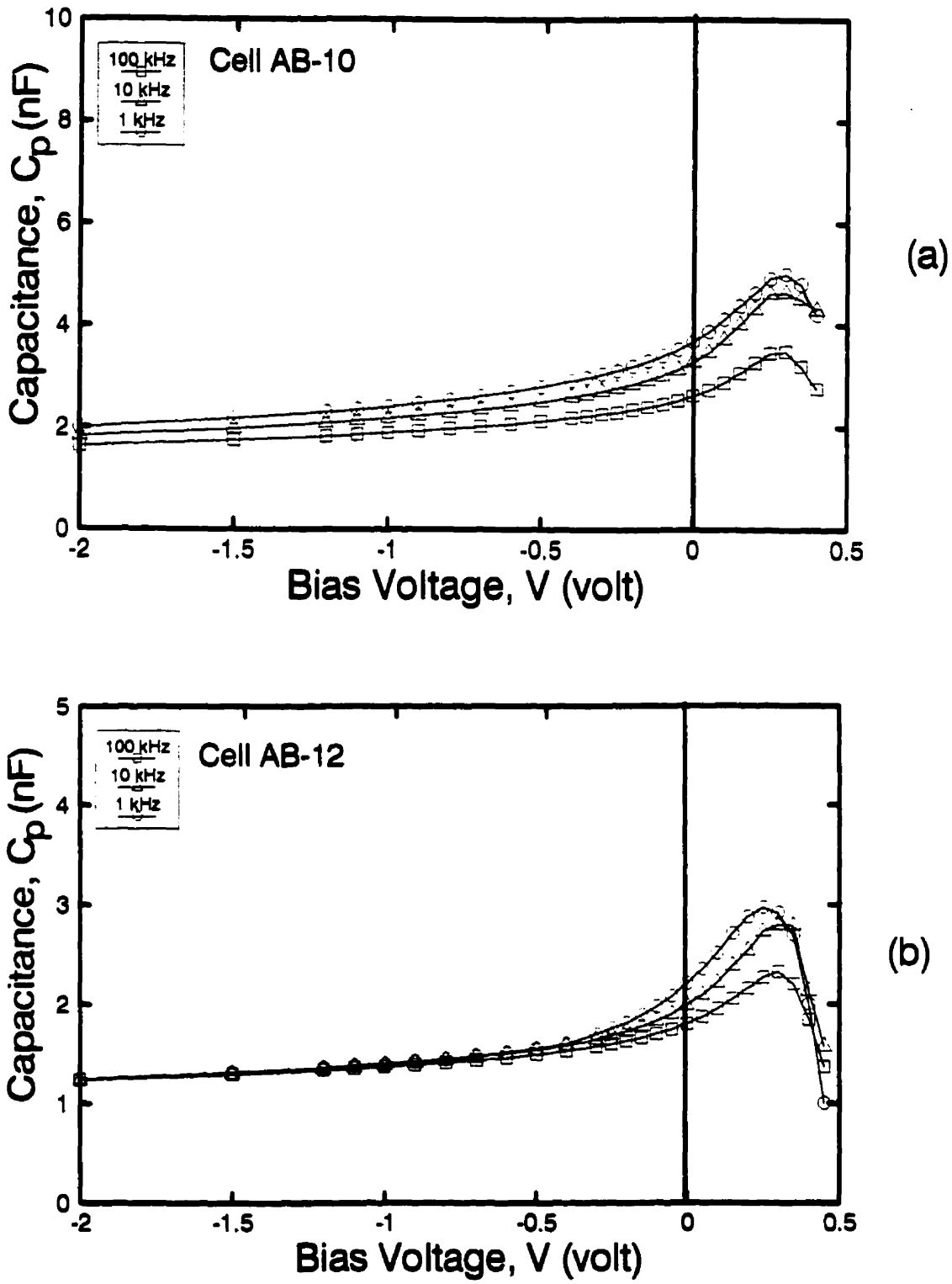


Figure 6.2 Plot of equivalent parallel capacitance, C_p, against bias voltage (V) at three different frequencies for (a) cell AB-10 and (b) cell AB-12.

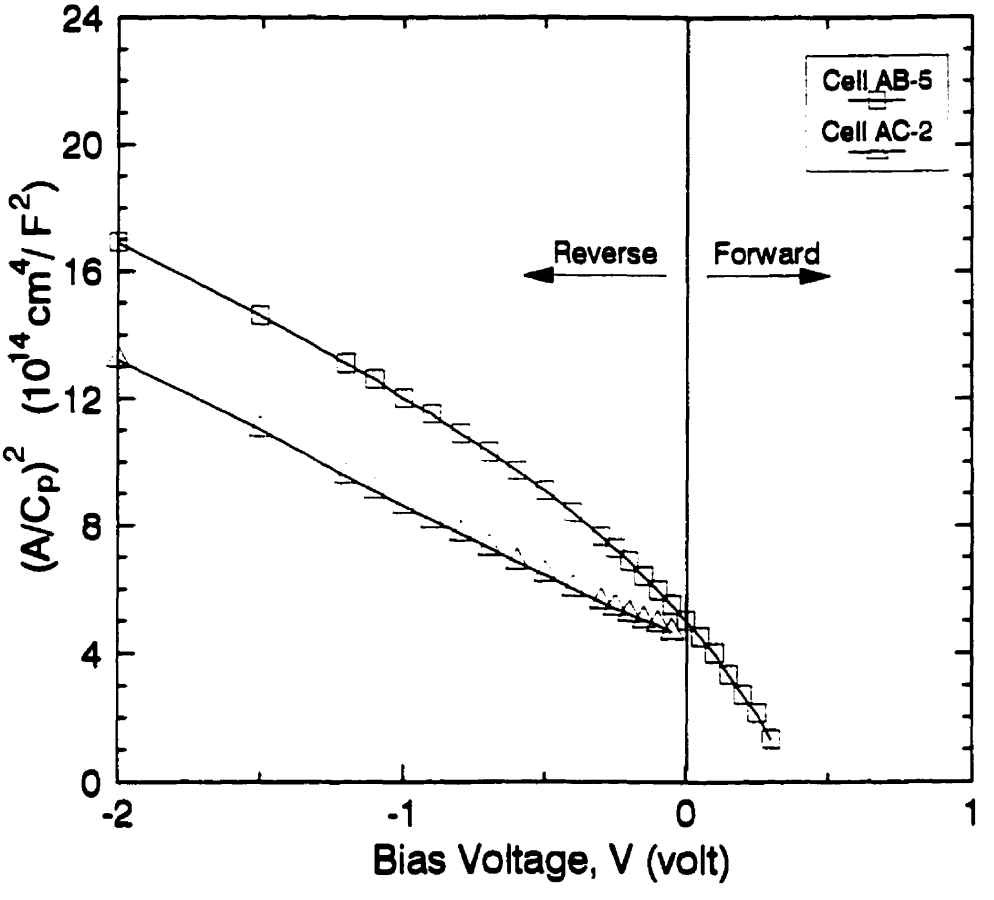


Figure 6.3 Mott-Schottky plot of $(A/C_p)^2$ against bias voltage (V) showing a comparison between annealed cell AB-5 and an earlier unannealed cell AC-2 at a frequency of 10 kHz.

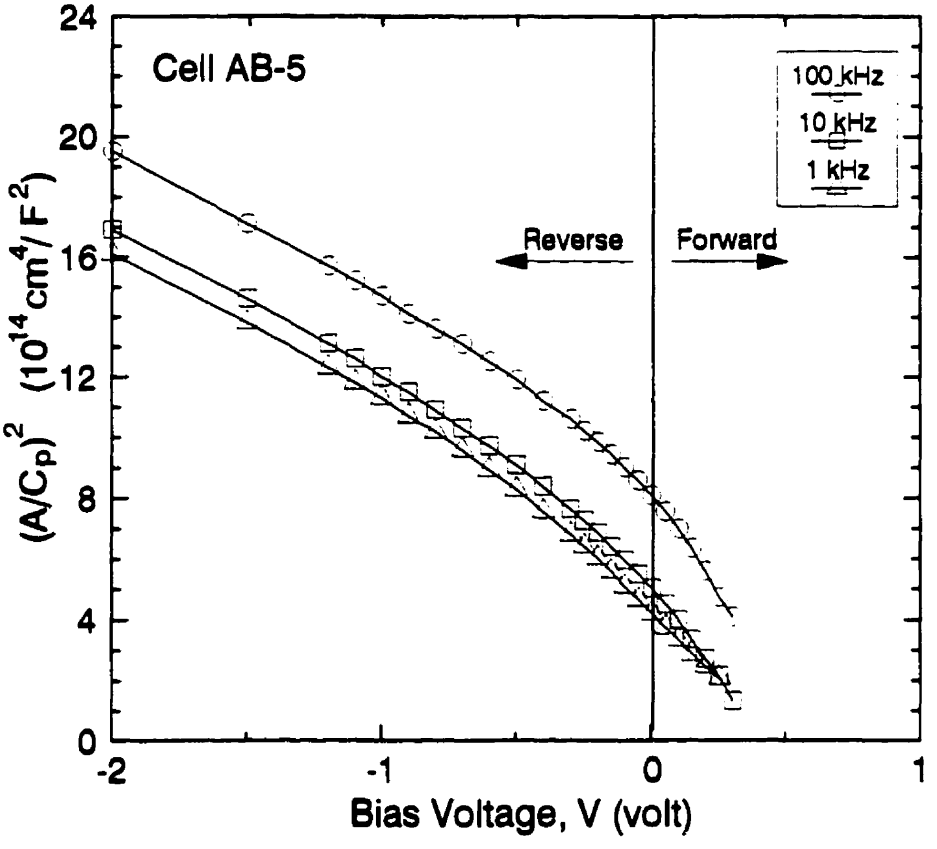


Figure 6.4 Mott-Schottky plot of $(A/C_p)^2$ against bias voltage (V) for cell AB-5 at three different frequencies.

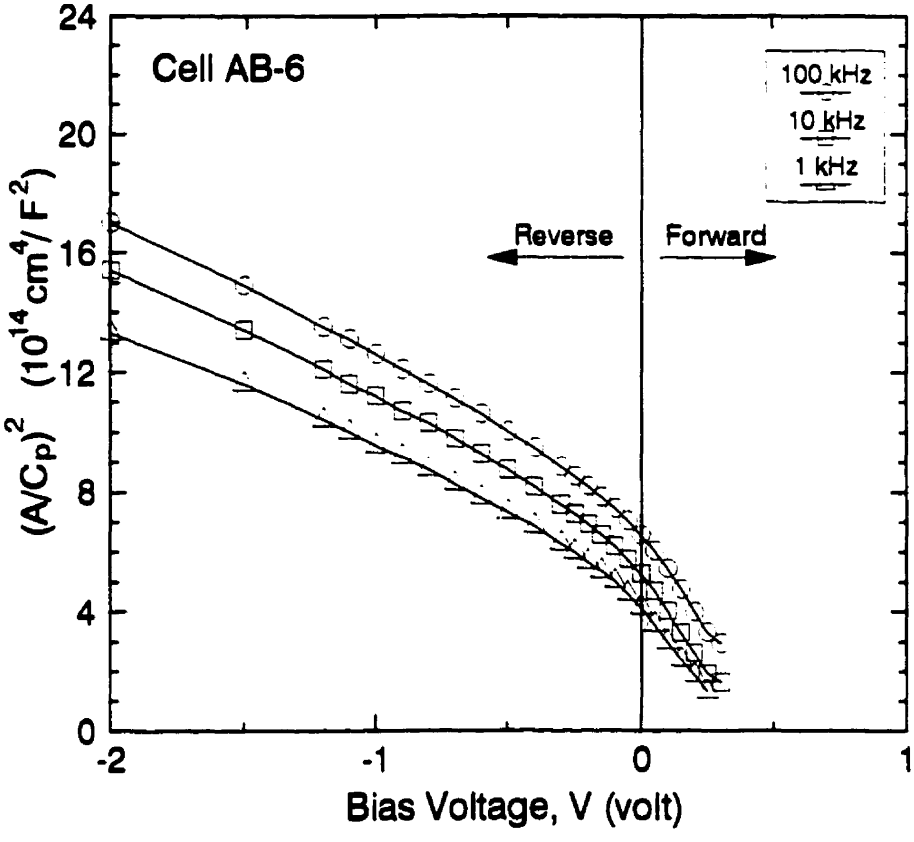


Figure 6.5 Mott-Schottky plot of $(A/C_p)^2$ against bias voltage (V) for cell AB-6 at three different frequencies.

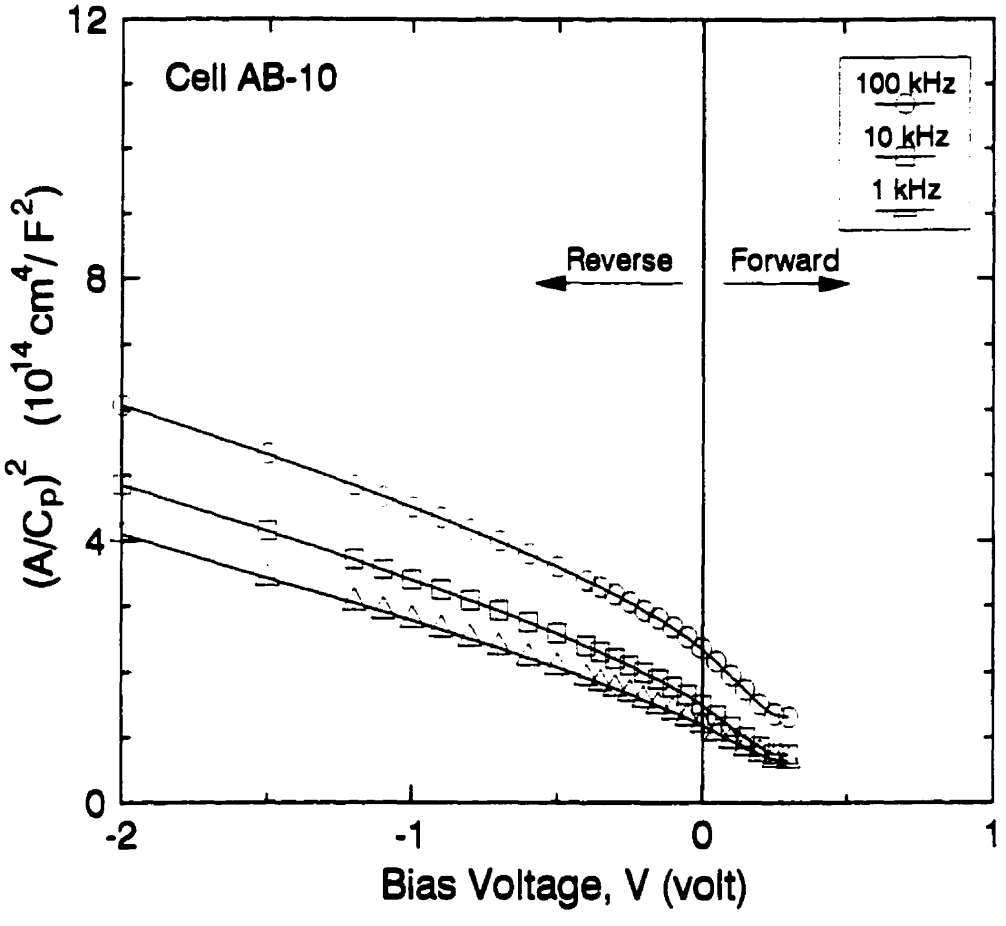


Figure 6.6 Mott-Schottky plot of $(A/C_p)^2$ against bias voltage (V) for cell AB-10 at three different frequencies.

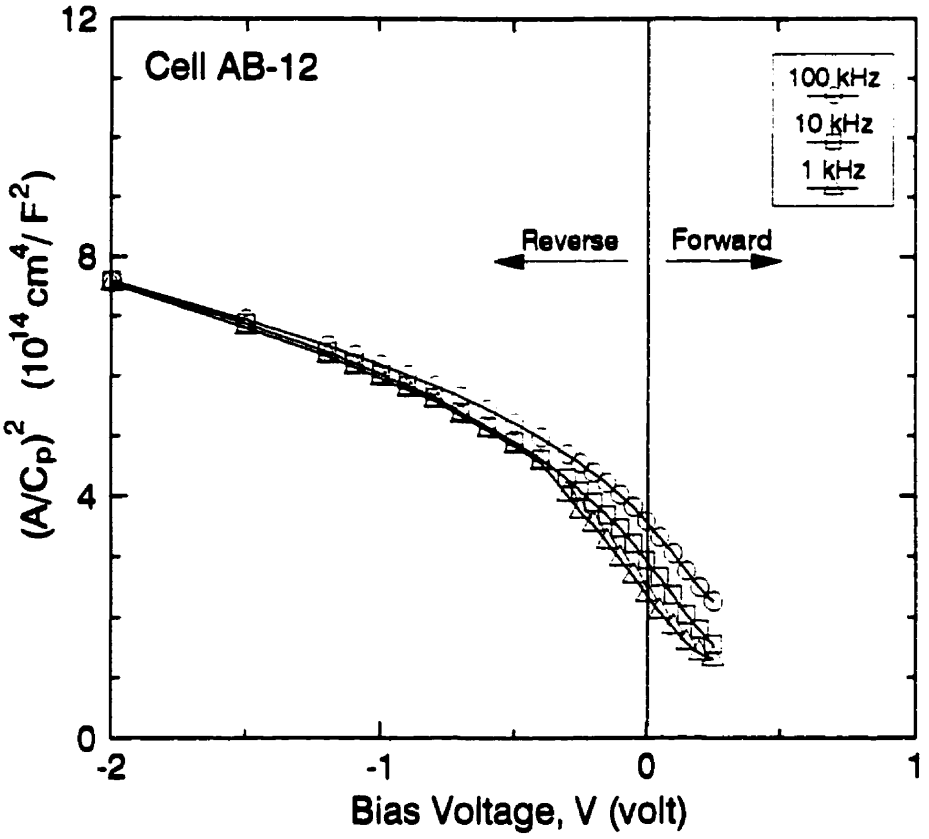


Figure 6.7 Mott-Schottky plot of $(A/C_p)^2$ against bias voltage (V) for cell AB-12 at three different frequencies.

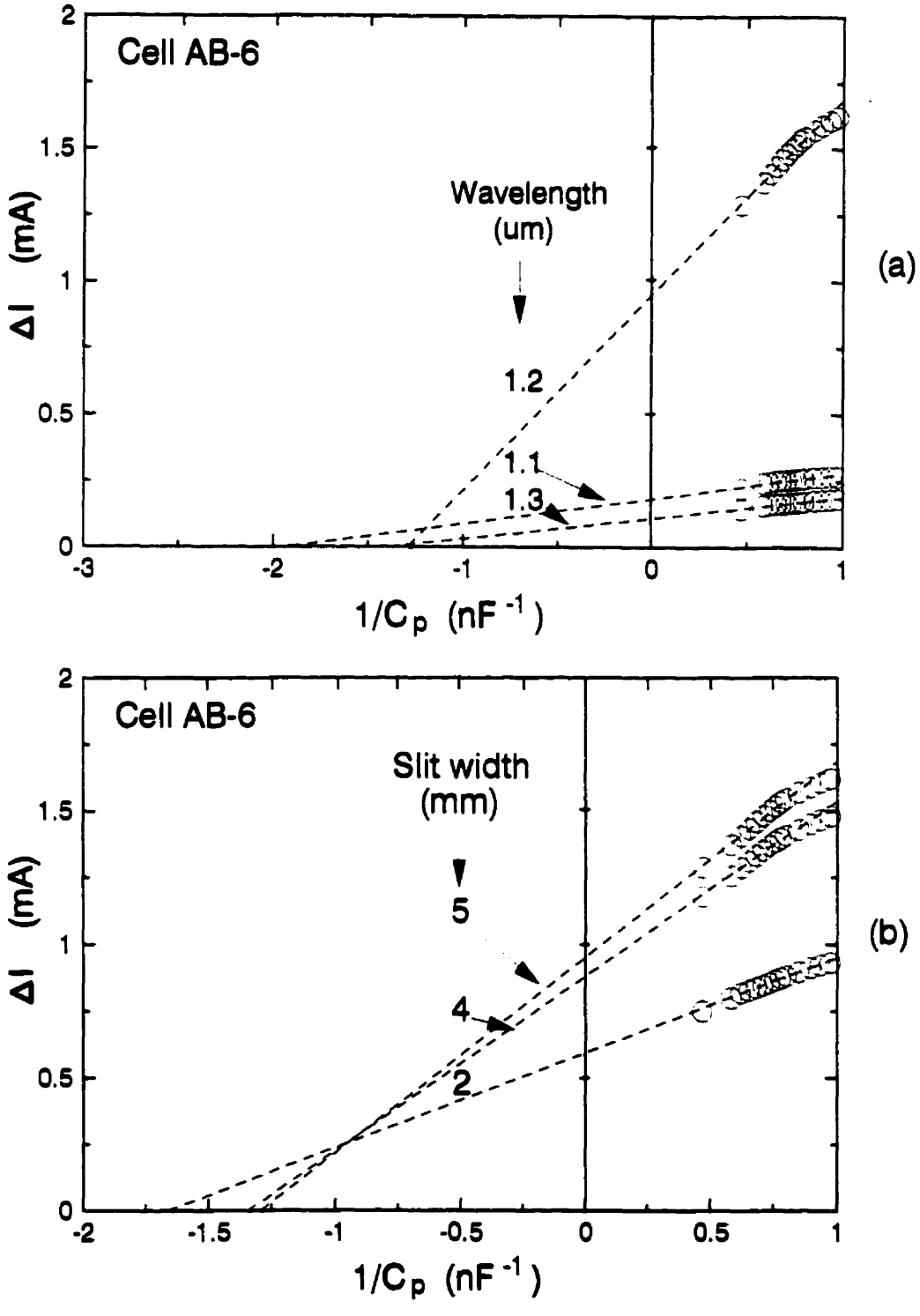


Figure 6.8 Plot of ΔI against $1/C_p$ for cell AB-6 with variation of (a) incident wavelength and (b) monochromator slit width. The broken lines were extrapolated from the linear portion of a straight line through the experimental points.

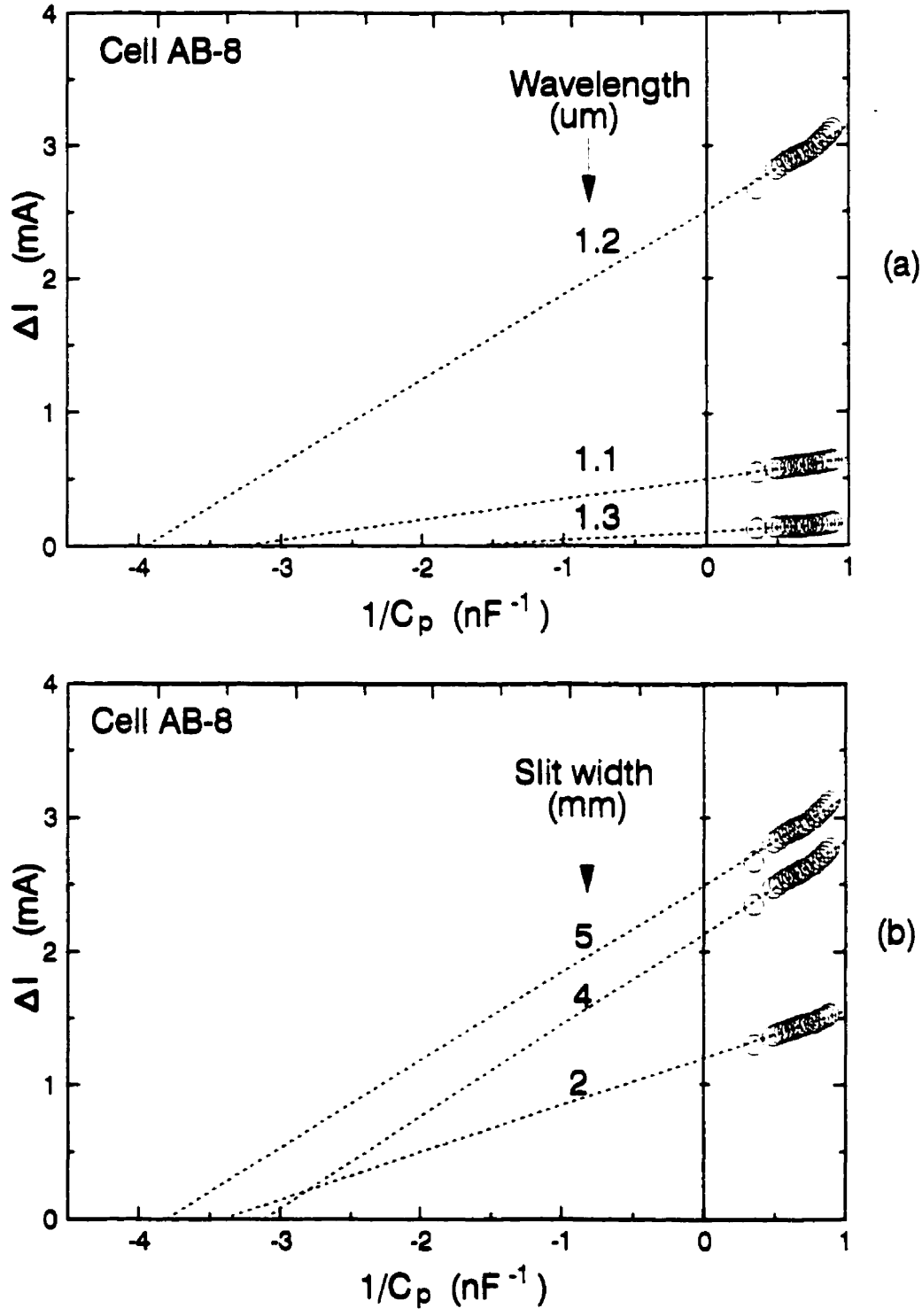


Figure 6.9 Plot of ΔI against $1/C_p$ for cell AB-8 with variation of (a) incident wavelength and (b) monochromator slit width. The broken lines were extrapolated from the linear portion of a straight line through the experimental points.

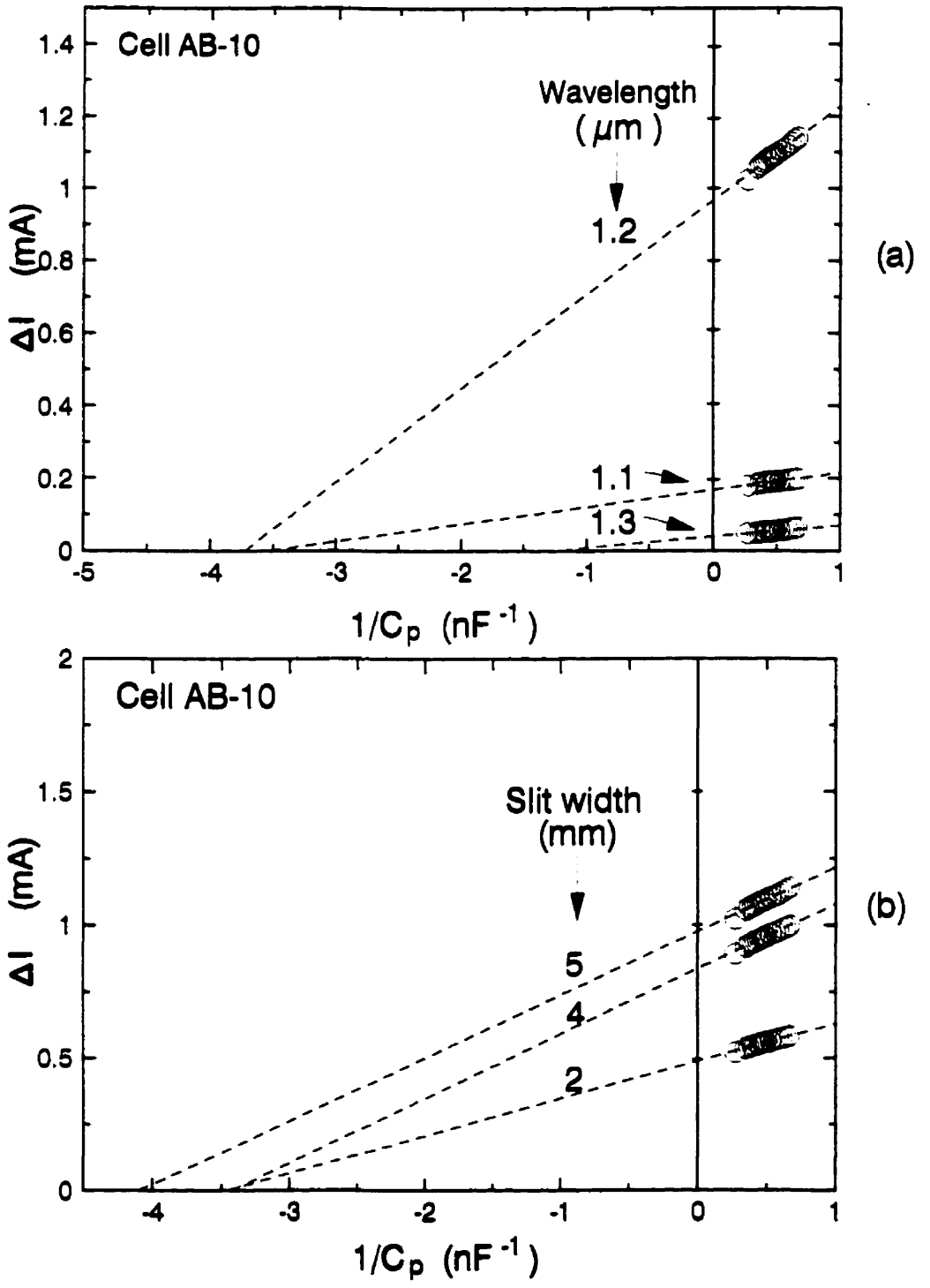


Figure 6.10 Plot of ΔI against $1/C_p$ for cell AB-10 with variation of (a) incident wavelength and (b) monochromator slit width. The broken lines were extrapolated from the linear portion of a straight line through the experimental points.

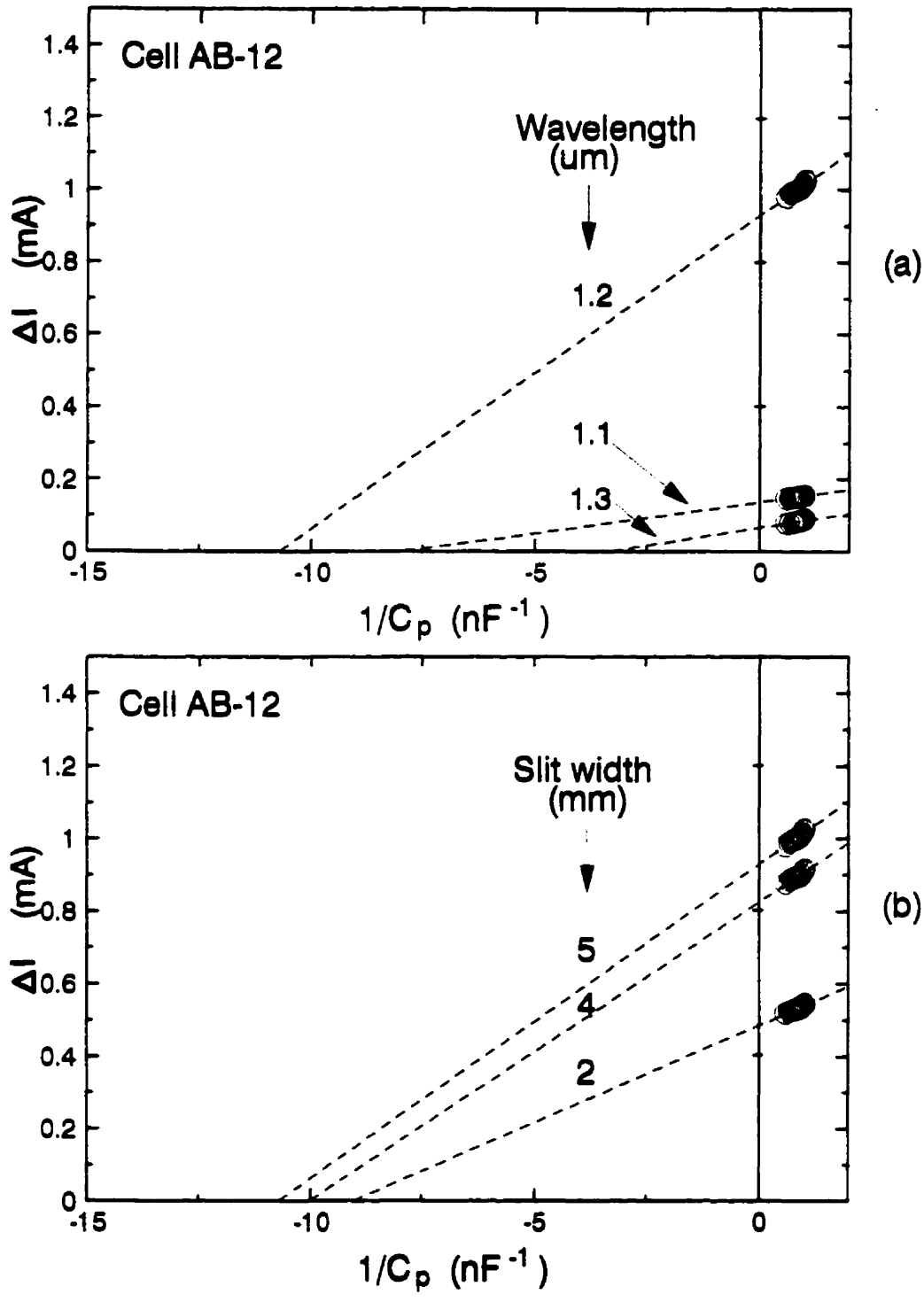


Figure 6.11 Plot of ΔI against $1/C_p$ for cell AB-12 with variation of (a) incident wavelength and (b) monochromator slit width. The broken lines were extrapolated from the linear portion of a straight line through the experimental points.

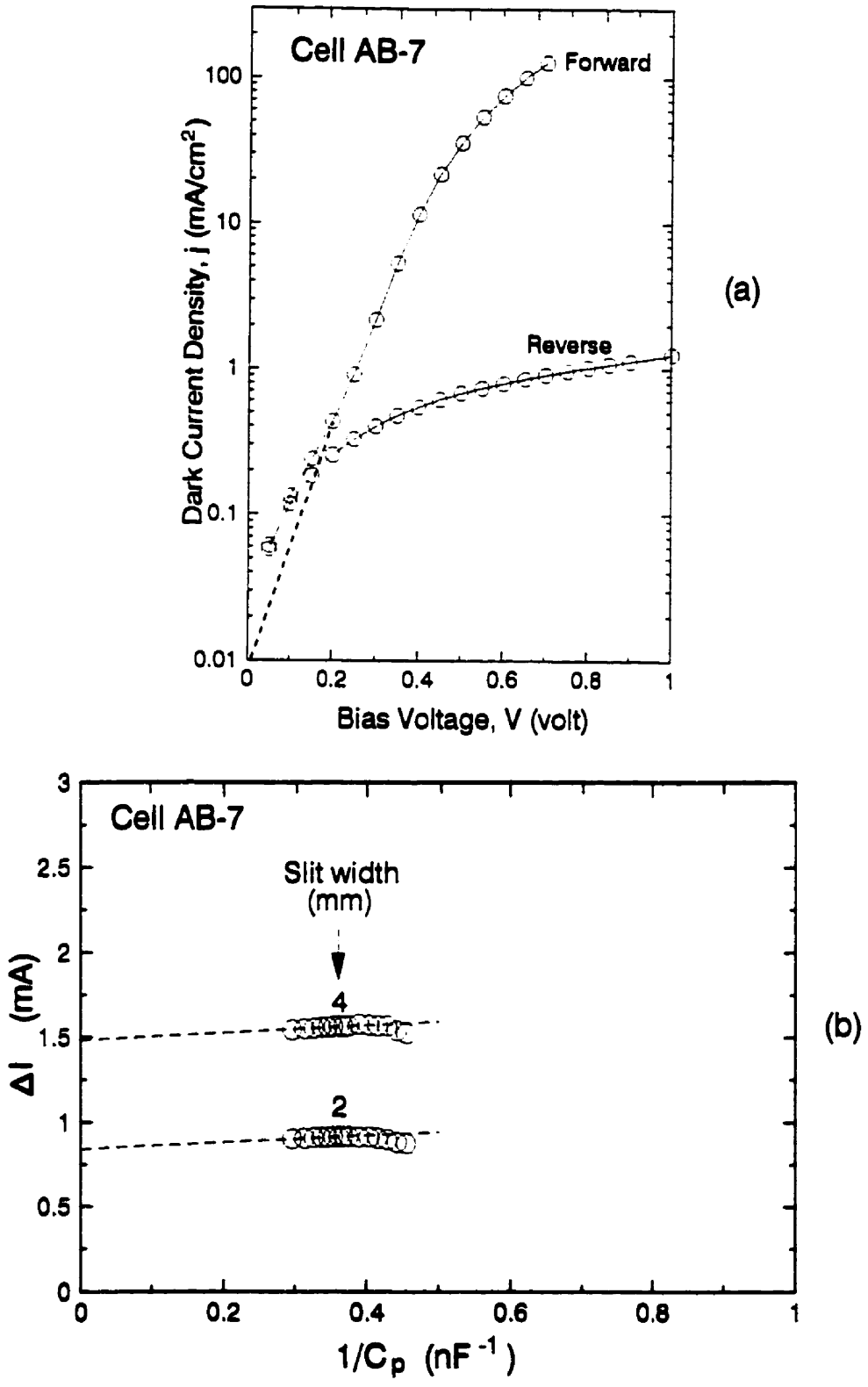


Figure 6.12 (a) Dark ln(j)-V for cell AB-7, showing excess shunt current above the extrapolated dashed line. (b) ΔI against $1/C_p$ plot for cell AB-7, indicating anomalous extrapolations arising from the excessive shunt current.

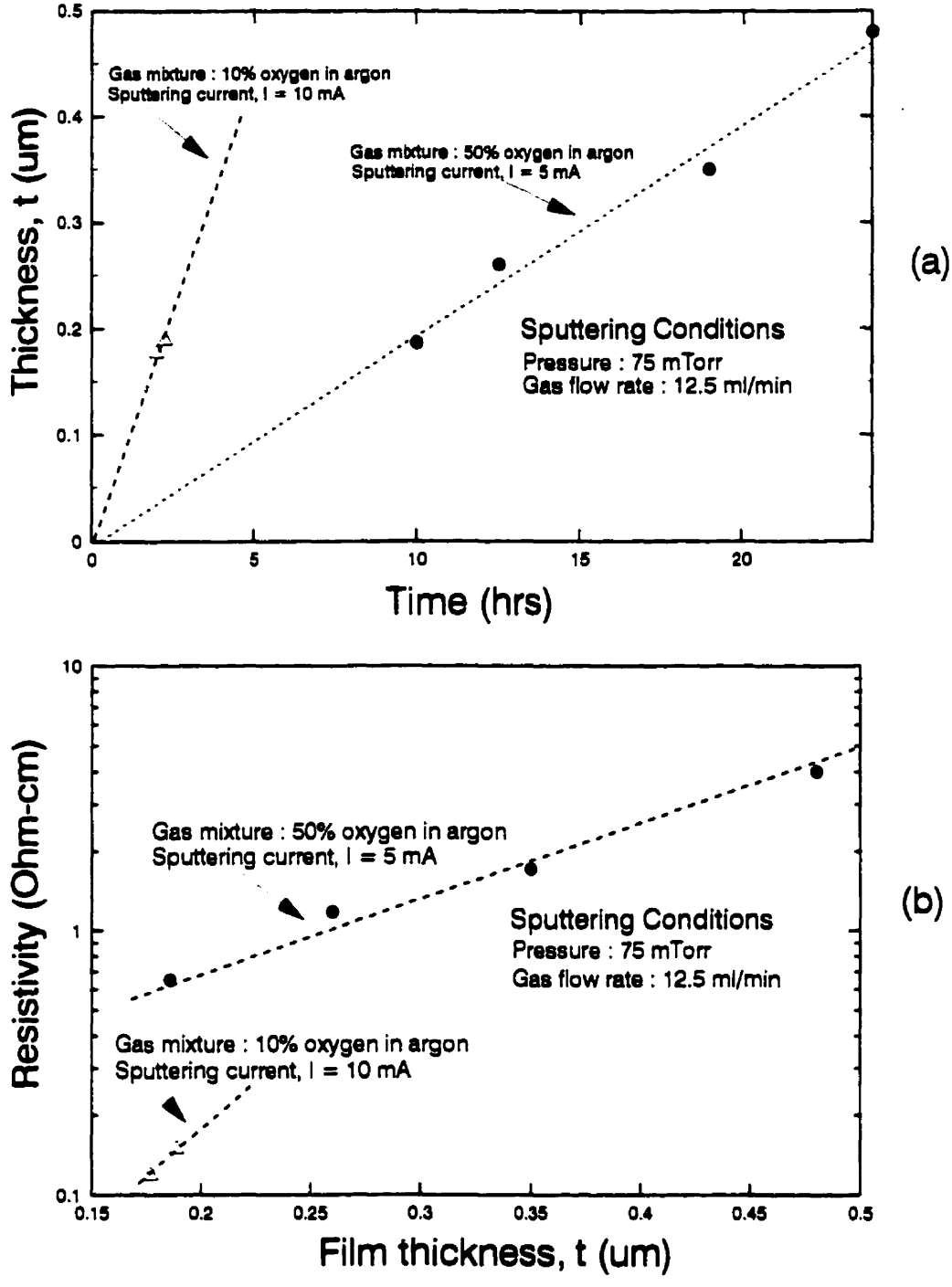


Figure 6.14 Plot of (a) variation of CdO film thickness (t) with sputtering time and (b) variation of resistivity with CdO film thickness (t), under the sputtering conditions indicated.

CHAPTER 7

ANALYSIS, DISCUSSION AND CONCLUSIONS

7.1 INTRODUCTION

While some discussion of the results was given at the end of chapters 5 and 6, a fuller more comprehensive discussion of the findings in the thesis are presented in this chapter, along with some further analyses of the measured data. Some suggestions for further studies are also offered at the end of this chapter.

7.2 CdO AND CdS DEPOSITION

At the start of this project, it was hoped that a very high resistance initial layer of CdO could be deposited in a $CuInSe_2$/CdO cell by dc reactive sputtering at a very low deposition rate. Such a layer, immediately adjacent to the $CuInSe_2$ surface, could potentially yield high junction integrity, with a high shunt resistance. This layer could then be followed with a second low resistivity CdO layer to reduce series resistance to the contacts. However, this was not to be. Very low deposition rates were, indeed, obtained using a low sputtering current, a high gas pressure and a high oxygen content but, when the films were sufficiently thick to be continuous, the resistivity was not as high as expected. The increases in resistivity found were about an order of magnitude but this was not enough for a high resistivity layer to be effective in a cell. Nevertheless, in this work, at least the trends were confirmed that

the CdO thickness increases linearly with sputtering time and that the resistivity increases with decrease of sputtering current and increase of both gas pressure and its oxygen content. As a result of these studies, work was done to introduce a high resistivity layer of CdS adjacent to the $CuInSe_2$ by a dipping process, already described in the literature. This CdS film, as an intermediate layer, would not only improve junction integrity but would act as a lattice matching agent to the $CuInSe_2$, with a lattice mismatch of only about 1 %. For these reasons CdS is already the favoured n-type partner to $CuInSe_2$, as reported in the extensive literature on chalcopyrite thin film solar cells. The work in this thesis has indeed confirmed that good cells can result with a CdS interlayer between the $CuInSe_2$ and the CdO window layer. However, the studies have also demonstrated the surprising result that the same level of conversion efficiency can be obtained even in a cell without the CdS interlayer.

7.3 SMALL EFFECT OF WINDOW LAYER LATTICE MISMATCH

The surprising insensitivity of the cell performance to the large lattice mismatch in a $CuInSe_2$/CdO cell suggests that the active junction lies within the substrate at a distance far enough away from the interface of the two semiconductors that carrier recombination does not play a dominant role [7.1]. However, the dark ideality factors in these cells were always greater than 2 and, while the exploratory EBIC tests did not confirm a junction clearly within the $CuInSe_2$, they did not rule it out either because a cell without the CdS interlayer was not successfully examined by EBIC. An alternative but possible explanation arises from the diffraction work of Shukri and Champness [1.5], in which CdO was deposited on a cleaved {112} plane of $CuInSe_2$. They found evidence of some partial orientation of the CdO grains

with their <111> directions parallel to the [221] direction of the $CuInSe_2$ substrate. Thus, for the {111} and {112} planes of CdO and $CuInSe_2$ respectively, the $a\sqrt{3}$ distance would be the relevant lattice parameter for comparison, so that the bulk lattice mismatch in **a** of about 23% would still apply. However, it is possible that some surface lattice reconstruction could occur, reducing the lattice mismatch, so that partial epitaxy could take place.

7.4 SERIES AND SHUNT RESISTANCES

Values of series (R_s) and shunt (R_{sh}) resistances can be calculated from the analysis given in chapter 2, arising from the cell equivalent circuit in Figure 2.2. For four of the cells, AB-5, 7, 10, and 12, values of j_o were obtained from extrapolating from the linear regions of their dark ln(j)-V plots to the ordinate. Gradients were also determined from the illuminated j-V plots of these cells at V=0 (short circuit) and at I=0 (open circuit). Then, using equations (2.8A) and (2.9) of chapter 2, values of R_{sh} and R_s were calculated assuming an ideality factor of n=2 in all cases. These values, expressed as area-resistances, are listed in columns 4 and 5 of Table II.

Table II

Cell Number		j_{sc} (mA/cm^2)	V_{oc} (volt)	R_{sh} (Ω-cm^2)	R_s (Ω-cm^2)
Cells without CdS	AB-5	29	0.42	54	3.5
	AB-12	30	0.41	1230	2.0
Cells with CdS	AB-7	34	0.41	240	0.4
	AB-10	33	0.38	155	1.1

The table indicates lower R_s values for the cells with the CdS interlayer present than with it absent and a higher R_{sh} value for cell AB-12 (without-CdS) than the other cells. Thus, except for the R_{sh} value for AB-5, an early fabricated device, the trend is lower resistances for the devices with the CdS layer present, a result opposite to what might have been expected. It should be remembered, however, that these are *illuminated* resistance values and that the trend may be a result of a greater number of photogenerated carriers when the interlayer is present. Alternatively, the abrasive polishing, in this case, may have played a role. It should also be pointed out here that the circuit model of Figure 2.2 is assumed to be an accurate representation of a cell, whereas we know that the photogenerated source current density (j_{ph}) is not exactly constant, since j_{ph} decreases with decrease of depletion width as the forward voltage is increased. This would apparently affect the slope $(dI/dV)_{sc}$ and thus, in turn, alter the calculated value of R_{sh}. Furthermore, if the measured values of n, determined from the slopes of the dark ln(j)-V plots, were used, the values above 2 would have yielded calculated negative values of R_s. Accordingly, the absolute values of R_s and R_{sh} in Table II should be regarded with some reserve.

7.5 DIFFERENCES IN V_{oc} AND j_{sc}

The cells without the CdS interlayer were found to have a slightly higher V_{oc} and a slightly lower j_{sc} than the devices with the interlayer. The higher V_{oc} could be due to a higher built-in voltage V_{bi} arising from a lower work function (ie. lower χ_n and δ_n from equation 2.10) in CdO. However, this would imply a larger value of the extrapolated intercept in the

Mott-Schottky plots of the $CuInSe_2$/CdO cells, which was not observed, at least at the frequency of 10 kHz. A larger energy gap for CdS would explain the slightly greater photoresponse at short wavelengths and the larger j_{sc} but not the smaller V_{oc}. However, the literature indicates no significant difference between the direct energy gaps of CdO and CdS, with a value of about 2.4 eV for both. Furthermore, an explanation of a difference of electron affinities assumes heterojunctions and is thus contrary to the earlier suggestion of a buried homojunction.

7.6 ACTION OF PRE-ANNEALING OF SUBSTRATE

From the difference in the Mott-Schottky plots between cells with and without the pre-annealing of the $CuInSe_2$ substrates prior to CdS or CdO deposition, it is deduced that the heat-treatment causes a decrease in the accepter concentration close to the surface, where the junction occurs. This could be caused by the partial out-diffusion of selenium, since a deficiency of this element acts as a donor to compensate the acceptors already present. Such a diffusion would be expected to yield a junction nearer in profile to linearly-graded than abrupt. In a linearly graded case, a straight-line variation would be expected on a plot of $(A/C_p)^3$ versus voltage. Figures 7.1 through 7.4 show such plots for cells AB-5, 6, 10 and 12, where except for cell AB-12, the lines for the frequencies of 10 and 100 kHz are much less curved than those on the corresponding $(A/C_p)^2$ versus voltage plots. Thus, this is consistent with a graded, rather than an abrupt junction, which could also result from in-diffusion of cadmium from the CdO or CdS layer, since Cd is known to be a donor in $CuInSe_2$.

7.7 ELECTRON DIFFUSION LENGTH ESTIMATES

The work done with the photocurrent-capacitance method indicates that this is a convenient non-destructive means of estimating the minority carrier diffusion lengths in the cells, provided the shunt current is sufficiently small. For the cleaved $CuInSe_2$ devices, L_n was estimated to be about 3 μm and in the abrasively polished samples about half this value. However, this difference was not reflected in a higher j_{ph} value in the former case. With further adjustment of the measuring conditions, such as chopping rate and photocurrent wave shape, this method should be capable of improved accuracy. If an electron mobility (μ_n) in the $CuInSe_2$ of 240 $cm^2volt^{-1}sec^{-1}$ is assumed, the Einstein relation gives for the diffusion coefficient $D_n = (kT/q)\mu_n = 6\ cm^2/sec$. With the electron diffusion length L_n given by $L_n = \sqrt{(D_n\tau_n)}$, the lifetime τ_n is therefore estimated to be of the order of 10^{-8} second.

7.8 FUTURE WORK

Arising from the results of the work of this thesis and from the experience of the author, work in the future should be done along the following lines:

1. In respect of cell fabrication, a critical step was the masking process to define the CdO area. An improved set of masks therefore should be employed in future work.

2. Mounting the substrate with a soldered wire for the back contact on the aluminum stud using an epoxy resin is relatively inefficient. A method of "pasting" the sample on the

aluminum stud (eg. using colloidal silver or silver paste) and having the aluminum itself serve a two- fold purpose namely, support the sample and provide a back electrical contact. should be incorporated in future work.

3. A wider band-gap window material should be employed if better overall cell performance is to be attained. Incorporating ZnO in future devices may be beneficial judging from the experience elsewhere in thin film $CuInSe_2$ cells.

4. Work is needed to optimize the parameters involved in the photocurrent-capacitance method of estimating diffusion length. This involves, for instance, examining the photocurrent-time wave shape with variation of chopping frequency and phase.

5. A more comprehensive electron beam induced current (EBIC) study should be done on $CuInSe_2$/CdO samples in order to test the hypothesis of a "buried" homojunction. Here, a difficulty to be overcome is developing a technique for sectioning a cell in a manner suitable for EBIC study.

6. In this work, heat treatment of the CdS after the dipping process was not performed. This step has been shown, by the extensive literature, to be beneficial to improve thin film solar cell performance. A heat treatment of the substrates after the CdS deposition should be investigated in future devices.

7. Post-fabrication treatments of the cells should be explored, such as "electrical forming" by applying a reverse voltage to a device over a period of time, and also having a modest heat treatment. Great care, however, is needed in these procedures to avoid destruction of the cells.

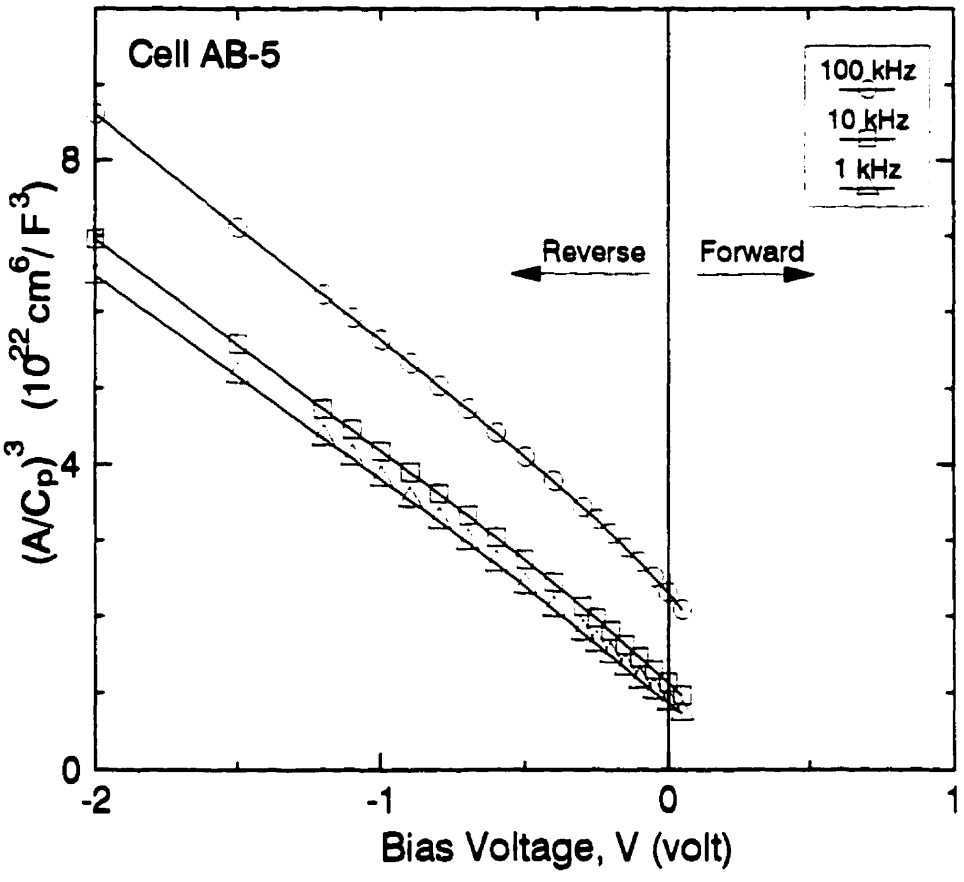


Figure 7.1 Plot of $(A/C_p)^3$ against bias voltage (V) for cell AB-5 at three different frequencies.

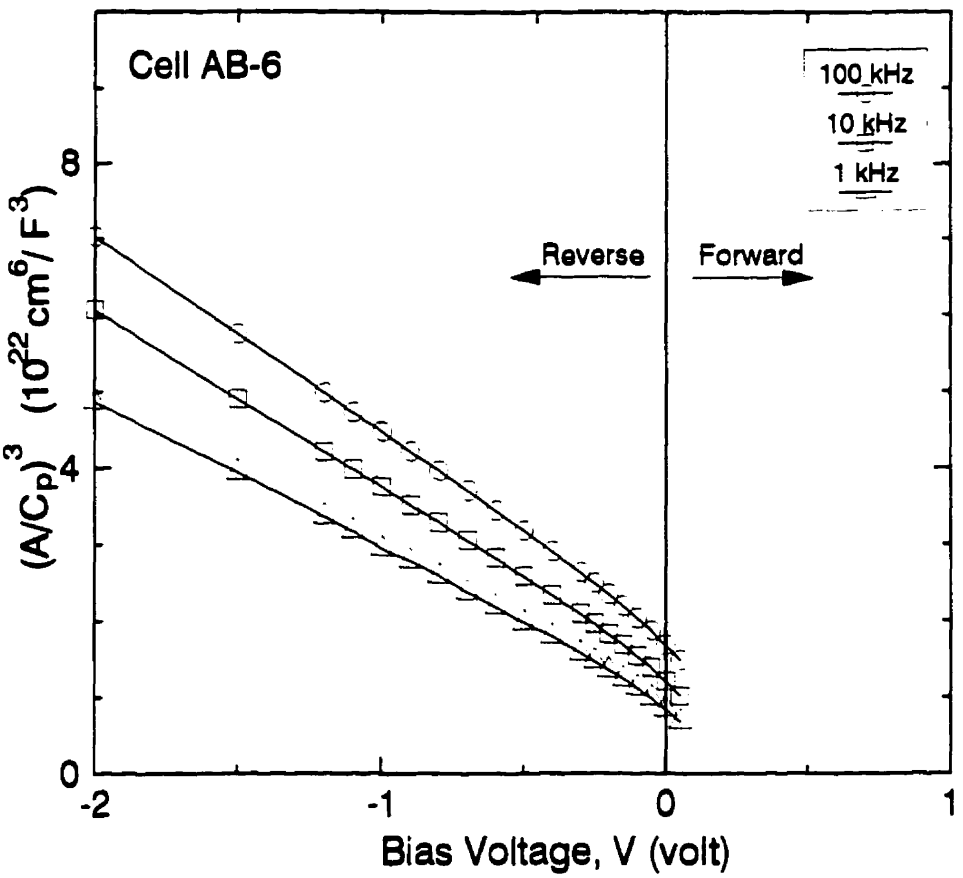


Figure 7.2 Plot of $(A/C_p)^3$ against bias voltage (V) for cell AB-6 at three different frequencies.

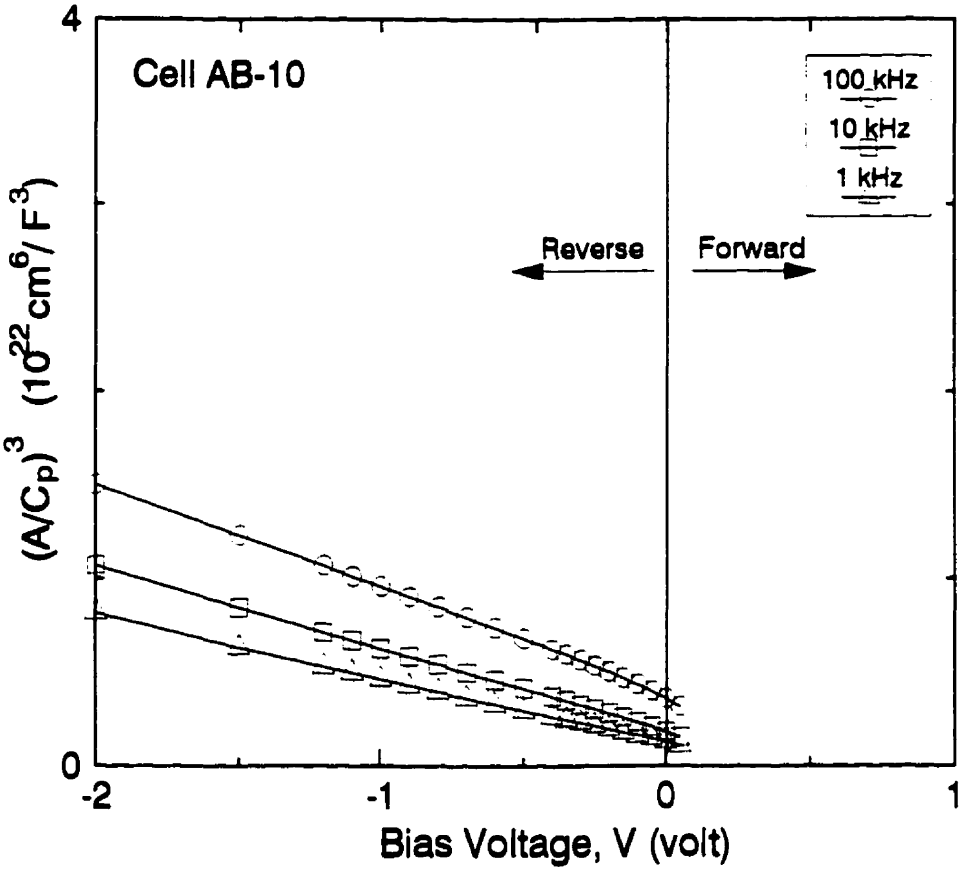


Figure 7.3 Plot of $(A/C_p)^3$ against bias voltage (V) for cell AB-10 at three different frequencies.

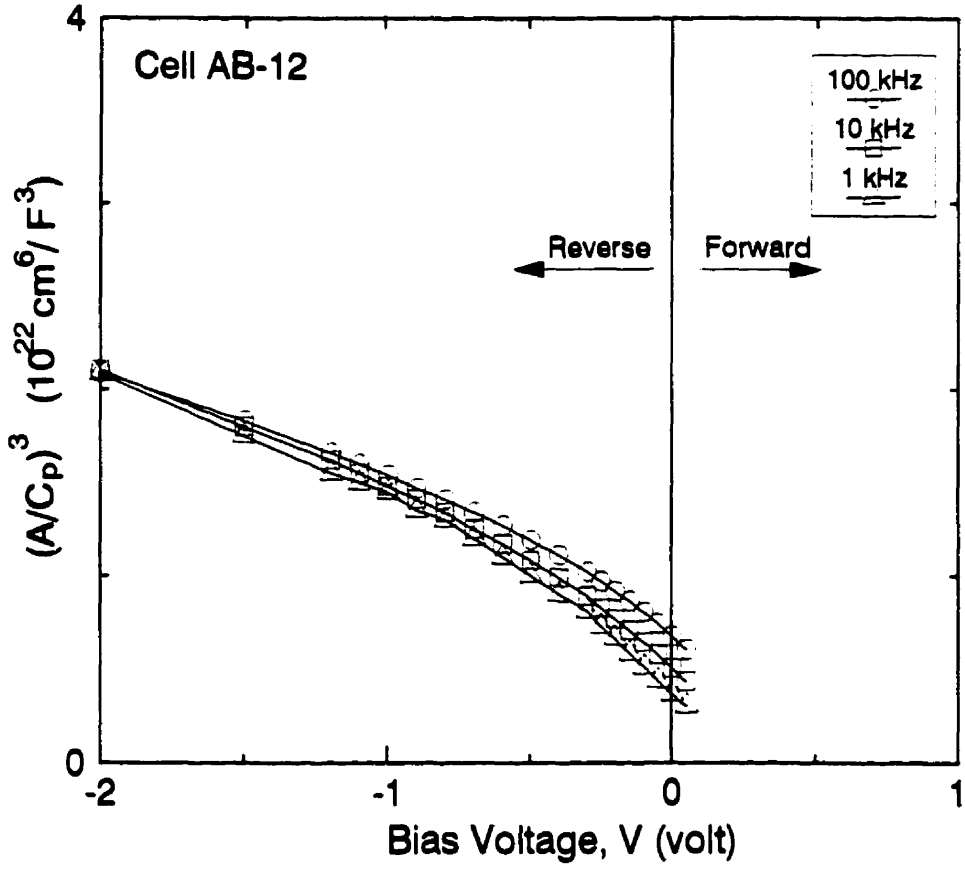


Figure 7.4 Plot of $(A/C_p)^3$ against bias voltage (V) for cell AB-12 at three different frequencies.

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APPENDIX I

BRIEF DESCRIPTION OF BRIDGMAN GROWTH OF $CuInSe_2$ MONOCRYSTALS

A brief description of the crystal growth procedure using the boron nitride (BN) coating pioneered in this laboratory (Shukri [1.3]) is presented here.

The crystal growth of $CuInSe_2$ in this work was carried out by a vertical Bridgman method, using a resistively heated two-zone furnace. A schematic diagram of the setup is shown in Figure 3.1 of reference [1.3]. The $CuInSe_2$ charge synthesis and crystal growth were carried out in the same ampoule. The ampoule was made from a quartz tube, having an inner diameter of 12 mm and an outer diameter of 16 mm. The ampoule was shaped, using an oxygen-hydrogen flame, from one end to obtain a pointed V-shaped tip (to facilitate nucleation during the early stages of growth). The quartz tube, with only one end open, was cleaned with a mixture of HNO_3 and HCl (1:1 by volume) for a period of about 24 hours and then rinsed thoroughly in de-ionized (DI) water. The ampoule was then soaked in acetone for an hour to remove any organic contaminants. Finally, the ampoule was rinsed again with DI water and dried gently with the flame. Next, the ampoule was coated with BN. It was found by Shukri [1.3] that the BN coating was an important step in the growth of adhesion- and void-free $CuInSe_2$ ingots. A more descriptive treatment on the effect of the BN coating is described in the Ph.D. thesis of Z. A. Shukri of this laboratory [1.3]. The BN used was in the form of a slurry. A small quantity of the BN source was thoroughly mixed with 10 to 20 ml of acetone to create a suspension. The mixture was then transferred to the ampoule and given a manual agitation for about 2 to 3 minutes. This resulted in an ampoule wall coated with BN particles. The excess quantity of the suspension was poured out of the ampoule. The coating was made more uniform by spreading it out with a special brush until the desired thickness was obtained on the wall. The coating area was localized at the bottom of the ampoule by rinsing the unwanted coating with DI water. After this, the ampoule was gently heated between 80 and a 100°C in a small oven furnace to drive out any residual acetone. At this stage the BN was loosely bound to the quartz ampoule, and was hardened by intense heating (flaming) of the ampoule. Residual BN particles were removed from the ampoule after a final rinse in DI water. Now, the charge, consisting of stoichiometric starting proportions of copper, indium and selenium (all with a nominal purity of 99.999%) was introduced into the ampoule. All the starting elements (copper, indium and selenium) were weighed out from a pre-etched supply. Having transferred the charge to the BN-coated ampoule, the ampoule was attached (in the vertical position) to a vacuum pumping system. With the ampoule in place, the vacuum system was pumped down to a pressure of about 4×10^{-7} for 2 to 3 hours. Using an oxygen-hydrogen flame, the ampoule was sealed from a position about 10 cm from the elemental charge pellets in order to avoid unwanted heating. However, the tip of the ampoule was kept cool with a water-soaked cloth. The sealing process was done very carefully in order to prevent any cracking of the quartz. With the influence of the vacuum, the quartz tube collapsed and formed a sealed neck. After sealing,

the ampoule, some 15-20 cm in length, was allowed to cool down. The charged and sealed ampoule was now ready for the initial reaction. It was placed inside a brick furnace where the temperature was slowly raised to 300°C. This initial reaction allowed the exothermic reaction between the indium and selenium to take place at approximately 220°C. To ensure a complete reaction, the temperature was maintained at 300°C for some 24 hours. At this stage, the reactants were only the indium and the selenium, while the copper remained in pellet form. Next, the ampoule was transferred to the top zone of the vertical growth furnace where the remainder of the reaction was carried out. The ampoule was first attached from its top end to a vertical quartz rod about 60cm in length. Then, the rod was connected to the mechanical lowering mechanism of the assembly and, with the furnace turned off, the ampoule was positioned in the center of the top zone. Next, the temperature was set to 300°C and the furnace was allowed to stabilize for 1 hour when the temperature was raised to 1100°C (above the melting point of $CuInSe_2$) at a rate of about 5°C/min. The mixture was temperature-soaked at 1100°C for 48 hours and was given a thorough manual agitation several times during this period.

Following the 48-hour temperature-soaking and reaction of the charge, the temperature of the furnace was lowered to 1025°C and the ampoule, using the motorized lowering mechanism, was lowered to the bottom zone of the furnace (not heated) at a rate of approximately 5 mm/hr. The growth was continued for 48 hours until the ingot was completely solidified and was well into the lower cooler zone of the furnace. At that time, the top zone temperature was reduced to that of the lower zone at a rate of approximately 30°C per hour. Finally, the ampoule was carefully broken from the top (opposite end of the tip) and the loose $CuInSe_2$ ingot was extracted.

APPENDIX II

BRIEF TREATMENT OF THE PHOTOCURRENT-CAPACITANCE METHOD

The photocurrent-capacitance method is a relatively simple way of estimating the minority carrier diffusion length in the semiconductor absorber layer of a photovoltaic Schottky junction. This method has been used by Smith and Abbot [A.1] in GaP cells, by Yong and Rowland [A.2] and by Dorantes-Davila, Lastras-Martinez and Raccah [A.3] in GaAs cells. It has also been used in semiconductor-electrolyte cells by Tyagai for CdS [A.4] and by Lastras-Martinez et al for CdTe [A.5]. It has also been applied to Se-CdO cells by Chan and Champness [4.1] [4.2] [4.3].

The basis of the method is as follows. Consider a reverse bias applied to a metal p-type semiconductor junction, where the metal is a film thin enough to transmit light through it. Suppose this cell is illuminated with monochromatic light such that $\alpha_p W << 1$, where α_p is the optical absorption coefficient of the semiconductor, a condition corresponding to light penetrating well beyond the width of the depletion layer W. In this case, the photogenerated current, I_{ph}, is given by:

$$I_{ph} = K_I (W + L_n) \quad . \tag{A1}$$

where L_n is the diffusion length of the electrons in the p-type semiconductor and K_I is a coefficient independent of the applied bias. An ideal cell may be considered to be a current generator, giving photocurrent I_{ph}, in parallel with a diode, carrying a current I_{diode}. If an external reverse bias V_R is applied to the device under illumination, the net current I_L is:

$$I_L = I_{ph} - I_{diode} = I_{ph} - I_o\left(e^{\left(-\frac{qV_R}{kT}\right)} - 1\right) \quad . \tag{A2}$$

which, if $V_R >> kT/q$, becomes:

$$I_L = I_{ph} + I_o \quad . \tag{A3}$$

Here, k is Planck's constant, T is the absolute temperature and q is the electronic charge. In darkness, I_{ph} is zero, so that the dark current I_D is just $I_D = I_o$. Hence, the illuminated-to-dark current change ΔI is:

$$\Delta I = I_L - I_D = I_{ph} \quad . \tag{A4}$$

so that equation A1 can be re-written as:

$$\Delta I = K_1 (W + L_n) \qquad \text{(A5)}$$

The capacitance of the Schottky junction (C_j) is given by $C_j = (\epsilon_o \epsilon_r A)/W$, where ϵ_r is the relative dielectric constant of the semiconductor, ϵ_o is the permittivity of a vacuum and A is the area of the junction. Substitution for W into equation A5 yields:

$$\Delta I = K_2 \left(\frac{1}{C_j} + \frac{L_n}{\epsilon_o \epsilon_r A}\right) \qquad \text{(A6)}$$

where $K_2 = K_1 \epsilon_o \epsilon_r A$.
From equation A6, it is seen that a plot of ΔI against $1/C_j$, as the reverse bias is varied, should yield a straight line, with an extrapolated intercept on the $1/C_j$ axis of $-L_n/(\epsilon_o \epsilon_r A)$. From this, the diffusion length L_n can be determined. Linearity would not be expected at low reverse and at forward bias due to the violation of the inequality $V_R >> kT/q$ and the deviation from the depletion approximation and ideal diode behaviour.

Apart from the application of this method to Schottky junctions, it can also be applied to pn homojunctions and heterojunctions as in the case of the cells in this work. Here, one must consider the collection of photogenerated carriers, not only in the depletion region and the p-type semiconductor but also in the n-type region close to the junction. However, if this layer acts as a window layer, it is possible that this contribution could be small and, therefore, may be neglected with a small error.

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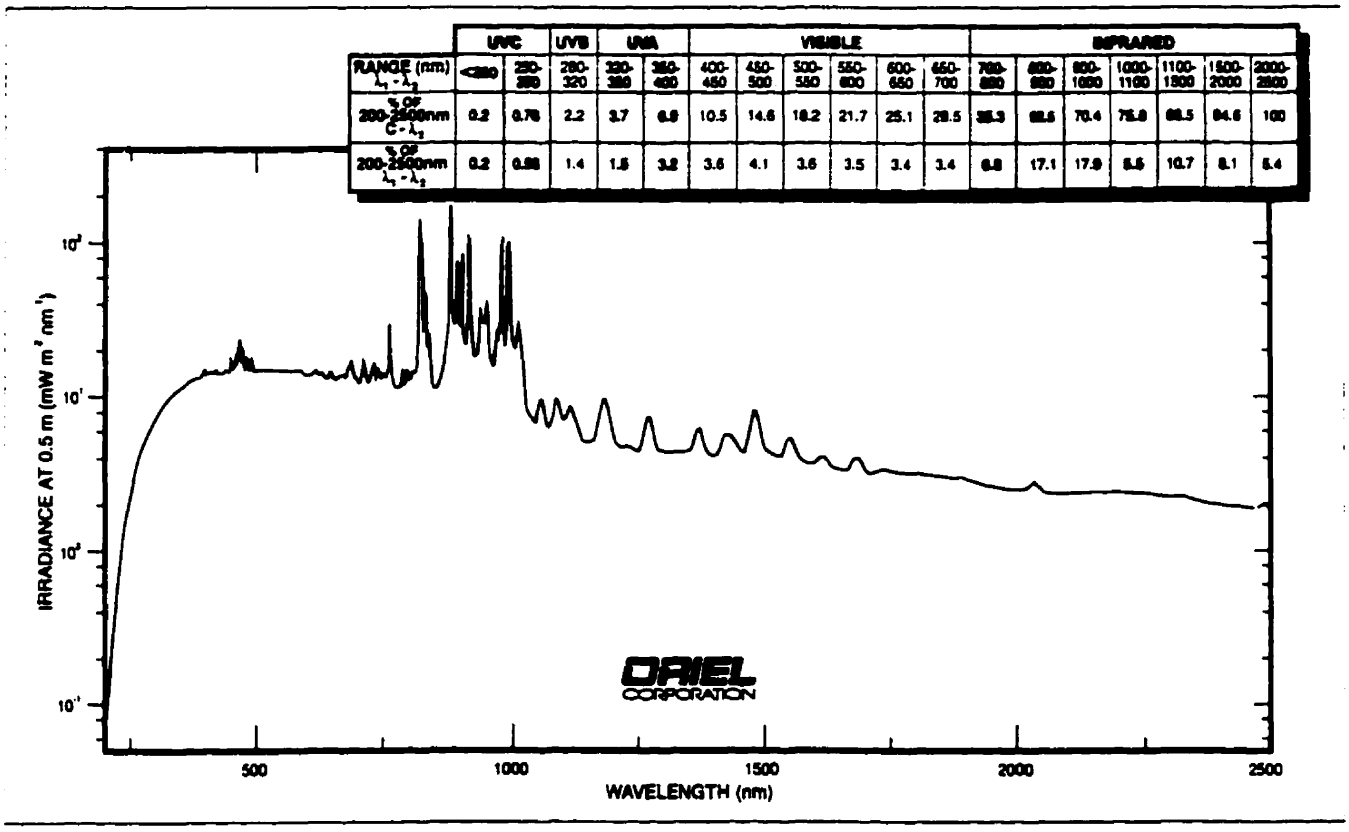
APPENDIX III

SPECTRAL IRRADIANCE DATA FOR SOLAR SIMULATOR ARC LAMP

(Xe 150W Arc Lamp)



Spectral irradiance versus wavelength (250-2500 nm) plot for the solar simulator 150 W Xe Arc Lamp (After ORIEL Corporation Product Catalog).