Thin Film Transistors with Chemically Deposited Active Channels

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Abstract

Using CdSe and CdS thin films as an active layer prepared by chemical bath deposition method (CBD), thin film transistors (TFT) have been fabricated and studied. There are two fabrication processes developed in this work for TFTs dependent on the substrates used. A procedure for the fabrication of TFTs on Si substrates and a procedure for devices on glass substrates will be presented. Both procedures are designed for the fabrication of TFTs with an inverted gate-staggered electrode configuration. The chemical bath deposition process developed has yielded CdSe-TFTs and CdS-TFTs on thermally grown oxide/Si substrate with very good performance. Typical values of mobility for those TFTs are about 10 $cm^2/V\text{-}s$ for CdSe-TFTs and 1 $cm^2/V\text{-}s$ for CdS-TFTs with W = 200 μm and L = 20 μm. The ON-current values of the CdSe-TFTs and CdS-TFTs at a gate bias of 10 V and a source-drain voltage of 10 V are about 100 μA and 5 μA, respectively. The OFF-current values of the CdSe-TFTs and CdS-TFTs at the source-drain voltage of 10 V are less than 10 pA.

The incorporation of the thermal oxidation process for the fabrication of TFTs described in the first procedure is useful for studying the properties and deposition of active semiconductor layers. However, it may not be suitable for large-scale production due to the high temperatures involved and the thermal requirements of the substrate. To reduce the process temperatures and the requirements for substrates, it is necessary to employ methods other than thermal oxidation for gate oxides. In this work, in addition to thermal oxidation, the anodization method will be used to form gate oxides for the second fabrication procedure on glass substrate. In addition, some samples were prepared with thin gate dielectric films by magnetron-sputtering method. The effects of anodization conditions on the quality of the anodic dielectric were investigated by measuring the breakdown electric field and leakage current density of the metal-insulator-metal (MIM) capacitors fabricated.

Results of electrical measurements carried out on the CdSe-TFTs with Al_2O_3 and Ta_2O_5 gate dielectrics showed field effect mobilities of 3.4 and 0.67 cm^2/V-s and threshold voltages of 3.2 V and 8.2 V, respectively. Field effect mobilities of 0.2 and 2 cm^2/V-s and threshold voltages of 4.3 and 5.2 V were observed for CdS-TFTs, again with Al_2O_3 and Ta_2O_5 gate dielectrics. The mobilities obtained from the present TFTs fabricated on glass substrates are smaller than that on similar TFTs fabricated on thermally grown gate oxides on Si substrates. Anodic oxides of Al and Ta developed in this work are usable for fabrication of TFTs on glass substrates by the CBD method. With further improvements, the fabrication of TFT circuits with complex functions is expected using the anodization and CBD methods.

The present TFT-fabrication procedure developed on glass substrate involves four masks using a G-line mask aligner, two vacuum deposition processes for gate and drain-source formation, one CBD dipping at 80 °C for the formation of active layer, three wet chemical etching processes, and a post fabrication annealing process at 400 °C for few minutes to improve the TFT devices. No CVD, stepper, ion implanter, reactive ion etching and high temperature processing are needed. The novel methods developed in this thesis thus provide a low cost and low temperature procedure for TFTs with a very good yield, uniformity, and reproducibility.

Resumé

Avec l'utilisation de couches minces de CdSe et de CdS comme couche active tel que préparé par la méthode chimique de dépôt de bain (CBD), les transistors de couche mince (TFT) ont été fabriqués et étudiés. Il y a deux processus de fabrication développés dans ce travail pour les TFTs dépendant des substrats utilisés. Un procédé pour la fabrication de TFTs sur des substrats de silicium et un procédé pour des dispositifs sur les substrats de verre seront présentés. Les deux procédures sont conçues pour la fabrication de TFTs avec une configuration inversée d'électrode "gate-staggered". Le procédé chimique de dépôt de bain développé a rapporté avec un très bon rendement du CdSe-TFTs et CdS-TFTs sur du substrat thermiquement développé d'oxyde/Si. Les valeurs typiques de la mobilité pour ces TFTs sont environ 10 cm^2/V-s pour CdSe-TFTs et 1 cm^2/v-s pour CdS-TFTs avec W = 200 μm et le L = 20 μm. Les valeurs de courant-actif du CdSe-TFTs et du CdS-TFTs à une polarisation "gate" de 10 V et une tension "source-drain" de 10 V sont d'environ 100 μA et de 5 μA, respectivement. Les valeurs de courant-inactif du CdSe-TFTs et du CdS-TFTs à une tension "source-drain" de 10 V sont inférieures à 10 pA.

L'incorporation du processus thermique d'oxydation pour la fabrication des TFTs décrit dans le premier procédé est utile pour étudier les propriétés et le dépôt des couches actives de semi-conducteur. Cependant, il n'est pas pratique pour la production à grande échelle due aux températures élevées impliquées et aux conditions thermiques du substrat. Pour réduire les températures des procédés et les conditions des substrats, il est nécessaire d'utiliser des méthodes autres que l'oxydation thermique pour des oxydes "gate". Dans ce travail, en plus de l'oxydation thermique, la méthode d'anodisation sera employée pour former des oxydes "gate" pour le deuxième procédé de fabrication sur un substrat de verre. De plus, quelques échantillons ont été préparés avec des couches minces diélectriques "gate" par la méthode de magnétron-pulvérisation. Les effets des conditions d'anodisation sur la qualité du diélectrique anodique ont été étudiés en

mesurant le champ électrique et la densité de courant de fuite des condensateurs de métal-isolateur-métal (MIM) fabriqués.

Les résultats des mesures électriques effectuées sur les CdSe-TFTs avec des diélectriques "gate" d'AlO et de TaO ont démontré des mobilités de champs de 3.4 et 0.67 cm^2/V-s de tension et des tensions de seuil de 3.2 V et de 8.2 V, respectivement. On a observé des mobilités de champs de 0.2 et 2 cm^2/V-s de tension et des tensions de seuil de 4.3 et 5.2 V pour les CdS-TFTs, encore une fois avec des diélectriques "gate" d'Al_2O_3 et de Ta_2O_5. Les mobilités obtenues à partir des TFTs actuels fabriqués sur des substrats de verre sont plus petites que ceux des TFTs semblables fabriqués sur des oxydes "gate" développés thermiquement sur des substrats de silicium. Les oxydes anodiques d'Al et Ta développés dans ce travail sont utiles pour la fabrication de TFTs sur des substrats de verre par la méthode de CBD. Avec des améliorations additionnelles, la fabrication des circuits de TFT avec des fonctions complexes est prévue en utilisant l'anodisait et des méthodes de CBD.

Le procédé de fabrication TFT- actuel développé sur du substrat de verre implique quatre masques utilisant un dispositif d'alignement de masque "G-ligne", deux procédés de dépôt "vacuum"pour la formation de "gate" et "drain-source", un CBD plongeant à 80 ^{o}C pour la formation d'une couche active, trois processus chimiques de gravure, et suivi d'un procédé de fabrication de recuit à 400 ^{o}C pendant quelques minutes afin d'améliorer les dispositifs de TFT. Aucun CVC, de "stepper", d'ion, de gravure réactive d'ion et de traitement à hautes températures sont nécessaires. Ainsi, les nouvelles méthodes développées dans cette thèse fournissent un procédé à prix réduit et à basse température pour des TFTs avec un bon rendement, uniformité, et reproductibilité.

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CAD	computer-aided design
CBD	chemical bath deposition
CdS-TFT	cadmium sulfide thin film transistor
CdSe-TFT	cadmium selenide thin film transistor
CRT	cathode ray tube
CVD	chemical vapor deposition
DSTN	double-layered super twisted nematic liquid crystal display
ELD	electroluminescent display
FPD	flat panel display
HDTV	high definition television
LCD	liquid crystal display
LED	light emitting diode display
LPCVD	low pressure chemical vapor deposition
MIM	metal-insulator-metal
PLD	plasma panel display
TFT	thin film transistor
TFT/LCD	thin film transistor addressed liquid crystal display
TN	twisted nematic
SEM	scanning electron scope
STN	supertwisted nematic
VFD	vacuum fluorescent display
τ	response time
ε	dielectric constant
σ	conductivity
μ_{fe}	field effect mobility
μ_H	Hall mobility
λ	wavelength
ϕ_m	work function
χ	electron affinity
g_m	transconductance
g_o	output conductance
I_d	drain current
N	carrier concentration
N_t	interface state density
n_o	initial carrier concentration
V_d	drain voltage
V_g	gate voltage
V_T	threshold voltage
t_{ox}	thickness of gate dielectric
h	thickness of semiconductor
L	channel length
S	subthreshold swing
W	channel width

Chapter 1

Introduction

1.1 Motivation and overview of the thesis

A display is an electronic component or subsystem used to convert electrical signals into images in real time that can be recognized by a user. It is a unique electro-optical device serving as the visual interface between the user and machine. The electronic display is dynamic in that it presents information within a fraction of a second from the time it is received and continuously holds that information. This is achieved using a refresh or memory technique, until new information is addressed. There are numerous user-oriented applications for electronic displays, ranging from the simplest readouts to the most complex displays for computer-aided design (CAD) and virtual reality.

There are different kinds of display in the industry. Cathode ray tube (CRT) probably remains the most important one in modern society, especially in applications

where the highest visual quality is required. Although the CRT displays remain to be the most common, there is a strong need to provide alternate displays for laptop computers, notebook computers, and other portable, battery-operated units. In these applications, electronic displays with flat panels are needed. Recently, there has been an exponential growth in the sale and use of other display technologies more compatible with the above units.

The flat-panel displays (FPDs) technologies that have been developed include: electroluminescent display (ELD), light-emitting diode display (LED), plasma display (PLD), vacuum fluorescent display (VFD), and liquid crystal display (LCD). ELD and PLD technologies have found certain applications in large area FPDs. For portable applications such as instruments and computers, LCD technology has dominated the market. VFDs have found some applications where ac power is available. LEDs are being used primarily as readouts when large character sizes are desired.

Following previous extensive research activities, the flat panel display industry has expanded rapidly in the past decade, primarily through the development of manufacturing techniques for liquid crystal displays. The main driving force for the growth of this industry is the application of portable computers. Although penetration of FDPs into the desktop computer market has been more difficult, due to the low cost and good performance of the CRTs, the tendency may change in the near future. This is due to the need to recover lost desk space to CRTs by the users. This change is expected to increase with the reduction of manufacturing cost and the improvements in resolution, brightness and color quality of FDPs.

Liquid crystal displays (LCDs) are available in a variety of forms, using different aspects of the liquid crystals. First, it should be pointed out that all LCDs are passive in that they do not emit light. They either block or transmit light generated by a light source. This source may be part of the display, or simply from ambient illumination. In the last few years matrix addressed LCDs have been developed with significant improvements in size, resolution and performance.

One of the main reasons why the LCDs have dominated the battery-operated electronic products is the low power consumption. Some LCDs can operate with only several microwatts under ambient illumination. LCDs with full color capability have been developed employing assemblies of light filters. Depending on the driving circuits used, they can be classified as active matrix LCDs and passive matrix LCDs. For passive matrix LCDs, multiplexed twisted nematic (TN) LC displays of up to 200 lines have been demonstrated. Multiplexed supertwisted nematic (STN) LC color displays of up to 768 lines are available in the market.

The construction of a large area LCD with high-resolution requires special fabrication technologies for large area electronic circuits. This is because a LCD involving a large number of small modules is technically and economically unattractive. To control a pixel and generate gray levels, nonlinear electronic control elements are required. These elements must be connected and integrated with each pixel to minimize the problems of interconnection, crosstalk, multiplexing. However, for the LCD technology, limitations in display performance such as response time, viewing angle and grey scale operation still exist.

At the present the popular display with large area, high information content, color and sufficient grey-scale is the active-matrix thin-film-transistor liquid crystal display (TFT-LCD). When the resolution requirement increases, the technologies for driving circuits (including decoders, drivers, scanners, line storage, or other memory) will also be more complicated. In addition to the performance requirements, there is strong need to develop low cost processes for the fabrication of these driving circuits. In general, the main emphasis of these low cost processes must be on the development of thin film transistors, which are the key elements in TFT/LCDs. In this work, research experiments have been carried out to explore novel and low cost processes for the fabrication of thin film transistors. The experimental details and the results obtained for CdSe-TFTs and CdS-TFTs will be described. A brief outline of the thesis will be given in Section 1.2 whereas the goals and contributions will be presented in Sections 1.3 and 1.4 respectively.

1.2 Thesis outline and brief description of the research work

In Chapter 2, a brief historical review of the TFT/LCD technology will be given. The basic theory and operation principle of the TFTs will then be addressed in Chapter 3. The novel methods developed in this work to fabricate TFTs with active semiconductor layers of CdSe and CdS thin films, employing a chemical bath deposition (CBD) method will be presented in Chapter 4 and Chapter 5, respectively. In the initial part of this work, gate oxide thermally grown on Si substrates was adopted for the CBD deposition experiments. After this initial phase, the novel methods were modified for the fabrication of TFTs on glass substrates. In these experiments on glass substrates, both anodic oxide and sputtered SiN_x have been used as the gate insulators. In Chapter 6, results of characterization of CdS-TFTs and CdSe-TFTs fabricated on thermally grown SiO_2 (on Si substrates) will be presented. Results obtained from TFTs fabricated on sputtered SiN_x, anodic Al_2O_3 and Ta_2O_5 (on glass substrates) will be discussed in Chapter 7. In Chapter 8, conclusions of this work and recommendations for further study are given.

The concentration of this research work is on the development of fabrication processes and characterization of thin film transistors based on CdS and CdSe. Various techniques, such as thermal evaporation, spray pyrolysis, and electrophoresis have been developed to obtain thin films of CdS and CdSe. These processes are either expensive or unable to provide high quality electronic grade thin films. A chemical bath deposition (CBD) method has been used and developed in our laboratory for photovoltaic devices. This method is rather simple, inexpensive and can be carried out at rather low deposition temperatures (25 ~ 90 ^{o}C). It was thus decided to develop this method further in this project for the fabrication of thin film transistors for display applications.

Compared to the well-developed vacuum methods, chemical bath deposition is a low cost technology. This is because it does not require high vacuum system, large power supply or other expensive equipment. In addition, the process can be controlled simply by adjusting the pH, temperature and relative concentrations of various reactants in the solution. The film formation in CBD is the deposition of compound rather than the co-

deposition of separate elements. The technique has been used to grow several II-IV semiconductor films, such as CdS, CdSe, and some ternary compounds. It involves a slow deposition of film from a diluted solution, which contains cadmium in a complex form and sulfur and selenium ions. These ions react to produce either cadmium sulfide or cadmium selenide in a thin film form. The basic principles underlying the chemical bath deposition of semiconductor thin films and early research work in this area have been presented in a 1982 review article [1-1], which has inspired many researchers to initiate work in this area. The subsequent progress in this area is described in review articles [1-2,3]. Recipes for the chemical bath deposition of some compounds are given in other papers [1-4].

In the fabrication of certain photodetectors, photovoltaic cells, and electro-optical devices, thin layers of CdS and CdSe are deposited on substrates to form optically transparent and electrical active regions. These layers are deposited by vacuum methods and screen printing method. In the late 1970s and early 1980s, certain research activities have been carried out on chemically deposited thin films for photovoltaic solar energy conversion applications. The use of chemically deposited semiconductor films as electrodes for photoelectrochemical solar cells was one of the interests. Results of a literature survey showed that very little work has been reported on the preparation of CdSe films by chemical method, especially for thin film transistor devices. In this thesis, research work has been carried out using this method for the preparation of the active layer of thin film transistors.

1.3 Research objectives

The first objective of this thesis research is to develop a low cost method to fabricate thin film transistors. In this method, the active semiconductor layer must be deposited at low temperature and the mobility of charge carriers should be as large as possible, preferably greater than 10 cm^2/V-sec. Furthermore, this method should be

capable of depositing semiconductor films on large area substrates without the need of expensive equipment. The second objective of this work is to develop a process to fabricate thin film transistors with a low thermal budget for display applications. In the thin film transistors, the mobility of charge carriers in the active semiconductor layer should be as large as possible.

1.4 Original contributions

This thesis research has resulted in several original contributions to the field of electronic displays, especially for thin film transistors. Some of the contributions have been described in a US patent No. US6225149 [1-5]. The specific contributions are as follows:

1. The chemical bath deposition process developed has yielded CdSe-TFTs and CdS-TFTs on thermally grown oxide with very good performance. Typical values of mobility are about 10 $cm^2/V\text{-}s$ for CdSe-TFTs and 1 $cm^2/V\text{-}s$ for CdS-TFTs with channel width, W = 200 μm and channel length, L = 20 μm.

2. Anodic oxide of Al and Ta developed in this work are usable for fabrication of TFTs on glass substrates by the CBD method. With further improvements, the fabrication of TFT circuits with complex functions is expected using the anodization and CBD methods.

3. The fabrication procedure developed in the present work involves four masks using a G-line mask aligner, two vacuum deposition processes for gate and drain-source formation, one CBD dipping at 80 °C for the formation of active layer, three wet chemical etching processes, and a post fabrication annealing process at

400 ^{o}C for few minutes to improve the TFT devices. No CVD, stepper, ion implanter, reactive ion etching and high temperature processing are needed.

4. The novel methods developed in this thesis thus provide a low cost and low temperature procedure for TFTs with a very good yield, uniformity, and reproducibility.

References

1. K. L. Chopra, R. C. Kainthla, D. K. Pandya, A. P. Thakoor, in: G. Hass, M. H. Francombe, J. L. Vossen, Physics of Thin Films, vol. 12, Academic Press, New York, pp. 201, 1982.

2. C. D. Lokhande, "Chemical deposition of metal chalcogenide thin films," Mater. Chem. and Phys., vol. 27, pp.1-43, 1991.

3. P. K. Nair, M. T. S. Nair, V. M. Garcia, O. L. Arenas, Y. Pena, A. Castillo, I. T. Ayala, O. Gomezdaza, A. Sanchez, J. Campos, H. Hu, R. Suarez, M. E. Rincon, "Semiconductor thin films by chemical bath deposition for solar energy related applications," Solar Energy Materials and Sollar Cells, 52, pp. 313-344, 1998.

4. Kolb Alkine, "Advances in electrochemical science and engineering," Wiley VCH vol. 6, pp. 165-235, 1999.

5. F. Y. Gan, I. Shih, "Methods to Fabricate Thin Film Transistors and Circuits," US patent No. US6225149, awarded on 05/01/2001 at the United States Department of Commerce, Patent and Trademark Office.

Chapter 2

Thin Film Transistor-Addressed Liquid Crystal Displays (TFT/LCDs)

2.1 Overview of TFT/LCDs

As stated before, there has been an increasing demand for flat panel displays (FPDs) in the fields such as consumer electronics, portable devices, and vehicle applications [2-1]. In comparison to the conventional cathode-ray tube (CRT), FPDs allow volume, weight and power consumption of equipment to be reduced. The successful FPDs developed so far in the market are plasma display (PD), electroluminescent display (ELD), vacuum fluorescent display (VFD), field emission display (FED), light emitting diode (LED) display and liquid crystal display (LCD). Among these, the LCD is considered to be the best candidate due to its full color display capability and low power consumption. Furthermore, progress in information technology has led the industry to a new era, in which users spend longer and longer time in front of

electronic displays. Hence, there is strong need to improve quality of electronic displays for various applications.

One of the final goals of FDPs in general and TFT/LCDs in particular is to replace papers. Numerous papers and reports have been published on the development of FDPs. In this chapter, the development of liquid crystal displays will be briefly described. This is followed by an introduction to thin film transistors, specifically for LCDs.

Liquid crystalline state in certain materials was discovered more than 100 years ago [2-2]. It took many years for the first popular liquid crystal-based electro-optical display to be developed [2-3]. The idea of using liquid crystals for display application was probably first proposed by G. Heilmeier and R. Williams, and demonstrated by a research group of RCA Corporation in New Jersey, USA, in 1963 [2-4,5,6]. Since then, many researchers and engineers have carried out work in order to improve the characteristics of liquid crystal displays. Detailed description of research efforts on TFT/LCDs can be found in various references [2-7,8,9,10]. The first functional TFT/LCD was successfully developed by T. P. Brody in 1973, where a CdSe-TFT was used as the switching element [2-8]. The interests then shifted towards amorphous silicon, which had been developed extensively for photovoltaic solar cell devices. The first amorphous hydrogenated Si (a-Si:H) TFT was reported by P. G. Lecomber [2-11]. After this, many laboratories started the development of TFT/LCDs using a-Si:H-TFTs. More recently, poly-Si-TFTs have been developed. The current LCD products developed for portable displays have screen sizes ranging between 3 and 24 inches (diagonal).

There are two main trends in the development of TFT/LCDs. One is the direct-view display for portable computers and television applications, where LCDs with large screen sizes and high pixel-content are the main requirements [2-9,10]. The other is toward compact LCD modules with high pixel density for projectors and video cameras [2-11]. As mentioned before, the current technology for most of LCDs is based on a-Si:H-TFTs. For LCD projectors and viewfinders in video cameras, the technology based on poly-Si-TFTs is more suitable due to the high pixel density required. This is because

complex monolithic driver circuits can be fabricated on poly-Si, which has high carrier mobility.

To construct a high performance electronic display based on liquid crystals, large area circuits of TFTs with high switching speed, high packing density, and high gray-scale must be obtained. To meet the above demand and to achieve large viewing angles, TFTs in an inverted gate structure has been utilized. The quality of TFTs in the driving circuits has a direct impact on the performance of the TFT/LCDs. In this work, the efforts will be made to develop a process for the fabrication of TFTs.

TFTs are based on field effect with insulated gate built on an insulating substrate or surface. The current flowing between drain and source electrodes of a TFT is modulated by the gate electric field through the gate oxide. The operation principle of TFTs is the same as that for MOSFETs. MOSFETs are normally fabricated on a monocrystalline Si substrate, while TFTs are often fabricated on insulating glass substrates with a thin poly-crystalline or amorphous film as the active layer. The fabrication of TFTs is more flexible than MOSFETs because the additional freedom in the choice of semiconductor other than Si. For example, large band gap semiconductors such as CdSe and CdS may be used. With the large band gap semiconductors as the active layer, the density of thermally generated carriers can be very small compared to the density of majority carriers.

When a voltage is applied across the two electrodes of a capacitor, electrons are drawn from an upper plate and forced into a lower plate. Due to the increase in the electron density, the electrical conductance of the lower plate will increase. However, due to the large number of free electrons in the metal without the voltage, the resulting change of the conductance is relatively small. When the lower plate is replaced by a semiconductor thin film, the capacitor is substantially unaffected. However, the number of electrons in the semiconductor plate may be very small compared to the electrons induced by the voltage between the two plates. Thus, the application of a control voltage can result in the modulation of the conductance of the semiconductor. This modulation

can be as large as several orders of magnitude. The amount of induced electrons can be controlled by the capacitance. By arranging the geometry and properties of the capacitor to give a large capacitance, a large number of free carriers can be induced in the surface even at a moderate gate voltage.

An active matrix LCD is a display which incorporates an active matrix circuit to assist the electrical addressing of the pixels. In this circuit, there is at least one TFT for each pixel element. The pixel element is defined by the crossover of a row line and a column bus line. Currently, the matrix circuit with a TFT and a capacitor in each pixel element is widely used. This circuit was first reported in 1971 by B. J. Lechner [2-7]. In flat panel electronic displays, elements for light switching are arranged in a two-dimensional array where the optical state of each element (or pixel) is controlled by at least one transistor. In addition to the control of optical state of the pixels, transistors are required to form column driving circuits and row driving circuits. These circuits control the flow of electrical signals to individual pixel. Since most of the flat panel electronic displays are fabricated on low cost glass substrates, the transistors used are usually in a thin film form.

The active region of a thin film transistor is a layer of semiconductor. There are several requirements for a thin film transistor used in high quality electronic displays. Firstly the leakage current between drain and source in off state must be small (<10 pA). Secondly, the on state current at a given voltage (10 volts for example) must be large (>1 μA). Finally, the threshold voltage must be small and the mobility of charge carriers in the channel must be large.

Thin films of a-Si for TFTs are typically deposited by CVD method at substrate temperatures of about 350°C. For poly-Si films, a LPCVD method is used at substrate temperatures ranging from 500 to 650° C. Hence the energy consumption for the deposition of Si films is high. Furthermore, the deposition of uniform Si films on substrates with large dimensions required for the electronic displays is difficult to achieve due to the distribution of molecules in the reaction chamber. Although the mobility of

charge carriers in poly Si as large as 200 cm^2/V-sec, the mobility in a-Si is quite small, in the order of 5 - 10 cm^2/ V-sec. The above mobility values are for Si films prior to the formation of field effect transistors. When a thin film field effect transistor is fabricated on a-Si, the effective mobility of carriers is reduced to 0.3 - 1 cm^2/ V-sec, whereas the effective mobility of carriers in poly-Si is reduced to 25 - 100 cm^2/ V-sec. The precise values of effective mobility in a-Si and in poly-Si TFT are determined by the deposition temperature of the a-Si and poly-Si films and fabrication processes.

Thin film transistors may be fabricated using CdS or CdSe as an active semiconductor [2-12,13]. Both Hall mobility, μ_H, and the effective mobility, μ_{eff}, of CdS and CdSe are greater than those of a-Si. Therefore, these two materials are potentially good candidates for thin film transistors. Thin film transistors based on CdSe have been fabricated for LCDs with high brightness. In these transistors, thin film of CdSe was deposited by a vacuum thermal evaporation method. Although some success has been demonstrated in the prior experiments, it has been observed that the reproducibility and uniformity of surface electronic properties of the vacuum deposited large area CdSe are difficult to control. Because of the difficulty in reproducibility of the surface electronic properties of vacuum deposited CdSe, variation of the threshold voltage of the thin film transistors from one substrate to others is too large to achieve high production yield.

Therefore, it would be desirable to develop a method to fabricate thin film transistors where the active semiconductor layer is deposited at low temperature using a low cost method. The mobility of charge carriers in the deposited films should be as large as possible, preferably greater than 10 cm^2/V-sec. Furthermore, this method should be capable of depositing semiconductor films on large area substrates without the need of expensive equipment. A more detailed discussion on the fabrication of TFT using the novel method will be presented in Chapter 4.

2.2 TFT/LCD Configuration

The basic configuration of a TFT/LCD is shown in Figure 2-1. Liquid crystal is encapsulated between two glass substrates, a TFT substrate and a color – filter substrate. The transparent common electrode on this substrate is made of indium tin oxide (ITO), and is deposited on top of the color filter. In order to obtain good display quality, the cell gap for the liquid crystal has to be precisely controlled to a specific value, e.g., 5 μm. This gap has to be uniform over the whole display area and reproducible from unit to unit. Therefore, transparent spacers such as plastic beads are placed between the two glass substrates.

Liquid crystal cells are constructed using twisted-nematic (TN) type liquid crystal in which the orientation of the liquid crystal director is twisted 90 degree between the TFT substrate and the common electrode substrate. In Figure 2-1, a cross-polarized system is shown where the first polarizer acts as a backlight polarizer and the second acts as an analyzer. In this system, light passes through the analyzer when no voltage is applied, and is blocked when the applied voltage is high enough to align the liquid crystal directors vertically. The liquid crystal is anchored on the surface of the glass substrates so that its molecules are oriented to the proper direction. In order to set the anchoring direction, the glass substrate is coated with an organic film such as polyimide and the surface of the film is rubbed with a fabric in a specific direction.

The TFT substrate consists of a TFT array and an array of external terminals on which the driver circuits are bonded or connected to drive the TFT panel. The driver circuits are essentially scan generators for the horizontal and vertical buslines. The backlight system can be either direct or indirect. With direct lighting, one or more fluorescent lamps are positioned directly beneath the rear polarizer, and with indirect lighting, a light guide is used to guide the light from lamp situated beside it.

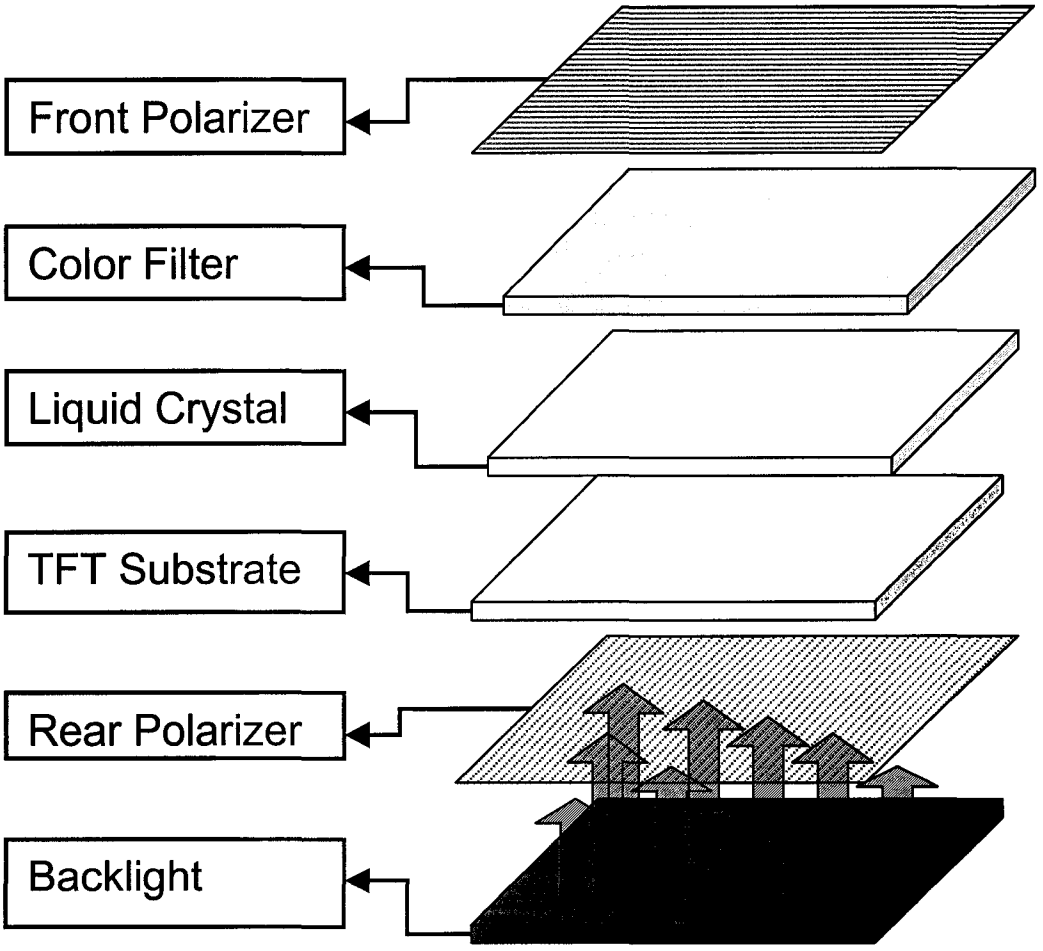


Figure 2-1 The configuration of TFT/LCD.

2.3 Principles of TFT/LCD

In normal materials, there are three phases, solid, liquid and vapor. However, liquid crystal has an additional mesomorphic state at room temperature. Specifically, liquid crystal exhibits liquid-like properties and crystal-like properties concurrently. This phenomenon is due to the long length of the molecule and orientational orderness in their molecular arrangement. The unique molecular arrangement gives rise to strong dielectric anisotropy, which is very important for the understanding the operation of liquid crystal displays.

Figure 2-2 shows the configuration and operation of a transmissive type twisted nematic liquid crystal cell. The cell comprises two glass substrates coated on their inner surfaces with transparent electrode and separated by several μm. The space between the two substrates is filled with a nematic liquid crystal material. Molecules of liquid crystal are twisted initially by the alignment layers on the two glass substrates, with the alignment directions perpendicular to each other. Since the polarizers are positioned with the directions of polarization perpendicular to each other, the polarization of light will be rotated by 90^{o} by the liquid crystal and allowed to transmit through the polarizer as shown in Fig. 2-2(a). When a voltage is applied, the molecules will arrange themselves to be parallel to the applied field as shown in Fig. 2-2(b), due to the positive dielectric anisotropy of the liquid crystal materials. Because the polarization of light transmitted through liquid crystal is different from the output polarizer in output end, the light will not be allowed to transmit. As a result, the light is switched on and off by using dielectric anisotropic characteristics of liquid crystal.

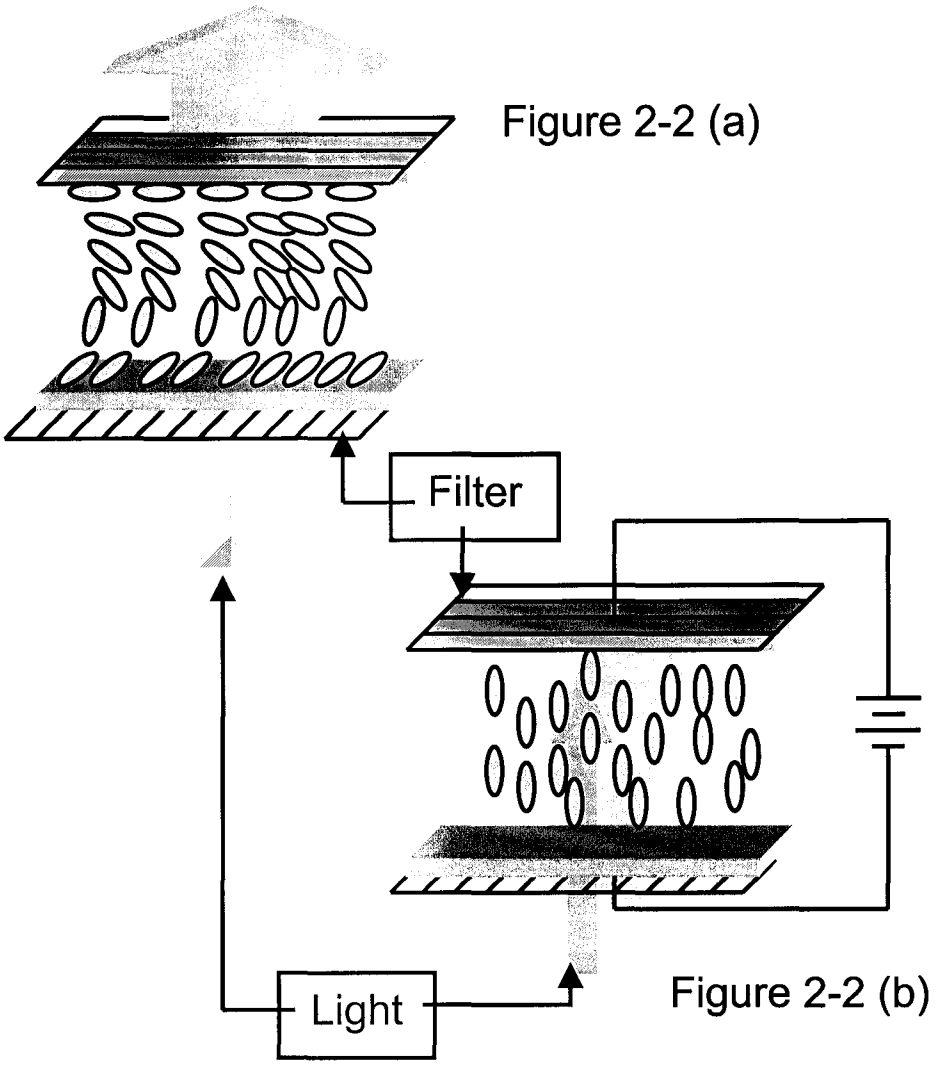


Figure 2-2 Operation of a twisted nematic liquid crystal cell.

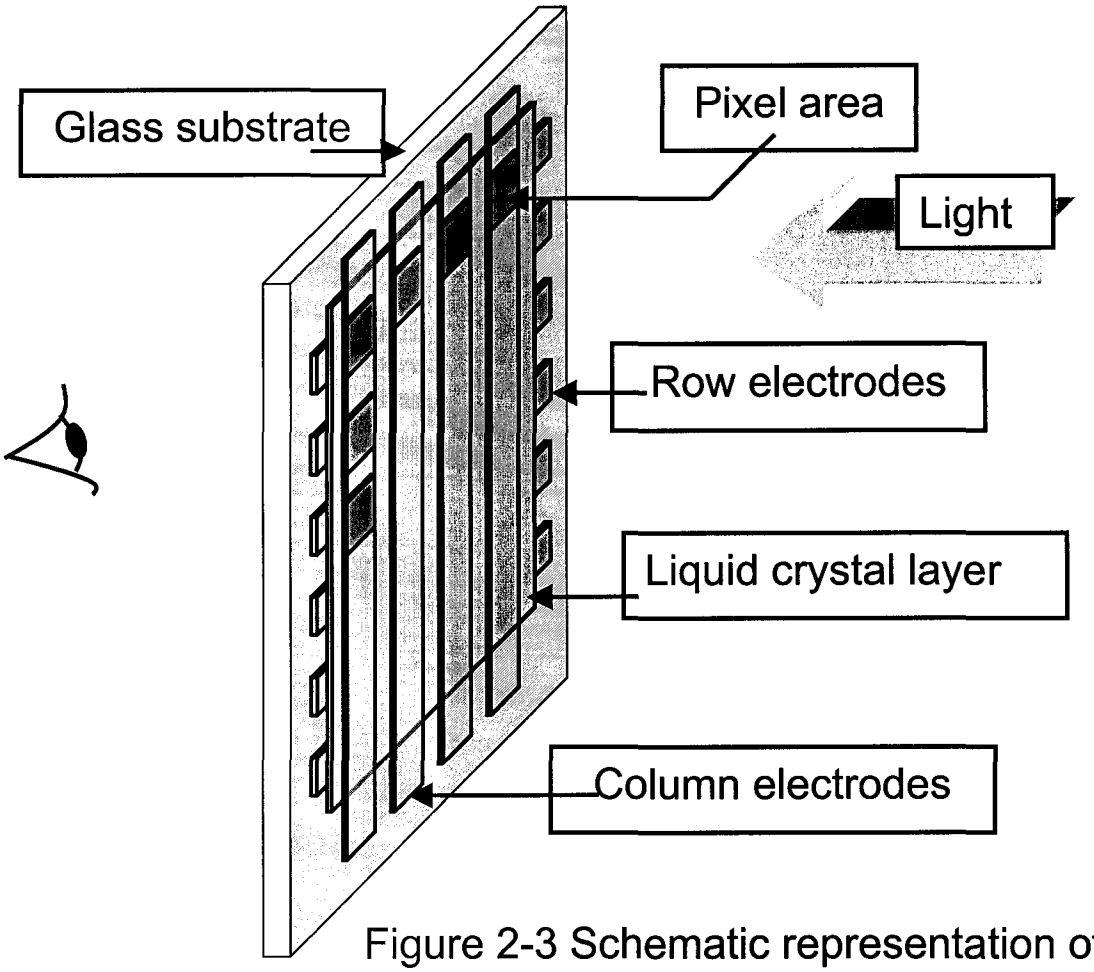


Figure 2-3 Schematic representation of a passive matrix LCD.

The driving methods for LCDs include passive driving for a passive matrix and active driving for an active matrix. Passive matrix driving [14] was employed in the early stage of LCDs development. In this method, transparent electrodes are deposited on the substrate along X and Y-axis to form row electrodes and column electrodes, as shown in Fig. 2-3. The row electrodes are selected (or connected to the driving voltage source) from the top to the bottom. In this method, a small voltage is applied to the pixel even when it is in the off state, because all electrodes are electrically connected together. Therefore, it is difficult to obtain high contrast for the large display using this passive driving method. Although the above problem can be partly solved by double-layered super twisted nematic (DSTN) liquid crystal, other inherent problems have limited the

applications in high quality FDPs. For instance, as the pixel density increases, the contrast decreases and the viewing angle reduces.

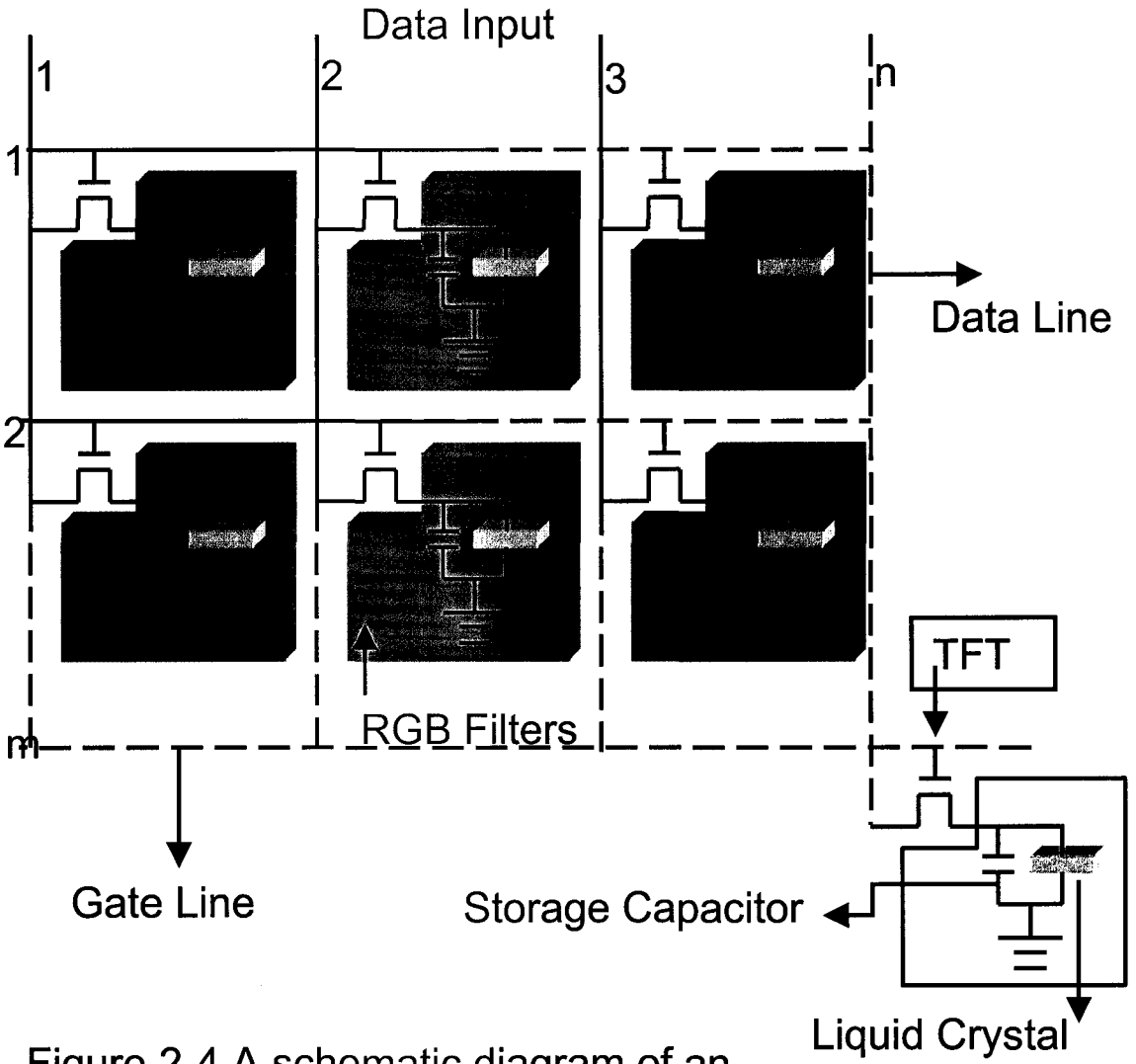


Figure 2-4 A schematic diagram of an active matrix LCD.

The drawbacks for the passive matrix driving method can be greatly reduced by employing the active matrix driving method incorporating thin film transistors. This is because the charge required to activate the pixel electrode can be stored and switched by a TFT, which acts as a nonlinear element. In a color TFT/LCD, a transmission mode is generally used. The general arrangement of a color TFT/LCD is shown in Fig. 2-4. The voltage on the pixel electrode, which controls the optical transmission of the pixel, is provided by a line-at-a-time addressing mode.

A row of TFTs, with a common electrode, would be turned on for a TV line time period of 32 μs, during which the capacitance of these pixels need to be charged to the data voltage. Following this, the gate will be switched off, and the charge at each node will need to be maintained until it is refreshed in the next frame (about 20 ms later). The conditions of charging the node capacitance during TV line time, and maintaining the charge during the TV frame time dictate the minimum required ON and OFF current ratio of the TFT. The current ratio needed is typically in excess of 10^5, with the absolute values of current determined by the size of the pixel and hence its capacitance. In order to drive the active matrix displays, it is necessary to make contact to each of the row and column connections. For a 500 row × 500 column for a full resolution TV, this amounts to ~ 1000 total connections.

One method to achieve these connections in a-Si:H and other displays has involved the usage of silicon integrated circuits, which are mounted around the edges of display. This method has increased the display cost significantly. A more efficient approach is to fabricate the scanning and addressing circuits on the substrate for LCD arrays. Complete integration of pixels and driving elements in this fashion would reduce the total number of external connections from ~1000 to ~20. To obtain driving circuits with high enough switching speed, the carrier mobility should be sufficiently high. This is because the row scanning circuit needs to operate at the TV line rate of 15 kHz and the column addressing circuit at an even higher frequency, the TV data rate of about 10 MHz. To fabricate circuits of these speeds, TFTs with a carrier mobility of > 0.2 cm^2/V-s are needed for the row drive circuit and a carrier mobility > 100 cm^2/V-s for the data

drive circuit (assuming a channel length of 6 μm). Whilst a-Si:H is capable of satisfying the mobility requirement for the row driver circuits, it is not sufficient for the column drive circuits. Moreover, due to the low mobility of a-Si:H, it is difficult to design compact, area efficient circuits to charge the large row capacitances.

For HDTV displays, where the number of rows and columns are expected to double, TFTs with even higher operating speeds will be required. For these displays, as well as for electronic workstations, the reduced addressing times will impose a greater demand upon the pixel TFT in order to supply sufficient ON-current to charge the pixel capacitance. To meet the above additional requirement, it is important to develop TFTs based on polycrystalline thin films with larger mobility such as poly-Si, CdSe and CdS. In this work, a chemical bath deposition method of CdSe and CdS thin films has been developed to fabricate TFTs for LCD displays.

2.4 TFT fabrication

As stated before, the fabrication of TFTs is based on thin film processes including thin film deposition and etching. For the a-Si used in TFT/LCDs, the processes used are natural extension of monocrystalline Si technology. In VLSI technology, the substrate is a Si wafer on which a variety of processing steps are performed, such as thin film deposition, thin film growth, oxidation, etching, lithography, impurity diffusion, heat treatment, and ion implantation. Si is quite stable under extreme conditions (temperature and environment) and oxidation, diffusion, and heat treatment can be carried out at temperatures above 1000 °C. Contrarily, TFTs have to be processed on transparent glass substrates and the process temperature is limited to below 400 °C. This is also a main reason why a-Si based technology has been so popular in FDP industry (the deposition of a-Si can be carried out below 400 °C). The process steps in a-Si technology include thin film deposition such as plasma CVD, metal sputtering, lithography, oxidation, etching,

and rinsing. The substrate size in TFT fabrication is usually larger than that of VLSI technology, 8"~12" being the most popular sizes for Si IC industry. Dimensions for TFT circuits in FDPs often are large. Substrates with a diagonal of 24" are now used in the production lines of TFT/LCDs and can be found in the market.

The procedure for TFT-fabrication has to satisfy various requirements since it involves thin film, low temperature, large area, and fine patterns. The requirements for low temperature result from the transparent glass substrate used, and fine patterns from high circuit resolution. In general, the TFT-fabrication process can be classified and described as follows:

1. Formation of the gate electrode (Al, Ta, W, Cr) of the TFT,
2. Formation of the active layer (a-Si, poly-Si, CdS, CdSe, etc.),
3. Formation of the gate oxide (SiO_2, SiN, Al_2O_3, Ta_2O_5),
4. Formation of the source and drain electrodes.

In this thesis, results of research work carried out on active layers and gate oxide formation will be specifically described. The work was developed in order to obtain TFTs of good performance with the aim to lower production cost for large area applications.

References

1. W. E. Howard, Proc. Of Japan Display, 89, pp.8, 1989.

2. B. Bahadur, Mol. Cryst. Lig. Cryst. 99, pp. 345, 1983.

3. J. A. Castellan, Mol. Cryst. Lig. Cryst. 165, pp. 389, 1988.

4. R. Williams, J. Chem. Phys., 39, pp. 384, 1963.

5. R. Williams and G. H. Heilmeier, J. Chem. Phys., 44, pp.638, 1966.

6. G. H. Helimeir, L. A. Zanoni and L. A. Barton, Appl. Phys. Lett., 13, pp. 46, 1968.

7. B. J. Lencher, F. J. Marlowe, E. O. Nester and J. Yults, Proc. IEEE Trans. Electron Device 59, pp. 1566, 1971.

8. T. P. Brody, J. A. Asars, and G. D. Dixon, IEEE Trans. Electron Devices, ED-20, pp. 995, 1984.

9. H. Tanaka, S. Molte, M. Hoshino, K. Takahashi, M. Ohta, T. Sakai and T. Toyama, Proc. Of Euro Display, 87, pp. 55, 1987.

10. K. Oki, Y. Nasu, J. Inoue, T. Hoshiya, K. Takahara and Y. Toyama, Proc. of Euro Display, 87, pp. 55, 1987.

11. P. G. Lecomber, W. E. Spear and A. Ghaith, Electron Lett., 15, pp. 179, 1979.

12. P. K. Weimer, "The TFT-a new thin-film transistor," Proceedings of The IRE, Vol. 50, pp. 1462-1469, 1962.

13. T. P. Body and D. J. Page, "Flexible thin film transistors," Elecronics, pp. 100, 1968.

14. K. Ichikawa, S. Suzuki, H. Matino, T. Aoki, T. Higuchi and Y. Oana, Tech. Digest of SID, 89, pp. 226, 1989.

Chapter 3

Thin Film Transistors

3.1 Overview of thin film transistors

Following Weimer's successful work in CdS-TFTs in 1962, results of research on TFTs were reported in a number of semiconductor materials. These include cadmium sulfide [3-1], cadmium selenide [3-2], tellurium [3-3], lead sulfide [3-4], indium antimonide [3-5], lead telluride [3-6] and silicon [3-7]. Some studies were also made to determine suitable combinations of semiconductors and insulators. The most commonly used insulators for TFTs are silicon oxides, nitride, and aluminum oxides whereas the most commonly used semiconductor materials are CdS, CdSe, a-Si, and poly-Si. The first successful TFT reported (Weimer, 1962) in fact used CdS. Whereas CdSe-TFTs have the longest history in TFT-LCD applications. They possess the required characteristics for both the matrix circuits and the peripheral driver circuits. However, a large-area high-resolution color display employing CdSe-TFTs has not been reported. The band gaps of CdS and CdSe (2.4 eV and 1.7 eV, respectively) are considerably larger than that of Si (1.1 eV). Therefore, dark resistivities of these materials are considerably higher than that of Si. It is also noted that both CdS and CdSe have always been found to be n-type.

Since the first successful development of functional CdS thin film transistors (CdS-TFTs) in 1962 and a scan generator made entirely by employing CdS-TFTs in 1967 [3-8] by Weimer, many discussions have come about to their quality, stability, reproducibility and usefulness. Most of the criticisms during the 1960's arose from comparing the TFT integrated circuits with the well-developed silicon counterparts. As a result, the corresponding development effort on TFT circuits and the systematic research necessary to understand the problems of the TFT were sustained by only a few groups. However, the advantages of the TFTs for specific applications ensure the continuous development of TFTs technology.

In the early 1980s, strong interests in TFTs have revived because of new large-scale applications. These include active matrix addressed flat panel displays and static random-access memories. For circuits requiring low production cost, large area substrates, high electrical insulation, high optical transparency or mechanical flexibility, the adoption of the TFT technologies may be advantageous. It is thus clear that with the remarkable advances of silicon technology, it still cannot satisfy the application requirements. For flat display applications, the ultimate objective is to create an all-solid-state flat-panel structure with high resolution and small volume (or mass).

As pointed out by Fischer [3-9], vacuum deposition of TFT is compatible with laying down a matrix of light-emitting or passive display elements and interconnecting them. The first attempt of constructing a thin film transistor addressed liquid crystal display (TFT-LCD) was reported in 1973 by the Westinghouse group led by Brody [3-10] which demonstrated the switching ON and OFF of one row of pixels in a 6″ × 6″ 20 line-per-inch (lpi) panel. It was followed by the report of video performance results of a 6″ × 6″ 30 lpi TFT-LCD panel in 1978 [3-11], all using CdSe film as an active layer. During the 1970's, the main efforts on TFT-LCD development were carried out at Westinghouse Research Laboratory using CdSe-TFTs fabricated by a shadow mask technique [3-12], with the display resolution limited to less than 50 lpi. The resolution of displays employing CdSe-TFT devices was increased to 50 lpi by a hybrid process combining

shadow mask and photolithography. This was increased to 80 lpi and 640 × 480 elements on an 8″ × 5″ active area by using an all-photolithographic process in 1985 [3-13].

Since the beginning of 1980's, there has been an upsurge of interest in the TFT-LCD technology mainly due to the availability of a-Si and poly-Si as the thin film semiconductor materials, which may be processed using conventional semiconductor processing equipment. Currently, flat panel displays up to 24″ (Samsung Electronics SyncMaster 240T) are available in the market using a-Si-TFTs. Pocket TVs up to 6″ diagonal dimensions are in production using both poly-Si and CdSe materials. The industry of TFT-LCD's is rising due to the large worldwide demand in high quality flat panel displays.

Due to the low OFF-currents, relatively large ON-currents and its commonality in processing equipment with Si MOS device fabrication, a-Si has been the most popular material in the present TFT-LCD market. However, the low field-effect mobility of a-Si (~1 cm^2/V-sec) has limited its application in displays requiring higher resolution. Although the ON-current can be increased by decreasing the channel length, the production cost will increase substantially due to the need of expensive equipment and lithography processes. High-resolution displays can be fabricated using poly-Si and CdSe-TFTs to obtain high field-effect mobilities. However, the production cost may be too high as they are deposited by LPCVD and thermal evaporation to allow them to become successful candidates in large area displays.

In the deposited semiconductor films, the field-effect mobility of charge carriers should be as large as possible, preferably greater than 10 cm^2/V-sec. Furthermore, the method should be capable of depositing semiconductor films on large area substrates without the need of expensive equipment. In order to obtain uniform films over large area, we have adopted CdS and CdSe as active layer materials due to their inherent high mobilities. A novel low cost method involving chemical bath deposition (CBD, to be presented in Chapter 5) has been developed in this work to fabricate the required TFTs. Thermally grown SiO_2 (to be presented in Chapter 6), sputtered SiN_x, and anodic Al_2O_3,

Ta_2O_5 are used as insulating layers (to be presented in Chapter 7). The detailed experimental setup and device performance will be discussed in the following Chapter. The following sections in this chapter will focus on the basic theory and operation of TFTs especially for CdS and CdSe materials.

3.2 Characteristics of TFTs

The operation of a TFT is similar to that of the conventional field effect transistor (Weimer [3-1]) where the output characteristics result from changes in the conductivity of a channel connecting the source and drain electrodes. The basic structure of a TFT can be shown as a capacitor in Figure 3-1, consisting of an active semiconductor layer and a gate electrode. When a positive voltage is applied to the gate electrode, the gate electrode is positively charged and electrons are induced in the active semiconductor (CdS or CdSe) to form an accumulation layer.

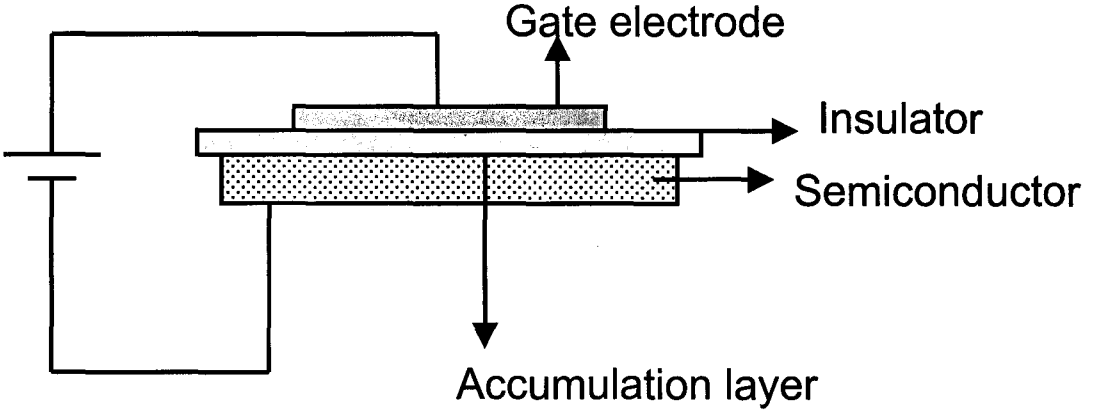


Figure 3-1 Representation of a TFT as a capacitor.

Since the electrical conductance of the active layer is a function of the total number of free electrons, the conductance may be controlled by the gate voltage. If the number of electrons in the semiconductor film without the gate voltage is small, then the change of conductance due to control voltage can be several orders of magnitude. A large capacitance permits a large number of free carriers to be induced in the surface region.

A typical TFT is shown schematically in Figure 3-2. If all the induced carriers are free to conduct, then the change in the sheet conductivity, $\Delta\sigma$ (σ is the sheet conductivity), of the semiconductor film is given by $\Delta\sigma = e\mu\Delta n_c$, where e is the electronic charge, μ is the electron mobility, and Δn_c is the change in the mobile electron concentration near the surface of the active layer. Since $\Delta\sigma$ is proportional to the change in the field, this method of modulation is commonly known as the field effect modulation.

Two assumptions will be made here to simplify the treatment: a) the mobility of the induced charges along the channel is constant and is independent of the gate voltage, b) the gate capacitance along the channel is constant and again is independent of the gate voltage. The charge induced on the gate electrode per unit area is $C_{ox} \times [V_g - V(y)]$, where C_{ox} is the insulator capacitance per unit area, V_g is the potential applied to the gate relative to the source electrode, and the V(y) is the potential of the semiconductor at a point y from the source electrode. The basic device parameters are the channel length L (~20 μm in this work), which is the distance between the drain and source electrodes; the channel width W (~200 μm); the thickness of gate insulator t_{ox} (60 ~ 200 nm); the thickness of semiconductor layer h_s (~200 nm). The source contact will be used as the voltage reference throughout this thesis.

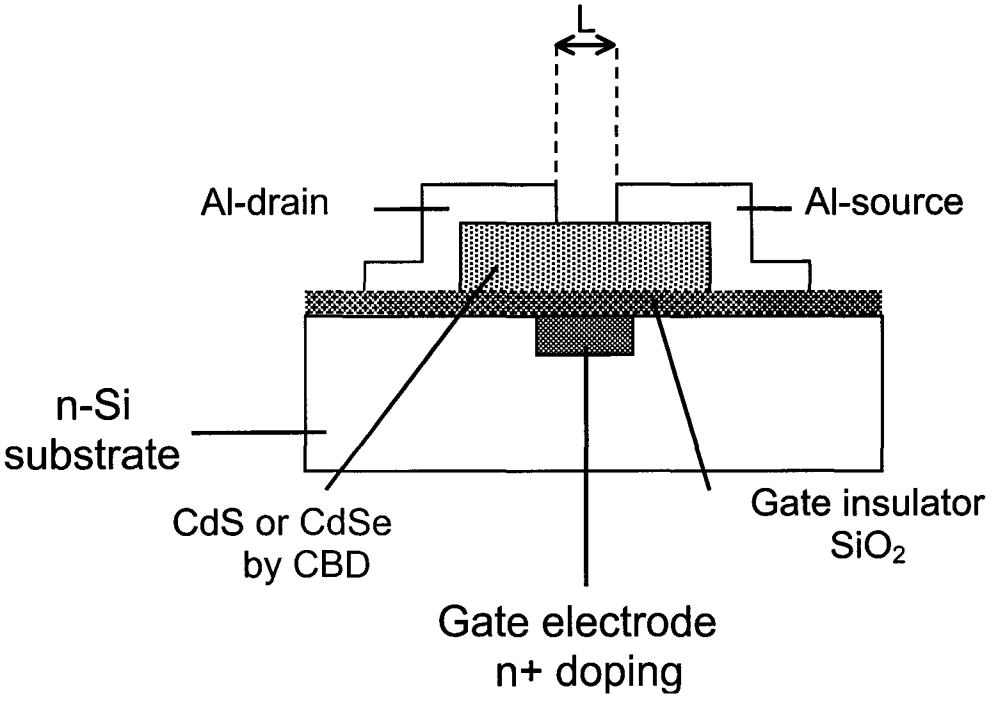
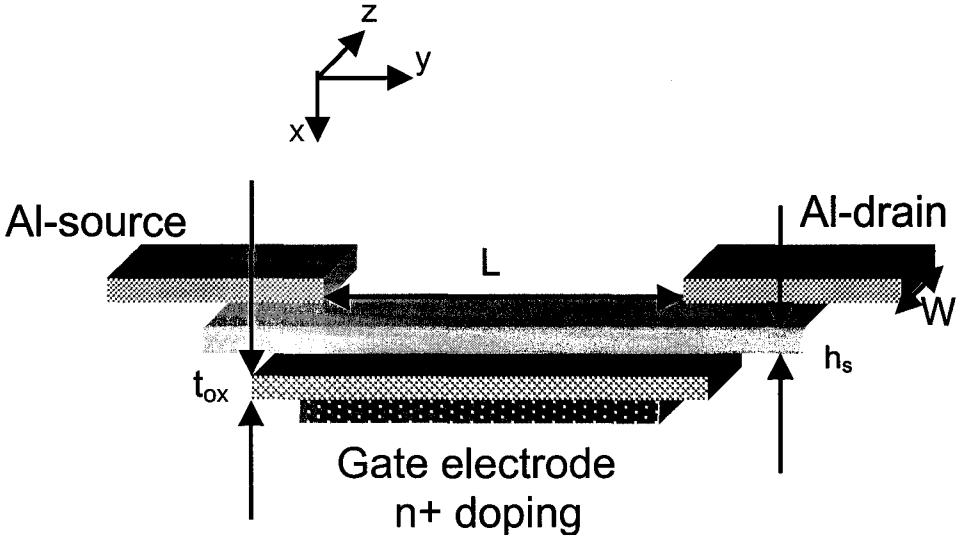


Figure 3-2 Schematic diagram of TFT on a Si substrate.



L: channel length
W: channel width
t_{ox}: thickness of insulator
h_s: thickness of the semiconductor

Enlarged 3-D cross section view of figure 3-2

If the initial number of free carriers per unit surface area (electrons or empty traps) in the semiconductor is n_o and all of the induced charges are free to increase the conductance, then the total mobile charge per unit area in the semiconductor is $n = n_o + C_{ox} \times (V_g\text{-}V(y))/q$. When an electric field, E_y, is applied along the channel, a drain current given in equation 3.1 will flow,

$$\frac{I_d}{Wh} = J = nq\mu E_y = [\frac{n_o q}{h} + \frac{C_{ox}(V_g - V(y))}{h}]\mu E_y$$

$$I_d = W\mu[n_o q + C_{ox}(V_g - V(y))]\frac{dV(y)}{dy}$$

3.1

where W is the channel width; h is the thickness of accumulation region; J is the drain current density and n is the carrier concentration.

Value of $V_T \equiv -n_o q / C_{ox}$ can be defined as the threshold voltage of the TFT. For an enhancement mode transistor, V_T is positive and is negative for a depletion mode device. By re-arranging the terms and performing integration, the following equation is obtained: $I_d \int_0^L dy = C_{ox} W\mu \int_0^{V_d} [(V_g - V_T) - V(y)]dV(y)$. The result is given below:

$$I_d = \frac{C_{ox} W\mu}{L}\left((V_g - V_T)V_d - \frac{V_d^{\,2}}{2}\right) \qquad 3.2$$

where V_d is the voltage applied between the drain and the source electrodes. In the above derivation, the drift mobility was assumed to be constant and independent of V_g. Equation 3.2 also shows that for a given V_g, the drain current increases with V_d, and reaches a maximum when $V_d = V_g - V_T$.

This equation is valid only in a voltage range of $0 \le V_d \le V_g - V_T$ ($V_d = V_g - V_T$ is the on-set of saturation point). Beyond this onset of saturation point, the current is

assumed to be constant as predicted by Shockley [3-14] for the field effect transistors. The voltage range where $V_d > V_g - V_T$ is called the saturation region. The drain current in the saturation region is given by:

$$I_{dsat} = \frac{C_{ox} W \mu}{2L} (V_g - V_T)^2 \qquad 3.3$$

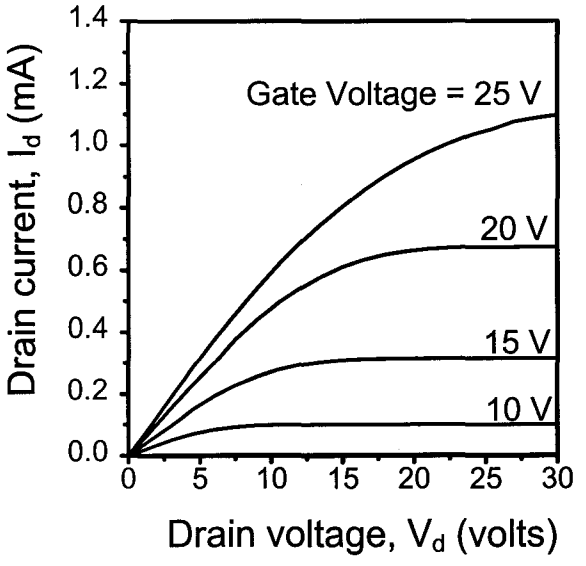


Figure 3-3 Typical output characteristics of a TFT.

The drain current (or output) characteristics for a typical TFT are shown in Figure 3-3. Here, it is noted that the channel length is 20 μm and width is 200 μm for this TFT. It is also noted that the drain current is nearly constant for $V_d > V_g - V_T$. When charges are capacitively induced in the semiconductor, they are attracted towards the semiconductor surface by the electric field applied in the insulator rather than distributing uniformly throughout the semiconductor film. The conducting channel between the drain and source electrodes can be divided into two regions, the one near source and the other near drain. The channel near the drain region is usually very short compared with that

near the source region. Before current saturation can occur, the source region extends to the drain electrode. As the drain potential is increased, the decrease of potential difference across the insulator at the drain end causes evacuation of the carriers. When the carrier concentration in the channel near the drain end is negligible or zero, pinch-off occurs. This operating point corresponds to the onset of current saturation. In the region near the drain where the channel potential difference exceeds $V_g - V_T$, the channel is entirely pinch-off and the flow of current is maintained by the high field and the injection of majority carriers into the region from non-pinch-off region. Current flow in non-pinched-off region is ohmic in nature while that in pinch-off region is emission-limited and the conductance mechanism is nonohmic i.e., the current density is not proportional to the field. In some TFTs non-constant saturation current is observed which could be due to the existence of other current paths. These cannot be modulated completely by the gate voltages. Such characteristics would also be expected if the depletion region could not be formed near the drain. Possible factors that can lead to such behavior are [3-15]:

1. An unmodulated parallel conductance path between source and drain.
2. Insufficient electrostatic shielding of the gap region from the drain field by the gate. This would occur for a high resistivity semiconductor if the source-drain gap is too small or the gate insulator is too thick.
3. Internal breakdown in the semiconductor channel in the high field region, which exists near the drain for drain voltages above the knee.
4. Insulator breakdown from the gate to the drain or to the channel near the drain.

Equation 3-3 is often used to determine the value of V_T. To determine V_T, the gate and drain of the TFT are shorted and the drain current is measured as a function of applied drain voltage (gate voltage). Because V_{ds} is equal to V_{gs} in this configuration, the TFT is in the saturation region of operation. A plot of $\sqrt{I_d}$ versus V_{gs} should be a straight line. Extrapolation of the line to abscissa gives V_T as shown in Figure 3-4. In fact, plotting $\sqrt{I_d}$ versus V_{gs} is the most widely used in determining the so-called extrapolated

threshold voltage value for a transistor. In this thesis, the threshold voltages of TFTs fabricated will be determined by this method.

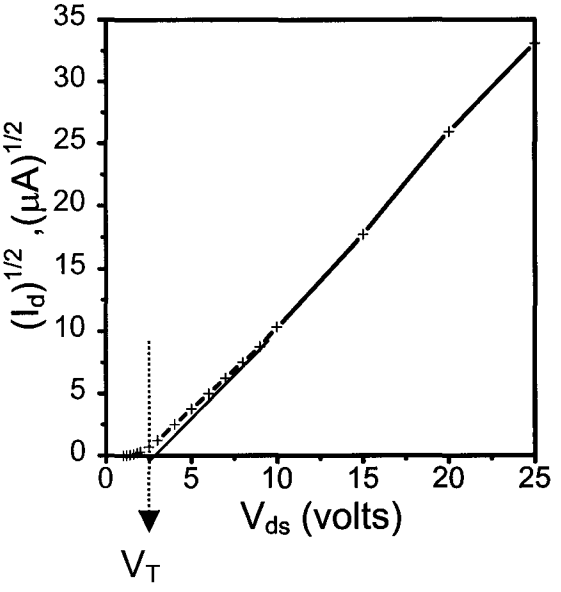


Figure 3-4 Typical plot of $\sqrt{I_d}$ versus V_{ds} for a TFT in saturation region.

The transconductance, g_m, in the saturated region is obtained by differentiating Equation 3.3 with respect to V_g.

$$g_m = \frac{\partial I_{dsat}}{\partial V_g} = \frac{CW\mu}{L}(V_g - V_T) = \left(\frac{2CW\mu I_{dsat}}{L}\right)^{1/2} \qquad 3.4$$

A plot of g_m^2 versus I_{Dsat} should yield a straight line. Fig. 3.5 shows such a plot for the TFT shown in Fig. 3-3.

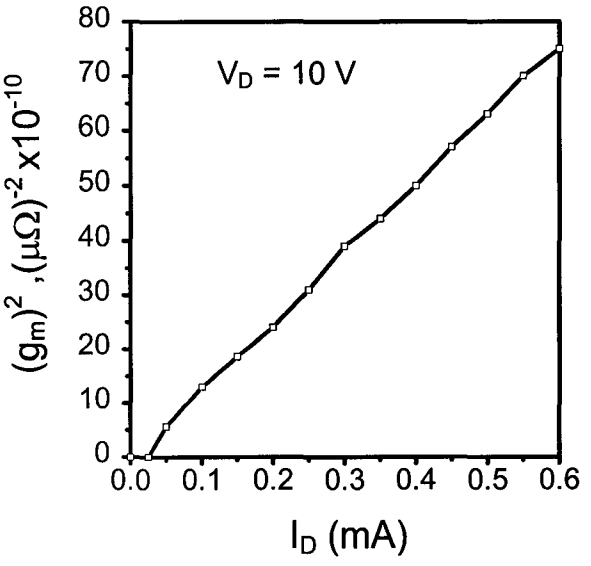


Figure 3-5 Dependence of transconductance on drain current in the saturated mode.

The output conductance, g_o, in the linear region is obtained by differentiating Equation 3.2 with respect to V_d.

$$g_o = \frac{\partial I_d}{\partial V_d} = \frac{CW\mu}{L}(V_g - V_T - V_d) \qquad 3.5$$

Thus, when the TFT is operated well below the onset of saturation, the output conductance is proportional to $(V_g - V_T)$.

High frequency performance of a transistor can be characterized by the gain-bandwidth product, $\frac{g_m}{2\pi C_g}$, where C_g is the total gate capacitance. In saturation, the gain-bandwidth product is given by:

$$gain - bandwith - product = \frac{\mu(V_g - V_T)}{2\pi L^2} \qquad 3.6$$

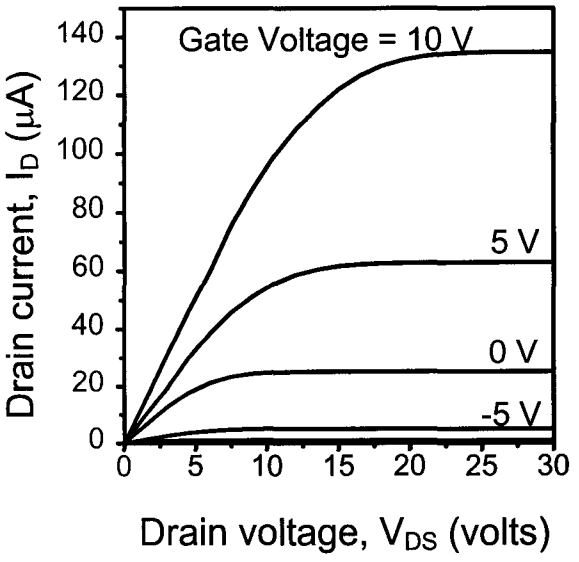


Figure 3-6 Typical output characteristics of the depletion-type TFT.

Another important parameter of the transistor is response time. The response time of the TFT, assuming a first-order approximation, is $\tau = \frac{L^2}{\mu(V_G - V_D)}$. This expression shows the importance of having a short channel length for the transistors. For a TFT with fixed geometry, the only other property, which can influence this parameter, is the carrier mobility. To achieve high gain-bandwidth products, the semiconductor should be fabricated so that it has near-single-crystal mobilities. It is also required to control the density of fast trapping states at the semiconductor-insulator interface.

Anderson [3-16] has shown that there is an optimum crystallite size for a given thin film semiconductor material which will allow one to achieve the best barrier modulation characteristics. This can generally be reached by controlling film thickness and a subsequent annealing treatment. In addition to enhancement mode, TFTs have been produced in the depletion mode. Such devices exhibit saturated characteristics with

sizeable drain current flowing without the gate voltage. The drain current may be reduced by applying a negative gate voltage or increased by a positive gate voltage. The drain current characteristics for a depletion-type TFT are shown in Figure 3-6.

For this TFT, the channel length is 20 μm and the width is 200 μm. The depletion-type TFT is useful for input, detector, and other applications where zero bias is desirable. For depletion-type TFTs, the drain current can be expressed as

$$I_d = \frac{\mu W C_{ox} V_T^{\ 2}}{2L} = \frac{\mu W n_o^{\ 2} q^2}{2LC_{ox}} \qquad 3.7$$

It is noted that I_d in the depletion-type TFTs can be made to be small even with semiconductors having a very high carrier density. This can be achieved by reducing the thickness of the semiconductor or increasing the capacitance of gate insulator. The large number of vacancies in polycrystalline compound semiconductor such as CdS or CdSe films may dominate its electrical properties. This is because the vacancies can ionize as donors or acceptors. For instance, if there is a Cd vacancy in CdS or CdSe then two neighboring S atoms may not complete the covalent bonding. Thus, two vacant states or holes may exist to permit conduction in the valance band. Hence, a Cd vacancy acts as an acceptor. On the contrary, an S vacancy acts as a donor.

After the first electron is removed from the Cd atom, the resultant positive charge on the Cd ion makes the removal of the second valance electron more difficult. Hence, two donor levels occur. However, the ionization energy associated with the second level (~0.6 eV for Se vacancy, ~1 eV for Cd vacancy) is greater than the first (~0.14 eV for Se vacancy, ~0.6 eV for Cd vacancy) and the contribution to the carrier concentration is negligible. The main reason why the vacancies control the conductivity of CdS and CdSe (rather than having a negligible effect as in Si and Ge) is due to the relatively large band gap (~2.4 eV for CdS, ~1.7 eV for CdSe). Due to the large bandgap, few carriers will be created by thermal generation. Thus, vacancies are the principal source of carriers in an undoped CdS and CdSe semiconductor. The reason why most of the CdS and CdSe

samples reported are n-type is due to the large differences in the ionization energies of the donor and acceptor levels in these materials. This is also consistent with the results obtained in the present work for CdSe and CdS prepared by the novel CBD method.

The maximum number of electrons per unit area, n_{max}, which may be induced or withdrawn from the semiconductor by the field effect, is independent of the insulator thickness and is dependent only on the dielectric constant (ε) and breakdown field strength (E_b) of the insulator:

$$n_{\max} = \frac{E_b \varepsilon}{q} \qquad 3.8$$

In a semiconductor, enhancement modulation will occur when $n_{\max} > n_t > n_o$, where n_o is the initial number of free carriers per unit area, n_t is the trapping states per unit area. Large number of surface states may render the injected charge immobile and prevent it from enhancing the conductance. Since the total charge induced, n_{in}, equals the sum of the increment of free and trapped charges, $\Delta n_{in} = \Delta n_c + \Delta n_t$, the transconductance varies as the fraction of induced charge, $g_m \propto \frac{\Delta n_c}{\Delta n_c + \Delta n_t}$.

In the presence of trapping, a mobility value less than the drift mobility is often observed; this is known as the field effect mobility, $\mu_{fe} = \mu \frac{\Delta n_c}{\Delta n_c + \Delta n_t}$. When the semiconductor contains many traps or surface states, the large fraction of trapped electrons may cause the drift mobility to be much smaller than the microscopic or Hall mobility by the factor: $\mu_{fe} = \mu \frac{\Delta n_c}{\Delta n_c + \Delta n_t}$. In this case, the drift mobility μ in the previous equations has to be replaced by the field effect mobility, μ_{fe}. The scattering properties of the surface are different from those of the interior because the surface represents a large discontinuity, In addition, it may contain a number of unoccupied surface states or traps which act as charged scattering centers and scatter more strongly

than the lattice. It can be readily known that too large a surface state density at the interface will also completely shield the space-charge region from the influence of the gate to allow carrier control action to be observed. Assuming an insulator layer (SiO_2 with a dielectric constant of 4) with a breakdown field of 10^6 volts/cm, the maximum carrier density which can be induced by the gate is approximately 2×10^{12} carriers/cm^2. The density of surface states having energy within a few kT of the Fermi level should therefore be considerably less than this value for effective modulation. It is apparent that the higher mobilities and fewer trapping states at the interface will permit lower fields and thicker insulator. The carrier concentration can be estimated by the majority carrier density and the related equation can be expressed as follows [3-17]:

$$N = -\frac{C^3}{q\varepsilon_s A^2 dC/dV} = \frac{2}{q\varepsilon_s A^2 d(1/C^2)/dV} \qquad 3.9$$

The subthreshold swing S, which is defined as the inverse slope of the I-V characteristics in a semi-log plot, $\frac{dV_g}{d(\log I_D)}$, is directly related to the ability of V_g to shift the Fermi level against the retardation of band-gap states. The interface state density N_i can be estimated by [3-18]

$$N_i = \frac{\varepsilon_{SiO_2}}{qt_{SiO_2}}\left(S\frac{q}{\ln 10kT} - 1\right) \qquad 3.10$$

where ε_{SiO2} = 4.0 x 8.854 x 10^{-14} F/cm, T is the temperature, k is the Boltzmann's constant. t_{SiO2} is the thickness of the gate insulator. Since TFT is a field effect transistor, the behavior is greatly influenced by the accumulation of electrons at the active layer surface. The initial number of free carriers, n_o (electrons or empty traps) evaluated by $V_T \equiv -n_o q/C$, the maximum number of electrons per unit area, n_{max} evaluated by Equation 3.8, the carrier concentration evaluated by Equation 3.9, and the interface state density evaluated by Equation 3.10 are all important parameters for TFTs. These will be

calculated for the TFTs developed in the present work and presented in Chapter 6 and 7. The condition for enhancement modulation when $n_{max} > n_t > n_o$, will be also examined.

3.3 Characteristics of the CdSe and CdS-based Metal-Insulator-Semiconductor (MIS) Structures

The first task to develop a new metal-insulator-semiconductor transistor is to construct an energy-band diagram. When a semiconductor such as a doped Si is used as the "metal" gate, fine-tuning of the band diagram is possible. The metal-insulator-semiconductor system is useful in understanding several important integrated-circuit structures: most notably the thin film transistors discussed previously. The discussion of the MIS system in this section (in a form of n^+-Si/SiO_2/CdS) will help us to focus on the physical electronics that underlies the operation of TFTs. In this discussion, we will adopt the silicon dioxide-CdS system. The method for the oxide-CdS system may also apply to structures with other insulator materials and semiconductors.

To derive an energy-band diagram for the n^+-Si/SiO_2/CdS system, which is one of the TFT structures used in this thesis, we start from the basic principles that have been developed for conventional metal/oxide/semiconductor (MOS) devices. Under thermal equilibrium conditions, Fermi energies in all materials are constant. For instance, for the three-component system, the Fermi level in all three materials are constant. We shall first idealize the MOS system by neglecting charges at the interfaces. When an MOS structure is formed, the Fermi levels in the various materials are equal due to the transfer of negative charges from the material with a smaller work function to the material with a larger work function.

In Figure 3-7, a general system of Al (work function, $q\phi_m$ = 4.2 eV), silicon dioxide (electron affinity $q\chi_{ox}$ = 0.95 eV), and CdS (electron affinity, $q\chi_{CdS}$ = 4.794 eV

and work function, $q\phi_{CdS}$ = 5.01 eV) is considered. These parameters obtained from the table in the Handbook Series on Semiconductor Parameters (World Scientific, 1996-v) are typical values. The vacuum level is designated as E_O, and the various energies when these materials are separated are indicated. When these materials form a single system, negative charges will be transferred from the Al into the CdS because the work function of the Al is 0.81 eV less than the work function of the CdS. Modified work function is also used to describe the system. The modified work function is defined as the minimum energy required to bring an electron from the Fermi level in the gate metal or the semiconductor to the conduction-band edge of the oxide. Therefore, the work function difference between the Al and CdS is 0.594 eV.

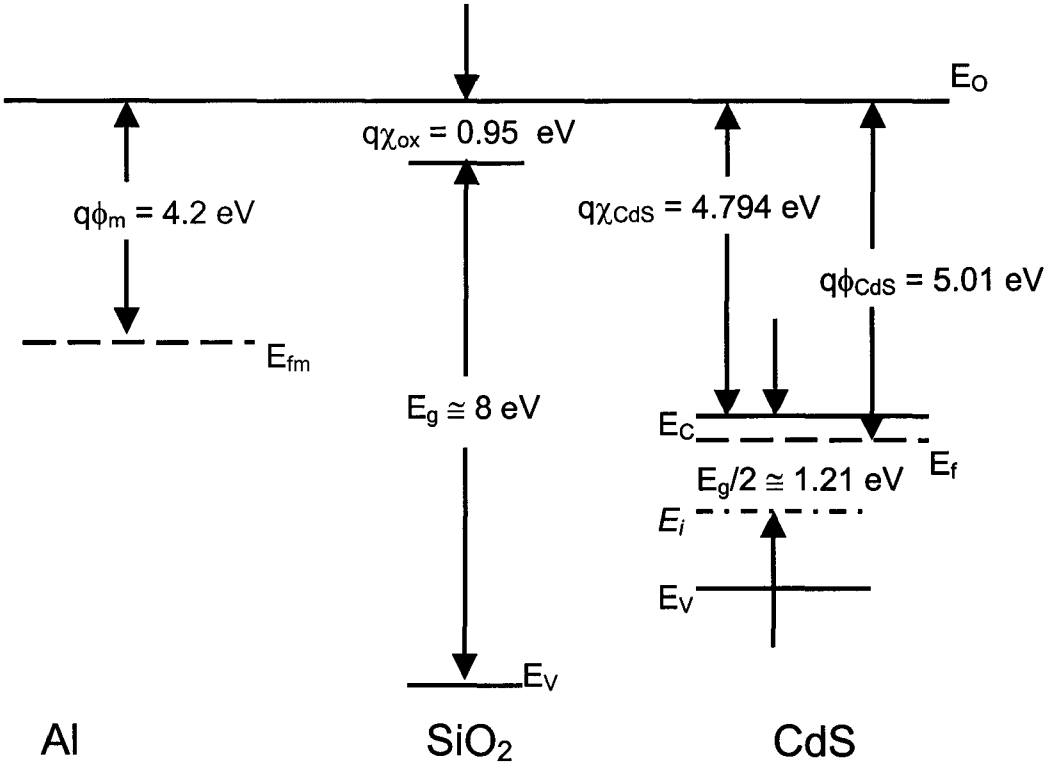


Figure 3-7 Energy levels in three separated components that form an MOS system: Al, thermally grown SiO_2, and chemical bath deposited CdS.

Under thermal equilibrium conditions, the simplified band diagram for the Al – SiO_2 – CdS structure shown in Figure 3-7 is given in Figure 3-8. The vacuum level, which plays no significant role in most device analysis, has been omitted.

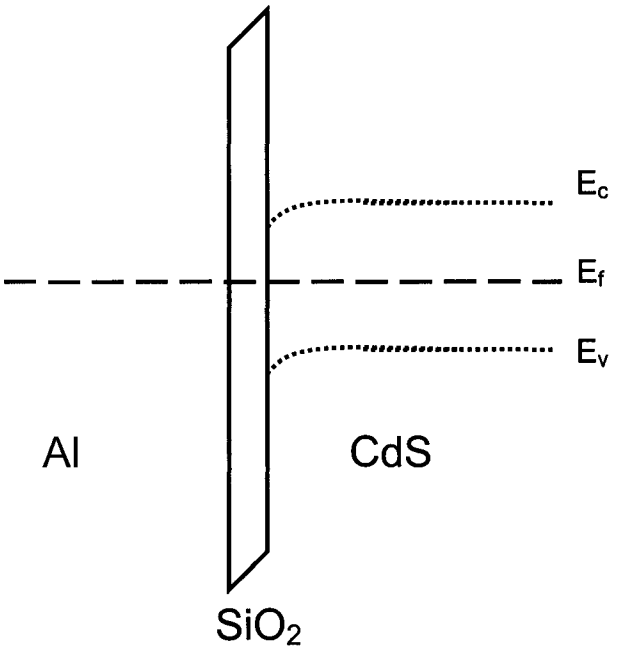


Figure 3-8 A simplified energy band diagram in the three-component MOS system: n^+-Si, thermally grown SiO_2, and chemical bath deposited CdS.

The energy band diagram For CdSe-TFT is similar to that for the CdS-TFT. The only differences are the values of energy gap, electron affinity, and work function. When an n^+-Si is used as a gate electrode, the band diagram will be modified as shown in Figure 3-9. Band diagrams can be easily established for other material combinations such as: $Al/Al_2O_3/CdS$ (or CdSe)-TFT, n^+-Si/SiN/CdS (or CdSe)-TFT and n^+-$Si/SiO_2/CdS$ (or CdSe)-TFT and will not be repeated here.

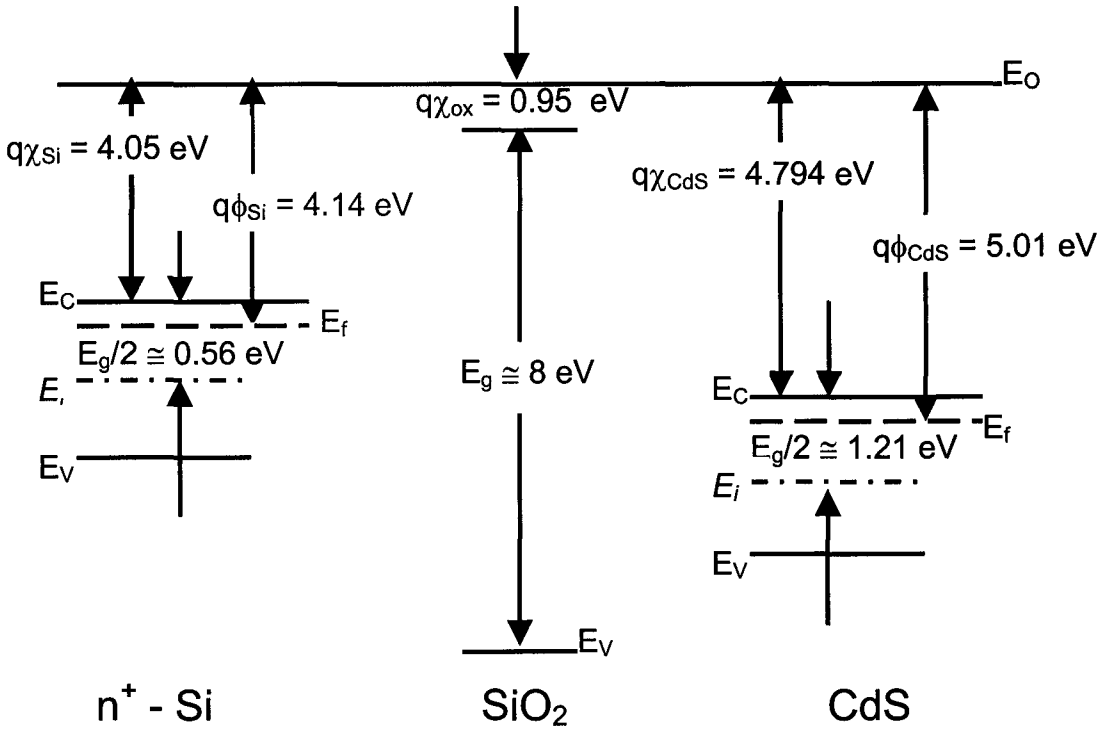
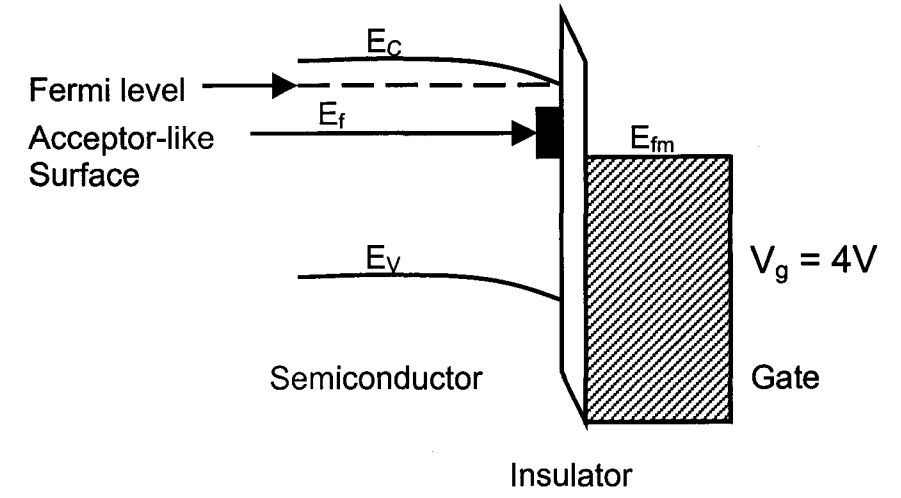


Figure 3-9 Energy levels in three separated components that form an MOS system: n^+-Si, thermally grown SiO_2, and chemical bath deposited CdS.

At the surface of a semiconductor, atoms cannot complete regular bonding. Consequently, new energy levels within the normally forbidden energy gap are formed. These levels are known as surface states. Figures 3-10 and 3-11 show how the presence of donor-like and acceptor-like surface states at the interface will affect the shape of the bands. Contact potential difference due to the work function of the gate may also play a role. A high density of acceptor-like states or deep traps will bend the bands upward as shown in the Figure 3-10. If this happens, a positive gate bias is required to induce the depletion layer into the otherwise accumulated layer. This condition results in an enhancement type TFT with a positive V_T. A high density of donor-like states at the

interface creates an accumulation layer even at zero gate bias as shown in Figure 3-11. A current may flow when a voltage is applied. To pinch off this current, a negative gate bias corresponding to a negative V_T is required. Since their energies are lower than the conduction band edge, they can act as traps for electrons. Electrons in these traps are rendered immobile and can neither diffuse thermally nor drift with an applied field until they are released.

Surface states play an important role in TFTs by influencing the value of V_T. In the equation $V_T = -n_o q / C$ for a depletion-type TFT, n_o represents the total numbers of free electrons per unit area initially present in the active layer. While in an enhancement-type TFT, n_o represents the number of unfilled traps or surface states per unit area initially present. If the semiconductor has a low resistivity the gate must be able to deplete the entire thickness of the active layer to obtain saturation operation. If the semiconductor is highly resistive with the conduction region confined to the accumulation layer at the surface, only this surface layer needs to be depleted. Normal operation of a TFT requires a source contact having low impedance for injection of majority carriers. With a suitable low resistance contact at the source, current densities of the order of tens or hundreds of amperes per square centimeter can be drawn for the CdS or CdSe film in spite of their high resistance. For the overlying source and drain contacts, Al is superior to Au for CdS or CdSe. This is due to the formation of a blocking contact on top of the CdS or CdSe film during Au contact evaporation, resulting from excess Cd atoms in the contact area [3-15]. Failure to achieve a good ohmic contact at the source electrode will give a low transconductance. Al has been chosen to make ohmic contacts in the thermally evaporated CdS and CdSe films. In this work, Al will be used as the metal contacts for the source and drain of TFTs.



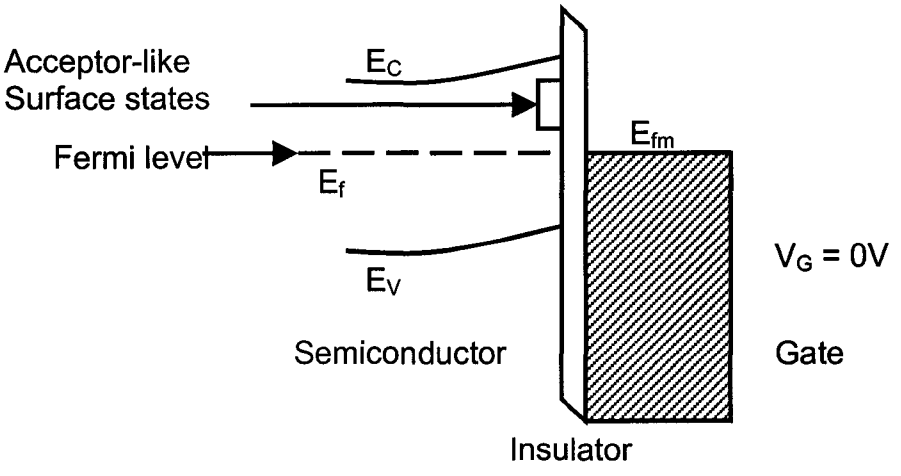


Figure 3-10 Effect of acceptor-like surface states upon the semiconductor energy bands at the insulator interface in enhancement-type TFTs.

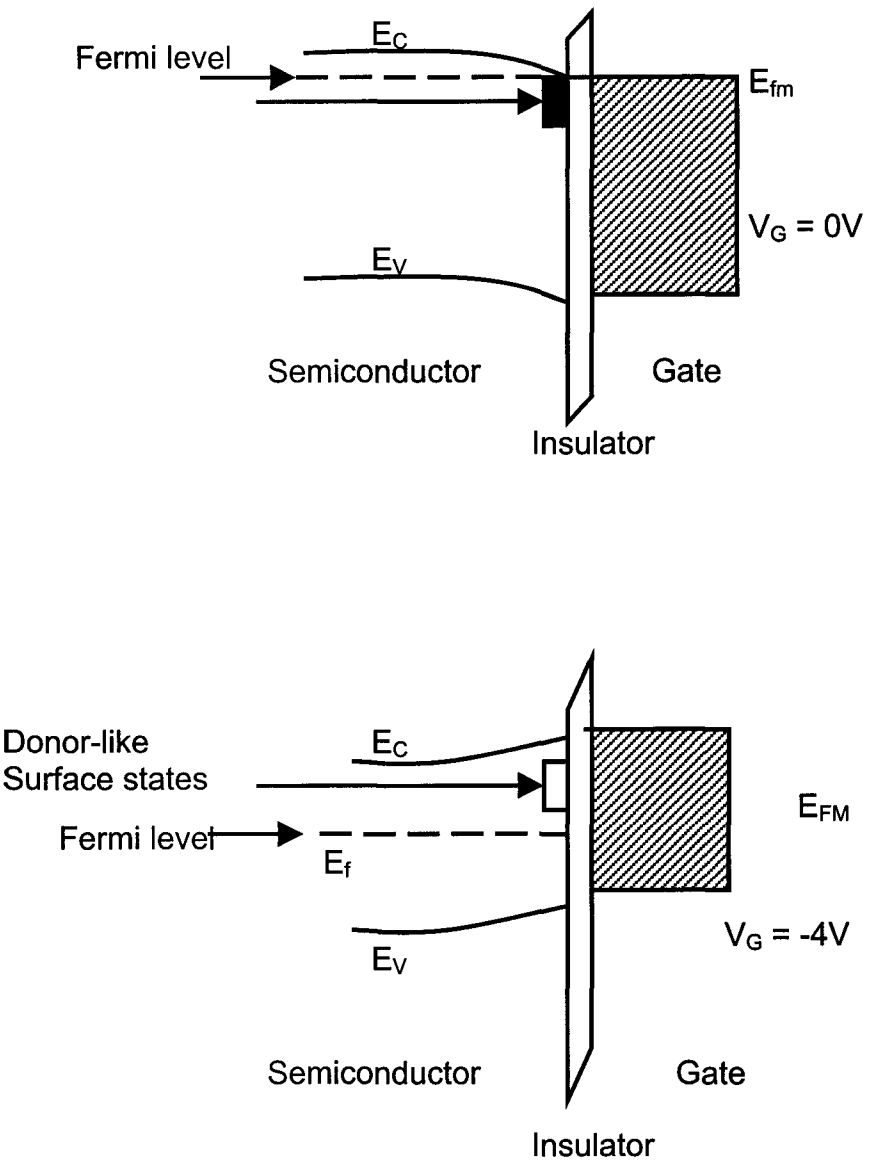


Figure 3-11 Effect of donor-like surface states upon the semiconductor energy bands at the insulator interface in depletion-type TFTs.

Figure 3-12 shows an energy band diagram for the contacts used at the source and gate electrodes in a TFT. At zero bias in an enhancement mode device, the bands should bend upwards at the semiconductor-insulator interfaces as shown in the Figure. When a positive voltage is applied, electrons are drawn toward the interface, causing the bottom of the conduction band at the interface to be lowered relative to the Fermi level and giving a highly conducting channel close to the insulator surface.

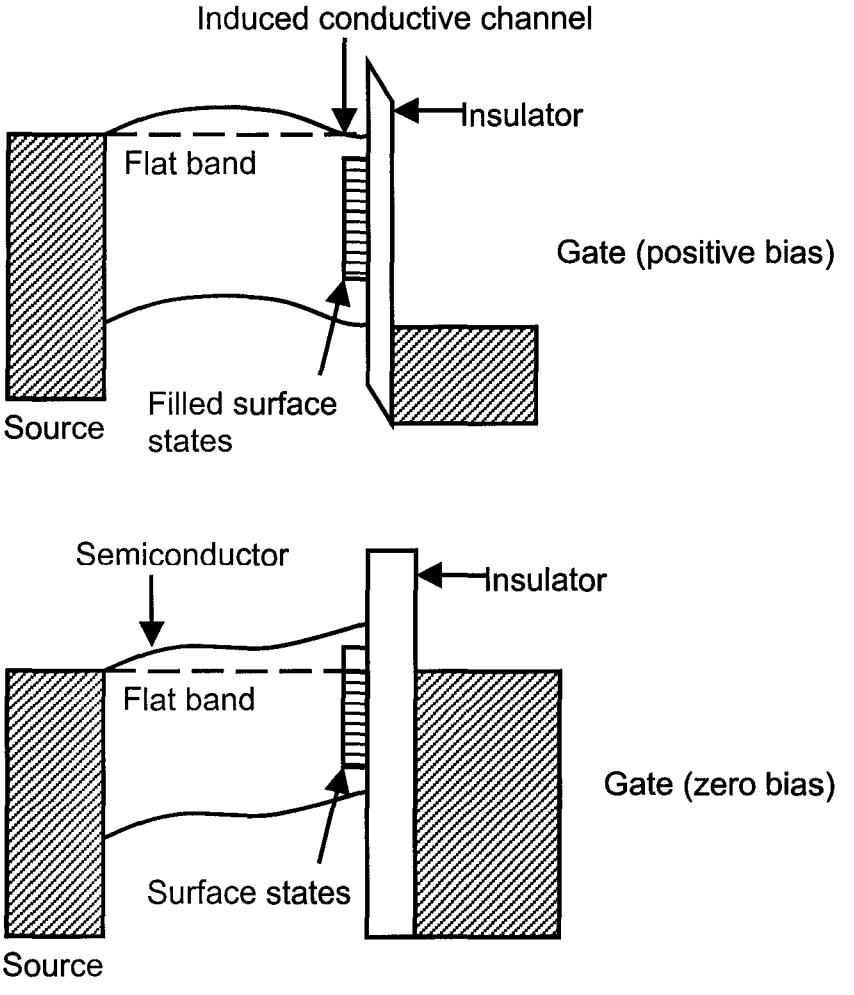


Figure 3-12 Energy band diagrams of the ohmic source contact and the gate-insulator contact in a TFT designed for an enhancement mode operation.

3.4 Conclusions

In this chapter, the basic theory and operation principles for TFTs have been described. The energy band diagrams for MIS TFTs, SISs TFTs have been given with CdS and CdSe as specific examples of the active material layers. The important parameters for TFTs such as threshold voltage, transconductance, conductance, and gain-bandwidth-product have also been described. From the theory, it is clear that the most important processes will be the formation of thin gate insulator layers and the formation of the active semiconductor layers. The insulator layers should be thin enough and with high enough breakdown field so that they can sustain the gate voltage applied. The carrier density and uniformity of the active semiconductor layers must be precisely controlled. This is required so that surface layer may be accumulated upon the application of the gate voltage. More importantly, all these processes need to be carried out at low temperatures so that low cost substrates such as glass plates may be used. It is also noted that although the basic equations for the TFTs are the same as that for MOSFETs, the role of interface states and trapped charges is more important. Hence, it is equally important to control the density of interface charges of the active semiconductor during the fabrication. During the development of the TFTs employing the novel CBD method in this work, the results will be compared with the theory in order to extract information needed for the improvement of the processes and devices.

References

1. P. K. Weimer, "The TFT-a new thin-film transistor," Proceedings of The IRE, Vol. 50, pp. 1462-1469, 1962.

2. T. P. Body and D. J. Page, "Flexible thin film transistors," Elecronics, pp. 100, 1968.

3. P. K. Weimer, Phys. Thin Films, Vol. 2, pp. 147, 1964.

4. W. B. Pennebaker, Solid-State Electron., Vol. 5, pp. 509, 1965.

5. V. L. Frantz, Proc. IEEE, Vol. 53, pp. 760, 1965.

6. J. F. Skalski, Proc. IEEE, Vol. 53, pp. 1792, 1965.

7. C. A. T. Salama and L.Young, Proc. IEEE, Vol. 53, pp. 2156, 1965.

8. P. K. Weimer, G. Sadasiv, L. Meray-Horvath and W. S. Pike, Proc. IEEE, Vol. 55, pp. 1591, 1967.

9. A. G. Fischer, "Design considerations for a future electroluminescent TV panel," IEEE Trans. Electron Devices, Vol. ED-18, pp. 802, 1971.

10. T. P. Brody, J. A. Asars, and G. D. Dixon, "A6x6 inch, 20 lines per inch liquid crystal display panel," IEEE Trans. Electron Devices, Vol. ED-20, pp. 995, 1973.

11. F. C. Luo, W. A. Hester, and T. P. Brody, "Alphanumeric and video performance of a 6x6 inch, 30 lines/inch TFT-LC display panel," SID Symp. Dig., pp. 94, 1978.

12. F. C. Luo and W. Hester, Trans. Electron Devices, ED-27, pp. 223, 1980.

13. F. C. Luo et al., SID 87 Digest, pp. 286, 1985.

14. W. Shockley and G. L. Pearson, Phys. Rev., Vol. 74, pp. 232, 1949.

15. J. C. Anderson, Thin Solid Films, Vol. 38, pp. 151, 1976.

16. H. Borkan and P. K. Weimer, "An analysis of the characteristics of insulated-gate thin film transistors," RCA Review, Vol. 24, pp. 153-165, 1963.

17. D. K. Schroder, "Semiconductor material and device characterization," Book published by John Wiley & Sons, INC, 1998.

Chapter 4

Fabrication Procedures and Experimental Set-Up

The fabrication processes developed in this work for TFTs will be described in this chapter. In these processes, four photo-masks are used. Since the exact fabrication steps will be dependent on the substrates used, a procedure for the fabrication of TFTs on Si substrates and a procedure for devices on glass substrates will be presented in this Chapter. Both procedures are designed for the fabrication of TFTs with an inverted gate-staggered electrode configuration.

4.1 Fabrication procedure for TFTs on Si substrates

In the procedure shown in Figure 4-1(a), an n-Si (100) is used as the substrate. A thermal diffusion process (n^+ dopant with Phosphorosilicafilm with a concentration of 10^{20} cm^{-3} from Emulsitone Corp.) is first used to form an n^+ diffused gate region in the substrate. After this, a thin layer of gate oxide is grown by thermal oxidation. Thickness of this gate oxide is about 60~100 nm. A layer of semiconductor (CdS or CdSe) is then deposited over the entire substrate surface by a chemical bath deposition method (CBD). Detailed description and discussion for the CBD method will be presented in Chapter 5. The deposited semiconductor film is selectively etched by photolithography and an etching method to create active channel region for the thin film transistor. After the selective etching, a layer of metal (Al) is evaporated over the entire surface. A lift-off process is needed to form drain and source contacts, since diluted HCl etching solution used for contact etching will also attack the semiconductor films. After the formation of the metal contact, a heat treatment is carried out to form ohmic contacts. The annealing conditions used for as-deposited CdSe and CdS films are: annealing temperature about 400 °C, annealing time 3 ~ 6 minutes, and in N_2 ambient. The detailed TFT-fabrication procedure on Si substrate developed in this thesis is described as follows:

1. Cut n-type Si wafer into appropriate size using diamond scriber

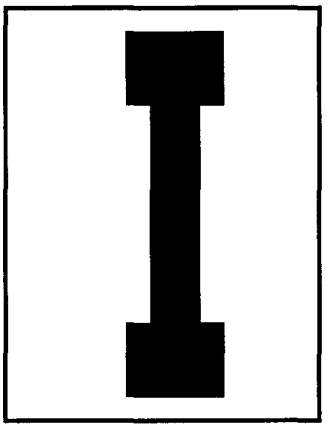
2. Carry out a cleaning process for Si substrate:

3. Perform wet oxidation process (thermally grown $SiO_2 \sim 0.8$ μm):

4. Carry out the first photolithography process using mask #1:
   a) Apply 3~5 drops of Shipley AZ-1400 onto the wafer using pipette
   b) Align and expose to UV light (Oriel Corp. Model 87100, Timer control, 77510 Dual Fiber Optical Illuminator, 68810 ARC-Lamp power supply 200~500 Watt Hg, Wavelength 436 nm G-line, power output at 300W) for 120 seconds
   c) Develop with Shipley developer

d) Post-bake the wafer at 115°C for 15 minutes

e) Carry out window opening process by immersing the wafer in buffered HF solution



Mask #1 for gate diffusion

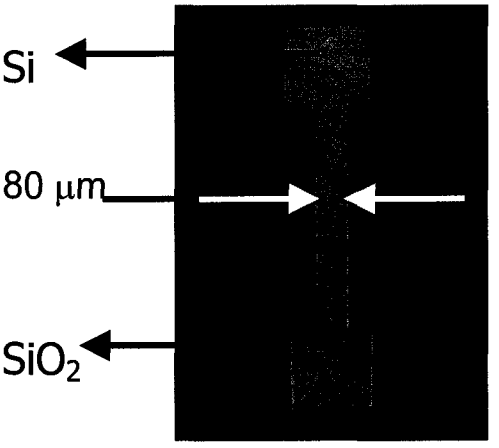


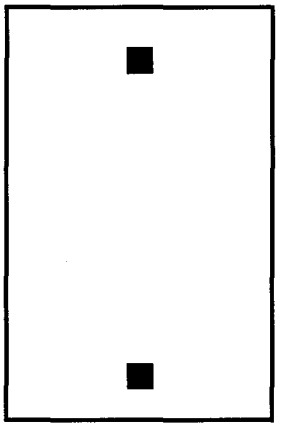
Figure 4-2 Photo for TFT after Mask #1

5. Perform diffusion process in the furnace for 1.5 hours at 1100°C:
   a) Apply dopant (Phosphorosilicafilm, Emulsitone Corp., Concentration 10^{20} cm^{-3}) to the wafer 2 or 3 drops using pipette

6. Remove dopant and oxide using buffer HF etching solution

7. Do gate oxidation process (thermally grown gate oxide 600~1000 Å):

8. Carry out the second photolithography process and window opening for gate using mask #2:



Mask #2 for gate contact

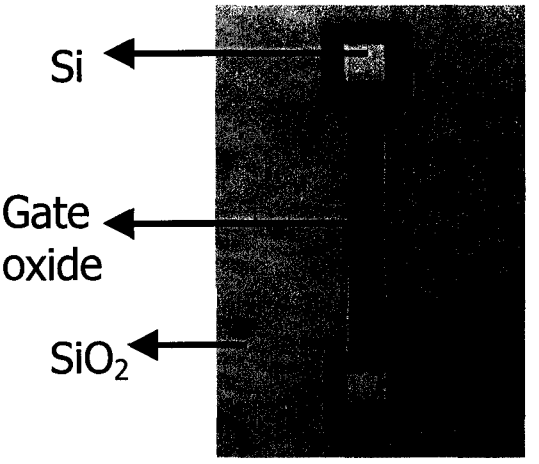


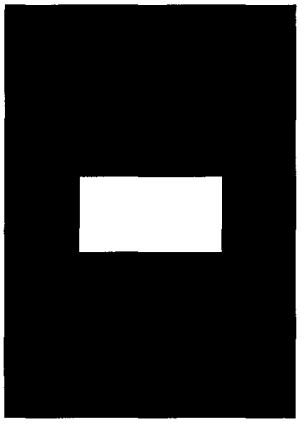
Figure 4-3 Photo for TFT after Mask #2

9. Perform CBD (chemical bath deposition) process:
   a) Prepare CdS solution A and B
      A) $CdCl_2$ (Fisher $CdCl_2$. 2.5 H_2O, 80.1%): [5.092×10^{-3}M]
      Thiourea (Fisher-T101 NH_2CSNH_2, 99.6%): [47.30×10^{-3}M]
      NH_4Cl (J.T.Baker Granular, 99.9%): [52.34×10^{-3}M]
      DI water:
      B) NH_4OH (Caledon Lab. LTD code 1525-1,
      1 L = 0.9 kg, NH_3: 28~30%): [0.7868 M]
      DI water:
      Prepare CdSe solution C, D and E
      C) $CdCl_2$ (Fisher $CdCl_2$. 2.5 H_2O, 80.1%): [1.0×10^{-1}M]
      DI water:
      D) Na_2SO_3: [1.0 M]
      Se powder: [0.1 M]
      DI water:
      Stirring at 80°C for 4 hours
      E) NH_4OH (Caledon Lab. LTD code 1525-1,
      1 L = 0.9 kg, NH_3: 28~30%): [6.5 M]
      DI water:
   b) Adjust relative ion concentration – CdS solution A and B (1:1)

Relative ion concentration – CdSe solution C and D (1:1), and E (1~5 ml)

c) Put beakers on the hot plat (Fisher Thermix with Stir-2 and Temperature Adjustment-5, 4, 3), Temperature range – 60 ~ 80°C

10. Carry out the third photolithography process for CdS, CdSe pattern using mask #3:



Mask #3 for active layer

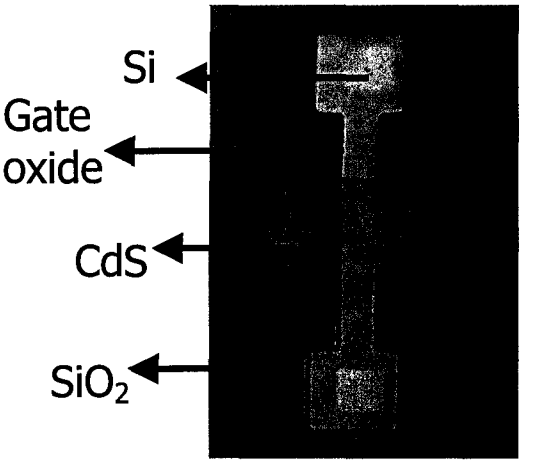
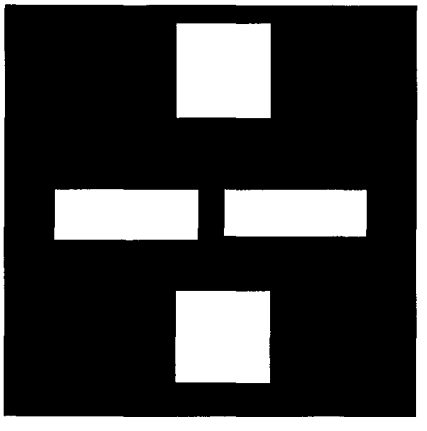


Figure 4-4 Photo for TFT after Mask #3

11. Perform Al lift-off process for drain, source contact using mask #4:



Mask #4 for electrodes

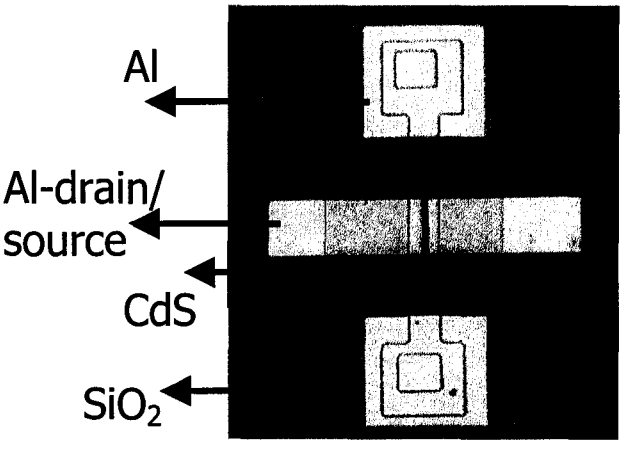


Figure 4-5 Photo for TFT after Mask #4

12. Carry out a heat treatment process:

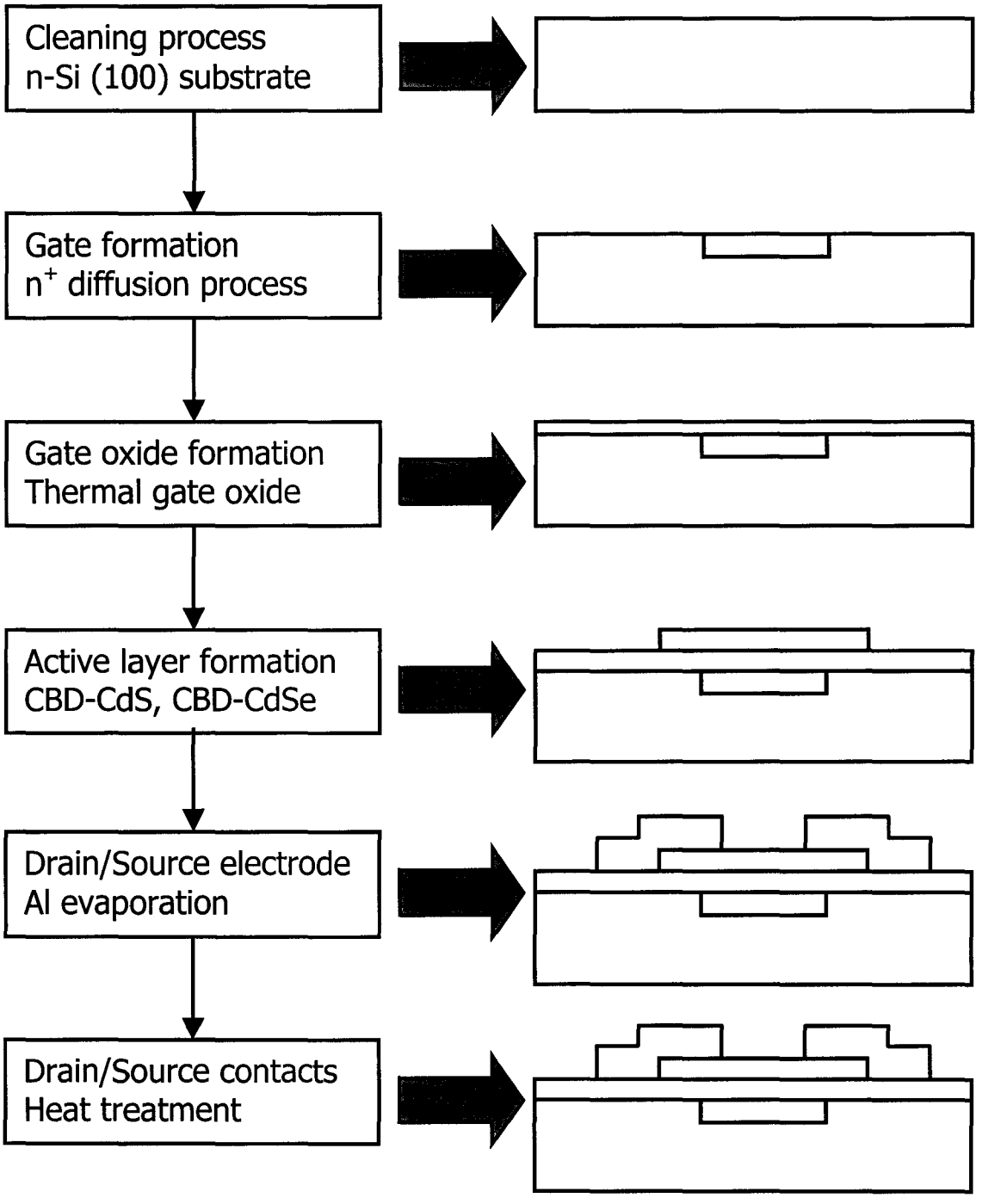


Figure 4-1(a) A schematic diagram showing the fabrication procedure for CdS-TFTs and CdSe-TFTs based on Si substrate and thermally grown oxide for gate insulator.

4.2 Fabrication procedure of TFTs on glass substrates

The incorporation of the thermal oxidation process for the fabrication of TFTs described in previous section is useful for studying the properties and deposition of active semiconductor layers. However, it may not be suitable for large-scale production. This is because the high temperatures involved and the thermal requirements of the substrate. To reduce the process temperatures and the requirements for substrates, it is necessary to employ methods other than thermal oxidation for gate oxides. One of these methods involves anodization. In this work, in addition to thermal oxidation, the anodization method will be used to form gate oxides. In addition, some samples were prepared with thin gate dielectric films by magnetron-sputtering method. Specifically, gate insulators of Al_2O_3, Ta_2O_5 prepared by anodization and SiN_x by magnetron sputtering have been prepared and studied. The details and the results will be presented in Chapter 7. Using the anodized or sputtered insulators, a fabrication procedure for TFTs on glass substrates has been established. This is shown in Figure 4-1(b) where a conventional glass substrate is used instead of monocrystalline Si. Figure 4-6 shows a top view of one of the TFTs fabricated in this work.

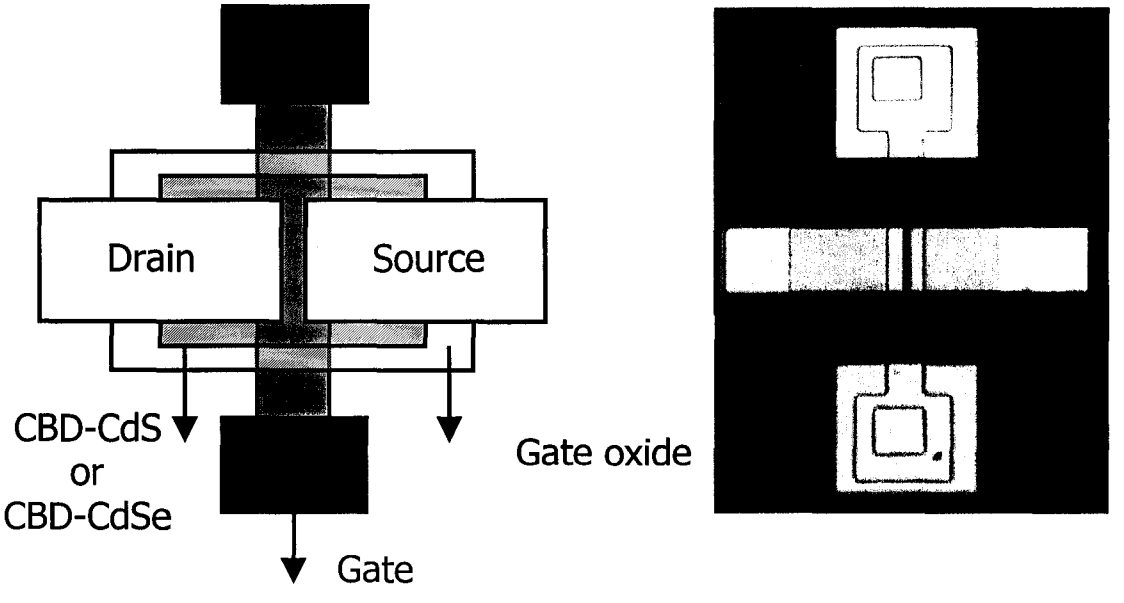


Figure 4-6 A top view of the TFT.

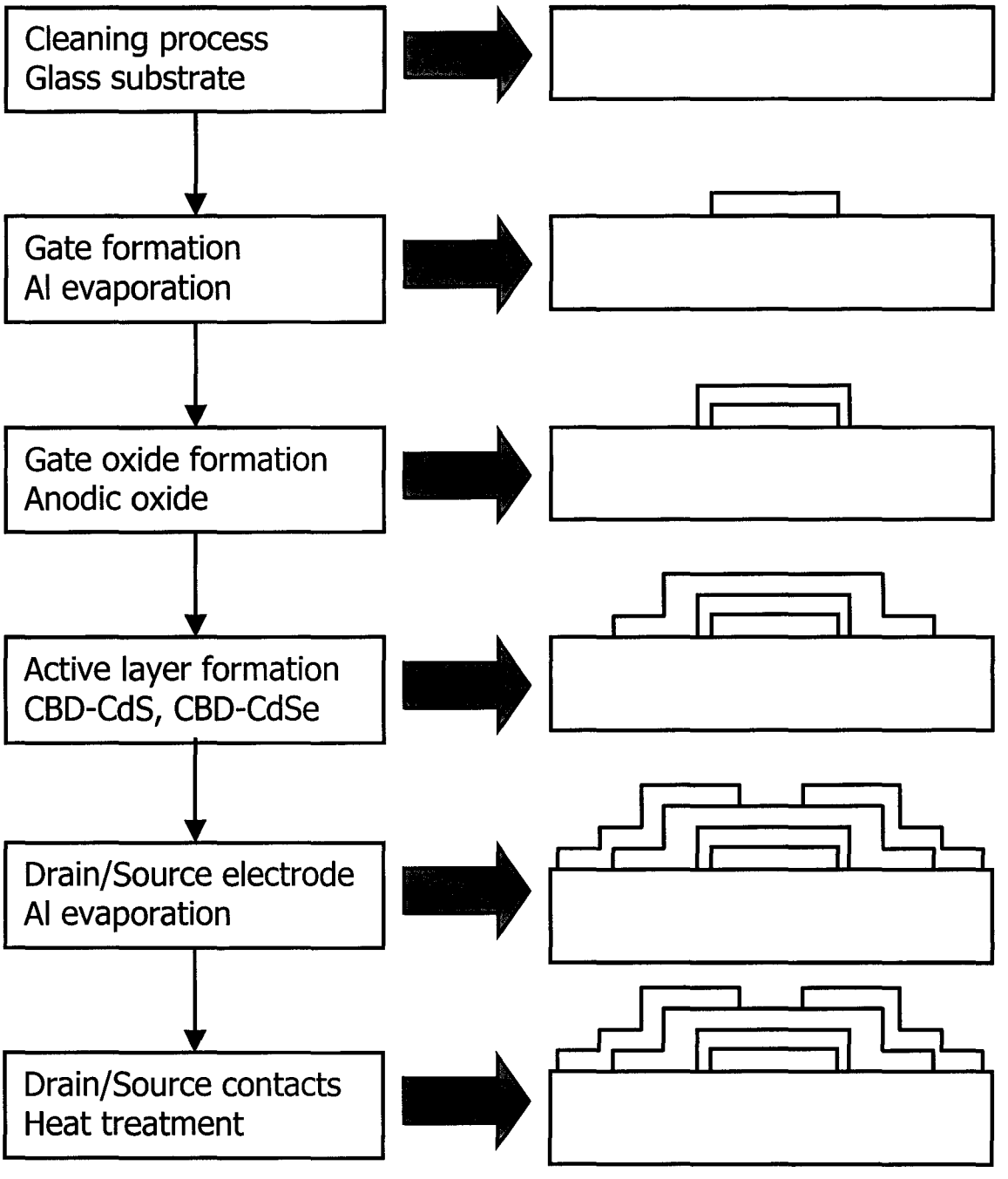


Figure 4-1(b) A schematic diagram showing the fabrication procedure for CdS-TFTs and CdSe-TFTs on glass substrates with anodic oxide or sputtered nitride for gate insulator.

The detailed TFT-fabrication procedure on glass substrate is very similar to those described in the previous section on Si substrate. Hence, the procedure will not repeated in this section. The simplified description in the procedure shown in Figure 4-1(b) is presented instead in the following. A metal is first deposited on a glass substrate to form a gate region. After this, a thin layer of gate oxide is formed by anodization. Detailed anodization process will be presented in Chapter 7. Thickness of the gate oxide is about 100~300 nm. A layer of semiconductor (CdS or CdSe) is then deposited over the entire sample surface by a chemical bath deposition method. Detailed description and discussion for the CBD method will be presented in Chapter 5. The deposited semiconductor film is selectively etched by photolithography and etching method to create active channel region of the thin film transistor. After the selective etching, a layer of metal (Al) is evaporated over the entire surface. The lift-off process is needed to form drain and source contacts, since the diluted HCl etching solution will also attack the semiconductor films and anodic oxides. After the formation of the metal contact, a heat treatment is carried out to form ohmic contacts. The annealing conditions used for the as-deposited CdSe and CdS films are: temperature about 400 °C, time 3 ~ 6 minutes in N_2 ambient. The detailed TFT-fabrication procedures on Si substrate can be applied to glass substrate with certain modifications on conditions of substrate cleaning and gate oxide formation.

The cleaning step for glass substrates is very important for obtaining uniform metal films with good adhesion. The uniformity and adhesion of the metal films are required for the subsequent anodization process.

The substrate cleaning process is as follows [4-1,2,3]:

(1) wash with Liquinox soap
(2) put the beaker containing the substrate and Liquinox soap solution in an ultrasonic bath
(3) rinse in DI water
(4) soak in chromic acid

(5) immerse the substrate in a beaker with ACE and put the beaker with substrate in an ultrasonic bath

(6) immerse the substrate in a beaker with DI water and put the beaker with substrate in an ultrasonic bath

(7) rinse in deionized water

(8) immerse in boiling DI water until used

To form Al_2O_3 gate dielectric, a layer of Al (~0.8 um) is deposited by thermal evaporation. For Ta_2O_5 gate dielectric, a layer of Ta film (~0.6 um) deposited by DC magnetron sputtering is employed. It is noted that in the TFT fabrication procedure on Si, an n^+-diffused region is used as the gate. Due to the nature of the anodization process, only the surfaces of the metal layer are covered by the anodic oxide as shown in Figure 4-1(b).

The Al or Ta-coated glass substrates were then used in anodization using the unit as shown in Figure 4-7.

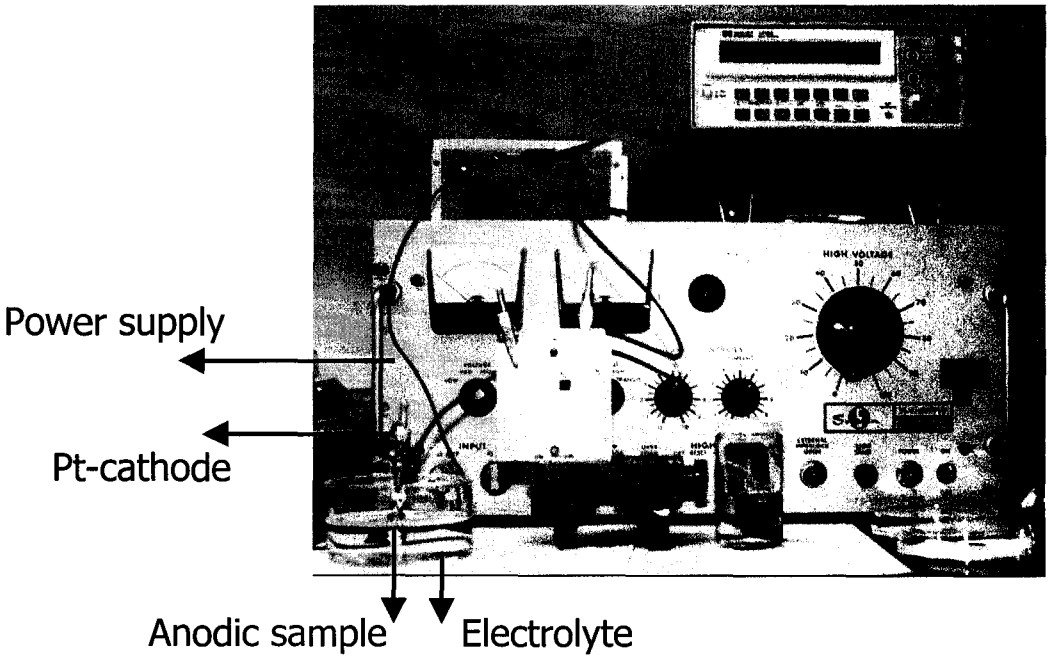


Figure 4-7 Experimental setup for anodization process.

The electrolyte used is an ethylene glycol solution mixed with the tartaric acid. The cathode is made of Pt, while the anode is one of the Al-coated samples. When a voltage is applied between the Pt (negative) and Al or Ta/glass (positive), some of H_2O molecules are electrolyzed into hydrogen ions and oxygen ions near the electrode surfaces. Hydrogen ions will react with the electrons from the cathode (Pt) and form H_2 gas. Oxygen ions will react with the ions of aluminum created by the release of electrons from aluminum atoms.

To maintain constant electrical current, the bias voltage needs to be increased. After a predetermined voltage (80~200 V) has been reached, the voltage will be kept constant while the current density (0.1~2.1 mA/cm^2) will be allowed to decrease until the anodization reaction is completed. After the formation of the first Al_2O_3 or Ta_2O_5 layer, subsequent anodization of underlying metal is achieved by the transport of ions of aluminum, ions of oxygen, or both through the first anodized film. The transport of the ions through the anodic film will be aided by the applied electric field, which is established in the film by the voltage applied between the anode and cathode. The detailed anodization process and mechanism will be presented in the Chapter 7. In addition, TFTs will also be fabricated using sputtered SiN_x for comparison with thermally grown oxide and anodic oxides. This will also be presented in Chapter 7.

References

1. M. E. Rincon, M. Sanchez, A. Olea, I. Ayala, P. K. Nair, "Photoelectrochemical behavior of chemically deposited CdSe and coupled CdS/CdSe semiconductor films," Solar Energy Materials and Solar Cells, vol. 52, pp. 399-411, 1998.

2. K. Tapan and D. Jim, "Anomalous transport properties in CdSe films," Solar Energy Materials and Solar Cells, vol. 27, pp. 327-334, 1992.

3. I. O. Oladeji and L. Chow, "Optimization of chemical bath deposited cadmium sulfide thin films," J. Electrochem. Soc., vol. 144, pp. 2342-2346, 1997.

Chapter 5

Chemical Bath Deposition

5.1 Introduction

Several methods have been developed and used for the preparation of large area thin films. These include thermal evaporation, sputtering, CVD, spray pyrolysis, screen-printing, electrochemical deposition and chemical bath deposition (CBD). The chemical bath deposition method has been used in the past to make polycrystalline films of CdS, CdSe, PbSe, etc. [5-1] for photovoltaic applications. This method is particularly suited for the fabrication large area electronic circuits and devices. The reason for this is partly due to the simple and inexpensive equipment involved and partly to the short processing time. This method is particularly appropriate for II-VI semiconductor compounds. Using this technique, thin films can be deposited on a variety of substrates including insulators, semiconductors, and metals. Chemical bath deposition is often carried out in an aqueous solution containing specific chemicals and ions. This may include sources for hydroxide, sulfide or selenide etc. The basic principles underlying the chemical bath deposition of semiconductor thin films have been presented in the recent review articles [5-2,3]. The main emphasis of previous CBD work reported in the literature is on the development of photoelectrochemical solar cells for energy conversion, where the main requirement is to form large area junctions.

If the CBD method can be developed to produce active semiconductor layers for thin film transistors, then the fabrication cost for circuits requiring large area substrates may be reduced. In this section, results of exploratory work carried out on the CBD deposition of II-VI compound semiconductor thin films will be described.

5.2 Selection of materials for the chemical deposition bath

In CBD process, the precipitation of compound semiconductors is controlled through the use of suitable complexing agents and the amount of ions. One complex agent used for metal ions is triethanolamine. The control of the amount of sulfide, selenide, or hydroxo ions in the bath further allows controlled thin film deposition to take place. Another condition for the precipitation is the availability of nucleation centers on the substrate. Such centers are normally formed through the adsorption of metal hydroxo species. In the initial phase of CBD, the hydroxo group would be substituted by the sulfide or selenide ions, which would thereby form an initial layer of the metal chalcogenide. The deposition of the thin film takes place through the condensation of the metal and sulfide/selenide ions on this initial layer, which act as a catalytic surface. Generally, the following description gives specific deposition processed for CdSe and CdS films based on the previous general description. The formation of films by CBD is truly a deposition of compound rather than co-deposition of separate elements. A literature survey shows very few CBD work [5-2] reported on the preparation of CdS for thin film transistors and no research work has been done on CdSe films by CBD method.

For the deposition of CdSe, compound materials such as selenourea and sodium selenosulfate are used to furnish selenium ions by hydrolysis in alkaline solution [5-3,4]. Selenourea solution is very unstable and has to be stabilized using antioxidants like sodium sulfite, which cannot be synthesized easily. Sodium selenosulfate can be synthesized easily by dissolving selenium in a sodium sulfate solution. In addition, the

resulting solution is fairly stable, which will be used as a selenium ion source for CBD process instead of selenourea in this work.

In the present work, thin films of CdSe were deposited on substrates by using a solution growth technique involving the reaction of Se^{2-} with Cd^{2+} in the solution. The precipitation is controlled by slowly generating ions that are in equilibrium with a chalcogenide precursor and a cation complexing agent, usually NH_3. In order to optimize conditions for deposition of CdSe films using selenosulfate solution, cadmium salt and sodium selenosulphate solutions are mixed in various ratios. Deposition experiments were then carried out and films with different compositions were obtained. It is noted that the growth is highly dependent on temperature and concentration of complexing agent. The models, reaction kinetics, effects of various preparative parameters and the role of complexant on the formation of CdSe films have been described by Kainthla et al. [5-1].

The preparation of chemical bath starts from the preparation of stable Na_2SSeO_3. Elemental selenium (99.99 %) is first dissolved in an aqueous solution of sodium sulfate at 75 °C to form a stable Na_2SSeO_3 compound. Weighted amount of the solution is then mixed with stoichiometric amount of a complex of cadmium for the deposition of CdSe films. In the solution, Na_2SSeO_3 yields Se^{2-} and SO_3^{2-} ions. Sulphite ions reduce $Cd(NH_3)_4^{2+}$ and generated Cd^{2+} ions. Sodium selenosulphate (Na_2SeSO_3) hydrolyzes in alkaline medium to give Se^{2-} ions as:

$$Na_2SSeO_3 + OH^- \Leftrightarrow Na_2SO_4 + HSe^-$$
$$HSe^- + OH^- \Leftrightarrow H_2O + Se^{2-}$$

It is noted that ammonia hydrolyzes in water to give OH^- according to equation

$$NH_3 + H_2O \Leftrightarrow NH_4^+ + OH^-$$

With the presence of Cd^{2+} ions in the bath, CdSe will form if the ionic product of Cd^{2+} and Se^{2-} exceeds the solubility product of CdSe. The formation of CdSe films is based on a heterogeneous nucleation. The rate of release of Cd^{2+} ions from the ammonia complex affects the rate of film deposition. Furthermore, the rate of release of Cd^{2+} ions is affected by pH, temperature and concentration of metal and chalcogen ions. The chemical bath deposition can thus be described by the formation of chalcogen ions, through the process of hydrolysis in alkaline medium, and then the combination of metal ions with chalcogen ions.

At room temperature, no film or precipitate is formed even when the solution is kept for a very long time. This is because at low temperatures, most Cd^{2+} ions combine with ions of NH_3 to form $Cd(NH_3)_4^{2+}$ and the ionic product of Cd^{2+} and Se^{2-} is less than the solubility product of CdSe. To get higher concentrations of Cd^{2+} and to initiate the deposition, the solution has to be heated (to a value in the range form 60 to 85 °C). The heating results in dissociation of the $Cd(NH_3)_4^{2+}$ complex and selenosulfate and an increase in concentrations of Cd^{2+} and Se^{2-}. In addition, the increase in temperature results in an increase in the kinetic energy of the ions causing more frequent collisions and increased probability of CdSe formation. Finally, the rate of dissociation of Na_2SSeO_3 may increase with the temperature. Hence, the deposition rate of CdSe increases with the increase in temperatures. It should be mentioned that CdSe films deposited at 60 – 85°C were uniform and adhered well to the substrates.

The control of CBD is very important in order to obtain a highly transparent and adherent layer. The thickness of the CdSe layer formed by CBD tends to saturate between 80 and 200 nm due to the limited source growth process in which heterogeneous reaction competes with the homogeneous one, which further depletes the reactants to form CdSe colloids in the solution. A predominantly homogeneous reaction often terminates the heterogeneous, and the film them grows by adsorption of colloids, leading to a porous and non-adhesive layer. The same situation also occurs in the deposition of CdS films by CBD and is described in the following.

Cadmium sulphide, CdS, is known to be an excellent heterojunction partner of p-type cadmium telluride, CdTe, or p-type copper indium diselenide, $CuInSe_2$. Very thin CdS films (<0.2 um) are commonly used as window layers in high efficiency thin film solar cells based on CdTe or $CuInSe_2$, owing to their transparency and photoconductivity among other properties. Chemical bath deposition has proven to be the most suitable method to produce CdS films for photovoltaic cells. In one part of the present thesis work, research experiments have been carried out on chemical bath deposition of CdS as active layer for thin film transistors. For the chemical bath deposition of CdS, a variety of combinations of source materials have been used [5-2,3,5,6]. Some examples are: (1) acetate, chloride, nitrate, or sulfate as the cadmium source, (2) ammonium hydroxide, potassium cyanide, or triethanolamine as the complexing agent, (3) thiourea or thioacetamide as the sulfidizing agent. A reaction mechanism for the formation of CdS based on the deposition kinetics of thin films of PbSe by Lundin [5-6] will be described below:

1. Cadmium salt reacts with ammonia to form the complex compound.

$$NH_4^+ + OH^- \leftrightarrow NH_3 + H_2O$$

$$Cd^{2+} + 4NH_3 \leftrightarrow Cd(NH_3)_4^{2+}$$

2. Diffusion of the complex ion, OH^-, and thiourea (NH_2CSNH_2) to the surface of the substrate.
3. Dissociation of the thiourea on the surface of the substrate in the ammonia

$$(NH_2)_2CS + OH^- \leftrightarrow CH_2N_2 + H_2O + HS^-$$

4. Formation of bivalent sulfide ions

$$HS^- + OH^- \leftrightarrow S^{2-} + H_2O$$

5. Formation of CdS

$$Cd^{2+} + S^{2-} \leftrightarrow CdS$$

With sufficient amount of NH_3, the Cd exists in the form of $Cd(NH_3)_4^{2+}$. The presence of ammonium salt, however, promotes the forward reaction in reaction 1. This

then reduces the pH value and OH^- concentration, in the reaction bath according to the relation [5-7]

$$pH = pK_a + \log(\frac{[NH_3]_o}{[NH_4^+]_o})$$

Here $[NH_3]_o$ and $[NH_4^+]_o$ are the initial ammonia solution and ammonium salt concentrations, respectively, and pK_a was reported to be 9.2 at 25°C.

When the concentration product of Cd^{2+} and S^{2-} in the solution exceeds the solubility product of CdS, CdS precipitates. The rate of formation of CdS is determined by the concentration of Cd^{2+} provided by the $Cd(NH_3)_4^{2+}$ and the concentration of S^{2-} from the hydrolysis of $(NH_2)_2CS$. The rate of hydrolysis of $(NH_2)_2CS$ depends on the pH and temperature of the solution. When the solution temperature is decreased, the concentration of $Cd(NH_3)_4^{2+}$ in solution is increased resulting in the reduction of the concentration of Cd^{2+}. The concentration of S^{2-} is also reduced. As a result, the rate of formation of CdS is reduced. The use of an excess amount of ammonia will increase the pH of the solution, promoting the formation of S^{2-}. However, the concentration of $Cd(NH_3)_4^{2+}$ will also increase, causing a reduction in the concentration of Cd^{2+} and the rate of CdS formation. Thus, the rate of formation of CdS can be adjusted by varying the concentration of either ammonia or NH_4-salt in the solution. Furthermore, the hydrolysis of $(NH_2)_2CS$ is enhanced as the temperature increases. Therefore, the temperature of the solution can also be used to control the rate of CdS formation.

The formation of CdS may take place heterogeneously on the substrate surface and homogeneously in the solution, which is the same as that in CdSe. The heterogeneous reaction competes with the homogenous one, which further depletes the reactants to form CdS colloids in the solution. The homogeneous process should be minimized since the CdS particulates formed in solution can be adsorbed on the growing surface yielding films of uncontrolled properties. The heterogeneous process is promoted at lower reaction rates and the CdS films deposited with minimal homogeneous reaction are highly transparent. CdS film prepared by the chemical bath deposition technique are uniform,

resistant to abrasion and has some advantages over those prepared by other techniques. For example, their properties are relatively insensitive to oxygen and moisture [5-5].

Although CBD is ideally suited for the application of large area devices, such as the window materials in thin film solar cells, it cannot be readily used for other applications requiring high quality films with a larger thickness. This is because, (i) the thickness of films formed by CBD tends to saturate at 0.2 μm [5-7], and (ii) with longer reaction time the resulted films often have a duplex structure [5-8]. This structure consists of an inner layer, which is very adherent, and an outer layer, which is less adherent despite its visual appearance. These limitations exist because CBD is a limited source growth process in which the heterogeneous reaction competes with the homogeneous one, which further depletes the reactants to form colloids in the bulk of the solution. In order to avoid the above problems and to obtain good quality films with an appropriate thickness for TFTs, a multiple deposition method was developed in this work.

5.3 Experiments

The fabrication starts from a Si or glass substrate. A layer of dielectric material is deposited on the top surface. This dielectric layer may be Ta_2O_5 and Al_2O_3 by anodization or SiO_2 prepared by thermal oxidation. After the formation, windows were cut through the dielectric layer by a photolithography and etching method for electrical contacts. A layer of CdSe or CdS film was then deposited over the entire sample surface by the chemical bath deposition method.

5.3.1 CBD for CdS films

The experimental set-up for CBD process is shown in Figure 5-1. The chemical bath deposition for CdS is performed from an aqueous solution in a Pyrex beaker containing

the following ingredients: 2 mM $CdCl_2$, 20 mM of thiourea, 20 mM of NH_4Cl, and 200 mM of NH_4OH. The solution must be thoroughly mixed until it turns yellow in color. The pH value of the aqueous solution is then adjusted to a value preferably in the range 11~12 at room temperature by adding ammonia hydroxide. However, a pH value in the range 9-13 may still be used. The Pyrex beaker with the solution is partly immersed in a hot water bath.

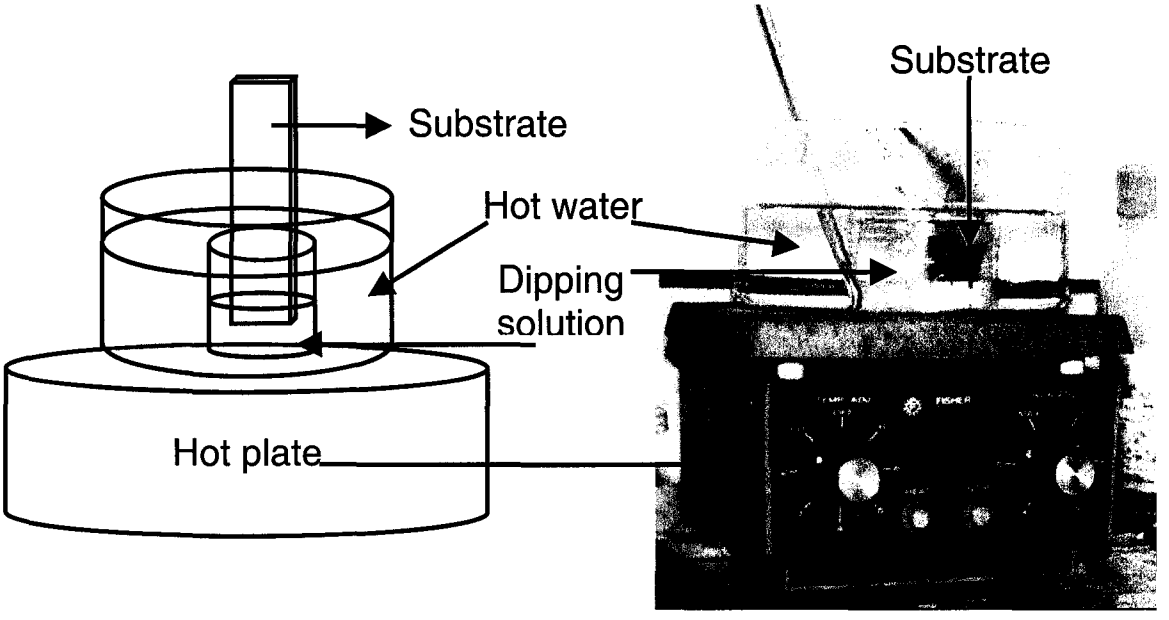


Figure 5-1 Experimental setup for CBD process.

The deposition may be carried out at solution temperatures in the range from 55°C to 95°C, but preferably at temperatures above 60°C and less than 95°C. After this, a clean glass substrate with the patterned gate electrode and dielectric layer is immersed in the aqueous solution. The glass substrate for the CdS deposition is suspended substantially vertically in the solution contained in the beaker. After this, the deposition of CdS film is allowed to proceed for a period of about 5 minutes for multiple deposition runs. The deposition time is from 10 to 20 minutes for experiments with a single deposition run.

For multiple deposition experiments, the substrate was removed from the bath and ultrasonically cleaned before continuing the subsequent deposition (each for 5 minutes).

It is also noted that the fresh solution used for each dipping should be continuously stirred to obtain uniform distribution of the chemical components. Four consecutive chemical baths were used in this deposition process. After 20 minutes of multiple depositions, the CdS film shows a yellow color with a good adherence on the substrate. The thickness of the CdS films deposited for thin film transistor and circuit applications may be controlled to a value in the range from 600 Å to 4,000 Å, by controlling the deposition time.

5.3.2 CBD for CdSe films

The chemical bath deposition of CdSe layer was carried out as follows: (a) prepare a 0.1 M solution of cadmium chloride. (b) Prepare a 0.1 M solution of sodium selenosulphate by dissolving elemental selenium into Na_2SeO_3 solution at 75 °C and with stirring for a few hours. The elemental selenium is preferably in a powder form, with an average powder size in the order of 325 meshes. This results in a nearly clear solution, which when filtered gives a clear solution of sodium selenosulphate. (c) Prepare a 4 M NH_4OH solution. (d) Prepare a deposition bath by mixing 10.0 ml of 0.1 M Na_2SSeO_3 reagent, 3.0 ml of 4 M NH_4OH, and 10.0 ml of 0.1 M $CdCl_2$, in the above order. Mix the deposition bath at room temperature thoroughly until it turns orange in color. The pH value should be adjusted to a value preferably in the range 12~13 at room temperature by adding ammonia hydroxide. However, a pH value in the range 10~13 may still be used.

After the above described deposition bath preparation, the deposition of CdSe should be started. This deposition is similar to that for the deposition of CdS, as shown schematically in Figure 5-1, except that the CdS solution is replaced by the solution for CdSe, which is prepared using the process described in the previous paragraph. A clean glass or Si substrate containing patterned electrodes and gate dielectric is suspended

vertically in the solution contained in a beaker. The beaker is immersed in water bath maintained at a constant temperature (80±2) °C to allow the CdSe deposition to start. Although the temperature of the water bath is indicated at 80°C in the above example, the deposition may be carried out in a solution at temperatures in the range from 55°C to 95°C, but preferably at temperatures above 60°C and less than 95°C.

The deposition of CdSe film is allowed to continue for a period of about 5 minutes. After each deposition and before the subsequent deposition, the substrate is removed from the bath and ultrasonically cleaned. It is noted that the fresh solution for each dipping should be continuously stirred to obtain uniform distribution of the chemical components. After 40 minutes of multiple depositions, the CdSe film shows a red/orange color with a good adhesion on the substrate. The thickness of the CdSe films deposited for the thin film transistor and circuit applications may be controlled to a value in the range from 500 Å to 4,000 Å by controlling the deposition time. Film thicknesses have been measured by utilizing a Dektak surface profile measurement unit and by examining cross-section in an SEM.

5.4 Results and Discussion

Figure 5-2 show typical curves for CdS film thickness as a function of dipping time, for different $CdCl_2$ concentrations. The other deposition parameters have been kept constant: 20 mM of thiourea, 20 mM of NH_4Cl, and pH ~ 12 for CdS deposition; 0.1 M Na_2SSeO_3 reagent and pH ~ 12 for CdSe deposition. The deposition temperature was kept at about 80 °C at all time. Figure 5-2 (a) shows the variation of CdS thickness with the $CdCl_2$ concentration ranging between 0.5 and 4.5 mM for two different deposition times, 10 and 20 minutes. It is seen that CdS thickness increases from 80 to 220 nm. It is thus clear that the deposition rate can be increased by increasing the concentration of $CdCl_2$.

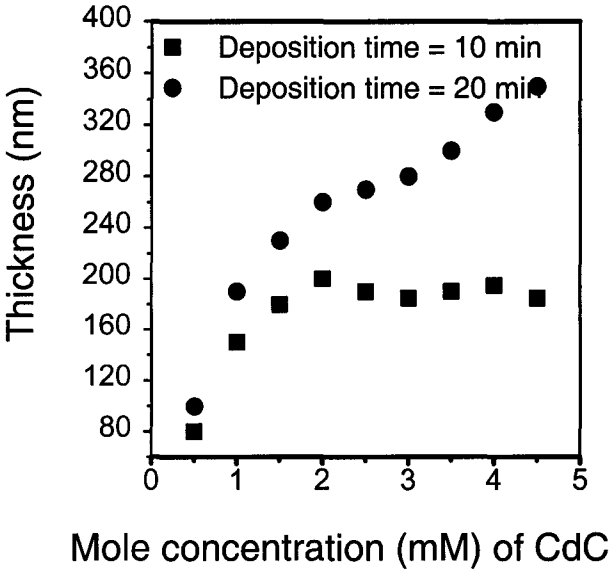


Figure 5-2 (a) Effect of the $CdCl_2$ concentration on the CdS thin film thickness for two different deposition times.

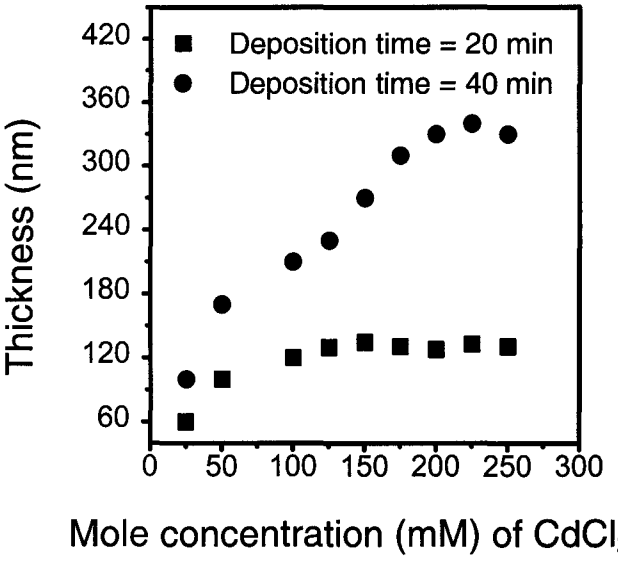


Figure 5-2 (b) Effect of the $CdCl_2$ concentration on the CdSe thin film thickness for two different deposition times.

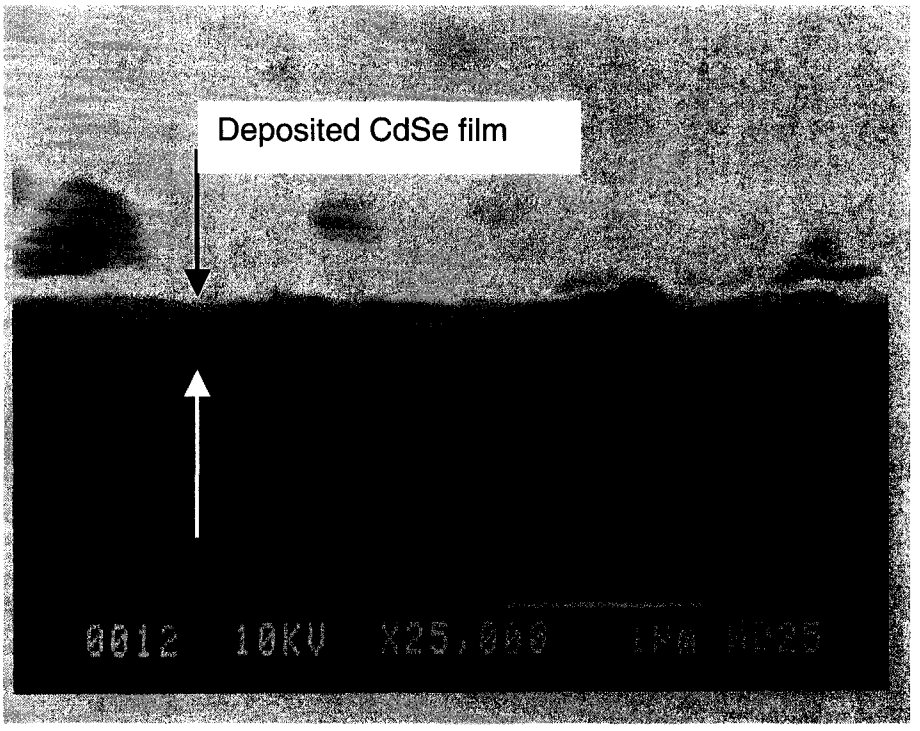


Figure 5-3 (a) A SEM photograph showing the cross-section of a deposited CdSe films by the CBD method.

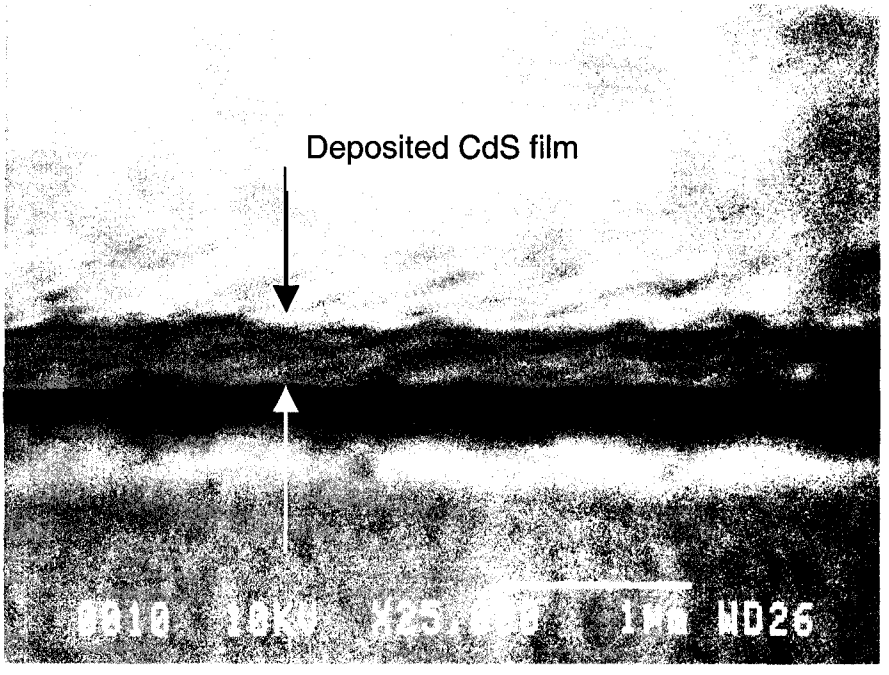


Figure 5-3 (b) A SEM photograph showing the cross-section of a deposited CdS films by the CBD method.

The experimental thickness variation with the increase in $CdCl_2$ concentration presented in Figure 5-2 (a) for a deposition time of 20 minutes shows a thickness increase from 100 to 350 nm, which is more than double in the thickness. This result thus indicates the initial growth rate cannot be maintained, and the thickness tends to its saturation value. A SEM photograph showing the cross-section of a film is given in Figure 5-3. Here, the thickness observed is consistent with that measured by a surface profiler. In the initial stages of growth, the growth rate is high. Subsequently, the rate decreases resulting in a terminal thickness.

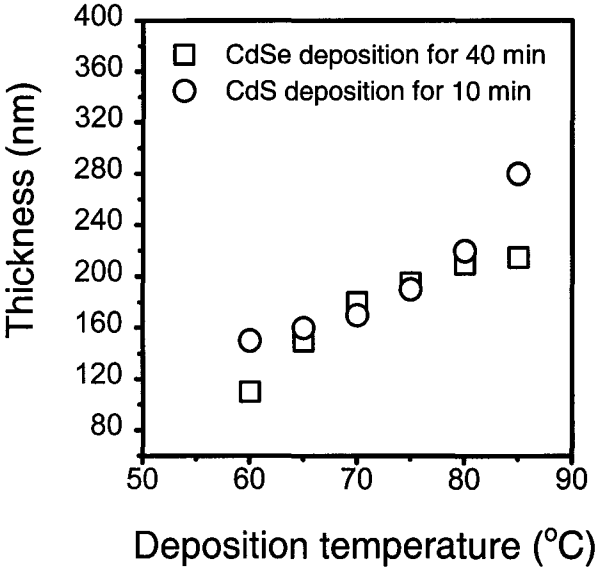
As described before, after having been ultrasonically cleaned in DI water (to remove any precipitate) the films are immersed again in a fresh solution to continue the deposition. Figure 5-2 (b) shows the thickness variation of CdSe films with the $CdCl_2$ concentration in a range between 25 and 250 mM, for two different deposition times of 20 and 40 minutes. The thickness of CdSe increases from 60 to 330 nm with the increase in the $CdCl_2$ concentration (for a fixed deposition time of 20 minutes). It is worthwhile to point out that, the terminal thickness of CdS is always greater than that of CdSe films under the same conditions. This observation is in good agreement with that reported by others, who have suggested this to be due to the solubility product of CdS, which is smaller than that of CdSe [5-1,2].

Crystalline CdSe can have two different crystalline structures, namely, wurtzite (cubic) and zinc blende (hexagonal). It has been reported that chemically deposited CdSe films, depending on preparative conditions, exhibited cubic, hexagonal or mixed (cubic + hexagonal) crystal structures [5-1,2]. However, many chemically deposited films are amorphous or consist of fine grains, making it difficult to draw any conclusion regarding the crystal structure of these films.

The rate of deposition, obtained from the initial part of the curves in Fig. 5-2 and Fig. 5-4, and the terminal thickness depend on the pH of the bath, concentration of the reactants, and temperature. The variation of thickness from samples with dipping solutions at different temperatures is shown in Figure 5-4. Since the concentration of Cd^{2+}

and the dissociation rate of the complexes are function of temperatures, the deposition rate increases as the temperature is increased. Furthermore, as stated before, the increased kinetic energy of the ions with increasing temperature will result in more frequent ions collisions so that the rate of film formation increases.

From the experiments carried out in the present work, it is evident that the deposition of CdSe and CdS at temperatures below 60 °C was much slower compared to that at high temperatures. For CdSe films, it was also observed that the deposition rate shows a maximum at about 80 °C. Above 80°C, the reaction is quite fast due to a high rate of release of Cd^{2+} and Se^{2-} ions so that most of the ions are consumed before significant amount of deposition on the substrates. This is because at the high temperatures the ions are released at a faster rate and they may not have enough time to condense in the substrate surface, leading to the precipitation of CdSe molecules in the solution [5-8,9]. However, for CdS deposition, the maximum occurs at a temperature higher than 85 °C.



Fixed deposition parameters:
CdSe: pH ~ 12, 0.1 M Na_2SSeO_3, 0.1 M $CdCl_2$, 6.5 M NH_4OH
CdS: pH ~ 12, 0.1 mM $CdCl_2$, 1 mM thiourea, 1 mM NH_4Cl, 10 mM NH_4OH

Figure 5-4 Effect of the deposition temperature on the CdS and CdSe film thickness.

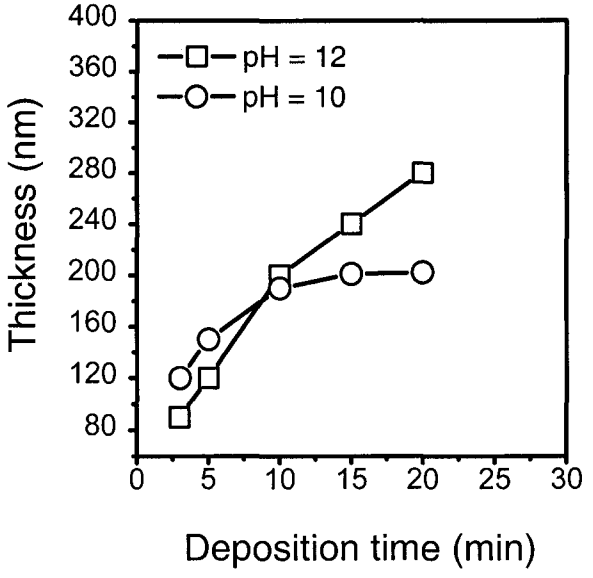


Figure 5-5 (a) Effect of the pH in the dipping solution on the CdS film thickness.

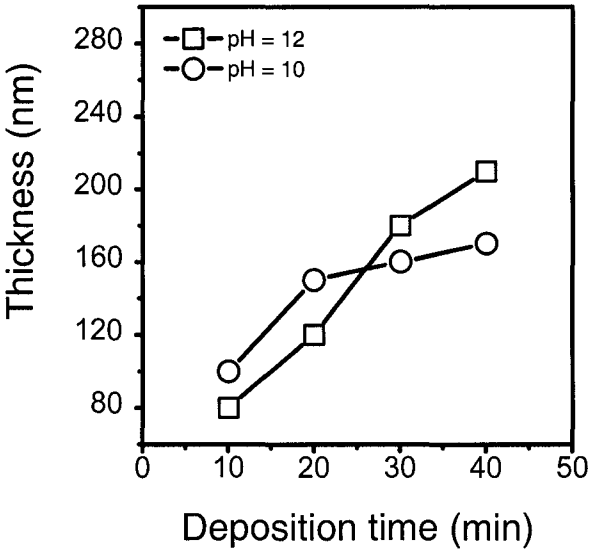


Figure 5-5 (b) Effect of the pH in the dipping solution on the CdSe film thickness.

Fixed deposition parameters:
CdSe: T = 80 °C, 0.1 M Na_2SSeO_3, 0.1 M $CdCl_2$, 6.5 M NH_4OH
CdS: T = 80 °C, 0.1 mM $CdCl_2$, 1 mM thiourea, 1 mM NH_4Cl, 10 mM NH_4OH

From Figure 5-5, it is also clear that the rate of deposition decreases with the increase in pH value, whereas the terminal thickness increases with the increase in the pH value. At 80 °C, uniform, adherent, and specularly reflecting films were obtained for pH values between 11 and 12. Using solutions with pH < 9.0, nonuniform and nonadherent films were resulted.

The CBD deposited CdS or CdSe films are highly resistive. Room temperature resistivity values for typical CdSe and CdS films are in the range of 10^6 – 10^8 Ω-cm by two-point probe method. The high value of the electrical resistivity may be due to the small grain size, grain boundary discontinuity effect, lack of stoichiometry and an increased amount of disorder during growth process [5-10,11]. In general, the growth of good quality semiconductor thin films by the CBD proceeds at a slow pace. The technique is ideally suited for producing uniform films with thickness in the range 80 – 400 nm.

During the experiments designed to establish the optimum conditions, many as-deposited thin films peeled from the substrates before reaching the terminal thickness. After numerous experimental runs, the optimum deposition conditions were finally obtained and the results are presented in the Tables 5-1 and 5-2. Even though thin films can be prepared using conditions other than the ones given in Tables 5-1 and 5-2, most of them cannot be patterned by etching in diluted HCl solutions, which are normally used to etch CdSe and CdS films. At low values of pH (<9), where no hydroxide formed in the solution or on the substrate, films with poor surface coverage and adherence were found. One of the central issues in CBD is whether the conditions allow deposition to proceed in an ion-by-ion manner on the substrate (i.e., growth by successive anion and cation adsorption on the growing films) or by a cluster or colloidal mechanism whereby colloids of the metal chalcogenide (or hydroxide) adsorb on the substrate and coagulate to form the film.

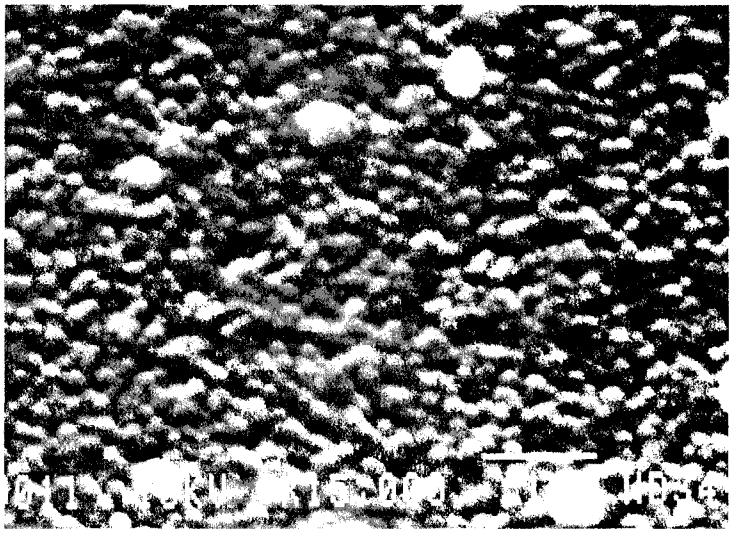


Figure 5-6 (a) A SEM micrograph of a deposited CdSe film by the CBD method.

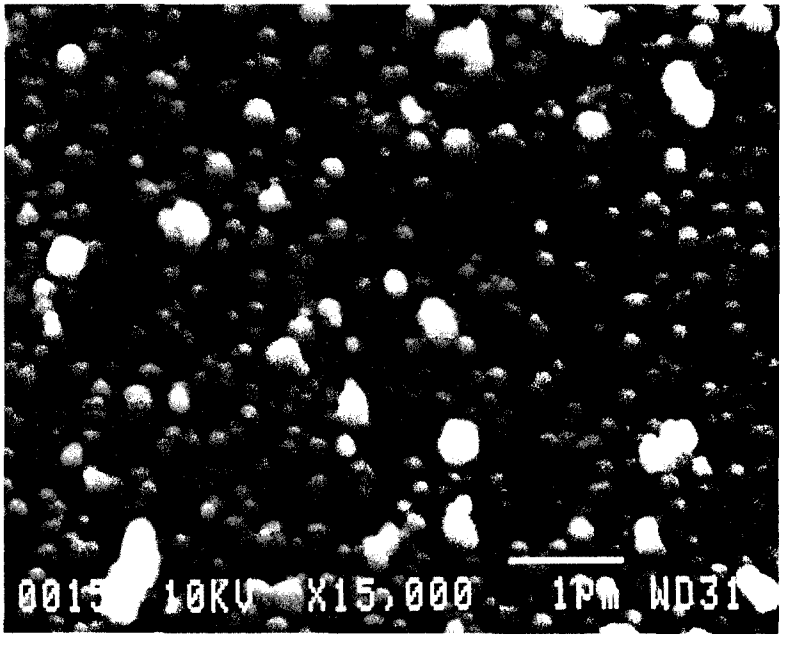


Figure 5-6 (b) A SEM micrograph of a deposited CdS film by the CBD method.

In general, the ion-by-ion process resulted in adherent and reflecting films while the others gave poorly adherent, diffusive reflecting films [5-12,13]. The post-deposition ultrasonic cleaning in DI water is important and serves to remove some clusters or colloids on the substrate, which will attract more colloids for the subsequent deposition process. The multiple dipping processes developed in this work have been shown to yield thin films with quality much better than that from continuous deposition runs (20 ~ 40 minutes). In the continuous deposition, the required film thickness can be obtained by extending the deposition. However, the film quality deteriorates after about 7 minutes due to adsorption of particulate precipitate at the film surface. Figures 5-6 show SEM photographs taken from the CdS and CdSe films, revealing the approximate grain size and microstructure (15000× magnifications).

The individual crystallites and their boundaries are clearly visible from these photographs. The average grain size ranges from 50 to 200 nm. Close inspection also reveals voids in between these grains. The dipping conditions used for the CdSe film shown in Figure 5-6 (a) are as follows: pH ~ 12, temperature = 80 °C, 0.1 M Na_2SSeO_3, 0.1 M $CdCl_2$, 6.5 M NH_4OH, while that for the CdS film shown in Figure 5-6 (b) are: pH ~ 12, temperature = 80 °C, 0.1 mM $CdCl_2$, 1 mM thiourea, 1 mM NH_4Cl, 10 mM NH_4OH. The further studies for the microstructure of the deposited films are needed to fine-tune the CBD dipping conditions for the good performance of the fabricated TFT.

5.5 Conclusions

In this Chapter, the chemical bath deposition techniques developed in our laboratories and the results for CdS and CdSe thin films have been presented. Using the multiple deposition process with appropriate ultrasonic cleaning in DI water, good quality films of CdS and CdSe have been successfully produced. From the results of examination under SEM and electrical measurements, it is believed that the quality of these films is suitable for the fabrication of TFTs. The process was found to be reproducible and reliable for the deposition of CdS and CdSe thin films with thicknesses in the range 80 – 400 nm. It should be pointed out that during the above described experiments; all chemicals used are reagent grade. Hence, the production cost may be further reduced with this method.

The deposition experiments carried out in this work are mainly focused on the effects of temperature, pH, and ion concentration control. From these studies optimum deposition conditions have been established. It was also observed that the rate of deposition and the terminal thickness both depend on pH, composition, and temperature of the bath.

Other effects related to the solution uniformity during deposition, the substrate position in the container, the effect of ultrasonic cleaning process after each dipping, the process of preparation for dipping solution, the purity of chemicals, the timing control for the starting deposition and the duration for each dipping all will affect the quality of film deposition. In addition, the recycling of chemicals and new system design for dipping of large substrates are important issues for the possible industrial application of this novel process. Furthermore, the problem of solution circulating may also need certain study. This deposition process can easily control the thickness and is reproducible. The performance of TFTs fabricated on the CBD deposited semiconductor thin films may be used to determine the suitability of this deposition technology. The recipes for CBD summarized in Tables 5-1 and 5-2 are used to produce thin film for the fabrication of TFTs and the results obtained will be presented in Chapter 6.

Tables

Table 5-1 the dipping condition for CdSe-TFT	
Relative ion concentration:	25 ~ 250 mM $CdCl_2$
Fixed Relative ion concentration	0.1 M Na_2SSeO_3, 6.5 M NH_4OH
pH value:	9 ~ 13
Temperature:	60 ~ 85 °C
Mixing time before dipping:	2 minutes
Stirring during CBD:	Yes
Dipping time:	5 minutes
Dipping times:	4 ~ 8
Cleaning the beaker after dipping:	yes
Ultrasonic cleaning after dipping:	1 minute
Ultrasonic cleaning solution:	DI water

Table 5-2 the dipping condition for CdS-TFT	
Relative ion concentration:	0.5 ~ 4.5 mM $CdCl_2$,
Fixed ion concentration:	1 mM of thiourea, 1 mM NH_4Cl, 10 mM NH_4OH
pH value:	9 ~ 13
Temperature:	60 ~ 85 °C
Mixing time before dipping:	3 minutes
Stirring during CBD:	Yes
Dipping time:	3 minutes
Dipping times:	2 ~ 7
Cleaning the beaker after dipping:	yes
Ultrasonic cleaning after dipping:	1 minute
Ultrasonic cleaning solution:	DI water

References

1. D. Lincot, M. Froment, and H. Cachet, "chemical deposition of chalcogenide thin films from solution," Advances in Electrochemical Science and Engineering, Wiley VCH vol. 6, pp. 165-235, 1999.

2. J. H. Schon, O. Schenker, B. Batlogg, "Solution processed CdS thin film transistors," Thin solid films vol. 385, pp. 271-274, 2001.

3. C. D. Lokhande, Mater. Chem. Phys., vol. 27, pp.1-43, 1991.

4. T. M. Racheva, I. D. Dragieva, D. H. Djoglev, P. P. Dimitrova, "Thin CdSe films obtained by the method of chemical deposition with selenourea," Thin solid films, vol.17, pp. 85-91, 1973.

5. N. R. Pavaskar, C. A. Menezes, and A. P. B. Sinha, "Photoconductive CdS films by a chemical bath deposition process," J. Electrochem. Soc., vol. 124, pp.743-748, 1977.

6. A. B. Lundin, Izv. Akad. Nauk SSSR Neory. Mater., no. 1, pp. 2107, 1965.

7. R. L. Call, N. K. Jaber, K. Seshan and J. R. Whyte, Solar Energy Materials 2, pp. 373, 1980.

8. I. Kaur, D. K. Pandya and K. L. Chopra, J. Electrochem. Soc. Vol. 127, pp. 943, 1980.

9. A. Mondal, T. K. Chaudhuri and P. Pramanik, Solar Energy Materials vol. 7, pp. 431, 1983.

10. W. J. Danher, L. E. Lyons and G. C. Morris, Solar Energy Materials vol. 12, pp. 137, 1985.

11. T. L. Chu, S. S. Chu, C. Q. Wu, J. Britt, and C. Wang, in Proceedings of the 22nd IEEE Photovoltaic Specialists Conferences, pp. 952, 1991.

12. D. Lincot and R. Ortega-Borges, ibid., vol. 139, pp. 1880, 1992.

13. R. Ortega-Borges and D. Lincot, This journal., vol. 40, pp.3464, 1993.

Chapter 6

Performance of CdS-TFTs and CdSe-TFTs on Si substrates

6.1 Introduction

An inverted staggered–electrode structure has been employed to fabricate thin film transistors in this work. The fabrication was done mainly to establish the processes of TFT fabrication involving CBD and to a lesser extent to determine the quality of the CBD deposited CdS and CdSe thin films. This structure is also the most commonly used one in the production of thin film transistor addressed liquid crystal displays (TFT/LCDs). In the display industry, most of the TFTs in LCDs are formed on amorphous Si (a-Si). More recently, some displays with TFTs fabricated using polycrystalline Si (poly-Si) have been reported [6-1]. TFTs for certain electronic displays with special high performance requirements have also been fabricated using CdSe or CdS as an active layer [6-2]. As described before, the Hall mobility, μ_H, and the field-effect mobility, μ_{FE} of CdSe and CdS, are greater than that of a-Si. Hence, they are potentially good candidates as active layers of thin film transistors. Thin film transistors based on

CdSe have been fabricated for high brightness LCD panels. In such a prior art CdSe-TFTs, thin films of CdSe were deposited by a vacuum thermal evaporation method [6-3].

Although CdSe is one of the first materials proposed for TFTs [6-4], it has not been successfully introduced in large scale into the market. This is because the reproducibility and uniformity of surface electronic properties for large area CdSe films prepared by vacuum deposition are difficult to control compared to that of amorphous silicon films [6-5]. For mass production, it is desirable to deposit the semiconductor thin films at low temperatures so that low cost substrates such as glass can be used. As stated before, the objective of this thesis is to develop a novel method to fabricate thin film transistors with the active layer (CdS or CdSe) deposited using the CBD method at low temperatures. To obtain a TFT having a large On/Off-current ratio with the CBD method, quality of the deposited films must be controlled or optimized. To obtain such films, effects of deposition conditions such as solution pH value, deposition temperature, and relative concentrations of various reactants in the solution must be studied. Furthermore, effects of gate insulator and interface between the insulator and active semiconductor film must be investigated. In this Chapter, experiments carried out to study the effects of varying the above conditions will be described. The results obtained will be discussed.

It is worthwhile to point out that, in order to be used in high quality electronic display and imaging applications, the TFTs must satisfy certain basic requirements. Firstly the leakage current between drain and source in the Off-state must be small enough (<10 pA). Secondly, the On-state current at a given applied voltage (10 volts) must be large enough (>1 μA). Finally, the threshold voltage (V_T) must be small and the mobility of charge carriers in the channel must be large. Typical values obtained on the TFTs fabricated in this work are; μ_{FE} = 10 ~ 15 $cm^2V^{-1}sec^{-1}$, V_T = 2.5 V for CdSe-TFTs and μ_{FE} = 0.8 ~ 1 $cm^2V^{-1}sec^{-1}$, V_T = 2.8 V for CdS-TFTs. It is thus evident that the CdSe and CdS thin films prepared by the novel CBD method may be suitable for circuits on large area and low temperature substrates specifically for display and imaging applications. All the dominant factors and resulting device characteristics for the CdSe-TFT and CdS-TFT fabricated in this work are listed in the Tables 6-1 to 6-4.

6.2 CdSe-TFTs and CdS-TFTs with thermally grown SiO_2

6.2.1 Film Deposition

As shown in Chapter 4, two procedures have been developed and used in this work to fabricate TFTs; one is based on monocrystalline Si substrates and the other on glass substrates. In this section, experiments and the results obtained on monocrystalline Si substrates will be reported. A block diagram showing the process flow has been presented in Chapter 4. Results on glass substrates will be described in Chapter 7. A cross section view of the TFT fabricated is shown in Figure 6-1. The TFTs to be reported here were fabricated on n-type Si (100) wafers. Dimensions of the channel defined by the photomask used are 20 μm in length and 200 μm in width.

The fabrication starts with an oxidized n-type Si substrate with a thickness of SiO_2 of about 0.8 um. A first photolithography process is carried out with mask No. 1 to etch away SiO_2 from a rectangular region to define the gate. After the etching of the SiO_2, an n^+ diffusion process is performed to convert the exposed n-type Si into heavily doped n-type. Next, a thin layer of SiO_2 is thermally grown to form the gate insulator (60 ~ 80 nm). After this, a layer of semiconductor thin film (CdS or CdSe) is deposited over the entire sample surface by a chemical bath deposition method (CBD). The deposited semiconductor thin film is then selectively etched by a photolithography and etching method (mask No. 3) to define active channel region. A layer of aluminum is finally evaporated and subsequently patterned (mask No. 4) to form gate and drain-source electrodes of the TFTs. The detailed preparation conditions of CdS or CdSe thin films by the CBD method were described in Chapter 5. It is noted that all chemicals used in the present experiments were reagent grade.

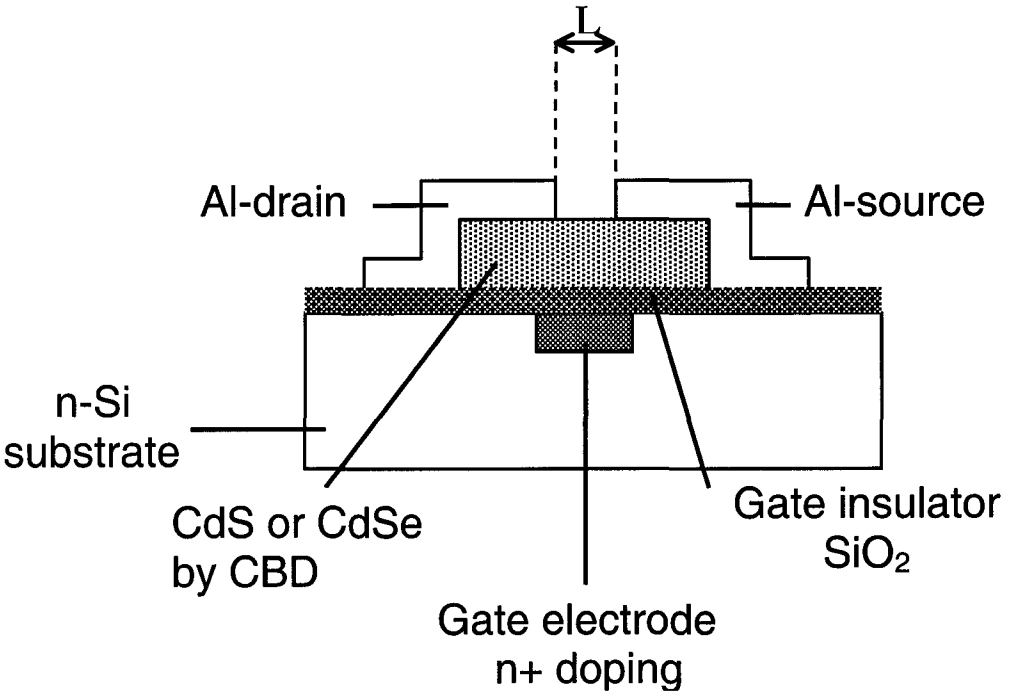


Figure 6-1 A schematic cross-sectional view of the TFTs.

For the deposition of CdSe films, a 0.1 M solution of cadmium chloride was prepared with deionized water. A 0.1 M solution of sodium selenosulphate was made by dissolving elemental selenium into a Na_2SeO_3 solution at 75 °C and with stirring for a few hours. This solution was filtered to result in a clear solution of sodium selenosulphate. The deposition bath was prepared by mixing 10.0 ml of the 0.1 M Na_2SSeO_3 reagent, 10.0 ml of the 0.1 M $CdCl_2$ and 3.0 ml of a 6.5 M NH_4OH, all at room temperature. After the mixing, deposition bath turned orange in color. Clean Si substrates with a thin SiO_2 layer were selected for CdSe deposition. The Si substrates were suspended vertically in the solution contained in a beaker. The beaker was immersed in a water bath at a constant temperature (80 ± 2) °C to initiate the deposition of the CdSe film. The deposition is allowed to continue for a period of about 5 minutes. After the first deposition, the substrates were removed from the bath and ultrasonically cleaned in deionized water for a

few minutes (details see Chapter 5) before proceeding to subsequent deposition runs. During each deposition run in the multiple depositions, the solution was continuously stirred to obtain uniform distribution of the chemical components (the total deposition time is about 40 minutes). After the 40 minute multiple depositions, the CdSe films showed a red color with a good adhesion to the Si substrates.

The chemical bath deposition for CdS is performed from an aqueous solution in a Pyrex beaker containing the following ingredients: 2 mM $CdCl_2$, 20 mM of thiourea, 20 mM of NH_4Cl, and 200 mM of NH_4OH. The solution must be thoroughly mixed until turning yellow in color. The Pyrex beaker with the solution is partly immersed in a hot water bath. The deposition is carried out at solution temperatures of about 80°C. Clean Si substrates for the CdS deposition are suspended substantially vertically in the solution contained in the beaker. After this, the deposition of CdS film is allowed to proceed for a period of about 5 minutes for multiple deposition runs. For multiple deposition experiments, the substrates were removed from the bath and ultrasonically cleaned before continuing the subsequent deposition (each for 5 minutes). It is also noted that the fresh solution for each dipping should be continuously stirred to obtain homogenous distribution of the chemical components. Four consecutive chemical baths were used in this deposition process. After 20 minutes of multiple depositions, the CdS film shows a yellow color with a good adherence on the substrate. Details for the CdS film deposition have been described in Chapter 5. Figure 6-2 and 6-3 show the photographs before and after CBD process for CdSe-TFT and CdS-TFT, respectively.

6.2.2 Heat Treatment

Since the mobility of electrons in as-deposited CdSe and CdS thin films is low, a heat treatment is carried out to improve the crystalline quality and thus the electron mobility. It has been reported that electrical properties of as-deposited CdSe films can be improved by post deposition annealing at a temperature between 250 and 400 °C for several minutes in N_2 [6-9,10]. In the present work, a series of experiments have been

carried out to determine the effects of heat treatment conditions on the electronic quality of the CBD films.

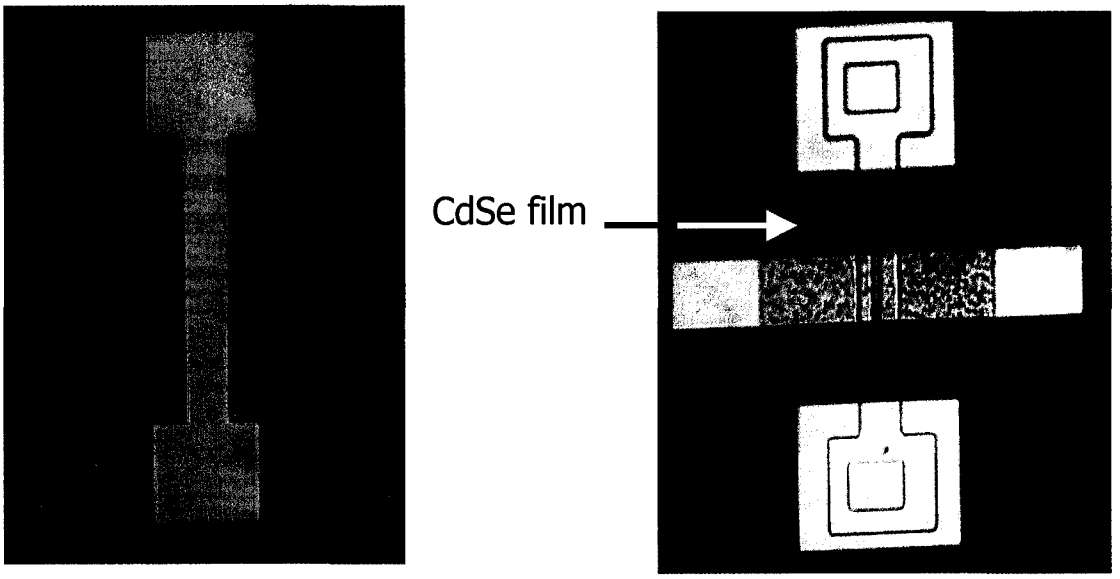


Figure 6-2 A Si substrate before and after CBD of CdSe film.

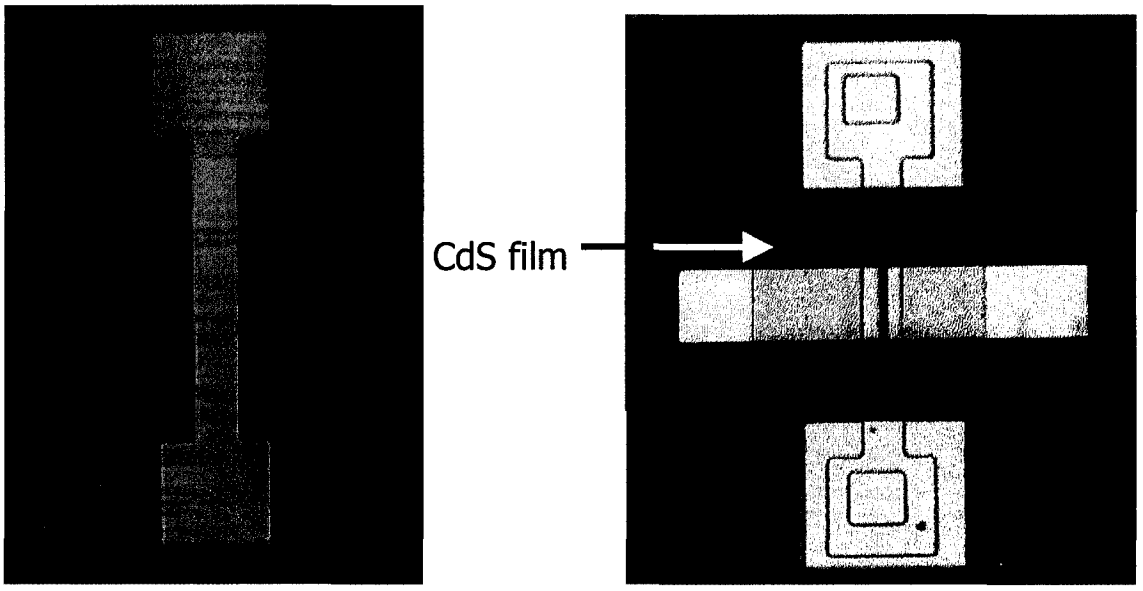


Figure 6-3 A Si substrate before and after CBD of CdS film.

It was observed that the best results were obtained by treating at 400°C in flowing N_2 for a period of time from 3 to 6 minutes. In the fabrication of TFTs, this post deposition heat treatment was performed after the formation of drain and source Al electrodes. This is because the heat treatment was also required to form ohmic contacts between the active layer and Al. After the above-described heat treatment, the fabrication of TFTs is completed and the devices are ready for testing.

6.2.3 Thickness and Electrical Measurements

As stated in Chapter 3, the electrical performance of TFTs is affected by the thickness of the active layer. After the fabrication, thickness of the CdS and CdSe films is measured by a Dektak 3030 profilometer and SEM cross section examination. Typical thickness of the CdSe and CdS thin films measured for the present TFTs is in a range from 1000 Å to 7000 Å.

Electrical characteristics of the fabricated CdSe-TFTs and CdS-TFTs were measured with an HP- 4145A semiconductor parameter analyzer. The drain voltage was swept from 0 to 30 V at various gate voltages with medium integration time. The results obtained will be described in subsequent sections.

6.2.4 Effects of concentration of Cd^+ in the CBD solution

For the TFTs to be described in this section, the common deposition conditions for both CdS and CdSe are as follows: deposition bath temperature = 80 °C, concentration of thiourea and NH_4Cl = 0.05 M for CdS deposition, 0.1 M Na_2SeSO_3 for CdSe deposition. The post deposition (fabrication) heat treatment experiments are carried out in flowing N_2 at about 400 °C for 5 minutes. The structure of all TFTs devices tested has been shown in Figure 6-1, with a channel length of 20 μm and a channel width of 200 μm.

By keeping all conditions and parameters to be constant except the concentration of Cd^+ ions, the effect of Cd^+ concentration on the performance of TFTs can be studied. The drain current (ON-current) at given gate and drain voltages is selected as the indication of performance of a given TFT. Figure 6-4 shows the variation of ON-current at a 10 V gate voltage and 10 V source-drain voltages with the variation of concentration of Cd^{2+} ion in the CBD solution. It is seen from this figure that the drain current increases gradually as the mole concentration of $CdCl_2$ is increased from 0.02 M to 0.06 M. This is followed by a drastic increase as the $CdCl_2$ concentration is increased further. A peak value is reached at 0.10 M for CdSe. Beyond this value, the drain current starts to decrease. Hence, the drain current of CdSe-TFT can be controlled by adjusting the mole concentration of the $CdCl_2$ in the deposition bath. The optimum concentration is about 0.10 M for CdSe in the present experiments.

In Figure 6-4, results of drain current from CdS-TFTs prepared using deposition baths having different concentrations of $CdCl_2$ are also given. Similar to the case for CdSe, one can see that the drain current increases gradually as the mole concentration of $CdCl_2$ is increased from 0.001 M to 0.003 M. This is followed by a drastic increase as the $CdCl_2$ concentration is increased further. A peak value is reached at 0.005 M. The drain current starts to decrease as the mole concentration of $CdCl_2$ is larger than 0.005 M. Hence, the drain current of CdS-TFT can be controlled by adjusting the mole concentration of the $CdCl_2$ in the deposition bath. The optimum concentration is about 0.005 M in the present experiments.

6.2.5 Effects of pH value in the CBD solution

By keeping all conditions and parameters to be constant (including concentration of Cd^+ ions) except for the pH value, the effect of pH on the performance of TFTs can be studied. The drain current (ON-current) at given gate and drain voltages is again selected as the indication of performance of a given TFT.

Fig. 6-5 show the variation of ON-current of TFTs at a 10 V gate bias and 10 V source-drain voltages with the variation of pH value. As seen in Figure 6-5, the drain current for CdSe TFTs increases first gradually as the pH value is increased from 9 to 10. As the pH value is increased further, the drain current increases rapidly, reaches a peak at pH = 12. When the pH is increased beyond 12, the drain current decreases.

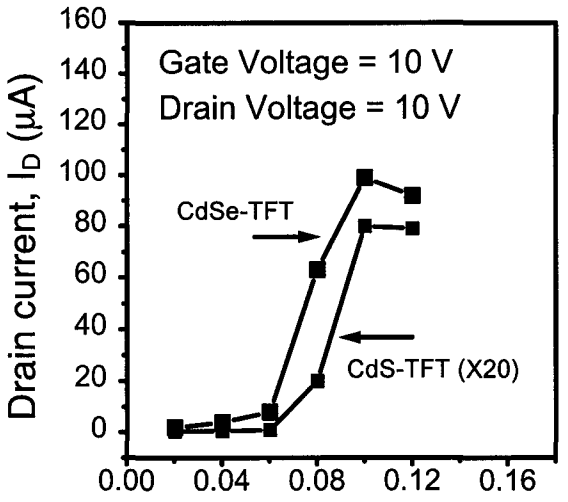


Figure 6-4 Drain current as a function of mole concentration of $CdCl_2$ for the CdSe-TFT (Sample #11100199~11100699) and CdS-TFT (Sample #07120199~07129699).

Results for CdS TFTs are also shown in Figure 6-5. Here, similar to CdSe TFTs the drain current increases first very gradually as the pH value is increased from 9 to 10.5. As the pH value is increased further, the drain current increases rapidly, reaches a peak at pH = 11.5. When the pH is increased beyond this value, the drain current decreases.

From the above results for both CdS and CdSe TFTs, it is evident that devices prepared from solutions with high pH values generally gives high On-currents. This is due to the rate of release of Cd^{+2} ions. This rate of release of Cd^{2+} ions from the ammonia complex, which is controlled by the pH value and concentration of metal ions, affects the

film deposition. As the pH value is increased, the rate of release of Cd^{+2} decreases, leading to a decrease of the deposition rate. However, it should be noted that in addition to the pH value the device performance is also affected by dipping time, deposition temperature, and annealing condition. Hence, the change of the above parameters will lead to a change of interface properties between the film and insulator. In order to obtain TFTs with the best performance, further optimization of all these parameters are required.

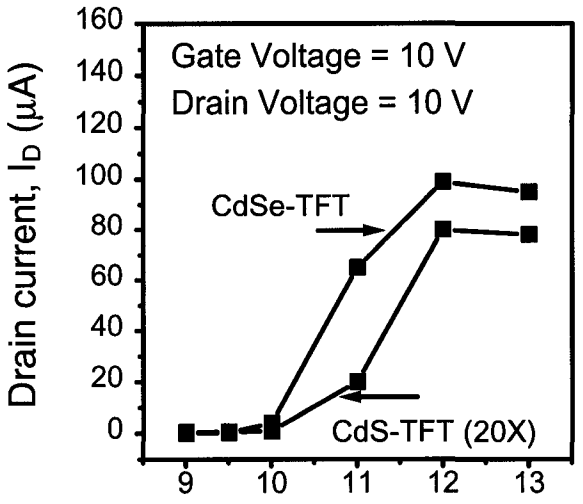


Figure 6-5 Variation of the drain current with the pH values in the dipping solution for the CdSe-TFTs (Sample #11100199, 11100799~11101199) and CdS-TFTs (Sample #07210199, 07210799~07211199).

6.2.6 Effects of film thickness

Another important parameter needs to be studied is the thickness of CBD thin films. This is because in TFTs, the active films need to be fully depleted of free electrons when switched into the off state with zero or negative gate bias. Hence, it is preferable to employ thinner active films in TFTs. However, the OFF-current in such TFTs may be low but the ON-current may not be high enough.

To study the effect of thickness of active films, a series of TFTs have been fabricated under the same conditions except for the thickness of the active films. The fabricated TFTs were characterized and the results obtained are summarized in Fig. 6-6 (a) for CdS TFTs and in Fig. 6-6 (b) for CdSe TFTs. It is noted that the ON-current was measured at a source-drain voltage 10 V and OFF-current at a gate bias of 10 V and 0 V. Figure 6-6 (a) shows the variation of ON and OFF-drain currents with the variation of thickness of CdSe films. As the thickness is increased from 0.1 um to 0.2 um, the On-current increases drastically by four orders of magnitude from 10^{-8} A to 10^{-4} A. Contrarily, the OFF-current increases gradually form $5x10^{-12}$ Amp, by less than one order of magnitude, to 10^{-11} A. Hence, within the thickness range from 0.1 to 0.2 um, the ratio of ON-current to OFF-current can be increased by increasing the active film thickness.

As the thickness is increased from 0.2 to 0.4 um, the increase in ON-current is very gradual whereas the OFF-current increases more rapidly from 10^{-11} A to 10^{-7} A. Therefore, within this thickness range the ratio of ON-current to OFF-current decreases by 5 orders of magnitude as the thickness is increased. Beyond 0.4 um thickness, the increase of both ON and OFF currents is gradual and the ratio of ON-current to OFF-current remained to be essentially constant, 10^3. From the above results, it is clear that the optimum active layer thickness is about 0.2 um for CdSe-TFTs. Incomplete depletion through the depth of the film, with films thicker than ~ 0.2 – 0.3 μm, results in a parasitic bulk electron channel. Hence, for some of the subsequent discussion, devices fabricated with 0.2 μm CBD layers will be used.

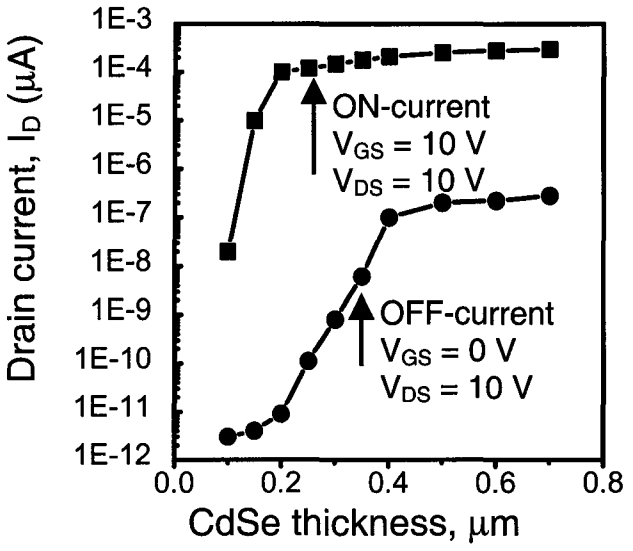


Figure 6-6(a) Dependence of TFT drain current on CdSe film thickness (Sample #04120100~04121000).

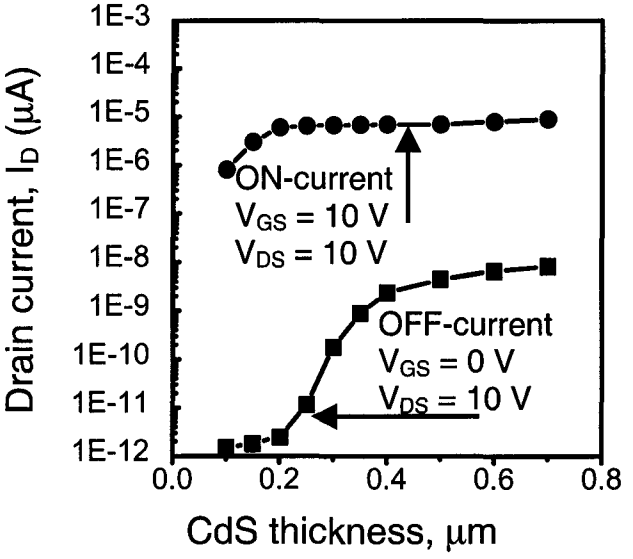


Figure 6-6(b) Dependence of TFT drain current on CdS film thickness (Sample #05070200~05071100).

Figure 6-6 (b) shows the variation of ON and OFF-drain currents with the variation of thickness of CdS films. As the thickness is increased from 0.1 um to 0.2 um, the On-current and OFF-current increases gradually from 10^{-6} A to 10^{-5} A and form $1x10^{-12}$ A to $3x10^{-12}$ A, respectively. Hence, within the thickness range from 0.1 to 0.2 um, the ratio of ON-current to OFF-current can be maintained at the same value ~ 10^{6}.

As the thickness is increased from 0.2 to 0.4 um, the ON-current is almost a constant whereas the OFF-current increases more rapidly from $3x10^{-12}$ Amp to 10^{-9}. Therefore, within this thickness range the ratio of ON-current to OFF-current decreases by 3 orders of magnitude as the thickness is increased. Beyond 0.4 um thickness, the increase of both ON and OFF currents is gradual and the ratio of ON-current to OFF-current remained to be essential constant, 10^{3}. From the above results, it is clear that the optimum active layer thickness is around 0.2 um for CdS-TFTs and is used for the following discussion.

6.2.7 Effects of solution temperature

To study the effect of solution temperature during the deposition on the quality of CBD thin films, a series of TFTs have been fabricated. The electrical properties of these devices were measured. From the results, field effect mobility of carriers was deduced and used as an indication of the film quality. Fig. 6-7(a) shows results for CdSe TFTs. One can see that the field effect mobility increases with the increase in solution temperature and reaches an estimated peak value of 15 cm^2/V-sec at 80°C. The field effect mobility decreases as the temperature is increased further. From the above results, it is clear that TFTs with the best performance should be prepared by depositing the active layers at a temperature in the range of 75 – 80 °C. Similar results for CdS-TFT are shown in Figure 6-7 (b) with a wider temperature range from 70 to 85 °C to obtain higher value of mobility, 1 cm^2/V-sec.

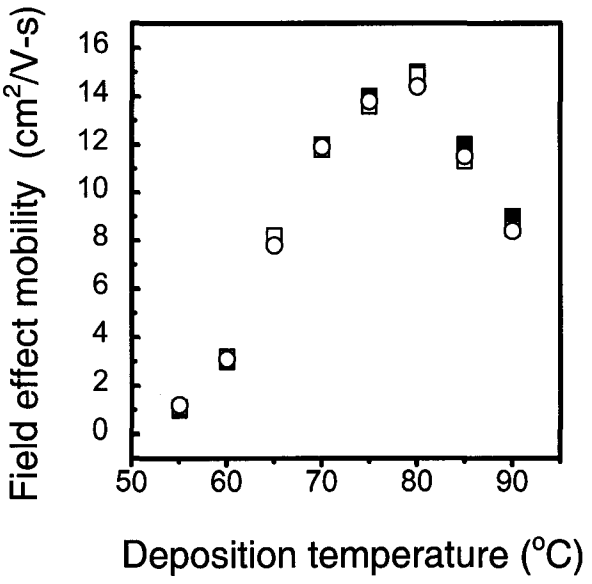


Figure 6-7(a) Relationship between CdSe deposition temperature and field effect mobility.

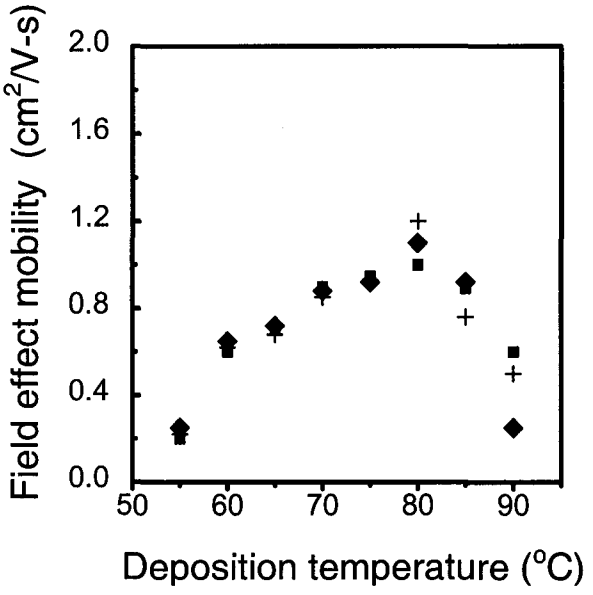


Figure 6-7(b) Relationship between CdS deposition temperature and field effect mobility.

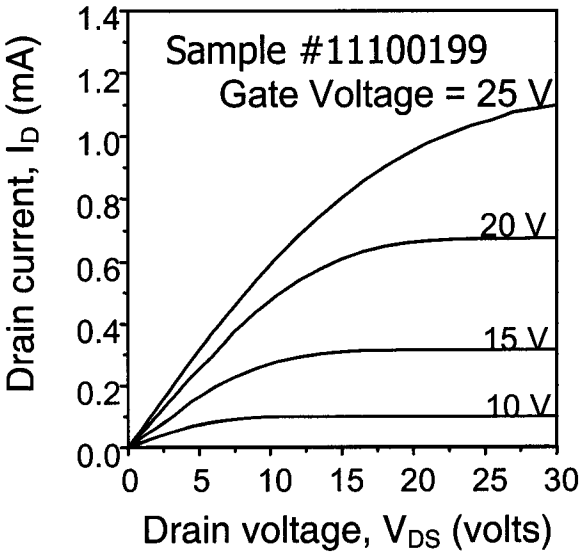


Figure 6-8(a) Output characteristics of a CdSe-TFT.

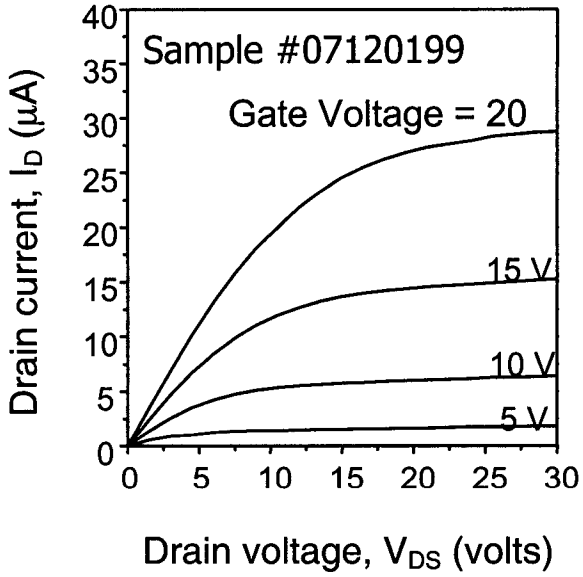


Figure 6-8(b) Output characteristics of a CdS-TFT.

6.2.8 Optimum CBD deposition conditions for CdS and CdSe

From the results shown in the previous sections, the best conditions for the fabrication of CdSe TFTs are as follows: CBD deposition temperature = 80 °C, thickness of CdSe = 200 nm, pH ~ 12, 0.1 M Na_2SSeO_3 reagent, 0.1 M $CdCl_2$ and 6.5 M NH_4OH.

For CdS TFTs, the best conditions are: deposition temperature = 80 °C, thickness = 200 nm, pH ~ 12, 0.005 M $CdCl_2$, 0.05 M thiourea, 0.05 M NH_4Cl, 0.8 M of NH_4OH for CdS-TFT.

6.2.9 Output characteristics, threshold voltage and transfer characteristics

In the previous discussion, On or OFF-current under specific biasing conditions is used to indicate the quality of the TFTs. Complete characterization of the TFTs require more complete set of data, which will be presented in this section. Figures 6-8 (a) and (b) depict drain current (I_D) – drain voltage (V_D) characteristics of a typical CdSe-TFT and a typical CdS-TFT fabricated under the best dipping conditions. Well-defined linear region and saturation can be seen. The ON-current of the CdSe-TFT and CdS-TFT at a gate bias of 10 V and a source-drain voltage 10 V was 100 μA and 5 μA, whereas the OFF-current at 10 V source-drain voltage was 9 pA and 3 pA, respectively.

From the output characteristics given in Fig. 6-8 (a), (b), values of the transconductance can be deduced. The transconductance values for the CdSe-TFT is 35.95 $\mu\Omega^{-1}$ and is 1.6 $\mu\Omega^{-1}$ for the CdS-TFT, both taken at V_D = 10 V and V_G = 10 V. As presented in section 6.2.7, the maximum field-effect mobility estimated for the CdSe-TFTs is 15 $cm^2V^{-1}sec^{-1}$ and is 1 $cm^2V^{-1}sec^{-1}$ for the CdS-TFTs.

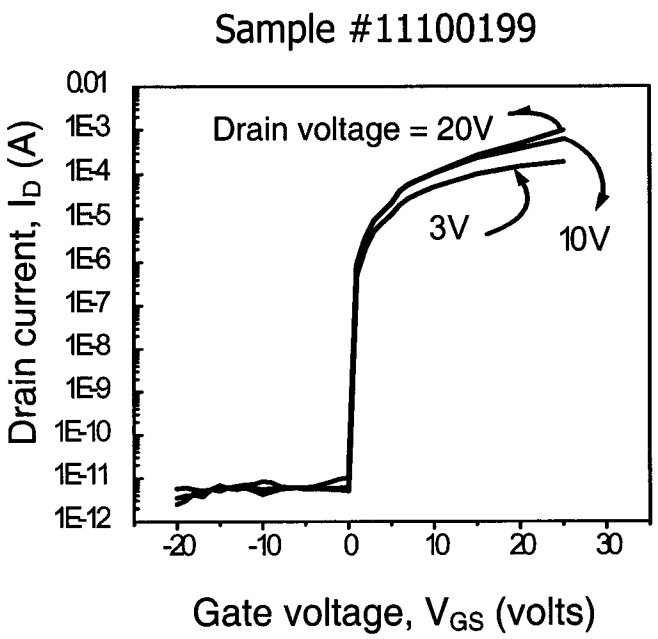


Figure 6-9(a) Transfer characteristics of a CdSe-TFT.

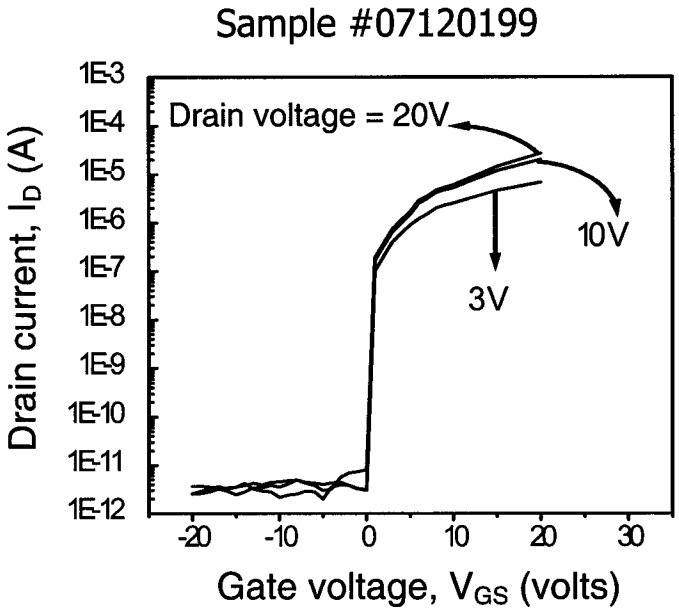


Figure 6-9(b) Transfer characteristics of a CdS-TFT.

Threshold voltage (V_T) of TFTs can also be obtained from the output characteristics. By plotting $(I_{DS})^{1/2}$ versus V_g and extrapolating the linear portion to abscissa, the value of V_T is determined. For the CdSe-TFT shown in Fig. 6-10, the threshold voltage value is 2.5 V and is 2.8 V for the CdS-TFT.

Transfer characteristics of the CdSe-TFT and CdS-TFT with a SiO_2 gate insulator are shown in Fig. 6-9 (a) and (b). Results show that a rapid transition from the OFF to the ON state as a gate voltage is increased from 0 to 3 V. For TFTs fabricated on a-Si and poly-Si, the drain current increases as the magnitude of gate voltage is increased. The increase in leakage current with the voltage is mainly due to the increase of electric field near the drain region. Since both CdSe and CdS are single carrier semiconductors, the OFF-current does not increase with increasing negative gate voltage. As can be seen in Fig. 6-9 (a) and (b), the ON/OFF current ratio I_{on}/I_{off} obtained from the plots of I_D versus V_G shown is about 10^7 at a gate bias of V_G = 20 V for both CdSe and CdS. This value exceeds that in TFTs based on a-Si or poly-Si. Therefore, the present TFTs may find applications in TFT/LCDs.

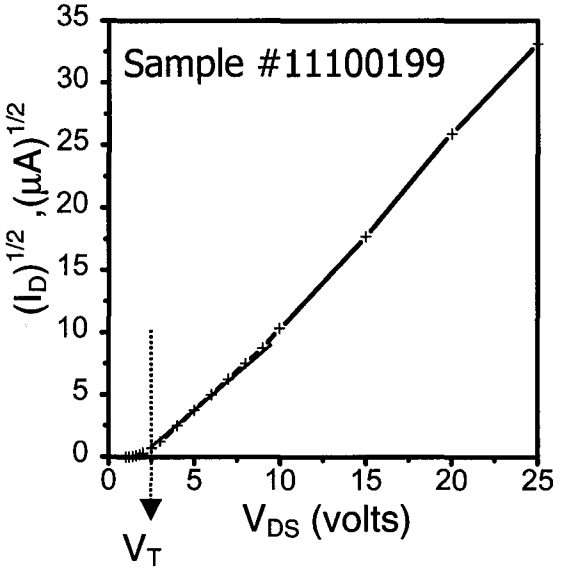


Figure 6-10 a plot of $\sqrt{I_D}$ versus V_{DS} for CdSe-TFT in saturation.

The threshold voltage estimated from extrapolation in Fig. 6-10 is about 2.5 V (for CdSe), with virtually no p-type conduction at negative gate bias voltage. Although the devices fabricated are not as good as poly-Si – TFTs by CVD or CdSe – TFTs by thermal evaporation, the method developed has potential for the production of array devices which require a low thermal budget and reduced production cost. The corresponding threshold voltage for CdS devices is 2.8 V.

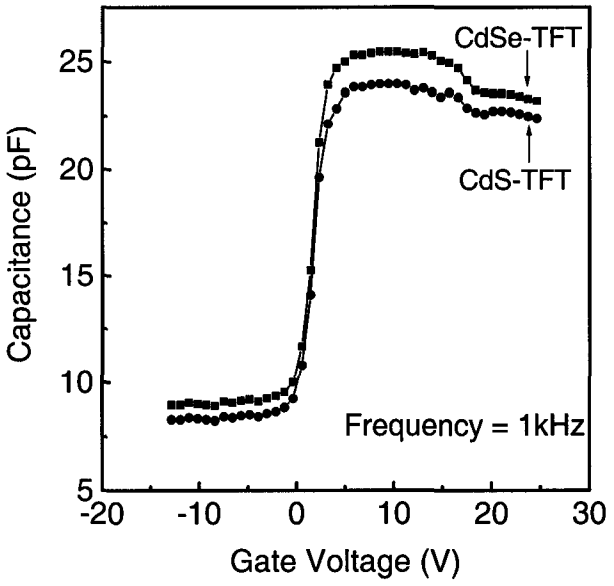


Figure 6-11 Plots of parasitic capacitance versus V_{GS} for CdSe-TFT (Sample # 11100199) and CdS-TFT (Sample # 07120199).

6.2.10 Differential capacitance versus voltage

In addition to the current-voltage measurements, it is necessary to carry out differential capacitance versus voltage measurements to characterize further the TFTs. This is required in order to confirm the on-set of accumulation and to estimate surface state density presented in Chapter 3. When operated in OFF state, the semiconductor in the MIS structure is depleted of carriers and the capacitance is small. When operated in the ON state, accumulation layer is formed in the semiconductor and the capacitance is large.

In a TFT, the parasitic capacitance, C_{gs}, may be determined by the overlap of the gate electrode and the source electrode. This overlap area is equal to the product of channel width and the overlap length. Fig. 6-11 shows plots of differential capacitance versus voltage for both CdS and CdSe-TFTs. It is seen that at low voltages, the contribution from the semiconductor layer causes low capacitances. When the gate voltage is increased, the contribution of the semiconductor capacitance decreases and the total capacitance increases. The capacitance reaches a maximum when an accumulation layer is formed so that the measured capacitance is equal to the capacitance of insulator.

The performance of the fabricated TFTs is also affected by a drift phenomenon. After the application of gate voltage, charging carriers may be trapped by the fast states in the semiconductor layer or by the slow states at the interface with the gate oxide [12]. These trapped electrons will screen the positive gate field. This will lead to a continuous decrease of ON current with time, or alternately a continuous increase of OFF current with time. The time dependence of the drain current at a gate voltage of V_G = 20 V measured as a function of time after being switched on is shown in Figure 6-12. Here, we can see that the current decreases by about 15 % in 90 seconds.

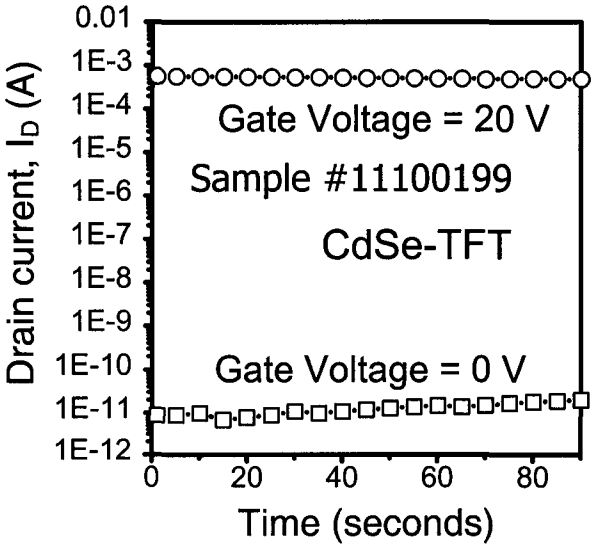


Figure 6-12 Drift of the ON current with time at V_D = 10 V for a CdSe-TFT with a thermally grown SiO_2.

6.2.11 Effects of ambient during the heat treatment

It is important to determine if the performance of TFTs can be improved further by treating them in difference atmospheres. Several CdSe-TFTs were fabricated under same conditions and then treated in vacuum, N_2, or air at a temperature range of 100 to 400°C for comparison. The results obtained are summarized in Figure 6-13. It is seen that the TFT with as-deposited CdSe is very resistive and the threshold voltage is greater than 30 V. This could be due to adsorption of oxygen molecules, which form acceptors in CdSe [13]. For the TFT annealed in vacuum, the threshold voltage is negative with a large magnitude. This could be due to a high donor concentration from the creation of Se vacancies after the vacuum anneal. For the one treated in air, the ON to OFF-current ratio is relatively small. The ON-OFF current ratio is the largest for the one treated in N_2 for a period of 5 minutes. When the heat treatment time is increased to 30 minutes, the current ratio decreases considerably. The results thus show that CdSe TFTs with the highest ON-OFF current ratio can be prepared by a short heat treatment in N_2. Any variations from the above have led to degradation of the device performance.

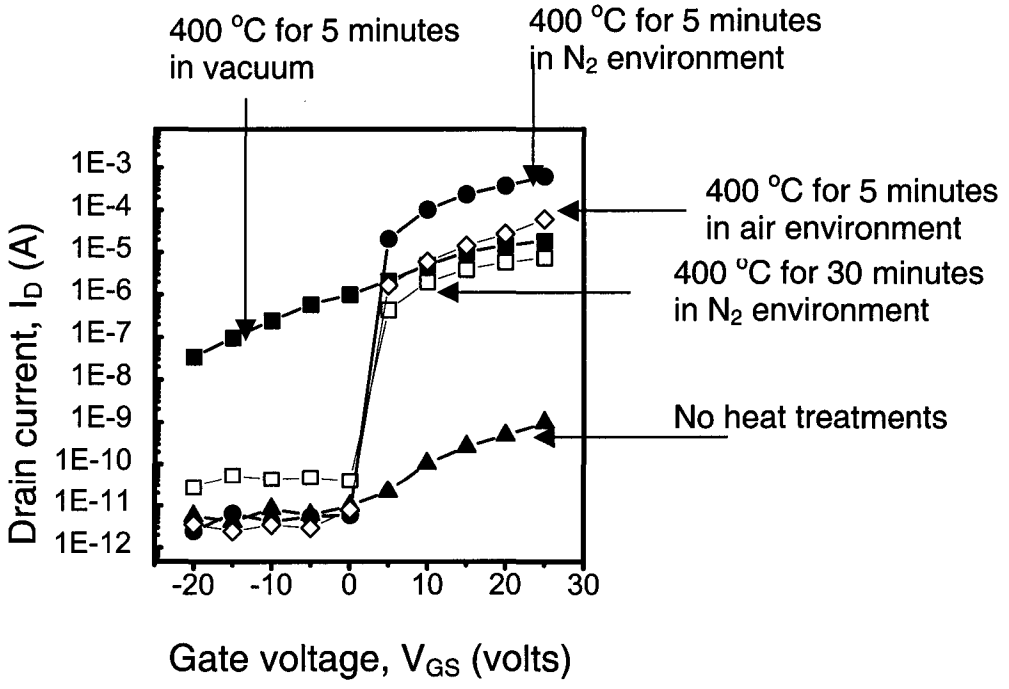


Figure 6-13 Transfer characteristics of the CdSe-TFTs with different annealing treatments (Sample #111099).

6.2.12 Thermal stability of TFTs prepared by CBD

One of the important parameters for any electronic devices is thermal stability. Thermal stability of the TFTs fabricated in the present work has been examined by periodic measurements of the threshold voltage up to a period of 6 months. One TFT treated in N_2 and another in air was selected for the stability studies for comparison. Figure 6-14 shows the variation of the threshold voltage for the two TFTs with time. The negative threshold shift in N_2-annealed CdSe-TFT is small. The TFT treated in air shows a large threshold voltage shift with time, which could be due to the desorption of surface acceptors, believed to be SeO_2 or H_2Se formed during annealing and exposure to the ambient. The surface reaction has been reported to be more pronounce with the presence of water related species during the heat treatment in air [14].

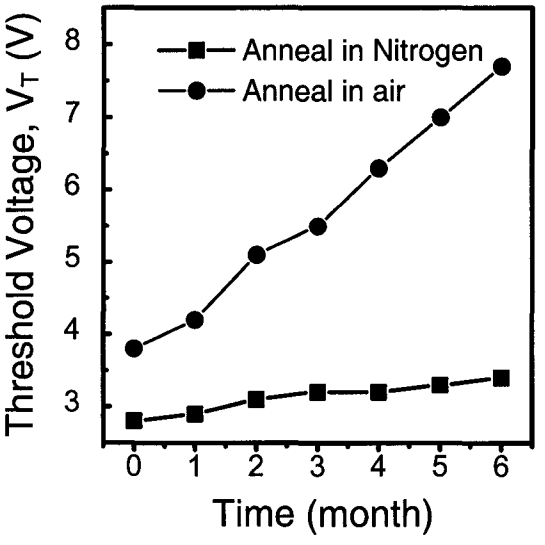


Figure 6-14 Change of threshold voltage with the time for the samples annealed either in N_2 or air at 400 °C for 5 minutes (Sample #111099).

6.2.13 Yield, uniformity and reproducibility of TFT fabrication

The yield of device fabrication can be defined as the number of working devices divided by the number of devices fabricated. In the present work for discrete TFTs with channel lengths or 20 μm or more, the yield is close to 100%. However, the yield decreased substantially when the channel lengths were reduced to 10 μm or less. For the TFTs with channel lengths equal to or less than 10 μm, leakage currents were unacceptably high. For the TFTs with a channel length of 20 μm, the uniformity in device characteristics for all 16 devices across the substrate as determined from the value of the ON current was also investigated. The results showed a deviation of ± 23 % for CdSe-TFTs and ± 16 % for CdS-TFTs.

The reproducibility was also estimated by carrying out 10 fabrication rounds under the same fabrication conditions and examining the variation of ON current of the resulted TFTs. The results show a deviation ± 11 % for CdSe-TFTs and ± 4.8 % for CdS-TFTs, averaged over all 16 TFTs in each substrate. It is noted that the fabrication of CdSe-TFTs is more time consuming and condition sensitive than that for CdS-TFTs. This is due to the critical dipping conditions and time length required to prepare the dipping solution for CdSe.

The initial number of free carriers, n_o (electrons or empty traps) was evaluated by $V_T \equiv -n_o q / C$. The maximum number of electrons per unit area, n_{max} was evaluated by Equation 3.8 in Chapter 3. The carrier concentration was also evaluated by Equation 3.9. Furthermore, interface state density was evaluated by Equation 3.10. The results obtained from the above calculations are summarized in the Tables 6-1 and 6-2. It is noted that the condition for enhancement modulation only occurs when $n_{\max} > n_t > n_o$.

6.3 Conclusions

The method developed in the present work involves the application of a novel CBD method to prepare thin films at low temperatures. In this method, controlled chemical reaction is allowed to take place in a chemical bath, which proceeds at a low rate in an aqueous solution containing the various reactants. The chemical bath deposition conditions for both CdS and CdSe have been investigated systematically by varying pH values, relative concentrations of reactants and temperature. It was found that TFTs fabricated on the films formed at higher temperatures and pH values (with appropriate concentrations of the reactants) showed higher On-currents and field effect mobilities.

A systematic characterization of TFTs with different thicknesses of active layers was also made. The results showed that the optimal thickness of active layers of TFTs having low leakage and large ON currents is around 0.2 μm. In this work, CdSe-TFTs and CdS-TFTs with a sharp transfer characteristic and a large switching ratio of 10^6 (at a gate voltage of 10 volts) have been successfully fabricated by the CBD method. The carrier mobility in the CdSe-TFTs exceeds 10 cm^2/V-sec with a maximum value of 15 cm^2/V-sec.

The best dipping conditions developed in this thesis for both CdS and CdSe have been established and these are summarized in Tables 6-3 and 6-4. Preliminary uniformity and reproducibility studies on the present TFTs have shown satisfactory results. Since the CBD process can be carried out at temperatures below the boiling point of water and the subsequent heat treatment carried out at 400°C, which is below the softening point of conventional glass substrates, the procedures established in this work may be further developed for low cost production of large area TFT circuits.

Table 6 – 1			
Parameters for CdSe-TFT with thermally grown SiO_2			Method or Note
$T_{thickness\ of\ CdSe}$	(nm)	200	CBD (80°C)
$T_{thickness\ of\ gate\ oxide}$	(nm)	60-100	Thermal (1050°C)
$\varepsilon_{dielectric\ constant}$	(SiO_2)	3.9	General
$\varepsilon_{dielectric\ constant}$	(CdSe)	10.8	General
$L_{channel\ length}$	(μm)	20	Measured
$W_{channel\ width}$	(μm)	200	Measured
$C_{gate\ capacitance}$	(nF/cm^2)	30-58	Measured
V_{gate}	(V)	10	Applied
V_{drain}	(V)	10	Applied
$V_{threshold}$	(V)	2.5 – 5.3	Calculated
$n_{o,\ initial\ trap\ density}$	(cm^{-2}) x 10^{11}	6.7 – 10.5	Calculated from V_t
$N_{t,\ interface\ state\ density}$	(cm^{-2}) x 10^{12}	1.9 – 2.8	Calculated from S
$N_{carrier\ concentration}$	(cm^{-2}) x 10^{11}	1.6 – 3.3	Calculated
$n_{max.}$	(cm^{-2}) x 10^{12}	2.2 – 3.8	Calculated
I_{ON}	(μA)	80 –100	Measured
I_{OFF}	(pA)	5 – 9	Measured
$\mu_{effective\ mobility}$	(cm^2/V-s)	10 –15	Calculated
$g_{transconductance}$	($\mu\Omega^{-1}$)	35.95 – 46.5	Calculated
$\tau_{response\ time}$	(ns)	35 – 62	Calculated
$S_{subthreshold\ slope}$	(V/decade)	0.8 – 1.2	Calculated
Annealing	(min)	3 – 5	400 °C in N_2
Performance Uniformity		± 23 %	(Variation in I_{ON})
Reproducibility		± 11 %	(Variation in I_{ON})
Yield		~ 100%	

Table 6 – 2			
Parameters for CdS-TFT with thermally grown SiO_2			Method or Note
$T_{thickness\ of\ CdSe}$	(nm)	200	CBD (80°C)
$T_{thickness\ of\ gate\ oxide}$	(nm)	60-100	Thermal (1050°C)
$\varepsilon_{dielectric\ constant}$	(SiO_2)	3.9	General
$\varepsilon_{dielectric\ constant}$	(CdS)	10.6	General
$L_{channel\ length}$	(μm)	20	Measured
$W_{channel\ width}$	(μm)	200	Measured
$C_{gate\ capacitance}$	(nF/cm^2)	30-58	Measured
V_{gate}	(V)	10	Applied
V_{drain}	(V)	10	Applied
$V_{threshold}$	(V)	2.8 – 5.2	Calculated
$n_{o,\ initial\ trap\ density}$	(cm^{-2}) x 10^{11}	7.5 – 9.4	Calculated
$N_{t,\ interface\ state\ density}$	(cm^{-2}) x 10^{12}	1.9 – 2.8	Calculated from S
$N_{carrier\ concentration}$	(cm^{-2}) x 10^{10}	2.4 – 5.8	Calculated
$n_{max.}$	(cm^{-2}) x 10^{12}	2.2 – 3.8	Calculated
I_{ON}	(μA)	3 – 10	Measured
I_{OFF}	(pA)	1 – 4	Measured
$\mu_{effective\ mobility}$	(cm^2/V-s)	0.8 –1	Calculated
$g_{transconductance}$	($\mu\Omega^{-1}$)	1.2 – 1.6	Calculated
$\tau_{response\ time}$	(μs)	0.5 – 2.6	Calculated
$S_{subthreshold\ slope}$	(V/decade)	0.8 – 1.2	Calculated
Annealing	(min)	3 – 5	400 °C in N_2
Performance Uniformity		± 16 %	(Variation in I_{ON})
Reproducibility		± 4.8 %	(Variation in I_{ON})
Yield		~ 100%	

Table 6-3 the best dipping condition for CdSe-TFT	
Relative ion concentration:	0.1 M Na_2SSeO_3, 0.1 M $CdCl_2$, and 6.5 M NH_4OH
pH value:	~12
Temperature:	80 ± 2°C
Mixing time before dipping:	2 minutes
Stirring during CBD:	Yes
Dipping time :	5 minutes
Dipping times:	8
Cleaning the beaker after dipping:	yes
Ultrasonic cleaning after dipping:	1 minute
Ultrasonic cleaning solution:	DI water

Table 6-4 the best dipping condition for CdS-TFT	
Relative ion concentration:	
5 mM $CdCl_2$, 50 mM of thiourea, 50 mM NH_4Cl, 0.8 M NH_4OH	
pH value:	~12
Temperature:	80 ± 2°C
Mixing time before dipping:	3 minutes
Stirring during CBD:	Yes
Dipping time:	3 minutes
Dipping times:	4
Cleaning the beaker after dipping:	yes
Ultrasonic cleaning after dipping:	1 minute
Ultrasonic cleaning solution:	DI water

REFERENCES

1. G. Fortunato, "Polycrystalline silicon thin-film transistors; A continuous evolving technology," Thin Solid Films, 296, pp. 82-90, 1997.

2. A. C. Tickle, 1st ed. (John Wiley & Sons, Inc., 1969) pp. 2-40.

3. T. P. Brody, J. A. Asars, and G. D. Dixon, IEEE Trans. Electron Devices, vol. ED-20, no. 11, pp. 995-1001, 1973.

4. P. K. Weimer, "The TFT – a new thin-film transistor," Proc. IRE, vol. 50, pp. 1462-1469, 1964.

5. T. L. Credelle, "Thin film transistors for video applications," International Display Research Conference, pp. 208-213, 1988.

6. R. S. Mane, and C. D. Lokhande, "Studies on chemically deposited cadmium sulphoselenide (CdSSe) films," Thin Solid Films, vol. 304, pp. 56-60, 1997.

7. C. D. Lokhande, "Chemical deposition of metal chalcogenide thin films," Materials Chemistry and Physics, vol. 27, pp. 1-43, 1991.

8. P. K. Nair, M. T .S. Nair, V. M. Garcia, O. L. Arenas, Y. Pena, A. Castillo, I. T. Anala, O. Gomezdaza, A. Sanchez, J. Campos, H. Hu, R. Suarez, M. E. Rincon, "Semiconductor thin films by chemical bath deposition for solar energy related applications," Solar Energy Materials & Solar Cells, vol. 52, 313-344, 1998.

9. M. T. S. Nair and P. K. Nair, "Enhancement of photosensitivity in chemically deposited CdSe thin films by air annealing," Journal of Appl. Phys., vol. 74, pp. 1879-1884, 1993.

10. V. M. Garcia, P. J. George, M. T. S. Nair, and P. K. Nair, "CdSe:In-In_2O_3 coatings with n-type conductivity produced by air annealing of CdSe-in thin films," Journal Electrochem. Soc. vol. 143, no. 9, pp. 2892-2895, 1996.

11. S. Morozumi, "Active matrix addressed liquid crystal displays," Proceedings of 1985, International Solid-State Circuits Conference, pp, 266-267, 1988.

12. J. C Anderson, "Thin film transistors," Thin Solid Films, vol. 36, pp. 299, 1976.

13. G. A. Somorjai, J. Phys. Chem. Solids, vol. 24, pp. 175, 1963.

14. S. Belkouch, D. Landheer, D. P. Masson, S. R. Das, T. Quance, L. LeBurn, and S. J. Rolfe, "Effects of initial annealing treatments on the electrical characteristics and stability of unpassivated CdSe thin film transistors," J. Vac. Sci. Technol. A, vol. 16, pp. 860 –863, 1998.

Chapter 7

TFTs on Glass Substrates

7.1 Introduction

In order to employ the novel process to form TFTs on glass substrates instead of the Si substrate, the thermal silicon oxide formed at high temperatures (~1050°C) must be replaced by other oxides or insulators which can be grown at low temperatures, preferably below 400°C. Dielectrics formed by two different methods have been used in this work to fabricate TFTs on glass substrates. One is anodic oxide prepared by anodization and the other is SiN_x prepared by a sputtering method. Both CdS and CdSe-TFTs were then fabricated and studied and the results obtained are presented in this chapter.

7.2 CdSe-TFTs and CdS-TFTs with anodic oxide

7.2.1 Anodic Al_2O_3 for gate insulator

Thin film transistors having an inverted structure have been studied extensively because of their use in TFT/LCDs. In addition to the development and improvements on active semiconductor layers, the development of interconnects and dielectrics are important. In the 1990s, due to the demand of TFT/LCDs with increased dimensions and resolution, various efforts have been devoted to developing low-resistivity gate lines to meet the need for large, high-resolution LCDs [7-1]. Among various candidates, Al has been accepted as a good candidate for fabricating gate lines because of their low resistivity, low cost, and good adhesion. However, the thermal expansion mismatch between Al films and glass substrates can result in a large stress in the Al films upon heating. This large stress could lead to the formation of hillocks [7-2] or whisker [7-3]. When Al films with hillocks or whisker are used to form gate lines, shorting and leakage may occur between the gate lines and data lines.

To reduce the formation of hillocks and whiskers, several methods has been proposed, such as anodization [7-4], capping with refractory metals [7-5], and alloying [7-6]. Among those, the most effective method to suppress the hillocks and whiskers is anodization. During anodic oxidation, aluminum oxide may be formed at room temperature and used as a protective layer against hillocks. The aluminum oxide may also function as a gate insulator in a TFT and will be discussed in the following section.

7.2.2 Experiments for anodization

The principle of anodization is relatively simple. When a piece of Al is immersed in a suitable acid electrolyte and with a voltage applied to induce a current through the Al, a layer of anodic oxide will form on the surface. It is noted that Al acts as the anode

whereas another metal (Pt) forms the cathode during the anodization. The acid used to form the electrolyte could be tartaric acid.

Although the principle is simple, anodization process still needs to be optimized in order to produce gate dielectrics with high breakdown field and low leakage current. Information to correlate the final anodization voltage to dielectric thickness is also required for the devices fabrication. Variations of quality of the anodized Al_2O_3 dielectric with the variations of deposition conditions are also important. Using the anodized dielectrics, TFTs have been fabricated in the present work. The experimental details and the results obtained will be described in subsequent sections.

Thin films of Al with a thickness of about 0.8 μm were deposited on cleaned glass substrates by evaporation. The Al-coated glass substrates were then used in anodization employing the unit as shown in Figure 7-1. The electrolyte used is an ethylene glycol solution mixed with the tartaric acid at a pH ~ 7 by adding ammonia hydroxide. When a voltage is applied between the Pt (negative) and Al/glass (positive), some of H_2O molecules are electrolyzed into hydrogen ions, which became H_2 gas after the reaction with the electrons, and oxygen ions will react with the ions of aluminum created by the release of electrons from aluminum, as shown in Figure 7-1. The bias voltage has to be increased to maintain constant electrical current. After reaching the predetermined voltage, the voltage will be kept constant while the current is allowed to decrease until the anodization reaction is completed. The more detailed mechanism for anodization can be found in the references [7-7,8].

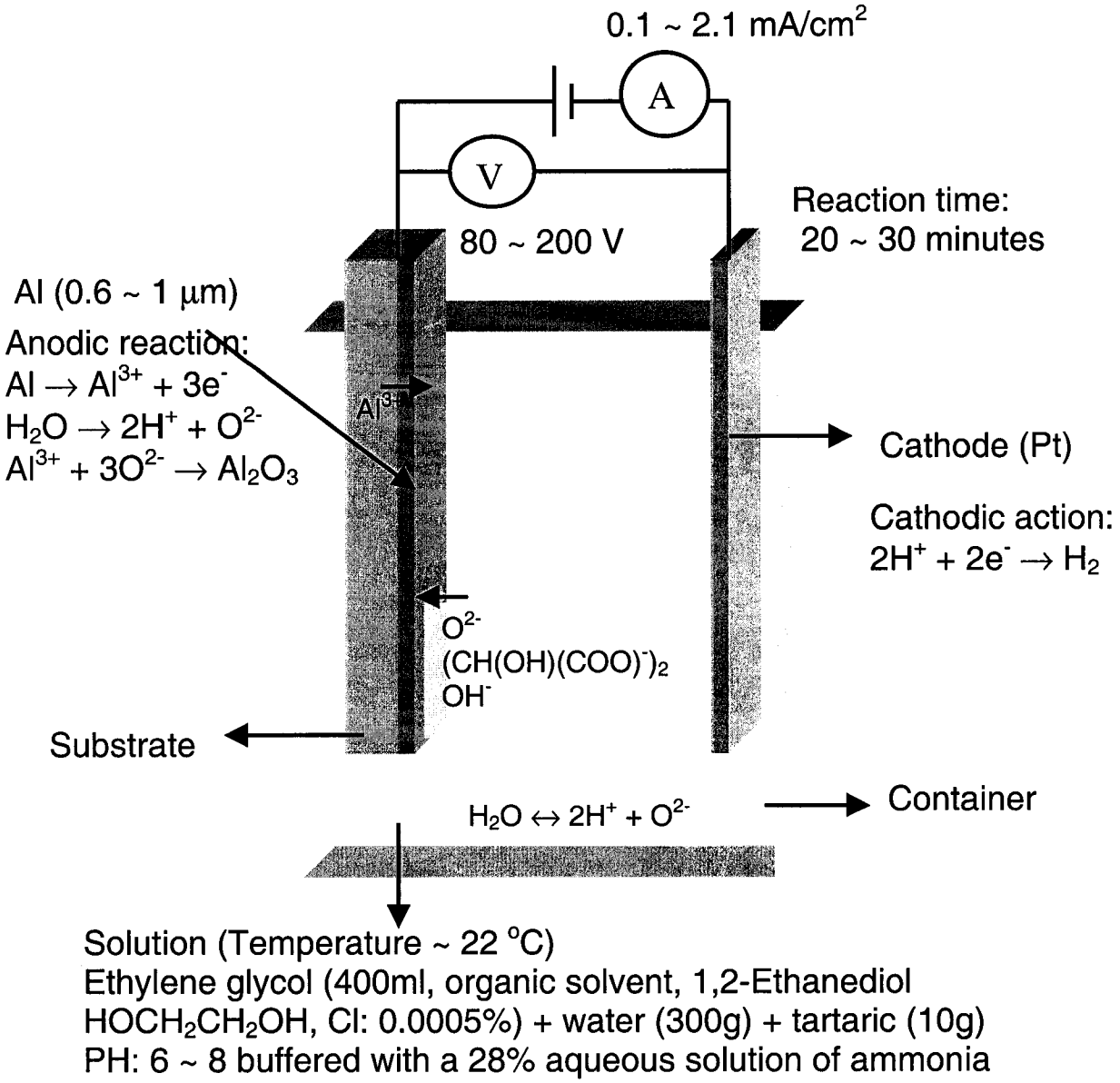


Figure 7-1 Experimental setup for Al anodization.

The rate of anodization (or formation of oxide) increases as the current density is increased, due to the enhanced rate of formation of aluminum ions (Al^{3+}) and the associated rate of combination with oxygen ions at the anode-electrolyte interface. At the

interface, the rates of transfer of oxygen and aluminum ions are coupled through the common potential difference according to the reaction. The chemical reactions can be described as follows:

$$H_2O + 2e^- \rightarrow O_2^- + H_2$$

$$Al_{Metal} \rightarrow Al^{3+} + 3e^-$$

$$2Al + 3H_2O \Leftrightarrow Al_2O_3 + 3H_2$$

Initially, barrier-layer formation is a strong function of the current density. However, as the anodization precedes the transport of anions and cations through the film is restrained, due to the decrease in field strength across the film with the increase in the thickness of the anodizing layer. The electrolytes used often consist of the following three components: (i) glycol, (ii) water, and (iii) a suitable acid. Here, water plays the role of the anodic oxidant for Al, while the acid is added to assist ionic conduction in the electrolyte. The selection of the acid is not inconsequential since it might cause some disastrous effects on the oxide growth, such as in-situ oxide dissolution if improperly used. As for component (i), ethylene glycol has been reported to be capable of reducing the limiting current density, the solubility of the initial anodic products and the transport rate of these products.

From the mechanism of anodic oxidation mentioned above, it is clear that many factors can determine the growth of Al_2O_3 layer. In the initial stage of the present anodization, the applied voltage is increased continuously to maintain a constant current density. Then, it is kept at a predetermined level for a period of time (from 2 minutes to 4 minutes), during which the current density begins to decay. As the predetermined limit of anodization current has been reached, the power is switched off and anodization is completed. It is thus clear that the thickness of the anodized Al_2O_3 film is control by the duration of the anodization with constant current density or the terminal voltage for the constant current density deposition. In the subsequent anodization stage where the current reduces to minimum, possible voids and defects in the anodized film are filled and the total thickness of the film remains essentially constant. After the above-described

anodization process the substrate with the Al_2O_3 film is removed from the electrolytic bath and immersed into a beaker containing ethylene glycol for a few minutes. This is followed by a final rinse in deionized water.

For applications as gate insulators in TFTs, the anodized Al_2O_3 must have a high breakdown voltage and low leakage current. This is because breakdown can lead to the destruction of capacitors formed and hence the TFTs whereas an excessive current leakages can reduce the value of On-Off current ratio and charge retention time. Physically, Al_2O_3 is required to have surface flatness, because the next layer takes on the morphology of the underlying surface. If the Al_2O_3 film has a rough surface, the surfaces of the CdSe or CdS layer will be rough, and the field effective mobility of the semiconductor layer will be affected. To obtain an anodically oxidized film with a high breakdown voltage and low leakage current, we have to focus on the anodic conditions. The current density and the ethylene glycol concentration of the electrolyte should also be included as the elements of the anodic oxidation condition matrix. The experiment in this work will be concentrated on the most influential factor of anodic DC voltage, DC current density and the ethylene glycol concentration. Therefore, there are two groups of applied bias conditions during anodic oxidation: one is under a constant anodic voltage (80 ~ 200 V), and the other is under a constant anodic current density (0.3 ~ 2.1 mA/cm^2). All the experiments were performed at room temperature (~22 °C). In addition, for investigating the annealing effect on the insulation properties, some of the examples with the Al_2O_3 layer densified at 200 – 400°C for 20 – 90 minutes in nitrogen ambient were prepared.

In order to evaluate the anodic oxidation rate of Al_2O_3 layer, the thickness of the Al_2O_3 film was determined by both capacitance-voltage (C–V) measurement and direct inspection of cross-section under scanning electron microscope (SEM). The thickness of the dielectric varied according to anodization conditions. Aluminum was anodized to a thickness between 0.1 μm and 0.4 μm, while the majority of the characterization was performed with dielectrics around 0.2 μm for the following chemical bath deposition process. After the anodization and annealing process, a new Al square region with an area 1.6×10^{-3} cm^2 was formed onto the Al_2O_3 film to produce metal-insulator-metal (MIM)

capacitors for the measurements of breakdown field and leakage current. C-V measurements were carried out using an HP model 4274 LCR meter, whereas an HP model 4145A semiconductor parameter analyzer was used for electrical characterization. The effects of ratio of the ethylene glycol to water, and the DC current density on the growth of anodic film were specifically investigated and the results will be presented in the following section.

7.2.3 Results and discussion

The anodization procedure starts with constant current and ends with constant voltage. Figure 7-2 shows the relationship between the applied current, voltage, and film thickness variation with time using the present procedure. The power supply is first set at constant current to initiate the anodization. Due to the initial formation of the oxide, the series resistance of the anodizing circuit increases.

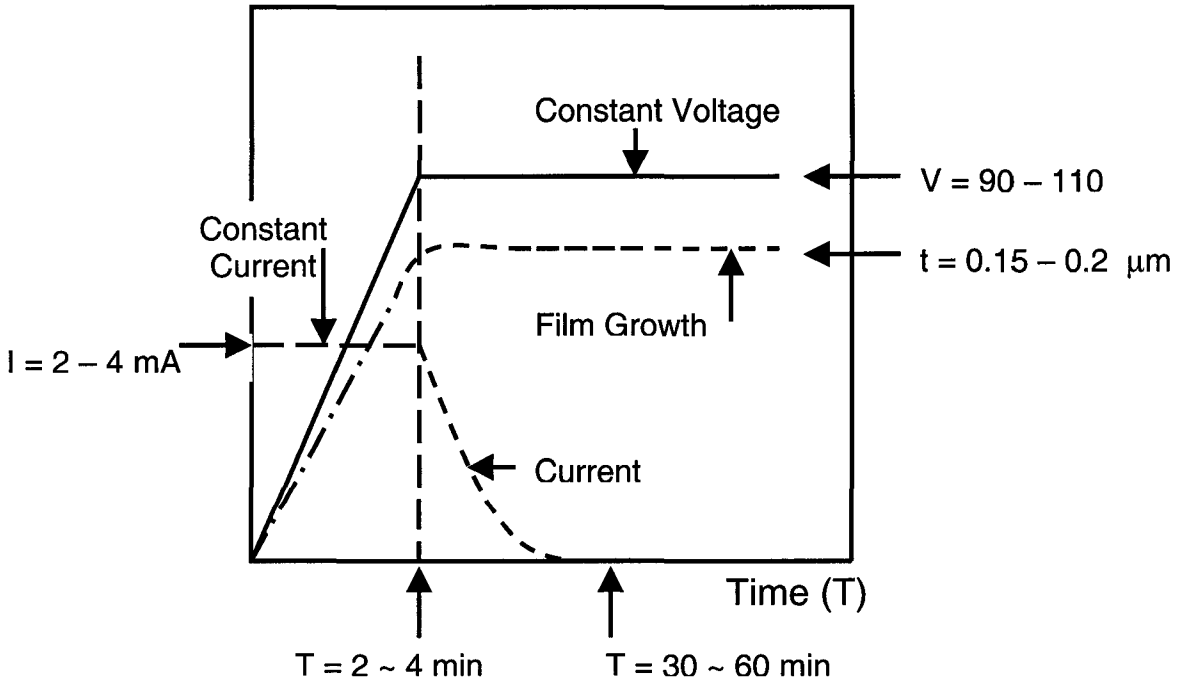


Figure 7-2 Anodization parameters as a function of time

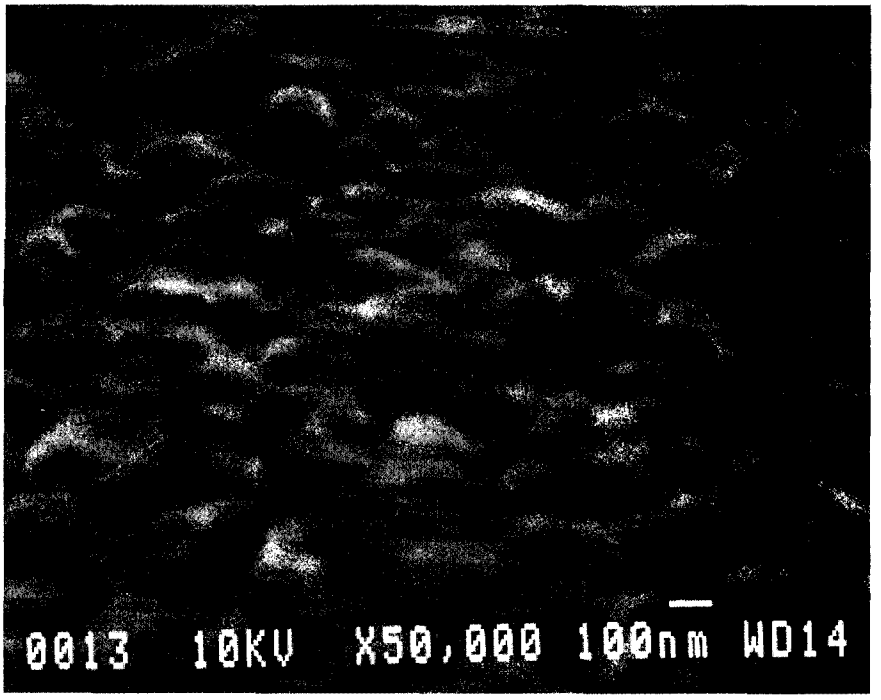


Figure 7-3 (a) SEM photograph of the surface of an anodic Al_2O_3 (Sample #145).

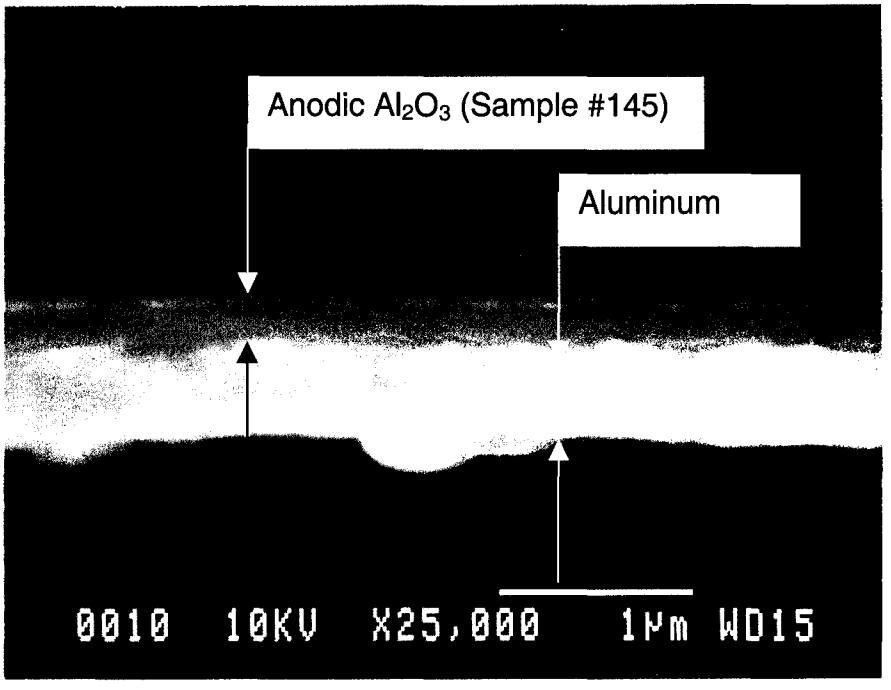


Figure 7-3 (b) SEM cross-section view of an anodic Al_2O_3.

To maintain the constant current, the voltage need to be increased. After the voltage has been increased to a pre-determined value, the power supply is switched to constant voltage mode and held at this voltage until the current decreased to below 10 % of the starting value in the constant current mode of operation. Using this procedure, the anodizing current in the growth phase is high, resulting in shorter processing times.

After the anodization, thickness of the anodized Al_2O_3 dielectric layers was determined by C-V method and by SEM examination. Figure 7-3 (a) is a SEM micrograph of the surface of the anodic oxide and (b) shows a fractured cross-section for the sample. The anodization rate is the highest in the initial stage with constant current density and the subsequent stage at constant voltage serves to densify the oxide film. Hence the density of voids can be minimized [7-7].

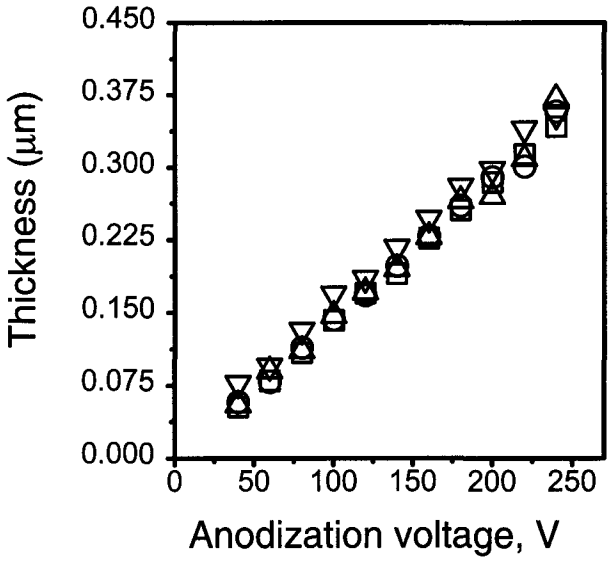


Figure 7-4 Thickness measurements with varied anodization voltage for Al_2O_3 layer (Sample #100~145).

Fig. 7-4 shows the variation of the film thickness with the variation of the final constant voltage. It is noted that the thickness of the Al_2O_3 films increases almost linearly with the increase of the final applied voltage. The ratio of the dielectric film thickness to

the final applied voltage was found to be around 14.5 Å/V. If the value of the final applied voltage is 100 volts, the resulted oxide film will be 1450 A. The values obtained have been used to compare with that obtained from capacitance measurements, indicating consistent thickness results.

In addition to the thickness control, the quality of oxide can be affected by the anodizing conditions. The quality of the anodized Al_2O_3 films was determined by measuring the breakdown electric field and leakage current density. Among the parameters, the concentration of ethylene glycol and pH values were found to be significant.

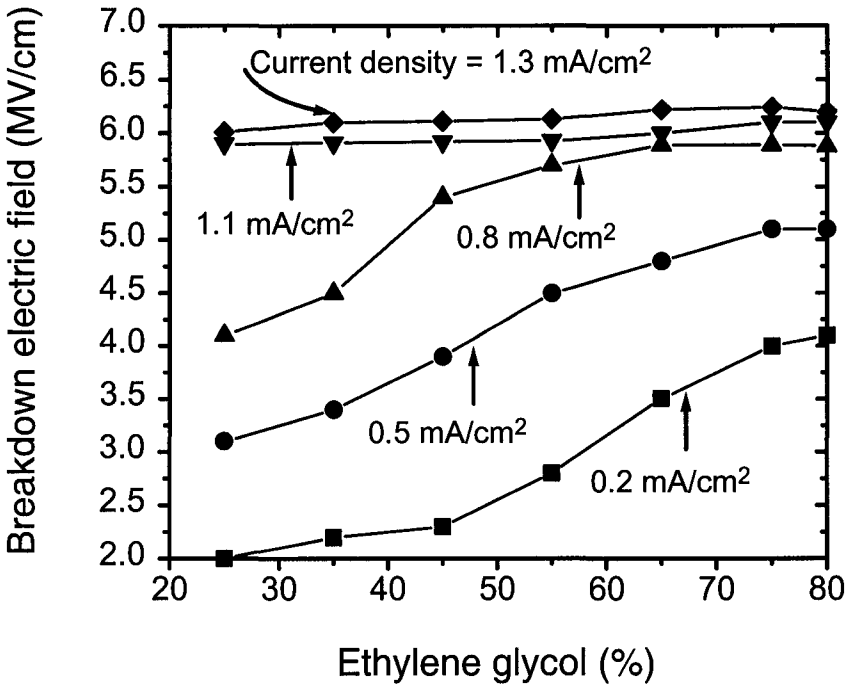


Figure 7-5 Breakdown electric field as a function of ethylene glycol concentration in the electrolytes for different current densities.

Figure 7-5 shows the variation of breakdown electric field of the Al_2O_3 films, with the variation of concentration of ethylene glycol, anodized at different current densities. It

is noted that the breakdown fields are low for the films formed at current densities below 0.8 mA/cm^2. For those formed at 1.1 mA/cm^2 and 1.3 mA/cm^2, the breakdown electric fields are about 6 MV/cm. It is also noted that at these two current densities, the effects of ethylene glycol concentration on the breakdown electric field is less compared to that anodized at low current densities. To form Al_2O_3 dielectric films with high breakdown electric fields at low current densities (< 0.8 mA/cm^2), electrolytes with ethylene glycol concentration greater than 65% are preferred.

In addition to the breakdown electric field, leakage current is another indication of the quality of the anodized dielectric layers. Figure 7-6 shows the variation of the leakage current density with the change in ethylene glycol concentration at different current densities. It is seen that the leakage current density decreases as the ethylene glycol concentration is increased from 25% to 80%. Minimum leakage current densities are achieved for those with the deposition current densities of 1.1 mA/cm^2 and 1.3 mA/cm^2.

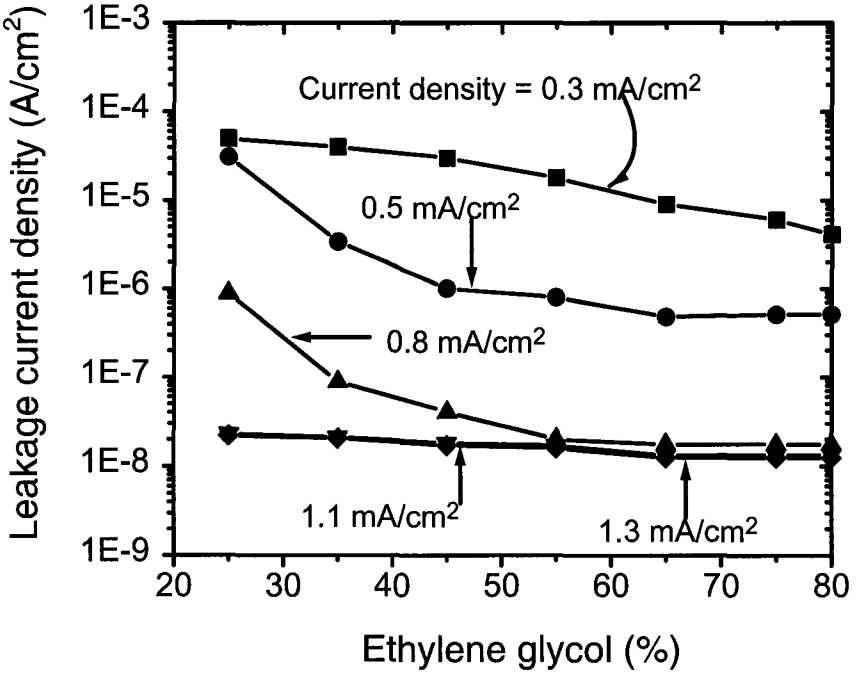


Figure 7-6 Leakage current density as a function of ethylene glycol concentration in the electrolytes for different current densities.

The effects of pH values of the electrolytes on the breakdown field were also studied in the present work and the results obtained are shown in Figure 7-7. These experiments were carried out using an electrolyte with 65% of ethylene glycol and a current density of 1.1 mA/cm^2. It is noticed that the breakdown electric field increases with the increase of pH value, reaches a maximum at pH = 7 then decreases with further increase of the pH value in the electrolyte.

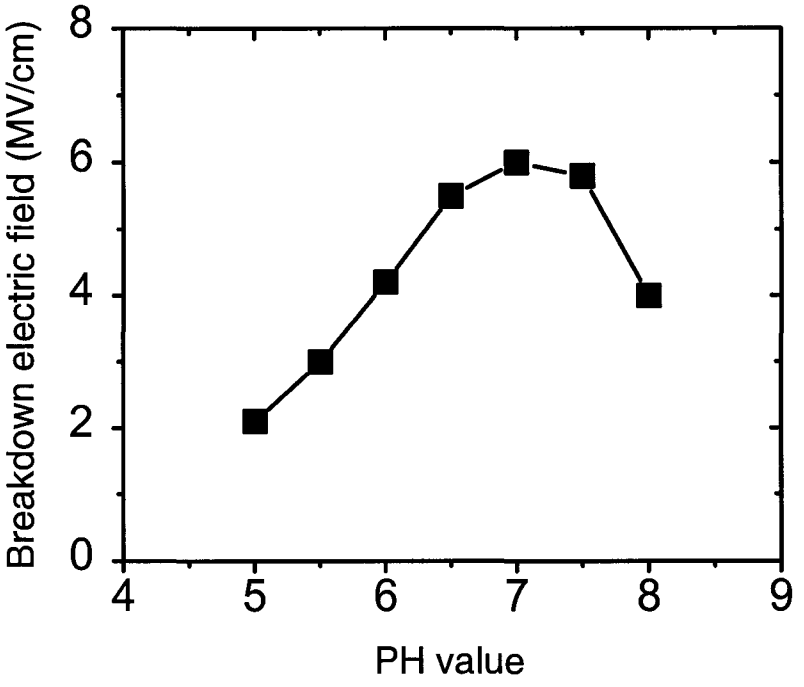


Figure 7-7 Breakdown electric field as a function of pH value.

The leakage current varies with the applied voltage across the MIM structure. Results for three samples fabricated on Al-coated glass substrates are shown in Figure 7-8. It is seen that the leakage current is only 15 nA/cm^2 even at a voltage of 40 V.

Several samples were selected to examine thermal stability of the anodized aluminum oxide. To test these devices, the applied voltage was limited to within the non-destructive breakdown voltage, which is defined as the potential difference required to increase the

current to 10 $\mu A/cm^2$ [7-16]. For the samples annealed at 250 °C for a period of 2 hours, the leakage current decreases by one order of magnitude from the original values, as shown in Figure 7-9. Additional annealing and higher temperature did not reduce further the leakage current.

From the results described above, we conclude that the best conditions for the preparation of anodic Al_2O_3 dielectric layers in this thesis are as follows: a current density of 1.1 mA/cm^2, ethylene glycol concentration of 65 % with a pH = 7, post anodizing annealing at 250 °C for 2 hours in N_2 environments. In subsequent experiments carried out for the TFTs, all of the Al_2O_3 dielectric gate layers will be prepared under the above conditions.

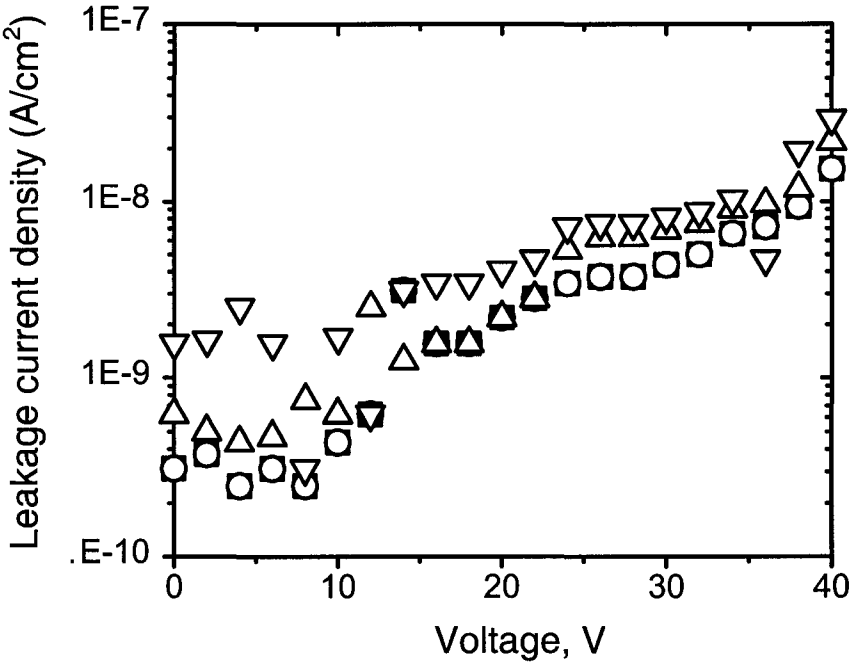


Figure 7-8 Leakage current density as a function of applied voltages for 48 nF/cm^2, Al_2O_3 capacitors on glass substrate (Sample #145).

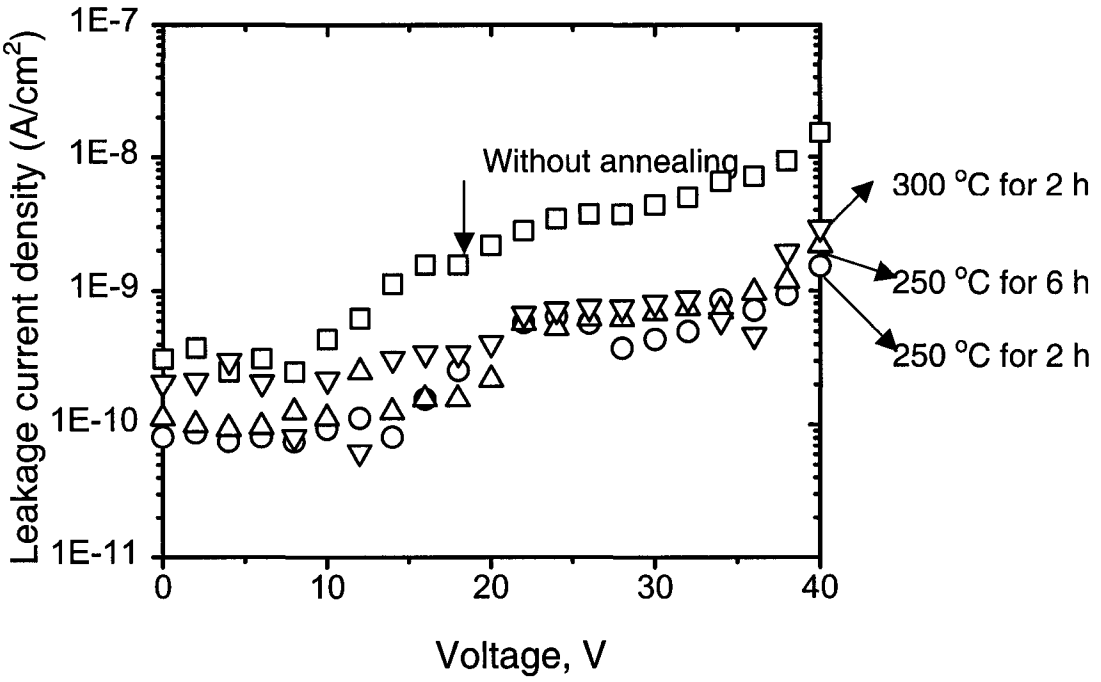


Figure 7-9 Leakage current density as a function of applied voltage for 48 nF/cm^2 Al_2O_3 capacitors on glass substrate with different annealing conditions (Sample #145~150).

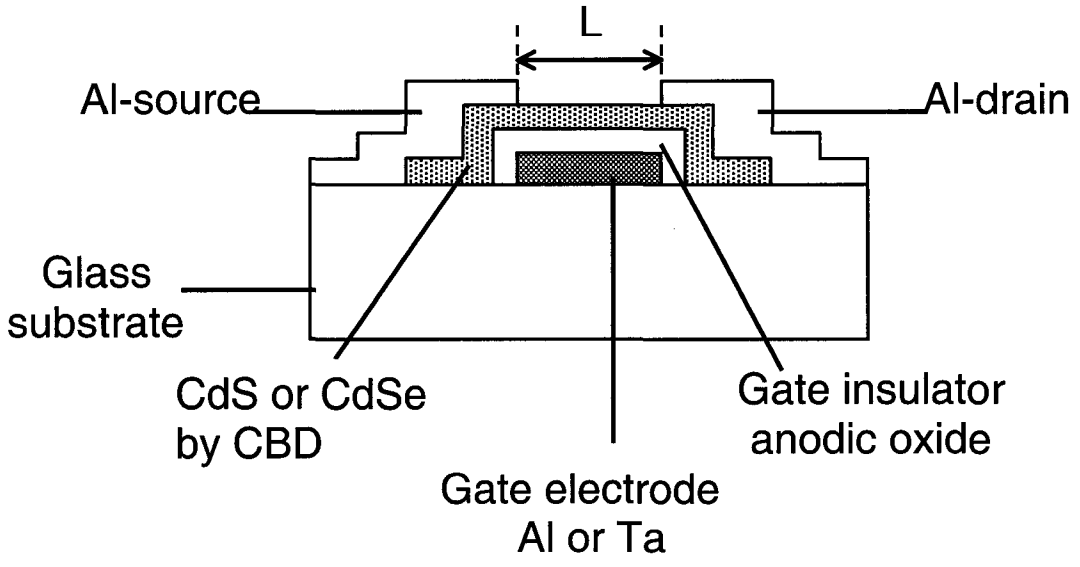


Figure 7-10 A schematic diagram of TFT with anodic oxide gate dielectric.

The fabrication procedures of the TFTs on Si substrates have been presented in Chapter 4. The fabrication of TFTs on glass substrates is similar to that on Si and will be briefly described below. Firstly, a layer of metal Al was deposited by standard vacuum evaporation then patterned to form the gate on a glass substrate. Secondly, a layer of Al_2O_3 dielectric was formed by the anodization process described above. Due to the nature of the anodization process, only the surfaces of the metal layer will be covered by the dielectric layers. Thirdly, a layer of CdS or CdSe was deposited over the entire sample surface by CBD method and this was patterned by a photolithography and etching method to create active channel region of the thin film transistor. Fourthly, electrical contacts for drain and source were prepared by a vacuum deposition and selective etching method. Finally, the fabricated TFTs were placed in a furnace for heat treatment.

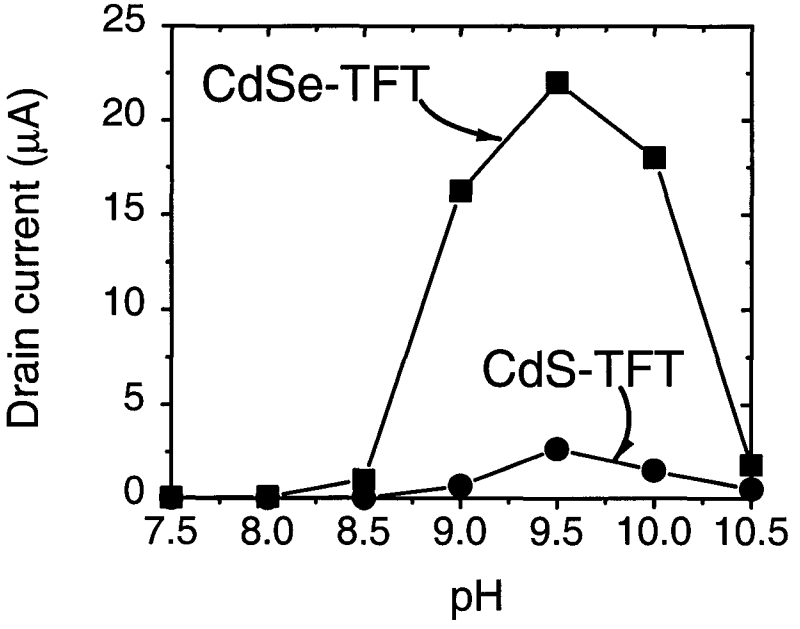


Figure 7-11 Drain current as a function of pH value in the dipping solution for the CdSe-TFT (Sample #115~122) and CdS-TFT (Sample #112~119).

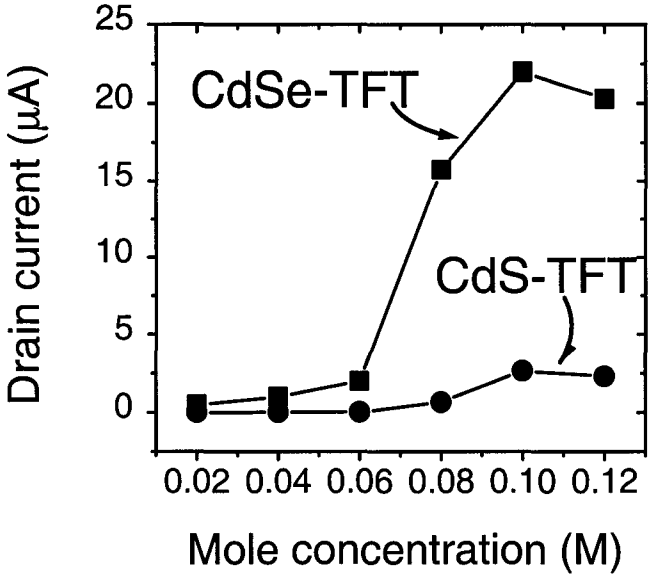
The dimensions of the channel for the TFTs fabricated on glass substrates are the same as that for TFTs on Si, 20 μm in length and 200 μm in width. A cross sectional view of the TFT fabricated is shown in Figure 7-10. After the fabrication, electrical characteristics of the CdSe-TFTs and CdS-TFTs were measured with the HP – 4145A semiconductor parameter analyzer. During the measurements, the drain voltage was swept from 0 to 20 V at various gate voltages with medium integration time.

The drain current in ON state at a gate voltage of 10 volts will be used as an indication of the quality of the TFTs in the following discussion. Figure 7-11 show the variation of drain current with the pH value in the CBD solution used during the deposition of CdS and CdSe. For CdSe-TFTs, the drain current increases as the pH value is increased from 7.5 to 8.5. A peak drain current value is reached at pH = 9.5. Beyond this peak value, the drain current decreases rapidly. Similar to the case of CdSe-TFTs, the pH value has shown a strong effect on the drain current on CdS-TFTs. As seen in Figure 7-11 for CdS-TFTs, the drain current increases as the pH value is increased from 7.5 to 9. A peak value is reached at pH = 9.5. As the pH value is increased further, the drain current decreases.

In Figure 7-12, results of drain current from CdSe TFTs prepared using deposition baths containing different concentrations of $CdCl_2$ are shown. The effects of $CdCl_2$ concentrations in the CBD solutions on the drain current were studied and the results are shown in Fig. 6-12. One can see that the drain current increases gradually as the mole concentration of $CdCl_2$ is increased from 0.02 M to 0.06 M. This is followed by a drastic increase as the $CdCl_2$ concentration is increased further. A peak value is reached at 0.10 M. Beyond this value, the drain current starts to decrease. Hence, the drain current of CdSe-TFT can be controlled by adjusting the mole concentration of the $CdCl_2$ in the deposition bath. The optimum concentration is about 0.10 M in the present experiments.

In Figure 7-12, results of drain current from CdS-TFTs from deposition baths having different concentrations of $CdCl_2$ are given. Similar to the case for CdSe, one can see that the drain current increases gradually as the mole concentration of $CdCl_2$ is

increased from 0.003 M to 0.004 M. A peak value is reached at 0.005 M. Beyond this value, the drain current starts to decrease. Hence, the drain current of CdS-TFT can be controlled by adjusting the mole concentration of the $CdCl_2$ in the deposition bath. The optimum concentration is about 0.05 M in the present experiments.



Mole concentration of $CdCl_2$
Unit: M ($CdCl_2$) for CdSe, M×20 ($CdCl_2$) for CdS

Figure 7-12 Drain current as a function of mole concentration of $CdCl_2$ for the CdSe-TFT (Sample #101~107) and CdS-TFT (Sample #92~98).

Figures 7-13 (a) and (b) depict drain current (I_D) – drain voltage (V_D) characteristics of a typical CdSe-TFT and a typical CdS-TFT prepared under the best dipping conditions and anodization conditions developed in this work. The ON-current of the best CdSe-TFT and CdS-TFT at a gate bias of 10 V and a source-drain voltage 10 V was 22 μA and 2.5 μA, whereas the OFF-current at 10 V source-drain voltage was 159 pA and 215 pA, respectively. The field effect mobility values obtained are 3.4 $cm^2V^{-1}sec^{-1}$ for the CdSe-TFT and 0.2 $cm^2V^{-1}sec^{-1}$ for the CdS-TFT.

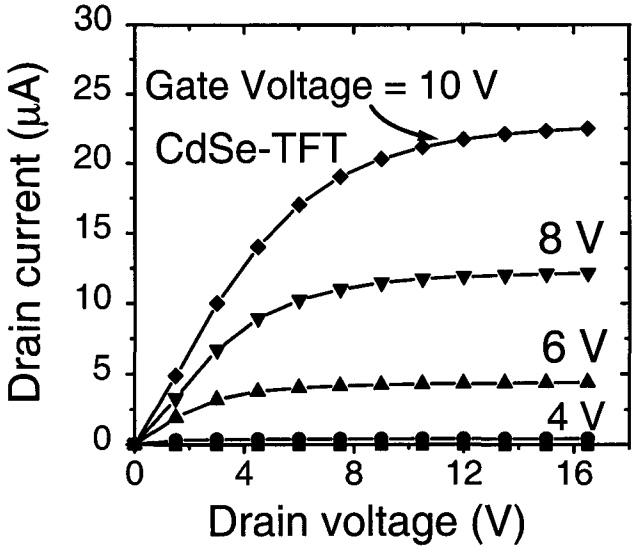


Figure 7-13(a) Output characteristics of the CdSe-TFT with anodic Al_2O_3 gate dielectric (Sample #145).

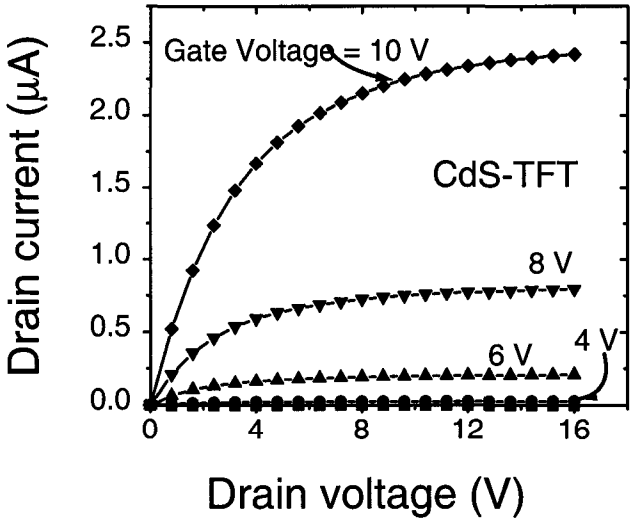


Figure 7-13(b) Output characteristics of the CdS-TFT with anodic Al_2O_3 gate dielectric (Sample #112).

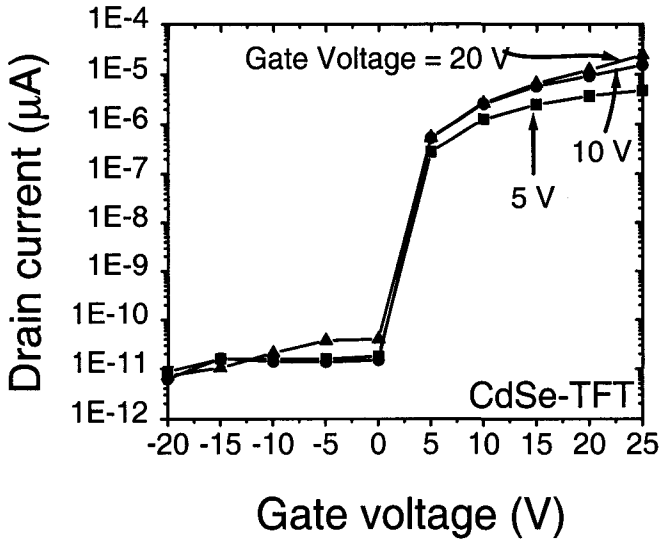


Figure 7-14(a) Transfer characteristics of the CdSe-TFT with anodic Al_2O_3 gate dielectric (Sample #145).

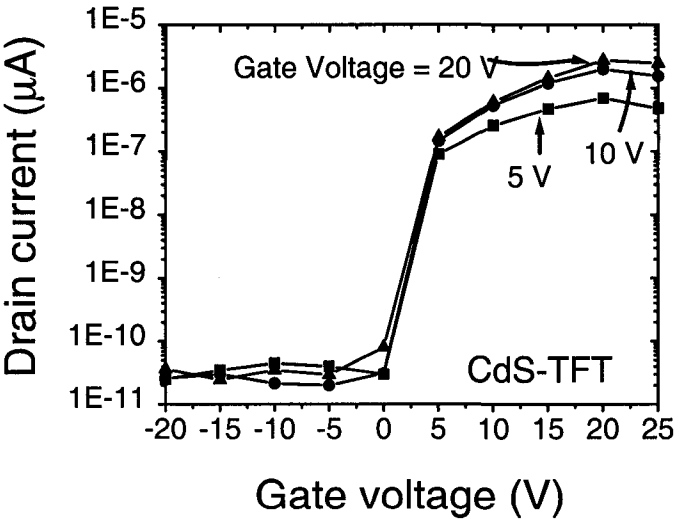


Figure 7-14(b) Transfer characteristics of the CdS-TFT with anodic Al_2O_3 gate dielectric (Sample #112).

Threshold voltage (V_T) of a TFT can be determined by the intersection of a plot of $(I_{DS})^{1/2}$ versus V_G with V_G axis and a value of 5.2 V was obtained for a typical CdSe-TFT, that for the CdS-TFT was 6.3 V. Transfer characteristics of the CdSe-TFT and CdS-TFT with the anodized Al_2O_3 gate insulator are shown in Figures 7-14 (a) and (b). As can be seen, the present TFTs have high ON-current values and large ON/OFF current ratios (I_{on}/I_{off}) making them suitable for TFT/LCDs applications. The ON/OFF current ratio I_{on}/I_{off} obtained from I_D versus V_G plots is about 10^5 for the CdSe-TFT and 10^4 for the CdS-TFT at a gate bias of $V_G = 10$ V.

From the above description, it is clear that the preliminary devices fabricated with a gate dielectric of Al_2O_3 are not as good as those on Si substrate with thermally grown oxide. This is because the quality of Al_2O_3 layer is affected by pH value of the dipping solution. The anodized Al_2O_3 layer can be dissolved at in a dipping solution with too low or too high pH values. This is also the reason why Al_2O_3 layers of the best quality are obtained in the anodizing electrolyte at pH ~ 7. However, quality of CdS films deposited from low pH CBD solutions is not sufficient for the active layer growth. Hence, it is necessary to develop an alternate oxide for the fabrication of TFTs by the CBD method. Ideally, this oxide should be capable of resisting electrolytes with different pH values.

7.2.4 Conclusions

It has been observed from the present results that the current density applied during the anodization of Al has rather strong effects on the resulted oxide. A current density of 1.1 mA/cm^2 has been found to give Al_2O_3 layers with low leakage currents. An increase in the current density to above 1.1 mA/cm^2 did not show a significant improvement in the film quality. It was also observed that the quality of the anodized films could be affected by the concentration of ethylene glycol in the electrolyte. The best results were obtained from electrolytes containing at least 65 % of ethylene glycol. Hence, the best conditions

for Al Anodization are: an anodizing current density in the range 1.1 – 1.5 mA/cm^2 and an ethylene glycol concentration of 65% or more (up to 70%).

It was also observed that the final applied voltage not only determined the thickness of the anodized films but also affected the quality. In addition, it was found that a post anodizing annealing treatment has resulted in further improvement in the film quality. The annealing treatment may have resulted in a loss of water molecules, which could have been incorporated into the oxide structure during anodic oxidation. After such an annealing, the breakdown electric field of the Al_2O_3 films has increased from 6 MV/cm to 8 MV/cm and the leakage current reduced to 10 nA/cm^2 at an electric field of 3 MV/cm.

The duration for the constant voltage mode of anodizing has strong effect on the leakage current and breakdown field. For the films anodized with a period of constant voltage mode for 10 minutes, the breakdown fields are too low and the leakage currents are too large for TFTs fabrication. However, the variations in breakdown electric field and leakage current are not significant for the films prepared with the period of constant voltage mode beyond 1 hour. Hence, the minimum time for constant voltage anodization was set at 1 hour in this work. The breakdown electric field of the metal-insulator-metal (MIM) capacitors made on the anodized Al_2O_3 is as high as 8 MV/cm, with a leakage current density of 10 nA/cm^2 at 3 MV/cm. Obviously, the breakdown voltage is a key indicator of the insulating quality of gate oxides. Using the anodized dielectric layers on glass substrates, preliminary TFTs with CdS and CdSe active films grown by the CBD method were fabricated and evaluated. The fabricated CdSe-TFTs exhibited a field effect mobility of 3.4 $cm^2/V\text{-}s$, threshold voltage of 5.2 V, subthreshold slope of 1.3 V/dec, and ON/OFF current ratios greater than 10^5. A field effect mobility of 0.2 $cm^2/V\text{-}s$, threshold voltage of 6.3 V, subthreshold slope of 1.5 V/dec, and ON/OFF current ratios exceeding 10^4 were observed for the CdS-TFTs.

7.3 Anodic Ta_2O_5 for gate insulators

Anodization involves the electrochemical oxidation of a metal anode in an electrolyte. Although this type of oxidation is limited to a few metals, aluminum and tantalum are among those that can be easily anodized. Tantalum oxide has received considerable attention for applications to coupling capacitors [7-17], memory storage capacitors [18,19], and gate dielectrics in the MOS devices [7-20,21]. The major advantage of tantalum oxide is its high dielectric constant of over 20.

7.3.1 Experiments for anodization

Thin films of tantalum with a thickness of about 0.6 μm were deposited onto the cleaned glass substrates by DC magnetron sputtering from a tantalum target. Tantalum oxide was created by anodizing the sputtered tantalum films on cleaned glass substrates. The anodizing electrolyte used is the same as that for Al and consists of tartaric acid, ethylene glycol, and water. The parameters used in Al anodization are applied for Ta anodizing process in this work. The purpose of adding ethylene glycol is to improve the tantalum anodization and to reduce the oxide blistering. The ammonium hydroxide was used to adjust the pH of the electrolyte. It is noted that the tantalum anodization is less sensitive to the pH value because tantalum is insoluble in aqueous solution over a wide range of pH values.

After Ta anodization, a layer of Al was evaporated onto these anodic oxides and photolithographically patterned for top electrodes to form the MIM capacitors. From preliminary capacitance measurements made on the tantalum oxide, the dielectric constant was estimated to be about 20. The ratio of voltage/thickness for the anodization was about 20 Å/V. The final applied voltages were varied from 50 to 250 V in the preliminary experiments but limited to the range of 90 – 110 V in subsequent work.

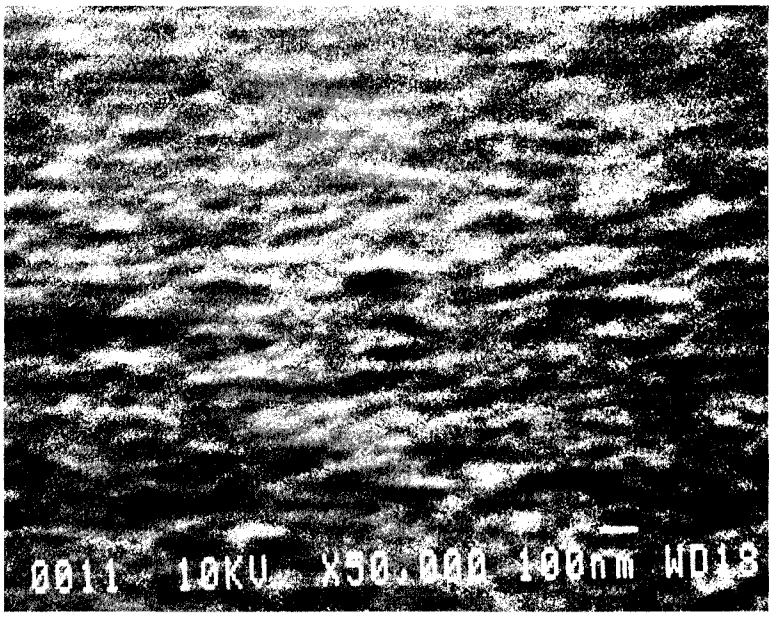


Figure 7-15 (a) A SEM photograph of the surface of an anodic Ta_2O_5.

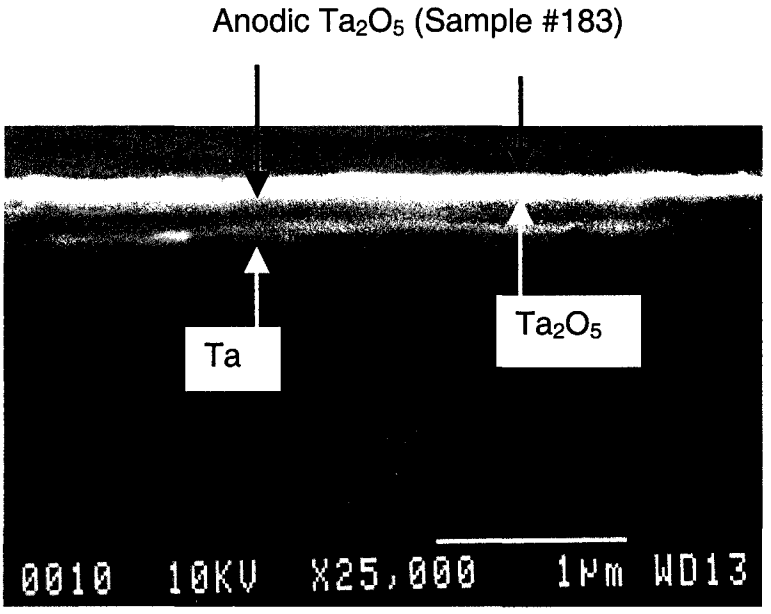


Figure 7-15 (b) SEM cross-section view of an anodic Ta_2O_5.

In the voltage range from 90 to 110 volts, thicknesses of the resulted films were from 0.18 to 0.22 μm. The constant current densities were controlled in a range 0.1 – 2.1 mA/cm^2 to control the anodization rate. Similar to Al, the anodization of Ta proved to be controllable and repeatable. Figure 7-15 (a) is a SEM photo of the surface of the tantalum oxide and (b) shows the fractured cross-section for this sample.

The anodization conditions for the best Al_2O_3 films were also applied here to obtain Ta_2O_5 films for comparison. Leakage currents have been measured for the tantalum oxide capacitors and the typical values were 0.3 $\mu A/cm^2$ at 10 V. This leakage current was much larger than the value of Al_2O_3 discussed in the previous section. It has been reported that tantalum oxide dielectric material exhibits ionic conduction, in which the leakage current is carried by tantalum ions that form in the interior of the oxide [7-22]. Hence, the anodized tantalum oxide films are more leaky compared to that of the anodic aluminum oxide.

7.3.2 Results and discussion

Figure 7-16 shows variation of leakage current with the applied voltage for an as-deposited Ta_2O_5 and an annealed Ta_2O_5 film. Results for an Al_2O_3 are also shown for comparison. As the voltage increases, the leakage currents of the Ta_2O_5 films increase rapidly beyond a critical electric field. As the voltage is increased further, the leakage current increases even more rapidly to cause the destructive breakdown. Generally, the critical electric field was defined as the breakdown field of the tantalum oxide capacitor. From the Figure 7-16, it is evident that for Ta_2O_5 the leakage current density is higher and breakdown electric field is lower than that for Al_2O_3. However, the resistant properties of Ta_2O_5 to CBD solution with high pH values will allow one to deposit high quality CdS or CdSe films to yield TFTs of large ON-currents. The breakdown field for the Ta_2O_5 was estimated to be about 0.6 MV/cm for a film with a thickness of about 0.2 μm. The breakdown field decreases drastically as the oxide thickness decreases. The results on these two oxides are summarized in Table 7-1.

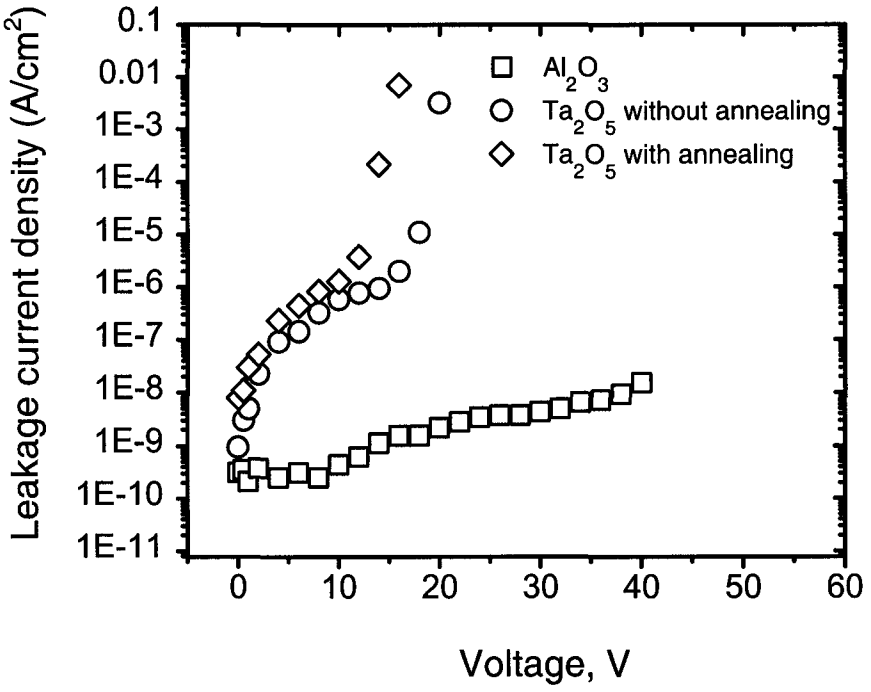


Figure 7-16 Leakage current density as a function of applied voltages for Al_2O_3 (Sample #145) and Ta_2O_5 (Sample #183) capacitors.

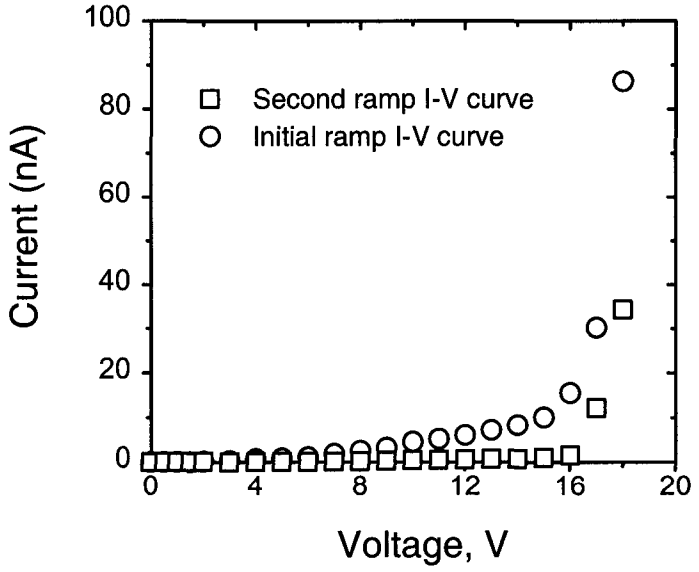


Figure 7-17 Two-step ramp I-V curves for 0.2 μm anodized tantalum oxide with Ta connected to positive potential (Sample #183).

Another parameter to determine the quality of oxide is the trapping of charges at interface with a metal. When a step ramping voltage is applied to a tantalum oxide capacitor, I-V curve corresponding to second voltage ramp may be shifted due to interface trapping [7-23]. From the shift in the I-V curve, the interface charge trapping can be estimated. Figure 7-17 shows I-V curves during a two-step ramping for the anodized tantalum oxide. In this experiment, a positive voltage is applied to the Ta electrode. The upper curve is the I-V cure during the initial ramping, corresponding to one of the curves (without annealing) in Figure 7-17. The lower one is for the I-V curve during the second–ramping with the trapping of interface charges. A large shift of the second I-V curve from the initial one indicates significant charge trapping at the metal-tantalum oxide interface. The second-ramp I-V curve shows a decrease in leakage current caused by electron trapping.

The TFT fabrication processes are the same as those used in the previous section employing Al_2O_3 gate oxide. Here, the optimum CBD conditions developed in Chapter 5 for thermally grown SiO_2 were applied for anodic Ta_2O_5. Figures 7-18 (a) and (b) depict drain current (I_D) – drain voltage (V_D) characteristics of a typical CdSe-TFT and a typical CdS-TFT with a Ta_2O_5 gate dielectric prepared under the best dipping conditions and anodization conditions developed in this work. The ON-current of the CdSe-TFT and CdS-TFT at a gate bias of 10 V and a source-drain voltage 10 V was 0.68 μA and 19.5 μA, whereas the OFF-current at 10 V source-drain voltage was 45 nA and 21 nA, respectively. The field effect mobility values obtained are 0.67 $cm^2V^{-1}sec^{-1}$ for the CdSe-TFT and 2 $cm^2V^{-1}sec^{-1}$ for the CdS-TFT. From the square law, field effect mobility of carriers may be estimated. Threshold voltage (V_T) was also determined from the intersection of a plot of $(I_{DS})^{1/2}$ versus V_G with V_G axis yielding a value of 8.16 V for the CdSe-TFT. The threshold voltage for the CdS-TFT with Ta_2O_5 gate oxide was 5.25 V.

It is noted that the ON-current for CdS-TFT is larger than that for CdSe-TFT. This was un-expected and is different from the previous TFT devices based on SiO_2 and Al_2O_3 dielectrics. The leakage currents for these TFTs with Ta_2O_5 gate dielectric are larger than

those with Al_2O_3. To reduce the leakage currents, the surface state density must be reduced. The anodizing conditions developed in this thesis are summarized in Table 7-1.

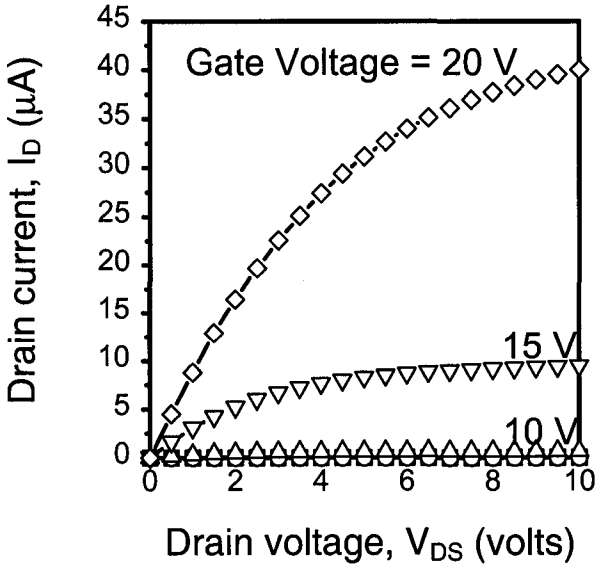


Figure 7-18 (a) Output characteristics of the CdSe-TFT with anodic Ta_2O_5 gate dielectric (Sample #183).

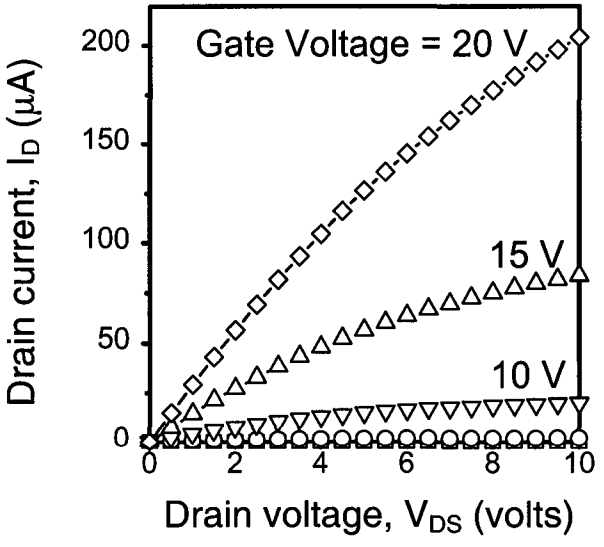


Figure 7-18 (b) Output characteristics of the CdS-TFT with anodic Ta_2O_5 gate dielectric (Sample #182).

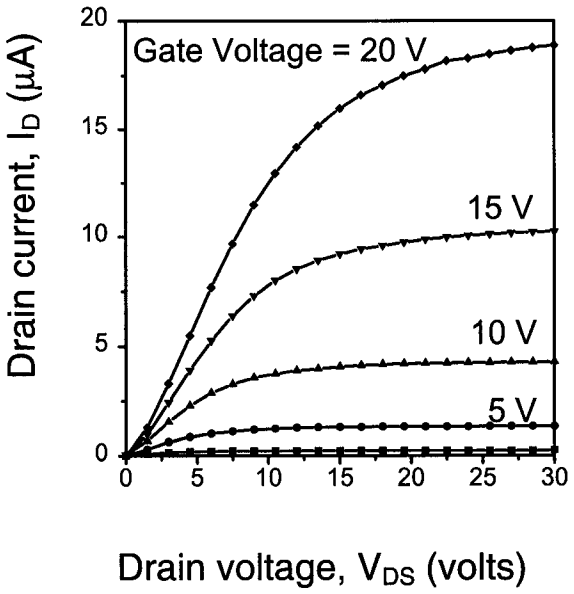


Figure 7-19 (a) Output characteristics of the CdSe-TFT with sputtered SiN_x gate dielectric (Sample #05170100).

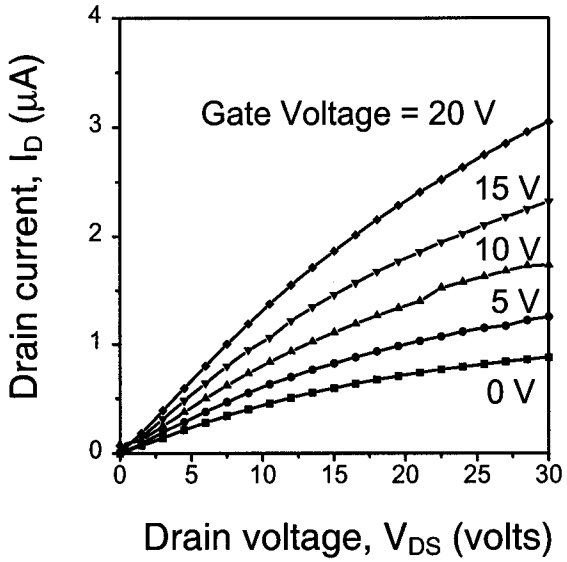


Figure 7-19 (b) Output characteristics of the CdS-TFT with sputtered SiN_x gate dielectric (Sample #05170200.

In order to study effects of gate oxide on the CBD deposited CdS and CdSe, some TFTs were fabricated on SiN_x. The SiN_x layer was prepared by reactive RF sputtering from a Si target. Figures 7-19 (a) and (b) depict drain current (I_D) – drain voltage (V_D) characteristics of a CdSe-TFT and a CdS-TFT with the SiN_x gate dielectric. It is noted that the ON-current of the CdSe-TFT and CdS-TFT at a gate bias of 10 V and a source-drain voltage 10 V is 3.75 μA and 0.85 μA, whereas the OFF-current at 10 V source-drain voltage is 0.22 μA and 0.45 μA, respectively. The results show that these TFTs behave as depletion-type devices with small ON-current. This is different from that fabricated on anodized Al_2O_3 and Ta_2O_5. In addition, the leakage current through the gate oxide is larger. This could be due to the presence of weak spots such as voids, metallic particles in the sputtered nitride. Alternately, it could also be due to thinner oxide regions in the sputtered nitride which is formed by physical impingement of oxygen atoms. Hence, further improvement is needed on the sputtered SiN_x gate dielectric in order to obtain a suitable surface for the following chemical bath deposition process and to obtain a good quality TFTs.

One way to improve the film quality is to anodize the sputtered oxide. As a high electric field is applied, Anodization may take place to enhance the weak spots. An electric field exceeding a critical value will cause an ionic current to flow through the weak spots, resulting in a self-sealing anodic oxidation. The self-sealing anodic oxidation at the weak spots causes the "filling in" of the voids, the reoxidizing of the metallic particles, and the thickening of the thinner oxide regions, leading to densification of sputtered/anodized oxide. During the densification of the oxide, the Ta or Al underlayer serves as a seed layer for sealing the weak spots. This two-step oxidation may improve the performance of the TFTs based on sputtered-SiN_x gate dielectrics.

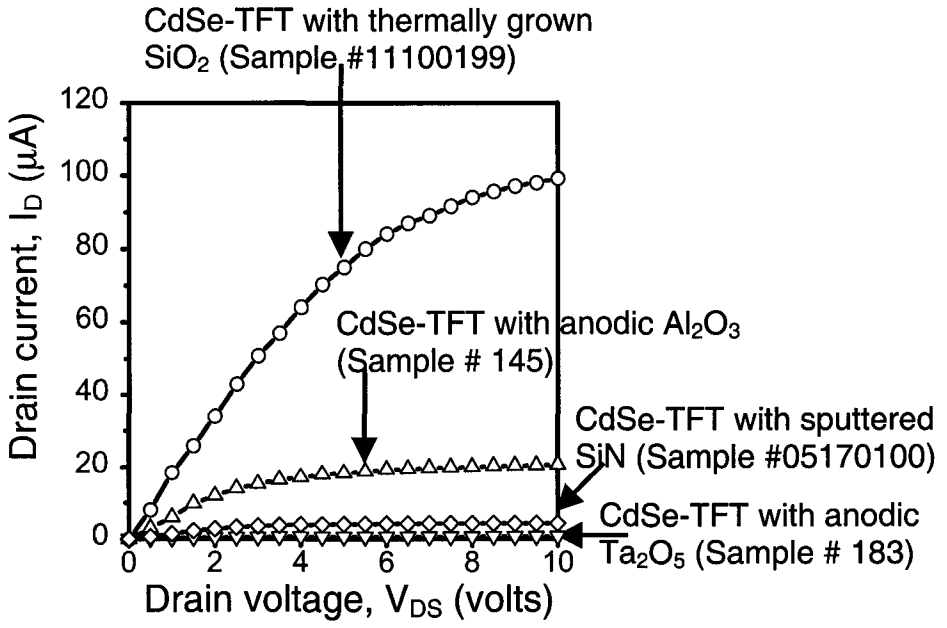


Figure 7-20 (a) Comparison of output characteristics of the CdSe-TFT with different gate dielectrics at V_G = 10 V.

In this work, we have developed three different gate dielectrics in addition to the thermally grown SiO_2 for CBD process to fabricate the TFT devices on glass substrates. A comparison of results with TFTs having a thermally grown SiO_2 (presented in Chapter 6) is shown in Figure 7-20. It is seen in Figure 7-20 (a) that the device with the largest ON current is the CdSe-TFT with thermally grown SiO_2 gate dielectric. This is because the thermally grown SiO_2 shows excellent resistance to CBD baths with large range of pH values, allowing the optimization of the quality of the deposited CdSe films. Since the CBD electrolyte can erode the anodic Al_2O_3, it is not possible to optimize the quality of the CdSe films (by adjusting pH values). Although the ON currents of the present TFTs with anodic Ta_2O_5 and sputtered SiN_x gate dielectrics are not as high as that for the thermally oxidized one, further improvement is possible. This may be achieved by improving and refining the dipping solutions and conditions.

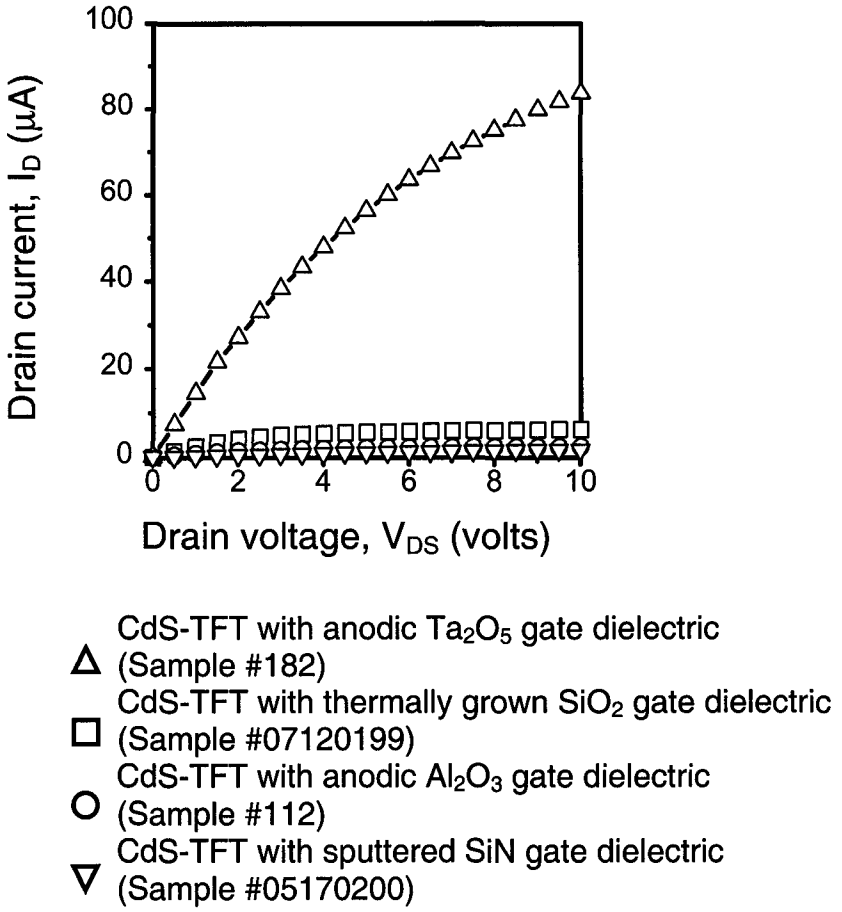


Figure 7-20 (b) Comparison of output characteristics of the CdS-TFT with different gate dielectrics at V_G = 10 V.

Results for CdS-TFTs made on different gate dielectrics are shown in Figure 7-20 (b). It is seen that the TFT on the anodic Ta_2O_5 gate dielectric has the largest ON current due to the resistant in a dipping solutions with a higher pH value. The ON currents are relatively small for the one on the anodic Al_2O_3 gate dielectric, due to the limit in pH value of the dipping solution. The performance of TFT with the sputtered SiN_x may be improved by adjusting the dipping solution, which was not done in the present work.

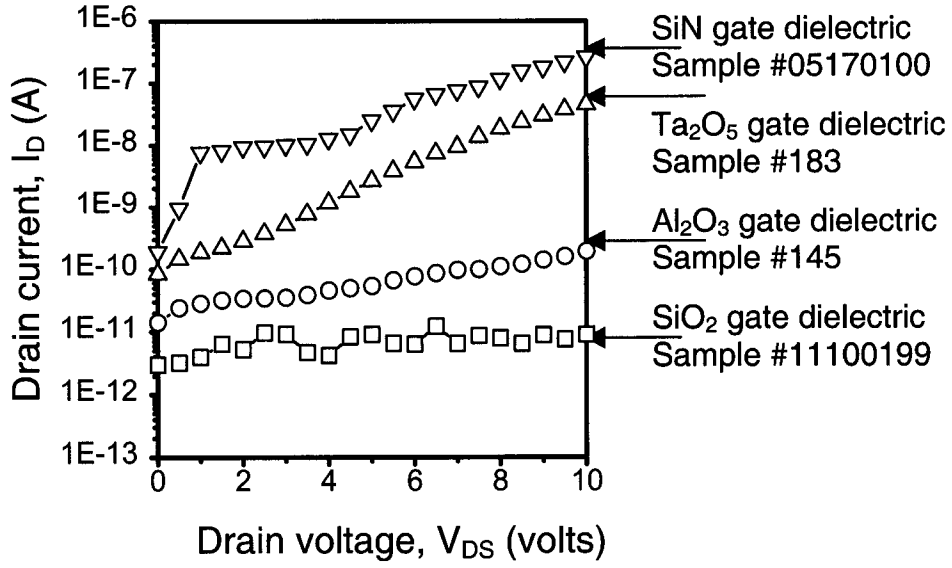


Figure 7-21 (a) OFF-current of the CdSe-TFTs with different gate dielectrics at $V_g = 0$ V.

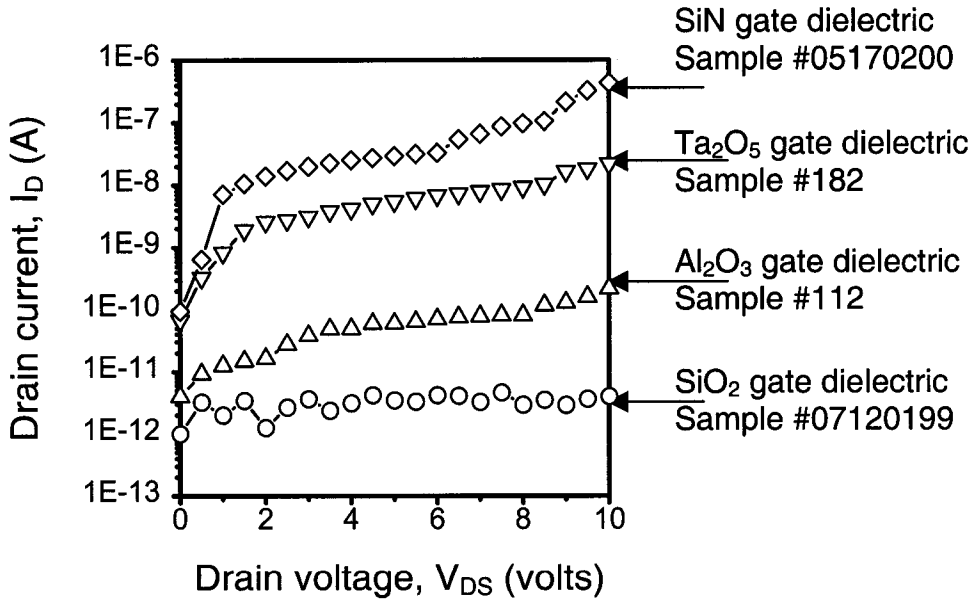


Figure 7-21 (b) OFF-current of the CdS-TFTs with different gate dielectrics at $V_g = 0$ V.

The OFF currents for TFTs on different gate dielectrics were also measured and the results are shown in Figure 7-21. It should be noted that both the CdSe-TFT and CdS-TFT on the thermally grown SiO_2 gate dielectric have the lowest OFF currents. This is believed to be due to the minimum interface surface state density in these devices. For TFTs on other gate dielectrics, the leakage currents are larger. In order to obtain TFTs with performance similar to the one on thermally grown SiO_2 gate dielectric, further optimization is needed. In addition, the CBD method has to be modified for the different gate dielectrics. The CBD conditions with different gate oxides used in this thesis are summarized in Tables 7-2 to 7-4 and the characteristics and parameters extracted from these TFTs are listed in Tables 7-5 – 7-7. The comparison with results of other researchers is also listed in the Appendix.

7.4 Conclusions

From the present results, it is clear that TFTs can be fabricated on the glass substrates with the anodic oxides or sputtered SiN_x as gate dielectrics and with CBD deposited CdSe or CdS as active layers. However, values of the ON/OFF current ratio are still too small (~10^4) compared to that with thermally grown SiO_2 (~10^6).

High quality Al_2O_3 layers were formed by anodic oxidation in an ethylene glycol solution mixed with the tartaric acid with pH ~7 at constant current and constant voltage operation. The Al_2O_3 layers are effective protective layers against formation of hillocks in aluminum. Combining the good dielectric characteristics of the anodized Al_2O_3 layer and the low electrical resistivity of aluminum, the anodized Al_2O_3 would be a good candidate for high resolution and high reliability TFT/LCDs.

However, the subsequent CBD process needed to deposit the active layer requires a gate dielectric, which is highly resistant to electrolytes over a wide range of pH. Unfortunately, the anodic Al_2O_3 layer cannot meet this requirement. Hence, the anodic

tantalum oxide could be a good alternate candidate for the CBD deposition in a CBD solution with a high pH value. For Ta_2O_5, the leakage current is large and the breakdown field is low. This will limit their application alone as gate dielectric in TFTs. It appears that a combination in the form $Al/Al_2O_3/Ta_2O_5$ may allow one to enjoy the advantages of the Ta_2O_5 dielectric and the low resistivity of Al metal. In the above structure, the intermediate Al_2O_3 layer will be introduced to serve as a buffer layer to relax the stresses, which otherwise will result the hillock generation between aluminum and anodic Ta_2O_5.

Tables

Table 7-1 the best solutions, the anodizing conditions and the results		
Material	Al_2O_3	Ta_2O_5
Electrolyte		
Ethylene glycol:	500 ml	500 ml
DI water:	300 ml	300 ml
Tartaric acid:	10 g	10 g
pH value:	~ 7	~ 7
Temperature:	22 ± 2°C	22 ± 2°C
Anodization conditions		
Current density:	1.1 mA/cm^2	1.1 mA/cm^2
Final voltage:	100 V	100 V
Time (CC-mode):	~2 min	~2 min
Time (CV-mode):	60 min	60 min
Annealing:	250 °C for 2 h	250 °C for 2 h
Results		
Capacitance:	48 nF/cm^2	56 nF/cm^2
Thickness:	~ 0.15 μm	~ 0.2 μm
Leakage current density:	15 nA/cm^2 @ 40 V	0.3 μA/cm^2 @ 10 V
Breakdown electric field:	6 MV/cm	1 MV/cm

Table 7-2 (a) the best dipping condition for CdSe-TFTs with Al_2O_3 gate dielectric	
Relative ion concentration:	0.1 M Na_2SSeO_3, 0.1 M $CdCl_2$, and 6.5 M NH_4OH
pH value:	9 ~ 10
Temperature:	80 ± 2°C
Mixing time before dipping:	2 minutes
Stirring during CBD:	Yes
Dipping time:	5 minutes
No. of dipping:	8
Cleaning the beaker after dipping:	yes
Ultrasonic cleaning of sample after dipping:	1 minute
Ultrasonic cleaning solution of sample:	DI water

Table 7-2 (b) the best dipping conditions for CdS-TFTs with Al_2O_3 gate dielectric	
Relative ion concentration:	
0.005 M $CdCl_2$, 0.5 M of thiourea, 0.5 M NH_4Cl, 0.8 M NH_4OH	
pH value:	9 ~ 10
Temperature:	80 ± 2°C
Mixing time before dipping:	3 minutes
Stirring during CBD:	Yes
Dipping time:	3 minutes
No. of dipping:	4
Cleaning the beaker after dipping:	yes
Ultrasonic cleaning of sample after dipping:	1 minute
Ultrasonic cleaning solution of sample:	DI water

Table 7-3 (a) the best dipping conditions for CdSe-TFTs with Ta_2O_5 gate dielectric	
Relative ion concentration:	0.1 M Na_2SSeO_3, 0.1 M $CdCl_2$, and 6.5 M NH_4OH
pH value:	~12
Temperature:	80 ± 2°C
Mixing time before dipping:	2 minutes
Stirring during CBD:	Yes
Dipping time:	5 minutes
No. of dipping:	8
Cleaning the beaker after dipping:	yes
Ultrasonic cleaning of sample after dipping:	1 minute
Ultrasonic cleaning solution of the sample:	DI water

Table 7-3 (b) the best dipping conditions for CdS-TFTs with Ta_2O_5 gate dielectric	
Relative ion concentration:	
0.005 M $CdCl_2$, 0.05 M of thiourea, 0.05 M NH_4Cl, 0.8 M NH_4OH	
pH value:	~12
Temperature:	80 ± 2°C
Mixing time before dipping:	3 minutes
Stirring during CBD:	Yes
Dipping time:	3 minutes
No. of dipping:	4
Cleaning the beaker after dipping:	yes
Ultrasonic cleaning of sample after dipping:	1 minute
Ultrasonic cleaning solution of the sample:	DI water

Table 7-4 (a) the best dipping conditions for CdSe-TFTs with SiN gate dielectric	
Relative ion concentration:	0.1 M Na_2SSeO_3, 0.1 M $CdCl_2$, and 6.5 M NH_4OH
pH value:	~12
Temperature:	80 ± 2°C
Mixing time before dipping:	2 minutes
Stirring during CBD:	Yes
Dipping time:	5 minutes
No. of dipping:	8
Cleaning the beaker after dipping:	yes
Ultrasonic cleaning of sample after dipping:	1 minute
Ultrasonic cleaning solution of the sample:	DI water

Table 7-4 (b) the best dipping conditions for CdS-TFTs with SiN gate dielectric	
Relative ion concentration:	
0.005 M $CdCl_2$, 0.05 M of thiourea, 0.05 M NH_4Cl, 0.8 M NH_4OH	
pH value:	~12
Temperature:	80 ± 2°C
Mixing time before dipping:	3 minutes
Stirring during CBD:	Yes
Dipping time:	3 minutes
No. of dipping:	4
Cleaning the beaker after dipping:	yes

Ultrasonic cleaning of sample after dipping: 1 minute
Ultrasonic cleaning solution of the sample: DI water

Table 7-5 (a)			
Parameters for CdSe-TFTs with anodic Al_2O_3			Method or Notes
$T_{thickness\ of\ CdSe}$	(nm)	200	CBD (80°C)
$T_{thickness\ of\ gate\ oxide}$	(nm)	200	Anodization (25°C)
$\varepsilon_{dielectric\ constant}$	(Al_2O_3)	~9	General
$\varepsilon_{dielectric\ constant}$	(CdSe)	~10.2	General
$L_{channel\ length}$	(μm)	20	Measured
$W_{channel\ width}$	(μm)	200	Measured
$C_{gate\ capacitance}$	(nF/cm^2)	39.82	Measured
V_{gate}	(V)	10	Applied
V_{drain}	(V)	10	Applied
$V_{threshold}$	(V)	~5.2	Calculated
$n_{o,\ initial\ trap\ density}$	(cm^{-2}) x 10^{11}	~14	Calculated from V_t
$N_{t,\ interface\ state\ density}$	(cm^{-2}) x 10^{12}	~7.8	Calculated from S
$N_{carrier\ concentration}$	(cm^{-2}) x 10^{11}	~1.1	Calculated
$n_{max.}$	(cm^{-2}) x 10^{12}	~6.6	Calculated
I_{ON}	(μA)	~22	Measured
I_{OFF}	(pA)	~160	Measured
$\mu_{effective\ mobility}$	(cm^2/V-s)	~3.4	Calculated
$g_{transconductance}$	($\mu\Omega^{-1}$)	~5.8	Calculated
$\tau_{response\ time}$	(μs)	0.24	Calculated
$S_{subthreshold\ slope}$	(V/decade)	~1.3	Calculated
Performance Uniformity		± 43 %	(Variation in I_{ON})
Reproducibility		± 41 %	(Variation in I_{ON})
Yield		~ 20%	

Table 7-5 (b)			
Parameters for CdS-TFTs with anodic Al_2O_3			Method or Notes
$T_{thickness\ of\ CdS}$	(nm)	200	CBD (80°C)
$T_{thickness\ of\ gate\ oxide}$	(nm)	200	Anodization (25°C)
$\varepsilon_{dielectric\ constant}$	(Al_2O_3)	~9	General
$\varepsilon_{dielectric\ constant}$	(CdS)	~10.6	General
$L_{channel\ length}$	(μm)	20	Measured
$W_{channel\ width}$	(μm)	200	Measured
$C_{gate\ capacitance}$	(nF/cm^2)	39.82	Measured
V_{gate}	(V)	10	Applied
V_{drain}	(V)	10	Applied
$V_{threshold}$	(V)	~6.3	Calculated
$n_{o,\ initial\ trap\ density}$	(cm^{-2}) x 10^{11}	~17	Calculated from V_t
$N_{t,\ interface\ state\ density}$	(cm^{-2}) x 10^{12}	~8.8	Calculated from S
$N_{carrier\ concentration}$	(cm^{-2}) x 10^{11}	~0.67	Calculated
$n_{max.}$	(cm^{-2}) x 10^{12}	~6.6	Calculated
I_{ON}	(μA)	~2.5	Measured
I_{OFF}	(pA)	~220	Measured
$\mu_{effective\ mobility}$	(cm^2/V-s)	~0.2	Calculated
$g_{transconductance}$	($\mu\Omega^{-1}$)	~0.8	Calculated
$\tau_{response\ time}$	(μs)	1.35	Calculated
$S_{subthreshold\ slope}$	(V/decade)	~1.5	Calculated
Performance Uniformity		± 49 %	(Variation in I_{ON})
Reproducibility		± 46 %	(Variation in I_{ON})
Yield		~ 25%	

Table 7-6 (a)			
Parameters for CdSe-TFTs with anodic Ta_2O_5			Method or Notes
$T_{thickness\ of\ CdSe}$	(nm)	200	CBD (80°C)
$T_{thickness\ of\ gate\ oxide}$	(nm)	200	Anodization (25°C)
$\varepsilon_{dielectric\ constant}$	(Ta_2O_5)	~20	General
$\varepsilon_{dielectric\ constant}$	(CdSe)	~10.2	General
$L_{channel\ length}$	(μm)	20	Measured
$W_{channel\ width}$	(μm)	200	Measured
$C_{gate\ capacitance}$	(nF/cm^2)	88.5	Measured
V_{gate}	(V)	10	Applied
V_{drain}	(V)	10	Applied
$V_{threshold}$	(V)	~8.6	Calculated
$n_{o,\ initial\ trap\ density}$	(cm^{-2}) x 10^{11}	~23	Calculated from V_t
$N_{t,\ interface\ state\ density}$	(cm^{-2}) x 10^{12}	~67.1	Calculated from S
$N_{carrier\ concentration}$	(cm^{-2}) x 10^{11}	~2.1	Calculated
$n_{max.}$	(cm^{-2}) x 10^{12}	~13.8	Calculated
I_{ON}	(μA)	~0.68	Measured
I_{OFF}	(nA)	~45	Measured
$\mu_{effective\ mobility}$	(cm^2/V-s)	~0.67	Calculated
$g_{transconductance}$	($\mu\Omega^{-1}$)	~0.38	Calculated
$\tau_{response\ time}$	(μs)	4.26	Calculated
$S_{subthreshold\ slope}$	(V/decade)	~3.3	Calculated
Performance Uniformity		± 18 %	(Variation in I_{ON})
Reproducibility		± 4.5 %	(Variation in I_{ON})
Yield		~ 94%	

Table 7-6 (b)			
Parameters for CdS-TFTs with anodic Ta_2O_5			Method or Notes
$T_{thickness\ of\ CdSe}$	(nm)	200	CBD (80°C)
$T_{thickness\ of\ gate\ oxide}$	(nm)	200	Anodization (25°C)
$\varepsilon_{dielectric\ constant}$	(Ta_2O_5)	~20	General
$\varepsilon_{dielectric\ constant}$	(CdS)	~10.6	General
$L_{channel\ length}$	(μm)	20	Measured
$W_{channel\ width}$	(μm)	200	Measured
$C_{gate\ capacitance}$	(nF/cm^2)	88.5	Measured
V_{gate}	(V)	10	Applied
V_{drain}	(V)	10	Applied
$V_{threshold}$	(V)	~5.25	Calculated
$n_{o,\ initial\ trap\ density}$	(cm^{-2}) x 10^{11}	~14	Calculated from V_t
$N_{t,\ interface\ state\ density}$	(cm^{-2}) x 10^{12}	~47.1	Calculated from S
$N_{carrier\ concentration}$	(cm^{-2}) x 10^{11}	~5.1	Calculated
$n_{max.}$	(cm^{-2}) x 10^{12}	~13.8	Calculated
I_{ON}	(μA)	~19.5	Measured
I_{OFF}	(nA)	~21	Measured
$\mu_{effective\ mobility}$	(cm^2/V-s)	~2	Calculated
$g_{transconductance}$	($\mu\Omega^{-1}$)	~4	Calculated
$\tau_{response\ time}$	(μs)	4.26	Calculated
$S_{subthreshold\ slope}$	(V/decade)	~2.3	Calculated
Performance Uniformity		± 15 %	(Variation in I_{ON})
Reproducibility		± 2.5 %	(Variation in I_{ON})
Yield		~ 100%	

Table 7-7 (a)			
Parameters for CdSe-TFTs with sputtered SiN			Method or Notes
$T_{\text{thickness of CdSe}}$	(nm)	200	CBD (80°C)
$T_{\text{thickness of gate oxide}}$	(nm)	100	Anodization (25°C)
ε dielectric constant	(SiN)	~7	General
ε dielectric constant	(CdSe)	~10.2	General
$L_{\text{channel length}}$	(μm)	20	Measured
$W_{\text{channel width}}$	(μm)	200	Measured
$C_{\text{gate capacitance}}$	(nF/cm^2)	59	Measured
V_{gate}	(V)	10	Applied
V_{drain}	(V)	10	Applied
$V_{\text{threshold}}$	(V)	~7.4	Depletion type-TFT
$n_{o,\text{ initial carrier density}}$	(cm^{-2}) x 10^{11}	~17.2	Calculated from V_t
$N_{t,\text{ interface state density}}$	(cm^{-2}) x 10^{12}	~88.9	Calculated from S
$N_{\text{carrier concentration}}$	(cm^{-2}) x 10^{11}	~2.1	Calculated
$n_{\text{max.}}$	(cm^{-2}) x 10^{12}	~9.4	Calculated
I_{ON}	(μA)	~3.5	Measured
I_{OFF}	(nA)	~220	Measured
μ effective mobility	($cm^2/V\text{-}s$)	~	Calculated
g transconductance	($\mu\Omega^{-1}$)	~	Calculated
τ response time	(μs)	~	Calculated
$S_{\text{subthreshold slope}}$	(V/decade)	~6.9	Calculated
Performance Uniformity		± 67 %	(Variation in I_{ON})
Reproducibility		± 45 %	(Variation in I_{ON})
Yield		~ 54%	

Table 7-7 (b)			
Parameters for CdS-TFTs with sputtered SiN			Method or Notes
$T_{thickness\ of\ CdSe}$	(nm)	200	CBD (80°C)
$T_{thickness\ of\ gate\ oxide}$	(nm)	100	Anodization (25°C)
$\varepsilon_{dielectric\ constant}$	(SiN)	~7	General
$\varepsilon_{dielectric\ constant}$	(CdS)	~10.6	General
$L_{channel\ length}$	(μm)	20	Measured
$W_{channel\ width}$	(μm)	200	Measured
$C_{gate\ capacitance}$	(nF/cm^2)	59	Measured
V_{gate}	(V)	10	Applied
V_{drain}	(V)	10	Applied
$V_{threshold}$	(V)	~8.3	Depletion type-TFT
$n_{o,\ initial\ carrier\ density}$	(cm^{-2}) x 10^{11}	~19.2	Calculated from V_t
$N_{t,\ interface\ state\ density}$	(cm^{-2}) x 10^{12}	~101.8	Calculated from S
$N_{carrier\ concentration}$	(cm^{-2}) x 10^{11}	~2.9	Calculated
$n_{max.}$	(cm^{-2}) x 10^{12}	~9.4	Calculated
I_{ON}	(μA)	~0.85	Measured
I_{OFF}	(nA)	~0.45	Measured
$\mu_{effective\ mobility}$	($cm^2/V\text{-}s$)	~	Calculated
$g_{transconductance}$	($\mu\Omega^{-1}$)	~	Calculated
$\tau_{response\ time}$	(μs)	~	Calculated
$S_{subthreshold\ slope}$	(V/decade)	~ 7.8	Calculated
Performance Uniformity		± 57 %	(Variation in I_{ON})
Reproducibility		± 56 %	(Variation in I_{ON})
Yield		~ 62 %	

Table 7-8 Performance of CdSe-TFTs with various gate dielectrics				
Gate dielectrics	SiO_2 (thermal)	Al_2O_3	Ta_2O_5	SiN
$V_{Threshold\ voltage\ (V)}$	2.5	5.2	8.6	7.4
$S_{Subthreshold\ (V/dec)}$	0.8	1.3	3.3	6.9
I_{on}/I_{off} (@ V_G = 10 V)	10^7	10^5	15	15
$I_{ON\ (\mu A,\ @\ V_G = 10\ V)}$	100	22	0.68	3.5
$I_{OFF\ (pA)}$	9	160	45 nA	220 nA

Table 7-9 Performance of CdS-TFTs with various gate dielectrics				
Gate dielectrics	SiO_2 (thermal)	Al_2O_3	Ta_2O_5	SiN
$V_{Threshold\ voltage\ (V)}$	2.8	6.3	5.25	8.3
$S_{Subthreshold\ (V/dec)}$	1.2	1.5	2.3	14
I_{on}/I_{off} (@ V_G = 10 V)	10^6	10^4	10^3	1.8
$I_{ON\ (\mu A,\ @\ V_G = 10\ V)}$	5	2.5	19.5	0.84
$I_{OFF\ (pA)}$	4	220	21 nA	450 nA

Appendix:

	CdSe	*CdS*	*a-Si*	*Poly-Si*
Substrate material	glass (Corning 7059)	glass	glass (Na-free)	quartz or glass (Na-free)
Channel properties				
Carrier mobility	250-450[1] (20~50)[4] (80~160)[6] 250[7] 484[8]	250-300[2] 140[5]	0.3-1.0[3]	25-100[1]
Carrier density[9] *(cm^{-3})*	10^{11}~10^{12} 10^{14}	10^{12}	10^{11}~10^{12}	10^{11}~10^{12}
Conduction type	n-channel enhancement[10]	n-channel enhancement	n-channel enhancement	n or p-channel enhancement
Channel thickness *(nm)*	10~40 [1]	< 100	300~500 [11]	50~100, 750 [9]
Channel length *(μm)*	15~50 [5]	5~50	5~40 [2]	5~25 [9]
Channel width *(μm)*	25~300 [5]	200~	100~600 [2]	~10 [9]
Deposition method	evaporation	evaporation	glow-discharge	LPCVD
Temperature[3] *(^oC)*	room-temp	175~300	350	550~650
Patterning[3]	low-resolution lithography	low-resolution lithography	high-resolution lithography	high-resolution lithography
Metal materials				
Drain-source electrode	In and Au		n+ a-Si:H[11]	n+-poly Si
Metal contact	Al Au	Au Al In	Al	Al
Fabrication	evaporation	evaporation	glow discharge	ion-implanted

Gate oxide				
Gate oxide thickness *(nm)*	60~400	100~400	300~500	30~100
Materials	(SiO_2, Al_2O_3) [6] Ta_2O_5	SiO_2	SiO_2 SiN_x Si_3N_4	SiO_2 SiN_x
Deposition method	thermal evap. (E-beam) Sputtering Anodize	Thermal evap.	LPCVD PECVD	LPCVD PECVD laser annealing
TFT OFF current *(A)*	(10^{-12}~10^{-14}) [3] (5.8×10^{-10}) [6]		(10^{-12}~10^{-15}) [3]	(10^{-11}) [3]
TFT OFF current *(A/μm)*	(2×10^{-11}) [5]		(10^{-11}) [2]	(10^{-9})[12]
TFT ON current[13] *(A/)*	(>10^{-5}) [3] (4.8×10^{-6}) [6]		(10^{-8}) [3]	(10^{-6}~10^{-7}) [3]
Response time[14] *(sec)*	4×10^{-8}	3×10^{-8}	10^{-7}	3×10^{-9}
Break down *(V)*	200~500			

Comparison with results of other researchers

Materials	Deposition Method	Deposition Temperature	I_{ON} (μA)	I_{OFF} (pA)	μ_{eff} $cm^2/V\text{-}s$	L (μm)	W (μm)	Thickness (nm)
Poly-Si	LPCVD	500~650	5~200	2~100	10~100	2~25	10~100	50~100
a-Si	CVD	350	1~10	1~10	0.2~1	2~40	100~500	300~500
CdSe	Evaporation	25~400	20~300	1~100	10~450	15~50	25~300	10~100
Results from the present work:								
CdSe	CBD	40~100	20~100	2~100	2~15	20~80	200	100~200
CdS	CBD	40~100	1~40	2~50	0.2~2	20~80	200	100~200

Performance:
$V_G = 10$ V, $V_D = 10$ V for I_{ON}
$V_G = 0$ V, $V_D = 10$ V for I_{OFF}.

General requirements for TFT:
$I_{ON} > 1\mu A$, $I_{OFF} < 10$ pA, $V_T < 5V$
Deposition temperature < 400 °C

References

1. P. M. Fryer, L. Jenkins, R. John, Y. Kuo, A. Lien, R. Nywening, B. Owens, L. Palmateer, M. E. Rothwell, J. Souk, J. Wilson, S. Wright, J. Batey, and R. Wisnieff, "04 SID International Display Research Conference Digest," p. 146-149 (1994).

2. U. Smith, N. Kristense, F. Ericson, and J-A. Schweits, "Local stress relaxation phenomena in thin aluminum films," J. Vac. Sci. Technol. A, Vol. 9, p. 2527 (1991).

3. E. Iwamura, T. Ohnishi, K. Yoshikawa, and K. Itayama, "In situ scanning electron microscopic observation of hillock and whisker grown on Al-Ta alloy films for interconnections of thin film transistor liquid crystal display," J. Vac. Sci. Technol. A, Vol. 12, p. 2922 (1994).

4. Toshihisa Tsukada, "Development of aluminum gate thin-film transistors based on aluminum oxide insulators," Mat. Res. Soc. Symp. Proc. Vol. 284, p. 371 (1993).

5. C. W. Kim, J. H. Lee, H. R. Nam, S. Y. Kim, C. O. Jeong, J. H. Choi, M. P. Hong, H. S. Byun, H. G. Yang, and J. H. Souk, "Low cost, high display quality TFT-LCD process," Proceedings of Euro Display'96, p. 591 (1996).

6. T. Arai, H. Iiyori, Y. Hirmoasu, M. Atsumi, S. Ioku, K. Furuta, "Aluminum-based gate structure for active-matrix liquid crystal displays," IBM Journal Research Development, Vol. 42, No. 3/4, p. 491 (1998).

7. C.W. Liang, David Su, Dept. of Electronics Engineering, National Chiao-Tung University, Taiwan, "Characterization of anodic aluminum oxide film and its application to amorphous silicon thin film transistors," Materials Chemistry and Physics 43, p. 166-172, 1996.

8. C.F Yeh, J.Y. Cheng, J.H. Lu, Dept. of Electronics Engineering, National Chiao-Tung University, Taiwan, "The characterization of Al_2O_3 prepared by anodic oxidation," Jpan. J. Appl. Phys. Vol. 32, p. 2803-2808, 1993.

9. Toshiaki Arai, Satoshi Tsuji, IBM Yamato Laboratory, Japan, "Nanostructure and electrical properties of anodized Al gate insulators for thin-film transistors," Mat. Res. Soc. Symp. Proc. Vol. 424, p. 37-42, 1997.

10. T. Arai, H. Iiyori, Y. Hirmoasu, M. Atsumi, S. Ioku, K. Furuta, "Aluminum-based gate structure for active-matrix liquid crystal displays," IBM Journal Research Development, VOL. 42, NO. 3/4, p. 491-497, 1998.

11. Kiyoshi Ozawa, Teiji Majima, Fujitsu limited, Japan, "Anodization behavior of Al, and physical and electrical characterization of its oxide films," J. Appl. Phys. 80 (10), p.5828-5836, 1996.

12. Kiyoshi Ozawa, Teiji Majima, Fujitsu limited, Japan, "Anodic oxide films as a gate dielectric for a thin film transistor," J. Electrochemical Society, vol. 141, No. 5, p. 1325-1333, 1996.

13. Toshihisa Tsukada, Central Research Laboratory, Hitachi, Ltd., Japan, "Development of aluminum gate thin-film transistors based on aluminum oxide insulators," Mat. Res. Soc. Symp. Proc. Vol. 284, p. 371-382, 1993.

14. Georg Hass, "On the preparation of hard oxide films with precisely controlled thickness on evaporated aluminum mirror," Journal of The Optical Society of America, Vol. 39, No. 7, p.532-540, 1949.

15. Yi Li, Hideki Shimada, Masatoshi Sakairi, Kazuhiro Shigyo, Hideaki Takahashi, and Masahiro Seo, "Formation and breakdown of anodic oxide films on aluminum in Boric acid/ borate solutions," J. Electrochem. Soc., Vol. 144, No. 3, p. 866-876, 1997.

16. M. Peters, M. Lee, Y. Takahashi, S. Beilin, "Thermally stable thin film tantalum pentoxide capacitor for MCM applications," The International Journal of Microcircuits and Electronic Packaging, Vol. 19, No. 4, pp. 364-368, 1996.

17. M. E. Elta, et al., IEEE Elec. Dev. Lett., EDL-3, pp. 127, 1982.

18. K. Ohta, et al., J. Appl. Phys., vol. 59, pp. 1587, 1986.

19. Y. Nishioka, et al., IEEE Trans. Electron Devices, ED-34, pp. 1957, 1987.

20. G. S. Oehrlein, J. Appl. Phys., vol. 59, pp. 1587, 1986.

21. Y. Nishioka, et al., J. Appl. Phys., vol. 61, pp. 2335, 1987.

22. C. Bean, J. Fisher, D. Vermilyea, "Ionic conductivity of tantalum oxide at very high fields," Physical Review, vol. 20, pp. 551-554, 1956.

23. P. Solomon, "High field electron trapping in SiO_2," J. Appl. Phys., vol. 48, pp. 3843-3849, 1977.

Chapter 8

Conclusions

8.1 Promises and Challenges

The main goal of this thesis is to develop a new, low cost and low temperature process to fabricate thin film transistors for flat panel display and sensor array applications. This goal has been successfully achieved and US patents have been awarded and pending on some of the methods/processes developed [8-1,2].

In the final chapter of the thesis, main conclusions of this research work are summarized for CdSe-TFTs and CdS-TFTs.

1. The chemical bath deposition process developed has yielded CdSe-TFTs and CdS-TFTs on thermally grown oxide with very good performance. Typical values of mobility are about 10 $cm^2/V\text{-}s$ for CdSe-TFTs and 1 $cm^2/V\text{-}s$ for CdS-TFTs with W = 200 μm and L = 20 μm.

2. Anodic oxides of Al and Ta developed in this work are usable for fabrication of TFTs on glass substrates by the CBD method. With further improvements, the fabrication of TFT circuits with complex functions is expected using the anodization and CBD methods.

3. The fabrication procedure developed in the present work involves four masks using a G-line mask aligner, two vacuum deposition processes for gate and drain-source formation, one CBD dipping at 80 °C for the formation of active layer, three wet chemical etching processes, and a post fabrication annealing process at 400 °C for few minutes to improve the TFT devices. No CVD, stepper, ion implanter, reactive ion etching and high temperature processing are needed.

4. The novel methods developed in this thesis thus provide a low cost and low temperature procedure for TFTs with a very good yield, uniformity, and reproducibility.

Specific conclusions and contributions of this thesis are described below.

8.2 Al_2O_3 and Ta_2O_5 thin film prepared by anodization

Anodic oxides of Al_2O_3 and Ta_2O_5 with low leakage current density and high breakdown electric field have been successfully fabricated. Various experiments have been carried out with different temperatures, pHs, and ion concentrations in order to obtain anodization conditions for high quality dielectric. Chemical bath deposition experiments have been carried out of substrates coated with these oxides to form active layers for TFT devices. It was observed that the anodized Al_2O_3 was eroded in dipping solutions within certain pH values. Specifically, Al_2O_3 reacts relatively vigorously in a CBD dipping solution with a large pH value. Hence, the range of pH values suitable for CBD deposition is limited. It has been found that the optimum pH value for the formation

of high quality CdS and CdSe thin films is about 10~11. Hence, the quality of CBD thin films on the anodic Al_2O_3 can not be optimized due to the limitation of the pH value. It would be ideal to develop a CBD process involving solutions with pH ~ 7, which is also the best value used for anodization of Al_2O_3.

The range of usable pH values was found to increase significantly for anodic Ta_2O_5. From the present experiments, it was observed that good quality CdS and CdSe can be CBD-deposited on anodic Ta_2O_5 in solutions even with high or low pH values. In addition, the large dielectric constant has allowed capacitors with large capacitance density to be fabricated. Although CBD-CdS and CdSe can be deposited from solutions with different pH values, there are still problems to be solved. One of the problems for tantalum oxide is its low breakdown field accompanied by a high leakage current as indicated in Table 7-1.

The breakdown electric field of the metal-insulator-metal (MIM) capacitors made on the anodized Al_2O_3 is as high as 6 MV/cm, with a leakage current density of 15 nA/cm^2 at 2.5 MV/cm. For the anodic Ta_2O_5, the MIM capacitors fabricated showed relatively large leakage current densities (about 0.6 $\mu A/cm^2$ at 10 V) and low breakdown electric field (~ 0.6 MV/cm) with a capacitance density of 85 nF/cm^2.

There are several possible mechanisms for the leakage current in a dielectric film such as Schottky emission, Poole-Frenkel emission, Fowler-Nordheim tunneling, and a space charge limited effect [8-3]. By carrying out annealing in N_2O, O_2 plasma, and two-step process, the leakage current of Ta_2O_5 dielectric may be further reduced. With these further improvements, it is expected TFT circuits for LCD applications can be fabricated using the anodization and CBD methods. In addition to the above improvements, either Al or Cu has to be deposited on top of the electrodes to reduce resistance. Finally, the thermal stability and adherence of these two materials have to be considered in the future applications.

8.3 CdSe and CdS thin films prepared by CBD method

The compositions of the dipping solutions for the TFTs have first been established in this thesis. These solutions have been tested and the results have shown very good reproducibility for the deposition of thin films in the thickness range 80 – 400 nm. It is noted that low cost reagents are sufficient for the preparation of the deposition solutions. Using these solutions, CdSe-TFTs and CdS-TFTs of good performance have been obtained. The novel CBD process has provided an alternate way to deposit the active layer in the fabrication of TFTs. Results obtained in this work also showed that the dipping conditions have to be controlled according to the dielectric materials used in order to fabricate good quality TFTs. The results in this work thus indicated that the best conditions established for thermally grown oxide couldn't be used on another anodic oxide. This is especially true for Al_2O_3. However, for anodic Ta_2O_5 the required change in dipping conditions for CdS-TFTs is less compared to Al_2O_3.

TFTs fabricated on the anodic Ta_2O_5 were found to have large ON-currents. It is expected that the present TFTs of CdSe will find applications in LCD circuits if the breakdown electric field of the Ta_2O_5 can be increased further. Parameters to be optimized in the future include uniformity of solution, substrate position in the solution, and ultrasonic cleaning process after each dipping. In addition, the purity of chemicals used and the exact steps for the solution preparation, the starting time and duration for each dipping need to be fine-tuned. For large-scale production, a study of recycling of the chemicals and a new design of deposition chamber for large substrates are required.

Since the CBD technique involves the use of diluted solutions of compounds at low temperatures, possible experimental or production hazards are minimized due to the low vapor pressures of the reactants involved. Furthermore, the un-reacted ions can precipitate in the bath as sulfides or selenides and the solid may be separated and stored for recycling to produce the starting materials. Overall, the potential for large area deposition and scaling with complete control of material handling in solid or liquid phase

of the CBD process has offered perspective toward the industrial production thin film devices for optoelectronics applications.

8.4 CdS-TFTs and CdSe-TFTs

Thin film transistors, once called "a late flowering bloom" by T. P. Brody, one of the pioneers of the TFT technology, is now entering full bloom stage. Mass production of active-matrix addressed liquid crystal displays using TFTs has begun. Further improvements in TFT technology are directed towards low cost and hence low temperature processes. These two requirements have been specifically addressed in this work on both CdS and CdSe active layers. The market share of circuits with TFTs will surely increase as technologies for CdSe-TFTs and CdS-TFTs are improved so that high performance circuits can be fabricated at low process temperatures and low cost.

From the systematic characterization of TFTs fabricated in this work, it has been concluded that both CdSe-TFTs and CdS-TFTs could be prepared by chemical bath deposition. The present TFTs showed sharp transfer characteristics with a switching ratio of 10^6 at a gate voltage of 10 volts. The mobilities in CdSe-TFTs were greater than 10 cm^2/V-sec with a maximum value of 15 cm^2/V-sec on Si substrates. Although the best results are obtained from TFTs on Si substrates with thermally grown SiO_2 gate dielectric, TFTs with relatively good characteristics were successfully fabricated on glass substrates with anodized dielectrics.

Using the anodic Al_2O_3 as a gate dielectric, TFTs with CdS and CdSe active films grown by the CBD method have been fabricated on glass substrates. The fabricated CdSe-TFTs exhibited a field effect mobility of 3.4 cm^2/V-s, threshold voltage of 5.2 V, subthreshold slope of 1.3 V/dec, and ON/OFF current ratios greater than 10^5. A field effect mobility of 0.2 cm^2/V-s, threshold voltage of 6.3 V, subthreshold slope of 1.5 V/dec, and ON/OFF current ratios exceeding 10^4 were observed for CdS-TFTs. Although

the TFTs with anodic Ta_2O_5 gate dielectric and sputtered SiN_x were also successfully fabricated, the performance is still not as good as the ones on thermally grown SiO_2. More work is therefore needed in the future to improve the anodization process and CBD process. Once good quality anodic oxides and CBD active layers are developed, TFTs with performance comparable to those on the thermally grown SiO_2 may be obtained. This will allow low cost TFT circuits to be fabricated on glass substrates.

8.5 Future studies

Several recommendations are given here as a result of the present research work for future improvements of CdS-TFTs and CdSe-TFTs.

1. The compositions of the CBD solutions should be improved further. This is because the quality of the CBD thin films is not only determined by temperatures, ultrasonic clean process, and timing control but also the relative concentrations and pH value. In addition, systematic post-deposition heat treatment experiments should be made in different atmospheres after the CBD deposition.

2. The quality of gate dielectric is the key to improving the performance of the TFTs. Hence, it is important to know how to provide a favorable surface for the growth of CdSe and CdS by the CBD method. One possible way to improve the dielectric properties is to adopt TaN or Ta_2Si instead of sputtered Ta layer for the anodization. It has been reported that Ta_2O_5 films obtained by anodization of TaN and Ta_2Si have very low leakage current (<1 nA/cm^2 at 10 V) and high breakdown fields (> 4 MV/cm) [8-4]. Another method is to adopt a multiplayer structure $Al/Al_2O_3/TaON_x$ structures or two-step oxidized sputtered/anodized films. It was also found that a post anodization annealing is important for the following deposition process of active layer, as the surface states and the roughness on the surface of the gate dielectric can be improved by the annealing. The anodization of a multiple-layer with $Al/Al_2O_3/Ta_2O_5$ structure should be tried. This should be

done to take advantage of chemical resistant of Ta_2O_5 and low resistivity of Al layer. Here, the intermediate Al_2O_3 layer will serve as a buffer layer to relax the stresses and to reduce hillock formation between aluminum and anodic Ta_2O_5. In addition, in view of the high trapping state density in the present CdSe and CdS films, it is necessary to passivate these semiconductors with a proper method. The hydrogen passivation used in poly-Si technology may be a key for this purpose.

3. New units for CBD deposition and anodization of large area substrates must be developed. For these new units, special attention should be paid to the control of the temperatures, pH values, and concentrations in the solution. Finally, a material recycling method needs to be explored.

With the above specific improvements and increased understanding of the materials and processes, it is anticipated the novel CBD and anodization will find applications in the TFT/LCD industry. This could provide a monolithic and low cost route for fully integrated array technology to challenge the present Si-based technology. In addition, the driving circuit applications for digital X-ray imaging system in the medical domain do also need the TFT fabrication process. Another important application of the CBD process is to provide a passivation surface for InP substrates. By combining the CBD-deposited CdSe or CdS with anodization process, surface state density of InP can be reduced.

References

1. F. Y. Gan, I. Shih, "Methods to Fabricate Thin Film Transistors and Circuits," US patent No. US6225149, awarded on 05/01/2001 at the United States Department of Commerce, Patent and Trademark Office.

2. F. Y. Gan, I. Shih, "Methods to Fabricate Thin Film Transistors and Circuits," Continuous patent application on 06/30/2001 at the United States Department of Commerce, Patent and Trademark Office.

3. R. R. Kola, M. Y. Lau, S. Duenas, H. Y. Kumagai, P. R. Smith. R. C. Frye, K. L. Tai, and P. A. Sullivan, " Thin film resistors and capacitors for advanced packaging," 1997 International Symposium on Advanced Packaging Materials, pp. 71-74, 1997.

4. P. Brazis, J. Mater. Sci. Lett. Vol. 9, pp. 266, 1990.