Frequency Reference MEMS-Based Oscillators

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To My Family

Acknowledgments

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List of Acronyms

AWG	Arbitrary waveform generator
BW	Bandwidth
CMOS	Complementary metal-oxide-semiconductor
CP	Charge pump
DAC	Digital to analog converter
DC	Direct current
DFF	D flip-flop
EMI	Electro-magnetic interference
EMS	Electro-magnetic susceptibility
FET	Field-effect transistor
FF	Fast-Fast
FinFET	Fin field-effect transistor
FSM	Finite-state-machine
GPS	Global positioning system
IC	Integrated circuit
LF	Loop filter
LPF	Low-pass filter
MEMS	Micro-electro-mechanical systems

MIDIS	MEMS Integrated Design for Inertial Sensors
MIM	Metal-insulator-metal
MOM	Metal-oxide-metal
MTBF	Mean-Time-Between-Failure
PCB	Printed circuit board
PDK	Process design kit
PFD	Phase-frequency detector
PLL	Phase-locked loop
PM	Phase margin
ppm	Part per million
QFN	Quad flat no-lead
QFP	Quad flat package
RF	Radio frequency
RGC	Regulated-cascode
RGT	Resonant gate transistor
SEM	Scanning-electron micrograph
SiP	System in package
SS	Slow-Slow
TIA	Transimpedance amplifier
ToF	Time-of-flight
TT	Typical-Typical
VCO	Voltage-controlled Oscillator

Abstract

Timing and frequency reference oscillators are pivotal blocks in almost all electronic systems. Emerging applications, including internet-of-things (IoT) and mobile devices, impose stringent requirements on power consumption (battery life), cost, and size. In recent years, reference oscillators based on microelectromechanical systems (MEMS) resonators have become a key alternative to those based on quartz crystal resonators for enabling miniaturized systems along with high-performance levels.

This dissertation introduces a 6.89 MHz MEMS oscillator based on an ultra-low-power, low-noise, tunable gain/duty-cycle transimpedance amplifier (TIA) and a bulk Lamé-mode MEMS resonator that has a quality factor (Q) of 3.24×10^6. Self-cascoding and current-starving techniques are used in the TIA design to minimize the power consumption and tune the duty cycle of the output signal. The TIA was designed and fabricated in a TSMC 65 nm CMOS process technology. Its open-loop performance has been measured separately. It achieves a tunable gain between 107.9 dBΩ and 118.1 dBΩ while dissipating only 143 nW from a 1 V supply. The duty cycle of the output waveform can be tuned from 23.25% to 79.03%. The TIA has been interfaced, wire bonded, in a series-resonant oscillator configuration with the MEMS resonator, and mounted in a small cavity standard package. The closed-loop performance of the whole oscillator has been experimentally measured. It exhibits a phase noise

of -128.1 dBc/Hz and -133.7 dBc/Hz at 1 kHz and 1 MHz offsets, respectively.

A 110.2 MHz ultra-low-power phase-locked loop (PLL) has been designed for MEMS frequency reference oscillator applications. It utilizes the 6.89 MHz MEMS-based oscillator as an input reference frequency. An ultra-low-power, high-resolution phase-frequency detector (PFD) has been designed to achieve low noise performance. Eliminating the reset feedback path used in conventional PFDs has led to dead-/blind- zone free phase characteristics, which is crucial for low noise applications and a wide operating frequency range. The PFD operates up to 2.5 GHz and achieves a linear resolution of 100 ps input time difference (Δt_{in}), without any additional calibration circuits. The linearity of the proposed PFD is tested over a phase difference corresponding to Δt_{in} from 100 ps to 50 ns. At a 1 V supply voltage, it shows an error of $<\pm 1.6\%$ with a resolution of 100 ps and a frequency normalized power consumption (P_n) of 0.106 pW/Hz. The PLL is designed and fabricated in a TSMC 65 nm CMOS process technology and interfaced with the MEMS-based oscillator. The system reports a phase noise of -106.21 dBc/Hz and -135.36 dBc/Hz at 1 kHz and 1 MHz offsets, respectively. It occupies an active CMOS area of 0.1095 mm^2 and consumes 6.709 μW at a 1 V supply voltage.

Résumé

Les oscillateurs servant de référence temporelle ou fréquentielle sont des blocs essentiels dans presque tous les systèmes électroniques. Les applications émergentes, en particulier l'internet des objets (IoT) et les appareils mobiles, imposent des exigences strictes en matière de consommation d'énergie (autonomie de la batterie), de coût et de taille. Ces dernières années, les oscillateurs de référence basés sur des résonateurs de systèmes microélectromécaniques (MEMS) sont devenus une alternative viable à ceux basés sur des résonateurs à cristaux de quartz, afin de permettre des systèmes miniaturisés avec un haut niveau de performance.

Cette thèse présente un oscillateur MEMS de 6,89 MHz basés sur un amplificateur transimpédance (TIA) à très faible puissance, à faible bruit, à gain/cycle de service réglable et un résonateur MEMS de 6,89 MHz en mode Lamé massif, dont le facteur de qualité (Q) est de $3{,}24\times10^6$. Des techniques d'auto-cascodage et de limitation du courant sont utilisées pour minimiser la consommation d'énergie et régler le rapport cyclique de signal de sortie. Le TIA a été conçu et fabriqué dans une technologie de processus CMOS TSMC 65 nm. Ses performances en boucle ouverte a été mesurée séparément. Ainsi le gain du TIA est réglable entre 107,9 dBΩ et 118,1 dBΩ tout en dissipant seulement 143 nW à partir d'une alimentation de 1 V. Le rapport cyclique de la forme d'onde de sortie peut être modifié entre 23,25 % à 79,03 %. Le

TIA a été interfacé, câblé, dans une configuration d'oscillateur résonnant en série avec le résonateur MEMS et monté dans un petit boîtier standard à cavité. Les performances en boucle fermée du l'oscillateur entier a été mesuré expérimentalement. Il présente un bruit de phase de -128,1 dBc/Hz et -133,7 dBc/Hz à des décalages de 1 kHz et 1 MHz, respectivement.

Une boucle à verrouillage de phase (PLL) de 110,2 MHz à très faible puissance a été conçue pour les applications d'oscillateur de référence de fréquence MEMS. Elle utilise l'oscillateur MEMS de 6,89 MHz comme référence d'entrée. Un détecteur phase-fréquence (PFD) haute résolution et à très faible consommation a été conçu pour obtenir des performances à faible bruit. L'élimination du chemin de retour de réinitialisation utilisé dans les PFD conventionnels a permis d'obtenir des caractéristiques de phase sans zone morte ou aveugle, ce qui est crucial pour les applications à faible bruit et une large gamme de fréquences de fonctionnement. Le PFD fonctionne jusqu'à 2,5 GHz et atteint une résolution linéaire de 100 ps de différence de temps d'entrée (Δt_{in}), sans avoir besoin de circuits de calibration supplémentaires. La linéarité du PFD proposé est testée sur une différence de phase correspondant à un Δt_{in} de 100 ps à 50 ns. A une tension d'alimentation de 1 V, il montre une erreur de $<\pm$1,6% avec une résolution de 100 ps, et une consommation d'énergie normalisée en fréquence (P_n) de 0.106 pW/Hz. La PLL est conçue et fabriquée dans une technologie de processus CMOS TSMC 65 nm et interfacée avec l'oscillateur basé sur les MEMS. Le système présente un bruit de phase de -106,21 dBc/Hz et -135,36 dBc/Hz à des décalages de 1 kHz et 1 MHz, respectivement. Il consomme 6,709 μW à une alimentation de 1 V et occupe 0,1095 mm^2 de surface CMOS active.

Chapter 1

Introduction

The basic concept of timing and frequency references is covered in this chapter. It begins with the evolutionary history and literature of different references. The chapter examines modern reference oscillators, demonstrates primary transduction techniques, and introduces the quartz and MEMS technologies. It goes over the various types, of reference oscillators, compensation techniques, requirements, and performance levels. The chapter finally concludes with contribution of this work and the dissertation's overall organization.

1.1 Evolution of Timing and Frequency References

Louis Essen and Jack Parry invented the revolutionary caesium atomic frequency standard in 1955, depicted in Figure 1.1 [1]. It was not a clock but rather a calibration device for external quartz clock frequencies, which led to redefining the "*Second*". Before arriving at this point, there has been a long history of time tracking. Since the dawn of consciousness, different civilizations have sought various methods to measure the time adequately. Over the centuries, many timekeeping devices have been devel-

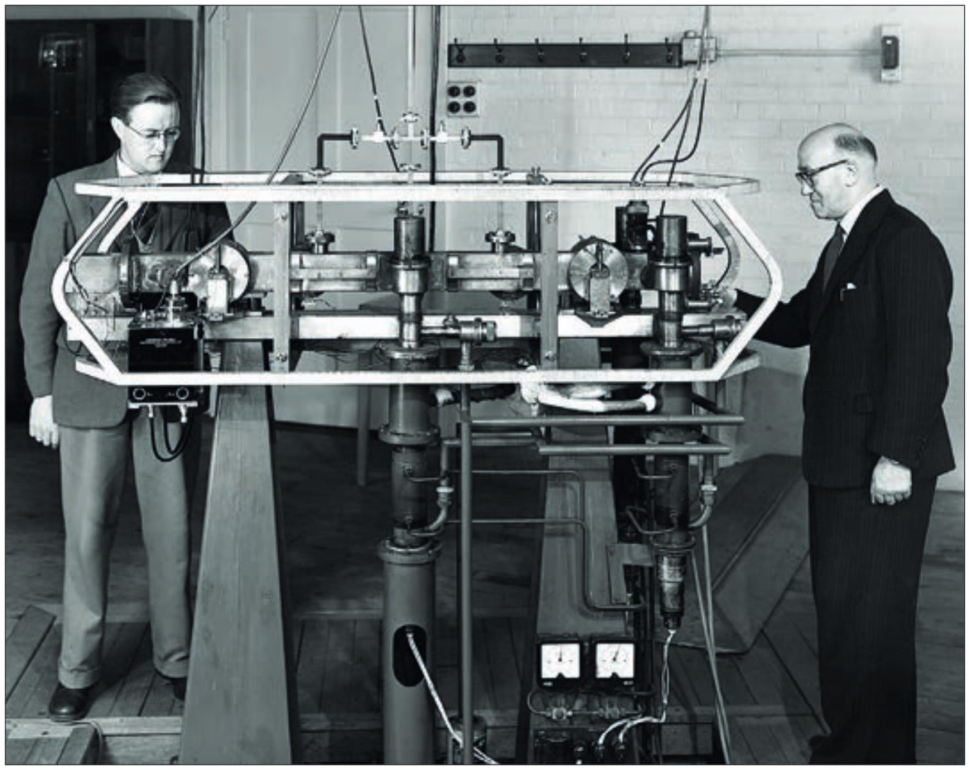


Fig. 1.1 Jack Parry and Louis Essen beside their caesium frequency standard, 1955 [1].

oped and have taken multiple forms [2]. The common thing between all of them is that they have all depended on repetitive, oscillating, periodic natural phenomena. The earliest human endeavors relied on the periodic motion of the sun and the stars. The sun position in the sky was used to estimate the time during the day by using shadow clocks or sundials. Figure 1.2 shows one of the earliest sundials used by ancient Egyptians during the reign of Thutmose III, *c.*1600 BC [3]. The sundial dependency on the sun and the need to track the time during night as well have led to the water clock invention that can track time independently of the sun. Water clocks use the constant rate of water flow through a fixed opening to measure the time passage. Ancient Egyptians have used them back in *c.*1300 BC [4, 5, 6, 7]. Later then, mechanical timing references started in the Renaissance era with the pendulum clocks and the spring-wound watches. Several developments on such devices have been introduced

Fig. 1.2 Egyptian L-shaped sundial, reign of Thutmose III, *c.*1600 BC [3].

over time to enhance performance. For example, the temperature dependency of the pendulum length is used to affect the accuracy of time tracking from one season to another. This has led to the idea of constructing the pendulum from two materials with different thermal expansion coefficients to cancel out, to the first order, the total pendulum length change caused by temperature variation. This is considered one of the very first forms of "temperature compensation" techniques in timekeeping applications. During the 1780s, after years of trials and experiments, the British clockmaker

John Harrison from Yorkshire has combined the accuracy and portability by introducing the first marine chronometer for longitude calculation [8, 9]. This device included compensation techniques for temperature and motion effects. It gave superiority, for years back then, for the British overseas.

These trials and developments over history show the continuous search for accurate, small, portable, and power-efficient timing and frequency reference systems. The work presented here tackles the exact specifications and requirements for timing and frequency reference systems, except it is orders of magnitude smaller, more power-efficient, and more accurate.

1.2 Modern Reference Oscillators

Frequency reference oscillators are key blocks in almost all electronic devices [10]. Emerging applications such as internet-of-things (IoT), implantable medical devices, smart watches, and mobile devices impose stringent requirements on power consumption (battery life), cost, and size [11]. MEMS-based reference oscillators have emerged as viable alternatives to those based on quartz crystal resonators, enabling system miniaturization and complete system-on-chip (SoC) while maintaining high performance [12, 13, 14]. Figure 1.3 shows an example of the monolithic integration of MEMS with CMOS [15].

A resonator is either a mechanical or an electrical device that resonates at a specific frequency, the resonant frequency (f_r). Based on the resonator's material properties, dimensions, and structure, some quantities are used to set the resonant frequency. These quantities are fixed, and the resonator's dimensions are accurately machined so that the designer can, theoretically, set a fixed resonant frequency throughout the

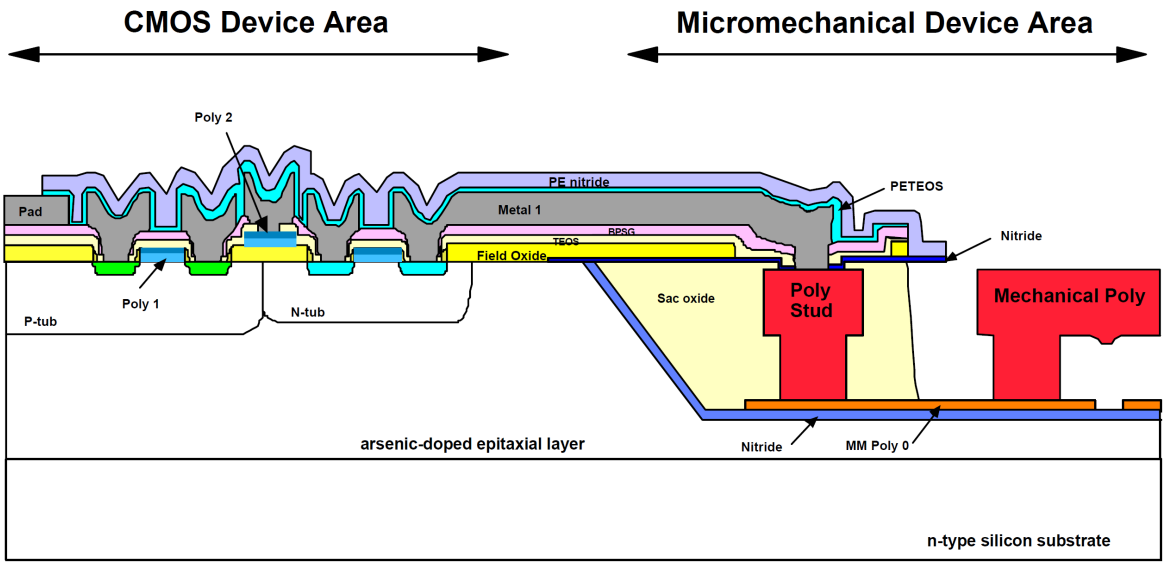


Fig. 1.3 SoC integration: Integrated embedded MEMS technology, a subsurface cross-section [15].

resonator's lifetime. The resonator creates a decaying sinusoidal signal.

It, ideally, blocks out all frequencies, except for the resonant frequency. A sustaining amplifier circuit is interfaced with the resonator in a positive feedback loop to build a self-sustaining oscillator.

Quartz is a dominant resonator technology that has been used in the market for decades to build up oscillators. This is due to the quartz stability and absolute frequency accuracy. However, microelectromechanical systems (MEMS) technology has shown a promising capability to compete with quartz and efficiently overcome the new challenges imposed by emerging electronic systems.

The rest of this chapter will address quartz and MEMS technologies. It introduces the categories (high, medium, low performance), the requirements, and the parameters of a reference oscillator. In the end, the motivation of this work will be shown and discussed.

1.3 Resonator Transduction Types

A transducer is an electronic device that is responsible for changing the energy from one form to another. A mechanical movement, or a mechanical force, transforms into an electrical energy in resonators like quartz and MEMS. There are two types of how this transformation occurs:

- **Piezoelectric Transduction:** It causes an electromechanical coupling that excites the resonance mode of the mechanical structure.
- **Capacitive Transduction:** An electrical force is used to excite a particular resonance mode of the mechanical structure.

1.4 Quartz Crystal vs Micromachined Based Oscillators

1.4.1 Quartz Crystal Resonators

Quartz crystal is one of the oldest used resonators. Its high stability and frequency accuracy made it the dominant choice for the industry over decades in timing reference market and frequency synthesis applications. According to the market research report issued by "Allied Market Research" in January 2020, the global quartz market valued $8.32 billion in 2018 [16]. J. W. Horton and W. A. Marrison have developed the first quartz clock at Bell Telephone Laboratories (Bell Labs) in the summer of 1927 [17]. Figure 1.4 shows the quartz crystal, in its original mounting, used in the first quartz clock in 1927 [18]. Figure 1.5 shows the Bell frequency standard system in 1930, made out of four temperature-controlled ring crystals in their separate ovens [19]. Figure 1.6 shows one of today's commercial quartz crystals, with and without the encasement [20].

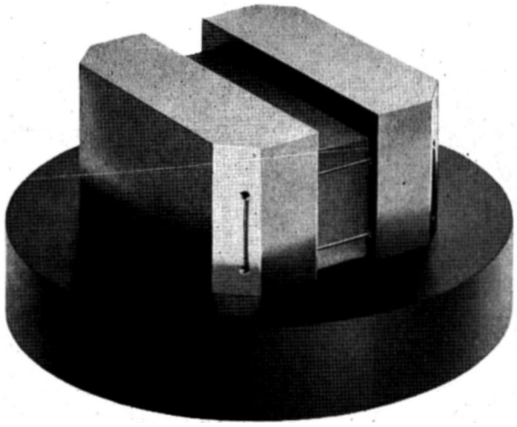


Fig. 1.4 The piezoelectric quartz plate resonator, in its original mounting, used in the first quartz clock, 1927 [18].

Fig. 1.5 The Bell Lab frequency standard system, 1930 [19].

Fig. 1.6 A commercial quartz crystal with the cap on the left and without the cap on the right [20].

Because quartz is a single crystalline material, its properties are highly stable and repeatable across multiple fabrication processes. It is a piezoelectric material that facilitates transduction from mechanical vibrations to electrical signals, allowing for an easy interface with electronic devices. The resonator's characteristics and physical features depend on the crystal's structure and cut angle [21, 22]. Based on the axis and the cut angle, the temperature sensitivity can be minimized, and a zero-temperature coefficient (TCF) can be reached in a small range, at one or two temperature degrees [23, 24]. There are different types of crystal cuts including AT-, BT-, CT-, SC-, ... cuts. Figure 1.7 shows the frequency-temperature characteristics for different crystal cuts [25].

The quartz has a lot of advantages that, indeed, led to dominating the frequency reference market for decades. However, cost, size, and system-on-chip (SOC) integration, required by new mobile, wearable devices, Internet of things (IoT) applications and multi-mode radio frequency applications, impose a real challenge on the quartz nowadays. Quartz fabrication is not compatible with the standard CMOS process used in the Integrated Circuits (ICs). This makes the quartz an off-chip component, limiting complete system integration, miniaturization, and power reduction. In addition, the

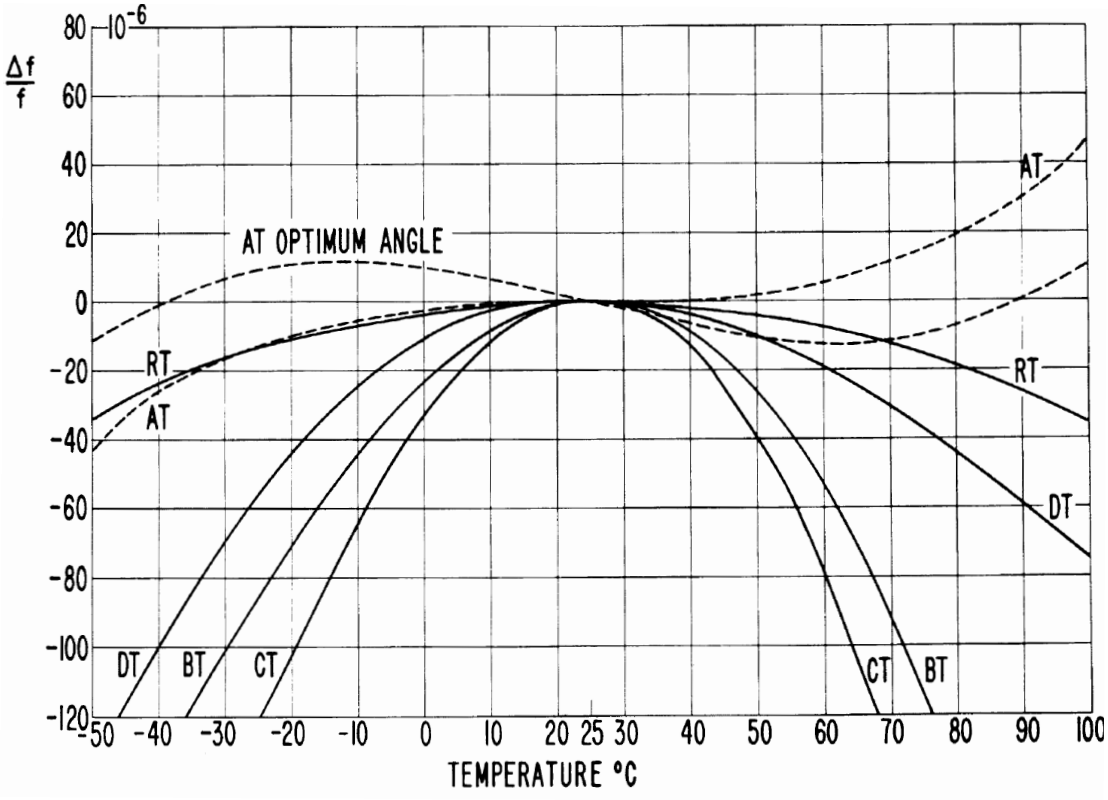


Fig. 1.7 Frequency-temperature characteristics for different quartz crystal resonator cuts [25].

maximum frequency offered by the quartz-based oscillators is limited. Hence, frequency synthesizers based on these reference oscillators need a reduced loop filter bandwidth, which requires increasing the filter size to the extent that it may not practically fit anymore as an on-chip block [26].

On the other hand, MEMS technology is a promising candidate that faces challenges mentioned above, offering higher stable frequency, significantly smaller form factor, more power reduction, and higher integration capability [11, 27].

1.4.2 Microelectromechanical Systems (MEMS) Resonators

MEMS is a micro-machined structure resonator that vibrates at a specific resonant frequency (f_r) upon external electrostatic excitement [28]. In 1965, Nathanson developed the silicon surface resonant-gate transistor, shown in Figure 1.8, with a high-Q band-pass property [29]. This has led to the exploration of the resonance properties of the MEMS structures. Then, in 1967, Nathanson has introduced the resonant gate transistor, shown in Figure 1.9, as a silicon integrable device that offers a high-Q frequency selection [30]. This is considered the first MEMS resonator that has been developed. It is a field-effect transistor (FET) with an etched oxide, leaving a suspended metal electrode. After Nathanson had applied an electrical AC signal with a frequency close to the resonant frequency of the suspended cantilever, the device started to vibrate. The electrodes placed below the cantilever and through electrostatic transduction have allowed for electrical actuation and sensing. This idea has initiated an enormous effort of studying, characterizing, and developing MEMS resonators for different applications, including sensors and oscillators. In the beginning, the realization of MEMS-based oscillators faced some challenges, including high insertion loss and temperature sensitivity. In addition, a clean vacuum encapsulation was

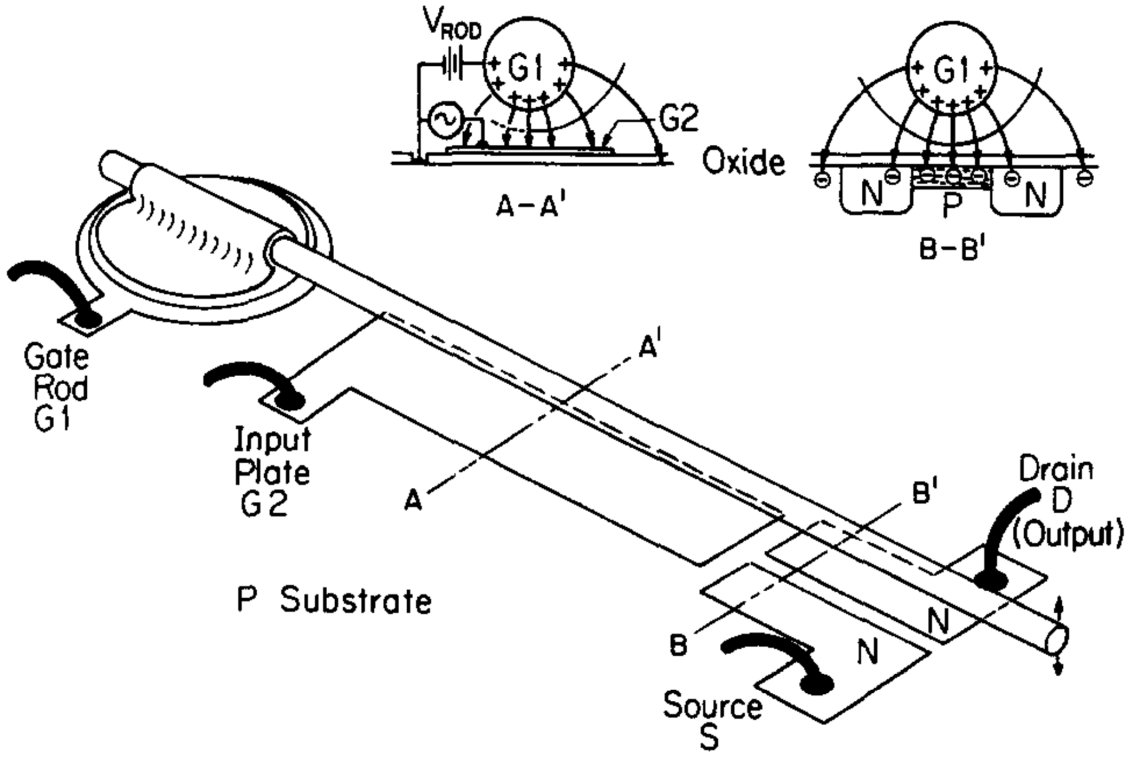


Fig. 1.8 The silicon surface resonant-gate transistor, 1965 [29].

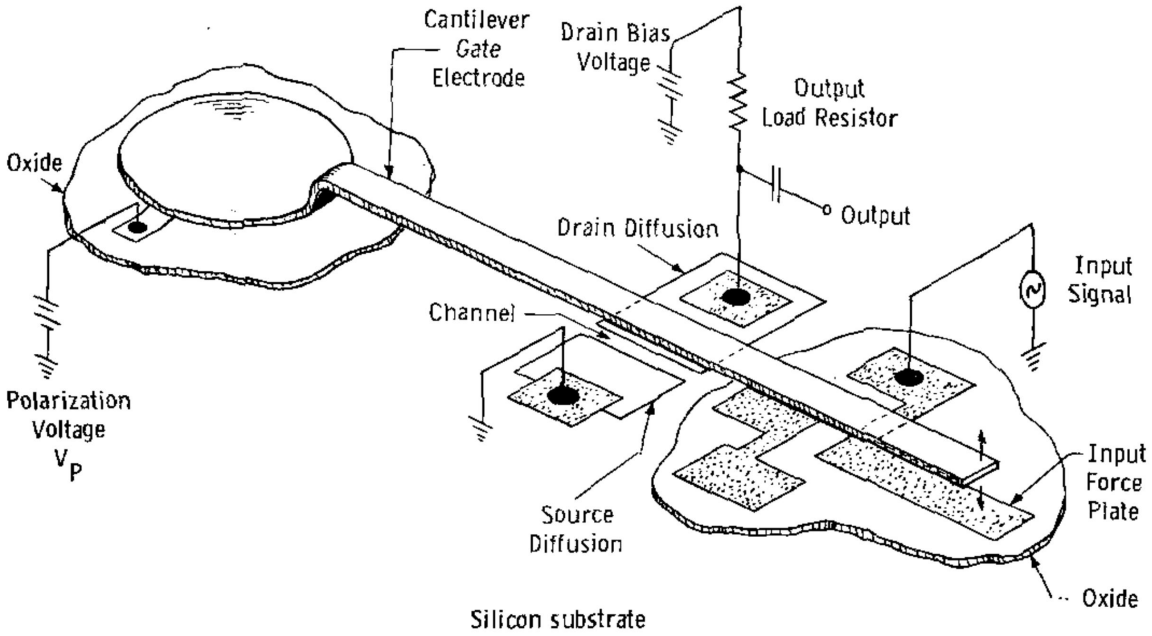


Fig. 1.9 The resonant gate transistor (RGT), 1967 [30].

needed to reduce the damping losses. In the 1980s and the 1990s, MEMS resonators for sensing applications emerged [31]. MEMS-based accelerometer [32, 33, 34], gyroscope [35, 36, 37], pressure [38, 39, 40, 41], vibration [42, 43, 44, 45], velocity [46, 47], gas [48, 49, 50, 51], strain [52, 53, 54, 55, 56], and flow [57, 58, 59, 60, 61, 62, 63] sensors have vastly evolved and used in applications including aerospace [64, 65, 66, 67, 68], automotive [69, 70, 71, 72, 73], medical [74, 75, 76, 77, 78, 79], and portable electronic devices [80, 81, 82, 83]. In 1999, Nguyen introduced the first fully CMOS integrated MEMS-based oscillator, shown in Figure 1.10, with one order of magnitude higher quality factor (Q) compared to that introduced by Nathanson in [84]. This has motivated the research community and has led to a series of breakthroughs, seeking more effective, more stable, and lower-cost designs. Now, MEMS-based oscillators have an enormous opportunity and a promising future to expand and get a bigger share in the frequency reference market.

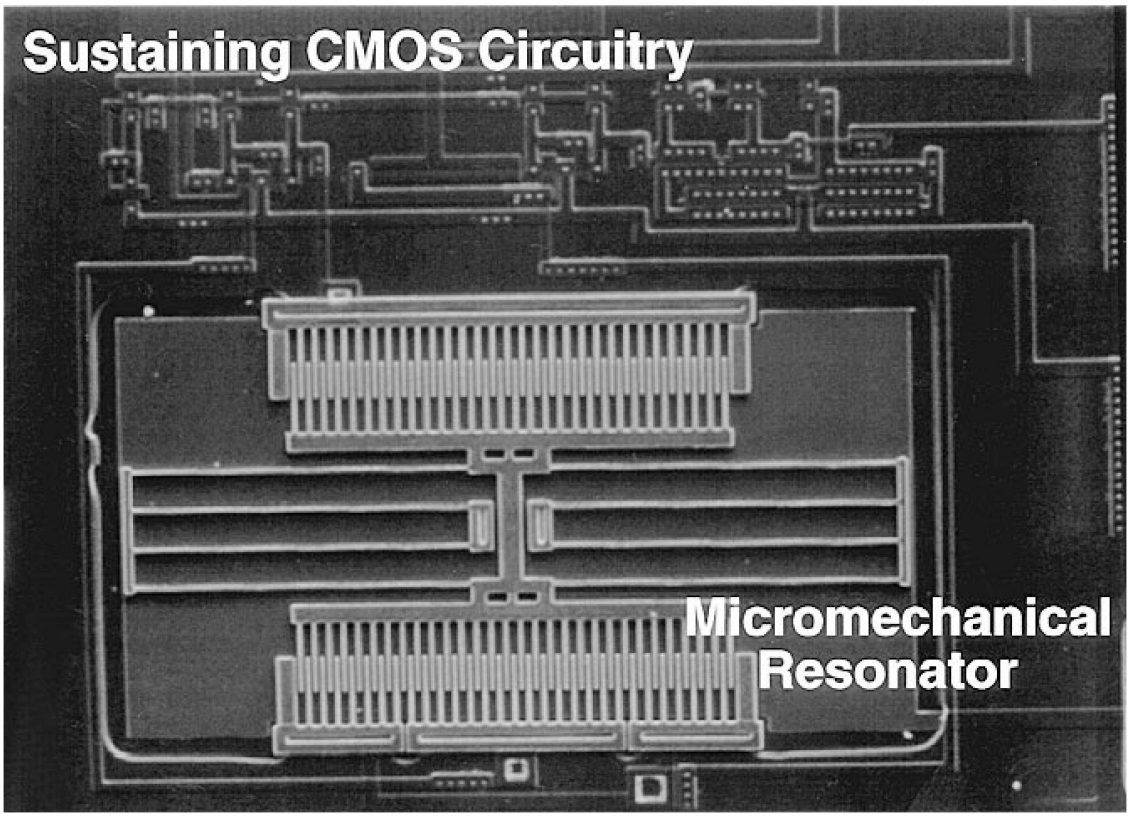


Fig. 1.10 Scanning electron micrograph (SEM) of the 16.5-kHz CMOS micro-resonator oscillator, 1999 [84].

1.4.3 Quartz-based Vs. MEMS-based Oscillators

As mentioned earlier, MEMS can overcome the challenges currently facing quartz due to emerging applications. Some of these crucial challenges include:

a) **Size:** MEMS devices are tiny compared to quartz crystals. They are in the range of 100s of micrometer (μm) and tend to get smaller. The MEMS size is inversely proportional with the resonant frequency it is designed for; the higher the resonant frequency, the smaller the MEMS device. This is important due to the continuous shrinkage of portable electronic systems. Figure 1.11 shows the comparison between two system oscillators' footprints. The MEMS-based oscillator is 50% smaller than the quartz-based counterpart.

b) **Shock and Vibration:** MEMS resonators are inherently more robust against shocks and vibration than quartz crystals which are sensitive to mechanical shocks by nature [28, 86]. This is very important for portable and wearable devices including, smart and sports watches. Center anchored, and single-point MEMS resonator designs virtually eliminate the sources of stress error [86]. The resonator moving mass is extremely small, requiring a tremendous acceleration to cause a sufficiently large force. The resonator structure operates like a very stiff spring, which is very difficult to be affected by an external force. Figure 1.12 shows how a MEMS from SiTime Corporation has 200× better performance than its quartz counterparts in terms of vibration sensitivity [87].

c) **CMOS Compatibility and Integration:** Quartz is made from a different material, through a separate process that needs single and unique processing techniques, even for packaging. On the other hand, MEMS technologies use standard CMOS processes, tools, and fabs, which allow for direct monolithic

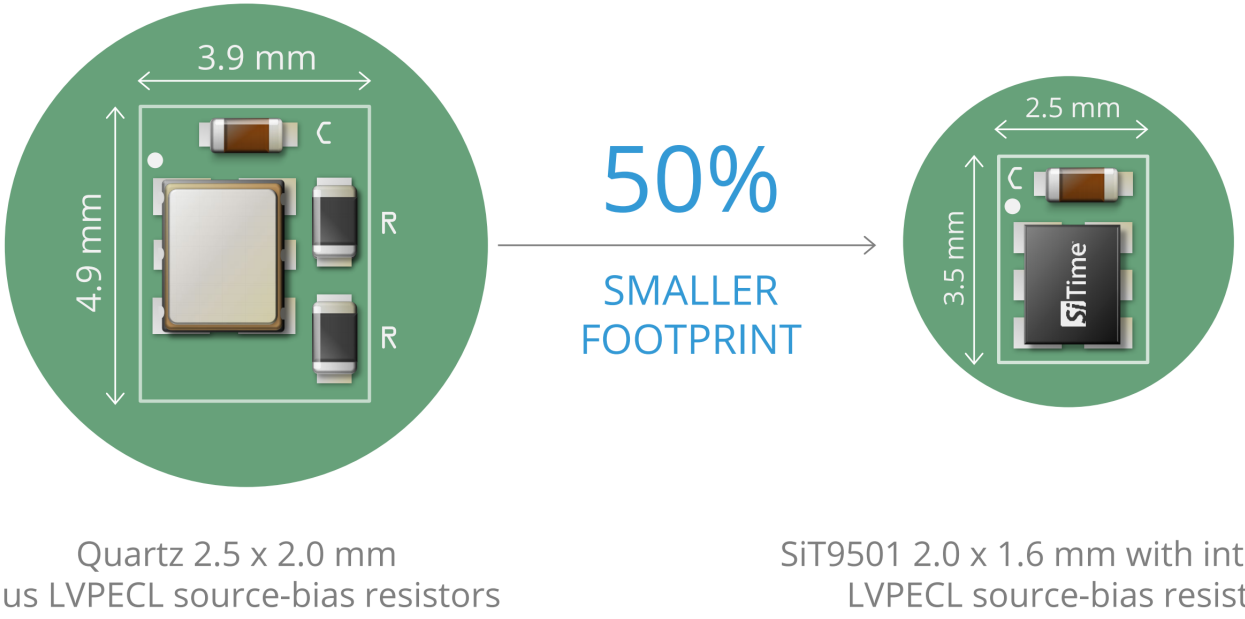


Fig. 1.11 Quartz-based vs. MEMS-based oscillator size [85].

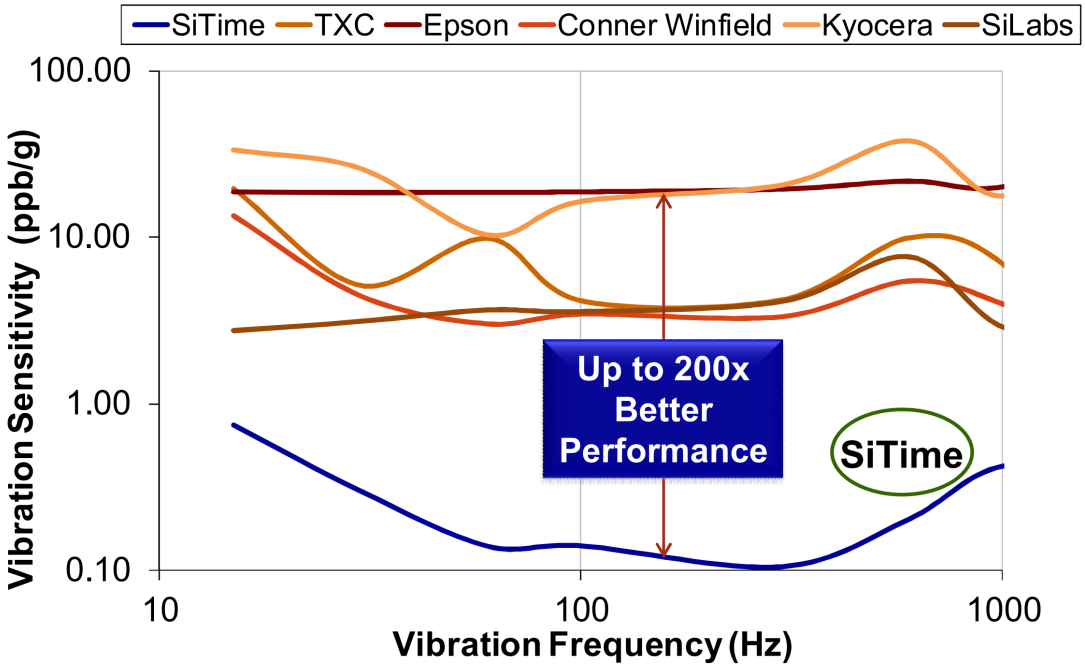


Fig. 1.12 MEMS vs. quartz vibration sensitivity [87].

integration with standard CMOS substrates [88]. This enables smaller size, lower power consumption, cheaper cost, and higher performance than the quartz, which is installed as a discrete component.

d) **Frequency:** Manufacturing a quartz resonator, reliably beyond hundreds of megahertz is very difficult due to the need for very thin quartz films to achieve high frequencies [89]. As mentioned earlier, frequency synthesizers based on low-frequency reference resonators should have a smaller loop bandwidth. This requires a bigger loop filter size, and the filter may become an off-chip component. On the other hand, MEMS has shown a competitive performance in the gigahertz frequency range, proposing itself as an emerging key player in the market because of the increasing demand for higher communication data rates [90].

e) **Supply Chain:** MEMS uses standard fabs and wafer-scale batch processing technology for fabrication; this allows for hundreds of thousands of devices to be fabricated simultaneously on a single wafer. On the other hand, the quartz needs specialized lines per package and scale by adding factories. In addition, it uses ceramic packages that only one supplier controls around 80% of their market. On the contrary, MEMS uses plastic packaging that multiple different suppliers offer. Technologies including epi-seal encapsulation allow packaging for MEMS on the wafer level [89]. All these advantages allow for cheaper and higher volume MEMS production. Table 1.1 from [91] shows the advantage of MEMS over quartz in different supply chain aspects.

f) **Electro-Magnetic Susceptibility (EMS)** measures the timing device's immunity to electro-magnetic interference (EMI) from other electronic devices. MEMS-based oscillators introduce a better EMS performance than those based on quartz crystals. The ultra-small size of MEMS resonators minimizes the antenna pick-up effects compared to large quartz counterparts. In addition, MEMS resonators are electrostatically driven making them, inherently, more immune to EMI than piezoelectric quartz resonators that are more susceptible to EMI [87].

g) **Aging:** Quartz resonators require special packaging to achieve lower aging rates, and they still can drift by a few parts per million (ppm) per year. On the other hand, MEMS, epi-sealed resonators, can perform better, even in plastic packaging, by order of magnitude [92].

h) **Reliability:** Due to its silicon-based nature, MEMS has recently proven longer-term reliability than quartz. Its mean-time-between-failure (MTBF) has reached 1960 million hours for some designs compared to less than 50 million hours for

Table 1.1 MEMS vs. quartz supply chain [91].

	MEMS	Quartz
Processes	• Standard CMOS tools and processes • High volume batch processing	• Proprietary processes • Serial, single part processes
Fabs Foundries	• Modern, standard • Highly controlled • Ultra-clean	• Specialized, unique fabs
Scalability	• Multiple sources to increase capacity	• Slow to ramp and react
Quality control	• CMOS standard • Single customer qualification for many frequencies	• Every part and frequency require customer qualification • High customer audit effort
Cost	• Low-cost foundry • Batch processes	• Custom tooling • Strongly dependent on the utilization

the quartz [93]. Figure 1.13 shows a SiTime MEMS design that reports 35 times better reliability than the quartz counterparts [94].

1.4.4 Oscillator Types and Compensation Techniques

There are different techniques used to stabilize the resonator frequency of an Oscillator: VCXO, TCXO, MCXO, DCXO, OCXO . . . etc. To avoid any confusion, it should be mentioned that the abbreviation "XO" is historically used for the term "Crystal Oscillator." The two letters preceding the "XO" are used to refer to the used compensation technique; for example, TCXO stands for Temperature-Compensated-Crystal-Oscillator. These compensation concepts can be generally applied with any oscillator regardless of the resonator type used. With the emergence of MEMS-based oscillators, some market key players continued to use the abbreviation "XO" to refer generally to the word "Oscillator" even if it is totally based on MEMS resonators, as in SiT5155 [95]. The same convention is used in this dissertation to explain the different compensation techniques generally applied in oscillators. Regardless of the resonator type used, the same concept can be applied.

Different Oscillator Types Brief Explanation

– **Voltage Controlled Oscillator (VCXO):** In this type a control voltage is used to tune the output frequency of an oscillator. It is an electrically tunable oscillator that can be employed in phase-locked loops (PLLs), various applications in telecommunications, and electronic instruments. The oscillator circuit design determines the transfer characteristics, the frequency change vs. the control voltage. The amount of frequency change is defined as the full range. A varactor diode is an example of the electric elements used to vary the oscillation frequency

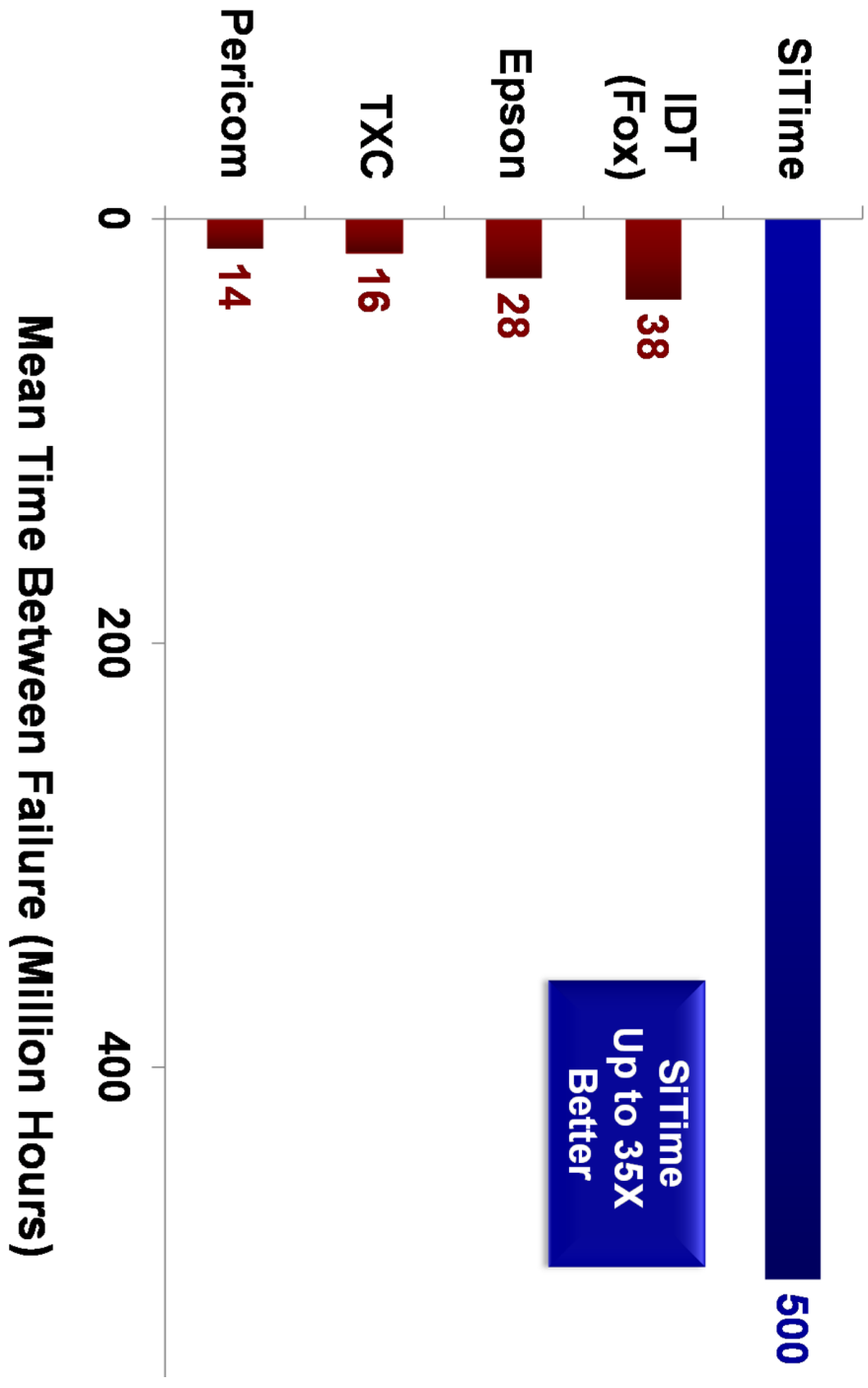


Fig. 1.13 MEMS vs. quartz reliability [94].

based on an applied control voltage.

– **Digitally Controlled Oscillator (DCXO):** Similar to VCXO, DCXO allows tuning or pulling the oscillator output frequency. The difference is that the DCXO allows adjusting the frequency by writing a digital word using one of the bus interfaces as the SPI or the I2C interface. Sometimes it is capable of programming the output frequency to a broader range beyond that of the VCXO. On the other hand, it might suffer from a frequency-jumping problem due to its digital topology [96].

– **Temperature Compensated Oscillator (TCXO)** employs a temperature compensation network to compensate for the resonator's frequency-temperature characteristics. A VCXO is an implicit part of the TCXO; the temperature sensors are used to bias the control voltage of the VCXO circuit.

– **Digitally Controlled Temperature Compensated Oscillator (DCTCXO):** It is a TCXO incorporating the programmable digital functionality of the VCXO in frequency pulling. It has higher frequency stability than the TCXO over a range of temperatures, but it also suffers from a frequency-jumping problem due to its digital topology.

– **Oven Controlled Oscillator (OCXO):** It is based on enclosing the resonator – MEMS or quartz – and other temperature-sensitive components in a temperature controlled stable oven. It offers higher stability and better phase noise performance than other oscillators. The oven is adjusted at a specific temperature at which the resonator has a minor frequency drift. Different circuits are needed to control the oven temperature.

– **Microcomputer Compensated Oscillator (MCXO):** It digitally monitors any drift in the frequency and compensates for it through a DAC connected to a tuning port. It, generally, has better stability than TCXO but worse stability than that of the OCXO. It also suffers from a frequency-jumping problem due to the limitation of the digital circuits in covering the infinite range of the natural analog signals.

1.4.5 Oscillator Characteristics and Performance Categories

Timing reference oscillators are deployed in almost every electronic system. Some requirements or characteristics identify a certain reference oscillator and make it suitable for a specific application. These characteristics include power consumption, cost, oscillator size, accuracy, short- and long-term stability, tunability, duty-cycle, waveform shape, shock, vibration, and EMI sensitivity.

Stability: It measures how the oscillator maintains its designed nominal frequency with the environmental and electrical changes. There are two types of stability:

a) **Short-term stability** measures the frequency stability in the steady-state operation and is usually expressed by jitter or phase-noise.

b) **Long-term stability:** It is the measure of the change in the frequency due to environmental effects, including temperature, humidity, etc., and over time (aging). It is measured in ppm per the environmental effect; for example: stability over temperature is measured in ppm/°C.

Accuracy: measures the change in the oscillator output frequency, in ppm, from the nominal intended designed frequency. It is essential to mention that some references

use the terms stability and accuracy interchangeably when they generally refer to the variation in frequency.

All these specifications determine the performance of the reference oscillator. There are different trad-offs between these characteristics. There is a fundamental trade-off between frequency-tunability and stability. A more stable oscillator tends to be less tunable; it resists any frequency change. Small form-factor oscillators tend to jeopardize and compromise the accuracy due to implicit difficulties and inaccuracy in the fabrication process regarding small sizes [97]. Based on the application, the designer should direct his/her effort toward a specific specification over another and manipulate the trade-offs in his/her favor. For example, the accuracy of a wristwatch is expected to be within a minute over a year. An accuracy within ±100s ppm will be sufficient in this case. It is more important now for this application to focus on decreasing the form-size and the power consumption for the sake of portability than improving the accuracy to less than ±1 ppm [89]. In this dissertation, we are focusing on introducing timing reference oscillators for sports watches where portability and battery lifetime are crucial aspects. On the contrary, this trade-off will not be applicable for the global positioning system (GPS). GPS needs frequency reference at least stable to ±1 ppm or even better to handle its operation properly [98]. In this application, a traded-off stability higher than ±1 ppm cannot save more power or get a smaller device size. Based on the performance, oscillators can be categorized into three categories:

- **High performance:** These oscillators are usually built over a high Q (>50,000) resonator – Quartz or MEMS – with adding a PLL. These oscillators offer extreme stability, long- and short-term, and absolute frequency accuracy. On the other hand, they are hard to tune without incorporating a PLL. This consumes more power and occupies a larger area. These types of oscillators are the ideal ones

for different wireless communication transceivers.

- **Low performance:** This category trades off short- and long-term stability and frequency accuracy for a more comprehensive tuning range, cheaper cost, and lower power consumption. CMOS ring oscillators for low frequencies and LC oscillators for high frequencies are considered different kinds of oscillators and can be deployed in microprocessors and microcontrollers.

- **Medium performance:** This type stands in the middle between the high and low performances. It uses low Q (<10000) resonators. It offers a broader tuning range than the high-performance oscillators with lower power consumption but at the expense of a worse jitter and frequency accuracy. These oscillators are used in applications like wireline broadband data transfer [97].

1.5 Motivation and Research Goal

Emerging applications, including internet-of-things (IoT), portable and implantable medical devices, impose stringent power consumption (battery life), cost, and size requirements. For example, through Neuralink, Elon Musk has announced the launch of the fully integrated brain-machine interface (BMI) system, the "Link" project. It is the first neural brain implant, shown in Figure 1.14, intended to directly communicate with mobile and computer [99]. One of the biggest challenges for this project is the enormous amount of small neural brain signals required to be real-time processed simultaneously. Each neural signal needs many electrodes and channels, which demands a radical reduction for the chip size and power consumption per channel. This example shows the future trend in electronic IC design and how miniaturization and power-saving play a key role in it. Time-frequency reference oscillators are pivotal blocks in almost all

electronic systems. Some systems may need more than one reference oscillator, especially with the evolving high data-rate and multi-mode frequency applications. This makes the reference oscillator size and power consumption an issue of major concern. As mentioned earlier, MEMS have become a key alternative to the quartz crystal in reference oscillators, enabling a fully integrated and miniaturized system and a high performance.

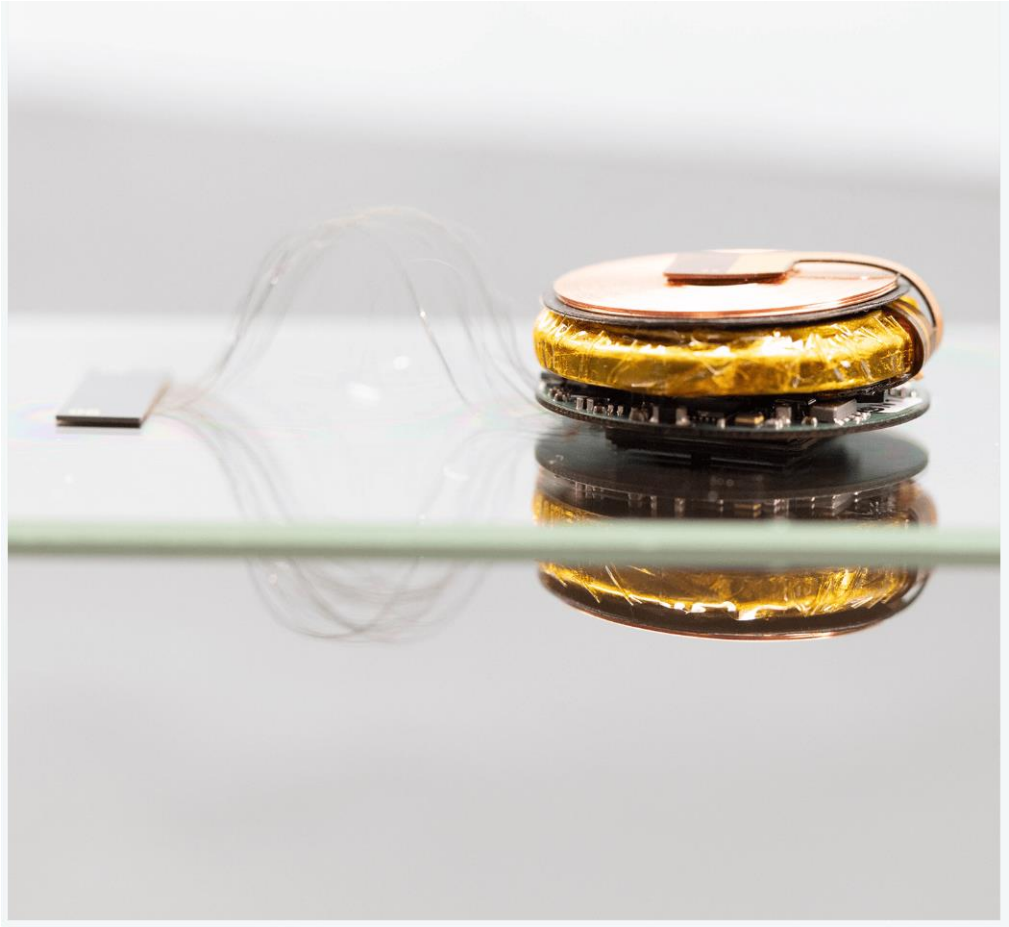


Fig. 1.14 Neuralink fully integrated brain machine interface (BMI) system, the "Link" project [99].

The proposed work aims to design an ultra-low-power, low-noise, compact size

MEMS-based reference oscillator. It focuses on the design of the CMOS interfacing circuits and on introducing an integrated prototype with the MEMS resonator, paving the road for a fully integrated system-on-chip (SoC). It targets frequency generation for low-frequency portable applications such as sports watches, where the size and the battery life are essential design parameters. The targeted work can be summarized as:

- An ultra-low-power, low-noise, small size transimpedance amplifier (TIA) designed to interface with the MEMS resonator, forming an oscillator.
- An ultra-low-power, compact size integer-N phase-locked loop (PLL) fed with the MEMS-based reference oscillator. A careful design for the PLL blocks is required to tackle power consumption and noise performance. New circuit designs and techniques are needed for different blocks to reduce the power consumption and miniaturize the footprint area of the overall system.
- A complete system including the MEMS resonator with the CMOS interfacing circuits, TIA and PLL, to be integrated and tested for different performance specifications including power consumption and size.

1.6 Dissertation Contribution

The main contribution in this work is that starting form a very high quality factor (Q) resonator, which is very competitive among these available in the state-of-the-art, we have explored our different options of what to do to take the full advantage of the high Q of the resonator in implementing high performance oscillators with a very competitive figure of merit (FoM) compared to these existing in the state-of-the-art. We have decided to trade-off a tolerable amount of phase shift across the oscillator's loop for

the sake of saving significant amount of power consumption, that would have otherwise been needed to design for a larger bandwidth while not taking the full advantage of the resonator's high Q. This has been done by designing for the first time a sustaining amplifier with a bandwidth ($f_{cut-off}$) less than the frequency of operation ($f_{Operation}$); $f_{cut-off} < f_{Operation}$. A new design technique that has enabled the implementation of a high-performance oscillator with low power consumption while delivering an acceptable and comparable noise performance. The main objective all along has been to make use of the high Q resonator in minimizing the power consumption and not to solely minimize the noise. What allows the design to achieve very low power consumption with a very competitive FoM is the novel circuit techniques used, making the maximum benefit of the unprecedent very high Q of the MEMS resonator. The main contributions in this work throughout its two parts can be represented as follows:

- *MEMS-Based Oscillator*

  Proposing an ultra-low-power MEMS-based reference oscillator for time-frequency reference applications. An ultra-low-power, low-noise, compact size trans-impedance amplifier (TIA) with tunable gain and duty-cycle is introduced. The TIA design is based on self-cascoding and current-starving techniques to minimize the power consumption and tune the output duty cycle. A robustness test has been carried out to test the proposed TIA sensitivity over process, voltage, temperature (PVT) variations, and transistor mismatches. The TIA was designed and fabricated in a TSMC 65 nm CMOS process technology. An open-loop experimental validation was used to test the TIA's performance. It achieves a tunable gain between 107.6 dBΩ and 118.2 dBΩ with only 143 nW power consumption from a 1 V supply. The duty-cycle of the output waveform can be tuned from 23.9% to 79.7%. The TIA has been interfaced and wire-bonded in a series-resonant oscil-

lator configuration with a 6.89 MHz bulk Lamé-mode MEMS resonator that has a quality factor (Q) of 3.24×10^6. The entire system has been mounted in a small cavity standard package, which significantly reduces the system cost and form factor compared to using of an external quartz crystal as a reference. A closed-loop experimental validation was used to test the performance of the oscillator. The measured values of the oscillator output phase noise are -128.1 dBc/Hz and -133.7 dBc/Hz at 1 kHz and 1 MHz offsets, respectively. This work is published in:

A. Kira, M. Elsayed, K. Allidina, V. P. Chodavarapu, and M. N. El-Gamal, "A 6.89-MHz 143-nW MEMS Oscillator Based on a 118-dBΩ Tunable Gain and Duty-Cycle CMOS TIA," *MDPI - Electronics*, , 2021, no. 21: 2646 (17 pages).

A. Kira proposed the design, performed the needed simulations and measurements, worked on data curation, and prepared the original manuscript draft. All authors participated in the conceptualization and methodology review of this work. M. Elsayed and K. Allidina helped in data curation and reviewed the manuscript draft preparation. V. P. Chodavarapu and M. N. El-Gamal edited and reviewed the manuscript. M. N. El-Gamal supervised the research process. This research work is included in Chapter 2 and Chapter 3 of this dissertation.

- Phase-Locked Loop with input MEMS-Based Reference Oscillator

  Introducing a 110.2 MHz ultra-low-power, compact size integer-N PLL based on the proposed MEMS reference oscillator. It utilizes the 6.89 MHz MEMS-based oscillator as an input reference frequency. A charge-transfer-based charge pump has been adopted to overcome the traditional challenges that face the standard current-based charge pumps. It offers a very low power consumption without the

need for extra matching circuits.

An ultra-low-power, high-resolution phase-frequency detector (PFD) has been designed to achieve low noise performance. Eliminating the reset feedback path used in conventional PFDs has led to a dead-/blind- zone free phase characteristics, which is crucial for low noise applications and wide operating frequency range. The PFD operates up to 2.5 GHz and achieves a linear resolution of 100 ps input time difference (Δt_{in}) without any additional calibration circuits. The linearity of the proposed PFD is tested over a phase difference corresponding to Δt_{in} from 100 ps to 50 ns. At a 1 V supply voltage, it shows an error of $<\pm 1.6\%$ with a resolution of 100 ps and a frequency normalized power consumption (P_n) of 0.106 pW/Hz.

The PLL is designed and fabricated in a TSMC 65 nm CMOS process technology. It has been interfaced with the MEMS-based oscillator by wire bonding the MEMS and CMOS die together. The whole system performance has been tested. The system reports a phase noise of -106.21 dBc/Hz and -135.36 dBc/Hz at 1 kHz and 1 MHz offsets, respectively. It consumes a 6.709 μW at a 1 V supply and occupies 0.1095 mm^2 active CMOS area. This work has been submitted for publication in:

A. Kira, M. Elsayed, K. Allidina, V. P. Chodavarapu, and M. N. El-Gamal, "A 6.7-μW Low Noise Compact PLL with an Input MEMS-Based Reference Oscillator Featuring a High-Resolution Dead-/Blind- Zone Free PFD," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. x, pp. 1–13, 2021.

A. Kira proposed the system design, performed the related analysis and data curation, collected the needed measurements, and prepared the original manuscript

draft. M. Elsayed and K. Allidina helped in preparing the measurement setups and reviewed the manuscript draft. V. P. Chodavarapu and M. N. El-Gamal edited and reviewed the manuscript. M. N. El-Gamal mentored the research progress. This research work is included in Chapter 4 and Chapter 5 of this dissertation.

1.7 Dissertation Organization and Structure

This dissertation is divided into two parts, following the introductory chapter. ***Part I – A 6.89-MHz 143-nW MEMS Oscillator Based on a 118-dBΩ CMOS TIA Featuring Tunable Gain and Duty-Cycle:*** This part covers the oscillator design. **Chapter 2** presents an overview of MEMS oscillators. It discusses the MEMS resonator used in this work, followed by a literature review of the different TIA configurations and topologies. **Chapter 3**, then, covers the proposed TIA architecture, and the closed-loop oscillator integration. It discusses the various trade-offs, the circuit design, and the test setup, reporting the different performance results. ***Part II – A 6.7-μW Low Noise Compact PLL with a MEMS-Based Input Reference Oscillator Featuring a High-Resolution Dead-/Blind- Zone Free PFD:*** This part focuses on the PLL design using the MEMS-based oscillator as an input reference source. **Chapter 4** covers the PLL fundamentals and operation. It investigates the different PLL components providing a PLL system level modeling, frequency response and noise analysis. **Chapter 5** introduces the design of the integer-N PLL with the MEMS-based reference oscillator. It covers the PLL different component's architectures and circuit designs. It demonstrates the whole system integration and assembly technicalities. It presents as well the system testing and measurement setup. Finally,

chapter 6 concludes the whole dissertation and explores the potential future work.

Part I

A 6.89-MHz 143-nW MEMS Oscillator Based on a 118-dBΩ Tunable Gain and Duty-Cycle CMOS TIA

Chapter 2

System Overview and MEMS Resonator

This chapter provides an overview of the MEMS-based oscillator's system. It describes the MEMS resonator used and its various features. The electrical equivalent model for MEMS is introduced and explained. The chapter also shows and briefly discusses different TIA configurations, topologies, and features.

2.1 Introduction

A MEMS resonator behaves as a frequency selective network. It can be modeled, in its simplest form, with an RLC circuit. It gets stimulated/driven by a voltage signal (v_{drive}) to produce an output current (i_{sense}). Hence, a transimpedance amplifier (TIA) is responsible for sensing, amplifying, and converting this output current into a voltage signal. Figure 2.1 shows the block diagram of a MEMS-based oscillator system, where a transimpedance amplifier (TIA) and a MEMS resonator are connected in a positive feedback loop. R_M, C_M, L_M, C_f, and C_P are the MEMS resonator's electrical

model motional resistance, motional capacitance, motional inductance, feedthrough capacitance, and parasitic capacitance, respectively.

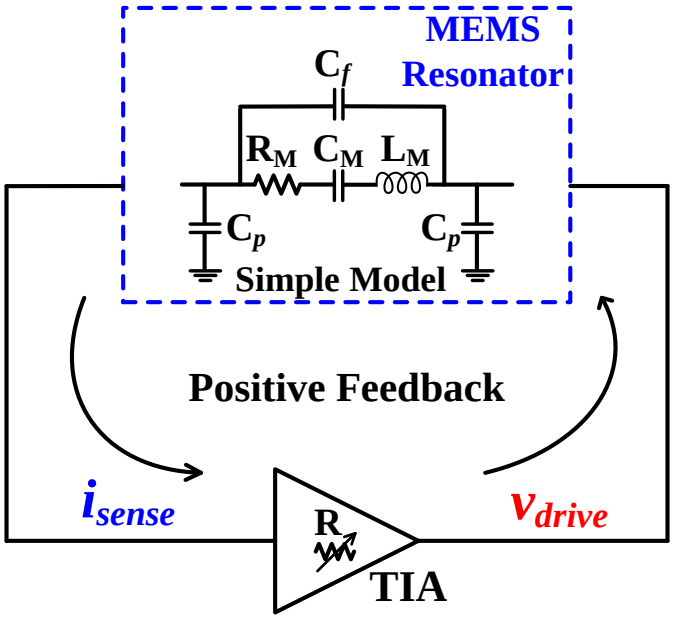


Fig. 2.1 MEMS-based series resonant oscillator.

To sustain oscillations in a positive feedback system, two main conditions, known as the "Barkhausen criteria," are required:

- **The total loop gain should be ≥ 1**

  This implies that the forward gain of the TIA overcomes the resonator series losses represented by R_M.

- **A low phase shift near the oscillation frequency (f_o), theoretically 0°**

  This results in the trade-off between the need for a high gain-bandwidth product (GBW) and low power consumption.

Typically, MEMS resonators are actuated by either piezoelectric or capacitive transduction mechanisms. Piezoelectrically-transduced resonators have smaller R_M (less

losses), but require specialized fabrication technologies that are not available in many standard semiconductor foundries. Capacitively-transduced resonators have a higher R_M, in the range of tens of kΩ, but are more suited for monolithic CMOS integration [100] and these devices offer high-quality factor (Q), small size, and good stability [101, 102, 103, 104, 105, 106]. Capacitive MEMS resonators require a high gain TIA to compensate for the high R_M. Further, a low phase shift near the oscillation frequency (f_o) is needed to sustain oscillation. This results in the trade-off between the need for a high gain-bandwidth product and low power consumption. Later, in Chapter 3, the design of an ultra-low-power, low-noise TIA with a tunable gain and duty-cycle is introduced.

Fig. 2.2 shows the MEMS-based oscillator block diagram. The oscillator is based on a differential bulk square resonator connected in a positive feedback loop with the TIA. The oscillator is then to be connected to an integer-N PLL to synthesize a higher output frequency from the proposed input MEMS-based reference oscillator. The focus of this part is the MEMS-based oscillator (not the PLL).

2.2 Bulk Lamé-Mode Square MEMS Resonator

The MEMS resonator used in this work is a bulk Lamé-mode wafer-level silicon resonator vacuum-encapsulated at 10 mTorr, fabricated using the MEMS Integrated Design for Inertial Sensors (MIDIS) technology, discussed in detail in [107]. MIDIS is a pure-play commercial process provided by Teledyne DALSA Semiconductor Inc. [108]. It offers a low-leakage and a vacuum level ultra-clean encapsulation. In addition, it does not need release etch holes compared to the developed process by SiTime Corporation, thus less fabrication steps [109].

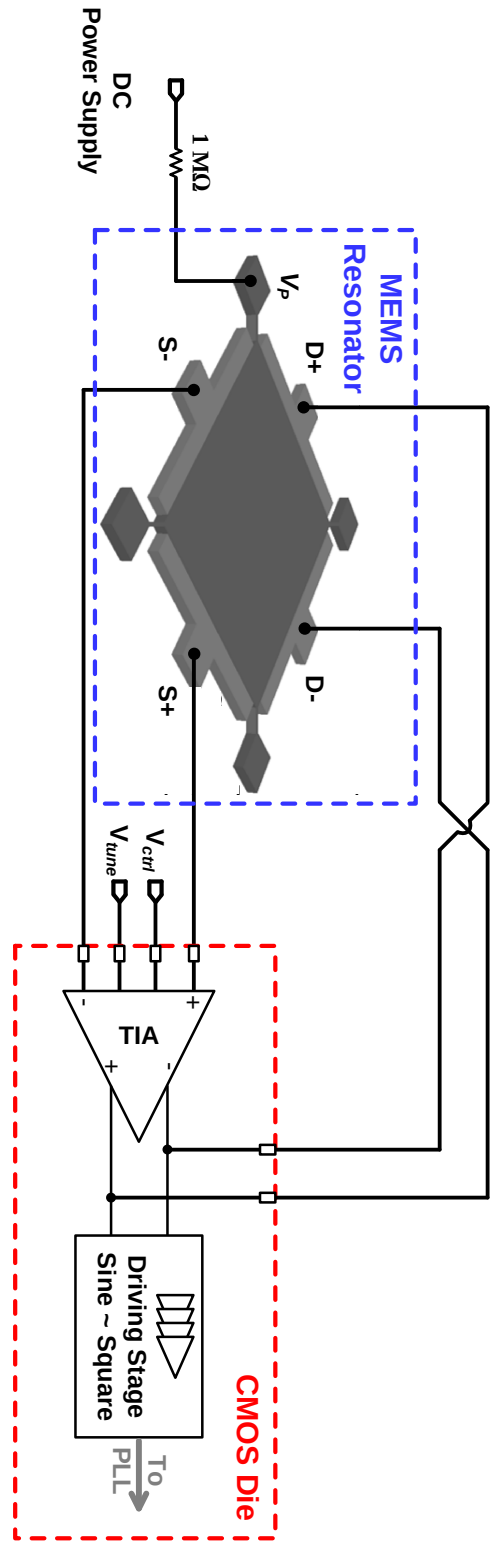


Fig. 2.2 Proposed MEMS-based oscillator block diagram.

The square bulk Lamé-mode resonator design has a length of 600 μm, a width of 600 μm and a height of 30 μm. It has a differential actuation and sensing scheme which helps in reducing the feedthrough signals and the noise. The design includes four straight anchor supports, one on each corner. Each anchor has a length of 60 μm, a width of 10 μm and a height of 30 μm. The transduction gap size is the minimum allowed by the MIDIS process; a 1.5 μm gap size. Although it is relatively wide for electrostatically transduced resonators, the device layer thickness, 30 μm, permits a large transduction area. This keeps a relatively low motional resistance (R_M) [107]. A detailed analysis of the Lamé-mode resonator is proposed by Majjad et al. in [110].

At a polarization/bias voltage (V_P) of 40 V, the measured resonance frequency (f_r) is 6.8953 MHz, with a Q factor of 3.24×10^6. This leads to a frequency-quality factor (f-Q) product of 2.23×10^{13} Hz. Figure 2.3 shows the measured frequency response of the resonator at a V_P of 40 V [111].

2.3 MEMS Resonator Electrical Equivalent Model

The MEMS resonator is an electromechanical device. An electrical voltage signal drives the MEMS resonator causing a mechanical vibration of its structure, which produces an electrical current signal. An electrical equivalent model for the MEMS is needed to properly design the interfacing circuits to drive and sense the MEMS resonator. The detailed dynamic response of the resonator is studied in [112]. The motional resistance (R_M), motional inductance (L_M), and motional capacitance (C_M) needed to model the MEMS resonator electrically can be estimated using Equations (2.1 - 2.3) [107]:

$$R_M = \frac{d^4\sqrt{mk}}{A^2 Q \varepsilon_o^2 V_P^2} \tag{2.1}$$

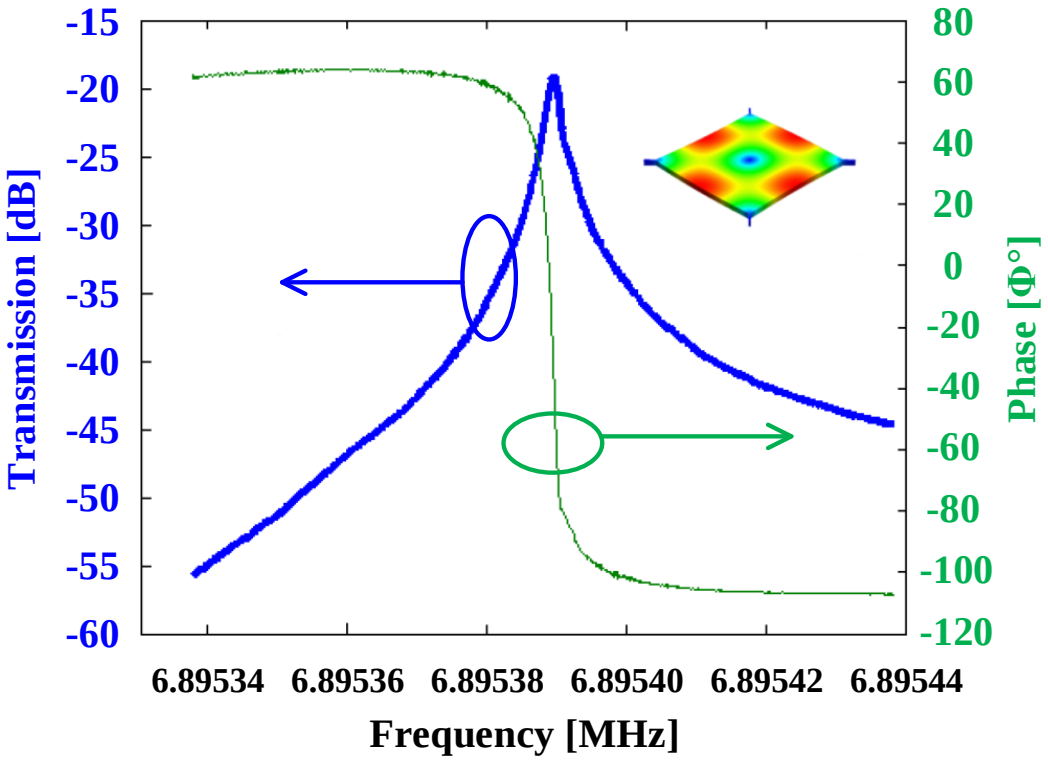


Fig. 2.3 Measured MEMS electrical transmission (S21): the blue curve is the magnitude (left Y-axis), and the green curve is the phase (right Y-axis) [107].

$$L_M = \frac{d^4 m}{A^2 \varepsilon_o^2 V_P^2} \tag{2.2}$$

$$C_M = \frac{A^2 \varepsilon_o^2 V_P^2}{d^4 k} \tag{2.3}$$

where d is the transduction gap, m is the effective mass of the resonator, k is the effective spring constant, A is the transduction area, Q is the quality factor, ε_o is the free space permittivity, and V_P is the polarization voltage. R_M, L_M, and C_M of the resonator, connected to 50 Ω ports, can be estimated as well from the measured transmission (S_{21}) parameter using Equations (2.4 - 2.6) [107]:

$$R_M = \frac{v_{drive}}{i_{sense}} = 50 \times 10^{\frac{InsertionLoss}{20}} \tag{2.4}$$

$$L_M = \frac{QR_M}{2\pi f_r} \tag{2.5}$$

$$C_M = \frac{1}{2\pi f_r Q R_M} \tag{2.6}$$

v_{drive} is the MEMS input drive voltage, i_{sense} is the MEMS output sense current, and f_r is the resonance frequency.

Figure 2.4 shows the fitted linear RLC electrical equivalent model extracted by measuring the output of the resonator at 6.89 MHz, while being biased at a V_P of 40 V. The resonator is capacitively transduced; hence, the vibration is not affected by the interfacing circuits. The feedthrough capacitance (C_f) has also been calculated from the MEMS structure and added to the model.

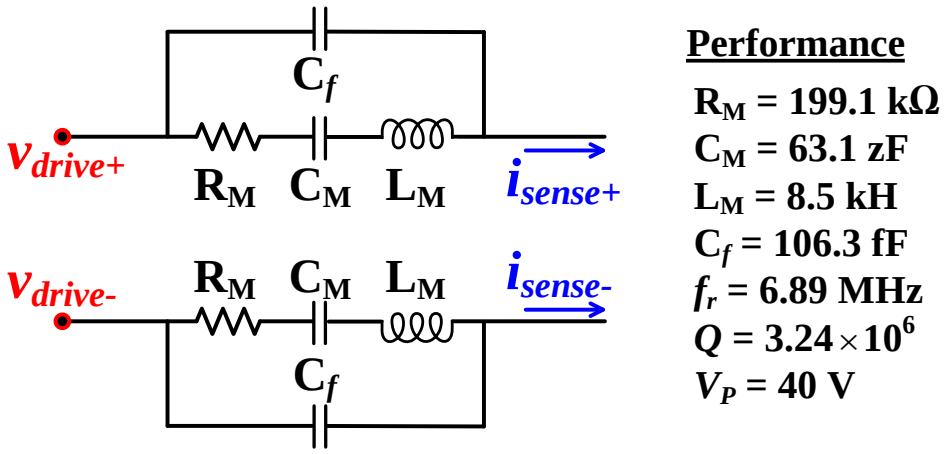


Fig. 2.4 Extracted RLC electrical equivalent model from resonator measurements.

2.4 Transimpedance Amplifier Configurations and Topologies

The transimpedance amplifier (TIA) is a current-to-voltage amplifying convertor. Its gain is defined as the ratio of its output voltage to its input current, expressed in dBΩ. Accordingly, very low input and output impedances are required to allow for a maximum input current transfer into the TIA and a maximum output voltage transfer out from the TIA. Fig. 2.5 shows simple diagrams of different TIA configurations and topologies.

2.4.1 TIA Configurations

There are two main general configurations used to realize a TIA: the open-loop configuration, and the closed-loop (feedback) configuration.

Open-Loop TIA Configuration

The open-loop TIA configuration amplifies the input current using a current amplifier (A_I), then converts it to an output voltage by passing the output current through a

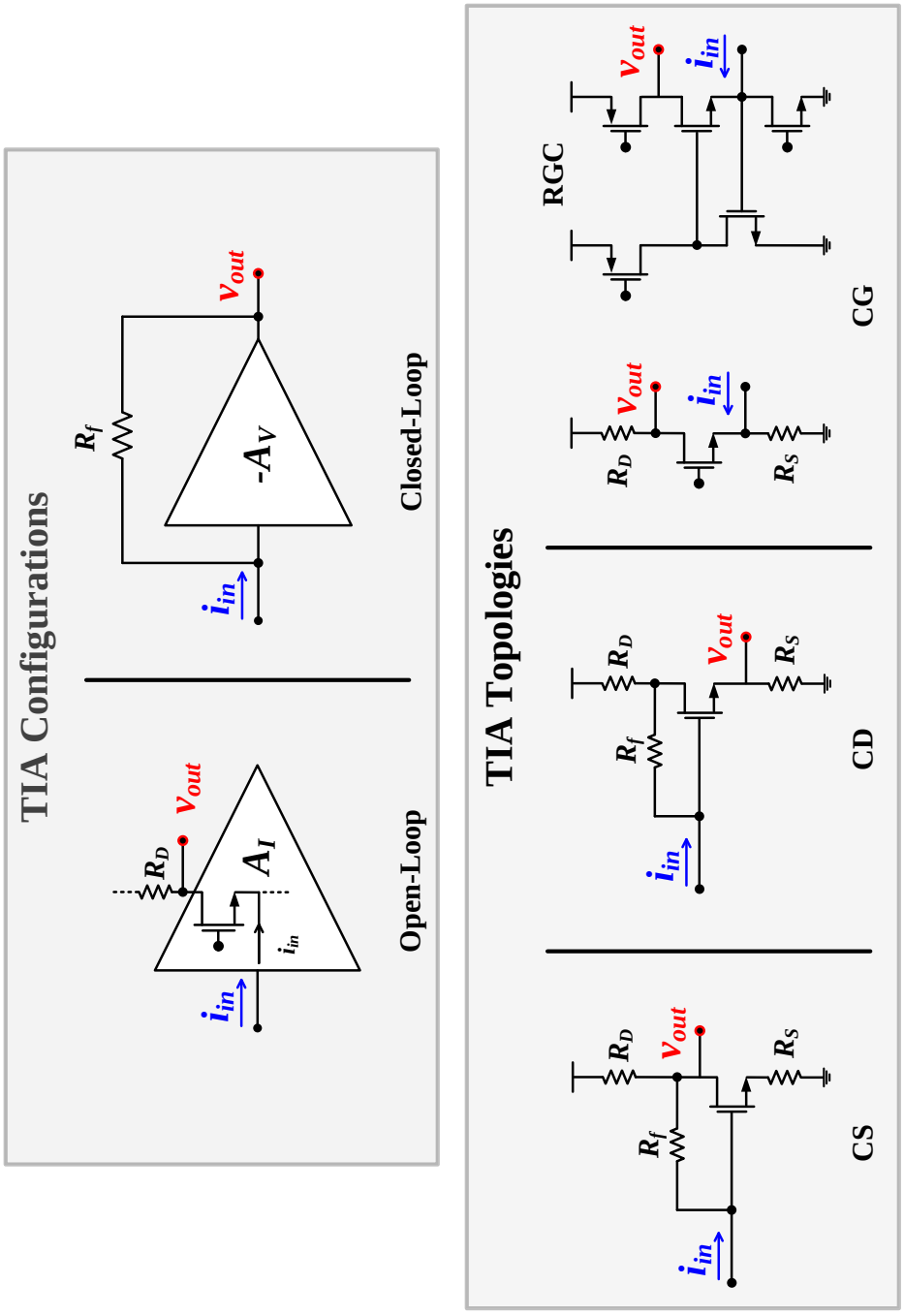


Fig. 2.5 Different TIA configurations and topologies.

resistive load. Although open-loop TIAs may offer a lower power consumption than closed-loop ones, they have a higher noise that cannot be tolerated for some applications [113].

Closed-Loop (Feedback) TIA Configuration

On the other hand, the closed-loop configuration offers lower noise and a more flexible gain-bandwidth (GBW) trade-off relationship. This makes it the most used configuration in micromechanical oscillators. This configuration is based on a voltage amplifier (A_V) with negative shunt-shunt feedback from the output to the input. The shunt-shunt feedback lowers the system input and output impedances by the loop gain, which helps in increasing the TIA's bandwidth (BW). In addition, the amplifier's input-referred noise is reduced by the square of the feedback resistor, bringing an extra advantage for low phase-noise MEMS-based oscillator applications.

2.4.2 TIA Topologies

Different topologies, including common-source (CS), common-gate (CG), and common-drain (CD), are used to realize the single-stage or multistage amplifier. The CG topology, such as the regulated-cascode (RGC) amplifier, inherently, has low input impedance but suffers from high input-referred noise. This makes the CG topology unsuitable for low-phase noise and low-power applications [26]. The CD topology offers a low output impedance but exhibits poor linearity and low dynamic range, resulting in higher phase noise. The CS topology provides a larger output swing and can be operated from a lower supply which further helps in reducing the power consumption. In addition, the dynamic range is improved due to the higher output swing resulting in a lower phase-noise floor. All these features make the closed-loop configuration, negative

shunt-shunt feedback CS topology better suited for capacitive MEMS resonators, and an optimum choice for our application. Table 2.1 and Table 2.2 briefly summarize the mentioned features of the different TIA configurations and topologies.

Table 2.1 Different TIA configurations.

Open-Loop	Closed-Loop
• Lower power. • Higher noise, not tolerable by some applications.	• Lower noise. • Flexible GBW trade-off. • Lower input/output impedance; hence, larger BW • Reduced input-referred noise

Table 2.2 Different TIA topologies.

Common Gate (CG)	Common Drain (CD)	Common Source (CS)
• Low input impedance. • High input-referred noise. • Not for low-phase noise applications. • Not for low-power applications.	• Low output impedance. • Poor linearity. • Low dynamic range. • High phase noise.	• Large output swing • Wider dynamic range. • Lower phase-noise floor. • Low supply operation • Lower power consumption.

Chapter 3

Transimpedance Amplifier and Closed-Loop Oscillator

A 6.89 MHz MEMS oscillator is presented based on a high Q bulk Lamé-mode MEMS resonator and ultra-low-power, low-noise TIA. A design methodology is proposed to achieve low power consumption and low phase noise, demonstrating the efficacy of using a high (Q) resonator in reaching an ultra-low power design for the CMOS sustaining circuitry. The novel use of the self-cascoding and current-starving techniques in the TIA design has been introduced to minimize the power consumption and tune the duty-cycle of the output signal. Duty-cycle tuning is an added feature used by other applications requiring a tunable duty-cycle, including switched-capacitor filters [114] and pulse-width control [115]. Applications like envelope tracking power amplifiers (ETPA) can make use of a wide duty-cycle tuning range. ETPA are based in their design on DC-DC converters, as Buck converters, on which the design is mainly dependent on tuning the duty-cycle of the input frequency feeding the switching transistors in the converter. The fully integrated and packaged oscillator solution at this frequency achieves a very

competitive performance in terms of power consumption and phase noise. The entire mounted system in a small cavity standard package significantly reduces the system cost and form factor compared to using an external quartz crystal as a reference resonator.

This chapter discusses the MEMS-based oscillator showing the resonator and the sustaining amplifier circuit used in forming the oscillator. It presents the proposed methodology, TIA circuit design, and noise analysis. It covers the performance and robustness of the proposed TIA circuit. It shows the experimental validation used to test the stand-alone TIA performance, the measurement results of the overall oscillator system, and provides a comparison with the state-of-the-art designs.

3.1 Proposed Methodology and TIA Circuit Design

For an RLC circuit in a closed loop with a TIA, as shown in Figure 2.1, the total phase in the loop at the frequency of oscillation (f_o) is, theoretically, zero. For a TIA phase shift (φ), where $|tan\varphi| \ll Q$, equations (3.1) and (3.2) from [116] can be applied:

$$f_o \approx f_r(1 + \frac{tan\varphi}{2Q}), \tag{3.1}$$

where f_r is the resonance frequency. A unity loop gain should be maintained at f_o; hence a TIA gain (R_{TIA}) is required as:

$$R_{TIA} \geq \frac{R_M}{|cos\varphi|}. \tag{3.2}$$

Thus, for a very high Q MEMS resonator as the one used here, which has a Q of 3.24×10^6, a phase shift of -80° changes f_o by only 2 ppm, which meets the requirements here. Equations (3.1) and (3.2) show that a tolerable phase shift can be used to save

significant power that would have otherwise been needed to obtain a large bandwidth while not taking full advantage of the high Q of the resonator. Thus, as shown in Figure 3.1(a), the proposed TIA uses three distinct features: (a) self-cascoding, (b) current-starving, and (c) long transistor channel length (L). Figure 3.1(b) shows the self-cascoding technique that is used for low voltage operation. It reduces the channel length modulation effect while offering a high output swing and DC gain [117].

The self-cascode structure consists of two transistors forming a composite transistor that mimics the same DC characteristics of a single long-channel transistor with a uniform width. It introduces two advantages over its DC-equivalent uniform-width single transistor: (a) a substantial area-saving and (b) a higher cut-off frequency [118]. M_2 in Figure 3.1(b) always operates in the triode region, while M_1 can be operating either in the triode or the saturation regions. At the edge of saturation, the composite drain-source voltage ($V_{DS_{sat}-composite}$) can be expressed as:

$$\begin{aligned} V_{DS_{sat}-composite} &= V_{DS_{sat}1} + V_{DS2} \\ &= V_{OV1} + I_{D2}R_{DS2}, \end{aligned} \tag{3.3}$$

where, V_{OV1} is the overdrive voltage of M_1. R_{DS2} is the on-resistance of M_2 while operating in the triode region. This implies that the V_{DS2} is very small and makes no discernible difference in the composite V_{DSsat} compared to that of its equivalent single transistor. This qualifies the self-cascode structure for low power and low voltage applications compared to regular-cascode structures that need a higher operating voltage [119, 120]. The composite achieves a larger effective L – lower output conductance – by stacking smaller, shorter-length transistors. Assuming $L_1 = L_2$ and $W_1 = mW_2$,

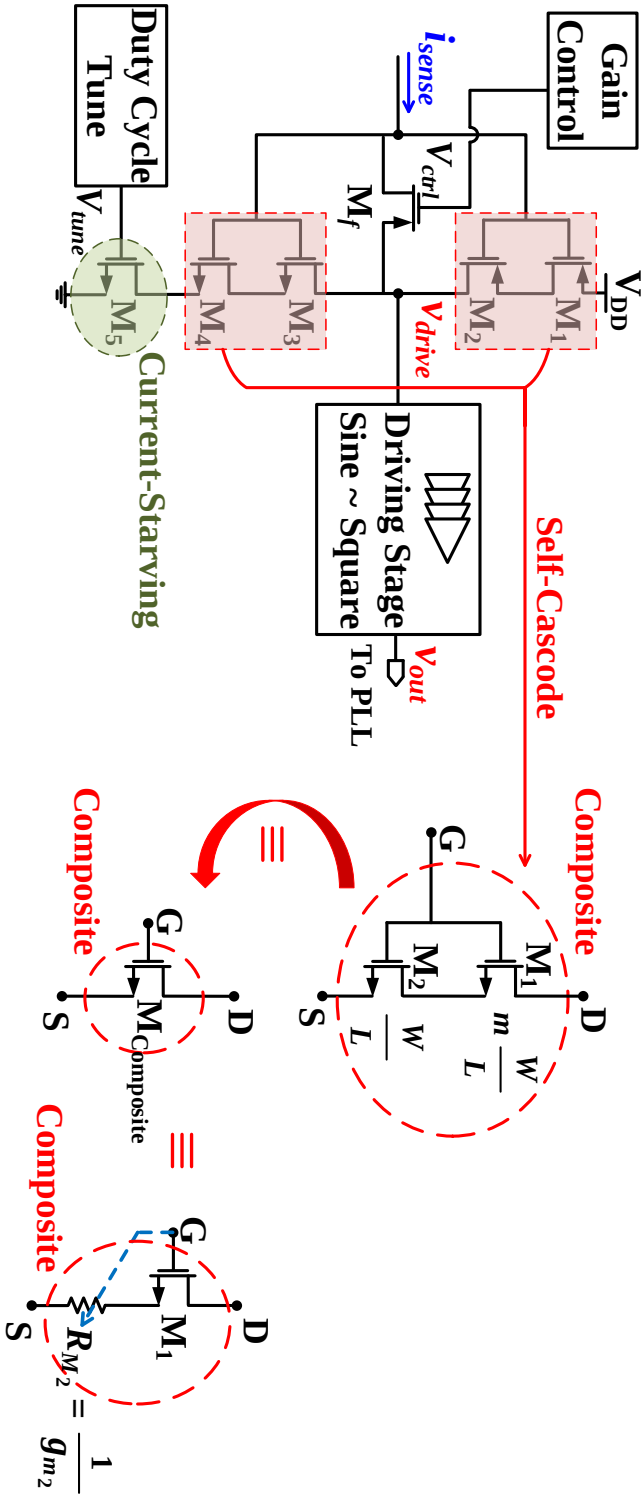


Fig. 3.1 Proposed TIA circuit diagram: (a) one half of the differential signal path for simplicity and (b) self-cascode composite structure.

the composite effective aspect ratio is expressed as:

$$\frac{W}{L}|_{composite} = \frac{1}{m+1}.\frac{W}{L}|_1 = \frac{m}{m+1}.\frac{W}{L}|_2. \tag{3.4}$$

From a layout perspective in advanced CMOS process technology nodes, most foundries, in their process design kits (PDKs), recommend building a long gate transistor length by stacking short gate transistors. This improves matching and the uniformity of the layout, which results in a more compact area by reducing the use of extra dummy layout cells used to ensure transistor layout uniformity post fabrication. In addition, it is more precise in terms of the device model introduced by the PDK, as the device models may become inaccurate for very long gate lengths. The sum of the area footprints of M_1 and M_2 is smaller than that of the equivalent simple transistor. In addition, stacking reduces the leakage when the transistors are off. A stack of 2-transistors has 10× reduced leakage than that of an equivalent single transistor. This helps in reducing power dissipation. For equal chip areas, the voltage-gain (A_V) relationship between the regular-cascode, the self-cascode, and a simple transistor is given by:

$$A_{V_{regular-cascode}} > A_{V_{self-cascode}} > A_{V_{simple-transistor}}. \tag{3.5}$$

Although the regular cascode has a higher A_V, this comes at the expense of a higher voltage drop (less headroom) and more power consumption.

The current starving technique controls the charging/discharging current flow to tune the duty-cycle, offering a better noise performance [121, 122] and reducing power consumption. Finally, increasing the transistor channel length helps in reducing the output phase noise and power consumption.

3.2 Noise Analysis

In MEMS oscillators, there are two main noise sources; (a) thermal noise from the resonator represented by $4k_BT/R_M$, where T is the absolute temperature and k_B is the Boltzmann constant, and (b) the TIA's input-referred current noise $\overline{i_n^2}$. From [123, 116, 105], for $|tan\varphi| \ll Q$ and at low frequency-offsets (Δf), close to the carrier, the phase noise will be low as the resonator high Q shapes it, and it is given by:

$$\mathcal{L}(\Delta f)|_{Resonator} = \frac{1}{v_{drive}^2}\frac{K_BTR_M}{Q^2}\frac{f^2}{\Delta f^2}, \tag{3.6}$$

the phase noise floor is proportional to R_M^2 and $\overline{i_n^2}$, and can be expressed as:

$$\mathcal{L}(\Delta f)|_{Floor} = \frac{1}{v_{drive}^2}\overline{i_n^2}\frac{R_M^2}{\Delta f}, \tag{3.7}$$

where v_{drive} is the resonator input driving voltage thus, it is essential to minimize $\overline{i_n^2}$. The shunt-shunt negative feedback reduces the amplifier's input-referred noise power spectral density by the square of the feedback resistance and helps compensate for the direct proportionality of the noise floor to R_M^2. Neglecting the flicker noise, the thermal input-referred current noise for the design proposed here can be expressed as,

$$i_n^2 = 4k_BT[\frac{\omega^2C_{in}^2\gamma}{g_{m1}+g_{m4}} + \frac{1}{R_{ctrl}}], \tag{3.8}$$

where, k_B is the Boltzmann constant, T is the absolute temperature, ω is the angular frequency, C_{in} is the TIA total input capacitance, γ is a noise coefficient that depends on the transistor channel length (L), g_{m1} and g_{m4} are the transconductances of M_1 and M_4, respectively, and R_{ctrl} is the shunt-shunt feedback resistor realized by

transistor M_f.

3.3 System Performance and Robustness

3.3.1 Specifications and Performance

Enough high gain is required to sustain oscillations to compensate for the MEMS resonator losses modeled with the electrical model's resonator motional resistance (R_M). The used bulk Lamé-mode resonator has an R_M of 199.1 kΩ which corresponds to a 105.97 dBΩ loss. The designed TIA should have at least a gain of 105.97 dBΩ to compensate for the resonator losses. Practically, at start-up, a higher gain may be needed to start the oscillation, where having a tunable gain feature becomes valuable.

The proposed TIA is developed in the TSMC 65 nm CMOS process technology. An open-loop simulation test is performed while loading the TIA with the MEMS resonator electrical model to check the TIA gain (G_{TIA}) and performance. The designed TIA has a minimum gain of 107.6 dBΩ, covering the minimum required gain to compensate for the resonator losses and any extra parasitic losses. The gain is tunable between 107.6 dBΩ and 118.2 dBΩ. The duty-cycle of the output waveform, tested after the driving stage, is tunable between 23.9% and 79.7%.

3.3.2 Robustness

To test the sensitivity of the proposed TIA circuit over transistor mismatches, a Spectre post-layout (*conservative*-type) simulation was carried on the circuit shown in Figure 3.1(a) using a Monte-Carlo analysis with a number of runs N=500. Figure 3.2(a) shows the histogram of the TIA's maximum gain; $G_{TIA-Max}$=118.2 dBΩ. It reports a mean of 118.17 dBΩ and a standard deviation (std) of 0.226 dBΩ. For the TIA's minimum

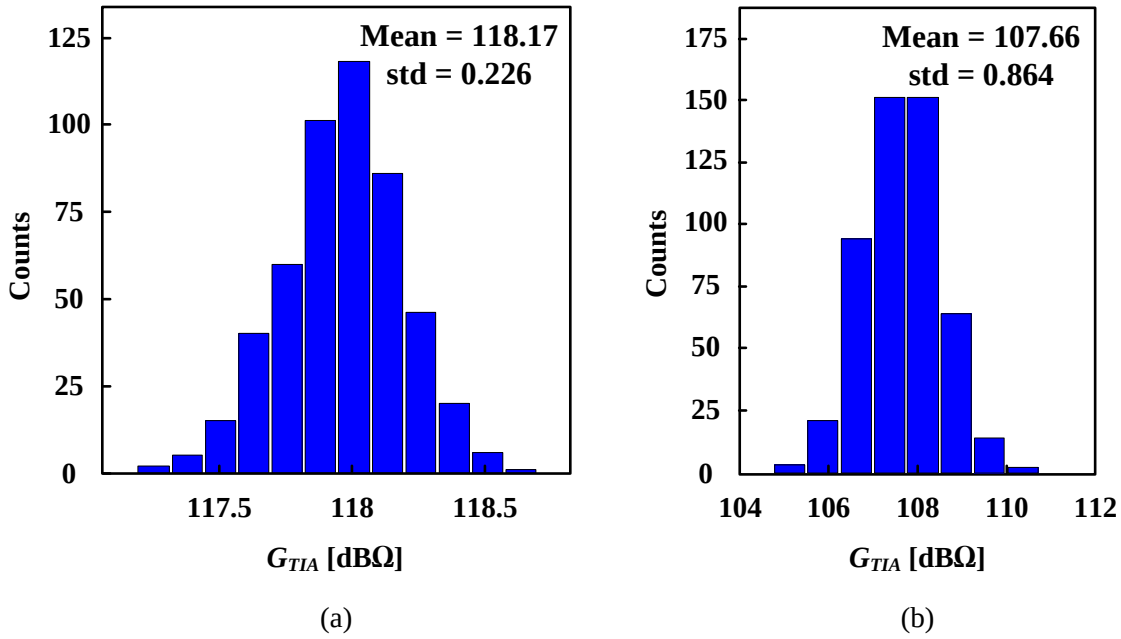


Fig. 3.2 Monte-Carlo histograms of the proposed TIA (N=500): (a) $G_{TIA-Max}$=118.2 dBΩ and (b) $G_{TIA-Min}$=107.6 dBΩ.

gain; $G_{TIA-Min}$=107.6 dBΩ, as shown by the histogram in Figure 3.2(b), the mean and the std are 107.66 dBΩ and 0.864 dBΩ, respectively. Figure 3.3 shows the post-layout TIA gain over three process corners (FF, TT, SS), supply variation range (1V±0.05V), and temperature between (-10℃→ 80℃) to test the design robustness over process, voltage, and temperature (PVT) variations. The graph indicates a maximum gain tuning range of 10.6 dBΩ under the TT corner and a minimum gain tuning range of 9.3 dBΩ under the SS corner.

3.4 Experimental Results

To validate the fabricated design, the CMOS circuits have been tested in an open-loop configuration while considering all parasitic loads to validate the TIA open-loop performance. Then, closed-loop testing was performed after wire bonding the CMOS

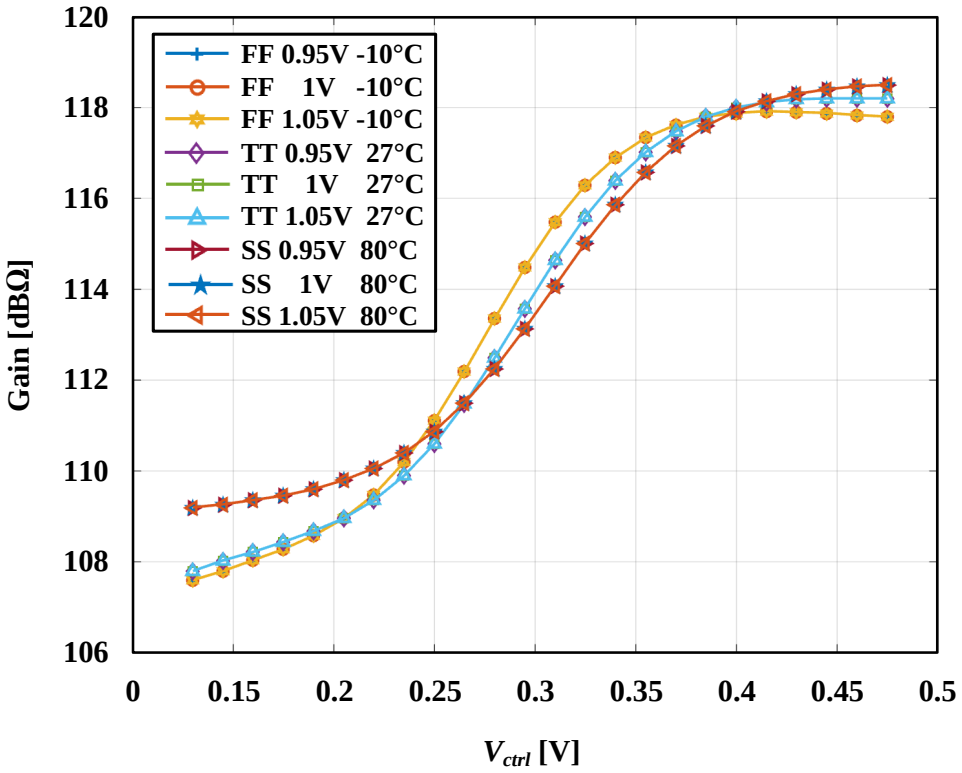


Fig. 3.3 The TIA gain control under PVT variations.

circuits to the MEMS resonator to test the closed-loop feedback oscillator performance. Five CMOS dies have been tested in total, all the results are within 0.3% of the TT corner performance, which is in a good agreement with our Monte-Carlo simulations.

3.4.1 Open-Loop Validation

The stand-alone performance of the proposed TIA has been tested separately, without the MEMS resonator. Figure 3.4(a) shows the micrograph of the fabricated die highlighting the TIA block. The total active TIA CMOS area is 150.29 μm^2 (12.38 μm $\times$ 12.14 μm). The prototype CMOS die is assembled in an 80-pin ceramic quad flat pack (CQFP) package and mounted on a custom 4-layer printed circuit board (PCB) as shown in Figure 3.4(b). The test board includes SMA connectors for the input/output signals, coupling capacitors (1 uF) at the input signals to filter out the DC component, and a voltage regulator (Analog Devices ADP1707ARDZ-1.2-R7) to regulate the input supply from a DC power supply source (Agilent E3646A). In addition, all power nets are decoupled with a network of decoupling capacitors (10nF, 100nF, 1μF) connected in parallel and in ascending order from the integrated circuit (IC) package lead. There are other components on the PCB – Figure 3.4(b) – that are not related to this specific TIA test.

A measurement setup has been built to test the TIA in an open-loop configuration, without being connected to the MEMS resonator. First, we have built a post-layout simulation environment on Cadence that only includes the TIA in an open-loop configuration. Second, we modeled all the loading and the parasitic effects added by the measurement equipment and the PCB in the simulation environment to fairly compare the simulation results with the measurements. This validates the TIA performance and assures proper functionality when bonded to the MEMS resonator in a closed-loop

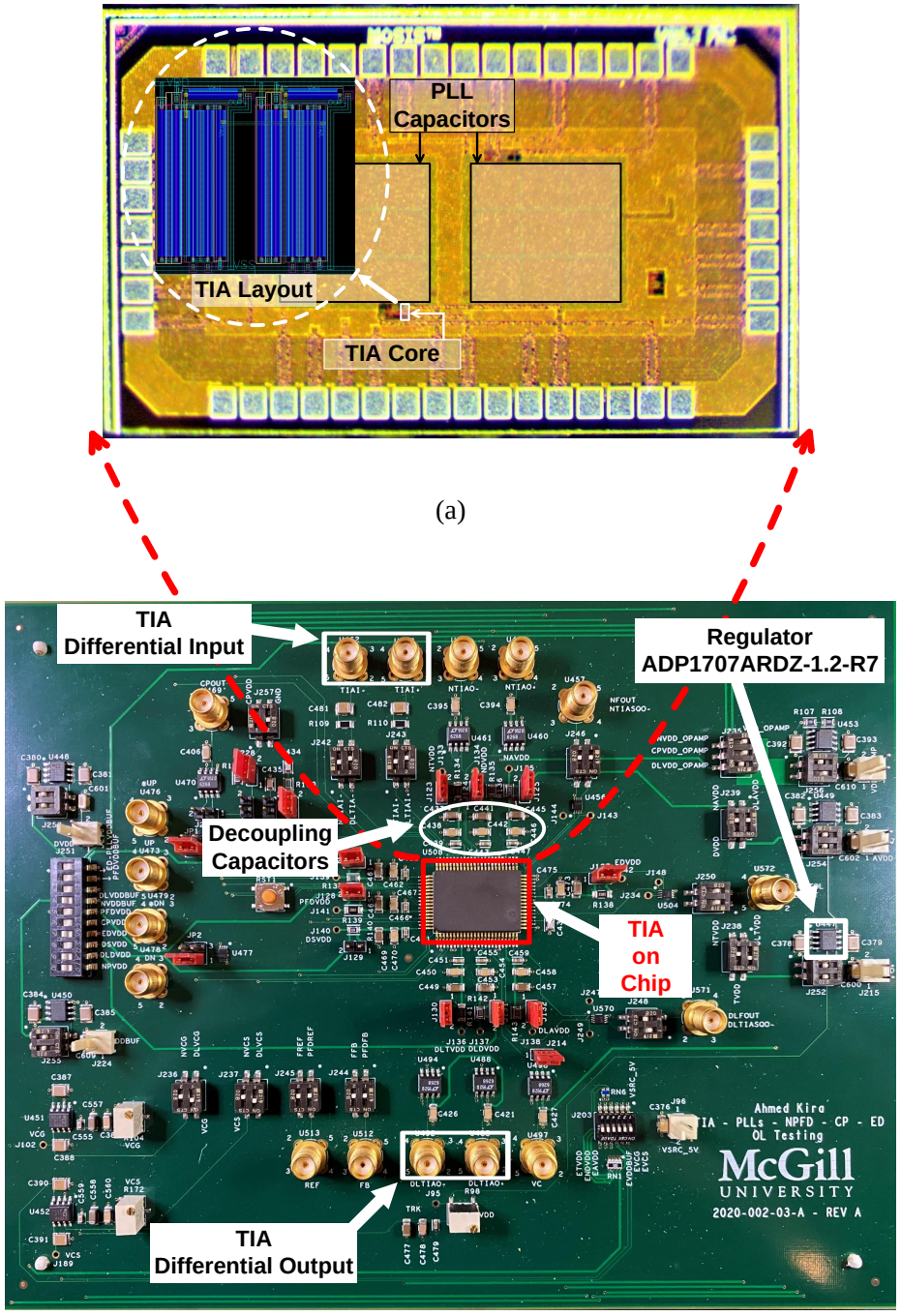


Fig. 3.4 (a) Fabricated die micrograph and (b) photograph of the PCB used to test the TIA.

feedback configuration.

To mimic the MEMS resonator, an excitation voltage at a frequency of 6.89 MHz was used. A resistor ($R_{v\sim i}$) was placed in series with the TIA input to convert this excitation voltage to a current in the range of the MEMS resonator sensed current. Figure 3.5 depicts the testing method, including all sources of parasitics. The test has

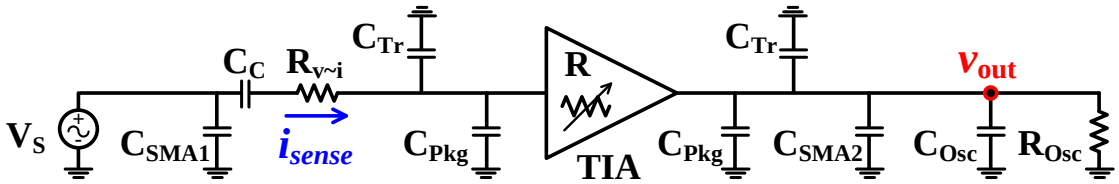


Fig. 3.5 TIA open-loop test method, showing one half of the differential signal path for simplicity.

been applied in both the Cadence simulation environment and the measurement setup. Figure 3.6 shows the matching of the transient differential outputs obtained from both the simulation and the measurement.

The amount of parasitics seen by the TIA on the PCB while connected to the measurement equipment is very large compared to when only connected directly to the MEMS resonator. When the TIA is connected to the MEMS resonator in a closed feedback loop – which is the case in the end application – it is only loaded by less than 0.5 pF parasitic capacitance. On the other hand, in this PCB measurement setup, as will be shown shortly, the total parasitic capacitances loading the TIA output and input are 74.85 pF and 105.4 pF, respectively. Adding these loads in the Cadence simulation model will decrease the output signal amplitude by a considerable amount. This is expected as the TIA is designed to interface directly with the MEMS resonator, where parasitics are significantly reduced. By replicating the PCB parasitics in our Cadence model simulations, we can directly compare the results to see if the TIA is performing

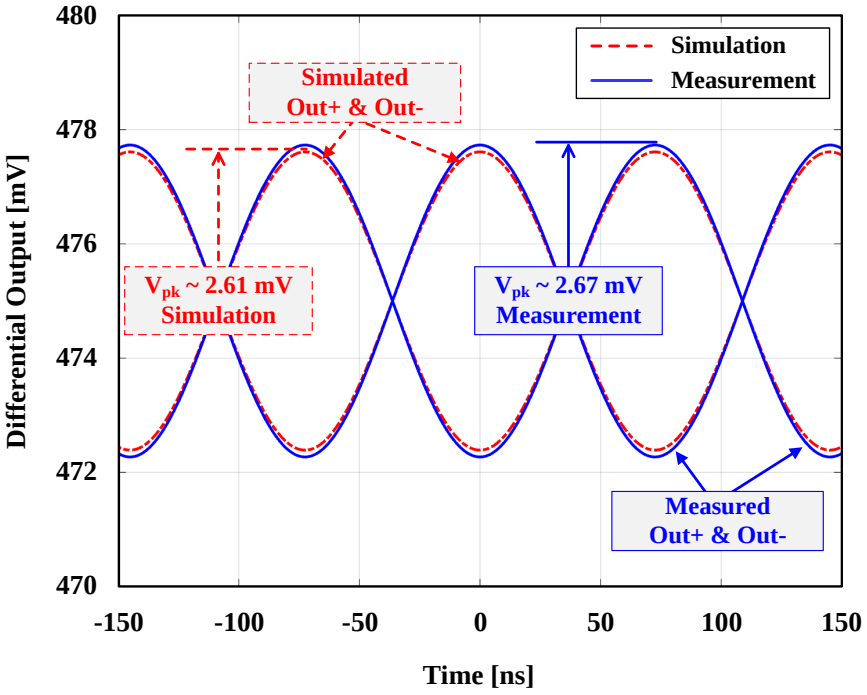


Fig. 3.6 TIA differential output transient response, both measured and simulated.

as expected. Table 3.1 shows the list of loads and parasitic effects. The capacitances

Table 3.1 Loading and Parasitic Capacitances.

Parasitic/Load Type	Symbol	Value
Oscilloscope	C_{Osc} R_{Osc}	11 pF 1 MΩ
SMA Connector	C_{SMA1} C_{SMA2}	104.15 pF 62.6 pF
Package Lead	C_{Pkg}	0.25 pF
PCB Trace	C_{Tr}	1 pF

of the used SMA connector cables (C_{SMA1}, C_{SMA2}) have been measured using a bench LCR/ESR meter (BK Precision 889B). The PCB traces capacitances and the CQFP package lead capacitance have been estimated based on [124] and [125], respectively. The oscilloscope loading resistance (R_{Osc}) and capacitance (C_{Osc}) were found in the oscilloscope (Agilent InfiniiVision DSO-X 2004A) manual [126]. After de-embedding the loading effects of the parasitics, the TIA performance has been captured. Figure 3.7 shows the measured transimpedance gain of the TIA. It reports the maximum gain at the resonance frequency (f_r). The corresponding phase shift is -75.41°, which is the maximum phase shift that can occur. It is within the acceptable range as discussed and shown earlier using (3.1) and (3.2). For lower gain, the phase shift will decrease.

It is worth noting that, in this work, the main objective all along has been to minimize power consumption while delivering an acceptable noise performance. The goal was not to solely minimize noise.

After an oscillator starts up, comes equation (3.1) to determine the noise performance. The effect of the phase shift, namely how far it occurs away from the resonator peak, is directly reflected in the phase noise performance. What permits the design here to achieve very low power consumption is the very high Q-factor of the resonator used.

If we were to solely target noise minimization with this high Q-factor MEMS resonator, instead of minimizing power, we could have achieved a much better noise performance than what we report here, but this obviously would have come at the expense of more power consumption and may have affected the overall figure of merit (FoM) achieved. This is a classic example of design parameters "*balancing,*" based on the resources at hand and on the ultimate target objectives of the work – minimize power consumption while delivering a competitive FoM.

The measured tunable TIA gain with V_{ctrl} is shown in Figure 3.8. It can be tuned between 107.9 dBΩ and 118.1 dBΩ. Figure 3.9 shows that the duty-cycle is tunable between 23.25% and 79.03%. All results are in good agreement with the simulations. The actual measurement setup and its block diagram are depicted in Figure 3.10.

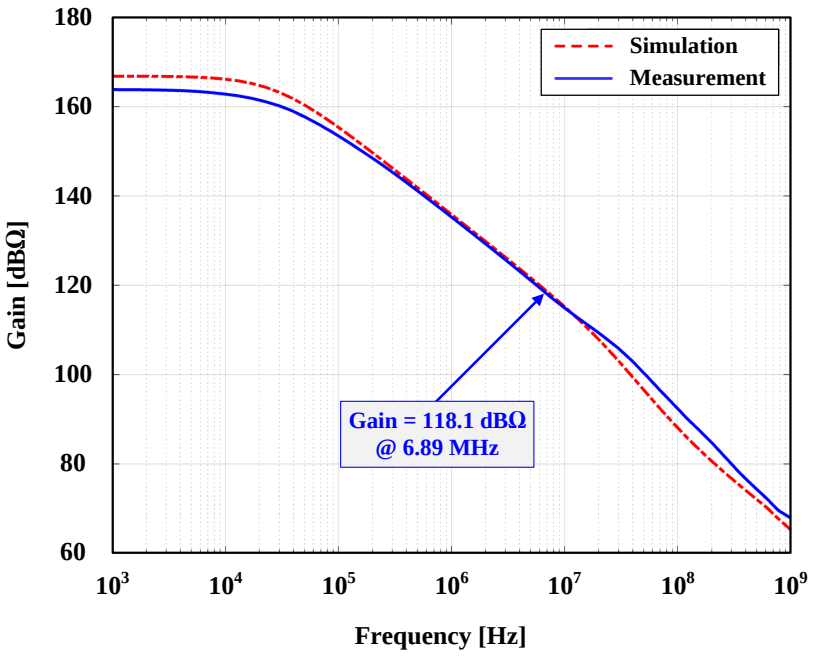


Fig. 3.7 Measured TIA transimpedance gain compared to simulation.

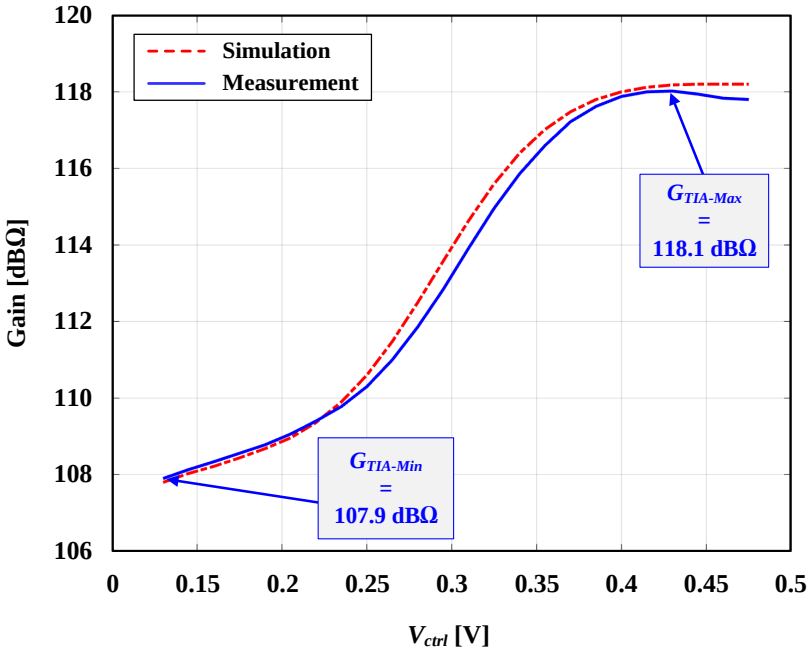


Fig. 3.8 Measured tunable TIA gain from 108 dBΩ up to 118.03 dBΩ compared to simulation.

3.4.2 Closed-Loop Validation

The loop is closed to measure the oscillator's performance after de-embedding the loading effects. The two dies – MEMS and CMOS – are wire-bonded together and packaged in an 80-pin quad flat no-lead (QFN) package. The QFN package has been chosen instead of the QFP due to the less loading capacitance of its leads [125, 127]. The package is mounted on a new custom PCB. All power nets are decoupled with a network of decoupling capacitors (10nF, 100nF, 1μF) connected in parallel and in ascending order from the IC package lead. A resistor of 1 MΩ has been connected in series between the MEMS V_P and the DC power supply source (BK PRECISION 9110) to limit the maximum current on the polarization terminal in the case of an accidental pull-in between the electrodes of the MEMS device. Another DC power supply source

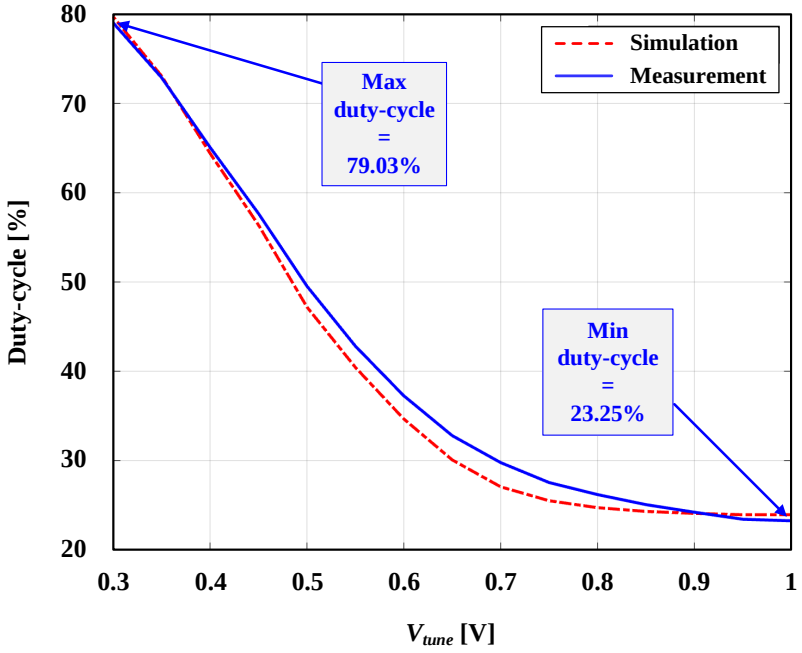
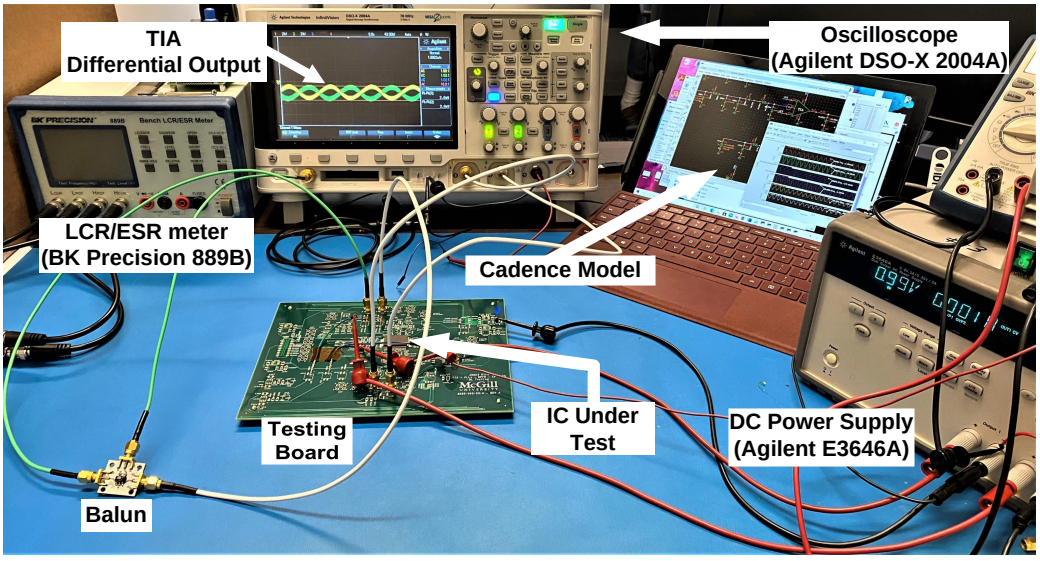
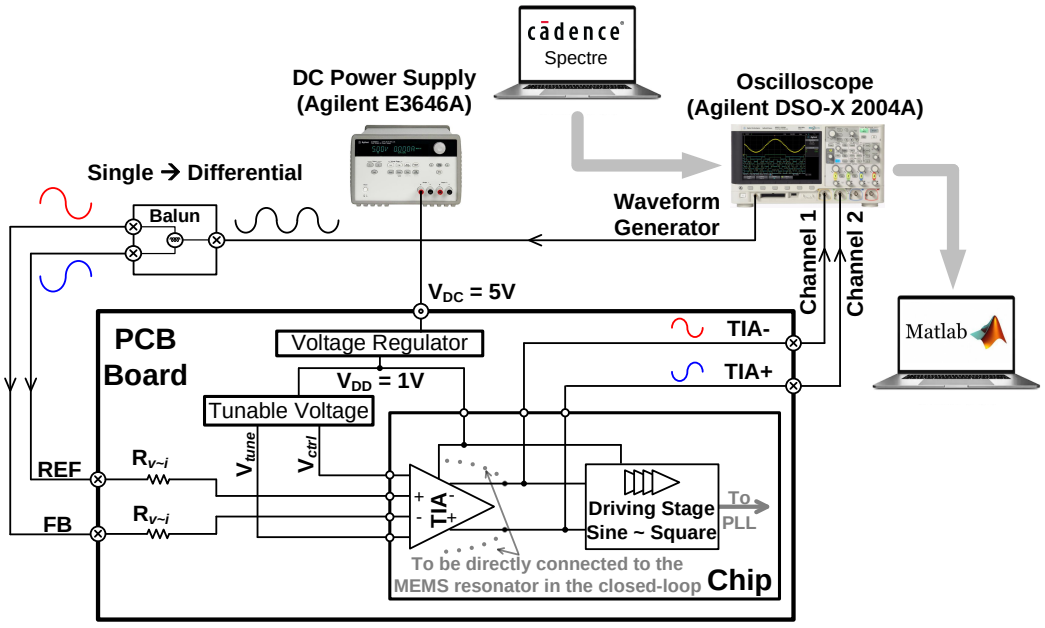


Fig. 3.9 Measured tunable duty-cycle from 23.25% to 79.03% compared to simulation.

(Agilent E3646A) was used to supply the CMOS circuits with a 1 V supply voltage. The (V_P) has been raised up gradually, reaching a stable output at $V_P = 40V$. Oscillation start-up was ensured by design: The nominal gain of the TIA was set to be higher than the absolute minimum theoretical value to account for all process corners and potential PVT variations. The natural nonlinearities of the TIA/resonator act as intrinsic gain control. The provision of an additional/backup manual gain control could be used to reduce the gain to emulate an AGC, whenever that was needed. Figure 3.11 shows the phase noise of the oscillator's output. It reports a phase noise (PN) of -128.1 dBc/Hz and -133.7 dBc/Hz at 1 kHz and 1 MHz offsets, respectively. The TIA total power consumption (P_{DC}) is 143 nW from a 1 V supply. Figure 3.12 shows the testing PCB and the wire-bonded dies in the mounted package.



(a)



(b)

Fig. 3.10 TIA open-loop validation: (a) picture of the actual setup and (b) setup block diagram.

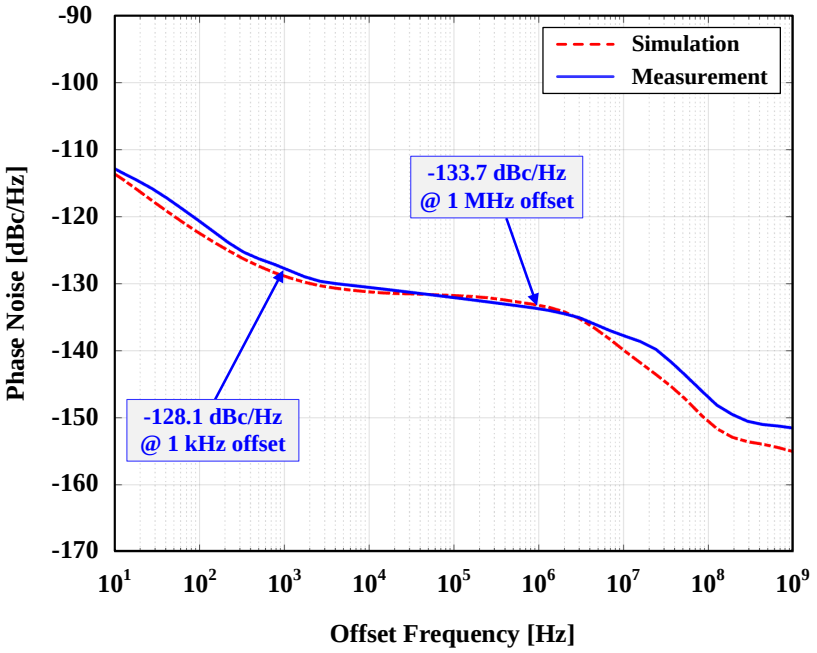


Fig. 3.11 Measured 6.89 MHz oscillator phase noise compared to simulation.

3.5 Figure of Merit

To fairly compare different oscillators with different resonator R_M and f_o values, the figure of merit (FoM) as proposed by Seth et al. [116] was used,

$$FoM = \frac{1}{\mathcal{L}(\Delta f \rightarrow f_o)} \frac{k_B T}{P_{DC}} R_M^2 f_o^2, \tag{3.9}$$

where, $\mathcal{L}(\Delta f \rightarrow f_o)$ is the phase noise at 1 MHz offset, and P_{DC} is the DC power consumption in Watt.

It considers several points, including (a) for a very high Q the $1/f^2$ and $1/f^3$ regions occur at low-frequency offsets. Thus, the PN at 1 MHz offset dominates and becomes the primary performance metric in these reference oscillators. (b) The DC power consumption, hence, the PN should be normalized to it. (c) The square of the

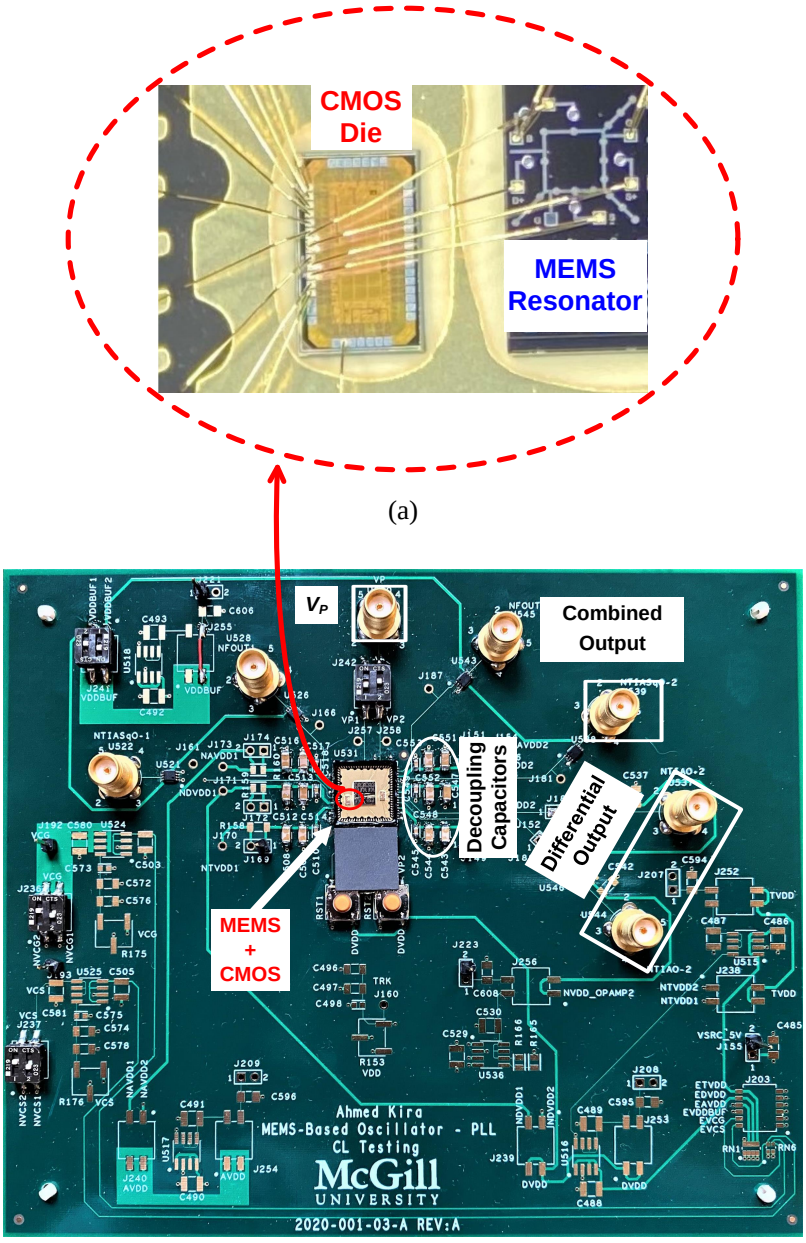


Fig. 3.12 (a) Picture of the wire bonded CMOS and MEMS dies. (b) Photograph of the testing board used to test the oscillator.

division ratio scales the PN at 1 MHz offset of a reference oscillator in a PLL, thus the reference oscillator's PN should be scaled to the inverse square of the reference frequency ($1/f_o^2$). (d) The PN at 1 MHz offset also scales with the square of the resonator motional resistance R_M, which is not part of the TIA circuit design, so the PN should be scaled as well by $1/R_M^2$.

This FoM is used in Table 3.2 to compare this work with previously published state-of-the-art. This work reports the highest FoM compared to other works reported in the literature. The reason behind this high FoM is the unprecedented low power consumption achieved by the design, making use of the very high Q of the resonator, while delivering a comparable noise performance.

Table 3.2 Oscillator Performance Summary and Comparison to the State-of-the-Art.

Ref. No.	[12]	[116]	[128]	[129]	[130]*	[131]	[132]	[133]	[134]	**This work**
Trans" Mech	Piezo+	Cap!	Cap	Cap	Piezo	Cap	Cap	Cap	Cap	**Cap**
Process	65 nm	0.35 μm	0.13 μm	0.35 μm	0.18 μm	65 nm	0.35 μm	0.35 μm	0.35 μm	**65 nm**
f_o (MHz)	14.42	20	20	0.551	75.01**	17.93	61	1.23	1.12	**6.89**
V_P⊗ (V)	-	-	5	18	-	100	7.45	7	25	**40**
Q	4.9e3	1.6e5	1e4	2e3	9.5e3	8.9e5	8e4	1.9e3	2.1e3	**3.24e6**
R_M (kΩ)	0.9	65	31	930	0.0326	35	13.8	16e3	2e3•	**199.1**
G_{TIA} (dBΩ)	69	-	112.5	157	-	98	-	138	121	**118.1**
P_{DC}	1.4 mW	6.9 mW	360 μW	8.5 μW	7.8 mW	900 μW	78 μW	150 μW	930 μW	**143 nW**
PN$\|_{1kHz}$ (dBc/Hz)	-116	-	-125.6	-103.8	-108	-120	-130	-106	-	**-128.1**
PN$\|_{1MHz}$ (dBc/Hz)	-130	-131$	-131.9	-121$	-133.15	-127	-152$	-111$	-	**-133.7**
$FoM\|_{1MHz}$ (Hz$^2\Omega^2$)	4.98e15	1.4e19	6.8e19	1.6e20	6.56e13	3.8e19	5.96e22	1.44e21	-	**1.3e24**

" Trans Mech: Transduction Mechanism.

+ Piezo: Piezoelectric.

! Cap: Capacitive.

⊗ V_P is the MEMS resonator polarization voltage.

• Deduced, approximately, from the measured motional resistance plot in the paper.

* This paper includes a PLL as a part of the whole oscillator. The reported performance (f_o, PN, P_{DC}) includes the PLL.

** This is the oscillator center/carrier frequency output from the PLL after being converted up from the MEMS (f_r = 27.19 MHz).

$ Deduced, approximately, from the measured phase noise plot in the paper.

Part II

A 6.7-μW Low Noise Compact PLL with a MEMS-Based Input Reference Oscillator Featuring a High-Resolution Dead-/Blind- Zone Free PFD

Chapter 4

Phase-Locked Loop Overview and Background Fundamentals

This chapter introduces the phase-locked loop (PLL), demonstrating its concept and essential operation. It introduces the different PLL components and provides overall system-level modeling for the PLL. It covers the PLL system frequency response and provides a noise analysis for the PLL.

4.1 PLL Overview

PLL is one of the most ubiquitous blocks deployed in almost all electronics and communication systems. It plays versatile roles including clock generation and synchronization in processors and digital applications, signal recovery, frequency synthesis and multiplication in communication systems. Although the basic concept of the PLL is the same, each of the design methodology, circuit design and implementation is quite different from an application to another. Designing a PLL for clock generation is different from designing it for frequency synthesis in high-speed communication applications. Design-

ing a PLL for clock generation in a microprocessor is different from designing it for clock generation in a wristwatch. A microprocessor jitter comes as the main concern, playing the key role in synchronizing the digital blocks and operations. On the other hand, a wristwatch, which only counts time, jitter-noise is not the primary concern [135], while power consumption (battery life) comes as a priority in this case. Thus, for each specific application, a different design methodology is used to meet a different set of requirements and challenges.

For a MEMS-based oscillator, a PLL plays a crucial role in either providing a frequency correction over fabrication process and temperature variations [136, 137, 138, 135] or synthesizing a different output frequency for different applications [139, 140, 141]. It is a key block that enables an efficient and complete implementation of a MEMS oscillator. Designing for portable timekeeping applications brings a different set of priorities, including power consumption, cost, and size (footprint area). Scalability and design migration to an advanced, smaller technology node process become a concern for analog IC designers to enable their designs in next-generation applications [142].

4.2 Definition and Concept

The PLL is a negative feedback control system. It compares and forces the phase of an output signal (Φ_{OUT}) to follow a clean input reference signal phase (Φ_{REF}). It is necessary to highlight that the variable of interest in this system is the signal phase (Φ). A basic PLL building block diagram is shown in Figure 4.1. The PLL main components are a voltage-controlled oscillator (VCO), a phase-frequency detector (PFD), a loop filter (LF), and a divider with a division ratio (N). The PLL tracks the phase changes trying to reach a zero-phase difference between the input reference (REF) and the

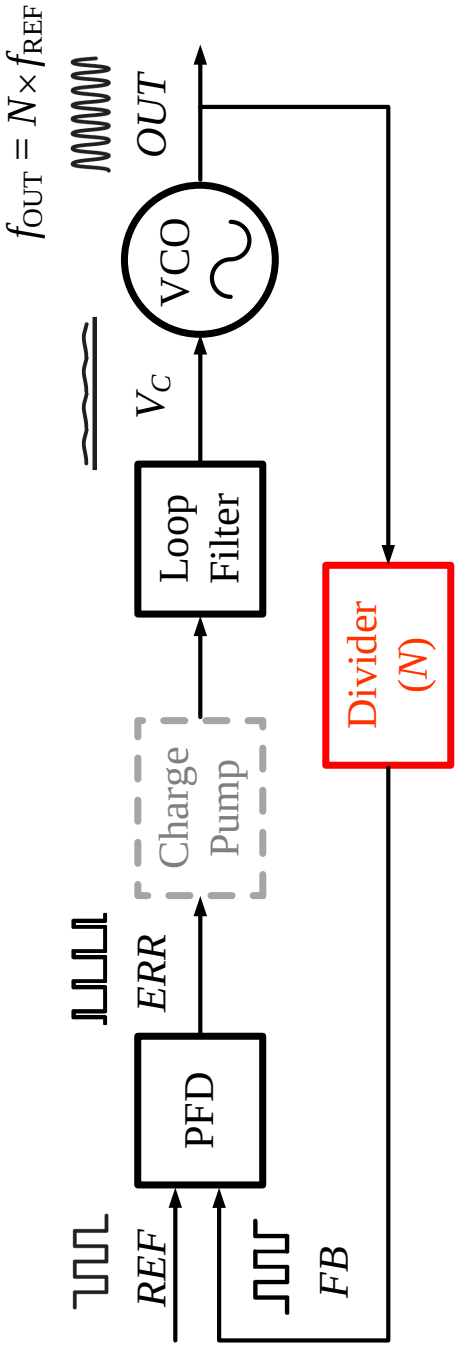


Fig. 4.1 PLL basic building block diagram.

output (OUT) signals. A PLL, in its simplest form, no divider added in the loop, creates an OUT signal with the same REF signal frequency and phase.

Basic Operation

The PFD compares the phase, and the frequency of both the reference (REF) and the feedback (FB) signals to each other and produces an error signal (ERR). ERR is then filtered using a loop filter (LF) – low-pass filter (LPF). The LF creates a controlling voltage signal (V_C) that controls the VCO and tunes its oscillation frequency to align and lock its output signal (OUT) with the REF signal frequency. When adding a divider (N) in the feedback loop, the VCO output frequency is divided by the divider ratio (N) and then compared with the REF signal. Hence, the PLL is in lock when the FB signal, from the divider output, has the same phase and frequency as the REF signal. This implies that the VCO output frequency (f_{OUT}) is N times the REF signal frequency (f_{REF}) when the PLL is in a lock state. The role and the behavior of the charge pump (CP) will be illustrated below after the "*PLL Types*" subsection.

4.3 PLL Components and System-Level Modeling

If the PLL loop bandwidth is much smaller than the REF frequency, the PLL can be treated as a linear system. A safe margin is to have the REF frequency at least 10 times higher than the PLL loop bandwidth to overlook the PFD sampling effect and approximate the PLL to a linear system [143]. The behavior of the different PLL blocks should be understood to be appropriately modeled, which is essential for an adequate PLL system-level analysis. In the following subsections, the fundamental behavior of each PLL component is introduced. Later in Chapter 5, more analysis and circuit

implementation will be discussed for each block.

VCO

The VCO oscillator generates a tunable output frequency (f_{OUT}) depending on an input control voltage ($\mathrm{V_C}$). Figure 4.2 depicts the two main VCO structures. An LC

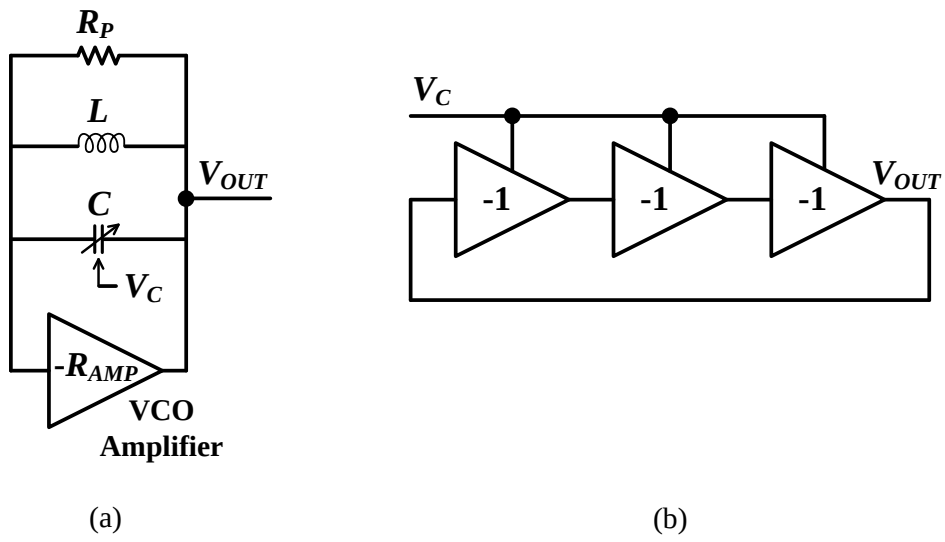


Fig. 4.2 VCO main structures: (a) LC oscillator, (b) Ring Oscillator.

oscillator consists of a variable-capacitor/varactor (C) controlled by voltage ($\mathrm{V_C}$) and an inductor (L), an LC tank. R_P resembles the parasitic losses in a non-ideal LC oscillator. Hence an amplifier ($-R_{AMP}$) is used to compensate for these losses and sustain a positive feedback oscillation. A simple, single-ended ring oscillator consists of an odd number of inverting amplifiers controlled by $\mathrm{V_C}$ and connected in a positive feedback loop. More details on how $\mathrm{V_C}$ controls the ring VCO output frequency will be discussed in Chapter 5. An LC oscillator can offer a low phase noise but at the expense of a large area trade-off and an increased power consumption. On the other

hand, a ring oscillator may have a higher phase noise but offers low power consumption, minimal area, more comprehensive tuning range, scalability between advanced CMOS technology nodes, and it is easier to integrate. The rate of change of the VCO output frequency (f_{OUT}) concerning the VCO input control voltage ($\mathrm{V_C}$) is defined as the VCO gain (Kvco); expressed as:

$$\frac{df_{OUT}}{dV_C} = K_{VCO}. \tag{4.1}$$

Figure 4.3 shows the relationship of the VCO control voltage versus the VCO output frequency. Considering the linear region, with a constant VCO gain, the previous equation can be linearly expressed in the time-domain as:

$$f_{OUT}(t) = K_{VCO} \times V_C(t). \tag{4.2}$$

As mentioned earlier, the phase is the variable of interest in the locking process of the

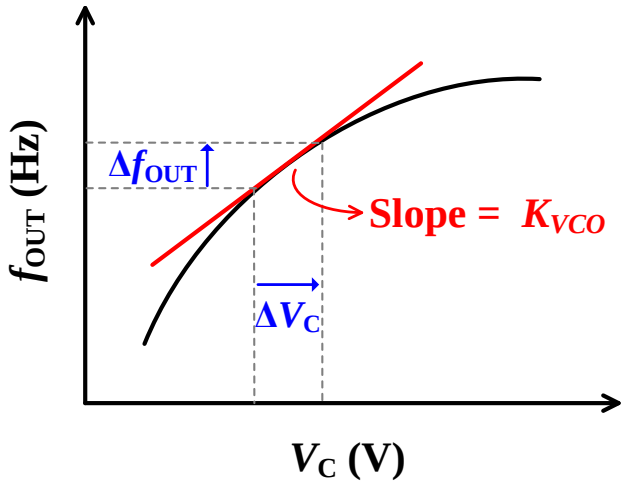


Fig. 4.3 VCO voltage to frequency mapping.

PLL system. In general, the phase of a signal is the integration of its frequency. Therefore, the time-domain output phase ($\Phi_{OUT}(t)$) relationship with the output frequency can be expressed as:

$$\Phi_{OUT}(t) = \int_{-\infty}^{t} 2\pi f_{out}(\tau)d\tau, \tag{4.3}$$

hence the output phase, time-domain, relationship with the control voltage will be:

$$\Phi_{OUT}(t) = \int_{-\infty}^{t} 2\pi K_{VCO} V_C(\tau). \tag{4.4}$$

The corresponding Laplace (s-domain) relationship representation between the output phase and the control voltage can be given as:

$$\frac{\Phi_{OUT}(s)}{V_C(s)} = \frac{2\pi K_{VCO}}{s}. \tag{4.5}$$

PFD

The PFD compares the phase of the input reference signal to the divided-down, fed back, VCO output signal – the divider output signal – and produces output pulses – typically voltage pulses – that resembles the phase difference ($\Delta\Phi$) between the two signals.

One of the typically used implementations is the tri-state PFD, shown in Figure 4.4. It produces two output pulses, UP and DN, used to control a subsequent circuit to create an error signal (ERR). The average value of the error signal – extracted later by the loop filter – corresponds to the phase error between the two input signals of the PFD. The relationship between the error signal average ($\overline{ERR}$) and the PFD input phase difference ($\Delta\Phi$) is shown in Figure 4.5. It shows an asymmetric phase error characteristic around the zero-phase, the origin. This is the critical feature that

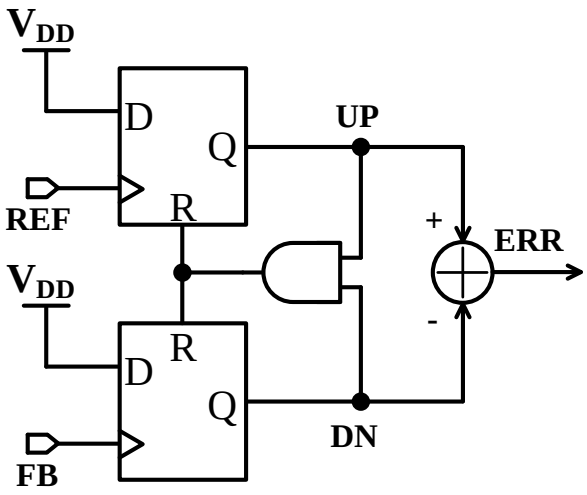


Fig. 4.4 Traditional tri-state PFD.

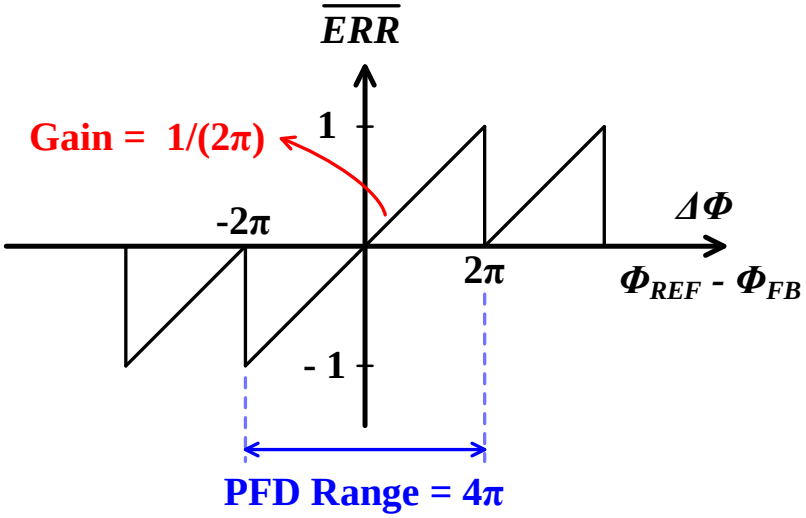


Fig. 4.5 Tri-state PFD characteristic.

enables frequency detection compared to phase detection in the XOR phase detectors (PD) [144]. The tri-state PFD characteristic shows a detection range of 4π and a gain of $1/(2\pi)$. Therefore, the PFD can be modeled in both the Laplace-domain and the time-domain as a constant gain element:

$$K_{PFD} = \frac{\overline{ERR}}{\Delta\Phi} = \frac{1}{2\pi}. \tag{4.6}$$

Loop Filter

The loop filter consists of a low-pass filter (LPF) that smooths the nonlinear PFD error pulses, extracts their average value and creates a DC voltage to control the VCO output frequency. It affects the loop dynamics and the PLL frequency response. The transfer function of the loop filter depends on its implementation. Figure 4.6(a) shows a first-order realization of the LPF as an example. For this implementation, the Laplace

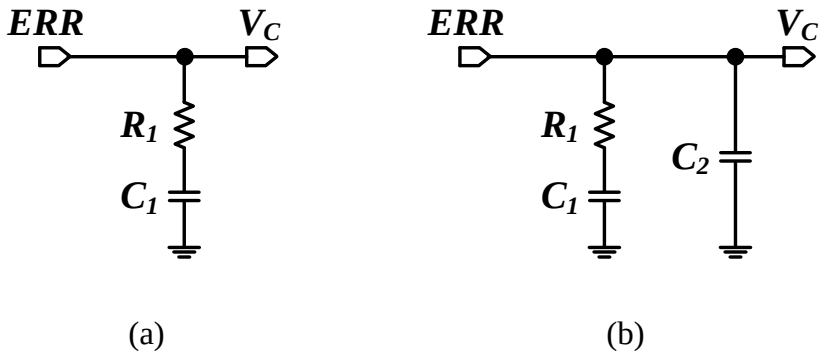


Fig. 4.6 LF examples: (a) first-order LPF, (b) second-order LPF

transfer-characteristic ($H(s)$) model is given by:

$$H(s) = \frac{1 + sC_1R_1}{sC_1}. \tag{4.7}$$

A second-order LPF filter, shown in Figure 4.6(b), can be used to further smooth the ripples on the VCO input control voltage (V_C). In this case the LF transfer characteristics ($H(s)$) is given by:

$$H(s) = \frac{1 + sC_1R_1}{s(C_1 + C_2)} \frac{1}{1 + \frac{C_2}{C_1+C_2}(sC_1R_1)}. \tag{4.8}$$

Divider

A frequency divider scales down an input signal frequency. It generates an output signal with a frequency scaled down by a division ratio (N) in comparison to the input signal frequency. In other words, it is a counter that for every one complete cycle of its output, it counts N cycles of its input signal. Figure 4.7 shows an example of a divider block, and it divides the input signal (OUT) by $N = 4$. As shown earlier, the signal

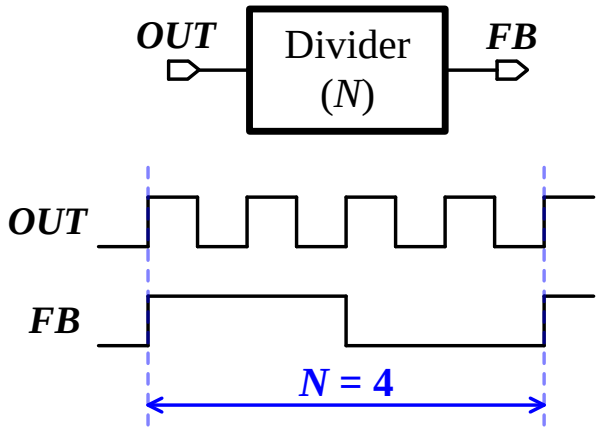


Fig. 4.7 An example of a divider block and its timing diagram.

phase is the integral of the signal frequency, hence the output phase will also be divided by N version of the input phase. Thus, the relationship between the divider output phase and the VCO output phase – divider input – can be written in the time-domain

as

$$\Phi_{FB}(t) = \frac{1}{N}\Phi_{OUT}(t), \tag{4.9}$$

and in Laplace (s-domain) as

$$\Phi_{FB}(s) = \frac{1}{N}\Phi_{OUT}(s), \tag{4.10}$$

PLL Types

The type of the PLL depends on how many integrators are in the PLL open-loop transfer function, how many poles are at DC. There are two PLL types:

- **Type I:** The PLL has one integrator in the open-loop transfer function

  VCO: The VCO characteristic, as shown in Equation (4.5), naturally adds a pole at DC.

  LF: The chosen filter implementation has no integrators in its characteristic, H(s).

- **Type II:** The PLL has two integrators in the open-loop transfer function

  VCO: One integrator is added from the VCO characteristics.

  LF: Adds another integrator. The chosen filter implementation has one integrator in its characteristic, H(s).

Type I versus Type II PLLs

Figure 4.8 shows the range of DC output from a constant gain, $H(s) = K$, block versus an integrator, $H(s) = K/s$, block [144]. The issue is that the DC gain of a loop filter is often small, and the PFD has a limited output range. Thus, a loop filter with no

integrator fails to cover the full VCO input range. As illustrated in [144], achieving a

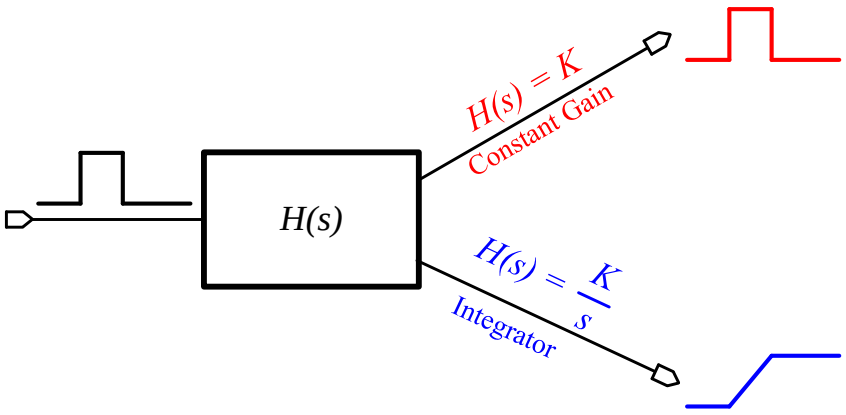


Fig. 4.8 DC output range of a constant gain ($H(s) = K$) block versus an integrator ($H(s) = K/s$) block.

full span VCO range is different for each PLL type:

Type I: A digital-to-analog (D/A) converter needs to be added to provide a coarse tuning

- This consumes more power and adds more design complexity.
- It, inconsistently, sets a steady-state phase error.

Type II: A loop filter with an integrator in its transfer function, automatically, provides a DC level shifting that covers the VCO input range

- This results in lower power consumption and simpler implementation.
- It always sets the steady-state phase error to zero.

CP and type II PLL implementation

A current going in and out from a capacitor forms the integrator. A CP can be used to create this integrator. A well-known standard current-based CP connected

to the tri-state PFD is shown in Figure 4.9. It consists of two current sources, I_{UP}

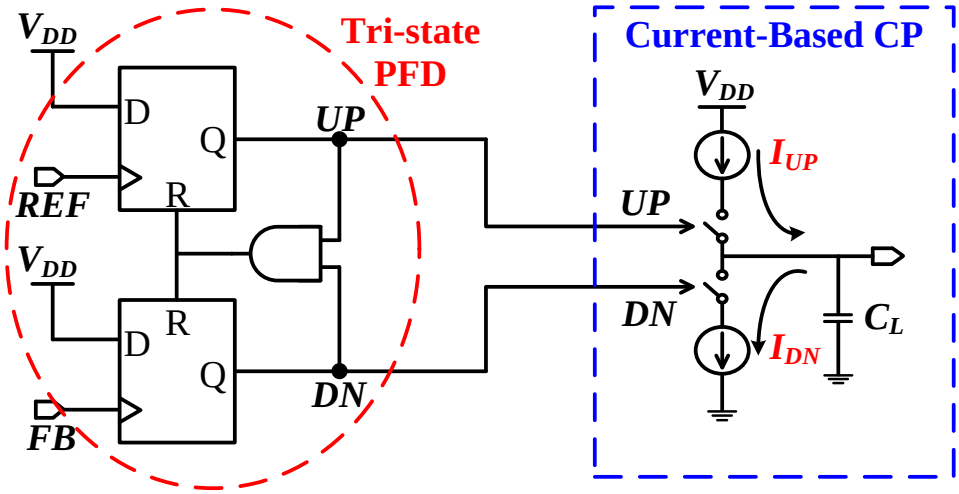


Fig. 4.9 A standard current-based CP connected to the traditional tri-state PFD.

and I_{DN}, ideally matched, to pump charges into or out from the output node, to which a loading capacitor (C_L) is connected. If REF leads FB, the PFD will produce UP pulses instructing the CP to source current, I_{UP}, in the output node. This accelerates the VCO output signal forcing it to get in phase with the REF signal. If REF lags FB, the PFD will generate DN pulses triggering the CP to sink current, I_{DN}, from the output node, which slows down the VCO output signal locking back the loop in phase. The CP output current (I_{CP}), charges ($I_{CP} = I_{UP}$), or discharges ($I_{CP} = I_{DN}$) the output node for a time (Δt_p) that corresponds to the phase difference between the REF signal and the FB signal. The loop filter gain can be adjusted based on the CP current. The CP is a gain element and can be modeled as (I_{CP}). Figure 4.10 shows the CP connected to a second-order loop filter. The I_{CP} into the capacitor (C_2) forms an integrator. The other lumped resistor (R_1) and capacitor (C_1) add an extra pole and zero to the transfer function.

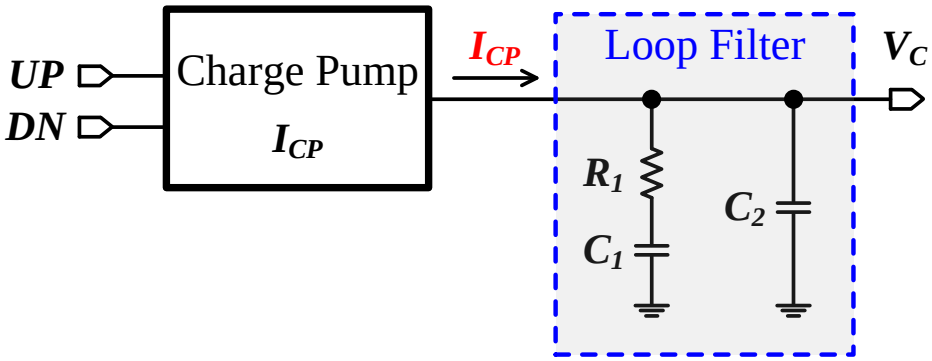


Fig. 4.10 A CP is connected to a second-order loop filter.

The loop filter transfer function is given by Equation (4.8).

Note that the PFD/CP works as a discrete sampling component. Its linearized model is valid only when the PLL loop bandwidth is smaller than the input reference signal frequency [145]. This note plays an essential role while designing the PLL and choosing its different blocks' coefficients, as will be shown later.

4.4 PLL System Frequency Response

After combining all PLL individual components models, the overall PLL linearized model can be constructed as shown in Figure 4.11. The PLL open-loop (loop-gain) response in Laplace-domain ($A(s)$) is given by

$$A(s) = \frac{1}{\pi} I_{CP} H(s) \frac{K_{VCO}}{s} \frac{1}{N}, \tag{4.11}$$

and the closed-loop PLL transfer-function (G(s)), in terms of A(s), is given by

$$G(s) = \frac{A(s)}{1 + A(s)}. \tag{4.12}$$

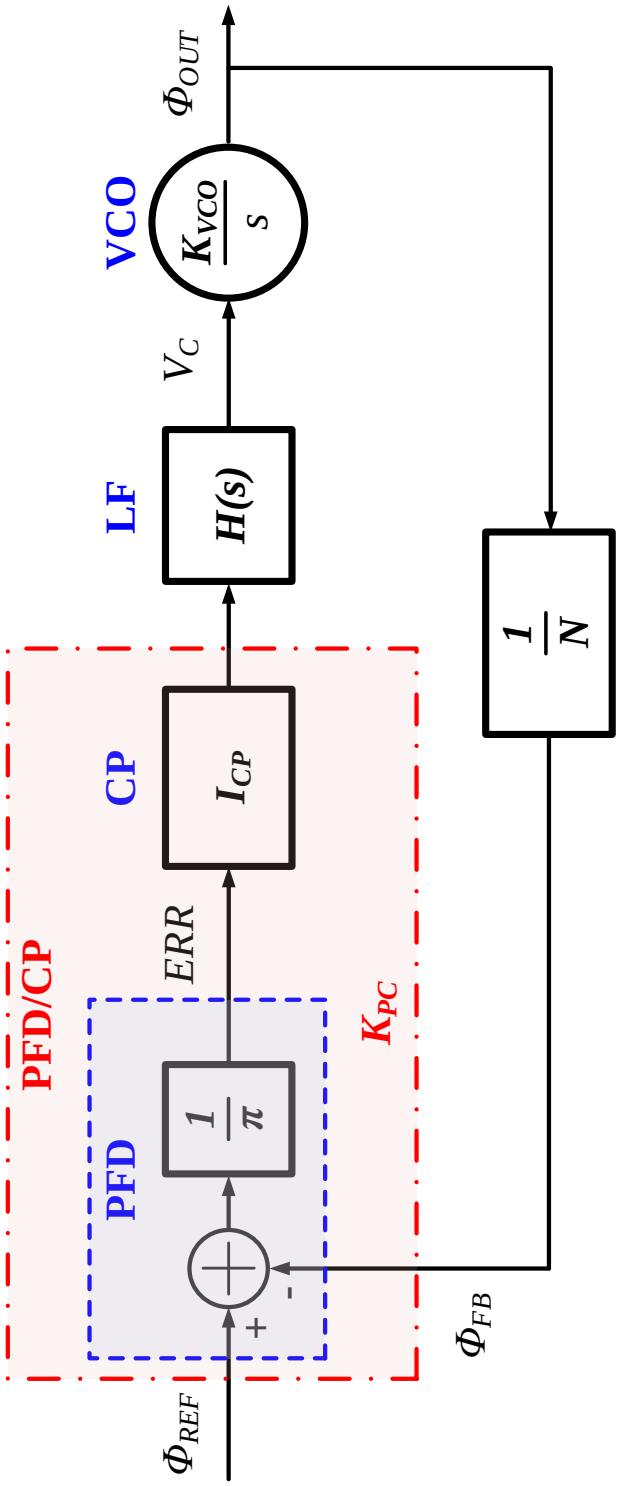


Fig. 4.11 PLL linearized model.

Defining K_{PC} as the gain coefficient of the PFD and CP combined, therefore, K_{PC} can be expressed as

$$K_{PC} = \frac{I_{CP}}{\pi}, \tag{4.13}$$

hence Equation 4.11 can be written as

$$A(s) = \frac{K_{PC}K_{VCO}H(s)}{N.s}, \tag{4.14}$$

An appropriate loop filter topology ($H(s)$) should be chosen. The $H(s)$ pole/zero locations should be higher than the required PLL bandwidth to pursue stable PLL dynamics. In addition, the open-loop gain ($A(s)$) should be adjusted to reach the required PLL bandwidth while keeping stability.

Using the first-order loop filter, shown in Figure 4.6(a), with an $H(s)$ expressed by Equation (4.7), the open-loop PLL transfer function can be written as

$$A(s) = \frac{K_{PC}K_{VCO}}{N}\frac{1+sC_1R_1}{s^2C_1}, \tag{4.15}$$

and the open-loop PLL transfer-function using the second-order loop filter, shown in Figure 4.6(b), with an $H(s)$ expressed by Equation (4.8), is given by

$$A(s) = \frac{K_{PC}K_{VCO}}{N}\frac{1+sC_1R_1}{s^2(C_1+C_2)}\frac{1}{1+\frac{C_2}{C_1+C_2}(sC_1R_1)}. \tag{4.16}$$

Equations (4.15) and (4.16) have two poles at DC, hence representing a type II PLL implementation. The resistor (R_1) introduces a zero (f_Z) that ensures loop stability. A PLL open-loop gain should be chosen for an adequate phase margin (PM). Hence, the pole and zero should be chosen so that the zero (f_Z) is lower and the pole (f_P) is

higher than the required PLL bandwidth.

PLL Order

The open-loop transfer function order is known as the PLL order. It is higher than the loop filter order by one degree. Therefore, Equation (4.15) is the transfer function for a second-order PLL and Equation (4.16) is the transfer function of a third-order PLL.

4.5 PLL Noise Analysis

It is essential to briefly discuss and introduce the main noise sources in a PLL system. This is helpful in the initial PLL theoretical analysis, shown later in Chapter 5, and how to choose the PLL bandwidth optimally.

Figure 4.12 shows the different noise sources in a PLL, and Figure 4.13 shows the PLL linearized model after adding the noise sources [144]. The PLL impacts the VCO noise in two ways: (a) other PLL circuit blocks add an extrinsic noise to the VCO, and (b) the PLL feedback dynamics high pass filter the VCO noise. The extrinsic noise sources to the VCO comes from the jitter in the reference, jitter in the divider, the reference feedthrough, and the charge pump noise.

To model the impact of the noise on the PLL output phase (Φ_{OUT}), a transfer-function needs to be derived from each noise source to the output phase of the PLL (Φ_{OUT}). For simplification, all noise sources – except for the VCO noise source – can be referred to the PFD output as (E_n), as shown in Figure 4.14. It corresponds to the sum of all other noise sources – not including the VCO noise source – and refers them to the PFD output. As shown in [144], the transfer function describing the relationship between the output referred noise (Φ_{OUTn}), and the PFD-referred noise (E_n) in the

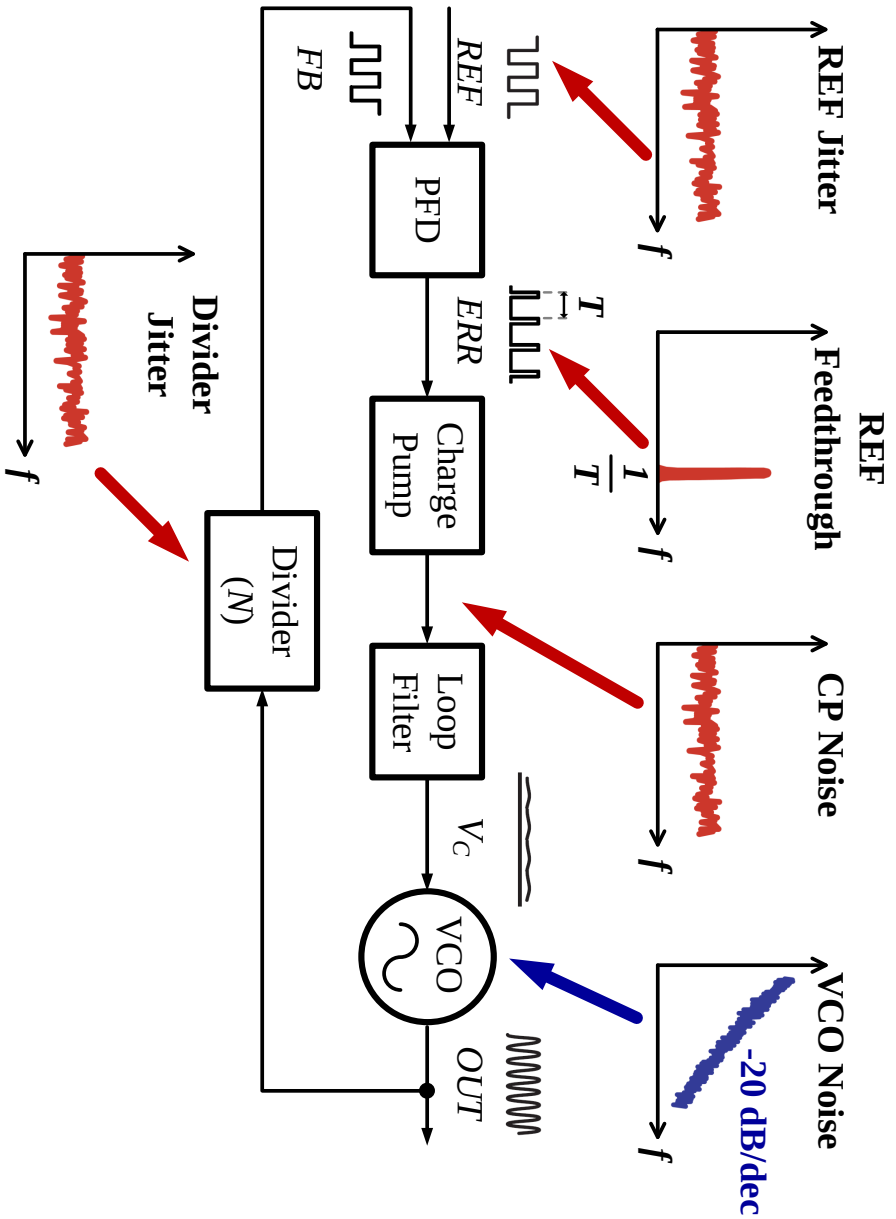


Fig. 4.12 Noise sources in a PLL.

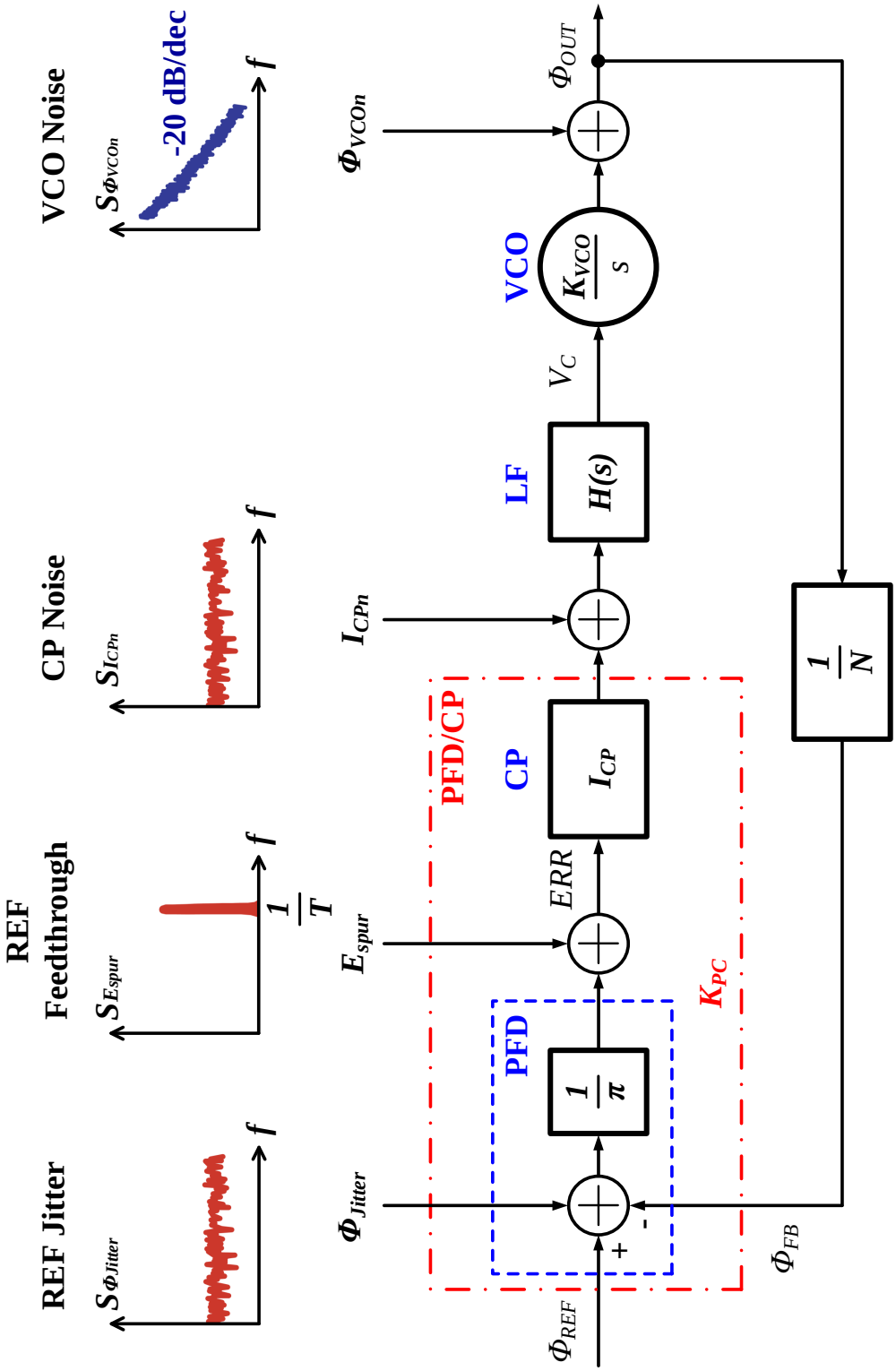


Fig. 4.13 PLL linearized model with noise sources.

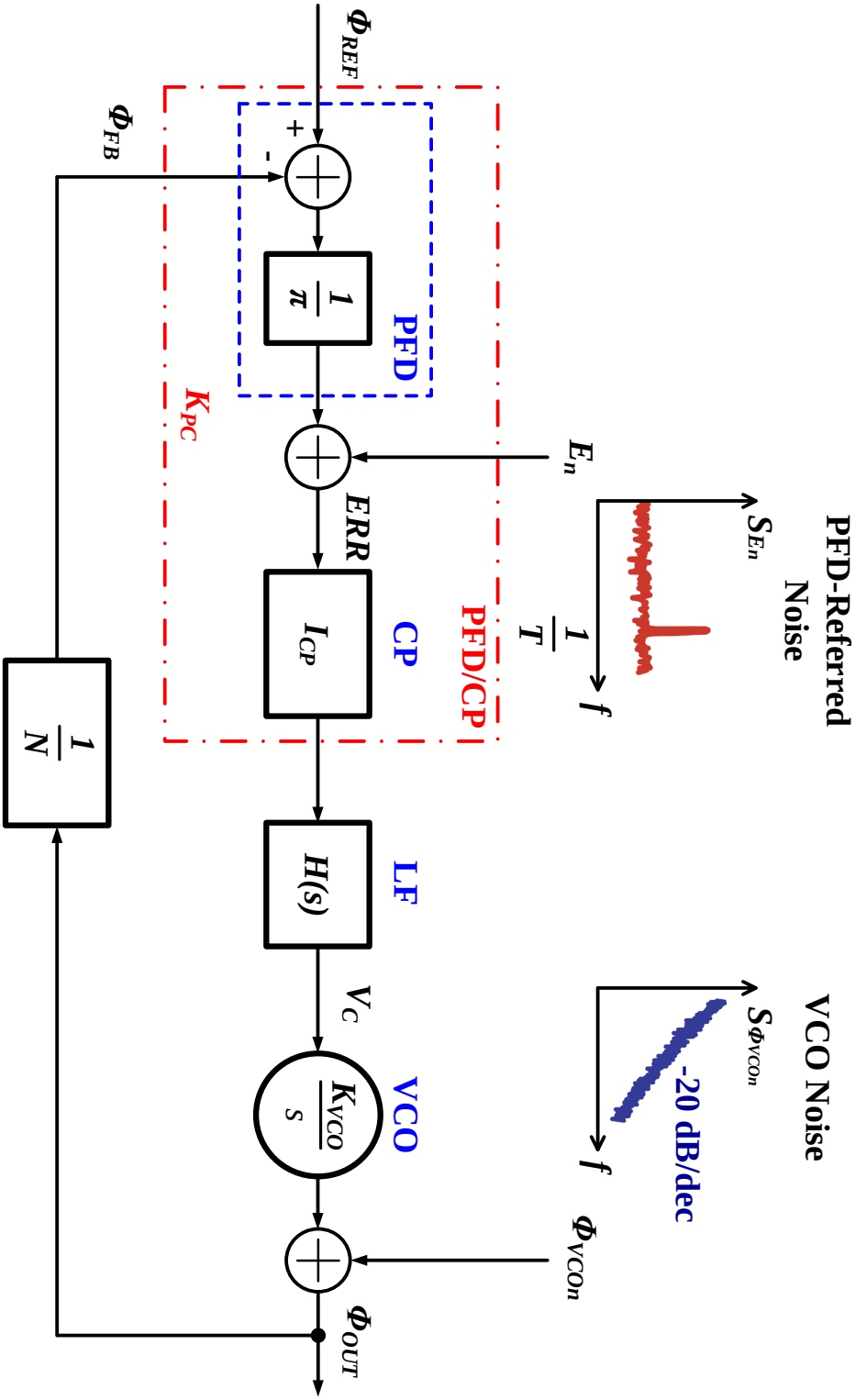


Fig. 4.14 Simplified PLL noise model.

Laplace-domain can be given by

$$\frac{\Phi_{OUTn}(s)}{E_n(s)} = \frac{I_{CP}H(s)\frac{K_{VCO}}{s}}{1+\frac{1}{2\pi}I_{CP}H(s)\frac{K_{VCO}}{s}\frac{1}{N}}, \tag{4.17}$$

and the transfer function of the output referred noise (Φ_{OUTn}) in response to the VCO-referred noise (Φ_{VCOn}) can be expressed as

$$\frac{\Phi_{OUTn}(s)}{\Phi_{VCOn}(s)} = \frac{1}{1+\frac{1}{2\pi}I_{CP}H(s)\frac{K_{VCO}}{s}\frac{1}{N}}. \tag{4.18}$$

Using Equations (4.11) and (4.12), Equation (4.17) can be parametrized in terms of $G(s)$ and written as

$$\frac{\Phi_{OUTn}(s)}{E_n(s)} = 2\pi N\frac{A(s)}{1+A(s)} = 2\pi NG(s), \tag{4.19}$$

and Equation (4.18), as well, can be expressed as

$$\frac{\Phi_{OUTn}(s)}{\Phi_{VCOn}(s)} = \frac{1}{1+A(s)} = 1-\frac{1}{1+A(s)} = 1-G(s), \tag{4.20}$$

As shown in [146], Figure 4.15(a) shows the parametrized PLL noise model. The PFD-referred noise is low-pass filtered by the loop cut-off frequency (f_c), while the VCO-referred noise is high-pass filtered by f_c. Thus, the PFD-referred noise dominates at the low frequencies, while the VCO-referred noise dominates at the high frequencies. The PFD-referred noise is scaled by the inverse of the PFD gain (2π) and the square of the divide ratio (N^2). Thus, a large N will lead to higher multiplication of the noise.

Figure 4.15(b) shows that the optimum choice of the PLL bandwidth is where the two noise sources intersect, $f_{c|optimum}$. The higher the PLL bandwidth,

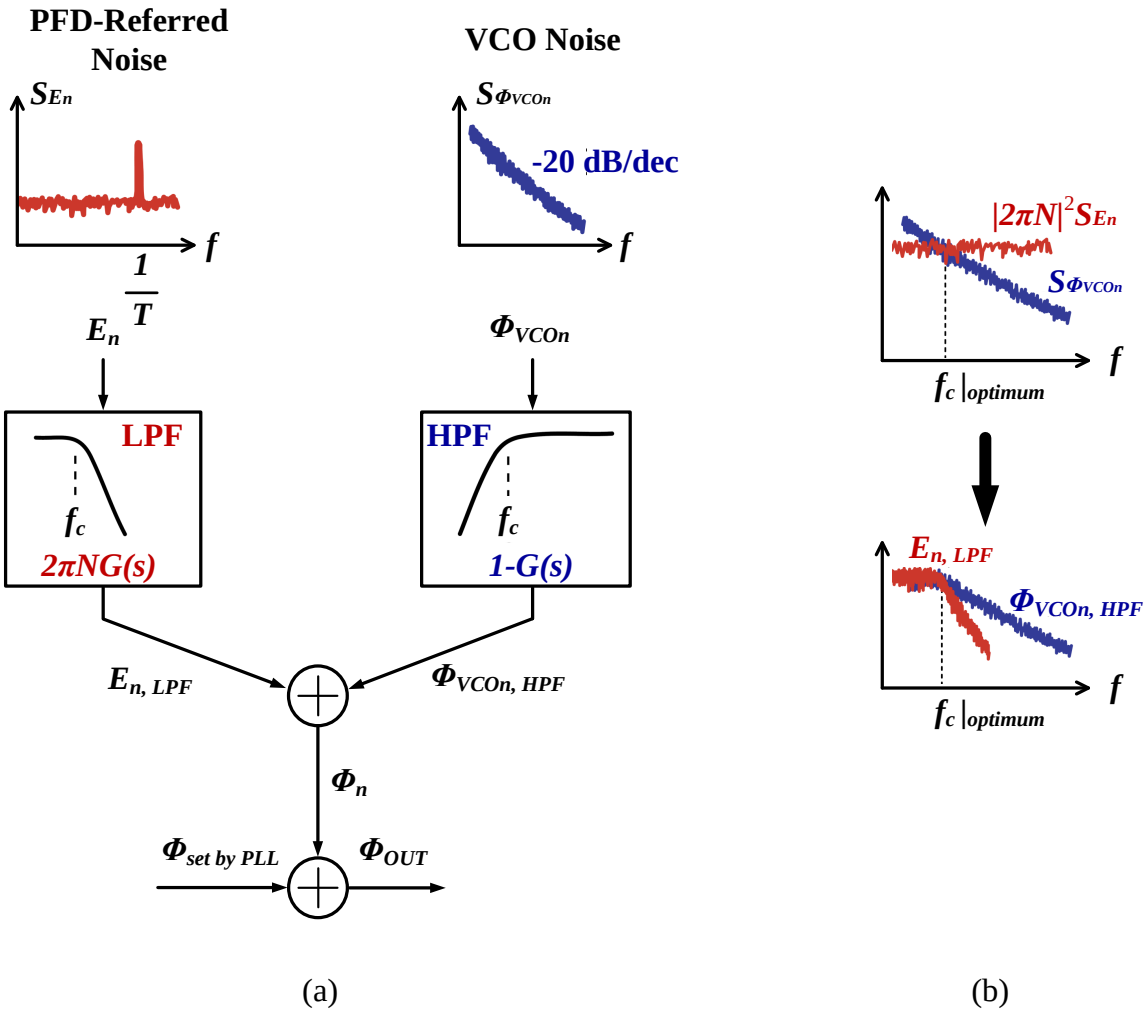


Fig. 4.15 Parametrized PLL noise model.

$BW > f_{c|optimum}$, the more PFD-referred noise allowed in-band and the lower the PLL bandwidth, $BW < f_{c|optimum}$, the more VCO-referred noise allowed in-band [138, 143].

Chapter 5

PLL With a MEMS-Based Input Reference Oscillator

This chapter reports the implementation of a MEMS-based frequency synthesizer. The resonator and the oscillator were discussed in detail in part I. Part II focuses on the PLL. Figure 5.1 shows the overall system block diagram. The MEMS resonator is wire-bonded to the CMOS die containing the oscillator sustaining amplifier circuit and the integer-N synthesizer. The oscillator output provides a 6.89 MHz input reference frequency to the integer-N PLL, which generates a higher output frequency at 110.2 MHz.

This chapter focuses on proposing the design of ultra-low power, low noise, less complex, and compact integer-N PLL with an input MEMS-based reference oscillator. In particular, it introduces the design of ultra-low power, high resolution, dead-/blind-zone free phase-frequency detector (PFD), providing a smaller area and less design complexity. In addition, when combined with the used charge-pump (CP), it offers smoother scalability between fabrication processes compared to traditional PFD de-

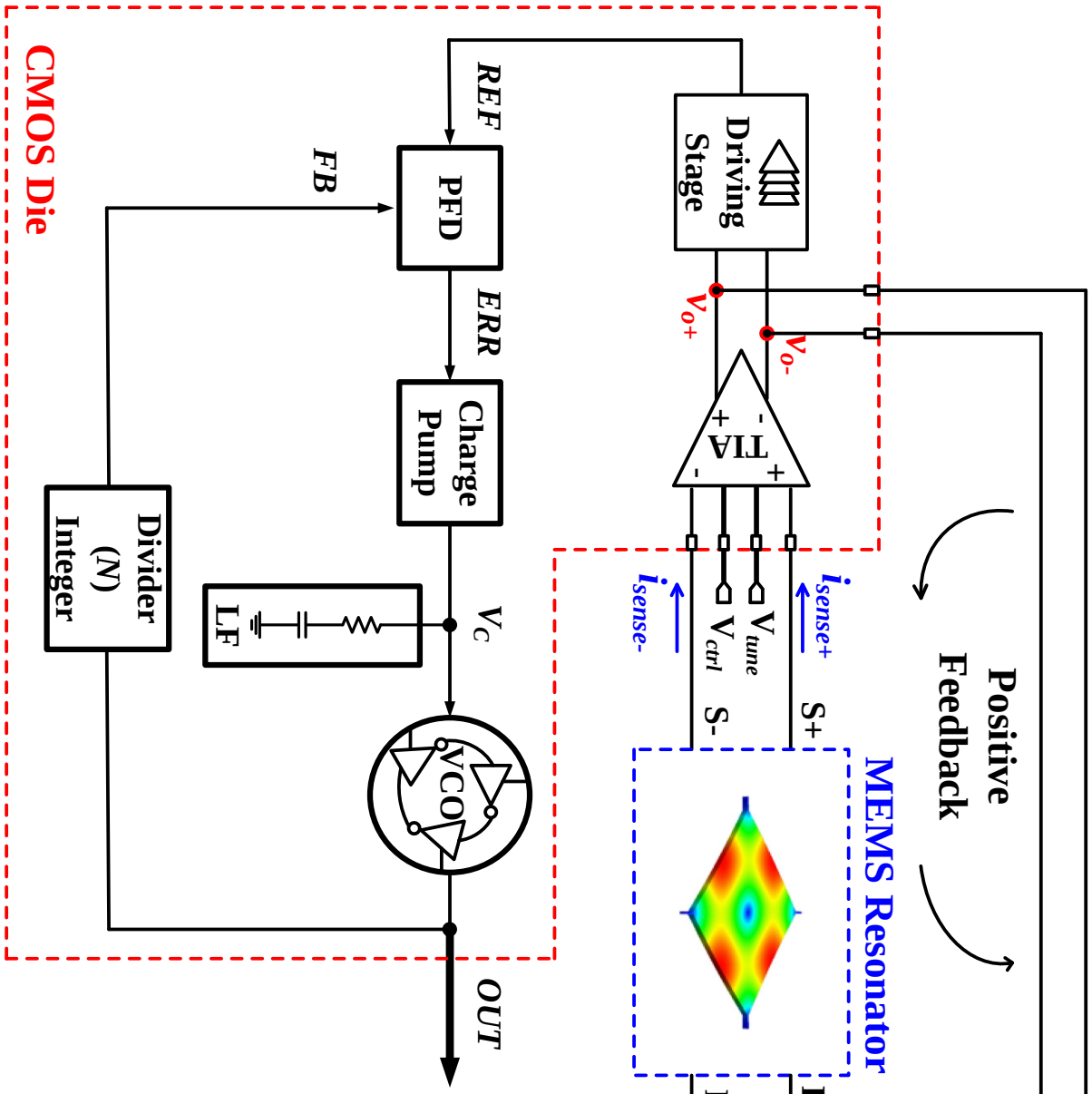


Fig. 5.1 The PLL system with the MEMS-based input reference oscillator.

signs. A charge transfer-based CP is used, offering a lower power consumption, a smaller footprint, and a lower noise PLL design.

5.1 PLL DESIGN

The PLL has been carefully designed to efficiently tackle power consumption and overall system performance to meet the emerging reference oscillator demands needed by mobile electronics and future applications. The block diagram of an integer-N PLL is shown in Figure 5.2. A type-II charge-pump based PLL has been selected to achieve low power consumption [143], as detailed in this section. The PFD compares the phase and the frequency of the reference (REF) signal to the feedback (FB) signal and produces, with the CP, an error signal. This error signal is then filtered through a low-pass filter (LPF) to create a voltage controlling signal (V_C) that controls the VCO and tunes its output oscillation frequency. With a divider in the feedback loop, the VCO output frequency is divided by the divider ratio (N) and then compared with the REF. This forces the FB from the divider to have the same phase and frequency of the REF; hence the PLL is in lock, which implies that the VCO output frequency, the PLL output (f_{OUT}), is N times the REF signal frequency (f_{REF}).

To treat the PLL as a linear system, the PLL loop bandwidth should be much smaller than the REF frequency. A safe margin is to design the loop bandwidth at least 10 times smaller that the REF frequency to overlook the PFD sampling effect and approximate the PLL to a linear system [143].

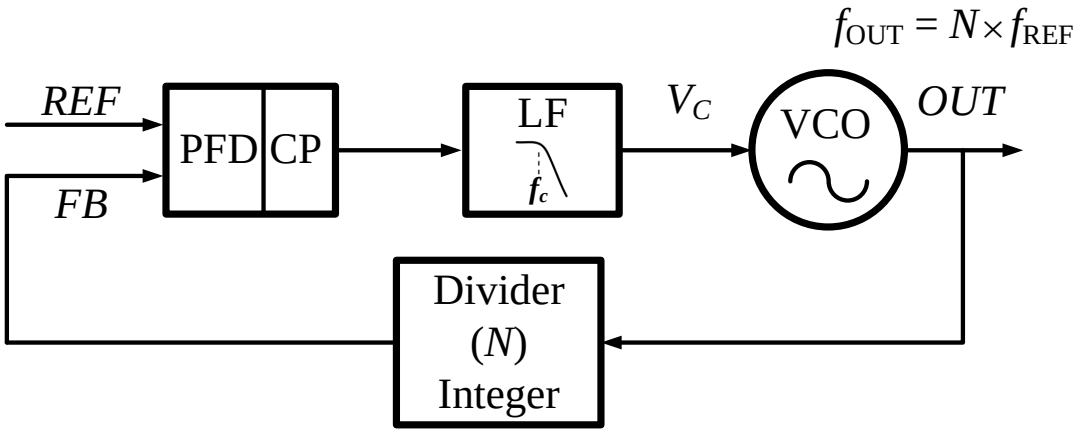


Fig. 5.2 Integer-N PLL basic building block diagram.

5.1.1 Loop Filter

Based on the PLL performance parameters the loop filter topology and order can be determined. An on-chip first-order RC loop filter, shown in Figure 5.3, was designed to set the loop bandwidth around 50 kHz to minimize the voltage-controlled oscillator's (VCO) overall noise. Equation (4.7) represents the LF transfer function. The loop

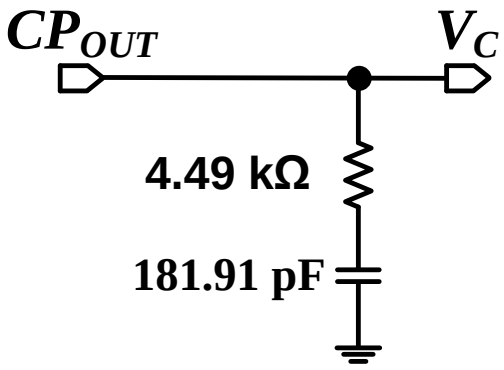


Fig. 5.3 First-order loop filter design.

filter component values must be selected to set the PLL transitional frequency, the

PLL bandwidth, at a frequency where the VCO spectral noise intersects with the PFD-referred noise ($f_c|_{optimum}$), as illustrated earlier in Figure 4.15. This optimizes the PLL performance and guarantees minimum noise at the PLL output [147].

The LF has been on-chip fabricated in the TSMC 65 nm CMOS process technology. The total active LF CMOS area (A_{LF}) is 0.1027 mm^2 (314.08 μm $\times$ 327.05 μm). As expected, the LF consumes the majority of the area of the PLL.

5.1.2 Voltage-Controlled Oscillator

The VCO block is a critical component in determining the PLL performance. The decision of using either a ring-based VCO or an LC-based VCO depends on the application requirements in terms of power consumption, area, and noise. The LC-VCO can offer a more practical solution for applications with high, stringent noise requirements as in radio frequency (RF) communication systems [148, 149]. On the other hand, as illustrated in Chapter 4, ring VCOs introduces a desirable solution to minimize the power consumption and the system area. The absence of passive components results in a more compact design. The easy start-up condition permits for much less power consumption. Thus, the ring VCO fits very well in our application.

The VCO is a current-starved ring-based oscillator, shown in Figure 5.4, with a nominal frequency of 110.24 MHz. A modification in the transistor aspect ratio has been adopted, including long transistor channel length (L), to further help in consuming less power and producing less noise [150, 151].

The VCO power consumption (P_{VCO}) is 2.204 μW at 110.2 MHz and a 1 V supply voltage. The VCO has been on-chip fabricated with a total active CMOS area (A_{VCO}) of 30.16 μm^2 (2.52 μm $\times$ 11.97 μm).

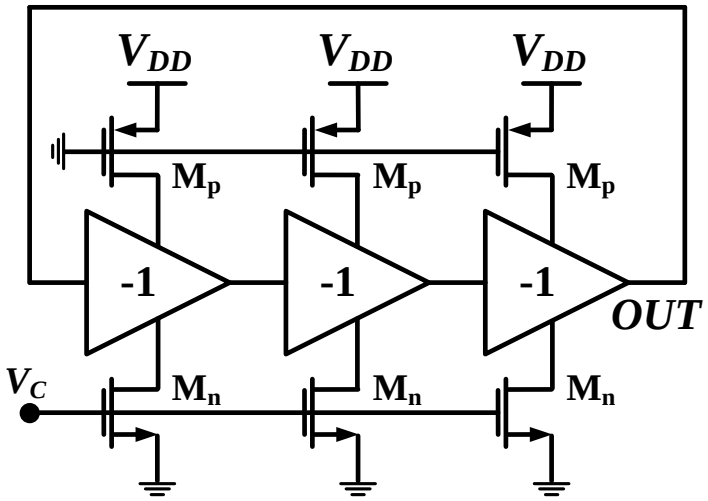


Fig. 5.4 A simplified diagarm of the ring-based VCO.

5.1.3 Frequency Divider

A divider with a divide-ratio (N) of 16, shown in Figure 5.5, was designed based on low power dynamic D flip-flops (DFFs) [152, 153] to save power and area.

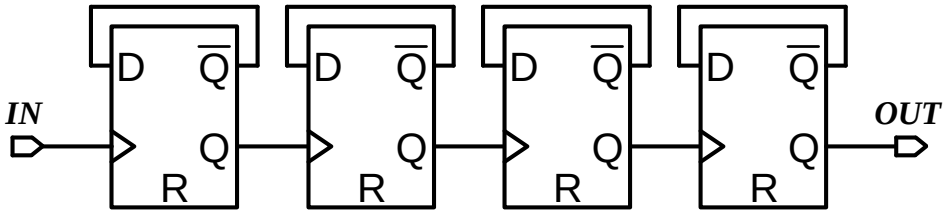


Fig. 5.5 A simplified diagarm of the $N = 16$ divider.

At a 1 V supply voltage, the divider power consumption (P_{DIV}) is 2.582 μW. The fabricated divider occupies a total active CMOS area (A_{DIV}) of 106.76 μm^2 (3.3 μm $\times$ 32.35 μm), using the TSMC 65 nm fabrication process.

5.1.4 Charge Transfer-Based CP

The standard current-based CP, shown in Figure 5.6(a), suffers from significant design challenges, including:

- **Wasted static power**

  Bias and current mirror circuits are always active (on) even in phase-lock.

- **Extra matching circuitry**

  It is used to match the charge-up current (I_{UP}) and charge-down current (I_{DN}).

- **Large active area**

  Current mirror circuits and extra matching circuitry.

- **Slow analog switching times**

  Large transistor switches take a longer time to switch on and off. This adds more delay to the PLL control loop.

- **Sensitivity to process variations**

  Current sources, amplifiers, large transistors.

- **Current leakage through large switches**

  Causes errors on V_C, hence affecting the VCO output frequency during the lock.

- **Limited headroom**

  Stacked transistors, therefore, restricted use in low-supply voltage applications.

- **Hard scalability**

  The usage of large current mirrors and large switches needs a redesign when moving to an advanced small CMOS process node.

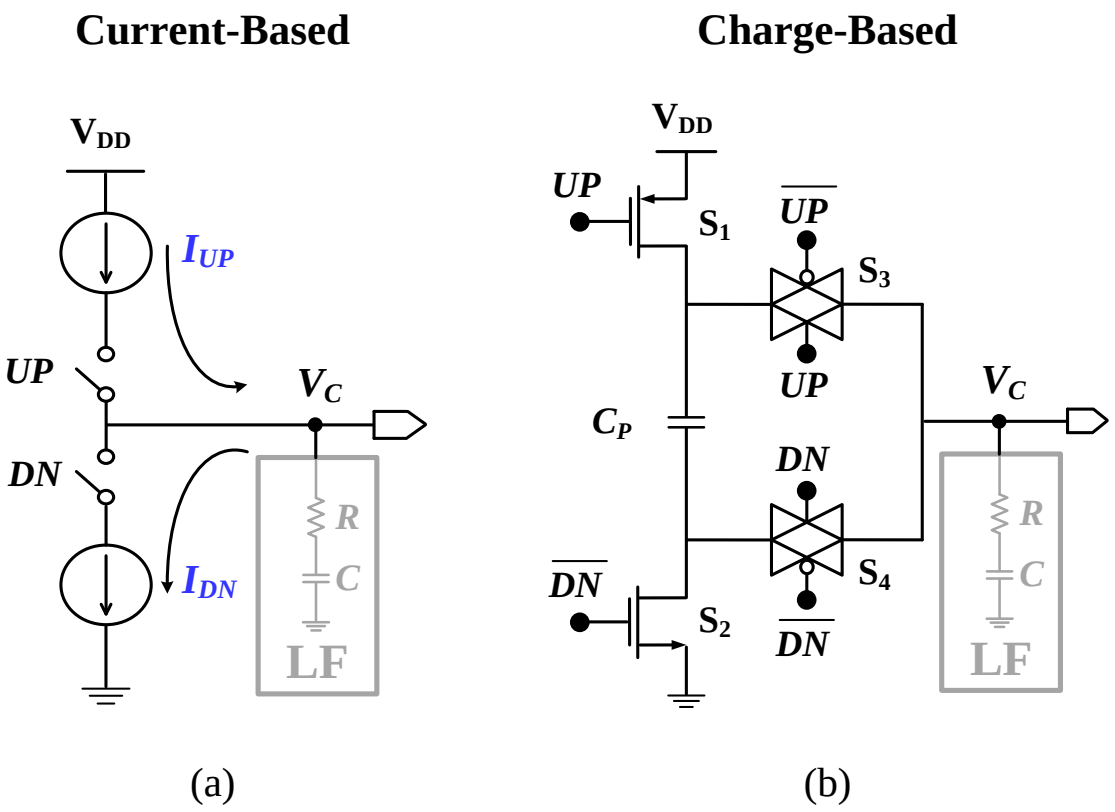


Fig. 5.6 CP: (a) standard current-based and (b) charge transfer-based.

The charge transfer-based CP shown in Figure 5.6(b), proposed by Schober and Choma [154], has a great advantage over the current-based CP, efficiently mitigating the challenges mentioned earlier. It does not suffer from device mismatch errors and can be operated from a low supply voltage. Most importantly, its fast-switching action allows the use of a non-delayed PFD, which results in reduced reference spurs and low noise characteristics in the frequency spectrum of the PLL.

The CP design consists of four minimum sizes, transistor switches (S_1, S_2, S_3, and S_4) and a small interconnect capacitor (C_P). C_P is sized to be dominant over parasitic. In the current design, C_P is 100 fF. C_P itself acts as an extra filter in the control loop of the PLL [142]. The CP operation is based on charge transfer between C_P and the LF (C_L). It works in one of three modes: (a) Idle, (b) Pump-Up and (c) Pump-Down.

Idle: Both UP and DN are low ($UP = 0$ and $DN = 0$). Both switches S_1 and S_2 are on, while switches S_3 and S_4 are off. In Idle mode C_P charges up to V_{DD} and holds its charge. No change on V_C happens during the Idle mode. The CP enters this mode either (a) when the PLL is in lock or (b) to recharge C_P between Pump-UP and Pump-Down modes.

Pump-Up: The CP enters this mode when REF leads FB. UP is high ($UP = 1$) and DN is low ($DN = 0$); thus, switches S_2 and S_3 are on, but S_1 and S_4 are off. This allows for the charge stored on C_P to transfer to C_L and raise up the V_C voltage. Therefore, the VCO will raise up its output frequency pushing the PLL to lock. The amount of charge transfers every Pump-Up cycle depends on the pulse width of the UP signal. As V_C voltage increases every cycle, the phase difference between the REF and the FB decreases; hence, the UP signal's width decreases and less charge will transfer to C_L and so on till the PLL lock back on the REF frequency. At the end of each Pump-UP cycle, the CP returns to the Idle mode to fully charge up C_P.

Pump-Down: The CP enters this mode when REF lags FB. DN is high ($DN = 1$) and UP is low ($UP = 0$), thus switches S_1 and S_4 are on, but S_2 and S_3 are off. This allows for pulling the stored charge away from C_L, hence lowering the V_C voltage. This decreases the VCO output frequency pushing back the PLL in lock. The amount of pulled charge in every Pump-Down cycle depends on the DN signal's pulse width. As V_C decreases every cycle, the phase difference between the REF and the FB decreases; hence, the DN signal's width decreases, and less charge will be pulled from C_L and so on until the PLL gets back in lock. At the end of each Pump-Down cycle the CP returns to the Idle mode and fully recharges the C_P.

To check the power consumption, at a supply voltage of 1 V the CP has been fed by two out of phase signals ($\Delta\Phi = \pi$) each at a 6.89 MHz frequency – the input reference frequency in the PLL. This should produce the largest pulse width by the CP either on the UP or the DN, depending on either it is a lead or a lag case and both are similar in terms of power consumption. Consequently, this causes the max charge transfer and the max power consumption. The CP total power consumption (P_{CP}) is 187.5 nW.

The whole CP has been on-chip fabricated. Its core CMOS area – without C_P – is 13.17 μm^2 (2.98 μm $\times$ 4.42 μm) and the total area (A_{CP}) – with C_P – is 119.4 μm^2 (10.23 um μm $\times$ 11.67 μm).

5.1.5 Phase-Frequency Detector

Phase-frequency detectors are used in various applications, including radars, interferometers, and system clock. They are used in time-to-digital converters that have broad applications in time-of-flight (ToF) systems and all-digital PLLs [155], successive-approximation-register analog-to-digital converters [156], and time-mode signal processing. The PFD in a PLL plays a key role, along with the proper choice of the CP

topology. It operates in one of the three states shown in Figure 5.7(a). The well-known tri-state PFD, shown in Figure 5.7(b), is a sequential DFF based on a reset feedback loop mechanism. In fact, this architecture suffers from several problems including the

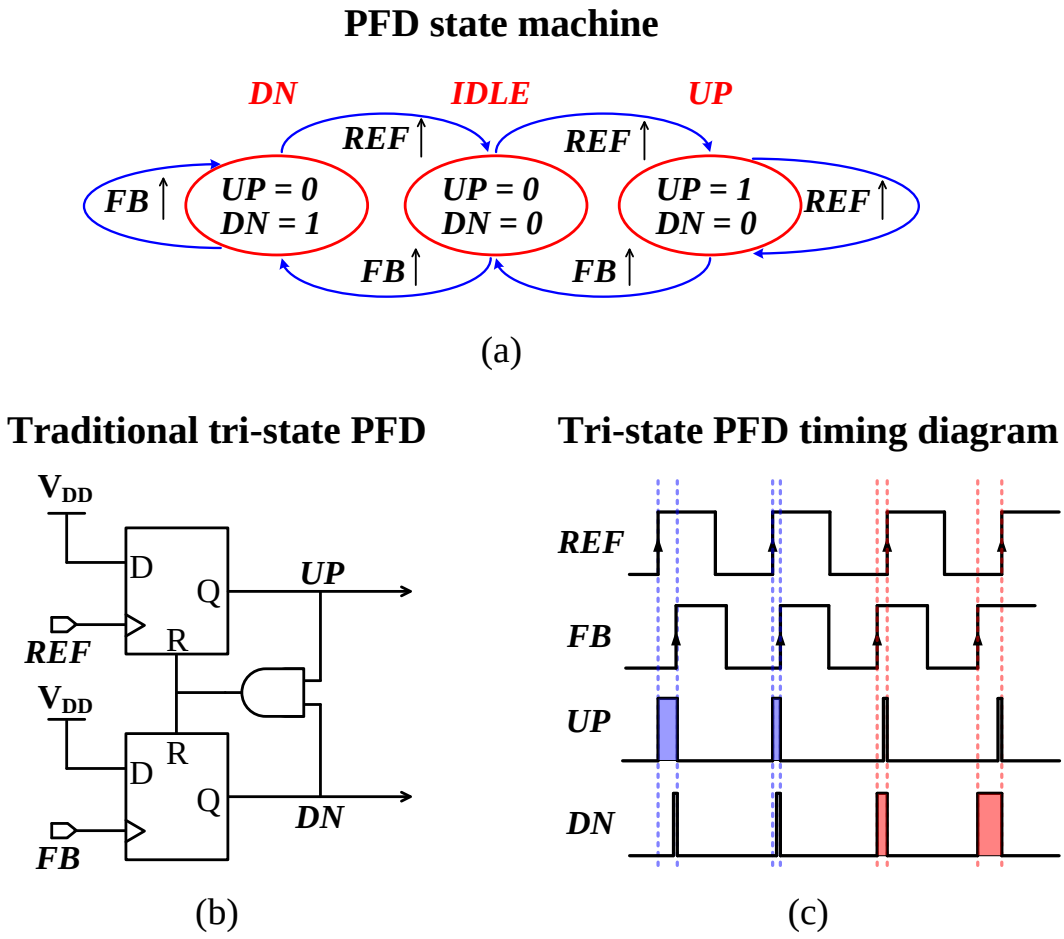


Fig. 5.7 (a) A PFD state machine. (b) Traditional tri-state PFD block and (c) timing diagrams.

mismatch between the fast propagation delay (τ_p) of the DFFs and the slow analog switching times (τ_s) of the CPs' large switches, which causes the dead-zone issue. This is directly responsible for phase noise and spurious tones. Typically, this is mitigated by adding a delay circuit in the feedback reset path, which introduces an undesirable

delay (τ_d) to the PLL control loop contributes significantly to the noise seen as jitter and acts as a source of instability [157]. Other techniques like dynamic-logic PFD (DL-PFD) have been proposed as candidates for a high-frequency operation - they try to mitigate the dead-/blind- zone issues [158]. They operate on creating a delayed version of the input reference signal (REF) and the feedback signal (FB) after the divider in the PLL, with a delay larger than the reset time. The delayed feedback reset mechanism is not guaranteed to work as intended after fabrication and would still need additional calibration circuitry. A direct consequence of adding a delayed feedback path is the generation of an unwanted brief UP/DN 1/1 state to every cycle as shown in Figure 5.7(c), even during phase lock, which causes fluctuations in the CP and contributes to the PLL jitter. This also increases both the power consumption and the delay lock period of the PLL. While addressing the above issues, the PFD proposed here would, (a) improve matching between the PFD logic (τ_p) and the CP (τ_s), (b) balance UP/DN signals for a given phase error, (c) cause no output glitches while in *idle* mode, (d) provide a wide range of frequency operation, and (e) be scalable across different CMOS fabrication processes.

5.2 Proposed PFD Design

The proposed PFD architecture is designed to integrate with a fast-switching accurate charge transfer-based CP, where there is no need for the traditional delayed feedback reset mechanism. Instead, a PFD with the minimal possible delay is required, which in turn allows for a high resolution in phase error correction, resulting in a deficient level of added noise compared to other designs.

5.2.1 Architecture

Figure 5.8 shows the PFD design proposed here, consisting of two branches. One

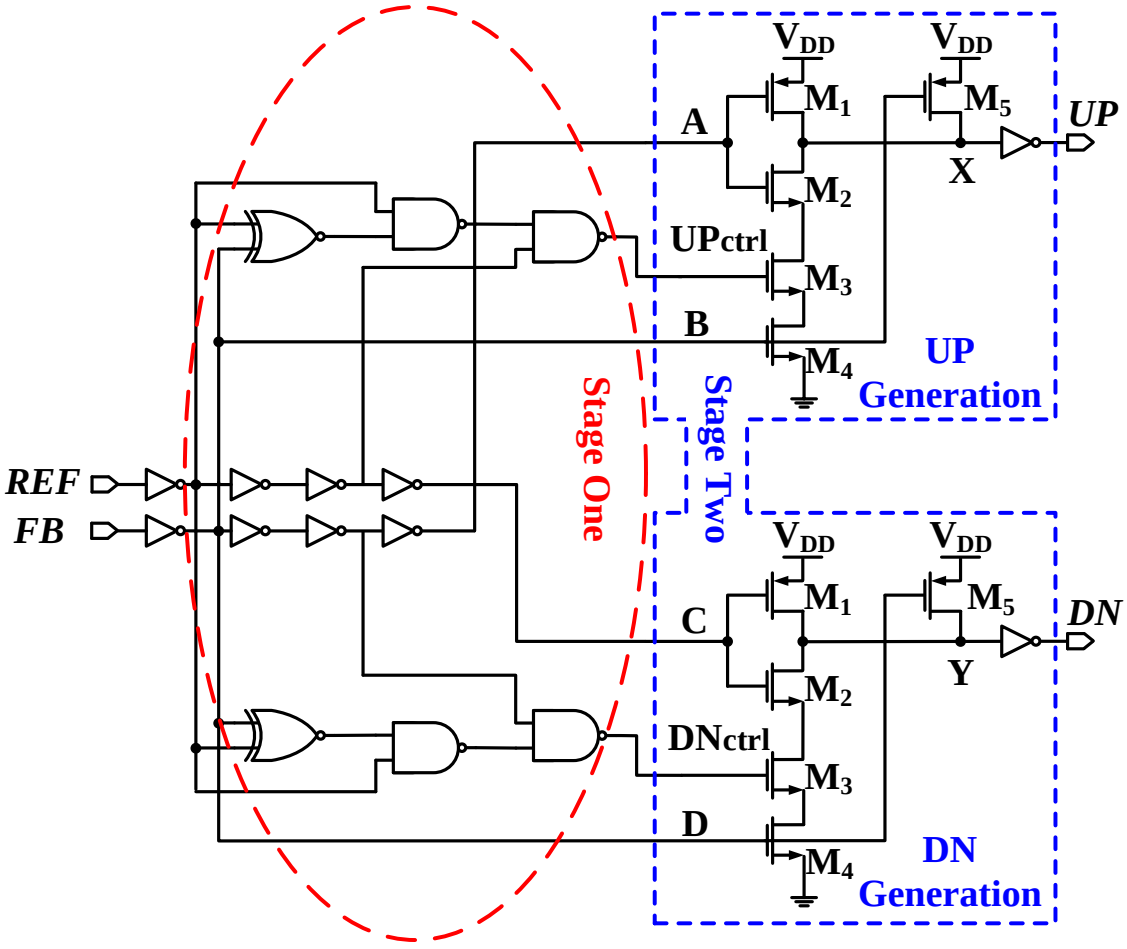


Fig. 5.8 Circuit diagram of the proposed PFD.

branch is responsible for generating the UP signal and resembles a phase-lead case – the REF signal leads the FB signal. The other branch is responsible for the DN signal generation in the case of a phase lag. Each branch consists of two stages. The first stage, shared between both branches, generates a pulse width equal to the phase difference between the two input signals. The inverters in this stage are optimised and used to buffer the signal and guarantee a fast-steep rising edge (τ_r). This pulse is

then used as a control signal for the next stage. The second stage determines whether it is a phase lead or lag situation. Hence, it allows for only either an UP or a DN signal to be generated at any time. The inverter at the end buffers the output for better driving capability while delivering a positive pulse signal at node X (Y). The two stages operate together to replace the usage of DFFs, and the feedback reset path mechanism commonly used in many PFD designs. Hence, no reset or dead-/blind-zones are present in this design. The system is enabled all the time and would not miss any of the edges at the inputs.

5.2.2 Circuit Design and Operation

As shown in Figure 5.8, the first stage consists of two NAND gates and one XNOR gate to measure the phase difference between the two input signals. Hence, an output control pulse with a width equal to the difference between the two input edges (Δt_{in}) appears at the output of the first stage. The second stage is implemented with five transistors per branch. Transistors M_1-M_4 act as a pull-down network that pulls down node X (Y) for a period of time equal to the input phase difference while blocking the other branch from generating any pulses - it guarantees that X and Y are never enabled at the same time. Transistors M_5 are responsible for pulling up node X (Y) at the end of the created pulse. After the inverter, a positive pulse with a width equal to the phase difference between the REF and the FB input signals is created at one of the two branch outputs, depending on whether it is a phase lead or lag case.

5.2.3 Performance and Robustness

The proposed PFD is developed in the TSMC 65 nm CMOS process technology. An open-loop simulation test is performed to check the PFD performance. First, a sweep

test was carried out to check the resolution and the linearity over different input phase differences in the time domain based on the Δt_{in}. The results shown here are based

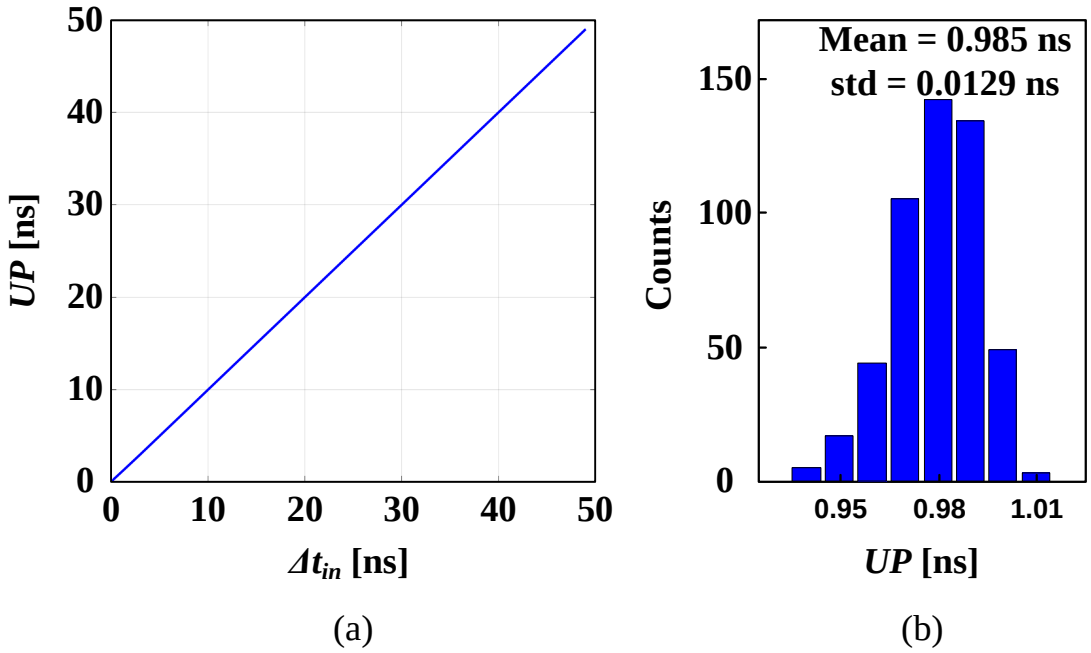


Fig. 5.9 Proposed PFD: (a) transfer curve, (b) Monte-Carlo histograms (N=500) of the UP output at $\Delta t_{in} = 1$ ns.

on a phase-lead case. Similar results are obtained for a phase-lag case. Figure 5.9(a) shows the output response of the PFD for different Δt_{in}, when the REF signal leads the FB signal. The linear range starts from as low as 100 ps of resolution.

To test the sensitivity of the proposed PFD circuit over transistor mismatches among the digital components, a Spectre post-layout simulation was carried out on the circuit shown in Figure 5.8 using a Monte-Carlo analysis, with several runs $N = 500$. Figure 5.9(b) shows the histogram of the PFD output for a $\Delta t_{in} = 1$ ns. It reports a mean of 0.985 ns and a standard deviation (std) of 0.0129 ns.

An error defined as:

$$Error = \frac{|PW_{out} - \Delta t_{in}|}{\Delta t_{in}} \times 100\%, \tag{5.1}$$

is calculated for different Δt_{in}, where Δt_{in} is the input time difference, and PW_{out} is the corresponding pulse width output. Figure 5.10 shows the post-layout simulated error over three process corners (FF, TT, SS), supply variation range (1V±0.05V) and temperature between (-10℃→+80℃), to test the design robustness over the process, voltage, and temperature (PVT) variations. The graph indicates a max error of ±3%

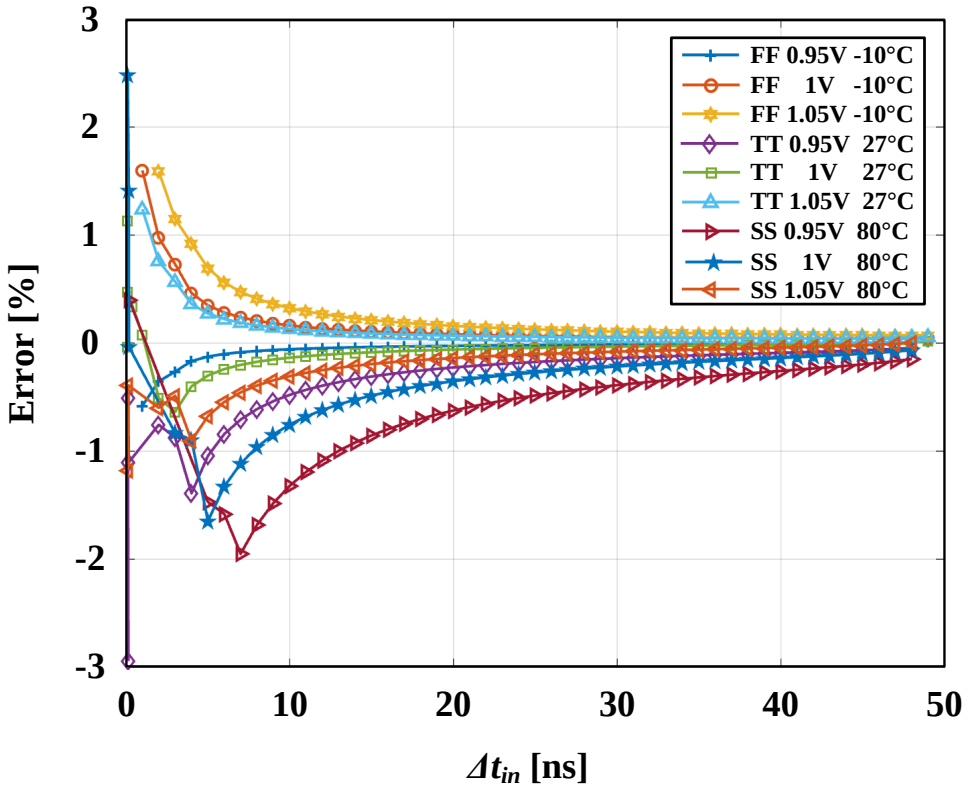


Fig. 5.10 Error under PVT variations.

in the pico-second range for all corners.

5.3 Experimental Validation

To validate the fabricated design, the PFD CMOS circuit has been tested separately in an open-loop configuration, while being loaded by the charge-based CP, to validate its performance. Then, testing the entire closed-loop system was performed after wire bonding the CMOS circuits to the MEMS resonator to realize the overall targeted system.

5.3.1 PFD Validation

A measurement setup has been built to test the PFD separately in an open-loop configuration without being connected in a closed-loop PLL. A copy of the designed PFD loaded with a charge-based CP has been added separately on the die for the sake of carrying out this test without probing the closed-loop PLL. Figure 5.11(a) shows the micrograph of the fabricated die highlighting the separate PFD block with its dedicated driving stage. The driving stage is used to drive the measuring equipment in the PFD stand-alone measurement. It is not a part of the fully integrated PFD in the closed-loop PLL. The total active PFD CMOS area is 92.29 μm^2 (9.86 μm $\times$ 9.36 μm). The CMOS die assembled in an 80-pin ceramic quad flat pack (CQFP) package and then mounted on a custom 4-layer printed circuit board (PCB) as shown in Figure 5.11(b). The PCB includes SMA connectors for different input/output signals and a voltage regulator (Analog Devices ADP1707ARDZ-1.2-R7) that regulates the input supply from the DC supply source (Agilent E3646A). In addition, all power nets have been decoupled with a network of decoupling capacitors (10 nF, 100 nF, 1 μF). The decoupling capacitors are connected in parallel and assembled in ascending order from the integrated circuit (IC) package lead. There are other components on the PCB

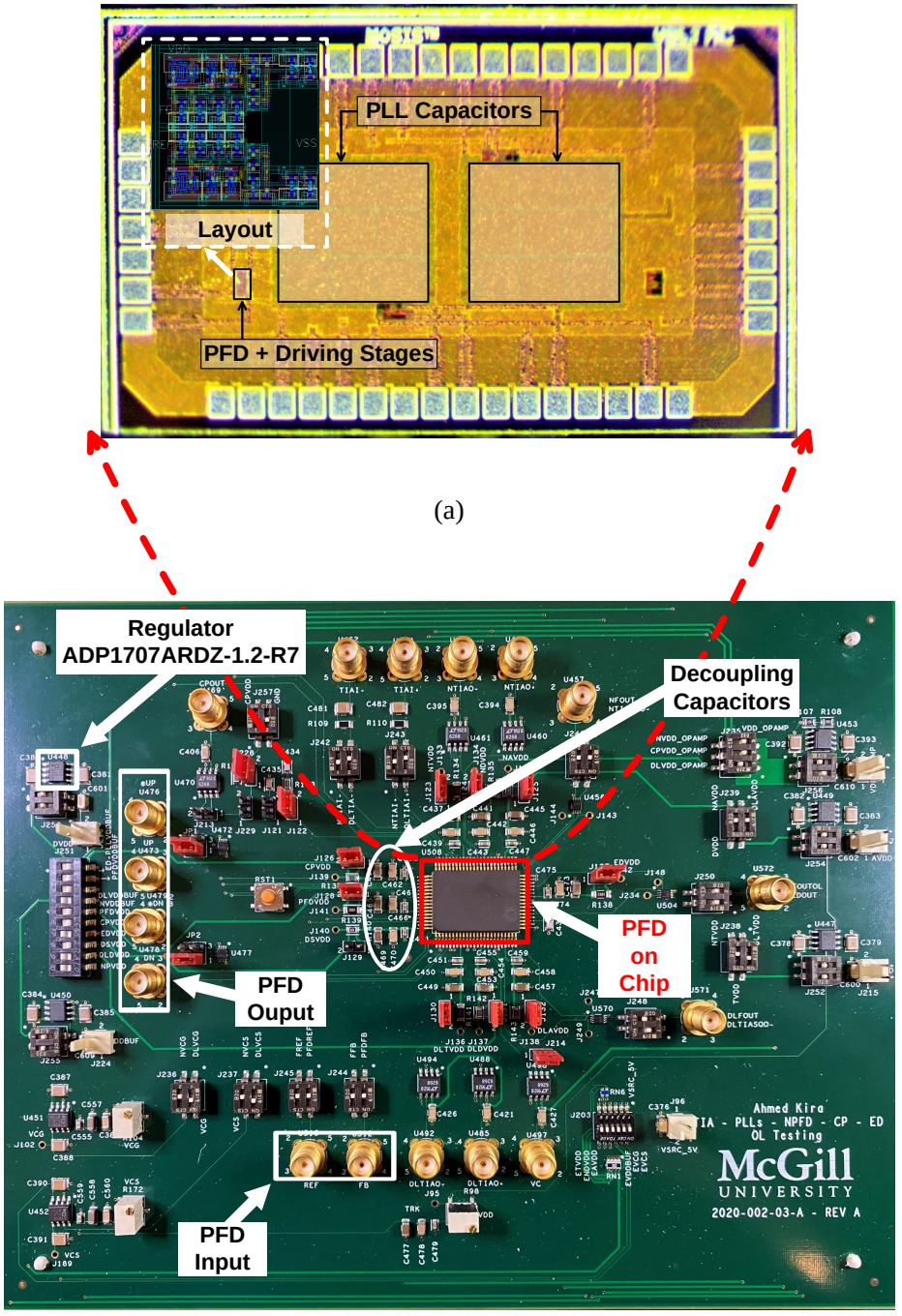
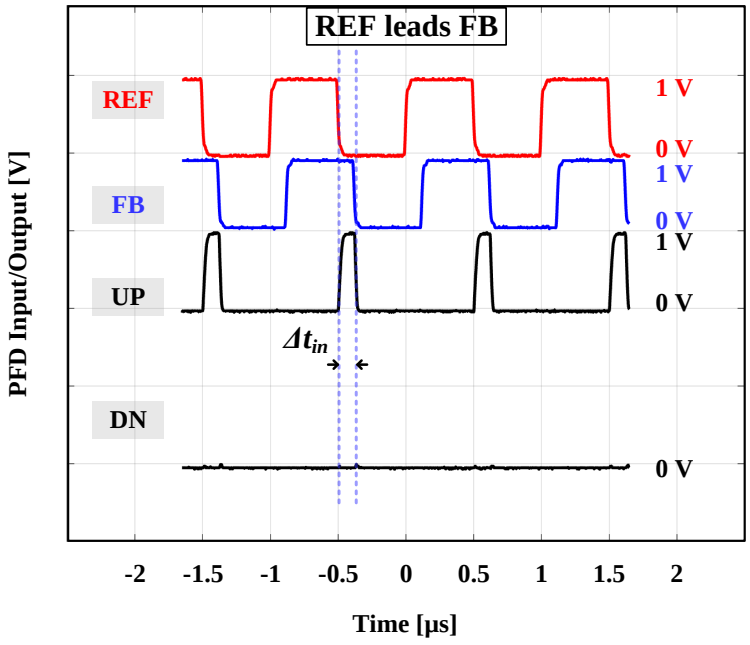


Fig. 5.11 (a) Fabricated die micrograph, (b) photograph of the testing board used to test the PFD.

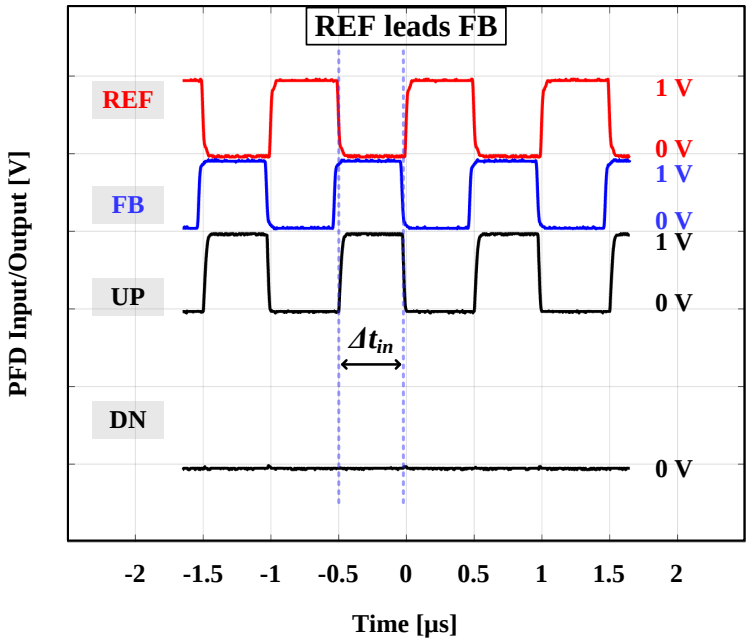
shown in Figure 5.11(b) that are not related to this specific PFD test.

Two input 1 V peak-to-peak synchronous square wave signals (REF and FB) were synthesized using two synchronized clock generators (Stanford Research Systems - Model CG635 - 2.05 GHz Synthesized Clock Generator) to feed the PFD block under test. One CG635 clock generator is used to generate the REF signal, and the other one is used to generate the FB signal with a controllable Δt_{in} time difference (phase shift) out of the REF signal. An oscilloscope (Keysight/Agilent MSO-X 92504A) is used to display the PFD input, REF and FB signals. Another oscilloscope (Tektronix MSO71254C) is then used to monitor the 4 PFD output signals: UP, $\overline{UP}$, DN, and $\overline{DN}$. Figure 5.12(a) shows the measurement of the PFD output at a 1 MHz operating frequency when REF leads FB by $\pi/4$ (Δt_{in} = 125 ns), and Figure 5.12(b) shows the case of REF leading FB by almost π (Δt_{in} = 470 ns). Obviously, there are not any generated pulses or glitches on the DN output in both cases. Figure 5.13(a) depicts the case when REF lags FB by $-\pi/4$ (Δt_{in} = -125 ns) and Figure 5.13(b) shows the case when REF lags FB by almost $-\pi$ (Δt_{in} = -470 ns). Similarly, no pulses or glitches are generated on the UP output.

Figure 5.14 shows the measured Error of the PFD. It reports a maximum absolute measured Error of around 1.6% in the pico-second range of Δt_{in} and $\leq$ 1% in the nano-second range. The result is in good agreement with the simulation. The PFD frequency normalized power consumption (P_n) is 0.106 pW/Hz at a 1 V supply voltage. The performance of the proposed design is summarized in Table 5.1, with other works reported in the literature. Compared to other designs, this work reports the lowest P_n, the lowest percentage of error in the PFD output, and a competitive maximum operating frequency (f_{max}) covering the intended application range of operation. The actual measurement setup and its block diagram are depicted in Figure 5.15.

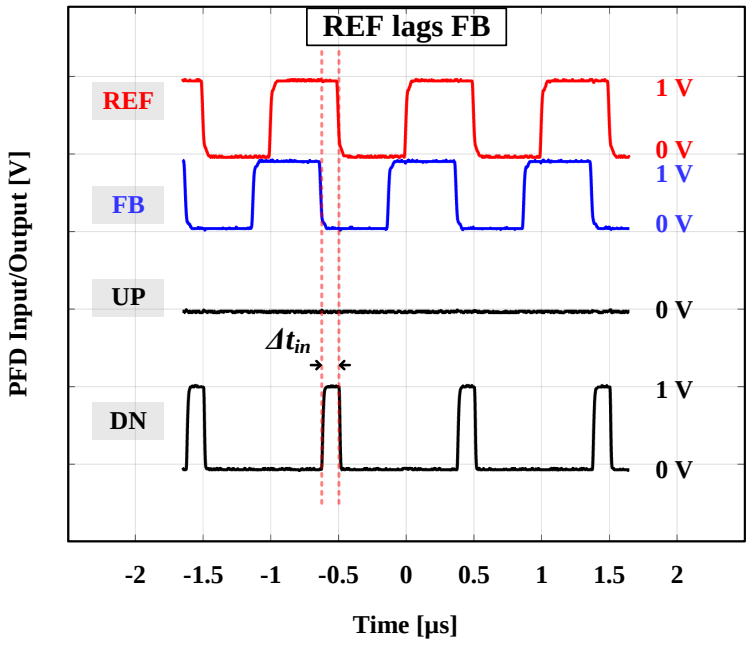


(a)

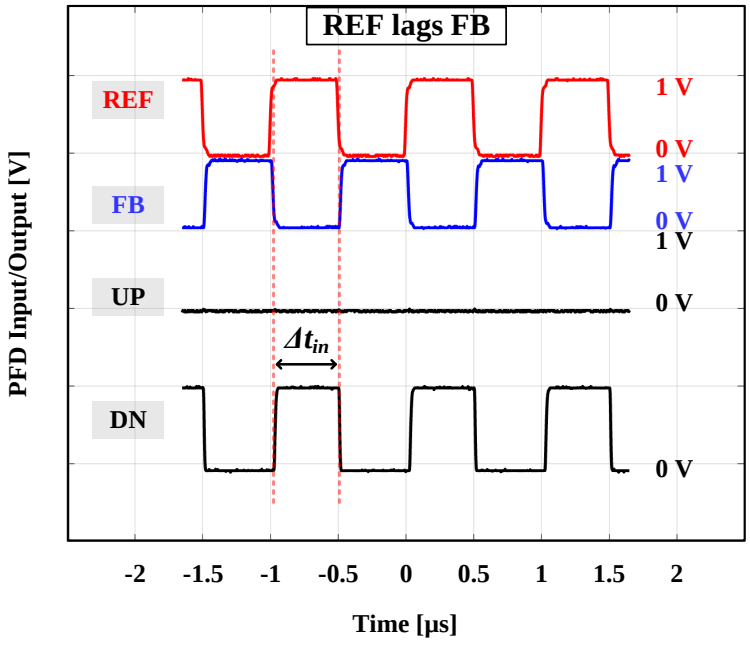


(b)

Fig. 5.12 *REF* leads *FB*: (a) $\Delta t_{in} = 125$ ns, and (b) $\Delta t_{in} = 470$ ns.



(a)



(b)

Fig. 5.13 *REF* lags *FB*: (a) Δt_{in} = -125 ns, and (b) Δt_{in} = -470 ns.

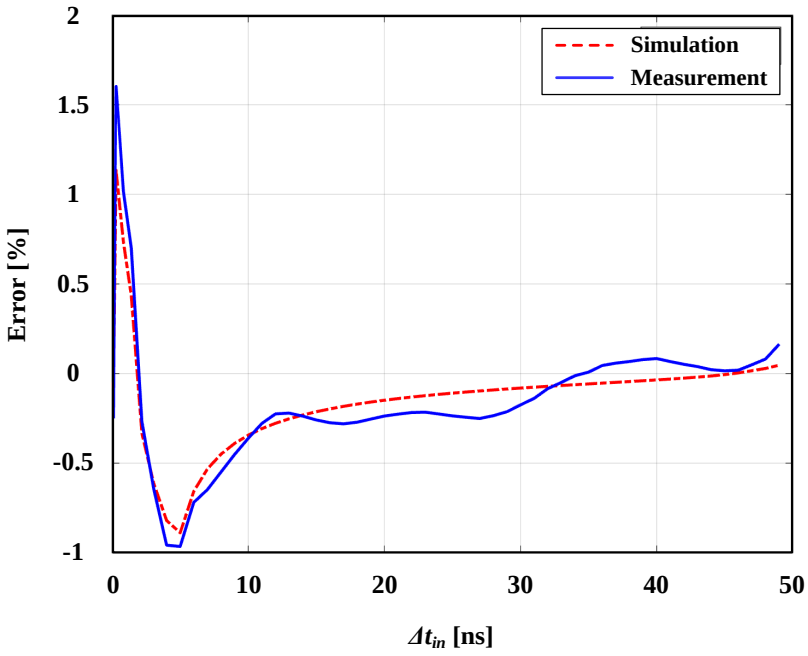


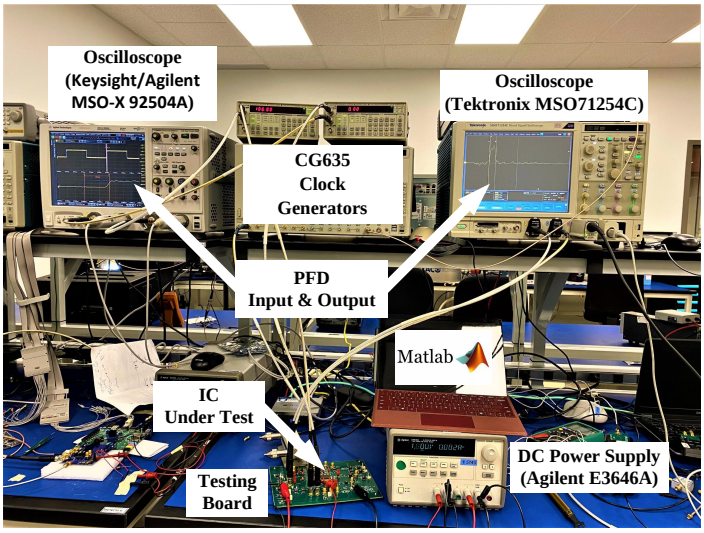
Fig. 5.14 Measured PFD Error compared to simulation.

Table 5.1 PFD Performance Summary and Comparison.

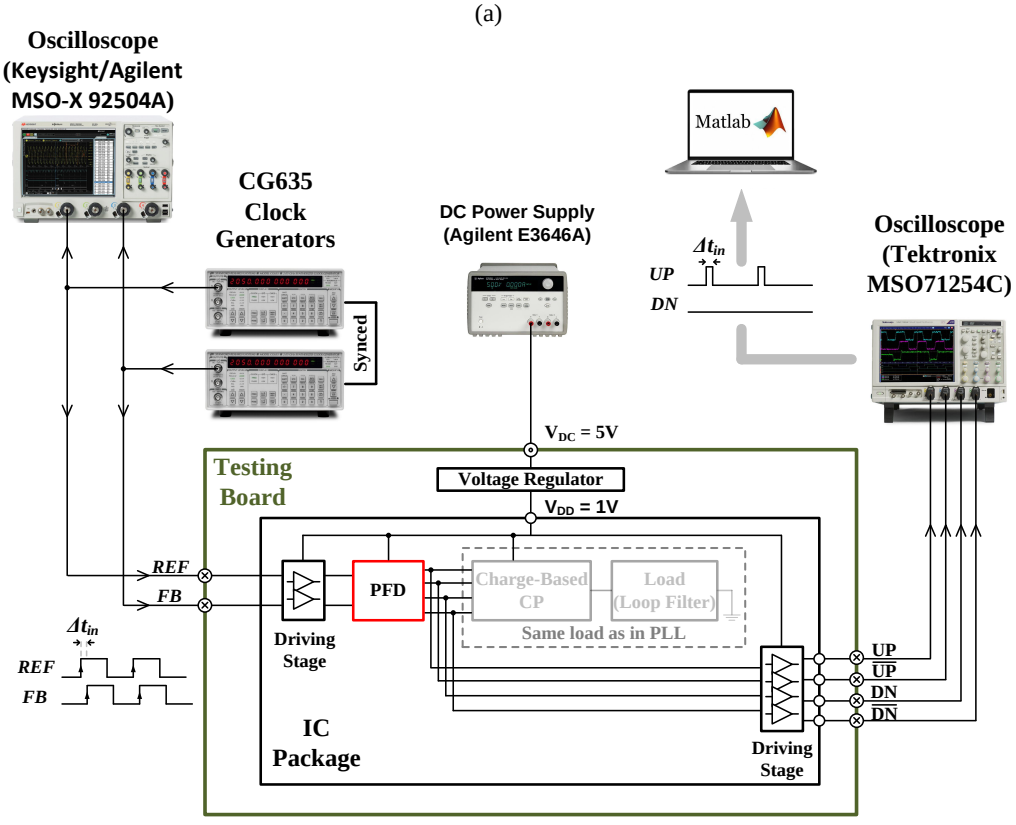
Ref. No.	[159]	[160]	[161]	**This Work**
Process (nm)	90	65	180	**65**
Supply (V)	1.2	1.2	1.8	**1**
P_n (pW/Hz)	-	0.62	0.132	**0.106**
f_{max} (GHz)	6	0.1	2.5	**2.5**
Dead-zone (ns)	near 0*	-	free	**free**
Error (% $\leq$)	$\pm$15	$\pm$12•	-	**$\pm$1.6**

* The author has not shown how much it is close to 0.

• Extracted from the reported results.



(a)



(b)

Fig. 5.15 PFD stand-alone validation: (a) picture of the actual setup and (b) setup block diagram.

5.3.2 Prototype and Overall Closed-Loop System Validation

The loop is then closed, connecting the MEMS resonator to the TIA, forming the MEMS oscillator to test the overall system, the PLL with input reference MEMS-based oscillator. Table 5.2 shows the summary of the TIA open-loop performance parameters presented in Chapter 3. The MEMS and CMOS dies are wire bonded to

Table 5.2 TIA Open-Loop Performance Summary.

Parameter	Measured Values
Process (nm)	65
Supply (V)	1
Gain (dBΩ)	107.9 →118.1
Duty-Cycle (%)	23.25 →79.03
Power Consumption (nW)	143
Active CMOS Area (μm^2)	150.29

each other. The wire bonding diagram is provided in Figure 5.16. The 80-pin quad flat no-lead (QFN) package has been used for packaging. As mentioned earlier, the QFN package pads have less loading capacitance than the pads of the quad flat pack (QFP) [125, 127]. A different custom PCB was used for this test. A network of decoupling capacitors (10nF, 100nF, 1μF) is connected in parallel and assembled in ascending order from the lead of the IC package to decouple all the power nets. The MEMS V_P has been supplied by the DC power supply source (BK PRECISION 9110) with a 1 MΩ resistor connected in series between the resonator and the supply generator. The 1 MΩ series resistor helps limit the maximum supply current on the polarization terminal in the case of pull-in between the MEMS device electrodes. The CMOS circuits have been supplied with a 1 V supply voltage from another DC supply source (Agilent E3646A). The MEMS (V_P) has been gradually raised up to notice the MEMS behavior, a stable output reached at $V_P = 40V$. Figure 5.17 shows the phase noise of the

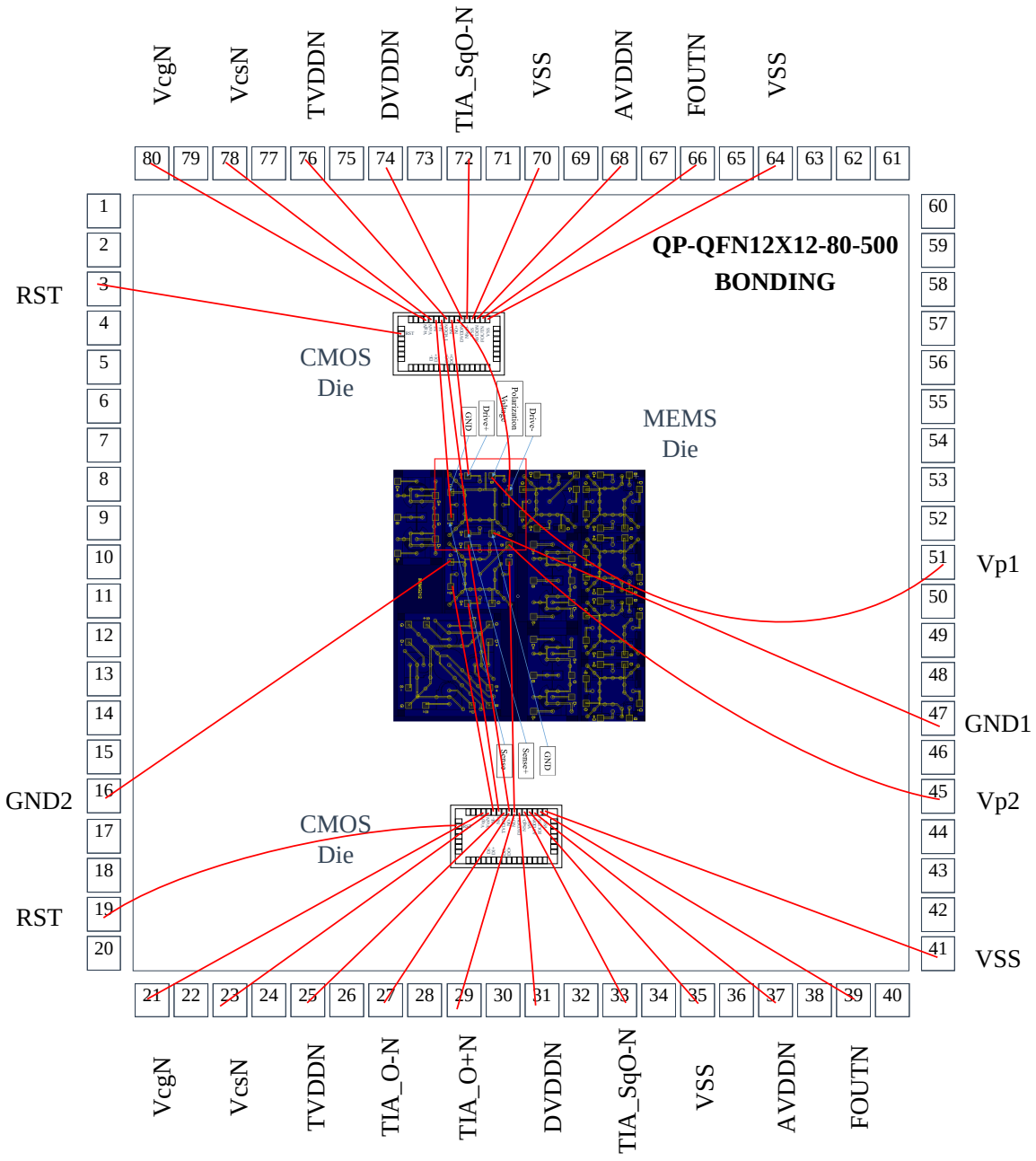


Fig. 5.16 Wire bonding diagram of the MEMS and the CMOS dies in an 80-pin QFN package.

output after the PLL. It reports a phase noise of -106.21 dBc/Hz and -135.36 dBc/Hz at 1 kHz and 1 MHz offsets, respectively. Table 5.3 summarizes the occupied area of the

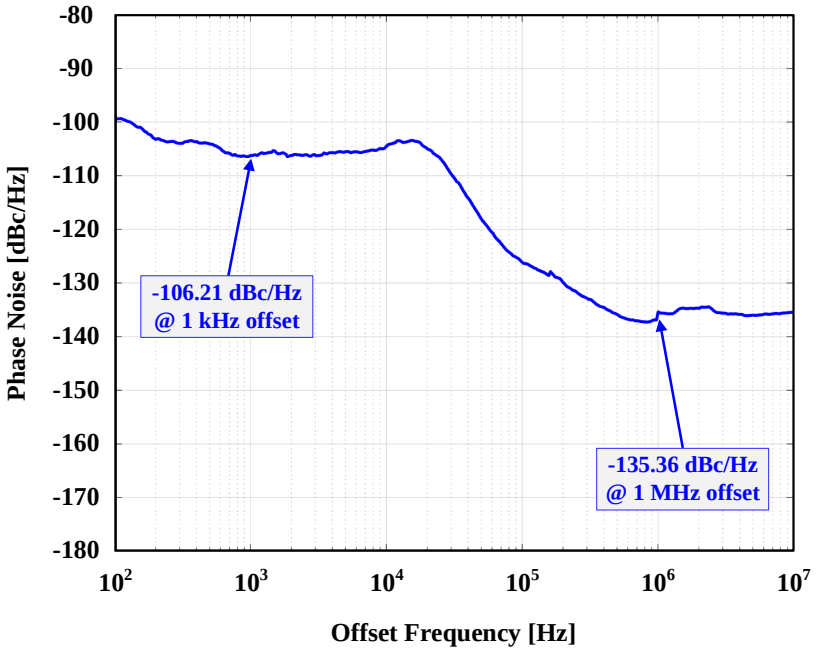


Fig. 5.17 Measured phase noise at 110.2 MHz output frequency.

different blocks in the PLL. At a 1 V supply, the total power consumption of the PLL is

Table 5.3 Area of the PLL different sub-blocks.

Block	Area (μm^2)
PFD	92.29
CP	119.4
LF	102700
VCO	30.16
Divider	106.76

6.566 μW and the system total power consumption (P_{DC}), the TIA and the PLL, is 6.709 μW. Figure 5.18 shows the breakdown of the system power consumption at 110.2 MHz output frequency. Figure 5.19 shows the wire-bonded dies in the mounted

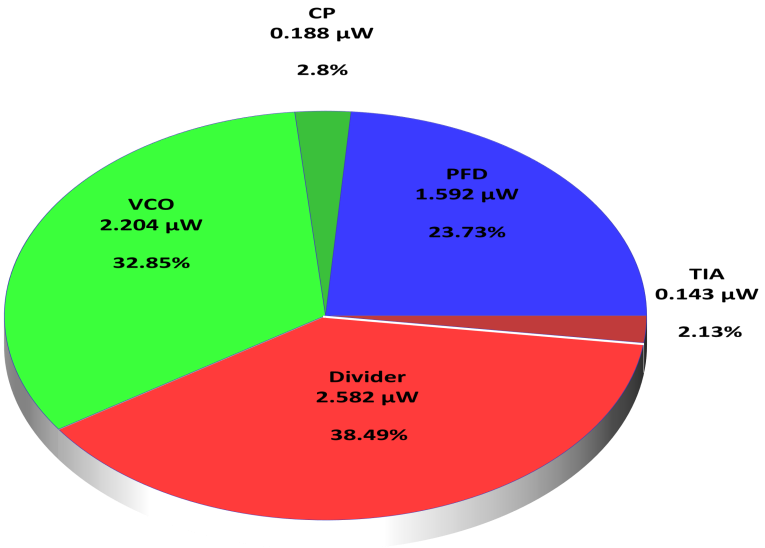


Fig. 5.18 Power consumption breakdown of the system at 110.2 MHz output frequency.

package and the testing PCB.

To compare the performance of different oscillators fairly, a well-known figure-of-merit, used by [12, 130], and based on the oscillator noise and power consumption has been utilized in this work. It normalizes the oscillator phase noise at a specific offset frequency (Δf) to the oscillator's frequency of oscillation (f_o) and to the DC power consumption [92]. The FoM is expressed as:

$$FoM = \mathcal{L}(\Delta f) - 20\log(\frac{f_o}{\Delta f}) + 10\log(\frac{P_{DC}}{1\ mW}), \tag{5.2}$$

$\mathcal{L}(\Delta f)$ is the oscillator output phase noise at a specific offset frequency (Δf), f_o is the oscillator frequency of oscillation, and P_{DC} is the oscillator DC power consumption in milliwatts.

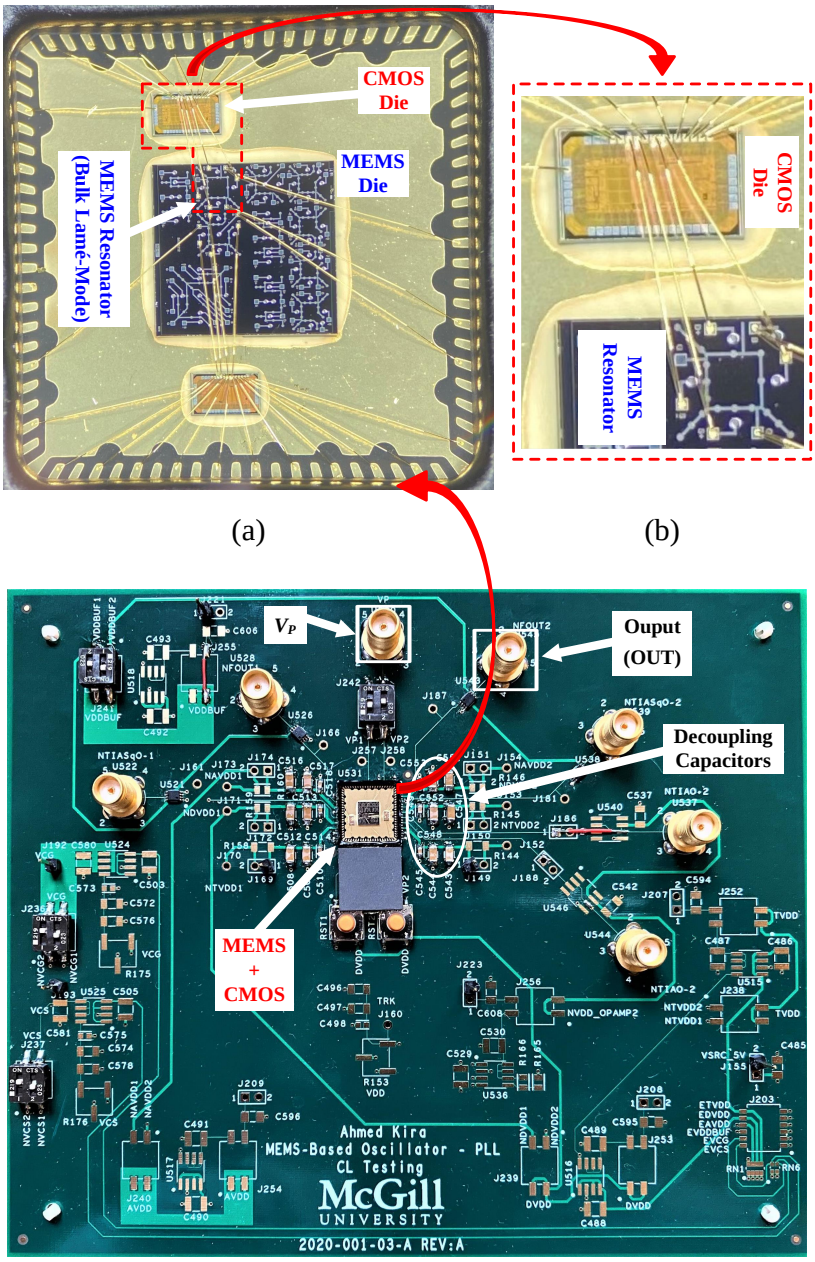


Fig. 5.19 (a) Picture of the wire bonded dies in the package. (b) Zoomed-in capture for the MEMS device wire bonded to the CMOS die forming the system. (c) Photograph of the testing board used to test the system.

The FoM has been used in Table 5.4 to compare this work with previously published state-of-the-art. The system demonstrated in this work reports a competitive high performance compared to other works reported in the literature. The achieved FoM is mainly due to the low amount of power consumed by the system while delivering a competitive noise performance.

Table 5.4 System Performance Summary and Comparison to the State-of-the-Art.

Ref. No.	[130]•	[162]	[163]•	[164]	[165]	[166]	**This Work**
Process (nm)	180	65	180	40	65	65	**65**
PLL Architecture Type	Analog Fractional-N	Digital Fractional-N	Analog Fractional-N	Analog Integer-N	Analog Integer-N	Digital Integer-N	**Analog Integer-N**
Supply voltage (V)	-	0.85$^{\otimes}$	1.5^{+}	1	1	0.8*	**1**
Reference Frequency (MHz)	27.19	10	5	250*	10	2*	**6.89**
Output Frequency (MHz)	75.01	2466	100*	25000*	1000	240*	**110.24**
P_{DC} (μW)	7800	265	3000$^{\$}$	1080	320	63.5	**6.709**
Power Efficiency (μW/MHz)	103.99	0.1075	30	0.0432	0.32	0.26	**0.0609**
Core CMOS Active Area (mm^2)	5$^{"}$	0.25	0.36	0.0048	0.315	0.016	**0.1095**
$PN\|_{1\text{ kHz}}$ (dBc/Hz)	-108	-68	-84.2907	-98$^{!}$	-64$^{!}$	-44.34	**-106.21**
$PN\|_{1\text{ MHz}}$ (dBc/Hz)	-133.15	-105	-134.1	-121.1	-73	-76.48	**-135.36**
$FoM\|_{1\text{ kHz}}$ (dB)	-196.58	-190.07	-179.52	-246.29	-179.05	-139.97	**-185.32**

• The used input reference: MEMS-based input reference oscillator.

$^{\otimes}$ The DCO works at 0.45 V supply, while the rest of the DPLL is supplied with a 0.85 V supply.

$^{+}$ Internal supply voltage of the core CMOS circuits.

* Selected value by the author of the paper, from a tunable range, at which he measured the reported data.

$^{\$}$ Estimated for internal, core CMOS, PLL circuit blocks.

$^{"}$ The whole ASIC CMOS chip size, core areas of different circuits are not mentioned.

$^{!}$ Deduced from the reported data.

Chapter 6

Conclusion and Future Work

This chapter concludes the research introduced in this dissertation. The first section covers the main outcomes and contributions. The second section discusses the different proposed ideas to extend this research in the future.

6.1 Summary

This dissertation presents a MEMS-based oscillator for frequency reference applications focusing on power consumption, size, and circuit designs that can be easily adopted in advanced CMOS technology processes.

The first part of this dissertation introduces the MEMS-based oscillator. An extremely low-power, tunable gain/duty-cycle TIA. The TIA was integrated with a very high-quality factor (Q) bulk Lamé-mode MEMS resonator to implement an oscillator with competitive performance in terms of power consumption and phase noise. The TIA structure is based on the self-cascoding technique. The TIA has been fabricated in a TSMC 65 nm CMOS process. Experimental validations, an open-loop and a closed-loop, have been carried out to test the TIA performance. The TIA has a tunable gain

from 107.9 dBΩ to 118.1 dBΩ and a tunable duty-cycle between 23.25% and 79.03%. The TIA occupies a total active CMOS area of 150.29 μm^2 and consumes 143 nW at a 1 V supply. The proposed design enables the TIA to be easily transferred and adopted into new advanced CMOS technologies with lower supply conditions, thanks to the self-cascoding technique used. The oscillator reaches a phase noise of -128.1 dBc/Hz and -133.7 dBc/Hz at 1 kHz and 1 MHz offsets, respectively.

The second part of the dissertation covers the implementation of a 110.2 MHz ultra-low power PLL using a MEMS-based input reference oscillator as a replacement for external quartz crystal-based reference. The design focuses mainly on achieving minimum PLL power consumption and footprint area. A charge-based CP has been adopted in this design instead of the standard current-based CP. It overcomes the current-based CP challenges including, static power consumption, the need of matching circuitry, slow switching time, sensitivity to process variations, current leakage, limited headroom, and overhead time needed to transfer the design to an advanced CMOS technology processes.

An ultra-low-power, dead-/blind- zone free, glitch-free, high-resolution PFD was successfully implemented. The PFD structure consists of two branches with two stages that replace any feedback reset mechanism and allow only for the generation of either UP or DN signal at a time. A stand-alone experimental validation has been done for the PFD separately. Results report a resolution of 100 ps with less than ±1.6% error and a frequency normalized power consumption (P_n) of 0.106 pW/Hz. They show a compact, accurate, and efficient PFD with a competitive performance compared to the other in the state-of-the-art.

The whole system has been fabricated in a TSMC 65 nm CMOS process and experimentally validated to test the overall performance. It occupies a total active CMOS

area of 0.1095 mm^2 and consumes a total power of 6.709 μW at a 1 V supply. The system phase noise is -106.21 dBc/Hz and -135.36 dBc/Hz at 1 kHz and 1 MHz offsets, respectively. The proposed design can be easily transferred and adopted into new advanced CMOS technologies with lower supply conditions.

6.2 Future Work

Based on the work done in this research, some suggested ideas can be considered to extend the current research work in the future. With the emergence of MEMS technology for different applications, the need to develop CMOS interfacing circuits increases. TIAs are among the most crucial interface circuits. Therefore, the future work on them can include:

- extending the current design to include a tunable bandwidth technique and accommodate it for other types of MEMS resonators and applications,
- testing with other MEMS resonators,
- implementation of the current design in advanced transistor process technologies, including fin field-effect transistor (FinFET) whenever available.

For the PLL, the future work can include:

- exploring other VCO types that focus more on noise performance for other applications, including injection locking and charge coupling based VCOs
- designing a fractional-N PLL based on the same MEMS resonator as a reference frequency source, synthesizing multiple frequencies targeting RF communication applications.

- using a metal-oxide-metal (MOM) capacitor instead of Metal-insulator-metal (MIM) whenever available in the process design kit (PDK). MOM capacitors offer a higher capacitance density allowing for a smaller footprint area.

For the whole system, the PLL with the input reference MEMS-based oscillator, the future work can comprise:

- exploring 3-D system-in-package (SiP) integration for the MEMS and CMOS dies, including die interposer,
- delivering a fully monolithic system.

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