Resonant tunneling in gallium nitride and aluminum nitride nanowire heterostructures

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Abstract

III-V gallium nitride and aluminum nitride semiconductor nanowire heterostructures have emerged as promising candidates for numerous photonic device applications, ranging from the visible to the near-, mid- and far-infrared spectral range. In this work, the electrical properties of gallium nitride and aluminum nitride nanowire heterostructures were studied in the context of resonant tunneling. The negative differential resistance was observed in current-voltage measurements at room temperature and at 77 K for single nanowire devices as well as for large area devices, confirming the presence of resonant tunneling through the aluminum nitride barriers. Effects of different silicon doping profiles have also been discussed. This work represents a preliminary step in developing gallium nitride and nanowire based intersubband devices such as quantum cascade lasers and infrared-based photodetectors.

Résumé

Les nanofils semi-conducteurs hétérostructurés composés de nitrure de gallium et d'aluminium III-V ont émergé comme des candidats prometteurs pour de nombreuses applications de dispositifs photoniques, allant de la lumière visible à l'infrarouge proche, moyen et lointain. Dans ce projet, les propriétés électriques et l'effet tunnel résonnant de nanofils semi-conducteurs hétérostructurés de nitrure de gallium et d'aluminium ont été étudiés. La résistance différentielle négative a été observée dans les mesures de courant-tension à la température ambiante et à 77 K pour les dispositifs à un seul nanofil ainsi que des dispositifs de grande surface avec plusieurs nanofils, ce qui confirme la présence d'effet tunnel résonnant à travers les barrières de nitrure d'aluminium. Les effets des différents profils de dopage de silicium ont également été discutés. Ce travail représente une étape préliminaire dans le développement des appareils intersousbandes de nanofils de nitrure de gallium tels que les lasers à cascade quantique et photodétecteurs infrarouge.

Acknowledgements

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Chapter 1 – Introduction

The electron transport and resonant tunneling properties of semiconductor multiple quantum well (MQW) heterostructures was first studied by Esaki and Tsu (1970). A MQW consists of several thin layers of a low band gap semiconductor (typically with thicknesses < 10 nm) acting as the quantum wells which are confined between two other thin layers made up of a different high band gap semiconductor acting as the potential barriers. The quantum wells can effectively trap electrons in one of their discrete finite energy states.

In the following year, it was proposed by Kazarinov and Suris that superlattice heterostructures could be used for the generation and amplification of electromagnetic waves via intersubband transitions (ISBT) (Kazarinov and Suris, 1971). Intersubband transitions, as opposed to the typical interband transitions, permits for low energy absorption and emission of infrared photons. This opened up the possibility of designing MQW heterostructure devices, such as the quantum cascade laser with emission spectra in the mid- and far-infrared, for numerous imaging and sensing applications such as high-resolution spectroscopy, terahertz imaging for non-invasive inspection, and plasma diagnostics (Williams, 2007; Hu, 2008). Beyond ISBT and imaging applications, semiconductor MQW heterostructures are used in blue light emitting diodes (LED), ultra-fast oscillators, as well as in functional devices such as multiple-valued memory cells (Yang et al., 2000; Seabaugh et al., 1992).

For the imaging applications, however, light amplification requires not only the ISBT property, but also resonant tunneling. Resonant tunneling is the phenomenon in which electrons travel, in a non-classical fashion, through potential barriers into a resonant quantized state. A MQW device utilizing resonant tunneling is simply called a resonant tunneling diode (RTD). Hence, one can imagine a system with multiple potential barriers and wells in which electrons tunnel across the RTD and relax from one finite energy state to the next within the same conduction band for each quantum well, effectively releasing several low energy photons.

Resonant tunneling can be identified through electrical measurements such as by observing the negative differential resistance (NDR) in the current-voltage (I-V) characteristics. NDR is characterized by a negative I-V slope, as shown in the theoretical non-linear curve in figure 1.1, and manifests itself in systems such as MQW heterostructures. It can, thus, be said that NDR is the signature property of resonant tunneling (Capasso and Kiehl, 1985), and by extension the benchmark of ISBT.

Devices exhibiting negative differential resistance, including tunnel diodes and Gunn diodes, are classified as non-ohmic. In the case of devices with I-V characteristics similar to the one in figure 1.1, the static resistance R (equation 1.1) remains always positive whilst the differential resistance r (equation 1.2) becomes negative between the peak voltage V_{peak} and the valley voltage V_{valley}. Moreover, we can define the peak-to-valley ratio (PVR) as the ratio between the

peak current I_{peak} and valley current I_{valley}. The PVR is a useful measure of the performance of these devices.

$$R = \frac{V}{I} > 0 \quad \text{(Eq. 1.1)}$$

$$r = \frac{dV}{dI} \quad \text{(Eq. 1.2)}$$

$$Peak\ to\ valley\ ratio = PVR = \frac{I_{peak}}{I_{valley}} \quad \text{(Eq. 1.3)}$$

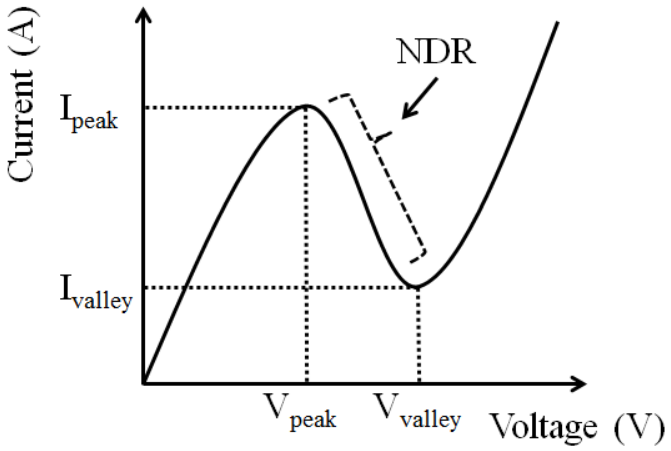


Fig. 1.1 – Theoretical current-voltage curve showcasing negative differential resistance.

For the past two decades, research groups have studied MQW heterostructures used for intersubband absorption and emission of infrared light. Specifically, III-V and II-VI semiconductors such as gallium arsenide / aluminum gallium arsenide (GaAs/AlGaAs), indium arsenide / aluminum antimonide (InAs/AlSb), and zinc oxide / magnesium zinc oxide (ZnO/MgZnO) have been reported (Helm et al., 1988; Warburton et al., 1995; Ohtani et al., 2009). More recently, lots of work has been done on gallium nitride / aluminum gallium nitride (GaN/AlGaN), semiconductors known for their high breakdown voltage and high

heat capacity. Furthermore, GaN and its nitride alloys have many properties that favour ISBT, outlined in Chapter 2.

Resonant tunneling diodes, on the other hand, have been around since the beginning of the 1970s and have seen a huge surge in development in the 1980s due to the emergence of molecular beam epitaxy (MBE). MBE enabled researches to grow higher quality heterostructures with high control of the quantum well and potential barrier thicknesses, resulting in more pronounced NDR characteristics. In 1983, Sollner and his team demonstrated a single quantum well GaAs-based resonant tunneling diode capable of signal mixing at frequencies up to 2.5 THz (Sollner et al, 1983). This work stimulated efforts for terahertz operating resonant tunneling diodes.

The first GaN/AlN resonant tunneling diode was fabricated by Kikuchi et al. (2001). Kikuchi was able to grow a MQW GaN-based planar heterostructure and achieved an NDR with a peak-to-valley ratio just under 10 at room temperature (RT), shown in figure 1.2. However, Kikuchi's results were criticized by Belyaev for not performing both positive and negative sweeps, saying that the NDR property is highly sensitive to the measurement method (Balyev et al., 2003). In 2006, Golka fabricated planar GaN/AlGaN double barrier resonant tunneling diodes with a peak-to-valley ratio of 2 at RT (Golka et al., 2006). In 2010, the first GaN/AlN MQW nanowires were grown by molecular beam epitaxy (MBE) with small NDR being observed at up to 250 K, shown in figure 1.3 (Rigutti et al., 2010). Nanowire structures are favored over planar ones because of their lateral strain relaxation leading to a very low threading dislocation density

(Fathololoumi et al., 2011). So far, limited work has been published on GaN-based MQW nanowires used as resonant tunneling diodes.

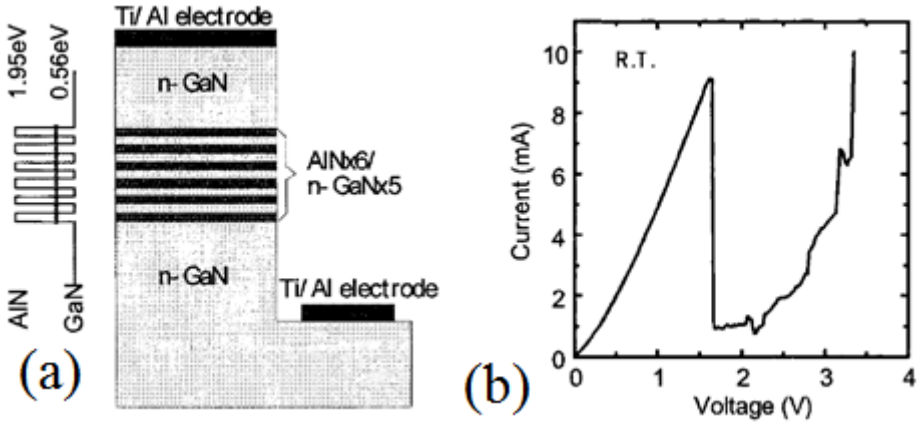


Fig. 1.2 – (a) First GaN-based planar multiple quantum well heterostructure with (b) negative differential resistance at room temperature (Kikuchi et al., 2001).

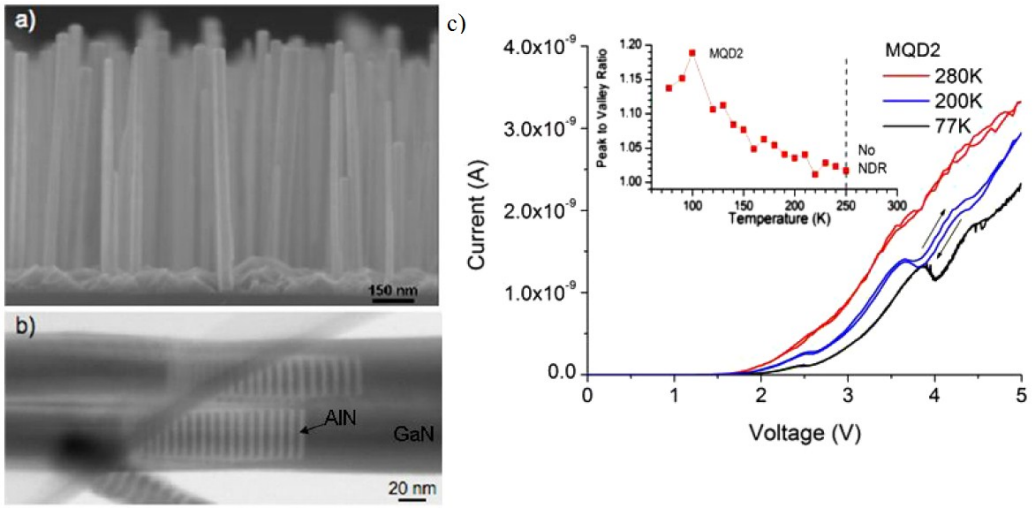


Fig. 1.3 (a) First GaN-based 1-D nanowire multiple quantum well heterostructure made with (b) AlN barriers. (c) Negative differential resistance was achieved up to 250 K (Rigutti et al., 2010).

For this work, we have grown, by radio-frequency plasma-assisted molecular beam epitaxy, three different samples of high quality GaN/AlN 1-D nanowire heterostructures with varying silicon doping concentrations. The samples were used to fabricate single nanowire and large area nanowire devices. The electrical properties were then measured systematically at cryogenic and room temperatures where negative differential resistance is reported. Chapter 2 describes the properties of the GaN and AlN semiconductors used in this work as well as benefits of the nanowire heterostructure over planar ones. Chapter 3 introduces the resonant tunneling diode, its associated negative differential resistance property, as well as the intersubband transition optical phenomenon. Chapter 4 provides details on the different applications of the multiple quantum well heterostructures. Chapter 5 explains the growth of the nanowires and the fabrication of the devices. Chapter 6 presents the experimental setup and the electrical measurement method. Finally, chapter 7 displays the electrical measurement results and the discussion.

Chapter 2 - Gallium Nitride Nanowires

2.1 Semiconductors

A semiconductor is a material with an electrical conductivity in between that of a conductor (e.g. metal, salts) and an insulator (e.g. glass, ceramic, wood). Examples of semiconductors include silicon (Si), germanium (Ge), gallium arsenide (GaAs), gallium nitride (GaN), aluminum nitride (AlN), zinc oxide (ZnO), indium nitride (InN), and copper indium diselinide ($CuInSe_2$). Semiconductors were first observed and classified in the mid-19^{th} century when Michael Faraday made the discovery that some materials exhibited a decrease in resistivity as temperature increases, contrary to typical metals (Faraday, 1838). Presently, silicon is by far the most popular and most widely used semiconductor in the world due to its cheap manufacturing cost and is present in billion dollar industries such as integrated circuits as well as photovoltaic cells (Jaeger, 2001). Semiconductors are of such interest because of their variability and modularity in conductance. Dopants such as impurities can be introduced into semiconductors in the form of acceptors or donors, making them p-type or n-type respectively. Dopants determine the form of the charge carriers within the material: electrons for n-type and holes for p-type. Moreover, applied electric fields can modulate the functionality of a semiconductor by creating or removing a conducting channel, effectively capable of turning ‘on’ or ‘off’ a field effect transistor. Refer to table 2.1 for a list of common and important semiconductors**.**

Table 2.1 – List of commonly used semiconductors and their properties. Values are taken from Ioffe Institute (Siklitsky, 2001) except where indicated.

Semiconductor	Band gap (eV)	Type of band gap	Mobility of electrons ($cm^2 \cdot V^{-1} \cdot s^{-1}$)
Si	1.11	Indirect	≤ 1400
Ge	0.67	Indirect	≤ 3900
GaAs	1.43	Direct	≤ 8500
GaN	3.44	Direct	≤ 2000 (Eastman and Mishra, 2002)
AlN	6.28	Direct	≤ 300
InP	1.34	Direct	≤ 5400
GaP	2.26	Direct	≤ 250
SiC	2.36	Direct	≤ 700 (Eastman and Mishra, 2002)

2.2 Band Gap

Certain key properties are used to help define different semiconductors from each other. For one, the band gap of a semiconductor is the range of energies between the electron abundant valence band and the electron deficient conduction band where electron states typically cannot exist. The larger the band gap, the more energy it takes to move an electron from the valence band into the conduction band. In general, large band gaps indicate insulating properties whereas small ones tend towards conducting properties. Furthermore, band gaps are classified as either direct or indirect. In the case of direct band gaps, the momentum of free carriers in both the conduction and valence band are matched, allowing for the emission of a photon with energy equal to that of the band gap

itself. For indirect band gaps, the conduction band minimum and valence band maximum do not occur at the same momentum (k position). Therefore, a phonon assisted transition is required for an electron to recombine with holes in the valence band, lowering considerably the probability of a photon emission.

2.3 Mobility

Mobility, μ, is yet another property crucial for semiconductors. Mobility, typically specified in $cm^2/V \cdot s$, quantifies the speed of the free carriers under the influence of an electric field E. In other words, the drift velocity of an electron is proportional to the mobility and the electric field, and can be expressed as:

$$v_d = \mu E \qquad \text{(Eq. 2.1)}$$

The higher the mobility, the faster an electron can travel from one end to the other, effectively dictating the operating speed of the device. Mobility is highly dependent on temperature, pressure, carrier concentration, defects and impurity incorporation (Pierret, 1988).

2.4 Other Semiconductor Properties

Other properties such as the thermal conductivity ($W \cdot m^{-1} \cdot K^{-1}$), the ability to conduct heat, as well as the breakdown electric field voltage (V/m), the largest reverse bias applied before large current starts to flow through an electronic device in the reverse operation mode, are also used to help characterize semiconductors. For example, GaN has been identified to have high thermal

conductivity and high breakdown electric field, making it ideal for power amplifiers (Millan, 2007).

2.5 Gallium Nitride and Aluminum Nitride

During the past thirty years, research groups have studied and developed many multiple quantum well heterostructures used for resonant tunneling diodes as well as intersubband emission and absorption of infrared light. For example, III-V and II-VI materials such as GaAs/AlGaAs, InAs/AlSb, and ZnO/MgZnO have been reported (Helm et al., 1988; Warburton et al, 1995; Ohtani et al, 2009).

More recently, GaN, with a direct band gap of 3.4 eV, and its nitride alloys have attracted a lot of attention due to its advantages over the other semiconductors. Firstly, its 1.7 eV conduction band offset with AlN, a semiconductor with a direct band gap of 6.2 eV, allows for deep confinement of states within the quantum wells (Rigutti et al., 2010). Therefore, thermal energy will play a less significant role in the carrier transportation, leading to potential room temperature optical operation. Secondly, short relaxation times of less than 150 fs promote the development of high frequency oscillators and ultrafast optical switches (Iizuka et al., 2000; Hamazaki et al., 2004). Thirdly, GaN has a large longitudinal optical (LO) phonon energy of 92 meV, permitting photon emission in the wavelength regions that were not accessible previously (e.g. between 30 and 70 μm and below 2.5 μm) (Kishino et al, 2002). The GaN/AlN system can thus be designed for the fiber-optics transmission wavelength range of 1.3 to 1.55 μm (Kandaswamy, 2008).

GaN is also very interesting due to its high breakdown field (3 MV/cm), high electron mobility (1000-2000 $cm^2 \cdot V^{-1} \cdot s^{-1}$), as well as high heat capacity and thermal conductivity (>1.5 $W \cdot cm^{-1} \cdot K^{-1}$), making it the ideal semiconductor for power transistors such as high electron mobility transistors (HEMTs) (Eastman and Mishra, 2002). With its numerous interesting properties, GaN has found its way in the light emitting diode (LED) industry and is also being used in violet laser diodes for Blu-ray Discs (Nakamura et al., 1991; Trivellin et al., 2009). Furthermore, it was shown that GaN is non-toxic and stable in aqueous solutions, opening up possibilities for in vitro and in vivo medical applications (Jewett, 2012).

GaN, as well as AlN, has a hexagonal wurtzite structure, as depicted in figure 2.1. This non-centrosymmetric structure, one that lacks inversion symmetry, can lead to the phenomenon called piezoelectricity. Piezoelectric materials, such as GaN, AlN, ZnO and $LiNbO_3$, exhibits induced electric fields under mechanical stress. The converse is also true in piezoelectric materials: electric fields induce mechanical stress. Taking a GaN/AlN MQW heterostructure as an example, one can make the layers thin enough to avoid dislocations at the interfaces, even though there is a ~2.5% lattice mismatch between the two semiconductors. However, to avoid dislocations, internal strains in the crystals will induce an electric field and lead to band bending, potentially an undesirable effect.

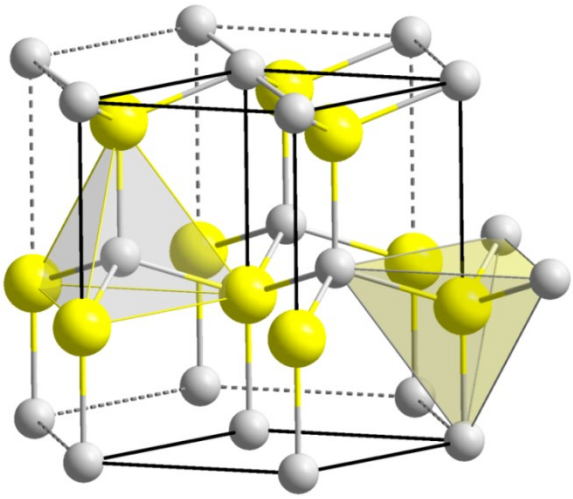


Fig. 2.1 – Hexagonal wurtzite structure (Wikipedia, 2012)

The growth of high quality GaN/AlN heterostructures is not only limited by the existing lattice mismatch, but also by the lack of suitable large area substrates. Typically, GaN is grown epitaxially on silicon carbide or sapphire substrates to alleviate the lattice mismatch between active region and substrate. However, these substrates prove to be quite expensive. High quality GaN/AlN 1-D nanowire heterostructures with very low threading dislocation density can be grown by molecular beam epitaxy to circumvent the lattice mismatch issue (Wang et al., 2012; Nguyen et al., 2011; Fathololoumi et al., 2011; Rigutti et al., 2010).

2.6. Nanowire Heterostructure

The nanowire structure with a high aspect ratio can be employed in the growth of the GaN/AlN multiple quantum well heterostructures and is favored over the standard planar structure for the critical reason of strain relaxation. In planar heterostructures, large mismatches between lattice constants can lead to

many dislocations and defects in the devices, shown in figure 2.2, compromising its performance. Nanowire structures can utilize their free top and lateral surface for elastic strain relaxation. It was shown that the critical thickness (height of the nanowire) at which dislocations occurs depends on the radius of the nanowire (Glas 2006). Moreover, the critical dislocation thickness tends toward infinity for a small enough critical radius r_0^c, depicted in figure 2.3. Assuming linear isotropic elasticity, the critical radius is given by the solution of the following equation:

$$\frac{2\pi}{A_v}\left(\frac{\alpha^2 b_{eff}^2}{4} - \alpha b_{eff}\epsilon_0 r_0^c\right) + C\left(1 + \ln\frac{\beta r_0^c}{b}\right) = 0$$

where b is the magnitude of the Burgers vector (BV), b_{eff} is the edge component of the BV, $\alpha = \frac{4}{\pi}$, $\beta = \frac{2}{\pi}$, $C = \frac{(1-\nu\cos^2\theta)b^2}{2\pi(1+\nu)}$, ϵ_0 is the misfit, ν is the Poisson's ratio for both active region and substrate which is taken to be 1/3, $A_v = 27.3 \pm 0.55$ for the given ν, and θ is the angle between the dislocation line and its BV.

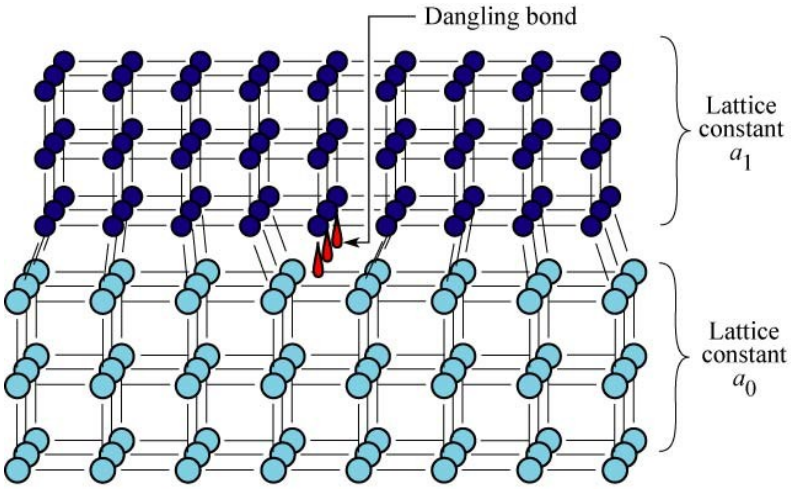


Fig. 2.2 - Lattice mismatch between two different materials with different lattice constants, resulting in dislocations at the interface (Schubert, 2006).

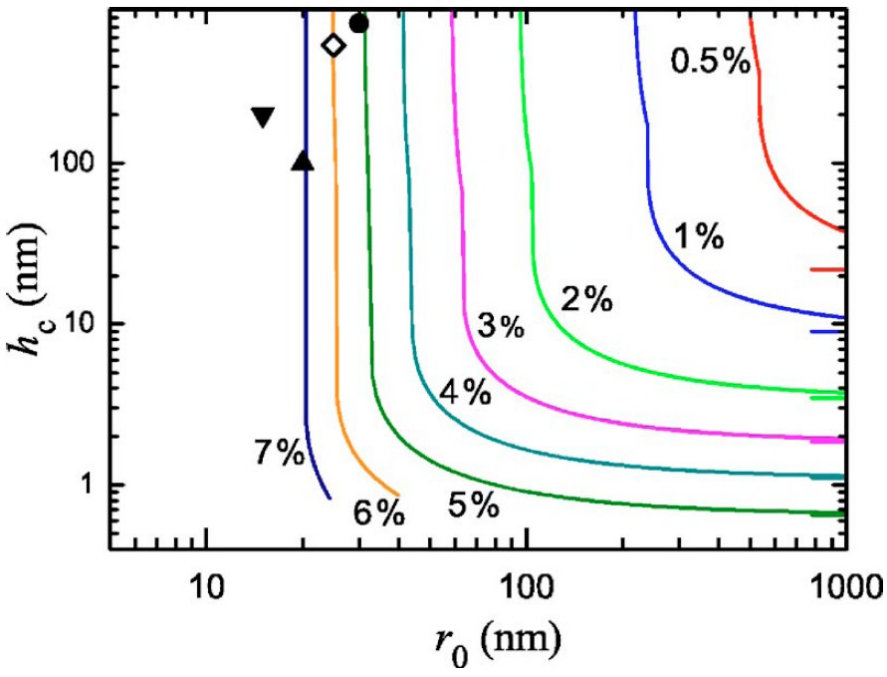


Fig. 2.3 – Relationship between critical dislocation thickness of a nanowire and its radius for different values of misfit (Glas 2006).

Nanowire structures can be grown from either a top-down approach, using fine lithography processes, or from a down-up approach, using epitaxial growth methods. In this work, the method used to grow GaN/AlN nanowires is the molecular beam epitaxy, discussed in chapter 5.

Chapter 3 - Multiple Quantum Well Properties

3.1 Resonant Tunneling

The concept of a resonant tunneling began in the 1970s (Tsu and Esaki, 1973), shortly after the wide spread use of molecular beam epitaxy in semiconductor growth, discussed in chapter 5. Consider the conduction band profile of a double barrier quantum well heterostructure as depicted in figure 3.1 (a). A quantum well is formed by bringing the two barriers within a few de Broglie wavelengths from each other, allowing for the creation of discrete energy states within the well. Resonant tunneling involves the transmission of an electron across the device, passing through the thin barriers, and occurs when the discrete state in the quantum well aligns itself with the Fermi level on the emitter side, bringing the transmission probability close to unity. Resonant tunneling can be further understood by studying the conduction band profiles of a double barrier heterostructure under the influence of different electric fields, as seen in figure 3.1. Initially, under zero bias, the quantized energy state E_0 within the quantum well resides above the Fermi level, resulting in minimum transmission of electrons. As the bias starts to increase to a certain threshold voltage, E_0 falls and aligns itself with the Fermi level. At this point, electrons from the emitter side start to resonate with the finite energy state and transmission of electrons starts to take place, tunneling through the potential barriers. Increasing further the bias brings E_0 between the Fermi level and the bottom of the emitter conduction band, where the current through the device reaches its maximum. Finally, as more and

more bias is applied, E_0 falls below the conduction band and electrons no longer tunnel through the device, going off resonance.

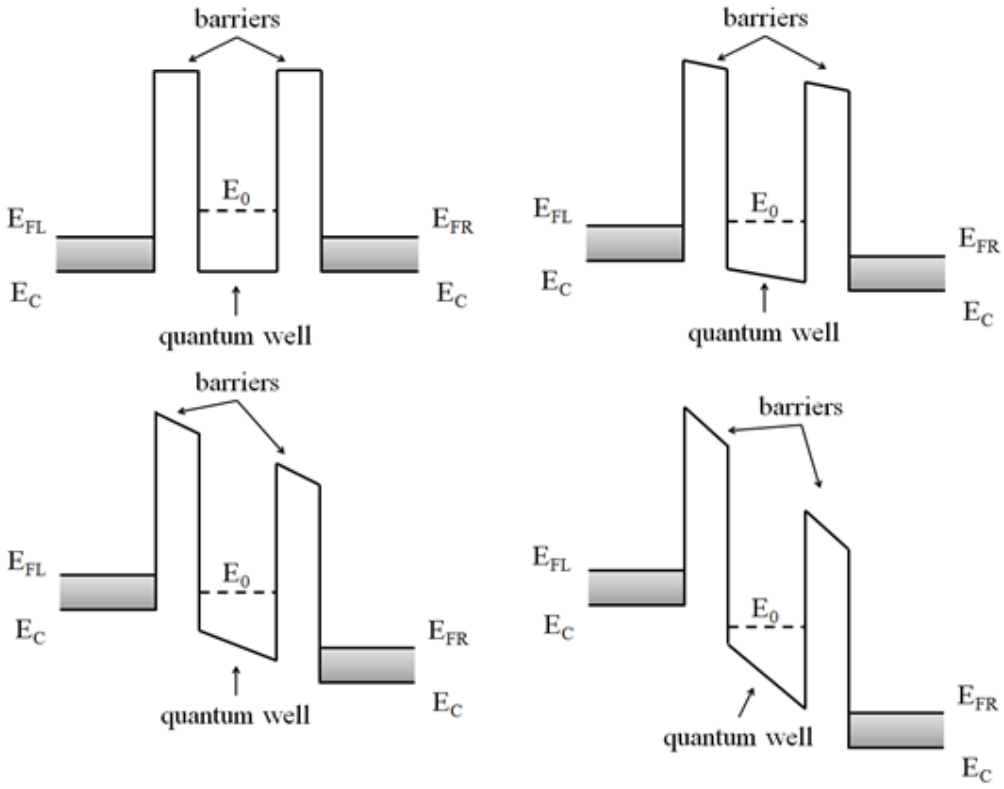


Fig. 3.1 – Conduction band profiles of a double barrier heterostructure with a quantum well under different bias conditions: a) zero bias, b) threshold-resonance, c) resonance, d) off resonance.

In an ideal resonant tunneling structure, energy and momentum are conserved and the total energy of electrons can be expressed as the sum of the parallel and perpendicular energies (Mizuta and Tanoue, 1995):

$$E(\boldsymbol{k}) = \frac{\hbar^2(k_x^2+k_y^2)}{2m^*} + E_z \qquad \text{(Eq. 3.1)}$$

where m^* is the effective electron mass, (k_x, k_y) are the lateral wavenumbers and E_z is the applied electric field in the perpendicular direction of the barriers. The electronic states involved in the resonant tunneling correspond to the interaction of the plane $k_z = q_R$ with the Fermi sphere, shown in figure 3.2. The variable q_r represents the wavenumber of the energy of the resonant state relative to the conduction-band edge E_C and is given by

$$q_r = \frac{\sqrt{2m^*(E_0 - E_C)}}{\hbar} \qquad \text{(Eq. 3.2)}$$

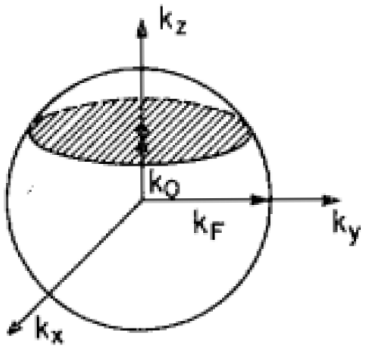


Fig. 3.2 – The Fermi sphere of electrons in the emitter side of the resonant tunneling structure (Capasso et al, 1986).

The tunneling current density can be shown to be proportional to the density of the states indicated by the grey intersecting circle, and hence proportional to the energy level difference between the Fermi level on the emitter side and the energy of the finite resonant state. The tunneling current density is represented by the following expression, as long as E_0 does not fall below the Fermi level.

$$J \propto \pi\left(k_f^2 - q_R^2\right) \propto (E_{FL} - E_0) \qquad \text{(Eq. 3.3)}$$

From the 1D, time-independent, effective mass Schrodinger equation

$$H\Psi(z) = E_z\Psi(z) \quad \text{(Eq. 3.4)}$$

expressions can be found for the transmission probabilities $T(E_z)$ through the resonant tunneling structure by solving for the wavefunction via boundary conditions and by deducing the relationship between the incoming and the transmitted wavefunction amplitudes. The transmission probability of a single barrier structure, for $E_z < V$, can be written as

$$T_{sb}(E_z) = \left(1 + \frac{V^2}{4E_z(V-E_z)} sinh^2(\kappa_z d)\right)^{-1} \quad \text{(Eq. 3.5)}$$

where $\kappa_z = \sqrt{\frac{2m^*(V-E_z)}{\hbar^2}}$, V is the potential barrier height and d is the barrier thickness. In the case of a double barrier and multiple barrier heterostructures, the transmission probability can be approximated by the use of the transfer matrix method, a method used in the analysis of propagating electromagnetic waves through different layered mediums.

Resonant tunneling is characterized by the electron dwell time, τ_d. The dwell time is the time an electron resides between two potential barriers in a quantum well. Alternatively, it can be thought as the time needed to travel across two potential barriers. The expression for the dwell time is approximated to be

$$\tau_d \approx \frac{1}{2T_{sb}(E_z^0)} D + \frac{2/k_z^0}{v_z^0} \quad \text{(Eq. 3.6)}$$

where D is the thickness of the quantum well, v_z^0 is the velocity of the electron in the quantum well, and $2k_z^0$ is a quantum mechanical well width correction due to penetration of the electron into the potential barriers, as shown in figure 3.3. The

dwell time is minimized for high-speed applications and generally has a value between a few tens of femtoseconds to a few hundred nanoseconds.

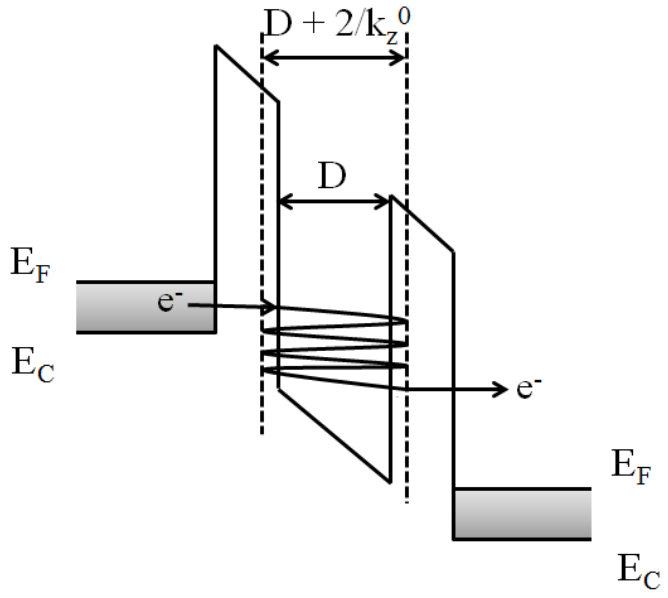


Fig. 3.3 – Conduction band diagram of a double barrier heterostructure highlighting the multiple reflections of an electron inside the quantum well.

Resonant tunneling can also be characterized by either a global coherent or incoherent (sequential) transport mechanism. In the former case, there is little scattering of the electron within the quantum well which leads to a large anticrossing between the coupled states and results in a Fabry-Perot like carrier transport (Capasso et al., 1986). In other words, the electron waves inside the quantum wells in both the forward and backward direction cancel out the reflected waves and enhance the transmitted ones. However, in the latter case, significant electron scattering within the well leads to energy and momentum relaxations, which breaks the phase-coherence and makes each quantum tunneling

independent of each other (Aleshkin et al., 2006). The schematic for sequential tunneling is shown in figure 3.4. The presence of negative differential resistance in the I-V characteristics does not imply either the coherent or sequential tunneling method. In fact, additional tests involving the variation of the well widths are needed to distinguish between the two (Capasso et al., 1986). Coherent tunneling occurs when the intrinsic resonance width ($\sim\hbar/\tau_d$) is greater than or equal to the collision broadening ($\sim\hbar/\tau$), where τ is the scattering time or, in other words, the inverse of the elastic and inelastic scattering rate.

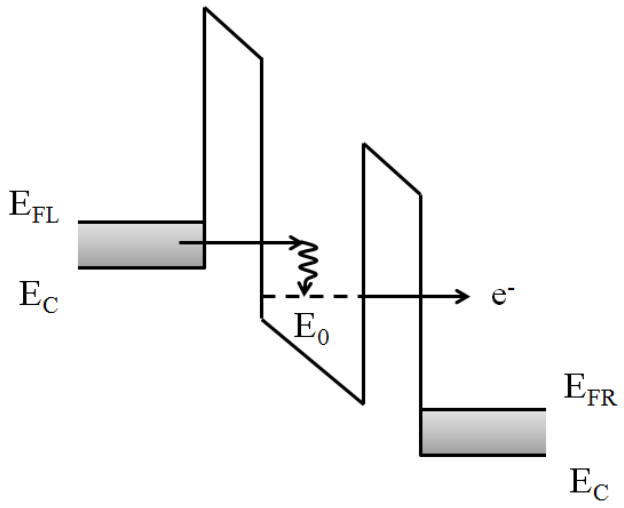


Fig. 3.4 – Conduction band diagram of sequential tunneling in a double barrier heterostructure.

3.2. Intersubband Transitions

In 1971, Kazarinov and Suris proposed the amplification of electromagnetic waves via resonant tunneling and intersubband transitions in superlattice structures (Kazarinov and Suris, 1971). Intersubband transitions involve the movement of an electron from one discrete energy state to another

within the same conduction band, shown in figure 3.5. This is different from the typical interband scheme, shown in figure 3.6, where electrons travel from the conduction band to the valence band or vice versa, emitting or absorbing respectively a photon of energy given by equation 3.7 and 3.8.

$$\lambda(nm) = \frac{1240}{E_g} \quad \text{(Eq. 3.7)}$$

$$E_g = band\ gap\ (eV) \quad \text{(Eq. 3.8)}$$

Intersubband transitions allow for the emission and absorption of far-infrared photons, a phenomenon not possible in the interband scheme because of the relatively large band gap energy. The first experimental observation of intersubband emission in the terahertz range was performed using GaAs/AlGaAs superlattices (Helm et al., 1988). To create the different discrete energy states within the conduction band, quantum wells and potential barriers are used, as in the case of the double barrier heterostructure. With proper care, the quantum wells can be fine-tuned to exhibit energy separation in the meV between its different discrete energy states. Table 3.1 shows the different infrared ranges and their respective wavelength and photon energy range.

Table 3.1 – Infrared characterization.

Name	Wavelength (μm)	Photon Energy
Near-infrared (IR)	0.75-1.4	0.9-1.7 eV
Short-wavelength IR	1.4-3	0.4-0.9 eV
Mid-wavelength IR	3-8	150-400 meV
Long-wavelength IR	8-15	80-150 meV
Far IR	15-1000	1.2-80 meV

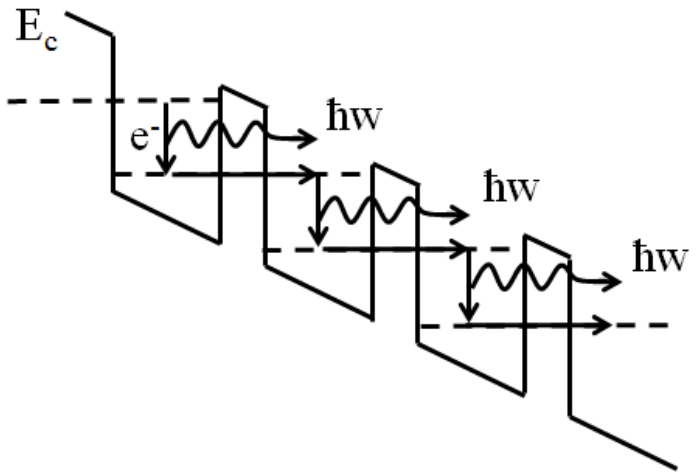


Fig. 3.5 – Conduction band profile of a superlattice heterostructure, showcasing intersubband transitions and the emission of low energy infrared photons.

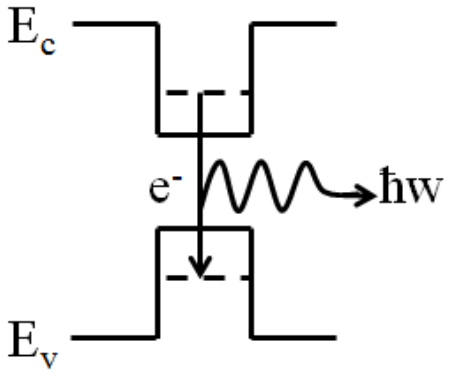


Fig. 3.6 – Band profile of an interband scheme where an electron travels from the conduction band to the valence band.

Chapter 4 – Applications

4.1 Quantum Cascade Laser

The terahertz frequency range is broadly defined between 300 GHz and 10 THz and is one of the least developed in terms of radiation sources and detectors due to the lack of semiconductor materials with a small enough band gap (Williams, 2007). Fortunately, the use of intersubband transitions can circumvent this problem. The quantum cascade laser (QCL) is one of the semiconductor devices that apply intersubband transitions for various near-to-far infrared imaging applications. A QCL uses periodic barrier and quantum well structures for its active region, typically arranged in a chirped superlattice, as shown in figure 4.1 (a). Other important QCL structures are also shown in figure 4.1 (b) and (c), such as the bound-to-continuum and resonant-phonon. In the case of the chirped superlattice, the energy band can bend appropriately under an applied electric field and under the right conditions, the energy states within the quantum wells of a module can couple tightly together to form minibands, depicted by the shaded grey regions in figure 4.1. Electrons at the bottom of the second miniband can then relax into the top of the first miniband, effectively releasing a low energy photon.

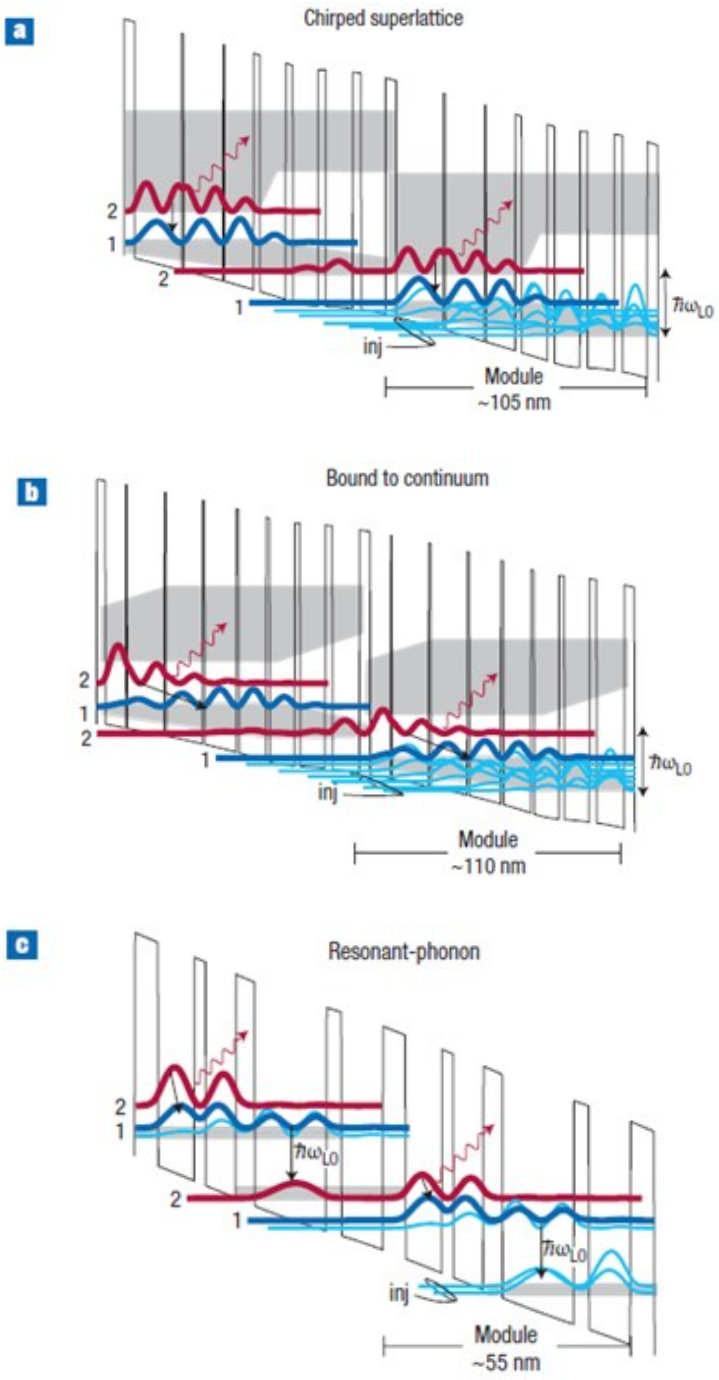


Fig.4.1 Conduction band diagrams of quantum cascade laser's active region. The quantum cascade laser can have different active region structures called (a) chirped superlattice, (b) bound-to-continuum, and (c) resonant-phonon (William, 2007).

Faist and Capasso were the first to fabricate a QCL using InGaAs/InAlAs (1994). In 1998, GaAs/AlGaAs was also explored (Sirtori et al., 1998). However, the prevailing issue with QCLs is the fact that it is extremely difficult to achieve lasing at room temperature. Most QCLs operate at cryogenic temperatures, making it problematic to introduce QCLs into the market. In some cases, however, it is beneficial to be operating at low temperatures like in space applications. Ideally though, QCLs would be able to operate in a full range of environmental conditions. Recently, GaN/AlGaN materials have been implemented in QCLs, achieving room temperature operation (Vardi et al., 2008).

QCLs are of interest because of their non-invasive evaluation and their non-destructive nature. Due to these two properties, QCLs are found in numerous terahertz imaging applications. For example, QCL are used in quality control in the pharmaceutical, biomedical, and aerospace industries, remote sensing of environmental gases, cancer diagnostics, as well as security screening (Hosako and Oda, 2011). Moreover, QCLs can help see through smoke, aiding emergency firefighters in dire situations.

4.2 Oscillator

Multiple quantum well structures are used as oscillators to achieve frequency oscillations in the giga- and tera-hertz range. Currently, resonant tunneling diodes are the semiconductor device that can achieve the highest frequency oscillation at just above 1 THz (Suzuki, 2010). Oscillators are important for their use in converting direct current to alternating current and in generating clock signals.

Taking a simple LC circuit as an example, the circuit acts as a resonant oscillator with the charges flowing back and forth between the inductor and the capacitor. However, in the presence of a resistance R in series with the inductor and capacitor, a damping effect occurs and the total current flowing through the circuit decreases. From Kirchhoff's voltage law, we can write the following equation for the RLC circuit shown in figure 4.2:

$$0 = \frac{di(t)}{dt}L + i(t)R + \int \frac{i(t)}{C}dt \qquad \text{(Eq. 4.1)}$$

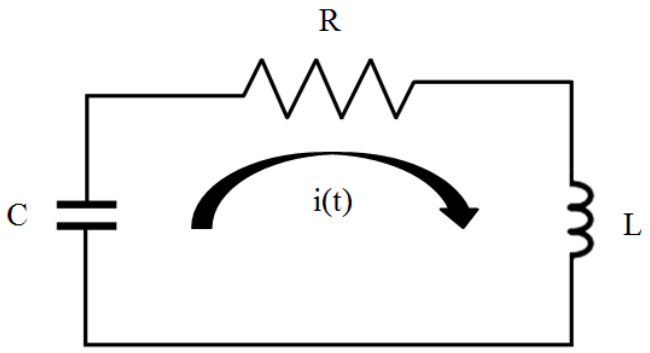


Fig. 4.2 – RLC circuit.

It can be shown that the general solution of the above equation is of an exponential form $i(t) = e^{At}$ with $A = \frac{-R \pm \sqrt{R^2 - 4L/C}}{2L}$. In the case where $R^2 < 4L/C$, we can write the general solution as $i(t) = e^{at}e^{jwt}$ with $a = -\frac{R}{2L}$ and $w = \left|\frac{\sqrt{R^2 - 4L/C}}{2L}\right|$. Thus, the current flowing through the RLC circuit becomes of sinusoidal form with an exponential decrease in the presence of positive resistance R. By examining the general solution, one can see that with negative resistance, the current increases exponentially, and with positive resistance, the current

decrease exponentially. By bringing the value of $a = 0$, one can achieve a sinusoidal current without exponential decay.

In figure 4.3, an alternate RLC circuit is shown with the addition of a negative differential resistance device. A direct current (DC) voltage V_{bias} is applied to the device via a large inductor L_{bias}. The dynamic resistance of the circuit is the sum of that of the resistor R and the NDR device and is plotted, against the applied bias voltage, in the y-axis of figure 4.4. If V_{bias} is set such that the NDR device is biased into the negative differential region of its I-V characteristics, then the amplitude of the oscillation frequency will increase because the total dynamic resistance of the circuit is less than zero. As the voltage swing increases, the voltage across the NDR device will eventually bring it out of the negative differential region. In this case, the total dynamic resistance of the circuit increases above zero and the voltage swings will decrease in amplitude.

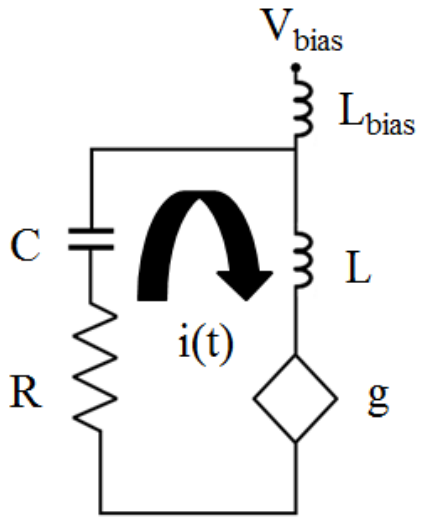


Fig. 4.3 – RLC circuit with a negative differential resistance device in series.

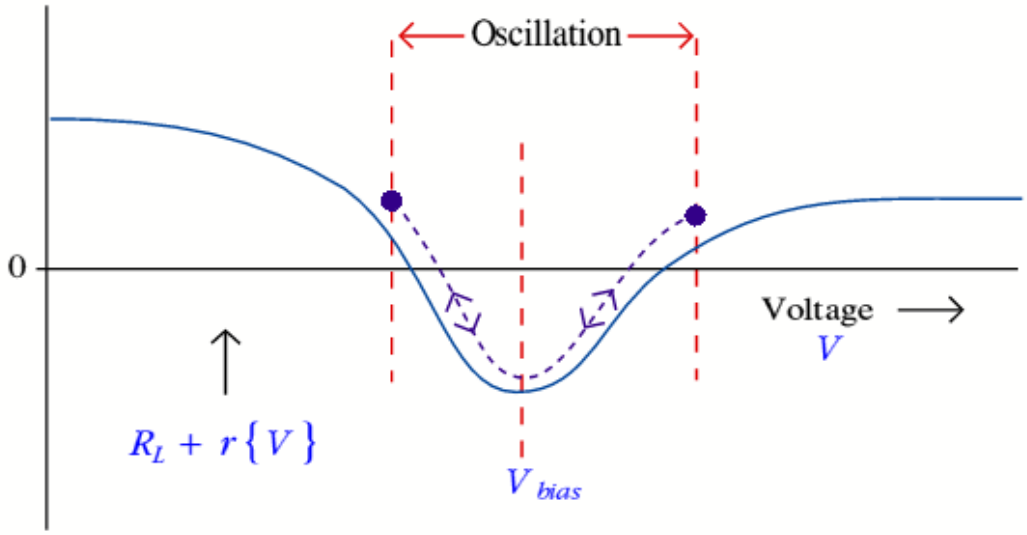


Fig. 4.4 – Dynamic resistance of the RLC circuit shown in figure 4.3 versus the applied DC voltage across the NDR device (Lesurf).

4.3 Memory Circuits

Multiple quantum well heterostructures used as a resonant tunneling diode can be placed in series with a transistor, acting as the current load, to make a multi-valued memory circuit shown in figure 4.5 (Seabaugh, 1992). Negative differential resistance in the diode's I-V characteristics, as seen in figure 4.6 (a) (Seabaugh 1993), plays an important role in the circuit's memory capabilities by having multiple voltage values outputting the same current. The stored voltage is written through the temporarily open write line which then sets a voltage across the diode. When the write line is closed, the output voltage will then move itself towards the nearest stable operating point corresponding to the predetermined current flow. Many works have been published on the use of resonant tunneling diodes for memory applications. For example, Seabaugh et al. have made an

AlAs/InGaAs/InAs based resonant tunneling diode capable of storing 9 different values, shown in the transfer characteristics in figure 4.6 (b) (Seabaugh, 1993).

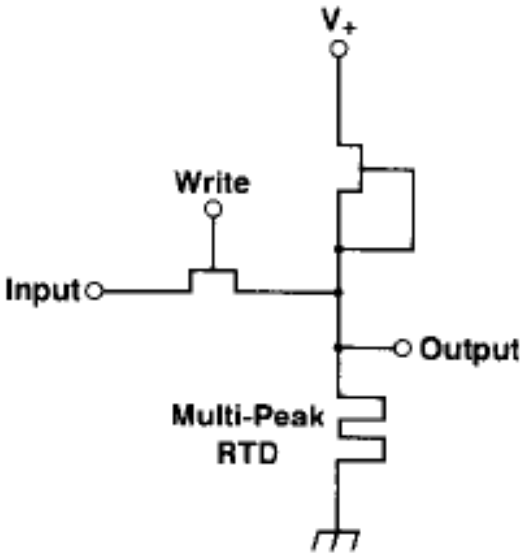


Fig. 4.5 – Resonant tunneling diode memory circuit (Seabaugh, 1993).

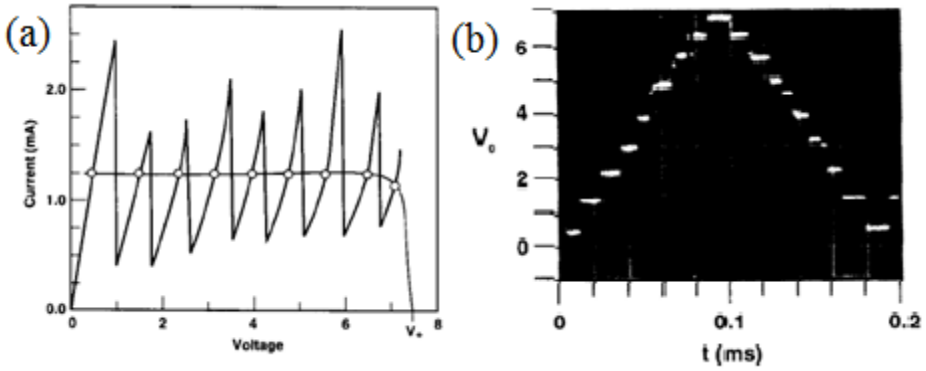


Fig. 4.6 – (a) I-V characteristics of a nine-state resonant tunneling diode and (b) its transfer characteristics (Seabaugh, 1993).

Chapter 5 - Growth of Nanowire and Device Fabrication

5.1 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) is an epitaxial growth technique that allows one to grow very thin and high quality semiconductors, with a thickness precision of one monolayer. The MBE system used for this work is a Veeco model Gen2 unit as shown in figure 5.1. A typical schematic of a MBE system is shown in figure 5.2.

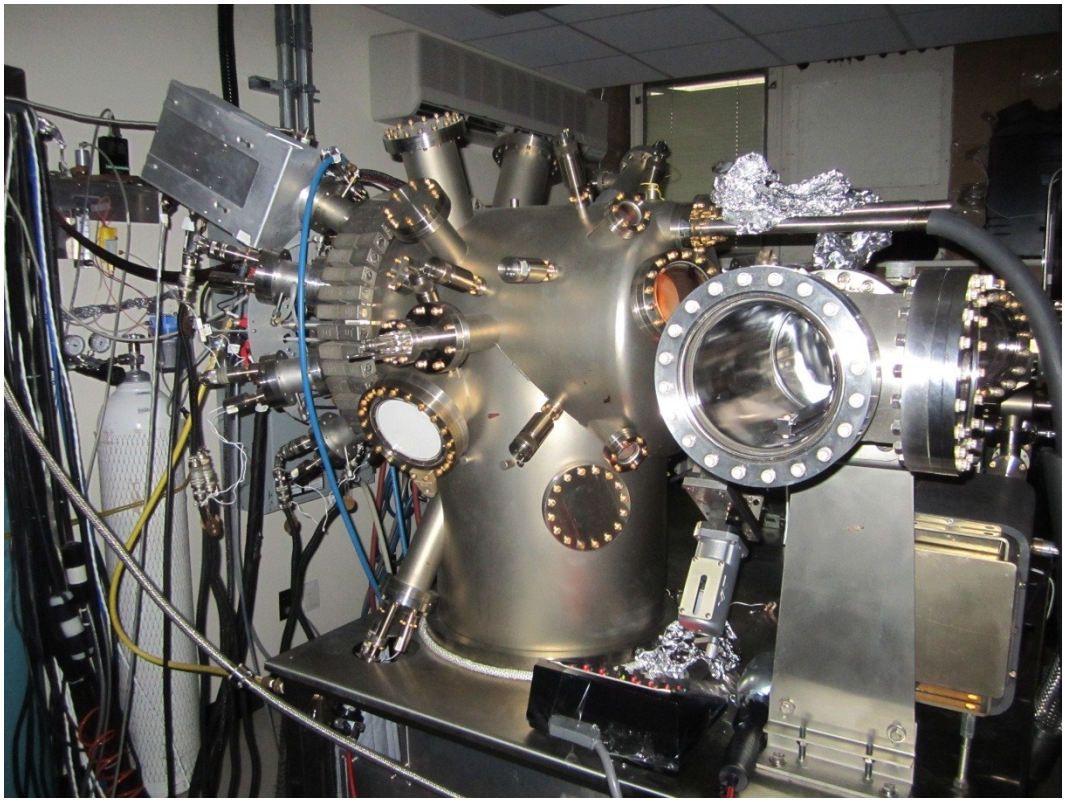


Fig.5.1 – MBE system used to grow GaN/AlN nanowires.

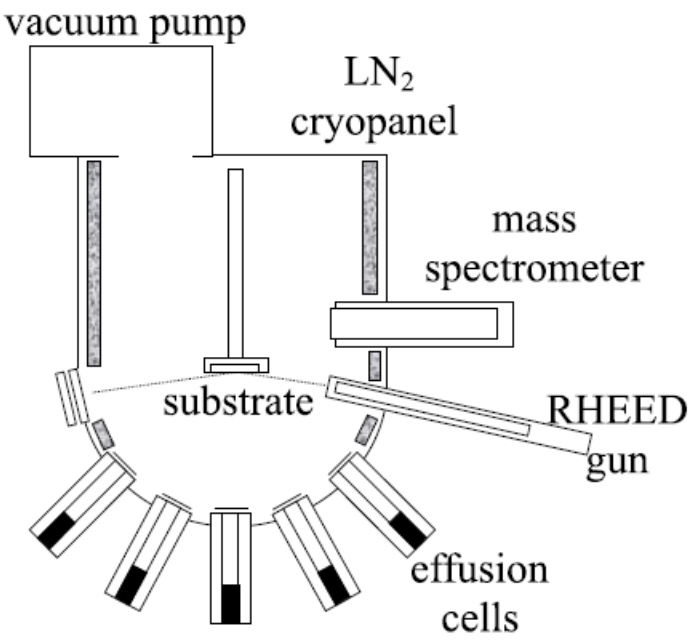


Fig. 5.2 – Setup of a MBE system (Rinaldi, 2002).

An MBE system consists of a high or ultra-high (10^{-5} to 10^{-8} Torr) vacuum chamber that can be cooled via a liquid nitrogen exchange line. Within the chamber, an array of angled effusion chambers is used to introduce the desired elements by evaporation and adsorption onto a slowly rotating and heated substrate. The effusion chambers, one for each desired element, utilize fast shutters to allow for abrupt transitions in layer composition. Moreover, the effusion chambers can be used to introduce dopants into the layers. In line with the substrate, a reflection high energy electron diffraction (RHEED) is placed to monitor the quality and thickness of the layer deposited. The RHEED detects incoming electrons of energy 5-40 keV that are reflected and scattered off of the surface of the substrate, as shown in figure 5.3. Depending on the diffraction pattern seen on the RHEED screen, one can determine if the surface is smooth or

rough, or alternatively, regular or irregular. An example of a RHEED measurement is shown in figure 5.4.

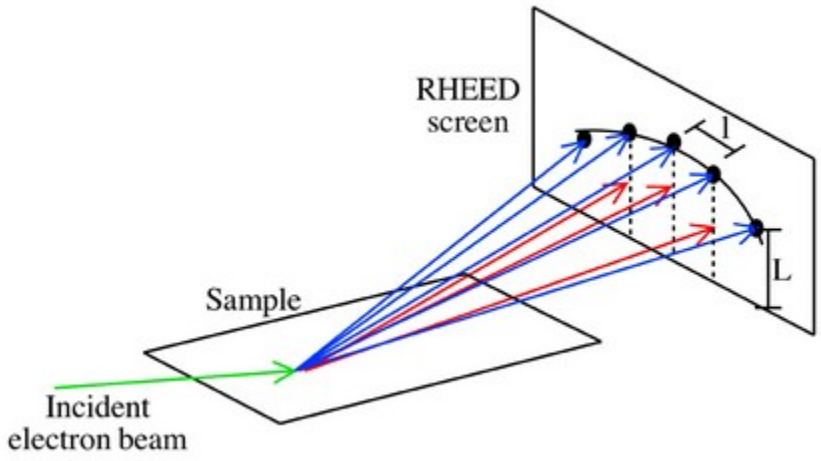


Fig. 5.3 – RHEED measurement for quality monitoring in MBE (Barron, 2009).

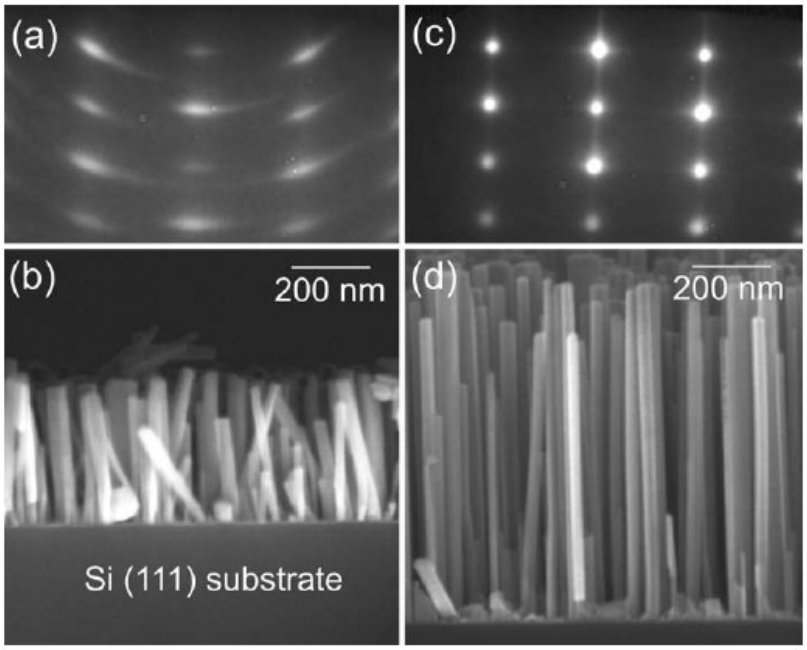


Fig. 5.4 – RHEED patterns and their associated GaN nanowires (SEM micrograph). (Songmuang et al., 2007).

Before loading a substrate into the MBE chamber, it is chemically cleaned to minimize the amount of surface impurities. Furthermore, the substrate is annealed within the MBE chamber to remove any native oxide layers on the surface that might act as an unwanted insulating barrier.

Although MBE systems are grossly expensive (700 thousand to 1 million dollars) and are limited by its low throughput, it is widely used in the compound semiconductor industry for its high layer thickness precision, its high uniformity (1%) and for its abruptness in layer transitions, making the growth of thin and high quality heterostructures possible. Furthermore, MBE does not need toxic gases as does the commonly used metalorganic chemical vapour deposition system.

5.2 Growth Conditions

A radio-frequency plasma-assisted MBE process is used to grow the GaN/AlN heterostructure nanowires used in this work. The nanowires consist of 10 AlN barriers and 10 GaN quantum well regions, and were grown on Si (111) substrates. The growth process was carried out in nitrogen rich conditions, which favours the formation of the nanowire structures as opposed to a planar one. Moreover, a thin gallium seeding layer was first deposited onto the heated substrate (680 °C) which then self-agglomerates and forms gallium droplets on the surface. These gallium droplets help in a self-catalytic process and act as the seed of the nanowire formation. The gallium droplets are used to avoid any unwanted contamination with metal catalysts that are typically employed in other III-V nanowire growth procedures (Calarco et al., 2007). For the effusion cells,

the Ga and Al sources are set to 815 and 1020 °C respectively. The density of the droplets and nanowires can be more or less controlled by varying the substrate temperature, Ga seeding layer thickness, as well as the active region growth temperature. Preliminary results, not presented in this work, have shown sparser density of the nanowires at a higher substrate growth temperature (710 °C instead of 685 °C). The overall growth process is quite lengthy and consists of many steps.

The orientation of the nanowires is pointed along the [0001] polar direction with the sidewalls being non-polar m-planes. The nanowire structure with its associated conduction band profile is shown in figure 5.5. A high-resolution scanning electron microscopy (SEM) image depicts dense hexagonal nanowires in figure 5.6 (a). The density of the nanowires was estimated to be 1E10 cm^{-2} and is growth temperature dependent. Upon investigation of the SEM micrograph, it became clear there were two types of nanowires: the long and the short. The long nanowires were the ones designed for, with a height and diameter (near the GaN/AlN periodic structure) of approximately 850 nm and 45 nm, though the height varied between 800 and 1000 nm. The short nanowires have a considerably reduced height between 300 and 600 nm, as seen in figure 5.7. The appearance of the short nanowires is due to the high density of the nanowires. Some nanowires overshadow its close neighbors and accumulate more than its share of the gallium nitride. The nanowires were also investigated under a transmission electron micrograph, which revealed structures grown nearly free of dislocations, seen in figures 5.6 (b) and (c).

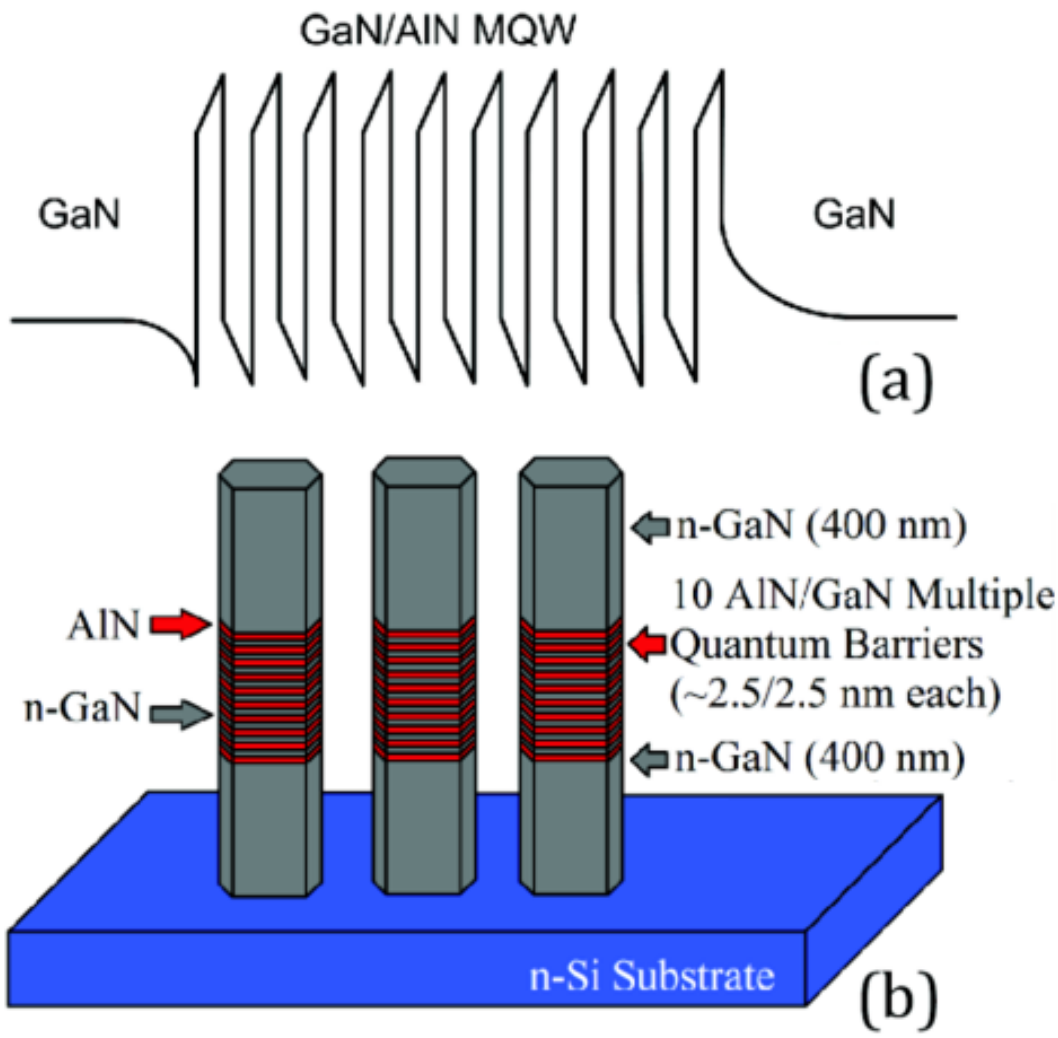


Fig. 5.5 - a) Conduction band profile of the GaN/AlN multiple quantum well nanowire and b) the design of the GaN/AlN nanowires with 10 periods of GaN/AlN structure.

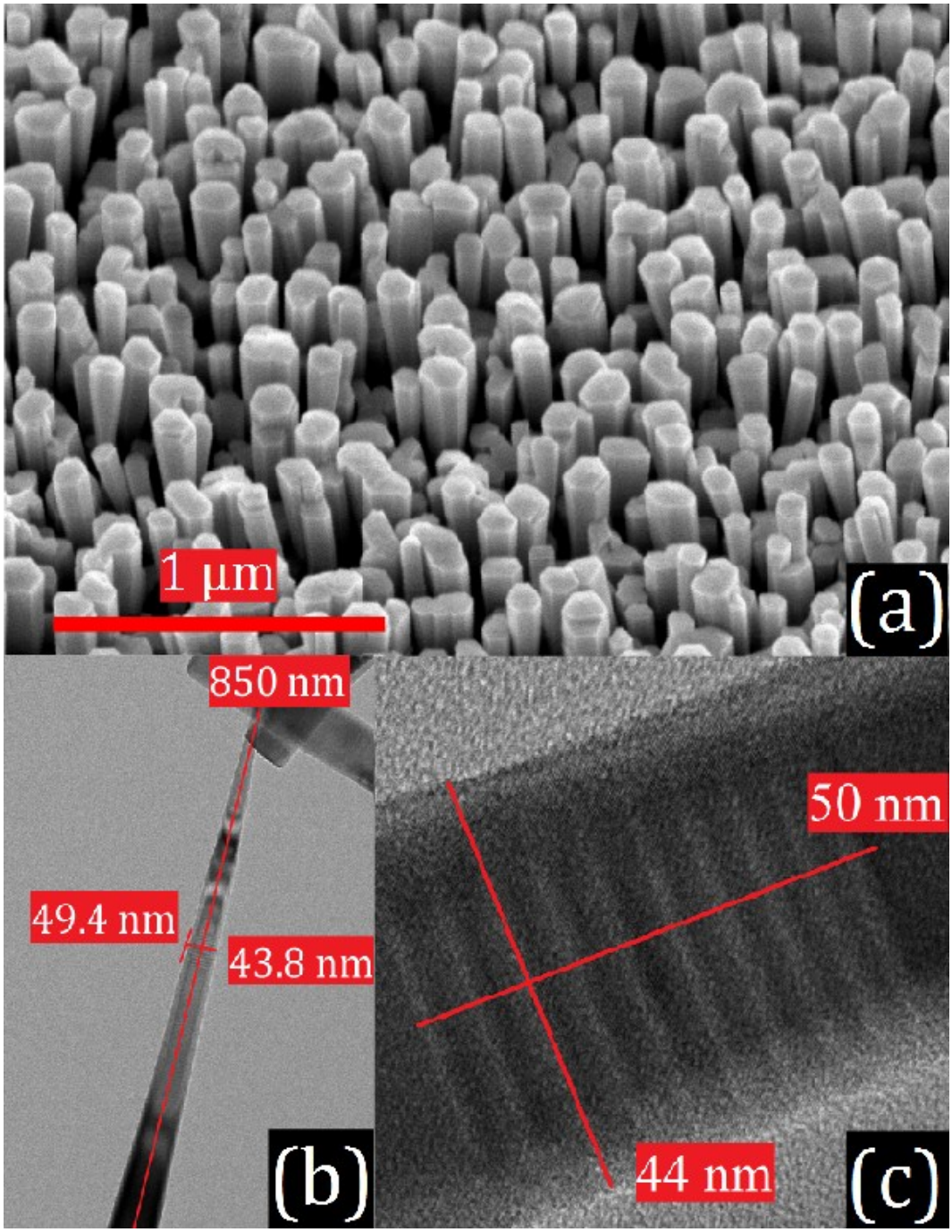


Fig. 5.6 - (a) SEM micrograph of an array of GaN/AlN nanowires (sample B) and (b, c) TEM images of a single GaN/AlN heterostructure nanowire.

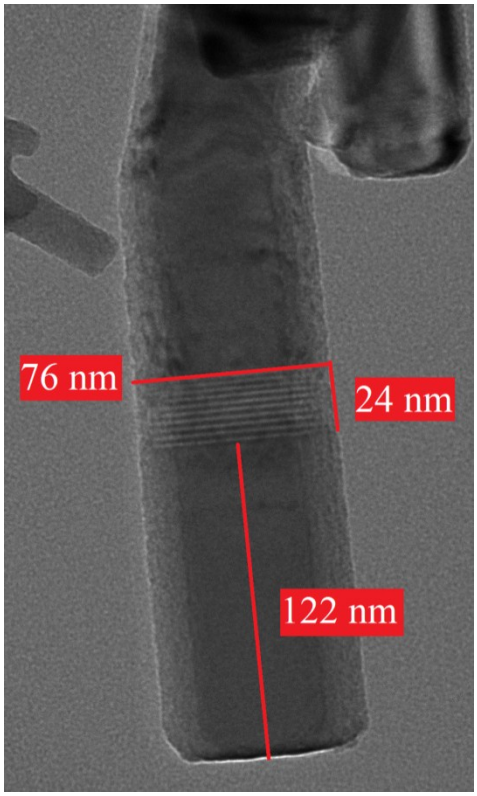


Fig. 5.7 – An undesired short nanowire with a GaN cladding layer length of 122 nm instead of 400 nm and a GaN/AlN periodic structure length of 24 nm instead of 50 nm.

To further investigate the quality of the nanowires, micro-photoluminescence measurements were performed using a HeCd laser ($\lambda \sim 325$ nm), a high-resolution spectrometer and a photomultiplier tube. The measurements resulted in a pronounced peak at 3.42 eV with a narrow FWHM of 0.1 eV, suggesting low defect density, shown in figure 5.8. In addition, yellow luminescence was not detected at 2.2 eV at room temperature. Yellow luminescence in GaN is considered to arise from transitions between the

conduction band (or shallow donors) and deep acceptor levels (Shalish et al, 1999) and can severely degrade the performance of optoelectronic devices by creating a secondary recombination path (Kucheyev et al, 2002).

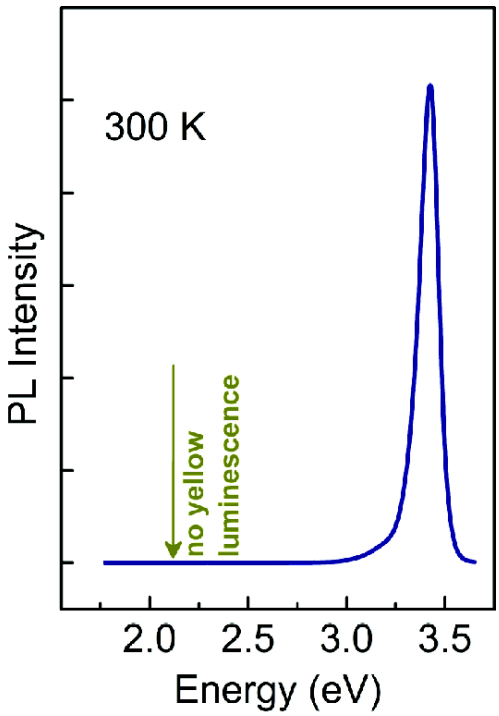


Fig. 5.8 – Micro-photoluminescence measurement of the GaN/AlN multiple quantum well nanowire with a strong peak at 3.42 eV and with no yellow luminescence, suggesting defect free structures.

Although the nanowires were grown nearly without defects, the widening of the diameter as the nanowires grow vertically (tapering) was present. Tapering is partly caused by the introduction of the AlN layers. The slower migration rate of Al atoms versus Ga atoms leads to a slower vertical growth rate of AlN compared to GaN and ultimately wider diameters at the AlN layers. Tapering can

also lead to coalescence of the wires. Coalescence can create unwanted electrical behaviour with current bypassing the periodic tunnelling structure and effectively shorting the device. Tapering of the nanowires can possibly be controlled by a Ga-flux during the growth process (Meijers et al., 2006).

In this work, three different samples, labelled here as samples A, B, and C for convenience, were grown with varying silicon doping concentrations in the GaN quantum wells and cladding layers. SEM micrographs of samples A and B are shown in figures 5.9 to 5.12. The quality of the nanowires was found to be of higher near the middle point between the center and the edge of the wafer when compared to the edge. Table 5.1 details the three different samples, with their silicon doping value as well as their associated in-house label. The silicon doping value was measured by a secondary ion mass spectroscopy method.

Table 5.1 – Sample names and their silicon doping level.

Sample Name	In House Label	Silicon doping level in quantum wells
A	MN637	~ 0 cm^{-3}
B	MN658	2E16 cm^{-3}
C	MN659	1E17 cm^{-3}

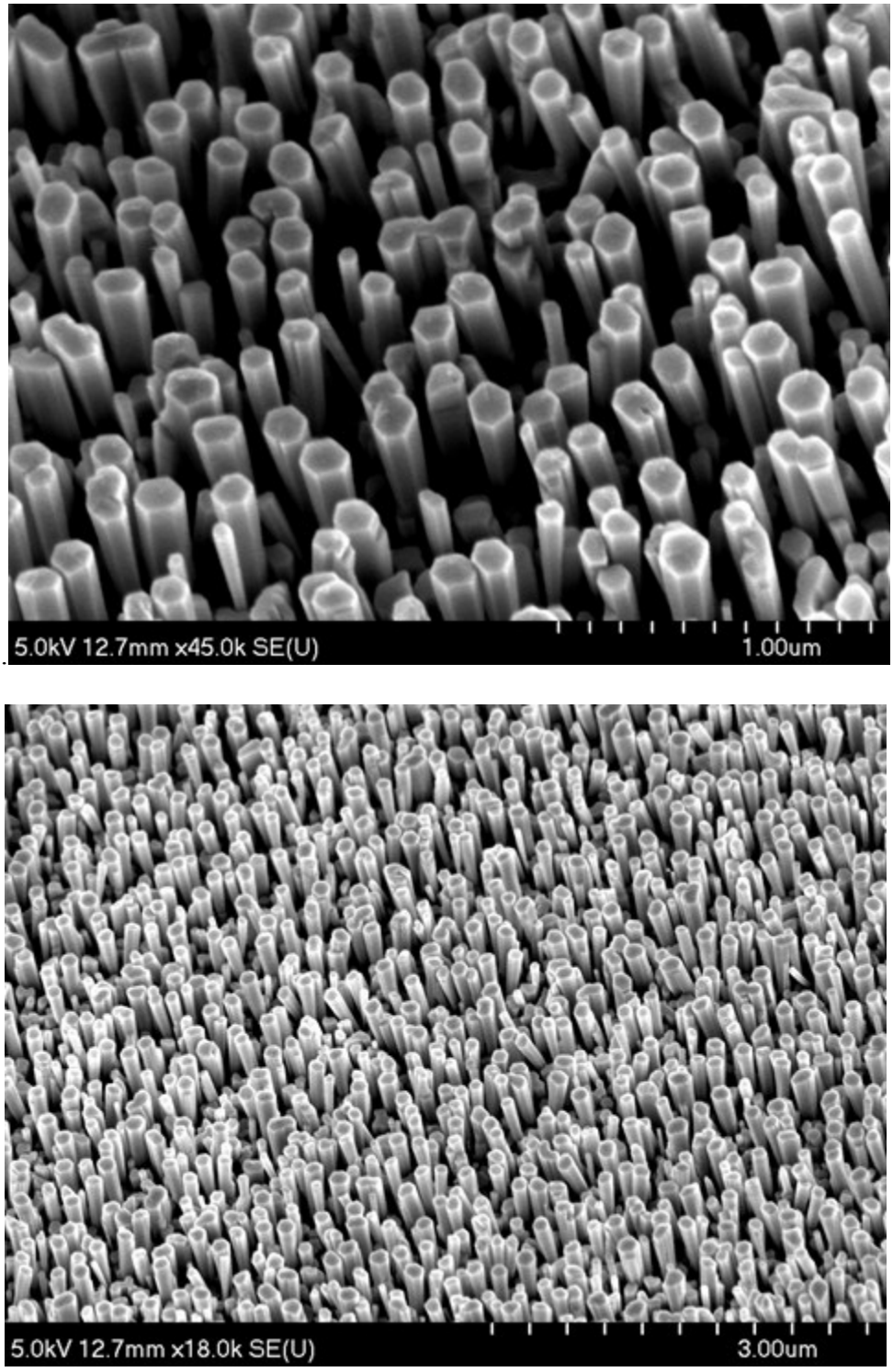


Fig. 5.9 – SEM micrographs of sample A near the middle point between the center of the wafer and the edge.

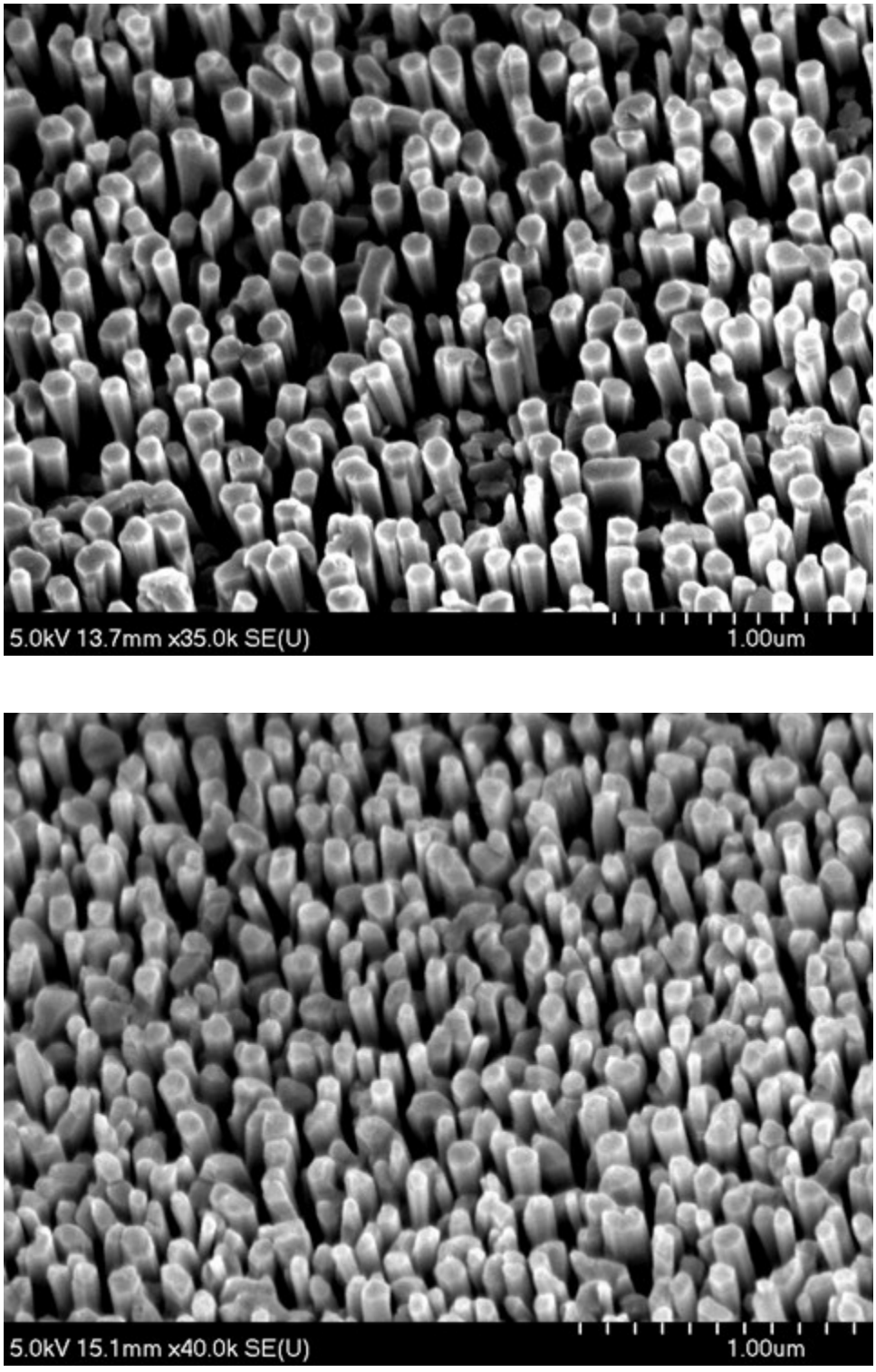


Fig. 5.10 – SEM micrographs of sample A near the edge.

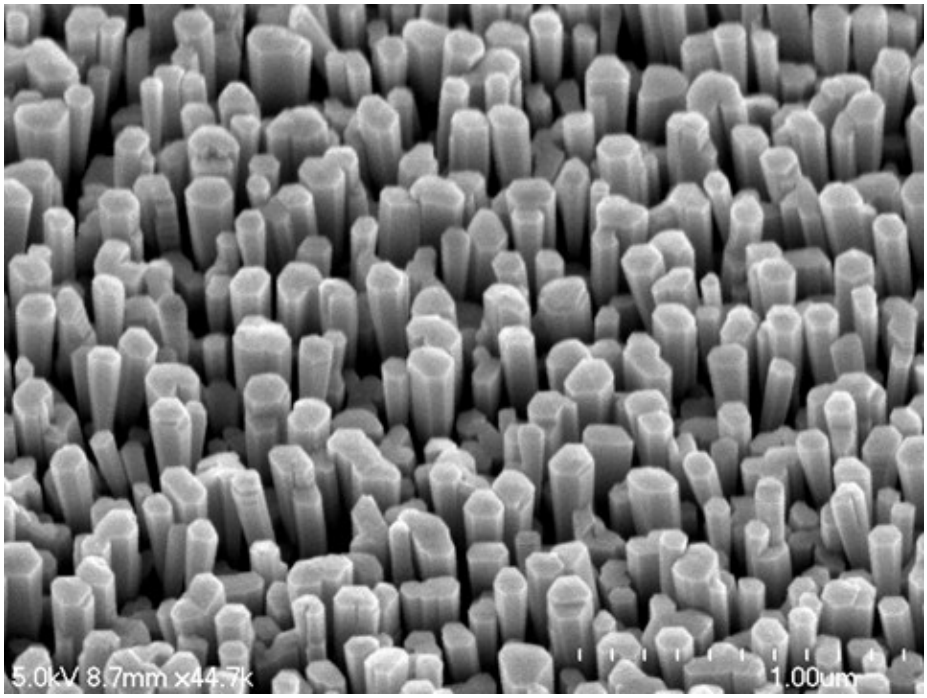


Fig. 5.11 – SEM micrographs of sample B near the middle point between the center of the wafer and the edge.

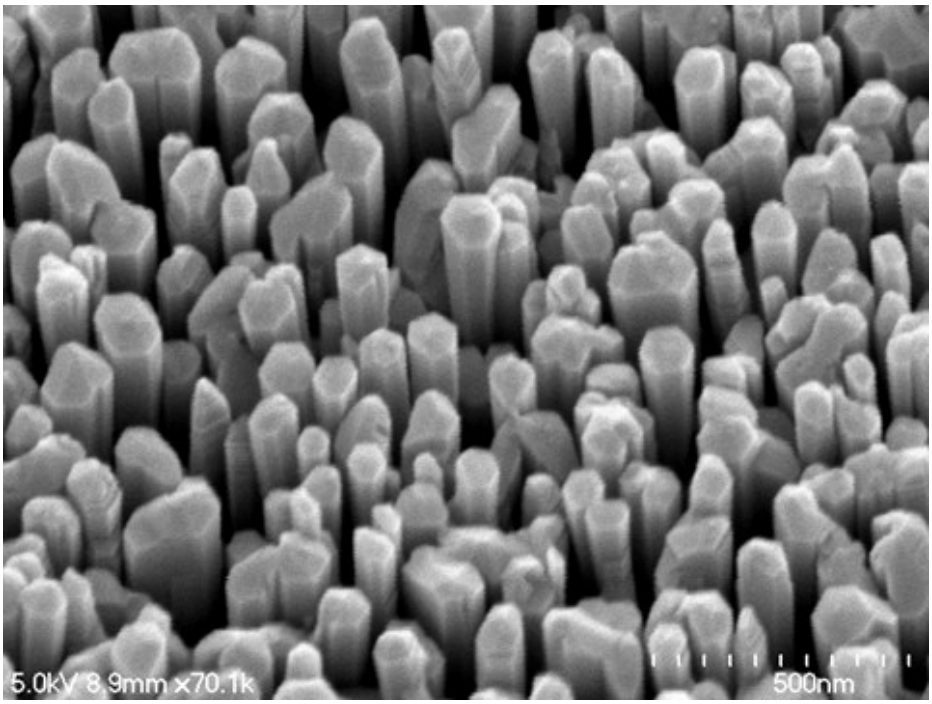
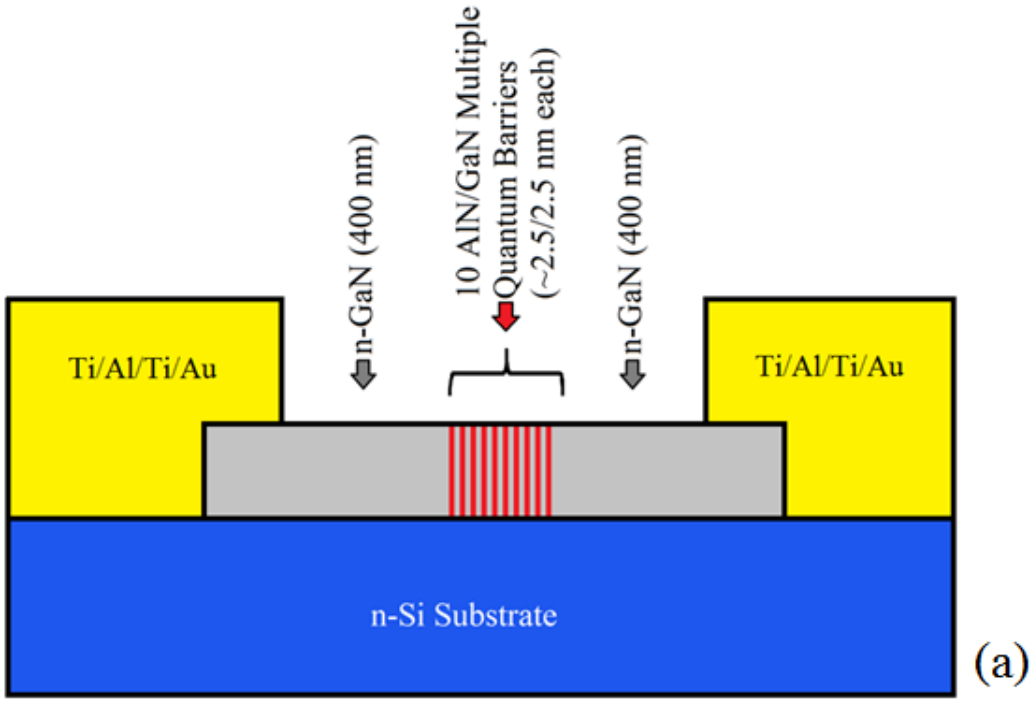


Fig. 5.12 – SEM micrographs of sample B near the edge.

5.3 Fabrication of Devices

Once the GaN/AlN nanowires are grown, single nanowire and large area nanowire devices can be made using a standard photolithography process. The cross sectional views of both devices are shown in figure 5.13. The single nanowire device is a horizontally placed GaN/AlN nanowire sitting on a silicon substrate with metal contacts at either ends. On the other hand, the large area nanowire device consists of millions of nanowires standing vertically and being contacted at the tip of the nanowire as well as at the bottom of the substrate. The fabrication procedure for the single nanowire will be discussed first, followed by the large area nanowire device. The details on the device fabrication can be found in appendix A.



(a)

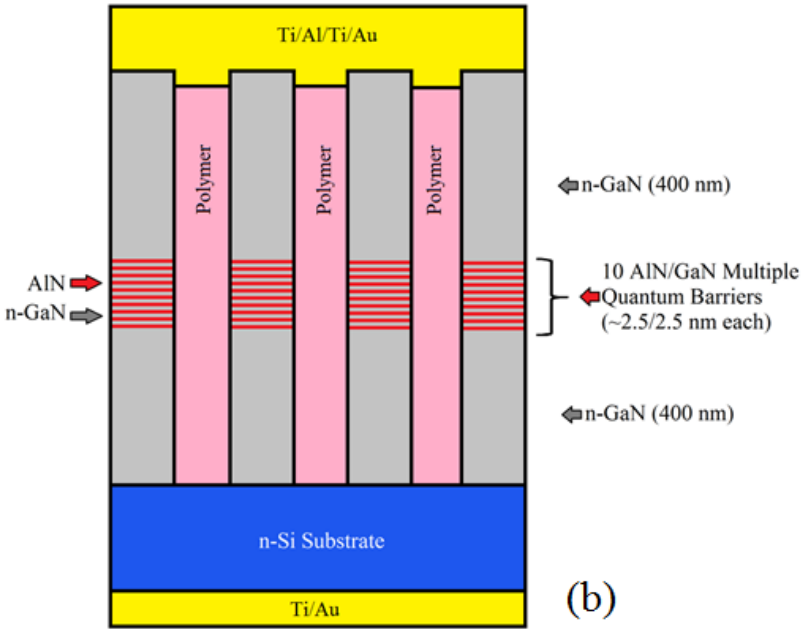


Fig. 5.13 – Cross-sectional views of (a) a GaN/AlN single nanowire device and (b) a GaN/AlN large area nanowire device.

For the single nanowire device, the nanowires are transferred from the growth substrate to a metal pre-patterned silicon substrate, shown in figure 5.14. The pre-patterned substrate helps in the alignment phase of the electron beam lithography (EBL) process. The nanowires can be cut with a knife. This, unfortunately, can damage the wires due to the relatively large thickness of the blade. Moreover, using a knife resulted in an excessive amount of nanowires (>1000) bunched together once transferred onto the pre-patterned substrate, rendering the metal contacting of a single nanowire near impossible. Instead of cutting them, they can be ripped away from the silicon wafer by vibrational motion in an ultrasonic bath, which typically resulted in a workable amount of undamaged nanowires. The nanowires are then accumulated in DI water which is

used to deposit them horizontally onto the pre-patterned substrate. This method, however, appeared to create moisture surrounding the nanowires, making metal contacting difficult. Following the nanowire deposition, the sample is submerged in hydrochloric acid (HCl) prior to the metal deposition to remove any native oxide that may reside on the surface. In this case, etching did not seem to remove the thin moisture surface layer on the nanowires. Alternatively, nanowires could be transferred mechanically by having the growth substrate and the pre-patterned silicon substrate face to face with slight rubbing between the two, avoiding the use of DI water. A standard EBL process, with the help of a Hitachi SU-70 scanning electron microscope (SEM) seen in figure 5.15, is used to pattern the two Ti/Al/Ti/Au metal contacts on either ends of the nanowire, with thicknesses of 10/50/10/100 nm. A Temescal E-Beam Evaporator BJD 1800, shown in figure 5.16, is used to deposit the different metals sequentially. A rapid thermal annealing (RTA) process is followed at 550 °C for 1 minute to create ohmic contacts. Annealing temperatures above 550 °C is avoided due to the relatively low GaN/AlN nanowire growth temperatures. The final single nanowire devices are showcased via an optical microscope and SEM micrographs in figures 5.17, 5.18, and 5.19.

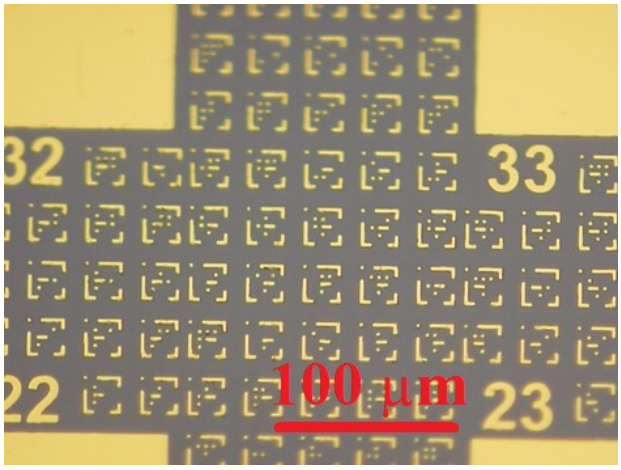


Fig. 5.14 – Close up of the metal pre-patterned silicon substrate used for alignment purposes during the EBL process.

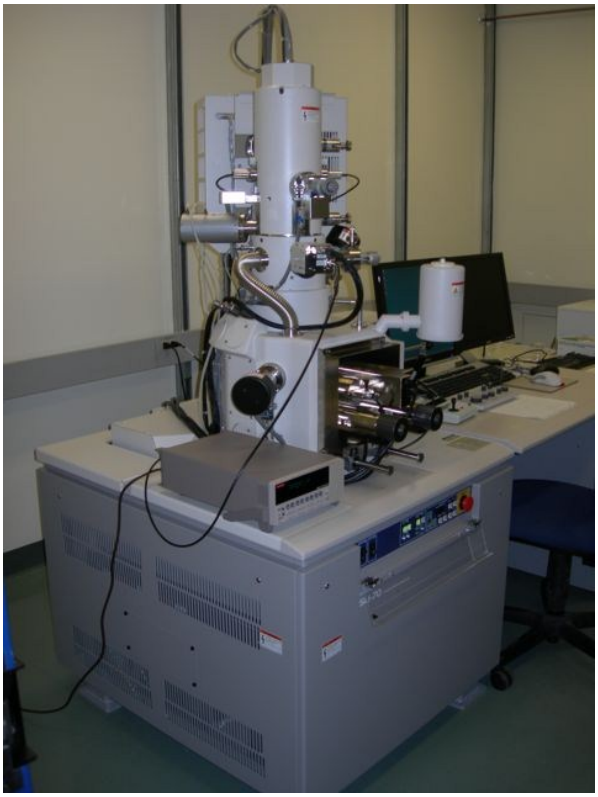


Fig. 5.15 – Hitachi SU-70 Scanning Electron Microscope (Szkopek, 2012).

Fig. 5.16 – The Temescal E-Beam Evaporator BJD 1800 (Photonics.com, 2002).

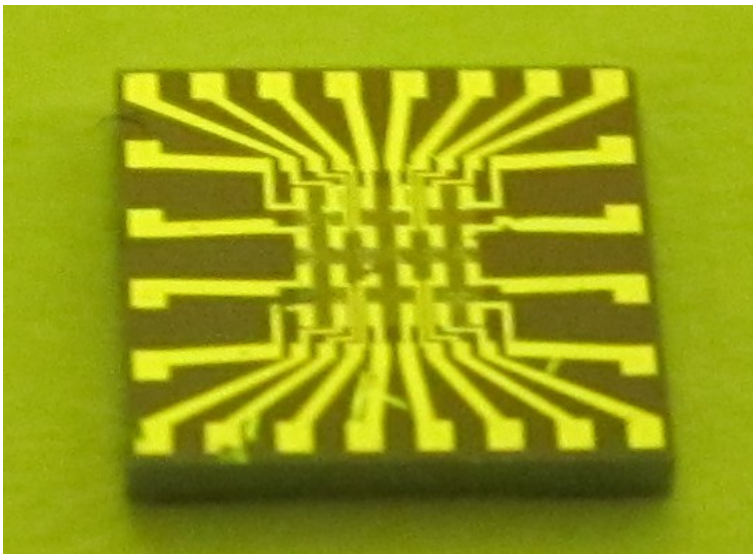


Fig. 5.17 – Pre-patterned silicon substrate (~3.5 mm by 3.5 mm) with metal contact pads used for measurement probing. Single nanowire devices are fabricated here.

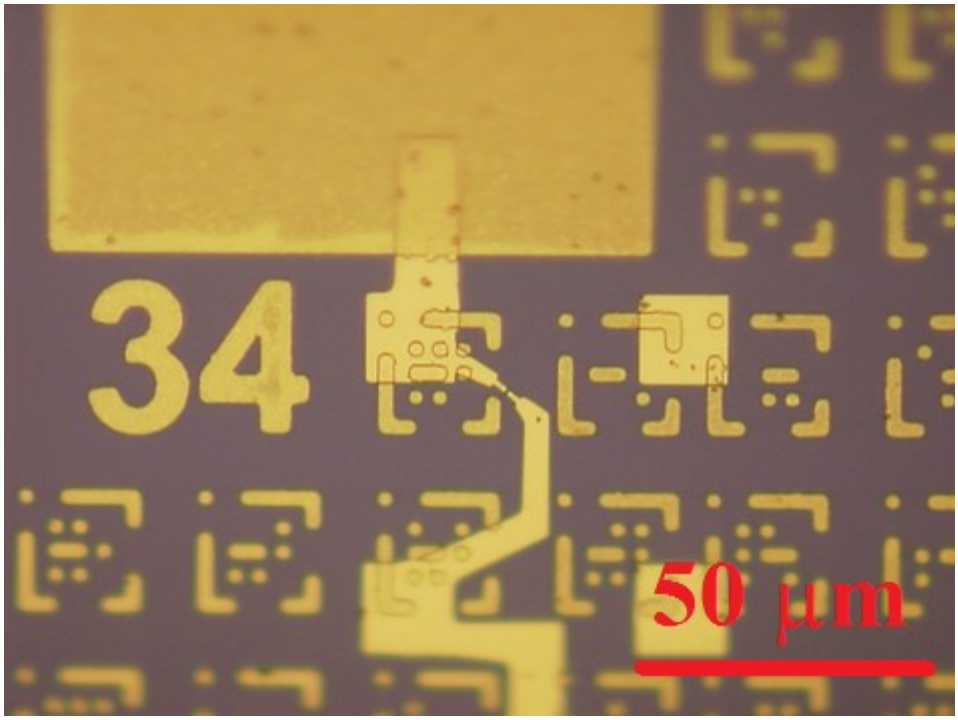


Fig. 5.18 – An optical micrograph (40x) of the metal contacts on a single nanowire device.

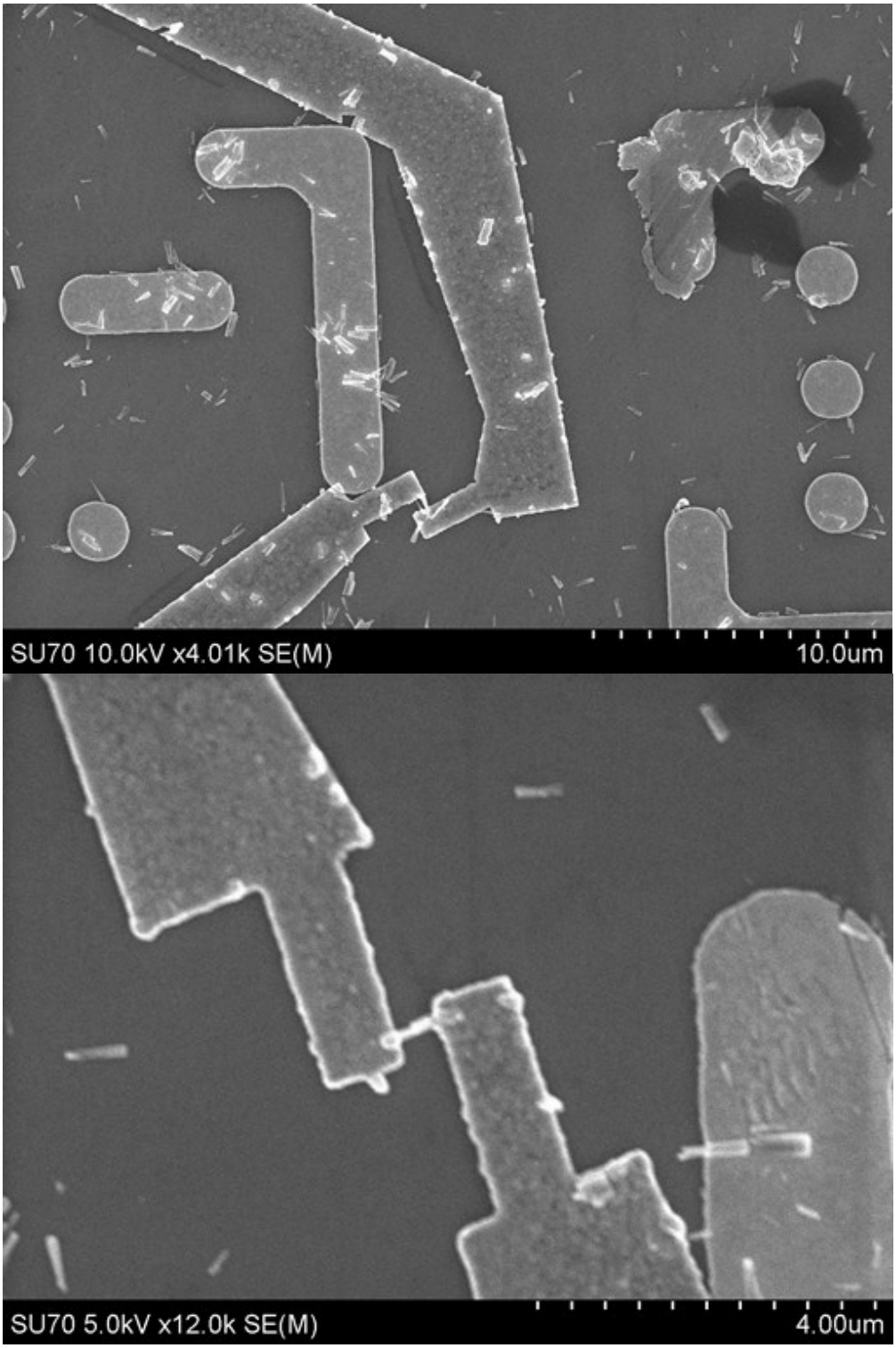


Fig. 5.19 – SEM micrographs of two single nanowire devices, from sample B.

For the large area nanowire devices, the nanowires were left standing vertically on the silicon substrate it was grown on. After a cleaning process involving acetone and DI water, a metal contact made of titanium and gold with thicknesses of 10 and 100 nm respectively was deposited on the back side of the substrate. RTA was performed at 550 °C for 1 minute. The samples are then submerged in HCl to remove any native oxide that may have formed. The top metal contact is then deposited on top of the standing nanowires and consists of a Ti/Al/Ti/Au combination with thicknesses 10/100/10/100 nm. However, before this is done, a thick polyimide (Pyralin Polyimide Coating – PI2732) needs to be spin-coated onto and between the columns to give the nanowires support. A series of reactive ion etching (RIE) and SEM imaging steps are performed to have the tip of the nanowire sticking out of the polyimide layer. Once the RIE is successful, the top metal contact may be deposited. Finally, another RTA process at 450 °C for 1 minute is performed. A lower annealing temperature is used to avoid damage to the underlying polyimide. The final large area nanowire devices are shown in figures 5.20 and 5.21. SEM micrographs of the top metal contact were also taken after fabrication, seen in figure 5.22. It appears that the top metal does not cover uniformly the nanowires, leaving the surface rugged. In some areas, there are relatively deep cavities indicated by the darker regions in the SEM micrograph between the nanowires. Although unclear on how deep these cavities are, they may or may not play a role in the current flow. In other words, it is possible for the metal deposited into these cavities to short circuit the active region. Continuing optimization of the fabrication procedure is needed to remove the irregular top metal contact.

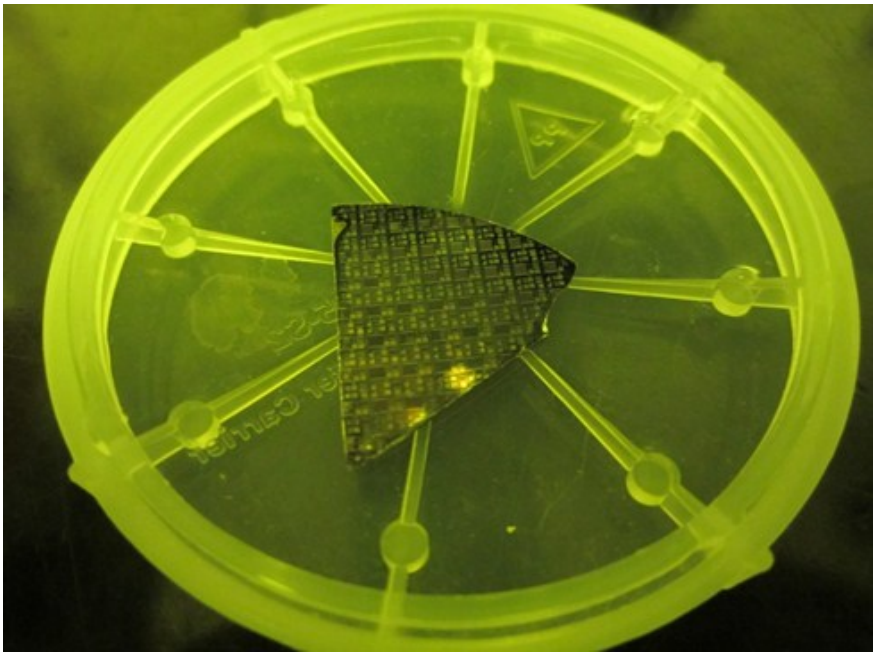


Fig. 5.20 – Array of large area nanowire devices fabricated on a 2-inch silicon wafer, cut into a pie-shaped pieces.

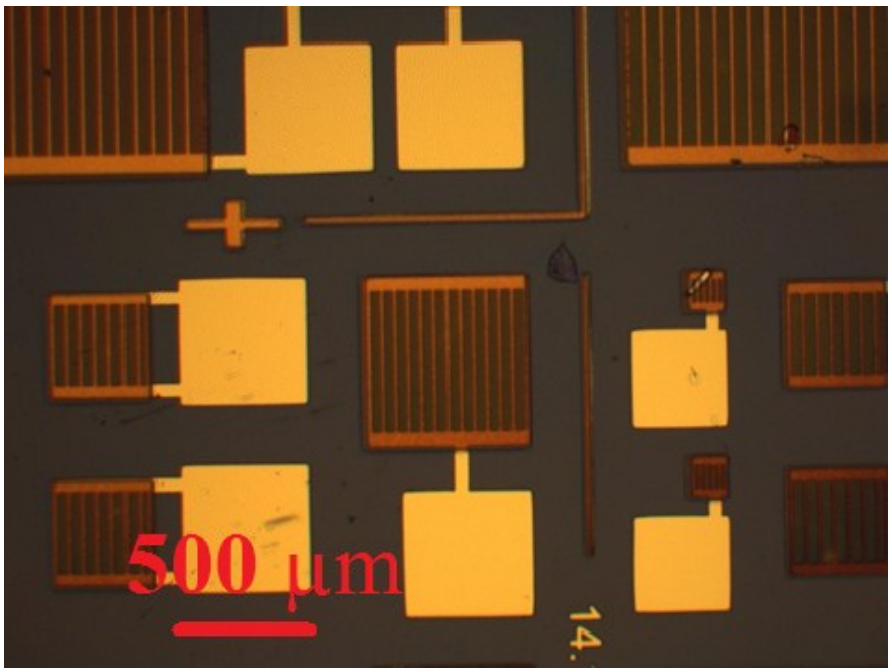


Fig. 5.21 – Optical micrograph of large area devices.

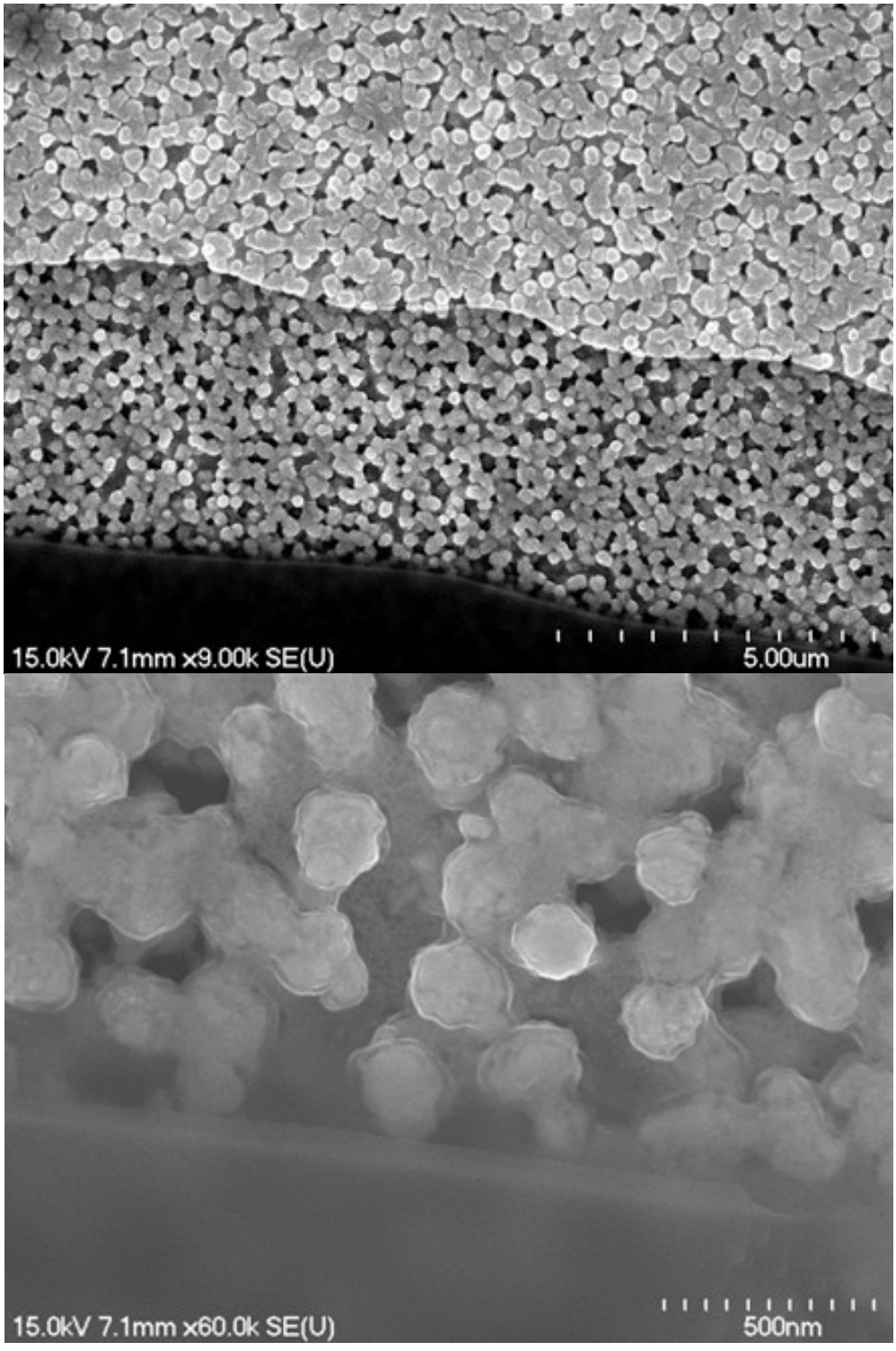


Fig. 5.22 – SEM micrographs of the top contact of a large area device made from sample A, highlight non-uniform metal deposition across the nanowires.

Chapter 6 – Electrical Measurements

6.1 Experimental Setup

The experimental setup is shown in figures 6.1. A ST-500 LHe/LN2 Cooled Probe Station from the Janis Inc. was used to measure the electrical properties of the devices, seen in figure 6.3. The probe station has four available probes, a substrate contact port, liquid nitrogen or liquid helium exchange port, and a small test chamber. The test samples are placed inside the probe station onto a metal plate. The probe station can achieve high vacuum of 5E-6 Torr after pumping overnight with a turbo pump, shown in figure 6.4 (a). Once the high vacuum is achieved, the chamber can also be cooled down with liquid nitrogen to 77 K via an exchange line, seen in figure 6.4 (b). Liquid nitrogen boils at 77 K and it is the resulting nitrogen gas that cools down the probe station. An auxiliary source of RT nitrogen gas can be used to help circulate the cool nitrogen into the probe station, effectively reducing the overhead time. The temperature of the stage is further varied by a temperature controller which allows one to vary the temperature between 77 K and RT. It takes 10-15 minutes for the chamber temperature to stabilize at the value set by the temperature controller. The center piece of the experimental setup is the Keithley 2400 power source, shown in figure 6.2. The Keithley 2400 power source is used to apply voltage across the devices and to measure the resulting current, with a measuring accuracy of 0.012% and 5 ½ digit resolution. The voltage is supplied by the Keithey power source via a Bayonet Neill-Concelman (BNC) connector and cable, with the core

propagating the signal and the shell being grounded. A BNC cable box was prepared to split the signal and ground into two separate BNC cables, each leading into different needle probes.

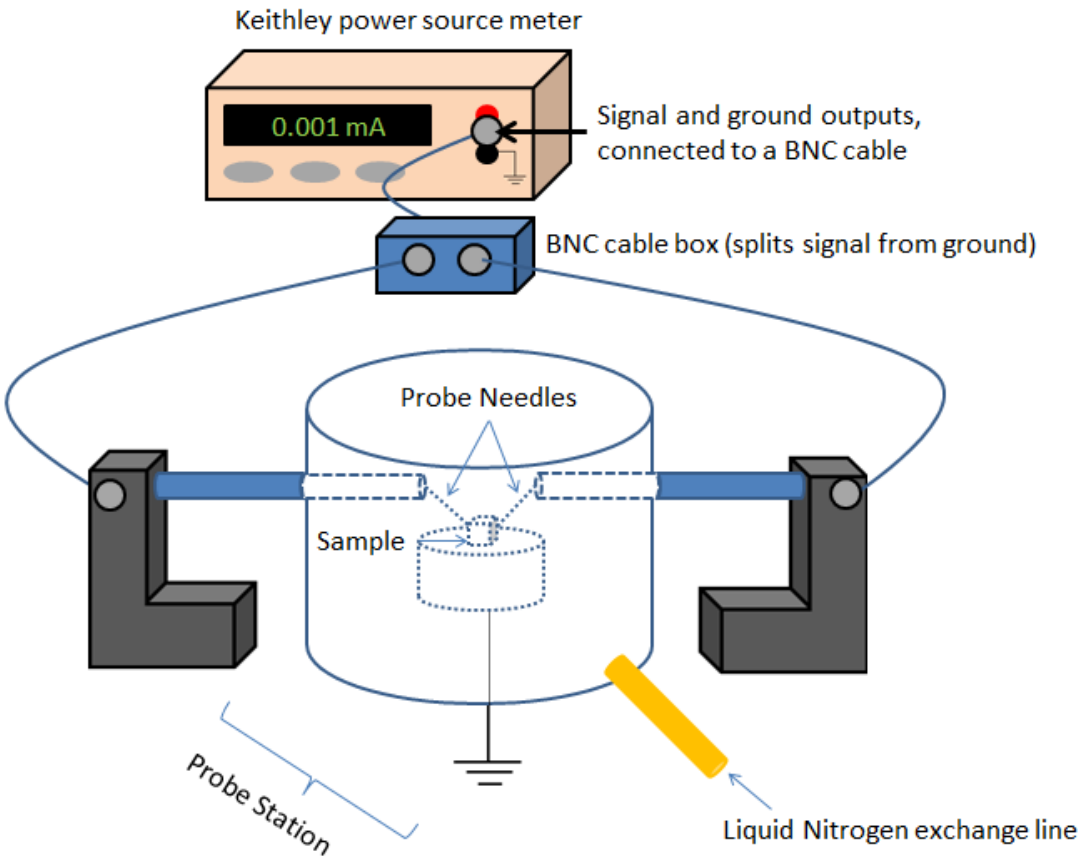


Fig. 6.1 – A schematic of the experimental setup

Fig. 6.2 – Keithley 2400 Power Source Meter (Keithley).

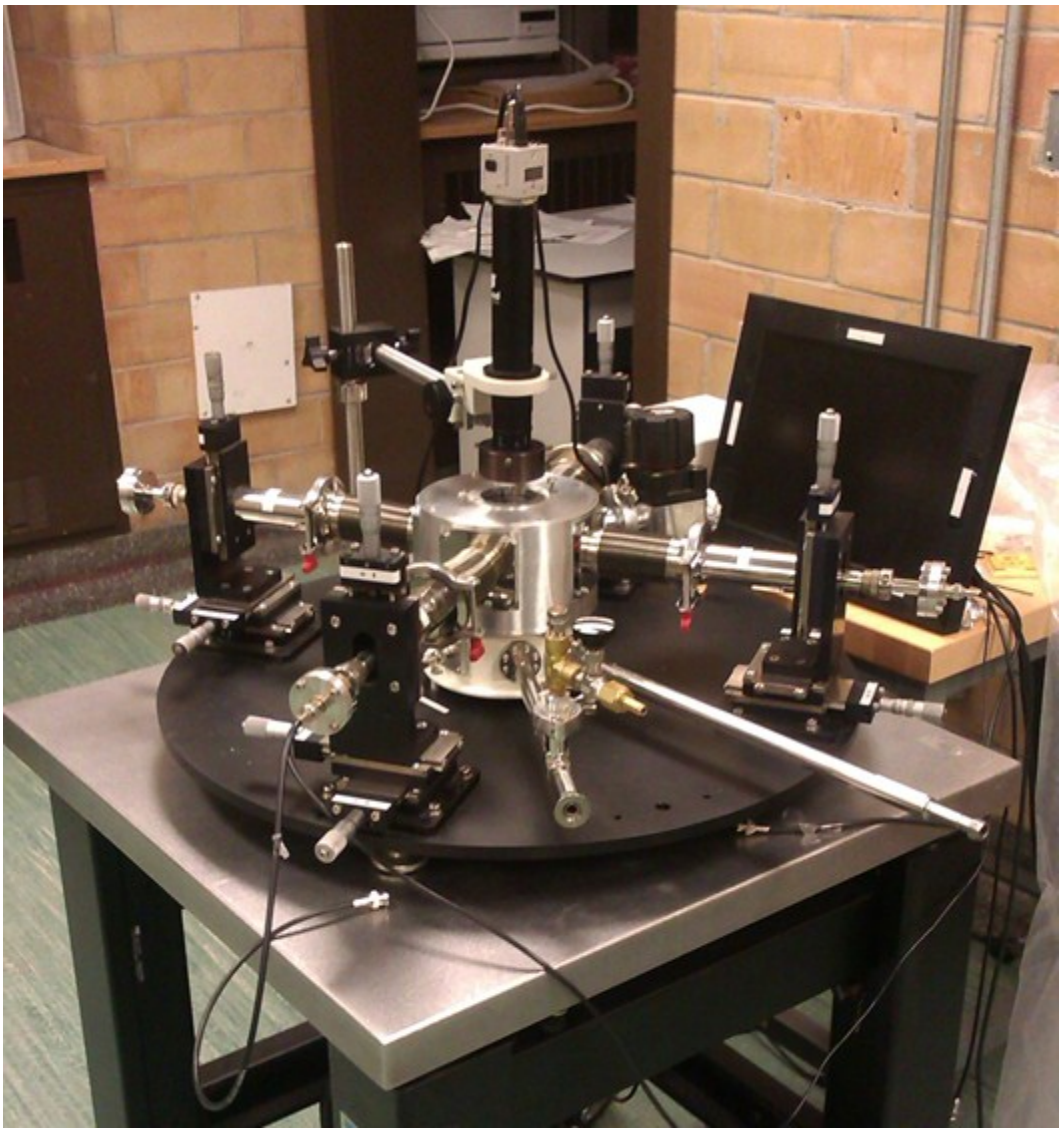


Fig. 6.3 – ST-500 LHe/LN2 Cooled Probe Station used to measure the electrical properties of the nanowire devices.

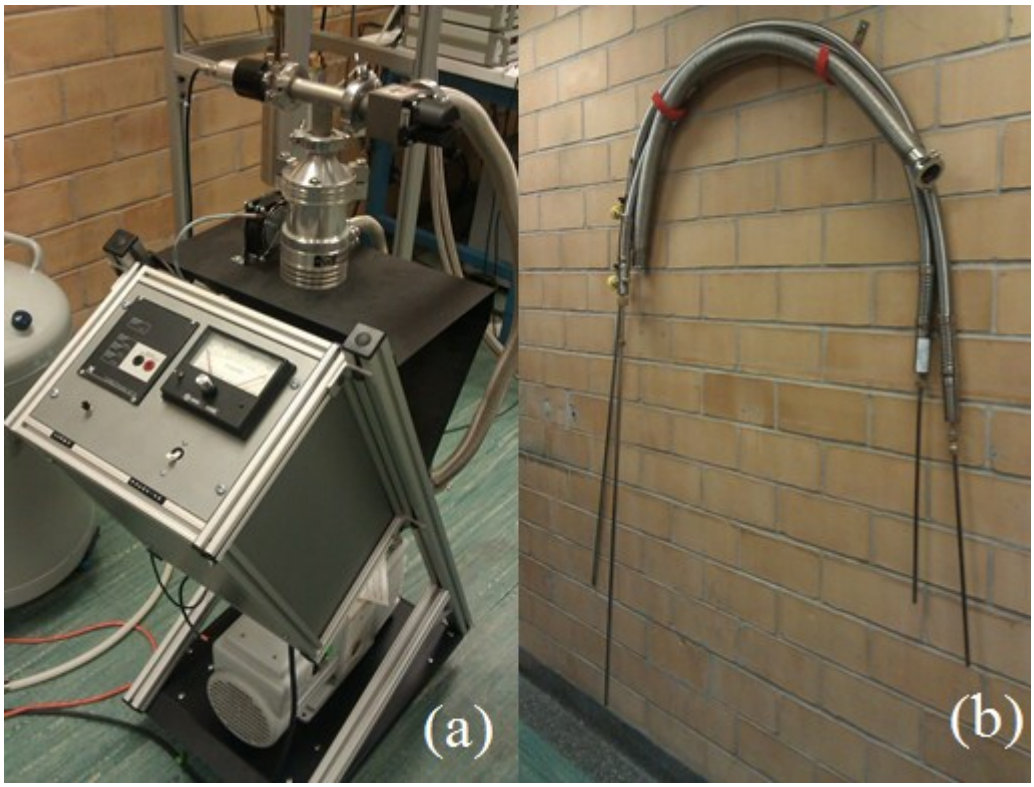


Fig. 6.4 – (a) Turbo Pump used to achieve high vacuum conditions in test chamber. (b) Exchange lines used to cool down the test chamber with liquid nitrogen.

Setting a common ground throughout the experimental setup is crucial to avoid unnecessary noise. Therefore, the stage was directly connected to the ground supplied by the power source.

The measured current from the power source can be extracted via a GPIB to USB connector and interfaced with a standard LabView virtual instrument. A screenshot of the LabView virtual instrument used is shown in figure 6.5.

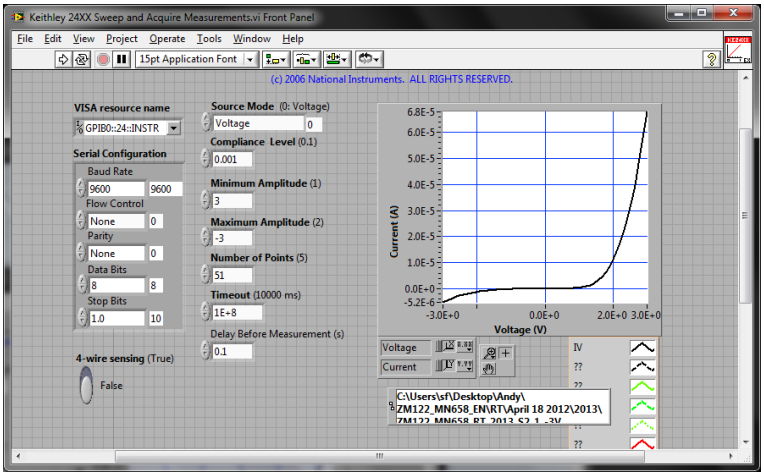


Fig. 6.5 – LabView virtual instrument used to acquire electrical measurement data from the nanowire devices.

6.2. I-V Measurement Methods

With the experimental setup as described in the previous chapter, I-V curves can be measured from single nanowire and large area nanowire devices. I-V curves are produced by applying a signal bias across the two terminals of the device via the conducting probes and a power source. Specifically, voltage sweeps are performed in this project, in which the voltage is varied linearly between two end values. The current is then extracted by the power source and is plotted against the voltage to yield an I-V curve in which properties like negative differential resistance can be identified and quantified. During the I-V measurements, a current compliance is set to 10-100 μA in an attempt to prevent accidental burning of the nanowires.

Electrical measurements were done systematically in the following way. The probes are initially brought into contact with ground to remove any residual charges that may destroy the nanowires upon contact. From there, the probes are

lifted and are brought gently onto the metal contacts with the help of a live feed camera. Once the probes are in place, the peripheral electronic machinery (light source, camera and live-feed monitor) is turned off to minimize noise generation. Furthermore, the top of the sample chamber is covered to prevent any light from shining onto the samples. The pattern of the voltage sweeps were initially swept from a negative to a positive value, but was later changed to adopt a more systematic measurement which involved starting at zero bias, increasing towards a positive value (Vmax), decreasing towards a negative value (Vmin), and finally coming back to the initial zero bias, effectively completing one voltage sweep cycle. Vmax and Vmin were initially set relatively low (+/- 0.5-1 V) and were increased on every cycle up to 15 V in some cases. This was done progressively to prevent the nanowires from burning prematurely due to high voltage bias. Typically, it was found that applying a few voltages (~ 3 V) more than the V_{peak} resulted in the damaging of the device and an open circuit. Temperature dependence tests were also performed, and typically involved voltage sweeps at RT, 77 K, 100 K, 125 K, 150 K, 200K and 250 K, in that order.

Chapter 7 - Results and Discussion

The I-V measurement results for single nanowire as well as large area nanowire devices, made from samples A, B and C, mainly at RT and at 77 K are presented below. Hundreds of devices have been made, with the fabrication procedure going through multiple iterations. Here, a total of 13 devices that best represent the general trends are highlighted and their specific behaviours are outlined.

7.1 - Single Nanowire Devices

Test results on single nanowire devices made from sample A were taken. In general, the devices exhibited relatively large currents (0.1 - 1 mA range) with relatively low resistance (1 - 10 kΩ range) and little to show of NDR, even at 77 K. The I-V characteristic of device 1 is shown in figure 7.1. No NDR was found in this device; however, it did have some form of oscillations in current.

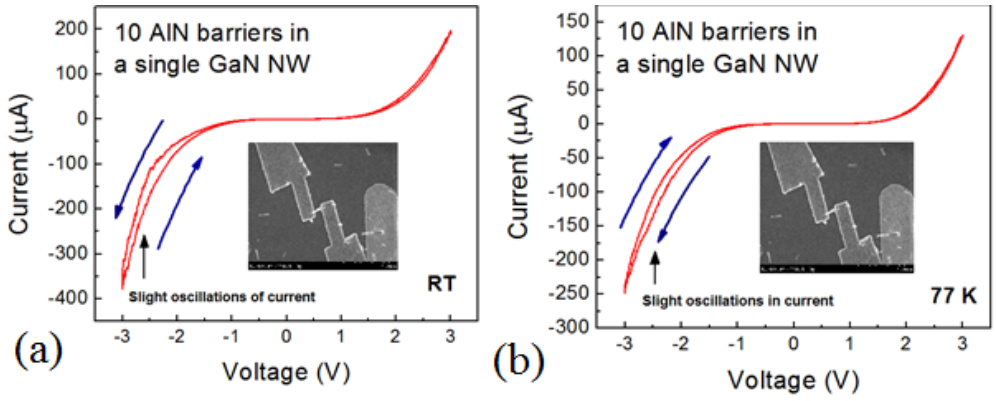


Fig. 7.1 – I-V characteristics of device 1 (single nanowire, sample A) at (a) RT and at (b) 77 K.

Although there was a relatively low success rate with the single nanowire devices made from sample A, some did show clear signs of multiple NDR regions at both 77 K and room temperature. The I-V measurements of one of those devices (device 2) are shown in figure 7.2. Multiple voltage sweeps were performed to evaluate the stability of the device. On the first voltage sweep, ranging from -7 to 7 V, three distinct NDR regions appeared with peaks at ~ 5.92, 6.35 and 6.76 V, indicating the alignment of the resonant energy states with one another in the multiple quantum wells, as shown in figure 7.2 (a). The peak-to-valley ratios of the three NDR regions are ~ 2.1, 1.44 and 1.24. Large oscillations were also observed in the reverse negative bias. A secondary voltage sweep was performed to evaluate how well the device could reproduce its electrical behaviour. The second voltage was also increased to range from 0 to 10 V to see if extra peaks would occur beyond 7 V. As seen in figure 7.2 (b), the peaks that once appeared at around 6 V now increased to the range between 7 and 8 V, with twice as much current. Moreover, the peaks were not as clearly defined as the ones in the first voltage sweep. At 8.5 V, the device undergoes a sudden change with a large increase in current, going from 30 μA to nearly 100 μA. This sudden change in current also permanently changes the electrical behaviour at lower voltage, as seen in the subsequent voltage sweeps number three and four in figure 7.2 (c) and (d) respectively. In the second voltage sweep, current peaks occur at ~ 8.56 and 9.38 V with many oscillations along the peak and valley. On the third voltage sweep, the device was swept from 0 to 12 V. Potential NDR regions were once again observed between 6 and 8 V. The more apparent NDR regions, however, remained at the higher voltages of ~ 9 and 10.7 V with a potential NDR

region at ~ 10 V. A peak-to-valley ratio of 1.4 was achieved here. Upon performing the fourth and last voltage sweep, from 0 to 15 V, the device deteriorated and resulted in an open circuit. Thus, low temperature measurements were not performed. Most subsequent voltage sweeps were limited to ~10 V to avoid premature damage of the device.

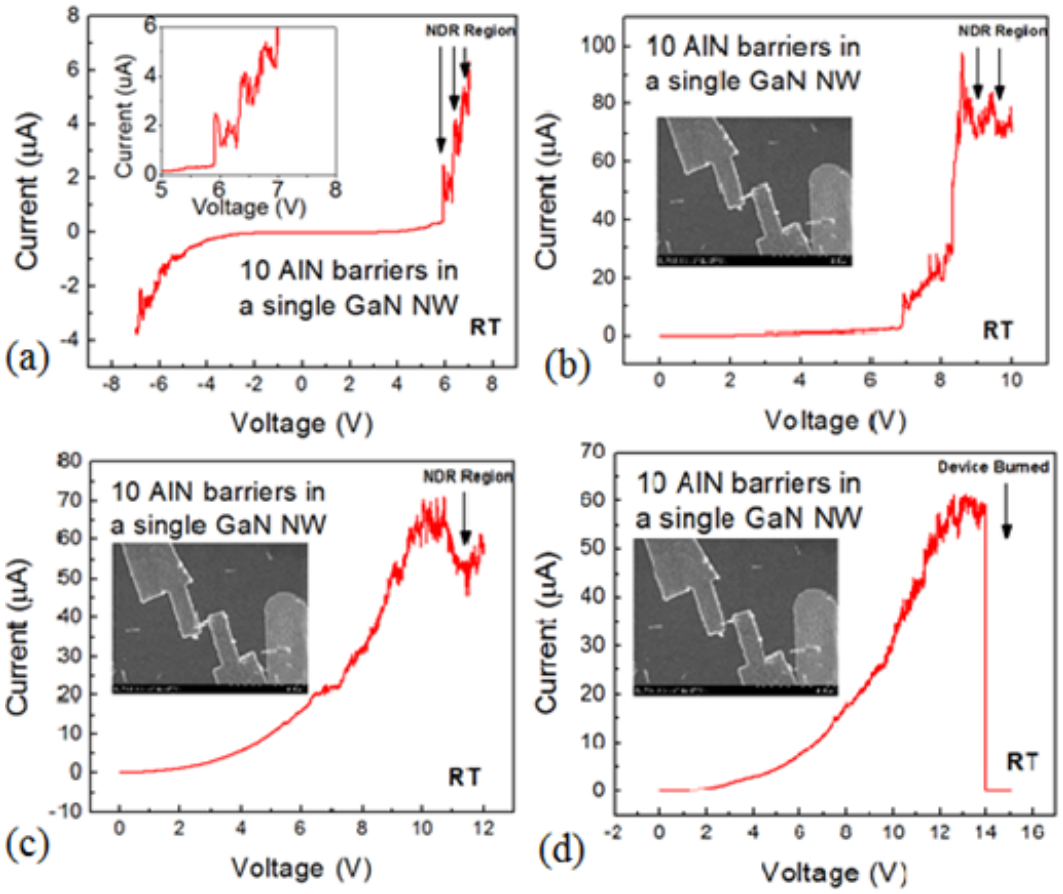


Fig. 7.2 - I-V characteristics of device 2 (single nanowire, sample A), at RT, measured at its (a) first, (b) second, (c) third, and (d) fourth voltage sweep.

Device 3 made from sample A is yet another working device exhibiting NDR. At RT, small NDR regions were detected at around ~9.2 V, as shown in figure 7.3. In this case, low temperature measurements were performed at 77 K and it was observed that an NDR region appeared at ~9.8 V. Unfortunately, upon the following voltage sweep, the device deteriorated, resulting in an open circuit characteristics. Nonetheless, it was found that this device showed much larger currents at lower temperatures (5 times more), which may have caused the accelerated loss of stability of the device. It would be determined, later on, that devices with little to no NDR at RT but prominent NDR at lower temperatures typically had higher conductivity at lower temperatures, too. This matches well with the observations made in AlGaAs/GaAs superlattice structures (Capasso et al., 1985). However, previous works done on GaN/AlN superlattice nanowires showed the exact opposite in which decreasing temperatures brought higher resistivity as well as more prominent NDR (Rigutti et al., 2010). In this case, there is the possibility of a “hard breaking” in the device, in which a permanent physical change has occurred due to electrical stress.

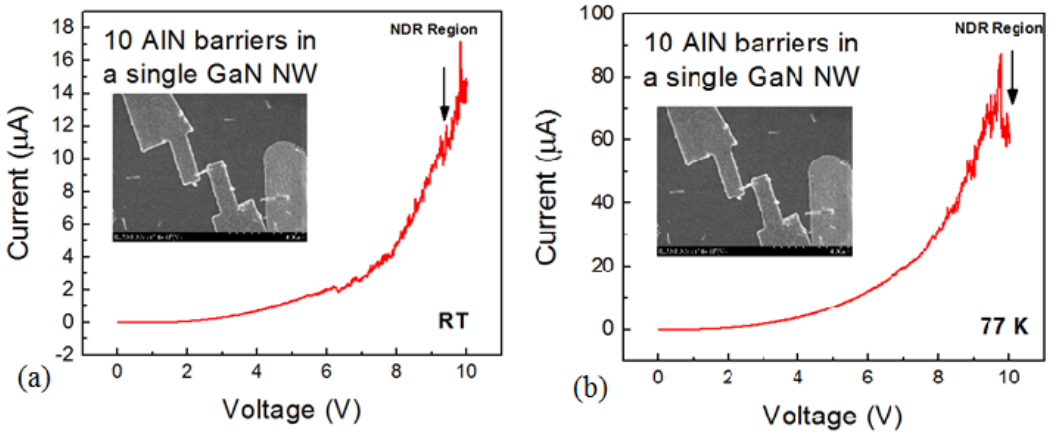


Fig. 7.3. - I-V characteristics of device 3 (single nanowire, sample A) at (a) RT and at (b) 77 K.

To improve the PVR ratio and the stability of the nanowire devices, properties necessary for the development of ultrafast oscillators, silicon doping was performed on the GaN quantum wells to introduce higher electron population in the active region. Sample B, as mentioned earlier, has a doping level of 2E16 cm^{-3}. In general, single nanowire devices made from sample B showed more prominent NDR and higher stability.

For example, device 4 from sample B shows highly stable and non-symmetric I-V characteristics, seen in figure 7.4.1. For one, the device was able to withstand 15 V bias multiple times without deteriorating in performance. This was highly atypical, with devices generally breaking down at lower voltages (anywhere between 5 and 12 V). The device was also able to maintain its electrical properties through multiple (more than 5) subsequent voltage sweeps, as shown in figure 7.4.2. NDR was mainly present at 77 K with a PVR of 1.9, but

was also distinguishable at RT with a PVR of 1.2. This result shows the potential for stable and highly repeatable GaN-based multiple quantum well nanowire resonant tunneling diodes. The temperature dependence test was also performed in the following manner. The room temperature characteristics were first measured, as shown in figure 7.4.1 (a). The temperature was then brought down to 77 K, which showed the large NDR region and a sudden increase in conductivity, as seen in figure 7.4.1 (b). Upon increasing systematically the temperature from 77 K to RT again (with intermediate temperatures of 100, 125, 150, and 200 K), the NDR region was slowly lost with the current remaining relatively constant, as seen in figures 7.4.1 (c) and (d).

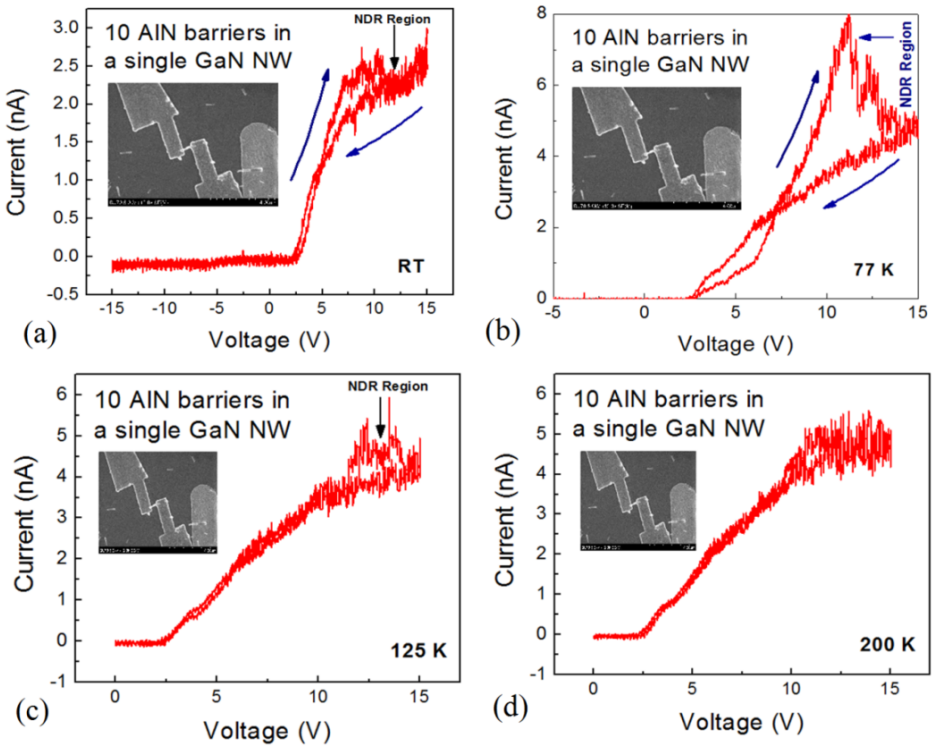


Fig. 7.4.1 - I-V characteristics of device 4 (single nanowire, sample B) at (a) RT, (b) 77 K, (c) 125 K, and (d) 200 K.

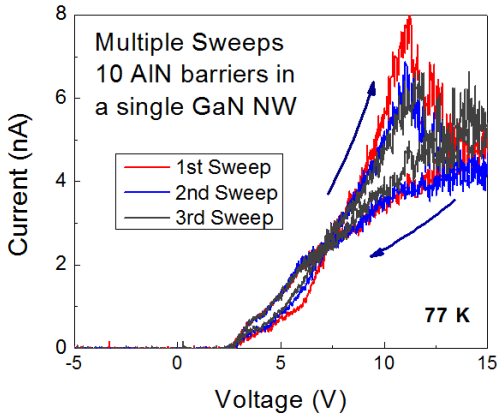


Fig. 7.4.2 - I-V characteristics of device 4 (single nanowire, sample B) at 77 K. Multiple sweeps show high stability of the device.

It was observed that hysteresis was only found in devices that had some form of pronounced NDR. Devices without NDR showed no signs of hysteresis. For example, device 4 showed hysteresis properties at 77 K, but no hysteresis is observed at higher temperatures once the NDR disappeared. Hysteresis can be attributed to the bias-dependent trapping of electrons in the quantum wells (Belyaev et al., 2003).

Device 5, made from sample B, also exhibits NDR and its associated hysteresis, as seen in figure 7.5. However, in this case, NDR was observed at room temperature with a PVR of 2.4, the largest reported in any single nanowire device in the present work, near the current peak of ~7.5 V. This was an exciting result and demonstrated the capabilities of GaN/AlN multiple quantum wells for room temperature operation, potentially making commercially available infrared imaging devices possible. NDR and hysteresis was also observed at 77 K with a higher conductivity than that found at RT.

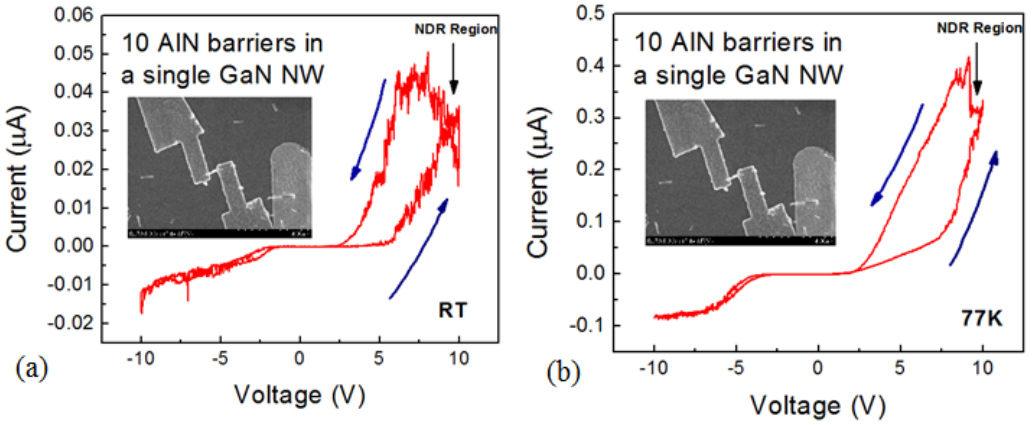


Fig. 7.5 - I-V characteristics of device 5 (single nanowire, sample B) at (a) RT and (b) 77 K

Device 6, made from sample B, also showed negative differential resistance at room temperature at around ~ 4.2 and 3.8 V for its first and second voltage sweep, as shown in figure 7.6 (a) and (b) respectively.

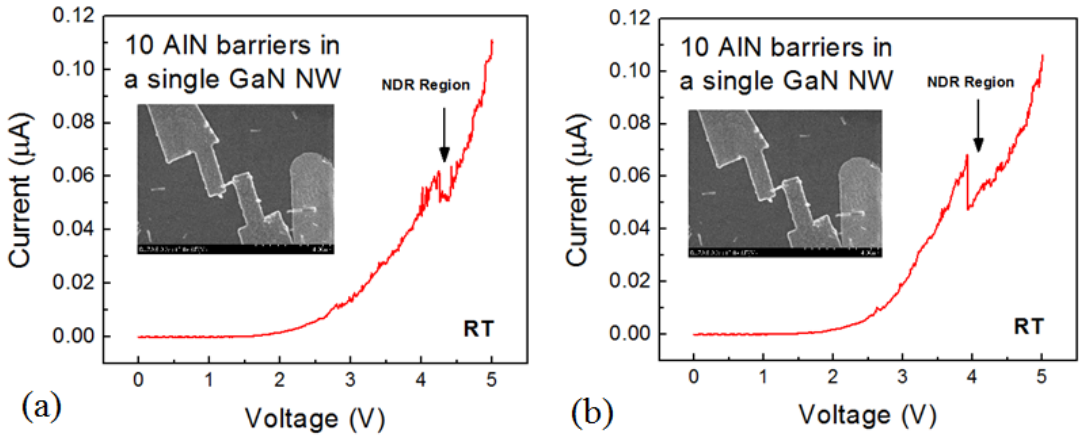


Fig. 7.6 - I-V characteristics of device 6 (single nanowire, sample B) at RT, showing only the forward bias for (a) its first voltage sweep and (b) its second.

More single nanowire devices were fabricated using sample C, which had an even higher silicon doping concentration compared to sample B in the GaN quantum wells. The idea was to see if the resonant tunneling features could be improved by further increasing silicon doping. Device 7, made from sample C, exhibited quite interesting I-V characteristics, as shown in figure 7.7. Although no apparent NDR was measured at RT, NDR appeared at temperatures ranging from 77 to 250 K with current peaks at ~10, 10.5 and 11.5 V. The highest PVR achieved with sample C is ~1.4. From the temperature dependence test, it is again highlighted that the conductivity is higher at lower temperatures than at room temperature. As temperature increases from 77 to 250 K, there is a slight tendency of decreasing conductivity.

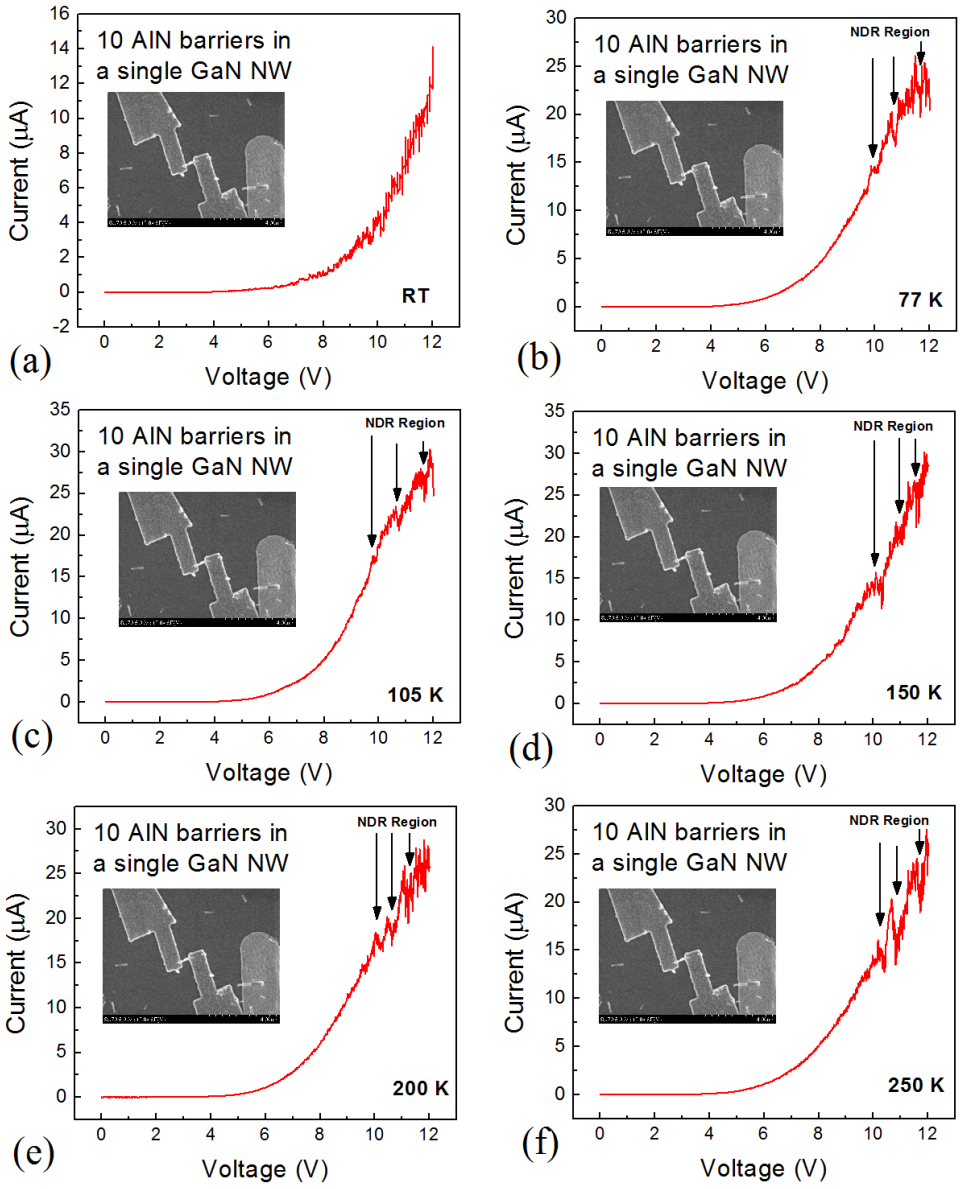


Fig. 7.7 - I-V characteristics of device 7 (single nanowire, sample C) at (a) RT, (b) 77 K, (c) 105 K, (d) 150 K, (e) 200 K, and (f) 250 K.

The addition of extra silicon doping (from sample B to sample C) did not appear to improve the appearance and stability of the resonant tunneling diodes. In fact, the yield was less compared to that of devices made from sample B. This

result, however, may be attributed to the less successful fabrication runs and may have been caused by experimental error.

Among all three samples, the single nanowire devices typically exhibited non symmetrical I-V characteristics. Although the nanowire structure is symmetrical, the conduction band diagram of the multiple quantum wells is affected by band bending due to the polarization nature of the III-V material. Moreover, devices that exhibited NDR showed much higher resistivity compared to those that did not at all. Resistance values ranged from 100 kΩ to 1 GΩ for NDR devices and ranged from 1 kΩ to 100 kΩ for non-NDR devices. This indicates that the resonant tunneling nature of the GaN/AlN nanowires is inherently quite resistive. Devices with no apparent NDR may be experiencing current flowing through the surface of the nanowire and bypassing the active region. Therefore, surface treatments by HCl etching have been added into the fabrication procedure to remove unwanted oxide layers or any other layers that may be covering the active region. The success of the surface treatment, however, is still unclear. Further measurements comparing with and without surface treatments as well as direct SEM imaging of the etching process constitutes potential future work for this project.

7.2 – Large Area Nanowire Devices

Large area devices were also measured. Generally, it was harder to achieve NDR compared to the single nanowire devices, due to the non-uniformity of the height of the nanowires locally and across the silicon wafer. It was shown in a previous chapter that the nanowires were tapered and coalescing to each other.

This can lead to unwanted short circuiting of the nanowires, with the current bypassing the active region. Moreover, the variation in the growth temperature across the silicon wafer caused varying nanowire heights and quality, making it hard to contact all the nanowires at the same time. Good devices, nonetheless, were still made with a PVR reaching 3.14. Similar trends are observed in the large area nanowire devices as in the single nanowire devices.

Device 8 is the first large area nanowire device tested from sample A. The I-V characteristics are non-symmetric with small NDR regions at 3 V. The curve was shown to exhibit some hysteresis properties, with the directions of the curve indicated by the blue arrows in figure 7.8. Similar to the single nanowire devices, the conductivity of the device also increased when going towards a lower temperature.

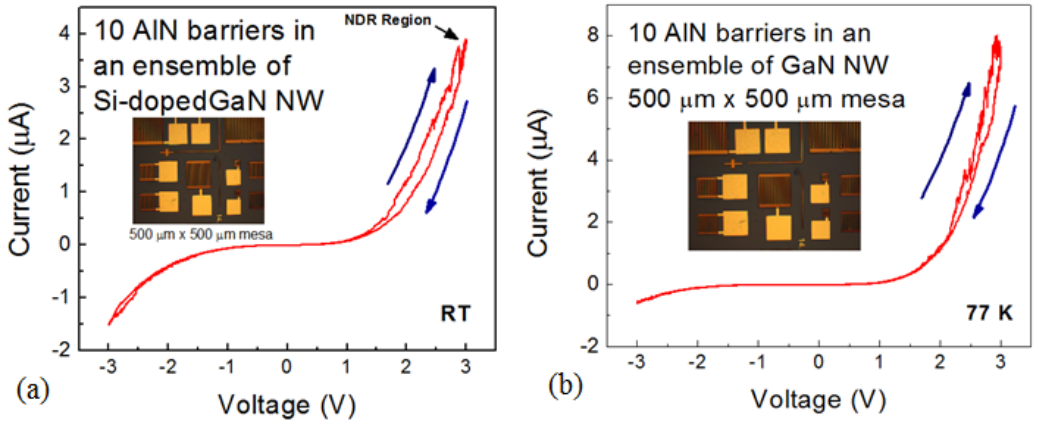


Fig. 7.8 - I-V characteristics of device 8 (large area, sample A) at (a) RT and at (b) 77 K.

Device 9 shows signs of NDR at 77 K but not at RT, seen in figure 7.9.1, with a PVR of ~2.2. The device exhibited varying electrical behaviour on subsequent voltage sweeps. In figure 7.9.2 (a), the first voltage sweep at 77 K shows NDR regions as well as hysteresis at a low current. In figure 7.9.2 (b), the second voltage sweep showed a large increase in current. In figure 7.9.2 (c), the current decreases considerably with the device burning at ~-3V. Subsequent voltage sweeps performed displayed no NDR and no hysteresis, as seen in figure 7.9.2 (d). Although the device appeared to have been broke down, a temperature dependence test was still performed. The I-V measurements at low temperature (77 K, 125 K, and 150 K) showed no NDR. However, at 200 K, the device showed clear signs of NDR and hysteresis in the negative bias of figure 7.9.3. The reappearance of NDR at 200 K accompanied by a large current might be attributed to the slight shifting of the probe during temperature variations and thermal expansion. It was noted for large area devices that even though they might break down and result in open circuit current, the probe could be moved to another position on the metal contact and seemingly measure a different electrical property. It is possible that when a device is burned, only the nanowires and the metal contact positioned directly under the probe are destroyed. The temperature dependence test showed increasing conductance for increasing temperature.

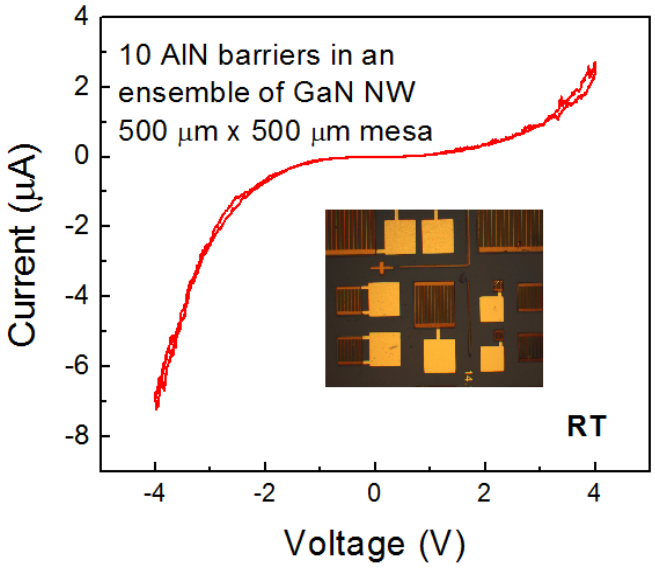


Fig. 7.9.1 - I-V characteristics of device 9 (large area, sample A) at RT. No NDR was present.

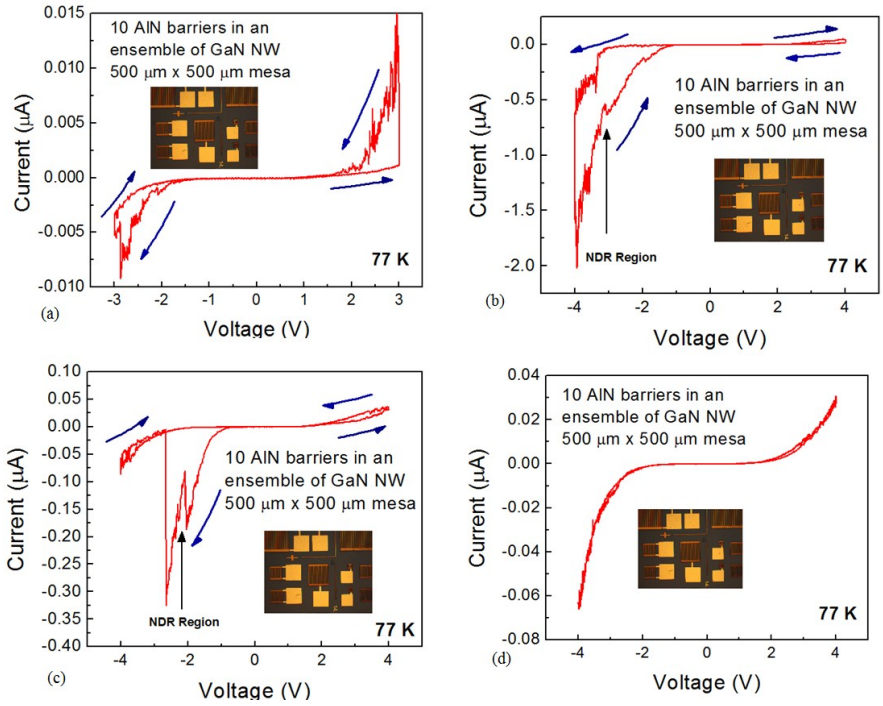


Fig. 7.9.2 - I-V characteristics of device 9 (large area, sample A) at 77 K for its (a) first, (b) second, (c) third and (d) fourth voltage sweep.

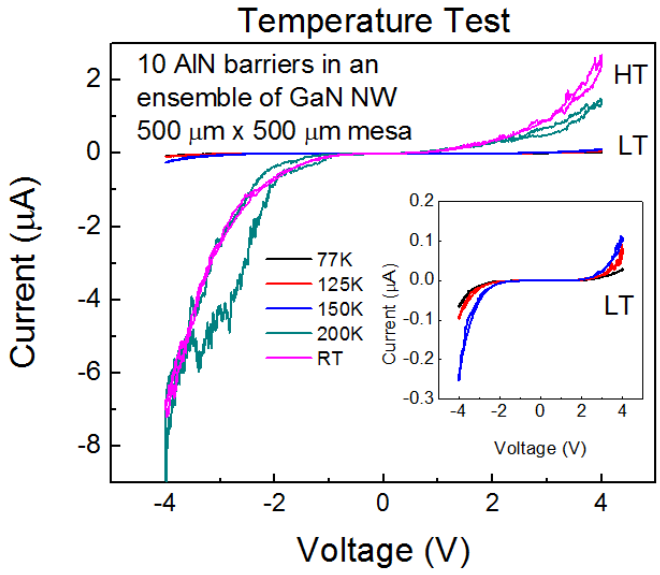


Fig. 7.9.3 – Temperature dependence test, from 77 K to RT, performed on device 9 (large area, sample A) after performing the multiple voltage sweeps at 77 K. NDR reappears in the electrical characteristics at 200 K.

Device 10, made from sample A, represents one of the few large area nanowire devices that were able to exhibit NDR at room temperature, with a PVR of 1.274, shown in figure 7.10.

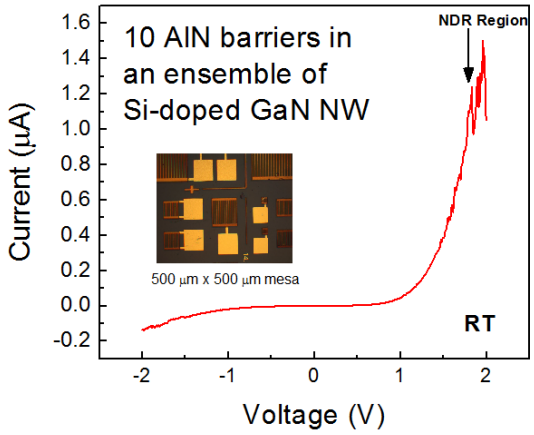


Fig. 7.10 - I-V characteristics of device 10 (large area, sample A) at RT.

Device 11 summarizes the results measured from sample B. Little to no NDR was present in any of the devices. Even though sample B provided the best single nanowire devices, large area devices were unsuccessful. High currents were measured (milliamp range) through the devices, indicating some unwanted short circuiting of the device. Current oscillations, nonetheless, were observed.

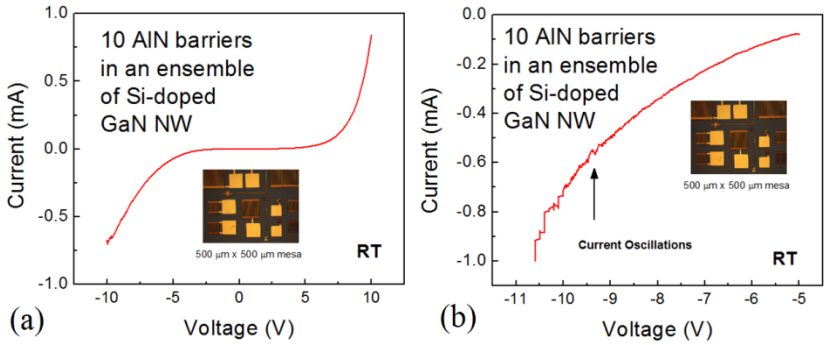


Fig. 7.11 – I-V characteristics of device 11 (large area, sample B) at RT. (a) Full voltage sweep and (b) close up on current oscillations near -10 V.

Device 12, made from sample C, displayed no NDR at room temperature, but significant peaks emerged at 77 K, seen in figure 7.12.1 through 7.12.3.

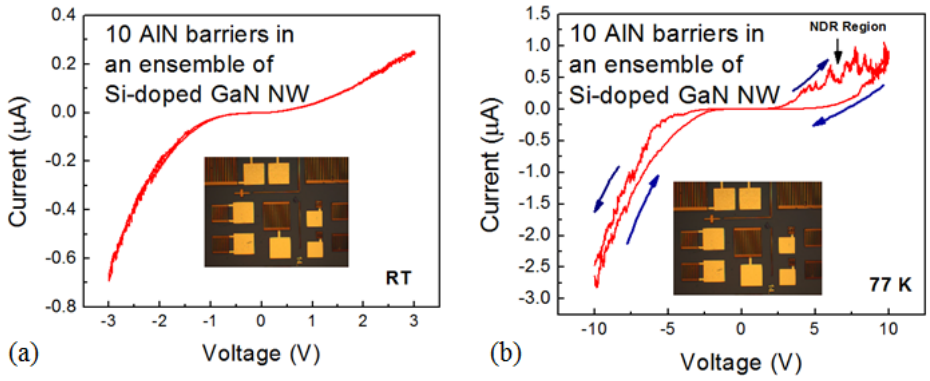


Fig. 7.12.1 - I-V characteristics of device 12 (large area, sample C) at (a) RT and at (b) 77K.

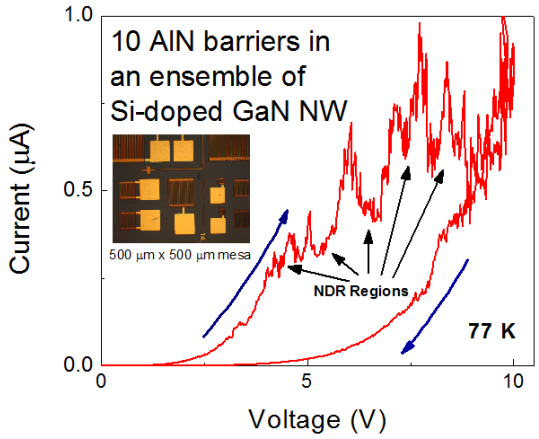


Fig. 7.12.2 – Close up on the positive bias of the I-V characteristics of device 12 (large area, sample C) at 77 K. Many peaks are observed.

In the case of device 13, made from sample C, the highly symmetric I-V characteristics displayed an NDR of 3.14, the highest achieved in this work, at 77 K. After performing two voltage sweeps, the device proceeds to decrease in ratio and lose its NDR property, as seen in figure 7.13.

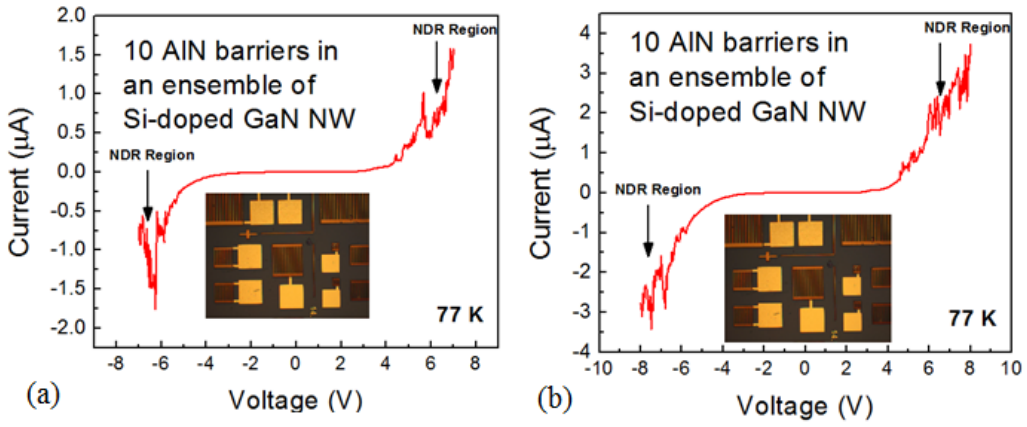


Fig. 7.13 - I-V characteristics of device 13 (large area, sample C) at 77 K. (a) First and (b) second voltage sweeps show significant NDR in both the positive and negative bias.

Chapter 8 – Conclusions and Future Work

The goal of this project was to grow high quality gallium nitride / aluminum nitride multiple quantum well nanowires with varying doping concentrations on silicon substrates and to characterize their electrical properties in terms of negative differential resistance and resonant tunneling. Three samples of GaN/AlN nanowires were grown by radio-frequency plasma assisted molecular beam epitaxy and these were shown to have few defects, although the nanowires were tapered. Generally, two types of nanowires were grown in parallel on a single wafer: long and short nanowires. The density of the nanowires was slightly too high, resulting in some nanowires overtaking its neighbours. The nanowire density can be decreased by increasing the growth temperature; however, temperature affects the quality of the grown structure and would need to be further optimized. Moreover, the use of surface treatments via HCl etching and the mechanical transfer process seemed to improve the NDR properties. Further investigation is needed concerning surface treatments and optimized nanowire transfer method.

Single nanowire and large area nanowire devices have been fabricated using photolithography and electron beam lithography processes. Single nanowire devices showed more consistent results while the large area nanowire devices had a smaller success rate due to the difficulty in contacting uniformly the top of the metal nanowire. More often than not, the I-V characteristics of the large area nanowire devices would show relatively high current, on the order of milliamps, indicating some form of short circuiting. Longer nanowires can be designed to

rectify this issue. By having longer GaN cladding layers, the margin of error can be reduced. However, this may introduce further tapering of the nanowire.

Negative differential resistance was observed both at 77 K and at room temperature for both types of devices, confirming the presence of resonant tunneling through the aluminum nitride barriers. This proves to be an important step in achieving room temperature infrared emission and absorption via intersubband transitions. A peak-to-valley ratio of 2.4 and 3.4 was measured in a single nanowire and large area device respectively. Generally, the PVR across the working devices varied between 1.2 and 2. Moreover, nanowire devices exhibiting NDR typically had a resistance between 100 kΩ and 1 GΩ.

It was discovered that doping the nanowires with Si improved the occurrence of NDR, increased the peak-to-valley ratio, and introduced higher stability in the single nanowire devices. For example, this was the case in sample B when compared with sample A. Further increasing the doping concentration in the quantum wells, as in sample C, did not appear to improve the performance of the device. Overall, the best single nanowire devices with the highest success rate were made from sample B. In terms of stability, most devices showed repeating NDR properties on subsequent voltage sweeps, however, at a varying degree. Some devices would be pushed beyond its limits and breakdown, while others, like device 4, could withstand high bias several times. Due to the potential sudden breakdown, care needed to be taken when increasing the bias voltage during electrical measurements. Overall, it has been shown experimentally that GaN/AlN

have the potential for extremely high stability in electrical behaviour, a property necessary for the development of high quality tunneling diodes.

Finally, temperature dependence tests showed higher conductivity at lower temperatures, due to either a “hard breaking” of the device or the emergence of resonant tunneling. Moreover, NDR is more apparent and more common at low temperatures than at room temperature. Little to no variations in conductivity of the nanowire devices appeared when the temperature was increased from 77 K to 250 K. The few discrepancies to this result in large area nanowire devices where increasing temperature led to a large increase in current and even a reappearance of NDR, is most likely attributed to the movement of the needle probe during thermal expansion. To avoid this in the future, thicker metal contacts may be used or, alternatively, wire bonding can be employed to avoid manual probing altogether.

Potential future works would involve studying the variation of well and barrier widths in the active region and see the effects it has on the transmission coefficient and dwell time. Exploring longer nanowires to ease the fabrication of large area nanowire devices is another possibility. Control tests involving surface treatments should be performed to understand the nanowire surface’s role in current flow. Furthermore, exploring different methods of transferring as-grown vertical nanowires horizontally onto a pre-patterned substrate, without relying on water solutions, may help in obtaining good ohmic contacts. Electroluminescence and photoluminescence measurements would also be performed to investigate the intersubband transition property and to observe infrared photon emission. Finally,

nanowire based intersubband devices such as quantum cascade lasers would be designed, fabricated and tested.

9. References

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Appendix A

Single Nanowire Device Fabrication Procedure:

0. Metal pre-patterned silicon substrates are fabricated by standard photolithography. This pattern is used to locate singe nanowires after dispersion.

1. Vertically standing nanowires are removed from the substrate by vibrational motion via an ultrasonic bath and collected in deionized (DI) water.

2. Nanowires are dispersed onto pre-patterned substrate mechanically.

3. Position of single nanowires is determined by SEM.

4. A polymer EL6 is first coated on the dispersed horizontal nanowires via spin coating at 4000 rpm.

5. Soft baking is performed to solidify the polymer at 150 °C for 90 seconds. The sample is then placed on a metal chilling pad for efficient cooling.

6. PMMA 950 A2 is then spin coated on at 4000 rpm, creating a bilayer co-polymer. Total thickness of the bilayer is approximately 400 nm.

7. Soft baking at 180 °C for 90 seconds, followed by efficient cooling via the metal chilling pad.

8. PMMA is exposed by via a standard electron beam lithography process (EBL) via a Hitachi SU-70 scanning electron microscope.

9. PMMA is developed in a solution of methyl isobutyl ketone: isopropyl alcohol (MIBK:IPA) with a ratio of 1:3 for 1 minute, followed by DI water rinsing for 30 seconds and N2 blow drying.

10. Samples are immersed in HCL for 30 seconds to remove native surface oxides on the nanowires.

11. Metal contacts are deposited onto the ends of the nanowires by physical vapour deposition via a Temescal E-Beam Evaporator BJD 1800. The metals used are Ti (bottom) / Al / Ti / Au (top) with thicknesses (10/50/10/50 nm). The deposition rate is 2 Å/s for Al and Au and 1 Å/s for Ti.

12. Excess PMMA and metal are lifted off in a PG remover for 1 hour.

13. Rapid thermal annealing is performed at 600 °C for 2 minutes.

Large Area Nanowire Device Fabrication Procedure:

1. Clean sample with acetone and DI water.

2. Metal deposition of Ti/Au (10/100 nm) on the backside of the substrate.

3. Rapid Thermal Annealing is performed at 550 °C for 1 minute.

4. Add photoresist (PR) onto back metal contact to protect it from HCl.

5. Submerge sample in HCl for 1 minute to remove native oxide and rinse it in DI water.

6. Spin coat a layer of polyimide – (2723 or 2610) onto the sample at 3000 rpm for 45 seconds, followed by soft baking at 120 °C for 2 minutes (results in a thickness of 8220 Å - 8520 Å).

7. Reactive ion etching (RIE) is performed to etch away the top of the polyimide, until the tip of the nanowire is exposed. The etch rate is ~25 Å/s to 35 Å/s. SEM observation is done to check the height of the polyimide. RIE takes about 80 to 120 seconds.

8. Hard baking (to make the polyimide non etchable) at 250 °C - 300 °C for 30 minutes.

9. Spin coat PR (S1813) at 4000 rpm for 30 seconds. This gives a PR of thickness 1.5-1.6 µm.

10. Expose the sample under UV light via a shadow mask.

11. Develop pattern (using a PR developer MF319) for 1 minute, followed by DI water rinsing.

12. Deposit metals Ti (bottom) / Al / Ti / Au (top) (10/50/10/50 nm) onto samples.

13. Lift off by acetone.

14. RTA at 450 °C for 1 minute.