2-D Free-Space Optical Backplane Using Vertical Cavity Surface-Emitting Laser

A thesis submitted to the Faculty of Graduate Studies in partial fulfillment of the requirement for the degree of Master in Electrical Engineering

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July, 1996

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Abstract

Board-to-board electrical connectivity is a limiting factor for very high bandwidth electronic backplanes. Many physical constraints such as maximum copper trace line density, power consumption of line drivers, transmission line effects and heat dissipation, limit the maximum data throughput achievable for conventional electronic backplanes. On the other hand, photonic backplanes do not have many of the physical limitations that electronic backplanes do. Therefore, by replacing the electronic transceivers in a backplane with optical transmitters and receivers, we can circumvent many of the limitations of conventional electronic backplanes and obtain higher data trafic.

This thesis examines the use of vertical-cavity surface-emitting laser (VCSEL) as transmitters in two-dimensional free-space optical backplanes. The thesis presents design considerations, limitations of present technology and possible improvements in order to make the VCSEL-based free-space backplane system practical and realizable. To show the consept, a working backplane demonstrator (Phase II) was built using VCSEL as transmitter and metal-semiconductor-metal (MSM) as receiver inside a conventional electronic backplane chassis. The design, layout and the performance of assembled Phase II system will be presented throughout the chapters as well as possible future improvements.

Résumé

Le facteur limitant le taux de transfert d'information dans un système électronique est l'interconnection électrique d'une carte à une autre. Certaines limites physiques imposent un plafond au taux de transfert possible dans les fonds de panier ("backplanes") électriques conventionnels: la densité maximale de connections électriques (en cuivre), la consommation des alimentations, les problèmes d'adaption d'impédance dans les connections et la dissipation de chaleur. Il est possible de contourner ces problèmes tout en augmentant le taux de transfert d'information en substituant les émetteurs/récepteurs électroniques d'un fond de panier conventionnel par une technologie d'émetteurs/récepteurs optiques.

Cette thèse examine l'utilisation d'une matrice de lasers à cavité verticale et à émission de surface (VCSEL) comme émetteurs dans un fond de panier optique à l'air libre. Dans le but de réaliser de tels interconnections optiques basées sur la technologie des VCSELs, des considérations de design, les limitations de la technologie existante ainsi que des améliorations possibles seront présentées. Pour fin de démonstration, un fond de panier photonique (la phase II du programme de recherche) utilisant des émetteurs VCSELs et des détecteurs métal-semiconducteur-métal (MSM) a été implémenté dans un châssis conventionnel. Le design, la disposition des éléments, la performance ainsi que des améliorations possibles pouvant être apportées à ce démonstrateur seront présentées dans les chapitres ultérieurs.

Acknowledgements

I am grateful to my supervisor, Dr. David V. Plant, for his help and support throughout the completion my thesis. Without him, I would not be completing my degree at this time. I am specially thankful for Dr. Plant's complete faith in my skill and ability during my stay with the Photonics Systems Group of McGill University. I would also like to thank Prof. H Scott Hinton who invited me to his group and pointed me towards right direction at the beginning of my graduate study. I would like to extend my gratitude to all members of Photonic Systems Group of McGill university for their help and for providing a competent and professional working environment. For last but not for least, I would like to thank my beloved parents for their support throughout my education.

Chapter 1

1.0 Introduction

The complexity of modern electronic printed circuit boards (PCB) are increasing every day due to the ever growing size of microprocessors, digital logic and electronic memories. With the amount of data processing that each board is capable of, communication between boards becomes the limiting factor when building a large system, be it computing, telecommunication or any other multi board systems. As the bandwidth of the modern digital telecommunication system increases, the demand on data processing and routing capabilities of switching systems also increases. With the advances in the high speed serial fiber links, data communications of up to 10Ghz or more on a single fiber are commonplace in today's commercial telecommunication systems. Using wavelength division multiplexing (WDM), the amount of information transmitted through a single fiber link with existing technology can easily reach hundreds of gigabits/sec. The aggregate bandwidth of a fiber link can be further increased with multiple fiber lines like fiber ribbon cables. The maximum available bandwidth of a fiber link can be filled with several channels of voice, data, video and other digital informations using methods such as time-division multiplexing (TDM), code-division multiple access (CDMA), time-division multiple access (TDMA) and packet switching. Once the information has been demulplexed on the receiving end of the fiber, routing or switching of all those channels becomes a formidable task. It is in that data routing or processing stage where the flow of information encounters

bottleneck due to the lir ted board-to-board bandwidth of electronic backplanes in which the system is built. This is also the case for massively parallel supercomputers which require high bandwidth communication between processors and memories located in several printed circuit boards. Electronic backplanes capable of handling teraherz communication systems, massively parallel supercomputers and other complex multi-board data processing system are too costly and complex to build, if not impossible, with existing technology. Beside, the physical limitations of electronic backplanes will soon limit their size and complexity.

Free-space optical backplanes, like the one shown in figure 1.0.1, can have great board-to-board communication bandwidth by virtue of the large space-bandwidth product of photonic devices. As well, they do not have many of the physical limitations that electronic backplanes do. The benefit of free-space optical backplane over an electronic counterpart

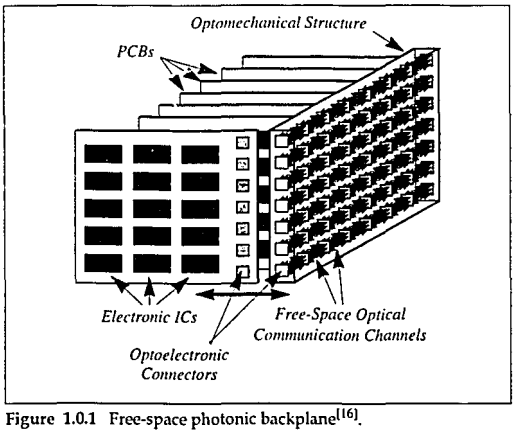

Figure 1.0.1 Free-space photonic backplane[16].

for future computing or communication systems is evident. For example, the network topology of a Cray T3D Supercomputer can be embedded in a optical backplane with physical size of several fold smaller than the current system[1]. Large asynchronous transfer mode (ATM) switching systems with several teraherz aggregate throughput are also possible with free-space optical backplanes[2]. Building an all optical backplane is imprac-

tical, cost ineffective and impossible in a near future. Instead, the approach taken by many, including the Photonic Systems Group (PSG) of McGill University, in the design of free-space optical backplane, is to utilize the inexpensive storage capability and the reliable processing power of current electronics and combine them with the massive connectivity and the high bandwidth of photonic devices. Threfore, the photonic devices will enhance and complement the performance of a backplane by integrating optics and optoelectronics in a conventional electronic backplane. In this way, we can take advantage of the existing infrastructure created by electronic backplanes instead of creating a new one. The advantages of building an optical backplane by integrating free-space photonic devices into the current electronic backplanes, makes it worthwhile to investigate its possibility and potential use for future supercomputing or telecommunication applications. Perhaps, free-space photonic backplanes are the solution for alleviating some of the information bottlenecks of modern or future backplanes.

1.1 Motivation

Modern electronic backplanes provide connections between PCBs trough a linear array of copper trace lines as illustrated in figure 1.1.1. Normally, the physical trace lines are on a PCB board with some passive component for impedance matching and some logics to form a data bus. The limited connectivity and speed of the electrical backplanes are due to several factors:

1 Limited number of I/O

A high connection density electronic backplane like in the *futurebus+* standard has around 51pins/inch. The total data I/O pins of a 10 inch *futurebus+* board is 256, less than 500, due to overheands like power and ground pins. Therefore, even a connection density of 1000 lines for a 10 inch PCB would be a very optimistic figure in a near future.

2 The large power dissipation associated with driving 50-100 Ohm terminated transmission lines.

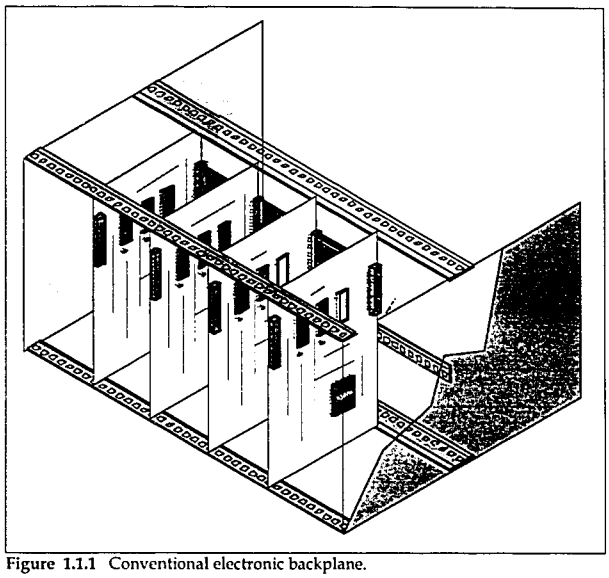

Figure 1.1.1 Conventional electronic backplane.

Emitter coupled logic (ECL) line drivers dissipate about 25mW to 40mW of power[3]. With a 100 Ohm terminated line and a mean ECL voltage level of -1.32, there is a additional power dissipation of 17 mW at the end of the line. Assuming that the average power dissipation per line is 30mW+17mW and with 1000 lines per PCB, each board will dissipate 47Watts just on line drivers!.

3 Large power supplies capable of handling large current surges

If 100 lines terminated to 100 Ohm have to simultaneously swing 1 Volt (0.8 volt for ECL), the power supply should be able to supply 1A of current to each PCB. At a high switching speed, large current surges in the power supply introduces voltage fluctuation causing errors in the data.

4 Capacitive and inductive coupling of signals.

As the density of electrical trace line increases, inductive and capacitive coupling between lines increases, specially with small signal rise time.

5 Signal reflections and skewing.

Signals at data rate of 1 GHz or higher, can only travel 25 cm or less in a metal conductor before being attenuated by -3dB[4] from the DC level. Therefore if the connection length is 25 cm or more and the data rate is 1GHz of

higher, a first or second reflection from a previous data may appear during the next data transfer causing erroneous reading of the data bit. Proper line temination will reduce of eliminate those signal reflections at a cost of incresed power consumption.

6 Limited simultaneous connection.

The connection density along an electronic backplane is the same as the connection density of the boards I/O pins. This means that the backplane can only provide point-to-point connection between 2 boards at any time.

In contrast, 2-D free-space optical backplane can provide high density board-to-board interconnection at a high data rate thanks to the large space-bandwidth product of photonic devices. The advantages of free-space optics and optoelectronics are better exploited for a interconnect distance of few inches, due to diffraction and alignment constraints. For larger interconnection lengths, guided-wave photonic interconnect would be a more suitable solution. Because of this, a lot of the effort is being focused toward employing the free-space optical link for board-to-board or chip to chip communication.

Two dimensional free-space optical links allows the implementation of 3-dimensional interconnect architectures like the 3-D extended generalized shuffle (EGS)[5], Hypercube, and Hyperplane[2]. In a large scale packet switching system, the number of connections that a highly dense 3-D interconnection architectures can provide will minimize blocking probability and hence loss of the data packets. In addition to large connectivity, the performance of an optical backplane can be further enhanced by adding logic to each transmitting and receiving node making it a "smart pixel"[5]. In addition to having multifunctional capabilities, an intelligent optical backplane based on smart pixels should be dynamically reconfigurable. Dynamic, as opposed to static, reconfigurability allows rapid programing of the network in real time so it can perform multiple tasks using minimum hardware. The dynamically reconfigurable inteconnect architecture such as the Hyperplane[6] can take advantage of the smart pixels by choosing the most suitable interconnect

architecture for each application. Figure 1.1.2 shows a smart pixel design for implementing the Hyperplane architecture. An example of operation of this intelligent free-space optical backplane in a packet switching is as follows:

1) The backplane is configured to a desired interconnection architecture depending on the nature of the transmission, i.e. broadcast, point-to-point, etc.
2) The packet header is sent to the backplane to establish the connection path.
3) Once the path is established, the data packets are sent.

A more detailed description of this architecture and its functionality is discussed in [6]. The concept of smart pixel and its current device technology will be discussed in detail in the following section.

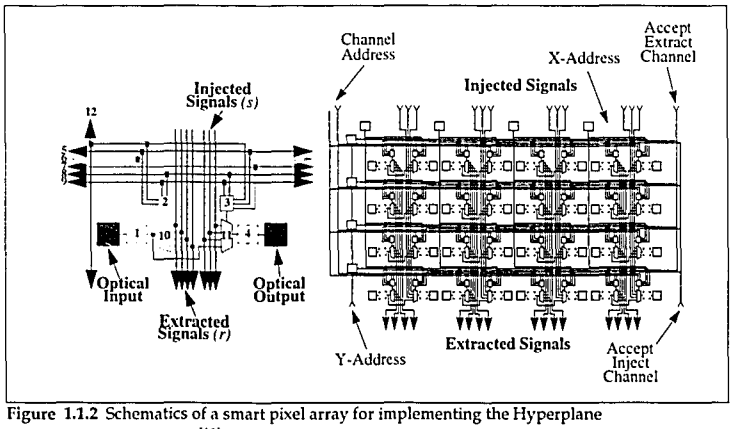

Figure 1.1.2 Schematics of a smart pixel array for implementing the Hyperplane architecture[16]

1.2 Smart pixel technology

As mentioned in the previous section, instead of providing just the interconnect, the performance of an optical backplane can be further enhanced by adding function-

ality to each transmitting and receiving optical node. An optoelectronic integrated circuit (OEIC), can monolithically integrate transistors with optoelectronic transmitters and receivers to form a smart pixel array. With smart pixels, an intelligent optical backplane can be built one that could perform header address recognition in a packet switching applications like ATM and/or dynamic embedding of different network topology[2]. There are two types of smart-pixel technology from a device point of view; modulator-based and emitter-based. Among the modulator-based smart pixel technologies, self-electro-optic effect devices or SEEDs[7] are well developed due to the efforts of AT&T, Hariot Watt and other institutions pursuing this particular technology. Since 1988, AT&T has been producing yearly system demonstrators with SEED technology. The last free-space switching system demonstrator from AT&T using GaAs field-effect transistors (FET) integrated with SEED windows (FET-SEED) was system 5[8]. The latest advance in SEED based OEIC is the so called hybrid CMOS-SEED devices[9]. They integrate GaAs SEED windows with silicon complementary metal oxide semiconductor transistors using solder-bump bonding techniques. The optical I/O densities of a hybrid CMOS-SEED OEIC can reach up to 6400 channels/cm^2[10].

Among the emitter-based devices, vertical-cavity surface-emitting lasers (VCSEL)[11] are one of the most promising recently emerging technologies, providing high density 1-D or 2-D array of laser beams. However, in contrast to SEED devices, VCSELs have not yet been integrated in large scale with transistors and detectors. So far, VCSELs have been integrated with a few GaAs MESFETs and MSMs[12] or with heterojuction phototransistors and photothyristors in a single substrate[13]. Nevertheless, the potential benefit and advantages of VCSELs for free-space or any other system application as descrived in Chapter 3, is so great that much effort is being devoted currently to avancing this technology.

1.3 Concept of Motherboard/daughterboard.

Physical integration of the smart pixels in a free-space photonic backplane can be done in several ways. One, is to integrate the smart pixels in a board with all the other

electronics (motherboards). The advantage of this approach is that the smart pixels can be extracted and inserted with the motherboard. However, the requirement for the alignment is such that positioning of the board after insertion should fall within few microns within the desired position to have the beams aligned to the device windows. One possible solution is the use of active alignment of the beams using Risley steerers[14]. However, the overall system will be very complex if between each board there has to be an active alignment system. Another solution is to have the smart pixels mechanically decoupled from the motherboard by having a separate PCB with smart pixels and its associated electronics (daughterboard). Figure 1.3.1 shows this concept of mother/daughterboards (M/D) without showing the optics and optomechanics. The electrical link between the M/D could

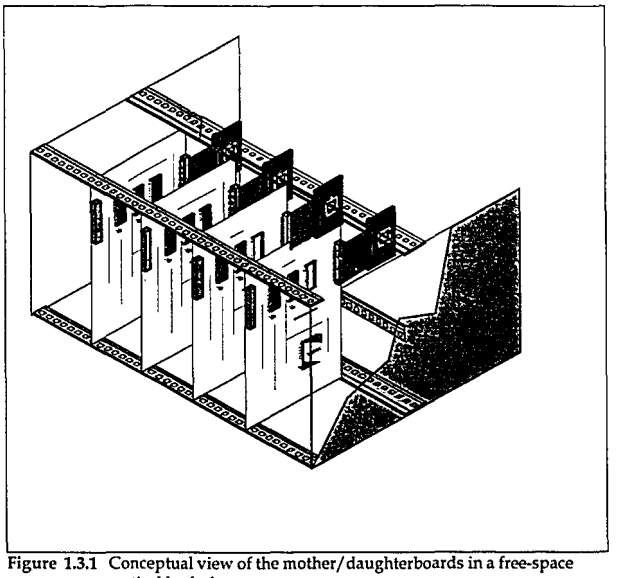

Figure 1.3.1 Conceptual view of the mother/daughterboards in a free-space optical backplane.

done through a high speed impedance controlled electrical ribbon cables or a flexible PCB. Even though the number of electrical channels that can be run between the M/D is limited

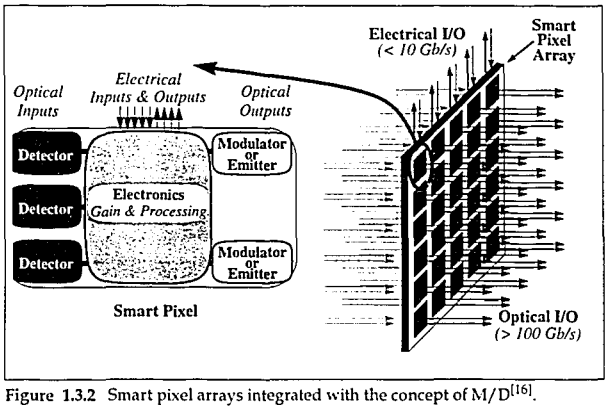

Figure 1.3.2 Smart pixel arrays integrated with the concept of M/D[16].

by the size of the daughter PCB, i.e. limited beachfront, since the distance between M/D is short, signals can be run at a high data rates. Commercially available microstrip ribbon cable assemblies are capable of handling data rates of few Gbit/sec for a cable length of 3 inch or less. With densities of 40 channels per inch, the data throughput between motherdoard and daugtherboard can reach 40 Gbit/sec. With such a large data throughput, the optical links running through the daugtherboards can provide large aggregate bandwidth. At the same time, the motherboards can be inserted and extracted without misaligning the optics. This point is well illustrated in figure 1.3.2.

1.4 Project Overview

The Photonics Systems Group of McGill University, with the support of the Canadian Institute of Telecommunication Research (CITR) and Nortel Technologies, is committed to investigating the feasibility of free-space photonic backplane systems. The long term objective of the group is the implementation of a representative portion of a large scale ATM switching system with a photonic backplane. The group is investigating both the architectural and the hardware aspect of the free-space optical backplane. One of

the main goals of the group is to build yearly demonstrators that shows proof of concept, concentrating both on the modulator based technology and the emitter based technology. Since the forming of the group in Sep. of 1993, the group has produced two working demonstrators. The first demonstrator based on the SEED modulator technology, *PhaseI*, showed a unidirectional and the bidirectional point-to-point link using diffractive micro optics[15] all on a slotted baseplate (see figure 1.4.1). The second demonstrator, *PhaseII* VCSEL-MSM (see figure 1.4.2), also showed unidirectional point-to-point interconnect integrated in a conventional electronic backplane using emitter-based technology. The authors contribution was in the design, implementation and characterization of part of the *PhaseI* and *PhaseII* demonstrator systems. This thesis focuses on the work done in the *PhaseII* VCSEL-MSM system.

1.5 Scope and layout of the thesis

After having introduced in this chapter the concept and motivation behind free-space optical backplane, the subsequent chapters will be organized in following manner. Chapter 2 will discuss the basics of VCSELs and the driver electronics including the current status of VCSEL technology. Chapter 3 gives a detailed description of the PhaseII VCSEL-MSM systems with emphasis to the transmitter part of the system. The details and the results of system characterization of the *PhaseII* system is discussed in chapter 4. Chapter 5 will present system requirements for improved future systems with a concluding remarks.

1.6 References

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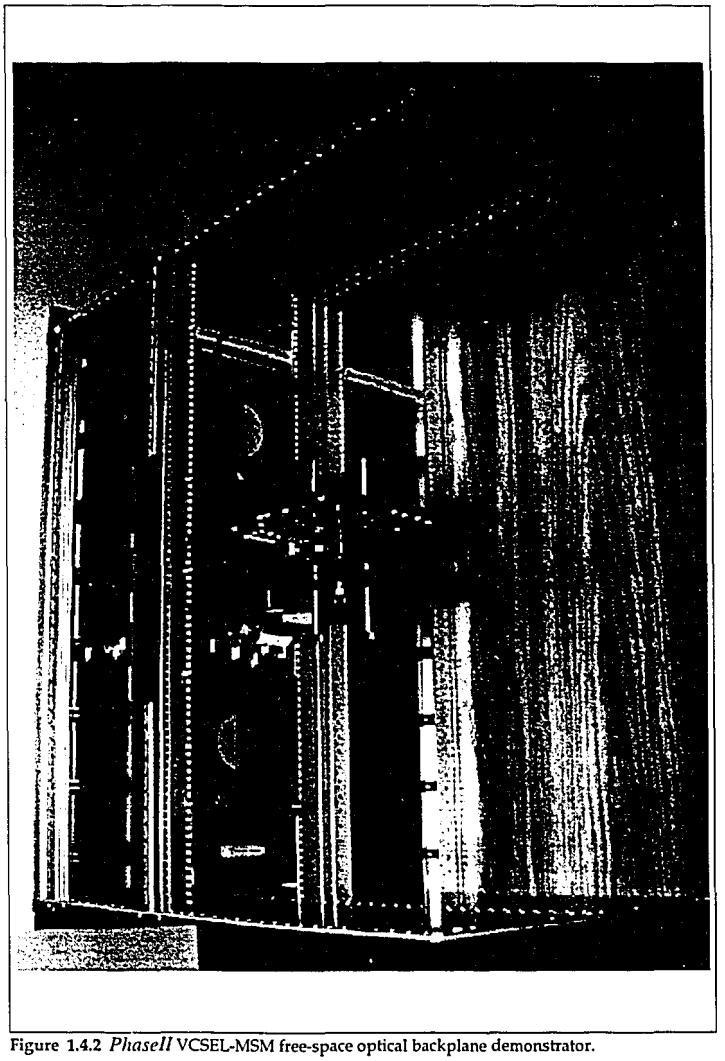

Figure 1.4.2 *PhaseII* VCSEL-MSM free-space optical backplane demonstrator.

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Chapter 2

2.0 Emitter-based optical power supplies

Emitter-based optical power supplies offer the advantage of being able to directly modulate each optical channel in a free-space optical interconnect. Board-to-board free-space optical channels using light emitters as transmitters require simpler optics than interconnects using electro-optic modulators as transmitters because there is no need to bring optical power to transmitters. Some of the advantages of having simple optics are easy alignment and low cost. Electrically pumped light emitters that can be used in a parallel optical interconnect are: light emitting diodes (LEDs), edge-emitting diode laser arrays and vertical cavity surface emitting lasers (VCSELs). For high speed, high density 2-dimensional free-space interconnects, VCSELs are better suited than LEDs and edge-emitting lasers due to their small switching transients, symmetrical output beam profile and high device packing density. Also, LEDs are not power efficient and high speed compared to diode lasers. In this chapter, the theory of operation of a VCSEL, the current device technology and electronic drivers for VCSELs will be presented along with design considerations for using VCSELs in a free-space optical interconnect.

2.1 Vertical-cavity surface-emitting laser

Vertical Cavity Surface-Emitting Lasers (VCSELs) were pioneered by Iga et al.[1]. Starting in the late 70's with an electrically pumped laser operating at 77 ^{o}K emitting at 1.2 μm, they later produced the first room-temperature continuous-wave (CW) VCSELs. Recently, significant advances in device fabrication technologies, specially in epitaxial growth, has lead to improvements in VCSEL performance to the point that they are starting to find their place in commercial products. There are already commercially available VCSELs, as well as prototype of optical links using VCSELs and fiber ribbons[2]. Beside industrial laboratories, many research facilities are also capable of fabricating VCSELs. Due to their potential applications and advantages over other diode lasers, VCSELs have generated tremendous interests from both the industrial and the academic communitiy.

Vertical Cavity Surface Emitting Lasers are fabricated using growth techniques such as molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD), in which thin active layers and mirror layers are grown. Unlike edge-emitters, VCSELs lase perpendicularly to the active layer which have the following advantages:

- One or two dimensional arrays of VCSELs can be fabricated with submicron level uniformity in device spacing. This is useful for multichannel fiber ribbon or free-space interconnects
- The geometry of the gain region can be made perfectly circular.
- The output aperture size and shape can be lithographically controlled.

As an example, the 4x4 array of VCSELs shown in figure 2.1.1 (fabricated by VIXEL corp.) have an output aperture of 5μm and an interdevice spacing of 125μm. So far, 2-dimensional arrays of VCSELs as large as 32 rows by 32 columns have been demonstrated in a 4 mm^2 die[3]. Since the gain region and the output aperture of VCSELs can be made to a symmetrical geometry, the output profiles of VCSELs are also symmetric. The above mentioned and other attributes of VCSELs are key for integrating them with fiber bundles,

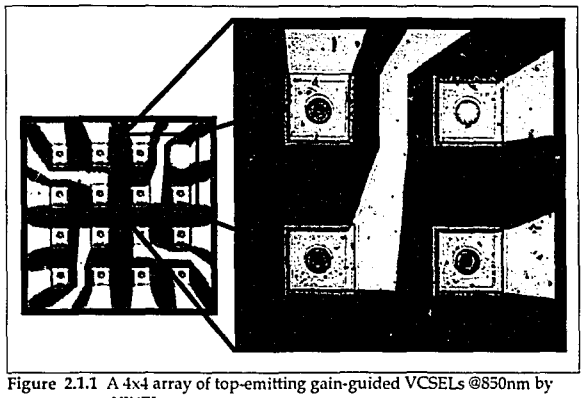

Figure 2.1.1 A 4x4 array of top-emitting gain-guided VCSELs @850nm by VIXEL corp.

microlenses and other micro-optics for multi-channel free-space and guided wave interconnects.

2.2 Cavity structure of VCSELs

A Vertical Cavity Surface Emitting Laser structure is basically a multiple quantum-well active region surrounded by two distributed Bragg reflectors (DBR) with very high reflectivity. In a near infrared (NIR) VCSEL, the DBR structure consists of AlAs/AlGaAs quarter wave multilayers and an active region of GaAs/AlGaAs layers. The two DBR mirrors are doped n and p type respectively and the current is injected to the active region through the metal contact to one of the mirrors. Figure 2.2.1 shows a cavity structure of a top-emitting gain-guided VCSEL like the ones shown in figure 2.1.1. Typical cavity lengths of NIR VCSELs are about 1 μm to 2 μm defined by the effective cavity length between the top and bottom mirror stacks. Details of the device design, fabrication and characteristics are described in detail in [3]. VCSELs can be divided into two classes depending on the optical mode confinement: index-guided and gain-guided. In an index-guided device, the laser cavity is formed by etching the layers around the desired shape of

the cavity. The light is confined by the virtue of the cavity material having refractive indices higher than the surrounding volume (usually air). Gain-guided VCSELs on the other hand, have planar structures in which the light is confined by the injection of the charge carriers. The regions of the semiconductor were there is a current flow have slightly higher refractive index than the surrounding volumes because of the presence of the charge carriers, thus providing the guiding structure. The electrical insulation between the cavity and the surrounding volume is achieved by proton implantation. The index-guided devices have more stable transverse mode than gain-guided ones, however, gain-guided devices are easier to fabricate and have better heat dissipation that index-guided VCSELs.

VCSELs can be further subdivided into top and bottom emitting devices in which the laser emission occurs either through the transparent substrate or through the aperture in the top metal contact. The VCSELs used in the *Phase II* optical backplane were top-emitting gain-guided NIR devices made by VIXEL corp. The operating characteristics and current technologies of VCSELs will be discussed in next section.

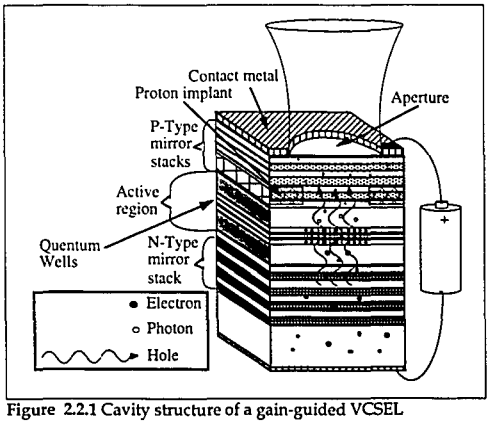

Figure 2.2.1 Cavity structure of a gain-guided VCSEL

2.3 Operating characteristics of current VCSELs

Despite its apparent ideal characteristics as described in the previous chapter, current VCSELs are not yet as efficient and practical as edge-emitting diode lasers. Although wall-plug efficiencies of up to 17.3% in a 30μm diameter InGaAs VCSEL have been reported[4], it is still far from matching the wall-plug efficiencies of edge-emitting diode lasers that are currently near 50%. VCSELs can now achieve output optical powers of 1mW or more which is suitable for many applications, however, the problem is in the removal of the heat generated due to the low power conversion efficiencies and high series resistance, especially for high density 2-D arrays. Having active or passive cooling near the die would bring the average temperature of the die down, but since the distance between the VCSELs is significantly smaller than the substrate thickness, there will still be temperature gradients across the array. For example, typical die thickness of GaAs wafer is 625μm and the common spacing between VCSELs is 125 or 250 μm (for applications using fiber ribbons) or even smaller if larger and denser array is desired. Due to the small size, VCSELs have high thermal resistivity which presents problems for both device fabrication and system applications. In a GaAs laser, as the junction temperature rises, the band gap shrinks and as a result the peak of the gain spectrum shifts toward longer wavelengths (red shifting). This wavelength shift is approximately 4 times faster than the shift of the cavity mode due to change in material index[4]. Since VCSELs have large longitudinal mode spacings (≈50nm), instead of the output mode hopping to match the mode of the cavity like edge-emitters, the threshold current increases due to the mismatch of the cavity mode and the peak of the gain spectra causing the output power to decrease. This is often referred as thermal roll-over and it is a repeatable non-destructive phenomenon that can be observed from an L-I curve of VCSELs as a roll-off of the output power with increasing current. High temperature operation of the VCSELs will also cause thermal crosstalk and shortening the device operating lifetime. A Peltier cooler monolithically integrated with a single VCSEL has been demonstrated [5] but it would be difficult to implement it in a large array, specially considering the low thermal conductivity of GaAs. Also, any type of active

cooling system will increase the average power consumed per channel. To be able to use VCSELs for a high-density 2-D optical interconnect, reliable high wall plug efficiency devices are needed in order to build systems with large connectivities.

Among the characteristics that give VCSELs advantages over edge-emitting diode lasers are their longitudinal mode spacing, linewidth and transverse mode characteristics. The longitudinal mode spacing of a laser is inversely proportional to its cavity length according to the formula $\Delta\lambda=(\lambda^2/2Ln_{eff})$, where n_{eff} is the effective refractive index and L the effective cavity length. For a 1.5 μm-cavity AlAs-GaAs (n_{eff}=3.2) VCSEL lasing at 850nm, the corresponding longitudinal mode spacing is about 75 nm. Since the gain at 75 nm away from the peak gain is not enough to generate stimulated emission, VCSELs can be considered as true single wavelength devices. In terms of linewidth and transverse mode characteristics, the theoretical linewidth of VCSELs are several hundred of megahertz[6] the spatial mode of VCSELs are Gaussian unless designed otherwise. In order to achieve single transverse mode output, the diameter of a VCSEL is made small enough to allow stable operation in the TEM_{00} mode up to a desired maximum operating power. The trade-off of having a small cavity and output aperture in a VCSEL is that the diffraction angle of the output beam is large. As an example, 5μm diameter aperture VCSELs have output beam divergence of 13°. A large beam divergence requires a small f# lens to collimate the output beam setting tighter tolerances to the optics and optomechanics of the system. The two *Phase II* systems were practically insensitive to wavelength variations since they only used refractive bulk optics and metal-semiconductor-metal (MSM) detectors that have broad responsivity. On the other hand, if any diffractive optics and (or) narrow spectral responsivity detectors were to be used in a system, VCSELs with good wavelength characteristics are needed.

The output of the VCSEL is linearly polarized, however, the direction of polarization varies randomly from laser to laser in an array. There is some evidence that the crystal structure of the gain media produces small anisotropy that tends to orient the direction of polarization to the crystal axis. Still, the anisotropy is so weak that with small change in injected current or temperature the direction of polarization is easily changed. Therefore,

polarization dependent optics cannot be used with current VCSELs. The output polarization of the VCSELs could be controlled by introducing bifringent axis with mechanical stress in the cavity or by asymmetric gain medium geometry.

The threshold current of a VCSEL is significantly higher than an edge-emitting laser mainly because of the high electrical resistivity of the mirrors. Although threshold currents lower than a milliamp was reported in a 8μm diameter VCSELs[7], it is difficult to obtain uniform threshold current across an array of VCSELs in parallel operation due to temperature gradient across the array and current leakage between adjacent devices. Non-uniform threshold currents will cause phase delays between signals. The modulation bandwidth of VCSELs is limited by its dynamic impedance and the parasitics. There are several modulation schemes that can be used to drive the VCSEL which will be discussed in next section.

2.4 VCSEL modulation schemes

High modulation efficiencies of VCSELs have already been demonstrated showing modulation bandwidths of more than 5Ghz[8]-[9]. Therefore the speed of operation of a VCSEL array is dictated by the speed of its packaging and the driving circuitry. Ideally, when modulating VCSELs the current level corresponding to the "logic low" should be exactly at threshold current ($I_{threshold}$). Biasing the laser at larger current than $I_{threshold}$ will decrease the contrast ratio and increase the quiescent power dissipation but minimize the phase delay. On the other hand, biasing at a lower current than threshold will lower the quiescent power dissipation and increase the contrast ratio but it will cause asymmetry between the logic high and logic low cycle of the output as illustrated in figure 2.4.1

The simplest way to drive a diode laser is using the bias tees and supplying the bias current through the DC port and connecting the AC port to the output of a pulse or data generator. To limit the current flowing to the laser, a series resistor is connected between the VCSEL and the AC port of bias-tee to provide the right amount of current swing at a given voltage

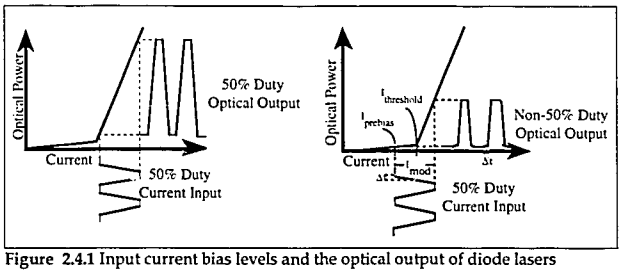

Figure 2.4.1 Input current bias levels and the optical output of diode lasers

swing of the data generator. Care must be taken since the output of the pulse or function generator cannot be current limited to protect the VCSELs from current surges. Another way of driving the VCSELs is to construct simple current steering circuits using either complementary metal oxide semiconductor (CMOS) or integrated bipolar junction transistors (BJTs). For higher speeds, GaAs integrated circuits could be used. An example of CMOS driver circuit is shown in figure 2.4.2.

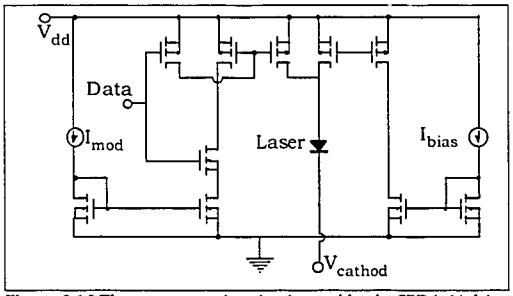

Figure 2.4.2 The current sterring circuits used by the SPDA-16 driver from VIXEL corp.

Most commercially available diode laser drivers are not suitable for driving VCSEL arrays since they are designed to drive single diode laser. Also, they do have meet the high voltage compliance required for current VCSELs. As a result, the first part of the *Phase II* demonstrator used the SPDA-16 driver by VIXEL which is an application-specific integrated circuit (ASIC). This offered the convenience of modulating all 16 VCSELs from a single driver chip. The DC bias levels for all 16 outputs of the SPDA-16 is set by supply-

ing current to a single reference input port. The drawback of SPDA-16 was the lack of good output current uniformity (due to a single stage current mirror) and limited modulation bandwidth (25 Mbit/Sec). In the second part of the same system, bias-tees were used to explore the inherent high bandwidth capability of the packaged and cooled VCSELs. The results of those two driving schemes will be described in detail in chapter 4.

2.5 Conclusion

For PCB to PCB optical interconnect using VCSELs to be competitive with current electronic interconnects, several important improvements will have to be made to the performance of VCSELs. For example, in order for the VCSEL-base l optical transmitter to compete with current ECL line drivers, the average power consumed by a single VCSEL interconnect and its driver should be less than 34mW[10] (average dissipation of ECL line drivers terminated to 100 ohms at -2 Volts). Because of that, VCSELs will have to have low threshold currents and designed for high temperature operation without the requirement of active cooling. As a comparison, the VCSELs used for Phase II system have quiescent power dissipation of around 20 mW. Also, to have a comparable or smaller propagation delay time than an electrical interconnect that consists of line driver and receiver with a copper transmission line in between, propagation delays between the VCSEL and the VCSEL driver will have to be shorten. For this, monolithic integration of VCSELs and its driver in a same die, or packaging VCSELs and driver chip in a multi chip module will eventually have to replace external VCSEL drivers in order to take advantage of the high modulation capability of VCSELs. To get a high channel density in a free-space optical interconnect, integration of VCSELs with micro-optics is essential since bulk optics with large field of view required for large VCSEL arrays are complex, expensive and bulky. Either direct growth of diffractive of refractive microlenses on top of the VCSELs or some novel packaging scheme that integrates micro-optics with VCSEL die will be required in order to achieve large connectivity.

There have been studies that show the feasibility of getting channel densities of more than $3000/cm^2$ using 5μ VCSELs, 5 to 45μ detectors and 85μ microlenses in an interconnection length of 2cm[11]. Moreover, device half life time of almost 10^5 hours has recently been measured when operated at 50°C[12]. These and other recent improvements on VCSELs performance are existing proof that their use in a real systems may be near.

2.6 References

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Chapter 3

3.0 VCSEL-MSM system overview

An optical backplane demonstrator (*Phase II*) was built to show the feasibility of 2-D free-space board-to-board interconnect. The system provides simple 1-to-1 unidirectional interconnection between two boards, having no data processing power embedded in the VCSEL or MSM die nor in the boards. Instead, the main objectives of the demonstrator were:

- to integrate an optical backplane in a conventional electronic backplane chassis.
- to investigate the performance of VCSEL and MSM as transmitting and receiving devices in a free-space optical backplane.
- to determine the alignment stability of barrel and PCB optomechanics.
- implement the concept of Motherboard/Daugtherboard.

The system was incorporated into a conventional electronic (VME size 6U) backplane chassis in a such a way that both the motherboard and the daughterboard are contained inside the chassis. The motherboard fits directly into the chassis and the daughterboard assembly, i.e. transmitter and receiver boards with optics and optomechanics, is attached to the chassis by adapter optomechanics. All the relay optics are housed inside a barrel which in turn holds the 2 daughterboards through an optomechanical plate attached to each boards. Inside the barrel, bulk optics are used to collimate and then focus the 4x4 array of

VCSEL outputs to 4x4 array of metal-semiconductor-metal (MSM) detectors. Figure 3.0.1 shows the entire *PhaseII* VCSEL/MSM system.

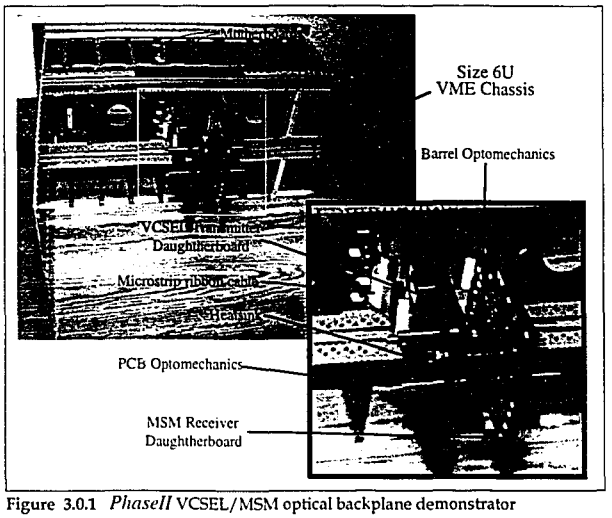


Figure 3.0.1 *PhaseII* VCSEL/MSM optical backplane demonstrator

The first VCSEL transmitter and MSM receiver boards for the *PhaseII* system were built using speed-wire boards, in order to simplify the board assembly and reduce assembly time. However by using a speed-wire board, the system had reduced speed, increased noise and large electrical crosstalk. Despite its shortcomings, the speed-wired boards allowed the testing of the optical design , the optomechanics and their alignment stability. After having built and tested the system with speed-wire boards, the motherboard and daughterboard were replaced with custom designed printed circuit boards. The main objective there was to take advantage of the inherent high bandwidth of the VCSEL and MSM and push the operational speed of the system at a higher data rate. The design of the custom PCB transmitter and receiver was a two step process. First, a test board was fabricated in which only a few channels were operational. It had additional features to test different driver configurations, cooling and packaging. Part of the testing included the bandwidth of the board and of the chip carrier. Once the prototype board was tested and

the design of the board finalized, the final and fully functional board was fabricated and integrated to the system using previously designed optics and optomechanics.

The VCSEL chip was fabricated by VIXEL Inc. and the MSM detectors fabricated by McMaster University. The design of the receiver board was done in the same way as the transmitter board having additional electronics to convert the photocurrent generated by the detectors into a several hundred mV voltage swings. In the following sections, more detailed descriptions of the system components such as the board, packaging, cooling, optics and optomechanics will be given.

3.1 Transmitter board fuctions

As mentioned in the previous section, the first VCSEL transmitter board was based on speed-wire boards. Figure 3.1.1 shows the front and the back view of the VCSEL transmitter board. Despite the obvious drawback of this board, such as limited bandwidth

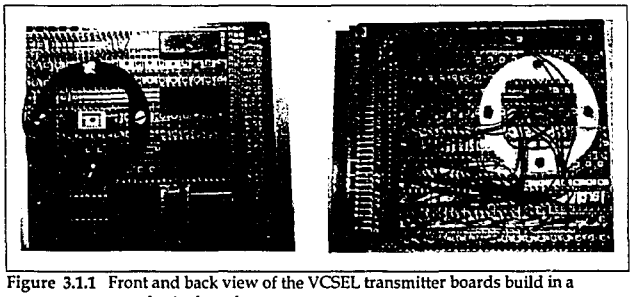


Figure 3.1.1 Front and back view of the VCSEL transmitter boards build in a speed-wire board.

and the large electrical crosstalk, its easy reconfigurability and fast assembly time made it an attractive alternative to custom printed circuit boards. The VCSEL driver used for this board was a 16 channel common-cathode VCSEL array driver from VIXEL corp. (SPDA-16). The SPDA-16 is a silicon CMOS application specific integrated circuit capable of

driving 16 VCSELs in parallel to a speed of up to 25Mbit/sec. The input signal was fed from a HP80000 data generator to the motherboard through a 50 Ohm shielded cable assembly made by AMP, terminated to 25 SMA connectors in one side and to a single dual- in-line connector on the other side. The motherboard had female receptacle for the AMP dual-in-line connector on one side. The motherboard and the daughterboard are electrically linked by a 60 channel dual-in-line connector with standard computer ribbon cable. Figure 3.1.2 shows the picture of the entire mother/daughter assembly with the AMP cable assembly.

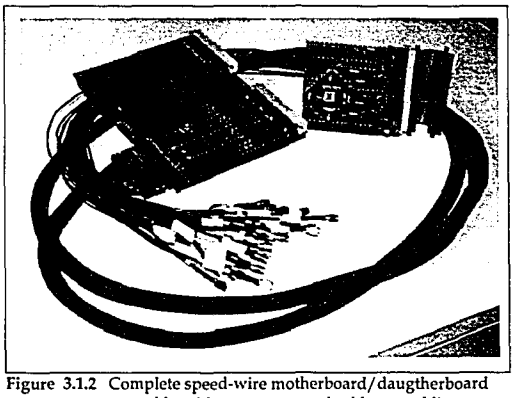


Figure 3.1.2 Complete speed-wire motherboard/daugtherboard assembly with connectors and cable assemblie.

All transmitter electronics were located in the daughterboard, making the motherboard entirely passive. The circuit diagram for the speed-wire based VCSEL transmitter board is shown in figure 3.1.3. The 100325 ECL to TTL voltage converters shown in figure 3.1.3 converts the data generator's ECL output voltage level to appropriate CMOS voltage levels of the input of SPDA-16. The bias current level of all 16 output of the SPDA-16 is set by programing the I_{bias} input port with appropriate current, which then gets mirrored to all 16 output ports. The modulation current level, i.e. the output current level corresponding to logic input high, is also set by providing current to I_{mod} port. The I_{bias} and I_{mod} currents are set using a constant current source (LM334Z) and can be adjusted using a potentiometer. Finally, the output of the SPDA-16 is connected to a 4x4 array of VCSELs packaged in

a 18 pin dual-in-line (DIP) chip carrier using ball-bonding. There were several drawback with this system which are:

- the driver had poor output current uniformity (>5%).
- the VCSEL had dynamic impedance of bigger that 450 Ohms which limited the modulation bandwidth of the driver.
- the VCSEL chip carrier did not provide adequate heat dissipation for the VCSELs which lowered the output power of the VCSEL when in parallel operation.

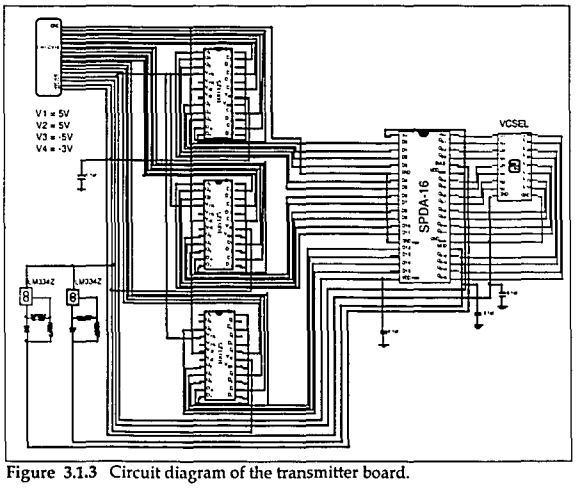


Figure 3.1.3 Circuit diagram of the transmitter board.

Due to obvious shortcomings in the previously mentioned board, the system was upgraded with new transmitter and receiver boards using different die packaging, custom PCB, high-speed ribbon cables and active cooling system. The PCB opted for the upgrade was a 4 layer board with impedance controlled microstrip lines. The 2 middle layers are ground and V_{CC} planes and the 2 outer layers are signal planes. The signal trace lines width are 8 mil (200 μm) and the dielectric thickness between a ground and a signal plane are 6 mil (150 μm) in order to achieve characteristic impedance of 50 Ohm. Figure 3.1.4 shows the picture of the upgraded transmitter daughterboard.

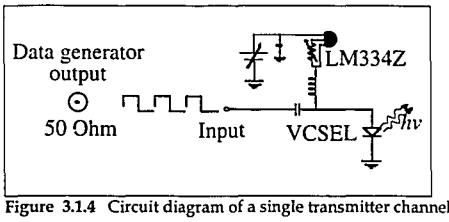


Figure 3.1.4 Circuit diagram of a single transmitter channel

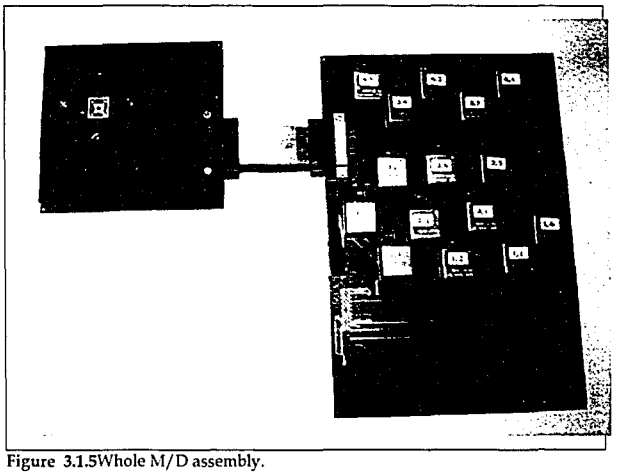


Figure 3.1.5Whole M/D assembly.

Due to the lack of appropriate high speed VCSEL drivers available, and to avoid design of custom IC, bias-tee was used instead to modulate the VCSELs with constant current source (LM334Z) providing the DC current level. The schematic diagram of a single transmitter channel is drawn in figure 3.1.4. One of the advantages of using bias-tees, beside its speed, is the ability to control the bias current of each channel independently which help minimize the phase delays between VCSEL outputs. The bias-tees are PCB mountable and are packaged in a metal can. Since these bias-tees are relatively large and heavy, 15 of them were mounted in the motherboard and 1 in the daughterboard in order to reduce stress to the optomechanics. To preserve the high speed connection from the output of the bias-tee on the motherboard to the VCSELs on the daugtherboard, a 40-channel imped-

ance-matched (50 Ohms) microstrip ribbon cable assembly from AMP (3 Ghz 3dB bandwidth) was used to connect the motherboard to the daughterboard. The motherboard was interfaced to the test and measuring equipments through a similar AMP connector (80 channel) having one end terminated to a SMA connector. The complete assembly is shown in figure 3.1.5 and figure 3.1.6 shows the S_{21} parameter measurement of the entire assembly including the AMP connector, PGA package and PGA socket. The measurement shows the board assembly 3dB bandwidth of around 300Mhz

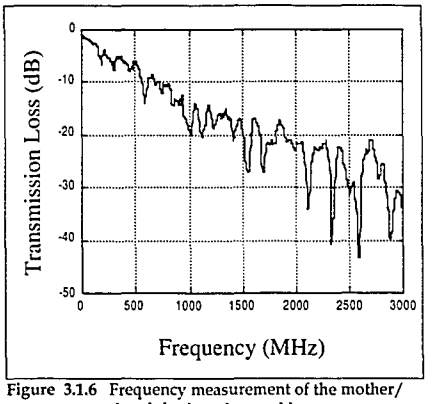


Figure 3.1.6 Frequency measurement of the mother/ daughtherboard assembly.

3.2 Packaging and cooling

The VCSEL used in the speed-wired transmitter board was packed by VIXEL corp. in a 18 pin DIP carrier using ball bonding. Figure 3.2.1 shows the packaged VCSEL including the board optomechanics. As previously mentioned, the there were no active cooling or heatsink used with this package. As a result, it limited the number of channels that could be operated in parallel. The 4x4 array of VCSEL used in the upgraded system was delivered in a bare die form. This allowed in house packaging of the die which gave the choice of choosing among different packaging schemes. To take advantage of the

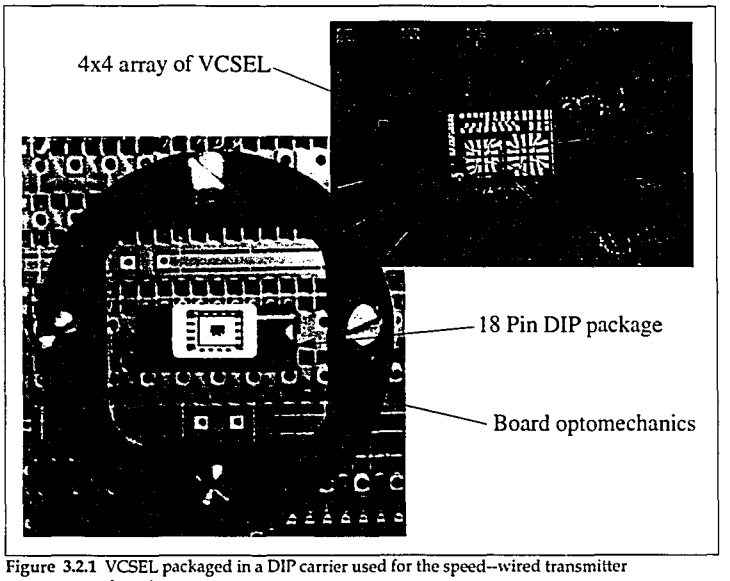


Figure 3.2.1 VCSEL packaged in a DIP carrier used for the speed--wired transmitter board.

board speed, the VCSEL die was packaged in a 64 pin pin-grid-array (PGA) chip carrier which offers higher bandwidth than the previous 18 pin DIP package. The die was wedge-bonded to the package with 1 mil (25 μm) gold wire using K&S wire-bonder. The PGA was then mounted to the PCB through a socket so that the VCSELs can be replaced without having to desolder from the board.

The PGA package is a good heat conductor however, to better remove the large amount of heat generated by VCSELs and to control the package temperature, a Peltier (or thermo-electric (TE)) cooler was mounted in the back of the PGA. In addition, a thermistor was installed in the front side of the package to monitor the temperature. A square hole incorporated in the design of the PCB allows for a heatsink to be mounted on the hot side of the TE cooler (see figure 3.2.2). During the operation of the system, a standard computer fan was installed in the chassis to help remove the heat from the TE cooler's heat sink. The

cooling system was able to keep the VCSEL at room tempature or lower when operating at maximum output power.

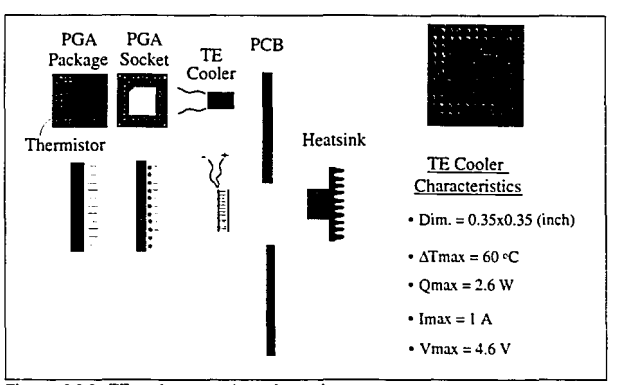


Figure 3.2.2 TE cooler mounting schematics.

3.3 Optics and Optomechanics

The optical system layout used in the PhaseII system is shown in figure 3.3.1. The 2 aspheric lenses (f#=1.67) were used to collimate the laser beam and to focus on the MSM detectors. The 50/50 beam splitter is used for imaging and illumination and the Risley beam steerers are used to translate the beam arrays to give additional alignment capability. All the optics used were bulk instead of being microlenses for several reasons. One of them is the large divergence angle of the VCSELs (FWHM 13o) requires f# of <3 to collect all of energy. Due to the lack of availability of low f# refractive microlenses or diffractive lenses with high troughput at low f#, bulk optics were chosen instead.

The optics are housed inside a barrel, which is shown in figure 3.3.2, and the PCBs are mechanically coupled to the barrel by a plate attached to the PCBs. The whole barrel and PCB optomechanics are then able to give 3 axis translation plus tilt of the boards through the use of set screws. The system opto-mechanics, when assembled, maintained the system

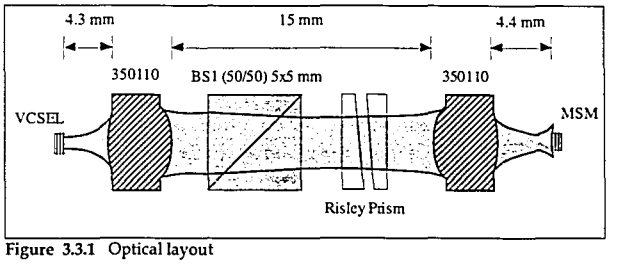


Figure 3.3.1 Optical layout

aligned for weeks at a time showing good stability, low drift and little sensitivity to vibrations.

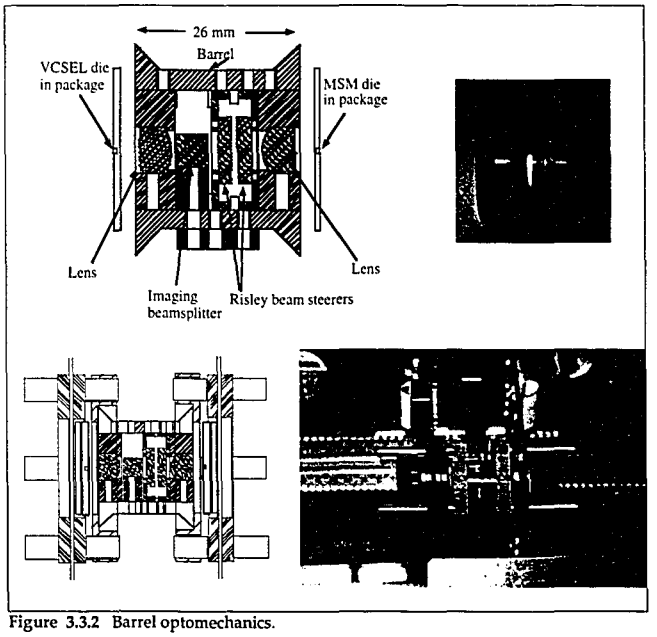


Figure 3.3.2 Barrel optomechanics.

The choice of components in Phase II system described in this chapter,i.e. the optics, optomechanics, optoelectronics and electronics, was dominated by the availability, cost, deliv-

ery time and complexity in fabrication. The optics used in the system was inexpensive (less than $500) off-the- shelve commercial components. By using standard optics instead of custom optics, the compinet and developmentcosts cost are lowered. Also for the opto-mechanics, custom piece design was kept at its minimum and commercial optomechanics or modification of them were used wherever possible. With the system assembled with all the components previously described, its operation was characterized. In next chapter, details of this measurement will be given

Chapter 4

4.0 Performance of the VCSEL transmitter board

As mentioned in previous chapter, the Phase II system was built in 2 step; first with speed-wired boards and then with custom impedance matched boards. In this chapter, the result on the performance of the *Phase II* transmitter board and the entire assembled system will be presented. Several system behavior like modulation bandwidth, wavelength drift, VCSEL threshold current and others were characterized. Those aforementioned characteristics are important in identifying the physical limitations, limitations of current technology and improvements needed for next generation of emitter- based free space optical backplanes.

4.1 Modulation characteristics

The first performance characteristics of the Phase II free-space optical backplane demonstrator measured was the output waveform of the VCSEL transmitter boards. The output waveform of both the speed-wired and the impedance matched VCSEL boards were measured as well the output from the receiver boards.

4.1.1 Speed-wired board

The optical output of the speed wired VCSEL transmitter was measured using the Hewlett Packard HP8000 data generator (200 ps risetime) as input and the Antel ARX-SA (< 210 ps risetime) avalanche photo diode (APD) as detector. The output of the APD was then displayed on a HP 54120B dizitizing oscilloscope using HP 54124A DC to 50 GHz sampling unit. The schematic diagram and the picture of the measurement setup is shown in figure 4.1.2. The measurement of speed-wired transmitter includes the whole mother/daughter assembly with the AMP connector as shown in figure 3.1.2. The naming convention adopted for the 4x4 VCSEL array is the mathematical convention used for a 4x4 matrix, i.e. (1,1), (1,2)....(4,4). The result shown in figure 4.1.3 was obtained by modulating all 16 channels one channel at a time, keeping all other channels biased at threshold current ($I_{threshold}$). The amplitude of the waveform shown in figure 4.1.3 is negative, since the APD output is inverted. The input waveform chosen for all 16 channels was a 50% duty cycle square wave at a frequency of 100KHz with peak output optical power from the VCSELs of 600 μW and a coupling efficiency onto the Antel detector of around 80%. The VCSEL chip was cooled by natural convection (i.e. no forced air flow) at a room temperature with no active cooling. In most channels, the amplitude rolled off quickly after 100KHz with some channels having faster roll-off than others. This is due to the signal degradation in the speed-wired board. The discrepancies in bandwidth between difference channels, shown in figure 4.1.3, is due to the fact that each channels had different wire length and therefore different impedances and capacitances. The SPDA-16 laser diode driver was designed to drive impedance load of around 50 Ohm and since the impedance of the VCSELs near 1mW was 450 Ohms, is RC limited the bandwidth of the system. To show the contrast between the outputs of the SPDA-16 driver with low and high load impedances, 15 outputs of the SPDA-16 were terminated with 50 Ohm resistor network and one to a 50 Ohm input of the digitizing scope. The channel connected to a oscilloscope was modulated with a 50% duty squarewave. With 50 Omh output load impedance the output of the driver, shown in figure 4.1.4, had better square wave output even at a data rate of 7 Mbit/sec. This is closer in accordance with the specified speed of

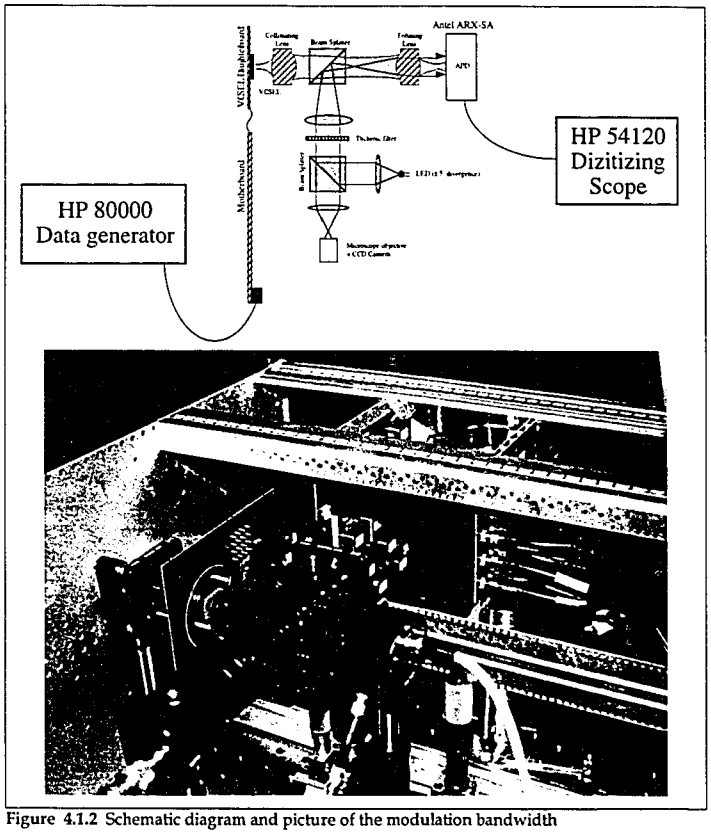


Figure 4.1.2 Schematic diagram and picture of the modulation bandwidth measurement setup.

25Mbit/sec of the SPDA-16 driver. There was still a diffrence betweeen the specified and the measured speed of the driver. This is possibly due to the connection scheme between the 50 ohm SMA cable and the VCSEL package.

The optical output of the speed-wired VCSEL transmitter operated in parallel was measured, with the channels (1,1), (2,4), (4,1) and (4,4) being modulated simultaneously. The dual-in-line (DIP) package of the VCSEL didn't provide adequate heat dissipation to be

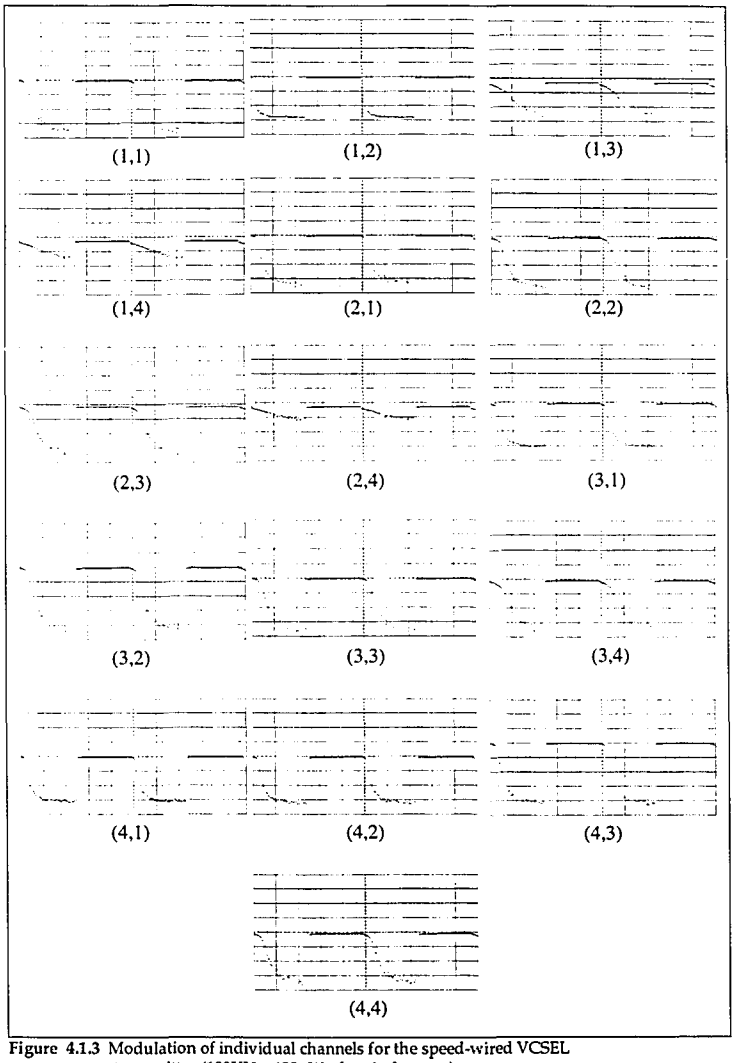


Figure 4.1.3 Modulation of individual channels for the speed-wired VCSEL transmitter (100KHz, 480uW of optical power).

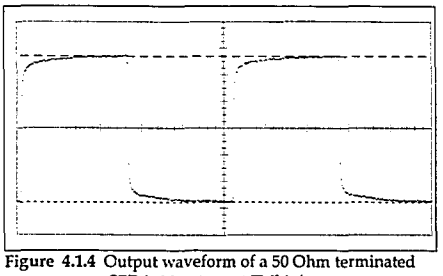


Figure 4.1.4 Output waveform of a 50 Ohm terminated SPDA-16 output.at 7Mbit/sec.

able to operate more than 4 channels at a time. The addition of more channels in pararell operation increased the temperature of the VCSEL chip to a degree that decreased the output optical power by large amount. The increased the risk of damaging and accelerated aging of the devices prevented the transmitter from running more than few channels simultaneously. The 4 channels mentioned previously were chosen because of their relatively higher bandwidth exhibited during the individual operation and large distances between them. The distance between devices is important in order to get good heat dissipation and

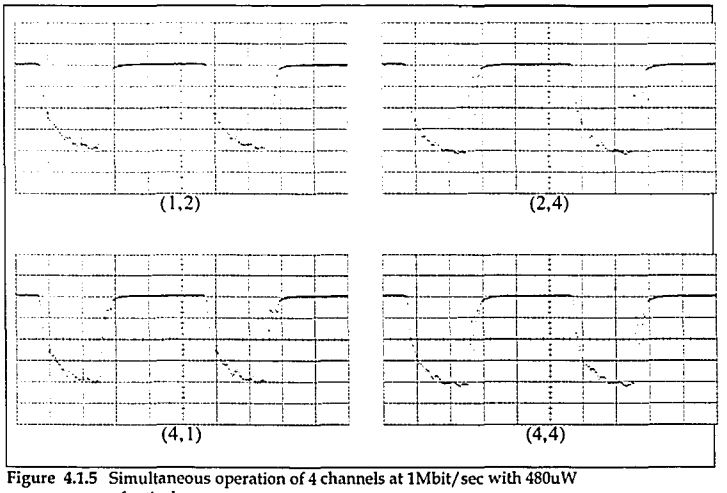


Figure 4.1.5 Simultaneous operation of 4 channels at 1Mbit/sec with 480uW ofoptical power.

minimize thermal crosstalk. Figure 4.1.5 shows the output of the APD operating 4 VCSELs simultaneously at 1Mbit/sec.

After assembling the entire *Phase II* system with speed-wire boards, the parallel operation of the entire assembled system including the MSM receiver board was tested. The diagram of the test layout is shown in figure 4.1.6. Included in the Figure 4.1.6 is the circuit diagram for a single amplified MSM receiver channel. The receiver channel has a NE5212 Phillips transimpedance amplifier that converts and amplifies the photocurrent generated by the MSM into a voltage output of 450 mV amplitude. The NE5217D post amplifier then takes the differential output of the NE5212 and provides with additional voltage amplification and with voltage clamping (or hysteresis) to "clean" the output digital signal. The receiver board had 4 MSM outputs amplified as previously described and they corresponded to VCSEL (1,1), (2,4), (4,1) and (4,4). The 12 non amplified channels couldn't generate enough photocurrent to produce voltage swings larger than 5mV through a 50 Ohm input of the oscilloscope. It had very poor signal-to-noise ratio due to the RF noise picked up by the long wires. Despite its performance, the speed-wired transmitter and receiver board played a key role in identifying immediate improvements that could be implemented to the system. As well, it allowed the testing of optics and optomechanics which showed good mechanical stability and allowed the operation of the system without realignment for extended periods.

4.1.2 Impedance controlled PCB

As mentioned in Chapter 3, to increase the bandwidth of the system, the speed-wired transmitter and receiver board were replaced with custom impedance-controlled PCBs. Prior to building a fully functional boards, prototype PCBs were built first to test the bandwidth of the VCSEL, the packaging and the board itself. A bandwidth measurement of the prototype transmitter board was done in a way similar to mentioned in the previous section. The main purpose of this measurement was to find out the limitation of the VCSEL's new PGA chip carrier, wire bonding, PGA socket and the board trace line. The

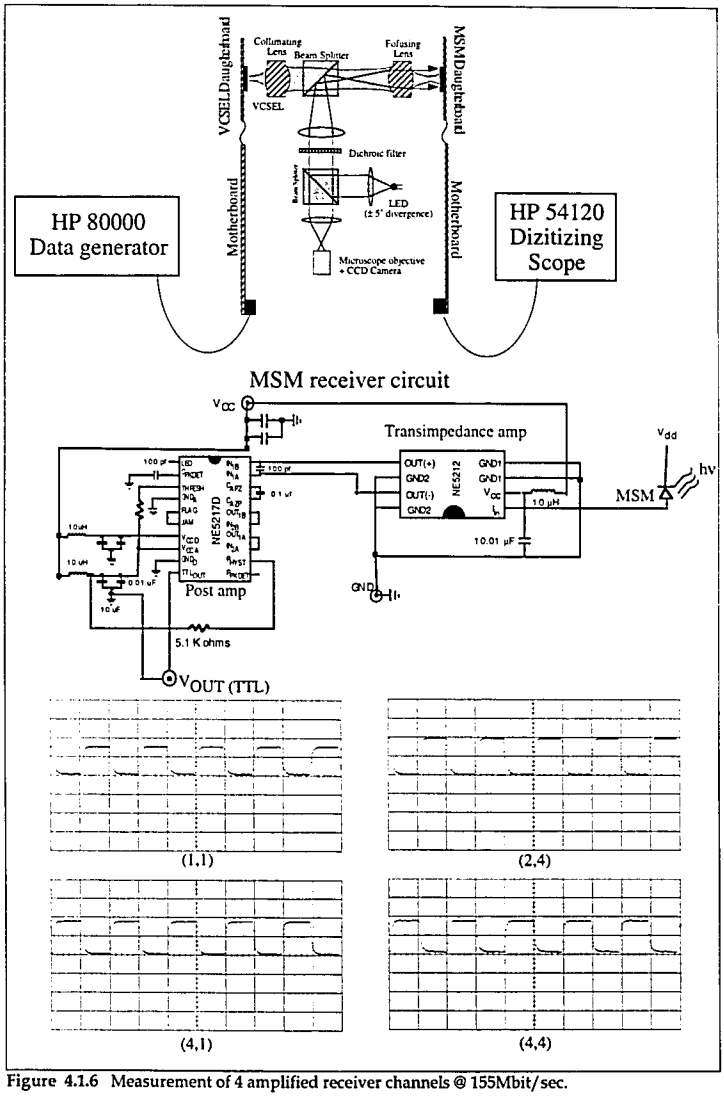


Figure 4.1.6 Measurement of 4 amplified receiver channels @ 155Mbit/sec.

test setup is similar to that of figure 4.1.2 however, the modulation scheme of VCSEL was different. An external bias-tee was used to provide DC current bias and AC signal source. The VCSEL was voltage driven by directly connecting the input of the VCSEL, a board mounted SMA receptacle near the PGA socket (see figure 4.1.3), to the output of the HP8000 data generator. Only 2 VCSEL had external connection through the SMA receptacle and no electrical input were given to other channels including DC bias. The output

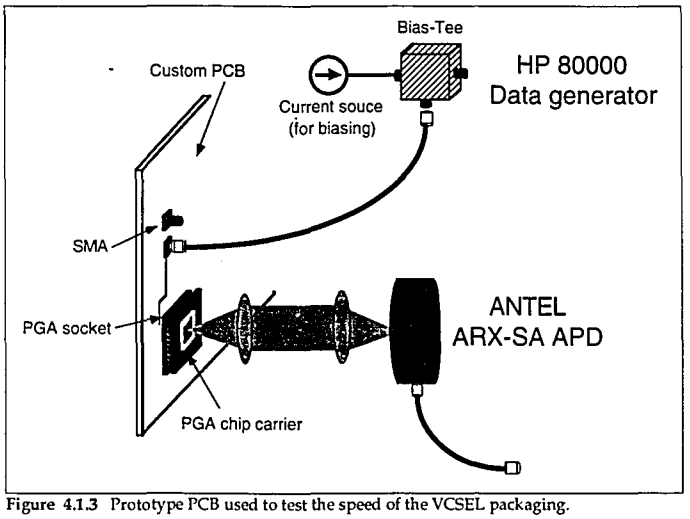


Figure 4.1.3 Prototype PCB used to test the speed of the VCSEL packaging.

waveform, shown in figure 4.1.4, has risetime of 400ps and reasonably square signal up to a data rate of 600Mbit/sec. Even at a data rate of 1Gbit/sec., the amplitude of the fundamental component of the squarewave showed no attenuation. The 400ps risetime falls within the specified value of these VCSELs which are 100ps nominal and 500 ps maximum. The RF noise pick-up was also dramatically reduced compared to the speed-wired board. However, there was a phase delay between the input and the output due to several factors. One, the SMA cable length between the signal generator and the SMA receptacle on the board and the DC blocking capacitor in the bias-tee which introduces 90^{o} phase

shift. The S_{21} parameter measurement of the same setup (see figure 3.2.1), without the bias-tee and with direct wirebonding of chip cavity bondshelf, shows the 3dB frequency of the fundamental to be about 1GHz. If 3 times the fundamental frequency is needed to have a reasonably square signal, this correspond to squarewave frequency of about 300 MHz or 600Mbit/sec. This shows that the limit of the system data rate will be 600Mbit/sec and is dictated by the speed of the PGA chip carrier, PGA socket and bond wire length which introduces about 1nF of inductance per mm (1μm thick gold wire). Unfortunately, the cavity size of the PGA in this case is significantly bigger than the VCSEL die forcing wirebond length of 3mm between the bondpad of the die to the bond shelf of the cavity. This was due the difficulty in obtaining smaller cavity size PGA (in small quantities). It is worth mentioning that the result of figure 4.1.4 was obtained with a VCSEL having 450 Ohm of operating point impedance. If a VCSEL with dynamic impedance of 80 Ohm or less, which is available, was to be used in conjunction with higher bandwidth chip carriers like ball grid array or quad flat packs, improved performance is to be expected. To get even

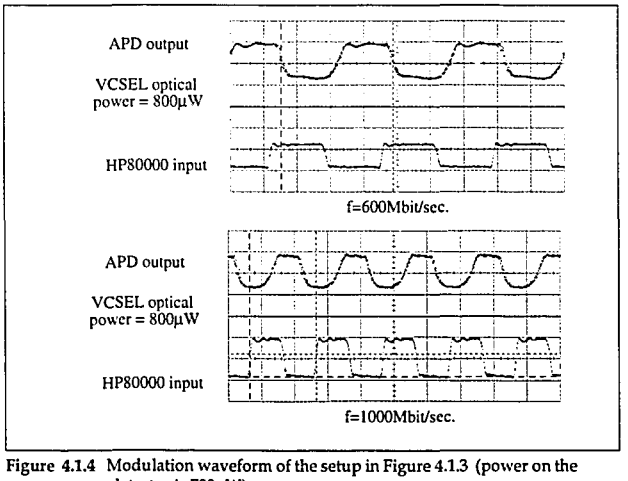


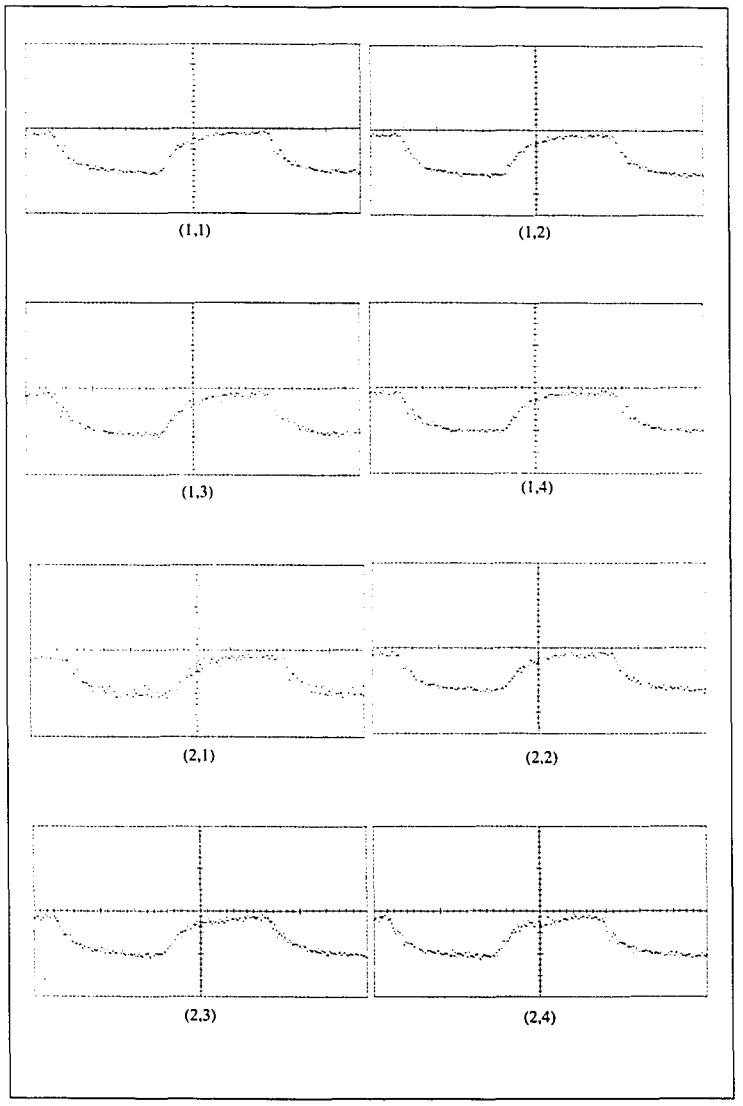
Figure 4.1.4 Modulation waveform of the setup in Figure 4.1.3 (power on the detector is 700uW).

higher bandwidth, chip carriers could be directly soldered to the PCB instead using socket,

however, the removability of the chip carrier was essential for chip replacement which constrained to the use of sockets. The MSM receiver prototype board was also built and using same packaging and board technology as the VCSEL prototype transmitter board. The receiver board had no PGA socket instead, the chip carrier was directly soldered to the board. Also, the receiver board had different configurations of transimpedance amplifiers and post amplifiers in order to test them.

The result obtained from the prototype board was used to build a transmitter daughter board capable of modulating all 16 VCSELs at a speed of 155Mbit/sec. In addition, the final VCSEL transmitter board integrated a TE cooler in the rear of the PGA package in order to operate the VCSELs in parallel. The final *PhaseII* VCSEL transmitter board as described in chapter 3 was tested with a measurement setup similar to that of figure 4.1.2 before being assemble in to the final system. The figure 4.1.5 shows output waveforms, detected with the Antel ARX-SA APD, of the M/D assembly as shown in figure 3.1.5 in serial operation, i.e. its channels modulated one at a time. The input signal generated by the HP8000 was a 50% duty cycle, 155Mbit/sec square-wave signal. The VCSELs were modulated from threshold to 1mW peak output power. At the same time, the PGA chip carrier was kept at room temperature (22-24^{o}C). The results of figure 4.1.5 shows a rise time of about 2 ns in contrast to the 400ps risetime measured previously with the prototype board. This is due to the added capacitance and impedance of the motherboard, cables and connectors.

After testing the different components individually, the *PhaseII* system was reassembled now with several improvements over the previously assembled system. The complete system as shown in figure 3.0.1, was then tested. The schematic diagram of the system is similar to of that illustrated in figure 4.1.6. The circuit diagram and details in device packaging, cooling and other physical descriptions are given in chapter 3. On the receiver board, the output of all 16 MSMs were amplified using the Hewlett Packard ITA-06300 transimpedance amplifier and the IVA-05208 post amplifier. The ITA-06300 comes in a unpackaged (bare die) form which allowed in-house mounting of 16 transimpedance amplifiers in the same chip carrier cavity as the MSM chip (see figure 4.1.6). The ITA-


(1,1)
(1,2)
(1,3)
(1,4)
(2,1)
(2,2)
(2,3)
(2,4)

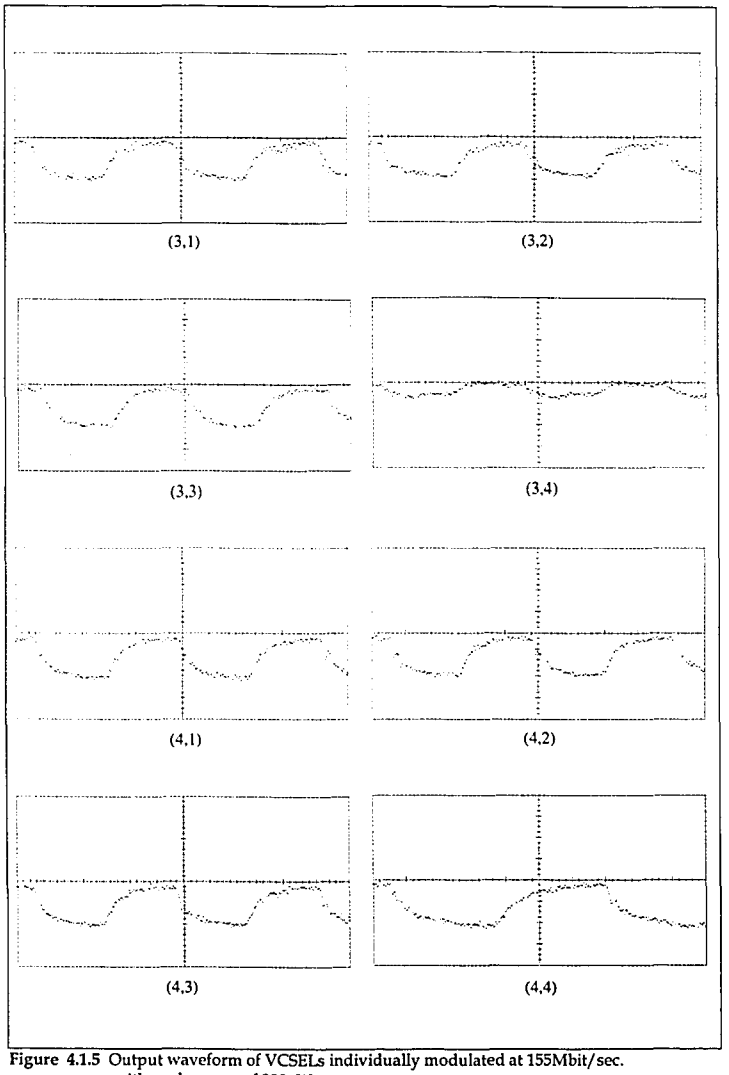


Figure 4.1.5 Output waveform of VCSELs individually modulated at 155Mbit/sec. with peak power of 800μW.

06300 has large gain, therefore, any noise coupled through the conductor between the MSM and the ITA-06300 would also be amplified. By mounting the transimpedance amplifiers close to the MSM, the noise coupling can significantly be reduced. This arrangement of MSM and transimpedance amplifier was tested with the prototype PCB before being implemented in the final system. The 16 ITA-05208 post amplifiers were surface mounted by soldering them to the daugtherboard. The post amp provides additional voltage amplification as well as voltage thresholding to give cleaner square waveform. The entire MSM receiver circuitry provided maximum output voltage swing of 450mV. Figure 4.1.6 shows the circuit diagram of a receiver channel and the packaged MSM and transimpedance amplifiers dies.

The new system was tested first, by generating an eye pattern to each of each channel. A 2^{23}-1 pseudo-random bit stream was generated using the HP8000 at a data rate of 155Mbit/sec. Figure 4.1.7 shows the 16 output eye pattern generated by input pseudo-random bit streams displayed on a HP 54120B dizitizing scope using 9 second display persistence. The optical power incident on the MSM detector was 800uW. The 450mV output voltage swing of the receiver was not large enough to drive a bit error rate tester (BIRT) which required TTL voltage levels. It would have been possible to use amplifiers to convert the voltage level to that which is suitable for the BERT but the added noice from the amplifier ,extra connectors and wires would introduce noices not inherent from the system. From the figure 4.1.7 it can be seen that some channels have better eye pattern that others. This might to be due to variation in boards traceline impedance, causing signal reflection, and parasitic capacitance associated with each channel.

The parallel operation of the channels was then tested also at a data rate of 155Mbit/sec. The input data pattern chosen were 16 bit patterns (permutations of 111, 000, 11, 00, 1, 1, 1, 0, 0, 0). Eight distinctive 16 bit patterns was input through 11 VCSELs simultaneously. Figure 4.1.8 shows the output of the MSM receivers captured using dizitizing scope. Simultaneous operation of more than 11 channels was not possible due to signal degradations associated with the addition of more channels. This is mainly because of the poor electrical and possibly optical isolations between VCSELs as will be shown in later sec-

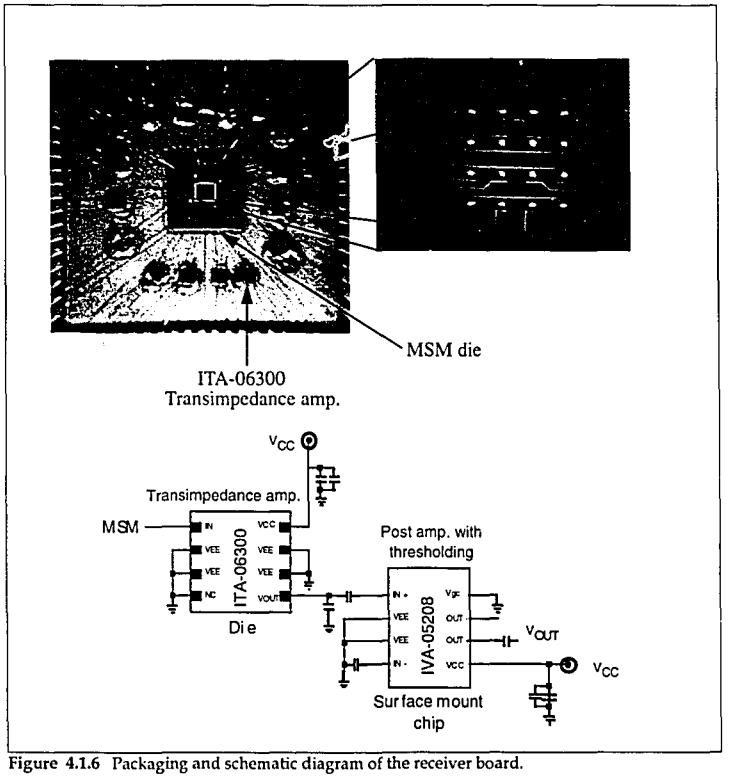
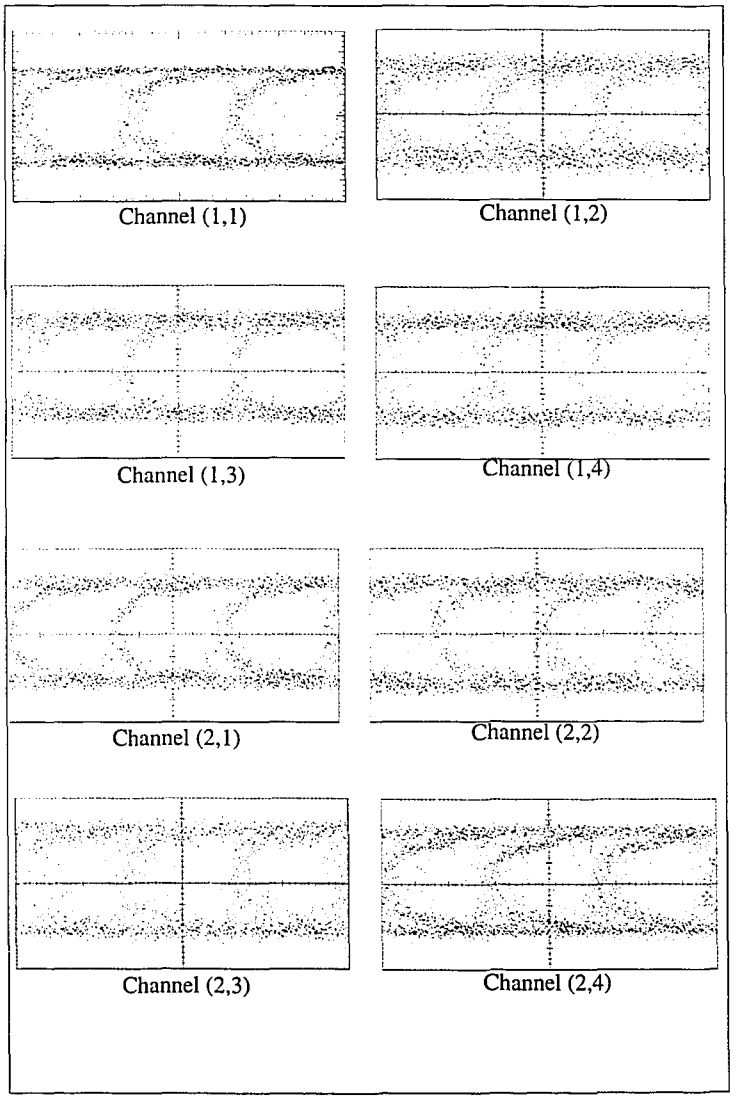


Figure 4.1.6 Packaging and schematic diagram of the receiver board.

tions. The VCSELs in the center of the 4x4 array, i.e. (2,2) (2,3), (3,2),(3,3), had the worst waveforms and signal-to-noise ratio than those located in the periphery. This crosstalk due to the current leakage between VCSELs is quantified and better explained in section 4.7.


Channel (1,1)
Channel (1,2)
Channel (1,3)
Channel (1,4)
Channel (2,1)
Channel (2,2)
Channel (2,3)
Channel (2,4)

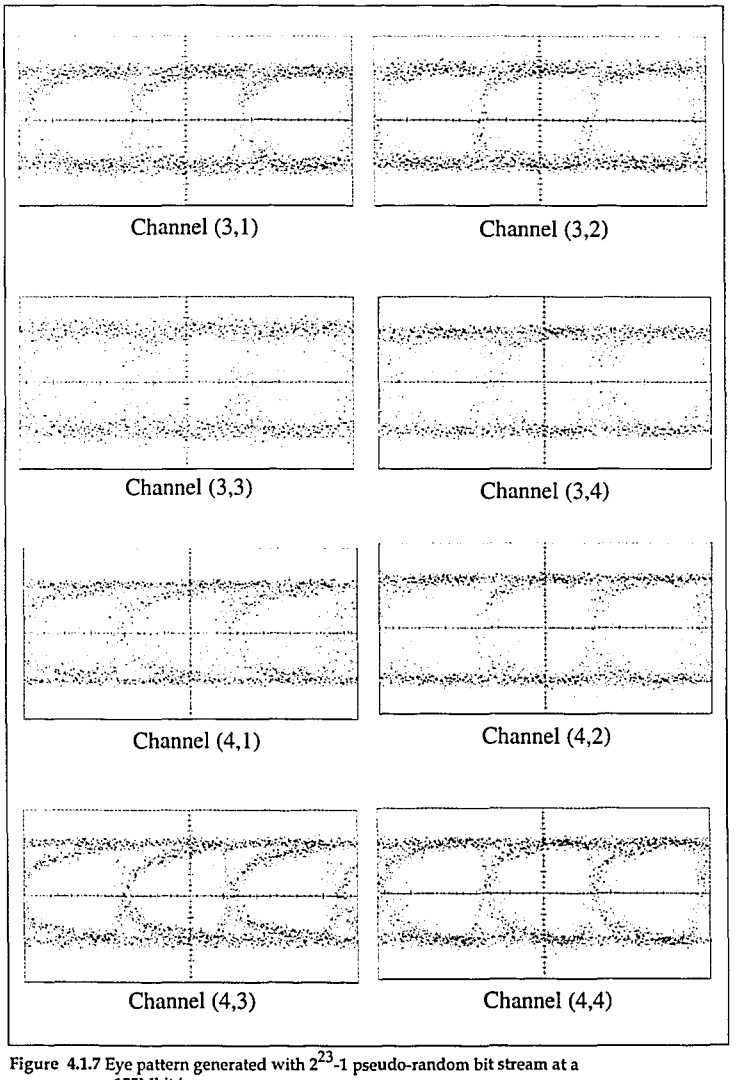


Figure 4.1.7 Eye pattern generated with 2^{23}-1 pseudo-random bit stream at a 155Mbit/sec .

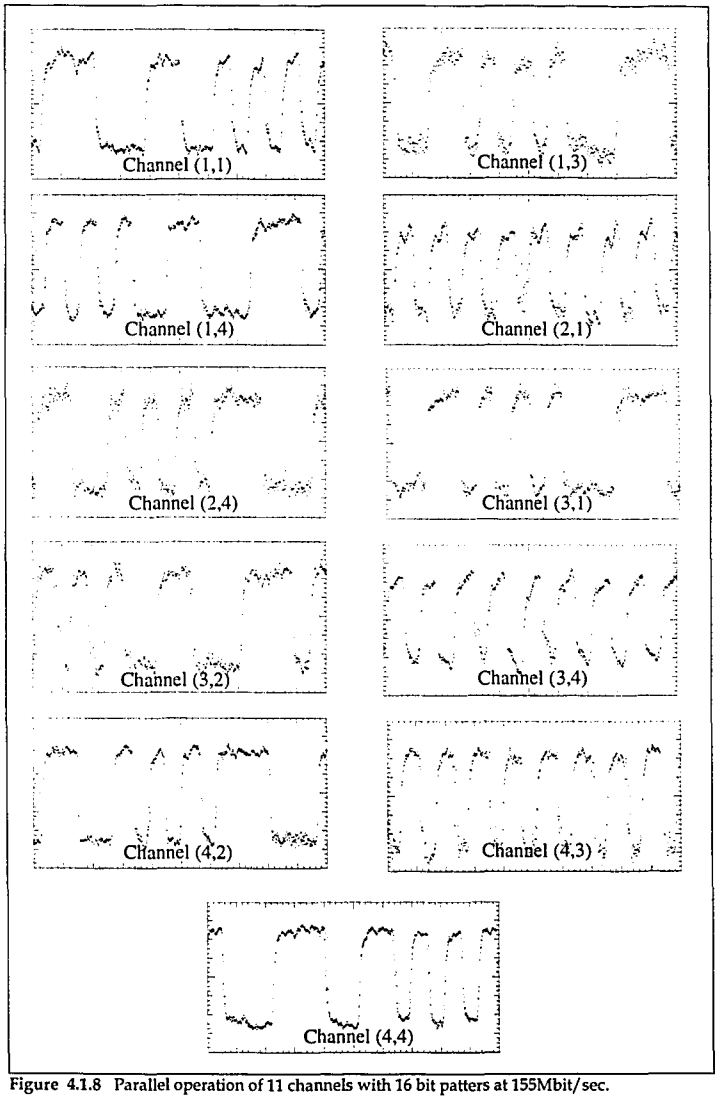


Figure 4.1.8 Parallel operation of 11 channels with 16 bit patters at 155Mbit/sec.

4.2 Power conversion efficiency

The wall-plug efficiency of the VCSELs or any semiconductor laser has strong dependencies on the temperature as discussed in chapter 2. One of the reasons that the speed-wired board couldn't operate more than few VCSEL simultaneously is because of the high temperature of the DIP chip carrier that the VCSELs were packaged in. With a TE cooler and a thermistor mounted in the PGA, it was possible to monitor and control the temperature of the package. A standard computer fan was used to remove the heat of the heatsink mounted on the hot side of the TE cooler. The TE cooler was capable of keeping the package temperature as low as 18°C while the VCSELs were dissipating about 450mW of power. Without the fan, the TE cooler could keep the PGA temperature around 22-24°C at a ambient temperature of 24°C. The PGA itself is a good heat conductor and since the entire chip carrier was exposed to ambient temperature, prevented from cooling it down further. Power conversion efficiency of 16 simultaneously operating VCSELs at 1mW continuous wave (CW) was measured at several temperatures. The current and the voltage across the VCSELs were measured using Fluke 75 multimeters and the optical power was measured with Newport 1835-C optical power meter with silicon detector head. The result is plotted in figure 4.2.1 and shows the power conversion efficiency at room temperature (24°C) to be about 3%. The temperature dependance conversion efficincy is about 0.2%/°C around the measured temperature range. With such a high dependency of conversion efficiency to the temperature, good thermal management is needed to have stable output power. As well, larger device separation is preferred in order to avoid large temperature gradient across the array.

4.3 Wavelength drift

The output wavelength of a VCSEL shifts with temperature due to the expansion and contraction of the cavity. For example, with increased operating temperature the output drifts toward longer wavelength. This wavelength drift is of important interest if

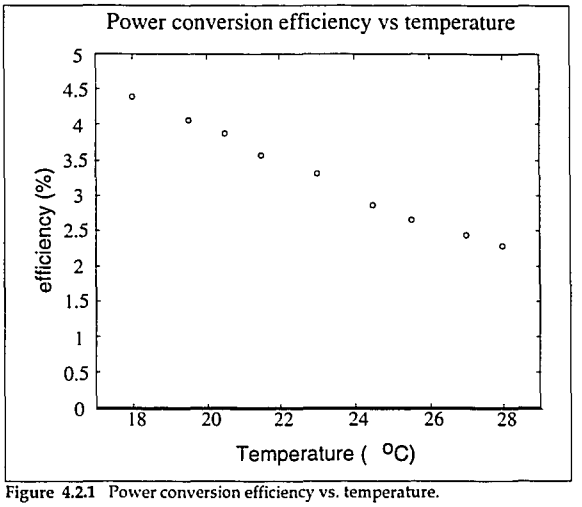


Figure 4.2.1 Power conversion efficiency vs. temperature.

any wavelength sensitive optics like diffractive lens or were to be used. The output wavelength of the VCSEL(1,3) emitting 1mW of CW power was measured at different die temperature using the Anritsu MF9630A wavelength meter. The estimated measurement error is less than 0.1nm measured by repeated sampling of a specific data point during the course of measurement. The rate of wavelength drift over the measured temperature range can be estimated to be about 0.1nm/°C from the result shown in figure 4.3.1. This wavelength drift is small compared to the fabrication tolerance of +/- 15nm (not between individual devices) of this particular VCSELs . It means that the wavelength variation due to fabrication tolerance has way bigger impact than the variation due to the operating temperature.

4.4 Output beam profile

The spatial profile of VCSEL for several output power was measured using Merchantek's PC-Beamscope beam analyzers. The beamscope measures spatial profile of

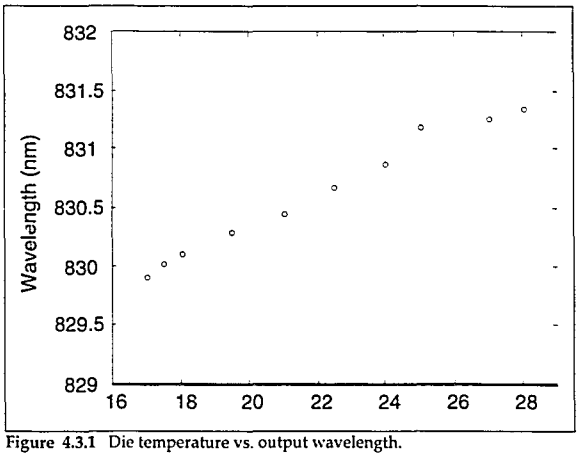


Figure 4.3.1 Die temperature vs. output wavelength.

a beam along the x and y axis by mechanically moving a slit across the beam. The unit is computer controlled and the datapoints sampled and analyzed also by a computer. The beam analyzer was placed at a distance of 9.5mm in front of the VCSELs without any optics. The temperature of the VCSEL package was kept at 21°C during the measurement while the output power was varied from 0.15mW to 3mW. The divergence angle was measured at the full-width-half-maximum point (FWHM). Figure 4.4.1 shows the x and y axis beam profile at 1mW and the table 4.4.2 shows the divergence angles and the percent Gaussian curve fit at different output power. The spatial mode at 1mW of output power is Gaussian with 97.2% fit to the theoretical Gaussian curve and the divergence measured at FWHM is 8.02° and8.16° in x and y direction respectively. The table 4.4.2 shows the important advantage of VCSELs over the edge-emitters; the TEM_{00} mode at maximum rated output power and the symmetry of the output beam.

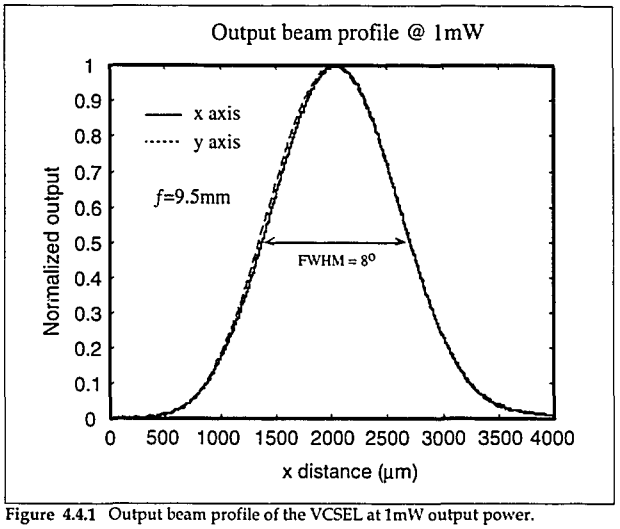


Figure 4.4.1 Output beam profile of the VCSEL at 1mW output power.

Power (mW)	Gauss fit x	Gauss fit y	Divergence x	Divergence y	symmetry x/y
0.15	94.9 %	91.5 %	8.28°	8.53°	0.96
0.3	96.4 %	96.5 %	8.13°	8.43°	0.96
0.5	97.1 %	97.2 %	8.09°	8.31°	0.97
0.8	97.1 %	97.1 %	7.98°	8.31°	0.96
1	97.2 %	97.2 %	8.02°	8.16°	0.98
1.4	97.2 %	96.9 %	8.09°	8.22°	0.98
2	97.5 %	97 %	8.25°	8.31°	0.99
3	98.7 %	97.3 %	8.76°	8.87°	0.99

Table 4.4.2 Spatial profile of VCSEL at various output power.

4.5 Wavelength Uniformity

The output wavelength uniformity of the parallel CW operation of VCSELs was measured. This was done in order to find out if the temperature gradient present in

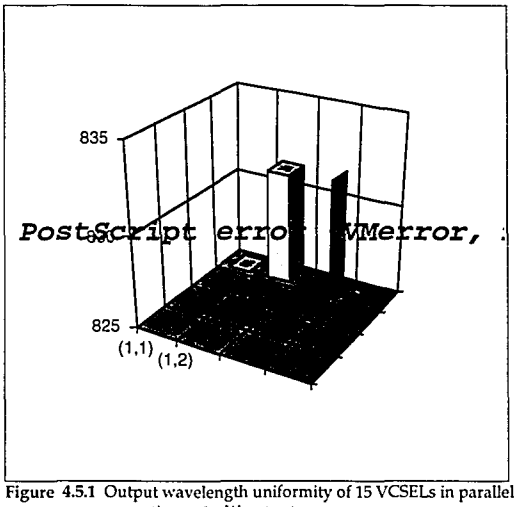


Figure 4.5.1 Output wavelength uniformity of 15 VCSELs in parallel operation at 1mW output power.

parallel operation of VCSELs was significant enough to affect the wavelength uniformity in a noticeable way. The wavelength was measured with the Anritsu MF 9630A wavelength meter. The output power of each VCSEL was set to 1mW and the temperature was kept at 24°C. The measured uniformity shown in figure 4.5.1 does not have any particular distribution related to temperature gradient across the array, indicating that the non-uniform output wavelength is due to other factors. This is in accordance to result in section 4.5 that showed wavelength sensitivity to temperature of VCSEL of only about 0.1nm/°C. However, figure 4.5.1 shows maximum difference of 1.6nm between wavelength. Since previously it was determined that the output wavelength does not vary much with temperature, this might be due to the decay of the cavity structure.

4.6 Threshold current

Variation in threshold current in a VCSEL causes non-uniform output power and phase delay between channels. The change in threshold current to temperature was measured using a optical power meter and a ampmeter. Current was supplied to VCSEL(3,3) while all other lasers were off. The temperature was varied from 16.5 to 27.5 °C and the Newport 1835-C powermeter with a silicon detector was used to detect the power. The result plotted in figure 4.6.1 shows that the threshold current fluctuate about 14% between 16.5 and 27.5°C. The temperature sensitivity around the measured tempera-

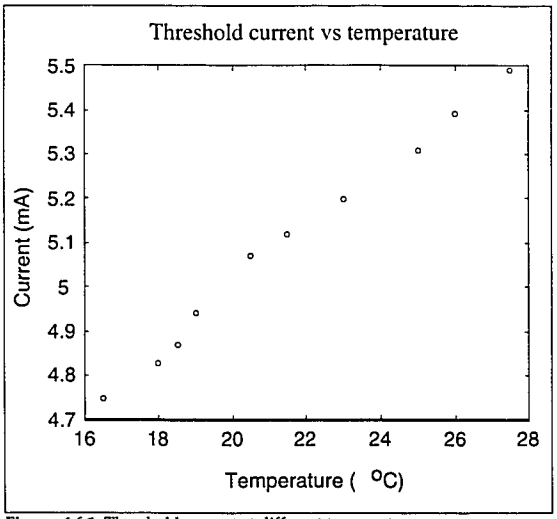


Figure 4.6.1 Threshold current at different temperature.

ture range is 39μA/°C. The result indicates that if no active temperature control were to be used, the system must somehow compensate for the threshold current drift. For example, for an laser array driver like the SPDA-16, where the DC current bias point is same for all the output, the circuit should shift the bias point about a rate of 40μA/°C.

Another factor that affects the threshold current of a VCSEL in a 2-D array is the current leakage from adjacent VCSEL (or VCSELs). To show this, different combinations of neighboring VCSELs to VCSEL(3,3) was operated at 1mW of output power. The threshold current of VCSEL(3,3) measured for each combinations while the chip temperature was maintained to 23°C. The result in figure 4.6.2 shows the effect of current crosscoupling to the threshold current. The threshold current changes from 5.19mA, when single operation, to 0.9 mA when 4 adjacent VCSELs are operating. This is due to poor electrical and possible optical isolation of VCSELs. As mentioned in chapter 2, the disadvantage if planar 2-D VCSEL structures is its electrical isolation. The isolation is achieved trough proton implantation and with small device spacing (250μm for the *Phase II* VCSELs), it becomes more difficult to achieve good electrical isolations.

4.7 Crosstalk

There were two 3 factors contributing to the crosstalk between channels in the *PhaseII* system. First, the inductive and capacitive crosstalk between channels due to electrical conductors. Second, the optical crosstalk in which the optical beam from one channel is bleeded onto the detector of a channel near by. Third, current leakage between VCSELs because of the finite resistance between them. Because of the finite resistance of the proton implantation, there is a current leakage between one device to next. The crosstalk was most noticeable between adjacent devices specially if more than one neighbor device is operating at the same time. To measure the extent of this crosstalk, a setup illustrated in figure 4.7.1 was used. To isolate the output of each VCSEL, a pinhole mounted on a xyz translation stage was used having the array of VCSEL imaged by a microscope objective. For accuracy, the optical power was measured in darkness with a Newport 18835-C optical power meter. The temperature of the chip was fixed at 23°C during the entire measurement. While keeping the VCSEL in interest lasing at 1mW CW, the output power of neighboring VCSEL (or VCSELs) was varied from few μW to 1mW in order to measure the cross talk due to change in power in nearby VCSELs. For the first measurement, the VCSEL(3,2) was kept at 1mW while the output power VCSEL(2,2) was

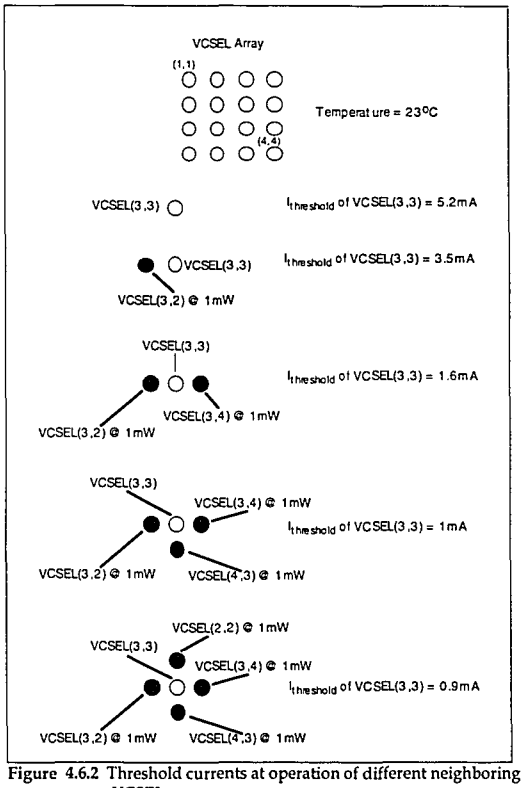


Figure 4.6.2 Threshold currents at operation of different neighboring VCSELs.

varied. The result is plotted in figure 4.7.2 shows that if VCSEL(2,2) is modulated between 0.05mW (threshold) to 1mW, the fluctuation of output power in VCSEL(3,2) is almost 4%. The crosstalk gets larger as the number of neighboring VCSELs being modulated are increased. The previous crosstalk measurement was repeated, this time having VCSELs (2,2) and (4,2) changing power as the VCSEL(3,2) output power is kept constant. The result (in figure 4.7.2), shows output power fluctuation of 8% if the VCSEL(2,2) and (4,2) is simultaneously modulated between threshold and 1mW. The increased power of VCSEL(3,3) indicates that as in previous section, the current from adjacent VCSELs are

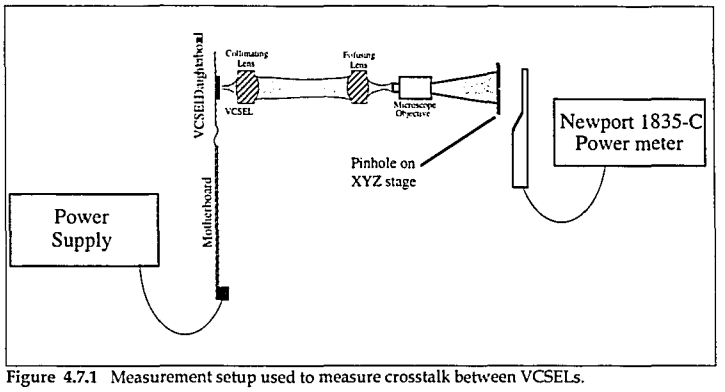


Figure 4.7.1 Measurement setup used to measure crosstalk between VCSELs.

being coupled. The current coupling between VCSEL(4,2) and (2,2) was also measured but in this case the output power fluctuation was negligible showing that the large distance between those two devices in enough to prevent current leakage.

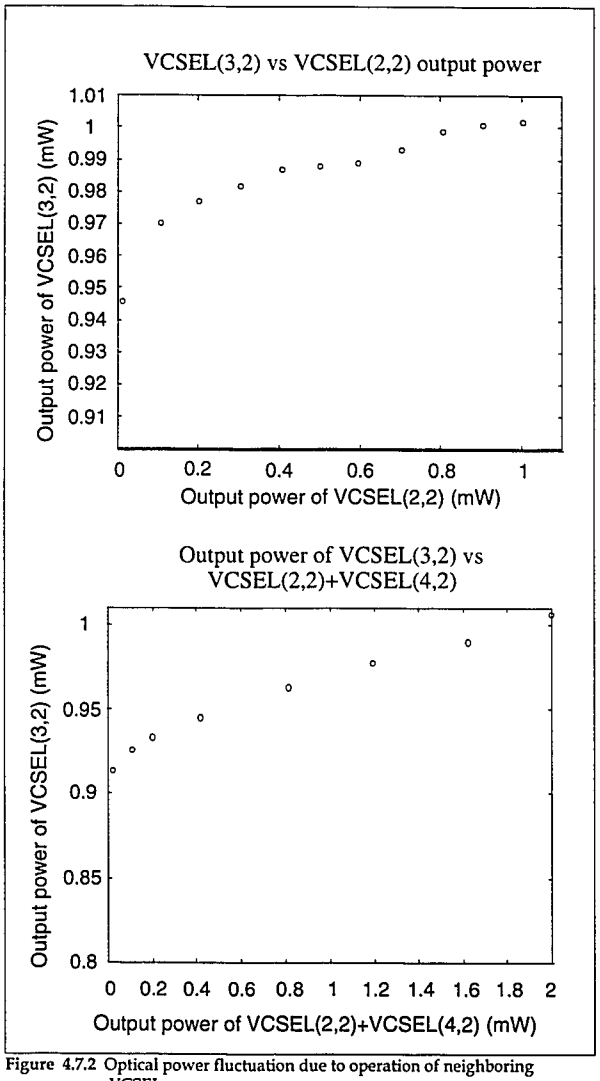


Figure 4.7.2 Optical power fluctuation due to operation of neighboring VCSELs.

Chapter 5

Conclusion and future work

In order for a free-space optical backplanes to be fully functional in comparison with current electronic backplanes, it has to meet certain requirements. The system has to be scalable without its physical dimensions being much larger than the equivalent electronic system. Also, the bidirrectionality, i.e. the ability to transmit and receive, from each board is essential if any practical system is to be built. Power dissipated from the optical backplane should be considerably less than its electronic counterpart since one of the strong arguments for the optical backplane is its low power consumption. The system shouldn't require an elaborate cooling scheme. To achieve all aforementioned, it puts a certain requirement to the optics, optoelectronics and optomechanics. With the results from previous chapters, which were obtained by characterizing the PhaseII free-space optical backplane demonstrator, we can identify many of the issues that should be addressed in order to make the VCSEL-MSM free-space optical backplane feasible. In this chapter, we will take many of the results from previous chapters specially from chapter 4, which deals with the demonstrator system performance, and present some of possible solutions and future directions in order for the VCSEL-MSM based backplane systems be competitive with all-electronic backplanes.

For the system to be scalable in comparison with existing electronic backplanes, the board pitch should be comparable to those of electronic backplanes (not more than inch or two). A larger board pitch will lead to systems with large physical dimensions therefore undesirable. The PhaseII VCSEL-MSM system showed that board pitch comparable to electronic backplanes is possible using bulk optics, for 4x4 array of transmitters and detectors with 125μm device separation. Although bulk optics can handle slightly larger arrays than 4x4, it is not practical to use bulk optics for systems with large VCSEL and MSM device arrays. To illustrate this point, suppose that a 32x32 array of VCSELs with 125μ m pitch is to be used to build a system. The optics in the system should be able to relay a 4mm x 4mm square image without any distortion at a distance of about an inch. To image large areas using bulk optics without distortion, requires multiple lens system with large apertures. A more realistic method of relaying a large array of VCSEL outputs to MSM detectors is to use either refractive or diffractive microlens arrays. Use of diffractive microlenses with VCSEL won't be practical unless the output wavelength tolerances are improved from present few nanometers to sub nanometers. Sub nanometer wavelength control for large VCSEL arrays, specially during parallel operation, is difficult to achieve in a near future. Another way of relaying the output of VCSELs to MSM detectors is to use refractive microlenses. The fabrication of most refractive microlenses relies on the surface tension of the lens forming liquid and therefore the shape of the lens is inherently spherical. Spherical aberrations of the lenses should be taken into consideration when using short focal length refractive microlenses. To integrate 2-D array of microlenses with VCSELs, new packaging schemes or growth methods must be developed. The later is preferred since it is difficult to align microlenses with submicron accuracies over VCSELs without introducing lateral, rotational and tilt misalignment. Due to this tight tolerance in packaging VCSELs with microlenses, the fabrication cost would be high unless the microlenses are grown on top of the VCSELs. Among the 3 types of imaging optics so far discussed for VCSELs, i.e. bulk lenses, refractive microlenses and diffractive microlenses, the most realistic near term solution for free-space optical backplane systems is the use of refractive microlenses.

Another aspect of the system affecting the scalability is the bidirectionality of each board. In the case of the demonstrator system, this means the ability of the daughter board to transmit as well as receive information. This means that each daughterboard should have both the transmitter and receiver arrays. To achieve this, the VCSELs and the MSMs can be packaged in a multichip module. The smart pixel electronics can be either integrated with VCSEL and (or) MSM chip or be in its own die, packaged in the same multichip module. Although this method of packaging is clearly possible, it is difficult to align the VCSEL and MSM dies within optical alignment tolerances. As an alternative, the monolithic integration of VCSELs and MSM with GaAs logic, as mentioned in chapter 3, seems like a more attractive solution. However, the technology needed to generate high-yield, high-density, uniform devices could take years to develop. Among the current device technologies, the flip-chip bonding of GaAs optoelectronics with CMOS logic is among the most feasible approach to produce a single die with high VCSEL and MSM array density with enough processing power needed to implement smart-pixel based architectures. Using flip-chip bonding, inexpensive and reliable CMOS logic can be combined with GaAs optoelectronics without device misalignment.

The VCSEL driver electronics should also be integrated in a same chip with smart pixel electronics for several reasons. Having the VCSEL and VCSEL drivers integrated together will allow for faster modulation of VCSELs and less noise coupling. Also, external driver sources cannot accommodate the electrical connections needed to drive a large number of devices. The driver design should incorporate the temperature compensation for bias current. As seen in chapter 4, VCSEL threshold current was highly dependant on the temperature. Therefore the bias current of the VCSELs should be shifted proportionally with the device temperature in order to keep the output power constant. Unfortunately, unlike the diode laser drivers used for fiber optic communication systems, it is difficult for the VCSEL used for free-space systems to have output feedback for current control. This means that the VCSEL array must have well defined and uniform L-I characteristics to be able to use open loop current control for their drivers.

Based on the results of chapter 4, it is evident that the performance of VCSEL has to be improved in several aspects. The power conversion efficiency should be improved in order to avoid active cooling of the chip, the devices should have longer lifetime, the output power and wavelength have to be uniform and the power conversion efficiency should be high. The device has to be better isolated thermally, electrically and optically before large 2-D array of VCSELs can be used in a real system.

The continued work on the VCSEL-MSM based free-space backplane systems should be geared toward the demonstration of what is possible with the available technology. The optoelectronics will eventually evolve to the point that large connectivities are possible, due to the many potential uses that push the technology to evolve rapidly. Having said that, the demonstrator should be a reduced connectivity version of the intelligent backplane, in our case the Hyperplane architecture. The next demonstrator system, i.e. Phase III, should implement the hyperplane architecture in a small array (4x4 or 8x8) with bidirectional daughterboards and microlenses for relay optics.

With the Phase II system, the first free-space VCSEL-MSM backplane, constructed using the existent electronic backplane frame, was demonstrated. The operation of up to 11 channels at a speed of 155Mbit/s was demonstrated, showing the feasibility of practical system in a near future.