Three-Dimension Integrated Circuit Design and Through-Silicon Via Characterization

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Abstract

This thesis presents the design of a prototype chip of a 3D IC made in the Tezzaron Process. As this work is the first of its kind at a Canadian University, this thesis is focused on the characterization of the one of the key components of this technology, that being, the Through-Silicon Via or TSV for short. The TSV is modeled as a lumped-equivalent RC circuit, whereby embedded instruments have been constructed to measure the R and the C of a TSV. Specifically, a Kelvin four-point probe has been devised to measure the series resistance of a TSV and several versions of a parasitic capacitance meter has been constructed to measure the effective shunt capacitance of a TSV. One approach to measuring the shunt capacitance makes use of a frequency-based approach whereby the frequency of two ring oscillators, one loaded by a TSV, the other left opened, are measured and used to predicted the capacitive load difference. The other approach makes use of a charge-based method whereby the average difference in the amount of charged transferred in any one charging cycle is measured using a current meter. To ease the measurement control and data capture, an analog JTAG test bus was developed and used to extract the test data in a manner that is compatible with that used in the semiconductor industry. An extension to the JTAG analog boundary scan cell is proposed that reduces the silicon overhead required when used in a 3D-IC.

Résumé

Cette thèse presénte la conception d'une puce prototype d'un IC 3D réalisés dans le processus Tezzaron. Comme ce travail est le premier de son genre dans une université canadienne, cette thèse se concentre sur la caractérisation de l'un des éléments clés de cette technologie, que l'être, la Via biais de silicium ou TSV pour faire court. Le TSV est modélisée comme un circuit RC équivalent-localisées, dans lequel les instruments embarqués ont été construits pour mesurer la R et C d'un TSV. Plus précisément, un Kelvin quatre points de sonde a été conçue pour mesurer la résistance série de quelques versions TSV et plusieurs d'in compteur de capacité parasite a été construit pour mesurer la capacité shunt efficace d'un TSV.Une méthode pour mesurer la capacité de shunt utilise une approche de fréquence basée sur la fréquence selon laquelle des deux oscillateurs en anneau, l'un chargé par un TSV, l'autre gauche ouverte, sont mesurées et utilisées pour prédire la différence de charge capacitif. L'autre approche faire usage d'une méthode de charge à base de sorte que la différence moyenne dans la quantité de particules chargées transféré cours d'un cycle de charge est mesurée à l'aide d'un courantomètre. Pour faciliter le contrôle de mesure et de capture de données, un bus de test analogique JTAG a été développé et utilisé pour extraire les données d'essai d'une maniére qui est compatible avec celle utilisée dans l'industrie des semi-conducteurs. Une extension de la cellule JTAG boundary scan analogique est proposé qui permet de réduire les frais généraux du silicium nécessaire lorsqu'il est utilisé dans un 3D-IC.

Acknowledgments

Foremost, I would like to express my sincere gratitude to my supervisor Professor Gordon W. Roberts for the continuous support and guidance of my master study and research, and also for his enthusiasm, vision, immense knowledge and patience. It was him who lead me into the analog and mixed-signal design and test world, and offered me the great opportunity to work with.

Besides my supervisor, I would like to thank McGill University and CMC Microsystems for the opportunity to design the first prototype 3D chip in Canada. I am grateful to Hsu L.Ho, Jim J. Quinn and Hudson An from CMC Microsystems, for the technical support in the design and fabrication process.

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List of Acronyms

TSV	Through-silicon Via
SoC	Systems on Chip
SiP	System in Package
PiP	Package in Package
PoP	Package on Package
DfT	Design for Test
PISO	Parallel in Shift out
JTAG	Joint Test-Action Group
CUT	Circuit-under-test

Chapter 1

Introduction

Since the early 70's, the semiconductor industry seems to have doubled the number of transistors integrated on a single monolithic substrate every 18 to 24 months as depicted by Fig. 1.1. Such a phenomena is commonly referred to as *Moore's law*. By reducing the dimensions of a transistor, better performance and lower cost products were introduced into the various electronic markets, resulting in an exponential growth in those markets. Greater revenues, drew more investment, which continues to demand further transistor scaling. Such a relationship between market growth and transistor scaling is illustrated in Fig. 1.2. The virtuous circle of the semiconductor industry has kept the entire semiconductor industry growing in a healthily and steadily manner, until now, where the scaling of a transistor can no longer be performed on account of reaching the atomic scaling limit (i.e., a transistor constructed from a single atom).

The International Technology Roadmap for Semiconductors (ITRS) divided the trends of miniaturization into two. One is the miniaturization of the digital functions, which is the scaling down of transistor size, also known as *More Moore*. The other is the functional diversification, more functionalities in a single packaged chip, known as *More-than-Moore*, as illustrated in Fig. 1.3.

More-than-Moore technologies, which focuses on system integration, have made significant contribution to the semiconductor industry world-wide. A new virtuous circle needs to be created and adapted to relay these industries and their investments, in a manner depicted by that shown in Fig. 1.4. Instead of relying on a transistor scaling paradigm, innovations at all levels must occur, including the system, circuit, device and technology

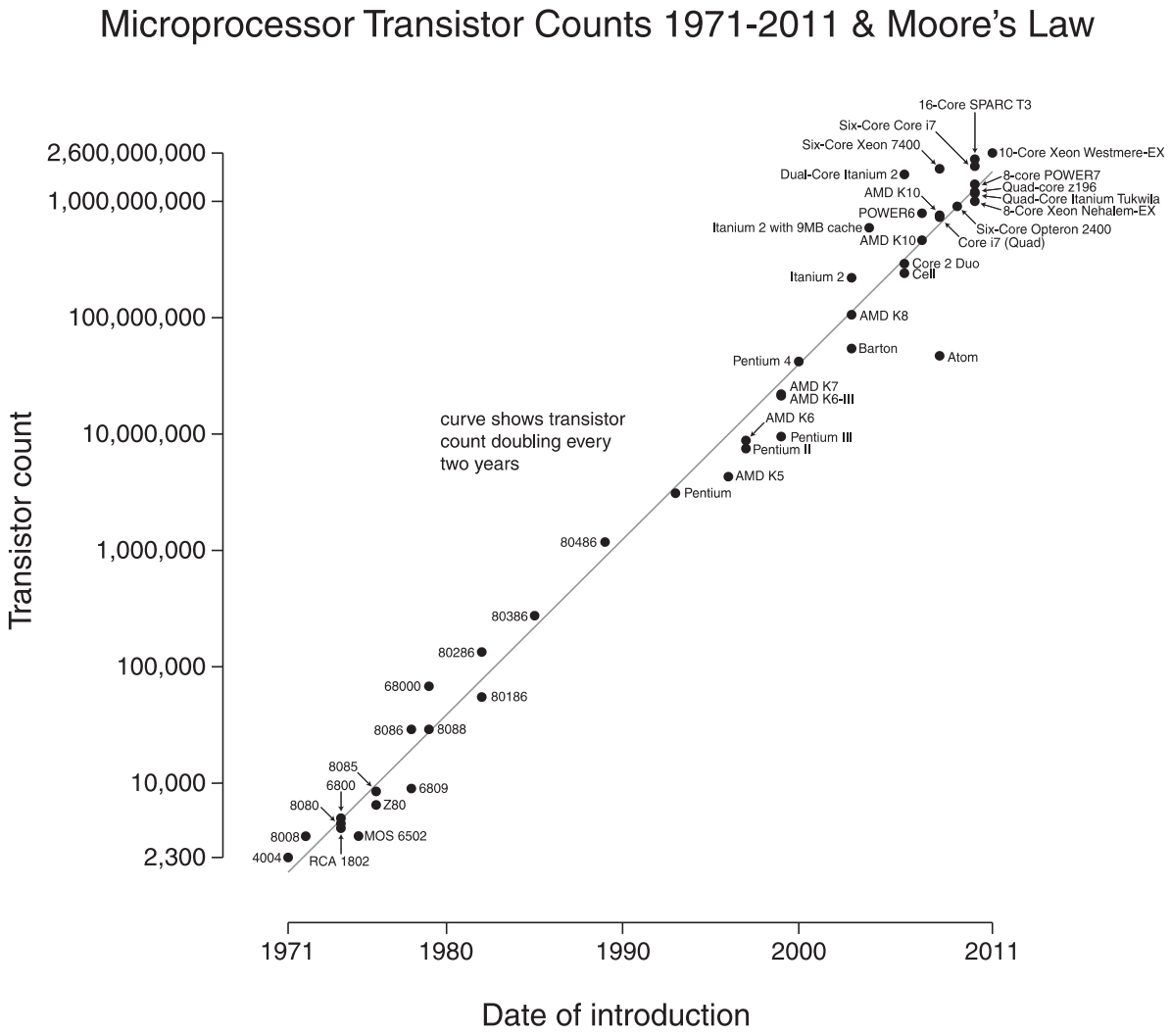


Fig. 1.1 Moore's Law 2011

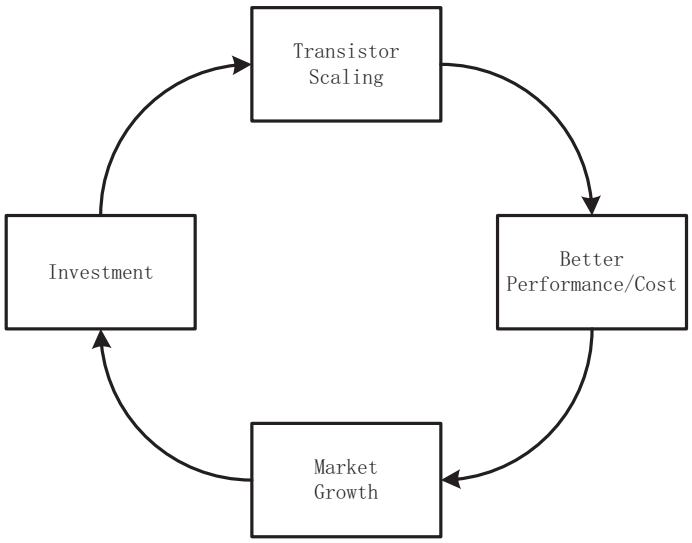


Fig. 1.2 The Virtuous Circle of the Semiconductor Industry

levels. Innovations should address both the functionalities and cost of a whole chip. This also encourages the growth of various domains of scientific research, which leads to further opportunities.

1.1 3D IC

While opportunities in a More-than-Moore paradigm are huge, so too are the challenges. The integration of multiple chips in a single package serves as another path to move forward in the More-than-Moore domain. Systems-on-chip (SoC) and System-in-package (SiP) are the two most popular integration types seen in the market today.

1.1.1 SoC and SiP

Systems-on-chip (SoC) packs several functionalities into a single silicon die. It usually includes digital, analog, mixed-signal and even RF intellectual property cores, or IPs for short, in a single chip substrate. However, there are some drawbacks for the single-die SoC. These can be listed in point form as follows:

- All components are placed on the same die using the same process technology.

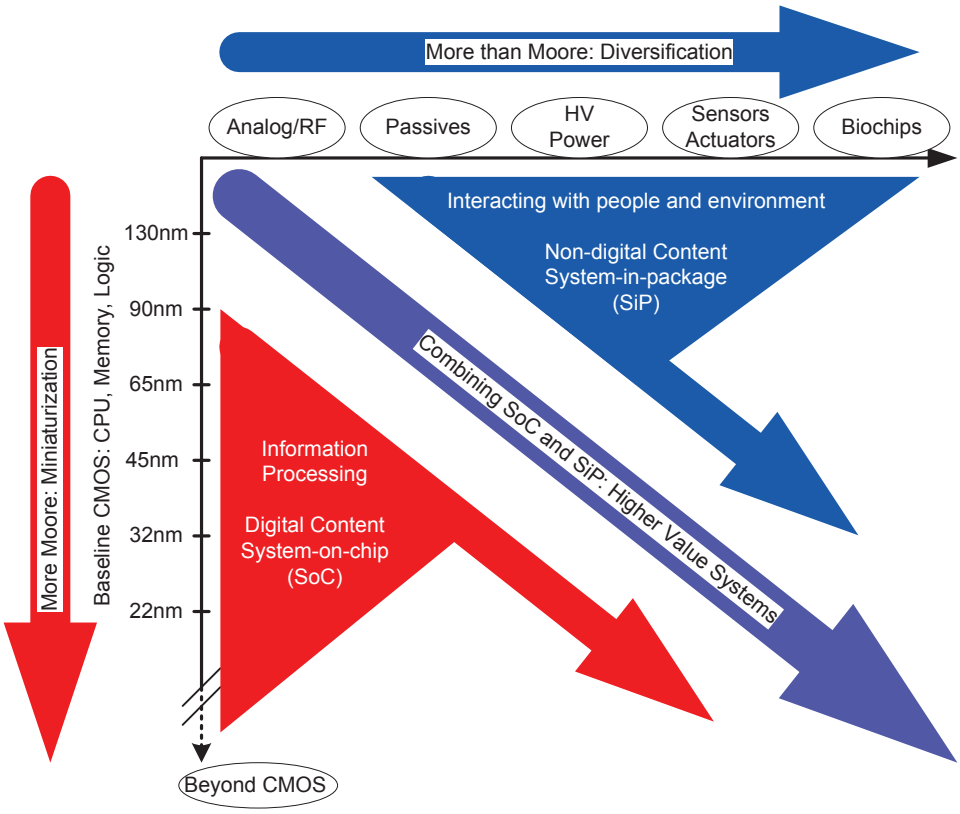


Fig. 1.3 The Trends In Electronic Miniaturization

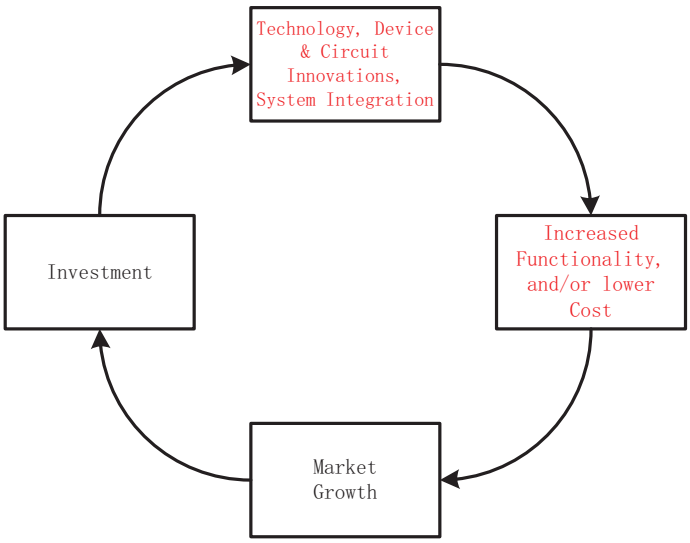


Fig. 1.4 Virtuous Circle with More than Moore

- The migration of analog and RF circuit into the same process takes time, thereby extending the product's time-to-market and increasing its engineering costs.

The Systems-In-Package (SiP) approach offers several advantages over SoC. Digital, analog, mixed-signal and RF circuits can be implemented using separate technology processes, thereby optimizing the performance of each. The comparison of SoC and SiP is illustrated in Fig. 1.5. Meanwhile, micro electromechanical systems (MEMS) could also be integrated into the same package; something one is finding in many electronic products today, e.g., iPhone. Fig. 1.6 shows a photograph of twenty-four stacked dies by Amkor Technology. Such an example demonstrates the capability of an SiP approach.

Other packaging alternatives have since been created. These include package-in-package (PiP), where a number of smaller SiPs were mounted on top of one another to form a larger SiP, and package-on-package (PoP), where one SiP was assembled on top of the other SiP. Nonetheless, these technologies offer the advantages that a 3D-IC approach using thru-silicon-vias (TSVs) seems to provide, such as performance, power improvement, density and overall cost of manufacturing.

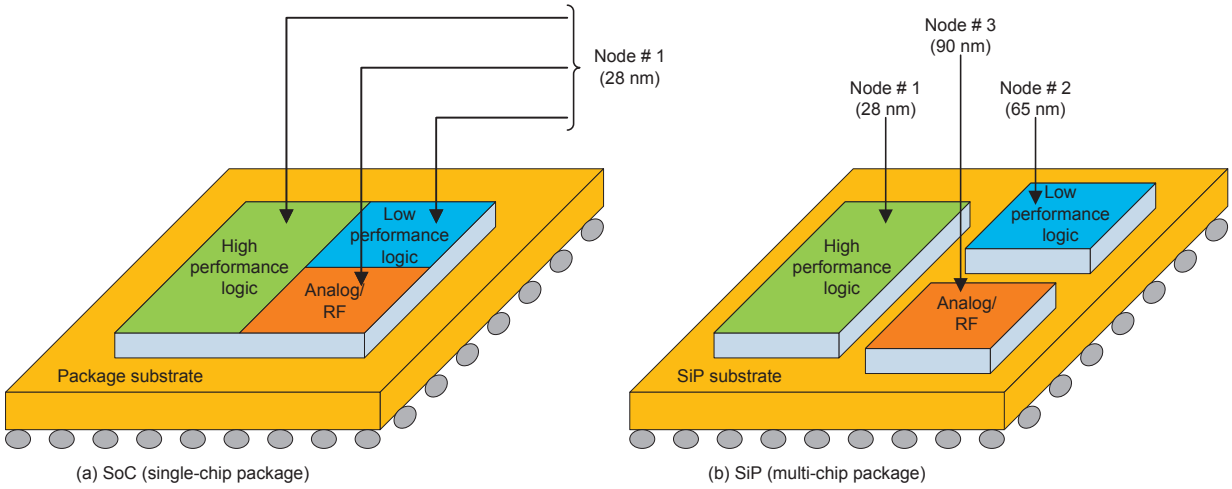


Fig. 1.5 SoC VS SiP

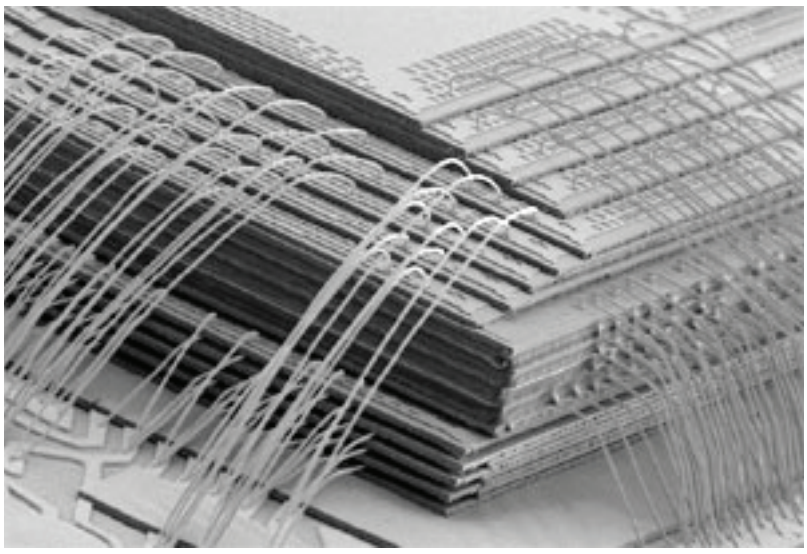


Fig. 1.6 24 Stacked Dies In A Single Package By Amkor Technology

1.1.2 3D-IC with TSV

Thru-silicon-vias (TSV) is a vertical electrical connection made to pass through the silicon wafer/die in a vertical manner. TSVs are made of copper whose diameters may range from 1 to 30 micrometers. A 3D-IC usually connects two or more dies with TSVs. Depending on the process and numbers of stack dies, commonly referred to as tiers, the 3D-IC may be bonded in back-to-face (B2F) manner such as that shown in Fig. 1.7 or face-to-face (F2F) manner as shown in Fig. 1.8. Bonding between tiers may or may not rely on TSVs. It could be a copper bump instead.

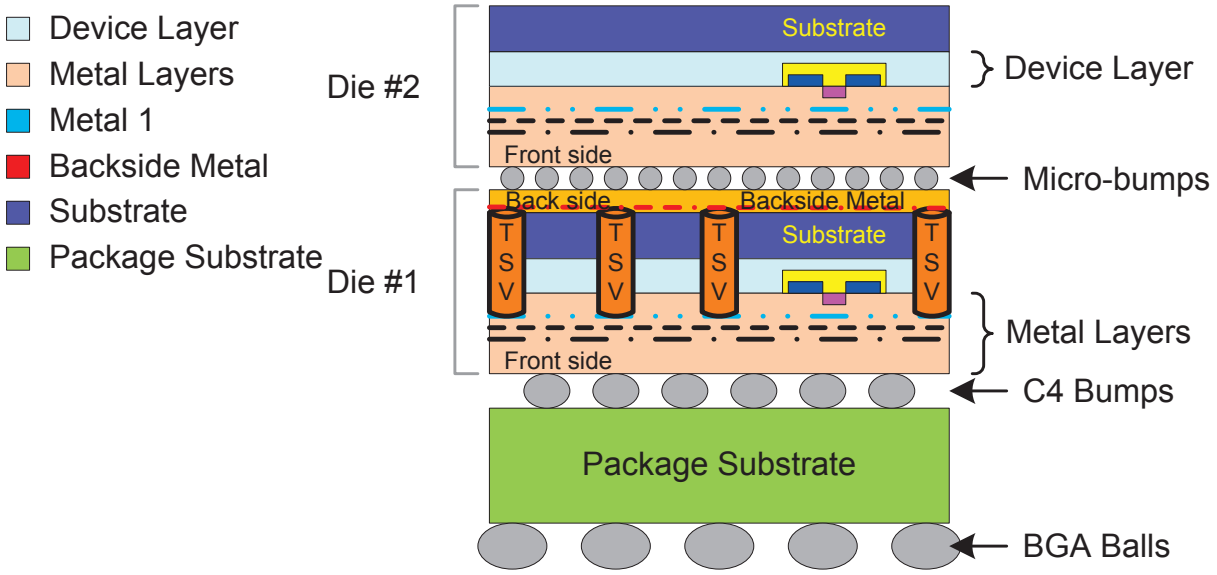


Fig. 1.7 Back-to-face bonding 3D-IC

3D-ICs constructed using TSVs have the following advantages over a stacked-die package arrangement:

- Interconnect between dies are shortened, allowing high-speed performance.
- Big drivers can be eliminated, which will end up saving a lot of power.
- 3D-IC also allows more miniaturization, saving a lot of space; they are ideal for the compact mobile market.
- Re-use of dies increases the manufacturing yield.

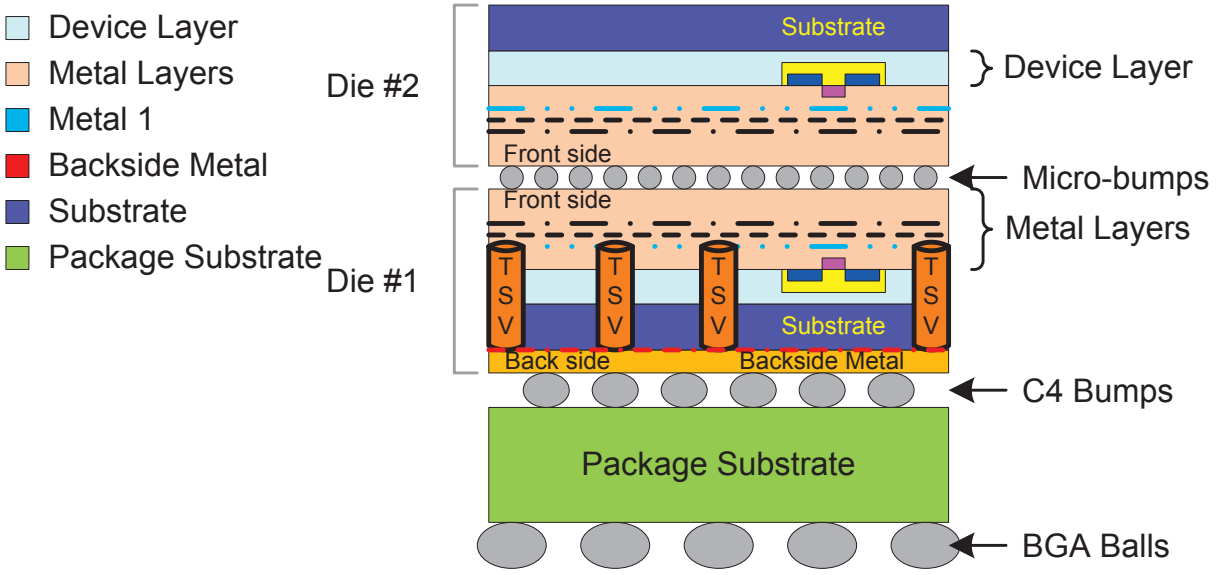


Fig. 1.8 Face-to-face bonding 3D-IC

- Beside integration of multiple functions, 3D-IC also shorted the time-to-market, which results in lower cost.

All of these points are summarized in Table 1.1 for easy access.

Table 1.1 3D Packaging VS 3D-IC

Spec	3D Packaging	3D-IC with TSVs
Interconnect	Long	Short
Performance	Slow	Fast
Power Consumption	High	Low
Density	Low	High
Chip Area	Large	Small
Yields	High	Low
Cost	High	Low

1.2 3D Integration Process

Generally speaking, the 3D integration process follow three main manufacturing steps [1]: (1) Through-silicon via formation, (2) Wafer thinning, and (3) Wafer aligning or die bonding. Each of these steps can be described as follows:

1. TSV Fabrication:
   (a) TSVs were fabricated during the IC fabrication process:
      i. Front-end-of-line (FEOL) TSVs are fabricated before the wiring process in IC fabrication.
      ii. Back-end-of-line (BEOL) TSVs are done during the metal wiring process in the fabrication.
   (b) TSVs were fabricated after the complete ICs were fabricated, which is also known as Post-BEOL TSVs.
      i. TSVs are fabricated before die bonding (vias first).
      ii. TSVs are fabricated after die bonding (vias last).
2. Wafer Thinning:
   (a) The wafers were thinned on temporary handle wafers.
   (b) The wafers were thinned after bonding to the 3D-IC stack.
3. Wafer Aligning or Die Bonding:
   (a) Metal bonding (multiple methods, all create electrical interconnect between layers.)
      i. Direct Cu/Cu, Au/Au, and so on.
      ii. Eutectic CuSn, and so on.
      iii. Hybrid SiO_2/metal.
   (b) Direct bonding (e.g. SiO_2-SiO_2).
   (c) Adhesive bonding.

Tezzaron®Semiconductor is one of the world wide leaders in 3D-IC manufacturing, specialized in 3D wafer stacking and TSV processes. Canadian Microelectronics Corporation (CMC) collaborates with Tezzaron, MOSIS and Circuits Multi-Projets®(CMP) to work on 3D-IC prototype design and test. This dissertation is one of the first endeavours into 3D integration within the Canadian university system.

1.3 Tezzaron 3D-IC Technology Description

The Tezzaron 3D-IC technique bonds two silicon dies face-to-face with a Cu-to-Cu thermo-compression process (referred to as a FaStack®process) as shown in Fig. 1.9. The two dies are named WTOP and WBOTTOM by Tezzaron. Each die or tier has six layers of metal and the ability to integrate thru-silicon vias or TSVs from metal one to the top/bottom of the die where an additional metal layer may be formed. The WTOP tier contains this additional backside metal layer, wheres the WBOTTOM tier does not. This backside metal layer is used to connect signals from within to the chip's I/O. Also seen in the figure, are many TSVs in the WBOTTOM tier. These TSVs are essentially left unconnected and is a by-product of the Tezzaron 3D-IC technique at this time. Future versions of the technology may include a backside metal layer on the WBOTTOM tier. Signals in the WBOTTOM tier will have to be routed through metal layer 6, which is electrically connected to metal layer 6 of the WTOP tier and onwards through out the structure.

1.4 Test Challenges

Similar to the conventional single-die IC test, 3D-IC testing should be performed at both the wafer level and after the IC is package. However, there are many more manufacturing steps for 3D-IC, like die stacking and TSV bonding, which requires more tests at the wafer level. Moreover, wafer testing is more challenging than a conventional single-die IC test for the following reasons:

- The probe nowadays can not handle the finer pitch and dimensions of TSV tips.
- The scrub marks left by the probe technology could potentially cause problems for the bonding step.
- Probe needle movement may results in crashes into the various die stacks.

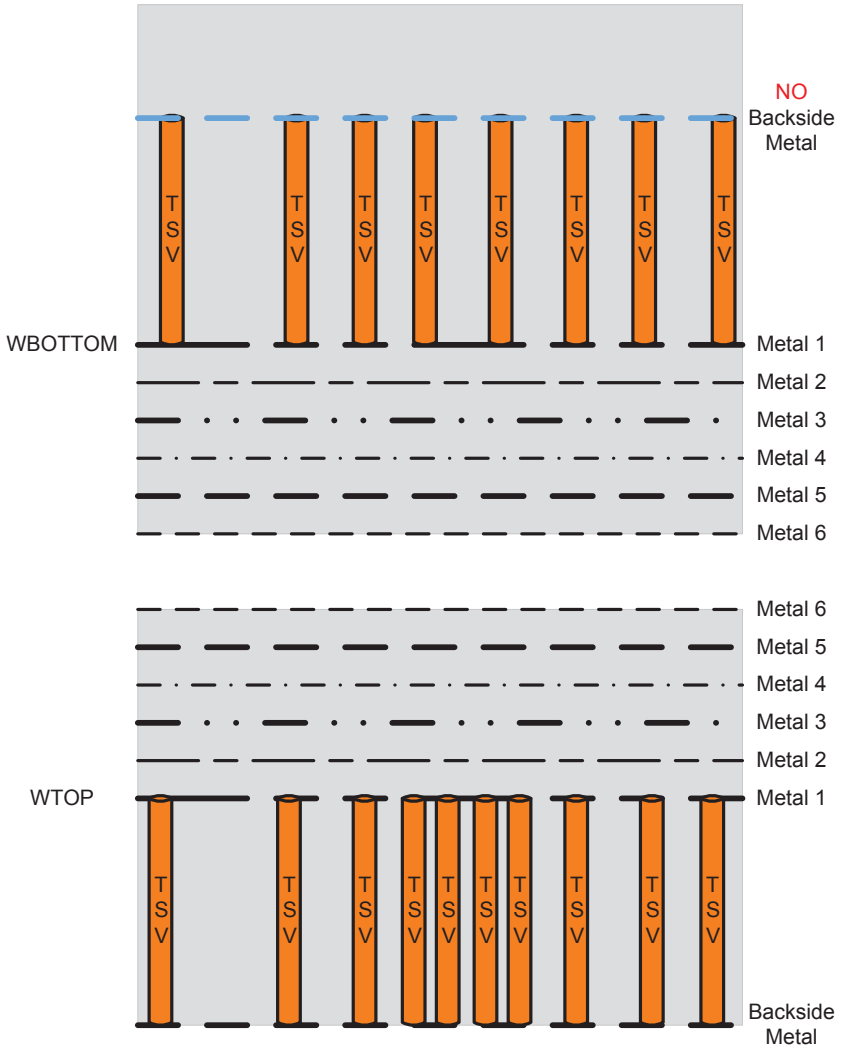


Fig. 1.9 Illustrating The Metal Layers and TSVS in the WTOP and WBOTTOM tiers of the Teazzaron 3D-IC technology

Also, a 3D-IC process introduces new intra-die defects into the package part on account of wafer thinning or die bonding. Thermal or heating effects are another sources of defects. Mechanical stress can also served as a source of new defects.

The thermo-mechanical reliability of TSV structure has been studied in literatures[2] [3] [4] [5]. Because of the coefficients of thermal expansion (CTE) between different TSV filled materials, copper (Cu) and silicon substrate, the thermo-mechanical stress is induced in the fabrication process. This can affect the device performance or even cause device breakdown. Thus, we need to figure out ways reduce the probing requirements but at the same time provide probe access to 3D-IC chips. The following are the testing issues raised by a 3D-IC technology:

- Is the interconnect TSVs reliable?
- How to probe inside the die stacks?
- Where is the test access? Is primary I/O sufficient?
- How to de-bug and isolate faults?

It is the objective of this dissertation to consider the above questions and identify a possible contender to the conventional wafer probe approach.

1.5 Thesis Overview

This thesis began with an introduction to 3D-IC technology where through-silicon vias and the 3D process was described. Some technology details for the Tezzaron 3D process was also provided in this chapter.

Chapter 2 introduces some modern measurement techniques for characterizing the signal integrity of a TSV in a 3D CMOS process. This will include measurements of its end-to-end series resistance and its corresponding capacitance-to-ground. A frequency-based direct capacitance measurement approach and a charge-based capacitance measurement will be described.

Chapter 3 discusses the DFT techniques used to capture and transfer the information captured by the embedded instruments described in Chapter 2. This chapter will describe a DFT technique that is compatible with the JTAG test bus standard but optimized for a 3D-IC configuration.

Chapter 4 presents the physical details pertaining to the design of the 3D chip made from the Tezzaron technology.

Chapter 5 describes the experimental setup for testing the prototype 3D-chip. This chapter should have provided experimental results as well, but unfortunately, due to manufacturing delays, the chip has not yet returned from fabrication.

Chapter 6 provides the thesis conclusions and some ideas for the future work.

Chapter 2

TSV Characterization

This chapter will introduce some modern measurement techniques for characterizing the signal integrity of a TSV in a 3D CMOS process. This will include measurements of its end-to-end series resistance and its corresponding capacitance-to-ground. In order to control this capacitance, the TSV in question will be surrounded by two separate TSV that are ground at one end as shown in Fig. 2.1. A frequency-based direct capacitance measurement approach and a charge-based capacitance measurement will be described. Looking at the bigger picture, these measurement techniques will be incorporated into a design-for-test (DFT) strategy that attempts to standardize the measurement interface between the IC and its test equipment. We shall delay any detail discussion of the DFT approach until Chapter 3. Here we will focus exclusively on an embedded resistance and capacitance measurement technique.

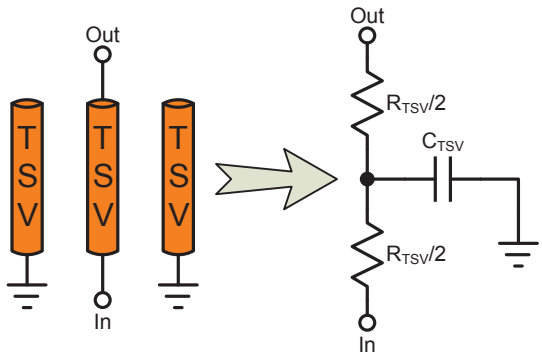


Fig. 2.1 TSV Lumped RC Model

2.1 TSV Resistance Measurement

According to [2] [6] [7] the series resistance is approximately 20 mΩ for a 5 μm diameter and 25 μm length TSV in the 3D CMOS process created by IMEC. Owing to this very small quantity, making a direct measurement of a single TSV resistance will be subject to many obstacles, such as the influence of other trace resistances, package parasitics, noise, etc. In order to increase this resistance, one hundred TSVs are connected in series, increasing the resistance a 100 fold. However, this resistance was reduced by about a factor of 5, as 5 TSVs were also connected in parallel in order to increase the current capability of the series-parallel circuit combination to about 20 mA. A single TSV from Terrazon Semiconductor has a current carrying limit of 2 mA. Collectively, the increased resistance combined with the higher current limit enables a more accurate measurement.

In order to eliminate the influence of any trace parasitic in series with an instrument off-chip, a Kelvin connection was made to the resistance network. This is shown in Fig. 2.2. Here a DC current is forced into the series circuit through IC pads A and D and the voltage drop across the resistor network is measured off-chip with a voltmeter through another set of internal traces connect to pads B and C. As the current through the voltmeter is very low, the effect of the trace resistance connected to pads B and C are insignificant and a true measurement of the voltage dropped across the resistor network can be made [8].

Assuming all the TSVs are identical, and we have P TSVs connected in parallel and S TSVs in series, a single TSV resistance R_{TSV} can be found from the following

$$R_{TSV} = \frac{V}{I} \cdot \frac{S}{P} \tag{2.1}$$

where I is the current forced into the resistor network by the current source and V is the voltage measured by the voltmeter. For the case we have defined here, with 5 TVSs in parallel and 100 components in series, the TSV resistance expression becomes

$$R_{TSV} = \frac{100}{5} \cdot \frac{V}{I} \tag{2.2}$$

2.2 Measuring Capacitor Mismatch

Measuring small valued capacitances directly on-chip, such as the capacitance shunting the TSV of Fig. 2.1, through an off-chip measurement is highly susceptible to stray capacitances

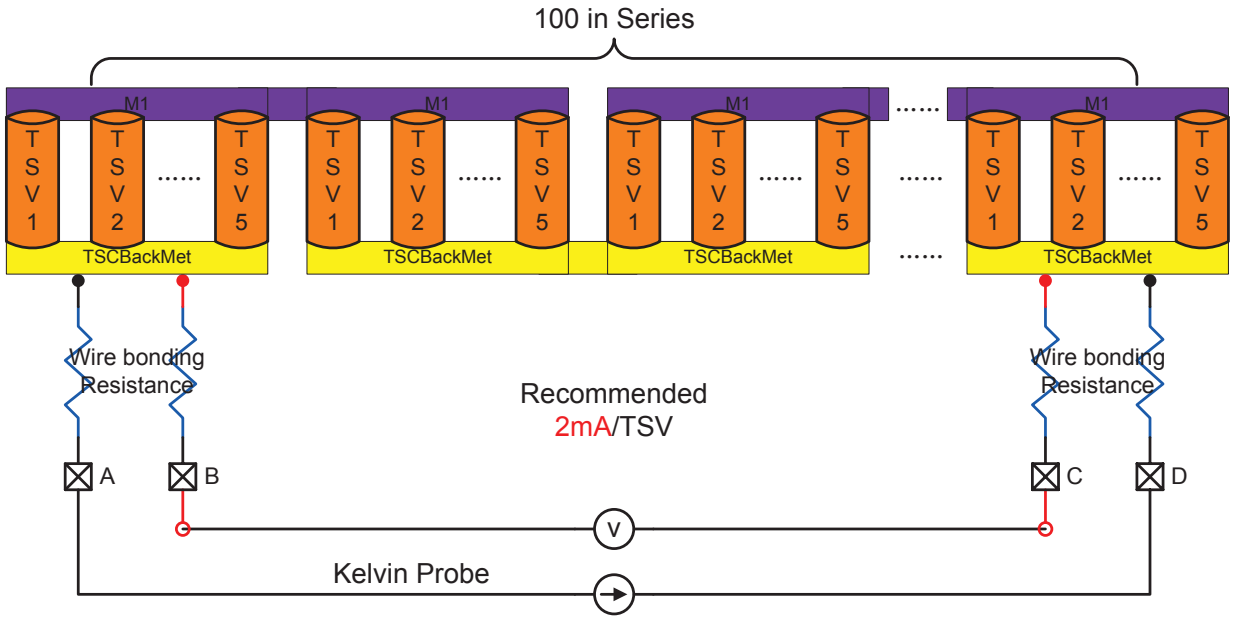


Fig. 2.2 Kelvin Probe for TSV Resistance Measurement

such as those seen at the bonding pads of the IC. Moreover, as these capacitances are quite small, on the order of 50 fF, they are generally beyond the measurement resolution of any bench-top capacitance meter. Before we tackle the measurement of the absolute value of some small parasitic capacitance, in this section we shall first review several methods used to measure the capacitance mismatch between two supposedly identical capacitors. One method is based on a voltage-based step method [9] applied to a capacitor network, another is based on two independent ramp signals applied to a similar capacitor network [9] [10] and a third method is based on measuring the frequency difference caused by the capacitance mismatch on the load of an oscillator [9].

2.2.1 Ramp-Based Capacitor Mismatch Measurement

Consider a test cell whereby two similar capacitors (C_1 and C_2) are connect in series. Nominally, $C_1 = C_2 = C$, but due to mismatches, they different slightly with magnitude $\Delta C = |C_1 - C_2|$. In addition, an amplifier with gain A is connected to the common point of the two capacitors as shown in Fig. 2.3. At each end of each capacitor is a voltage source. During the first phase, a voltage ramp V_X is applied to one end of the capacitor

network while the voltage source at the other end is held at ground potential. The next phase reverses the roles that each voltage source assumes and repeats the measurement at the output of the amplifier. The slopes of the corresponding output signals to these two separate excitations, denoted as S_1 and S_2, are measured. The relative mismatch between C_1 and C_2 can then be calculated according to

$$\frac{\Delta C}{C} = 2 \cdot \frac{S_1 - S_2}{S_1 + S_2} \tag{2.3}$$

One limitation of this approach is the noise from the amplifier. Measurements should be averaged multiple times for a more repeatable measurement of capacitor mismatch.

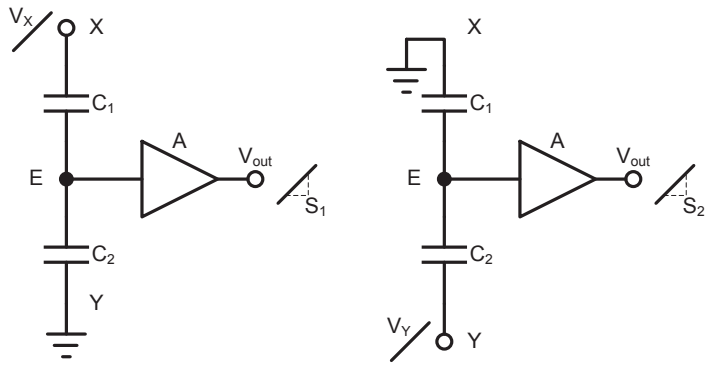


Fig. 2.3 Ramp-Based Capacitor Measurement Approach

2.2.2 Frequency-Based Capacitor Mismatch Measurement

In this measurement situation, a voltage-controlled oscillator (VCO) is loaded with two switched capacitive loads assumed to be matched. As the frequency of oscillation is a function of its load capacitance, relative differences in the frequency of oscillation will be proportional to relative capacitive mismatch according to

$$\frac{\Delta f_{out}}{f_{out}} = \alpha \cdot \frac{\Delta C}{C} \tag{2.4}$$

To use this method, the α term must be identified through some calibration procedure.

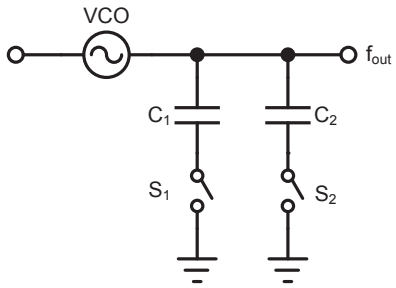


Fig. 2.4 Frequency-Based Capacitor Mismatch Measurement Approach

2.3 Frequency-Based TSV Capacitor Measurement

In this section we shall make use of the frequency-based mismatch measurement approach to measure the capacitance of a TSV. This approach was selected as the order of magnitude of the TSV capacitance is similar in magnitude to a capacitor mismatch. For the convenience of this dissertation, this method will be referred to as the frequency-based TSV capacitor measurement approach, or FBCM method for short. Two methods will be provided, one involving a single VCO and the other using two.

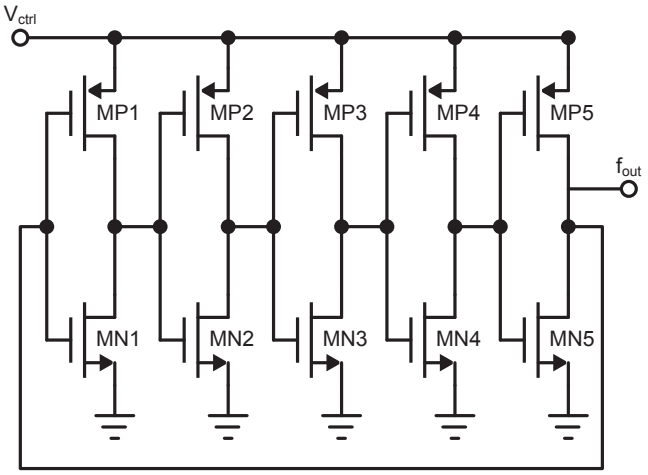


Fig. 2.5 Five-Stage VDD-Tuned Ring Oscillator

The VCO is to be constructed using the 5 stage VDD-tuned ring oscillator shown in Fig. 2.4. This oscillator provides a very small silicon footprint using a regular layout structure. This simple test circuit can reach frequencies as high as 2.5 GHz, which increases the sensitivity to very small capacitances. All like-transistor types (NMOS and PMOS) of the

ring oscillator are identical. A summary of the dimensions of these transistors can be seen listed in Table 2.1.

Table 2.1 Transistor Dimensions For A Five-Stage VDD-Tuned Ring Oscillator

	NMOS	PMOS
L (μm)	0.13	0.13
W (μm)	2	4

As the actual oscillation frequency of the ring oscillator will vary from chip-to-chip on account of process variations, the α parameter in Eqn. 2.4 must be found for each and every chip. To extract this value, two sets of frequency measurements will be made; one involving the VCO under no-load conditions and the other with the TSV attached. Under such conditions, we can write Eqn. 2.4 as

$$\frac{f_{out,TSV} - f_{out,noload}}{f_{out,noload}} = \alpha \cdot \frac{(C_{TSV} + C_{eff,parasitic}) - C_{eff,parasitic}}{C_{eff,parasitic}} \tag{2.5}$$

which reduces to

$$\frac{f_{out,TSV} - f_{out,noload}}{f_{out,noload}} = \alpha \cdot \frac{C_{TSV}}{C_{eff,parasitic}} \tag{2.6}$$

where $C_{eff,parasitic}$ correspond to the effective parasitic capacitance seen at the output of the VCO under no load conditions and C_{TSV} is the additional capacitance added when the TSV is connected to the VCO output. Parameters $f_{out,noload}$ and $f_{out,TSV}$ are the measured frequencies corresponding to the unloaded and load conditions, respectively. As the objective of the measurement is to find C_{TSV}, rearranging Eqn. 2.6 and isolating C_{TSV}, we find

$$C_{TSV} = \frac{C_{eff,parasitic}}{\alpha} \cdot \frac{f_{out,TSV} - f_{out,noload}}{f_{out,noload}} \tag{2.7}$$

As mentioned earlier, the α term is unknown and needs to be identified. Also, $C_{eff,parasitic}$ is also unknown and must be identified. A different approach is therefore required.

Going back to first principles, the frequency of oscillation f_{out} of the ring-oscillator can be described in general terms as a function of its load capacitance C_L, i.e.,

$$f_{out} = g(C_L) \tag{2.8}$$

Here the function $g()$ represents any nonlinear expression. The expression $f_{out} = g(C_L)$ can be illustrated using the graph shown in Fig. 2.6.

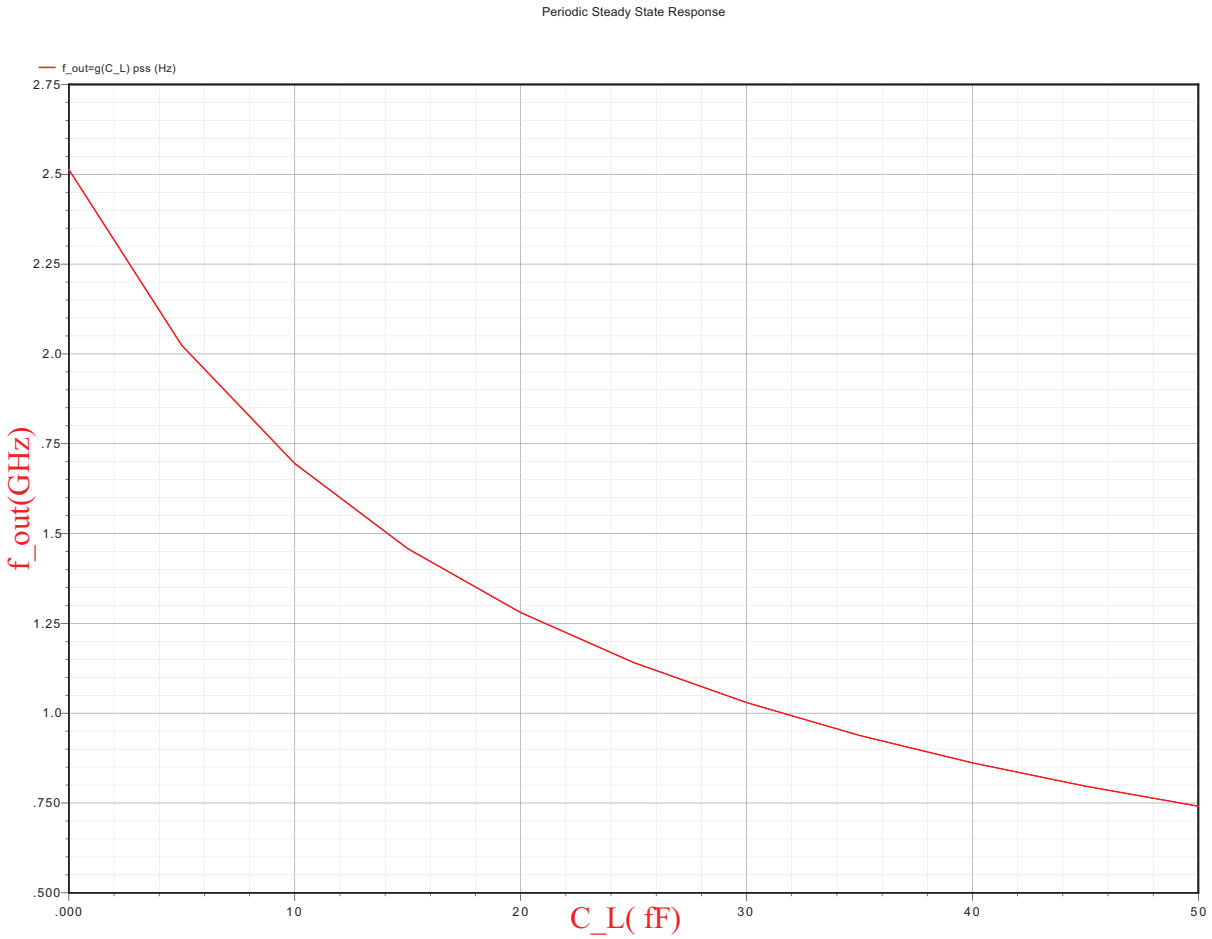


Fig. 2.6 VCO Output Frequency Vs. Load Capacitance $f_{out} = g(C_L)$ Nonlinear Curve

Now, assuming that this function $g()$ is known and invertible, the load capacitance on the ring oscillator can be determined according to

$$C_L = g^{-1}(f_{out}) \tag{2.9}$$

Operating the VCO under two different load conditions, i.e., $C_{L,1} = C_{eff,parasitic}$ and $C_{L,2} = C_{eff,parasitic} + C_{TSV}$ and measuring the corresponding oscillating frequencies, as previously

identified as $f_{out,noload}$ and $f_{out,TSV}$, allows one to identify the load capacitances as

$$C_{L,1} = g^{-1}(f_{out,noload}) \tag{2.10}$$

and

$$C_{L,2} = g^{-1}(f_{out,TSV}) \tag{2.11}$$

Subsequently, the unknown TSV capacitance C_{TSV} can then be found from the following expression

$$C_{TSV} = C_{L,2} - C_{L,1} \tag{2.12}$$

The above process is summarized in the flow chart shown in Fig. 2.7.

2.3.1 TSV Capacitor Formation

The TSV-under-test is surrounded with several dummy structures and all are connected directly to ground at each end as shown in Fig. 2.8. These grounded dummy structures isolate the TSV-under-test from the rest of the IC.

2.3.2 FBCM Using The Single-VCO Approach

In this measurement case, the FBCM is constructed with a single ring-oscillator VCO and several switchable loads, in much of the same fashion as that depicted in Fig. 2.4. Specifically, the VCO is realized as a cascade of five inverter sections, with each section loaded with a programmable-TSV load, as shown in Fig. 2.9. Here the programmable-TSV consists of a parallel combination of two floating TSVs surrounded by two other TSVs that can be connected to ground through the two analog switches.

Output Buffer Design

In order to drive the VCO signal directly off-chip for a frequency measurement, a voltage buffer was also constructed as shown in Fig. 2.10. The buffer consists of a cascade of three inverter stages with transistor dimensions seen listed in Table 2.2.

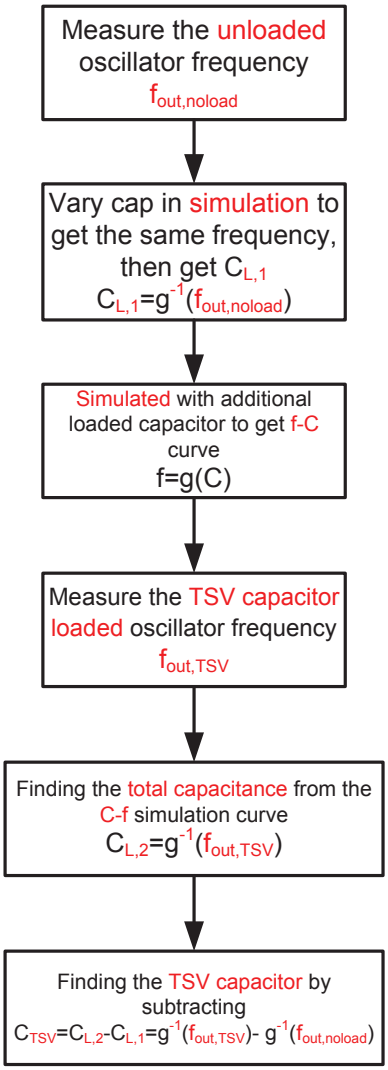


Fig. 2.7 A Flow Chart Illustrating The Measurement Approach For A Two-VCO Frequency-Based TSV Capacitor Cell

Table 2.2 Voltage Buffer Dimensions

	MN1	MN2	MN3	MP1	MP2	MP3
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13
W (μm)	1	4	16	2	8	32

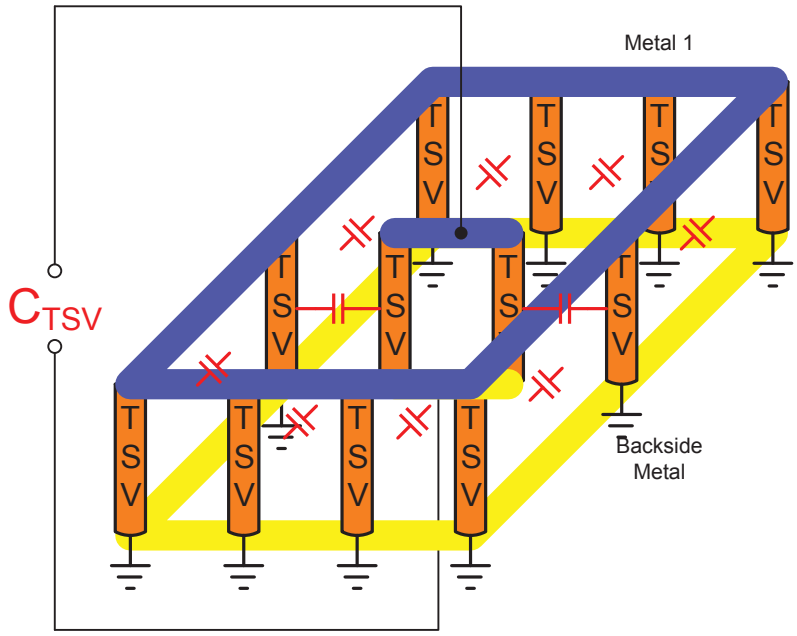


Fig. 2.8 TSV Formation With Grounded Dummy Structures

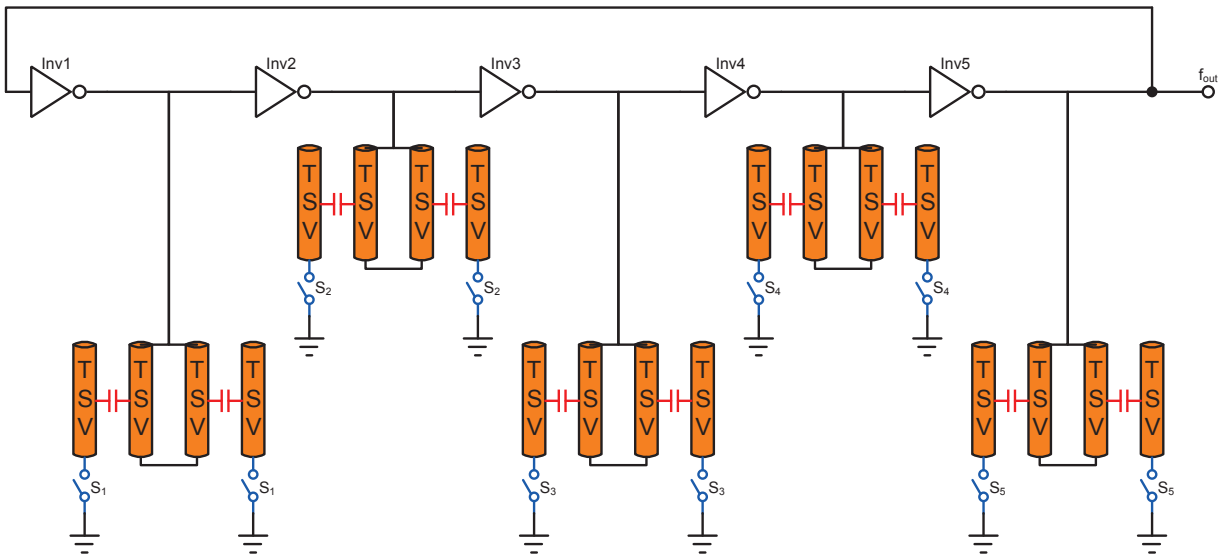


Fig. 2.9 A Single-VCO Frequency-Based TSV Capacitor Measurement Circuit with Programmable-TSV Loads

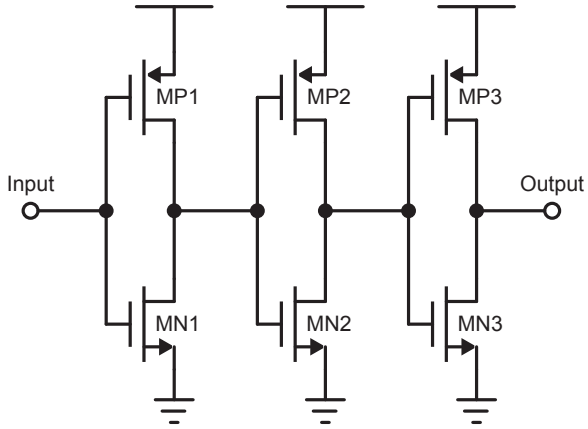


Fig. 2.10 A Voltage Buffer For Driving A Ring Oscillator Signal Off-Chip

Investigating The Impact Of The Analog Switches on FBCM Operation

The analog switch is constructed using a grounded TEE-connected arrangement of three transistors driven from a single control port as shown in Fig. 2.11. This particular switch introduces a small amount of parasitic capacitance to ground at each terminals of the switch. This capacitance is the sum of all the capacitance that appears at either the drain or source terminal of a single transistor to ground. Two different implementations of the switch were compared; one where the transistor width of all three transistors making up the TEE-switch was set to 10 μm and the other with widths of 90 μm each. As a point of reference, these two switch realizations are compared to the situation with the switch either removed in an open or infinite impedance state or closed in a zero impedance state. Using this ideal switch conditions as a point of reference allows one to compare the reduction in performance caused by a real switch.

The simulation results for the FBCM arrangement of Fig. 2.9 for the situation when the TSV switches are placed in the closed or ON state are shown in Fig. 2.12 for a 0 to 50 fF effective capacitance load on the FBCM. The load introduced by the TSV was simply modeled as an ideal capacitor. The control voltage V_{ctrl} is set to 1.4 V. Also shown in this plot are the simulation results for the ideal switch (i.e., replaced by a short circuit). The simulation is repeated but this time with the switches placed in the open or OFF state. The results of these simulations are shown in Fig. 2.14. To summarize these two sets of results, Tables 2.4 and 2.5 lists the output oscillation frequency for TSV capacitive loads of 10 fF and 40 fF, respectively.

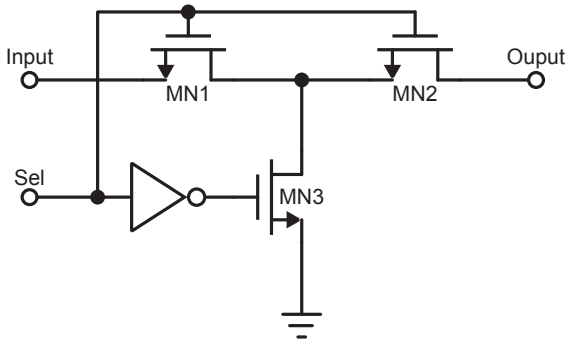


Fig. 2.11 Analog Switch

Table 2.3 Analog Switches Dimensions

(a) 10 μm Analog Switches

	MN1	MN2	MN3
L (μm)	0.13	0.13	0.13
W (μm)	10	10	2

(b) 90 μm Analog Switches

	MN1	MN2	MN3
L (μm)	0.13	0.13	0.13
W (μm)	90	90	20

From Fig. 2.12 to Fig. 2.15, the label $M0$ indicates the simulation with 10 fF load capacitance and 10 μm switch, the label $M1$ is with 40 fF load capacitance and 10 μm switch, the label $M2$ is with 10 fF load capacitance and 90 μm switch, the label $M3$ is with 40 fF load capacitance and 90 μm switch, the label $M4$ is with 10 fF load capacitance and without switch, and the label $M5$ is with 40 fF load capacitance and without switch.

Each set of results can also be compared to the ideal switch situation. As is evident from these two tables of results, there is a huge gap between output oscillation frequency of the ideal switch situation and that generated by either the 10 μm or 90 μm switch implementation. We also notice that the smaller switch realization (i.e., width of 10 μm) leads to a higher oscillation frequency. The reason for these differences can be attributed to the switch capacitive parasitics.

To better understand the reason for this oscillation loss, consider the small-signal model of the TEE-connected switch arrangement of Fig. 2.11 in Fig. 2.16. Here R_{sw} is the resistance of the switch and C_{gs}, C_{gd}, C_{sb}, and C_{db} represents the small-signal capacitances of the NMOS transistor. Also included is the small capacitance between the source and drain of the transistor C_{ds} created by an electric field under the channel region of the transistor. Also shown is the capacitance C_{TSV} that is used to represent the capacitance of the TSV. The output oscillation frequency f_{out} is inverse proportional to the total equivalent capacitances no matter the switch is ON or OFF. When the switch is *ON*, the output oscillation frequency f_{out} is determined by

$$1/f_{out} \propto ((C_{gs} + C_{sb}) + (C_{gd} + C_{db}) + C_{TSV}) \tag{2.13}$$

and while the switch is *OFF*,

$$1/f_{out} \propto ((C_{gs} + C_{sb}) + C_{ds}||((C_{gd} + C_{db}) + C_{TSV})) \tag{2.14}$$

As can be seen listed in Table 2.6, the various parasitic capacitance of the two switches is also in fF range, which is relatively close to our TSV capacitance value. Thus, the parasitic capacitance of switches cannot be ignored.

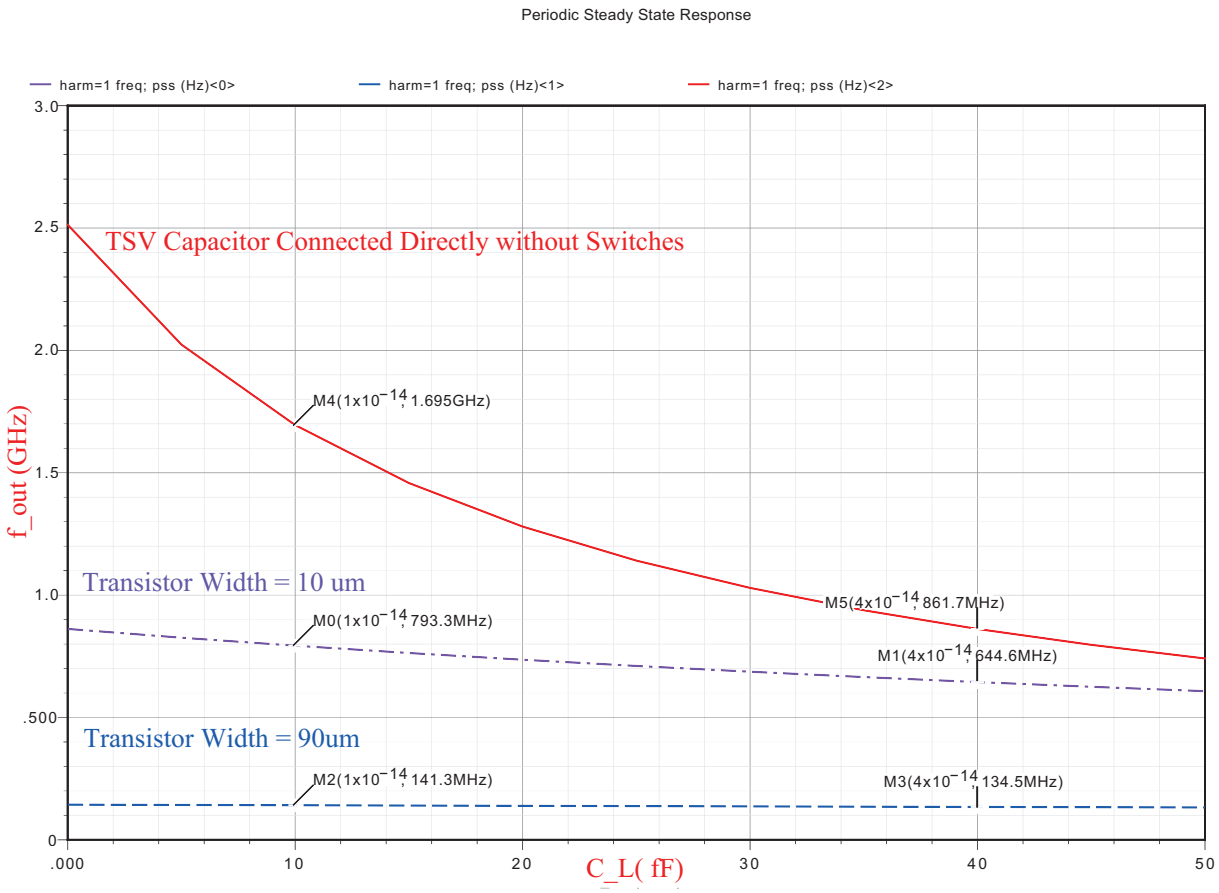


Fig. 2.12 Single-VCO-Based with Switches In ON State Comparison

Table 2.4 Ring Oscillator Output Frequency With Switches In The ON State

Frequency (Hz)	10μm Switch	90μm Switch	NO Switch
$C_{TSV} = 10fF$	793.3 MHz	141.3 MHz	1.695 GHz
$C_{TSV} = 40fF$	644.6 MHz	134.5 MHz	861.7 MHz

Table 2.5 Ring Oscillator Output Frequency With Switches In The OFF State

Frequency (Hz)	10μm Switch	90μm Switch	NO Switch
$C_{TSV} = 10fF$	1.867 GHz	730.1 MHz	2.513 GHz
$C_{TSV} = 40fF$	1.867 GHz	730.1 MHz	2.513 GHz

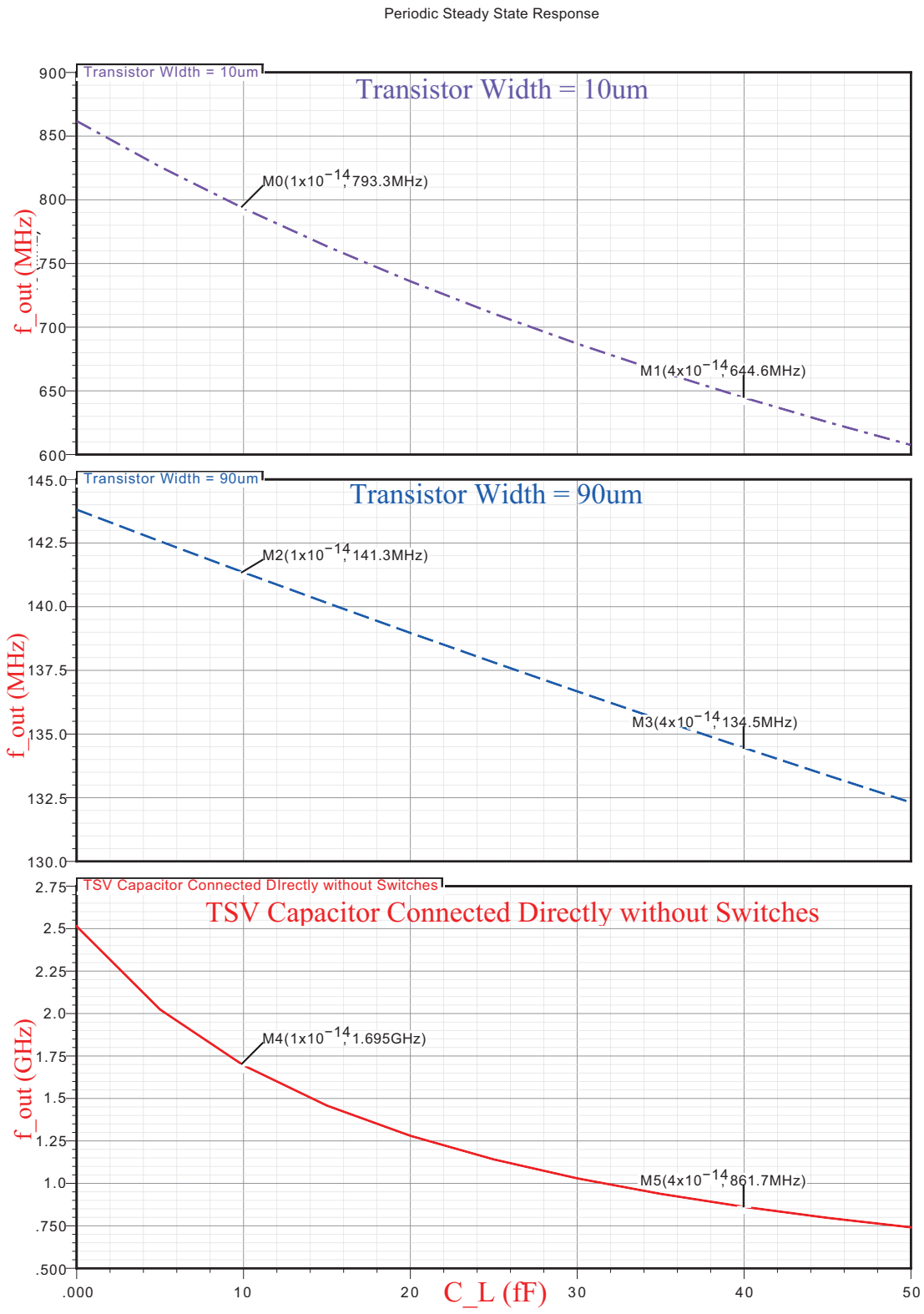


Fig. 2.13 Single-VCO-Based with Switches In ON State Comparison Details

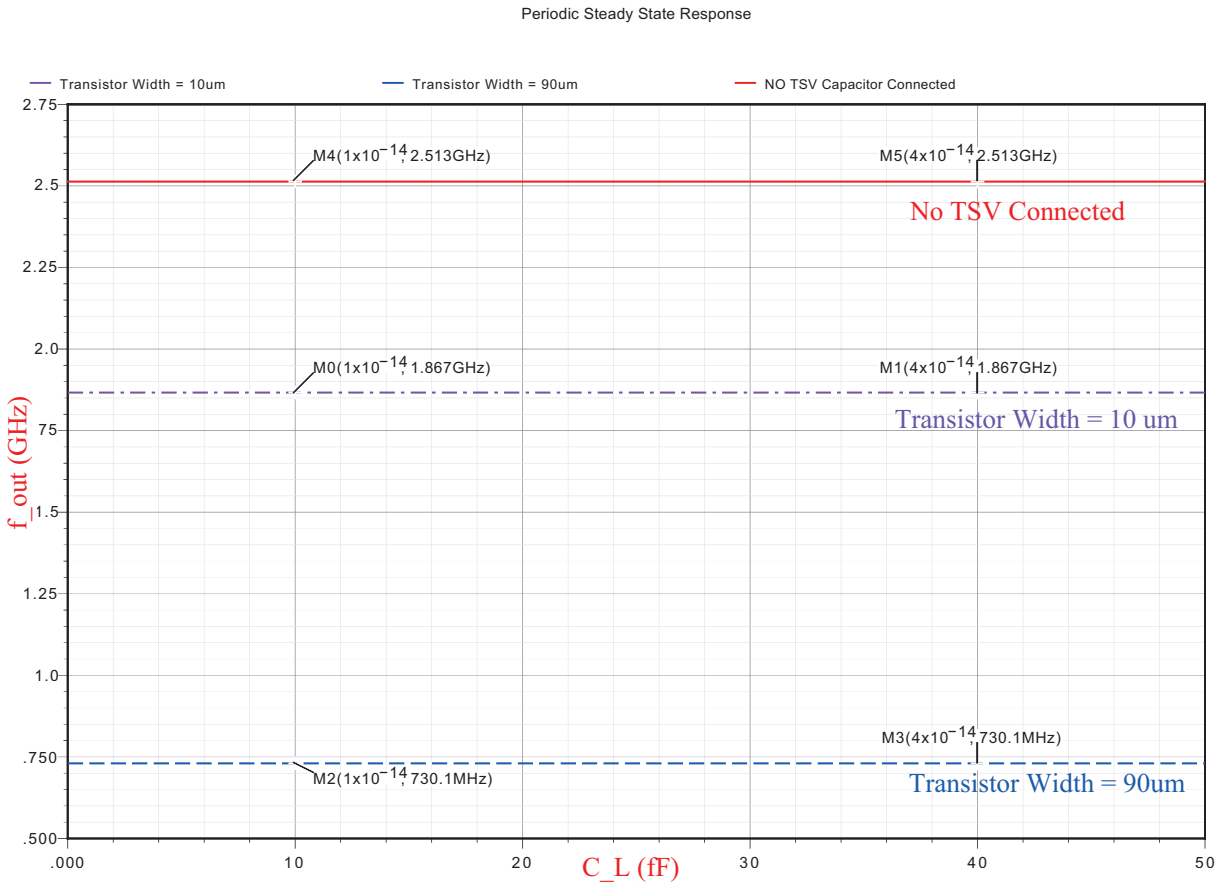


Fig. 2.14 Single-VCO-Based with Switches In OFF State Comparison

Table 2.6 NMOS TEE-Switch Parasitics

Parasitics Capacitance	ON 10μm Switch	ON 90μm Switch	OFF 10μm Switch	OFF 90μm Switch
C_{gs}	7.049 fF	63.46 fF	3.501 fF	31.51 fF
C_{sb}	387.6 aF	3.492 fF	1.769 fF	16.04 aF
C_{gd}	7.411 fF	66.73 fF	4.255 fF	38.30 fF
C_{db}	387.6 aF	3.492 fF	2.651 fF	24.02 aF
C_{ds}	2.446 fF	22.04 fF	391.2 zF	3.545 aF
C_{sd}	1.792 fF	16.13 fF	10.99 aF	99.60 aF

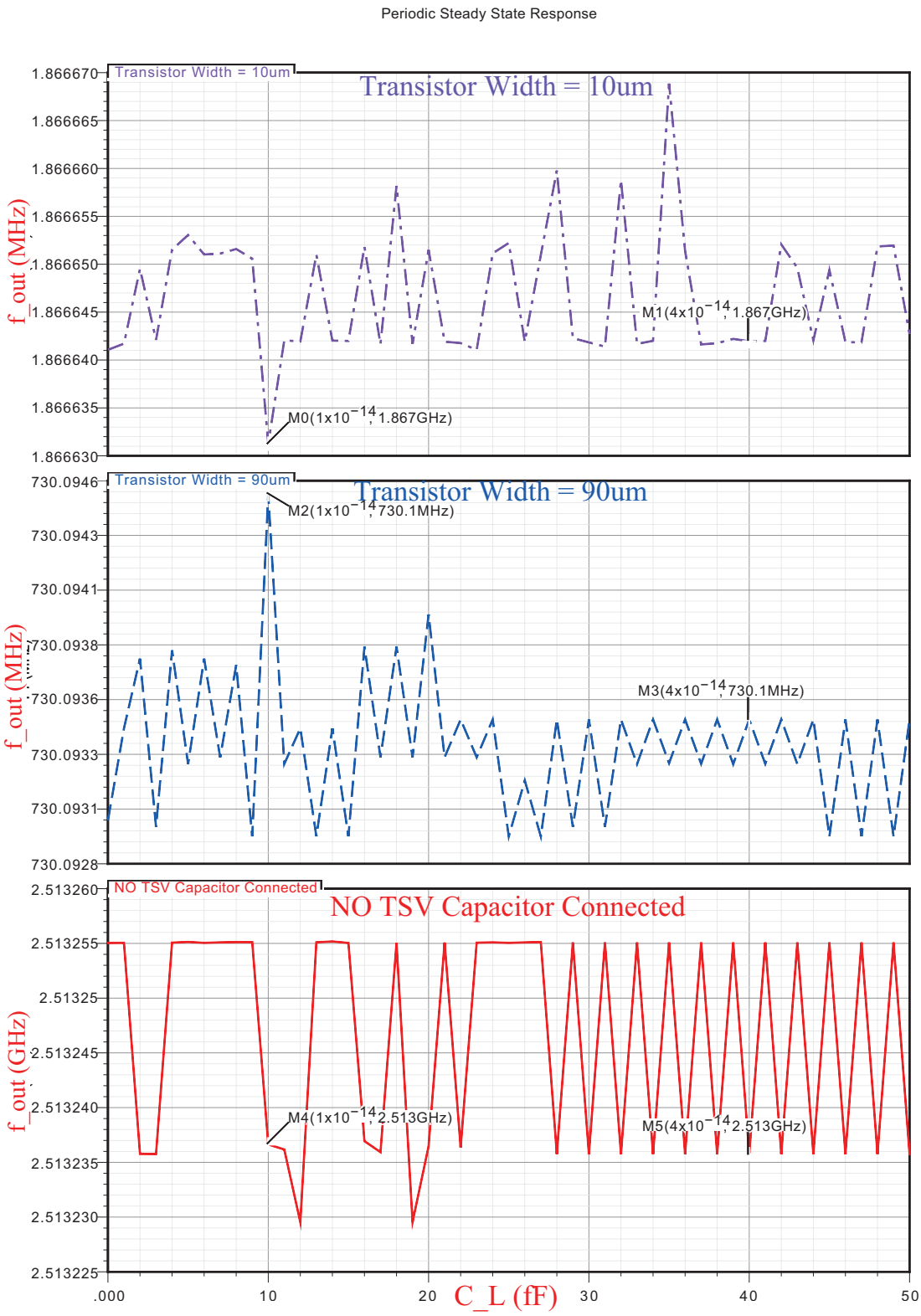


Fig. 2.15 Single-VCO-Based with Switches In OFF State Comparison Details

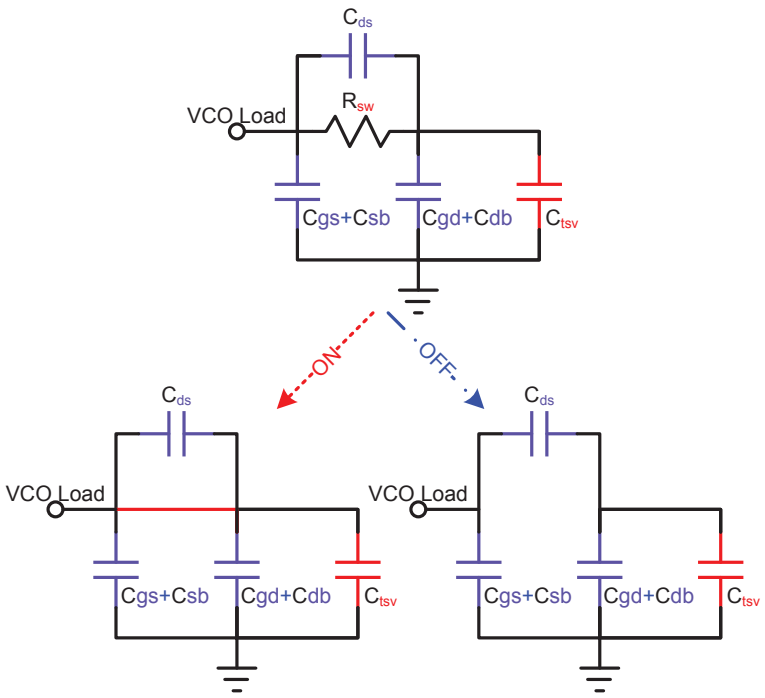


Fig. 2.16 Parasitics Analysis Of The TEE-Connected Switch

2.3.3 FBCM Using The Two-VCO Approach

An important limitation of the single or one VCO FBCM implementation method of the previous subsection is the dependence of the oscillation frequency on the switch parasitics and, in turn, the TSV capacitance measurement. In this section, a second approach is provided that is based on a two VCO implementation. Such an implementation provides a higher measurement resolution than the single or one VCO approach and solves the parasitic dependence problem. Fig. 2.17 shows the schematic diagram for the two VCO FBCM measurement approach. On the top part of the figure is a 5-stage ring oscillator with no additional load. On the bottom part is the same 5-stage ring oscillator but loaded with TSVs without the aid of analog switches. This particular arrangement eliminates the analog switches altogether and with it their corresponding parasitic problem. In normal operation the unload VCO will oscillate with frequency $f_{out,noload}$ and the TSV-loaded VCO will oscillate with frequency $f_{out,TSV}$. Under ideal conditions, the TSV capacitance would be found using the exact same formula as seen in Eqn. 2.7. In practice, however, transistor mismatches between the loaded and unloaded ring oscillator will introduce errors in the

TSV measurement. It is therefore imperative that the layout of the two VCOs is done in a careful and symmetric manner so as to minimize these types of errors. Using large sized transistors also helps to reduce these mismatches.

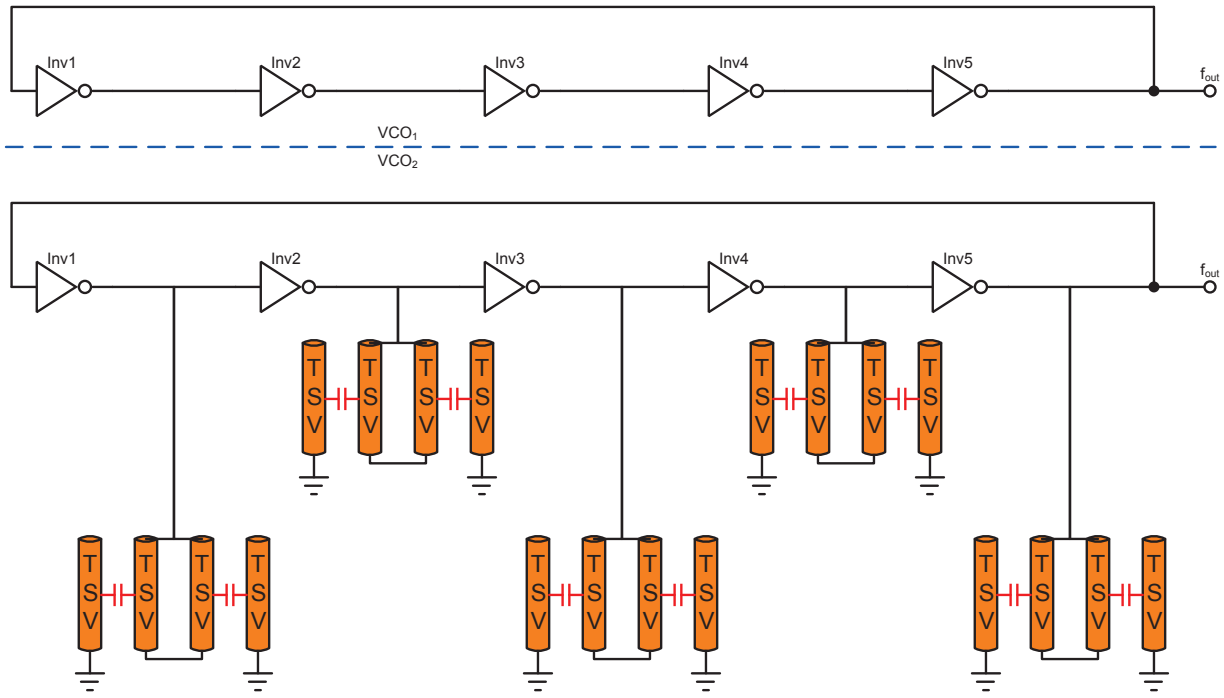


Fig. 2.17 Two VCOs Frequency-Based TSV Capacitor Measurement Approach Without Analog Switches

A comparison of the single- or one-VCO approach versus the two-VCO approach can be seen listed Table 2.7. While each approach has its pros and cons, it is believed by the author that the two-VCO approach is better suited to a TSV capacitance measurement and will be the method of choice as a frequency-based measurement approach.

2.3.4 External Access To Frequency-Based Capacitance Measurements

From Eqn. 2.7, we can see that two frequencies are required: $f_{out,noload}$ and $f_{out,TSV}$. If a frequency-to-digital converter (FDC) is used, then the frequency quantity will appear in the form of an integer value expressed in general terms as

$$M = \beta \cdot f \tag{2.15}$$

Table 2.7 A Comparison Summary Of The One and Two VCO FBCM Implementations

	Pros	Cons
One-VCO FBCM	• Single VCO, saving space and power.	• Parasitics R_{sw} and C_{sw} introduce measurement error. • Loss of measurement resolution when $C_{sw} \approx C_{TSV}$.
Two-VCO FBCM	• No switch parasitics to care about. • Higher sensitivity to the capacitor variation.	• Mismatch between VCOs introduce the measurement error. • Noise from one VCO couples into the other.

where β represents the gain of the FDC. Since the digital count M_{out} is linear with respect to output frequency f_{out} as it is derived directly from a counting procedure, M_{out} will have the same nonlinearity with respect to the load capacitance C_L except with a different gain factor, β. By combining Eqn. 2.8 with Eqn. 2.15, we can write

$$M_{out} = \beta \cdot g(C_L) \tag{2.16}$$

By defining a new nonlinear function $G(x) = \beta \cdot g(x)$, Eqn. 2.12 can be written as

$$C_{TSV} = G^{-1}(M_{out,TSV}) - G^{-1}(M_{out,noload}) \tag{2.17}$$

The relation between the frequency count M_{out} and the load capacitance C_L is illustrated in Fig. 2.18. Notice that the gain of the FDC does not appear in the computation of the TSV capacitance quantity.

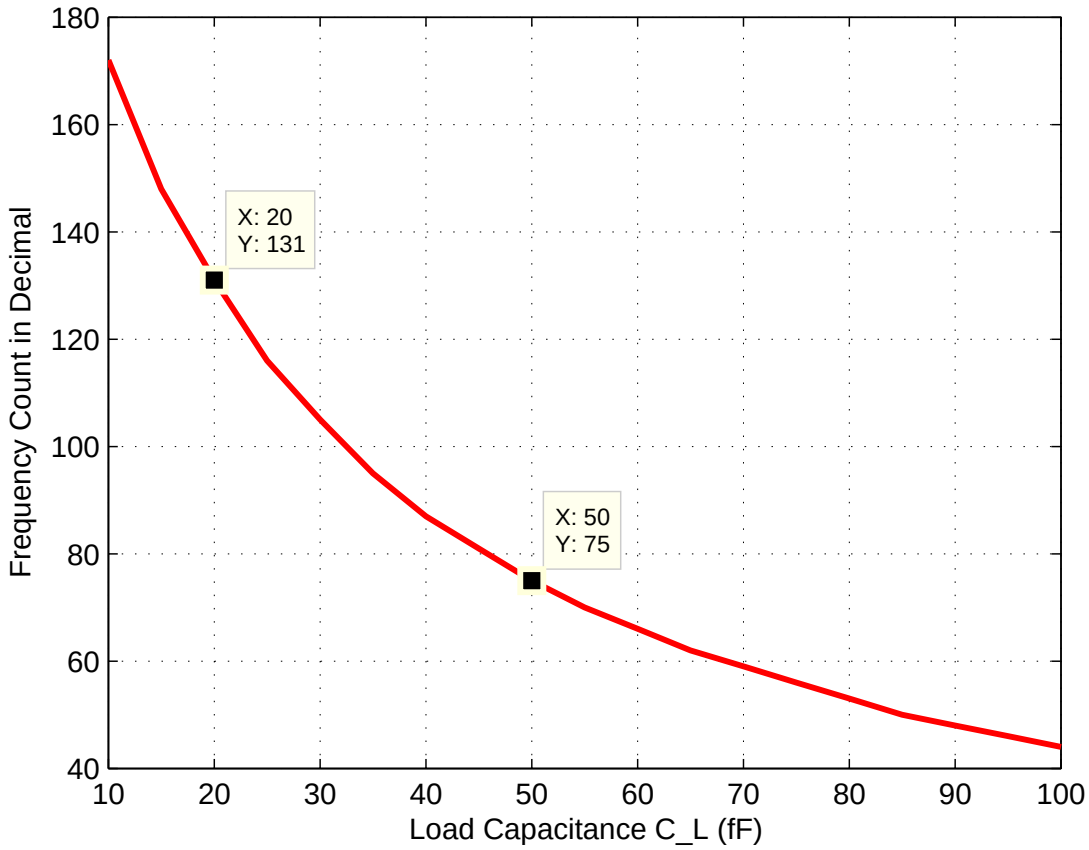


Fig. 2.18 Frequency Count VS Load Capacitance

Frequency-To-Digital Converter Principle

The FDC shown in Fig. 2.19 consists of three parts: frequency divider, counter and reset pulse signal generator. The FDC takes as input a square wave signal from the VCO. This signal is first divided down in frequency using the divide-by-N frequency divider circuit and directed to the clock input of the counter. A second input consisting of the enable signal (START COUNT) initiates the counting cycle. The count completes when the reset pulse is generated (STOP COUNT). The pulse generator is clocked using an off-chip reference signal with frequency f_{ref}.

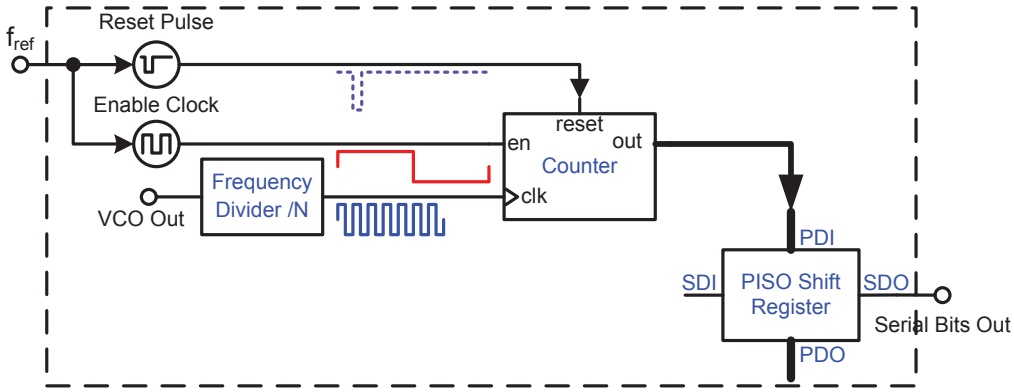


Fig. 2.19 Frequency-To-Digital Converter With External Access

The frequency of the incoming VCO signal is then determined from the count value denoted as M according to

$$f_{vco} = 2 \cdot N \cdot M \cdot f_{ref} \tag{2.18}$$

This phase of operation is referred to as the *Counting Phase*. The next phase of operation is called the *Shifting-Out Phase*, whereby the digital count value is passed to the user off-chip. This is explained next.

To further improve the on-chip test, a parallel-in-serial-out (PISO) register associate with the frequency counter is included. The serial output requires only a single pin, saving pins for other chip functions. The PISO register is eight-bits wide and an additional eight-ones are added as the flag bits to indicate the start of a word count transmission.

The timing diagram corresponding to the FDC is illustrated in Fig. 2.20. From top to bottom, the first waveform represents the *Count-Number*, the next waveform represents

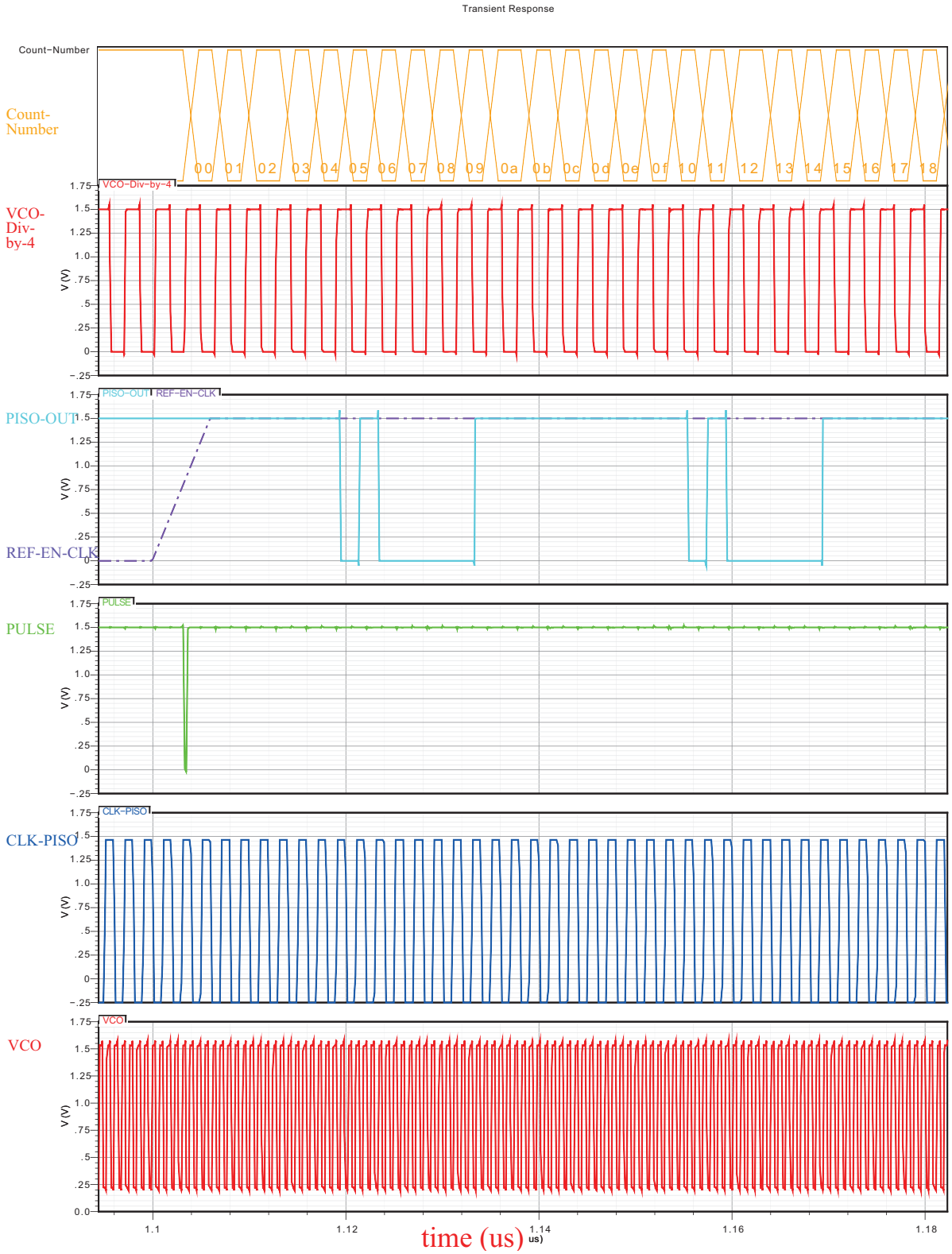


Fig. 2.20 FBCM Counter and PISO Output Waveform Details

the VCO output after the frequency divider *VCO-Div-by-4*, the third plot is for the shift register output signal *PISO-OUT* and the reference clock signal *REF-EN-CLK*, the forth waveform is for the pulse signal *PULSE*, the fifth plot is for the clock signal of PISO shift register *CLK-PISO* and the bottom waveform is for the VCO output signal *VCO*.

At the beginning of every conversion cycle, the *PULSE* signal resets the counter to a decimal zero value. The counter is clocked by divide-by-4 output and the counter is allowed to increment only when the reference clock *REF-EN-CLK* is set high. When the reference clock goes low, the frequency counter stop counting and the PISO register begins to shift out the counter bits with eight redundant ones (as seen in the waveform plot as *PISO-OUT*).

2.3.5 Example Simulation and Discussion

In this subsection, we are going to show the TSV capacitance extraction procedure using the two-VCO FBCM method through a Spectre simulation. Each VCO will be loaded with a 20 fF parasitic capacitance and the TSV capacitance will be made equal to 30 fF. The timing diagram corresponding to this simulation is shown in Fig.2.21 following the exact same signal format as the previous timing diagram. In this simulation, there are two full counting cycles, one for the unloaded VCO and the other for the TSV-loaded VCO. At the end of each count phase, the shifting-out phase is also shown.

Let us assume the frequency count of decimal 131 with the timing diagram of the FDC process shown in Fig. 2.21 is the measurement result corresponding to an unloaded TSV capacitance. The TSV capacitance calculation is then performed according to the flow chart of Fig. 2.7.

1. Find the Count-C_L plot from simulation. (This is shown in Fig. 2.22 as C_L-Count for ease of use)

2. Determine the *unloaded* oscillation frequency output count. In our case here, the top plot of Fig. 2.21 obtain from simulation indicates a count of '83' in HEX or 131 in decimal.)

3. Using the Count-C_L curve of Fig. 2.22, for a decimal count of 131, $C_{eff,parasitic}$ is 20 fF.

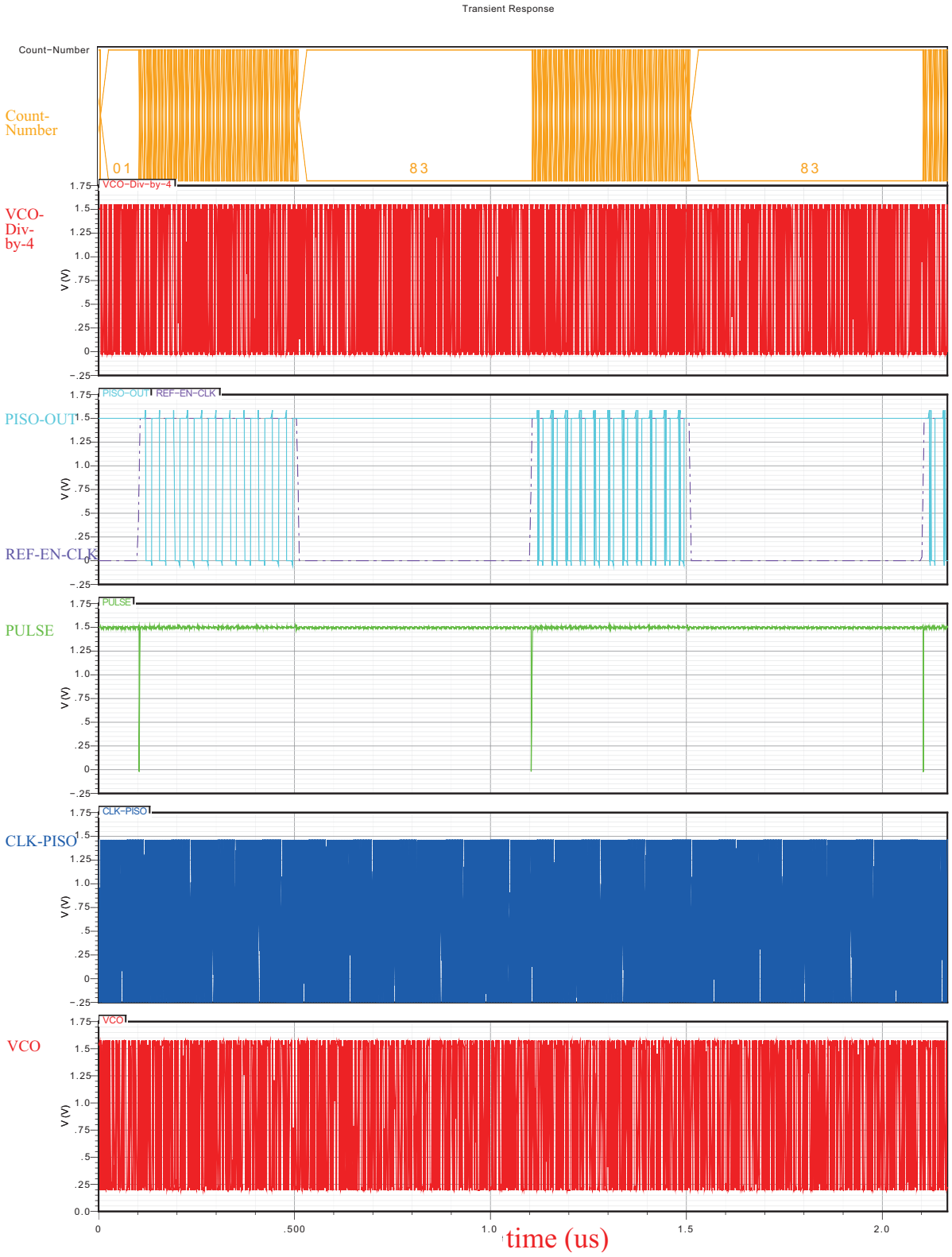


Fig. 2.21 FBCM Counter and PISO Output Two Full Cycle Waveform

4. Next, repeat the above steps but this time make reference to the TSV-loaded VCO. For the simulation situation of Fig. 2.23, we observe the *loaded* oscillation frequency output count as a HEX value of 4b or a decimal value of 75.

5. Using the Count-C_L curve of Fig. 2.22, for a decimal count of 75, C_{total} is 50 fF.

6. The TSV capacitance is simply the difference between C_{total} and $C_{eff,parasitic}$ leading to C_{TSV}=30 fF.

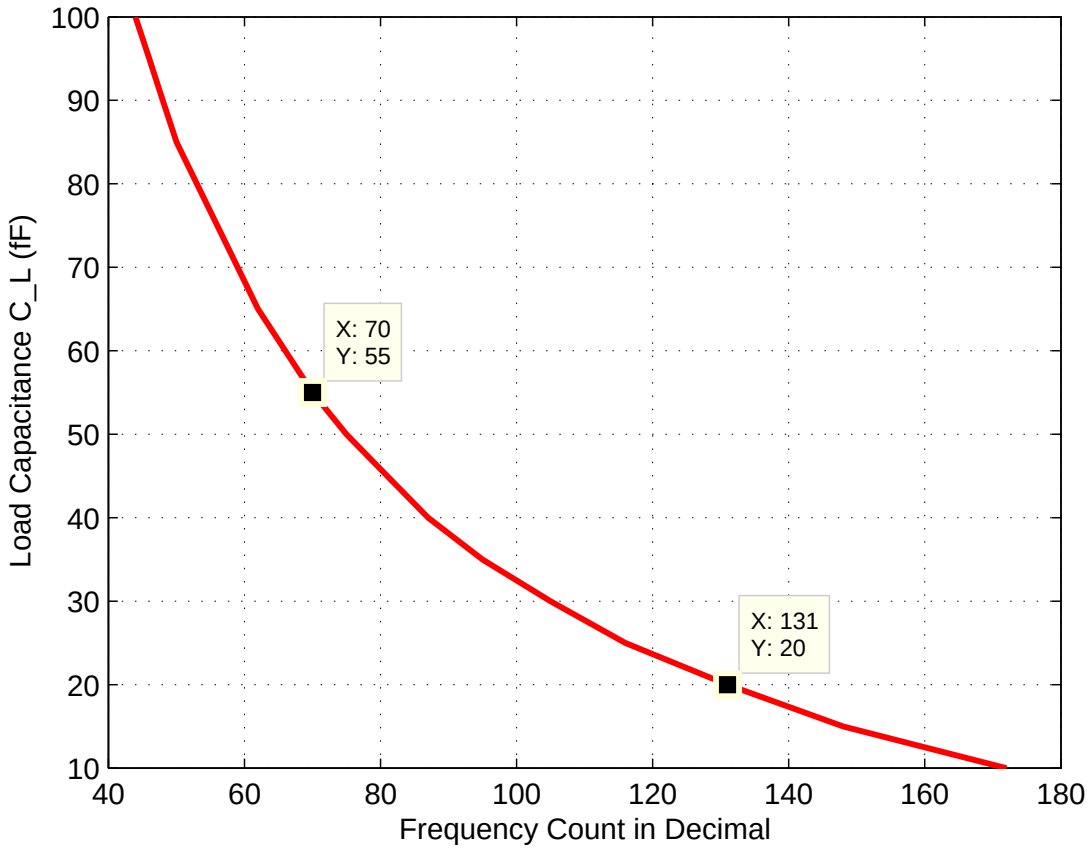


Fig. 2.22 Load Capacitance VS Frequency Count

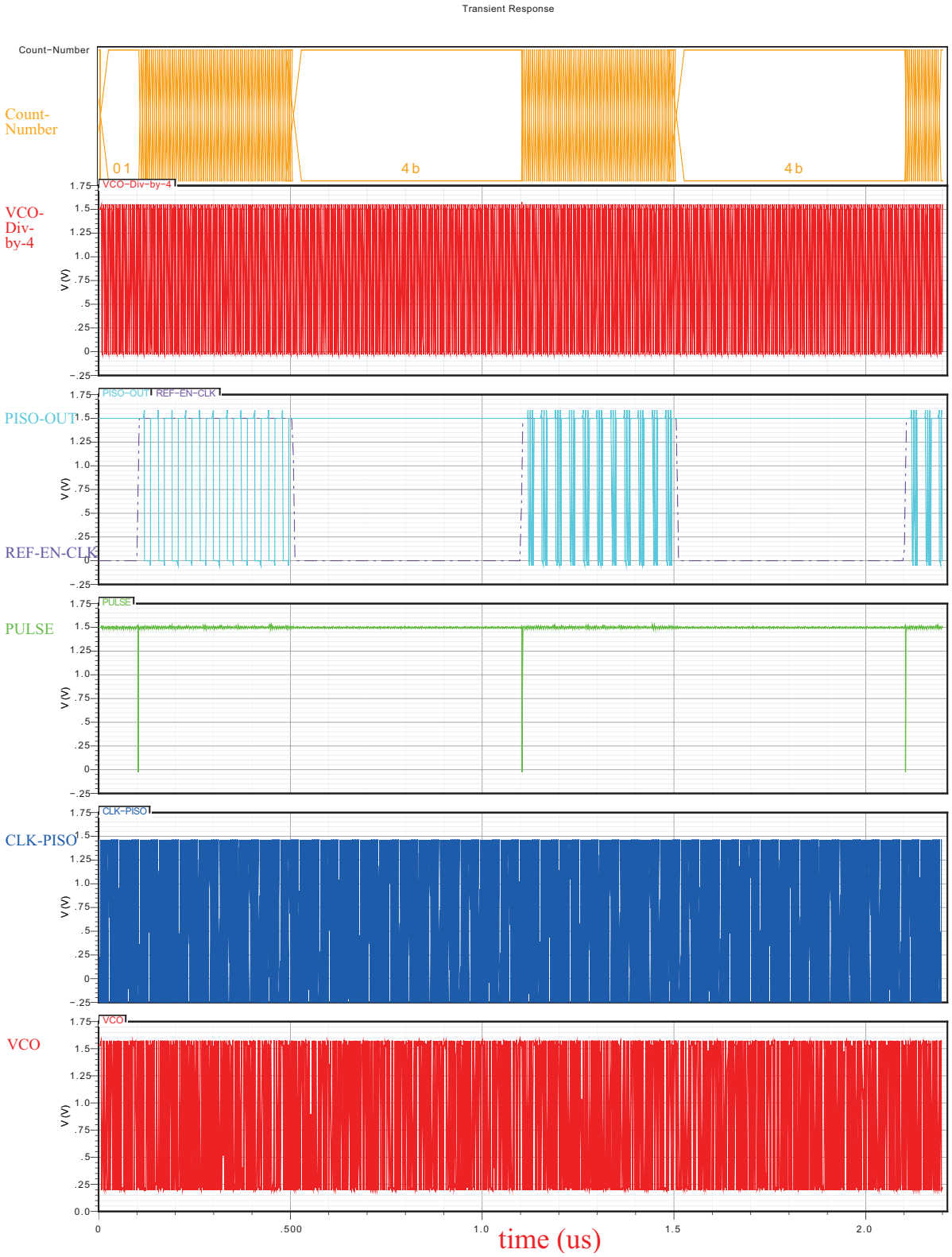


Fig. 2.23 Timing Diagram Corresponding To An Unloaded And Loaded VCO Output.

2.4 Charge-Based TSV Capacitor Measurement

The charge-based capacitor measurement method (CBCM) was first proposed in [11][12]. As showed in Fig. 2.24, there are a pair of NMOS and PMOS transistors connected as a matched pair of *pseudo* inverters. The gate of each inverter is driven with separate inputs. The right inverter is loaded by TSV capacitor, while other inverter does not include the TSV capacitance but includes its parasitic capacitance C_P and any capacitance included with the metal routing associated with the TSV capacitance, denoted by C_{Metal}, as illustrated in Fig. 2.8. This cell wil act as the reference cell.

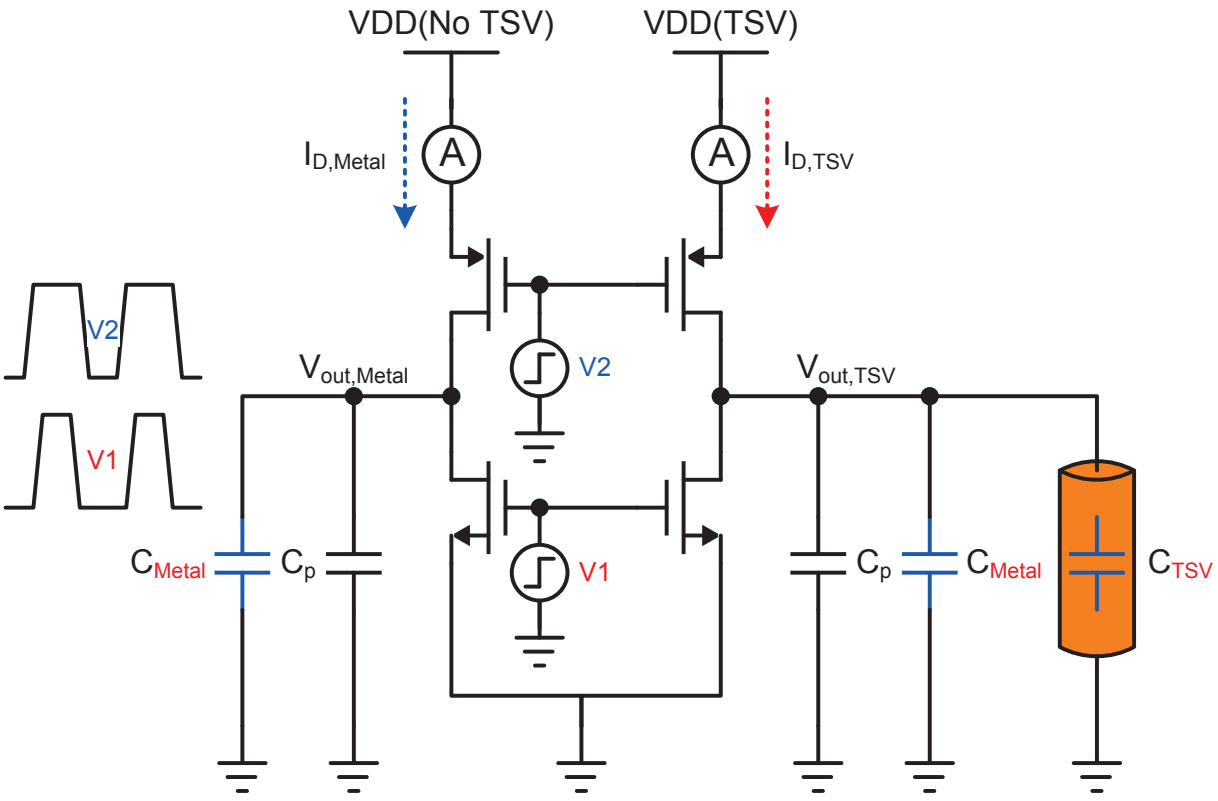


Fig. 2.24 Charge-Based Capacitance Measurement

2.4.1 CBCM Principle

Voltage signals V_1 and V_2 in Fig. 2.24 are two independent control signals used to ensure the NMOS or PMOS transistors are conducting at non-overlapping times. Once the PMOS

transistor turns on, charge flow from VDD into the TSV capacitor to charge up the capacitor. The same amount of charge will then be discharged through the NMOS transistors to ground on the other half of the charging cycle. Driving the nodes associated with V_1 and V_2 guarantees separate charging and discharging processes for each of the load capacitors.

Precision ammeters, like the Keithley 2602/2400 Source Meter, are used to measure the charging currents of each inverter with nA measurement accuracy. The ammeter is connected in series between VDD and source of each PMOS transistors to capture the charging current (or between ground and source of NMOS transistors if a discharge current is to be measured).

The charging and discharging process of a capacitor could be characterized in gneral terms using a i-v relationship of a capacitor as

$$i(t) = C\frac{dv(t)}{dt} \tag{2.19}$$

By integrating equation 2.19 over the period of the charging or discharging cycle, we can write

$$I_{ave} = C \cdot VDD \cdot f \tag{2.20}$$

where I_{ave} is the average current over the whole cycle and f is the frequency of the charging and discharging process.

In the TSV capacitance measuring, we have TSV with associated metal layers connected on the right side combining to form a total capacitance C_1. While the metal layers without TSV connected on the left side is said to have a total capacitance C_2. Where each capacitor can be written as

$$C_1 = C_P + C_{Metal} + C_{TSV} \tag{2.21}$$

and

$$C_2 = C_P + C_{Metal} \tag{2.22}$$

With the same VDD and f, the capacitance of the TSV C_{TSV} can be found from the difference of C_1 and C_2, i.e.,

$$C_{TSV} = C_1 - C_2 = \frac{I_{D,TSV} - I_{D,Metal}}{VDD \cdot f} = \frac{I_{diff,ave}}{VDD \cdot f} \tag{2.23}$$

where $I_{diff,ave}$ is the difference of the average charging or discharging current of the two sides of the pseudo inverters. Eqn. 2.23 reveals the linear relationship between C_{TSV} and $I_{diff,ave}$. Getting slightly ahead of the reader, Fig. 2.25 illustrates a Spectre simulation of a specific case of the CBCM circuit where we see the average charing current is very much a linear function of the TSV capacitance.

For ease of use, we introduce the slope factor, k, according to

$$k = \frac{I_{diff,ave}}{f} \tag{2.24}$$

This term represents the slope of the $I_{diff,ave}$ vs f transfer characteristic for a specific supply voltage VDD. We shall make use of this parameter later on when extracting the TSV capacitance from a current measurement.

2.4.2 CBCM Method Circuit Design

In the CBCM method, the most critical issues are matching the pseudo inverters and ensuring non-overlapping control signals. We'll discuss these two issues one by one.

Pseudo Inverter Design

Since the current difference is very small and sensitive to the load capacitance at the output of each inverter, it is critical that the parasitic capacitance at each *pseudo* inverter output is well matched. By placing each inverter close to one another and using common-centroid layout, mismatches in the parasitics can be minimized.

Also, we recognize from Eqn. 2.20 that the average difference current is a linear function of frequency, f. Hence, a higher operating frequency will result in a larger current difference level, thereby improving the signal-to-noise ratio of any particular measurement. However, to operate at higher frequency (i.e., guarantee a fully charge and discharge process) we must make use of small-sized transistors. The dimensions of the transistors used in the design of the CBCM circuit are listed Table 2.8.

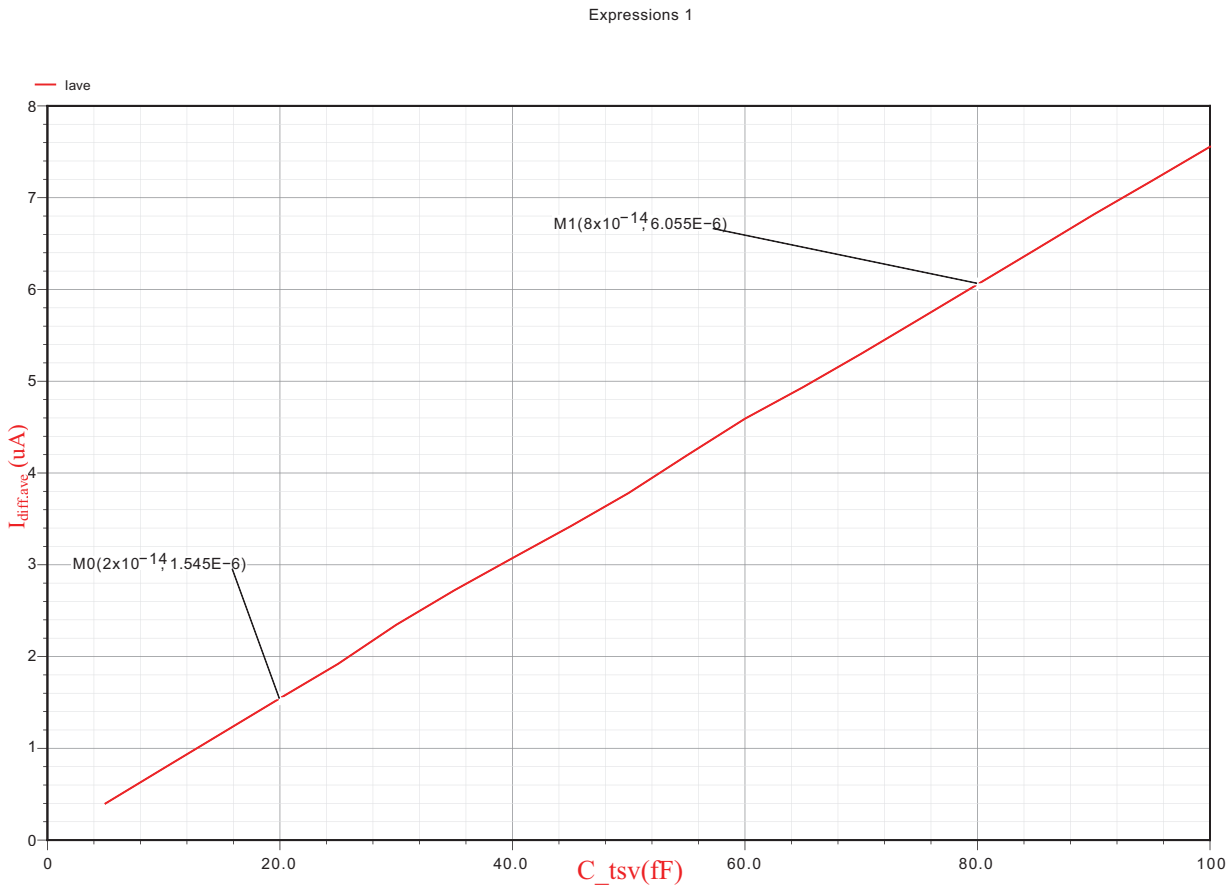


Fig. 2.25 Averaged Difference Current VS TSV Capacitance

Table 2.8 Transistor Dimensions Of Each Pseudo Inverter Circuit

	PMOS	NMOS
L (μm)	0.13	0.13
W (μm)	0.5	0.5

Non-Overlapping Control Signal Generator Design

The non-overlapping signal can be generated either on- or off-chip as mentioned in [11][12]. However, in order to get fast rising edges for better measurement accuracy, in this work, the non-overlapping control signal generator was implemented directly on chip. The schematic for this design is shown in Fig. 2.26. Here the inverter chains are used to introduce delays to create non-overlapping signals from the same reference signal. A Spectre simulation of the behaviour of this control signal generator subject to a 50 MHz input clock signal acting as the reference is shown in Fig. 2.27. The bottom waveform represents the input clock signal with a 0.5 ns rise and fall time and the top waveform represents the generated output non-overlapping signal $V1$ and $V2$. As is clearly evident from this plot, signals $V1$ and $V2$ do not overlap.

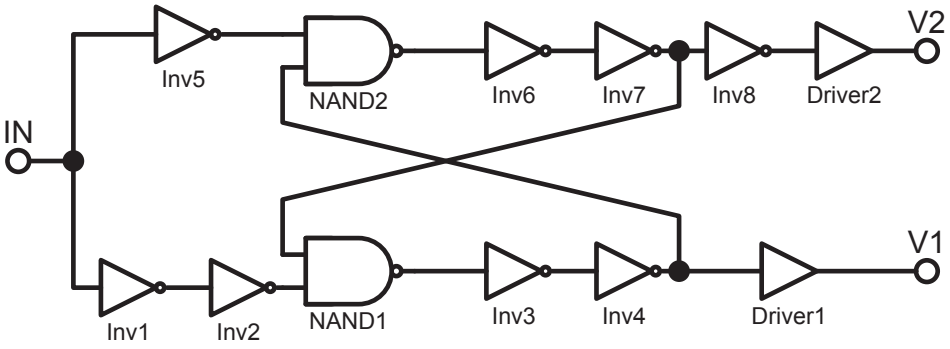


Fig. 2.26 Non-Overlapping Clock Signal Generator Schematic

2.4.3 Example Simulation and Discussion

By applying the non-overlapping waveform in Fig. 2.27 to the CBCM circuit of Fig. 2.24, we can measure the average difference current $I_{diff,ave}$. Under four separate supply voltage conditions, , i.e., 0.8 V, 1.0 V, 1.2 V and 1.4 V, the $I_{diff,ave}$ versus f was extracted through a Spectre simulation. The results are shown in Fig. 2.28. For each voltage condition, the TSV capacitance C_{TSV} can be derived directly from the slope of each curve. For instance, with $VDD = 1.4$ V, we find $I_{diff,ave} = 3.553\mu A$ at $f = 50MHz$, hence using Eqn. 2.24, we find

$$k = C_{TSV} \cdot VDD = \frac{I_{diff,ave}}{f} = 7.106e - 14 \tag{2.25}$$

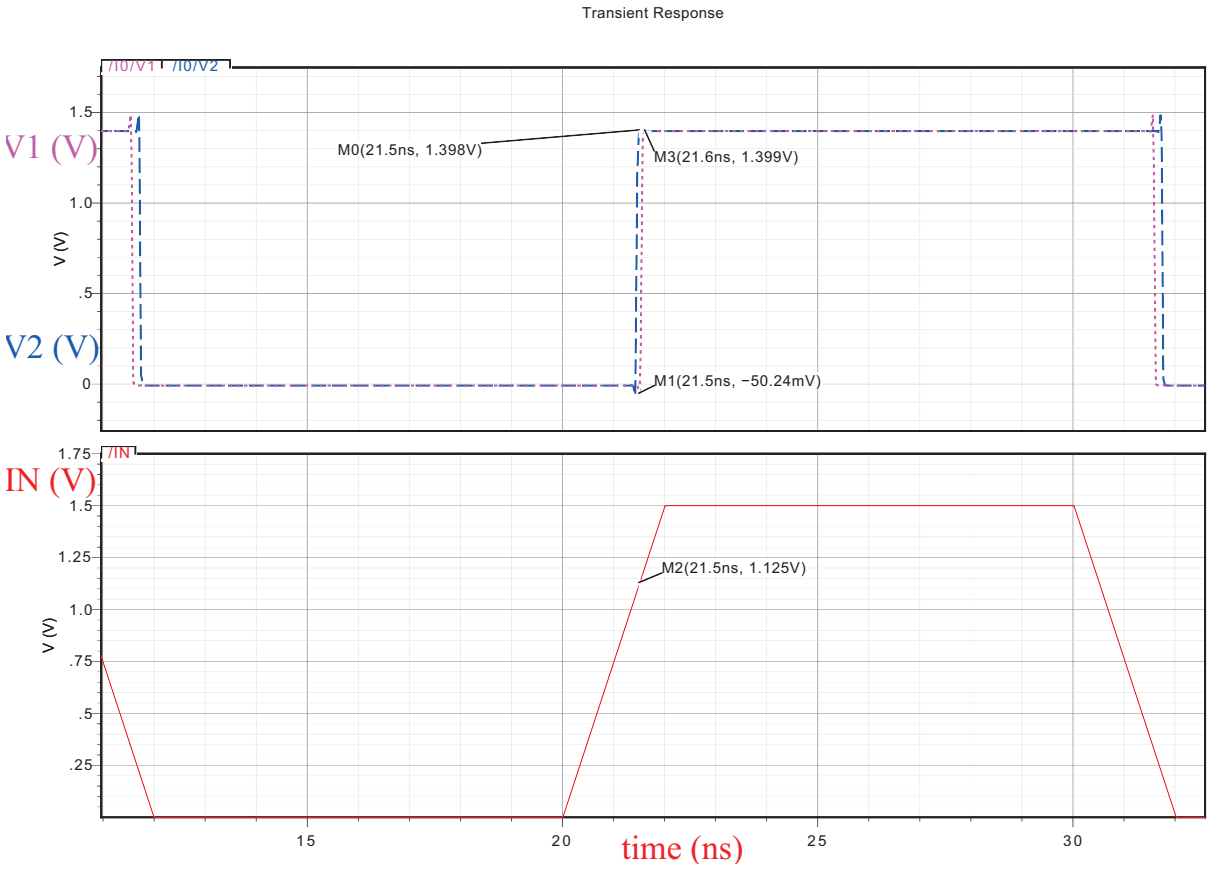


Fig. 2.27 A Spectre Simulation Of The Non-Overlapping Clock Signals

Subsequently, the TSV capacitance C_{TSV} is found from Eqn. 2.23 to be

$$C_{TSV} = \frac{k}{VDD} = \frac{7.106e-14}{1.4} = 50.76fF \tag{2.26}$$

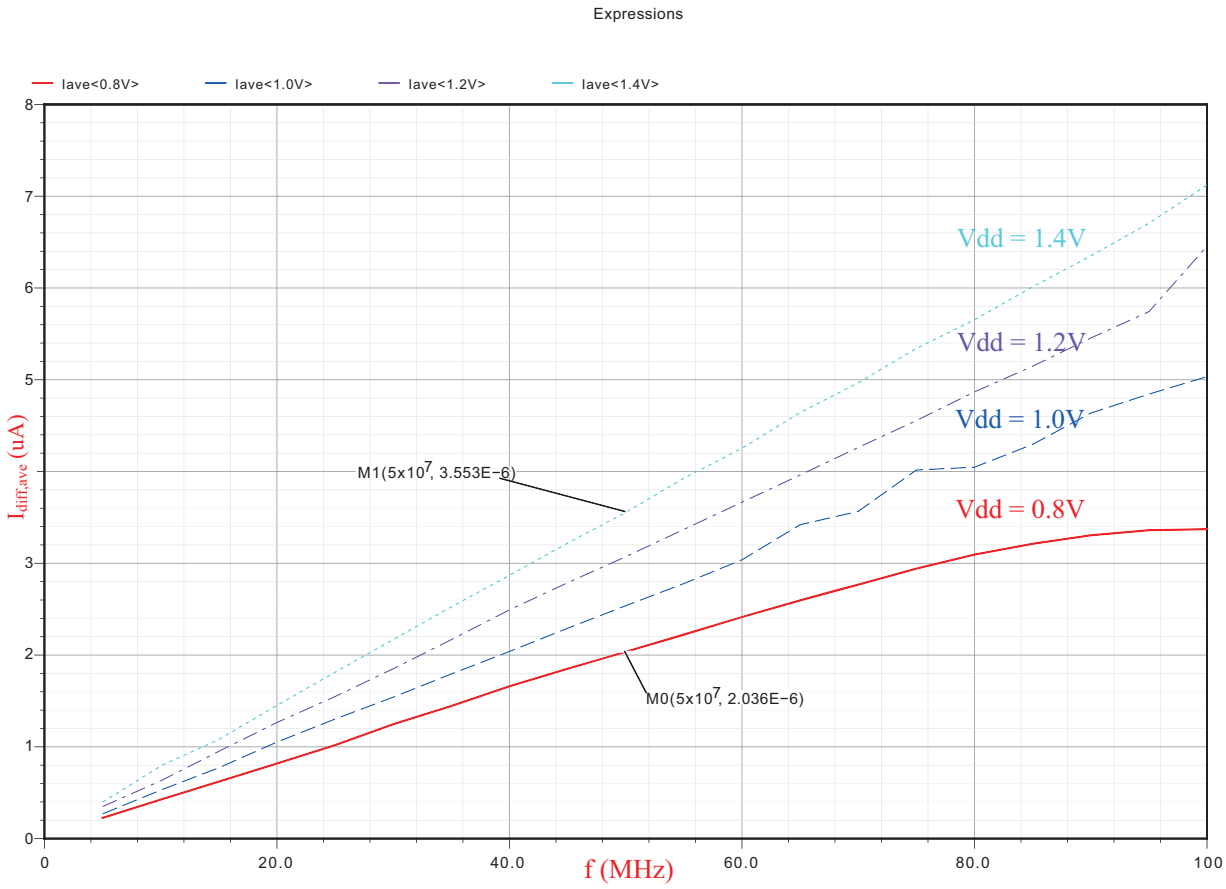


Fig. 2.28 Averaged Difference Current VS. Frequency Under Four Different Voltage Supply Conditions

In a similar manner, we can also calculate the TSV capacitance for a supply voltage of 0.8 V. There we see at $50MHz$, $I_{diff,ave2} = 2.036\mu A$, leading to

$$C_{TSV} = \frac{I_{diff,ave2}}{f_2 \cdot VDD} = \frac{2.036}{50e6 * 0.8} = 50.9fF \tag{2.27}$$

The charging and discharging currents, together with the difference current is shown in Fig. 2.29 for a 1.4 V supply level operating at a frequency of 50 MHz are shown in Fig. 2.29. The outputs of each pseudo inverter is charged to VDD when the control signal V_1 and

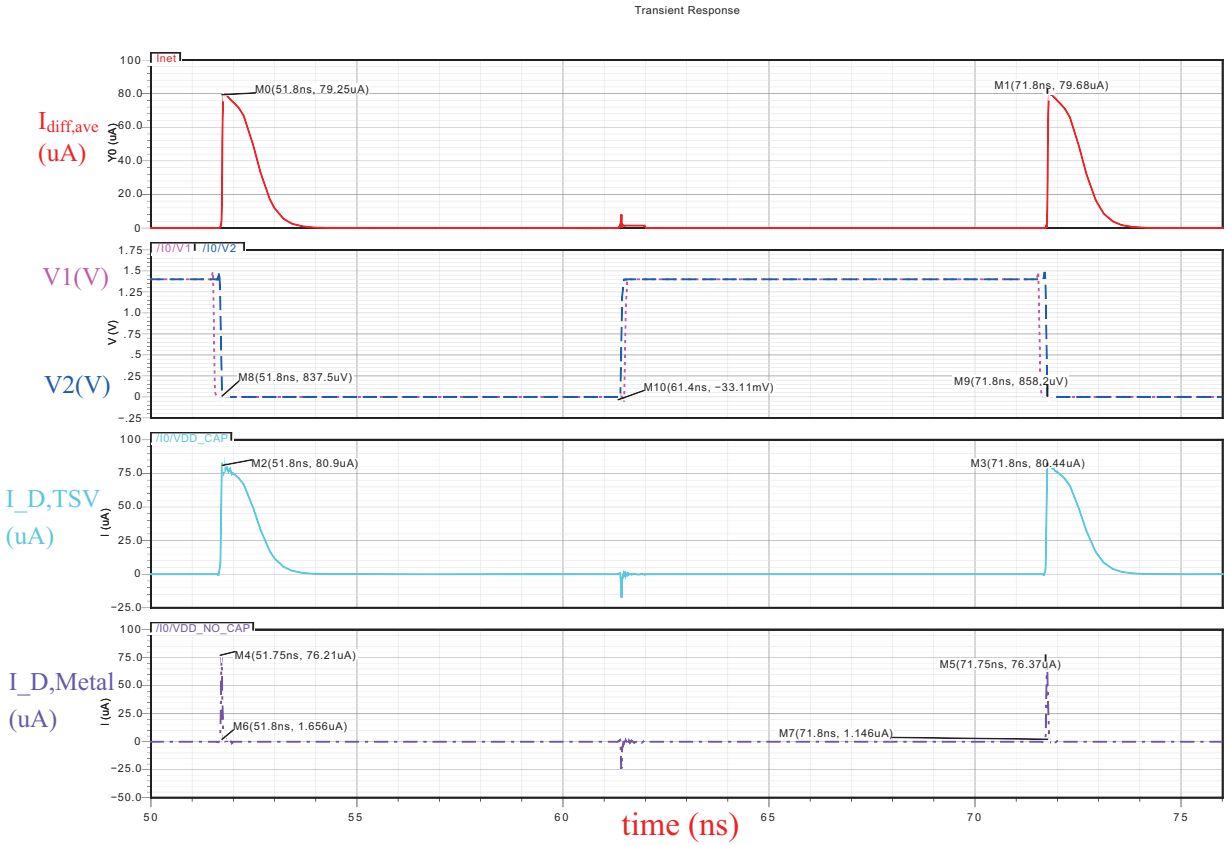


Fig. 2.29 Time Domain Charging and Discharging Current With/Without TSV Capacitor

V_2 are set low. The plot corresponding to *IO/VDD_TSV* is the current of the TSV loaded cell and the plot of *IO/VDD_NO_TSV* is the current of the reference cell. The top plot corresponding to *Inet* is the difference between these two currents. Its time average value (generally averaged over several cycles of the waveform) provides an estimate of $I_{diff,ave}$, which in turn is used to estimate C_{TSV}.

As an aside, the TSV capacitance extraction process described above can be re-developed with respect to variations in the supply voltage. For instance, one can use four different input clock frequencies, say 20 MHz, 40 MHz, 60 MHz and 80 MHz. By sweeping the supply voltage VDD and measuring the difference of the average charging and discharging current $I_{diff,ave}$, we can get the plot shown in Fig. 2.30. In this case, the TSV capacitance C_{TSV} would be derived from the slope of the $I_{diff,ave}$ versus VDD curve.

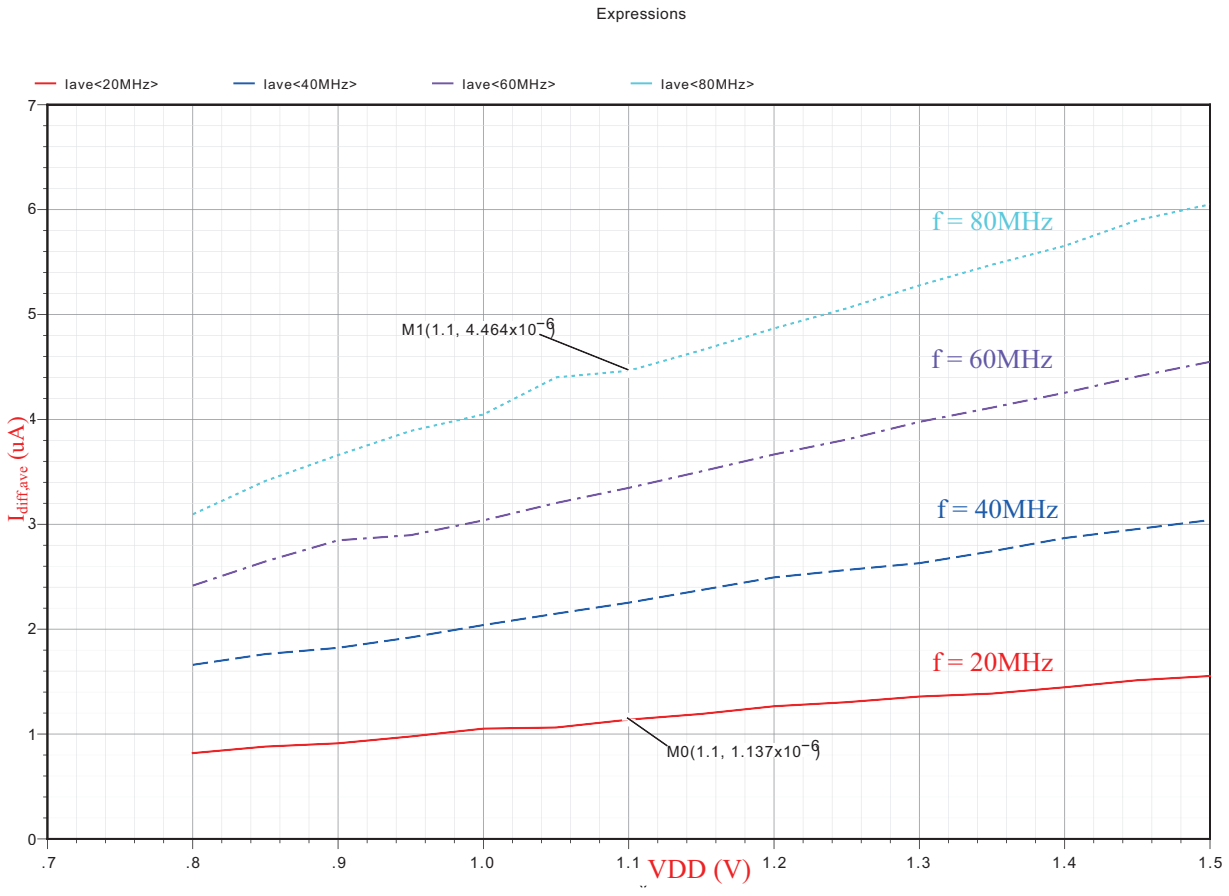


Fig. 2.30 Averaged Difference Current VS. Supply Voltage At Four Different Operating Frequencies

2.5 Conclusion

In this chapter several techniques for characterizing the signal integrity of a TSV in a 3D CMOS process was described. A four-point probe method for measuring the series resistance of a TSV was described. This was then followed by two methods to measure the end-to-end equivalent capacitance of a TSV structure. Each method can be classified as either a frequency-based or charge-based method. In the case of the frequency-based approach, two techniques were described; one involving a single-VCO and the other a two-VCO approach. Here it was shown that the two-VCO approach is less sensitive to switch parasitics and hence the preferred frequency-based method. The charge method is very simple in principle but is subject to mismatches issues. The accuracy of this method improves with supply voltage but, of course, is limited to what the technology can support.

Chapter 3

3D-IC Test Access and DfT Techniques

Test access is a popular way to externally stimulate a circuit-under-test (CUT) and extract its response with external instruments. For 2D chips, on-chip circuits can be accessed externally by a wafer probe such as that shown in Fig. 3.1. Here it can be seen that a set of fine needle-like fingers touch down on the surface of a wafer containing many individual dies. Through various metal pads, the probing needles make contact and direct power, control and signalling information to and from each IC. In the case of 3D chips, whereby multiple tiers of dies are stack on top of one another, preventing direct access to dies below the top layer as shown in Fig. 3.2. Here it is shown how the wafer probe can reach tier 1 but not tier 2 and tier 3 of the die stack.

This begs the question, "How does one access the circuits that reside on the various layers of a 3D-chip?" As first mentioned in [13], the use of DfT (Design for Test) techniques had a tremendous impact on the test costs associated with 2D-chip by providing test access through the application of on-chip test circuits. Such an approach is believed to be applicable to 3D-chips are well. This is the subject of this chapter.

DfT refers to adding testability features to microelectronic circuits. When properly implemented, DfT can achieve higher product quality with higher test coverage and lower production costs. Plenty of DfT literature exists for testing digital circuits; very little material can be found on analog or mixed-signal circuits. This chapter will focus on the latter area.

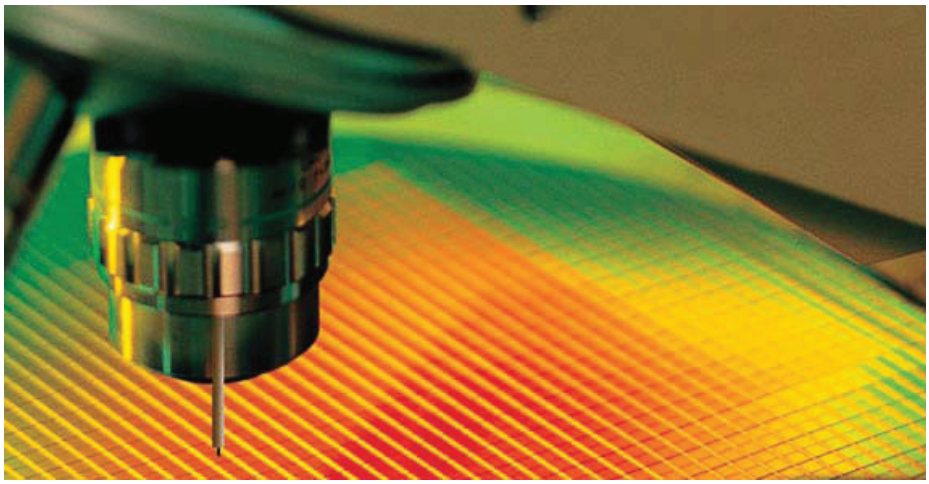


Fig. 3.1 Wafer Probe

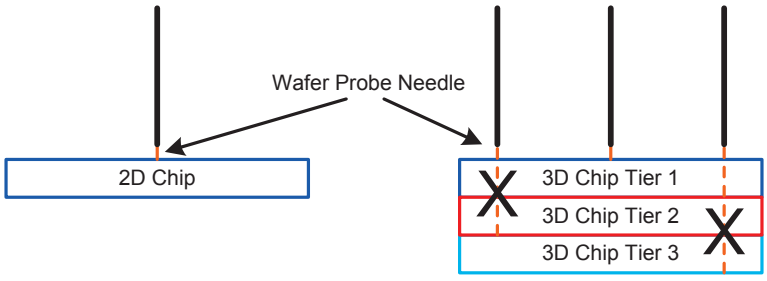


Fig. 3.2 Wafer Probe of 2D VS 3D

At the core of most, if not all, analog DfT techniques is the conversion between analog and digital signals, generally through the application of analog-to-digital (ADC) or digital-to-analog (DAC) conversion circuits. We'll begin this chapter by first describing the various logic circuits used to capture digital signals. This will then be followed by a discussion of the DfT techniques used for the TSV capacitance measurement techniques described in Chapter 2. Finally, the chapter will close with a discussion of an analog boundary scan technique for accessing internal analog/mixed-signal functions of a 3D-chip.

3.1 Digital Logic Gates Designs

Most DfT techniques are implemented using some form of digital logic. This section will describe the basic logic gates used to implement the DfT function of this dissertation.

3.1.1 Inverter Design

The inverter is designed to be simple and have a compact layout. The dimensions of the NMOS and PMOS transistors used in this dissertation are listed in Table 3.1. As is evident, the length of each transistor is assigned the minimum dimension of 0.13 μm but the widths are either 1 or 4 μm depending on whether it is an NMOS or PMOS transistor. This arrangement provides equal rise and fall times.

Table 3.1 Inverter Dimensions

	MN	MP
L (μm)	0.13	0.13
W (μm)	1	2

3.1.2 NAND Gate Design

Similar to the inverter design, the NAND gate is also chosen to be simple and have a compact layout. The schematic for the NAND gate is shown in Fig. 3.3. The transistor dimensions are listed in Table 3.2.

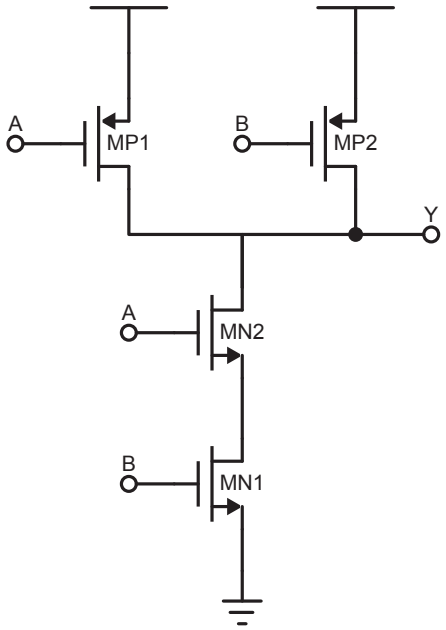


Fig. 3.3 NAND Gate

Table 3.2 NAND Gate Transistor Dimensions

	MN1	MN2	MP1	MP2
L (μm)	0.13	0.13	0.13	0.13
W (μm)	2	2	2	2

3.1.3 NOR Gate Design

The schematic of the NOR gate can be seen in Fig. 3.4 and the corresponding transistor dimensions are provided in Table 3.3.

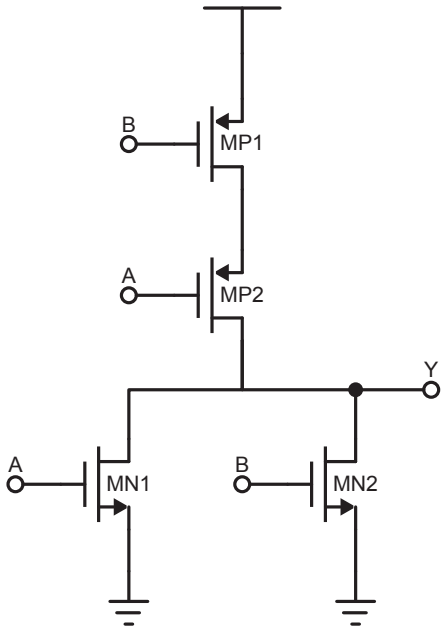


Fig. 3.4 NOR Gate

Table 3.3 NOR Gate Transistor Dimensions

	MN1	MN2	MP1	MP2
L (μm)	0.13	0.13	0.13	0.13
W (μm)	1	1	4	4

3.1.4 True-Single-Phase Clock D-Type Flip-Flop Design

The true single-phase clock (TSPC) structure [14][15] is used to implement the D-type flip-flop (DFF) used in this work. It provides better performance by introducing a pre-charge stage between stages to speed up the circuit operation. There are two types of TSPC DFFs used in this work; one has a reset function and the other one does not.

TSPC DFF Without Reset

The schematic diagram for the TSPC DFF without reset is shown in Fig. 3.5. This particular DFF will be used as part of a frequency divider circuit. The TSPC DFF without reset will be used to realize a frequency divider circuit. The transistor dimensions can be seen listed in Table 3.4(a) and Table 3.4(b).

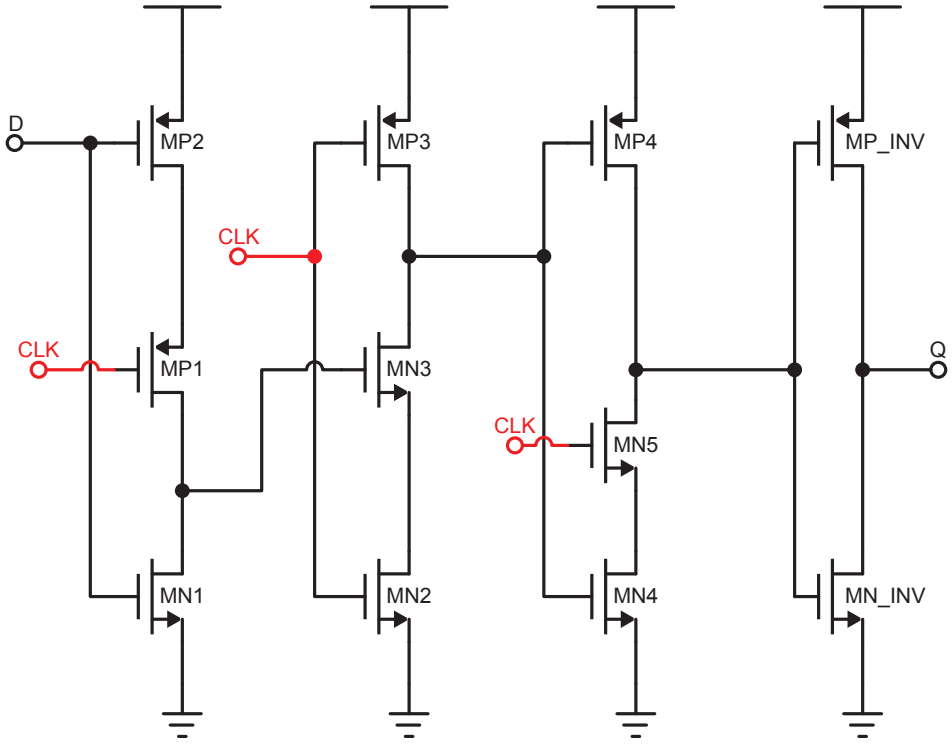


Fig. 3.5 TSPC DFF Without Reset

TSPC DFF With Reset

The schematic diagram for the TSPC DFF with reset is shown in Fig. 3.6. This particular TSPC DFF will be used in for constructing the counter circuit. The transistor dimensions for this DFF can be seen listed in Table 3.5(a) and Table 3.5(b).

3.1.5 MUX Design

The multiplexer (MUX) acts as a digital switch in order to select the appropriate signal path. It is also used in the implementation of the shift register. The multiplexer is shown

Table 3.4 Transistor Dimensions For The TSPC DFF Without Reset

(a) NMOS Dimensions

NMOS	MN1	MN2	MN3	MN4	MN5	MN_INV
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13
W (μm)	1	1	1	1	1	1

(b) PMOS Dimensions

PMOS	MP1	MP2	MP3	MP4	MP_INV
L (μm)	0.13	0.13	0.13	0.13	0.13
W (μm)	2	2	2	2	2

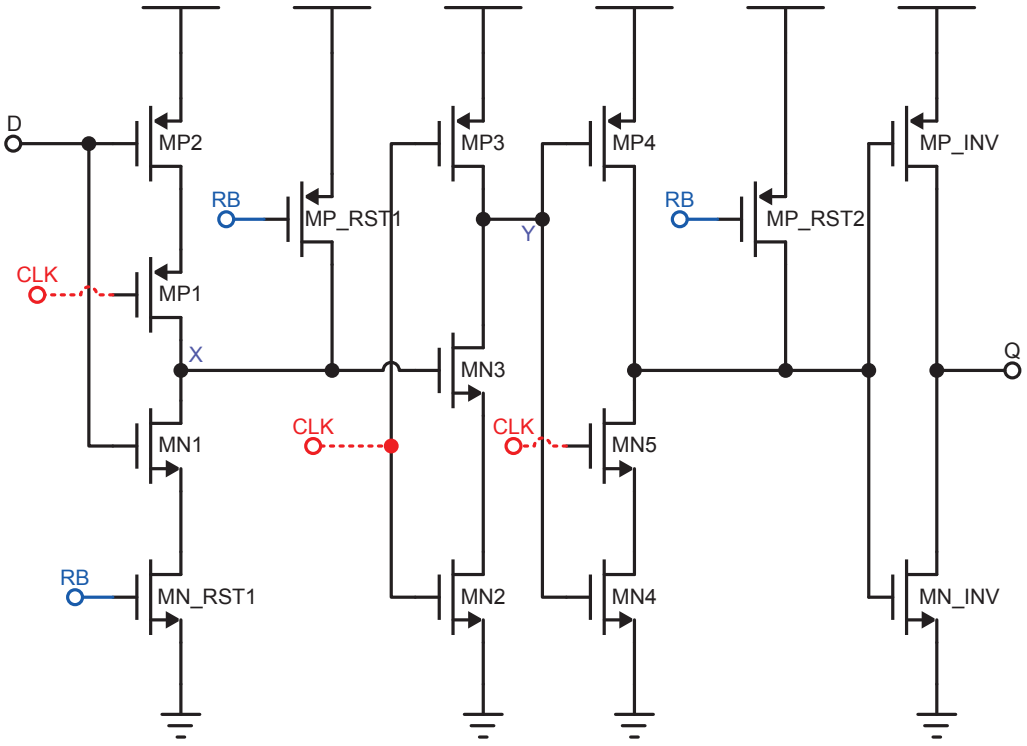


Fig. 3.6 TSPC DFF with Reset

Table 3.5 TSPC DFF with Reset Dimensions

(a) NMOS Dimensions

NMOS	MN1	MN2	MN3	MN4	MN5	MN_RST1	MN_INV
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.13
W (μm)	1	1	1	1	1	1	1

(b) PMOS Dimensions

PMOS	MP1	MP2	MP3	MP4	MP_RST1	MP_RST2	MP_INV
L (μm)	0.13	0.13	0.13	0.13	0.13	0.13	0.13
W (μm)	2	2	2	2	2	2	2

in Fig. 3.7 consisting of the previously described logic gates.

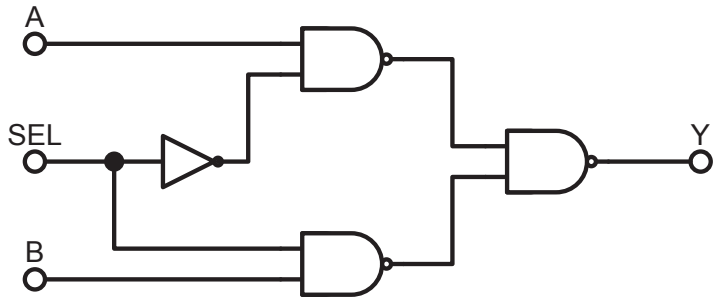


Fig. 3.7 Multiplexer

3.2 Support Circuits For FBCM

In this section, we'll look at the DfT techniques and support circuits used for FBCM described previously in Chapter 2. This includes the frequency-to-digital converter (FDC) and the PISO shift register design.

3.2.1 Frequency-to-Digital Converter

In the frequency-based capacitance measurement method that we discussed in Chapter 2, the frequency-to-digital converter (FDC) is used to convert a frequency quantity into a digital integer value. By converting the oscillation frequency of the ring oscillator into

a digital number and passing the digital value off-chip using a common digital bus, it eliminates the need for a specialized driver and I/O pin, thereby saving power and silicon space.

The FDC is constructed from three parts: Frequency Divider, Counter and PISO Shift Register as illustrated in Fig. 3.8.

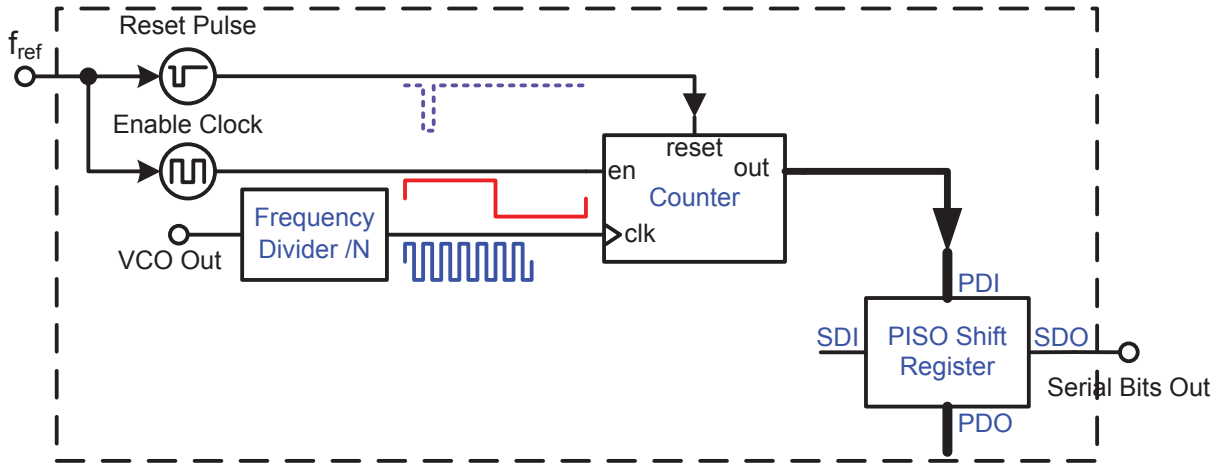


Fig. 3.8 Frequency-To-Digital Converter

Frequency Divider

Since the output oscillation frequency lies in the low-GHz range, in order to use an eight-bit counter with a MHz reference frequency we have to divide down the oscillation frequency. The basic architecture of frequency divider is shown in Fig. 3.9. It consists of three DFFs configured as an divide-by-8 ripple counter.

Counter

An 8-bit up counter is built for the FDC. While the Enable input is high, the counter will count the number of rising edges associated with the clk input. When the Enable input is low, the count is left unchanged.

Pulse Generator

The pulse generator is used to reset the counter once the final count is passed to the PISO shift register.

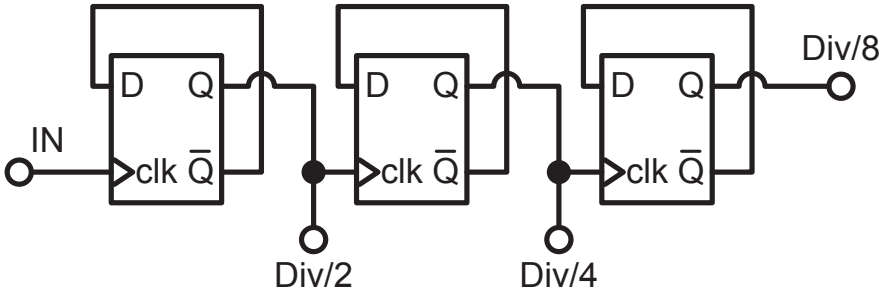


Fig. 3.9 Frequency Divider

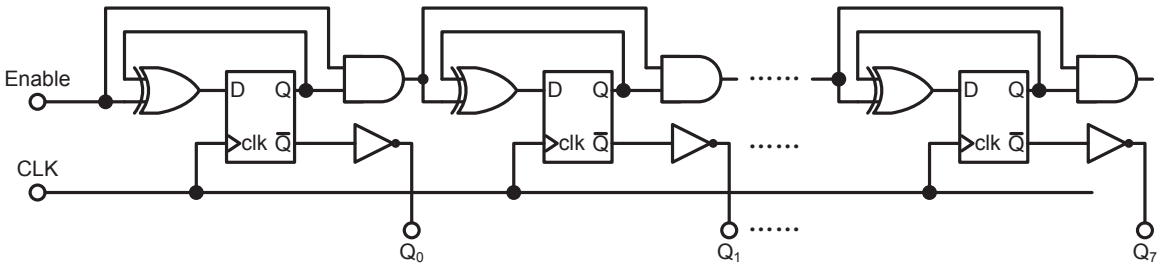


Fig. 3.10 Up Counter

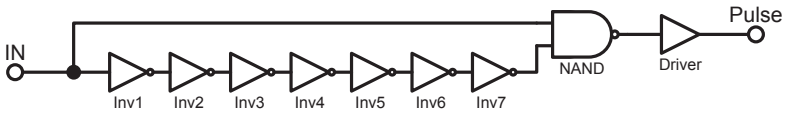


Fig. 3.11 Pulse Generator

3.2.2 PISO Shift Register

In order to reduce the impact of the test circuitry on the overall functionality of the chip, the 8-bit digital count value is captured in parallel form by the PISO and passed across the chip boundaries in a serial 1-bit form. The schematic for the PISO is shown in Fig. 3.12.

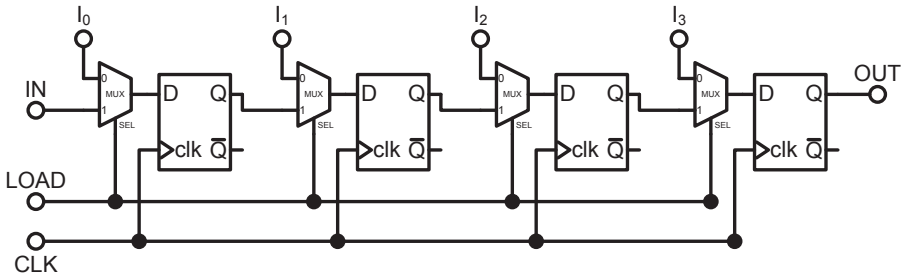


Fig. 3.12 Parallel-In Serial-Out Shift Register

3.3 Boundary Scan

Boundary scan isolates various digital blocks from surrounding circuits for the testing and debugging purposes. It is a method that is widely used for testing the interconnect associated with printed circuit boards (PCBs) and the functionality of digital logic circuits, both on the PCB as well as internal to the IC [8].

3.3.1 Boundary Scan Cell

The boundary scan cell (BSC) serves as the 'Virtual Bed-Of-Nails' around the core circuit, bounding the nets and providing continuity testing. It requires minimal on-chip resources (pins) to observe/stimulate various test conditions. The boundary scan cell needs to act as a serial-in, parallel-out (SIPO) shift register and a parallel-in, serial-out (PISO) shift register. The boundary scan cell can be implemented as shown in Fig. 3.13.

The BSC has four different states of operation: normal, capture, shift and update state. The Mode line in Fig. 3.13 is used to select normal or test mode of operation. During the *normal* state, data is passed directly through the BSC as a parallel-in to parallel-out operation. It essentially does nothing to the incoming data. During the *capture* state, the Serial In signal is routed into the Scan FF and the value is captured on the next rising edge

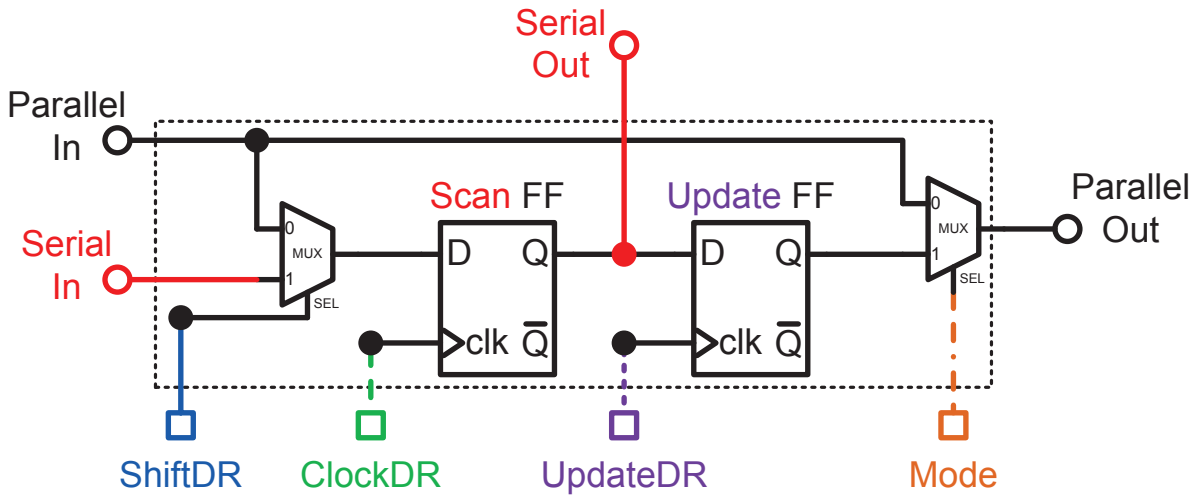


Fig. 3.13 Boundary Scan Cell Architecture

of the ClockDR signal. When set in *shift* mode, data in one BSC is passed to the next BSC through the Serial-In to Serial-Out path. Under the *update* mode, the content of the Update FF is passed through Parallel Out port of the BSC.

3.3.2 JTAG Architecture

In the 1980s, the Joint Test-Action Group (JTAG) formed by representatives from industry participants and users of components and boards. The JTAG group developed the standard to allow different IC vendors to design chips compatible with a consistent board-level testing architecture. In 1990 the IEEE adopted the standard as *IEEE Standard 1149.1* [16] [8].

After years of discussion, the JTAG organization finally proposed the The IEEE 1149.1 boundary scan architecture shown in Fig. 3.14. The main components of this architecture are as follows:

1. A set of dedicated test pins: Test Data In (TDI), Test Mode Select (TMS), Test Clock (TCK), Test Data Out (TDO) and one optional test pin Test Reset (TRST). These pins are collectively referred to as the Test Access Port (TAP).

2. Boundary scan cells to form a boundary scan register around the perimeter of the chip.

3. A finite state machine TAP controller with inputs TCK, TMS, and TRST.

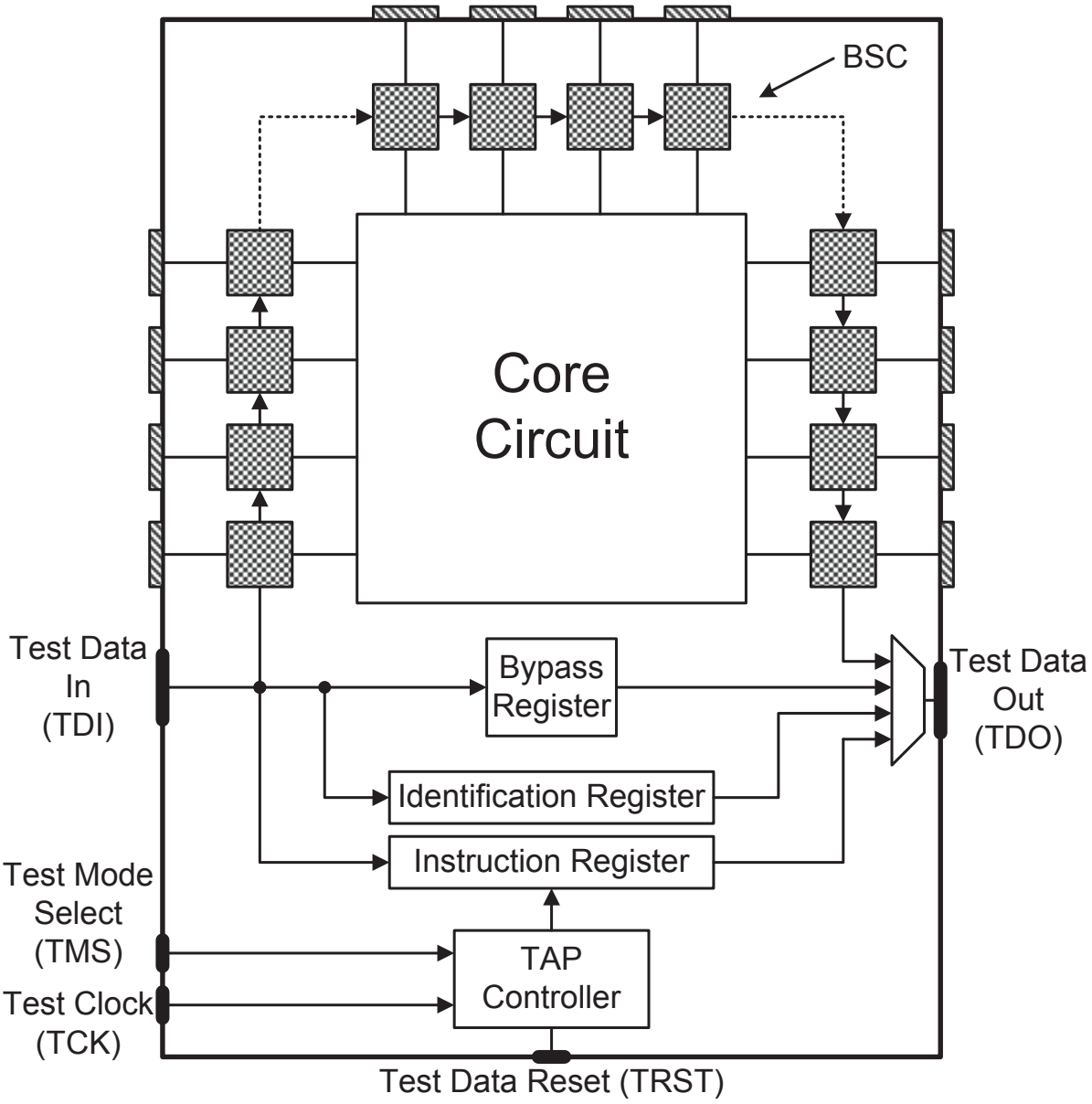


Fig. 3.14 IEEE 1149.1 Boundary Scan Architecture

4. An n-bit (n≥2) Instruction Register (IR), holding the current instruction.
5. A one-bit Bypass Register.
6. An optional 32-bit Identification Register capable of being loaded with a permanent device identification number.

At any time, only one register can be connected from TDI to TDO. The selected register is identified by the decoded output of the IR.

3.3.3 JTAG Interconnect Test Example

In a system with JTAG embedded, the test structures from multiple ICs could be tied together in a daisy-chain configuration. Thus the entire system can be accessed through a single interface port, which save a a lot of test resource for the core circuits. Fig. 3.15 illustrates a chip-to-chip interconnect test example using JTAG. Here two ICs are daisy-chained together using a common TAP configuration. Let us consider the implications of the interconnect between Chip 1 and Chip 2 at pins N1 - N4. If a set of test vectores are applied to the TDI port of Chip 1 and routed to pins N1 - N4, and the corresponding logic values appearing at the pins of Chip 2 are routed to the TDO port of Chip 2, then an analysis of the interconnect at pins N1 - N4 can be made. If the captured data is equal to the input data sequence, i.e., '1110', '0101', '1001' and '0011' then one can conclude that the interconnects between pins N1 - N4 are fully intact and fault-free. However, if the data is different, say appearing at the output as the data sequence, '1110', '0100', '1000' and '0010', where the last bit of all four sequences remain at logic 0 level, it can be surmised that the pin at N4 of Chip 2 is "stuck-at-0" due to an open on pin N4. Conversely, if the output data sequence appears as '1110', '0001', '0001' and '0011' where it can be observed that the first two bits of each sequence appears are a "wire-AND" operation, then it can be surmised that a short appears across pins N1 and N2. These two fault conditions are depicted in the diagram of Fig. 3.15. While other faults can appear, this example serves to illustrate how the input and output data can be used to deduce the interconnect between different chips.

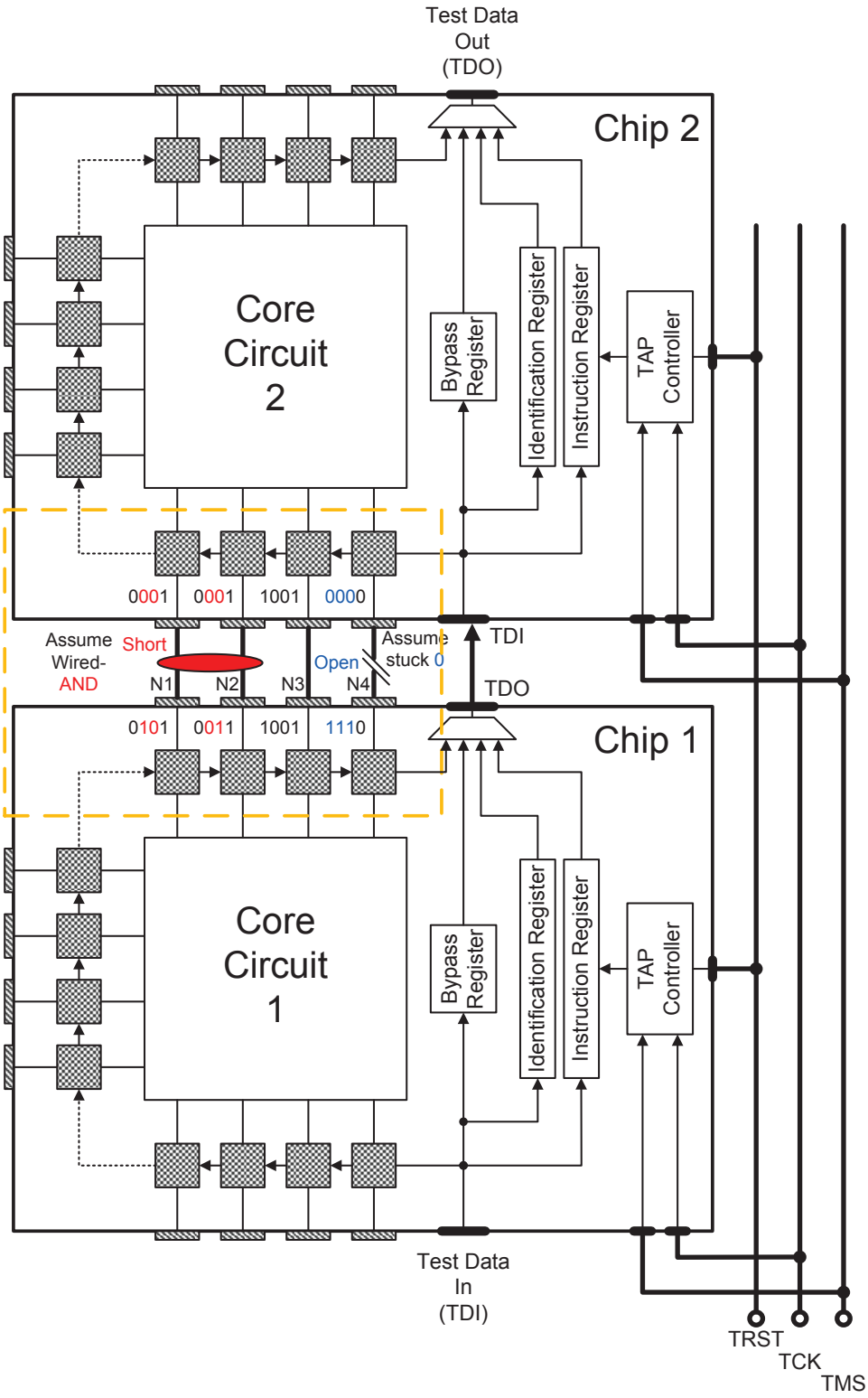


Fig. 3.15 Boundary Scan Architecture with Chip-to-Chip Interconnect Testing

3.4 Analog and Mixed-Signal Boundary Scan

The IEEE Std. 1149.1 has achieved a great amount of success in the digital testing area. However, the 1149.1 standard fails when it comes to testing analog circuits. As the percentage of analog circuits on a mixed-signal chips has steadily been increasing over the past decade, the need for a standard interface to aid the testing of both analog and digital on the same IC has reached a critical level. The response has been to introduce a new standard called the IEEE 1149.4 Mixed-Signal Boundary Scan Standard. It is built upon the 1149.1 digital boundary scan methodology. The 1149.4 standard is compliant with the 1149.1 test bus standard. The major difference is the addition of several test pins and analog switches for stimulating the non-digital circuits and for extracting non-digital signals.

3.4.1 IEEE 1149.4 Architecture

The IEEE 1149.4 architecture is implemented by adding Analog Boundary Modules (ABM) to the IEEE 1149.1 implementation as shown in Fig. 3.16. It behaves in a similar manner as the Boundary Scan Cell (BSC) in the IEEE 1149.1 standard. Beside the addition of the ABMs, test buses AT1 and AT2 is also added. The boundary scan cell (BSC) is also known as the digital boundary module (DBM). The TDI path goes through both the digital and analog boundary modules to facilitate interconnect diagnostics.

3.4.2 Analog Boundary Module Architecture

The circuit composition of the ABM [17] is illustrated in Fig. 3.17. A pair of switches at each analog input and output pin of the IC together with the comparator change the normal analog signal into two digital levels, V_H or V_L. These two signals are usually set to be V_{DD} and digital ground. The logic levels V_H and V_L enables a simple interconnect test to be performed in much the same way as that performed in the IEEE 1149.1 test bus standard. By comparing the incoming signal level to the threshold voltage V_{TH} on any of the analog pins, a simple logic test can be performed indicating whether the interconnect is in intact or not. In addition, the IEEE 1149.4 also include a secondary test bus involving test lines AT1 and AT2. Analog signals can be routed in and out of the chip through the application of several analog switches designated as SB1 and SB2. This analog bus provides 'virtual probing', as any inner two nodes can be accessed externally from the chip.

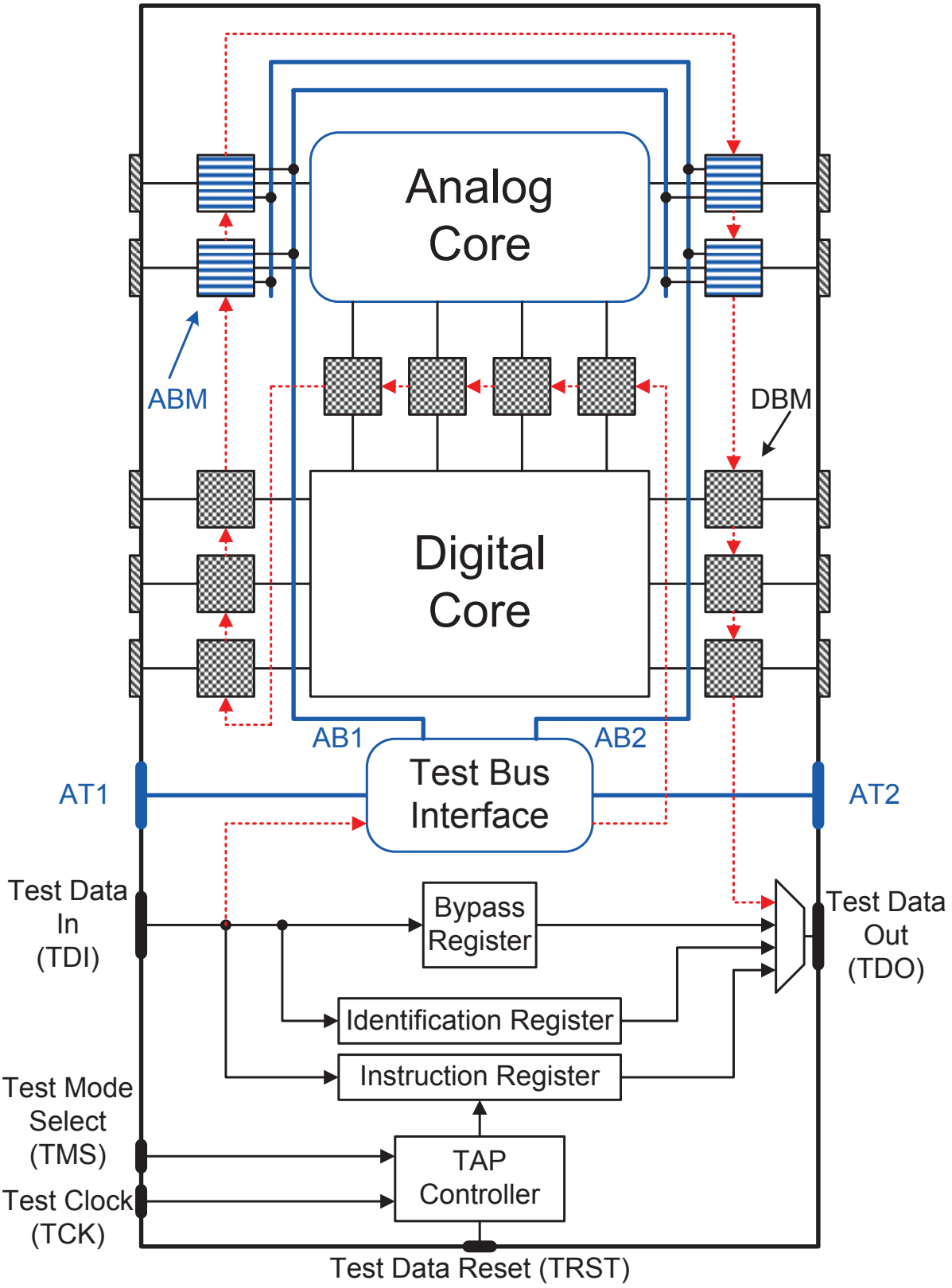


Fig. 3.16 IEEE 1149.4 Architecture

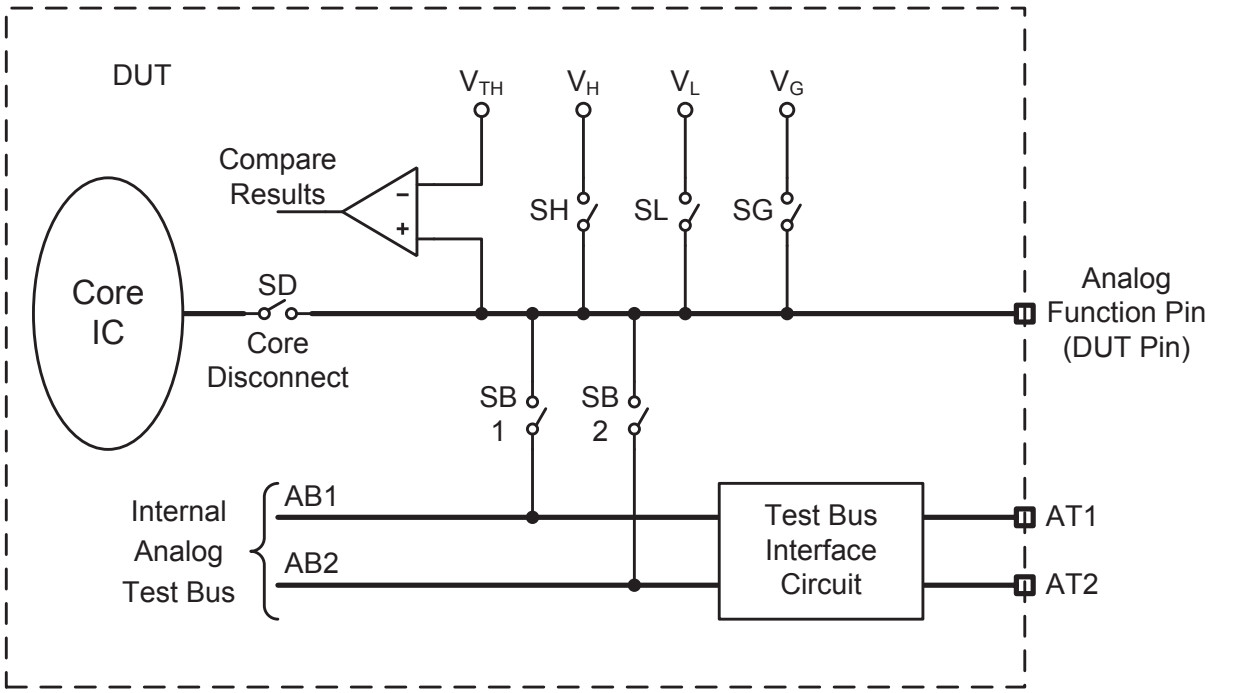


Fig. 3.17 IEEE 1149.4 Standard Analog Boundary Module Architecture

The IEEE 1149.4 standard only prescribed the general implementation symbolically rather than with a specific circuit implementation. One circuit implementation of the ABM was first presented in [18] [19] and is shown in Fig. 3.18. The ABM implementation is based on the boundary scan cell (BSC). It has four states of operation: normal, capture, shift and update states. **Mode 1** and **Mode 2** are used to control the state in which the ABM operates in. When **Mode 1** is set low, the ABM is placed into its *normal* operational mode, i.e., the signal is driven from the IC core to the IC pad. Conversely, when **Mode 2** is set high, it is placed into its *test* mode. In this mode, the three states of the ABM (i.e., capture, shift, update) can be activated for testing purposes. During the *capture* state, the SDI signal are routed into the flip-flops and the value are captured on the next rising edge of the ClockDR signal. When ABM is in *shift* mode, data in one ABM is passed to the next ABM through the SDI to SDO path. Under the *update* mode, the content is passed to the output of the ABM. Analog buses AB1 and AB2 are also controlled by the register inside the ABM.

In the design of Fig. 3.18, the ABM can be controlled by almost the same TAP controller as that used for the IEEE 1149.1 standard. So the test code for 1149.1 could be easily

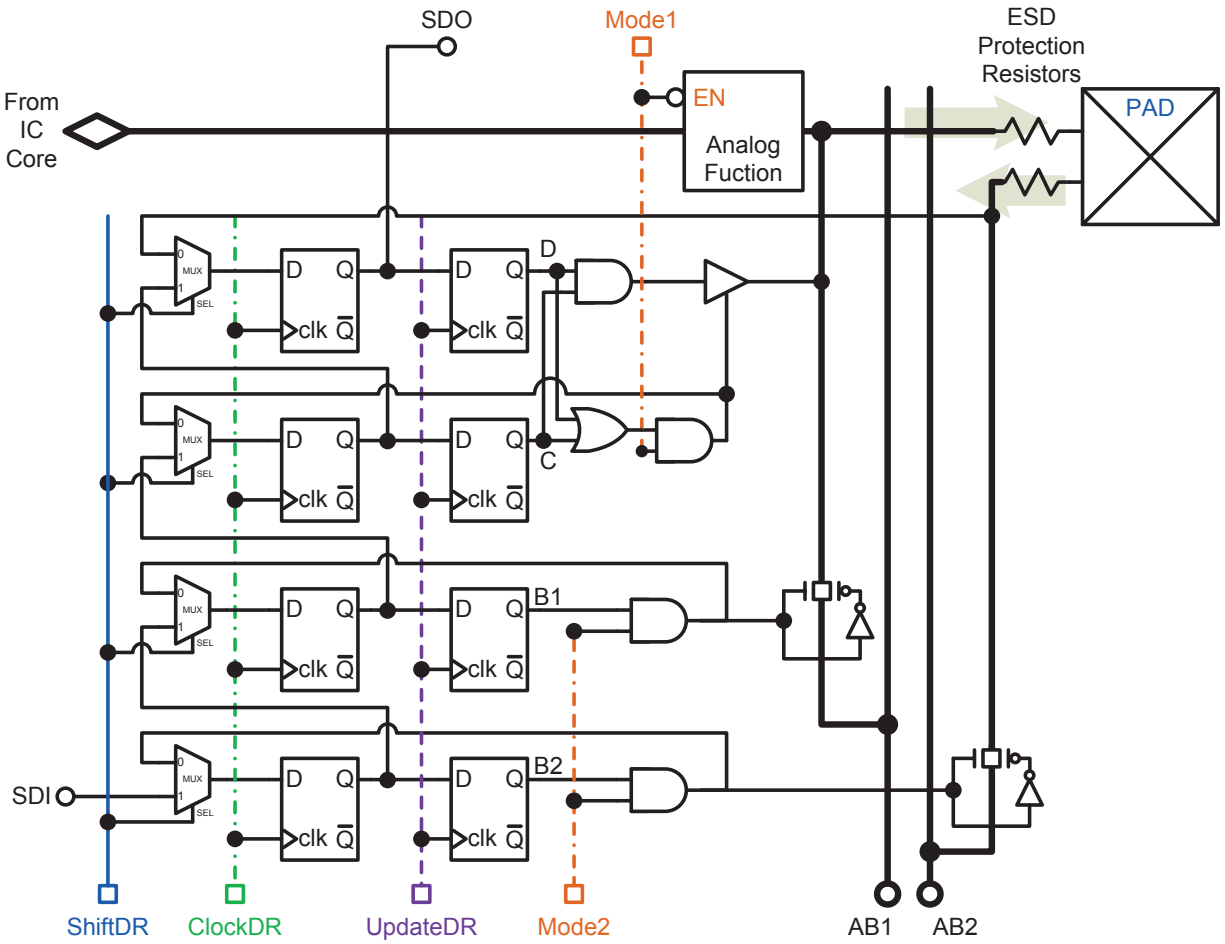


Fig. 3.18 IEEE 1149.4 Implementation - Analog Boundary Module Schematic

inherited and modified for the analog ABM usage. New instructions for probing, either stimulating or response extraction, will have to be added. When the ABM operates under EXTEST mode, all the pins are controlled by the scan register, as that found with the 1149.1 TAP controller. The states of each condition is list in the following Table 3.6.

Table 3.6 EXTEST Test Mode States

Data D	Control C	AB1 B1	AB2 B2	States
0	0	X	X	Core Disconnect (Tristate)
1	0	X	X	Drive 'ground' out
Data	1	X	X	Drive data out (1149.1)
X	X	1	X	Connect pin to AB1
X	X	X	1	Connect pin to AB2

3.4.3 Analog ABM Switch Design

The analog switches are controlled by shifting control bits into the 1149.1 TAP, allowing a standard method of controlling the switches and interface different ICs to the test equipment. The switches in IEEE 1149.4 standard must meet the following criteria:

- Signal propagation from one side to the other with minimum signal loss.
- Isolation of a signal from all the others.

An important practical issue facing the analog test bus is the crosstalk between AB1 and AB2 [8]. A major source of the coupling between these two analog lines comes from the parasitic capacitance introduced by the switches. A CMOS switch in the OFF state will have a parasitic capacitive path between its source and drain regions, thereby coupling signals across an open switch or, even worst, causing unwanted internal oscillations.

T-switch Design

One common solution to eliminate these coupling problems is to incorporate T-switch configuration as shown in Fig. 3.19. The T-switch is implemented using three NMOS or PMOS (or both) configured in a TEE-structure, where two switches are connected in series

and the third is connected to the middle node and ground. The ON and OFF states of the T-switch can be described as:

- OFF state. The grounding switch is closed while the others are open.
- ON state. Both the switches in serial are closed, but the grounding switch is open.

The CMOS implementation of the T-switch used in this dissertation is shown in Fig. 3.20. The transistors' dimensions are listed in Table.3.7.

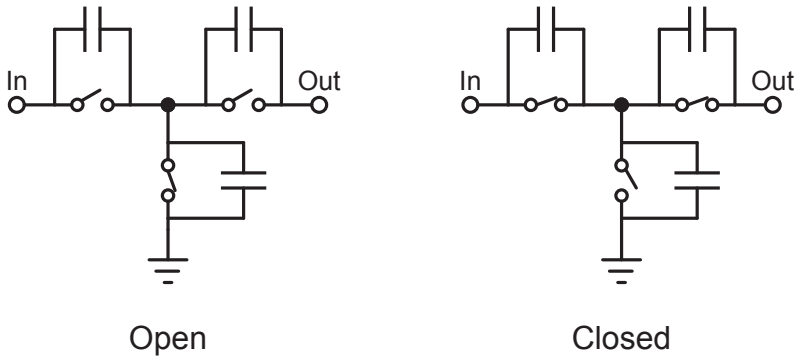


Fig. 3.19 T-switch Topology to Avoid Crosstalk

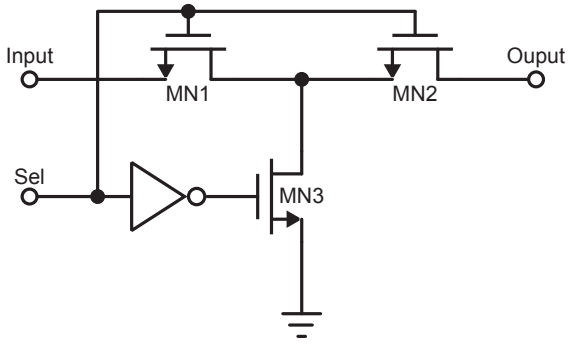


Fig. 3.20 T-switch Schematic

3.5 On-Chip Test Tier for 3D IC

Since we have more than one tier for the 3D IC design, why not consider that one of the tiers will act as the test engine for the entire 3D IC? Several ideas emerge. One is to consider

Table 3.7 Transistor Dimensions Of The TEE-Switch

	MN1	MN2	MN3
L (μm)	0.13	0.13	0.13
W (μm)	90	90	20

the test engine is constructed completely out of a FPGA fabric and, hence, is programmed fully in software. Another is to consider the test engine as a custom IC layer that is used during first silicon debug and production ramp. It may be remove from manufacturing once the chip is yielding large volume.

The classical test methodologies, such as the IEEE 1149.1 and 1149.4 test bus standards will be modified and adopted for the 3D-IC test. In this dissertation, we shall focus exclusively on the analog and mixed-signal test functions.

The prototype 3D chip is implemented in two tiers; one tier contains the core circuits and the other one will contain the test circuits as illustrated in Fig. 3.21. All the test structures, boundary scan cells, analog and digital supporting circuits are all placed in the Test Circuits Tier (also referred to as the WBOTTOM tier). The core circuits are placed on the Core Circuits Tier, also referred to as the WTOP tier. All the I/O pads are in the WTOP tier, hence, all signaling enters and exists the WTOP tier. This includes all test signals as well. The two tiers are bonded face-to-face by the bonding bumps, which are illustrated by the green dash line in Fig. 3.21. The ABMs act as a bed-of-nails, as illustrated by the solid orange lines with arrows. These are used to probe the analog/mixed-signal circuits on the core circuits tier. The green dashed line signifies a test signal interconnect.

3.5.1 Internal Analog Scan

The IEEE 1149.4 provide the ability to scan analog signals internal to the IC through the application of the two analog test lines, AB1 and AB2. This functionality is often depicted using the symbolic diagram shown in Fig. 3.22. Here three separate analog or mixed-signal stages are connected in cascade with no direct connection to the external I/O. However, by placing the ABM between the input and output nodes of the middle stage, enables the middle stage to be tested using the external test bus. The state of each switch within the ABM is controlled by digital bits route to each ABM through the scan chain of the test bus.

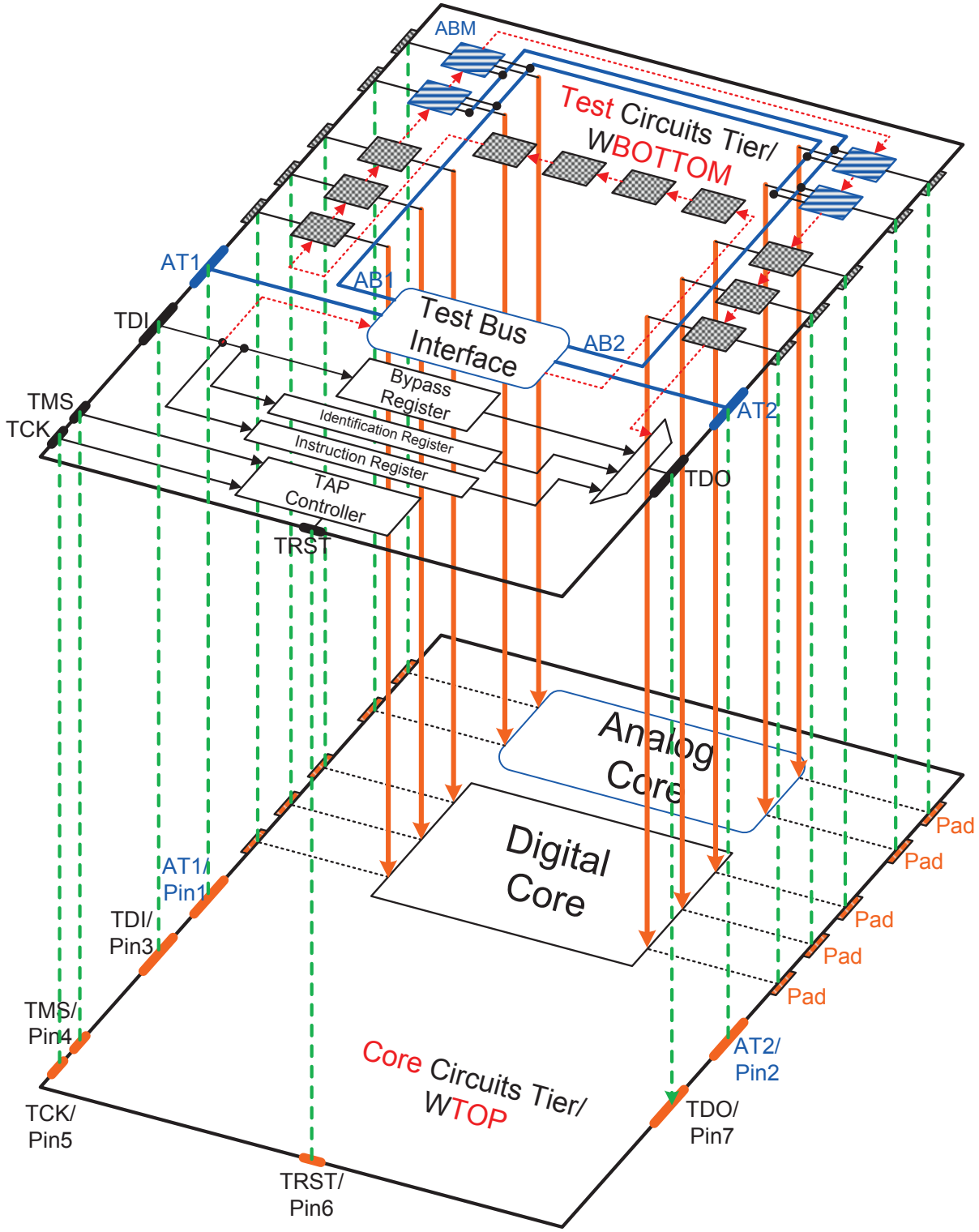


Fig. 3.21 Two Tiers Of A 3D Chip: Top Tier Provides The Core Chip Functionality, Bottom Tier Provides Test Infrastructure.

There are three modes of operation: Normal Mode, Force Input and Monitor Output. A description of each is as follows:

- *Normal Mode*: The signal could easily pass from one stage to the next with limited distortion.
- *Force Input*: Test data is force into the stage via the test bus AB1 (AB2).
- *Monitor Output*: Test results are routed through the other test bus AB2 (AB1) to the output port for measuring.

Unlike a digital test, where faulty operation can be deduce from a set of tests that are performed on the sum of individual components that make up the system, the same cannot be said for an analog or mixed-signal circuit. While testing individual building blocks may reveals faults, success for tests on individual building blocks is not sufficient to guarantee that the overall system will be fault free. As a result, an analog or mixed-signal system requires a system level or mission-mode type test as well.

3.5.2 Modified Analog ABM For 3D Testing

The ABMs in Fig. 3.21 act as a bed-of-nails that are used to probe the circuits on the core circuits tier. They are controlled by the *ClockDR*, *ShiftDR* and *UpdateDR* signals, which is shown in Fig. 3.24.

The ABM shown in Fig. 3.18 are compatible with IEEE 1149.4 test standard. However, this implementation of the ABM is more elaborate than it needs to be for 3D testing, as testing across the chip boundary or pad frame is not generally required by all ABMs. Instead, the ABM will be designed to probe inside the chip, in particular, when several dies are stacks together to form a 3D chip. The proposed ABM shown in Fig. 3.23 is used to control the switches to connect or disconnect a node from the analog test bus AB1 and AB2. As a result, fewer logic gates and flip-flops are required to implement this ABM than that shown in Fig. 3.18. An additional delay element is required to delay the control signal to switch 1 control. This will ensure that only one bus is connected to an internal analog node at any given time. The delay is realized by inserting a negative-edge trigger DFF in the serial scan chain as shown in Fig. 3.23.

A Spectre simulation of the modified ABM is provided in Fig. 3.24. From the top to bottom, the first plot represents the serial-in control bits of JTAG, *SDI* and the serial-out

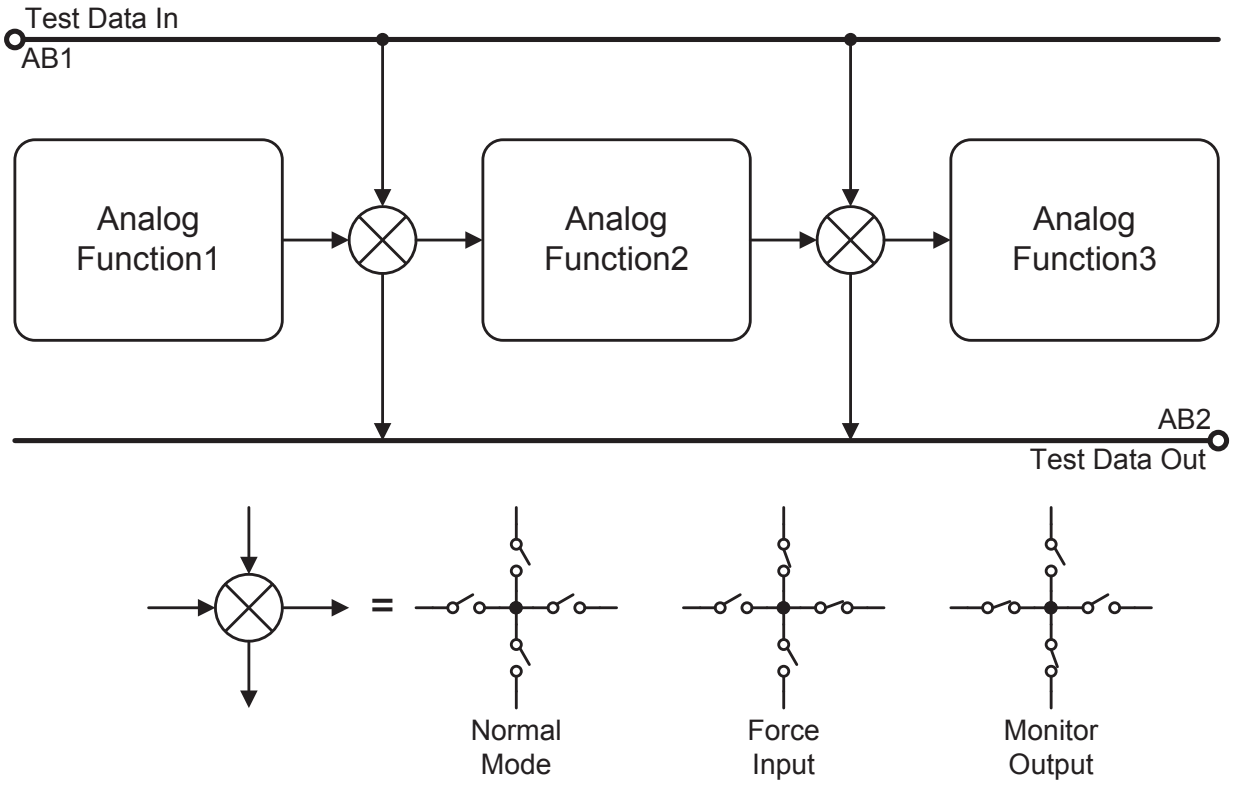


Fig. 3.22 Internal Analog Scan

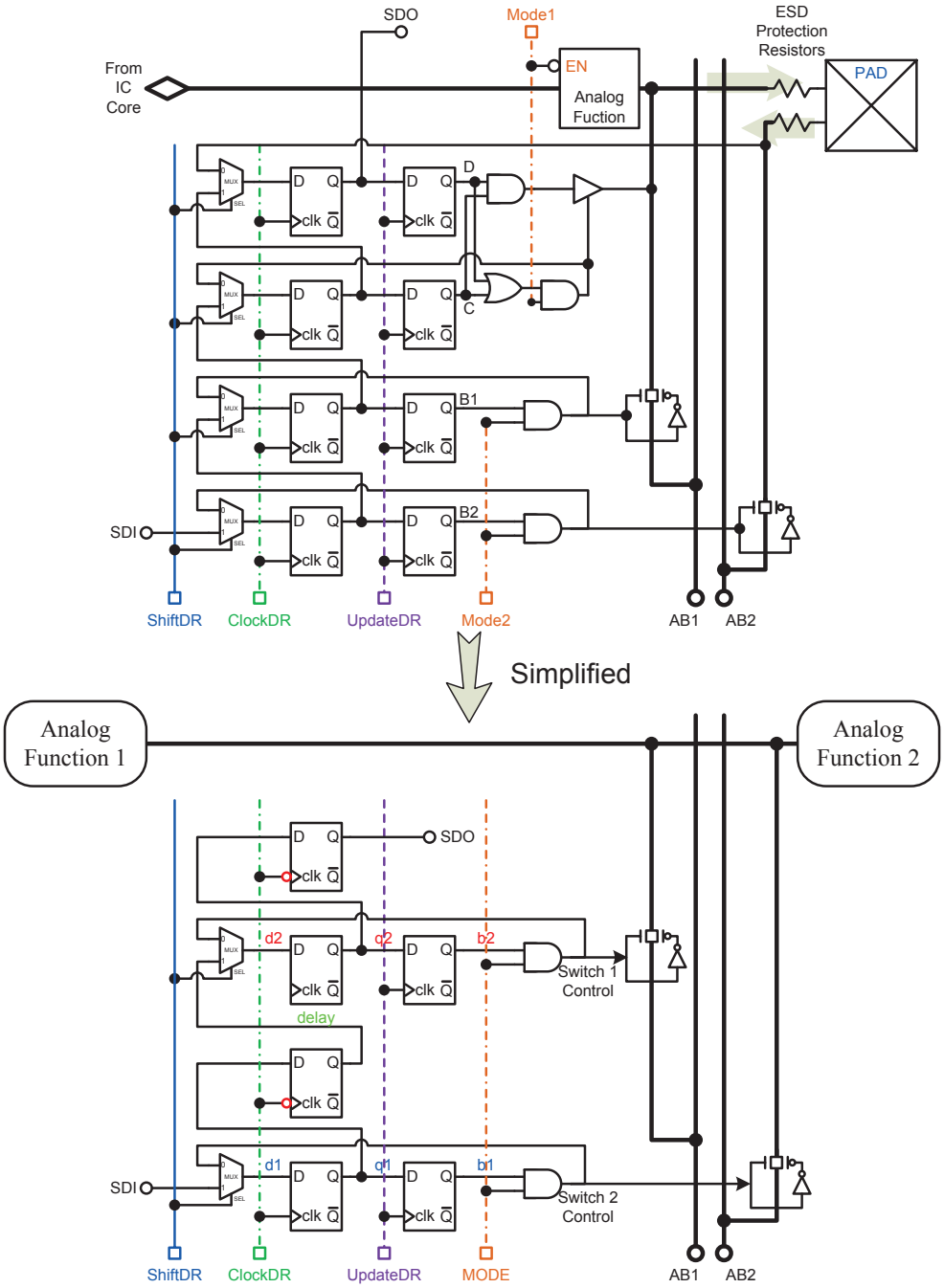


Fig. 3.23 Modified Analog Boundary Module VS Traditional Analog Boundary Module

control bits, *SDO*. The second one is the *ShiftDR* and *UpdateDR* control signals. The third plot are the input data of the FF, which are *d1* and *d2*. The fourth are the *delay* and *ClockDR* signals. The fifth plot are the output of the first stage FFs, *q1* and *q2*. And the bottom plot are the output of the second stage FFs, *b1* and *b2*. At the rising edge of the *ClockDR*, signal *b1* and *b2* pass through the first stage FF, which generate the signal *q1* and *q2*, this is the **capture** mode of ABM. The *ShiftDR* signal is always high, so as to pass the data from *SDI* to *SDO*. At the **update** mode, *b1* and *b2* are updated at the rising edge of *UpdateDR* signal.

3.6 Simulation and Discussion

In this section, simulation of analog switch design, on-resistance, range of linear operation and AC response will be presented. And the simulation of ABMs with analog switches connected will also be included. It describe how the control bits are routed into the ABM, and how the ABM control the analog switches.

3.6.1 Analog Switch Characterization

Below are the results of a Spectre simulation of the T-switch found in Fig. 3.20. Specifically, the series on-resistance, range of linear operation and AC response was captured. From Fig. 3.25, the ON resistance of the T-switch is around 25 Ω from 0.2 V to 1.5 V of input voltage level. The switch behaves linear over an input level from -0.8 V to 0.7 V as seen from Fig. 3.26. Outside of these levels, the switch saturates and no longer allows signal to pass through unimpeded. The 3-dB bandwidth of the switch reaches a very high level of 45.95 GHz, as can be seen from the plot of the AC behaviour in 3.27.

3.6.2 ABMs with Analog Switch

While in the test mode, one ABM would be used to inject signal into the core circuit and the other ABM would be connected to its output. Thus, during any one test, there will be at least two ABMs in any one signal path to and from the test equipment. In order to explore the impact of two ABS in series, the following Spectre simulations were performed.

Firstly, a test signal consisting of a 600mV peak to peak 500 MHz sin wave is forced on the AB1 test line and the corresponding response is observed at the output of the AB2

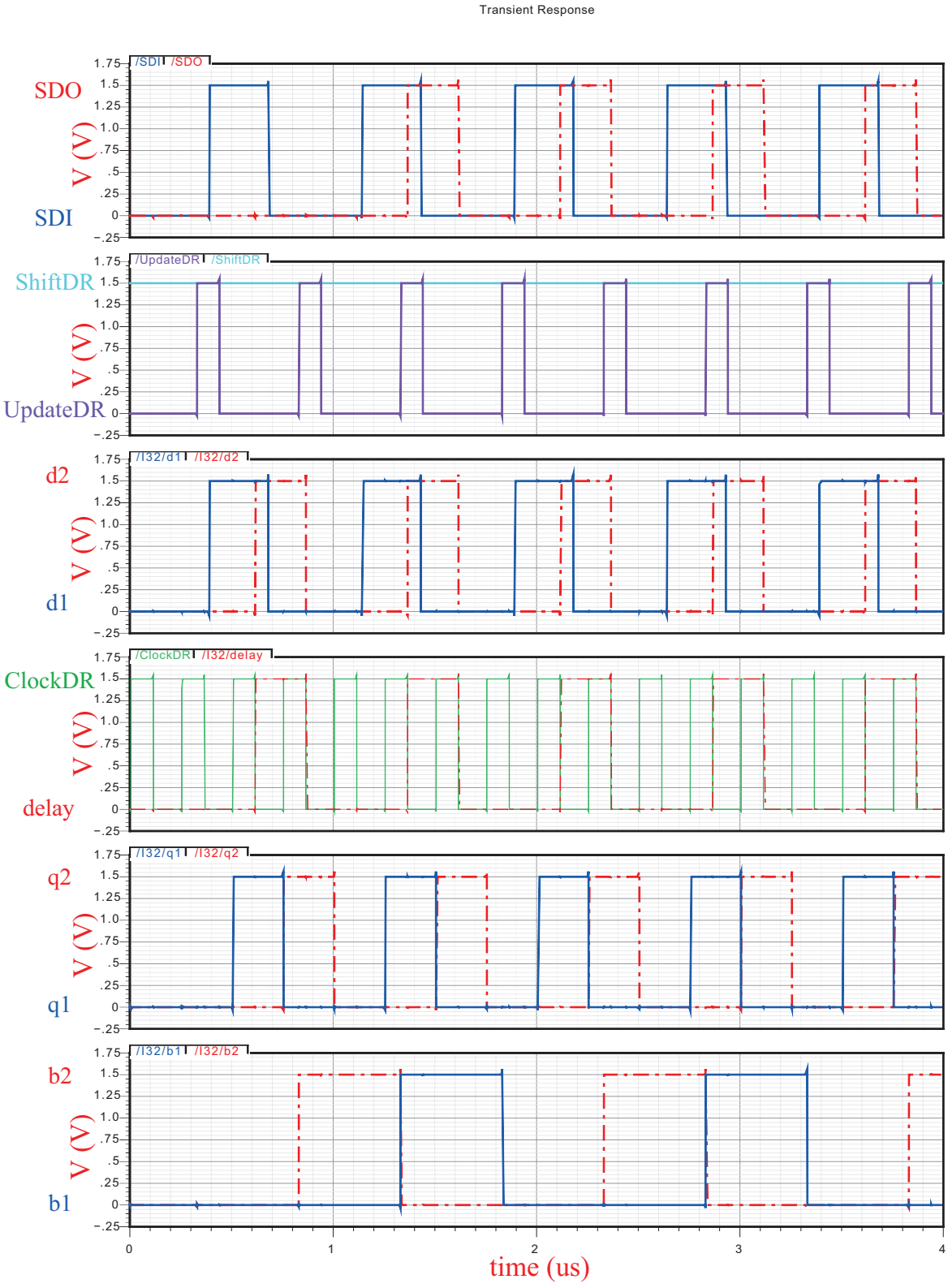


Fig. 3.24 Modified ABM Time Waveform

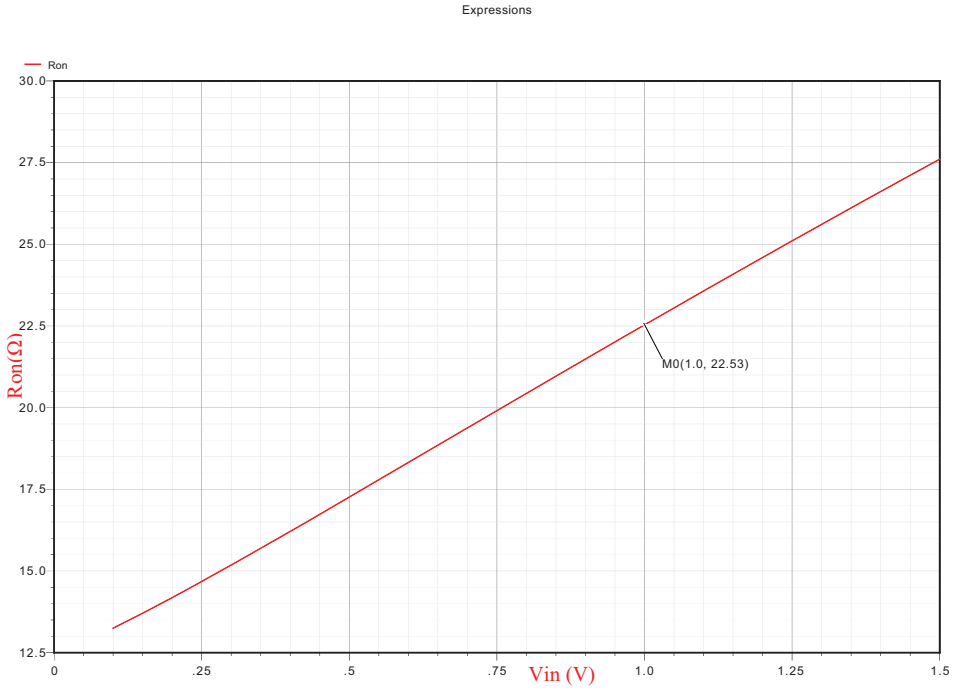


Fig. 3.25 Analog Switch ON Resistance

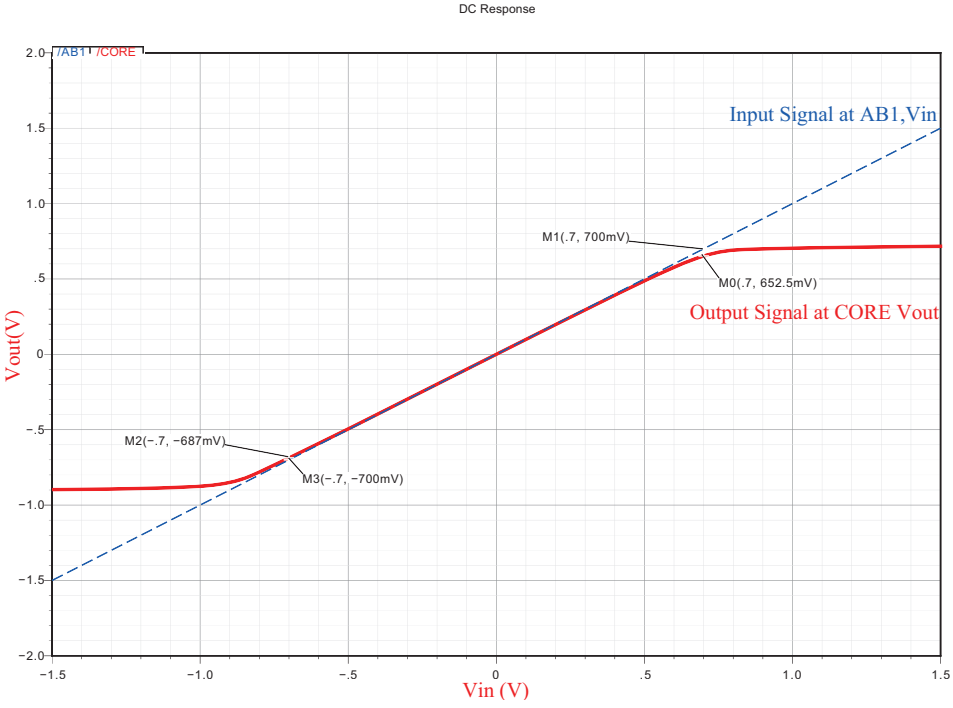


Fig. 3.26 Analog Switch Input Range

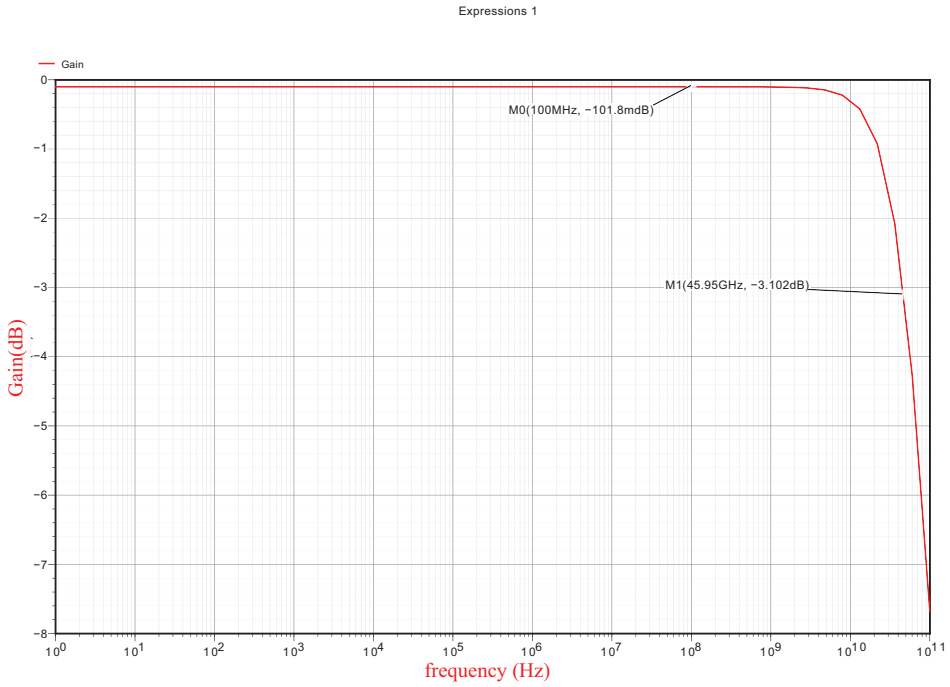


Fig. 3.27 Frequency Response of Analog Switch

test line. In addition, the control signals used for each ABS is also observed. The results of the simulation are shown in Fig. 3.28.

From top to bottom, the first graph represents the two control signals *Swc11* and *Swc12* for the switch in ABM1, while the second graph shows the control signals *Swc21* and *Swc22* for the switch in ABM2. When the control signal *Swc11* is high and *Swc12* is low, the test signal is passed from the *AB1* bus to the *CORE* bus through the **ABM1** module. Consequently, when the control signal *Swc21* is low and *Swc22* is high, the output signal propagates from the *CORE* bus to the *AB2* bus through the **ABM2** module. The third graph is for the serial-in control bits of JTAG, *SDI* and the serial-out control bits of JTAG, *SDO*. These are used to control the signal path for the ABM switches. The forth set of waveforms are for the *ClockDR* and *UpdateDR* signals. These are used to update the data in the register of ABM; they help to keep the ABM functional. The last two graphs correspond to the output signal on the AB2 bus and the input signal on the AB1 bus. Signal *AB2* can only propagate through ABM1 to ABM2 when the control signals for the switches *Swc11* and *Swc22* are both high.

Secondly, the performance associated with the two switches in series through the two

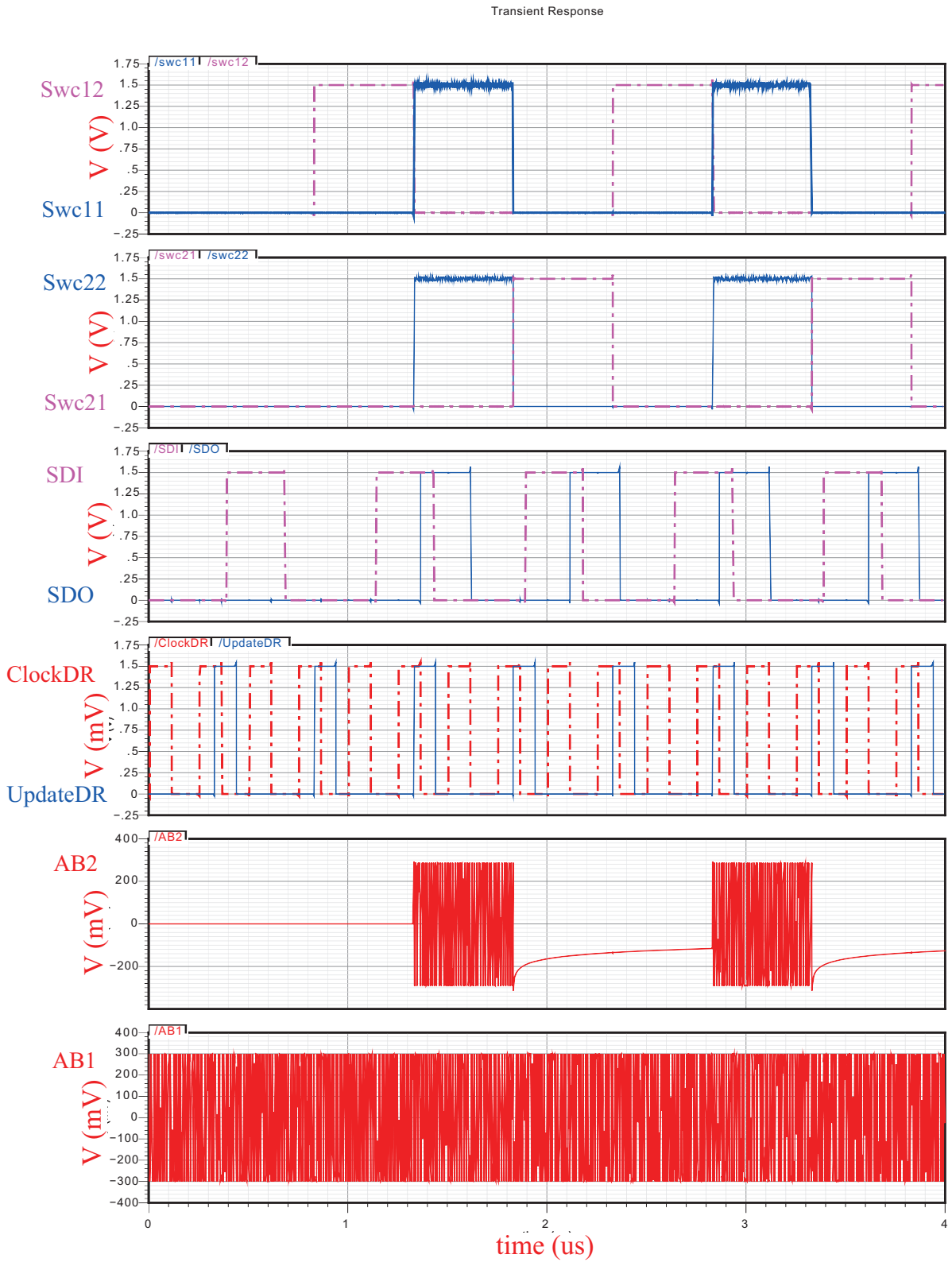


Fig. 3.28 Routing Signal from one ABM to the other ABM

ABMs was characterized through a Spectre simulation. Figures 3.29, 3.30 and 3.31 provides a characterization of the two-switch cascade from the perspective of its series on-resistance, linear range of operation and its AC frequency response. Comparing to the single analog switch, the ON resistance of two ABMs connected in series is about two to three times that found for a single switch. The input range for linear operation is reduced by a about 60 %, from $\pm 0.3V$ to $\pm 0.1V$.

The frequency response of the two-switch cascade appears to undergo the greatest change from a single-switch arrangement. The 3-dB point drop down to 2.75 GHz from 45.95 GHz. This is a lagre reduction AC performance but may still be suited for some high-frequency test applications.

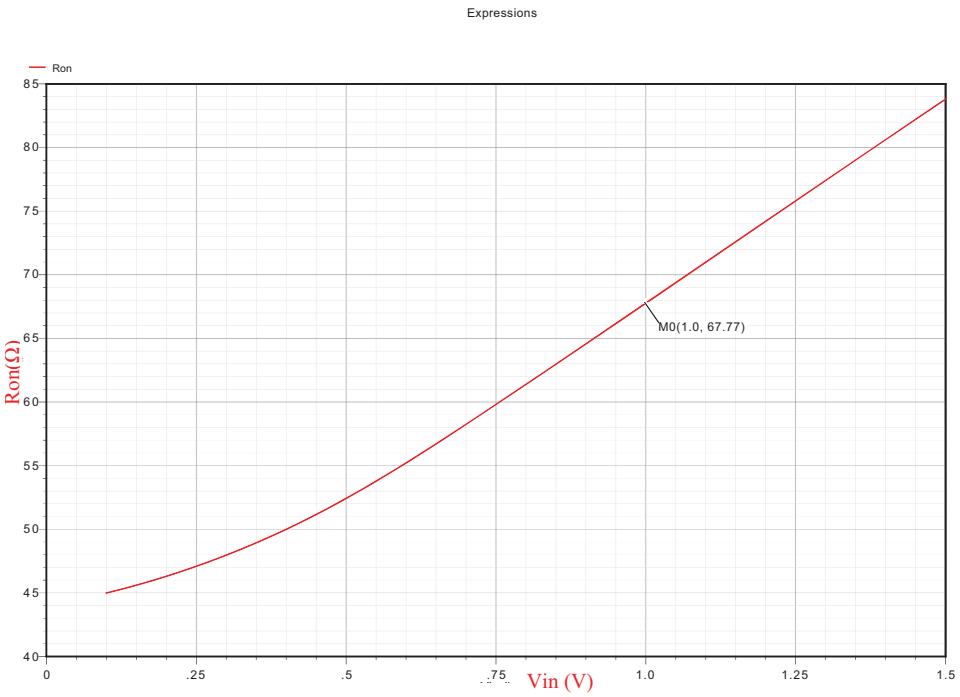


Fig. 3.29 ABM Switches' ON Resistance

3.7 Conclusion

The difficulty to probe and test circuit inside a 3D chip is one of the biggest impediments to the advancement of 3D technology. The analog boundary scan test approach is one possible approach to make analog inside a 3D chip. The simulation results of this chapter

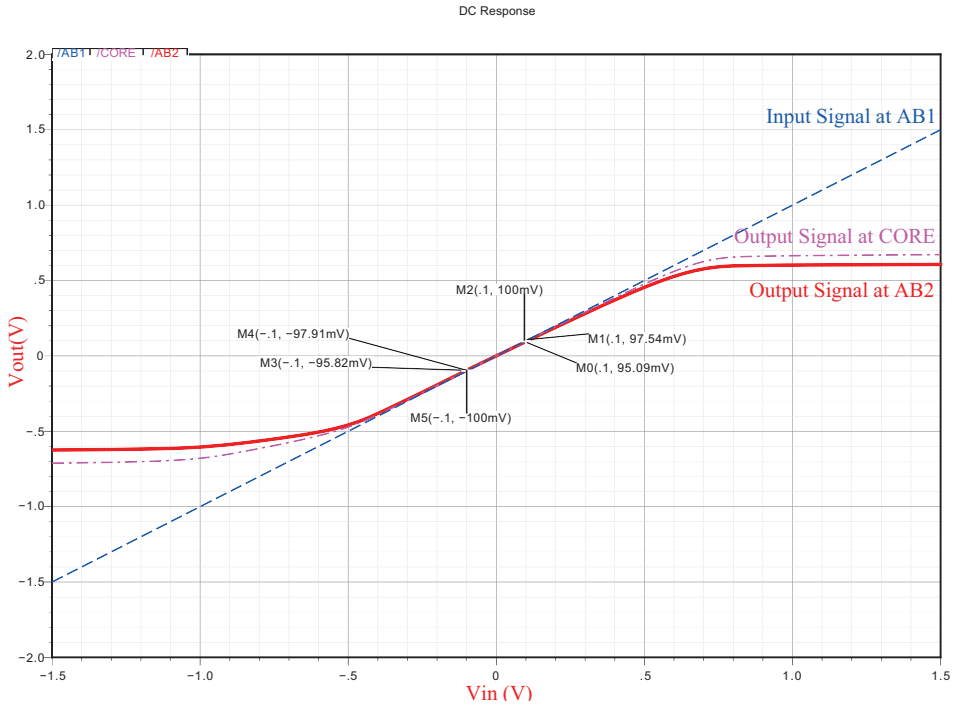


Fig. 3.30 ABM Switches' ON State Input Range

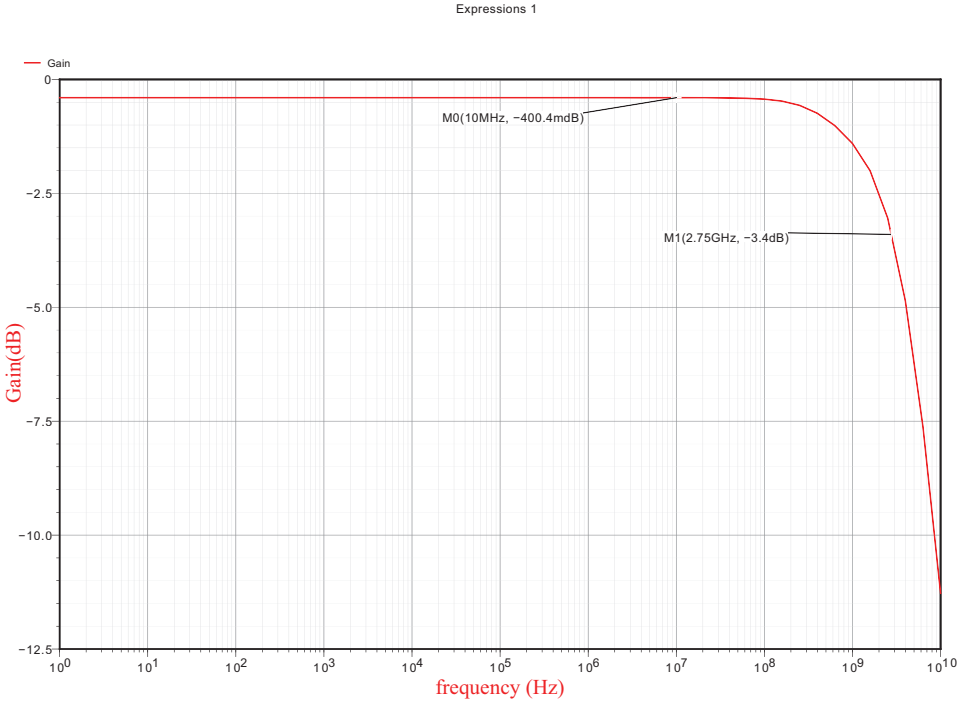


Fig. 3.31 ABM Switches Frequency Response

demonstrated that the analog boundary scan approach can be used for analog and high speed test of future 3D chips. Meanwhile, embedding JTAG or other DfT techniques on chip, or adding a complete test tier on chip may be the way to test more complicated chips, and probably the most efficient and economic way to performance 3D testing.

Chapter 4

Chip Overview Using The Tezzaron 3D Technology

In this chapter the physical details pertaining to the design of the 3D chip made from the Tezzaron technology will be described.

4.1 Chip Overview

In the prototype 3D chip from Tezzaron 3D technology, two silicon layers are to be constructed and bonded together. One layer contains the core circuits and will be referred to as the WTOP tier. The other layer will contain the analog boundary scan module (ABM) and will be referred to as the WBOTTOM tier. The Kelvin probe TSV resistance measurement circuit, the frequency-based TSV capacitance measurement (FBCM) circuit and the charge-based TSV capacitance measurement (CBCM) circuit will all be placed on the WTOP tier. The ABM circuit together with a few amplifier stages in cascade will be placed on the WBOTTOM tier. Fig.4.1 provides a pictorial representation of the two die stack and their corresponding circuit components. The two tiers will be bonded face-to-face as first described in Chapter 1 of this thesis (see Fig. 1.8). All I/O pads will be placed on the WTOP tier. Signals will be routed to the pads using the metal backside on the WTOP tier.

In the following, layout details for each tier will be provided as well as any new circuit information (e.g., ABM and op amp circuit).

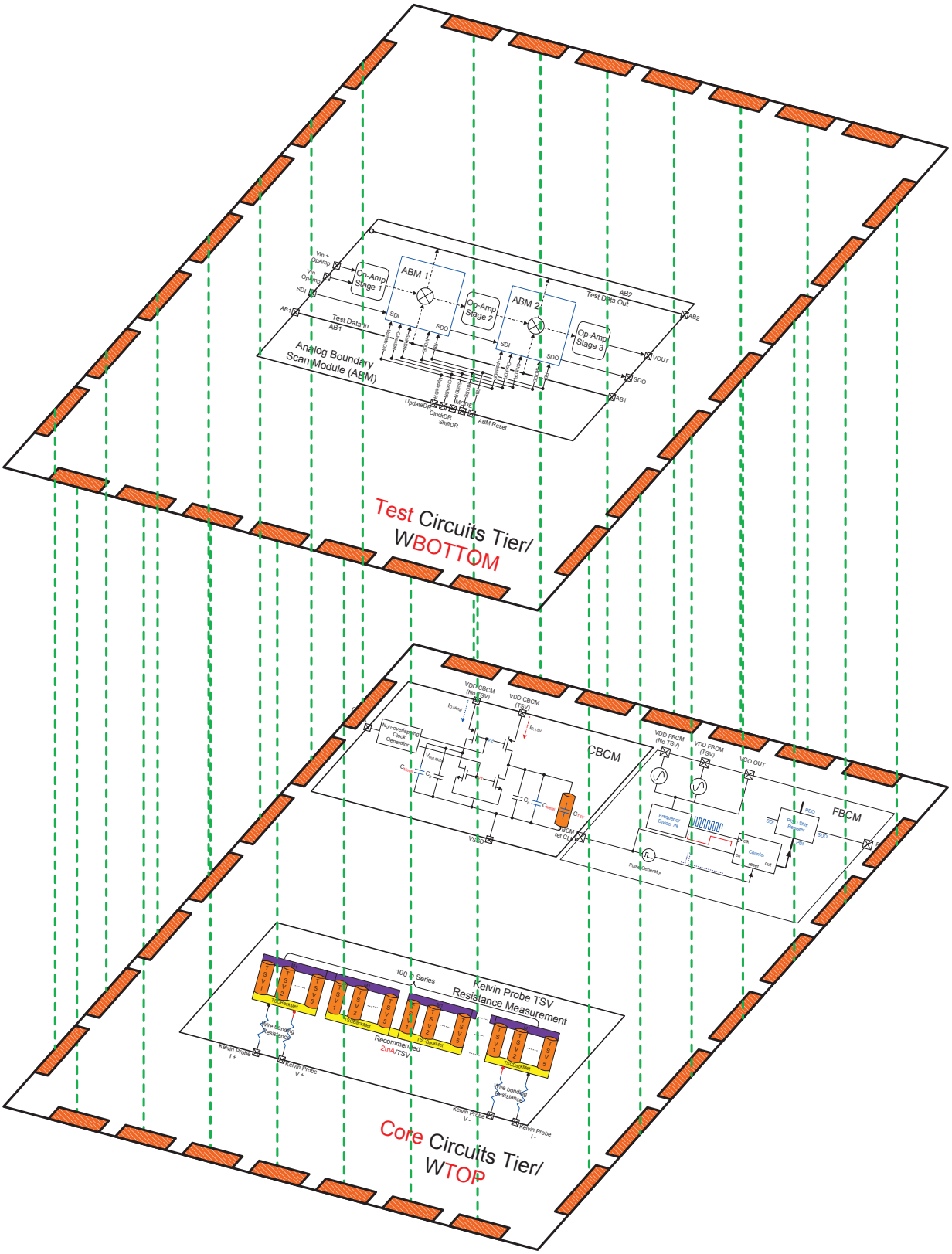


Fig. 4.1 Two Tier Layout Blocks Diagram

4.1.1 WTOP Tier Layout

The WTOP tier contains the FBCM and CBCM as well as the Kelvin probe circuits for the TSV characterization. In addition, a three-stage op-amp circuit is also included on the WTOP layer (more details on this in a moment). This amplifier will be used in conjunction with the ABM circuit found on the WBOTTOM tier. A Cadence view of the layout for this die is shown in Fig. 4.2.

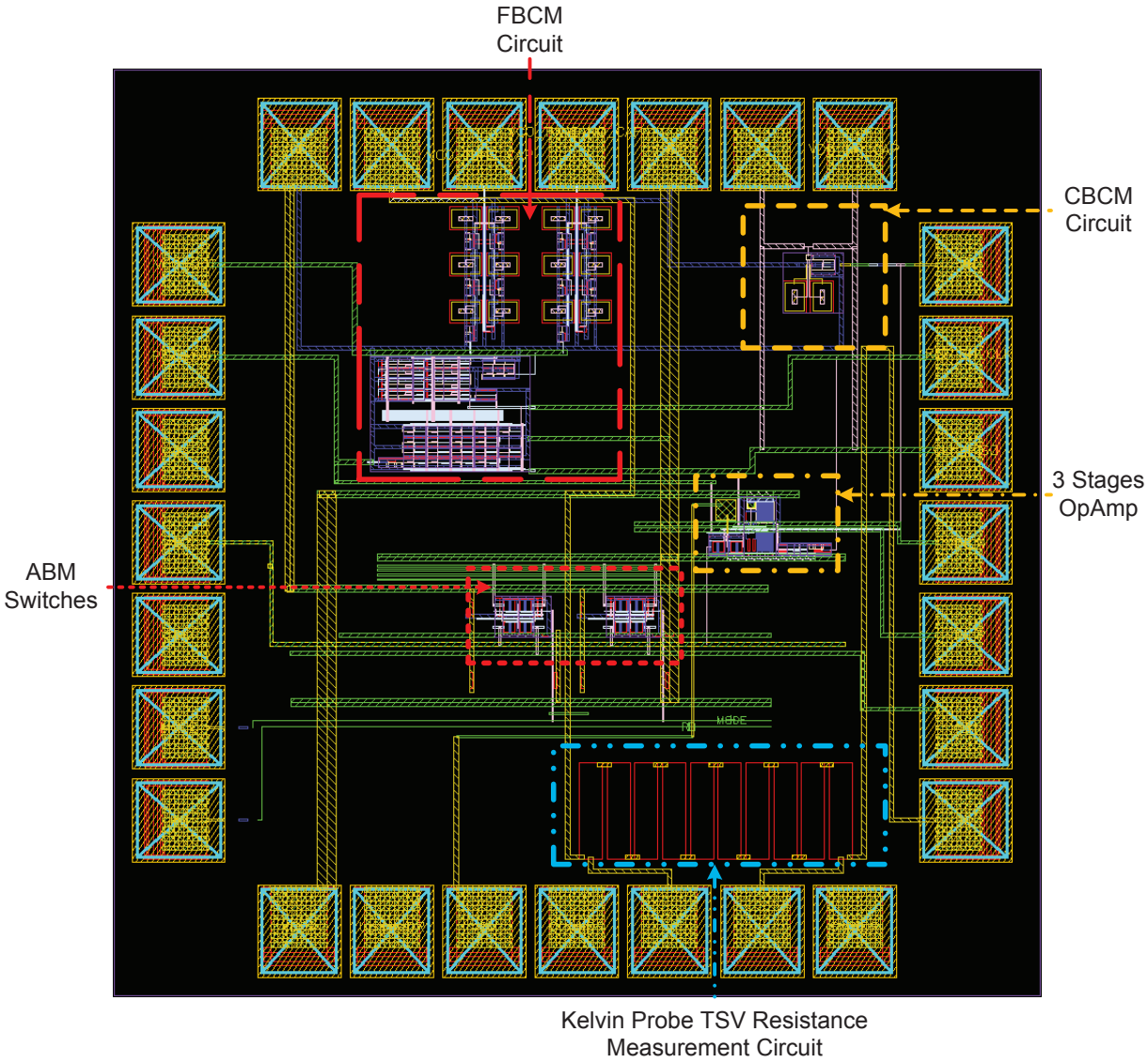


Fig. 4.2 WTOP Tier Layout With Each Circuit Component Identified

An expanded view of each circuit found on this tier is provided below.

TSV Capacitance Formation Layout

The TSV capacitance is formed in the way as illustrated in Fig. 4.3. Connections are made to the middle TSV and all other TSVs are connected to ground.

Frequency-Based TSV Capacitance Measurement Layout

The frequency-based TSV capacitance measurement circuit schematic and layout is shown in Fig. 4.4.

Charge-Based TSV Capacitance Measurement Layout

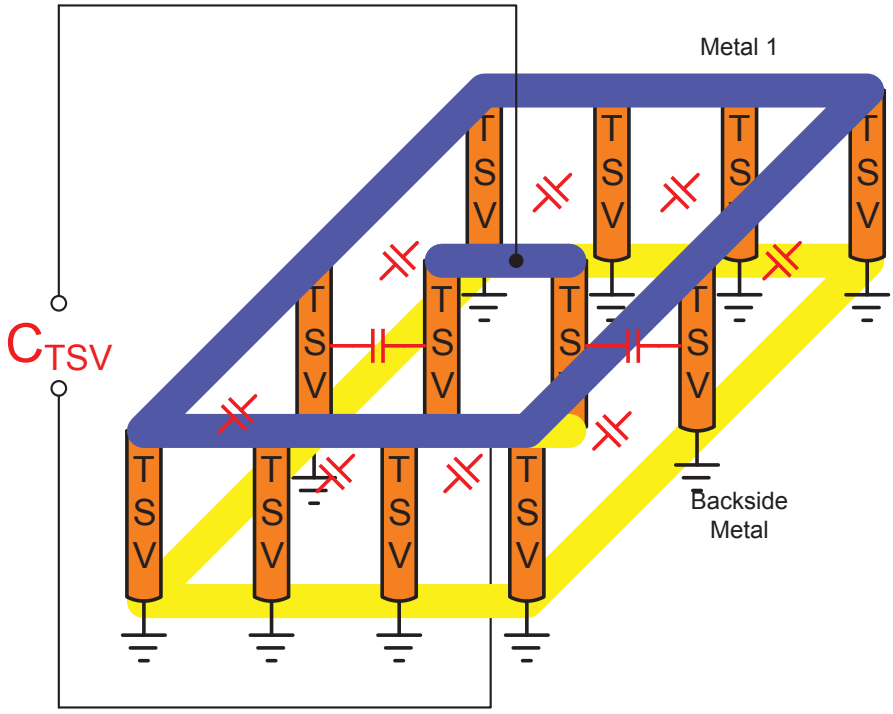
The charge-based TSV capacitance measurement schematic and layout is shown in Fig. 4.5. The pseudo inverter and TSV capacitors are placed in a symmetrical arrangement for parasitic matching purposes.

Three-Stage Op-Amp Layout

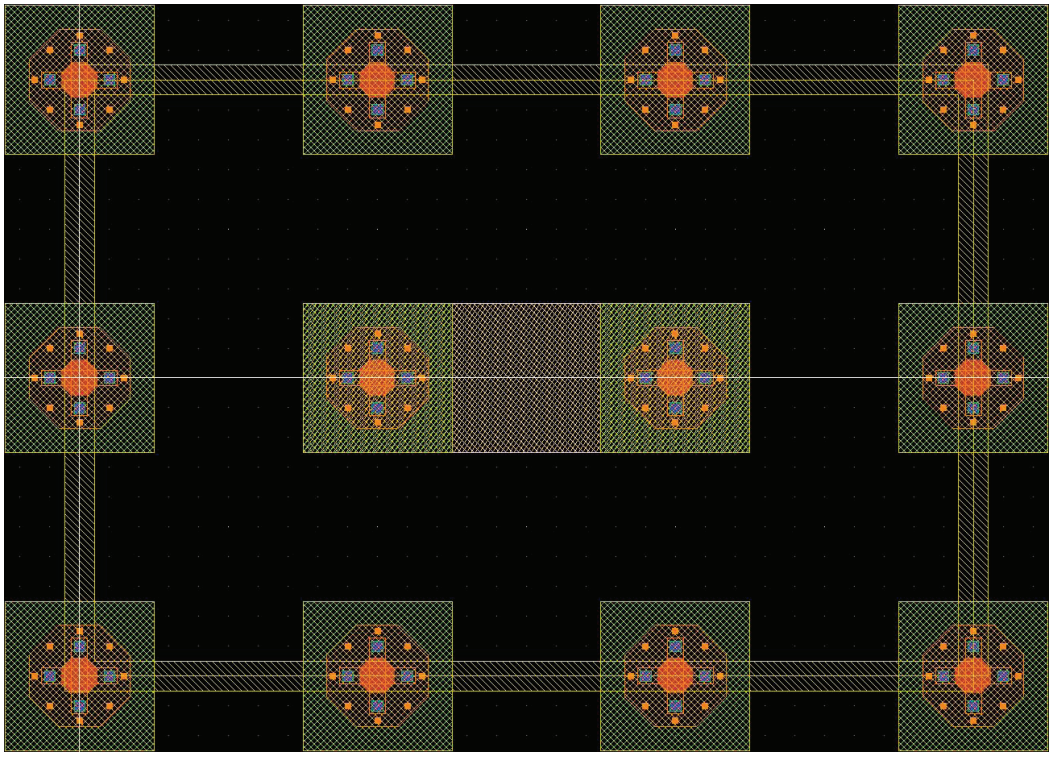
The three-stage Op-Amp is used as the circuit under test (CUT) to verify the functionality of the ABMs. The schematic and layout are illustrated in Fig. 4.6. The first stage is constructed as a diff-pair, and the second and third stages are made from common source amplifiers. The ABM is connected between the stages, where the red dash lines denoted as *stages connection* are shown in Fig. 4.6.

4.1.2 WBOTTOM Tier Layout

The analog boundary scan module (ABM) is the sole component on the WBOTTOM tier. This circuit interacts with the three-stage op-amp found on the WTOP tier. A view of the schematic and layout for this die is shown in Fig. 4.7. Other circuits can easily be added to this die, if the need arises.

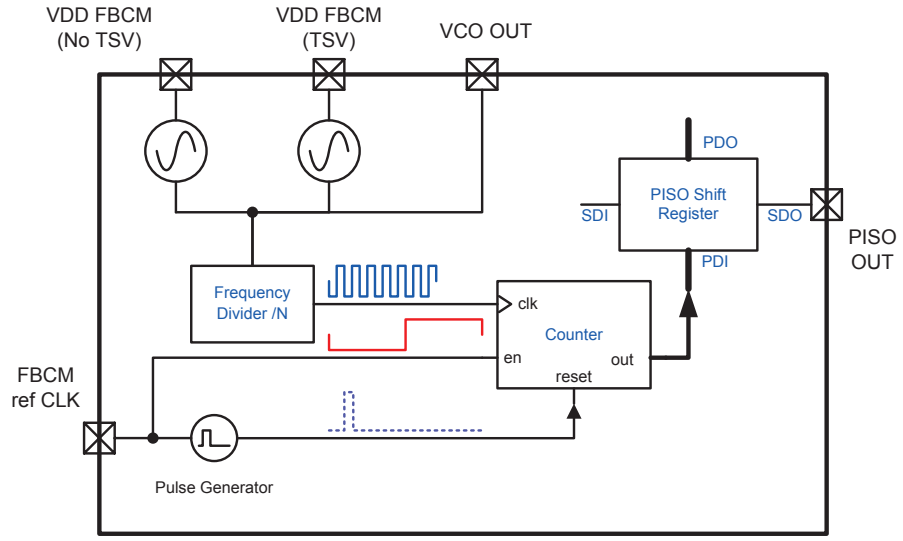


(a) Schematic View

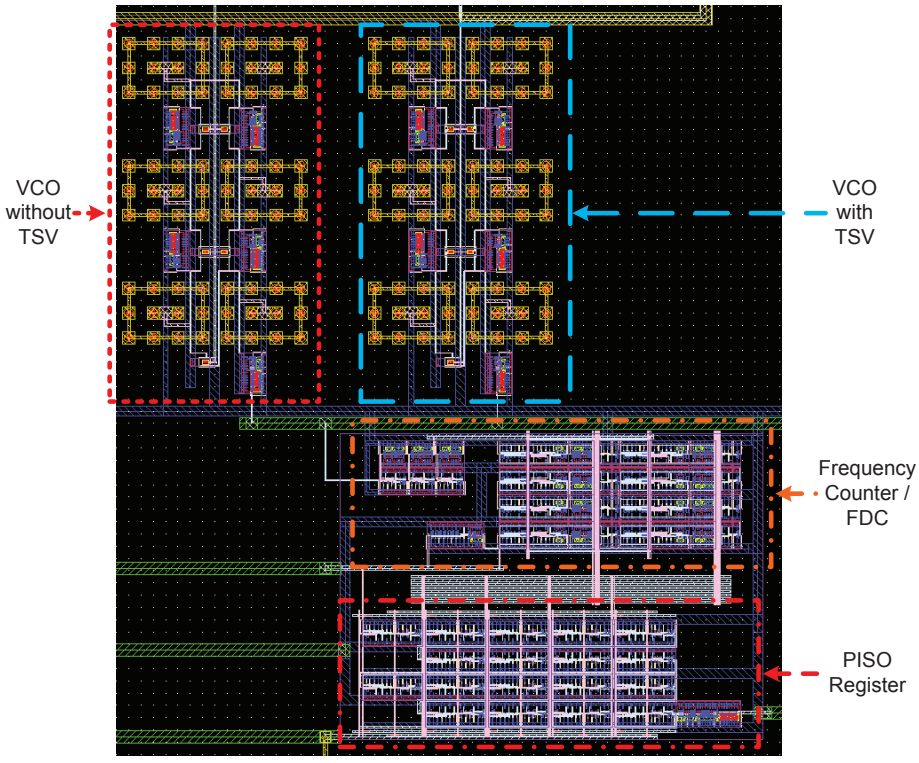


(b) Cadence Layout View

Fig. 4.3 TSV Capacitor Formation

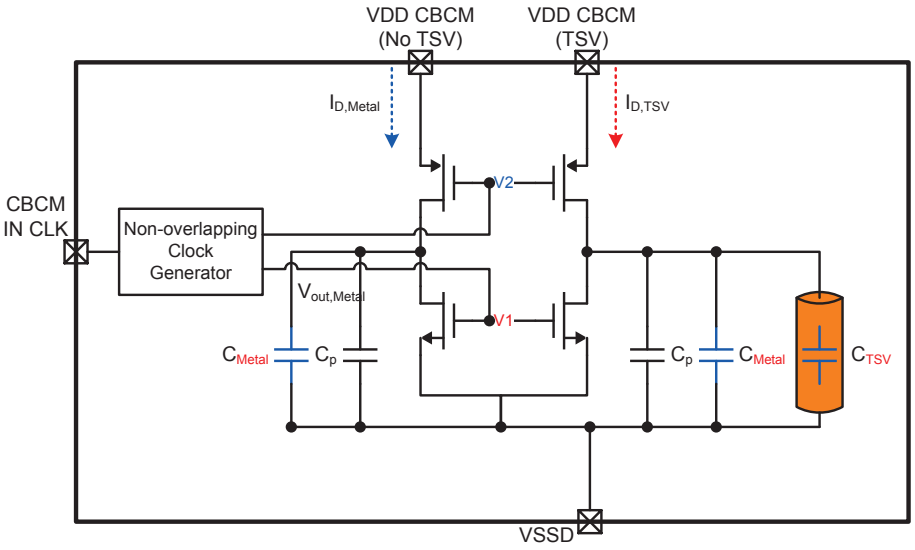


(a) Schematic View

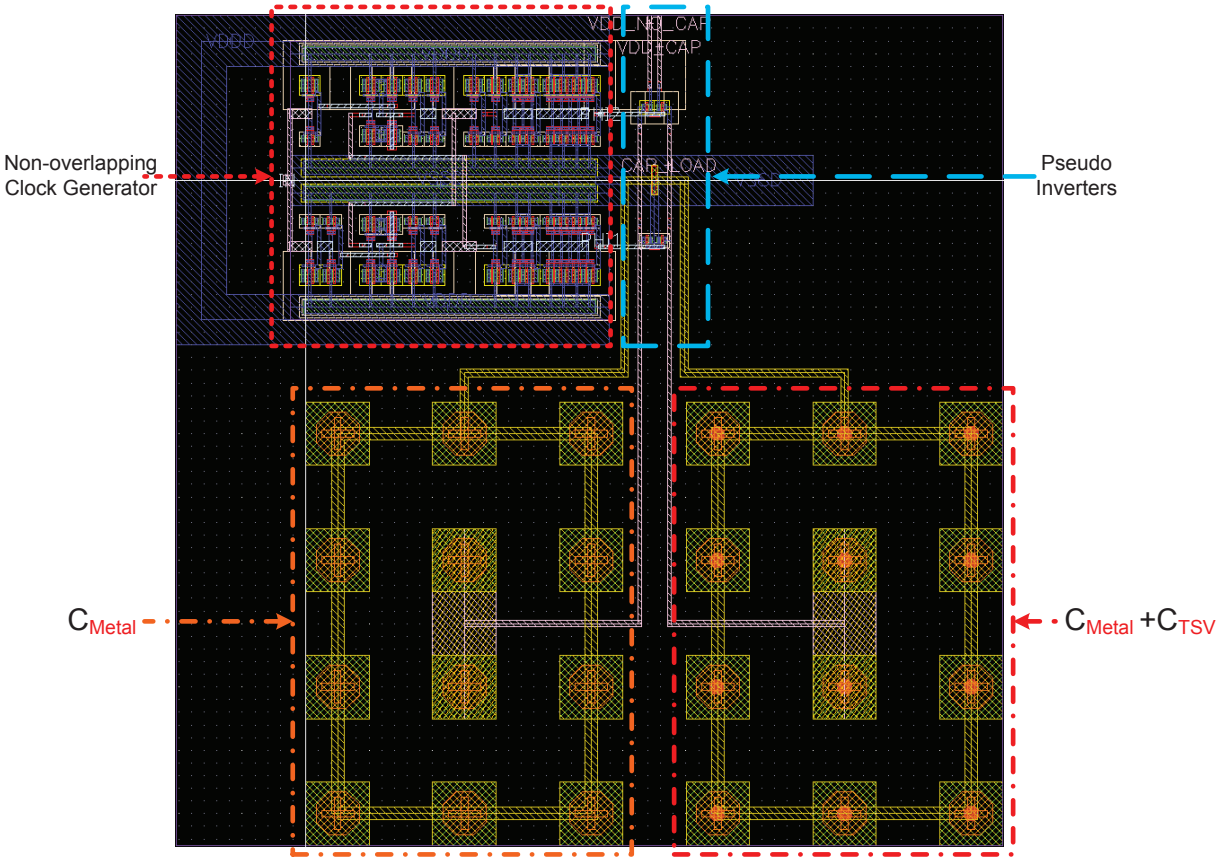


(b) Cadence Layout View

Fig. 4.4 The FBCM Embedded Instrument

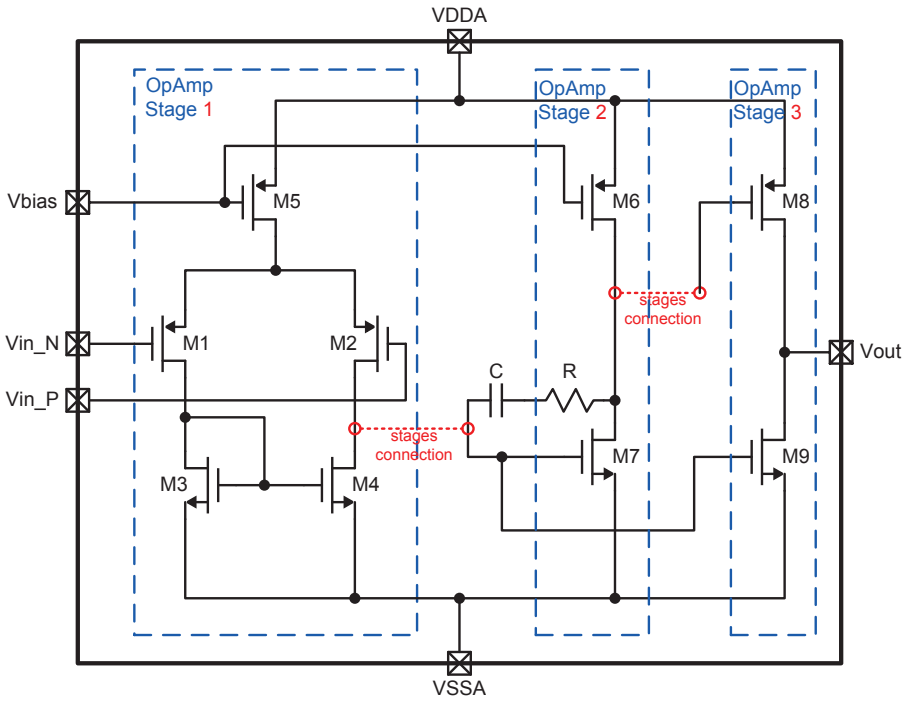


(a) Schematic View

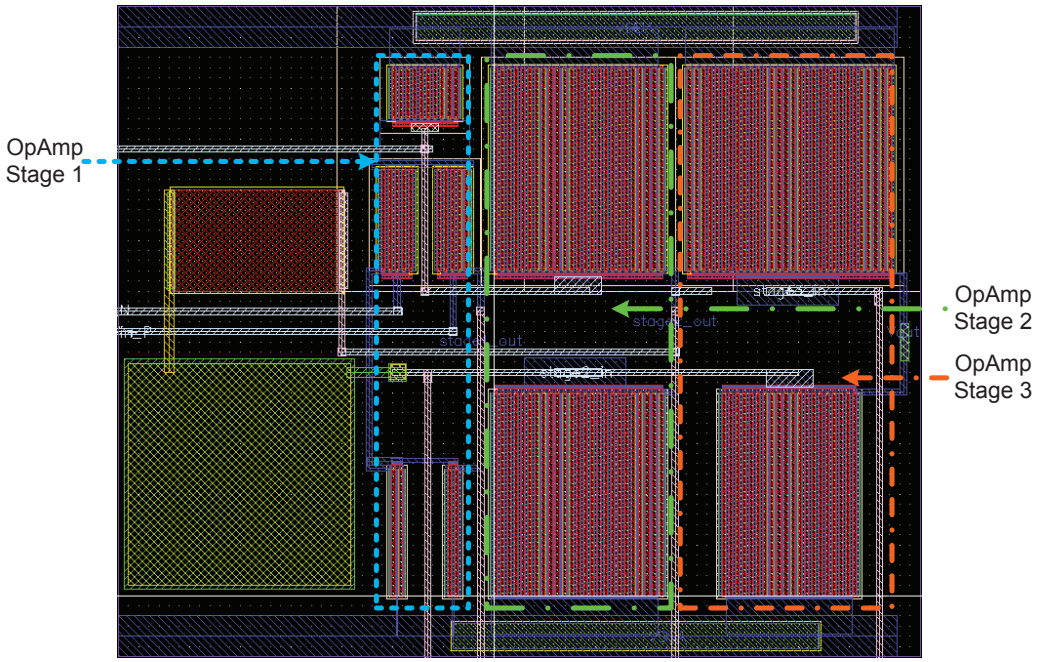


(b) Cadence Layout View

Fig. 4.5 The CBCM Embedded Instrument



(a) Schematic View



(b) Cadence Layout View

Fig. 4.6 Three-Stage Op-Amp Circuit

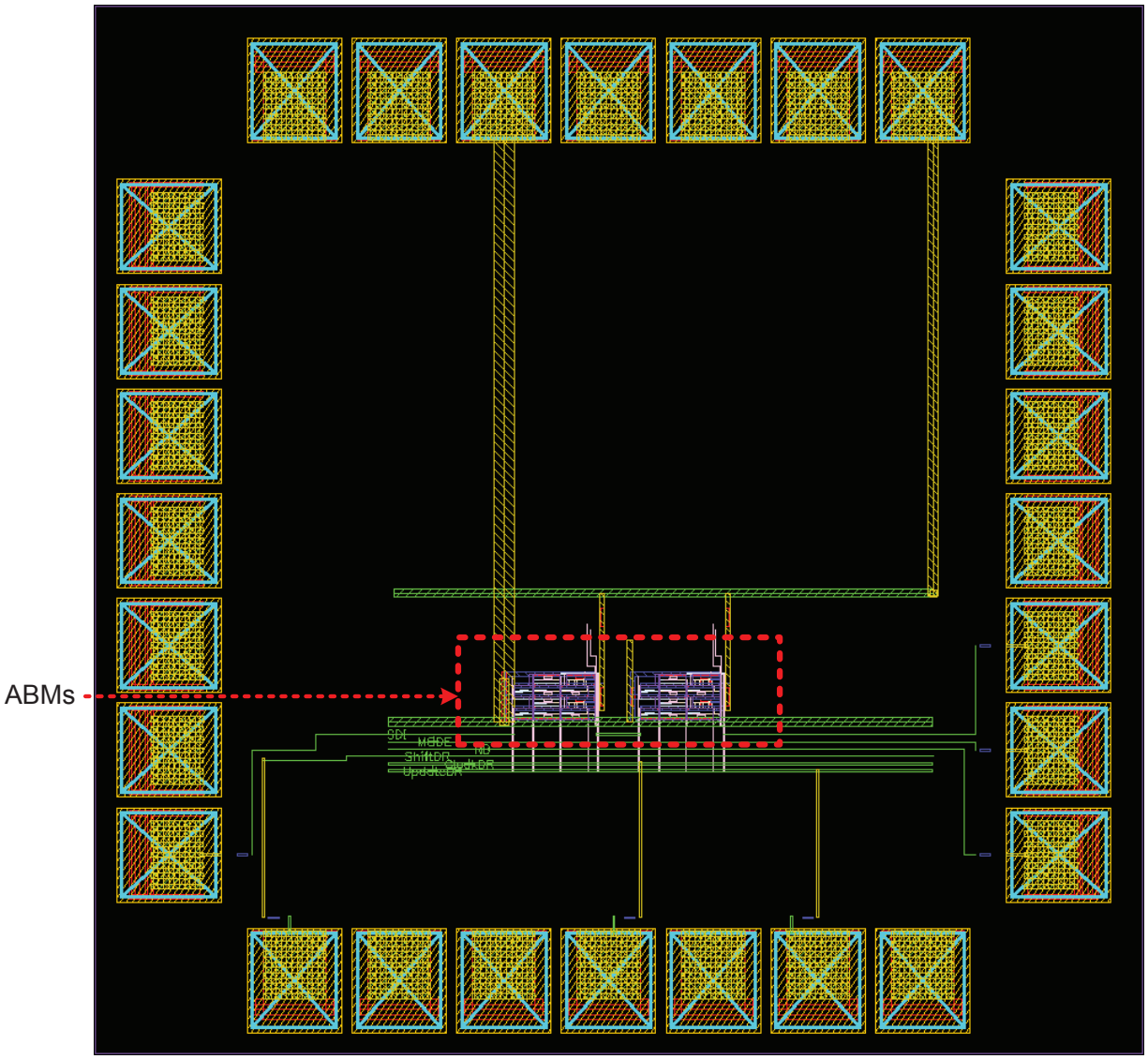


Fig. 4.7 WBOTTOM Tier Layout With Each Circuit Component Identified

4.2 User Pad/Pin Connections

Since we have only 28 bonding pads in total to interface the 3D chip to the outside world, we had to reuse some pads for several different functions. Through a power down option designed in the chip, some circuits are shut down while others are using a shared IC pad. For example, the connections *SDI* for the input serial data pad for the analog boundary scan circuit and *Kelvin probe V +* port of the four-port Kelvin probe measurement circuit both share the same pad/pin of the IC. The complete pad/pin arrangement is illustrated in Fig. 4.8.

4.3 Conclusion

A physical description of the two tiers of the 3D chip implemented in the Tezzaron 3D technology is described. The chip prototype is divided into a core circuit (WTOP) tier and a test circuit (WBOTTOM) tier. The WTOP tier includes circuits for the frequency-based capacitance measurement, charge-based capacitance measurement, Kelvin probe TSV resistance measurement circuits and a three-stage op-amp circuit. On the WBOTTOM tier, the analog boundary scan module is placed. Due to the pad limitations, the pads were reused for different measurement functions.

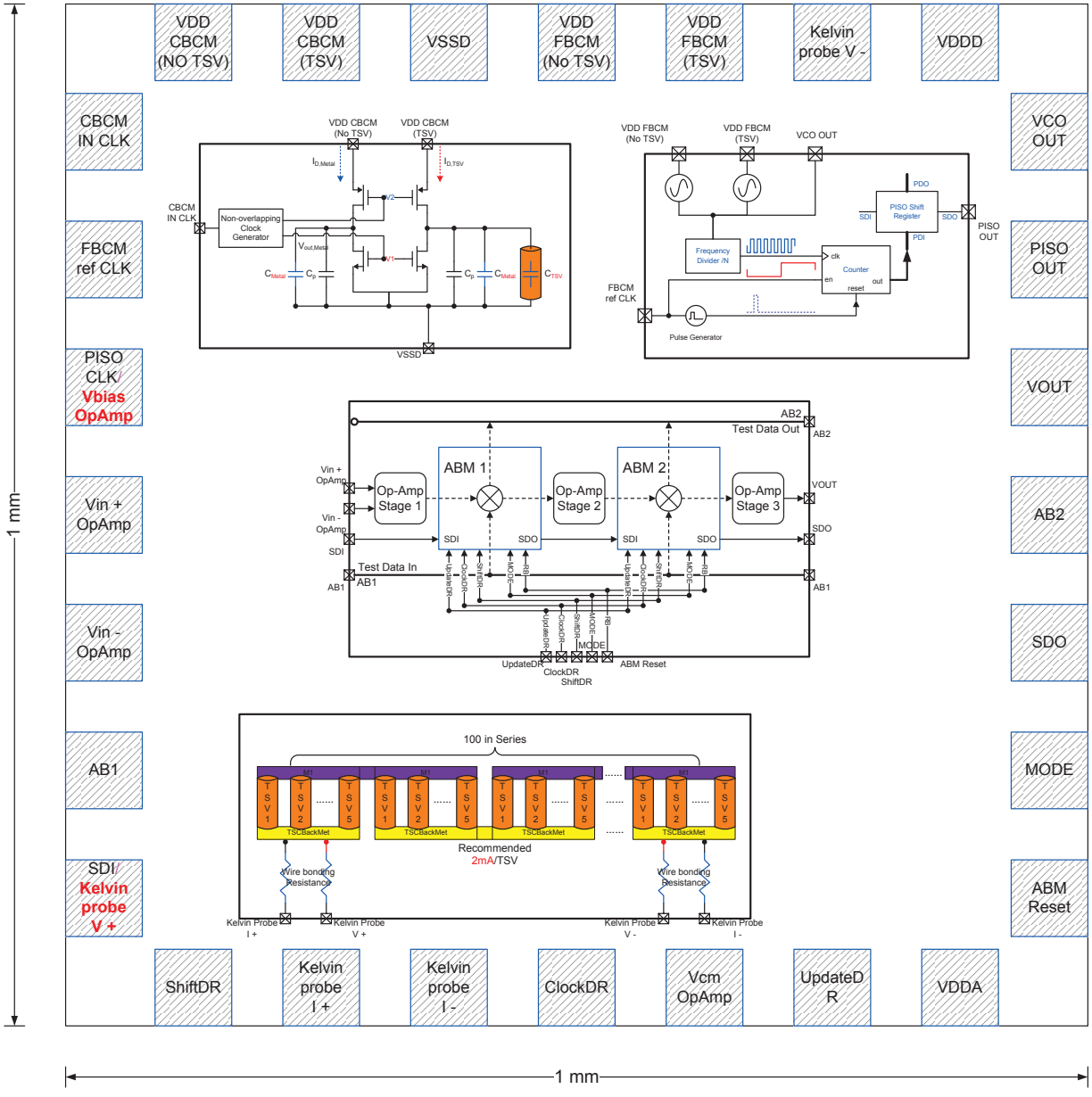


Fig. 4.8 3D-Chip Pad/Pin Connections

Chapter 5

Experimental Setup And Measured Results

This chapter was intended to describe the experimental setup and results gather from testing the prototype chip. Unfortunately, time to submit the thesis for evaluation has come to an end after almost three years of work on this 3D chip development (more on this in a moment). As a result, only the test setup will be provided in this chapter.

5.1 Reason For Chip Delay

Due to technical problems with the Tezzaron®design kit provided by the Canadian Microsystems Corporation (CMC), the chip prototype did not get fabricated in a timely manner. The first version of the chip was submitted for fabrication on October 20th, 2011. On December 20th, 2011 a request from CMC to alter the design to incorporate additional changes to the backside metal layer. Due to internal delays at CMC, the final version of the chip was not sent to CMC for fabrication until March 23rd, 2012. In it is now our understanding that the fabricated chip in a 2-die stack formation is to return sometime in the middle of August, 2012. As the final date of thesis submission for this candidate is mid-July, 2012, this thesis is submitted without any experimental data. Nonetheless, the thesis does provide important engineering insight into the development of a 3D-chips. For this reason, the thesis should be capable of standing on its engineering merits without the luxury of experimental data. The situation is summarized in the Table 5.1.

Table 5.1 Tezzaron 3D-IC Time Schedule

Time	Mission
Octorber 20th, 2011	Initial chip submission.
December 20th, 2011	Modify backside metal layer due to the request from CMC and MOSIS.
March 23rd, 2012	Chip submitted to fab.
Mid-August, 2012	Chip is expected to come back.

5.2 Experimental Setups

The prototype chip is a two-die stack of two 1 mm by 1 mm dies. The overall functionality of the chip is divided into 4 parts: the charge-based TSV capacitance measurement (CBCM) circuit, the frequency-based TSV capacitance measurement (FBCM) circuit, the analog boundary scan module (ABM) circuits and the Kelvin probe TSV resistance measurement circuit. Since the 4 parts of the prototype chip are independent to each other, we can power and set up the measurement for each of them separately. This section will provide the measurement set up for each subsystem. As a reminder, the I/O pin placement was provided previously in Fig. 4.8.

5.2.1 TSV Resistance Measurement

The TSV resistance is measured with a four-port Kelvin probe configuration. The Keithley 2400 series source meter is used provide the four-point probe connection and measurement. The test setup is illustrated in Fig. 5.1.

5.2.2 Frequency-Based TSV Capacitance Measurement

In the frequency-based TSV capacitance measurement (FBCM) method, there are two ways of making a measurement. One way is to measure the frequency of both the TSV-loaded and non-TSV loaded VCO using an external oscilloscope, one step at a time. The other way is to capture the frequency count provide on-chip through the internal shift register. Both ways are used in our measurement. The VCOs in the FBCM method are powered by the Agilent E3648A dual output DC power supplies but only one VCO is powered up at one time. The Agilent 33250A 80 MHz function generator is used to provide the reference clock signal for the frequency counter and the LeCroy SDA 6000 is used to capture and

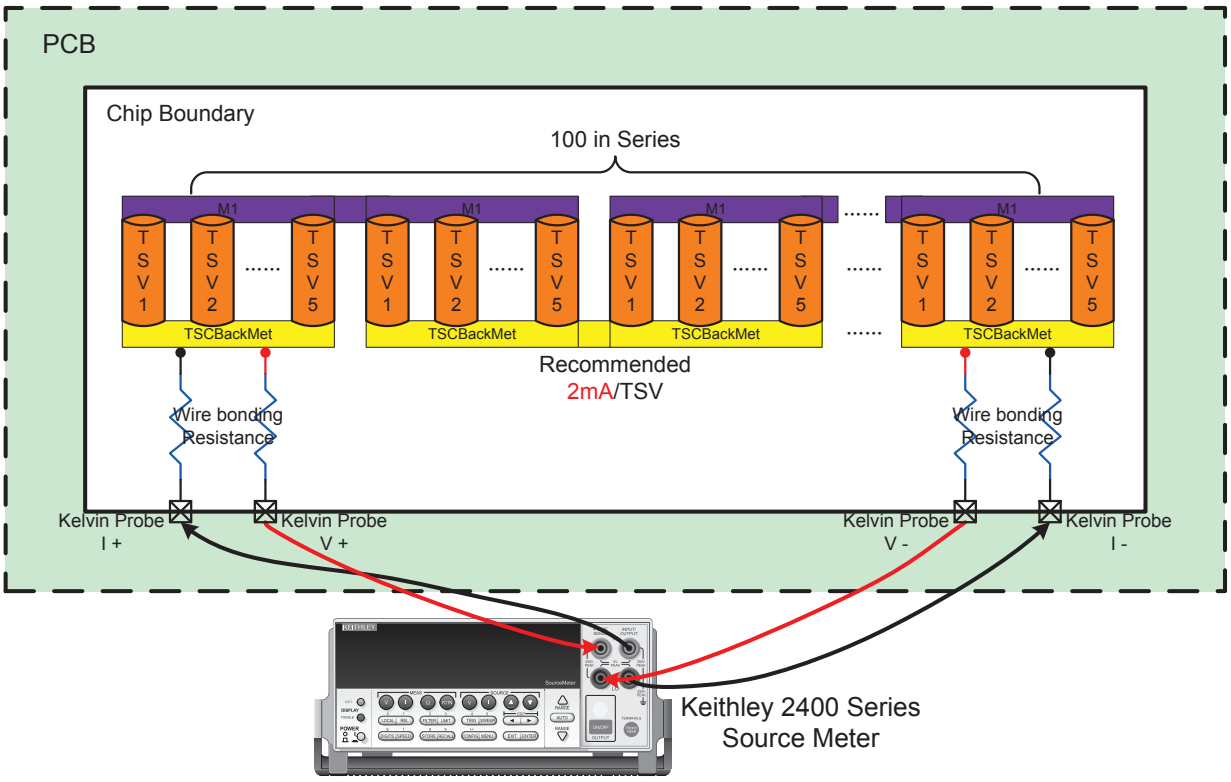


Fig. 5.1 TSV Resistance Measurement Set Up Using An Keithley 2400 Series Source Meter

analyze the output data. The test set up for the FBCM method is shown in Fig. 5.2.

5.2.3 Charge-Based TSV Capacitance Measurement

The crucial part of this capacitance measurement method is extracting the average difference charging (or discharge) current to the CBCM circuit. To do this two Keithley 2400 series source meters are connected to the CBCM circuit; one for each pseudo inverter leg. The clock used to control the charging/discharging frequency is controlled by the Agilent 33250A 80 MHz function generator. The test set up is shown in Fig. 5.3.

5.2.4 Analog Boundary Scan Module Measurement

This measurement is trying to demonstrate the analog signal accessibility of the analog boundary scan modules (ABMs) in a 3D-IC test. Two ABMs are place between each stage of a 3-stages op-amp. The Teradyne FLEX tester available at McGill University will be used to generate the control bits for ABM and the Agilent 33250A 80 MHz function generator will provide the input analog signal. The LeCroy SDA 6000 will be used to capture both the analog and digital data at the output. The entire set up is shown in Fig. 5.4.

5.3 Summary

This chapter provides the various test set ups for the various circuits placed on the prototype 3D chip. Owing to internal delays at CMC and their suppliers, the 3D-chip is not expected back until mid-August 2012, too late to perform measurements and include in this thesis.

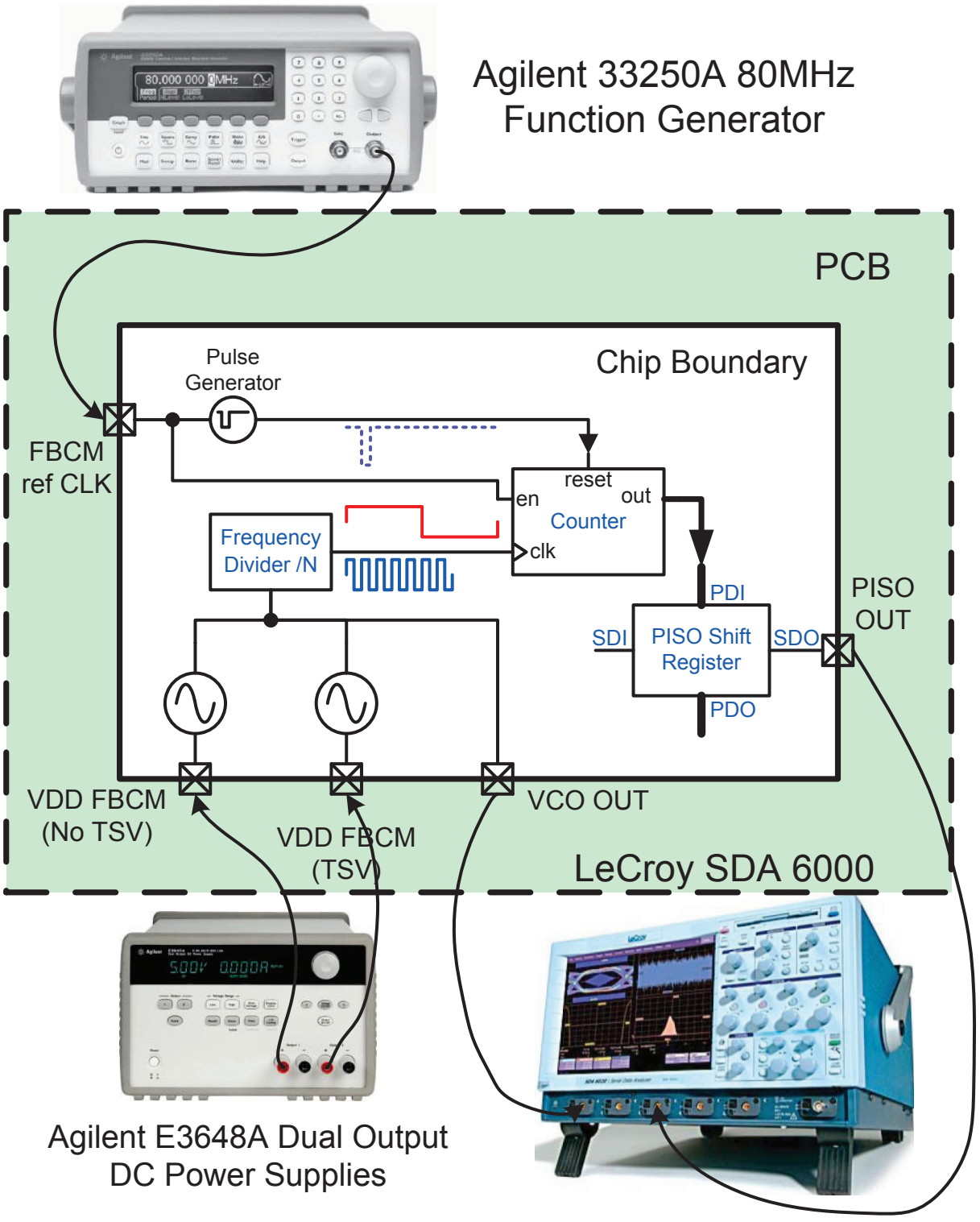


Fig. 5.2 Frequency-Based TSV Capacitance Measurement Set Up

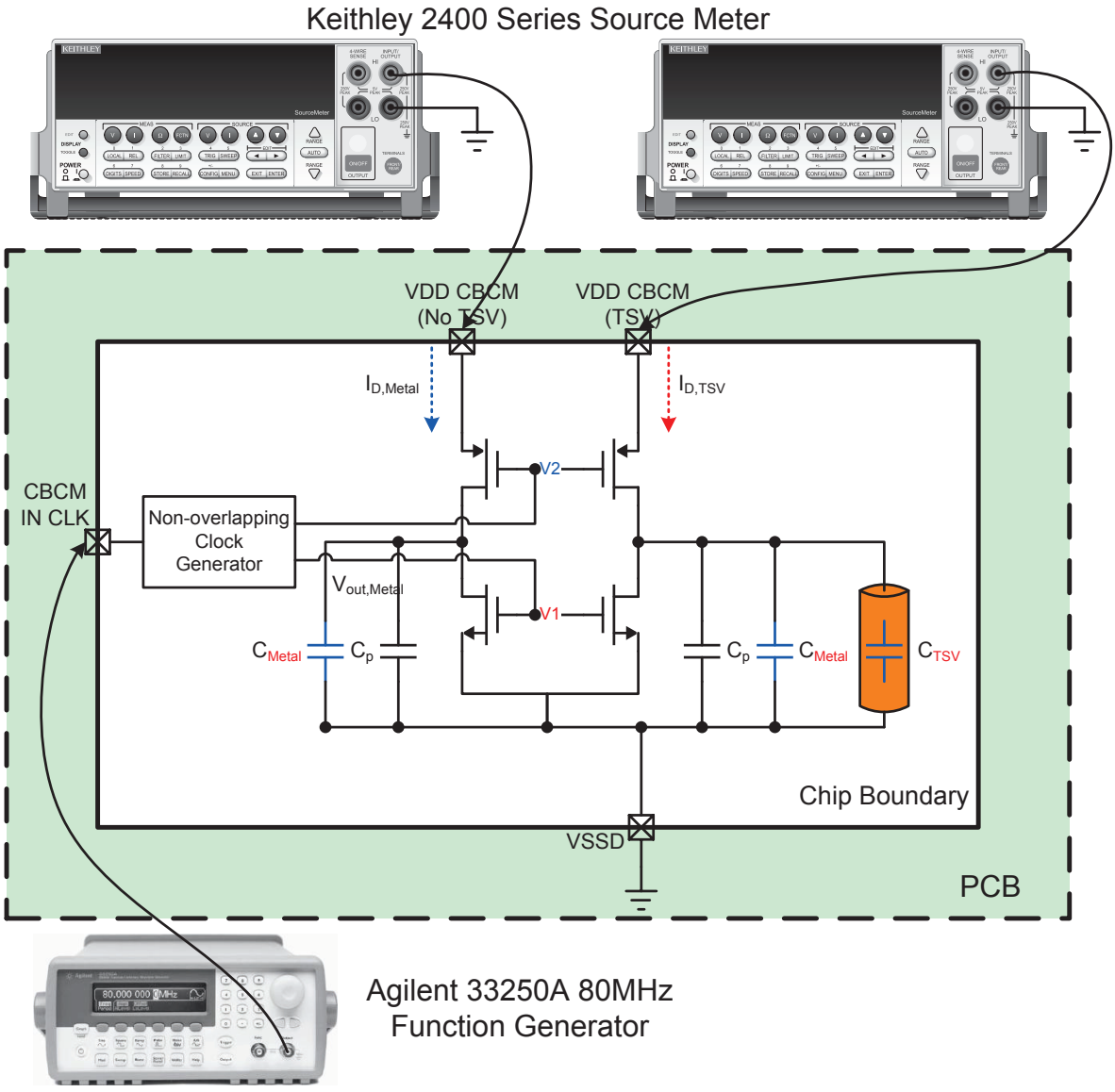


Fig. 5.3 Charge-Based TSV Capacitance Measurement Set Up

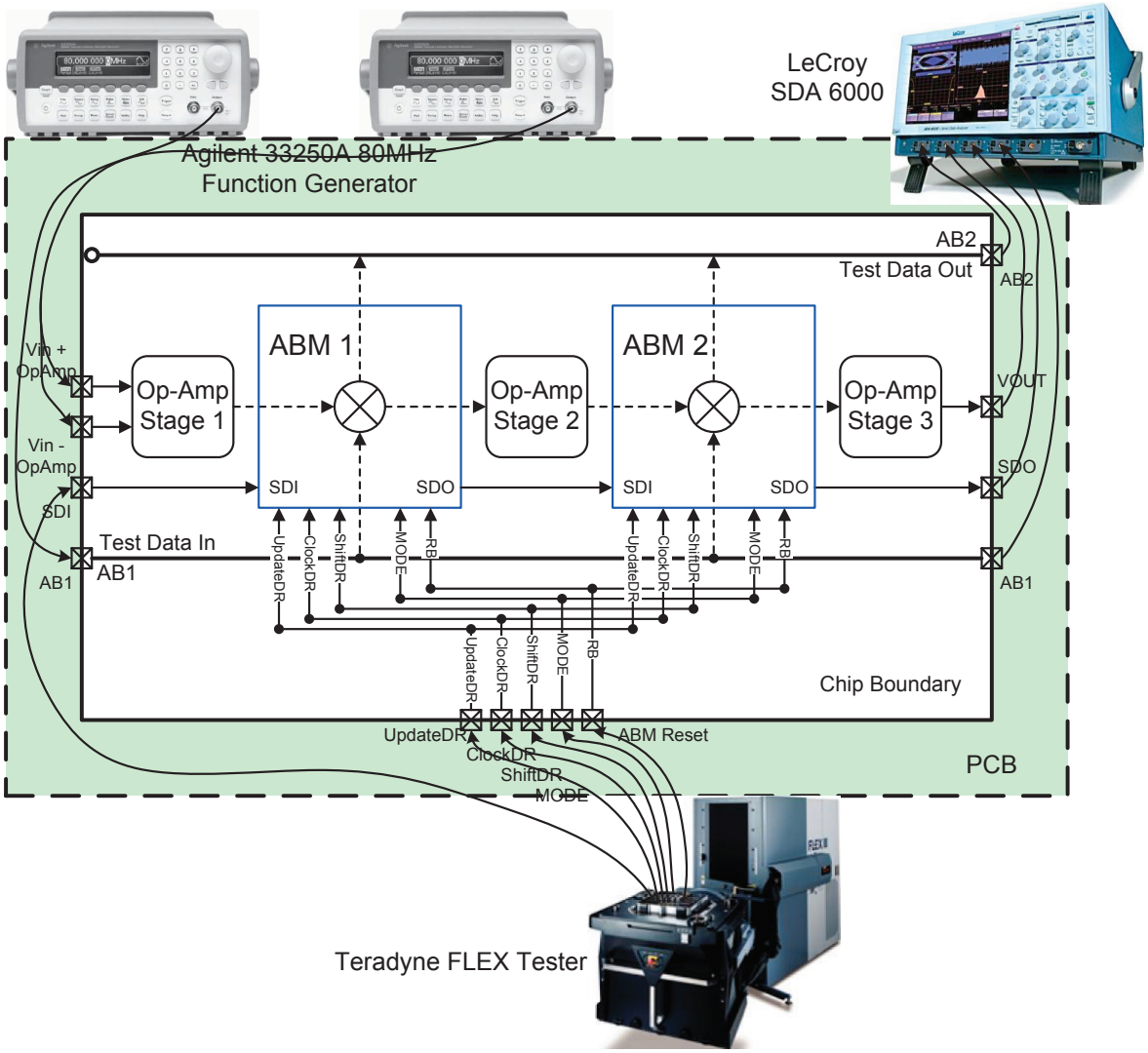


Fig. 5.4 Analog Boundary Scan Module Measurement Set Up

Chapter 6

Conclusion

As Moore's law appears to be reaching its limit, the semicondutor industry is beginning to turn from *More Moore* to a *More-than-Moore* paradigm. Constructing ICs using a 3D structure using Thru-Silicon Vias (TSVs) is consider the front-runner for a *More-than-Moore* approach. Like all things that are new, a 3D-IC technology proposes many challenges. One involves the TSV itself, as its dimensions and electrical attributes varies immensely from one technology to another. To speed up the development of the 3D-IC technology, this dissertation is focused on creating a set of embedded instruments coupled together using an industry standard JTAG test bus that will enable the characterization of TSVs in any technology.

Most of the literatures describe methods to measure the capacitance of a TSV using an external LC meter. This kind of measurement can be classified as a low-frequency measurement, and does not provide sufficient information about the TSV at high frequencies; in a frequency regime that is critical for high-speed digital applications and for RF circuit design. In this thesis, two methods of TSV capacitance measurement is provided: the frequency-based capacitance measurement (FCBM) method and the charge-based capacitor measurement (CBCM) method, both of which overcome the LC meter's frequency limitation. Moreover, both of these two method have been shown through simulation of reaching fF accuracy. Beside the TSV capacitance extraction, the TSV resistance is also extracted by a 4-point Kelvin probe method. The dissertation concludes with a description of the JTAG test bus that was created to allow external instruments to control and extract the measured data found on chip. This approach is believe to be important for accessing

analog and mixed-signal information associated with a 3D-IC. Finally, the thesis concludes with the idea of an "ATE-on-a-Layer" whereby a single tier is reserved exclusively for test purposes.

6.1 Thesis Summary

This thesis began in Chapter 1 with an introduction to 3D-IC technology where through-silicon vias and the 3D process was described. Some technology details for the Tezzaron 3D process was also provided in this chapter.

Chapter 2 introduced several methods for extracting the resistance and capacitance of a TSV in the Tezzaron 3D-IC process. A frequency-based direct capacitance measurement approach and a charge-based capacitance measurement was described for extracting the capacitance. A Kelvin four-point probe technique was used to extract the series resistance of the TSV.

Chapter 3 describes a JTAG DFT technique to transfer off-chip the information captured by the embedded instruments described in Chapter 2. A new JTAG cell for analog/ mixed-signal testing was proposed in this chapter.

Chapter 4 presents the physical details pertaining to the design of the 3D chip made from the Tezzaron technology.

Chapter 5 describes the experimental setup for testing the prototype 3D-chip. This chapter should have provided experimental results as well, but unfortunately, due to manufacturing delays, the chip has not yet returned from fabrication.

6.2 Future Work

In the future, a method to characterize the inductance of a TSV directly on chip should be pursued. This will provide a more complete model of TSV signal integrity. This may draw much more attention from RF circuit community and help to push 3D-IC technology forward much faster.

Analog switches in the JTAG implementation consumes lots of silicon area. Alternative approaches to achieving the same functionality without the use of the analog switches would help to reduce the cost overhead of DFT on any design in a 3D-IC.

Finally, attempting to incorporate all the embedded instruments on a single tier of a

3D-IC would provide an *ATE-on-a-Chip* that could be standardized across the industry and help to facilitate test and reduce test costs significantly.

Appendix A

Test Bench Schematics

All the Cadence schematics of test bench circuits are illustrated and listed in this appendix.

A.1 Frequency-Based Capacitance Measurement Method Test Bench

The frequency-based capacitance measurement method test bench is showed in Fig.A.1. It includes a five-stage VCO, a frequency divider, a pulse generator, an up counter, a PISO and an ADC.

A.2 Charged-Based Capacitance Measurement Method Test Bench

The charged-based capacitance measurement method test bench is illustrated in Fig.A.2. It includes a pseudo inverter pair, non-overlapping signal generator and a loading capacitor.

A.3 Analog Boundary Scan Module Test Bench

The ABM test bench is showed in Fig.A.3. There are two AMBs connected in serial and signal source passing the buffers.

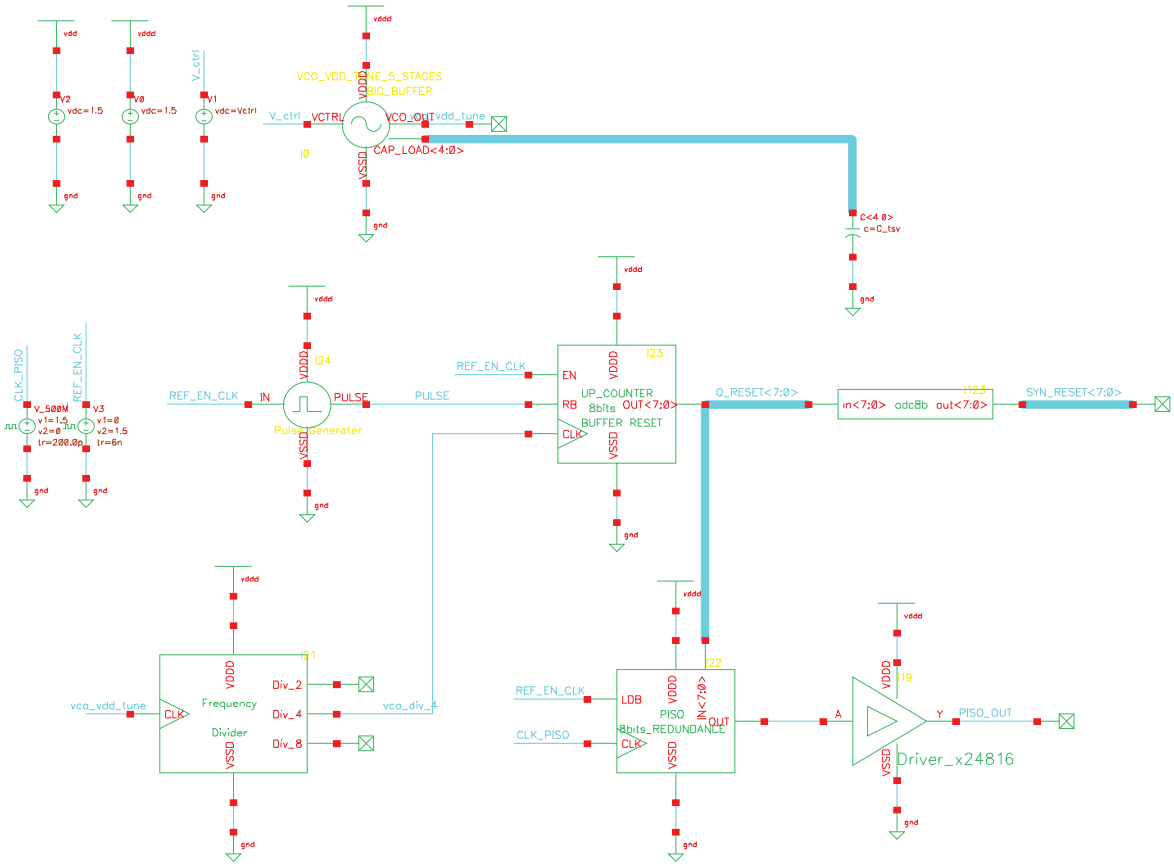


Fig. A.1 Test Bench for Frequency Based Capacitance Measurement Method

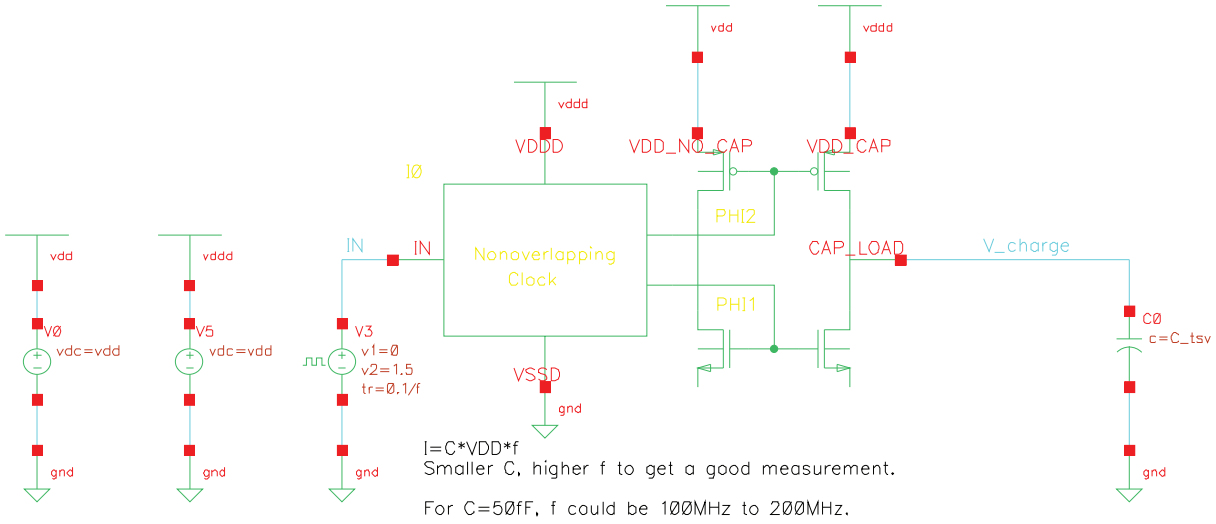


Fig. A.2 Test Bench for Charged Based Capacitance Measurement Method

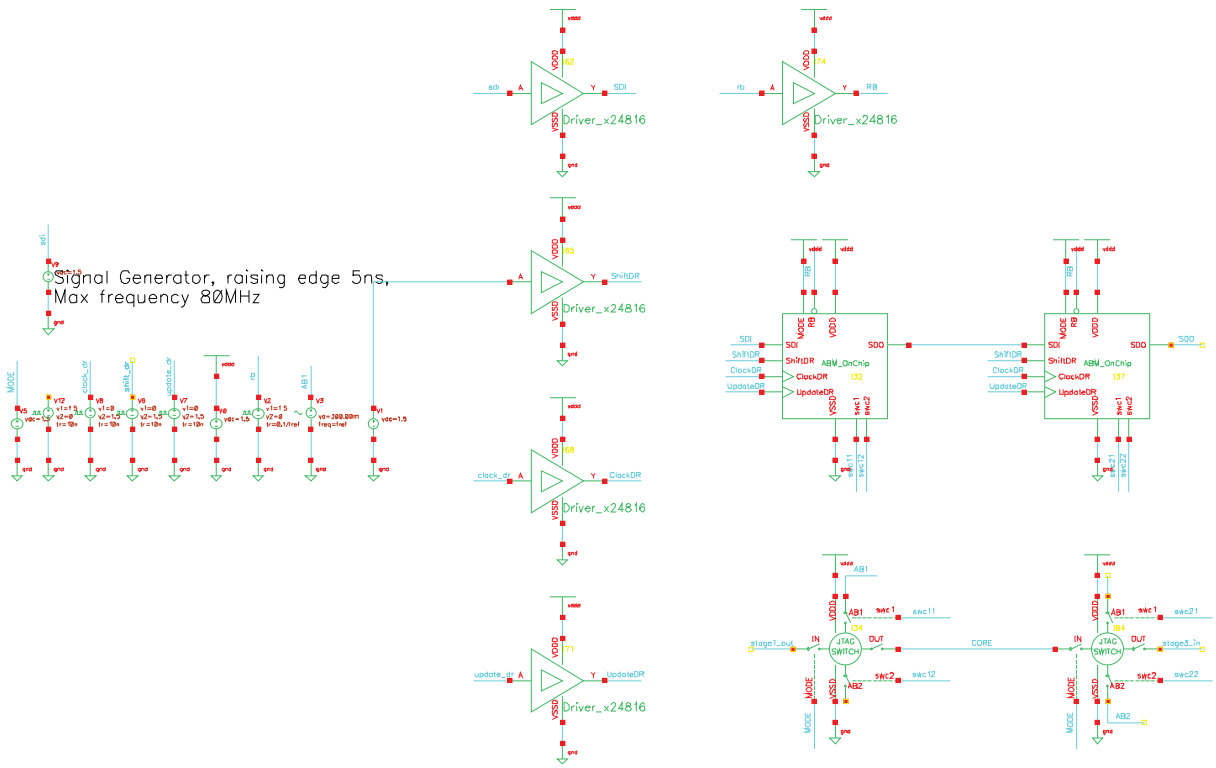


Fig. A.3 Test Bench for Analog Boundary Scan Module

A.4 ABM Switch DC Analysis Test Bench

There are two switches connected in serial with the DC test bench of the ABM switch, which is illustrated in Fig.A.4.

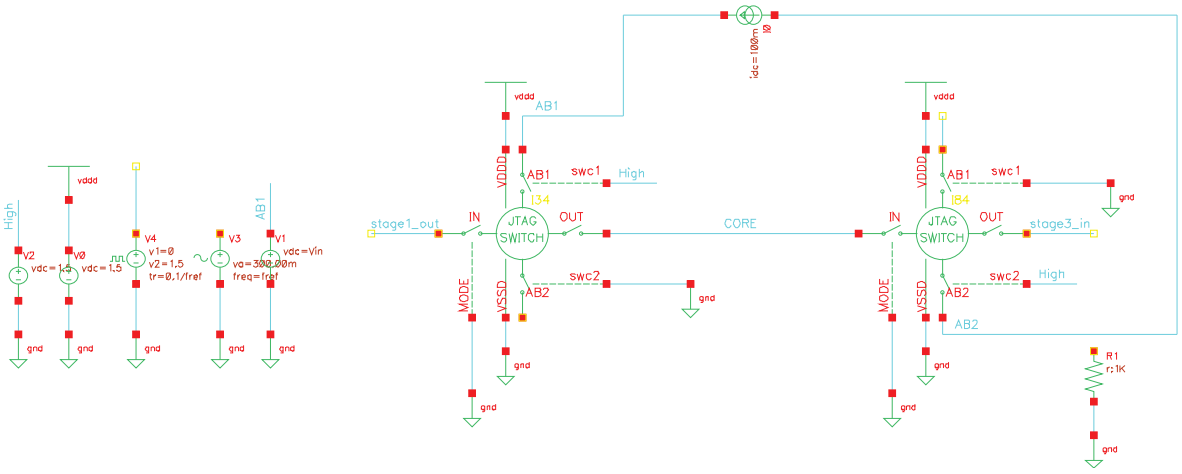


Fig. A.4 Test Bench for DC Analysis of ABM Switches

A.5 ABM Switch AC Analysis Test Bench

For the AC analysis test bench of the ABM switches, the two ABM switches are connected in serial, which is showed in Fig.A.5.

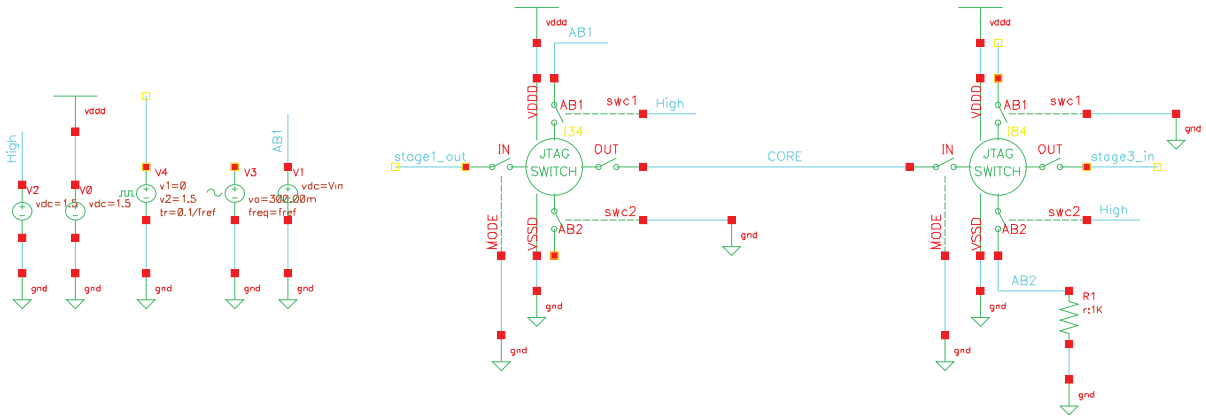


Fig. A.5 Test Bench for AC Analysis of ABM Switches

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