Temperature compensation of oscillators using a phase-locked loop with a thermal feed-back

By

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
CMOS	Complementary Metal-Oxide-Semiconductor
CP	Charge Pump
CTAT	Complimentary to Absolute Temperature
DAC	Digital to Analog Converter
IoT	Internet of Things
MEMS	Micro-Electromechanical Systems
OCXO	Oven Controlled Crystal Oscillator
PCB	Printed Circuit Board
PFD	Phase-Frequency Divider
PLL	Phase-locked Loop
PPM	Parts Per Million
PTAT	Proportional to Absolute Temperature
PVT	Process, Voltage, Temperature
Q	Quality Factor
SiC	Silicon Carbide
SOI	Silicon on Insulator
TCF	temperature Coefficient of Frequency
TCO	Temperature Controlled Oscillator
VCO	Voltage Controlled Oscillator
XO	Crystal Oscillator

ABSTRACT

Using an integrated micro-heater and a phase-locked loop (PLL) configuration, a technique to create a temperature-insensitive area on a die is described. The proposed PLL configuration employs thermal feedback through the micro-heater to significantly improve the temperature stability of the die area.

Two oscillators are employed in the PLL to act as temperature sensors to detect the ambient temperature variations and command the thermal loop to compensate them. The temperature stability of these oscillators located in the temperature-compensated die area is improved significantly and can provide a stable timing signal needed for the system. The temperature compensation of oscillators provided by this technique is studied in more detail.

Design methodologies and system-level analysis are presented. An application on temperature compensation of MEMS-based oscillators is studied with analysis and simulations. Based on these preliminary steps, an all-CMOS test-chip for proof-of-concept is designed and fabricated using a standard 130 nm CMOS technology. Analysis and experimental results show that the micro-heating system employed in this technique can provide

a low pass filtering effect enough to replace the electrical low pass filtering effect provided by a charge pump and a loop filter. Therefore, the charge pump and the loop filter existing in the conventional PLL loops can be eliminated in this system.

Test characterization of the realized proof-of-concept chip shows that the temperature stability of the die area can be improved by a factor as large as 50x for an ambient temperature range of 36°C to 52°C. Simulation shows that this range can be improved by many folds using more heat preserving technologies like SOI CMOS instead of bulk CMOS.

ABRÉGÉ

L'invention concerne une technique pour créer une zone insensible à la température sur une puce à l'aide d'un micro-réchauffeur intégré et d'une configuration de boucle à verrouillage de phase (PLL). La configuration PLL proposée utilise une rétroaction thermique à travers le micro-réchauffeur pour améliorer considérablement la stabilité de la température de la zone de la matrice.

Deux oscillateurs employés dans la PLL agissent comme des capteurs de température pour détecter les variations de température ambiante et commander à la boucle thermique de les compenser. La stabilité en température de ces oscillateurs situés dans la zone de matrice à compensation de température est améliorée de manière significative et peut fournir un signal de synchronisation stable nécessaire pour le système. La compensation de température des oscillateurs fournie par cette technique est étudiée plus en détail.

Les méthodologies de conception et l'analyse au niveau du système sont présentées. Une application sur la compensation de température des oscillateurs à base de MEMS est étudiée avec analyse et simulations. Sur la base de ces étapes préliminaires, une puce de test entièrement CMOS pour la preuve de concept est conçue et fabriquée à l'aide d'une technologie

CMOS 130 nm standard. L'analyse et les résultats expérimentaux montrent que le système de micro-chauffage utilisé dans cette technique peut fournir un effet de filtrage passe-bas suffisant pour remplacer l'effet de filtrage passe-bas électrique fourni par une pompe de charge et un filtre à boucle. Par conséquent, la pompe de charge et le filtre de boucle existant dans les boucles PLL classiques peuvent être éliminés dans ce système.

La caractérisation de test de la puce de preuve de concept réalisée montre que la stabilité de la température de la zone de la matrice peut être améliorée d'un facteur aussi grand que 50x pour une plage de température ambiante de 36 ° C à 52 ° C. Il est démontré par simulation que cette gamme peut être améliorée par de nombreux plis en utilisant davantage de technologies de préservation de la chaleur comme SOI CMOS au lieu du CMOS en masse.

Chapter 1 Introduction

1.1 Motivation

Nowadays, electronic devices are required more than ever to operate in various environmental conditions with little or no degradation in performance. Temperature is one of these environmental conditions that vary in many applications. There have been numerous circuit techniques to compensate for the effect of temperature on the performance of electronic systems. For decades, bandgap reference circuits have been designed specifically to address the need for temperature-stable circuits.

More recently, the ever-growing applications of high-resolution and high-speed data converters, including digital-to-analog converters (DACs) and analog-to-digital converters (ADCs), have demanded high-precision voltage references. This has made temperature compensation techniques for bandgap reference still relevant to the research community [1-5].

Similarly, obtaining stable current references is very important for many mixed-signal applications like current-mode analogue-to-digital converters (ADCs). The research is still conducted to improve these circuits [6-9].

With the introduction and spread of the internet of things (IoT) and sensor networks, more and more sensors are used in electronic circuits and compensation of the effect of temperature on them has been a demanded area for researchers [10-14].

In addition, in digital systems, timing circuits as important components of the system, require reference oscillators that must yield a stable frequency under all operating conditions. Temperature compensation techniques have been proposed and are still being investigated by researchers for all the different types of oscillators, consisting of quartz crystal oscillators [15-18], microelectromechanical systems (MEMS) based oscillators [19-28], and all-silicon integrated oscillators [29-44].

The temperature compensation techniques proposed to date are mostly based on the use of circuits or devices with lower intrinsic temperature sensitivity [24], or the addition of a component with an opposite temperature sensitivity to cancel out the temperature sensitivity of the circuit, mostly in an open-loop fashion [42, 45]. In all of these temperature compensation techniques, it is assumed that the ambient temperature can change the temperature of the system and the circuit under investigation. However, an extra level of temperature compensation can be added on top of these techniques that is maintaining the temperature of the circuits and devices fixed in the presence of ambient temperature variations. In this method, variations in the ambient temperature are sensed, and heating (in some cases, a cooling system) serves to counteract this effect on the system. This is accomplished by providing more heat to the system when the ambient temperature drops and less when the ambient temperature increases. This is the same familiar scheme used at the macroscopic scale to regulate the ambient temperature in living spaces using thermostats in heating systems or air conditioning systems. This scheme has been of interest for the semiconductor circuit research community for a long time. It has been used for temperature compensation of reference signal generators [46-48] and for creating highly stable OCXOs [15, 17]. In addition, more recently, it has been applied to microelectromechanical systems (MEMS)-based oscillators [26, 49-53].

The interesting aspect of this method is that it can be applied to the system concurrently with other temperature compensation methods, which can significantly reduce the temperature sensitivity of the system.

1.2 Research Goal

This research work aims to propose an integrated temperature compensation scheme to counteract the effect of the ambient temperature change on the system. It explores the use of oscillators as temperature sensors to detect ambient temperature variations and compensate for its effect on the oscillators and the die area surrounding them by employing thermal feedback made in a PLL configuration leveraging micro-heaters. Electrothermal integrated circuits have been under study since the 70s [54-56]. Compared to other works using integrated heaters, the work here attempts to bring some added perspective to the

heating system architecture by considering a model similar to a typical PLL and adding new implementation aspects. Notably, a combination of analysis and measurements, including electro-thermal simulation, system-level analysis and simulations, and fabrication results are detailed here and have not been reported before.

In this research, a scheme is proposed for temperature compensation for a CMOS die area. This temperature compensation scheme aims to keep the temperature of the die area fixed while the ambient temperature changes. For this purpose, there is a need for a heating system (or, if possible, a cooling system) to provide heat when it is needed to counteract the effect of the ambient temperature changes. In addition, there is a need for a sensor to sense the ambient temperature variations and send this information through a commanding (possibly feedback) path to the heating system. In short, it can be said that the three main components of this system are the heating system, the sensory one, and the commanding path.

On the other hand, one important issue that oscillators encounter is their temperature sensitivity. Generally, the frequency that an oscillator generates is highly dependent on the temperature it operates in, and efforts to compensate for the temperature sensitivity of oscillators have been going on for decades [29].

Using this property of oscillators as an advantage and using the temperature sensitivity of the oscillators to sense the temperature variations in a temperature compensation system can be a fascinating idea. This way, the temperature sensitivity of an oscillator is used to provide a temperature-stable environment which in turn can place an oscillator that is less affected by the ambient temperature changes.

To use the frequency of an oscillator as a temperature sensor, it needs to be compared with a reference point. One natural candidate for this is using a second oscillator and a phase-locked-loop (PLL) to compare the frequency of the two oscillators feeding it. To use a second oscillator as a reference point, the two oscillators should have different temperature sensitivity. Therefore, when their temperature changes, their frequency changes at a different rate compared to one another. Hence, the PLL can detect this change and generate

a different command signal for the heating system. This will form a feedback system from the oscillators, PLL, and the heating system, which can reduce the temperature sensitivity of the oscillators and the environment this system is affecting.

1.3 Contributions

The contribution of this work can be described in the below categories.

1.3.1 Proposing a Temperature Compensation Scheme Using Temperature Controlled Oscillators in a Phase-Locked Loop Configuration

As mentioned, the difference between frequencies of two oscillators with different Temperature Coefficients of frequency (TCf) can create a signal that can be used in a feedback loop to keep the temperature and consequently the frequency of oscillators fixed. A new scheme for temperature compensation of electronic circuits in general and oscillators specifically was proposed based on this idea. This scheme uses a new PLL structure that has not been analyzed before, and it is designed with an integration possibility in mind.

1.3.2 Modeling and Analysis of Temperature Compensation Capability of the Proposed Scheme

The proposed temperature compensation scheme is simplified with a linear model, and this linear model is used to analyze the behavior of the system and its temperature compensation capability. Since the system has both electrical and thermal components, mathematical models of both domains are combined, and the insight from the analysis is used for predicting and improving the system.

A simulation verification of the analysis also is performed in this work.

The contributions associated what mentioned in sections 1.3.1 and 1.3.2 are highlighted below [57]. The author's contribution was to generate the main idea of the work and also to design, analyze, the circuit level and system level simulations. The contribution of K. Allidina was

advice on circuit simulation and providing some circuit models for circuit simulation. The contribution of T. Saha, has been in circuit level simulations and the contributions of M.N. El-Gamal and F. Nabki has been in general guidance and advice of the direction of the research.

S. A. Gorji Zadeh, T. Saha, K. Allidina, F. Nabki and M. N. El-Gamal, "Electronic temperature compensation of clamped-clamped beam MEMS resonators," *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*, 2010, pp. 1193-1196.

1.3.3 Analysis of the Phase Noise of a Dual Oscillator PLL System

To examine the phase noise behavior of the whole system when there are two oscillators with possibly different phase noise, an analysis of the phase noise of a dual oscillator PLL system is performed. A system-level behavior simulation accompanies this analysis for verification purposes.

The contributions associated with this work are mostly highlighted below [49]. The author's contribution was to define the main idea of the work and perform the analysis and run the simulation. The contribution of M.N. El-Gamal and F. Nabki has been in general guidance and advice of the direction of the work conducted.

S. A. Gorji Zadeh, M. N. El-Gamal and F. Nabki, "The phase noise of an oscillator employing a dual MEMS resonator temperature compensation scheme," *2010 International Conference on Microelectronics*, 2010, pp. 160-163,

1.3.4 Analysis, Application, and Measurements of the Filtering Effect of the Heaters in the Whole PLL System

The heating system used in this design consists of micro-heaters, and they are simplified, and a linear model is analyzed in the system analysis. Based on this analysis, the PLL loop is implemented using the loop filter effect obtained from the heating system. Second-order modeling and analysis of the heating system show that the heating system has a filtering effect in time and frequency domain, which can replace the filtering that a loop filter in a

standard PLL system can provide. Step response tests and measurements are performed on the micro-heater in this work to demonstrate how this filtering effect behaves. All these are new contributions of this work.

1.3.5 Implementing the Proposed System Along with the Integrated Heaters in CMOS Technology

An integrated implementation of the proposed scheme is performed using IBM CMOS 130nm technology. The system that is designed and implemented for this purpose consists of on-chip micro-heaters and all building blocks of PLLs. This includes current-starved ring oscillators, frequency dividers, phase-frequency detectors (PFDs), charge pumps, and the buffers needed for the heaters.

The whole dual oscillator system implemented for this work is tested with a printed circuit board (PCB) designed for this purpose.

1.3.6 Feasibility Study of Using the Proposed Temperature Compensation Scheme for MEMS-based Oscillators

The possibility of using the proposed structure in an integrated way with MEMS-based oscillators is explored in this thesis. This is performed by examining the temperature behavior of the in-house fabricated MEMS resonators and simulations and analysis.

The contributions associated with the work mentioned in sections 1.3.4 to 1.3.6 are highlighted below [58]. The author's contribution was to generate the main idea of the work, analysis, simulation, and system and circuit design for the proof of concept. To this end, preparing the layout for fabrication of the test chip, designing the PCB for testing the circuit and running measurement are performed by the author. The contribution of K. Allidina was to provide PFD/CP circuits and advice on circuit implementations. The contribution of P. V. Cicek has been in MEMS resonator's behavior description, and COMSOL simulations of heat dissipation in bulk and SOI die

fabrication. The contributions of M.N. El-Gamal and F. Nabki have been in general guidance and advice of the direction of the research conducted.

S. A. Gorji Zadeh, K. Allidina, P. V. Cicek, F. Nabki, and M. N. El-Gamal, "CMOS die area temperature compensation using a phase-locked loop with thermal-feedback," Analog Integrated Circuits and Signal Processing, vol. 113, no. 3, pp. 315-329, 2022/12/01 2022.

1.4 Thesis Outline

An overview of schemes for temperature compensation is presented in Chapter II. The proposed scheme of this work is described and analyzed in chapter III. In chapter IV, the phase noise behavior of the system with two oscillators is analyzed, and in chapter V, the possible application of this scheme for temperature compensation of MEMS-based oscillators is analyzed and modeled using simulations. Chapter VI explains the implementation of the proposed temperature compensation for an all-silicon oscillator system and presents the results and discussions, while chapter VII makes the conclusion.

Chapter 2 Overview of Temperature Compensation in Electronic Circuits

2.1 Introduction

As a warm-blooded creature, human has always needed to keep the variations of the temperature of his body limited in different environmental conditions. The use of cloth and even taking caves as a shelter has partly been due to this need. As warm-blooded creatures, compared to cold-blooded ones, have more robust performance, providing a controlled environment with limited variations helps in getting a steady performance from a system located in that environment.

Obtaining robust and predictable behavior from electronic systems is an objective in most of these systems. To achieve this, one important design aspect for electronic systems is their robust and controlled performance in the presence of temperature variations.

Therefore, numerous ways to compensate temperature sensitivity of electronic systems and their circuits have been introduced. This chapter will introduce an overview of the main electronic systems and circuits used for temperature compensation. The main electronic temperature compensation systems will be discussed in the coming sections.

2.2 Bandgap Voltage Reference

Providing a circuit that generates a stable voltage reference is essential for any analog mixed-signal circuits design. The signal generated by this block is used for analog-to-digital converters (ADCs), digital-to-analog converters (DACs), voltage regulators, clock references and sensors [59-62]. Bandgap reference (BGR) voltage generators are the most common types of voltage reference generator circuits intended to provide a signal independent from the process, supply voltage and temperature (PVT).

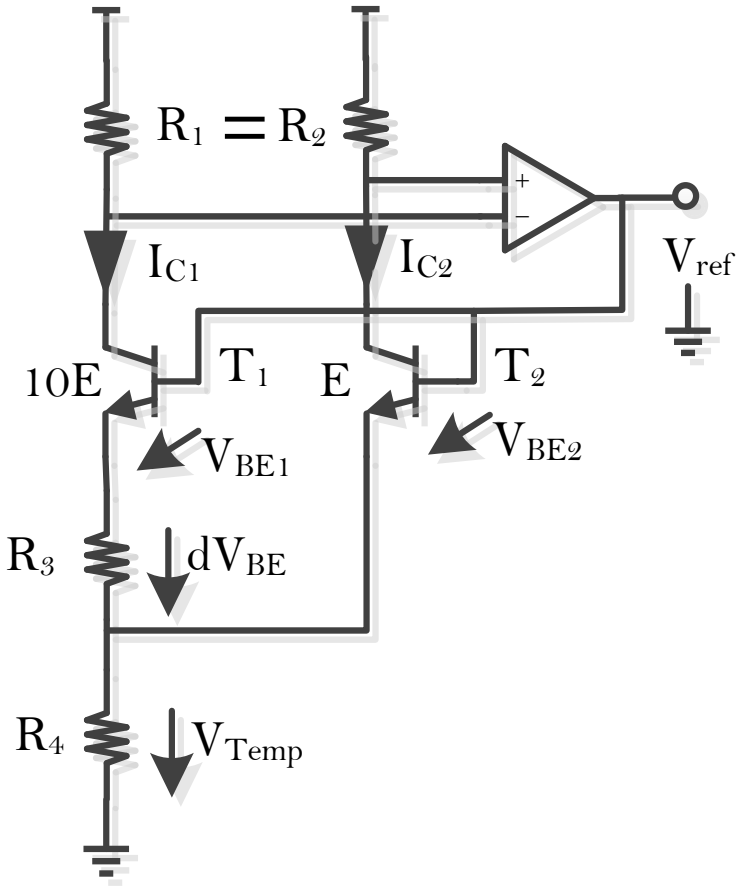


Figure 2-1. Brokaw bandgap reference voltage circuit.

In BGR circuits, two voltages acting opposite each other with respect to temperature cancel out the effect of temperature on the overall voltage generated by the circuit. In these circuits, as shown in one of its simple forms by A. P. Brokaw in [63], and depicted in Figure 2-1, a scaled version of the voltage difference between two p-n junctions with different current densities ($V_{Temp} = 2\frac{dV_{BE}}{R_3}R_4$), which is proportional-to-absolute-temperature (PTAT), is added to the voltage of a single p-n junction with a constant current (V_{BE2}), which is complementary to absolute temperature (CTAT).

As shown, the compensation system used in these circuits does not use any feedback and tries to cancel two opposite effects with each other in an open-loop fashion.

Many aspects of reference voltage circuits like non-linearity over a higher temperature range and precision voltage reference generation, temperature drift and low voltage applications have been the research community's focus in recent years. [4, 7, 64-69].

2.3 Bandgap Current Reference

Current references are also essential blocks in most analog, mixed-signal blocks such as digital-to-analog converters (DACs), digital-to-analog converters (ADSs), amplifiers and phase-locked loops (PLL). Current references designs can be categorized into two main types.

In the first type, the reference current is generated by adding a proportional-to-absolute-temperature (PTAT) current and a complementary-to-absolute-temperature (CTAT) current to each other [7, 8, 70, 71].

In the second type of reference current circuits, a PTAT or CTAT voltage is applied to a PTAT or CTAT resistor to create an insensitive temperature current [6, 71, 72]. This type is used for low power applications like the Internet of things (IoT) [71, 73].

2.4 Temperature Compensation in Sensors

With the prevalence of the internet of things (IoT) and sensor networks, many circuits for sensors have been introduced. These sensors measure various parameters like pressure, humidity, acceleration, inertia and more [74-77].

To obtain a reliable read-out from the sensors in different temperatures is an important specification needed for all the sensory systems and circuits. In general, the temperature compensation of sensors happens in two different ways. One way is hardware compensation, and the other method is software compensation.

In hardware compensation, symmetry is created in the system using circuit elements with opposite sensitivity to temperature [78-80]. Even though the hardware temperature compensation for sensors is rather easy, it lacks high accuracy. Without any feedback, it

cannot adapt to the possible changes in the circuits like process, voltage, and different ranges of temperature (PVT).

In software temperature compensation, as opposite to hardware temperature compensation, the system's temperature is measured. Using digital circuits, a command is sent to the appropriate circuits to compensate for the effect of temperature variations [81, 82]. With the complexity added, higher accuracy and an ability to respond to variation in the circuit condition is added to the system.

2.5 Temperature Compensation in Oscillators

Nowadays, electronic devices are required more than ever to operate in various environmental conditions with little or no degradation in performance. Precise timing is a crucial requirement in almost all digital electronic systems, which requires a clock signal to serve as a reference. This reference clock must yield a stable frequency under all operating conditions to ensure consistent operation of the system. In this work, the frequency stability of oscillators in the presence of temperature variations will be explored.

The three main oscillator types used in electronic systems are crystal, MEMS-based, and all-silicon oscillators. Each type exhibits a different degree of frequency stability in the presence of temperature variations.

2.5.1 Crystal Based and non-Integratable Oscillators

Crystal oscillators are the most stable of these three types and have essentially had a monopoly on applications requiring high precision and highly stable frequency since 1919 [16]. A basic crystal oscillator (XO) can provide frequency stability of less than ± 50ppm without temperature compensation, and a temperature compensated XO (TCXO) can provide frequency stability of ± 2.5ppm over a temperature range of 125°C [83]. Oven controlled crystal oscillators (OCXO) can provide even higher stability, and have been demonstrated to have frequency stability in the range of ± 5ppb over a range of 75°C [17] and more recently, have shown frequency stability of ± 3ppb over a range of 125°C [18]. Although crystal oscillators can provide very good temperature stability and a very high-

quality factor (Q) (and consequently very low phase noise [16, 84]), they suffer from several drawbacks. Their operating characteristics are sensitive to vibration and shock, and they need to be packaged in a vacuum or gas-filled hermetic package to prevent contamination. In addition, the large form factor and technological limitations render crystal oscillators unsuitable for monolithic integration with microelectronics. These drawbacks have led researchers to look for possible replacements for crystal oscillators.

2.5.2 MEMS-Based Oscillators

Research into creating oscillators using MEMS has been conducted ever since the idea of using silicon as a mechanical material for electronics was proposed in the 1980s [85, 86]. Significant effort has been devoted to this research area, and promising results have been achieved [19, 20, 22, 23, 87]. Because the output frequency of MEMS-based oscillators is inherently more sensitive to temperature than that of crystal oscillators, several compensation methods have been proposed, including mechanical compensation by coating the device with a material to cancel its temperature dependence [24, 88, 89], electronic compensation by including a tuning capacitor in the circuit or adjusting the temperature of the devices through heat induction [20, 25, 90, 91], and a combination of mechanical and electronic compensation techniques [26]. Recent work has achieved temperature stability of lower than 1 ppm for MEMS-based oscillators over a temperature range greater than 100°C [23, 28, 92-94].

Research on integrated oscillators has been ongoing in parallel to MEMS-based oscillators since the 1960s [29]. New advances in semiconductor technology in general and CMOS specifically have renewed interest in all-silicon integrated oscillators [30]. Although the high-temperature sensitivity of all-silicon oscillators has been a significant hurdle in their practical use as timing references, recent improvements in this area have been significant. The research community has presented relaxation and RC oscillators [31-36, 95, 96] and ring oscillators [97-100] with temperature stabilities on the order of 400 ppm over a range of up to 130°C [35]. Meanwhile, LC oscillators have been shown to achieve temperature stabilities as low as 200 ppm over a temperature range of 90°C without the need for complex post-processing calibration/compensation techniques [40-44, 101].

2.5.3 All Silicon Oscillators

The majority of the temperature compensation techniques proposed to date are based on the use of circuits or devices with lower intrinsic temperature sensitivity [24], or the addition of a component with an opposite temperature sensitivity to cancel out the temperature sensitivity of the oscillator, mostly in an open-loop fashion [42].

2.6 Summary and Conclusion

This chapter highlighted the importance of temperature compensation in electronics circuits and systems by presenting a brief overview of many electronic circuits that use temperature compensation. Bandgap voltage and current references, electronic sensors and oscillators are the main circuits that temperature compensation techniques for them were discussed. In the brief discussion, some literature published in these areas was also presented.

Chapter 3 System Description and Analysis of the Proposed Scheme for Temperature Compensation

3.1 Introduction

In this chapter, the proposed temperature compensation scheme is introduced and is analysed. First, the proposed compensation scheme is introduced and then it is modelled using a linear approximation to be able to analyse it. Initially, the analysis is performed on a simplified system. Then practical details and non-idealities are added to the system for a better analysis of the system that can provide a better understanding of its behaviour and predict its functionality. The proposed scheme is described in the next section.

3.2 The Proposed Temperature Compensation Scheme

One way to compensate for the ambient temperature change effect on the desired device is to provide a mechanism to keep the temperature of the device fixed independently from the ambient temperature variations. In this method, changes in the ambient temperature can be sensed, and a heating system (and in some cases a cooling system [102]) can be employed to cancel out the effect of this ambient temperature variation on the oscillator. In the system implementing this, a heater is used to push more heat into the system when the ambient temperature drops and less heat is pumped into the system when the ambient temperature increases. This is the same familiar scheme used at the macroscopic scale to regulate the ambient temperature in living spaces utilizing heating and air conditioning systems. This scheme has been of interest to the semiconductor circuit research community for a long time. It has been used for temperature compensation of reference signal generators [46, 47] and for creating highly stable OCXOs [15, 17]. In addition, more recently, the same scheme has been applied to MEMS-based oscillators [26, 49]. Even though there have been suggestions that some MEMS-resonators can be implemented on top of silicon-based integrated circuits [19], an integrated compensation system with MEMS-based resonators using this concept has yet to be presented. However, using this concept is just gaining the research community's attention to be realized on all-silicon oscillators. Recently, an integrated micro-heater was

shown to create a voltage-temperature compensated area on-chip [103]. The current work proposes an integrated compensation scheme that can be used for both MEMS-based oscillators and all-silicon oscillators. This work exposes a different heater structure than the one in [103], and in addition, it provides an analysis of the loop and behaviour of the dual loop PLL created for this purpose. It models the system in its entirety, both with respect to the dual loop PLL and the thermal feedback, and it illustrates its design procedure, metrics, and considerations [58].

The proposed temperature compensation scheme uses integrated micro-heaters built on top of the oscillators to keep the temperature of the oscillators fixed against the ambient temperature variations. The power delivered to the micro-heaters and, consequently, the heat transferred to the oscillators increases when the ambient temperature drops and decreases when the ambient temperature increases. The objective of this compensation technique is to keep the actual temperature of the oscillators fixed and independent from the ambient temperature variations.

To change the amount of heat provided by the micro-heaters in response to ambient temperature variations, a mechanism to detect ambient temperature changes is needed.

To show how the temperature variations can be detected, let's consider two oscillators whose frequency reacts to temperature differently, as shown in Figure 3-1. In this figure, the frequency of each oscillator divided by a specific number is plotted as a function of its temperature. As Figure 3-1 shows, if the two lines do not have the same slope, they can only meet at one temperature(T0) and frequency point. Therefore, if the system is biased at temperature T0, any temperature change causes the two frequencies to further depart from each other. Thus, this frequency difference can be used as a temperature change indicator in a temperature compensation system. It can be used in a feedback loop to control the amount of heat required to be transferred to the oscillators to push back the temperature to its original value.

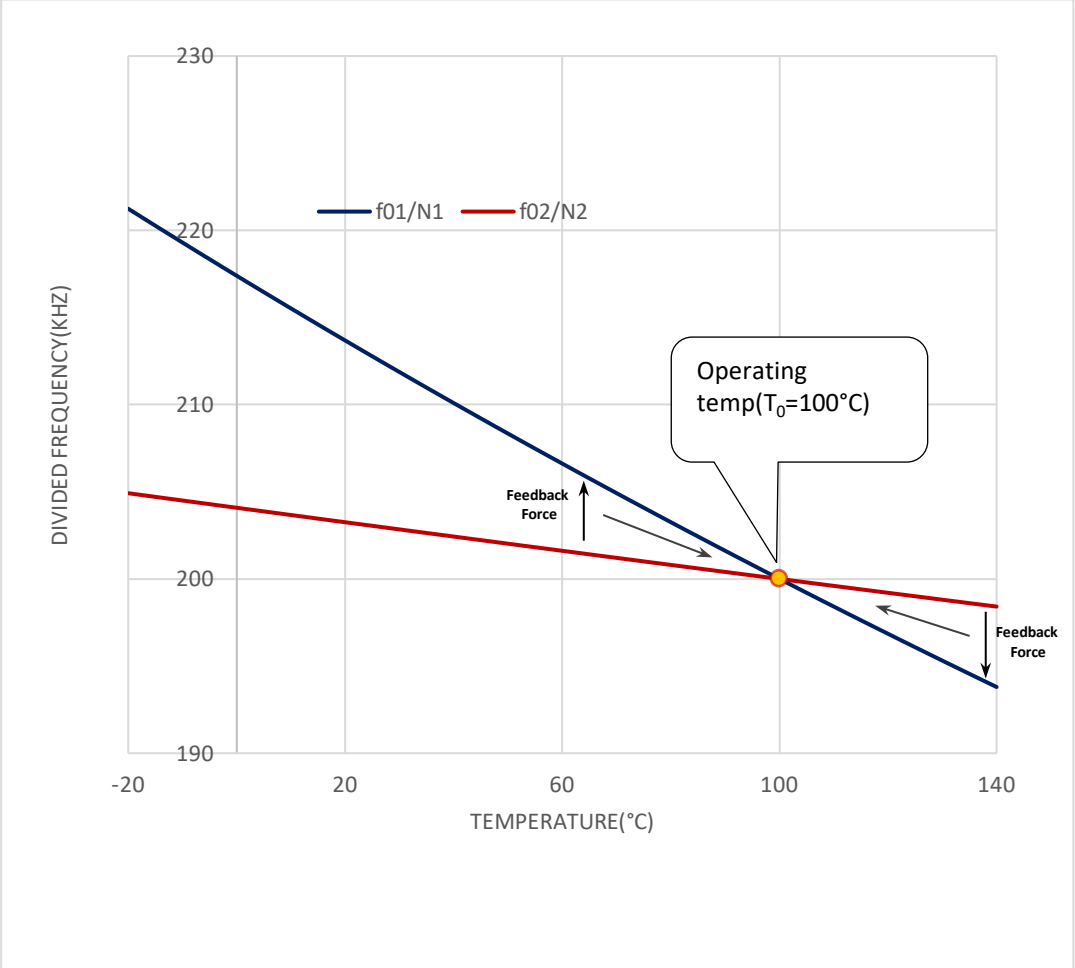


Figure 3-1. The difference between the slopes of the two lines produces the feedback force.

Since frequency comparison and frequency differentiation is needed for this purpose, a PLL structure is a good candidate to perform this job[104]. Thus, a feedback system depicted in Figure 3-2 is proposed for the temperature compensation system.

There are two oscillators equipped with micro-heaters in this system, each feeding one programmable integer frequency divider. The frequency dividers are added to the design to provide the ability to divide down the two oscillators' frequencies and make them closer to each other. This adds the capability to the system to employ two oscillators operating at possibly very different frequencies. By dividing them down to close enough frequencies, they make them suitable phase frequency detector (PFD) block inputs. The division ratio in each path can be adjusted independently to provide an extra degree of freedom in the design.

The divided down signals are compared to each other in a phase-frequency detector (PFD), and a signal corresponding to the difference between the two frequencies is generated by the PFD. In this phase-locked loop (PLL) system, the output of PFD can go through a charge pump (CP) and loop filter to provide a clean feedback control signal. However, as it will be shown in the next chapters, the dynamics of the heating system and the micro-heaters can act like a filter and there is a chance that both charge pump and loop filter be eliminated from a PLL system consisting of a heating system.

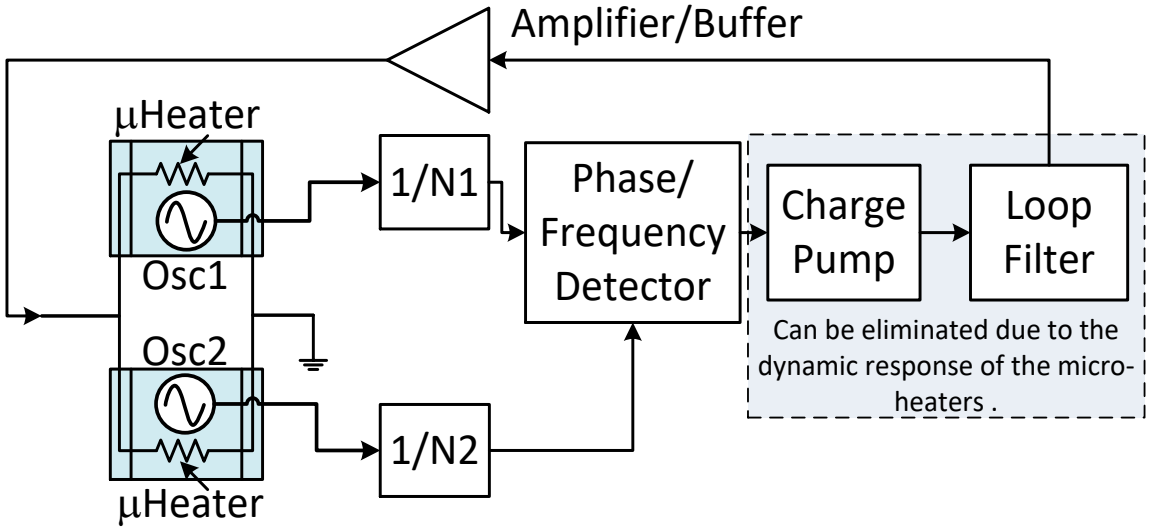


Figure 3-2. Block diagram of a possible realization of the PLL-based compensation system.

In the proposed system, the heat forces the loop to lock and makes the signal frequencies going into the PFD of the same value. To achieve this, the control signal corresponding to the difference between the two frequencies controls the current mirrored by the current buffer/amplifiers into the micro-heaters built on top of the oscillators. The current amplifier/buffers are necessary to drive the low impedance micro-heaters.

It should be noted that the oscillators in this PLL are temperature-controlled oscillators (TCOs) as opposed to voltage-controlled oscillators (VCOs) used in a conventional system. This is because the frequency of oscillators in this system is controlled by the temperature and the heat generated by the micro-heaters, as opposed to a voltage signal.

3.2.1 Temperature to Frequency Function

In Figure 3-1, it has been assumed that for simplicity, a straight line can show the frequency of each oscillator as a function of its temperature. This assumption is quite realistic for MEMS-based oscillators, as shown in [87, 105-109].

For silicon-based oscillators, the assumption that frequency changes with respect to temperature in a linear fashion is not completely realistic. Figure 3-1 shows the simulated frequency of a current-starved ring-oscillator versus temperature for different control voltage that controls the current going through the inverter chain in the ring-oscillator. This current-starved ring-oscillator is used in the implementation of the system that will be explained in future chapters. From Figure 3-3 it can be noticed that even though at most of the control voltage range, the frequency to temperature curves are straight lines, but there are situations that s straight like cannot represent frequency to temperature variations of the oscillators. When frequency to temperature curves of oscillators are not straight lines, special attention should be paid to designing the temperature compensation system explained in the next section.

3.2.2 Implications of not having a straight-line showing frequency versus temperature of oscillators

To ensure that the PLL locks at one frequency, in the proposed scheme as shown in Figure 3-1 it is assumed that the frequency to temperature curves of the oscillators meet each other at only one frequency/temperature point. As long as the two curves are straight lines, this assumption is true. However, if these curves are not straight lines, implications in functionality of the system might arise. Let us assume as shown in Figure 3-4.a, the frequency versus temperature curve of one of the oscillators is a straight-line and the other one is not. In this case, these two curves may meet each other at two points, as shown in Figure 3-4.a.

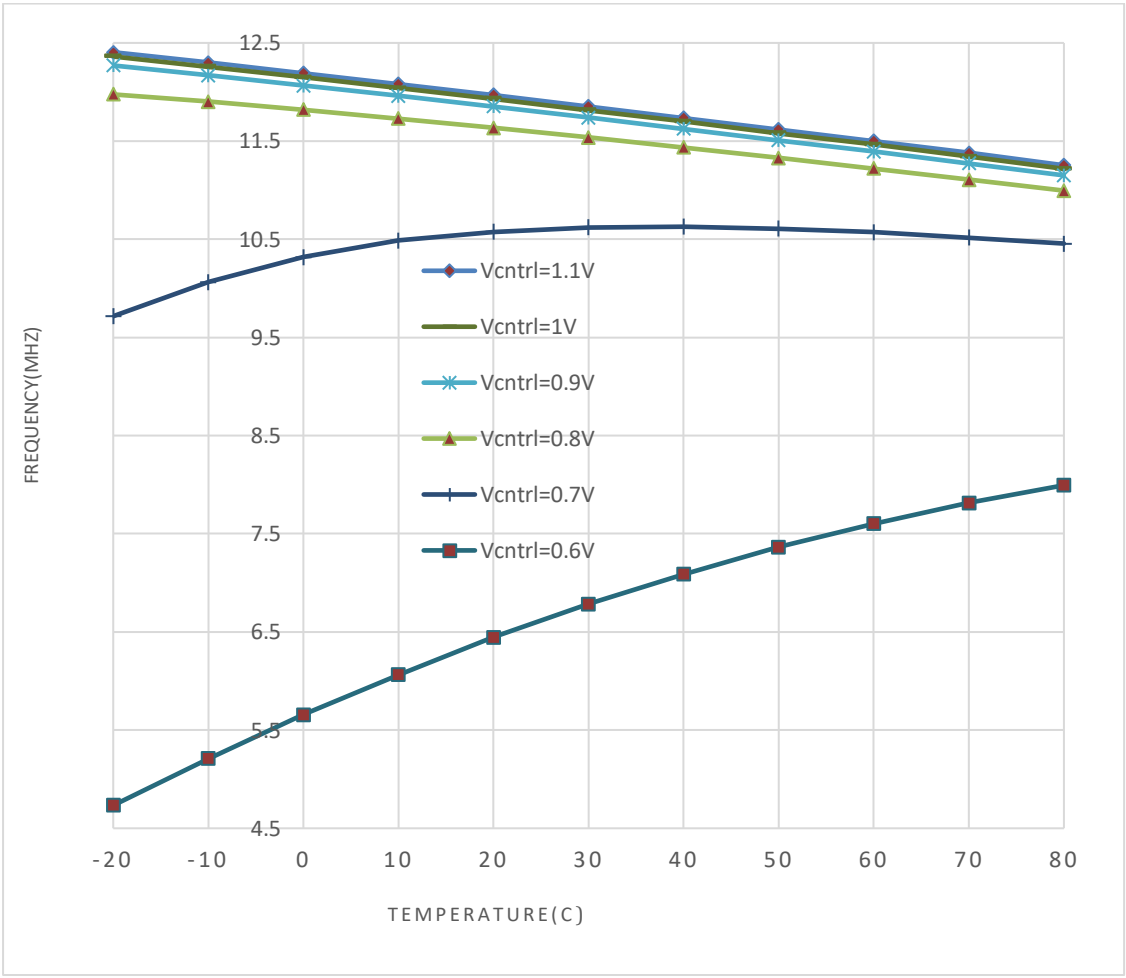
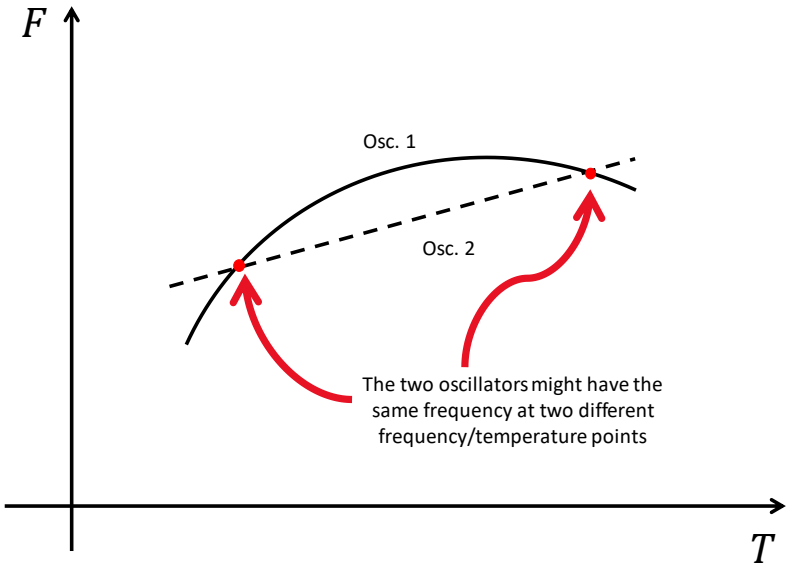


Figure 3-3. Simulated effect of temperature on the oscillation frequency at different control voltages (Vcntrl).

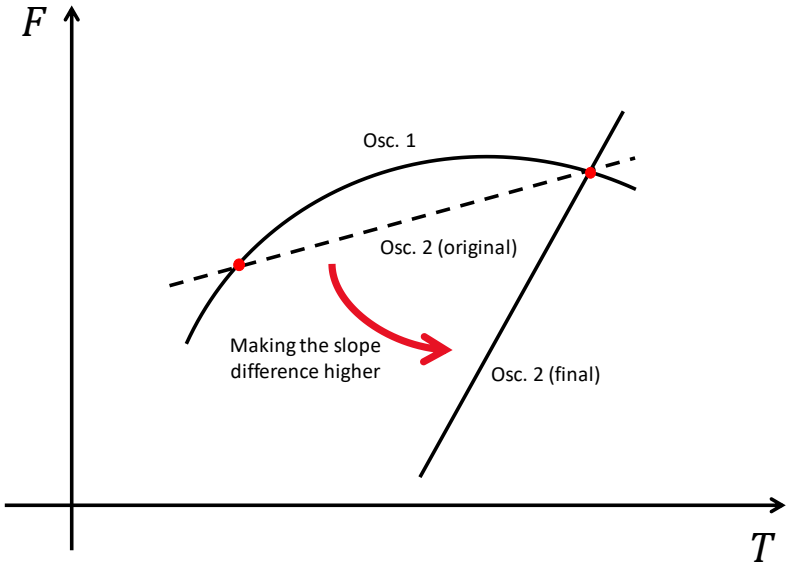
Now, if the slope of one of the two curves (without loss of generality in this case, we assume the slope of the straight-line) is pushed away from the other one, as shown in Figure 3-4.b, the curves only meet each other at one single point.

In general, if the frequency versus temperature of one of the oscillators is always more than the other one, the slope of the difference between the two curves is always positive or negative, which means the difference between the two curves is monotonic. This means it only crosses zero at one point, which means the two curves only meet at one point.

This discussion concludes that enough attention should be paid to the design of the circuit to prevent implications caused by this issue. As mentioned above, if the slope of one curve is always larger than the other one, the two curves can only meet at one point. However, if this is not possible over the whole temperature range, the system can still work over any specific range that this condition is met.



a) There are two frequency/temperature points that both oscillators can meet each other.



b) If the slope of oscillator 2 is increased and pushed away from the slope of oscillator 1, they might only meet each other at one frequency/temperature point rather than two points they crossed at originally.

Figure 3-4. Crossing at two points can be avoided by using a higher slope difference between the two oscillators.

3.2.3 Assuming Frequency versus Temperature is a straight-line

Indeed, even if the frequency versus temperature curves of the oscillators are not really straight lines, in a short enough temperature range, they can be assumed to be straight lines. In the following, it is assumed that the two curves are straight lines.

The slope of the frequency to temperature line of the oscillator is used to define the temperature sensitivity of that oscillator (and of the resonator if the oscillator is a resonator-based one). To quantify this frequency sensitivity to temperature, temperature coefficient of frequency or TCf is defined as the normalized variation of frequency to temperature, as shown below.

$$TCf = \frac{\frac{\Delta f}{f0}}{\Delta T} \quad (3.1)$$

, where, Δf=f-f0 and Δf/f0 is the normalized frequency variation and ΔT is the temperature variation.

As indicated in Figure 3-1, the PLL achieves lock at an operating temperature of T_0 when the following condition is satisfied:

$$\frac{f_{01}}{N_1} = \frac{f_{02}}{N_2} \quad (3.2)$$

where f_{01} and f_{02} are frequencies of each oscillator at T_0. To achieve this condition, the division ratios of the frequency dividers (N_1 and N_2) must be properly selected. It is assumed that oscillators have different and monotonic TCf, and therefore, the PLL can only lock at the only one temperature that meets the relationship in (3.2).

The above analysis assumes that the temperature of both oscillators is the same, which essentially means that the micro-heaters provide the same amount of temperature control/feedback to each oscillator. This condition needs to be adhered to as closely as possible during the design and implementation of the system.

Since the only cooling mechanism available in this system is to stop the micro-heaters from supplying heat, the only way to ensure that the loop locks at all ambient temperatures is to set T_0 above the maximum targeted ambient temperature. For example, if the system is designed to work at an ambient temperature of 85°C, the actual temperature of the oscillators must be set slightly higher than that (e.g. 100 °C, as shown in Figure 3-1). A temperature margin is helpful to account for process variations and non-idealities in the system. For instance, a margin would be necessary if the lowest current generated by the output buffer is greater than zero due to leakage currents.

3.3 Linear Approximation and System Analysis

3.3.1 Linear Approximation

The system can be approximated as a continuous-time linear system to simplify the analysis, and this model is shown in Figure 3-5. The system consists of three main parts. Oscillators and Phase Frequency dividers (PFD), Loop-Filter (will be realized by the heating system) and the heating system. Any changes in the ambient temperature will cause a frequency shift in the oscillator. The PLL feedback loop will adjust the temperature of the micro-heater to

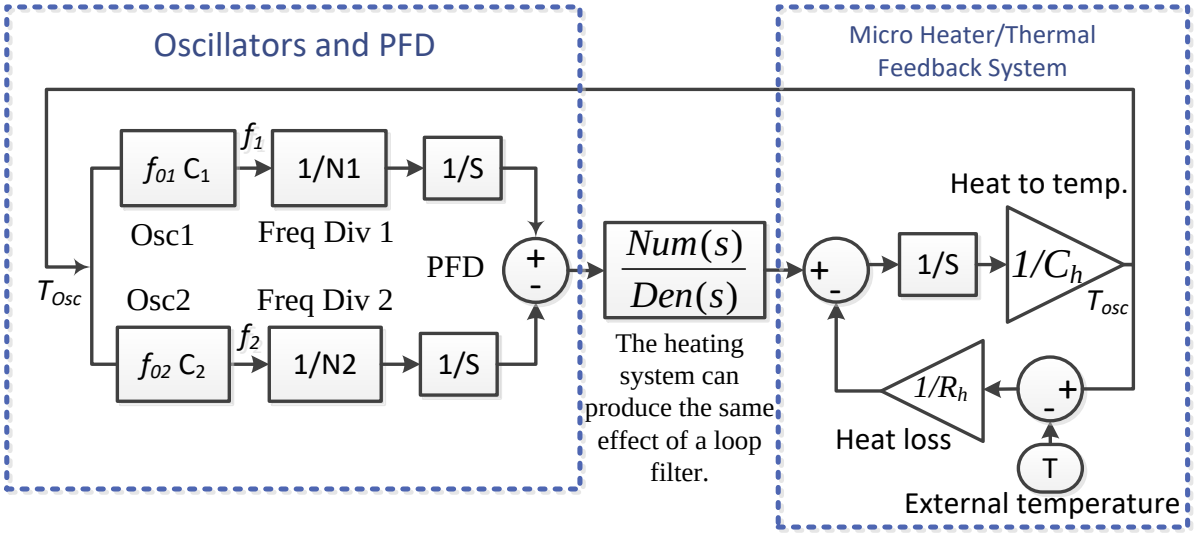


Figure 3-5. Linearized model of the proposed system.

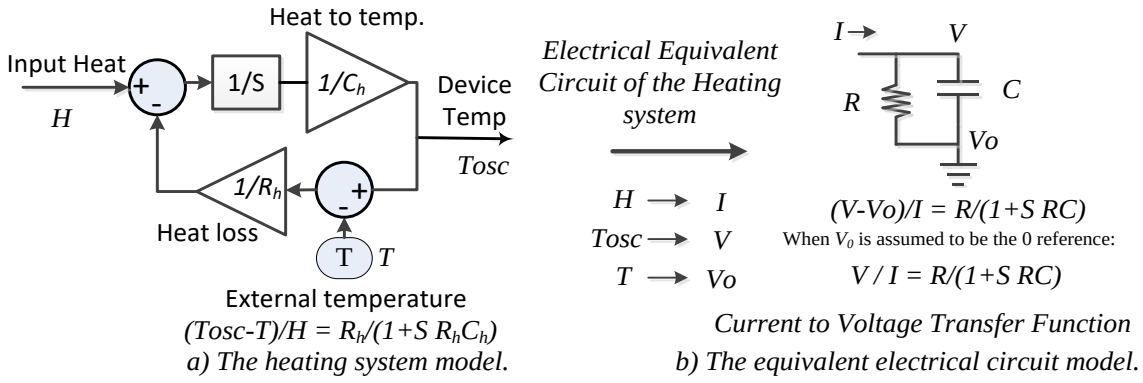


Figure 3-6. The heating system model and its equivalent electrical circuits.

compensate for this shift. It should be noted that this linear approximation is only valid if the loop bandwidth of the system is at least 10 times smaller than the frequency of the signal at the output of the frequency dividers [110].

For each oscillator, a temperature change from the initial temperature T_{osc0} to T_{osc} causes an oscillation frequency variation from f_0 to f expressed as:

$$f(T_{osc}) = f_0(1 + C(T_{osc} - T_{osc0})), \quad (3.3)$$

where C (C1 and C2 in Figure 3-5) is the oscillator's temperature coefficient of frequency (TCf). In this system, heat controls the frequency of oscillators through temperature-controlled oscillators (TCO) as opposed to voltage-controlled oscillators (VCO). Hence, the PLL system can be linearized around the initial temperature T_{osc0} and the frequencies f_{01} and f_{02} as depicted in Figure 3-5. Using this model, the variation of the frequency of the output signal of each TCO passes through a linear gain stage, a divider, and an integrator, which converts the frequency variations into a phase variation before being input to the PFD.

3.3.1.1 Micro-heater linear modeling

As shown in Figure 3-6, a simple heating system can be modelled as thermal feedback where heat loss is proportional to the difference between the oscillator and ambient temperatures. Therefore, total heat loss is subtracted from the electrical power injected into the micro-heaters to yield the net heat delivered to the oscillators. The power to energy conversion can

be modelled as an integrator (1/s in the Laplace domain), and energy is converted to temperature using a coefficient proportional to the inverse of the heat capacity of the system ($1/C_h$). Heat loss, proportional to the temperature difference between the heater and heat dissipation site, scales inversely to the system's heat resistivity (1/Rh). Therefore, the heat capacitance and resistance of the system defines its dynamics. Even though the ambient temperature affects the heat capacitance and resistance of the system, C_h and R_h are assumed to be constant for the sake of simplicity.

As dictated by general thermodynamics, the heater shows a very slow response to temperature variations compared to the electrical signal variations in the system. Therefore, a simple first-order model of the heater can be considered to add a pole near the origin (given by $1/R_hC_h$) to the open-loop transfer function of the PLL system. As will be shown in the following sections, in addition to this dominant pole in the vicinity of 0 Hz, the heating system can exhibit an extra pole and an extra zero that can enhance the stability of the PLL loop. As a result, the heating system can replace the loop filter.

Considering the model of Figure 3-5, the transfer function for the oscillator temperature variation in response to an ambient temperature change, T, assuming the initial ambient temperature $T_0 = 0$ and that both oscillators are at the same temperature, can be derived as:

$$H(s) \stackrel{\text{def}}{=} \frac{T_{osc}}{T}(s) = \frac{sDen(s)}{s^2R_hC_h\,Den(s)+s\,Den(s)+K_o\,R_hNum(s)}, \tag{3.4}$$

where $K_o = \frac{f_{02}\,C2}{N_2} - \frac{f_{01}\,C1}{N_1} = \frac{f_{01}\,\Delta C}{N_1} = \frac{f_{02}\,\Delta C}{N_2}$, and $\Delta C = C_2 - C_1$. The term $(1/R_hC_h)$ represents the dominant pole of the heater and Num(s) and Den(s) are the numerator and denominator of the loop filter model $\frac{Num(s)}{Den(s)}$. As shown in the next section, the loop filter can be completely removed since the heating system can provide the same functionality needed from a loop filter in a stable type II PLL.

As it is assumed that the frequency of the oscillators is linearly dependent on the temperature, the frequency shift in response to an ambient temperature variation can be written as:

$$H_{f1}(s) \stackrel{\text{def}}{=} \frac{f_1}{T}(s) = \frac{C_1 f_{01}\, T_{osc}}{T}(s) = C_1\, f_{01} H(s), \tag{3.5}$$

which presents the same dynamics of H(s) with the addition of the gain term $C_1\, f_{01}$.

Type II PLLs are generally employed to achieve a system with zero phase error and no residual error. This means the error between the output of this system and its input is finally reaching zero [104]. The open-loop transfer function of a type II PLL consists of two integrators or poles at the origin.

To be able to obtain a type II PLL from the system shown in Figure 3-5, $\frac{Num(s)}{Den(s)}$ is chosen to be only a gain factor K_d and therefore (3.4) can be written as:

$$H(s) \stackrel{\text{def}}{=} \frac{T_{osc}}{T}(s) = \frac{s}{s^2 R_h C_h\ + s\ + K_o\, K_d\, R_h} = \frac{s}{s R_h C_h \left(s\ + \frac{1}{R_h C_h}\right) + K_o\, K_d\, R_h}. \tag{3.6}$$

As mentioned before, the pole associated with the heating system is close to the origin, and then it can be assumed that $1/R_hC_h \rightarrow 0$. Hence, the transfer function of the system can be shown as:

$$H(s) \stackrel{\text{def}}{=} \frac{T_{osc}}{T}(s) \cong \frac{s}{s^2 R_h C_h\ + K_o\, K_d\, R_h}\ , \tag{3.7}$$

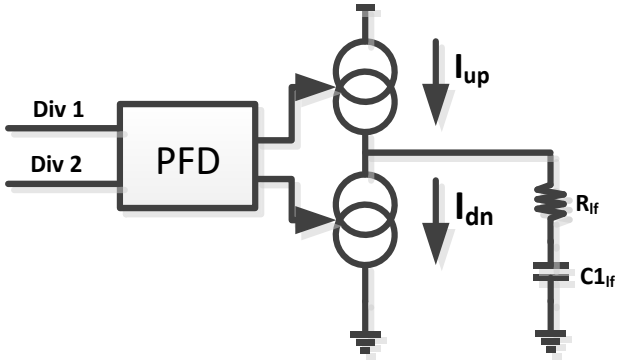
which has the same characteristics of a type II PLL.

Typically, a type II PLL consists of oscillators and a PFD and charge pump followed by a loop filter that can be a resistor and capacitor in series as shown in Figure 3-7. a to take charge from the charge pump [111]. The loop filter of such a system can be shown as:

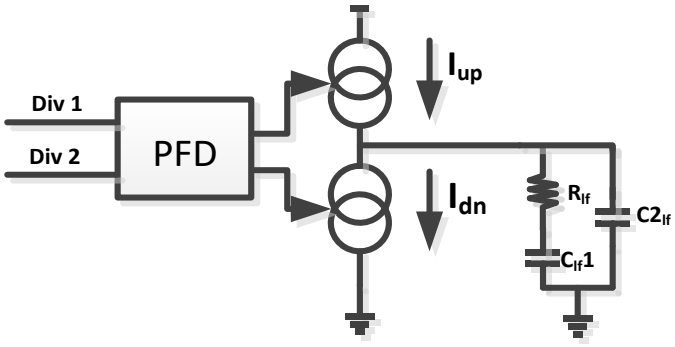
$$F_a(s) = R_{lf} + \frac{1}{s\, C1_{lf}} = \frac{1}{C1_{lf}} \left(\frac{s\, C1_{lf}\, R_{lf} + 1}{s}\right). \tag{3.8}$$

A type II PLL has a system transfer function with two poles at the origin and this means it is susceptible to instability. To increase the stability of such a system, a capacitor is added in parallel to the series resistor-capacitor of the loop filter. This new capacitor, shown as $C2_{lf}$ in Figure 3-7. b, is at least ten times smaller than $C1_{lf}$ to add a pole at higher frequencies. Therefore, the loop filter transfer function of this system can be shown below(C):

$$F_b(s) = \frac{1}{\frac{1}{R_{lf} + \frac{1}{sC1_{lf}}} + sC2_{lf}} = \frac{1}{C1_{lf} + C2_{lf}} \frac{1 + sR_{lf}C1_{lf}}{s\left(s\,R_{lf}\frac{C1_{lf}C2_{lf}}{C1_{lf} + C2_{lf}} + 1\right)}. \quad (3.9)$$



a) The loop filter has a pole at the origin and a zero.



b) The loop filter has pole at the origin and a pole-zero pair at higher frequencies to have a better stability.

Figure 3-7. A typical type II PLL has a charge pump and a loop filter with one pole at the origin and one zero(a) or a pole-zero pair at higher frequencies for stability reasons.

With the assumption that $C1_{lf} > 10 * C2_{lf}$, then (3.8) can be simplified as:

$$F_b(s) \cong \frac{1}{C1_{lf}} \frac{1 + sR_{lf}C1_{lf}}{s\left(s\,R_{lf}C2_{lf} + 1\right)}. \tag{3.10}$$

In the next section, similarities between the dynamics of the system with the heater and a type II PLL are discussed. It will be shown that the heating system can replace the charge pump and loop filter of a typical PLL while maintaining the characteristics of a type II PLL.

3.3.1.2 Heating system replacing the charge pump and the loop filter

As mentioned earlier, a stable type II PLL requires a loop filter consisting of a pole at the origin in addition to a zero and a pole at higher frequencies. Interestingly, it is noted that the micro-heater acts like a system with a pole close to the origin and a pole and zero at higher frequencies. This is like the response obtained from a charge pump and a loop filter, as shown in (3.10), and therefore it can be shown that the micro-heater in this system can eliminate the need for a charge pump and loop filter. To show this, the effect of the heating system is analysed here.

As presented in Figure 3-6.b, a first-order model of the heating system consists of a single-pole parallel RC equivalent circuit. The heat H going into the system is modelled as a current I, and the temperature T as a voltage V. A resistance models the heat loss mechanism of the heating system and capacitance models its heat capacity. The current-to-voltage transfer function of the equivalent electrical circuit is thus

$$\frac{V}{I}(s) = \frac{\frac{1}{C_h}}{s+\frac{1}{R_h C_h}}\ . \tag{3.11}$$

Therefore, a simple one-pole heating system with heat loss resistance of R_h and heat capacitance of C_h has been modelled with a parallel RC circuit with resistance R_h and capacitance C_h.

Since the heater has a very slow response, the pole in (3.11) can be considered to be almost at the origin and therefore, (3.10) can be written as:

$$\frac{V}{I}(s) \cong \frac{\frac{1}{C_h}}{s} . \tag{3.12}$$

This has the same effect as an integrator following a charge pump.

Further examination of the heating system shows that extra zero and pole can be modelled to model the system's behaviour at higher frequencies. Interestingly, this helps increase the stability of the system.

To find a more realistic model of the system, a higher order modeling of the system can be performed. A first step for this can be considering the second order effects of the heating system. For this purpose, the physical area between the heater and the outside environment is defined as an intermediate stage. It is assumed that the heater exchanges heat with this intermediate stage, which exchanges heat with the outside environment. This intermediate

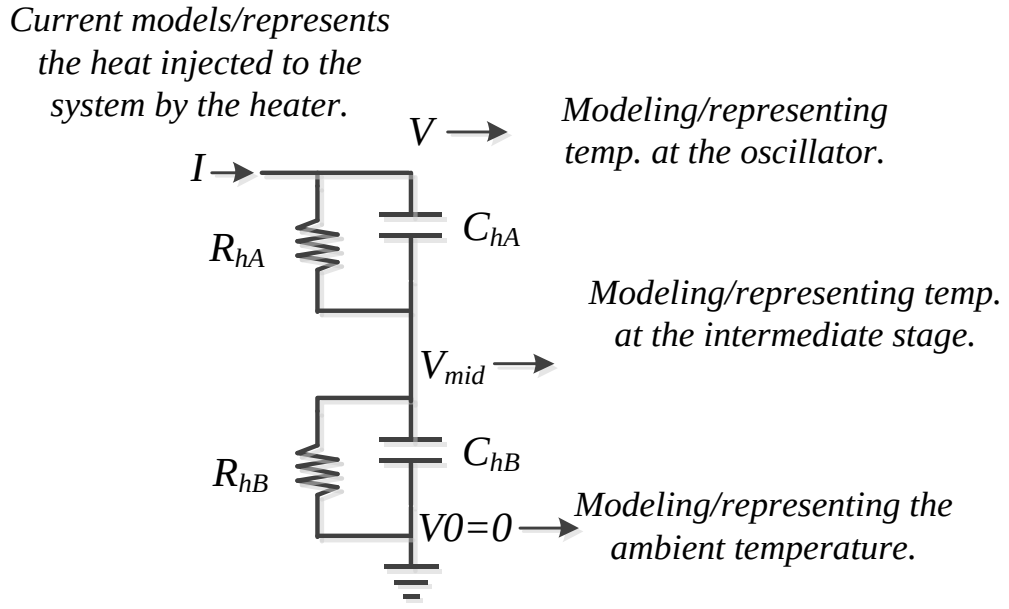


Figure 3-8. Second order RC circuit modeling the heating system.

stage represents the entire area of the chip starting from the immediate vicinity of the heater to the boundary of the chip and outside environment. This area is very large and has a very high heat capacity corresponding to a system model with a pole close to 0 Hz. The two-stage system can then be modelled by parallel RC circuits in series, as shown in Figure 3-8.

The transfer function from voltage to current of this system, which represents the oscillator temperature as a function of the heat injected by the heater, can therefore be expressed as

$$\frac{V}{I} = \frac{\frac{1}{C_{hA}}}{s + \frac{1}{R_{hA}C_{hA}}} + \frac{\frac{1}{C_{hB}}}{s + \frac{1}{R_{hB}C_{hB}}} = \frac{A(s-z)}{(s-p_A)(s-p_B)}, \tag{3.13}$$

which represents a system with two poles and one zero.

The second order model of the system can also be equivalently shown as in Figure 3-9.

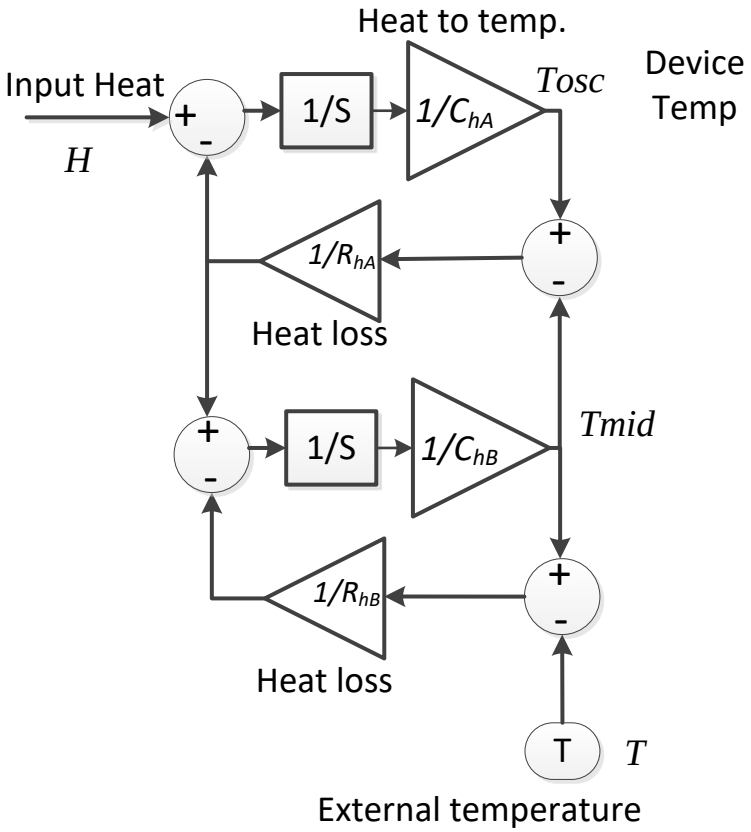


Figure 3-9. Second order modeling of the heating system.

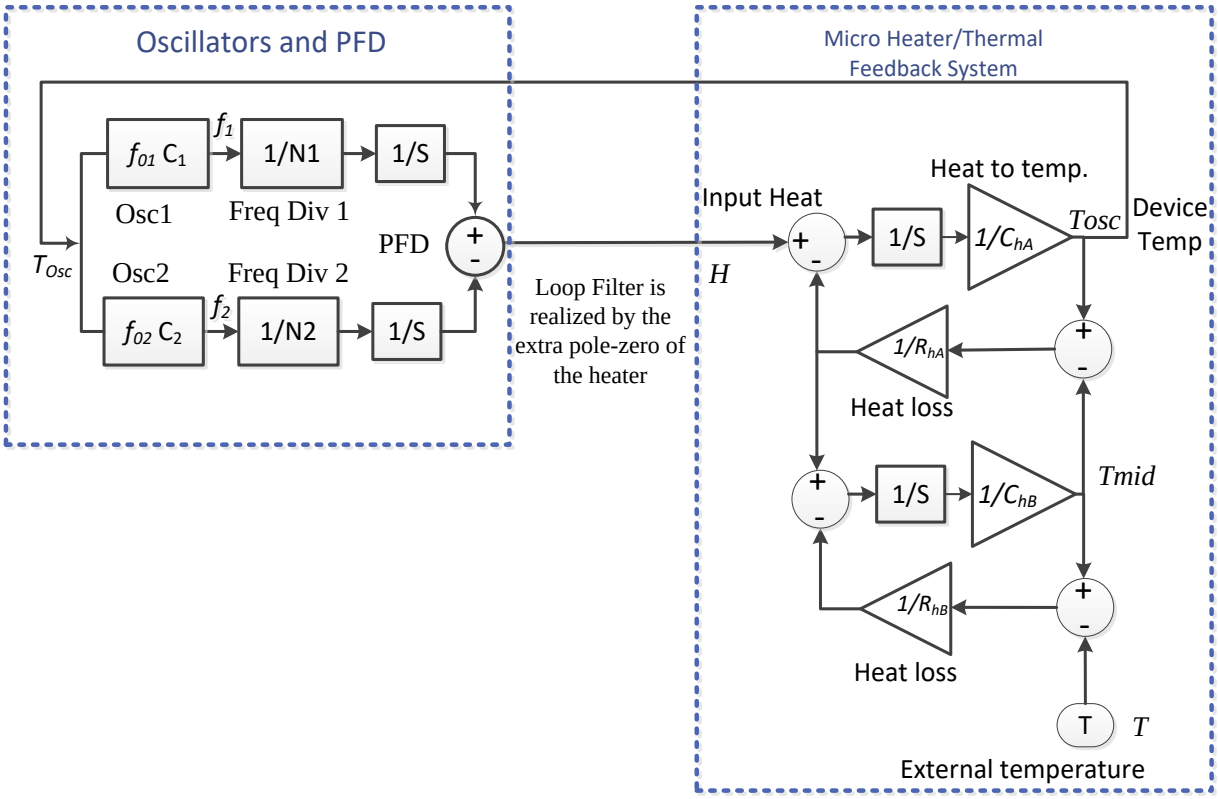


Figure 3-10. Second order effect of the heating system can produce the effect of the loop filter.

As previously discussed, one of the poles of the heating system can be considered to be almost at 0 Hz ($1/R_{hA}C_{hA} \cong 0$) and therefore, (3.13) can be simplified as (3.14).

$$\frac{V}{I} = \frac{T_{Osc}}{H} = \frac{\frac{1}{C_{hA}}\left(s + \frac{1}{R_{hB}C_{hB}}\right) + \frac{1}{C_{hB}}\left(s + \frac{1}{R_{hA}C_{hA}}\right)}{\left(s + \frac{1}{R_{hA}C_{hA}}\right)\left(s + \frac{1}{R_{hB}C_{hB}}\right)} \cong \frac{\left(\frac{1}{C_{hA}} + \frac{1}{C_{hB}}\right)s + \frac{1}{R_{hB}C_{hA}C_{hB}}}{s\left(s + \frac{1}{R_{hB}C_{hB}}\right)} \cong \frac{A(s-z)}{s(s-p)}, \quad (3.14)$$

This is the same filtering effect shown in (3.10) for a type II PLL with added zero-pole for stability. Such a PLL typically consists of a charge pump and an RC loop filter [111, 112]. However, here the heating system adds the same effect by adding a pole at the origin and an extra pole and zero to the system and therefore it can replace the charge pump and the loop filter needed in a type two PLL.

Eliminating the loop filter has the benefit of reducing chip area as integrated loop filters tend to be large, while removing the charge pump can reduce noise caused by issues such as charge sharing and clock feedthrough.

Figure 3-10 shows the system with no loop filter and charge pump, and the heating system provides the functionality of a charge pump and a loop filter.

In addition to the pole close to the origin and a zero, the higher order effects of the heating system add higher frequency poles and zeros to the system. However, these extra poles and zeros are at higher frequencies and can be assumed they are out of the bandwidth of the PLL.

3.3.1.3 Proportional and integral and higher frequency parts of the heating system transfer function

As explained in [111], the loop filter of a PLL in a general form can be shown as:

$$F(s) = F_{p+i}(s)\, F_{hf}(s), \tag{3.15}$$

where, $F_{p+i}(s)$ represents the proportional and integral parts of the loop filter and $F_{hf}(s)$ represents the high-frequency portion of it. $F_{hf}(s)$ has its greatest effects at higher frequencies and mostly out of the loop bandwidth of the PLL with the only constraint of it to be having a finite and non zero value at $F_{hf}(0)$. The proportional plus integral (P+I) factor of the loop filter, in general, can consist of as many integrators and not just limited to one integrator that is specific to the type II PLL. The general form of $F_{p+i}(s)$ is shown in (3.16).

$$F_{p+i}(s) = K_1 + \frac{K_2}{s} + \frac{K_3}{s^2} + \cdots. \tag{3.16}$$

In practice, only one integrator is mostly used in Fp+i(s), which creates a type II PLL. The number of integrators in the proportional plus integral part of the loop filter can only sometimes be two and rarely can be more than that [111].

Considering the first order model of the heating system shown in Figure 3-6, the transfer function of the heat injected to the system to its temperature variation can be shown as (3.11) and with the notation that pole added by the heating system is very close to the origin ($1/R_hC_h \cong 0$), the transfer function of the heating system can be modeled as an integrator as shown in (3.17).

$$\frac{V}{I} = \frac{T_{Osc}}{H} = \frac{\frac{1}{C_h}}{s + \frac{1}{R_h C_h}} \cong \frac{\frac{1}{C_{hA}}}{s}. \tag{3.17}$$

This model can provide the proportional plus integral part of the loop filter transfer function of a type II PLL. Similarly, it can be concluded that the higher frequency effects coming from the second order modelling of the heating system can make $F_{hs}(s)$ of the loop filter and can be eliminated for the frequencies inside the bandwidth of the PLL.

As a result, the heating system can be simplified using a first order model and only a gain stage is added to the system to model the gain obtained from different elements of the system as shown in Figure 3-11.

Therefore, the transfer function of the system can be deducted from (3.4) where $\frac{Num(s)}{Den(s)} = K_d$.

Thus,

$$H(s) \stackrel{\text{def}}{=} \frac{T_{osc}}{T}(s) = \frac{sDen(s)}{\left(s+\frac{1}{R_hC_h}\right) s\, R_hC_h\, Den(s)+K_o\, R_hNum(s)} = \frac{s}{\left(s+\frac{1}{R_hC_h}\right) s\, R_hC_h\, +K_o\, K_d\, R_h}. \qquad (3.18)$$

When the dominant heater pole $1/R_hC_h$ is close to zero, H(s) can be approximated as in (3.19):

$$H_{aprox}(s) = \frac{T_{osc}}{T}(s) \cong \frac{s}{s^2\, R_hC_h+K_oK_dR_h}\ , \qquad (3.19)$$

which is the transfer function of a type two PLL [111].

3.3.2 Analysis of the System Response to Step and Ramp of Ambient Temperature

Further insight into the system can be obtained by analyzing its response to a step and a ramp in the ambient temperature.

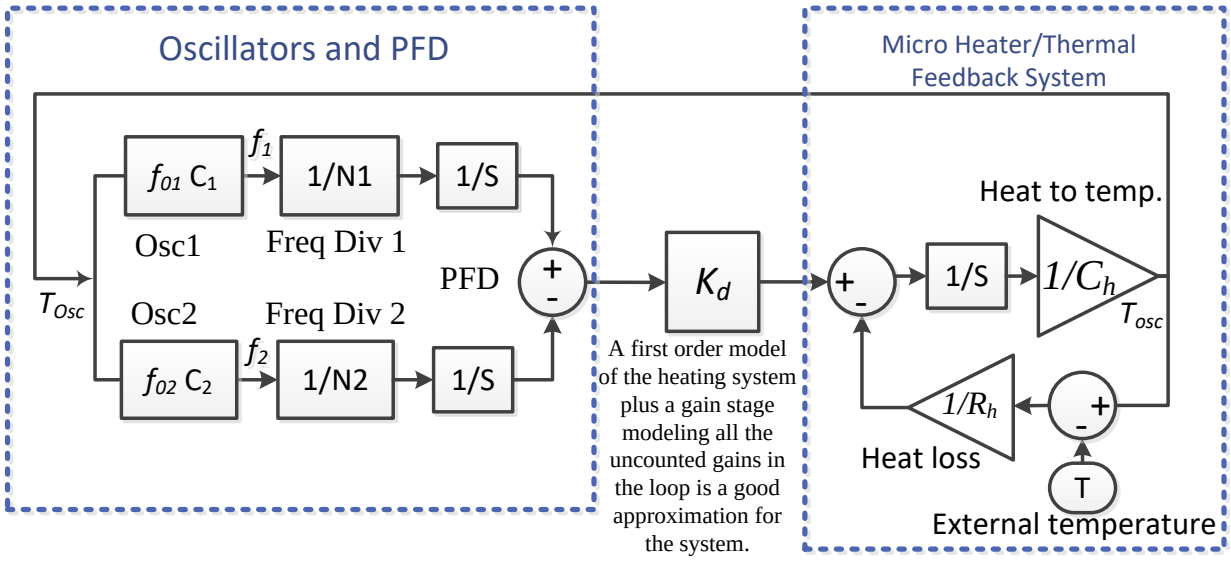


Figure 3-11. A first order model of the heating system plus a gain stage can be good approximation of the system in the frequencies in the bandwidth of the PLL.

From the finite value theorem, (3.19) leads to the conclusion that for the proposed system, a temperature step of T_s produces an actual oscillator temperature change of:

$$\Delta T_{osc}(t \to \infty) = \lim_{s \to 0} sH(s)\frac{T_s}{S} = H(0)T_s = 0 \tag{3.20}$$

Similarly, a temperature ramp having a slope $\dot{T}_r$ yields:

$$\Delta T_{osc}(t \to \infty) = \lim_{s \to 0} sH(s)\frac{\dot{T}_r}{s^2} \cong \frac{\dot{T}_r}{K_0 K_d R_h} \ . \tag{3.21}$$

It can be concluded that the final value of a change in T_{osc} caused by an ambient temperature step is zero. A ramp in the ambient temperature can cause a steady-state device temperature offset which is reversely proportional to $K_0K_dR_h$ and minimized by maximizing it.

3.4 Effects of Having Two Separate Micro-heaters on the System Performance

In the analysis presented in the previous section, it was assumed that both oscillators are at the exact same temperature. In systems where each oscillator has its own micro-heater, it is likely that this condition will not be met and the heating gain of each oscillator and its micro-heater will be slightly different than the other oscillator and its micro-heater. This will result in an additional frequency variation when the ambient temperature varies.

The system, in this case, can be modelled as shown in Figure 3-12, where Ch1 and Ch2 are the heat capacitance of each oscillator and RH1, and Rh2 are the heat resistance of them.

To find the temperature change at each oscillator in response to an external/ambient temperature change, the diagram in Figure 3-12 can be more simplified as the ones shown in Figure 3-13.a and Figure 3-13.b.

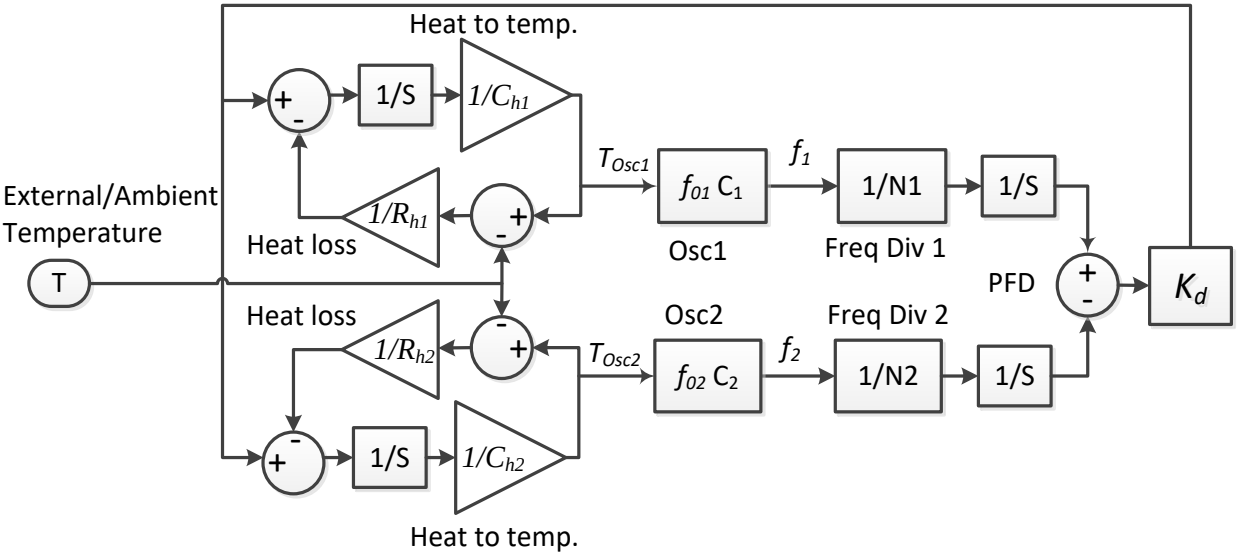


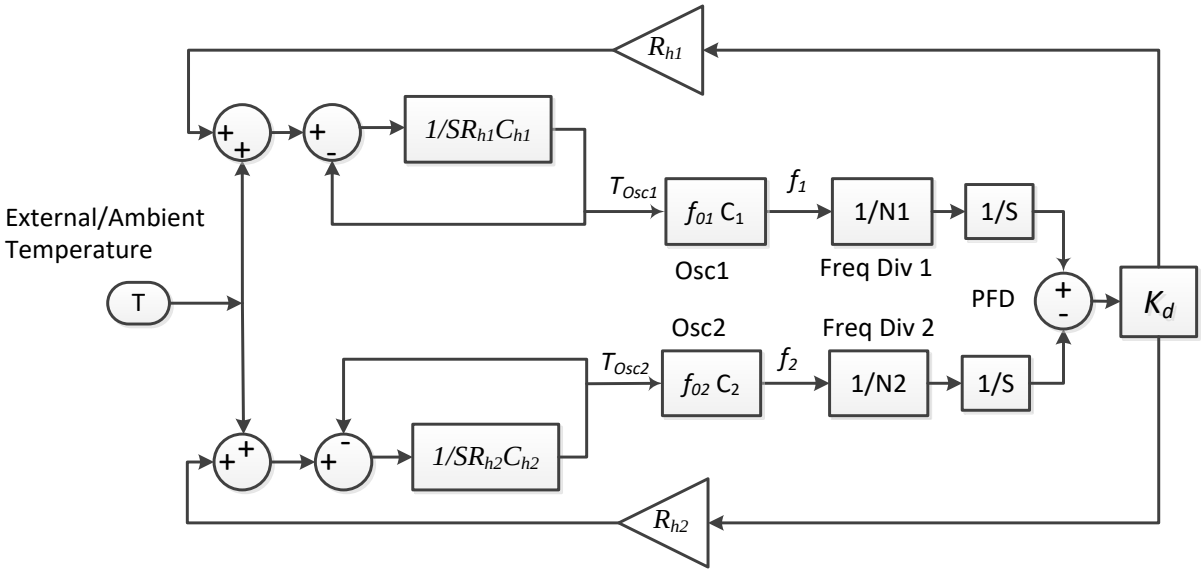
Figure 3-12. Linearized model of the system where each oscillator has a separate micro-heater.

Therefore, the temperature change at each oscillator in response to an external/ambient temperature change has the transfer function shown in (3.22):

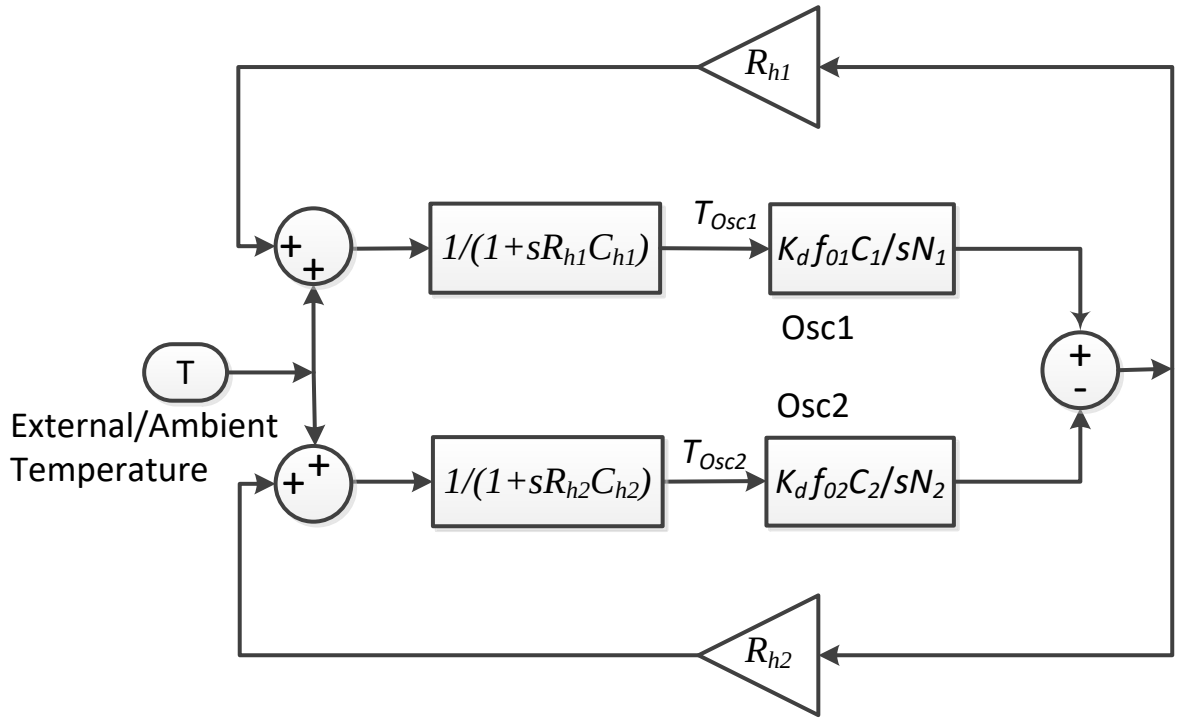
$$H_1(s) \stackrel{\text{def}}{=} \frac{T_{osc1}}{T}(s) = \frac{\frac{1}{1+sR_{h1}C_{h1}}\left(\frac{K_d f_{02} C_2}{sN_2(1+s\,R_{h2}C_{h2})}(R_{h1}-R_{h2})-1\right)}{\frac{K_d f_{01} C_1}{sN_1(1+s\,R_{h1}C_{h1})}-\frac{K_d f_{02} C_2}{sN_2(1+s\,R_{h2}C_{h2})}-1}, \tag{3.22}$$

where (3.22) can be written as (3.23):

$$H_1(s) \stackrel{\text{def}}{=} \frac{T_{osc1}}{T}(s) = \frac{\frac{1}{1+sR_{h1}C_{h1}}\left(\frac{K_d f_{02} C_2}{N_2(1+s\,R_{h2}C_{h2})}(R_{h1}-R_{h2})-s\right)}{\frac{K_d f_{01} C_1}{N_1(1+s\,R_{h1}C_{h1})}-\frac{K_d f_{02} C_2}{N_2(1+s\,R_{h2}C_{h2})}-s} \tag{3.23}$$



a) Simplified model of the system with two separate micro-heaters.



b) Simplified model of the system with two separate micro-heaters.

Figure 3-13. Simplified model of the system with two separate micro-heaters.

Using this transfer function, a temperature step of T_s produces an actual oscillator

temperature change of:

$$\Delta T_{osc1}(t \to \infty) = \lim_{s \to 0} sH_1(s)\frac{T_s}{s} = T_s \frac{\frac{f_{02}C_2}{N_2}\,(R_{h2} - R_{h1})}{\frac{f_{02}C_2}{N_2}R_{h2} - \frac{f_{01}C_1}{N_1}R_{h1}}. \tag{3.24}$$

Knowing that $\frac{f_{01}}{N_1} = \frac{f_{02}}{N_2}$ when the PLL is in lock, (3.24) can be simplified as

$$\Delta T_{osc1}(t \to \infty) = T_s \frac{\frac{f_{02}C_2}{N_2}\,(R_{h2} - R_{h1})}{\frac{f_{02}C_2}{N_2}\left(R_{h2} - \frac{C_1}{C_2}R_{h1}\right)} = T_s \frac{\left(\frac{R_{h2}}{R_{h1}} - 1\right)}{\left(\frac{R_{h2}}{R_{h1}} - \frac{C_1}{C_2}\right)}. \tag{3.25}$$

If the micro-heaters are identical (R_{h1}=R_{h2}), the numerator of (3.15) is equal to zero. This means that the final temperature at the oscillators does not vary due to a step-change in the ambient temperature. However, in the case where the heaters are not identical, any changes in the ambient temperature will induce a temperature difference between the oscillators even when the PLL is locked and thus causes a frequency variation on the oscillators.

Knowing that C_{h1} and C_{h2} are greater than zero, from the graph of the system depicted in Figure 3-13, it can be concluded that to maintain negative feedback around the loop, C_1 should be smaller than C_2, a condition that is ensured if C_1<0 and C_2>0. Therefore, in such a case, it can be concluded that a larger $|C_1/C_2|$ decreases the effect of the ambient temperature on the local temperature of the oscillators. For example, if R_{h2}/R_{h1}=1.01 and C1/C2 is very small, the effect of one-unit ambient temperature change will translate to only 0.01of a unit temperature change at the oscillators. However, if $|C_1/C_2|$ increases to 2, and for the same one-unit ambient temperature change, the temperature of the oscillators will change by 0.003 units, which is a three times improvement compared to the previous case.

In addition, as will be shown in the next chapter and in [49], selecting the right difference between the two TCfs can also reduce the phase noise obtained from the oscillators in the system.

3.5 Summary and Conclusion

In this chapter, the proposed compensation system was first introduced and its functionality was illustrated. To this end, a possible block diagram of the PLL system proposed to be employed for this scheme was presented. In the proposed PLL system, two oscillators are used to sense the temperature, and the effect of the temperature to frequency function of the oscillators on the system's behavior was examined. It was shown that unwanted effects of having non-monotonic temperature to frequency curves of oscillators could be avoided. Consequently, the temperature to frequency curve of the oscillators was assumed to be a straight-line for simplicity, and based on that, a linear approximation of the system was modelled.

Next, the system was analyzed using the linear model provided. The effects of step and ramp changes in the ambient temperature on the system were examined. In addition, the effect of having a separate micro-heater for each oscillator, which means each oscillator might have slightly different temperatures as opposed to having one micro-heater for both oscillators, were studied. It was shown that having a separate micro-heater for each oscillator can reduce the temperature compensation capability of the system, and in possible future works, it should be addressed.

Chapter 4 Phase Noise of a Dual Loop PLL for Temperature Compensation of Oscillators

4.1 Introduction

In the ever faster clocking systems nowadays, phase noise is the most important specification. In the proposed scheme, two oscillators interact with each other, and this needs to be analyzed and based on that, a better understanding of how this interaction works is obtained. This can lead to a better design approach to meet the phase noise requirements. Therefore, in this chapter, first, the system is modeled to analyze it next. In the end, possible design considerations resulting from this analysis are discussed.

4.2 System Description

4.2.1 Temperature Compensation Scheme

As stated in the previous sections, in the proposed temperature compensation technique, two oscillators' divided frequencies will be locked to each other using a PLL system. The feedback force in this PLL is applied through the heat injected into the oscillators using micro-heaters. The two oscillators used in this scheme need to have different temperature coefficients of frequency (TCf) to provide the force in the loop to keep their temperature and, consequently, their frequency fixed, as shown in Figure 4-1.

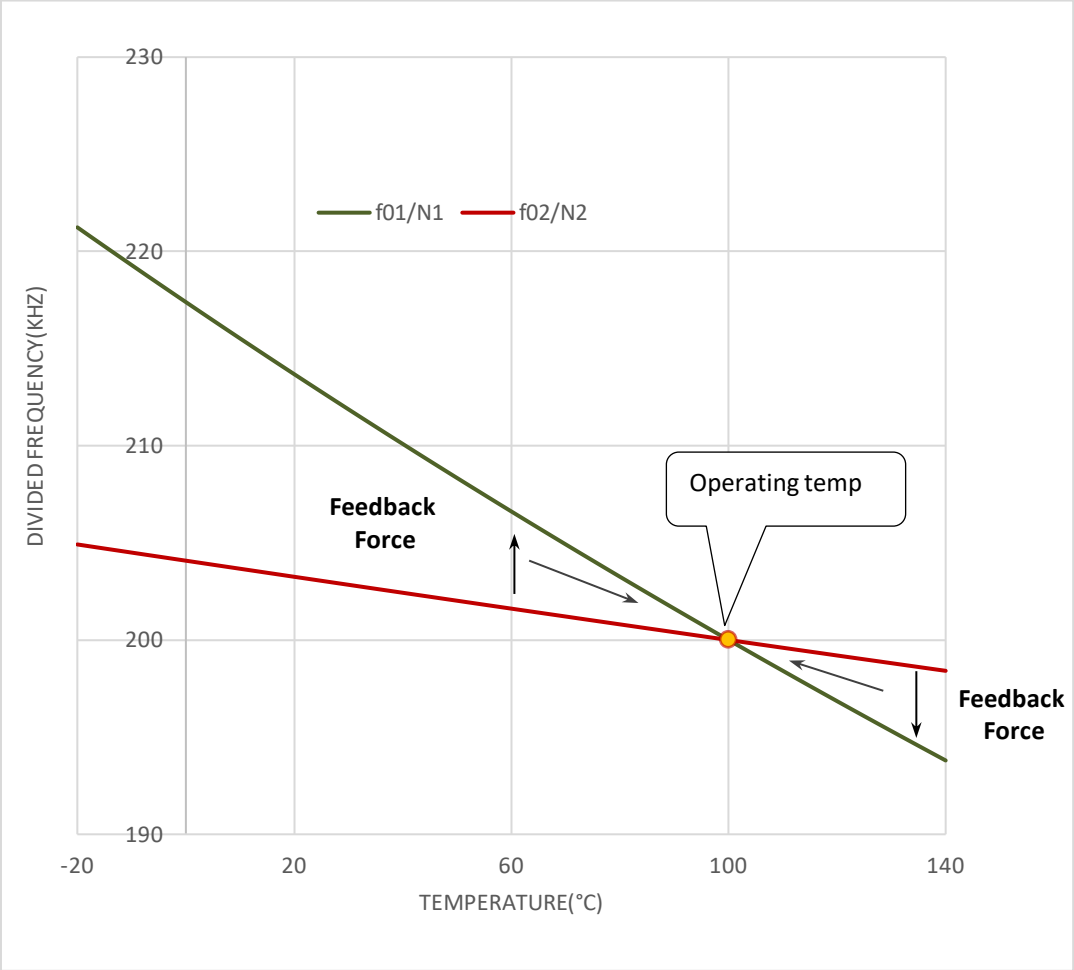
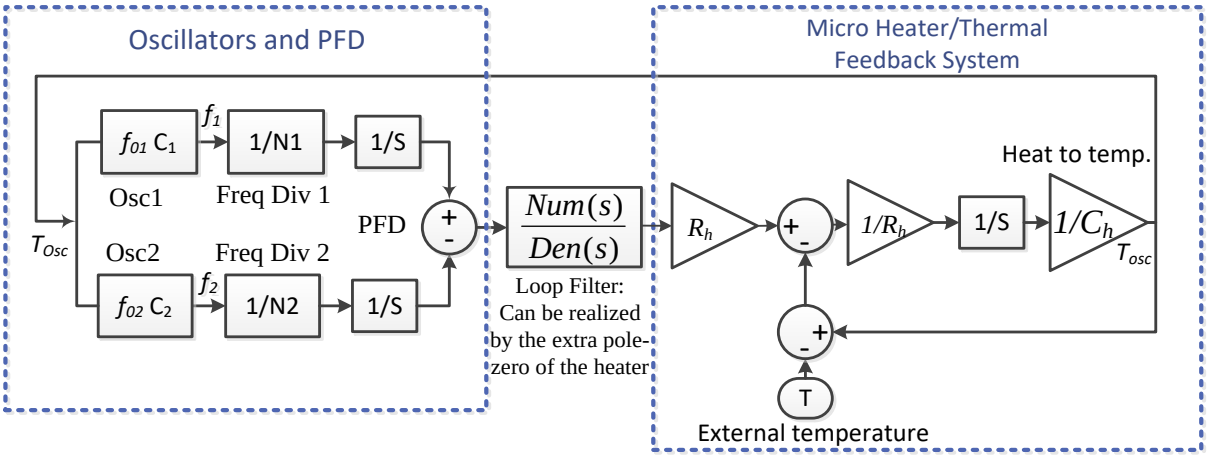


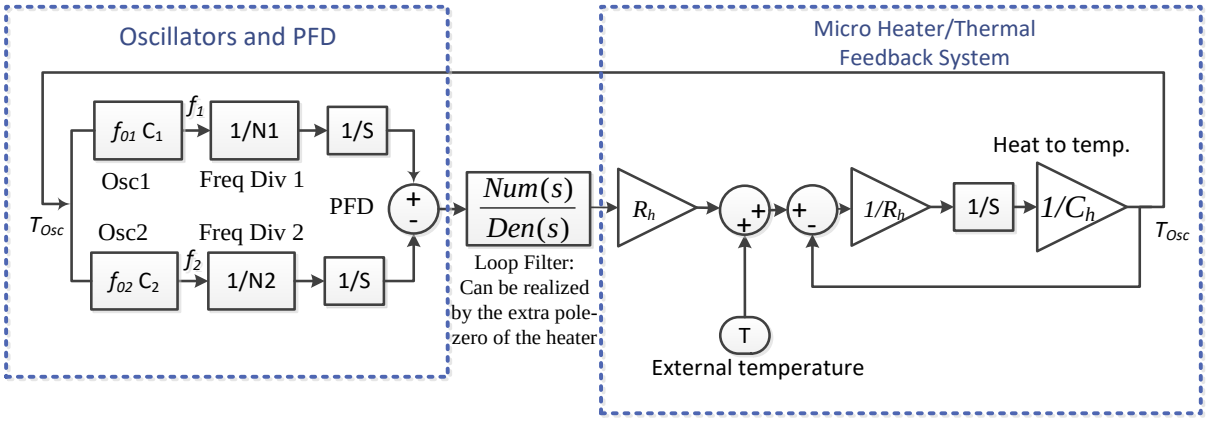
Figure 4-1. The difference between the slopes of the two lines produces the feedback force.

The mathematical system model shown in Figure 3-5 can be more simplified as in Figure 4-2 to have the ambient temperature as an input to the system. The system, as shown, consists of two oscillators, each followed by a frequency divider where the two frequency divider outputs feed the input of a phase-frequency detector (PFD). A possible loop filter is assumed to follow to account for any uncounted gain and set the loop dynamics. The division ratio of the frequency dividers is selected such that at the operating temperature, T_0:

$$\frac{f_{01}}{N_1} = \frac{f_{02}}{N_2}, \tag{4.1}$$



a) The heat loos resistance R_h can be moved to the feedback loop.



b) The linearized system model can be shown in response to ambient temperature as an input.

Figure 4-2. Linearized model of the system.

where each of f_{01} and f_{02} is the frequency of one of the resonators at T_0.

In the previous chapter, the functionality of the compensation system was elaborated. In this chapter, it is analyzed in terms of phase noise.

4.2.2 Phase Noise Interaction of the Two Oscillators

As the system consists of two oscillators in its feedback loop, the phase noise of each oscillator impacts the other one. This has not been considered for such a system before and is thus studied here.

4.3 System Analysis

4.3.1 Linear Approximation

To simplify the analysis, the system is approximated by a linear model. As suggested in [110], a linear approximation is valid for a system in a locked state. Therefore, the system can be modeled as shown in Figure 3-5 and thus Figure 4-2 [49, 113]. As stated in Chapter 3, the model parameters are detailed below.

As shown in Figure 4-2, a simple heating system can be modeled as thermal feedback where heat loss is proportional to the difference between the oscillator and ambient temperatures[114]. Therefore, total heat loss is subtracted from the electrical power injected into the micro-heaters to yield the net heat delivered to the oscillators. The power to energy conversion can be modeled as an integrator (1/s in the Laplace domain), and energy is converted to temperature using a coefficient proportional to the inverse of the heat capacity of the system ($1/C_h$). Heat loss, proportional to the temperature difference between the heater and heat dissipation site, scales inversely to the system's heat resistivity ($1/Rh$). Therefore, the heat capacitance and resistance of the system define its dynamics.

- R_h: The heat resistance which is inversely proportional to the amount of energy dissipated from the heating area to the ambient environment per the temperature difference between the two.

- C_h: The heat capacitance of the heating area which is proportional to the amount of energy needed to change the temperature of the heating area by one unit of temperature. This is inversely proportional to the ratio of the temperature change of the heating area to the thermal energy consumed to heat them up.

- C1, C2: The TCf's of Oscillators 1 and 2, respectively.

Analyzing this model, from Figure 4-2, the open loop transfer function can be written as:

$$G(s) = \frac{K_o}{s} \frac{\frac{1}{s\,C_h}}{1+\frac{1}{R_h s\,C_h}} \frac{Num(s)}{Den(s)} \tag{4.2}$$

where K_o is defined as

$$K_o \triangleq \frac{f_{01}\,C1}{N_1} - \frac{f_{02}\,C2}{N_2} = \frac{f_{01}\,\Delta C}{N_1} = \frac{f_{02}\,\Delta C}{N_2} \tag{4.3}$$

,with $\Delta C \triangleq C1 - C2 \geq 0$.

As suggested by (3.14), to obtain a type II PLL from this system, the second order effects of the heating system can be shown as

$$F(s) = \frac{K_d \left(1 - \frac{s}{z_{lf}}\right)}{\left(1 - \frac{s}{p_{lf}}\right)}, \tag{4.4}$$

where K_d is its combined gain. This makes (4.2) look like

$$G(s) = \frac{K_o\,K_d}{s} \frac{R_h}{1 + s\,R_h C_h} \frac{1 - \frac{s}{Z_{lf}}}{1 - \frac{s}{p_{lf}}} \ . \tag{4.5}$$

considering the pole created by the heating system is really close to the origin, (4.5) can be simplified as

$$G(s) = \frac{K_o\,K_d}{s} \frac{1}{C_h(s + \frac{1}{R_h C_h})} \frac{1 - \frac{s}{Z_{lf}}}{1 - \frac{s}{p_{lf}}} \cong \frac{K_o\,K_d}{C_h s^2} \frac{1 - \frac{s}{Z_{lf}}}{1 - \frac{s}{p_{lf}}} \ . \tag{4.6}$$

To ensure the stability of the second order system, the non-zero pole in G(s) is placed at a much higher frequency than the zero of the open-loop transfer function. Therefore, the open-loop transfer function can be approximated by:

$$G(s) \cong \frac{K_o K_d}{s^2 C_h}\left(1 - \frac{s}{Z_{lf}}\right). \tag{4.7}$$

The closed-loop system transfer function H(s) is then shown to be:

$$H(s) \stackrel{\text{def}}{=} \frac{G(s)}{1+G(s)} = \frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}\ . \tag{4.8}$$

As a result, the second-order parameters of this system, namely the loop gain, K, the natural frequency, ω_n, and the damping factor, ζ, can be given by: $K = \frac{K_o K_d}{C_h Z_{lf}}$, $\omega_n = \sqrt{\frac{K_o K_d}{C_h}}$ and $\zeta = \frac{1}{2}\sqrt{\frac{K_o K_d}{C_h z_{lf}^2}}$.

The phase domain linearized model of the system is shown in Figure 4-3, where the phase noise contributions are assumed to be additive [111]. To assess the effect of the two oscillators on the phase noise of each other, here, only the phase noise generated by the two oscillators is considered in the calculations.

Deducted from Figure 4-3, the transfer function of the output phase noise of an oscillator, with respect to the phase noise generated in itself, is given by:

$$P_{11}(s) \stackrel{\text{def}}{=} \frac{\Phi_{out1}(s)}{\Phi_{r1}(s)} = \frac{1 - \frac{f_{02}C_2}{N_2}\frac{K_d}{s^2 C_h}\left(1 - \frac{s}{Z_{lf}}\right)}{1 + G(s)}. \tag{4.9},$$

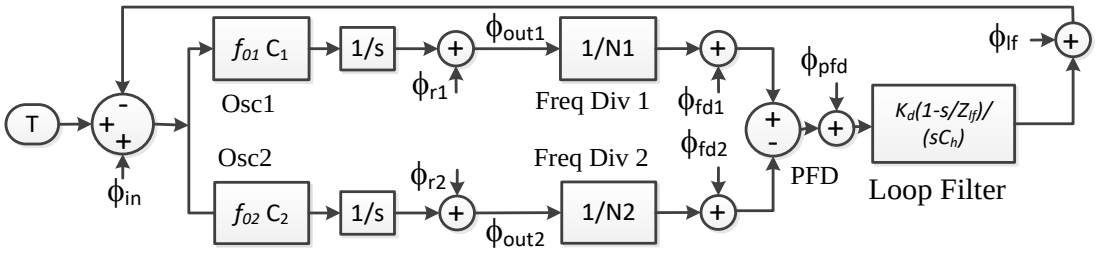


Figure 4-3. Phase noise contribution by each block of the system.

where $\Phi_{r1}(s)$, is the phase noise generated in oscillator 1 and $\Phi_{out1}(s)$ is the phase noise measured at the output of oscillator 1 when the loop is closed.

$P_{11}(s)$ can then be written as:

$$P_{11}(s) = \frac{1 + G(s) - G(s) - \frac{f_{02}C_2}{N_2}\frac{K_d}{s^2 C_h}\left(1 - \frac{s}{Z_{lf}}\right)}{1 + G(s)} = 1 - \frac{\left(\left(\frac{f_{01}C_1}{N_1} - \frac{f_{02}C_2}{N_2}\right) + \frac{f_{02}C_2}{N_2}\right)\frac{K_d}{s^2 C_h}\left(1 - \frac{s}{Z_{lf}}\right)}{1 + G(s)} \quad (4.10).$$

And therefore, using (4.3), $P_{11}(s)$ can be written as,

$$P_{11}(s) = 1 - \frac{\frac{f_{01}C_1}{N_1}\frac{K_d}{s^2 C_h}\left(1 - \frac{s}{Z_{lf}}\right)}{1 + G(s)} = 1 - \frac{\frac{C1}{\Delta C}G(s)}{1 + G(s)} = 1 - \frac{C1}{\Delta C}H(s). \quad (4.11).$$

A similar expression for the output phase noise resulting from a neighboring oscillator can be derived as:

$$P_{12}(s) \stackrel{\text{def}}{=} \frac{\Phi_{out1}(s)}{\Phi_{r2}(s)} = \frac{\frac{f_{01}C_1}{N_2}\frac{K_d}{s^2 C_h}\left(1 - \frac{s}{Z_{lf}}\right)}{1 + G(s)}. \quad (4.12),$$

where $\Phi_{r2}(s)$, is the phase noise generated in oscillator 2 and $\Phi_{out2}(s)$ is the phase noise measured at the output of oscillator 2 when the loop is closed.

Using (4.3), it will lead to

$$P_{12}(s)=\frac{\frac{f_{01}C_1}{f_{02}\Delta C}\frac{f_{02}\Delta C}{N_2}\frac{K_d}{s^2C_h}\left(1-\frac{s}{Z_{lf}}\right)}{1+G(s)}=\frac{f_{01}C_1}{f_{02}\Delta C}\frac{G(s)}{1+G(s)}=\frac{f_{01}}{f_{02}}\frac{C_1}{\Delta C}H(s). \quad (4.13)$$

For the sake of simplicity, if it is assumed that N1 is equal to N2, then $f_{01}\cong f_{02}$ and therefore, (4.13) can be rewritten as:

$$P_{12}(s)=\frac{\frac{f_{01}}{N1}}{\frac{f_{02}}{N2}}\frac{N1}{N2}\frac{C_1}{\Delta C}H(s)=\frac{N1}{N2}\frac{C_1}{\Delta C}H(s)\cong\frac{C1}{\Delta C}H(s) \quad ;N1=N2\ or\ f_{01}=f_{02}. \quad (4.14)$$

Similarly, relationships for the other oscillator can be obtained, and all the relationships between the phase noise the two oscillators on each other can be written as below.

$$P_{11}(s)\overset{\text{def}}{=}\frac{\Phi_{out1}(s)}{\Phi_{r1}(s)}=1-\frac{C_1}{\Delta C}H(s), \quad (4.15)$$

$$P_{12}(s)\overset{\text{def}}{=}\frac{\Phi_{out1}(s)}{\Phi_{r2}(s)}=\frac{f_{01}}{f_{02}}\frac{C_1}{\Delta C}H(s)\cong\frac{C_1}{\Delta C}H(s) \quad ;f_{01}\cong f_{02}, \quad (4.16)$$

$$P_{22}(s)\overset{\text{def}}{=}\frac{\Phi_{out2}(s)}{\Phi_{r2}(s)}=1+\frac{C_2}{\Delta C}H(s), \quad (4.17)$$

$$P_{21}(s)\overset{\text{def}}{=}\frac{\Phi_{out2}(s)}{\Phi_{r1}(s)}=-\frac{f_{02}}{f_{01}}\frac{C_2}{\Delta C}H(s)\cong-\frac{C_2}{\Delta C}H(s) \quad ;f_{01}\cong f_{02}, \quad (4.18)$$

As $H(s)\to 1$ for low frequencies ($|s|\ll\omega_n$), and $H(s)\to 0$ for high frequencies ($|s|\gg\omega_n$), simpler relationships can be derived for the simplified case where f_{01}=f_{02}. For low frequencies,

$$\begin{cases}|P_{12}(s)|=|P_{22}(s)|=\left|\frac{C1}{\Delta C}\right|\\ |P_{21}(s)|=|P_{11}(s)|=\left|\frac{C2}{\Delta C}\right|\end{cases} \quad ;|s|\ll\omega_n, \quad (4.19)$$

and for high frequencies,

$$\begin{cases}P_{11}(s)=P_{22}(s)=1\\ P_{12}(s)=0\\ P_{21}(s)=0\end{cases} \quad ;|s|\gg\omega_n. \quad (4.20)$$

As shown in (4.20), at higher frequencies, the two oscillators do not affect the phase noise of each other, and they act as stand-alone oscillators without much effect on the far-out phase noise of each other. However, at low frequencies, as shown in (4.19), the two oscillators in

the loop affect each other with a term inversely proportional to |ΔC|. Therefore, it can be concluded that increasing |ΔC| can help decrease the oscillators' close-in phase noise.

To examine the effect of the phase noise generated in both oscillators at the output of Oscillator 1, we can write the power spectral density of the total phase noise caused by both oscillators as:

$$\begin{cases} S_{\Phi_{out1}} = \left(\frac{C_2}{\Delta C}\right)^2 S_{\Phi_{r1}} + \left(\frac{C_1}{\Delta C}\right)^2 S_{\Phi_{r2}} & ; |s| \ll \omega_n \\ S_{\Phi_{out1}} = S_{\Phi_{r1}} & ; |s| \gg \omega_n \end{cases}, \tag{4.21}$$

where $S_{\Phi_{r1}}$ and $S_{\Phi_{r2}}$ are the power spectral density of the phase noise generated by Oscillators 1 and 2, respectively.

From (4.21), it can be concluded that Oscillator 2 does not contribute to the far-out phase noise of Oscillator 1. However, at small offsets, the phase noise at the output of Oscillator 1 can be decreased if $|\Delta C|$ increased and $|C1|$ and $|C2|$ are decreased. It may be difficult to engineer all of these parameters simultaneously, but tuning fewer parameters might be feasible for specific cases.

In practice, an interesting scenario to be considered is the one when the main oscillator is a high-quality, low noise oscillator, and a second low-cost, high noise oscillator is used to construct the PLL loop for the compensation purpose. Here, it is assumed that Oscillator 1 is the high-quality, low noise oscillator and Oscillator 2 is the low-cost high noise one. The objective is to decide the optimum TCf values for each oscillator to have the minimum phase noise out of Oscillator 1.

For this purpose, from (4.21), it can be determined that reducing $|C1/\Delta C|$ which means reducing $|C1|$ and increasing $|\Delta C| = |C1 - C2|$ can reduce the effect of the noisy Oscillator 2 on Oscillator 1. Therefore, one good choice can be using the minimum value possible for $|C1|$ and increasing value of $|C2|$ in comparison to $|C1|$. Picking the minimum possible TCf value for Oscillator 1 is also desired for the temperature stability of the oscillator. Therefore, picking a small value for $|C1|$ and a large value for $|C2|$ can make (4,21) simplified as,

$$\begin{cases} S_{\Phi_{out1}} = S_{\Phi_{r1}} & ; |C2| \gg |C1|, |s| \ll \omega_n \\ S_{\Phi_{out1}} = S_{\Phi_{r1}} & ; |s| \gg \omega_n \end{cases} . \quad (4.22)$$

As (4.22) shows, the phase noise effect of adding a low-cost noisy oscillator to the PLL compensation loop can be even removed by increasing the TCf value of the second oscillator.

It should be noticed that changing ΔC can change the dynamics of the loop. To avoid this, the increase in the loop gain caused by increasing ΔC $s$hould be compensated for in other blocks of the system, such as in the phase-frequency detector or the loop filter.

4.4 Simulation Results

A system is simulated in both circuit and system simulators to verify the analysis presented in the previous section. A system similar to that of Figure 4-2 is designed and used in simulations, with $\omega_n = 10KHz$ and $\zeta = 1$ to have a critically damped system.

Six different pairs of oscillators are used for the simulation. In each pair, Oscillators 1 and 2 have the frequencies f01=8.0895MHz and f02=8.2821MHz, and the dividers are set to N1= 42 and N2=43, respectively. To keep the dynamics of the system fixed, when different values of ΔC are used, the gain stage is changed to compensate for changes in ΔC, and to maintain the loop dynamics.

Firstly, the system is implemented in MATLAB Simulink, and the resulting phase noise transfer functions in response to each of the oscillators will be shown. Secondly, the phase noise generated in each resonator-based oscillator is modeled in Verilog-A, and the resulting output phase noise is examined.

4.4.1 System Response in Simulink

The linear model of Figure 4-2 is implemented in Simulink with two oscillators having different TCf values. Figure 4-4 shows the resulting transfer functions of the phase noise generated in each oscillator to the output of either oscillator. As predicted by (4.19) and as shown in Figure 4-4 (b) and Figure 4-4 (d), the phase noise effect of Oscillator 2 on Oscillator 1 and on itself, $|P_{12}(s)|^2$ and $|P_{22}(s)|^2$, will be smaller for the systems with lower $|C1/\Delta C|$. Moreover, for lower frequencies, when $|\Delta C|$ is doubled and $|C1|$ is fixed, both $|P_{12}(s)|^2$and $|P_{22}(s)|^2$ decrease by 6 dB. However, when $|C1|$ is set to its minimum value to reduce the effect of the phase noise of Oscillator 2 on the output phase noise, increasing $|\Delta C|$ implies an increase of $|C2|$ and this means $|C2/\Delta C|$ does not vary substantially. This explains the very small change of $|P_{11}(s)|^2$ and $|P_{21}(s)|^2$ shown in Figure 4-4 (a) and (c).

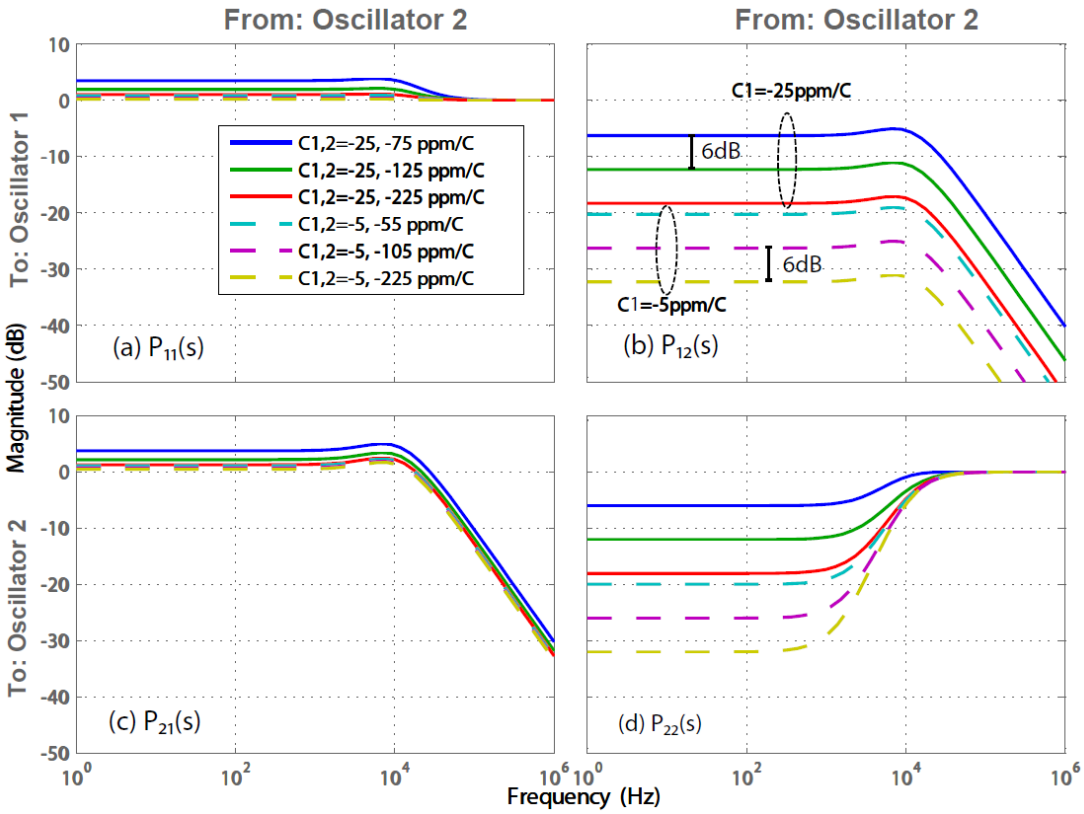


Figure 4-4. Transfer functions of the phase noise generated in each oscillator to the output of either oscillator.

4.4.2 Phase Noise Simulation in Verilog-A

As suggested in [115], to speed up the phase noise analysis of the whole system at the circuit level, each block of the system can be modeled in the phase domain, and then it is simulated at the circuit level. In this fashion, the phase noise of each building block of the system is included in its Verilog-A model, and noise analysis can show the effect of each noise component at any specific output point of the system. In this case, the effect of the oscillators on each other is considered. The system topology is similar to the one used before and is shown in Figure 4-2.

The phase noise generated in each oscillator is assumed to have a power spectral density of the form $K_3/f^3 + K_2/f^2$, as suggested in[115]. To model a realistic oscillator, by changing parameters K3 and K2, a phase noise similar to the resonator-based oscillator reported in [19] was modeled.

Figure 4-5 shows the phase noise at the output of Oscillator 1 when both oscillators 1 and 2 generate the same phase noise and compare it with the phase noise of one oscillator when it is standalone and not used in the loop. As predicted by (4.21), Figure 4-5(a) confirms that when $|C1|$ is small (-5ppm/°C), the phase noise generated in Oscillator 1 is the main contributor to its output phase noise, and this contribution is proportional to $|C2/\Delta C|$, which does not change significantly when $|\Delta C|$ is varied. Conversely, as depicted in Figure 4-5(b), when $|C1|$ is large (C1=-25ppm/°C), the effect of the phase noise generated in Oscillator 2 is a significant contributor to the output phase noise of Oscillator 1, and therefore, reducing $|C1/\Delta C|$ (by increasing $|\Delta C|$) can reduce the output phase noise significantly.

It is also observed from Figure 4-5 that at higher frequencies ($\omega \gg \omega_n$), regardless of the TCf values of the two oscillators, the output phase noise of the oscillators is equal to the phase noise generated standalone as predicted by (4.22).

As mentioned in the above simulations, two high-quality resonator-based oscillators with the same low phase noise values were modeled. An interesting observation comes from replacing resonator-based Oscillator 2 with an all-CMOS oscillator that is lower in price and has much higher phase noise. Such a system reduces the cost of implementation compared to a dual resonator system.

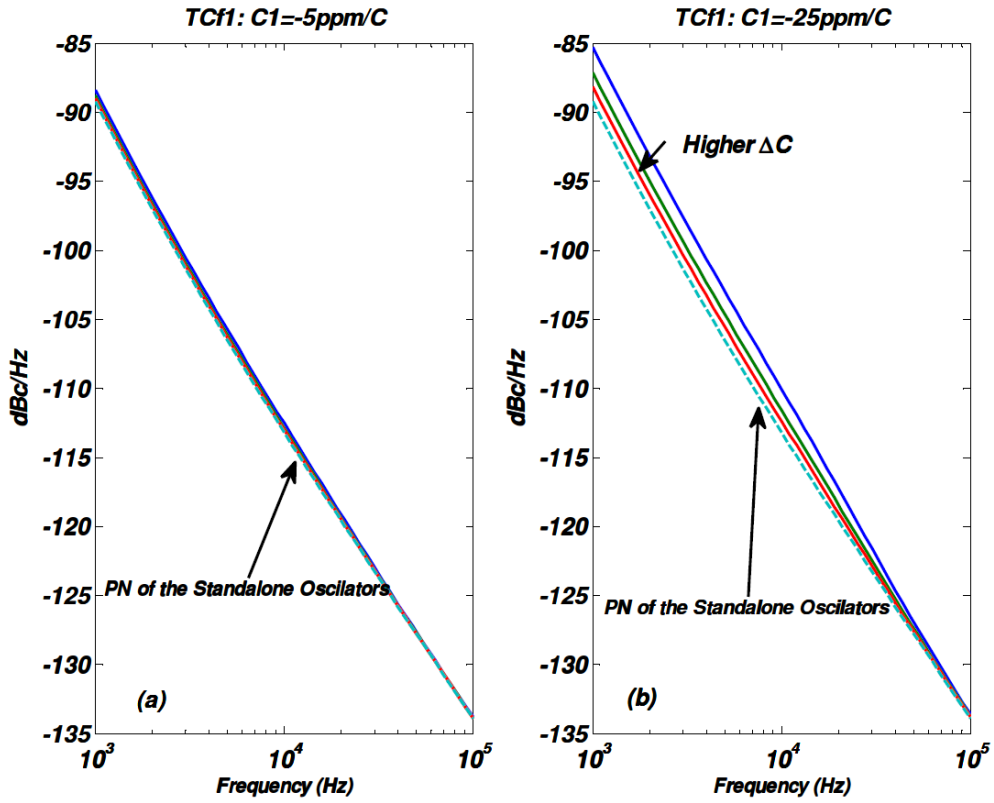


Figure 4-5. Phase noise observed at the output of Oscillator 1 when both oscillators generate equal phase noise, for ΔC=50, 100, 200 ppm/°C.

As suggested by (4.22), when $|C1|$ is small (C1=-5ppm/°C) compared to $|C2|$, similar to what was observed in Figure 4-5(a), Figure 4-6(a) shows that, the phase noise at the output of the Oscillator 1 is mainly affected by the noise generated in itself and varying $|\Delta C|$ has a marginal effect on the phase noise at the output of Oscillator 1(when $|\Delta C|$ varies, $|C2/\Delta C|$ does not vary significantly). Conversely, as shown in Figure 4-6(b), when $|C1|$ is larger (C1 = -25 ppm/°C), since $|C1/\Delta C|$ is increased considerably, the phase noise at the output of Oscillator 1 is deteriorated significantly by the CMOS oscillator and strongly depends on

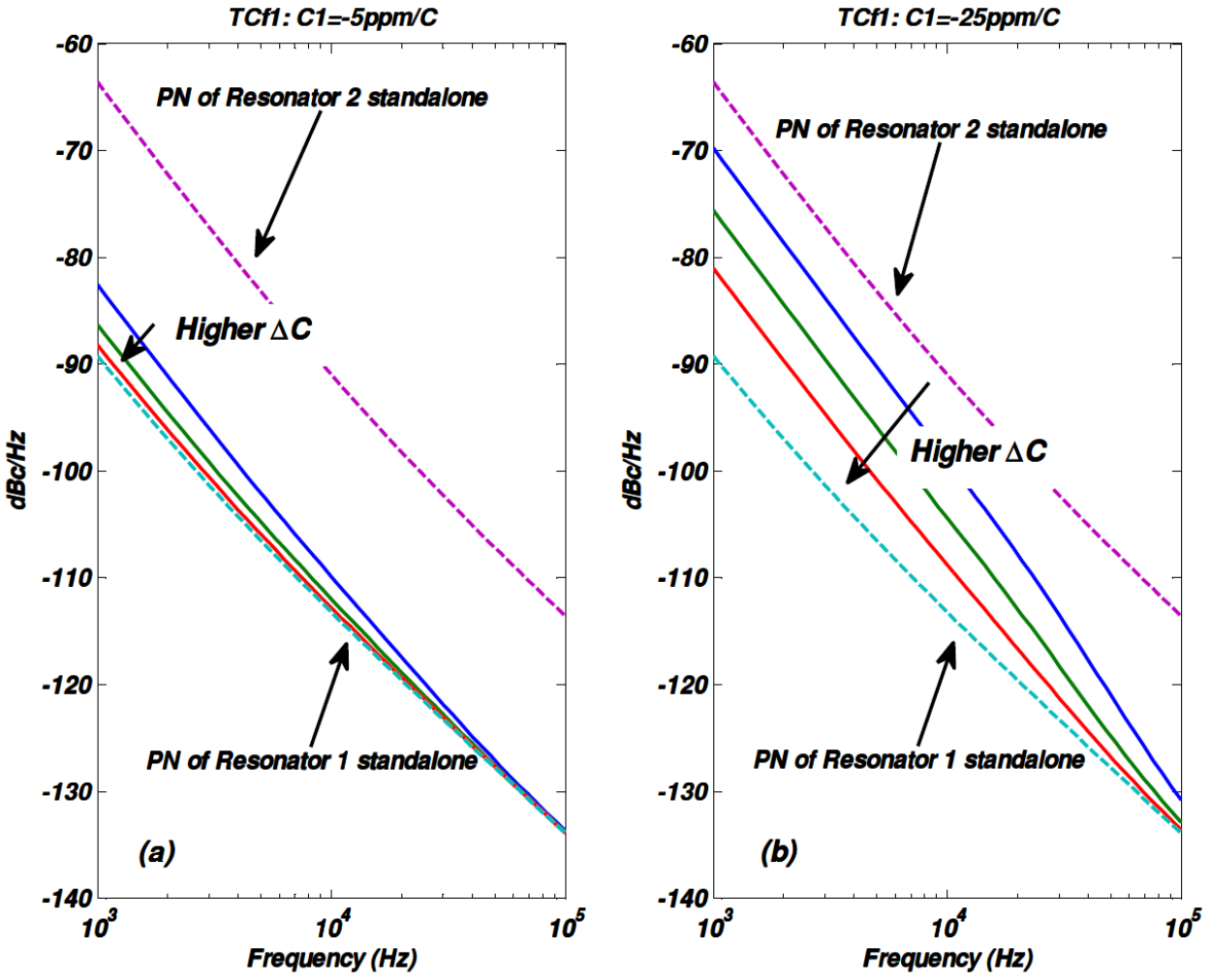


Figure 4-6. Phase noise generated at the output of Oscillator 1 (MEMS resonator-based) when Oscillator 2 (all CMOS-based) generates a much higher phase noise than Oscillator 1, for $|\Delta C|$ =50,100,200ppm/°C.

$|\Delta C|$. In this case, increasing $|\Delta C|$ reduces the phase noise effect of the CMOS-based oscillator at the output of the resonator-based oscillator.

4.5 Summary and Conclusion

The phase noise in a dual oscillator temperature compensation scheme was analyzed and simulated. It was shown that the low-frequency phase noise at the output of each oscillator is decreased when there is a higher difference between the TCf's of the oscillators. It was also shown that when the two oscillators generate different phase noise, the output phase noise can be reduced significantly by choosing optimized TCf values. Notably, a similar dual oscillator system employing a low phase noise MEMS resonator with low power and low cost but high phase noise all CMOS oscillator can be considered. The analysis presented here suggests that the impact of the all-CMOS low-cost noisy oscillator on the phase noise of a high-quality oscillator can be predicted and limited with increasing $|\Delta C|$. Such a hybrid oscillator system could lead to a lower cost and easier to implement system with marginally reduced phase noise performance but significant form factor, cost, and power consumption advantages.

Chapter 5 Simulating a Dual Loop PLL for Temperature compensation of MEMS based oscillators

5.1 Introduction

In recent years, the fabrication of micro-electro-mechanical systems (MEMS) has provided opportunities to reduce the form factor of various devices while maintaining excellent performance. This has allowed designers to enhance conventional systems and bring forth novel applications. Notably, it has been a while that MEMS accelerometers and temperature sensors are being used in smart phones and sensor networks. In addition, another MEMS device - the MEMS resonator – has started to replace Quartz crystals in timing applications. Such devices can be integrated with electronics to yield smaller, lower-cost timing solutions. However, a number of challenges associated with MEMS resonators still need to be addressed to fully realize this potential. These include their high insertion losses, limited quality factor, aging, accuracy, and temperature sensitivity. In this chapter, the application of the temperature compensation technique proposed and analyzed in Chapter 3 is studied for MEMS-based oscillators. For this purpose, the characteristics and specifications of an in-house built MEMS resonator are considered in designing and analyzing the temperature compensation scheme at circuit-level using simulations.

The system is described in the next section, and then the system and circuit level design are introduced, followed by presenting the simulations results.

5.2 System Description

5.2.1 MEMS Resonator

The system relies on the silicon carbide (SiC) clamped-clamped beam resonators presented in [19]. The resonator structure is a beam suspended above an actuation electrode, across a 100 nm gap, as shown Figure 5-1. Ignoring electrostatic effects, the resonant frequency, f_0, can be expressed as:

$$f_0 \approx 1.03 \frac{T_B}{L_B^2} \sqrt{\frac{E}{\rho}}, \tag{5.1}$$

where E is Young's modulus of the beam, and ρ is its density. L_B is the length of the beam, and T_B is its thickness. In this case, Young's modulus of SiC has a negative temperature coefficient and is the main contributor to the resonant frequency variation with temperature.

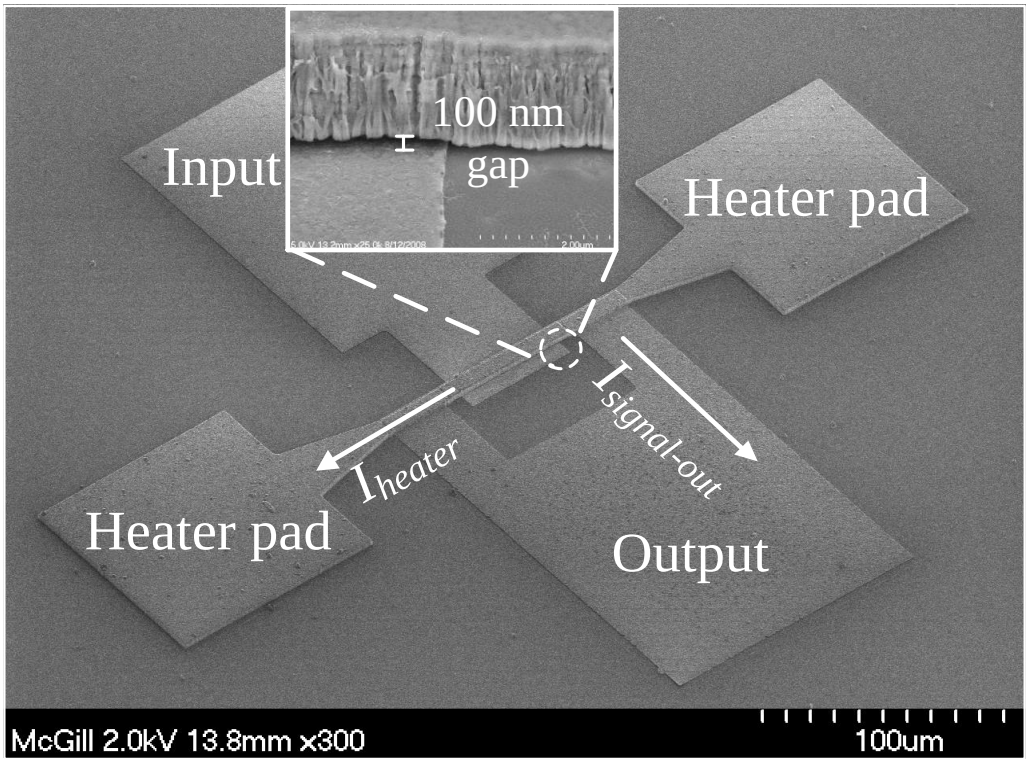


Figure 5-1. Micrograph of the resonator with a micro-heater.

As shown in Figure 5-1, a micro-heater lies on top of the beam so that a current, I_{heat}, can heat the resonator and tune its resonant frequency. Notably, the fabrication process of the resonator is CMOS-compatible [109], allowing it to be monolithically included with the circuitry presented here.

5.2.2 Temperature Compensation Scheme

The resonator can be heated to reduce its sensitivity to ambient temperature. This technique is similar to what is used to compensate crystal oscillators [15]. If two resonators with the same resonant frequency and different temperature coefficients of frequency (TCf) can be fabricated, a temperature change based on this difference can be detected. This effectively forms a temperature sensor that can keep the temperature (and thus the frequency) of the resonators fixed. A temperature sensor based on this technique was proposed in [116], where a mechanically compensated resonator having a small TCf was fabricated alongside an uncompensated resonator. This configuration was used in [26] to keep the temperature of the resonators fixed. The compensation scheme presented here is based on a similar concept and uses two resonators with similar resonant frequencies and different TCfs. However, unlike the mixer-based system proposed in [26], two integer dividers follow each resonator to allow greater system flexibility and eliminate the need to filter out undesired mixing terms. The system diagram of this dual-divider topology, which is similar to what presented in Chapter 3, is shown in Figure 5-2. The division ratio of the frequency dividers is selected such that at the operating temperature (T_0):

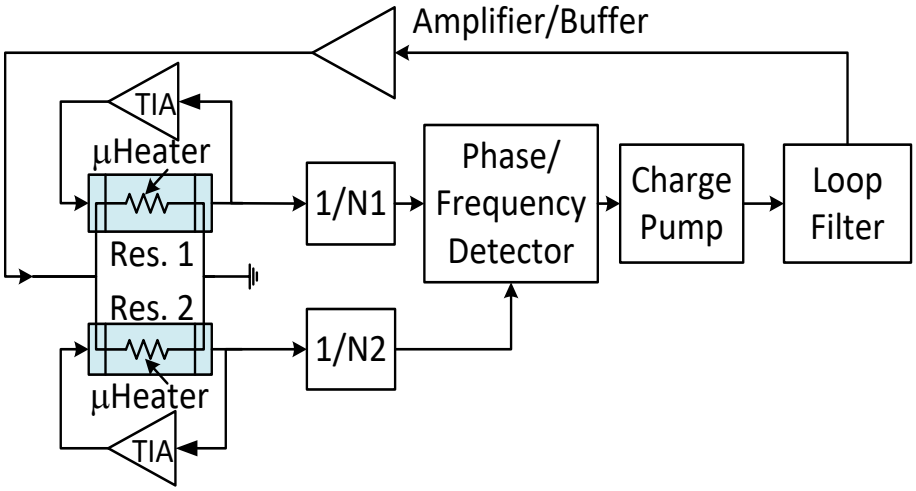


Figure 5-2. Block diagram of the compensation system.

$$\frac{f_{01}}{N_1} = \frac{f_{02}}{N_2}, \tag{5.2}$$

where f_{01} and f_{02} are the frequencies of each resonator at T_0.

As previously mentioned in Chapter 3, since both resonators have different TCfs, assuming the resonance frequency to temperature is a straight line [21], the relationship in (5.2) can only be valid for one temperature point as shown in Figure 5-3. Based on this fact, a phase/frequency detector (PFD) is used to monitor any frequency shifts due to temperature variations. The output of the PFD is conditioned by the charge pump (CP) and loop filter, and this signal is used to ensure that the temperature remains stable at the operating point, thus fixing the output frequency. The charge pump and loop filter control the loop dynamics, and the amplifier/buffer is necessary to drive the low impedance micro-heaters.

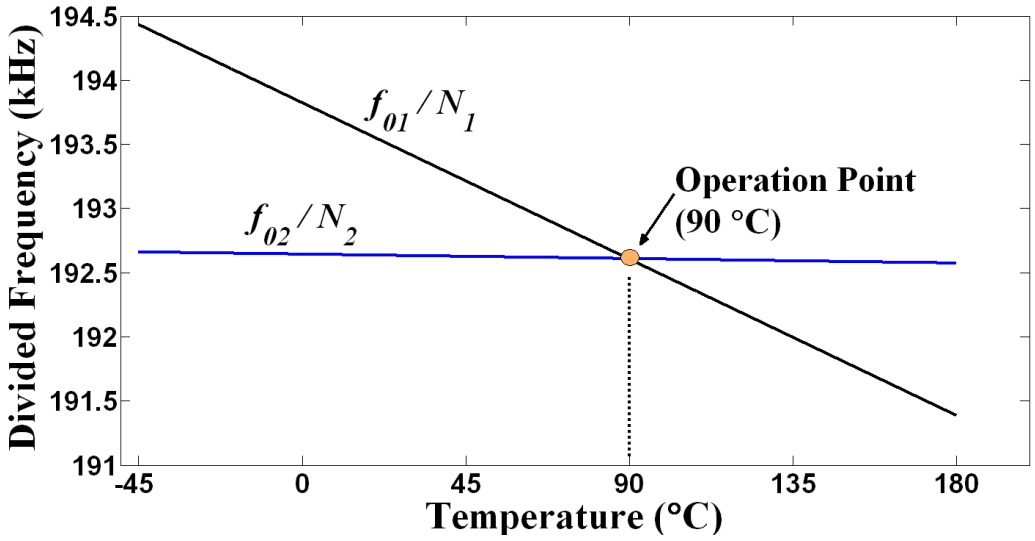


Figure 5-3. Frequencies at the outputs of both dividers vs. temperature.

The targeted operating temperature range is from -45 °C to 85 °C. Maximum heating current is used at -45 °C and zero at 85 °C. As the lowest current generated by the output buffer is greater than zero, the operating temperature is chosen to be slightly higher than the maximum ambient temperature (i.e. 90 °C, as shown in Figure 5-3).

5.3 System Analysis

5.3.1 Linear Approximation

As discussed in Chapter 3, a continuous-time linear approximation of the system can be developed to simplify the analysis, as shown in Figure 5-4. This approximation is valid for a loop bandwidth at least ten times smaller than the divided frequencies [110]. Heating is modeled as a thermal feedback system such that the heat loss is proportional to the temperature difference between the resonator and the ambient temperature. This quantity is subtracted from the electrical power injected into the heaters to yield the net heating power.

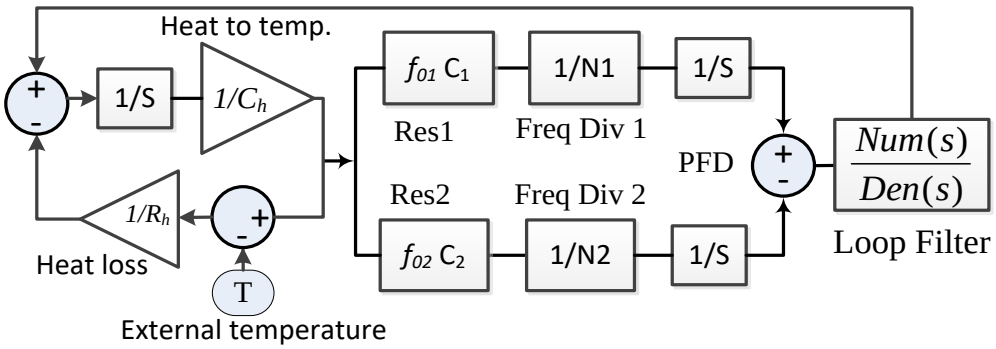


Figure 5-4. Linearized model of the proposed system.

An integrator (modeled by 1/s) converts power into energy while heat loss ($1/R_h$) and heat to temperature conversion ($1/C_h$) coefficients specify the dynamics of the heaters. In Figure 5-4, initial frequency of Oscillator 1 and Oscillator 2 are shown by f_{01} and f_{02} respectively and the TCf of each of the oscillators shown by C_1 and C_2. The divider following each oscillator has division ration of N1 and N2.

A temperature change from T_{osc0} to T_{osc} can cause a resonant frequency variation from f_0 to f. This can be expressed as [24]:

$$f(T_{osc}) = f_0\big(1 + C(T_{osc} - T_{osc0})\big), \tag{5.3}$$

where C is the TCf of the resonator. The phase variation of each resonator can thus be modeled as a linear gain followed by a divider and an integrator.

Considering the model of Figure 5-4, similar to what discussed in Chapter 3, the transfer function for the oscillator temperature variation in response to an ambient temperature change of T, assuming the initial ambient temperature $T_0 = 0$ and that both oscillators are at the same temperature, can be derived as:

$$H(s) \overset{\text{def}}{=} \frac{\Delta T_{osc}}{\Delta T}(s) = \frac{sDen(s)}{s^2 R_h C_h\, Den(s) + s\, Den(s) + K_o\, R_h Num(s)}\ , \tag{5.4}$$

where $K_o = \frac{f_{02}\, C2}{N_2} - \frac{f_{01}\, C1}{N_1} = \frac{f_{01}\, \Delta C}{N_1} = \frac{f_{02}\, \Delta C}{N_2}$, and $\Delta C = C_2 - C_1$. The term $(1/R_h C_h)$ represents the dominant pole of the heater and Num(s) and Den(s) are the numerator and denominator of the loop filter model $\frac{Num(s)}{Den(s)}$.

If $\frac{Num(s)}{Den(s)}$ as suggested in Chapter 3, is modeled as only a gain factor of K_d, as it is assumed that the frequency of the oscillators is linearly dependent on temperature, the frequency shift of Oscillator 1 in response to an ambient temperature variation can be written as:

$$H_{f1}(s) \stackrel{\text{def}}{=} \frac{\Delta f_1}{\Delta T}(s) = \frac{C_1 f_{01}\, \Delta T_{osc}}{\Delta T}(s) = C_1\, f_{01} H(s) = C_1 f_{01} \frac{s}{s^2 R_h C_h + s + K_0 R_h K_d} \quad , (5.5)$$

which presents the same dynamics as H(s) with the addition of the gain term $C_1 f_{01}$.

Thus, if the frequency shift of Oscillator 1 in response to an ambient temperature variation can be written in the form of a standard second order system, it can be shown as:

$$H_{f1}(s) = \frac{\frac{C_1 f_{01}}{R_h C_h}\, s}{s^2 + \frac{s}{R_h C_h} + \frac{K_d\, K_o}{C_h}} \stackrel{\text{def}}{=} K \frac{\omega_n^2\, s}{s^2 + 2\zeta \omega_n s + \omega_n^2} \,. \qquad (5.6)$$

As a result, the second order parameters of this system, namely the loop gain, K, the natural frequency, ω_n, and the damping factor, ζ, can be given by:

$$K = \frac{C_1 f_{01}}{K_0 K_d R_h} \,, \qquad \omega_n = \sqrt{\frac{K_o\, K_d}{C_h}} \,, \qquad \zeta = \frac{1}{2} \frac{1}{R_h} \sqrt{\frac{1}{K_o K_d C_h}} \,. \qquad (5.7)$$

5.3.1.1 Steady State Response of Frequency to Ambient Temperature

At this point, the steady-state value of the frequency when a change is applied to the ambient temperature can be studied.

Based on the analysis presented, the effect of a step ambient temperature changes with a step of value of T_s on the frequency of oscillator 1 can be shown. From the finite value theorem, it can be concluded that:

$$\Delta f_1(t \to \infty) = (f_1 - f_{01})(t \to \infty) = \lim_{s \to 0} sH_{f1}(s)\frac{T_s}{s} = 0. \qquad (5.8)$$

As such, the frequency change caused by a temperature step is zero.

The same way, it can be concluded that if the ambient temperature changes in the form of a ramp with the slope of $\dot{T}_r$, the frequency of Oscillator 1 is changed with the value shown below.

$$\Delta f_1(t \to \infty) = \lim_{s \to 0} sH(s)\frac{\dot{T}_r}{s^2} = C_1 f_{01}\frac{\dot{T}_r}{K_o K_d R_h} = K\dot{T}_r\,. \qquad (5.9)$$

Therefore, to be able to minimize the effect of a ramp change in the ambient temperature on the frequency of the oscillator, $\frac{C_1 f_{01}}{K_o K_d R_h}$ or the loop gain K can be minimized.

5.3.1.2 Instantaneous Change of Frequency Caused by Ambient Temperature Change

The conclusions shown in (5.8) and (5.9) are for the steady-state error of the temperature compensation system. However, it needs further considerations to calculate the instantaneous change of the frequency and its overshoot in response to the applied ambient temperature change.

If a step change with the value of T_s is applied to the ambient temperature, as suggested by (5.6), the change in the frequency of Oscillator 1 can be shown as:

$$\Delta f_1(s) = \frac{T_s}{s} K \frac{\omega_n^2\, s}{s^2 + 2\zeta\omega_n s + \omega_n^2} = T_s K \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}\ . \qquad (5.10)$$

Therefore, the maximum value of Δf_1 can be expressed as [117]:

$$\Delta f_{1Max} = T_s\, K\, \omega_n\, e^{\frac{-\zeta}{\sqrt{1-\zeta^2}} tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)}. \tag{5.11}$$

Hence, for the case of $\zeta = 1/\sqrt{2}$, the peak of the frequency deviation overshoot caused by a temperature step of T_s, can be quantified as:

$$\Delta f_{1Max} = T_s\, K\, \omega_n\, e^{\frac{-\pi}{4}} = T_s\, \frac{C_1 f_{01}}{R_h} \sqrt{\frac{1}{K_0 K_d C_h}}\, e^{\frac{-\pi}{4}} \;, \zeta = \frac{1}{\sqrt{2}}\,. \tag{5.12}$$

It is worth noting that (5.9) indicates that to minimize the steady-state error of the oscillator when the ambient temperature changes in a ramp format, the loop gain needs to be small. To minimize the overshoot and instantaneous error of the same system, as suggested by (5.12), the loop gain needs to be small as well.

A similar analysis can be performed to estimate the instantaneous frequency change of the system when a ramp of slope $\dot{T_r}$ Is applied to the ambient temperature.

In this situation, similar to (5.10), the change in the frequency of Oscillator 1 in response to a ramp with the slope of $\dot{T_r}$ in the ambient temperature can be shown as:

$$\Delta f_1(s) = \frac{\dot{T_r}}{s^2} K \frac{\omega_n^2\, s}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{\dot{T_r}}{s} K \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}\;. \tag{5.13}$$

Therefore, the maximum value of Δf_1 can be expressed as [117]:

$$\Delta f_{1Max} = \dot{T_r}\, K\; e^{\frac{-\zeta}{\sqrt{1-\zeta^2}}\pi}. \tag{5.14}$$

Therefore, for the case of $\zeta = 1/\sqrt{2}$, the peak of the frequency deviation overshoot caused by a temperature ramp with the slope of $\dot{T_r}$, can be quantified as:

$$\Delta f_{1Max} = \dot{T}_r \, K \; e^{-\pi} = \dot{T}_r \, \frac{C_1 f_{01}}{K_0 K_d R_h} \; e^{-\pi} \quad , \zeta = \frac{1}{\sqrt{2}} \, . \tag{5.15}$$

Equations (5.15) shows that when a ramp with the slope of $\dot{T}_r$ is applied to the ambient temperature, the peak error value of the frequency is affected by the loop gain. Therefore, selecting the right value for the loop gain ensures a sufficiently low instantaneous frequency deviation. For instance, for a system with the damping factor of $\zeta = \frac{1}{\sqrt{2}}$, if the maximum tolerable frequency deviation of a resonator is 5 kHz, to tolerate a ramp in the temperature change with the maximum expected slope of 100 °C/s, the loop gain should be less than 1157 $°C^{-1}$.

5.3.2 Circuit Implementation

The entire system was designed using a TSMC 0.18 µm CMOS technology. The MEMS oscillators (resonator and sustaining amplifier) were modeled using Verilog-A. The characteristics of these oscillators were based on experimental data obtained from previously fabricated MEMS oscillators [118] and are shown in Table 5-1. The lower TCf of Resonator 2 can be obtained by depositing an additional oxide layer [24], which can be done using plasma-enhanced chemical vapor deposition to maintain a CMOS-compatible thermal budget.

The compensation loop can operate in positive or negative polarities, depending on which resonator is connected to the positive or negative input of the phase/frequency detector (PFD). To ensure a stable negative feedback, the resonator with a higher TCf should be connected to the negative port of the PFD.

5.3.2.1 Divider, PFD, and CP

A multi-modulus divider, charge pump (CP), and phase/frequency detector were designed similarly to that described in [19]. The charge pump current, I_{CP}, was selected to achieve the desired gain with the loop filter.

5.3.2.2 Loop Filter

The loop filter was implemented using a simple RC filter, with values summarized in Table 5-1. Even though it was shown in Chapter 3 that the loop filter can be eliminated or be replaced by only a gain stage, here in this case, the loop filter is providing the necessary gain for the loop and higher pole-zero pair helping stability of the system. The trade-offs involved in choosing the loop bandwidth are system stability, maximum frequency overshoot, settling time of the loop, the chip area of the filter, and the ability to provide the heaters with a clean (spurious free) heating current. A low loop bandwidth results in

Table 5-1. Summary of system design values.

Resonator 1	f_{01} (MHz)	*8.282144*
	TCf1 (ppm/ ºC)	*-70*
	N_1	*43*
Resonator 2	f_{02} (MHz)	*8.089536*
	TCf2 (ppm/ ºC)	*-2*
	N_2	*42*
Loop Parameters	$I_{charge\text{-}pump}$ (µA)	*111*
	R_{lf} (kΩ)	*180*
	C_{lf} (pF)	*125*

a slower settling time and a larger chip area, but reduces spurs from the charge pump. In this work, a loop bandwidth of 15 kHz ($\omega_n = 10$ kHz) was chosen. This ensures a sufficiently small frequency overshoot for a range of temperature steps and ramps. The bandwidth requires the PFD inputs to be at least 150 kHz for stability reasons, which necessitates the use of division factors smaller than 53 for ~8 MHz resonators. The loop filter zero was selected to yield a phase margin of 65^o for system stability.

5.3.2.3 Output Buffer

The purpose of this buffer is to generate the large heating currents from the output voltage of the loop filter. The maximum heating current is needed during the lowest ambient temperature, which is -45 °C. The current needed to maintain the resonators at 90 °C at such low temperatures is ~60 mA. Such current levels can be generated using a simple common-drain amplifier. The buffer was designed to output a maximum current of 100 mA to the micro-heaters of the resonators which have impedances of ~4 Ω.

5.4 Simulation Results

5.4.1 System Level Simulation Results

The system is simulated in MATLAB Simulink using the design values of Table 5-1. Figure 5-6 shows the frequency deviation caused by a step-change in the ambient temperature. The frequency deviation will eventually settle to zero, but the frequency deviation shows an overshoot with different values depending on the TCf of each resonator.

Using another simulated example, Figure 5-5 shows the response of the same system to a set of ambient temperature ramps with slopes of 250, 500, 750, and 1000 °C/s. As predicted by (5.15), the frequency overshoot is

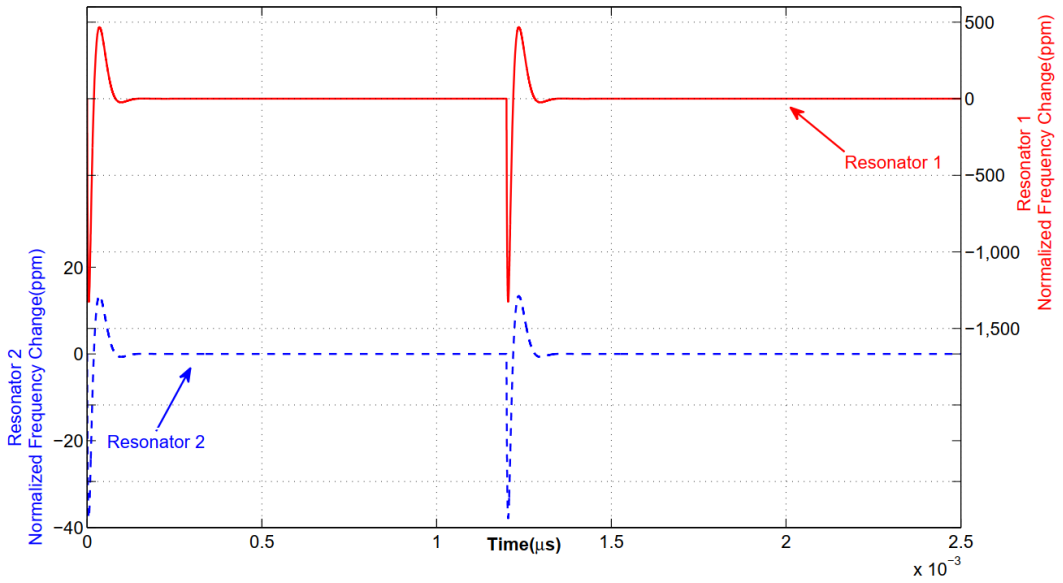


Figure 5-6. Step response of the system simulated in Simulink MATLAB.

proportional to the TCf of each resonator and the slope of the ramp, but remains quite small even for resonator 1 which has a much higher TCf than resonator 2.

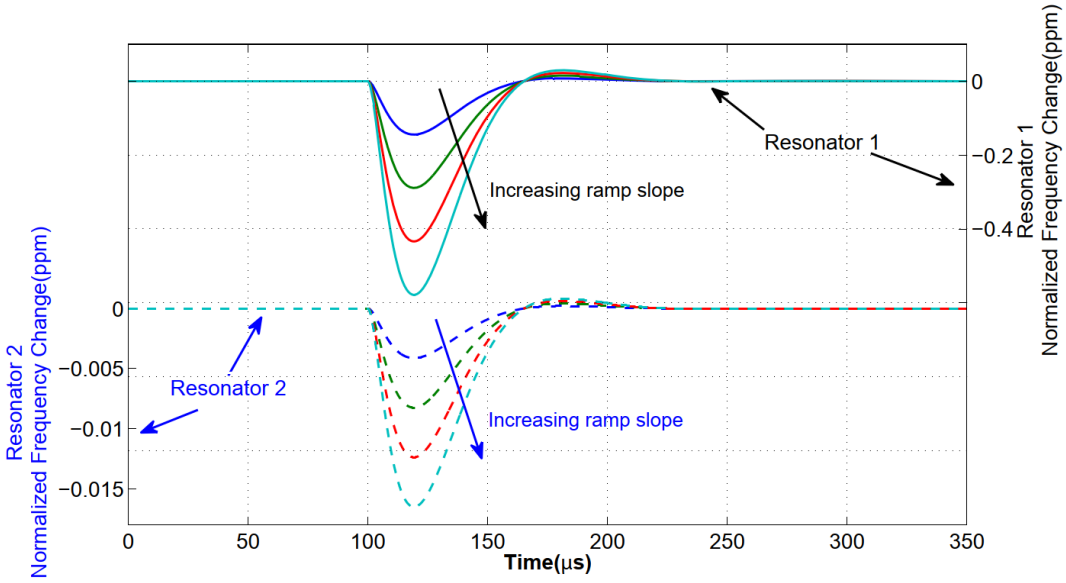


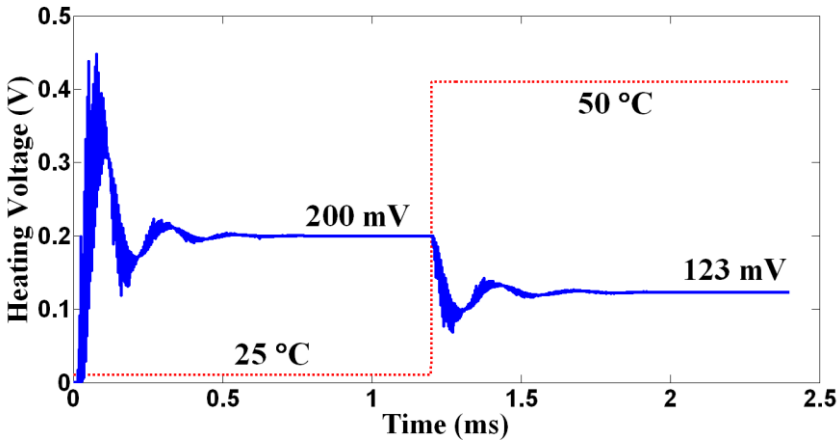
Figure 5-5. Resonators' frequency change caused by temperature ramps.

5.4.2 Circuit Level Simulation Results

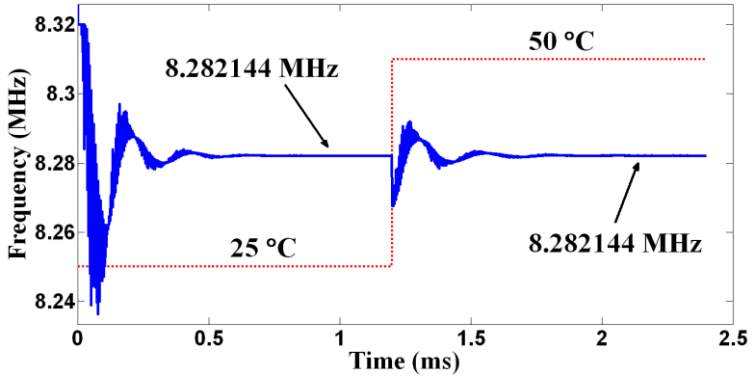
The simulation was performed at the circuit level to assess any non-idealities introduced into the system. The results below describe the output frequency response to both a step and a ramp in temperature.

5.4.2.1 Temperature Step Response

The response of the circuit implementation to a step is shown in Figure 5-7. The ambient temperature was maintained at 25 °C for 1.2 ms and then abruptly stepped up to 50 °C. The loop achieves initial lock by increasing the temperature of the resonator to 90 °C. This can be seen in Figure 5-7 a), which shows the transient response of the heater feedback control voltage. When the ambient temperature abruptly changes to 50 °C, the loop loses lock and responds by locking to a lower heating voltage. This brings the resonator temperature back to 90 °C, even after the ambient temperature increase. Hence, the resonant frequency is maintained at 8.282144 MHz, as shown in Figure 5-7 b), while in steady-state, the frequency variation is lower than $\pm$0.74 ppm. This is observed for any ambient temperature within the -45 °C to 85 °C range. This variation is due to the mismatch in the pull-up and pull-down currents of the charge pump, causing its output voltage to vary slightly even when the PFD inputs are at matched frequencies. As a result, the feedback voltage varies while in a steady state, introducing slight variations in the output frequency.



(a)



(b)

Figure 5-7. (a) Control voltage and (b) output frequency of resonator 1 in response to a step ambient temperature change.

5.4.2.2 Temperature Ramp

In addition, the system's response to different temperature ramps was simulated. As shown in Table 5-2, the frequency variation during a ramp is proportional to its slope. The frequency overshoot at the onset of a ramp also increases with the slope, similarly to that suggested by (5.15). The variation stabilizes at around ± 0.74 ppm for a ramp of 0.1 °C over 800 µs (125 °C/s). As such, for a temperature change of up to 125 °C/s, the compensation system can track the temperature change within ± 0.74 ppm of the frequency of resonator 1. Steeper slopes can be tracked by increasing the loop bandwidth.

The system's power consumption is dominated by the heaters and the buffer needed to drive their low impedances. At an ambient temperature of 25 °C, the power consumption is 181 mW, of which 1.2 mW is due to the control circuitry.

Table 5-2. Output frequency variation of resonator 1 vs. temperature ramps.

Ramp slope (°C/s)	Frequency Variation During the Ramp (ppm)	Frequency Overshoot (ppm)
25000	±42	≤86
2500	±10	≤15
1250	±4.8	≤7
250	±1.1	N/A*
125	±0.74	N/A*
62.5	±0.74	N/A*

*Smaller than the frequency variation during the ramp.

5.5 Summary and Conclusion

The temperature compensation system proposed was simulated at the system and circuit level for MEMS applications. It was shown that this system could stabilize the output frequency of a -70 ppm/°C MEMS resonator to within $\pm$0.74 ppm from -45 °C to 85 °C. This represents a significant improvement from the uncompensated variation of $\pm$4550 ppm over the same temperature span. The system can track temperature ramps as fast as 125 °C/s. The dual-divider architecture used here eliminates noise and non-linearities associated with the mixer-based architecture proposed in [26], resulting in additional system flexibility. This implementation was designed with on-chip integration of the whole system in MEMS or CMOS technology in mind.

Chapter 6 CMOS Implementation of a Dual Loop PLL for Temperature compensation of Silicon based oscillators

To verify the proposed compensation scheme, a system consisting of two CMOS oscillators and the necessary circuits for temperature compensation of the system is implemented. For this purpose, the system was implemented in an IBM 130nm standard CMOS technology (presently, Global Foundries has acquired IBM fabrication facilities). Implementation of the different blocks of the circuit is detailed in this section.

6.1 Circuit Implementation

An IBM 130nm standard CMOS technology is used to implement this system. Implementation of the different blocks of the circuit is detailed in this section.

6.1.1 Micro Heater Structure and Behavior

This work uses on-chip micro-heaters to construct the heat feedback loop. As suggested in [57], a pair of CMOS-based or MEMS-based oscillators, or one of each, can form a PLL loop. For MEMS-based oscillators, such as those presented in [19], a metal layer integrated on the beam resonator itself can serve as the heater. In this implementation, all-silicon oscillators are used. The metal layer M2 of a standard CMOS technology can form a serpentine micro-heater directly above the transistors that implement the oscillators. This way, the area under M2 is available to make the oscillator circuit while keeping the distance between the micro-heater and the circuit minimized. The system-level architecture proposed in this work is demonstrated using two CMOS current-starved oscillators having different TCfs in a PLL loop. This section discusses the structure of the implemented CMOS micro-heaters.

6.1.2 Heaters of the Ring Oscillator

A serpentine metal structure fabricated in layer M2 of the chosen IBM 130 nm CMOS process is used to heat the CMOS ring oscillators. The heater structure is designed by calculating the total heater resistance based on the sheet resistance of M2. The minimum dimension limits and maximum power limits of the M2 layer were considered in designing the heater. The layout view of the heater is shown in Figure 6-1.

To show how the micro-heater is placed in respect to the oscillator, Figure 6-2 shows the oscillator made out of the M1 metal layer and the below layers together with the micro-heater fabricated out of the M2 metal layer. The heater structure was verified by finite element electro-thermal simulation using COMSOL Multiphysics. Using this simulator, as illustrated in Figure 6-2, the effect of the electric power applied to the micro-heater on the temperature generated in the die area surrounding it can be observed.

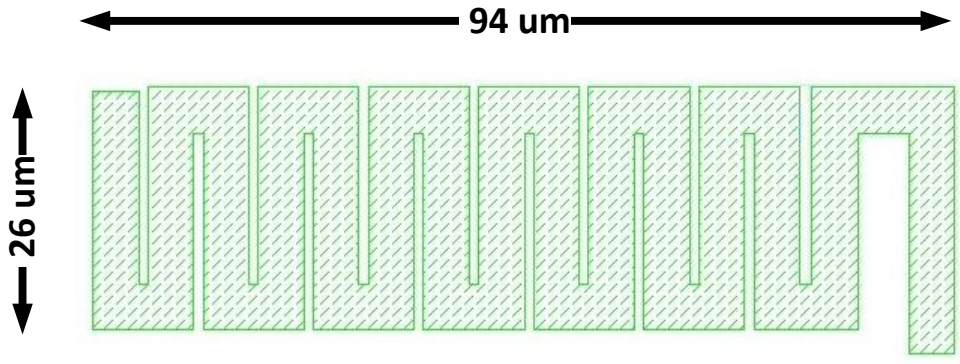


Figure 6-1 Layout mask of the M2 metal layer the micro-heater is built from.

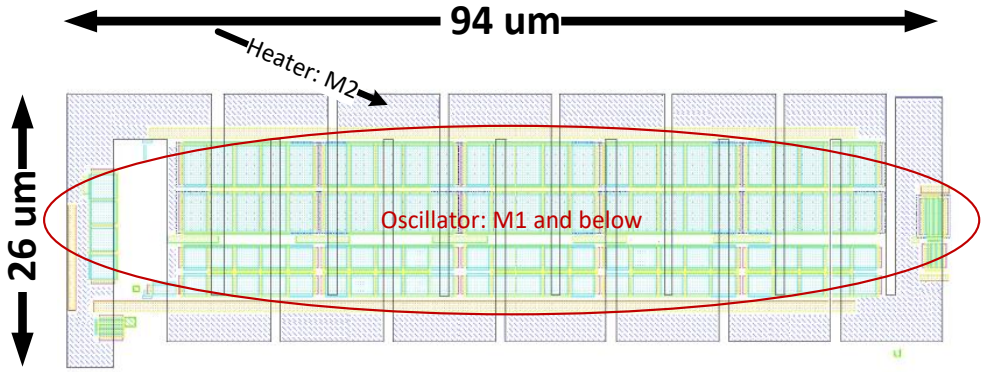


Figure 6-3 The layout of the oscillator and the micro-heater on top of it.

A steady-state thermal simulation is performed using the full dimensions of the die. This simulation estimates the temperature distribution caused by the DC current flowing through the heater. As shown in Figure 6-4, according to the technological parameters of the standard 130 nm CMOS bulk technology used in this work, a 20°C oscillator temperature change requires a current of 150 mA through the serpentine heater, which is a significant amount of electrical power for a moderate temperature change. The system using this heater design is intended as a proof of concept, and alternative methods to

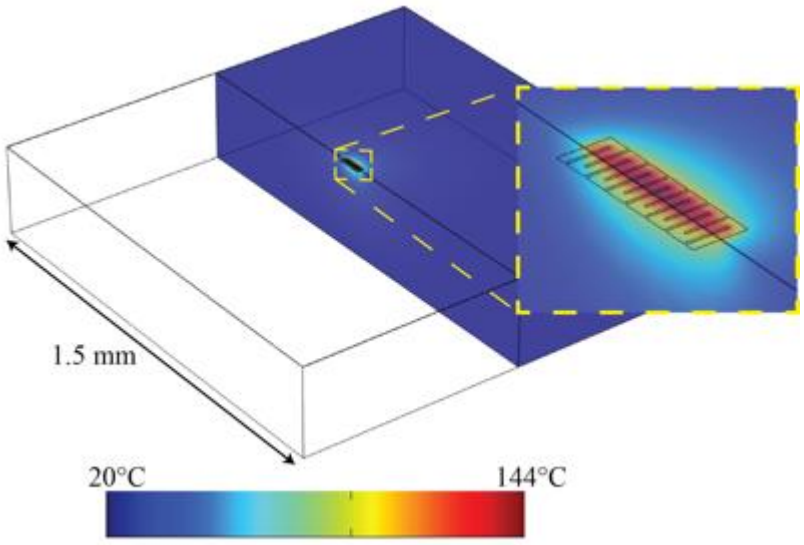


Figure 6-2 COMSOL Multiphysics is used to obtain an estimation of the micro-heater behavior on the die.

increase the system's power efficiency are needed to render its application viable. Several efficient on-chip heaters in MEMS or other non-standard IC processes have been proposed [119-121]. Still, even a standard CMOS process with a good thermal insulation layer (e.g., SOI) would provide higher efficiency. To show an example of how the power efficiency can be improved, Figure 6-4 shows a COMSOL simulation comparison between the non-SOI (silicon-on-insulator) technology of the current work and a possible design in an SOI technology. The SOI technology assumed in this simulation is similar to a standard 28nm SOI technology with the thicknesses of the functional Si equal to 2µm, buried oxide of a thickness of 4µm, and Si bulk under the buried oxide

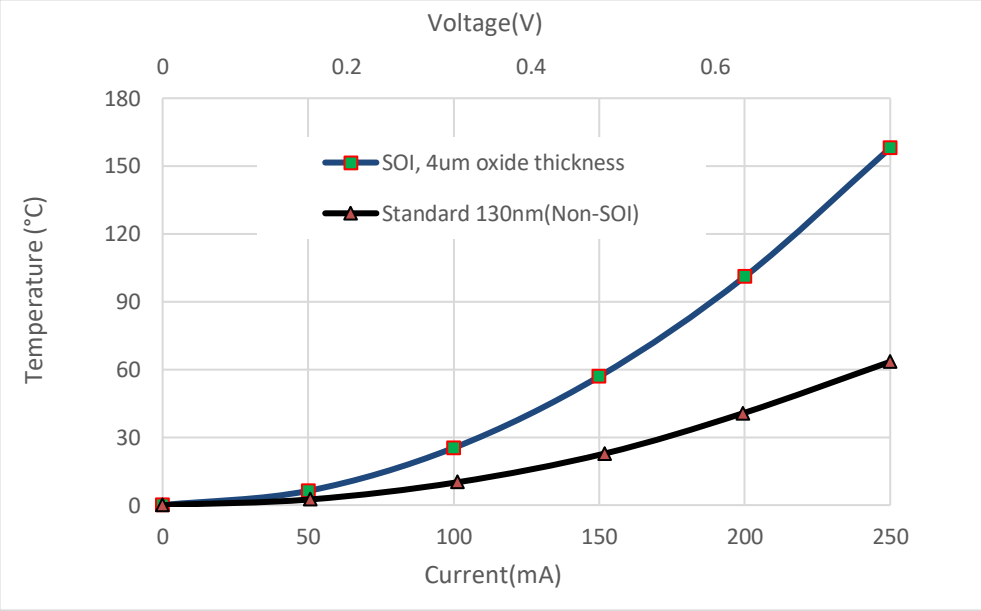


Figure 6-4 Thermal simulation results showing temperature change vs. current biasing of the micro-heater for both standard bulk and SOI technology.

of 300μm thick. In an SOI technology, the insulator under the substrate insulates heat, leading to better temperature conservation.

As Figure 6-4 shows, a 150 mA current only changes the temperature in the current non-SOI-based chip by about 20°C, but this same current can change the temperature in a similar hypothetical SOI technology by 55°C, which is an improvement of 175%.

6.1.3 CMOS TCO

The TCO (temperature-controlled oscillator) is implemented using a current-starved ring oscillator configuration. Ring oscillators occupy a small area, which reduces the required size of the heaters and, therefore, the power requirements of the TCO. In addition, the oscillation frequency can conveniently be tuned through the current starving mechanism, which can be used to counteract process variations. An added benefit of using a current-starved structure in this work is the ability to control current to alter the value and even sign of an oscillator's TCf.

The oscillation frequency of the ring oscillators is chosen to be 10 MHz to provide a situation comparable to crystals or MEMS-based oscillators. A five-stage ring oscillator is selected, with the schematic shown in Figure 6-5.

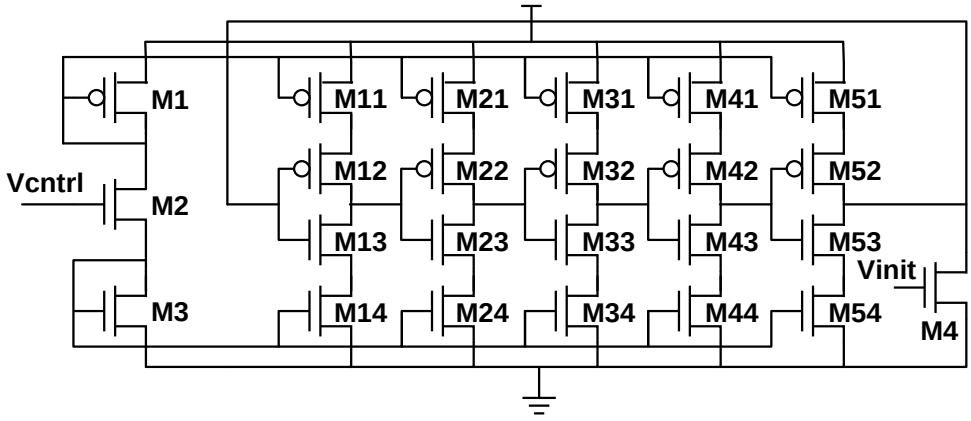


Figure 6-5 Current-starved CMOS ring oscillator.

Transistors M1 to M3 are used for biasing and mirror the current to each ring oscillator stage. The reference current can be tuned by varying the gate voltage of M2 (V_{cntrl}). Transistor M4 is connected to the feedback loop to ensure the oscillator starts up when the gate voltage V_{init} is excited. Figure 6-6 plots the oscillation frequency with respect to V_{cntrl} for this circuit at a temperature of 87°C. It shows that this circuit can achieve a tuning range from 0.3 MHz to 11 MHz.

The total area of the current-starved ring oscillator is less than 20 µm × 100 µm, and a micro-heater slightly larger is implemented above it.

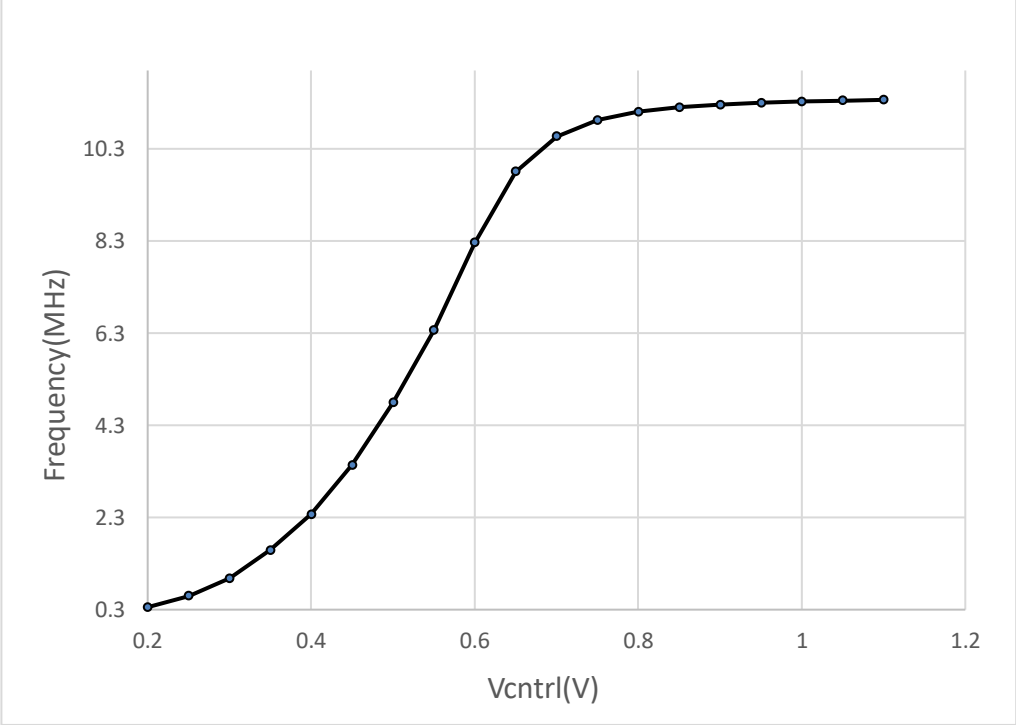


Figure 6-6 Frequency of oscillation vs. starvation control voltages at a temperature of 87°C.

Figure 6-7 shows the simulated effect of temperature on oscillation frequency at different values of V_{cntrl}. This reveals an interesting property of the current-starved ring oscillator: as the control voltage increases (i.e. more current provided to each stage), the TCf of the oscillator varies from positive to negative. Therefore, this structure can implement oscillators with either negative, positive or close to zero TCf by adjusting the control voltage. Hence, different TCf oscillators can be implemented to provide the feedback required.

6.1.3.1 Behavior of CMOS Oscillators over Temperature

To understand how the TCf of the oscillator changes with temperature, considering the behavior of the transistors used in the oscillators can be insightful. When the current going through the oscillator transistors is low enough, the transistors are biased in the sub-threshold region and in this region, increasing the temperature can add to the mobility of the electrons and

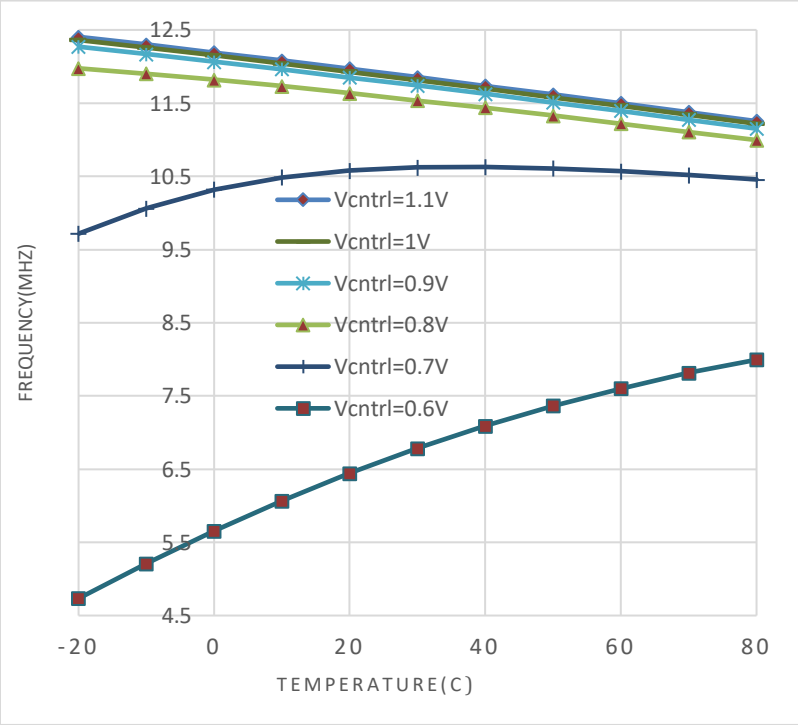


Figure 6-7 Simulated effect of temperature on the oscillation frequency at different control voltages (Vcntrl).

increase the oscillation frequency. Conversely, when Vcntrl is high, the transistors are biased above their threshold voltage. An increasing temperature increases electron collisions, reduces the speed of the transistors, and decreases the oscillation frequency.

As shown in Figure 6-7, at some biasing points, it is possible that the frequency versus temperature curves are not monotonic. Therefore, the frequency versus temperature of the two oscillators might cross each other at two frequency-versus-temperature points. Hence, attention should be paid to avoid non-monotonic curves during the design process. However, if the curves are still non-monotonic, there are ways to make sure they do not cross each other. For instance, if the slope of one curve is always smaller than the other one, the curves will not cross each other more than once. This is because if one curve has a smaller slope than the other one and crosses it at one point, to be able to become equal to that curve again, it has to have a higher slope than the other one at some point. Consequently, as shown in Figure 6-8, making sure the oscillators have slopes (TCfs) that are very different will guarantee that the curves cross each other only once. One way to obtain this is to use two oscillators in the loop, with one of them being a temperature-compensated one and the other one not.

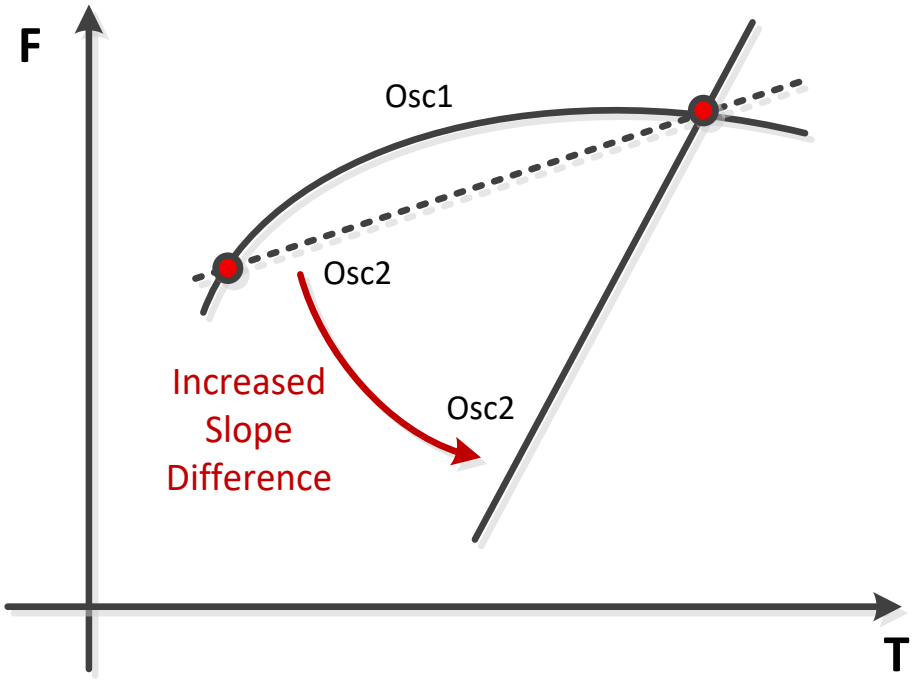


Figure 6-8. If the slope of the frequency to temperature curves of the two oscillators are pushed away from each other, the possibility that they can meet each other at two different points can be removed.

6.1.4 Frequency Divider, PFD, CP and Loop Filter

6.1.4.1 Frequency Divider

A frequency divider follows each oscillator implemented using an 8-bit counter. The counter counts down from a pre-set value in each cycle, and this pre-set value is fed into the chip via a shift register. The shift register is used to provide a serial to parallel functionality. It uses only one input pin on the chip to send in the initial values of the counter serially. The counter and the shift register are shown in Figure 6-9.

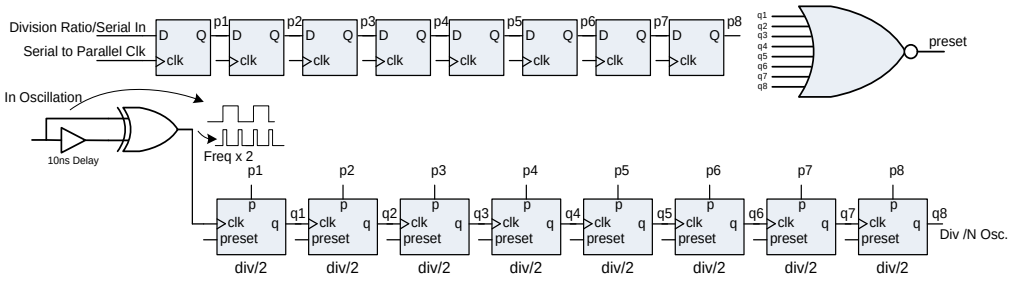


Figure 6-9 Frequency divider and the serial to parallel shift register to receive the division ratio serially.

6.1.4.2 Phase Frequency Detector

The PFD used in the design is shown in Figure 6-10. It is based on D flip-flops, and the outputs represent the time difference between the rising edges of the two frequency divider outputs. A delay is introduced into the reset signal path to eliminate the dead zone associated with this PFD. An output stage (labeled as the control signal generator in Figure 6-10 is used to convert the up and down signals generated by the PFD into eight separate control signals to mitigate non-idealities in the charge pump [122].

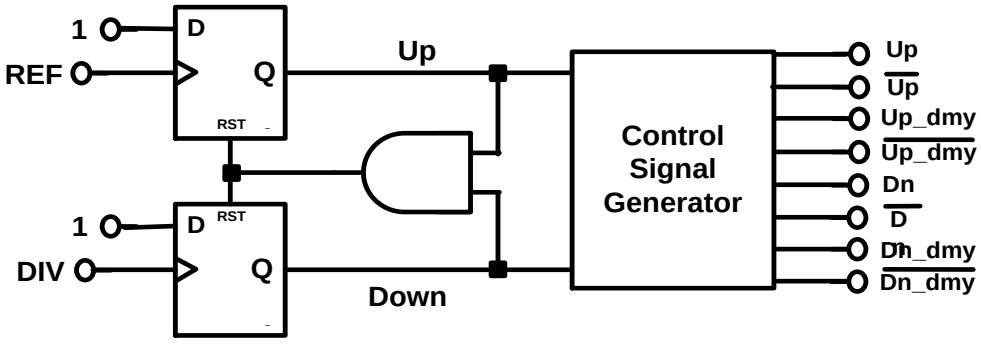


Figure 6-10 Phase Frequency detector with control signal generator.

6.1.4.3 Charge Pump

The schematic of the charge pump is shown in Figure 6-11. A dummy branch (M7-M10) is added to preserve the voltages at the drains of M1 and M2, thus avoiding current spiking due to charge sharing. To eliminate changes in these voltages during transitions, the eight control signals from the PFD are timed such that there is a slight overlap between the time when the output branch turns on and the time when the dummy branch turns off vice-versa. A simple differential amplifier in a unity-gain configuration is used to ensure that the voltage on the dummy branch matches that of the charge pump output [123].

The eight PFD control signals are needed to allow the use of complementary switches in the charge pump, which considerably reduces charge injection and charge feed-through errors, provided careful layout is observed to match the transistors. This reduces the ripples on the control line, and hence the level of spurs at the output of the VCO.

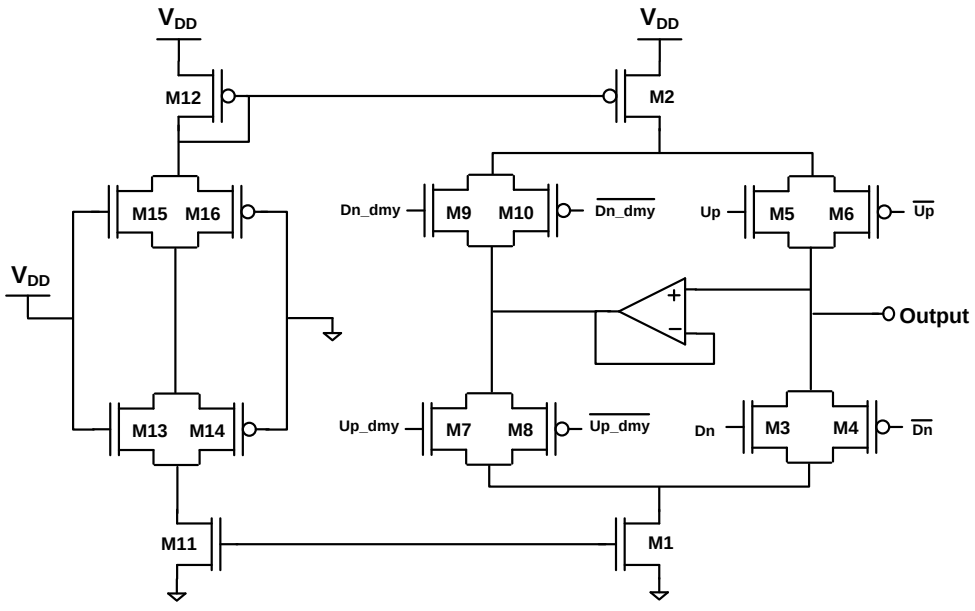


Figure 6-11 Charge pump used in the circuit implementation.

Biasing is set by M11-M16, where M13-M16 are used to reduce mismatches that result from channel length modulation when mirroring currents to the active branches of the charge pump. The charge pump is designed to provide a 50 μA current for optimal loop characteristics.

6.1.4.4 Loop Filter

An off-chip loop filter is used in this design to provide means of modifying the filter based on the location of the poles and zeros of the heater. As mentioned previously, if the second-order effects of the heating system are taken into account, the micro-heater adds a pole close to the origin and a pole and zero at higher frequencies. Therefore, as Figure 6-12 shows, the loop filter can be reduced to only a resistor able to convert the current of the charge pump to a voltage. In measurements, a 70 kΩ resistor was shown to have the best effect in this circuit.

6.1.4.5 Micro-heater Filtering Effect and Circuit Simplifications

The previously described filtering effect of the micro-heater enables system simplification by completely replacing the loop filter. In addition, it is also possible to completely eliminate the charge pump since there is no need to

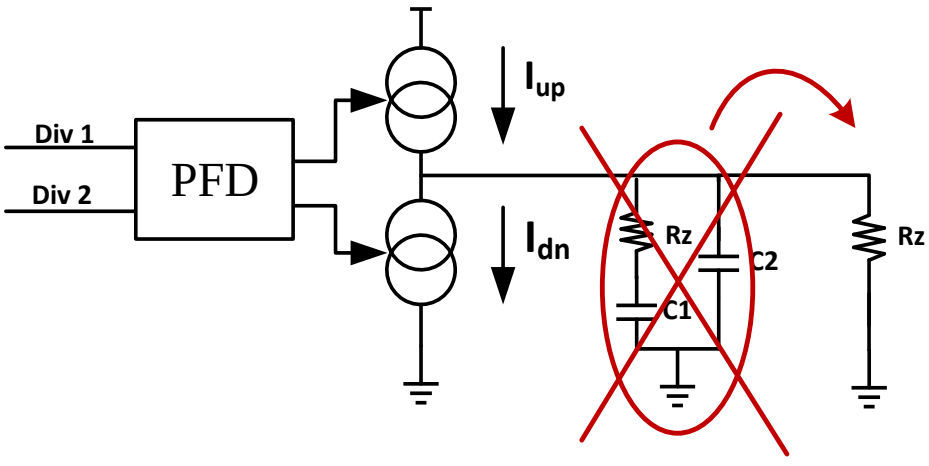


Figure 6-12 The loop filter that can be eliminated in this system.

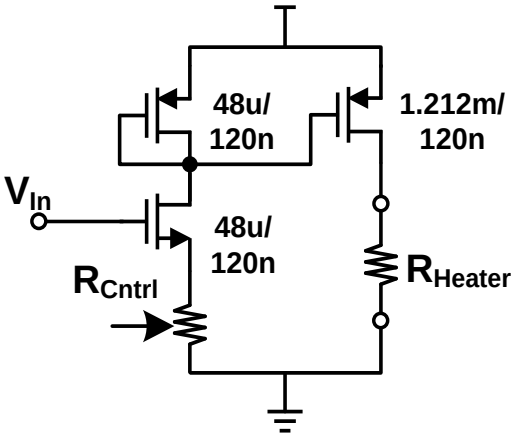


Figure 6-13. High power buffers for the heater indicating the W/L ratios of all transistors.

resort to a current-to-voltage transfer function to introduce a pole at 0 Hz. This is because the heating system creates such a pole in addition to a pole and zero at higher frequencies. This avoids issues associated with using charge pumps like charge sharing, charge injection, and mismatch.

6.1.5 Output Buffer for Heaters

A current buffer is needed to drive the power required by the micro-heaters. This buffer, shown in Figure 6-13, converts the input voltage to an output current through current mirroring with a large ratio of about 25. The output transistor is sized really huge with a width of 1.2mm to handle the high current required for driving the micro-heater. To allow for external control of the maximum current during characterization, a variable off-chip resistor R_{Cntrl} is added to the mirroring branch of the buffer.

Special attention must be given to the layout of this buffer due to its high current capacity. The outputs of these buffers are taken off-chip to measure the heater current. Two bonding pads and bond wires are used for each buffer to reduce the bond wire resistance and allow the heater's current, which can be more than 150mA, gets divided into two current paths.

The simulation results presented in Figure 6-4 showed that in the standard CMOS technology used here, a current of ~150 mA through the designed heater causes a 20°C local temperature increase at the oscillators. Considering this current as the maximum available current, the compensation range is limited to 20°C. This range is sufficient for proof of concept, while designing a more efficient integrated heater to increase the compensation range is the subject of ongoing research. For example, the heating efficiency and compensation range may be improved by using SOI technology to reduce the substrate heat loss.

6.2 Measurement Results

The circuit was implemented in parts of a 1.5 mm × 1.5 mm die in GF 130 nm technology. The actual area of the chip taken by this circuit, including the pads, is less than 0.4 mm2. A micrograph of the fabricated chip is shown in Figure 6-14. The active area of the whole system with two oscillators and heaters occupies ~0.23 mm2. The design contains two TCOs (consisting of two current-starved ring oscillators and their heaters and buffers), a frequency divider, PFD, charge pump, and an off-chip resistor to convert the charge pump current to the voltage without other possible components in the loop filter. In this design, a charge pump is included to provide the option to have an extra pole at 0 Hz by directing the current of the charge pump to a capacitor in case it is needed to obtain optimized loop characteristics. However, as shown in the

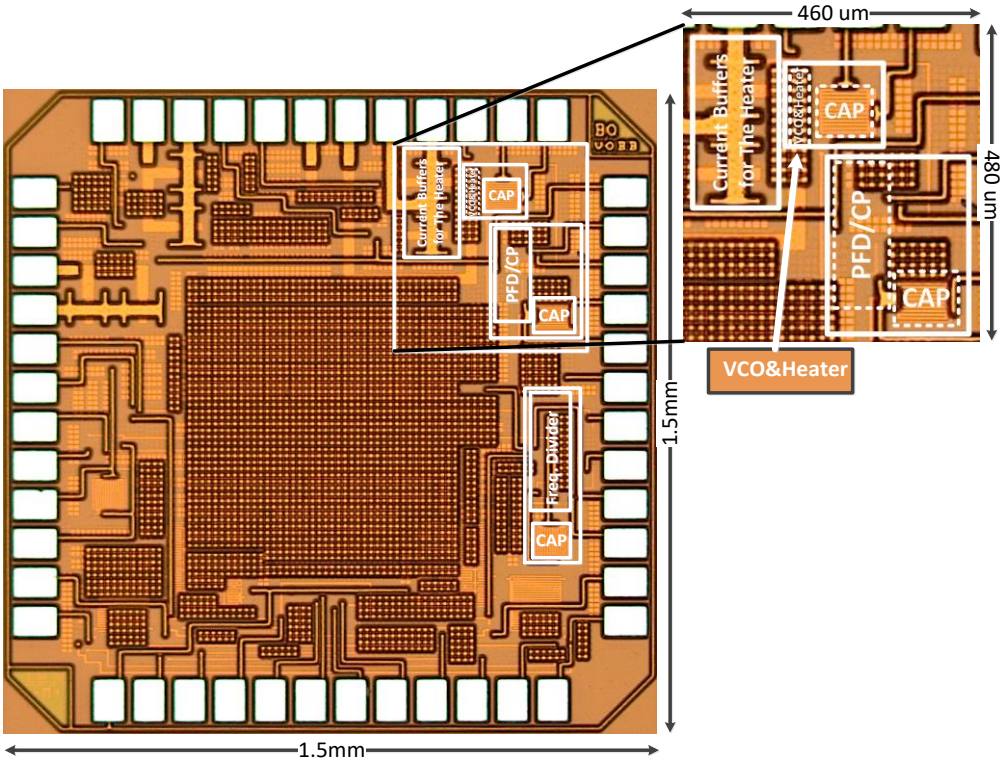


Figure 6-14. Die micrograph with active area outlined.

measurement setup, this optional capability is not used, and the actual charge pump is only passing current into a resistor and acting as a gain stage.

To test the circuit, a PCB was designed with the necessary biasing voltage controllers and the input and outputs required to set up the test, including the divider ratio key in the mechanism. Figure 6-15 shows the PCB designed for this purpose. In this PCB, the possibility of having a MEMS-based resonator alongside a CMOS-only oscillator has been provided for future works.

6.2.1 CMOS Current-Starved Ring Oscillator

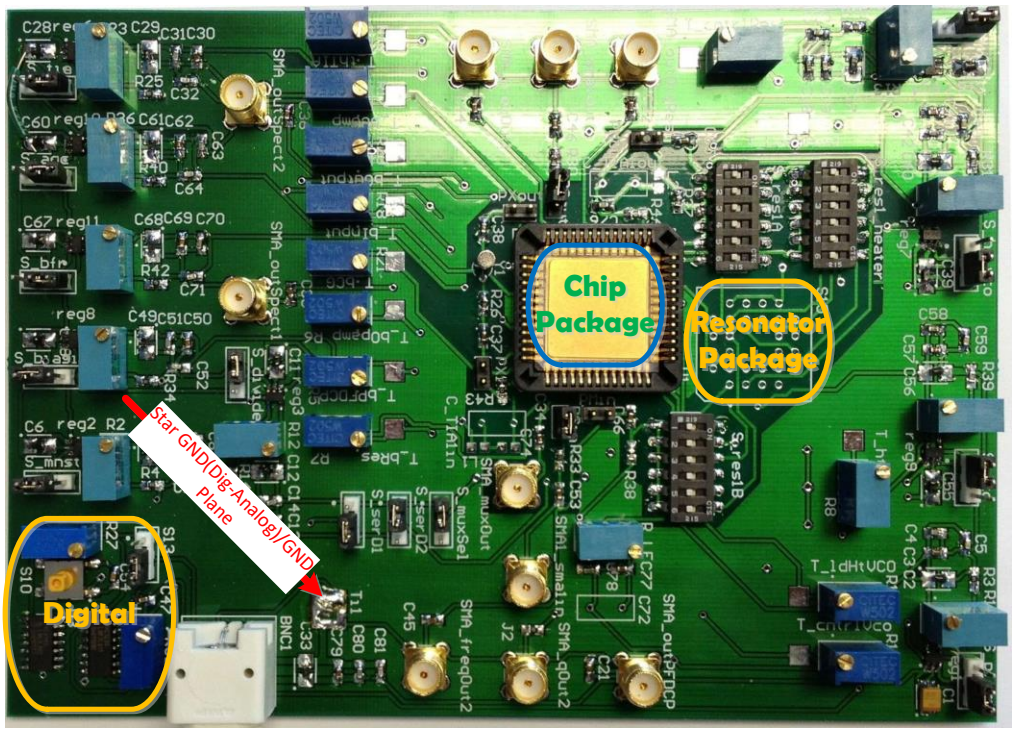


Figure 6-15. The PCB designed to test the compensation scheme using the fabricated chip.

As shown in the simulation result depicted in Figure 6-7, the TCf of the CMOS current-starved ring oscillators varies with the amount of current going through them. The fabricated oscillator was examined at two operating temperatures 20°C apart from each other to characterize this behavior. The low temperature was set to be 34°C, and the high temperature was set to be 54°C. Figure 6-16 shows the oscillator's frequency in each of these two cases, along with the corresponding TCf of the oscillator calculated from the difference between these two cases. These measurements confirm that the TCf of the oscillator can be tuned to a positive or negative value depending on the degree of oscillator current starving. As shown in Figure 6-16, the TCf is

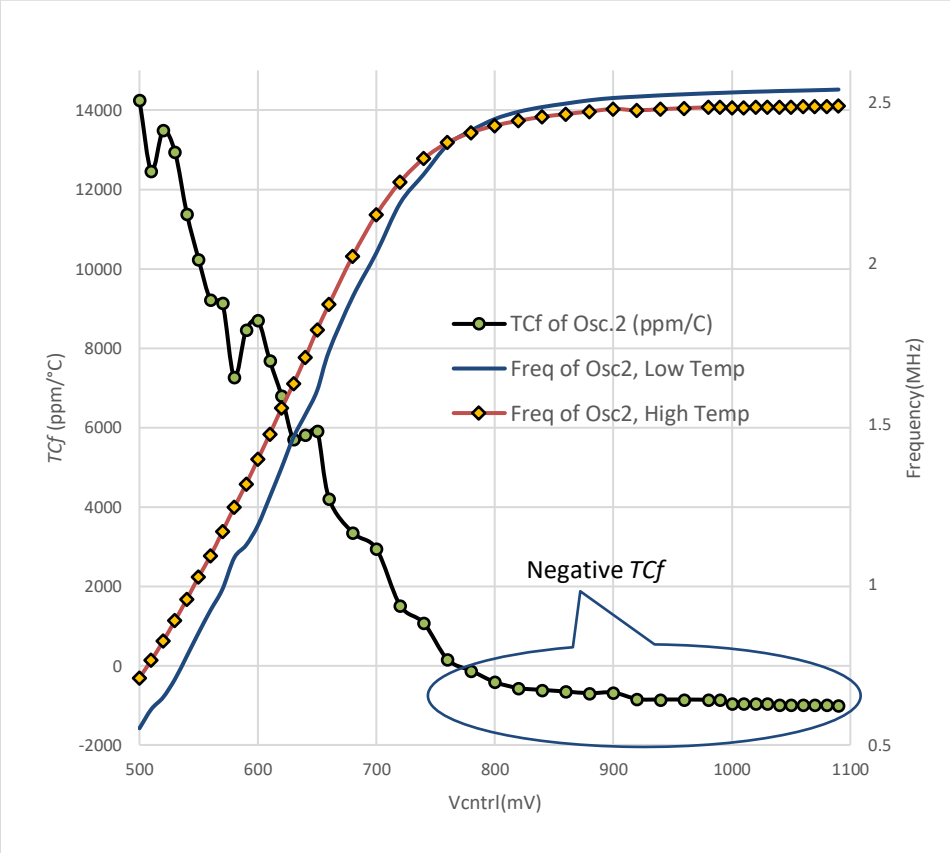


Figure 6-16. Frequency of oscillation vs. current starving control voltages.

positive when the oscillator is more starved (i.e. low Vcntrl) and it decreases as more current is allowed to feed the oscillators (i.e., higher Vcntrl). At a certain point, the TCf becomes negative, matching the observations from the simulation. This phenomenon provides the capability to tune the current-starved ring oscillator to model a range of oscillators with different TCfs.

6.2.2 Closed-loop Temperature Compensated Results

The two oscillators with two different TCfs of 6525 ppm/°C and -433 ppm/°C are configured to form the thermal feedback PLL loop. To maximize versatility, each oscillator operates with its own micro-heater. However, as explained in section II, using two different heaters on the oscillators limits the temperature compensation capability of the system. In addition, the voltage bias generation circuits can affect the oscillation frequency of the current-starved ring oscillators and degrade performance. For example, voltage regulators can have a TCf of about 10 ppm/°C which can be the lower limit of overall temperature compensation unless a careful design of voltage biasing circuits is used to cancel out this limit in the two different oscillators and reduce their impact on the total performance of the compensation system.

6.2.3 Heater power and its limiting effect on the range of temperature compensation

The efficiency of the heaters is a limiting factor in this implementation. To ensure the heaters stay in a linear region of operation to maintain stable closed-loop behavior, a maximum current of about 100 mA is set for each of the heaters. The current to temperature conversion starts to become non-linear above this current value. The system is placed on a test PCB in a heat chamber that can vary the ambient temperature of the test environment. Since the heat chamber only has the ability of heating up, the test temperature is set to be higher than the normal room temperature of 25°C to be able to cool down and heat up the chamber temperature in a timely manner. It is possible to obtain functionality at different temperature ranges like the normal room temperature by shifting up or down the temperature; the two oscillators lock to each other. This can be done by adjusting the division ratio of each oscillator. Figure 6-17 shows how the behavior of the loop changes as the ambient temperature is varied. The figure presents the divided down frequency of each oscillator and the current through one of the heaters. Since

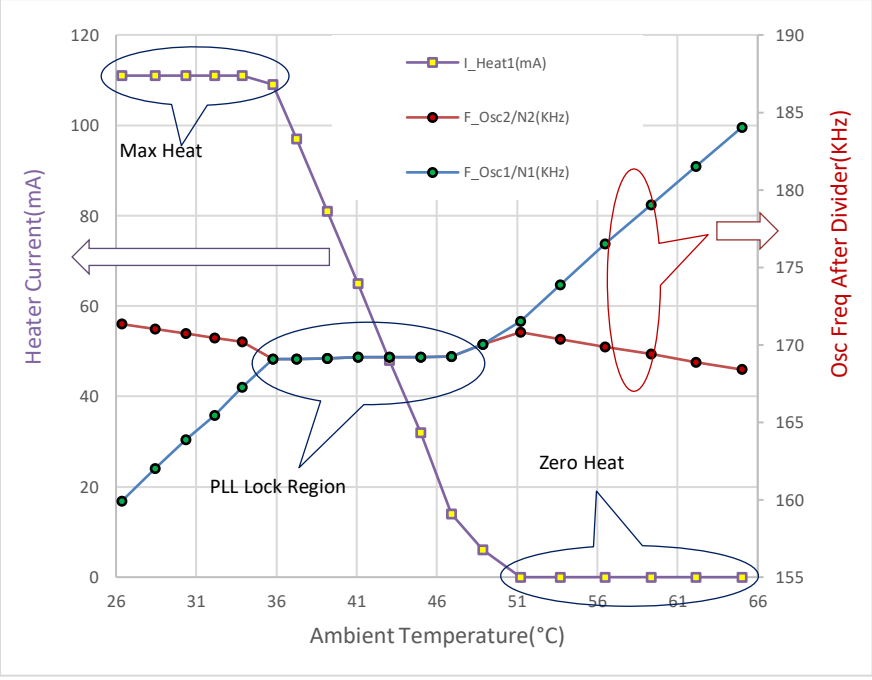


Figure 6-17. How the heater current limits PLL lock region current.

both heaters are controlled by the same signal generated by the PFD/CP and the loop filter resistor, the current in each heater shows the same trend. It can be seen that when the ambient temperature is low, the heater is at its maximum power output. However, the generated temperature is then insufficient to bring both divided oscillation frequencies together and lock the loop. As ambient temperature increases, there is a point where the PLL manages to lock the two oscillators to each other. In this region, the ambient temperature rise causes the heaters to pump less power to the oscillators to keep their frequency stable. This locked state lasts until the heaters reach the zero-current stage, making the loop lose its lock. This demonstrates that heaters with more heat power or slower heat dissipation by the oscillators to the substrate and environment are potential solutions to achieve a greater temperature compensation range.

6.2.4 Temperature compensation capability of the system

The measurements shown in Figure 6-17 are conducted to show how the heater current can limit the compensation range. As it shows, when the ambient temperature is too low, the micro-heater provides the maximum heat it can provide. Still, it is not enough to close the PLL loop, and the two oscillators oscillate at different frequencies with their intrinsic TCf. As the ambient temperature keeps increasing, at one point, the micro-heater will be able to provide enough heat to close the PLL loop. From that point on, as the ambient temperature increases, the heat provided by the heater is reduced to compensate for the ambient temperature effect on the die area. Therefore, the temperature of the die area will have minimal variations. As the ambient temperature increases more, the heater keeps reducing the heat it provides to the system until it is turned off. The loop will be open again from this point on, and the oscillators oscillate at different frequencies with their intrinsic TCf. The range between these two points where the PLL loop is locked through the

feedback provided by the heater is the temperature area that compensation is possible.

To find out how much the ambient temperature is compensated on the die area, the voltage biasing of the compensation circuits is optimized. First, the frequency versus temperature curve of each of the two oscillators is plotted when they are not compensated. This measurement is then compared with the frequency versus temperature curve of one of the oscillators when its temperature is compensated. Figure 6-18 shows these measurement results and depicts the temperature compensation capability of the system within its locked region. In this experiment, as suggested in 3.4 , to reduce the effect of two micro-heaters on the overall compensation capability of the system and also to reduce the effect of each oscillator on the phase noise of the other one

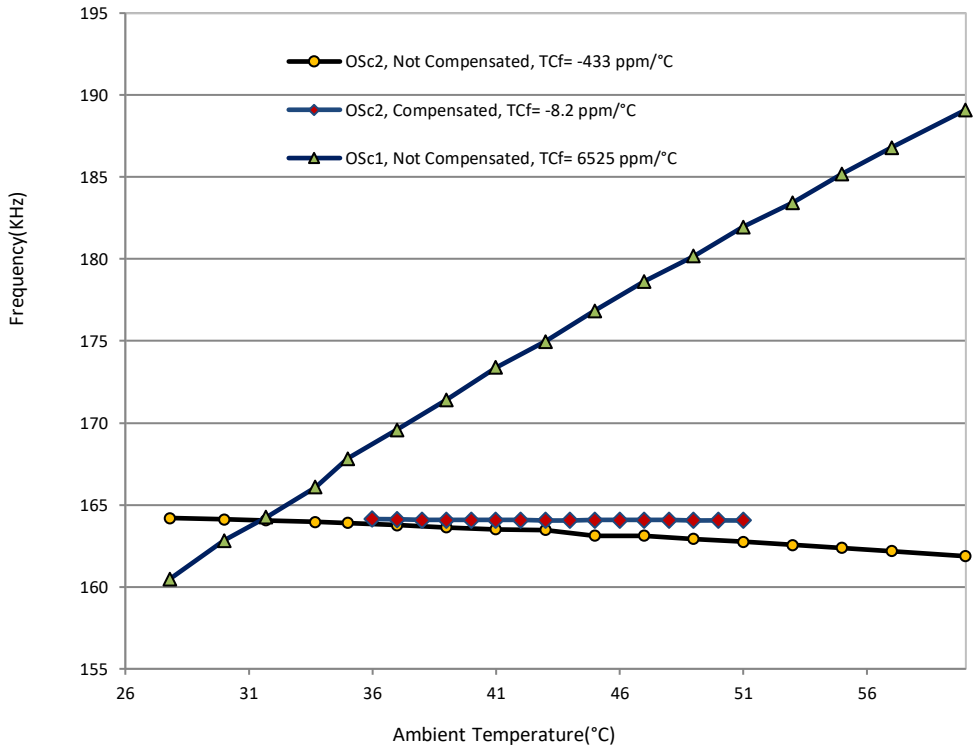


Figure 6-18. *TCf* of oscillators with and without compensation.

[49], the biasing of the two oscillators are set to have their TCfs very different from each other. In Figure 6-18, the frequency of the two oscillators with respect to the ambient temperature, which is in turn set by the oven temperature, are shown, with and without temperature compensation. Without temperature compensation, Osc1 has an intrinsic TCf of -433 ppm/°C, and Osc2 has an intrinsic TCf of 6525 ppm/°C. With the temperature compensation mechanism in place, the frequency of Osc1 and Osc2, which are locked, varies with temperature with a rate of - 8.2ppm/°C.

Since the intrinsic temperature sensitivity of Osc2 is -433 ppm/°C, the actual temperature of the die area Ocs2 is located in is varied at a rate at least 53 times (i.e., 433/8.2) smaller than the ambient temperature variations. This is achieved with a maximum heater current of 100 mA, corresponding to a compensated range of 16°C (from 36°C to 52°C). Therefore, this measurement shows that the temperature compensation system improves temperature stability of at least 50x. The temperature compensation in this system happens by preventing the die area's temperature from varying. Therefore, in addition, other temperature compensation mechanisms can be applied to the circuit concurrently, and other temperature-sensitive circuit blocks can be placed in the temperature stabilized area provided by this scheme.

6.3 Summary and Conclusion

This chapter explained a circuit implementation of the proposed temperature compensation system. The system was implemented in a 130nm standard CMOS technology. The design of the circuit elements making up the thermal feed-back controlled PLL system was elaborated. The design of the micro-heaters in the M2 layer of the die with the help of thermal simulation was presented first. It was shown that a more heat preserving technology like SOI could improve the temperature compensation range of the system by many folds. The structure of the CMOS oscillators used in the PLL loop was explained next. For this purpose, two current-starved ring oscillators were employed. The temperature to frequency function for the different starvation current was studied. The design of the frequency dividers, the phase frequency detector, the charge pump and the loop filter provided to the system were also explained. In addition, the design and challenging implementation of the output current buffers for the micro-heater was illustrated.

In the second part of the chapter the measurement results obtained from the operation of the circuit were presented. The measurement results showed that the temperature compensation system improves temperature stability of at least 50x. This of course is limited to a small compensated range of 16°C (from 36°C to 52°C) due to the maximum 100 mA limit of the heater current. As it was shown previously, a more heat preserving technology like SOI can overcome this limitation.

In addition, it was shown that the on-chip micro-heater acts as a low pass filter, which can remove the need for a separate loop filter and charge pump within the PLL.

Chapter 7 Conclusion

7.1 Research Summary

This thesis has aimed to introduce and verify a system for temperature compensation of electronic circuits. This is fulfilled by providing a temperature-insensitive chip area using thermal feedback and a PLL. A natural application of this compensation technique is temperature compensation of the oscillators used in the PLL, and this application was studied in-depth in this work. For this purpose, the proposed temperature compensation system was presented initially. The system consists of two oscillators with a different temperature coefficient of frequencies (TCf). Therefore, the frequency of the two oscillators varies differently when the ambient temperature changes. This different response to temperature can be detected in a PLL with two parallel loops with one oscillator in each loop.

After the system description, the behavior of the proposed PLL system with two parallel loops is analyzed. In the analysis, a linear approximation is used, and based on that, the system response to step and ramp changes in the ambient temperature is studied. In addition, the effect of non-idealities in some of the elements of the system is considered. These non-idealities include not having a straight line for the frequency versus temperature for oscillators and having two separate heaters for each oscillator instead of one for both.

One important characterization of any oscillator is its phase noise. Therefore, the effect of the interaction of the two oscillators used in the system on the phase noise of each of the oscillators was studied and presented in depth in the next step. It was shown that the system could be designed so that if one of the oscillators is a low-price and high-noise oscillator, its effect on the phase noise of the other oscillator can be minimized.

The application of this temperature compensation system on MEMS-based oscillators was also presented and simulated. For this purpose, the MEMS resonators built in-house were used as reference and the effect of the temperature compensation system on them was studied and the simulation result for both system level and circuit level simulations were presented showing the ability of the system to stabilize the effect of ambient temperature on the oscillators.

In the end, the system's performance was verified by the fully integrated implementation of the system in standard CMOS technology. For this purpose, two current-starved ring oscillators were implemented in a PLL loop with thermal feedback made by micro-heaters built on top of the oscillators. The implementation challenges like making huge current buffers to feed the micro-heaters were explained.

The measurement results presented showed some of the promising and shortcomings of the system. It showed that the system, if implemented in a regular bulk CMOS technology, can burn a large amount of power, and therefore the temperature compensation range it can provide is very small. To address that, using other technologies like silicon on insulator (SOI), were suggested. With simulation, it was shown that it could increase the temperature compensation range by multiple factors.

In addition, measurement results showed that the filtering effect of the heating system, as expected, can be used to replace the effect of the loop-filter, and both loop-filter and charge pump can be removed from the PLL system. This is an interesting effect of integrating the thermal system with an electronic circuit.

The measurement results showed promising temperature compensation capability of the system. It showed that implemented system could provide an area on the chip which sees the effect of the ambient temperature changes

with a factor of more than 50 times smaller. This is really promising since other temperature compensation systems can be applied to circuits placed in the temperature compensated chip area simultaneously. This can be an interesting subject for future work.

7.2 Future Work

Based on the results obtained in this thesis, there are a number of areas that future work seems to be insightful.

7.2.1 Implementing One Micro-heater for Both Oscillators

As shown in Chapter 3, when there are two micro-heaters each for one of the oscillators, the temperature of the two oscillators, even when the PLL loop is closed can have a small difference. This systematically allow some temperature fluctuation at the oscillators when the ambient temperature changes. To address this deficiently, a design with only one micro-heater for both oscillators in a way that the temperature of both oscillators always stays the same is the next natural step for future work.

7.2.2 Implementation in More Heat Preserving Technologies Like SOI

One main shortcoming of this implementation is its high heat dissipation, which consequently lowers the temperature compensation range of the system. It was shown that implementing the system in a technology like SOI that has a more heat preservation capability can reduce the system's power and increase its temperature compensation range by many folds. This improvement is necessary if the technique is going to be practical since the current proof of concept design has too much current dissipation and a very limited temperature compensation range. If some improvements in the compensation range is performed, this method can be used in applications that need very precise temperature stability and do not have a large power limitation like optical datacenters and server rooms.

7.2.3 Using the Current Scheme Concurrently with Other Electronic Temperature Compensation Schemes

A big advantage of the proposed scheme over other electronic temperature compensation schemes is the way it provides temperature compensation. In this scheme, a temperature compensated area on the die is created. Therefore, one future work idea can be applying other electronic temperature compensation schemes to the circuits located in the temperature compensated area of the die created by the scheme proposed here. This should significantly affect the temperature compensation ability of the system.

7.2.4 Study and Measurements of the Phase Noise of the Oscillators Used in the Proposed Scheme

One main application of the proposed scheme is the temperature compensation of oscillators used in the scheme. As explained in Chapter 4, the two oscillators employed in the scheme can affect the phase noise, and there are ways to tune the PLL loop for optimum phase noise performance. Study of this aspect and performing corresponding measurements can be very insightful when the scheme is used for temperature compensation of oscillators.

LIST OF REFERENCES

[1] J.-H. Li, X.-b. Zhang, and M.-y. Yu, "A 1.2-V Piecewise Curvature-Corrected Bandgap Reference in 0.5$\mu $ m CMOS Process," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 19, no. 6, pp. 1118-1122, 2010.

[2] C. M. Andreou, S. Koudounas, and J. Georgiou, "A Novel Wide-Temperature-Range, 3.9 ppm/◦C CMOS Bandgap Reference Circuit," *IEEE Journal of Solid-State Circuits,* vol. 47, no. 2, pp. 574-581, 2011.

[3] Z.-K. Zhou *et al.*, "A 1.6-V 25-μ A 5-ppm/◦ C Curvature-Compensated Bandgap Reference," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 59, no. 4, pp. 677-684, 2011.

[4] G. Rincon-Mora and P. E. Allen, "A 1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference," *IEEE Journal of Solid-State Circuits,* vol. 33, no. 10, pp. 1551-1554, 1998.

[5] H. Chen, C. Lee, S. Jheng, W. Chen, and B. Lee, "A Sub-1 ppm/°C Precision Bandgap Reference With Adjusted-Temperature-Curvature Compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 6, pp. 1308-1317, 2017.

[6] F. Fiori and P. S. Crovetti, "A new compact temperature-compensated CMOS current reference," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 52, no. 11, pp. 724-728, 2005.

[7] A. Bendali and Y. Audet, "A 1-V CMOS current reference with temperature and process compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 54, no. 7, pp. 1424-1429, 2007.

[8] T. Hirose, Y. Osaki, N. Kuroki, and M. Numa, "A nano-ampere current reference circuit and its temperature dependence control by

using temperature characteristics of carrier mobilities," *2010 Proceedings of ESSCIRC*, 2010: IEEE, pp. 114-117.

[9] M. S. E. Sendi, S. Kananian, M. Sharifkhani, and A. M. Sodagar, "Temperature Compensation in CMOS Peaking Current References," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 65, no. 9, pp. 1139-1143, 2018.

[10] Y. Wang, Y. Hong, W. L. Goh, K. C. Chai, X. Lou, and W. Ye, "A passively compensated capacitive sensor readout with biased varactor temperature compensation and temperature coherent quantization," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017: IEEE, pp. 1-4.

[11] Z. Zhu *et al.*, "A temperature compensation method for magneto-elastic tension sensor in rod-like structure tension measurement," *IEEE Transactions on Magnetics,* vol. 54, no. 4, pp. 1-16, 2018.

[12] L. Xu, J. H. Huijsing, and K. A. Makinwa, "A±4A high-side current sensor with 25V input CM range and 0.9% gain error from− 40° C to 85° C using an analog temperature compensation technique," *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*, 2018: IEEE, pp. 324-326.

[13] F. Ren, W. Zhang, Y. Li, Y. Lan, Y. Xie, and W. Dai, "The temperature compensation of FBG sensor for monitoring the stress on hole-edge," *IEEE Photonics Journal,* vol. 10, no. 4, pp. 1-9, 2018.

[14] C. A. Diaz *et al.*, "Liquid level measurement based on FBG-embedded diaphragms with temperature compensation," *IEEE Sensors Journal,* vol. 18, no. 1, pp. 193-200, 2017.

[15] F. G. Tinta, A. S. Matistic, and G. A. Lagasse, "The Direct Temperature Control of Quartz Crystals in Evacuated Enclosures," *24th Annual Symposium on Frequency Control. 1970*, 1970, pp. 157-167.

[16] V. E. Bottom, "A History of the Quartz Crystal Industry in the USA," *Thirty Fifth Annual Frequency Control Symposium. 1981*, 1981, pp. 3-12.

[17] R. Boroditsky and J. Gomez, "Very low power consumption, ultra low phase noise, miniature conventional OCXO," *European Frequency and Time Forum & International Frequency Control Symposium (EFTF/IFC), 2013 Joint*, 2013, pp. 160-163.

[18] W. L. Hsieh, C. L. Hsu, C. W. Chen, C. Y. Weng, and S. H. Kao, "Highly Stable Miniaturized OCXO with Heater-Embedded Ceramic Package," *2018 IEEE International Frequency Control Symposium (Ifcs),* pp. 291-294, 2018.

[19] F. Nabki, K. Allidina, F. Ahmad, P. V. Cicek, and M. N. El-Gamal, "A Highly Integrated 1.8 GHz Frequency Synthesizer Based on a MEMS Resonator," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 8, pp. 2154-2168, Aug 2009.

[20] K. Sundaresan, G. K. Ho, S. Pourkamali, and F. Ayazi, "Electronically temperature compensated silicon bulk acoustic resonator reference oscillators," *IEEE Journal of Solid-State Circuits,* vol. 42, no. 6, pp. 1425-1434, Jun 2007.

[21] W.-T. Hsu and C.-C. Nguyen, "Stiffness-compensated temperature-insensitive micromechanical resonators," *Technical Digest. MEMS 2002 IEEE International Conference. Fifteenth IEEE International Conference on Micro Electro Mechanical Systems (Cat. No. 02CH37266)*, 2002: IEEE, pp. 731-734.

[22] C. T. C. Nguyen and R. T. Howe, "An integrated CMOS micromechanical resonator high-Q oscillator," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 4, pp. 440-455, Apr 1999.

[23] G. Chance *et al.*, "Integrated MEMS Oscillator for Cellular Transceivers," *2014 IEEE International Frequency Control Symposium (Fcs),* pp. 244-246, 2014.

[24] K. Bongsang *et al.*, "Si-SiO2 Composite MEMS Resonators in CMOS Compatible Wafer-scale Thin-Film Encapsulation," *Frequency Control Symposium, 2007 Joint with the 21st European Frequency and Time Forum. IEEE International*, 2007, pp. 1214-1219.

[25] M. A. Hopcroft *et al.*, "Active temperature compensation for micromachined resonators," *Proc. Solid-State Sensor, Acutator and Microsystems Workshop,* p. 4, 2004.

[26] J. C. Salvia, R. Melamud, S. A. Chandorkar, S. F. Lord, and T. W. Kenny, "Real-Time Temperature Compensation of MEMS Oscillators Using an Integrated Micro-Oven and a Phase-Locked Loop," *Journal of Microelectromechanical Systems,* vol. 19, no. 1, pp. 192-201, Feb 2010.

[27] R. Tabrizian, M. Pardo, and F. Ayazi, "A 27 Mhz Temperature Compensated Mems Oscillator with Sub-Ppm Instability," *2012 IEEE 25th International Conference on Micro Electro Mechanical Systems (Mems),* 2012.

[28] M. H. Perrott *et al.*, "A Temperature-to-Digital Converter for a MEMS-Based Programmable Oscillator With <±0.5-ppm Frequency Stability and <1-ps Integrated Jitter," *IEEE Journal of Solid-State Circuits,* vol. 48, no. 1, pp. 276-291, Jan 2013.

[29] R. F. Adams and D. O. Pederson, "Temperature sensitivity of frequency of integrated oscillators," *IEEE Journal of Solid-State Circuits,* vol. 3, no. 4, pp. 391-396, 1968 1968.

[30] A. A. Abidi, "RF CMOS comes of age," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 4, pp. 549-561, Apr 2004.

[31] T. Tokairin *et al.*, "A 280nW, 100kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme," *VLSI Circuits (VLSIC), 2012 Symposium on*, 2012, pp. 16-17.

[32] A. Paidimarri, D. Griffith, A. Wang, A. P. Chandrakasan, and G. Burra, "A 120nW 18.5 kHz RC oscillator with comparator offset cancellation for±0.25% temperature stability," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 184-185.

[33] C. Ying, P. Leroux, W. De Cock, and M. Steyaert, "A 63,000 Q-factor relaxation oscillator with switched-capacitor integrated error feedback," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 186-187.

[34] G. Zhang, K. Yayama, A. Katsushima, and T. Miki, "A 3.2 ppm/° C second-order temperature compensated CMOS on-chip oscillator using voltage ratio adjusting technique," *IEEE Journal of Solid-State Circuits,* vol. 53, no. 4, pp. 1184-1191, 2018.

[35] Ç. Gürleyük, L. Pedalà, S. Pan, F. Sebastiano, and K. A. Makinwa, "A CMOS Dual-RCFrequency Reference With±200-ppm Inaccuracy From− 45° C to 85° C," *IEEE Journal of Solid-State Circuits,* vol. 53, no. 12, pp. 3386-3395, 2018.

[36] N. Liu *et al.*, "A 2.5 ppm/° C 1.05 MHz Relaxation Oscillator with Dynamic Frequency-Error Compensation and 8 μs Start-up Time," *ESSCIRC 2018-IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, 2018: IEEE, pp. 150-153.

[37] A. Savanth, J. Myers, A. Weddell, D. Flynn, and B. Al-Hashimi, "A 0.68nW/kHz Supply-Independent Relaxation Oscillator with +/- 0.49%/V and 96ppm/degrees C Stability," *2017 IEEE International Solid-State Circuits Conference (Isscc),* pp. 96-96, 2017.

[38] Y. K. Tsai and L. H. Lu, "A 51.3-MHz 21.8-ppm/degrees C CMOS Relaxation Oscillator With Temperature Compensation," *IEEE Transactions on Circuits and Systems Ii-Express Briefs,* vol. 64, no. 5, pp. 490-494, May 2017.

[39] Y. A. Chang and S. I. Liu, "A 13.4-MHz Relaxation Oscillator With Temperature Compensation," *IEEE Transactions on Very Large Scale Integration (Vlsi) Systems,* vol. 27, no. 7, pp. 1725-1729, Jul 2019.

[40] M. S. McCorquodale *et al.*, "A 25-MHz Self-Referenced Solid-State Frequency Source Suitable for XO-Replacement," *IEEE Transactions on Circuits and Systems I-Regular Papers,* vol. 56, no. 5, pp. 943-956, May 2009.

[41] M. S. McCorquodale and V. Gupta, "A History of the Development of CMOS Oscillators: The Dark Horse in Frequency Control," *2011 Joint Conference of the IEEE International Frequency Control Symposium/European Frequency and Time Forum Proceedings,* pp. 437-442, 2011.

[42] E. O. Ates, A. Ergul, and D. Y. Aksin, "Fully Integrated Frequency Reference With 1.7 ppm Temperature Accuracy Within 0-80 degrees C," *IEEE Journal of Solid-State Circuits,* vol. 48, no. 11, pp. 2850-2859, Nov 2013.

[43] Y. Satoh, H. Kobayashi, T. Miyaba, and S. Kousai, "A 2.9 mW,+/−85ppm accuracy reference clock generator based on RC oscillator with on-chip temperature calibration," *2014 Symposium on VLSI Circuits Digest of Technical Papers*, 2014: IEEE, pp. 1-2.

[44] C.-E. Hsieh and S.-I. Liu, "A 2.4-GHz Frequency-Drift-Compensated Phase-Locked Loop With 2.43 ppm/° C Temperature Coefficient," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 27, no. 3, pp. 501-510, 2019.

[45] Y. Wei, T. Xin, L. Wenhong, and L. Ran, "A resistorless CMOS current reference with temperature compensation," *Journal of Semiconductors,* vol. 32, no. 3, p. 035006, 2011.

[46] G. Bosch and J. Koster, "Integrated thermostat voltage stabilizer," *International Solid-State Circuits Conference (ISSCC). Digest of Technical Papers*, 1971, vol. 14: IEEE, pp. 144-145.

[47] J. Lieux and K. Lance, "An ultra-stable voltage reference using a new type of bulk zener diode," *International Solid-State Circuits Conference (ISSCC). Digest of Technical Papers*, 1972, vol. 15: IEEE, pp. 148-149.

[48] P. Gray, D. Hamilton, and D. Lieux, "Analysis and design of temperature stabilized substrate integrated circuits," *IEEE Journal of Solid-State Circuits,* vol. 9, no. 2, pp. 61-69, 1974.

[49] S. A. Gorji Zadeh, M. N. El-Gamal, and F. Nabki, "The phase noise of an oscillator employing a dual MEMS resonator temperature compensation scheme," *International Conference on Microelectronics(ICM), 2010*, 2010, pp. 160-163.

[50] Z. Z. Wu and M. Rais-Zadeh, "A Temperature-Stable Piezoelectric MEMS Oscillator Using a CMOS PLL Circuit for Temperature Sensing and Oven Control," *Journal of Microelectromechanical Systems,* vol. 24, no. 6, pp. 1747-1758, Dec 2015.

[51] K. E. Wojciechowski and R. H. Olsson, "A Fully Integrated Oven Controlled Microelectromechanical Oscillator-Part II: Characterization and Measurement," *Journal of Microelectromechanical Systems,* vol. 24, no. 6, pp. 1795-1802, Dec 2015.

[52] C. S. Liu, R. Tabrizian, and F. Ayazi, "A +/- 0.3 ppm Oven-Controlled MEMS Oscillator Using Structural Resistance-Based Temperature Sensing," *IEEE Transactions on Ultrasonics Ferroelectrics and Frequency Control,* vol. 65, no. 8, pp. 1492-1499, Aug 2018.

[53] D. Yang, J.-K. Woo, S. Lee, J. Mitchell, A. D. Challoner, and K. Najafi, "A micro oven-control system for inertial sensors," *Journal of Microelectromechanical Systems,* vol. 26, no. 3, pp. 507-518, 2017.

[54] P. R. Gray and D. J. Hamilton, "Analysis of electrothermal integrated circuits," *IEEE Journal of Solid-State Circuits,* vol. 6, no. 1, pp. 8-14, 1971.

[55] S. M. Kashmiri, S. Xia, and K. A. A. Makinwa, "A Temperature-to-Digital Converter Based on an Optimized Electrothermal Filter," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 7, pp. 2026-2035, Jul 2009.

[56] G. Bosch and J. Koster, "Integrated thermostat voltage stabilizer," *1971 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 1971, vol. 14: IEEE, pp. 144-145.

[57] S. A. Gorji Zadeh, T. Saha, K. Allidina, F. Nabki, and M. N. El-Gamal, "Electronic temperature compensation of clamped-clamped beam MEMS resonators," presented at the 2010 53rd IEEE International Midwest Symposium on Circuits and Systems, 1-4 Aug. 2010, 2010.

[58] S. A. Gorji Zadeh, K. Allidina, P.-V. Cicek, F. Nabki, and M. N. El-Gamal, "CMOS die area temperature compensation using a phase-locked loop with thermal-feedback," *Analog Integrated Circuits and Signal Processing,* vol. 113, no. 3, pp. 315-329, 2022/12/01 2022.

[59] M. J. Kramer, E. Janssen, K. Doris, and B. Murmann, "A 14 b 35 MS/s SAR ADC achieving 75 dB SNDR and 99 dB SFDR with loop-embedded input buffer in 40 nm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 50, no. 12, pp. 2891-2900, 2015.

[60] S. H. Shalmany, D. Draxelmayr, and K. A. Makinwa, "A ±36-A Integrated Current-Sensing System With a 0.3% Gain Error and a 400- μA Offset From −55 °C to +85 °C," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 4, pp. 1034-1043, 2017.

[61] A. Vaz *et al.*, "Full passive UHF tag with a temperature sensor suitable for human body temperature monitoring," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 57, no. 2, pp. 95-99, 2010.

[62] B. L. Hunter and W. E. Matthews, "A±3 ppm/° C single-trim switched capacitor bandgap reference for battery monitoring applications," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 4, pp. 777-786, 2016.

[63] A. P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE Journal of Solid-State Circuits,* vol. 9, no. 6, pp. 388-393, 1974.

[64] J.-H. Li, X.-b. Zhang, and M.-y. Yu, "A 1.2-V Piecewise Curvature-Corrected Bandgap Reference in 0.5 μm CMOS Process," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 19, no. 6, pp. 1118-1122, 2010.

[65] Q. Duan and J. Roh, "A 1.2-V 4.2- ppm/◦C High-Order Curvature-Compensated CMOS Bandgap Reference," *IEEE Transactions on Circuits and Systems I: regular papers,* vol. 62, no. 3, pp. 662-670, 2014.

[66] G. Ge, C. Zhang, G. Hoogzaad, and K. A. Makinwa, "A Single-Trim CMOS Bandgap Reference With a 3σ Inaccuracy of ±0.15% From −40◦C to 125◦C," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 11, pp. 2693-2701, 2011.

[67] K. K. Lee, T. S. Lande, and P. D. Häfliger, "A Sub-$\mu {\rm W} $ Bandgap Reference Circuit With an Inherent Curvature-Compensation Property," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 62, no. 1, pp. 1-9, 2014.

[68] H. Banba *et al.*, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 5, pp. 670-674, 1999.

[69] B. Ma and F. Yu, "A novel 1.2–V 4.5-ppm/° C curvature-compensated CMOS bandgap reference," *IEEE Transactions on circuits and systems I: Regular Papers,* vol. 61, no. 4, pp. 1026-1035, 2014.

[70] C. Wu, W. L. Goh, C. L. Kok, W. Yang, and L. Siek, "A low TC, supply independent and process compensated current reference," *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015: IEEE, pp. 1-4.

[71] D. Osipov and S. Paul, "Compact extended industrial range CMOS current references," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 66, no. 6, pp. 1998-2006, 2019.

[72] S. S. Chouhan and K. Halonen, "A 0.67- μW 177-ppm/°C All-MOS Current Reference Circuit in a 0.18- μm CMOS Technology," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 63, no. 8, pp. 723-727, 2016.

[73] L. Wang and C. Zhan, "A 0.7-V 28-nW CMOS Subthreshold Voltage and Current Reference in One Simple Circuit," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 66, no. 9, pp. 3457-3466, 2019.

[74] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors," *Proceedings of the IEEE,* vol. 86, no. 8, pp. 1640-1659, 1998.

[75] Z. Guo, C. Lu, Y. Wang, D. Liu, M. Huang, and X. Li, "Design and experimental research of a temperature compensation system for silicon-on-sapphire pressure sensors," *IEEE Sensors Journal,* vol. 17, no. 3, pp. 709-715, 2016.

[76] W. Chen, J. Huang, C. Zhu, F. Xu, and Q.-A. Huang, "An Interdigital Capacitive Humidity Sensor With Layered Black Phosphorus Flakes as a Sensing Material," *IEEE Sensors Journal,* vol. 19, no. 23, pp. 11007-11013, 2019.

[77] F. Fries *et al.*, "Design and Implementation of a Compact Rotational Speed and Air Flow Sensor for Unmanned Aerial Vehicles," *IEEE Sensors Journal,* vol. 19, no. 22, pp. 10298-10307, 2019.

[78] H. Bae, L. Dunlap, J. Wong, and M. Yu, "Miniature temperature compensated Fabry–Pérot pressure sensors created with self-aligned polymer photolithography process," *IEEE Sensors Journal,* vol. 12, no. 5, pp. 1566-1573, 2011.

[79] D. Li, T. Li, and D. Zhang, "A monolithic piezoresistive pressure-flow sensor with integrated signal-conditioning circuit," *IEEE Sensors Journal,* vol. 11, no. 9, pp. 2122-2128, 2010.

[80] M. Tavakoli and R. Sarpeshkar, "An offset-canceling low-noise lock-in architecture for capacitive sensing," *IEEE Journal of Solid-State Circuits,* vol. 38, no. 2, pp. 244-253, 2003.

[81] F. Reverter Cubarsí, G. Horak, V. Bilas, and M. Gasulla Forner, "Novel and low-cost temperature compensation technique for piezoresistive pressure sensors," *XIX IMEKO World Congress. Fundamental and Applied Metrology*, 2009, pp. 2084-2087.

[82] Z. Guo, C. Lu, Y. Wang, D. Liu, M. Huang, and X. Li, "Design and Experimental Research of a Temperature Compensation System for Silicon-on-Sapphire Pressure Sensors," *IEEE Sensors Journal,* vol. 17, no. 3, pp. 709-715, 2017.

[83] K. J. Schoepf *et al.*, "TCMO: A versatile MEMS oscillator timing platform," *Proc. of the 41st Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting,* 2009.

[84] D. B. Leeson, "A SIMPLE MODEL OF FEEDBACK OSCILLATOR NOISE SPECTRUM," *Proceedings of the Institute of Electrical and Electronics Engineers,* vol. 54, no. 2, pp. 329-&, 1966 1966.

[85] M. A. Schmidt and R. T. Howe, "Silicon resonant microsensors," *14th Automotive Materials Conference: Ceramic Engineering and*

Science Proceedings, 1986, vol. 8, no. 9/10: Wiley Online Library, pp. 1019-1034.

[86] J. Greenwood, "Etched silicon vibrating sensor," *Journal of Physics E: Scientific Instruments,* vol. 17, no. 8, p. 650, 1984.

[87] W. T. Hsu and C. T. C. Nguyen, "Stiffness-compensated temperature-insensitive micromechanical resonators," *Fifteenth IEEE International Conference on Micro Electro Mechanical Systems, Technical Digest,* pp. 731-734, 2002.

[88] K. Lakin, K. McCarron, J. McDonald, and J. Belsick, "Temperature coefficient and ageing of BAW composite materials," *Proceedings of the 2001 IEEE International Frequncy Control Symposium and PDA Exhibition (Cat. No. 01CH37218)*, 2001: IEEE, pp. 605-608.

[89] R. Abdolvand, G. K. Ho, J. Butler, and F. Ayazi, "ZnO-on-nanocrystalline diamond lateral bulk acoustic resonators," *2007 IEEE 20th International Conference on Micro Electro Mechanical Systems (MEMS)*, 2007: IEEE, pp. 795-798.

[90] J. C. Salvia, R. Melamud, S. A. Chandorkar, S. F. Lord, and T. W. Kenny, "Real-Time Temperature Compensation of MEMS Oscillators Using an Integrated Micro-Oven and a Phase-Locked Loop," *Microelectromechanical Systems, Journal of,* vol. 19, no. 1, pp. 192-201, 2010.

[91] R. Tabrizian, M. Pardo, and F. Ayazi, "A 27 MHz temperature compensated MEMS oscillator with sub-ppm instability," *IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS)*, 2012: IEEE, pp. 23-26.

[92] B. Pei, P. Zhong, K. Sun, H. Yang, and X. Li, "Micro-oven-controlled MEMS oscillator with electrostatic tuning for frequency trimming," *2018 IEEE Micro Electro Mechanical Systems (MEMS)*, 2018: IEEE, pp. 731-734.

[93] C.-S. Liu, R. Tabrizian, and F. Ayazi, "A±0.3 ppm Oven-Controlled MEMS Oscillator Using Structural Resistance-Based Temperature Sensing," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control,* vol. 65, no. 8, pp. 1492-1499, 2018.

[94] H.-K. Kwon, L. C. Ortiz, G. D. Vukasin, Y. Chen, D. D. Shin, and T. W. Kenny, "An Oven-Controlled MEMS Oscillator (OCMO) With Sub 10mw,±1.5 PPB Stability Over Temperature," *2019 20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII)*, 2019: IEEE, pp. 2072-2075.

[95] N. Liu, R. Agarwala, A. Dissanayake, D. S. Truesdell, S. Kamineni, and B. H. Calhoun, "A 2.5 ppm/° C 1.05-MHz Relaxation Oscillator With Dynamic Frequency-Error Compensation and Fast Start-Up Time," *IEEE Journal of Solid-State Circuits,* 2019.

[96] H. Jiang, P.-H. P. Wang, P. P. Mercier, and D. A. Hall, "A 0.4-V 0.93-nW/kHz relaxation oscillator exploiting comparator temperature-dependent delay to achieve 94-ppm/° C stability," *IEEE Journal of Solid-State Circuits,* vol. 53, no. 10, pp. 3004-3011, 2018.

[97] K. Sundaresan, P. E. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator," *IEEE Journal of Solid-State Circuits,* vol. 41, no. 2, pp. 433-442, Feb 2006.

[98] X. Zhang and A. B. Apsel, "A low-power, process-and-temperature-compensated ring oscillator with addition-based current source," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 58, no. 5, pp. 868-878, 2011.

[99] N. Wadhwa, P. G. Bahubalindruni, and S. Deb, "A PVT Insensitive Low-Power Differential Ring Oscillator," *International Symposium on VLSI Design and Test*, 2018: Springer, pp. 77-87.

[100] N. Rai, V. Agarwal, N. Wadhwa, B. Tiwari, and P. G. Bahubalindruni, "Temperature Insensitive Low-Power Ring Oscillator Using only n-type Transistors," *International Symposium on VLSI Design and Test*, 2018: Springer, pp. 359-369.

[101] K. Jung, K. Cho, S. Lee, and J. Kim, "A Temperature Compensated RF $ LC $ Clock Generator With±50-ppm Frequency Accuracy From− 40° C to 80° C," *IEEE Transactions on Microwave Theory and Techniques,* vol. 67, no. 11, pp. 4441-4449, 2019.

[102] L. Hao, N. Klein, J. C. Gallop, W. J. Radcliffe, and I. S. Ghosh, "Temperature compensated cryogenic whispering gallery mode resonator for microwave frequency standard applications," *IEEE Transactions on Instrumentation and Measurement,* vol. 48, no. 2, pp. 524-527, Apr 1999.

[103] W. Jung, "Low-Power Energy Efficient Circuit Techniques for Small IoT Systems," PhD, University of Michigan, 2017.

[104] F. M. Gardner, *Phaselock techniques*, 3 ed. Hoboken, N.J.: Wiley-Interscience, 2005.

[105] M. A. Hopcroft *et al.*, "Temperature compensation of a MEMS resonator using quality factor as a thermometer," *Mems 2006: 19th IEEE International Conference on Micro Electro Mechanical Systems, Technical Digest,* pp. 222-225, 2006.

[106] Y. C. Liu, M. H. Tsai, W. C. Chen, M. H. Li, S. S. Li, and W. L. Fang, "Temperature-Compensated CMOS-MEMS Oxide Resonators," *Journal of Microelectromechanical Systems,* vol. 22, no. 5, pp. 1054-1065, Oct 2013.

[107] M. A. Taghvaei, P. V. Cicek, K. Allidina, F. Nabki, and M. N. El-Gamal, "A MEMS-Based Temperature-Compensated Vacuum Sensor for Low-Power Monolithic Integration," *2010 IEEE International Symposium on Circuits and Systems,* pp. 3276-3279, 2010.

[108] S. Chen, T. V. Baughn, Z. J. Yao, and C. L. Goldsmith, "A new in situ residual stress measurement method for a MEMS thin fixed-fixed beam structure," *Journal of microelectromechanical systems,* vol. 11, no. 4, pp. 309-316, 2002.

[109] F. Nabki, T. A. Dusatko, S. Vengallatore, and M. N. El-Gamal, "Low-temperature (< 300° C) low-stress silicon carbide surface micromachining fabrication technology," *Hilton Head Workshop 2008: A Solid-State Sensors, Actuators and Microsystems Workshop*, 2008, pp. 216-219.

[110] F. M. Gardner, "Charge-Pump Phase-Lock Loops," *IEEE Transactions on Communications,* vol. 28, no. 11, pp. 1849-1858, 1980.

[111] F. M. Gardner, *PHASELOCK TECHNIQUES Third Edition INTRODUCTION* (Phaselock Techniques, 3rd Edition). 2005, p. 450.

[112] B. Razavi, *RF microelectronics*. Pearson Education, 2012.

[113] S. A. G. Zadeh, T. Saha, K. Allidina, F. Nabki, and M. N. El-Gamal, "Electronic Temperature Compensation of Clamped-Clamped Beam MEMS Resonators," *53rd Ieee International Midwest Symposium on Circuits and Systems,* pp. 1193-1196, 2010.

[114] A. Vassighi and M. Sachdev, *Thermal and Power Management of Integrated Circuits*. Springer US, 2006.

[115] K. Kundert, *Predicting the phase noise of PLL-based frequency synthesizers*, 2019. [Online]. Available: http://www.designers-guide.org. Accessed on: 2020.

[116] C. M. Jha *et al.*, "High resolution microresonator-based digital temperature sensor," *Applied Physics Letters,* vol. 91, no. 7, Aug 13 2007, Art no. 074101.

[117] K. Ogata and Y. Yang, *Modern control engineering*. Prentice hall Upper Saddle River, NJ, 2010.

[118] F. Nabki and M. N. El-Gamal, "A High Gain-Bandwidth Product Transimpedance Amplifier for MEMS-Based Oscillators," in *Esscirc 2008: Proceedings of the 34th European Solid-State Circuits Conference*, W. RedmanWhite and A. Walton, Eds. (Proceedings of the European Solid-State Circuits Conference, 2008, pp. 454-457.

[119] M. H. Li, C. S. Li, C. H. Chin, C. Y. Chen, and S. S. Li, "An Ultra-Low Power Ovenized Cmos-Mems Resonator Monolithically Integrated with Interface Circuits," *26th IEEE International Conference on Micro Electro Mechanical Systems (Mems 2013),* pp. 753-756, 2013.

[120] J. Laconte, U. Dupont, D. Flandre, and J. P. Raskin, "SOICMOS compatible low-power microheater optimization for the fabrication of smart gas sensors," *IEEE Sensors Journal,* vol. 4, no. 5, pp. 670-680, Oct 2004.

[121] L. Cao, A. A. Aboketaf, and S. F. Preble, "CMOS compatible micro-oven heater for efficient thermal control of silicon photonic devices," *Optics Communications,* vol. 305, pp. 66-70, 2013.

[122] J. Craninckx and M. S. J. Steyaert, "A fully integrated CMOS DCS-1800 frequency synthesizer," *IEEE Journal of Solid-State Circuits,* vol. 33, no. 12, pp. 2054-2065, Dec 1998.

[123] W. Rhee, "Design of high-performance CMOS charge pumps in phase-locked loops," *Iscas '99: Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, Vol 2,* pp. 545-548, 1999.