Modeling and Nanoprobe Experiments of Interband Tunneling Effects in Indium Nitride Nanowires

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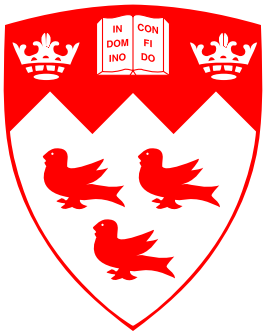

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Abstract

The study of interband tunneling effects is motivated by interest in low voltage transistors that function on the basis of modulated interband tunneling current. InN/Si junctions are modeled with numerical simulation program, APSYS, and are electrically characterized with a custom-built nanoprobe setup to investigate their interband tunneling properties for the first time. Numerical simulations show that a p-Si/n-InN junction behaves as a typical Esaki tunneling diode, with a tunneling current density peak of $\sim$ 6 kA/cm^2 at very low voltage biases ($\sim$ 35 mV). InN/Si tunneling field effect transistors are also designed and optimized with the software; they exhibit sub-threshold voltage swings S below 8 mV/decade over 5 decades, and current ratios exceeding 10^7. Our electrical measurements of the p-Si/n-InN diodes exhibit interband tunneling current densities up to 12 kA/cm^2 under a reverse bias of -1 V; however, tunneling is impeded due to interfacial layers and deep-level traps that restrict the observations of a tunneling current peak and a negative differential resistance region under forward bias. To circumvent the complications caused by the InN/Si interface, p-InN/n-InN homojunctions on Si substrates are also investigated with both software and electrical measurements. While the simulations show that the simple homojunction displays normal Esaki characteristics, the added n-InN/n-Si junction complicates the overall device behavior. Nevertheless, both simulations and electrical measurements demonstrate a tunneling peak and a negative differential resistance region. Tunneling current peaks above 5 kA/cm^2 and peak-to-valley-current-ratios higher than 3 are frequently observed with our measurements of the p-InN/n-InN/n-Si junctions.

Abrégé

L'étude des effets de tunnel interbande est motivée par l'intérêt en basse tension des transistors qui fonctionnent par modulation d'interbande courant à effet tunnel. Jonctions InN/Si sont modélisés avec le programme de simulation numérique, APSYS, et sont caractérisés électriquement avec une configuration de nanosonde construit sur mesure pour enquêter leurs propriétés interbande de tunnels pour la première fois. Les simulations numériques montrent qu'une jonction p-Si/n-InN se comporte comme une diode Esaki typique tunnel, avec un maximum de densité de tunnel courant ~ 6 kA/cm^2 à de trés faibles tension (~ 35 mV). InN/Si transistors à effet tunnel sont également conçus et optimisés avec le logiciel; ils présentent sous-seuil balançoires de tension S inférieures à 8 mV / décade plus de 5 décennies, et les ratios de courant dépassant 10^7. Nos mesures électriques des diodes présentent des densités de courant tunnel interbande p-Si/n-InN jusqu'à 12 kA/cm^2 en vertu d'une tension inverse de -1 V; toutefois, conduction de tunnel est entravée en raison de couche d'interface et des pièges à niveau profonde qui restreignent les observations d'un pic de courant à effet tunnel et une région de résistance négative différentielle sous polarisation directe. Pour contourner les complications à cause de l'interface InN/Si, les homojonctions p-InN/n-InN sur des substrats de silicium sont également étudiés à la fois avec des logiciels et des mesures électriques. Alors que les simulations montrent que les homojonction simples affichent à caractéristiques Esaki normales, l'ajoutés n-InN/n-Si jonction complique le comportement global de l'appareil. Néanmoins, les deux simulations et des mesures électriques montrent un pic de tunnel et une région de résistance négative différentielle. Pics de courant tun-

nel supérieures à 5 kA/cm ^{2} et rapports de courant pic-vallée supérieur à 3 sont observés fréquemment avec nos mesures des jonctions p-InN/n-InN/n-Si.

Acknowledgements

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I also want to thank my colleagues in the lab, both past and present: Shadi Sabri, Mohamed Abdelghany, Vahid Tayari, Nicholas Hemsworth, William Dickerson, Farzaneh Mahvash, Peter Gaskell, Jonathan Guillemette and Helgi Skulason. They helped me get accustomed to life as a researcher when I first joined the group, as well as making my time in the lab more enjoyable. They also shared their valuable advice and experience to assist me with the obstacles I faced.

I want to thank Daron Westly from the Cornell Nanoscale Facilty for his help during our nanoprobe measurements inside an SEM enviroment. I also thank Donald Pavlasek from the machine shop at the ECE Department at McGill University for helping me design and machine our own nanoprobe setup.

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Chapter 1

Introduction

1.1 The Energy Costs of the CMOS Transistor

Ever since the emergence of modern computing, Moore's law has been a self-fulfilling prophecy. In 1965, Gordon Moore, co-founder of Intel, predicted that the number of transistors per square inch on integrated circuits would double every year [1], and since then, his forecast has served as the goal for the entire semiconductor industry. It has been 50 years since Moore's prediction, and although he has revised the doubling time to every two years [2], the continued growth of the number of transistors per area on the silicon chip remains true, and is unparalleled in the history of industrial technology. The advances in miniaturization of transistors has come with significant improvements to our electronic devices, especially microprocessors and memory [3, 4, 5].

The cost of computation has always been at the heart of Moore's prediction, as well as a driving force for technological change, productivity, and economic growth [3]. With costs steadily falling, the information and communication tech-

nology (ICT) ecosystem is growing at remarkable rates; this growth however, has had a major impact on the global energy consumption, approximately 1500 TWhr per year (10% of global electricity production) [6]. The environmental implications of the unprecedented energy consumption by the computing infrastructure have finally caught the public's attention [7], and it is becoming vital to improve the energy efficiency of transistors, the key components in electronic circuitry.

The most common transistors in today's electronics are complementary metal-oxide-semiconductor (CMOS) field effect transistors (FETs). To a large degree, their energy efficiency has kept pace with five decades of Moore's prophecy. However, advances in CMOS technology, and Moore's law, are rapidly approaching physical limitations that lead to higher power and energy consumption [4].

Leakage is one of the major limitations of MOS based transistors that lead to higher energy consumption. With channel-lengths around 10 nm ($\sim$ 90 silicon Si atoms), and gate oxides nearly 1 nm in thickness, it is becoming increasingly difficult to prevent leakage currents that degrade the switching ratio of on and off currents I_{ON}/I_{OFF} [8]. Furthermore, the continued increase in the density of transistors on an integrated circuit (IC) has lead to more electrical interconnects between them and larger load capacitances C. Another challenge CMOS transistors face is their supply voltage; despite the constant miniaturization, their operating voltage has not been reduced proportionately [4, 8, 9, 10].

These obstacles are beginning to have significant effects on the energy consumed by CMOS transistors in logic operation. To better understand the effects of these obstacles on consumed energy, one should look at the formula govern-

ing such energy consumption. The mean energy E consumed per transistor per clock-cycle in a digital circuit is [4]:

$$E = CV^2(\alpha + \frac{I_{OFF}}{I_{ON}}\beta) \tag{1.1}$$

where C is the average load capacitance dominated by interconnects delay (~ 10 fF), V is the operating voltage of the transistor (~1 V), α is the logic activity factor (typically ~ 0.01), I_{ON}/I_{OFF} is ~ 10^6, and β is the ratio of clock period to intrinsic switch delay (~ 100-1000).

Researchers from different backgrounds have focused substantial efforts to tackle these obstacles and improve the energy E consumed during logic operation. One potential method is using optical fibers as interconnects instead of electrical wiring to reduce load capacitances C [11]. A different approach that researchers are investigating is reducing the operating voltage V while maintaining a fixed current ratio I_{ON}/I_{OFF} [4]. However, the major obstacle in reducing the voltage supply of CMOS FETs is inherent in its mode of operation. MOS based transistors rely on the thermionic injection of electrons over an energy barrier. This sets a fundamental limit on their operation and the transition from the "off-state" to the "on-state". The required gate voltage V_G to change the drain current I_D by one order of magnitude, when the transistor is operated in the sub-threshold region (the transition region), is a transistor's sub-threshold voltage swing S [4],

$$S = \frac{\delta V_G}{\delta \log I_D} \tag{1.2}$$

In the case of a MOS transistor, the sub-threshold voltage swing is limited to [4]:

$$S = \frac{\delta V_G}{\delta \log I_D} \cong (1 + \frac{C_d}{C_{ox}}) \ln 10 \frac{kT}{q} \cong 60 \text{ mV decade}^{-1} | T = 300\text{K} \qquad (1.3)$$

where kT/q is the thermal voltage, and C_d and C_{ox} are the depletion and the oxide capacitances, respectively.

Rather than limiting the sub-threshold voltage swing of transistors to thermionic injection, new physical principles should be investigated. To continue the advancement of integrated circuit performance, and improve the energy efficiency of electronics, it is important to look at technologies "beyond CMOS"; one such technology is the tunnel field effect transistor (TFET) [4, 8, 9, 10].

1.2 The Physics of TFETs

Unlike MOS transistors, where carriers flow over a potential barrier modulated by a gate voltage, the TFET is a quantum device that makes use of gate modulated interband tunneling, and charge carriers tunnel from one energy band into another at a heavily doped p-n junction.

Quantum tunneling arose during the infancy of quantum theory, when de Broglie introduced the wave-particle duality in 1923, that particles may exhibit wave-like characteristics [12]. While trying to understand radioactivity and decay of the atomic nucleus, George Gamow and independently Ronald Gurney and Edward Condon discovered, with the help of Schrödinger's wave equations

[13], that electrons can tunnel through a potential barrier [14, 15]. However, Max Born recognized the generality of quantum tunneling; it was not only restricted to nuclear physics, but also applicable to different physical systems [15]. In 1934, Clarence Zener first proposed interband quantum tunneling, also known as band to band tunneling (BTBT), to explain dielectric breakdown [16]. He showed through calculations that an energy gap could be treated in the manner of a potential barrier, and that electrons can tunnel through. Although his theory for interband tunneling never proved important for dielectric breakdown, due to avalanche breakdown occurring at much lower voltages, it did pave the way for Leo Esaki to demonstrate interband tunneling in 1957 using p-n Ge diodes [17]. It was the first time electron tunneling was proven in devices [15], and Esaki's discovery later led to the sharing of a Nobel prize in physics with Ivar Giaever and Brian David Josephson in 1973 [18].

Esaki demonstrated that by engineering an appropriate junction, it is possible to have the conduction band of the n-sided region below the valence band of the p-sided region (Fig. 1.1(a)). Applying a small voltage bias across the source (S) and drain (D), charge carriers can tunnel from the valence band to the conduction band, resulting in the flow of current through the diode.

The TFET's structure is very similar to an Esaki diode with a channel between the p-doped and n-doped regions. The channel can be intrinsic, lightly n-doped, or p-doped. In the "off-state" (Fig. 1.1(b)), the depleted channel acts as a barrier to the charge carriers and prevents any band to band tunneling, and subsequently the flow of current. However, by applying a gate voltage (Fig. 1.1(c)), the TFET is turned on, and the energy bands of the channel are lowered to enable

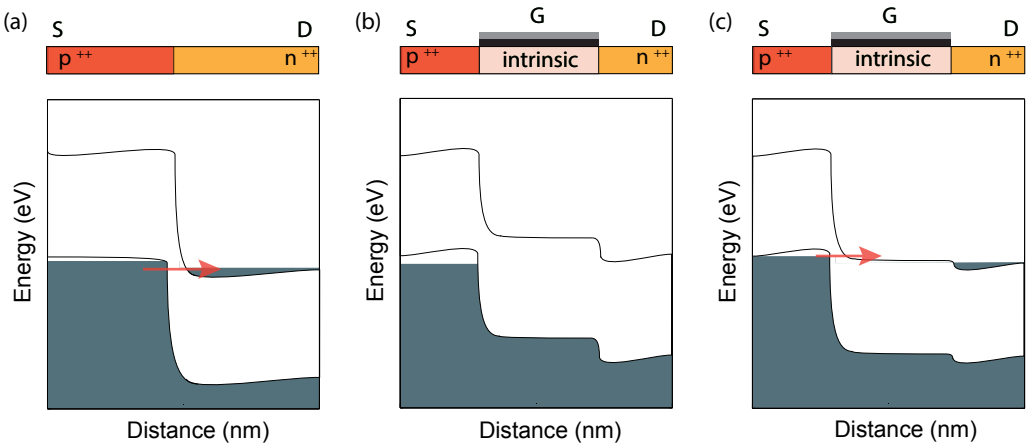


Fig. 1.1: Layer structures and energy band diagrams of (a) a tunneling Esaki diode, (b) a TFET in the "off-state", (c) and "on-state".

quantum tunneling and current to flow.

In principle, the TFET has all the necessary characteristics of a traditional transistor; it exhibits current gain, voltage gain, and current saturation. However, its most appealing characteristic is its theoretically ultra-low sub-threshold voltage swing S. Rather than being limited by thermionic injection, the TFET sub-threshold swing is limited by the ideality of quantum tunneling, providing a sharper modulation of channel current versus gate voltage than in a MOS transistor. Fig. 1.2 shows a comparison of S between a traditional MOS transistor and a TFET. Due to the TFET's superior S, it can operate at a low voltage (point A) with a superior performance (higher I_{ON}) and a better I_{ON}/I_{OFF} current ratio than a MOSFET at the same voltage. On the other hand, operating at a higher voltage performance, point B, the MOSFET becomes more suitable in terms of transistor performance but at the cost of higher energy consumption.

It is also important to note that, as a consequence of the BTBT mechanism, S in a TFET is not constant, but depends on the applied gate voltage (increasing

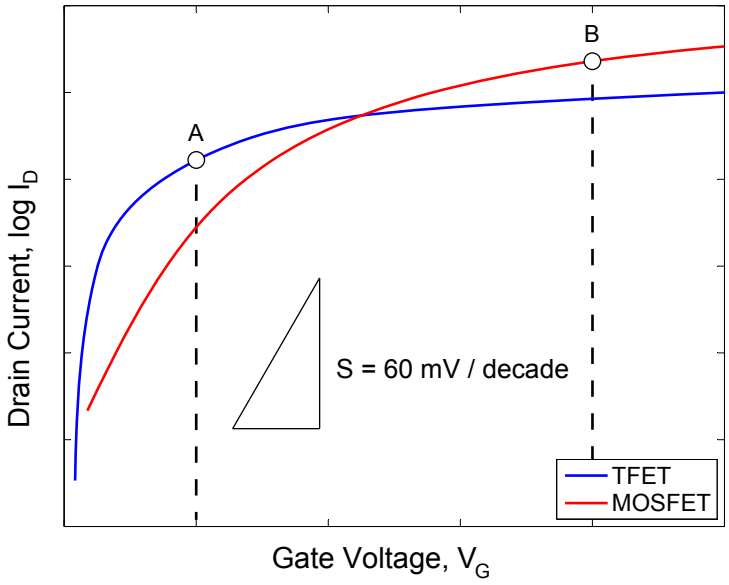


Fig. 1.2: A typical comparison of the drain current of both MOS and tunneling transistors with respect to gate voltage applied.

with gate voltage). Therefore, it is necessary for a TFET to maintain an S below 60 mV per decade over several orders of magnitude of drain current for it to be considered energy efficient [4]. S values below 60 mV/decade have been successfully demonstrated, with the record at 20 mV/decade; however, they have yet to be maintained over several decades [4, 10, 19]. A summary of existing state-of-the-art TFETs found in the literature is listed in Table 1.1.

For the TFET to outperform MOS transistors, it is important to optimize not only the sub-threshold swing over several decades, but to achieve high on currents as well. Current densities above 1 kA/cm^2 should be expected from TFETs with I_{ON}/I_{OFF} ratios exceeding 10^5 if they are to be considered as viable CMOS alternatives. The on current of a TFET depends on the interband tunneling of the device, and consequently on the transmission probability T_{WKB} through the

Structure	S (mV/dec)	I_{ON}	I_{ON}/I_{OFF}	Ref.
Si	~ 42	~ 0.1 μA/μm $\|V_{SD}$=1V	~ 10^6	[20]
Double Gate Ge	~ 50	~ 0.5 μA/μm $\|V_{SD}$=0.5V	~ 10^7	[21]
C Nanotube	~ 40	~ 20 pA $\|V_{SD}$=0.5V	~ 10^4	[22]
Si/InAs	~ 21	~ 1 μA/μm $\|V_{SD}$=1V	~ 10^6	[23]
GaSb/InAs R-TFET	~ 25	~ 1 μA/μm $\|V_{SD}$=0.3V	~ 10^6	[24]
InP/GaAs	~ 30	~ 0.1 μA $\|V_{SD}$=0.75V	~ 10^7	[25]
InGaAs	~ 58	~ 0.2 μA/μm $\|V_{SD}$=0.05V	~ 10^4	[26]

Table 1.1: A summary of state-of-the-art TFETs found in literature.

simple parabolic barrier (Fig. 1.3). The transmission probability can be determined with the Wentzel-Kramer-Brillouin (WKB) approximation [4, 10, 27]:

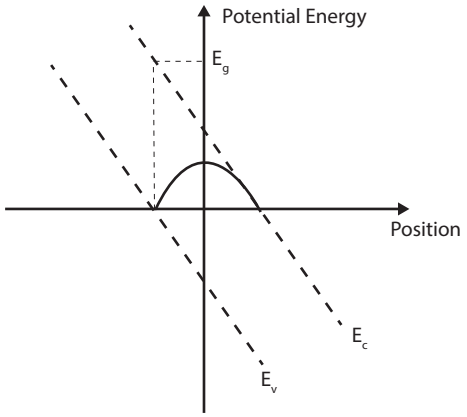


Fig. 1.3: A parabolic potential barrier across a junction.

$$T_{WKB} \approx \exp\left(-\frac{\pi\lambda\sqrt{m^*}\sqrt{E_g^3}}{2\sqrt{2}q\hbar(E_g+\Delta\Phi)}\right) \tag{1.4}$$

where λ is the tunneling length over which electrons propagate evanescently through the gap, m^* is the effective mass, E_g is the bandgap in the tunneling

region, q is an electron charge, and $\Delta\Phi$ is the bandwidth of conduction and valence band energy overlap. It is important to note that the formula works well with direct bandgap semiconductors, but has limited accuracy for indirect band gap structures such as Si and Ge [4].

This simple model captures the basic requirements to realize high on currents. The transmission probability of the tunneling barrier should be close to unity for a small change in gate voltage. In order to achieve that, smaller bandgaps E_g, lower effective carrier mass m^*, and shorter tunneling lengths λ are favorable; however, they should be sufficiently large to ensure that the channel can turn off. These parameters all rely on the materials of the junction, and consequently, it is important to investigate the correct material combinations to engineer the best tunneling junction with high barrier transparency.

A wide range of material combinations and TFET designs have been explored to achieve optimum tunneling characteristics with sub-threshold swings below 60 mV and high I_{ON}/I_{OFF} ratios, such as Si TFETs, group III-V TFETs and even carbon based TFETs. Although they have yet to replace MOS transistors, the semiconductor community is very optimistic about the TFET's future, especially group III-V TFETs [4, 8, 9, 10]. One of the promising materials for TFET design is indium nitride.

1.3 Properties of Indium Nitride

InN has many attractive features for interband tunneling, but most importantly, it has the largest electron affinity of all common semiconductors (Fig. 1.4 [28]). This allows for a large built-in field and ideal semiconductor band align-

ment with other semiconductors, especially silicon, for BTBT. Quite simply, InN's band structure makes it the ideal n-type material for a TFET. Furthermore, InN has the necessary characteristics for a transparent barrier; it has a narrow band gap (~0.65 eV [29]), low effective mass ($m_e^* = 0.05m_0$ and $m_h^* = 0.3 - 0.65m_0$ [30, 31]), and a short tunneling length in the tunneling region. InN also displays high electron mobility (~ 10^3-10^4 cm^2/Vs), and high conductivity, both of which are ideal for low access resistance and high current density operation [32].

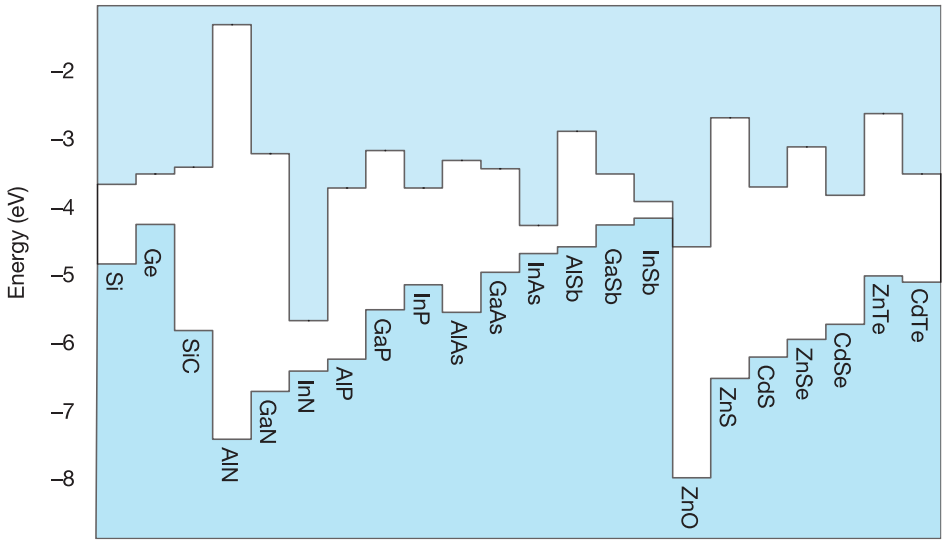


Fig. 1.4: Band energy comparison of the most common semiconductors - replotted from [28].

InN has a Wurtzite crystal structure which is energetically favored over cubic (zinc blende) nitride structure. Unfortunately, as other nitride semiconductors, InN's lattice constants (a = 3.5446 Å, c = 5.7034 Å [33]) differ significantly from other semiconductors, and lattice-matched substrates are very difficult to find. Because of lattice mismatch, there will be tensile strain on the nitride, and it will be impossible to grow layers of InN on substrates without forming dislocations.

These dislocations will act as carrier traps and have a negative impact on interband tunneling, electron mobility, and current density.

One way to overcome lattice mismatch is by growing the InN as nanowires. Due to the merit of effective lateral strain relaxation in nanowires, lattice-mismatch is no longer a problem, and high purity nanowires with low structural defect densities can easily be grown on various substrates. The most appealing of substrates is Si, due to its aforementioned ideal band alignment with InN, and the growth of high quality, defect-free InN nanowires of various doping concentrations on Si substrates has already been demonstrated [34]. The combined properties of InN and Si make the material system an ideal candidate for achieving extreme sub-threshold swings and high current density operations in TFETs to compete with MOS based transistors and improve the energy efficiency of electronics.

1.4 Original Contributions and Thesis Organization

This thesis explores the tunneling properties of the InN/Si material system for the first time, in order to solve one of the most important technological challenges in electronics. Through numerical modeling software "APSYS", we investigate the interband tunneling in a simple p-Si/n-InN Esaki diode, and expand the concept to fully investigating an Si/InN nanowire TFET.

After successful numerical modeling, the transfer characteristics of the p-Si/n-InN Esaki diode are examined in a custom built nanoprobe setup in our lab at McGill University. The nanowires themselves are grown by molecular beam epitaxy (MBE) by our collaborator Professor Zetian Mi and his group at McGill

University. We also examine the tunneling behavior of p-InN/n-InN Esaki diodes and compare the homostructure to simulations.

Contributions of our work to the field of electronics include:

1. Modeling of p-Si/n-InN junctions and demonstrating through numerical simulations for the first time that ideal Esaki diode behavior can be achieved, with a large resonant tunneling current ($\sim$ 6 kA/cm ^{2}) at small bias voltage ($\sim$ 35 mV).

2. Designing and modeling an InN/Si TFET through APSYS and demonstrating its potential to compete with MOS transistors and improve the energy efficiency of electronics. Through the numerical simulations, the InN/Si TFET exhibits sub-threshold voltage swings below 8 mV/decade over five decades and current densities exceeding 1 kA/cm^2 at low operating voltages.

3. Measuring the transfer characteristics of high quality n-InN nanowires on a p-Si substrate grown by MBE with a custom built nanoprobe setup. With these measurements, tunneling currents through the junction are observed for the first time.

4. Measuring the transfer characteristics of high quality p-InN/n-InN nanowires on a n-Si substrate grown by MBE and observing tunneling current peaks exceeding 5 kA/cm^2 and peak-to-valley-current-ratios above 3.

This thesis will adopt the following structure:

Chapter 2:

Crosslight's numerical simulation program, APSYS, is introduced with an

in-depth analysis of the physical phenomena and equations that the program takes into consideration when solving for interband tunneling currents. The p-Si/n-InN diode is then investigated using the simulator and expanded upon to include the Si/InN TFET.

Chapter 3:

An explanation of the growth process of high quality InN nanowires on Si substrates using MBE and its possible limitations. The electrical transport properties of the as-grown n-InN nanowires on Si are then investigated and compared to the numerical simulations.

Chapter 4:

Numerical simulations and electrical measurements of homostructure InN nanowires are presented, analyzed, and compared.

Chapter 5:

A synopsis of the work is presented which summarizes the findings and contributions demonstrated in the thesis. Future work for improving the tunneling current in the InN nanowires is also discussed including low temperature measurements and better growth techniques. The details of expanding the Esaki structure and fabricating an InN/Si TFET are also outlined.

Chapter 2

Numerical Simulations of Interband Tunneling in InN/Si junctions

2.1 Simulating with Crosslight

With InN's promising properties for barrier transparency and the ideal band alignment between Si and InN already established, the tunneling behavior between the two materials needs to be examined. The In/Si junction is studied using Crosslight's Advanced Physical Models of Semiconductor Devices (APSYS) simulation package. APSYS's simulators are based on finite element analysis in 2 dimensions and offer a very flexible simulation environment for modern semiconductor devices [35]. They involve a large number of sophisticated physical and numerical models.

For interband tunneling, the simulator first solves the tunneling probability T_{WKB} of an electron at energy E, within the WKB approximation, shown in Eq. 1.4. Once the carriers have tunneled through, they drift in the presence of an

electric field and can result in impact ionization. Consequently, the software also includes both drift-diffusion and impact ionization when solving for the current across the junction [35].

Based on the tunneling probability and the applied electric field, the simulator solves for the differential tunneling current density dI/A through the junction, where dI/A = (tunneling flux) × (probability of tunneling) × (volume).

If the electron tunnels across the junction at energy E, the tunneling flux per unit volume is [35]:

$$\Phi = \frac{q^2 F m^*}{2\pi^2 \hbar^3} f_E(E)(1 - f'_E(E))dE \tag{2.1}$$

where F is the electric field across the junction, $f_E(E)$ is the Fermi function. The $(1 - f'_E(E))$ is the probability that the final electron state for the tunneling process is unoccupied [35]. As a result, the differential tunneling current density across a junction is [35] :

$$dI/A = T_{WKB} \times \frac{q^2 F m^*}{2\pi^2 \hbar^3} f_E(E)(1 - f'_E(E))dEdx \tag{2.2}$$

The simulator's model for interband tunneling works very well in calculating the tunneling currents flowing through an ideal junction. Unfortunately, it does not take into consideration significant non-idealities that may occur in the actual device, such as trap-assisted tunneling from impurities, defects and dislocations at the junction, or phonon tunneling due to electron-phonon scattering (Fig.2.1). The model also fails to account Urbach band tails that may result from heavy doping. Despite not including these phenomena, the model that APSYS uses for

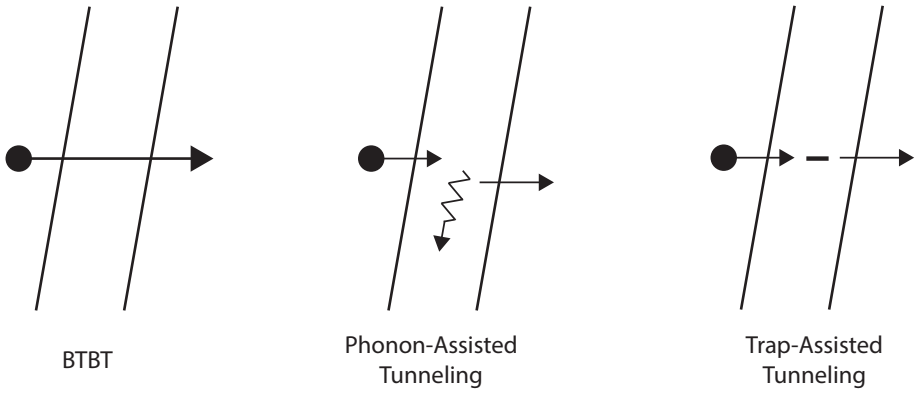


Fig. 2.1: The ideal BTBT current is modified by mechanisms such as phonon-assisted tunnelling and trap-assisted tunneling.

tunneling is sufficient when considering an idealized model. It is important to note that Crosslight has notified us that the contribution of each phenomenon to BTBT tunneling currents will be included in the near future, and a more realistic model can be studied.

2.2 Simulating a p-Si/n-InN Esaki Diode

Through APSYS, BTBT tunneling is first investigated in an n-InN nanowire on a p-doped silicon substrate. The InN nanowire is 500 nm in width and 1 μm in length - similar to the nanowires grown by MBE by our collaborators [34]. The n-doping concentration of the nanowire is 10^{19} cm^{-3}, while the silicon substrate's resistivity is 2mΩ.cm, equivalent to a p-doping concentration of 5.6×10^{19} cm^{-3}. An illustration of the device simulated is shown in Fig. 2.2(a). Ohmic contacts are placed on both sides of the diode.

In order to run the simulation, a finite element mesh is used based on the

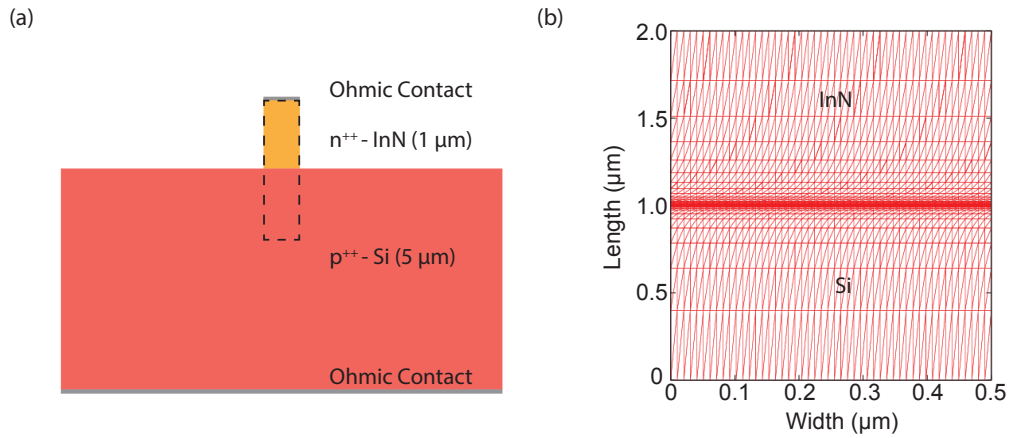


Fig. 2.2: (a) An illustration of n-InN nanowire on a p-Si substrate examined with APSYS. (b) Closeup of the meshing at InN/Si interface in the dashed region.

geometry of the device. Since the most interesting physics occur at the interface between the Si and InN, the meshing is set to become more fine towards that junction. A representation of the generated meshing used for the diode near the interface is shown in Fig. 2.2(b), and a more detailed explanation of the simulation parameters can be found in the Appendix.

After setting up the mesh of the device, the simulation is set to ambient conditions, and the current density J_{SD} of the diode is solved for, as a function of applied bias V_{SD} across the junction. The diode exhibits typical Esaki tunneling behavior with the transfer characteristics shown in Fig. 2.3. As expected, at equilibrium (no bias between source and drain), the conduction band of the InN lies below the valence band of the silicon (Fig. 2.4 (b)). A depletion region in the diode is non-existent due to the band misalignment between the two materials, as well as the high doping concentrations.

Under normal forward bias operation, there is no noticeable forward current injection, since there is a high potential barrier between the Si and InN. How-

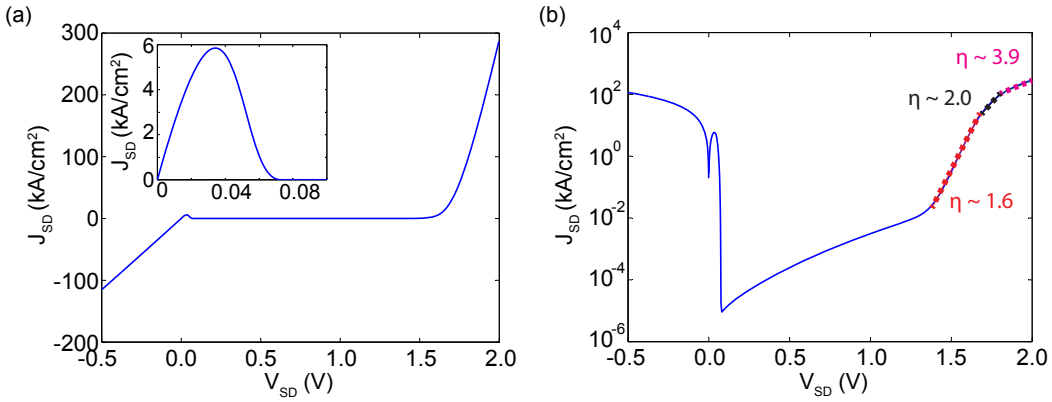


Fig. 2.3: (a)The IV transfer characteristics of the p-Si/n-InN Esaki diode through simulation. The inset is a zoom-up of the tunneling peak for clarity. (b) A semi-logarithmic plot of the transfer characteristics of the same Esaki diode. The ideality factors at different regions under normal operating behavior are also shown.

ever, electrons in the n-doped region tunnel into the empty states of the valence band and create a tunneling current. The higher the bias voltage, or the electrical field, the more carriers will tunnel, resulting in a higher current density. As the forward bias continues to increase, the energy overlap between the conduction band of InN and the valence band of Si decreases. Consequently, the tunneling probability decreases, less electrons are available to tunnel, and as a result, the tunneling current starts to decrease until no tunneling occurs. This causes two prominent features in any Esaki diode, a peak tunneling current and a negative differential resistance (NDR) region (shown in the inset of Fig. 2.3 (a)), and they present an ideal platform to characterize the device. The peak-to-valley current ratio (PVCR) and the peak current density (PCD) are the figures of merits used to evaluate the quality of the junction.

For this modeled diode, a tunneling peak current density of $\sim$ 5.8 kA/cm^2 is observed and is of the same order of magnitude compared to the best Esaki

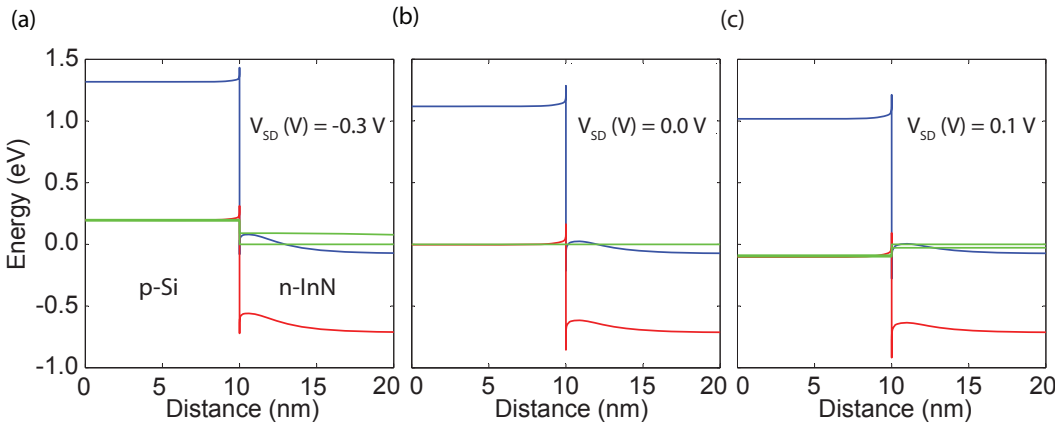


Fig. 2.4: The band energy diagram of the p-Si/n-InN Esaki diode with the valence band (red), conduction band (blue), and electron and hole quasi Fermi levels (green), at a voltage bias of (a) -0.3 V, (b) 0 V, and (c) 0.1 V.

nanowire diodes reported in the literature [36, 37, 38, 39, 40, 41]. This peak appears at a very low voltage bias, ~ 35 mV. The most impressive feature observed during the simulation is a PVCR exceeding 10^5 and is several order of magnitudes higher than the best ratios reported in literature (< 10) [40]. However, non-idealities such as trap-assisted tunneling, phonon tunneling, and Urbach tails will degrade our simulated ratio. Nevertheless, the BTBT effects are impressive and promising for InN/Si based TFETs.

In looking at Fig. 2.3, after applying enough voltage bias in the forward direction, the diode operates similarly to a normal diode, and forward injection currents dominate. Due to the band difference between the Si and InN, the turn-on voltage of the diode does not occur until around ~ 1.35 V. Between the two operating regions, tunneling and forward injection, recombination currents are observed. When the diode does turn on, it initially behaves ideally under Shockley's diode equation [42]:

$$I = I_0(e^{qV_{SD}/nKT} - 1) \tag{2.3}$$

where I_0 is the reverse bias saturation current, and n is the ideality factor, which typically varies from 1 to 2; for this particular case, n is ~ 1.55. However, by gradually increasing the voltage to ~ 1.65 V, high injection effects start to limit the diode current, and n becomes ~ 2. High injection occurs when the injected minority carrier density exceeds the doping density [42]. By further increasing the voltage, the series resistance of the junction limits the current even more, and the ideality factor exceeds 2.

On the other hand, under a reverse voltage bias, the junction reverts to interband tunneling. By gradually increasing the voltage, the energy bands of the InN are continuously lowered with respect to the bands of Si (Fig. 2.4(a)), and more electrons are available to tunnel. Consequently, the current density continues to increase with respect to the applied voltage in a linear fashion, with a tunneling current density ~ 120 kA/cm^2 at a reverse bias of -0.5 V. The linear behavior under reverse bias is a prominent feature in tunneling junctions and is sometimes taken advantage of as quasi-Ohmic contacts in multi-junction photovoltaics [43].

2.2.1 The Effects of Doping Concentrations on the Tunneling Current

The doping concentration of both the p and n regions has an effect on the Fermi levels of both materials in the junction, and consequently on how their energy bands align. This plays a significant role in the tunneling current where the effect is investigated in more detail through the simulator. While keeping the Si resistivity at 2 mΩ.cm (5.6×10^{19} cm^{-3}), different n-doping concentrations of

the InN nanowire are explored; Fig. 2.5 shows the transfer characteristics of these wires. With more n-dopants, the InN's Fermi level is raised, and consequently, its energy bands are lowered even further with respect to that of the Si at equilibrium (Fig. 2.6). As a result, more voltage is required to push the conduction band of the InN above that of the valence band of Si, resulting in the peak tunneling current density to occur at higher bias. Furthermore, with more carriers available to tunnel, a higher peak current density is observed. At higher voltage biases, under normal diode operation, diffusion currents dominate, and lower turn-on voltages are observed for higher doping concentrations.

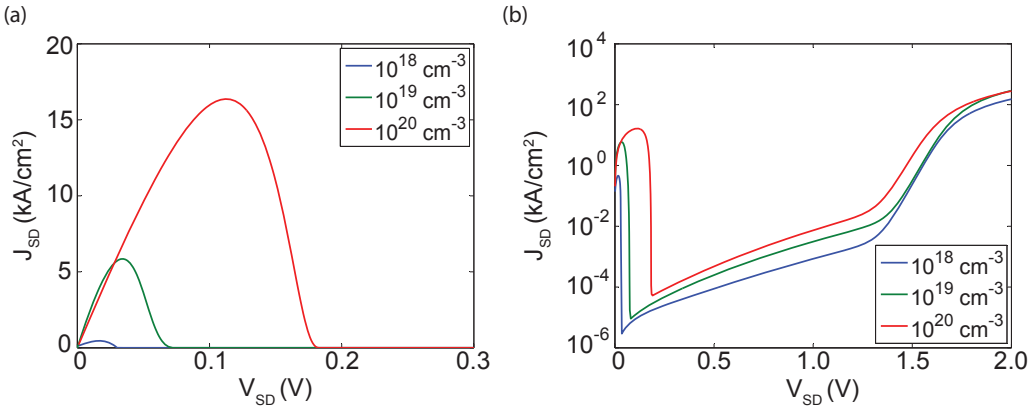


Fig. 2.5: (a) The tunneling current density peaks and (b) a semi-logarithmic plot of the current densities of the p-Si/n-InN Esaki diode at different doping concentrations of InN, while maintaining the Si resistivity at 2mΩ.cm.

A similar behavior can be observed by varying the doping concentration of the Si while keeping the n-doped concentration of the InN constant at 10^{19} cm^{-3} (Fig.2.7). Higher doping concentrations in the p-region lower the Fermi level below the valence band at equilibrium, and a band alignment more suitable for tunneling is observed. As a result, higher tunneling peak densities occur at higher

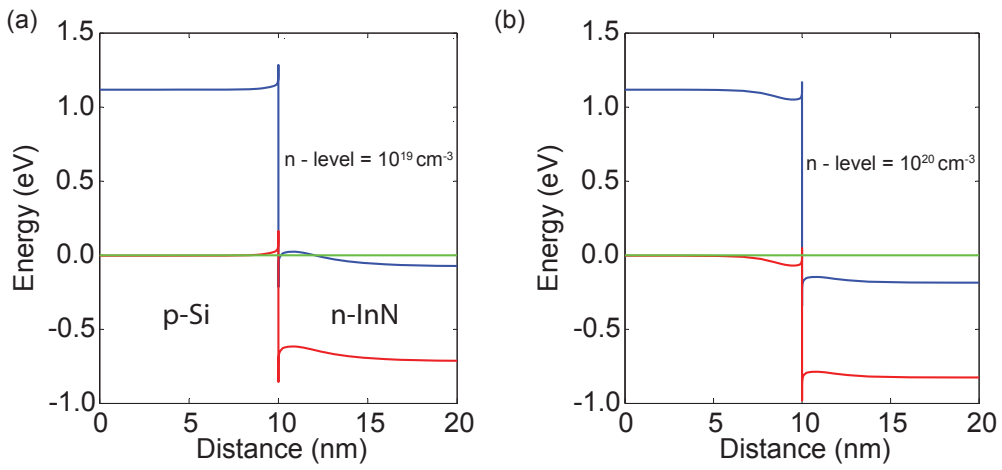


Fig. 2.6: The band diagram of the p-Si/n-InN Esaki junction at zero bias with the InN doping concentration at (a) 10^{19} cm^{-3} and (b) 10^{20} cm^{-3}, while maintaining the Si resistivity at 2mΩ.cm.

bias voltages. However, the higher Si doping concentrations lead to significant band bending of the InN near the interface, and under normal bias operation, higher turn-on voltages are required to overcome that barrier.

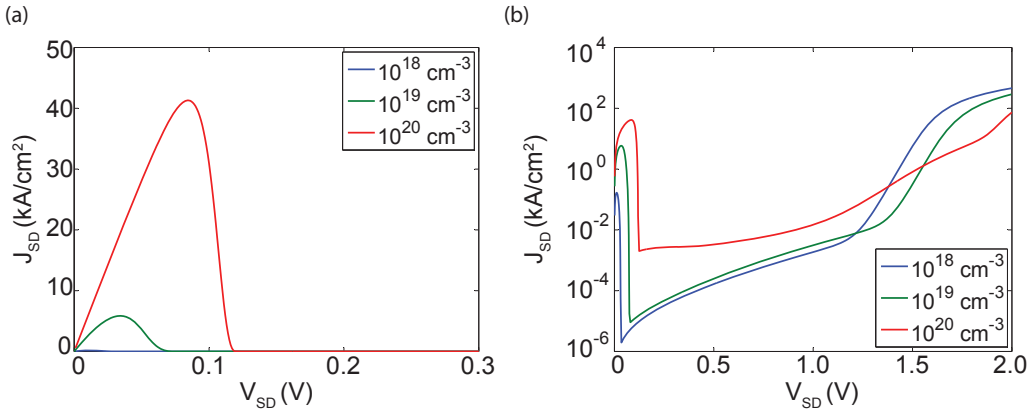


Fig. 2.7: (a) The tunneling current density peaks and (b) a semi-logarithmic plot of the current densities of the p-Si/n-InN Esaki diode at different doping concentrations of Si, while maintaining the doping concentration of InN at 10^{19} cm^{-3}.

2.2.2 The Effects of Temperature on the Tunneling Current

Temperature usually has a significant effect on physical phenomena, and it is important to study its effects on the interband tunneling of charge carriers, and consequently the tunneling current density. In reviewing the definition of the tunneling current density (Eq. (2.2)), both the Fermi function $f_E(E)$ and the band gap E_g show a dependence on temperature. The temperature dependence of E_g is usually determined experimentally and can be described by Varshni's empirical expression [44]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{2.4}$$

where $E_g(0)$ is the band gap at 0 K, and α and β are fitting parameters. However, the temperature dependence is very weak for most semiconductors and is not taken into consideration by the simulator. As for the Fermi function $f_E(E)$, it varies with temperature as follows [45]:

$$f_E(E) = \frac{1}{e^{(E-E_F)/kT)}+1} \tag{2.5}$$

However, in most cases $(f_E(E) - f'_E(E))$ can be approximated to one, and consequently, the tunneling current density is relatively independent of temperature [35]. Nevertheless, the simulator is run at different temperatures to investigate the effects of the temperature on the tunneling current through the p-Si/n-InN diode. Throughout this set of simulations, the doping of Si and InN is kept at 5.6×10^{19} and 1×10^{19} cm^{-3} respectively. Fig. 2.8 shows the tunneling current densities at temperatures ranging from 50 K to 350 K. It is important to note that the

meshing of the device is made slightly coarser than shown in Fig. 2.2 due to convergence problems at lower temperatures.

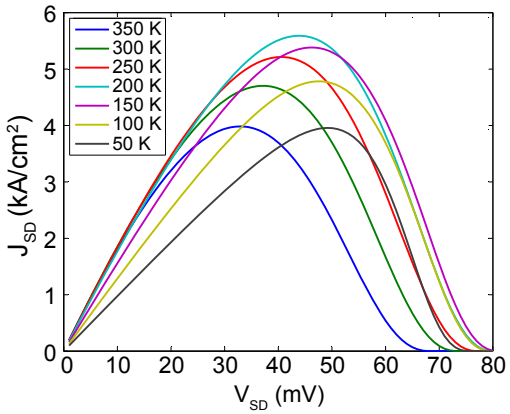


Fig. 2.8: The tunneling current density peaks of the p-Si/n-InN Esaki diode at different temperatures.

Although the tunneling current density shows little dependence on temperature, the peak increases with higher temperature until 200 K, where the current density peak drops for higher temperatures. This phenomena may be attributed to the effect of temperature on the mobility of carriers. At lower temperatures, the mobility decreases by $T^{3/2}$ due to ionized impurity scattering; while at higher temperatures, the mobility decreases by $T^{-3/2}$ due to phonon scattering, and as a result, the actual mobility reaches a maximum at an intermediate temperature [45]. Since the current depends on the mobility of the carriers, a similar effect with respect to temperature is observed.

2.3 Designing and Optimizing a p-Si/n-InN TFET with APSYS

The earlier simulations on the p-Si/n-InN Esaki diode have laid the ground work for designing a Si/InN TFET and have shown that the material combina-

tion is ideal for interband tunneling. It is important to expand upon the concept of the diode by designing InN/Si TFET structures with emphasis on optimization for sub-threshold swing <60 mV/decade over several decades, and on-current density exceeding 1 kA/cm^2. In order to achieve this performance, the InN/Si channel must be carefully designed through APSYS for efficient electrostatic coupling - to minimize short-channel effects - and a minimum tunneling length for efficient BTBT.

After trying many designs with the simulator, an optimum TFET was found and is depicted in Fig. 2.9(a). As with the Esaki diode discussed earlier, a p-doped Si substrate with 2mΩ.cm resistivity is used as the source of the device, while a 0.5 μm thick, 1 μm long n-InN nanowire with a doping concentration of 10^{19} cm^{-3} acting as the drain. The channel of the TFET is a 0.8 μm long, p-doped (5×10^{17} cm^{-3}) InN nanowire. The doping and the length of the channel are carefully chosen to ensure optimum performance. The reasons behind these choices will be explained later in this chapter.

In the ideal scenario, a wrap-around gate should be used to optimize the electrostatic TFET design, minimizing parasitic capacitance from channel to source (and drain) in comparison with the gate-channel capacitance, and thereby minimizing deleterious short channel effects. However, due to convergence issues with the simulator, only one side of the channel is gated. To capture the full effect of the gate modulation on the channel, the nanowire thickness is halved to 0.25 μm. A 3 nm thick hafnium oxide HfO_2 is used as the gate insulator due to its high dielectric constant K ($\sim$ 25). A high K dielectric is important to reduce the gate-channel capacitance C_{ox} [46].

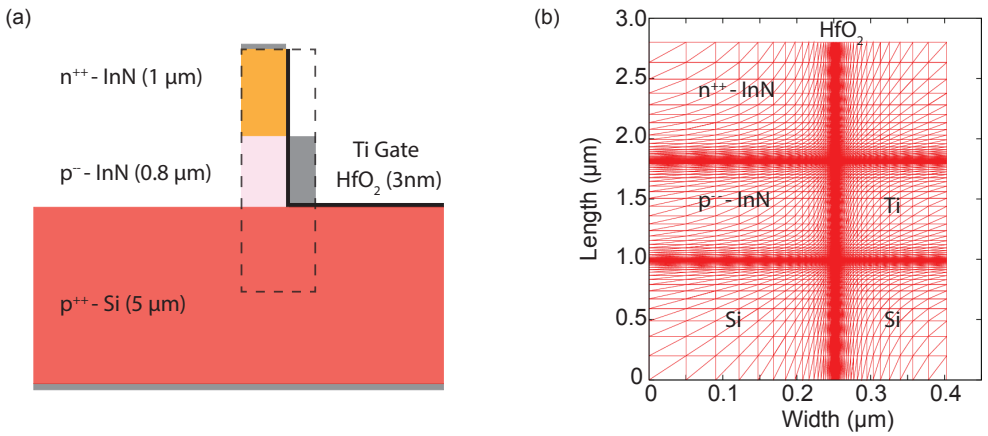


Fig. 2.9: (a) An illustration of n-InN/p-InN/p-Si TFET with a Ti/HfO_2 gate to modulate the channel examined with APSYS. (b) A closeup of the meshing near the InN/Si channel highlighted by the dashed region.

$$C_{ox} = K\epsilon_0 A/t \tag{2.6}$$

where ϵ_0 is the permittivity of free space, A is the capacitor area, and t is the oxide thickness. For the gate, a 40 nm thick titanium Ti contact is used.

To simulate the device, a finite element mesh is used for the numerical modeling with the mesh becoming more fine towards the gate-channel interface, as well as the p-Si/p-InN and p-InN/n-InN junctions. A representation of the mesh generated by the simulator is shown in Fig. 2.9 (b).

After setting up the parameters, the source-drain bias is set to voltages ranging from 0.01 V to 0.05 V, and the gate-source voltage is swept from 0 to 2 V. The transfer characteristics of the TFET is shown in Fig. 2.10(a); similar to CMOS transistors, the TFET exhibits sub-threshold, triode, and saturation regions.

At equilibrium, with no voltage applied to the device, the channel acts as a tunneling barrier (Fig. 2.11(a)). When a source-drain voltage bias is applied, the

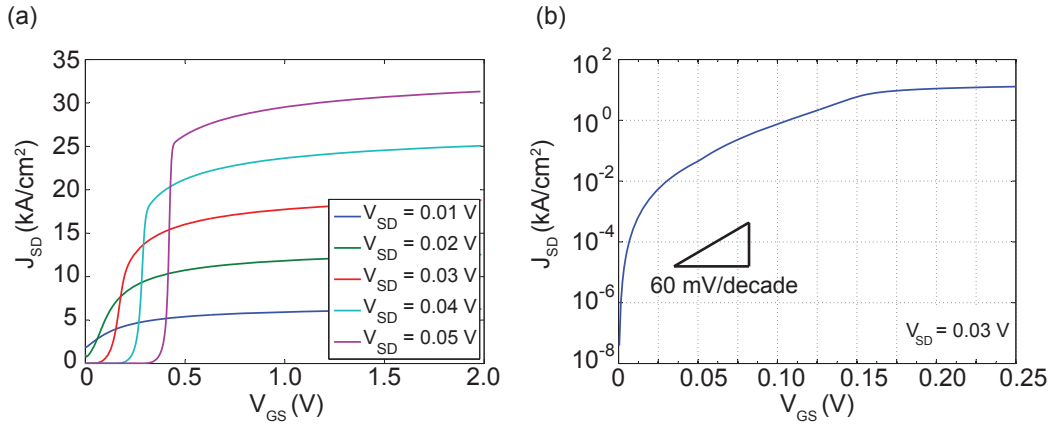


Fig. 2.10: (a) The transfer characteristics of the TFET with respect to gate voltages at different source-drain voltage biases. (b) A semi-logarithmic plot of the drain current density at a source-drain bias of 0.03 V.

energy bands of the channel are raised, further decreasing the tunneling probability (Fig. 2.11(b)). By applying a gate voltage, the channel's energy bands are slowly lowered, enabling tunneling and switching the transistor from the cut-off region into the triode (Fig. 2.11(c)). When enough gate voltage is applied, and the channel's energy bands are lower than that of Si, the tunneling current saturates.

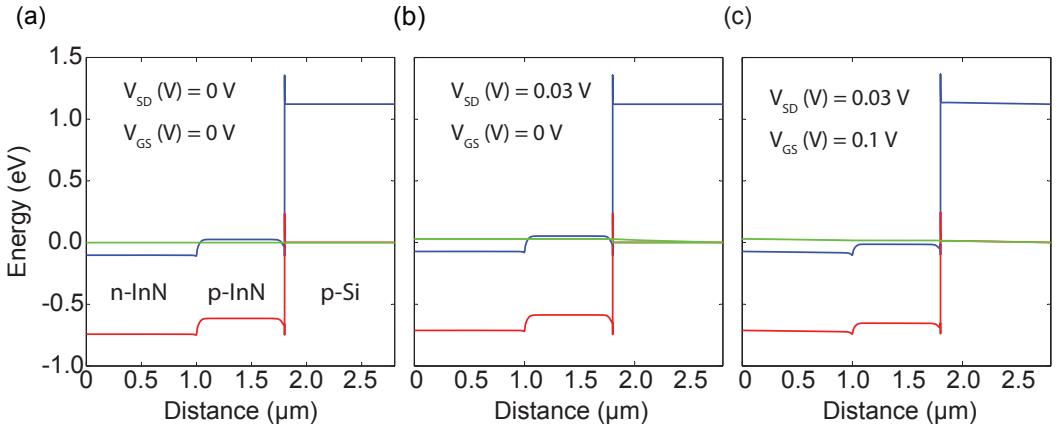


Fig. 2.11: The band diagram of the n-InN/p-InN/p-Si TFET at (a) V_{SD}, V_{GS} = 0 V, (b) V_{SD} = 0.03 V, V_{GS} = 0 V, and (c) V_{SD} = 0.03 V, V_{GS} = 1 V.

For the designed TFET, very low biases (0.01 V) and gate voltages (< 0.3 V) are required to achieve saturation currents exceeding 1 kA/cm^2; this is significantly better than the best MOS based transistors, and a step forward in the quest to more energy efficient switches. As explained earlier though, the key reason for the ulra-low operating voltages is the TFETs' S. Fig. 2.10(b) shows a semi-logarithmic plot of the current density with respect to gate voltage. The sub-threshold voltage swing of the In/Si TFET is significantly below the thermionic limit, with $S < 8$ mV /decade over five decades of current. Furthermore, the low S added to the high on-currents lead to I_{ON}/I_{OFF} current ratios exceeding 10^7. The combination of these factors lead us to hypothesize for an optimistic future for InN based TFETs.

2.3.1 The Doping Concentration of the Channel

As mentioned previously, the doping of the channel has to be chosen carefully to ensure optimum operation. The doping of the channel has an effect on Fermi level, and consequently the alignment of the energy bands of the channel with respect to both the source and drain. In essence, the doping of the channel modulates the barrier in the same manner the gate can modulate it. Even small changes to the doping levels can have drastic effects on the transfer characteristics of the device, as shown in Fig. 2.12. By reducing the p-doping concentration from the optimum 5×10^{19} cm^{-3} to 4×10^{19} cm^{-3}, the energy of the barrier is lowered to allow significant tunneling current without a gate voltage. As a result, the I_{ON}/I_{OFF} current ratio is extremely hampered and is not viable for a CMOS alternative. On the other hand, by increasing the p-doping of the channel to just

8×10^{19} cm^{-3}, the energy bands of the barrier are increased, and a higher gate voltage is required to turn the transistor on; this defeats the entire purpose behind the TFET.

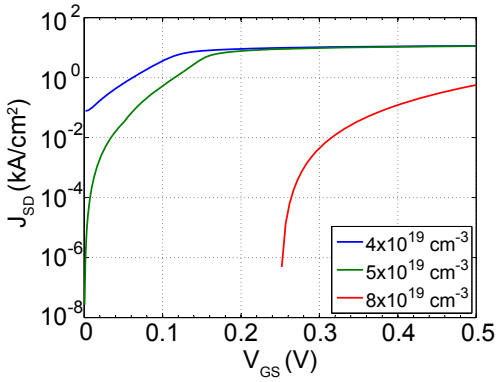


Fig. 2.12: Semi-logarithmic plot of the TFET current density with respect to gate voltage at $V_{SD} = 0.03$ V with changes in the p-InN channel doping concentrations.

2.3.2 The Length of the Channel

The length of the channel also plays a vital role in the behavior of the TFET. The length of the energy barrier created by the channel has a significant effect on the transmission probability of the carriers, and hence on the BTBT tunneling. A shorter channel leads to a higher T_{WKB}, and consequently, a higher tunneling current density (shown in Fig. 2.13). However, a shorter channel is not always the best option; if the channel is too short (0.7 μm), a significant amount of carriers can tunnel through without applying gate voltage, leading to lower I_{ON}/I_{OFF} current ratios.

Compromises between current ratios and operating voltages are always required when designing and optimizing a TFET, or any other electronic device.

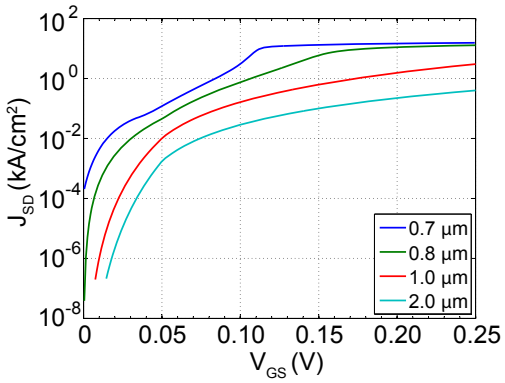


Fig. 2.13: Semi-logarithmic plot of the TFET current density with respect to gate voltage V_{SD} = 0.03 V with changes in the length of the p-InN channel.

Nevertheless, the designed TFET still exhibits both excellent current ratios and very low operating voltages.

In this chapter, we investigated the interband tunneling effects in an idealized model of a p-Si/n-InN junction with APSYS. The model showed high interband tunneling current densities and a tunneling current density peak of 5.8 kA/cm^2 at ~ 35 mV. A Si/InN TFET was also designed with the software and optimized to exhibit S below 8 mV/decade over 5 decades, as well as high on current densities (> 1 kA/cm^2) at very low operating voltages. Both models have shown the potential of interband tunneling in InN and the exciting prospect of using the material in low voltage transistors.

Chapter 3

Electrical Transport Measurements in p-Si/n-InN Esaki Diodes

After exploring the theory behind interband tunneling and demonstrating the ideality of p-Si/n-InN junction for interband tunneling through simulations, this chapter will explore the growth process of InN nanowires on p-Si substrates and the electrical transport measurements of the diodes.

3.1 Growing InN nanowires on Si substrates

Depending on the application, there is a very wide range of techniques to grow group III-nitride nanowires, but molecular beam epitaxy (MBE) growth is the most favorable due to the unprecedented approach for controlling the interface properties of nanoscale heterostructures. The most established method of growing nanowires through MBE is based on the now well-known vapor-liquid-solid (VLS) mechanism.

3.1.1 The Vapor-Liquid-Solid Mechanism

The VLS mechanism was established almost 50 years ago by Wagner and Ellis (1964) in the growth of Si whiskers of micron sizes [47]. The directional growth of a single crystal relies on the initial existence of a catalyst - very often metallic particles such as Au. The catalyst nanoparticles are dispersed on the required substrate, and the semiconductor is then supplied in vapor phase. The adsorption of the semiconductor in vapor form into the metal particles significantly lowers the melting point of semiconductor-metal alloy, such that the alloy forms droplets at a moderately elevated temperature on the substrate. With the continuous provision of semiconductor in vapor phase, the adsorption on to the alloy droplets leads to super-saturation. The resulting precipitation leads to the initial growth of solid wires along a preferential crystal direction, leaving the liquid alloy droplets largely intact [48].

Over the years, the VLS mechanism has developed greatly, with a wide range of materials being grown on substrates with relative ease. One disadvantage of VLS is that foreign metal catalysts usually diffuse into the semiconductor nanowires and serve as deep trap centers significantly affecting their electrical properties. To solve this issue, catalyst-free techniques based on the VLS mechanism were developed to improve the material purity, and hence the electrical properties of nanowires [34].

3.1.2 Unique Self-Catalytic Process

Despite the improvements in the VLS mechanisim or any other growth process, growing III-N nanowires, especially InN faces many problems. The InN

nanowires grown by the prevalent methods exhibit uncontrolled tapered surface morphology, and therefore poor electrical and optical properties. Yet, the biggest challenge with growing InN nanowires is the difficulty in doping, especially p-type doping. The conduction band minimum of InN lies ~ 1.2 eV below the charge neutrality level [28]; therefore, any defect or impurity will behave as a donor, leading to extremely high electron densities even in undoped structures [32].

Recently however, the growth of high-purity InN nanowires on Si substrates, with unprecedented control over doping, has been grown by our collaborators at McGill University using a unique self-catalytic growth process [32, 49]. Utilizing an *in situ* deposited In seeding layer, non-tapered intrinsic, n-type, and p-type InN nanowires are demonstrated, for the first time, with controlled electrical transport and surface charge properties (Fig. 3.1) [32, 49].

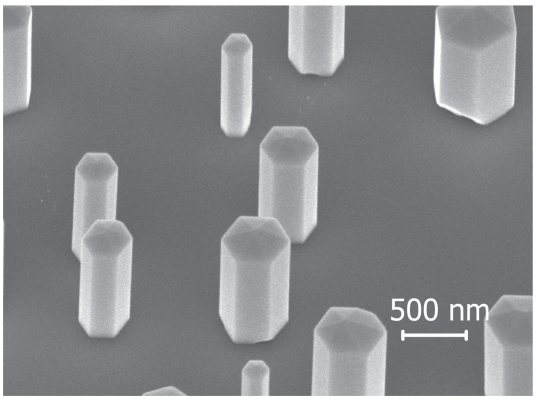


Fig. 3.1: SEM image of nontapered undoped InN nanowires grown on Si (111) substrate with diameters ~ 0.5 μm and lengths ~ 0.7 μm [32].

The InN nanowires are grown on a Si(111) substrate by radio frequency plasma-assisted MBE under nitrogen-rich conditions. Before introducing the nitrogen, a thin (~ 0.6 nm) In seeding layer is deposited on the Si substrate. At

high enough temperatures, the In seeding layer forms nanoscale droplets and promote the formation and nucleation of InN nanowires. The necessary conditions for the growth of the InN naowires include a substrate temperature of ~ 480 °C, an In beam equivalent pressure of ~ 6×10^{-8} Torr, a nitrogn flow rate of ~ 1.0 sccm, and an RF plasma forward power of ~ 350 W [32, 49]. Silicon and magnesium are used to n-dope and p-dope the nanowires respectively. By precisely controlling the fusion cell temperatures of the Si or Mg, the dopants can be incorporated at the atomic level. This is ideally suited to realize the sharp transitions in dopant density required for TFETs. The dimensions of the nanowires are dependent on the doping concentrations and the growth duration [32].

For our Esaki diode, the nanowires are grown on 2mΩ.cm resistivity Si(111) substrates, and the n-doping is achieved by varying the Si effusion cell temperatures between ~ 1250-1350 °C to achieve doping concentrations of 10^{17}-10^{19} cm^{-3}. A summary of the different n-InN nanowire samples grown for this thesis is listed in table 3.1.

Unfortunately, with the current process for growing the InN/Si nanowire structures, a thin (~ 1-3 nm) SiN_x interlayer has been commonly observed (Fig. 3.2), which is spontaneously formed when active nitrogen species are introduced prior to the growth initiation. Little is know about the nature of the interfacial layer and whether it is amorphous or epitaxial. The exact properties of the interfacial layer are also not completely understood at the moment, but the layer can potentially act as a barrier for tunneling.

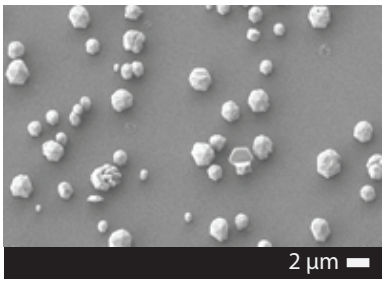
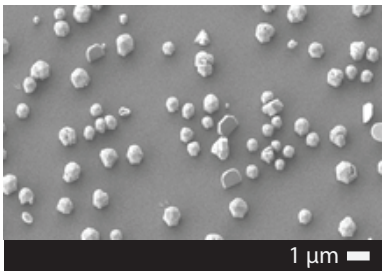
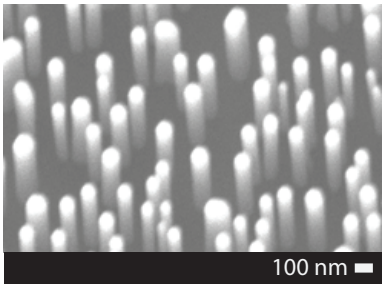
Doping	Length	Diameter	SEM Image
$\sim 10^{17}$ cm^{-3}	$\sim 1.0\ \mu$m	~ 1.00 - $3.00\ \mu$m	
$\sim 10^{18}$ cm^{-3}	$\sim 1.0\ \mu$m	~ 0.50 - $1.50\ \mu$m	
$\sim 10^{19}$ cm^{-3}	$\sim 0.5\ \mu$m	~ 0.05 - $0.15\ \mu$m	

Table 3.1: A summary of grown InN nanowires for Esaki diode.

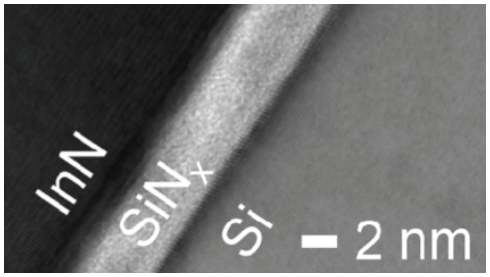


Fig. 3.2: TEM image of an InN nanowire grown on Si(111) substrates with a SiN_x interlayer.

3.2 Characterization of the InN/Si Junctions

3.2.1 Probing inside an SEM

The electrical transport properties of individual n-InN nanowires on p-Si are first measured as-grown in a scanning electron microscope (SEM) environment with the Zyvex S-100 Nanoprobe setup at the Cornell Nanoscale Facility (CNF). The S-100 consists of four individually controlled nanoprobes that can be placed with a precision of five nanometers. The probes themselves are made from tungsten and have a tip radius of fifty nanometers for precision measurements. Nanoprobe characterization of wires obviates the need for any processing following MBE growth, and thus gives the most direct window possible to the inherent electrical quality of InN/Si heterojunctions. Nanoprobe measurements have been critical to the demonstration of record electron mobilities in as-grown InN nanowires on n-type Si substrates [50].

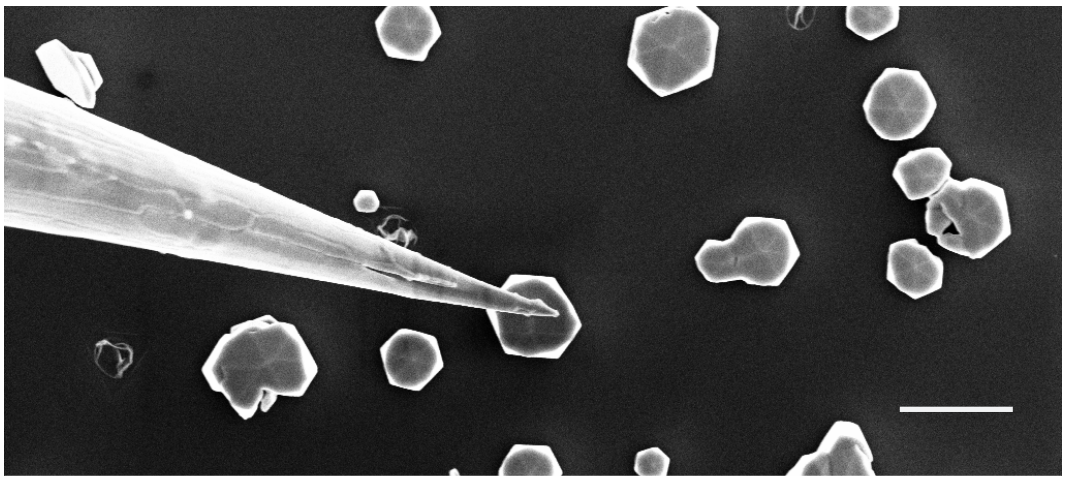


Fig. 3.3: An SEM image while probing an InN nanowire at the CNF; the scale-bar is 1 μm.

Two of the four probes are used to carry out the electrical measurements;

one is placed on top of a nanowire (Fig. 3.3), while the other is placed on the substrate. To characterize the diodes, a Keithley 4200 semiconductor characterization system is connected to the Zyvex Nanoprobes setup. The Si substrate (Source) is grounded through the probe, and the voltage across the nanowire (Drain) is swept, while measuring the current through the nanowire. Representative I-V characteristics of a 10^{18} cm^{-3} n-doped InN nanowire on a p-doped Si substrate measured using the setup is shown in Fig. 3.4.

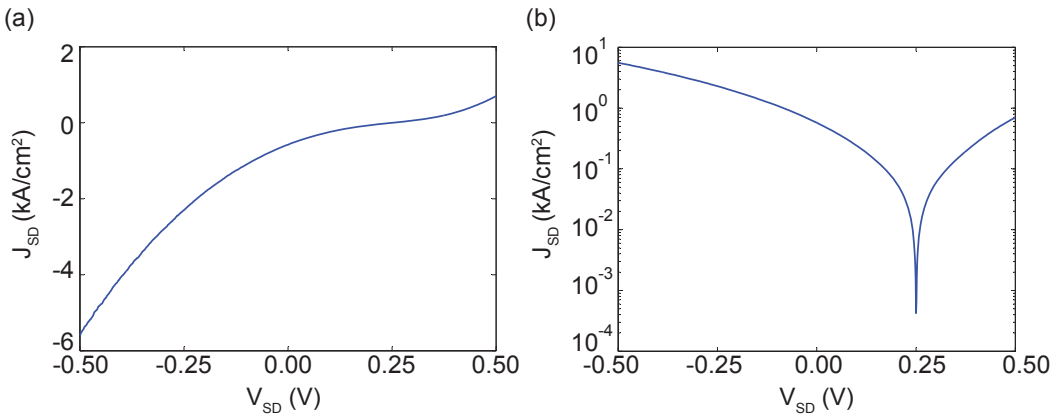


Fig. 3.4: (a) I-V characteristics of a 10^{18} cm^{-3} n-doped InN nanowire. (b) A semi-logarithmic plot of the I-V characteristics for the same nanowire.

An unexpected behavior is first observed during the electrical measurements; the InN nanowires appear photo-sensitive to the infrared lighting inside the SEM chamber, with a 0.7 kA/cm^2 current density measured at 0 V bias (see Fig. 3.4). Simulations with APSYS have later confirmed that the InN is sensitive to infrared wavelengths, and they have been demonstrated as viable near IR photodetectors by the research community [51]. Due to the high photo-currents observed, InN's IR sensitivity could have a significant impact on observing potential tunneling currents and possibly contribute to photon-assisted tunneling.

With that in mind, under forward bias, the nanowire I-V characteristics do not resemble the simulations of the Esaki diode in Chapter 2; there is neither a distinct tunneling current peak, nor a negative resistance region. As mentioned earlier, the high photo-currents might have masked any possible tunneling peak. Furthermore, the nanowire exhibits a normal diode-like behavior, with a non-linear I-V relationship at low voltage biases, unlike the required ~ 1.35 V observed in the simulations. The series resistance of the diode also appears to limit the diode current early on, with an ideality factor n of ~ 3.97 at ~ 0.4 V, and a 0.7 kA/cm^2 current density is observed at 0.5 V.

On the other hand, under reverse bias, the current density increases with voltage, unlike any normal diode or photodiode. The reverse bias current density is very similar to that observed when simulating the Esaki diode in Chapter 2, and may be attributed to interband tunneling. As shown in Fig. 3.4, a current density of 5.7 kA/cm^2 is observed at -0.5 V and is of the same order of magnitude solved during the simulations. However, it is important to note that photo-currents may be contributing to the current densities, and the actual interband tunneling currents are likely less.

Although probing the nanowires in an SEM environment is ideal for optimum viewing of the nanowires and control over the nanoprobes, conducting the measurements proved to be a big challenge. The tungsten probes available are very fragile; properly contacting these probes to nanowires is a very delicate exercise, as the probes are easily damaged when overdriven. This necessitated their frequent replacement, and as a result, the opening of the SEM's vacuum chamber, and the ensuing waiting period. Therefore, the measurement throughput was

low; only 10 nanowires were probed over 24 hours with the equipment. It was not possible to fully investigate the electrical transport properties of the p-Si/n-InN diodes with the SEM and elucidate the nature of the interband tunneling in InN or its photo-sensitivity.

3.2.2 Probing Under an Optical Microscope

After encountering difficulties while probing the nanowires in an SEM environment, we decided to custom build a relatively inexpensive nanoprobe setup in our lab at McGill University. The system is based upon a 100 X, numerical aperture $NA \sim 0.55$ optical microscope with vibration isolation, and a peizo-controlled 3-Axis NanoMax Flexure Stage to position the probe with a resolution of 20 nm.

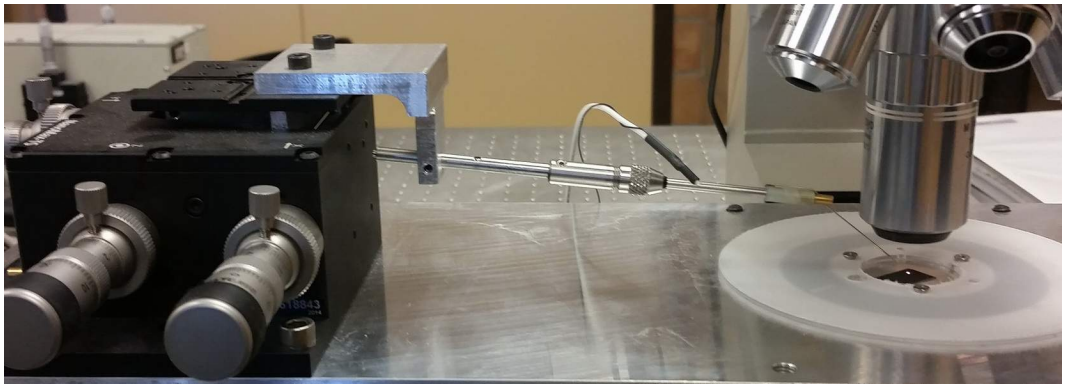


Fig. 3.5: Image of the custom built nanoprobe setup with a 3-axis stage and 100 X optical microscope.

"Cat whisker" T-4-5 tungsten probes from Picoprobe® are used to contact the nanowires; the 50 nm radius tips are soldered to the end of a 2 inch long tinned copper shaft. These tips can bow and straighten when over-driven instead of bending and breaking. Our new system is capable of high throughput

measurement of the I-V characteristics of individual nanowire devices, with over 500 nanowires exhaustively measured over a 6 month period.

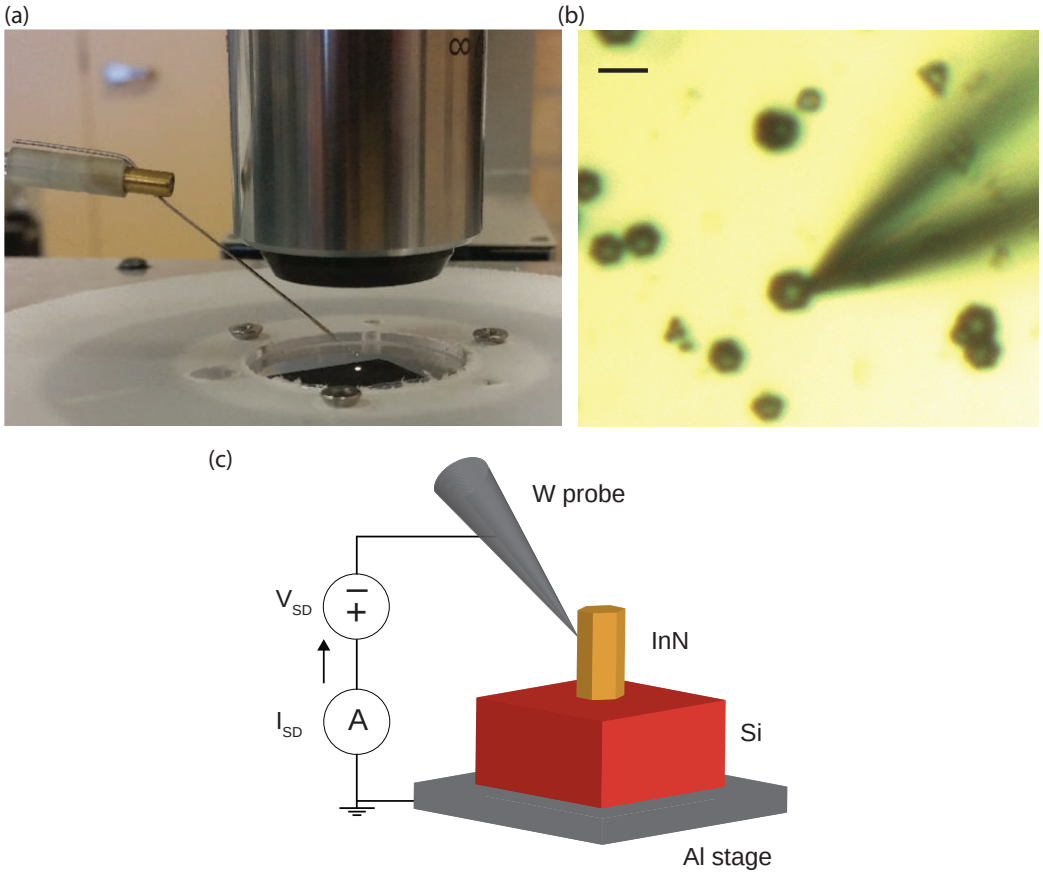


Fig. 3.6: (a) A close-up image of the setup. (b) An optical micrograph while contacting a large 10^{17} cm^{-3} nanowire; the scale-bar is 3 μm. (c) A schematic of the setup while measuring a nanowire.

To measure the electrical transport properties of the InN nanowires, the silicon substrate is grounded to a metal aluminum stage, while one probe is used to contact a nanowire. Due to the "cat whisker" nature of the probes, it is difficult to contact the top of a nanowire; instead, the probe is jammed into the side. An image and an optical micrograph while contacting a nanowire are shown in

Fig. 3.6. The current I_{SD} through the diode is measured with a semiconductor parameter analyzer (Agilent B1500A) versus the applied source drain voltage V_{SD} (Fig. 3.6(c)).

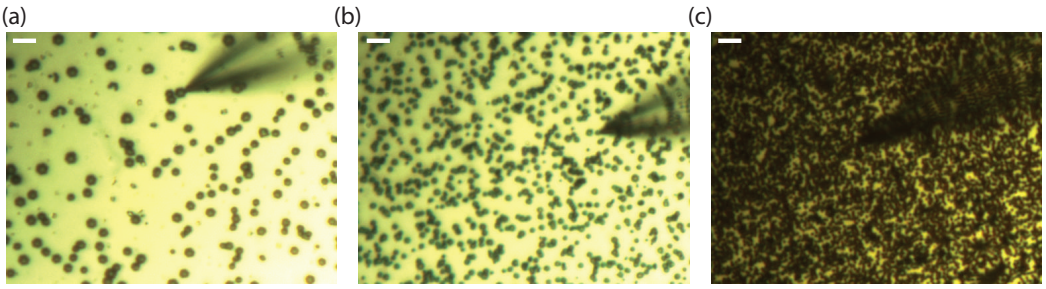


Fig. 3.7: Optical micrographs while contacting InN nanowires with a doping concentration of (a) 10^{17}, (b) 10^{18}, and (c) 10^{19} cm^{-3}. The scale-bar in all the images is 5 μm.

The electrical transport properties of all three different InN nanowire samples are thoroughly investigated and compared to the simulations. Fig. 3.7 shows optical micrographs of the different nanowires while being measured. Despite the challenges in contacting the nanowires, due to their size, as well as the optical resolution of the microscope ($\lambda/2NA \approx 500$ nm), the technique is mastered in a short period of time. However, with the limited resolution and magnification of the optical microscope, it is difficult at times to distinguish whether the nanoprobe is in contact with the Si substrate or the InN nanowire, but conducting a quick electrical measurement alleviates any uncertainty. When the probe is in contact with the Si, the measurements show a relatively linear I-V characteristic, with a $\sim 25\ \Omega$ resistance. On the other hand, when contacting a nanowire, a diode-like behavior is observed, with a non-linear I-V characteristic.

A representative sequence of an I-V characteristic of a 10^{19} cm^{-3} n-doped InN nano-wire is shown in Fig. 3.8 and compared to a simulation of the same device

on a semi-logarithmic plot. It is important to note that the dimensions of the nanowires are estimated through the optical microscope to calculate the current densities J_{SD}.

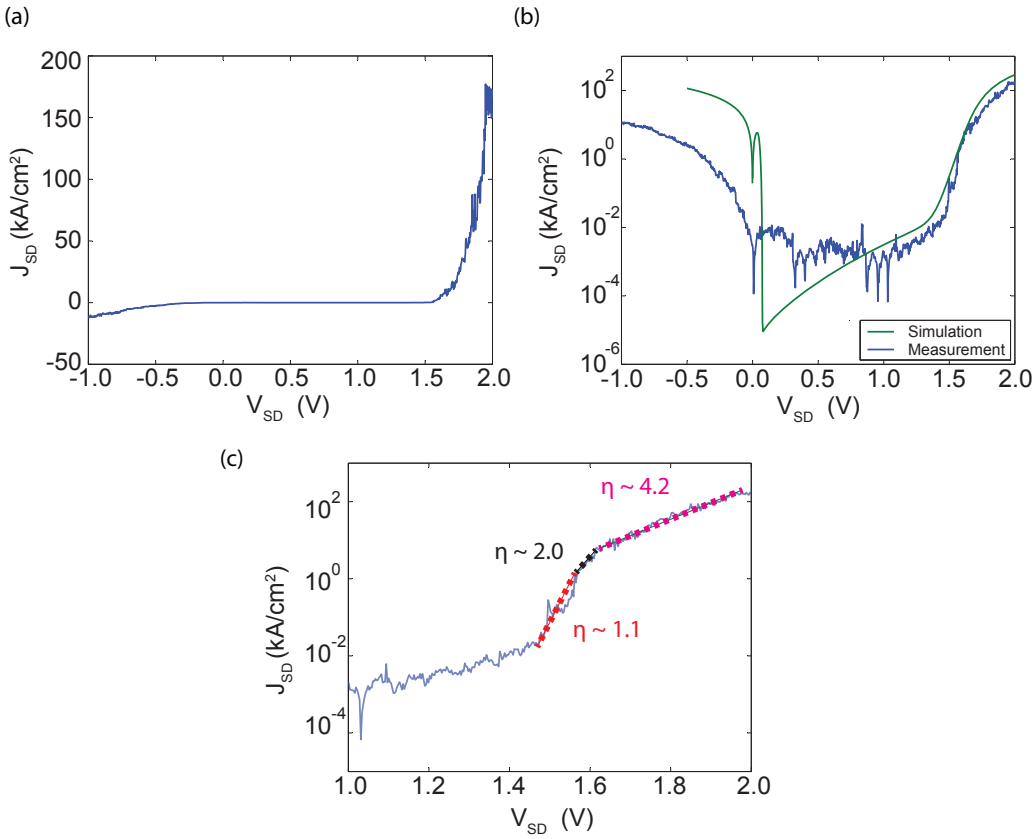


Fig. 3.8: (a) I-V characteristics of a 10^{19} cm^{-3} n-doped InN nanowire. (b) A semi-logarithmic plot comparing the I-V characteristics of the same nanowire with the simulation. (c) A close-up of the semi-logarithmic plot when the diode is under normal forward injection behavior.

Although the 10^{19} cm^{-3} n-doping of the nanowires is theoretically enough to observe the figures of merit of a typical Esaki diode, a tunneling peak and negative resistance region, none of the nanowires exhibit them. At low voltage bias, the diode appears to be turned off, with off currents ~ 1 A/cm^2 (~ 20 pA); the

high off currents appear due to a combination of noise and interference, and improved shielding is required for the setup in the future. As the voltage bias continues to increase in the forward direction, the diode behaves very similar to the simulations, and recombination currents are observed before the diode turns on at ~ 1.45 V. When the diode is on, it initially behaves ideally, with $n \sim 1.08$; however, high injection effects start to limit the current at ~ 1.6-1.65 V. Soon after, the series resistance of the diode further restricts its behavior, with $n \sim 4.21$. A current density of ~ 180 kA/cm^2 is measured at 2V.

Under reverse bias, tunneling currents through the n-InN/p-Si junction are repeatedly observed, and vary linearly with respect to the applied voltage. However, they are significantly lower than what is calculated during the numerical simulations; only ~ 12 kA/cm^2 at -1V for Fig.3.8. While the electrical measurements have shown that interband tunneling occurs through the junction, it is severely restricted, resulting in lower reverse bias current and the absence of a tunneling peak. The discrepancy between the simulations and electrical measurements is most likely attributable to the 1-3 nm SiN_x interfacial layer between the InN and Si. Since the exact nature or properties of the interfacial SiN_x are not known, especially its bandgap, it could not be included in the simulations; however, we believe, from the measurements, that the interfacial layer acts as a tunneling barrier, reduces the transmission probability of the junction, and hence, lowers the tunneling current densities. The interfacial SiN_x does not appear to have any significant effects when the diode is biased at higher voltages because it is a different mode of operation - normal forward injection. Under such behavior, carriers do not tunnel through the interfacial layer, but are injected over the

potential barrier caused by the SiN_x. With the diode turning on at ~ 1.45 V, the carriers appear to have enough energy to overcome the interfacial barrier and are not impeded by it.

Based on our measurements to date, we believe that eliminating the SiN_x interfacial layer is key to observing a tunneling peak and a negative resistance region. We have tried etching the layer with diluted hydrofluoric HF acid by placing the sample in the solution, expecting the acid to attack the layer from the sides slowly. Unfortunately, the etching had no effects on the interband tunneling. Meanwhile, our collaborators are developing special growth processes (outlined in Section 5.2) to eliminate the SiN_x without compromising the InN nanowire quality.

3.2.3 Excess Currents

The interfacial SiN_x as a tunneling barrier is not the only non-ideality encountered during the measurements; excess currents are frequently observed and contribute to the overall current through the junction. Excess currents generally occur at forward biases when the conduction band of the n-side lies between the energy bands of the p-region - the region between where BTBT and normal forward injection occurs. Electrons tunnel through part of the energy gap, making use of any present localized defect states, resulting in trap-assisted tunneling currents[27, 52]. These currents depend on the density of defect states in the bandgap and are sufficiently high in that region, considerably in excess of the normal diode current, hence the term excess current. However, since excess currents are dependent on trap-assisted tunneling, they can still be observed in

the other operating regions. Excess currents were first noted by Yajima and Esaki [53] and are observed with all Esaki diodes. They are the main limitation on the PVCR of an Esaki diode, and the reason PVCRs are below 10, even for state-of-the-art tunneling diodes [52]. Sometimes, excess currents in devices are significant enough to completely mask the tunneling peak and no longer exhibit a negative differential resistance region [41].

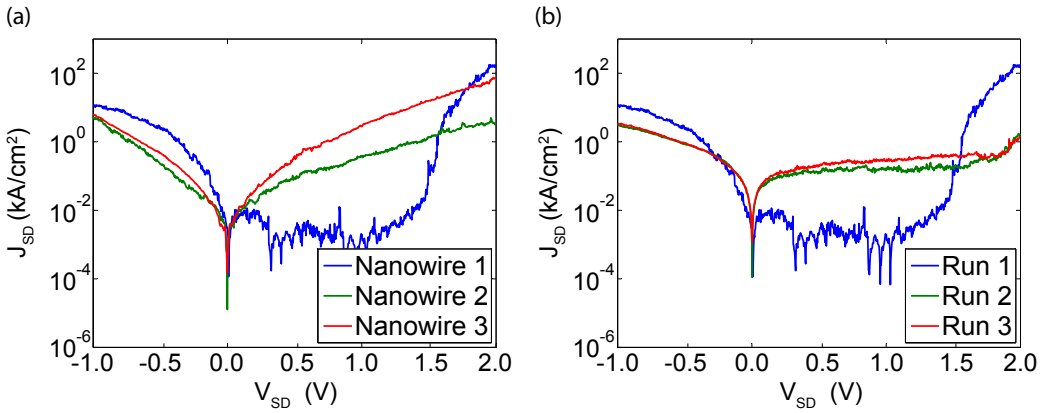


Fig. 3.9: a) A semi-logarithmic plot comparing the I-V characteristics of three different 10^{19} cm^{-3} n-doped nanowires. (b) A semi-logarithmic plot comparing the I-V characteristics of the same nanowire (Nanowire 1) in subsequent experimental runs.

Despite the high quality of our nanowires, excess currents are inevitable, especially with the unpredictable SiN_x interfacial layer. Fortunately, some of the 10^{19} cm^{-3} n-doped nanowires do not exhibit significant excess currents even when the diode is off, as evident from Fig. 3.8. However, other high doped nanowires do exhibit them and are dominant enough to affect the overall I-V characteristics of the diode. Fig. 3.9(a) compares three 10^{19} cm^{-3} n-doped nanowires; the first one being the same nanowire discussed earlier in Fig. 3.8. The reverse bias current for nanowires 2 and 3 are slightly lower than nanowire

1, and this can be attributed to slightly different doping concentrations. Consequently, the forward injection current is expected to behave similarly. However, the major point of interest is the region where the diode should supposedly be off, between 0.1 and 1.4 V. Both nanowires 2 and 3 exhibit high excess currents (> 100 A/cm ^{2}) and are significant enough to mask the normal diode behavior once the diode should turn on. Trap-assisted tunneling currents also contribute heavily to the reverse bias currents in our measurements, as they no longer depend linearly on the voltage, but rather $I \propto V^{4.5}$. The high excess currents observed may most likely be attributed to acceptor states caused by deep-level traps within the interfacial SiN_x. Conduction in SiN thin films have been commonly observed due to traps and field emission tunneling, also known as the Poole-Frenkel effect [54].

High excess currents are also observed when repeating measurements for the nanowires. Fig. 3.9(b) compares different voltage sweeps for the same nanowire (Nanowire 1). The measurements reveal that although trap-assisted tunneling is not heavily present on the first sweep, we are introducing it upon applying high voltages. After conducting the first sweep, the current measured in the off-region during the second sweep is increased by two orders of magnitude to ~ 100 A/cm^2. Fortunately however, this particular set of measurements shows that the excess currents are not high enough to fully mask the normal diode behavior, with forward injection currents dominating after 1.8 V. Subsequent sweeps still contribute to higher excess currents, but in decreasing amounts. Furthermore, reverse sweeps show no hysteresis, and it appears that there is no way to restore the original diode behavior. The introduction of trap-assisted tunneling with our

measurements may be associated with electrically stressing the nanowires and irreversibly damaging them by introducing defects at the Si/InN interface. This phenomena has been observed with Si/InAs nanowire tunneling diodes [41, 55].

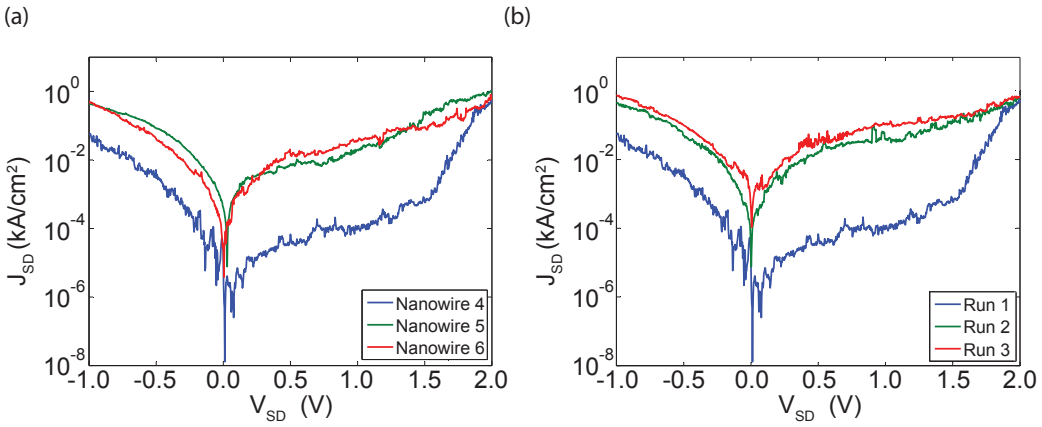


Fig. 3.10: (a) A semi-logarithmic plot comparing the I-V characteristics of three different 10^{18} cm^{-3} n-doped InN nanowires at the first time of measurements. (b) A semi-logarithmic plot comparing the I-V characteristics of the same 10^{18} cm^{-3} n-doped InN nanowire (Nanowire 4) at different times.

Excess currents are also heavily present in the lower n-doped nanowires, 10^{17} and 10^{18} cm^{-3}, with the majority displaying significant excess currents at their first time of measurement. Representative I-V characteristics of 10^{18} cm^{-3} doped nanowires are shown in Fig. 3.10 (a). Nanowire 4 exhibits an I-V characteristic similar to the simulations - minus the tunneling peak. Its reverse bias tunneling current is fairly linear, and as expected the lower doping concentrations has a noticeable effect on the current densities; 60 A/cm^2 at -1 V, and 2 orders of magnitude less than the 10^{19} cm^{-3} doped nanowires. Under forward bias, no tunneling peak is observed, and the diode is off. The diode then turns on at ~ 1.5 V and behaves normally with high injection effects limiting the current early on with an ideality factor $n \sim 2.1$ between 1.5 - 1.9 V.

The other two nanowires represent the majority of the 10^{18} cm^{-3} n-doped nanowires with significant excess currents. Just as with the higher doped InN, the excess currents are also around ~ 100 A/cm^2 in the off region and completely mask the expected diode behavior in both forward, and reverse bias. Furthermore, any diodes that do not initially display high excess currents, do so after their first sweep. Fig. 3.10 (b) compares the currents of the first 10^{18} cm^{-3} n-doped nanowire (Nanowire 4) after different voltage sweeps. Although the nanowire does not exhibit any significant trap-assisted tunneling currents initially, they do dominate in subsequent measurements, just as with the 10^{19} cm^{-3} n-doped nanowires. The induced excess currents mask any normal diode behavior and are remarkably similar to those observed during the first time measurements of the majority of the nanowires, as evident by comparing the two plots (a) and (b) in Fig.3.10. While we are unsure of the reasons behind the similarity of the excess currents, it may just be a coincidence with defects arising at the interface from the possible electrical stressing of nanowires similar in number to defects originally found in some nanowires.

Trap-assisted tunneling is also heavily present with 10^{17} cm^{-3} n-doped nanowires, and only one nanowire exhibiting low enough excess currents to allow the observance of the diode turning on. Fig. 3.11 displays a semi-logarithmic plot of the I-V characteristics of that nanowire (Nanowire 7) along with two other nanowires that represent the majority of the 10^{17} cm^{-3} n-doped nanowires. Under reverse bias, nanowire 7 exhibits low tunneling currents - only 10 A/cm^2 due to the lower doping. Under forward bias, the diode turns on at around ~ 1.3 V, but the current flow is instantly limited by the series resistance of the diode, with

an ideality factor of ~ 4.22. Nanowires 8 and 9 exhibit high excess currents with similar behavior to the higher doped ones and mask any normal behavior.

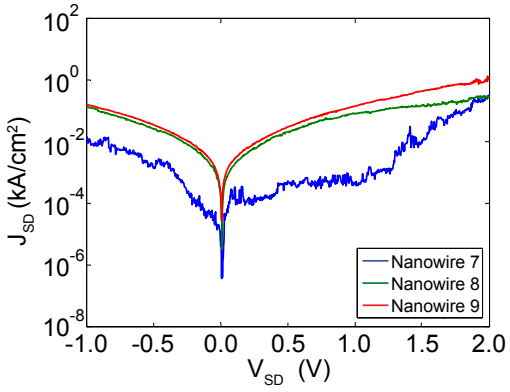


Fig. 3.11: (a) A semi-logarithmic plot comparing of the I-V characteristics of three 10^{17} cm^{-3} n-doped InN nanowires.

The difference in frequency with observing excess currents at the first time of measurement between the different samples may be connected to the diameters of the nanowires. Due to the large lattice mismatch between Si and InN (~ 7%), lateral stress relaxation is less effective with wider nanowires, especially those above 1 μm [56]. Consequently, the nanowires are more strained, and more defects and dislocations are present at the Si/InN interface and within the interfacial SiN_x.

In this chapter, we investigated the electrical transport properties of n-InN nanowires on p-Si substrates, grown by MBE with a unique self-catalytic process, with a custom-built nanoprobe setup. We have successfully detected interband tunneling with the Si/InN material system for the first time; however, the tunneling was impeded and not enough to observe a tunneling current peak, most likely due to an interfacial SiN_x layer within junction. Excess currents due

to trap-assisted tunneling are also commonly observed with our measurements; however, the exact nature of the trap-assisted tunneling is unclear at the moment. It can be any one of reasons outlined previously or a combination of them; however, we believe that it originates from the Si/InN interface and the SiN_x interfacial layer, and it is important to conduct more experiments to elucidate the matter.

Chapter 4

p-In/n-InN Esaki Diodes

In an effort to overcome the interfacial defects between the Si and InN, and observe a tunneling peak with InN, we study simple p-In/n-InN homostructures, similar to Esaki's first Ge diodes [17].

4.1 Simulating a p-InN/n-InN Esaki Diode

To understand the exact behavior of interband tunneling in an InN Esaki diode, we first model the junction with APSYS. A simple 10^{19} cm^{-3} n-doped / p-doped InN structure with 0.5 μm width and 1 μm length is designed and displayed in Fig. 4.1(a). As with all other modeled devices, the mesh is made more fine towards the junction interface.

The modeled InN structure behaves as any other Esaki diode. Under zero bias voltage, the conduction band of the n-region lies below the valence band of the p-region due to the doping concentrations chosen, as shown in Fig. 4.1(b). The junction is also very similar to Esaki's original Ge diode with a depletion region

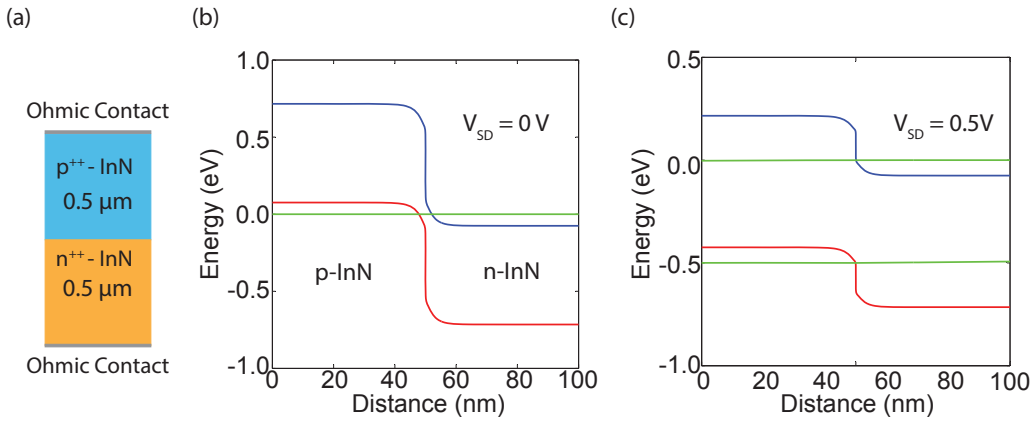


Fig. 4.1: (a) An illustration of a n-InN/p-InN junction examined with APSYS. (b) Energy band diagram of the junction with electron and hole quasi Fermi levels at a bias of 0 V and (c) 0.5 V.

width of ~ 10 nm.

With the simulator, the current densities through the diode are calculated with respect to the applied voltage bias and are displayed in Fig. 4.2. BTBT currents dominate at reverse bias, and at low forward biases, until there is no longer an overlap between the conduction band of n-region and the valence band of the p-region. At that point, the diode behaves according to Shockley's diode equation (Eq. 2.3), and forward injection currents dominate. The tunneling peak occurs at around ~ 38 meV - also similar to the Ge diodes - with a peak current density of 0.49 kA/cm^2. The similarity in tunneling behavior between our InN homojunction simulations and Esaki's Ge diodes can be attributed to the similar bandgaps of the two materials (0.65 eV for InN and 0.66 eV for Ge [35]).

From a practical situation, the InN nanowire homostructure needs to be grown on a Si substrate and probed as-grown with our custom built setup. Consequently, the junction between the Si and InN needs to be accounted for. This

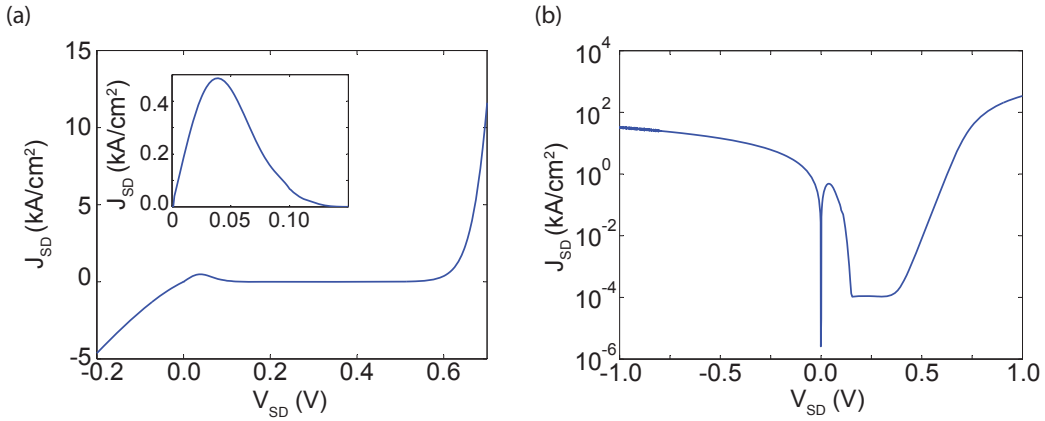


Fig. 4.2: (a) The IV transfer characteristics of the n-InN/p-InN Esaki diode through simulation. The inset is a zoom-up of the tunneling peak for clarity. (b) A semi-logarithmic plot of the transfer characteristics of the same Esaki diode.

design ensures that the interfacial SiN_x layer would not impede interband tunneling since the layer is no longer at the tunneling junction, but remains between the Si and InN. An illustration of the simulated nanowire on the Si substrate is displayed in Fig. 4.3. As with earlier simulations, the interfacial SiN_x is not taken into consideration since its exact properties are not fully understood.

The InN nanowire is 0.5 μm in width and 1 μm in length; the bottom of the nanowire is 10^{19} cm^{-3} n-doped, while the top 0.3 μm is 10^{19} cm^{-3} p-doped. Despite previously mentioning that our collaborator's growth process is capable of growing high quality p-doped InN nanowires, thick regions with high p-doping concentrations still pose some problems, and it is best to cap the p-doped region to 300 nm to limit defects. The nanowire itself is on a 10^{19} cm^{-3} n-doped Si substrate.

The new device is modeled with a finite element mesh and illustrated in Fig. 4.3(b). The overall current densities of the new device are calculated and shown

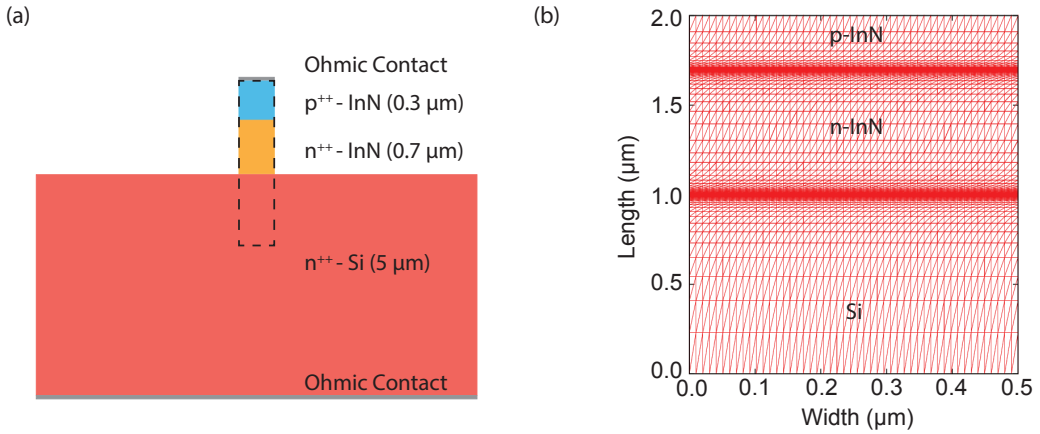


Fig. 4.3: (a) An illustration of a p-InN/n-In nanowire on a n-Si substrate examined with APSYS. (b) Closeup of the meshing in the dashed region.

in Fig. 4.4 (a); they are also compared to the previous p-InN/n-InN homostructure in Fig. 4.4 (b), while the band diagrams of the device at different bias voltages are shown in Fig. 4.5.

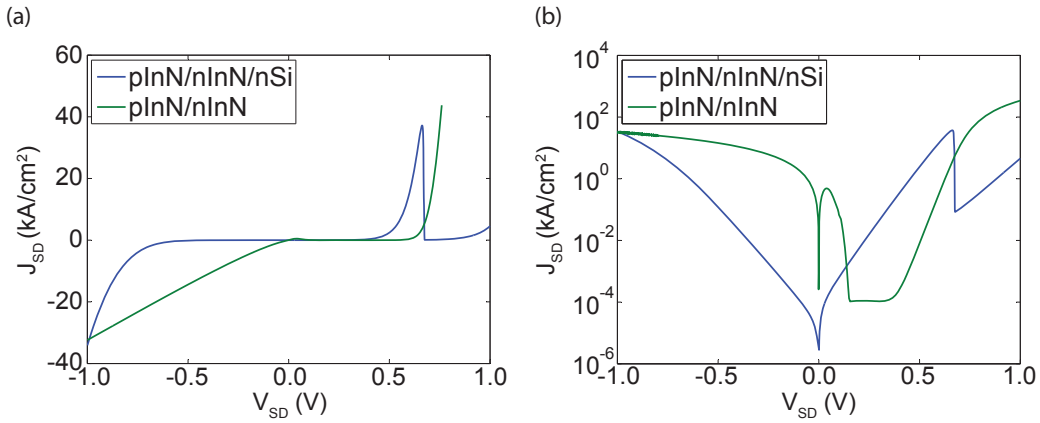


Fig. 4.4: (a) A comparison of the I-V transfer characteristics of the p-InN/n-InN/n-Si diode and the p-InN/n-InN homostructure through simulation. (b) A semi-logarithmic plot of the transfer characteristics for the same devices.

The Si substrate has significant effects on the overall behavior of the device. The n-Si/n-InN junction acts as a second diode and is in series to the tunneling

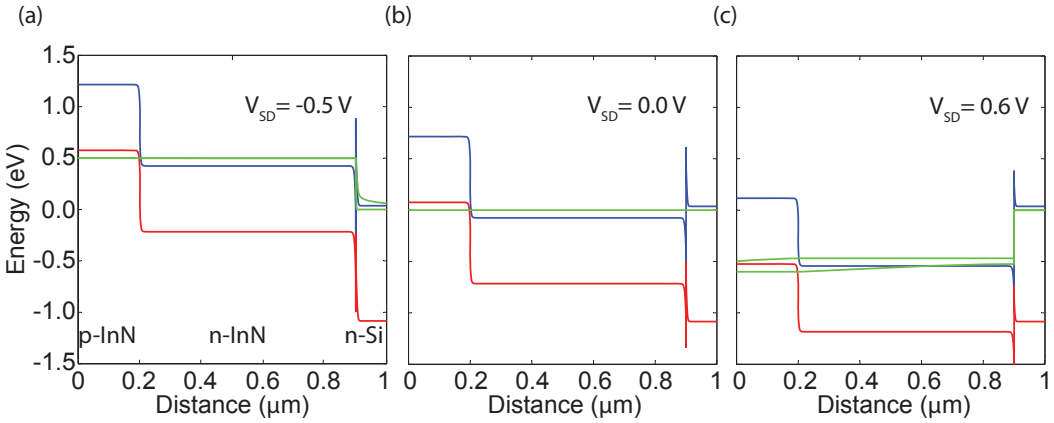


Fig. 4.5: Energy band diagram of the p-InN/n-InN/n-Si device with electron and hole quasi Fermi levels at a bias of (a) -0.5 V, (b) 0 V, and (c) 0.6 V.

diode, yet with an opposite polarity. When a negative bias is applied to the p-InN with respect to the grounded n-Si substrate, the p-InN/n-InN behaves as if under reverse bias, while the n-InN/n-Si junction is under forward bias. Under such a situation, the majority of the voltage drop across the n-InN/n-Si junction, and the energy bands of the p-InN and n-InN do not move with respect to each other, but move as a whole with respect to the Si substrate. Consequently, the tunneling current between the n-InN and p-InN does not increase when in reverse bias; however, the current through the n-InN/n-Si junction increases. Therefore, while the negative bias current is based on the tunneling through the p-InN/n-InN due to the initial band alignment of the materials, it is limited by the forward injection of the carriers through the n-InN/n-Si junction. This behavior is evident from the I-V characteristics of the device, where under negative bias, the current does not increase linearly with voltage - as with typical Esaki diodes - but follows a non-linear characteristic with $I \propto V^{7.13}$.

On the other hand, under a positive voltage bias, the energy bands of the p-

InN and n-InN do change with respect to each other. By increasing the voltage, the conduction band of n-InN is raised with respect to the p-InN, just like a regular Esaki diode. However, the majority of the voltage drop still occurs across the Si and not across the tunneling junction; this results in the observation of a tunneling current peak ($\sim$ 38 kA/cm^2) at unusually high voltage biases ($\sim$ 0.65 V). Moreover, due to non-linear series element, the NDR region for the new device is very abrupt, lasting only a few millivolts and unlike traditional Esaki diodes. By further applying a voltage across the device, interband tunneling ceases, and the junction reverts to normal diode behavior. Under such biases, the carriers will be confined within the n-InN region, until they have enough energy to overcome the p-InN potential barrier.

4.2 Probing the p-InN/n-InN Esaki Diode

The simulations have shown that the p-InN/n-InN/n-Si structure exhibits interband tunneling, albeit with a different behavior than traditional Esaki diodes due to the Si substrate. With no interfacial layer between the InN regions, observing a tunneling peak is now more likely with our measurements. With that in mind, new InN nanowires were grown on a 10^{19} cm^{-3} n-doped Si substrate. The nanowires themselves are similar to those simulated, $\sim$ 0.5 μm in width, $\sim$ 1 μm in length. The 10^{19} cm^{-3} n-doped region is $\sim$ 0.7 μm, while the 10^{19} cm^{-3} p-doped region is $\sim$ 0.3 μm. Unfortunately, problems were encountered during the growth process, especially with the Mg effusion cell. Some of the In droplets did not form nanowires, while other droplets promoted the growth of nano-structures other than the usual InN nanowires. Fig. 4.6 (a) shows an SEM

image of one of the most affected regions during growth, and displays one p-InN/n-InN nanowire along with In droplets and other nano-structures. Fig. 4.6 (b) shows an optical micrograph of a different region with our 100 X objective.

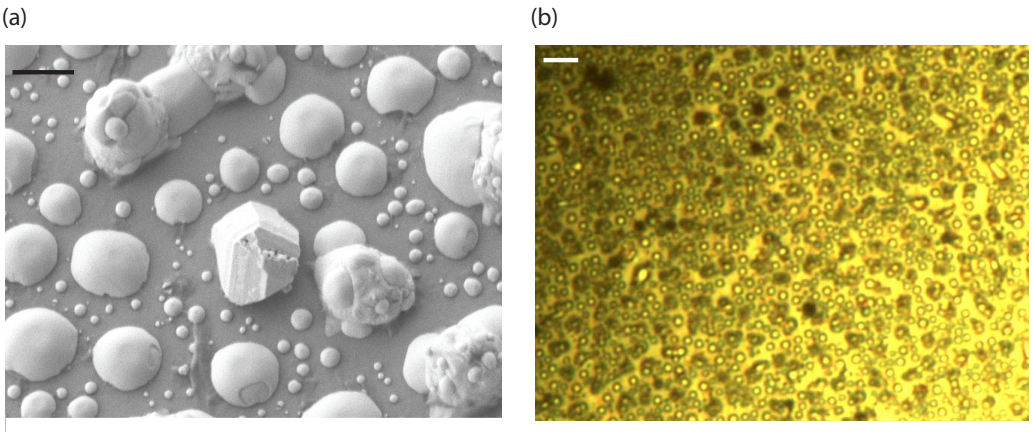


Fig. 4.6: (a) An SEM image of an p-InN/n-InN nanowire on a Si substrate along with In droplets and other nano-structures. The scale-bar is 1 μm. (b) An optical micrograph of the InN homostructure nanowires with a 100 X objective. The scale-bar is 5 μm.

The electrical transport properties of nanowires are measured with the same custom built setup in our lab. Despite the presence of structures other than the nanowires, it is possible to distinguish between them with the optical microscope. A representative sequence of transfer characteristics of two nanowires is shown in Fig. 4.7 and are compared to the simulation. Coincidently, the negative bias currents of both nanowires are nearly exact; however, they are significantly higher than the simulations at low voltage biases and vary with the applied voltage as a function of $I \propto V^{2.03}$. As mentioned earlier, the negative bias current densities depend on the forward injection of the carriers through the n-InN/n-Si junction; therefore, the high currents observed at the low bias voltages may be attributed to excess currents caused by traps at the InN/Si interface.

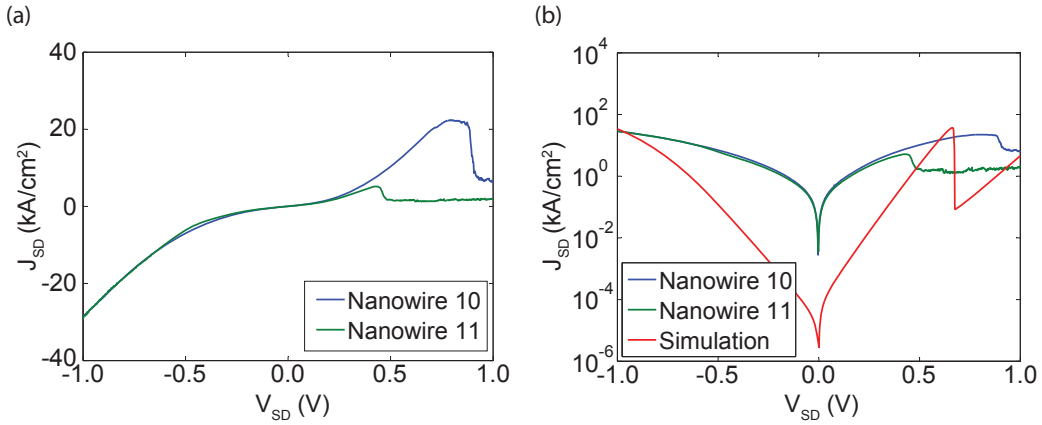


Fig. 4.7: (a) The I-V transfer characteristics of two different p-InN/n-InN nanowires. (b) A semi-logarithmic plot comparing the transfer characteristics of the same nanowires with the p-InN/n-InN/n-Si simulation.

Under positive bias, the current densities continue to increase with voltage, until they reach a tunneling peak and abruptly fall. The voltage at which the peaks appear largely depend on the Si and the SiN_x layer, since that is where the majority of the voltage drop occurs, as evident from the simulations. The tunneling peak of nanowire 10 appears at ~ 0.85 V with a current density of 22 kA/cm^2, while the second nanowire's peak current density (~ 6 kA/cm^2) occurs at a much lower ~ 0.44 V. Furthermore, the NDR region is less abrupt than the simulations and lasts ~ 20-30 mV. When interband tunneling ceases between the InN regions, excess currents start to dominate again and appear to mask any normal diode operation. The current seems to remain constant for both nanowires, without displaying any relation with the increasing voltage. Despite the excess currents, the nanowire 10 exhibits a remarkable PVCR of ~ 3.38, while nanowire 11 displays an even better PVCR of ~ 3.61.

Even though the InN nanowires have demonstrated that it is possible to ob-

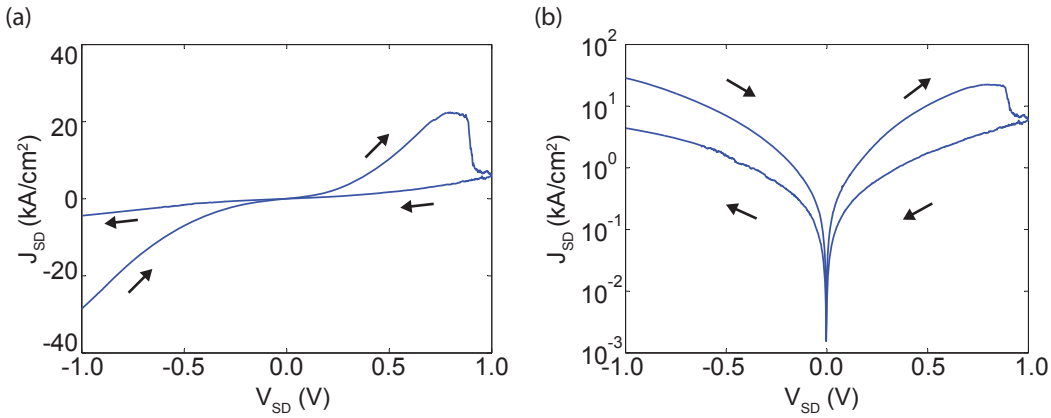


Fig. 4.8: (a) The I-V transfer characteristics of nanowire 10 with both forward and reverse sweeps (b) A semi logarithmic plot of the same I-V transfer characteristics.

serve a tunneling peak, some challenges are still encountered. First, all the new nanowires seem to exhibit a memory effect, with the reverse voltage sweep behaving differently than the forward sweep (shown in Fig. 4.8). Only the forward sweep exhibits a tunneling peak, while the reverse sweep exhibits a non-linear I-V relationship with $I \propto V^{1.45}$ under both forward and negative bias. While this memory effect is not completely understood at the moment, it may be due to the interfacial layer between the Si and InN. SiN_x has been commonly used in non-volatile memory device and utilizes charge-trapping to store information [27]. In our case, we might inadvertently be storing charge in the SiN_x layer during our forward sweep, and erasing the stored charge with the backward sweep (Fig.4.9).

The memory effect was not observed for the p-Si/n-InN diodes due to different possible reasons. First of the all, the nature of the traps in the interfacial SiN_x between the two structures may differ, especially with problems encountered during the growth of the p-InN/n-InN nanowires. Another possible reason

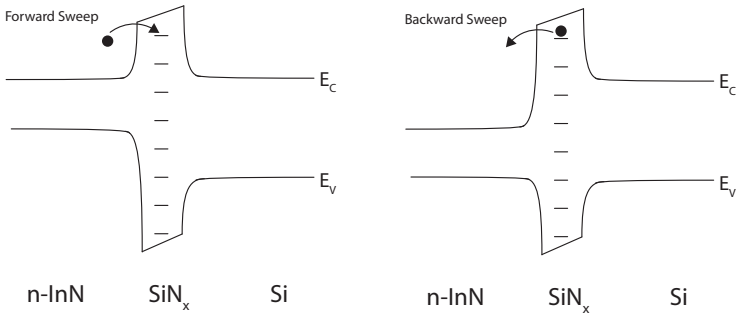


Fig. 4.9: Charge trapping and freeing with forward and backward sweeps

is the location of the SiN_x. In our initial devices, the nitride layer was in the tunneling junction, and the traps within the nitride probably contributed to trap-assisted tunneling currents. However, for the current devices, the nitride layer is in series with the tunneling junction, and the traps may just prevent subsequent tunneling.

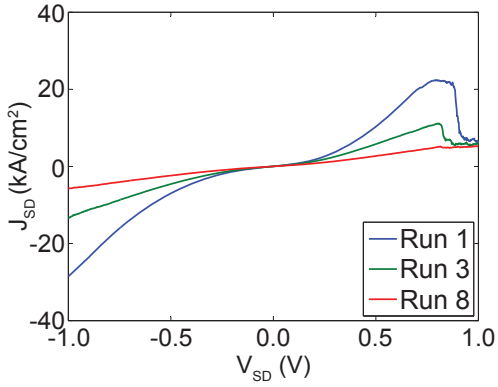


Fig. 4.10: The I-V transfer characteristics of nanowire 10 at different runs.

Another problem commonly observed with the p-InN/n-InN nanowires is that they become more resistive with every measurement. This behavior is noticeable in Fig. 4.10(a) and may be associated with the probable electrical stress-

ing of the nanowires with every measurement. The possible stress at the InN/Si interface will induce defects, increase the resistivity of the series junction, and decrease the amount of carriers available to tunnel through the homojunction. Consequently, with every subsequent run, the tunneling current is reduced until no peak is observed.

In this chapter we investigated the interband tunneling effects in an p-InN/n-In homojunction with both numerical modeling and nanoprobe characterization. By growing the nanowires on a n-Si substrate, the Si/InN junction appears in series along with the tunneling junction. In both simulation and electrical measurements, we observe interband tunneling currents exceeding 5 kA/cm^2. More importantly, we observe a tunneling peak and NDR region with our measurements at relatively high voltages (> 0.3 V) due to the majority of voltage drop occurring across the Si substrate. Unfortunately, we also observe non-idealities such as excess currents, memory effects, and impeded tunneling during our measurements. While we are not certain about the reasons behind each phenomena, we believe that the excess currents originate due to trap-assisted tunneling through the Si/InN interface, the memory effect appears due to charge trapping within the interfacial layer, and the impeded tunneling after every subsequent run occurs due to electrical stressing of the nanowires.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In this work, we have investigated the interband tunneling properties of the InN/Si junction, and its prospects as a viable material system for TFETs. InN has the largest electron affinity of all common semiconductors, which allows ideal semiconductor band alignment with Si for BTBT. However, InN's lattice constant differs by ~ 7% than that of Si, and to overcome the lattice mismatch between the two, InN is grown as nanowires using a unique self-catalytic process developed by our collaborators at McGill. The process allows for unprecedented control over the doping of the nanowires and is ideally suited to realize the sharp transitions in dopant density required for TFETs.

We first explored the tunneling properties of a simple p-Si/n-InN nanowire Esaki diode with numerical modeling software "APSYS" and expanded the concept to fully investigating an Si/InN nanowire TFET. The modeled diodes resembled traditional Esaki diodes, with the notable figures of merit. High tunneling

current densities were calculated, with a tunneling peak of ~ 6 kA/cm^2 at very low bias voltages (~ 35 mV), and a PVCR exceeding 10^5. The tunneling currents were notably dependable on the doping concentrations of materials, yet showed little dependence on temperature.

Once the simple modeled diodes showed promising tunneling behavior, the concept was expanded upon, and a TFET was designed with the software. The design took into careful consideration both doping concentrations and dimensions of the regions to ensure optimum behavior. The simulated TFET was very encouraging; the device showed a theoretically ultra-low sub-threshold voltage swing (below 8 mV/ decade for over 5 decades), high on-currents (> 1kA/cm^2), and current ratios (> 10^7).

With that in mind, our collaborators grew n-InN nanowires similar to those in the simulations on p-Si substrates, while we electrically characterized them. Over 500 nanowires were investigated with our custom built nanoprobe setup. Tunneling currents up to 12 kA/cm^2 were commonly observed at reverse bias voltages of -1 V; however, SiN_x interfacial layers impeded interband tunneling and prevented the observation of a tunneling peak. Compared to our simulations, the interfacial SiN_x reduced the reverse bias tunneling currents by nearly two orders of magnitude. Under forward bias and normal diode operation, our electrical measurements were very similar to simulations with the diodes turning on at ~ 1.45 V and behaving well under Shockley's diode equation.

Unfortunately however, excess currents were frequently observed and masked the expected diode behavior in many nanowires. The excess currents most likely resulted from trap-assisted tunneling due to defects and acceptor

states at the Si/InN interface within the SiN_x layer. Dislocations emanating from both tensile and electrical stress of the nanowires may have also contributed.

The tunneling junction was then moved into the nanowire, by growing p-InN/n-InN nanowires to bypass the effects of SiN_x on BTBT and provide us with a chance to observe a tunneling peak. Numerical simulations proved that the InN junction behaved as any other Esaki diode; however, by growing the nanowires on a Si substrate, an additional diode is introduced that affects the overall tunneling behavior. Nevertheless, both simulations and electrical measurements of the new nanowire structures exhibited interband tunneling along with the usual tunneling diode's figures of merit. The electrical measurements revealed peak currents exceeding 5 kA/cm^2 and PVCRs above 3. However, unwanted memory effects were also encountered with new devices.

Our work has shown the great potential of InN/Si material systems for interband tunneling and energy efficient electronics; however, there is still much work to be done before proceeding with fabricating TFETs.

5.2 Future Work

5.2.1 Eliminating the SiN_x

As stated numerous times throughout this thesis, we believe that the interfacial SiN_x layer has been a major impediment for optimum interband tunneling, and it is essential that we eliminate it. Our collaborators are developing different processes to eliminate the SiN_x without compromising the InN nanowire quality. One potential example, a thicker In seeding layer deposited on the Si substrate

surface prior to growth initiation may help consume the initially impinged active nitrogen species, thereby preventing the formation of SiN_x interface. Alternatively, during the initial nanowire nucleation stage (the first 5 to 10 minutes of growth), a higher In flux and/or lower nitrogen flow rate may be used to minimize or prevent the interaction between active nitrogen species and Si surface.

5.2.2 Low Temperature Measurements

It is also important that we perform more experiments to better understand the contribution of excess currents, and this can best be done with low temperature measurements. While interband tunneling is not temperature dependent, trap-assisted tunneling varies exponentially with temperature [52].

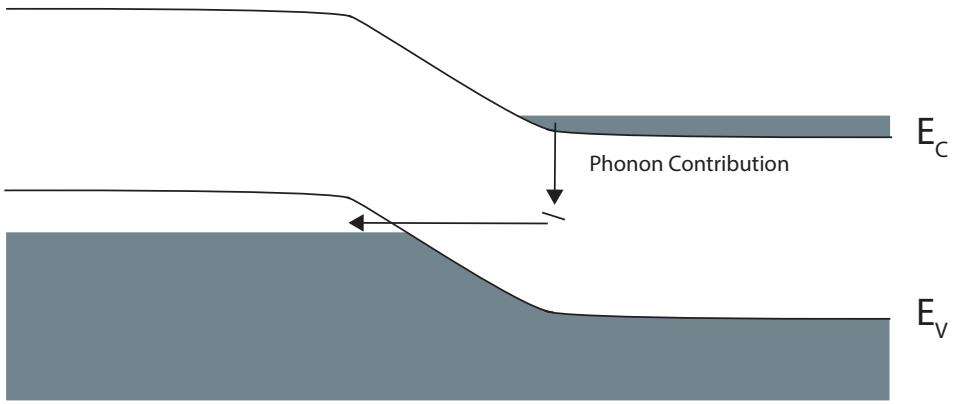


Fig. 5.1: Phonon contribution to trap-assisted tunneling.

The temperature dependence arises due to possible phonon contributions in BTBT transitions [52]. Fig. 5.1 shows the most likely mechanism for interband tunneling transitions within a junction. An electron in the conduction band drops to an empty trap within the bandgap due to phonons and then tunnels to

an empty state in the valence band with the same energy. By lowering the temperature of the junction, carriers dropping into the gap due to phonons become limited, and trap-assisted tunneling is restricted. Consequently, at low temperatures the excess currents can be reduced, and the PVCR can be improved significantly [38, 41, 52, 55].

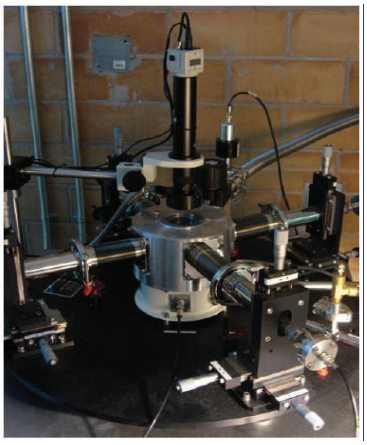


Fig. 5.2: High-vacuum probe station (Janis ST-500) for controlled environment measurements.

We are currently in the process of retrofitting our Janis ST-500 high-vacuum probe station (Fig. 5.2) to conduct low temperature measurements of our nanowires. A new arm is being installed to provide us with the necessary probe positioning resolution of 20 nm, and the 100 X microscopic objective is also being built in for the required optical resolution. With the new setup, we will be able to measure the charge transfer characteristics over a wide temperature range (77 K - 450 K) and elucidate the contributions of not only trap-assisted tunneling but also other non-idealities such as phonon-assisted tunneling and Urbach band-tails.

5.2.3 Fabrication and Characterization InN/Si Nanowire Arrays

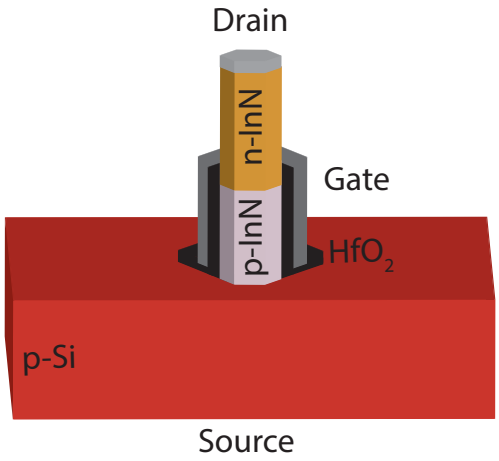


Fig. 5.3: Possible TFET structure after fabrication.

Fabrication will in no be doubt essential when designing the TFETs, and its important to develop processes to electrically contact the nanowires without deteriorating their electrical quality. Consequently, the InN/Si nanowires need to be electrically contacted, successfully characterized, and compared to our as-grown nanowires. This step will be very helpful when fabricating the TFETs in the near future. The contact process will combine Si dry etching, electron beam evaporation of Ni electrical contact layers, atomic layer deposition of insulating dielectric layers (Al_2O_3 or HfO_2), and finally standard electron beam lithography and photolithography techniques for interconnects. We will take advantage of the conformal nature of atomic layer deposition and self-aligned metal contact deposition to achieve lithographic contact to vertical nanowire structures.

By successfully characterizing the fabricated nanowires, we will have laid much of the ground-work for InN/Si TFET structures. With that, we can then proceed to work on the TFETs and the exciting prospects beyond CMOS.

Appendix A

Simulation Parameters in APSYS

APSYS uses three main input files with different file extensions: *.layer*, *.sol* and *.plt* to simulate any device. These files are used respectively to specify the device structure and generate the mesh, solve the equations, and plot the results [35].

A.1 The .layer File

The *.layer* file sets up the device geometry, doping, material information and mesh parameters simultaneously. To input the device structure in the *.layer* file, layers are placed on the top of each other in a similar manner to the deposition of layers during most fabrication processes. Lateral variations in materials due to etching or regrowth are depicted by columns in the *.layer* file. The meshing of the structure is generated by specifying the number of mesh lines within each column and layer; in addition, the mesh line distribution can also be controlled [35].

Start Page | InN_test.layer | InN_test.sol | InN_test.plt

```
0  begin_layer
1
2  column column_num=1 w=0.5 mesh_num=50 r=1.
3
4  layer_mater macro_name=si column_num=1 p_doping=5.64e+25
5  layer  d=1.  n=250  r=0.7
6  layer_position  label=pside  delta_y_from_bottom=0.9
7
8  layer_mater macro_name=inn_bulk column_num=1 n_doping=1.e+25
9  layer  d=1.  n=250  r=1.3
10 layer_position  label=nside  delta_y_from_top=0.9
11
12 bottom_contact column_num=1 from=0 to=0.5 contact_num=1 contact_type=ohmic
13 top_contact column_num=1 from=0 to=0.5 contact_num=2 contact_type=ohmic
14
15 end_layer
```

Fig. A.1: *.layer* file for n-InN nanowire on p-Si substrate

As an example, the *.layer* file for the simple nanowire structure in Sec. 2.2, is shown in Fig. A.1. In this case, only one column was needed with a thickness of 0.5 μm. The column had 50 mesh lines that were evenly distributed (r = 1). The parameter r is the geometric scale factor between successive mesh lines. The first layer was then set as the Si substrate with a p-doping concentration of 5.64×10^{19} cm^{-3}, while the second layer was the InN nanowire with a n-doping concentration of 1×10^{19} cm^{-3}. Both layers were 1 μm thick with 250 mesh lines spread along the materials; however, the mesh distribution was made more fine towards the interface with r = 0.7 and 1.3 in the Si and InN respectively. Finally, ohmic contacts were placed on the top and bottom of the device.

Similar layer files were created for all simulated devices with the same ratio of meshing lines to layer length and column width, as well as their distribution with respect to tunneling interface. This was done to maintain consistency when comparing devices. Only during the temperature simulations in Sec. 2.2.2 was the meshing number changed for each layer from 250 to 150 to maintain good convergence. Furthermore, it is also important to note that while it is possible to

change the material parameters, no changes were made to the stored parameters in APSYS for any material during the simulations.

A.2 The *.sol* File

The *.sol* file is the main simulation input used in APSYS. It consolidates all the device structural information as well as the material and simulation parameters. After including the input files generated by the *.layer* file into the *.sol* file, the physical models required for the simulation are then included [35]. In this case, interband tunneling was activated with the $tunnel\_junc$ and $use\_phyiscal\_model$ commands. The range where the tunneling equations were solved across the device was also specified. The tunneling range should be properly specified so that it represents the entire junction. An inaccurate evaluation of the tunneling current can occur if the specified tunneling range is too short, while a wide range may cause "divide by zero" errors [35]. For all simulated devices, the tunneling range was set to 0.1 μm on either side of the junction interface. Based on the APSYS manual [35] and many simulation trials, this range was appropriate to accurately calculate the tunneling currents of the devices.

After specifying the physical models, the simulator uses its Newton solver to find the final state of the device under bias. The $Newton\_par$ command controls the non-linear Newton solver to improve the convergence rate of difficult problems [35]. When solving the initial solution of any device under thermal equilibrium conditions and no bias, the $damping\_step$ was set to 5, the $maximum\_iterations$ was set to 100, and the tolerances for solving the equations, var_tol and res_tol, were set to 1×10^{-8}. When a bias voltage was applied,

Start Page | InN_test.layer | InN_test.sol | InN_test.plt

```
0  begin
1  load_mesh mesh_inf= InN_test.msh
2  include file=InN_test.mater
3  include file=InN_test.doping
4  output sol_outf=InN_test.out
5
6  tunnel_junc use_physical_model=yes yrange=(0.9 1.1)
7
8  newton_par damping_step=5. max_iter=100 print_flag=3 res_tol=1.e-8 &&
9    var_tol=1.e-8
10
11 equilibrium
12 newton_par damping_step=1. print_flag=3 res_tol=1.e-6 &&
13   var_tol=1.e-6
14 scan var=voltage_1 value_to=2 init_step=0.01 max_step=0.005
15 end
```

Fig. A.2: *.sol* file for n-InN nanowire on p-Si substrate

the tolerances were relaxed, with both var_tol and res_tol set to 1×10^{-8}, and the $damping\_step$ set to 1. The *.sol* file for the simple n-InN / p-Si junction is shown in Fig. A.2.

A.3 The *.plt* File

The *.plt* file is a simple file that plots the data generated by the *.sol* file where no input parameters are required. It is used to plot the I-V characteristic of the devices as well as the band diagrams.

References

[1] G. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, pp. 114–117, 1965.

[2] G. Moore, "Progress in digital electronics," *IEDM*, pp. 11–13, 1975.

[3] R. Keyes, "The Impact of Moore's Law," *IEEE Solid-State Circuits Society Newsletter*, vol. 11, pp. 25–27, Sept. 2006.

[4] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, Nov. 2011.

[5] T. N. Theis and P. M. Solomon, "It's Time to Reinvent the Transistor!," *Science*, vol. 327, pp. 1600–1601, Mar. 2010.

[6] M. Mills, "The Cloud Begins With Coal-Big Data, Big Networks, Big Infrastructure, and Big Power," 2013.

[7] J. Glanz, "Data Centers Waste Vast Amounts of Energy, Belying Industry Image," *The New York Times*, Sept. 2012.

[8] A. Seabaugh, "The Tunneling Transistor," *IEEE Spectrum*, 2013.

[9] T. Theis and P. Solomon, "In Quest of the "Next Switch": Prospects for Greatly Reduced Power Dissipation in a Successor to the Silicon Field-Effect Transistor," *Proceedings of the IEEE*, vol. 98, pp. 2005–2014, Dec. 2010.

[10] A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE*, vol. 98, pp. 2095–2110, Dec. 2010.

[11] D. Miller, "Device Requirements for Optical Interconnects to Silicon Chips," *Proceedings of the IEEE*, vol. 97, pp. 1166–1185, July 2009.

[12] L. de Broglie, "Waves and Quanta," *Nature*, vol. 112, p. 540, 1923.

[13] E. Schrödinger, "Quantisierung als Eigenwertproblem," *Ann. Phys.*, vol. 384, pp. 361–376, Jan. 1926.

[14] R. W. Gurney and E. U. Condon, "Wave Mechanics and Radioactive Disintegration," *Nature*, vol. 122, p. 439, Sept. 1928.

[15] M. Razavy, *Quantum Theory of Tunneling*. River Edge, NJ: World Scientific Pub Co Inc, 1st edition ed., Feb. 2003.

[16] C. Zener, "A Theory of the Electrical Breakdown of Solid Dielectrics," *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character*, vol. 145, pp. 523–529, July 1934.

[17] L. Esaki, "New Phenomenon in Narrow Germanium p-n Junctions," *Phys. Rev.*, vol. 109, pp. 603–604, Jan. 1958.

[18] L. Esaki, "Nobel Lecture: Long Journey into Tunnelling," 1973.

[19] H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art," *Electron Devices Society, IEEE Journal of the*, vol. 2, pp. 44–49, July 2014.

[20] F. Mayer, C. Le Royer, J. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, "Impact of SOI, SiGeOI and GeOI substrates on CMOS compatible Tunnel FET performance," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pp. 1–5, Dec. 2008.

[21] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and << 60mv/dec subthreshold slope," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pp. 1–3, Dec. 2008.

[22] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors," *Phys. Rev. Lett.*, vol. 93, p. 196805, Nov. 2004.

[23] K. Tomioka, M. Yoshimura, and T. Fukui, "Steep-slope tunnel field-effect transistors using III-V nanowire/Si heterojunction," in *2012 Symposium on VLSI Technology (VLSIT)*, pp. 47–48, June 2012.

[24] U. Avci and I. Young, "Heterojunction TFET Scaling and resonant-TFET for steep subthreshold slope at sub-9nm gate-length," in *Electron Devices Meeting (IEDM), 2013 IEEE International*, pp. 4.3.1–4.3.4, Dec. 2013.

[25] B. Ganjipour, J. Wallentin, M. T. BorgstrÃűm, L. Samuelson, and C. Thelander, "Tunnel Field-Effect Transistors Based on InP-GaAs Heterostructure Nanowires," *ACS Nano*, vol. 6, pp. 3109–3113, Apr. 2012.

[26] G. Dewey, B. Chu-Kung, J. Boardman, J. Fastenau, J. Kavalieros, R. Kotlyar, W. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. Then, and R. Chau, "Fabrication, characterization, and physics of III-V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, pp. 33.6.1–33.6.4, Dec. 2011.

[27] S. M. Sze, *Physics of Semiconductor Devices*. Hoboken, N.J: Wiley-Interscience, 2nd edition ed., 1981.

[28] C. G. Van de Walle and J. Neugebauer, "Universal alignment of hydrogen levels in semiconductors, insulators and solutions," *Nature*, vol. 423, pp. 626–628, June 2003.

[29] A. G. Bhuiyan, A. Hashimoto, and A. Yamamoto, "Indium nitride (InN): A review on growth, characterization, and properties," *Journal of Applied Physics*, vol. 94, pp. 2779–2808, Sept. 2003.

[30] B. Arnaudov, T. Paskova, P. P. Paskov, B. Magnusson, E. Valcheva, B. Monemar, H. Lu, W. J. Schaff, H. Amano, and I. Akasaki, "Energy position of near-band-edge emission spectra of InN epitaxial layers with different doping levels," *Phys. Rev. B*, vol. 69, p. 115216, Mar. 2004.

[31] S. P. Fu, Y. F. Chen, and K. Tan, "Recombination mechanism of photoluminescence in InN epilayers," *Solid State Communications*, vol. 137, pp. 203–207, Jan. 2006.

[32] S. Zhao, S. Fathololoumi, K. H. Bevan, D. P. Liu, M. G. Kibria, Q. Li, G. T. Wang, H. Guo, and Z. Mi, "Tuning the Surface Charge Properties of Epitaxial InN Nanowires," *Nano Lett.*, vol. 12, pp. 2877–2882, June 2012.

[33] I. G. Pichugin and M. Tlachala, "X-ray analysis of indium nitride," *Izvestiya Akademii Nauk SSSR, Neorganicheskie Materialy*, vol. 14, no. 1, pp. 175–176.

[34] S. Zhao, "Molecular beam epitaxial growth, characterization, and nanophotonic device applications of InN nanowires on Si platform," 2013.

[35] *Crosslight Device Simulation Software - General Manual*. Crosslight Software Inc., 2012.

[36] B. Ganjipour, A. W. Dey, B. M. Borg, M. Ek, M.-E. Pistol, K. A. Dick, L.-E. Wernersson, and C. Thelander, "High Current Density Esaki Tunnel Diodes Based on GaSb-InAsSb Heterostructure Nanowires," *Nano Lett.*, vol. 11, pp. 4222–4226, Oct. 2011.

[37] H. Schmid, C. Bessire, M. T. Björk, A. Schenk, and H. Riel, "Silicon Nanowire Esaki Diodes," *Nano Lett.*, vol. 12, pp. 699–703, Feb. 2012.

[38] W. Y. Fung, L. Chen, and W. Lu, "Esaki tunnel diodes based on vertical Si-Ge nanowire heterojunctions," *Applied Physics Letters*, vol. 99, p. 092108, Aug. 2011.

[39] M. Oehme, M. Sarlija, D. Hähnel, M. Kaschel, J. Werner, E. Kasper, and J. Schulze, "Very High Room-Temperature Peak-to-Valley Current Ratio in Si Esaki Tunneling Diodes (March 2010)," *IEEE Transactions on Electron Devices*, vol. 57, pp. 2857–2863, Nov. 2010.

[40] V. Reddy, A. Tsao, and D. Neikirk, "High peak-to-valley current ratio AlGaAs/AlAs/GaAs double barrier resonant tunnelling diodes," *Electronics Letters*, vol. 26, pp. 1742–1744, Oct. 1990.

[41] M. T. Björk, H. Schmid, C. D. Bessire, K. E. Moselund, H. Ghoneim, S. Karg, E. Lörtscher, and H. Riel, "Si-InAs heterojunction Esaki tunnel diodes with high current densities," *Applied Physics Letters*, vol. 97, p. 163501, Oct. 2010.

[42] G. W. Neudeck, *The PN Junction Diode: Volume II.* Reading, Mass: Prentice Hall, 2 edition ed., Jan. 1988.

[43] M. Yamaguchi, T. Takamoto, and K. Araki, "Super high-efficiency multi-junction and concentrator solar cells," *Solar Energy Materials and Solar Cells*, vol. 90, pp. 3068–3077, Nov. 2006.

[44] B. Van Zeghbroeck, "Principles of Electronic Devices," in *Principles of Semiconductor Devices*, Ece-www.colorado.edu, 2011.

[45] J. Davies, *The Physics of Low-Dimensional Semiconductors.* Cambridge University Press, 2009.

[46] Sedra and Smith, *Microelectronic Circuits.* Oxford University Press, 6th ed., 2009.

[47] R. S. Wagner and W. C. Ellis, "Vapor-Liquid-Solid Mechanism of Single Crystal Growth," *Applied Physics Letters*, vol. 4, pp. 89–90, Mar. 1964.

[48] M. Meyyappan and M. Sunkara, *Inorganic Nanowires: Applications, Properties, and Characterization*. Nanomaterials and their Applications, CRC Press, 2009.

[49] S. Zhao, B. H. Le, D. P. Liu, X. D. Liu, M. G. Kibria, T. Szkopek, H. Guo, and Z. Mi, "p-Type InN Nanowires," *Nano Lett.*, vol. 13, pp. 5509–5513, Nov. 2013.

[50] S. Zhao, O. Salehzadeh, S. Alagha, K. L. Kavanagh, S. P. Watkins, and Z. Mi, "Probing the electrical transport properties of intrinsic InN nanowires," *Applied Physics Letters*, vol. 102, p. 073102, Feb. 2013.

[51] B. Tekcan, S. Alkis, M. Alevli, N. Dietz, B. Ortac, N. Biyikli, and A. Okyay, "A Near-Infrared Range Photodetector Based on Indium Nitride Nanocrystals Obtained Through Laser Ablation," *IEEE Electron Device Letters*, vol. 35, pp. 936–938, Sept. 2014.

[52] A. G. Chynoweth, W. L. Feldmann, and R. A. Logan, "Excess Tunnel Current in Silicon Esaki Junctions," *Phys. Rev.*, vol. 121, pp. 684–694, Feb. 1961.

[53] T. Yajima and L. Esaki, "Excess Noise in Narrow Germanium p-n Junctions," *J. Phys. Soc. Jpn.*, vol. 13, pp. 1281–1287, Nov. 1958.

[54] D. Frohman-Bentchkowsky and M. Lenzlinger, "Charge Transport and Storage in Metal-Nitride-Oxide-Silicon (MNOS) Structures," *Journal of Applied Physics*, vol. 40, pp. 3307–3319, July 1969.

[55] C. D. Bessire, M. T. Björk, H. Schmid, A. Schenk, K. B. Reuter, and H. Riel, "Trap-Assisted Tunneling in Si-InAs Nanowire Heterojunction Tunnel Diodes," *Nano Lett.*, vol. 11, pp. 4195–4199, Oct. 2011.

[56] F. Glas, "Critical dimensions for the plastic relaxation of strained axial heterostructures in free-standing nanowires," *Phys. Rev. B*, vol. 74, p. 121302, Sept. 2006.