Fabrication of Diffractive Optical Elements by Electron Beam Lithography

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Abstract

Diffractive optical elements (DOEs) are an important component in the success of optical Microsystems. Electron beam lithography is a key part of fabricating these elements with submicron feature dimensions. This thesis presents work done on the development of a process for the fabrication of multilevel diffractive optics in glass substrates using this method. This project investigates various challenges involved in the process, addresses possible problems that may arise and proposes and investigates solutions to resolve them. Sources of possible error in the creation and transfer of the patterns are identified and methods of eliminating or minimizing these errors are presented. Some of the main sources of error arise from charging due to electron accumulation and alignment issues during electron beam lithography.

Sommaire

Éléments d'optiques diffractives (EODs) composent une partie essentielle dans le succès de microsystèmes optiques. Lithographie à faisceau d'électrons est un élément clé pour la fabrication des structures avec des dimensions critiques submicroniques. Cette thèse présente le travail fait sur le développement d'un processus pour la fabrication des optiques diffractives en utilisant cette méthode. Ce projet étudie des divers défis impliqués dans ce processus, traite des problèmes qui pourrait surgir et propose des solutions pour les résoudre. Les sources d'erreur possible dans la création et le transfert des modèles sont identifiées et des méthodes de les éliminer ou les minimiser sont présentées. Certaines des erreurs sont attribuées à l'accumulation d'électrons et aux problèmes d'alignement lors de la lithographie.

Acknowledgements

First and foremost, I would like to thank my supervisor, Dr. Andrew Kirk, for his patient guidance throughout this project. I would also like to thank the members of the integrated nanophotonics research group for their counsel and contributions to the development of the process.

I further extend my gratitude to the McGill Nanotools staff, in particular Dr. Matthieu Nannini, for assistance and instruction in operating various microfabrication facilities, resources and equipments. Further, the assistance of Dr. Thomas Szkopek in problems relating to electron beam lithography was invaluable.

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Chapter 1: Introduction

Diffractive optics is the means of implementing a whole spectrum of remarkable optical devices such as arrays of microlenses, beam splitters, displays and holograms. Optical elements designed for integrated optical systems can lead to efficient and compact systems. For these reasons, they are highly sought after in the design of various systems. Many of these elements are on the micrometre and nanometre scales or have features of those dimensions. Integrated optics make use of the same sort of fabrication techniques as exploited by the microelectronic industry. As such, the available fabrication technology allows diffractive elements to be made relatively easily. Naturally, these techniques must be adapted to meet the unique challenges specific to optical systems.

The goal of this project is to develop a complete process for fabricating diffractive optics by electron beam lithography, making use of the microfabrication resources available at McGill University. The process is to be implemented, upon completion, for the fabrication of an array of diffractive lenses used to create a highly integrated Surface Plasmon Resonance (SPR) biological sensor.

Electron beam lithography is a technique used for pattern writing in fabricating various nanotechnology devices. This method was chosen due to the small feature sizes of the diffractive elements involved in this device: As the features to be fabricated are in the submicron ranges, the conventional optical lithography approach is unsuitable. In addition, e-beam lithography offers unique flexibility in design and test of processes due to its use of digital layouts instead of physical masks.

Needless to say, such a process will be invaluable in developing other devices with similar challenges to this one using electron beam lithography. Challenges include the large area of each diffractive lens in the array coupled with the small writing field of the microscope, the stitching errors associated with the coupling of these latter design parameters, and the alignment requirements between the process steps for the multiple levels of the design

This thesis presents a fabrication process taking into account the aforementioned requirements. Chapter two presents an overview of diffractive and binary optics and fabrication procedures that have been used in implementing various diffractive elements. Chapter three discusses the device to be fabricated and presents a detailed, step-by-step process flow. In chapter four, electron beam lithography and its associated process characteristics are put forth and possible solutions to the perceived challenges are discussed. Finally chapter five is about transferring the lithographic pattern into the device material itself. To conclude, in chapter six, some reflections on the challenges of the proposed process lead to a discussion of possible alternatives.

Chapter 2: Diffractive Microoptics

Microoptics form an integral part of today's technological world. They can be found in devices from CD drives to integrated optical sensors. Diffraction is an optical theory that is extensively used in designing miniaturized optical systems. This chapter begins with a short overview of diffraction and elements that make use of it. It presents various methods used in fabricating these devices and examples of devices that have been fabricated with these methods.

2.1 Diffractive optics

Diffraction is an optical phenomenon that refers to the various effects caused by interactions of waves with obstacles such as the apparent bending of light around small objects or the spreading upon going through small openings. Like refraction and reflection, diffraction can be employed as a method of modifying the direction of light propagation. [1] A diffractive optical element (DOE) can be used to construct an arbitrary waveform given a known input wavefront. [2] This means that it can function as a regular refractive lens or allow the manipulation of light in ways impossible by traditional refractive and reflective optical elements, It can be used in conjunction with other optical components, for instance to correct various optical aberrations, as part of an integrated system or can be designed as a standalone element to transform incident light into the final desired waveform. Clearly, the flexibility offered by DOEs makes them an interesting avenue to explore in solving optical design problems. Other advantages offered by the technology are that the elements are often lightweight, cheap to fabricate and easy to integrate in compact systems.

A diffractive optical element is a component that uses interference and phase control to modify wavefronts. [2] The wave is initially segmented as it passes a geometric structure and the segments are redirected and the wave is reconstructed by interference. There are various terms used in specifying different types of DOEs. A kinoform is a DOE that has smoothly varying phase-controlling surfaces. Binary optic refers to a DOE that has a discrete number of phase-controlling surfaces. In its simplest form, this element has only two surfaces introducing either a 0 or π phase difference on the incident waveform. A multilevel binary optic has multiple steps, each of which introduces a phase shift.

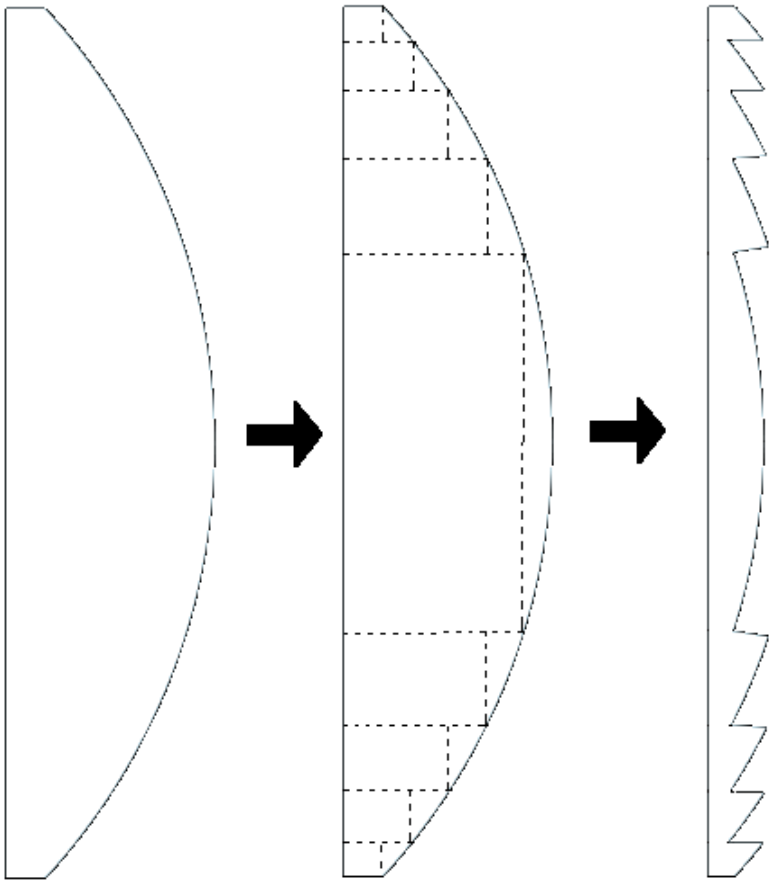


Figure 1 Conversion of a plano-convex lens into a Fresnel lens

As mentioned, a DOE can perform the same function as a refractive lens. Figure 1 depicts graphically the conceptual relationship between a plano-convex lens, a classic optical element, and a Fresnel lens which is its diffractive counterpart. The process involves the subtraction of pieces of glass that do not contribute to the final phase change. As a result, the Fresnel lens equivalent of the plano-convex refractive element is much thinner and lighter. The DOE acts only on the phase of the incident field. Otherwise, both optical elements act on the incident light in the same manner and focus it to the same spot. In fact, the process can be understood by ray traces through the surfaces with the application of the law of refraction at each surface.

A similar comparison can be made between a prism and a grating. A right-angled refractive prism can be sliced up into one-wavelength-high segments. Assembling only those parts that contribute to a change in path length results in a diffractive element known as the blazed grating. This process is illustrated in figure 2. A blazed grating will diffract all the incident light at that wavelength corresponding to the segments into the first order. A diffraction order is associated with a diffraction angle. Changing the wavelength of incident light will change the amount of light directed into the first order. At the design wavelength, this blazed grating has a diffraction efficiency into the first order of 100%. The efficiency of an order is defined by the percentage of incident light that gets directed into that order. As demonstrated by the blazed grating, a DOE can, in theory, be designed to have 100% efficiency for a certain design wavelength, angle of incidence and material.

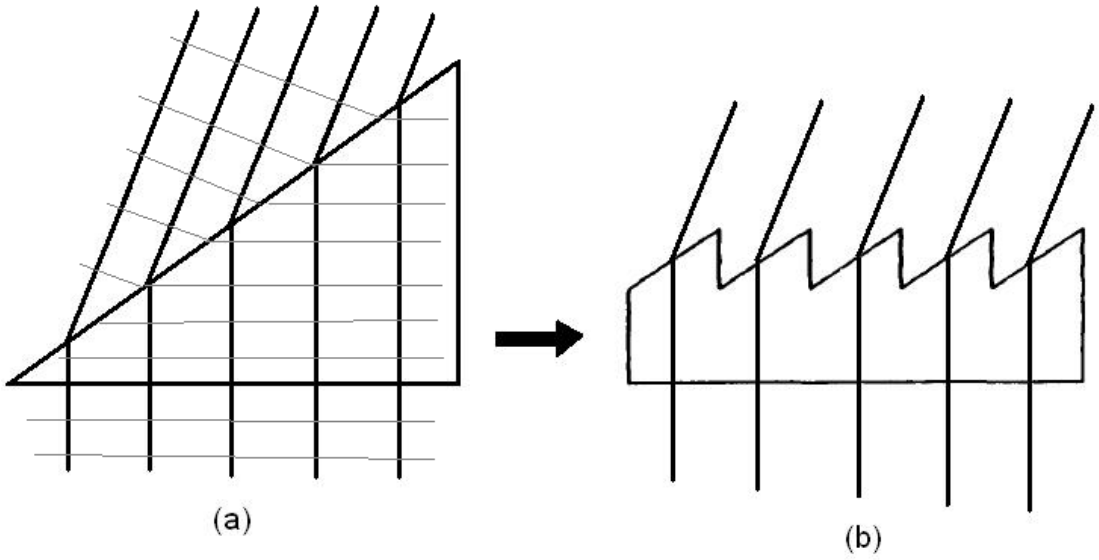


Figure 2 (a) Prism and (b) blazed grating used for deflecting wavefronts

A linear grating is perhaps the simplest example of a diffractive element. A blazed grating is a phase grating: The incident light field is modulated by a periodic phase delay which is due to the periodic change in the thickness of the grating material that the light traverses. For a grating with depth d and period Λ, the transmittance can be described by

$$t(x) = \mathrm{comb}\left(\frac{x}{\Lambda}\right) \otimes \mathrm{rect}\left(\frac{x}{\Lambda}\right) \exp\left(i\phi x/\Lambda\right)$$

where ϕ is the phase difference due to the grating depth and is given by

$$\phi = 2\pi\left(n-1\right)d/\lambda$$

with n being the refractive index of the grating and λ being the wavelength. Due to the periodic nature of the structure, light gets resolved into discrete diffraction orders and their angles of propagation are given by the grating equation:

$$\Lambda \sin \theta_m = m\lambda \,.$$

Here θ_m is the propagation angle of the m^{th} order. The angular separation of the different orders is dependent on the grating period. Light gets diffracted into different orders, but the diffraction efficiency or the fraction of light that goes into each of the orders is determined by the grating depth. A grating depth can be determined for which all of the light is diffracted into a certain diffraction order. A grating blazed for the first order needs to be etched to a depth given by

$$d = \frac{\lambda}{n-1}\,.$$

The above analysis is valid as long as the grating depth is small relative to the period so that the scalar approximation to the Maxwell equations can be used. The scalar theory is accurate when the period is greater than five wavelengths. [3] When the depth approaches the period, the efficiency decreases. As the diffraction efficiency is both depth and wavelength dependent, it will decrease at different wavelengths or with an error in the etch depth.

2.2 Binary optics

For DOEs to be accessible for use in a wide array of optical systems, they must be easy to manufacture. The surface of DOEs, as demonstrated in the Fresnel lens in figure 1 and the blazed grating in figure 2, varies smoothly over a 2π phase interval, Constructing such varying surfaces is a difficult endeavour. To allow diffractive elements to be more easily fabricated, the most commonly taken approach is to approximate the continuous surface relief by a series of discrete phase levels resulting in a multilevel structure. This process is illustrated in figure 3. Such structures are relatively easy to fabricate using

technology used by the IC fabrication industry. There is of course a price to be paid for this gain in fabrication simplicity. By approximating the profile of the DOE, some of its diffraction efficiency will be lost. The first order diffraction efficiency from an N-level binary optic structure is given by

$$\eta_1 = \left[\frac{\sin(\pi/N)}{\pi/N}\right]^2 .$$

Naturally, the more phase levels are added to the structure, the better it approximates the original continuous phase profile and hence the higher its theoretical efficiency will become. The first order efficiency for a two-level profile is 41%, the efficiency of a four-level structure is 81%, that of an eight-level structure is 95% and a 16-level structure can attain an efficiency of 99%. [3]

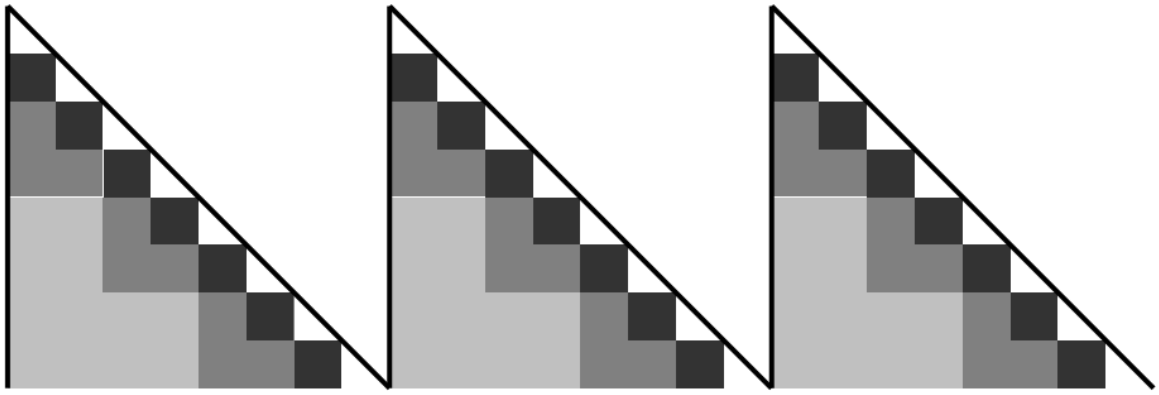


Figure 3 Continuous phase grating in comparison with two-level, four-level and eight-level discrete phase profiles

An N-level structure can be fabricated using M masks such that $N = 2^M$. The etch depth required for each of these masks is given by

$$d_M = \frac{\lambda}{2^M (n-1)}$$

where λ is the design wavelength, n is the refractive index of the material and M is the mask number.

2.3 Fabrication Methods

There is a long history of fabrication of optical elements of all sorts using techniques borrowed from the microelectronics fabrication industry. Many optical elements have been fabricated using all kinds of different fabrication methods. An overview of some of these methods follows.

2.3.1 Analogue Direct Write

One class of fabrication methods is known as analogue direct write or greyscale writing where the complete profile is written in one step. Structures are formed in a polymer on the surface of the structure by varying the exposure intensity over the surface. [4] The thickness of the film is chosen such that, at the wavelength of incidence, it causes a phase shift of 2π.

In 1981, micro Fresnel lenses were fabricated using electron beam lithography. [5, 6] These lenses where written in an electron sensitive film (resist) on glass for operation at a wavelength of 633 nm. A 20 nm layer of gold was evaporated over the resist to serve as a charge dissipation layer. The process flow appears in figure 4. The best diffraction efficiencies achieved by these lenses, determined experimentally, was 31%. The lenses

generally had diameter of 0.4 mm or 1 mm with a minimum pitch size of 1 µm between lens grooves. An array of three of such lenses was also fabricated.

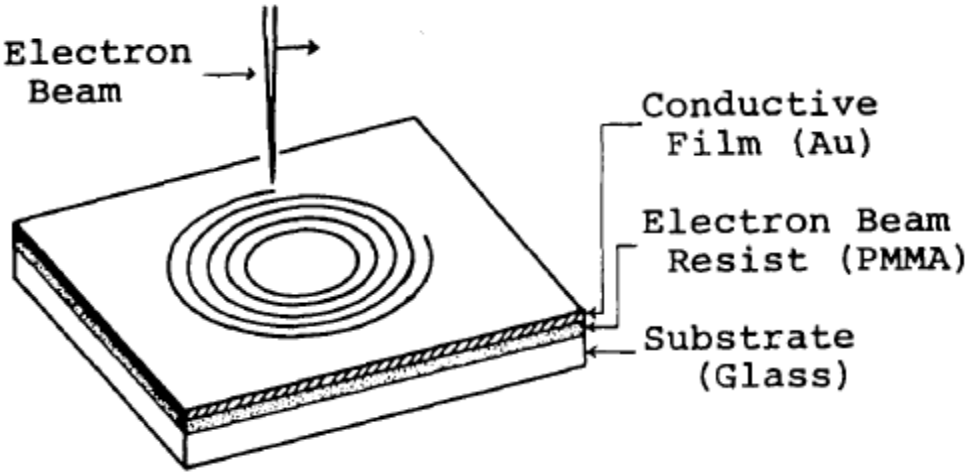


Figure 4 Fabrication of micro Fresnel zone plates by electron beam writing [6]

To improve the diffraction efficiency of diffractive microlenses, a technique was devised to fabricate blazed profiles by e-beam lithography. [7] In this method, the profile of the grating is written directly in the resist by varying the energy of the beam used for different heights in the profile. The fabrication process flow appears in figure 5. The sections of the resist receiving different electron doses will etch to different heights upon development. Once the electron dose versus etch depth characteristics of the resist are known, any profile can be written by varying the dose as a function of position on the substrate appropriately. In the previously discussed process, the exposure dose was not varied; the resist layer was exposed at a high enough dose to etch the entire resist layer on the surface, a procedure that resulted in a two-level structure as opposed to a blazed one.

Blazed gratings with periods of 5 and 10 µm were fabricated and tested at 633 nm. The diffraction efficiency of the first order was found to be 60% to 70%. The Fresnel lenses described earlier were also fabricated once more, this time using a similar method of varying exposure doses to obtain a blazed profile and it was shown that this increased their efficiency to 50%.

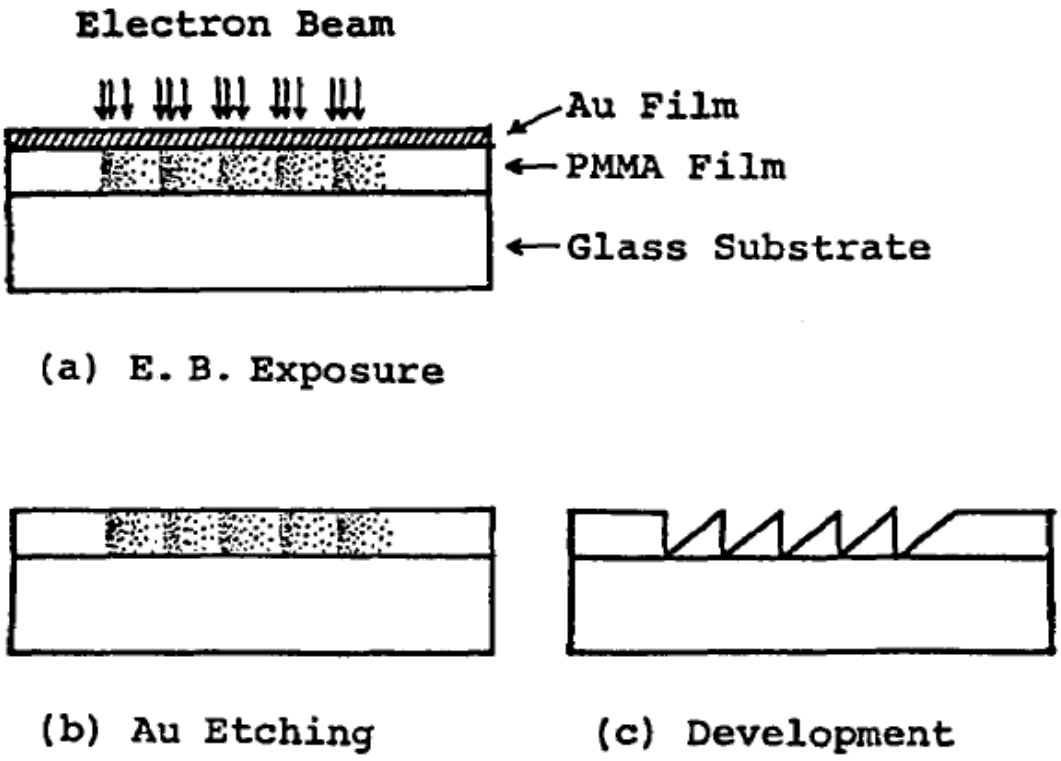


Figure 5 Fabrication process for blazed gratings by EBL where the higher dot density corresponds to a higher electron dose [7]

The same method of varying exposure dosage to obtain different etch heights in the film was used to fabricate arrays of micro Fresnel lenses with rectangular apertures. [8] The fabrication process for these structures appears in figure 6 (A). The glass substrate was coated with indium tin oxide (ITO) which is a transparent conductive layer and then

coated with resist. For each lens in the array, the beam was swept in circles to deliver the desired dose at each diameter before moving 0.1 or 0.2 µm away to write the next circle at the next dose. After each lens was written, the stage was moved the width of the lens aperture to write the next one. Upon development and postbaking, the blazed profiles were achieved. Figure 6(B) shows microscope images of the lens arrays fabricated by this method. Efficiencies of 69% and 74% were experimentally determined for the two arrays.

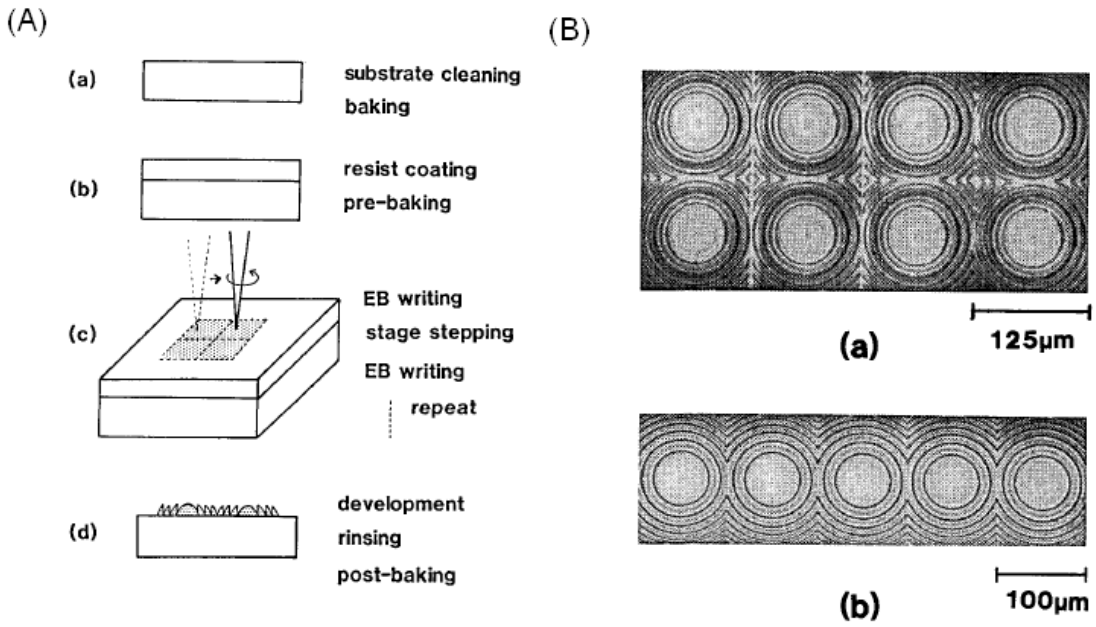


Figure 6 (A) Fabrication process for arrays of micro-Fresnel lenses with rectangular apertures (B) Blazed Fresnel lens arrays [8]

In the structures discussed thus far, the optical element is formed in the resist film and is not transferred into the glass substrate. Various other structures have also been fabricated in a similar manner. [9-11] Structures made in resist tend to be somewhat vulnerable as they are not resistant to thermal or mechanical changes. [4] Attempts have also been made at transferring such structures into the glass substrate. One

method that has been demonstrated is by use of chemically aided ion-beam etching (CAIBE) for etching a fused quartz substrate with a 4 × 4 array of lenses each of which having an aperture size of 250 µm × 250 µm. [4] Reactive-ion etching (RIE) has also been used to transfer kinoform profiles from the resist to fused quartz [11] and fused silica [12] substrates. For this type of transfer to be successful, it is necessary to optimize the etch rates in resist and the glass substrate. Typically, it is necessary for the etch rates in the two material to be identical.

2.3.2 Binary Lithography

The alternative to the analogue direct write method of DOE fabrication is, of course, binary lithography. This method involves the sequential building of discrete phase levels by using a set of binary masks. [3] The process of fabricating multilevel diffractive structures by successive photolithography steps has been used for fabricating various devices. Its details can vary in that the various layers constructed by each mask can be additive, where layers are deposited on top of each other, or subtractive, where each step increases the etch depth and removes more of the substrate. These processes have a common theme: Each layer in the structure has a carefully calculated height to deliver a specific phase difference to light travelling through it.

Multilevel structures must meet stringent alignment requirements wherein successive layers must be exactly aligned with 0% overlay tolerance. The etch depth also needs to be very precisely controlled. [13] Such requirements make the precise fabrication of DOEs with many levels an arduous task indeed.

In 1972, photolithographic techniques were first applied to the fabrication of multilevel lenses. [14] The fabrication process flow appears in figure 7. In this process, a thermal oxide (SiO_2) layer is grown on a silicon sample. The oxide is covered by photoresist and patterned through a binary mask using optical lithography. The oxide is then etched through the exposed sections. The procedure is repeated thrice to construct the desired four-level structure. This structure was then used as a mould for replication in plastic. The efficiency of a plastic copy was 63%. A 32 × 32 array of a binary lens, using a similar fabrication procedure, was also fabricated.

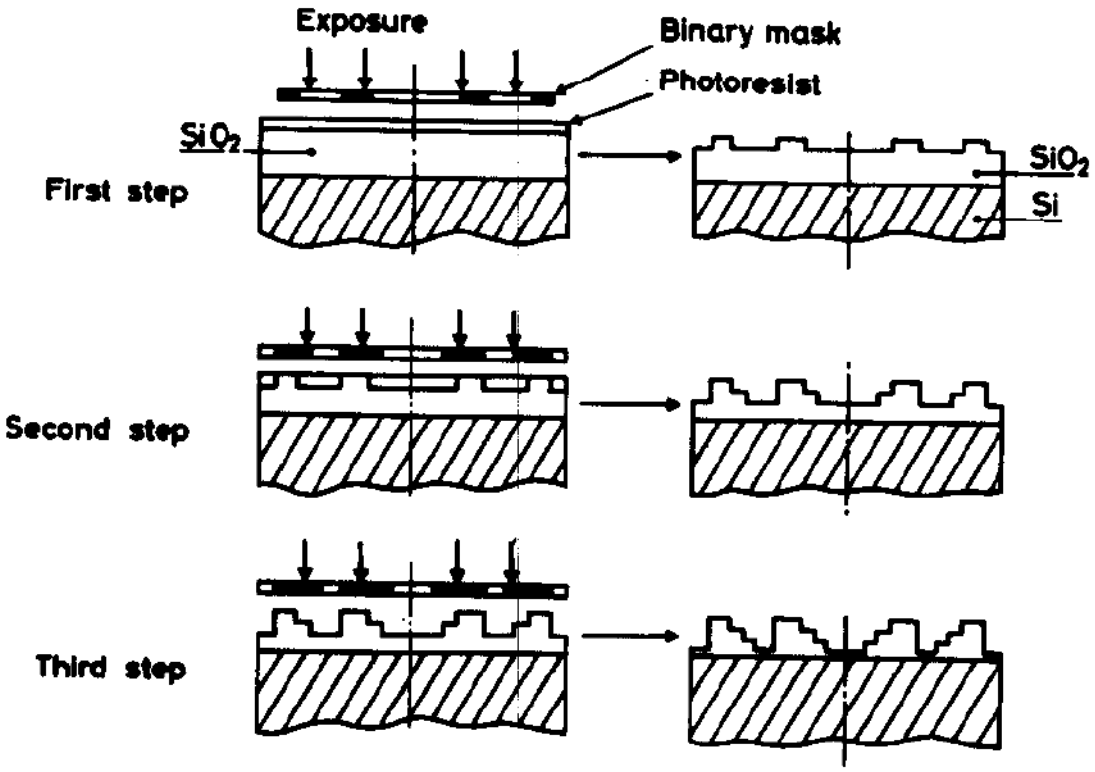


Figure 7 Fabrication process for multilevel lenses by successive lithography steps [14]

Multilevel phase structures were fabricated using thin film deposition in [15]. A quartz substrate was coated with photoresist which was patterned by photolithography. A

layer of silicon monoxide (SiO) was then evaporated onto the surface. Finally, the substrate was soaked in acetone to dissolve the resist and carry away the overlying SiO. A structure in SiO remains on the glass. By repeating the process several times, multilevel diffractive lens structures can be formed. Three lithographic steps were used to reach an eight-level structure with a minimum feature size of 2 μm. In addition, a 10 × 10 array of lenslets, each 1.5 mm x 1.5 mm, was also fabricated. The smallest feature size in the lenses in this array was 5 μm. These lenses were designed for operation at a wavelength of 1 μm and had a measured efficiency of 91%.

Another quite similar method of fabricating multilevel diffractive optical elements involves building the structure by successive deposition and patterning of resist layers. In [16], a four-level reflection grating with a period of 22.4 μm was fabricated. The process involves coating three sets of alternating layers of resist and aluminum on a silicon substrate. Each layer of resist is exposed using hard contact optical lithography for patterning. The underlying layer of aluminum protects the lower resist layers from being exposed. After development, the aluminum layer is etched and the process is repeated for the next layer. This describes a linear process where three masks form four layers. The technique could be applied to a logarithmic process as well wherein two masks would fabricate the same four-level structure. These gratings were able to achieve an efficiency of 63%.

Clearly, this type of fabrication method is applicable to many devices. Other structures fabricated by similar fabrication processes include high-efficiency beam splitters and beam deflectors. [17]

Traditionally, multilevel devices have been patterned by photolithography. Of course, the main limitation of photolithography is in the attainable feature sizes. A binary (two-

level) diffractive lens was fabricated with features less than 60 nm using electron beam lithography instead of photolithography. [18] The substrate in use was SiO_2 and was coated with 20 nm of silicon nitride as an adhesion layer and 150 nm of gold. The resist layer (PMMA) was 70 nm thick and was patterned by a beam with an acceleration energy of 30 kV. After development, the resist was used as a mask for ion milling of the gold layer with argon gas to remove it where the resist was exposed. The gold gets etched four times as fast as the resist. Finally, the pattern in the gold is used to transfer the lens into the SiO_2 substrate by reactive-ion etching. The final lens had a measured diameter of 36 µm and a measured etch depth of 400 nm with an estimated minimum feature size of 48 nm. This therefore demonstrates the possibility of attaining small lens features using e-beam lithography while the rest of the process is essentially the same as the ones with photolithography.

2.4 Subwavelength Diffractive Structures

Due to the highly demanding requirements imposed on the alignment between the various levels and the etch depths for fabricating multilevel structures, it is interesting to investigate alternate ways of implementing a diffractive structure. Figure 8 shows an arbitrary segment of a refractive optical element along with four different ways of implementing it as an equivalent diffractive structure. In 8(b) the Fresnel zone implementation is shown and 8(c) depicts the familiar binary optics implementation. The gradient index structure of figure 8(d) can provide the required phase but is difficult to fabricate on small scale. The structure known in figure 8(e) is known as a subwavelength binary diffractive optical element. It uses binary surface relief structures with features smaller than the wavelength of light within the material for implementing an arbitrary gradient index material. The effective index of the material could be varied by changing the binary pattern. [19]

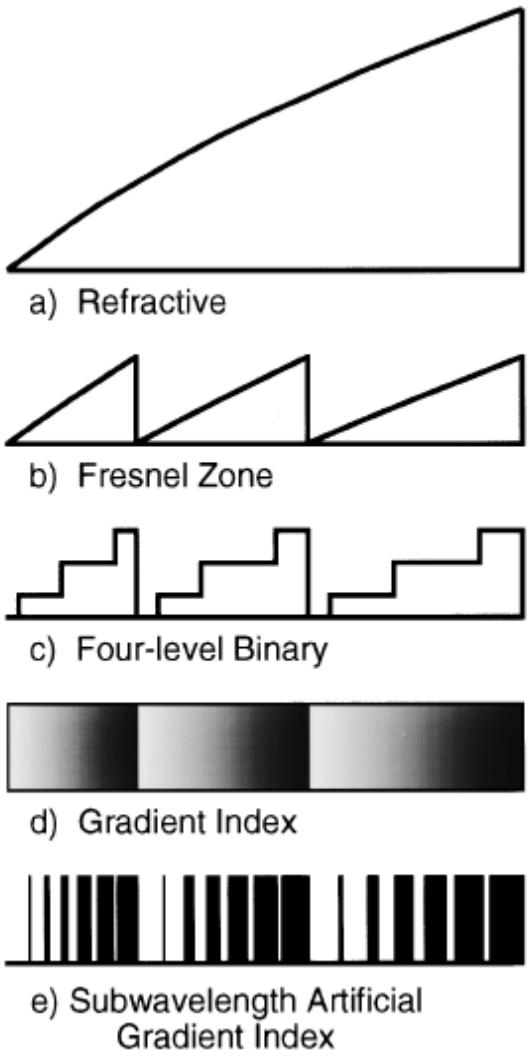


Figure 8 Four analogous diffractive implementations of an arbitrary refractive element.[19]

Using such a structure has various advantages over the usual multilevel diffractive optics. Primarily, it reduces the number of process steps as the fabrication of such a structure requires only a single set of lithography and etch steps. Arbitrary phase profiles can be implemented and very high efficiencies can be achieved. Of course, the feature dimensions required are very small and constitute a challenge in successful

implementation of such structures. Their performance is also highly dependent on light polarization.

Blazed gratings [19] and off-axis lenses [20] have both been fabricated as subwavelength structures in GaAs for operation at a wavelength of 975 nm. Both structures were designed with practical instrumental constraints, such as minimum writable feature size and maximum achievable aspect ratio, in mind. The fabrication process used for the two aforementioned devices is quite similar. For the binary diffractive lens, the GaAs substrate was first coated with 120 nm of SiO_2 and 100 nm of resist. E-beam lithography was used to write the lens pattern. The lens diameter is 80 μm and the e-beam field is also 80 μm so no field stitching was required for this write. Afterwards, 5 nm of titanium and 40 nm of nickel were evaporated onto the resist and lifted off. The pattern was then etched into the SiO_2 by reactive-ion etching and into the GaAs substrate by reactive-ion beam etching. The minimum feature size of the fabricated device was 50 nm and the lens, designed for a maximum theoretical efficiency into the first order of 92%, achieved a maximum measured efficiency of 72%. The loss of efficiency was attributed, among others, to variation in etch depths. Nevertheless, it is remarkable that high-efficiency diffractive elements can be fabricated with one lithography and etch processing whereas an eight-level structure and therefore three sets of processing would be required for a multilevel element to exhibit an efficiency above 90%.

Chapter 3: Device and Fabrication Overview

This chapter presents an overview of the target device and the proposed fabrication process. Further details on the specific steps in the fabrication process are given in the following chapters: Chapter four will discuss electron-beam lithography in detail and chapter five will cover substrate patterning processes.

3.1 Design Overview

The device to be fabricated is an off-axis cylindrical diffractive optical element designed to operate at a wavelength of 850 nm. A pair of these DOEs can be used to focus light coming in from an angle onto a sample well containing samples to be examined. An array of such pairs can be formed to function as a multichannel integrated sensor. A similar system using diffractive mirrors was previously discussed in [21]. The current design is refractive instead of reflective. A side view of multiple DOEs focusing on sample wells is shown in figure 9. The DOE is illuminated at an angle of 47º. The refracted rays will be at angles for 65º to 75º. The light is focused to the back plane of the 1.5-mm lens substrate where the sample well is located. The optical setup for illuminating and imaging the array of DOEs was simulated in Code V and appears in figure 10.

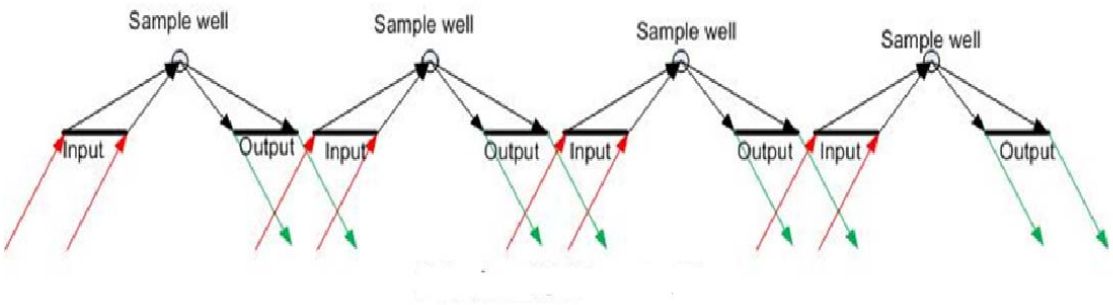


Figure 9 Side view of eight DOEs focusing on four sample wells

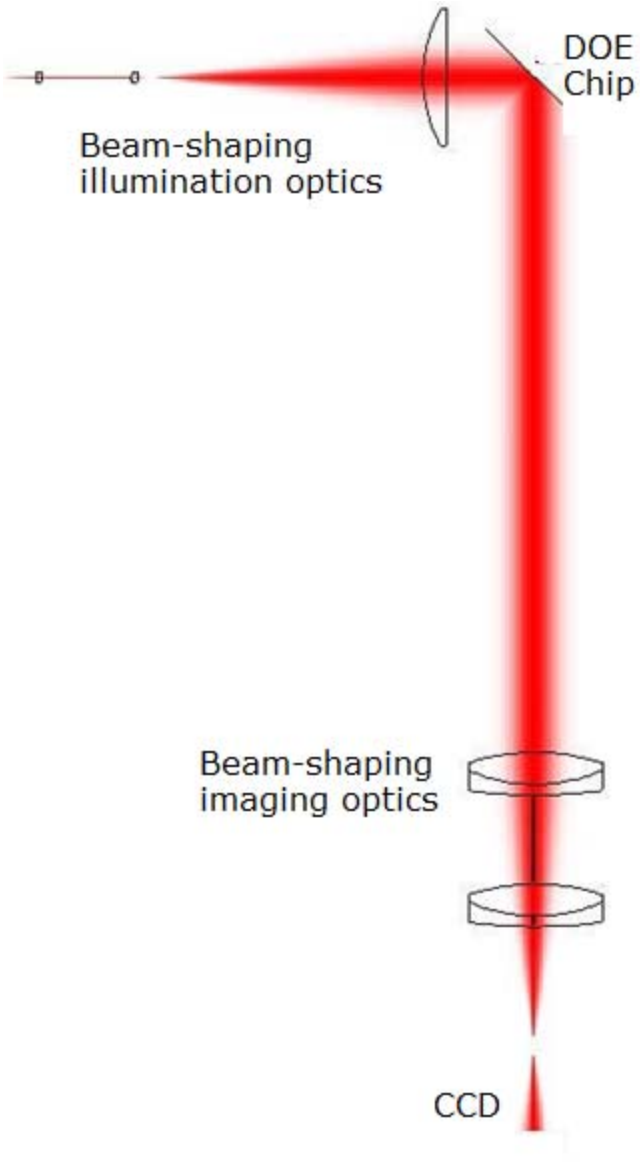


Figure 10 Optical setup for imaging the DOE array as simulated by Code V

A single DOE in this array has an aperture of 2.551 mm by 1 mm and consists of 2010 zones. The continuous phase profile was converted into a four-level binary optical equivalent which can be fabricated using two masks. The profile for one of the zones in the DOE appears in figure 11. Here Zp is the zone period while h_1 to h_4 are the heights of the different levels of the binary optical element with h_4 being considered to have a value of zero. The two masks required to create such a structure appear in figure 12.

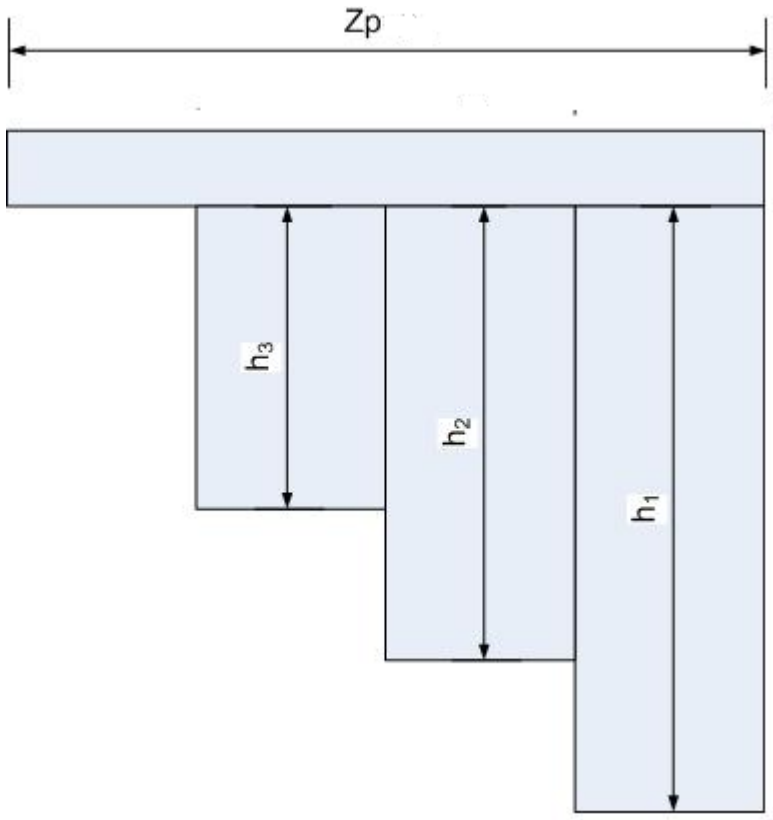
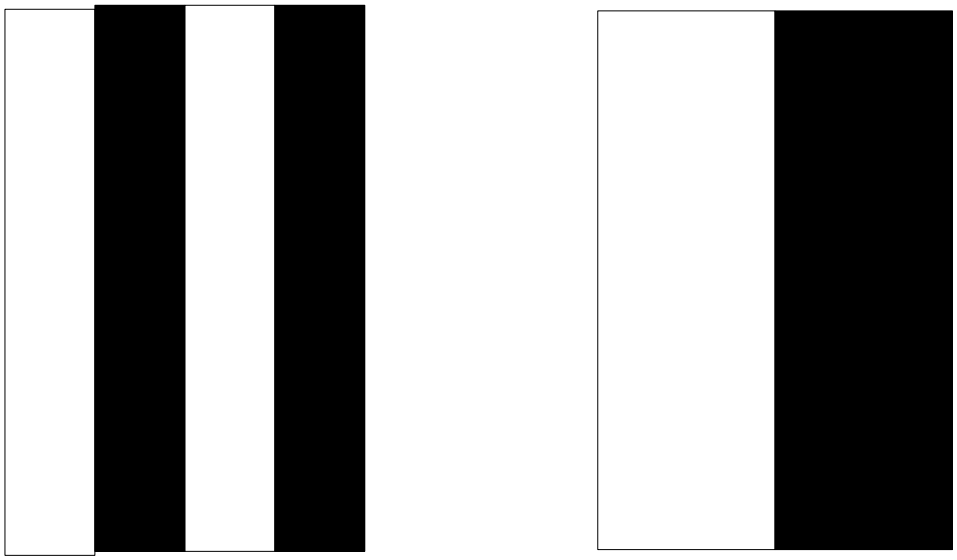


Figure 11 Profile of a single zone of the cylindrical diffractive optical element



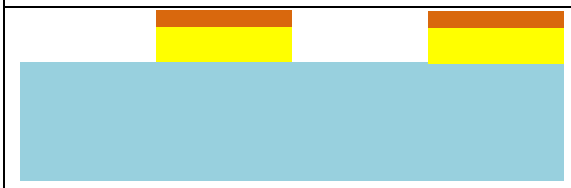
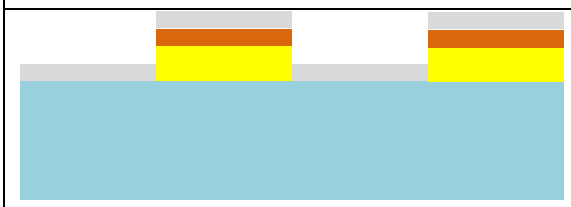
(a) (b)

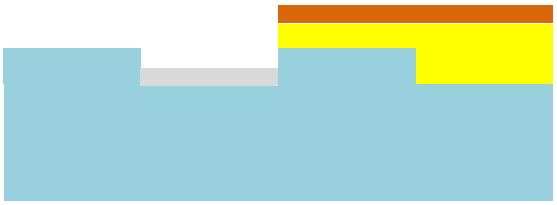
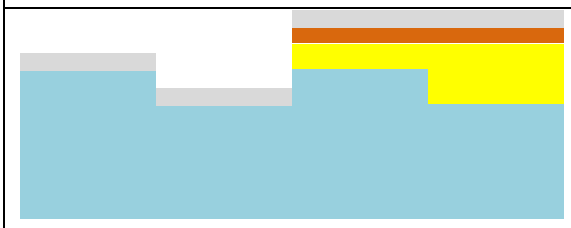
Figure 12 Mask layouts for (a) layer 1 and (b) layer 2 of the diffractive optical element

3.2 Fabrication Process

The major fabrication steps of the process are diagrammed and summarised below in figure 13 for the profile of one of the zone periods of the device. Most steps of the fabrication take place within the confines of a clean room in an attempt to eliminate any contaminations.

The substrate chosen for the fabrication of this device is fused silica. It is a form of glass that consists of silicon dioxide (SiO_2) in an amorphous (non-crystalline) form. This high-purity form of glass has improved optical transmission in the deep ultraviolet and is highly transparent throughout the spectrum until mid infra-red. The low value of its coefficient of thermal expansion over a wide range of temperatures ensures stable operations in varying temperatures. It has a low refractive index leading to a low Fresnel reflection constant. [22] The refractive index of fused silica at 850 nm is around 1.46. [23] On the other hand, as seen in chapter 2, the necessary etch depth in a material is inversely proportional to its index of refraction. The low refractive index of fused silica therefore leads to greater etch depths.

	1. Spin coat copolymer and PMMA on substrate.
	2. Pattern resist through mask 1.
	3. Evaporate 100 nm of chrome.

	4. Perform liftoff.
	5. Etch exposed glass 425 nm using RIE.
	6. Wet etch chrome mask.
	7. Spin on copolymer and PMMA.
	8. Pattern resist using mask 2.
	9. Evaporate 100 nm of chrome.
	10. Perform liftoff.
	11. Etch exposed glass 850 nm using RIE.

	12. Wet etch chrome mask.

Figure 13 Major steps in the fabrication process flow of a four level DOE shown for the profile of a single zone

Step 1: Substrate preparation

The fused silica pieces used in the process are 1.5 mm thick. They are now cut into small pieces approximately 1 cm x 1 cm.

Step 2: Cleaning

The substrate must be thoroughly and carefully cleaned prior to any processing. This is critical as any impurities or dust particles or other contaminations will jeopardize the successful fabrication of the device. To this end, the substrate is first immersed in acetone and placed in an ultrasonic bath at 40 ºC for 10 minutes. Subsequently, the substrate is transferred to an isopropyl alcohol (IPA) solution and is once more placed in an ultrasonic bath for 10 minutes at 40 ºC. Upon completion, the sample is rinsed using deionised water. It is finally blown dry using nitrogen gas. This is the cleaning procedure used for cleaning the sample between major steps.

Step 3: Coating 500 nm of EL-11 copolymer

Once thus cleaned, the sample is ready for processing to begin. The next step is to coat the sample with the resist layer used in lithography. In this case, an approximately 500 nm thick layer of EL-11 copolymer is first spun on the fused silica substrate. The purpose of this layer is to facilitate the lift-off of a metallic layer in a later step. A Laurel spin coater is used for all spin-coating purposes in this process. The substrate is placed and

centered on the o-ring on the spin-coater chuck and the vacuum is turned on. The vacuum will now hold the substrate firmly in place. The copolymer is then dispensed over the substrate using a disposable pipette such as to cover most of the surface. One must take care to dispense a uniform layer of liquid. It is very important that no air bubbles be present in the liquid as this will lead to the production of an uneven resist surface which will affect the quality of the pattern transfer. The spin coater lid can now be closed. The spin speed for the copolymer can be found in the datasheets provided by MicroChem. The spin speed versus resist thickness curve indicates that spinning at 4000 rpm will result in an approximately 500 nm layer of copolymer which should be sufficient for lifting off over a 150 nm metallic layer. The recipe used for creating this layer spins at 500 rpm for 5 seconds first to spread the resist and then spins at 4000 rpm for 45 seconds. The vacuum should be turned off before the sample can be removed from the chuck.

Step 4: Soft baking Copolymer

The sample is then baked on a hotplate set to 120 ºC for 60-90 seconds.

Step 5: Spin on 50 nm PMMA.

A layer polymethyl methacrylate (PMMA) resist is spun on next. To achieve the highest possible resolution, it is desirable to use a thin layer of imaging resist. The sample is once again positioned on the spin coater as previously explained in step 3 and the vacuum is turned on. This time the liquid dispensed is the MicroChem 950K PMMA A2 which consists of 2% of solids in anisole.. The two-step recipe consists of spinning at 500 rpm for 5 seconds to spread the liquid followed by spinning at 4000 rpm for 45 seconds. This results in an approximately 50 nm layer.

Step 6: Soft baking PMMA

The sample is then baked on the hot plate at 180 ºC for 60-90 seconds.

Step 7: Sample Marking

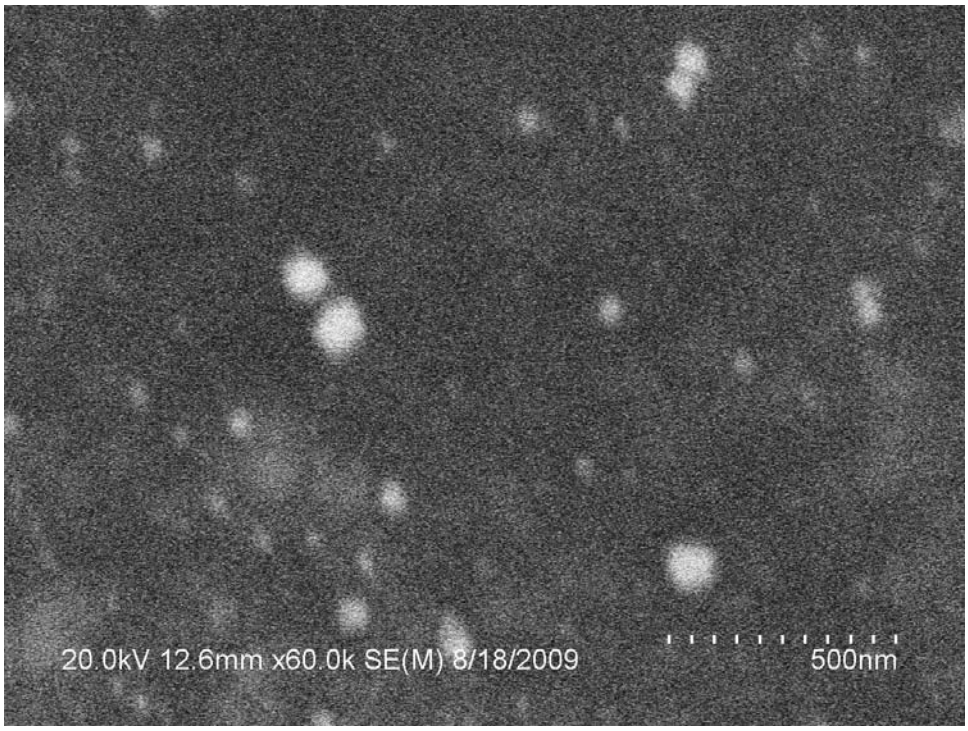


Figure 14 SEM image of gold nanoparticles, suggested as a potential means of beam focusing and refining in electron beam lithography

In further preparing the sample for patterning by electron beam lithography, a small scratch is made on a corner of the sample using a diamond scribe. This imperfection on the sample surface will create a feature to focus and refine the electron beam on and it provides a locating mechanism for a pattern written close-by. In essence, the presence of some sort of focusing or alignment marks on the sample is a necessity. Alignment marks could be patterned on the substrate using photolithography prior to its preparation for an electron beam patterning. Another possible method of providing small features on the substrate for focusing purposes is to deposit a small drop of a

solution of gold nanoparticles at the end of the scratch described above. These particles, being on the order of 20 to 50 nm, require a well-focused beam of electrons to be distinguished on the surface. Such a beam is necessary for the writing of fine features. Figure 14 shows a scanning electron microscope image of gold nanoparticles deposited on a silicon substrate.

Step 8: Sputtering discharge layer

Since both the fused silica substrate and the resist layers coated on it are insulators, they are prone to charging when bombarded with a beam of electrons. This phenomenon is examined in detail in chapter 4. In an attempt to dissipate the charge build-up, a thin conductive layer can be coated over the resist.

In this case, a 10 nm layer of gold is sputtered on the sample using the Denton Sputterer. The sample is placed on a clean 6 inch dummy silicon wafer and placed into the Denton's vacuum chamber which is pumped to a presser lower that 1×10^{-5} Torr before any deposition occurs. The recipe parameters for depositing gold are as follows:

- Pressure = 5 mTorr
- DC1 = 0.2 A
- RS = 50%
- Heat = NO

The deposition rate is measured regularly and can vary each time the targets are changed. In general the rates can be anywhere from 3.5 to 4.3 A/s. The deposition is time controlled and the time it takes to deposit any amount of metal is calculated using the most recently measured deposition rate and entered into the recipe.

In depositing the metallic discharge layer, it must be taken into consideration that electron beam evaporation cannot be used as this may expose the electron sensitive resist.

Step 9: Writing first layer

Thus prepared, the sample is now ready for the first electron beam lithography patterning step. The system used consists of a Hitachi SU-70 SEM and Nabity Nanometer Pattern Generation System (NPGS). The system also makes use of a Deben PCD beam blanking unit and an automatic stage which can be controlled using NPGS during the write. The sample holder for this system can accommodate samples of approximately 1 cm x 1 cm. Therefore the fused silica substrates used in this fabrication were cut to nearly that size to be able to fit on the sample holder. The sample is mounted and held in place using clips available for this purpose on the sample holder or, alternatively, by using carbon tape. The sample holder can then be loaded into the microscope.

The microscope is then turned on and the acceleration voltage is gradually increased to reach 30 kV. A condenser lens value of 16 is chosen to provide a current of 375 pA. This is the highest condenser lens available on the system and it provides the lowest possible current. The values of the current for each condenser lens are measured and provided for use in lithography.

The electron beam is then centered and the Deben unit is used to set the deflection coils to the blank position. At low magnification, where large areas of the sample can be seen, the scratch placed on the sample can be found. It is necessary to approach the sample from the side to avoid exposing the resist. Once the scratch, or other alignment and focusing features placed on the sample, is found, the feature is used to focus and refine the beam as the magnification is slowly increased up to a point when a field size 1 μm or smaller is reached. While focusing, special care must be taken to correct the

beam astigmatism as much as possible. A well focused beam without astigmatism and capable of distinguishing very small features is necessary for successful lithography for writing small features.

Upon adjusting the beam to satisfaction, control of the microscope is relinquished to NPGS and the beam is blanked using the software. The beam is also turned off using the Deben beam blanking unit. The pattern can now be written by running the prepared runfile for this purpose. The magnification of the microscope is set to match that specified in the run file. The magnification affects the size of the writing field: At 1000x, the field size is 90 µm. This means that any pattern larger than this field size will have to be fractured into smaller field sizes and each of these is then written on its own with the stage moving from one exposure field to the next. By putting the fractured segments together, the subfields can thus be stitched into the full pattern. The NPGS software can handle the fracturing if the runfile is suitably prepared for this purpose. The software can also control the automatic stage to enable the sample to move to its correct next exposure field. The beam current, as specified by the chosen condenser lens, is also specified in the runfile as well as the exposure doses to be delivered to the various features in the layout. These parameters, as well as the size of the pattern, define the amount of time the pattern writing will take. Other factors that influence the total exposure time are the stage movement time and the beam settling time between the fields. Other than the extra time added by the existence of a large number of fields, these are also liable to introducing pattern writing errors.

Once pattern writing is completed, the sample can be unloaded from the microscope.

Step 10: Removing gold layer

A wet chemical etch is used to strip the gold conduction layer. Working at the acid bench, the substrate is immersed in the etchant for a few seconds to remove the thin

layer of gold. It is then thoroughly rinsed with de-ionised water and blown dry with nitrogen.

Step 11: Developing resist

The developer used is a mixture of one part methyl isobutyl ketone (MIBK) to three parts isopropyl alcohol (IPA). The sample is immersed in this developer for 60 seconds and then rinsed with IPA for 20 seconds and blow-dried using nitrogen.

Step 12: Hard baking

The sample is then post-baked on a hot plate at 100 ºC for 60-90 seconds.

Step 13: Depositing chrome by evaporation

The first layer of the diffractive optical element pattern has now been transferred to the resist stack. The next step is to transfer this pattern into a chrome mask. For this purpose, 100 nm of chrome is evaporated on to the sample by electron beam evaporation.

Step 14: Lift-off

The sample is then immersed in acetone to perform lift-off. After some time, the solvent dissolves the underlying resist layers and allows the metallic layers over them to separate when rinsed. This leaves the reverse pattern to the one written left behind in metallic relief on the fused silica surface.

Step 15: Cleaning

Once lift off is complete, the sample should be cleaned using the procedure in step 2.

Step 16: RIE 425 nm

The chrome layer can then be used as a mask to transfer the patter at last into the substrate itself. To etch the glass, reactive ion etching is used to create straight and smooth side walls. A recipe of CHF_3 and Argon chemistry called Nanottools Fused Silica Etch is run on the Applied Material P5000 tool. The etch is time controlled and the etch rate is approximately 90 nm/min. The target etch depth of this step is 425 nm. The details of the etch recipe are as follows:

- Step 1: Stabilization
    - Time = 15 seconds
    - Pressure = 50 mTorr
    - RF Power = 0.0 W
    - Magnetic Field = 0.0 Gauss
    - Mixture: CHF_3: 30 sccm, Ar: 70 sccm
- Step 2: Etch
    - Time = ~283 seconds
    - Pressure = 50 mTorr
    - RF Power = 250 W
    - Magnetic Field = 70.0 Gauss
    - Mixture = CHF_3: 30 sccm, Ar: 70 sccm
- Step 3: Residue Evac
    - Time = 10 seconds
    - Pressure = Throttle open
    - RF Power = 50 W
    - Magnetic Field = 0.0 Gauss
    - Mixture = Ar: 70 sccm

As the tool works with 6 inch wafers, the sample must be mounted on one. A clean silicon wafer is placed on the hot plate and heated. A water-soluble wax, Crystalbond555, is melted over a small area at the centre of the wafer and the sample is attached there, staying in place as the wax solidifies in cooling down. Thus mounted, the wafer is placed into the loading cassette, moved into the vacuum chamber and the RIE recipe is run. Subsequently, the wafer is unloaded and placed once more on the hot plate to detach the sample. The wafer and sample are both rinsed with deionised water.

Step 17: Wet etching of chrome

The chrome mask on the glass can now be removed using a wet etch by immersion in the Cyantek Cr-7S chemical chrome etchant at the acid bench. Once all the chrome has been removed, the substrate is rinsed with DI water and blown dry using N2.

Step 18: Sample cleaning

The sample needs to be thoroughly cleaned as previously described in step 2 in preparation for the second layer processing.

The patterning of the next layer is, in many ways, quite similar to the first layer as it employs all the same processing steps.

Steps 19-22: Spinning copolymer EL-11 and PMMA 950K A2

Steps 3-6 are repeated to coat 500 nm of copolymer and 50 nm of PMMA onto the sample and soft bake each layer.

It is at this point worth noting that the sample is no longer perfectly flat and has features that are 425 nm deep. With the 500 nm of copolymer and the 50 nm PMMA, however, it is possible to coat a relatively flat resist layer. This is one reason why it is desirable to pattern the layer with the smaller features and the lower etch depth first.

Step 23: Depositing discharge layer

Repeat step 8.

Step 24: Writing second layer

This time, the lithographic pattern of mask 2 needs to be carefully aligned to that of the mask from the first layer. To help this task, alignment marks were written on the sample as part of the first layer. So in the second round of processing, once the sample has been loaded into the microscope, it is necessary to locate these marks. The NPGS program can be used to locate these marks and they can be used to correct the sample rotation and establish a coordinate system for the stage to use. In this manner, the centre of the pattern can be calculated as its distance from the alignment marks is known. With this information, the second layer pattern can be aligned to and written on top of the first one. The placement of the alignment features relative to the pattern is quite important: First, they must be placed such that they can be relatively easily found; they can then be used for focusing the beam. However, they must be far enough from the pattern so as to not expose the structure itself while the alignment marks are being used for beam focusing and rotation matrix and coordinate calculations. After these adjustments, the exposure itself can be carried out as before.

Step 25-30: Repeat steps 10-15

Once again, the discharge layer can be wet etched. The exposed pattern is then developed, hard baked and lifted off as before.

Step 31: RIE 850 nm

This time, the fused silica is etched to a target depth of 850 nm. Step 16 is repeated with the etch time in the second step of the etch recipe set to 567 seconds.

Steps 32-32: Wet etching chrome and cleaning substrate

Steps 17 and 18 are repeated. After removing the chrome, the four-level diffractive optical element structure is completed.

The process described in this section is the end-result of developing all the individual steps, each of which with their own inherent problems and associated issues to be resolved. Developing the details of these process steps is an important part of achieving a working final product. The following chapters will discuss various steps in this process and their problems and developments in further detail.

3.3 Mask Creation

A key part of the process is the creation of the masks used in patterning by e-beam lithography. The profile described in section 3.1 exists as a mathematical description of zone periods and the widths of the various levels in each zone. This mathematical description must then be converted into masks such as the ones appearing in figure 12.

The exact layout of this mask is dependent on the process chosen. The chosen e-beam resist in this process is PMMA which is a positive resist. This means that those sections of the layer exposed to the electron beam will wash away in the developer and open

windows to the surface below, while the unexposed sections will remain on the substrate. If the resist and the pattern written and developed into it are being directly used as a mask for etching the substrate, then the actual pattern must be written. However, if the etch selectivity of the resist material is not appropriate for a direct etching of the substrate given the chosen etching method, the pattern first needs to be transferred into a metallic layer which will then be used as the mask for etching the substrate. This is the case in the current project. The chosen method of patterning the metallic mask is by lift-off. This method has the property that it reverses the pattern. Therefore the mask has to be carefully created to actually write the reverse pattern in an attempt to get the real one after etching into the substrate.

The raw data describing all 2010 zones in this diffractive optical element has been organized within an Excel spreadsheet. To convert this data into a digital graphical mask, a mask design program by Design Workshop called dw-2000 is used. This program includes a scripting language called GPE which facilitates the automatic generation of large, repetitive structures.

To commence the conversion of raw DOE data into a mask, a MATLAB program was written to read the Excel file and import the data into MATLAB. This program uses the data to calculate the size and location of the various mask features. It also generates the GPE script used by dw-2000 and saves it to a text file. The contents of this file can then be transferred to a GPE file which is the format used by dw-2000. Running this script at the command prompt in dw-2000 generates the patterns and features as calculated by the MATLAB program from the DOE description.

Each of the two masks necessary in this process can be created using a different MATLAB program that makes the necessary calculations for that level and creates the corresponding GPE files.

Once the masks are created as dw-2000 structures, they can be saved as GDSII files. This is a universal format used for mask creation within the various industries utilizing lithographic technologies. The GDSII format can then be read by DesignCAD Express 16. This is the program used by NPGS for the design of patterns used for lithography. DesignCAD Express can convert the GDSII file into a DC2 file. It can also check the pattern for any errors which would impact its writing, calculate the maximum magnification at which the pattern can be written without being broken up into smaller sub-fields, and position the pattern appropriately to maximize this magnification using a function available in the software called MaxMag.

The designed diffractive element is 2551 μm wide and 1000 μm high. The height is chosen arbitrarily as resulting in a reasonably sized device on which a laser light can be shone to test its properties. According to DesignCAD Express, the maximum microscope magnification allowed for fitting the entire structure in one single field would be around 35×. It is, however, customary to perform lithography at magnifications such as 500× or 1000× or higher.

Chapter 4: Electron Beam Lithography

All methods of fabricating nanoscale devices generally consist of various steps of pattern transfer. Lithographic methods are the starting point of transferring any design onto a substrate. Electron beam lithography, often abbreviated e-beam lithography or EBL, consists of scanning a beam of electrons over a surface coated by a film known as a resist which is in some way sensitive to it. The properties of this resist layer have a significant impact on the outcome of the lithography. EBL is particularly suited to the creation of very small features. The technology has some very distinctive characteristics. It is known for being capable of achieving very high resolutions. It is a very flexible technique as it can work with a variety of materials and the patterns can be easily created digitally, eliminating the need for physical fabrication of lithographic masks. There are also some major drawbacks associated with the technique. Firstly it is quite slow in comparison with optical lithography techniques. This in turn makes e-beam lithography unsuitable for high throughput or mass manufacturing. In comparison to photolithography, electro-lithography is also a much more complicated technology. Finally, It is quite expensive; the equipment can cost millions of dollars and requires frequent maintenance to remain in good working order. [24]

The development of this e-beam lithography process is desirable because EBL is a suitable technique for creating prototypes of microoptical and nanooptical elements which can be used in integrated systems. The ability of the system to created submicron critical features along with the flexibility of easily modifying and testing designs make it the method of choice for research purposes for the creation of new integrated optical microsystems.

This chapter discusses e-beam lithography technology. A general overview of systems, materials, techniques and difficulties is given. Particular attention is given to the EBL system used in this project and various process development considerations.

4.1 Systems

A typical e-beam lithography system is composed of a number of different components. The electron beam is formed and shaped in the column with the help of various stages of electrostatic and magnetic lenses. The beam is scanned across the surface of the sample using electromagnetic deflection coils. A stage, located below the column, is used to move the sample from one writing field to the next. The entire system is kept under stringent vacuum conditions. There is also a set of electrostatic beam blanking plates that are used to deflect the beam out of the optical path of the electrons when necessary. The system electronics, electron beam optics and blanking system are all controlled by a computer which also takes care of other tasks such as aligning and focusing the beam and generating the patterns.

The setting in which an e-beam lithography performs its function is quite critical to its performance. Ideally, this should be a clean and quiet environment. Acoustic noise should be kept as low as possible. Sources of mechanical vibrations such as fluorescent lamps and mechanical pumps should ideally be kept a few metres away from the column. It should also be well isolated from stray magnetic radiation and temperature fluctuations should be kept to a fraction of a degree for best performance.

EBL systems come in various different types. There are a few manufacturers that make dedicated e-beam systems. These include JEOL, Vistec, and Elionix. These systems vary in specification according to application but generally have high stage accuracy, large writing fields and high throughput in the forefront of their features.

Other tools are conversions of scanning electron microscopy (SEM) or scanning tunnelling electron microscopy (STEM) devices. These systems make use of a pattern generator such as the Nabity NPGS and rely on other external hardware and software to

control the beam, stage, and various other necessary components. Such converted systems generally suffer from a small field of view and low throughput. In addition, the SEM stage, not being designed for the specific requirements of lithography, is not perfectly flat and its movement accuracy is lower than that of a commercial system with a laser interferometric stage. On the other hand, relative to the dedicated commercial system, they are considered inexpensive.

The e-beam lithography system for which this process is developed was converted from a Hitachi SU-70 SEM and uses the Nabity Nanometer Pattern Generation software (NPGS), an automated stage and a Deben PCD beam blanker. NPGS is a powerful system as it gives the user great control over a wide variety of parameters pertaining to the patterns and their exposure.

4.2 Resists

Electron beam resists are the media used for transferring layout in e-beam lithography. There exist two varieties of resists. Positive resists are those where the exposure to the beam of electrons breaks down the polymer causing it to dissolve in a developer solution. Negative resists, on the other hand, act the opposite way. The polymer hardens upon coming in contact with the electron beam and the unexposed sections hence get removed by developing. The standard resist used for e-beam lithography is a positive resist known as polymethyl methacrylate or PMMA for short. It is the first material ever used as e-beam resist and is still the benchmark against which all others are compared.

The sensitivity of a resist is a measure of its etch depth as a function of exposure dose. The minimum exposure dose required to remove all the resist at the exposure site is

known as the clearing dose. The sensitivity of PMMA depends on the development solution used. This solution also influences the resolution of the resist. In general, PMMA is a very high resolution resist. Table 1 shows various development solutions for PMMA and their affects on resolution and sensitivity. A mixture of one part MIBK to three parts IPA is often used to attain the highest possible resolutions. The electron beam acceleration voltage is another factor that influences the resist sensitivity in a roughly proportional manner. [24] Thinner resist layers also lead to higher resolutions.

Table 1 PMMA developer solution compositions and their properties

Developer Solution	Resolution	Sensitivity
1:1 MIBK to IPA	High	High
1:2 MIBK to IPA	Higher	Medium
1:3 MIBK to IPA	Very high	Low
MIBK	Low	High

4.3 Exposure Dose

Among other factors, e-beam writing resolution depends on resist thickness and exposure dose. The MicroChem datasheets for their PMMA indicate doses between 50 to 500 $\mu C/cm^2$ to be appropriate, depending on radiation source or equipment and developer used. They also recommend energies corresponding to 20-50 kV, with higher values resulting in higher resolutions. The system in use operates at a voltage of 30 kV. The development process, as previously explained, consists of immersing the sample in a 1:3 solution of MIBK:IPA for 45-60 seconds followed by rinsing in IPA for 20 seconds.

The necessary exposure dose further depends on resist thickness and the pattern itself. It is therefore necessary to perform tests to determine the ideal exposure dose.

One such test was performed on a silicon substrate coated with 50 nm of 950K PMMA. The test pattern consisted of an array of nine wheels. Each wheel has a diameter of 10 µm and the centre to centre separation of the wheels is 30 um. A different dosage is assigned to each wheel: The dose was varied linearly from 5 to 45 nC/cm for the nine wheels. The pattern was written three times with the currents doubling and tripling in the next writes. After development, the results were observed by scanning electron microscopy (SEM) and appear in figures 15 to 18.

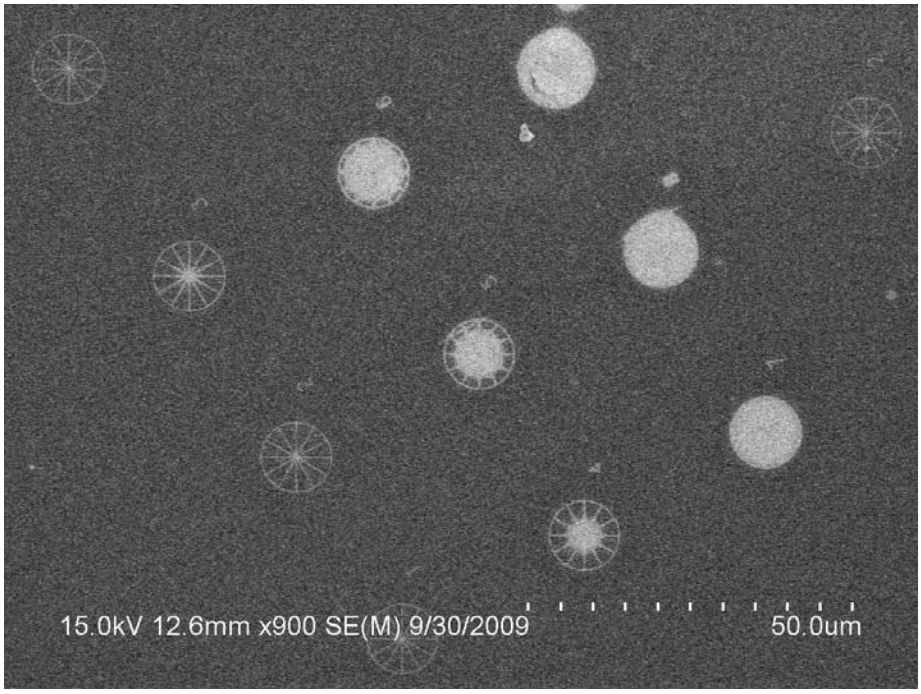


Figure 15 SEM image of array of wheels written by e-beam lithography on PMMA-coated Silicon substrate depicting the effect of increasing exposure dose from 10 nC/cm to 90 nC/cm

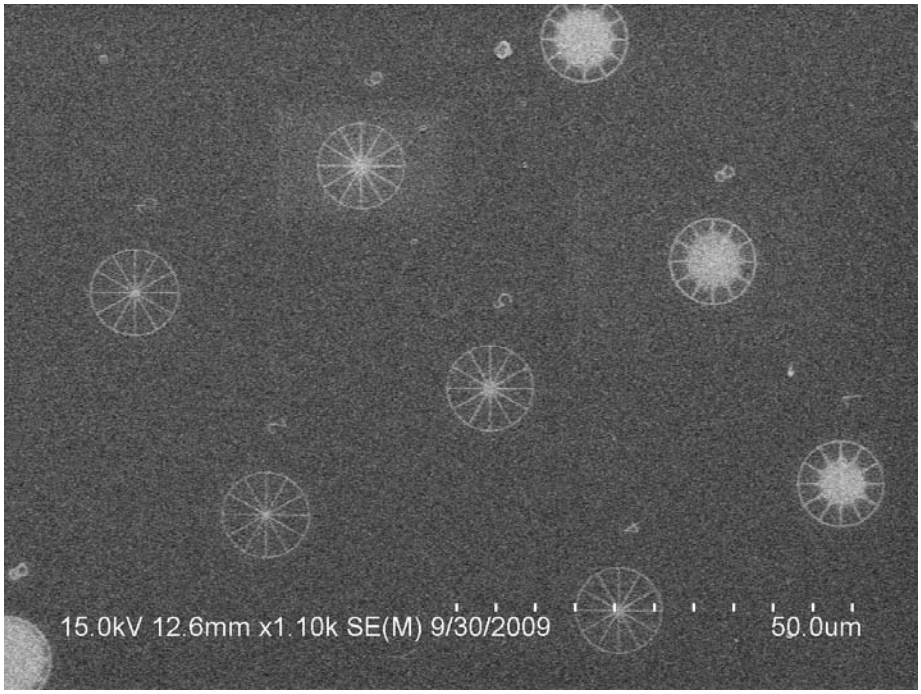


Figure 16 SEM image of the array of wheels exposed with doses from 5 nC/cm to 45 nC/cm

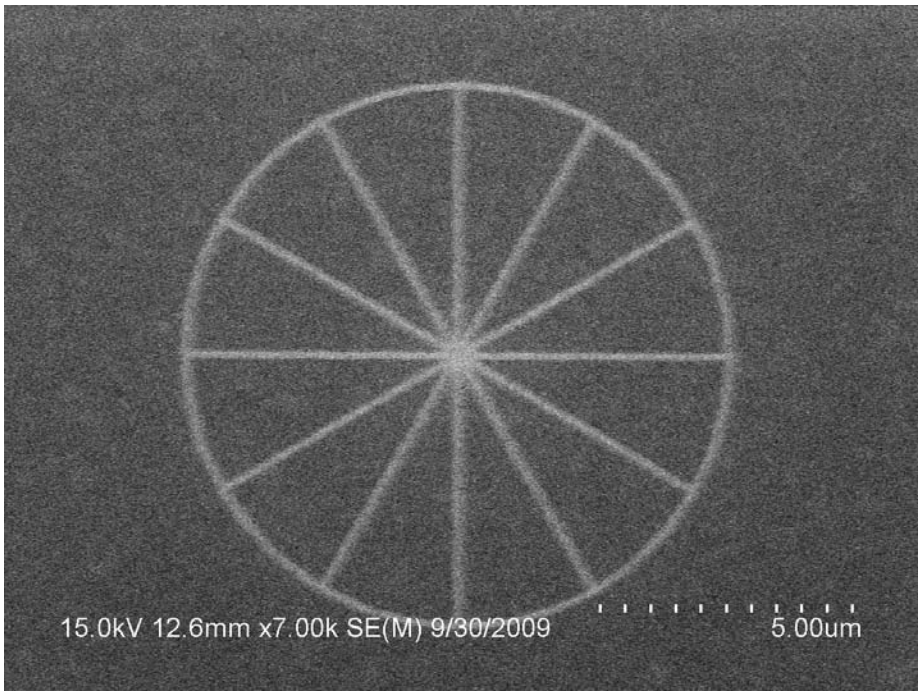


Figure 17 SEM image of a perfectly exposed pinwheel

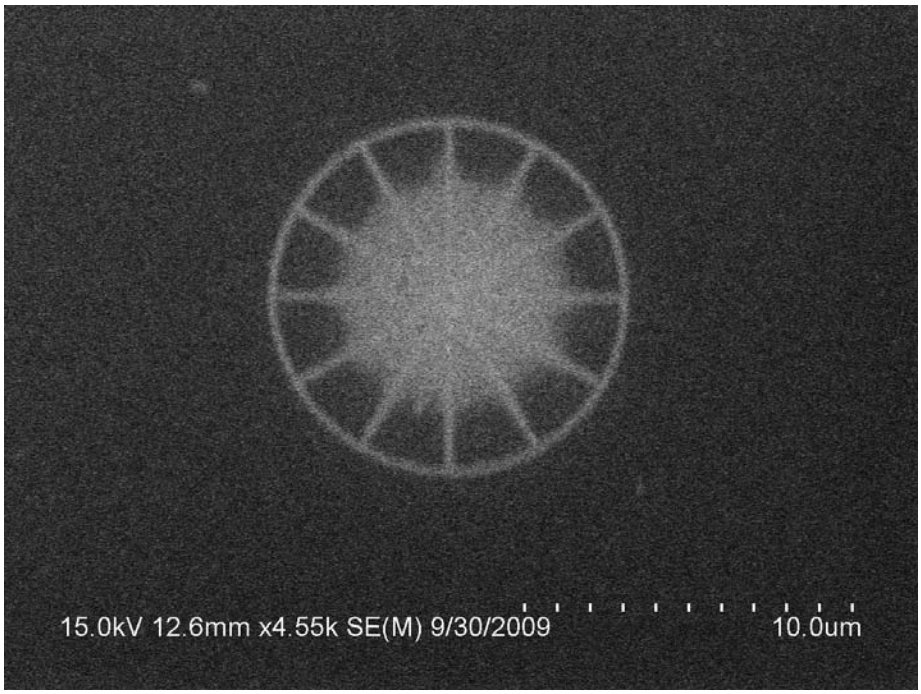


Figure 18 SEM image of an overexposed pinwheel: At the centre of the, where the maximum energy is being deposited, the pattern is lost.

The NPGS software allows dose values to be entered in any of line (nC/cm), area ($\mu C/cm^2$) or point (fC). Different doses get assigned to the different colours in the Design CAD pattern. The software can then use the assigned dose for the assigned pattern element to calculate a dwell time, in us, associated with the pair. This can then be used to get an estimate of the area dose for a line dose or vice versa. In this case, the doses of 5 to 45 nC/cm would correspond, approximately, to 1 to 9 mC/cm^2. These values are clearly much higher than the ones suggested by the manufacturer datasheets which indicate values of 50 to 500 $\mu C/cm^2$. However, it appears from the figures above that the lower doses in this range can produce adequately-exposed and high-resolution lithography for this pattern.

A similar test was repeated to test lower dose values. This time, the dose was varied from 50 to 500 μC/cm^2 throughout the nine wheels. The pattern was written four times with the first array using values half of the indicated ones while the last one used values twice the ones given. The other conditions of the test were kept as unchanged as possible to obtain a useful comparison. This time, it was observed that those wheels written with the lower end of the tested dose range were not written at all. In fact, the entire first instance of the array, which used dose values from 25 to 250 μC/cm^2 was not found after exposure and development. The wheels written with the higher end of the range, roughly 400 to 900 μC/cm^2, produced well-exposed patterns. It therefore appears that for a pattern with nanometre feature sizes, a relatively high exposure dose is necessary for successful pattern writing.

4.4 Exposure Time

Electron beam lithography is a time consuming method of pattern transfer when compared to other methods such as photolithography. The pattern writing time depends on various parameters. The relationship between these parameters can be written as follows:

$$D \times A = t \times I$$

In this relationship, D is the exposure dose, A is the exposure area, t is the dwell time and I is the beam current. [24] As an example, for a 1 mm by 1 mm pattern write area, an exposure dose of 500 μC/cm^2 and writing at a current of 300 pA, the write time is nearly 4 hours and 38 minutes.

Increasing the beam current will aid in decreasing this write time. However, a higher beam current is associated with a larger beam spot size and therefore lower writing resolution.

Likewise, lower doses will also decrease the writing time. As seen in the previous section, the dose necessary for successful pattern exposure depends on various factors itself and must be carefully optimised. However, various tests seem to indicate that doses between 500 and 1000 $\mu C/cm^2$ are likely to be necessary for exposing small feature sizes successfully when coupled with the resist thickness and development procedures used.

In the e-beam lithography system under consideration, the value of the beam current is determined by the condenser lens used for pattern writing. There are 16 condenser lenses. Condenser lens 1 corresponds to the highest available beam current while condenser lens 16 provides the lowest one possible.

It must be noted that the resolution of the EBL instrument is linked to the beam current. Reducing the beam current increases the demagnification of the column, denoted M^{-1}. The beam diameter d_g is given by

$$d_g = \frac{d_v}{M^{-1}}$$

where d_v is the virtual source size. [24] Clearly, increasing the demagnification leads to decreasing the beam diameter which in turn increases the system's resolution.

To better visualize the relationship between the varying parameters, the exposure time as a function of the exposure dose is graphically illustrated for various condenser lenses, and thus various currents, in figure 19 below. For a fixed area of 1 mm by 1 mm, the dose was varied from 200 to 1000 μC/cm^2.

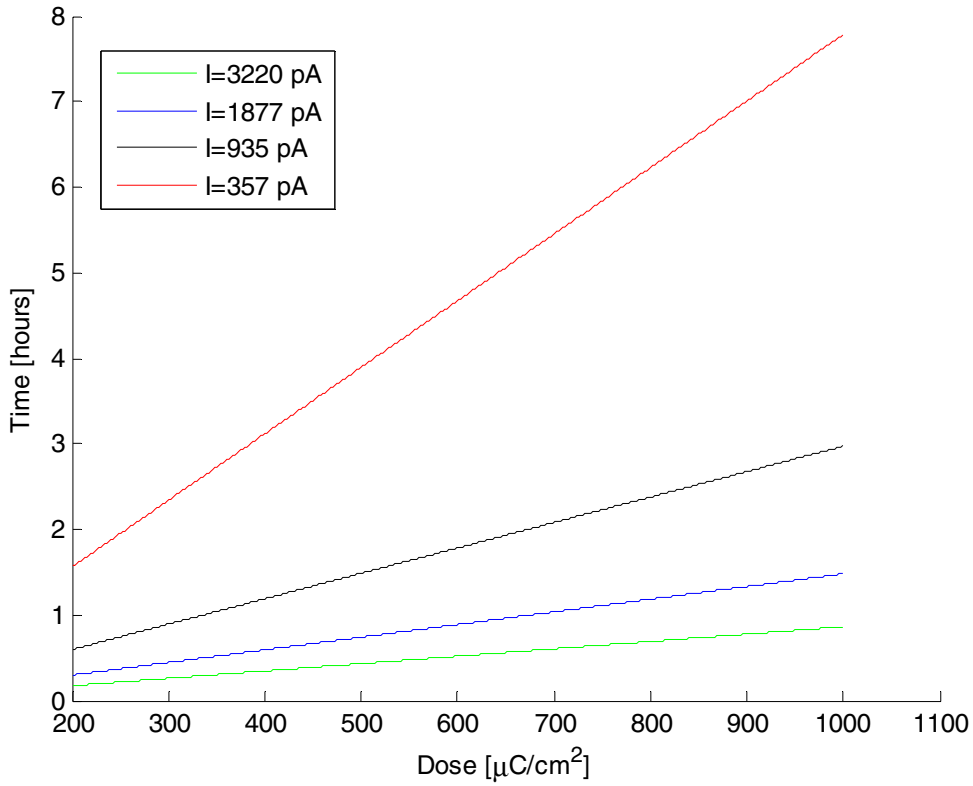


Figure 19 Variation of pattern writing time as a function of exposure dose for various beam currents

In figure 19, the current values correspond to condenser lenses 1, 5, 10 and 16 with condenser lens 16 corresponding to the red curve with a current of 375 pA. These current values correspond to the instrument as measured in July 2010. As a high resolution beam current would be around 500 pA or lower, most of these currents are

much too high for writing small features. Thus the red curve corresponding to condenser lens 16 is the most appropriate one to be considered in this case.

Once a DesignCAD pattern and a corresponding runfile have been created, NPGS can also calculate the pattern writing time. For instance, for the level one DOE mask, a beam current of 375 pA and an exposure dose of 500 $\mu C/cm^2$, NPGS calculates the write time to be 4 hours and 41 minutes. Increasing the exposure dose to 1000 $\mu C/cm^2$ increases the write time to 9 hours and 22 minutes. The write times for the second mask are quite similar.

It is notable that this only takes into consideration the pure writing time of the pattern. This factor however is not the only one that influences the total amount of time necessary for pattern exposure. For large patterns where many fields have to be written, the time for the stage to move from one write location to the next must be taken into consideration as well. In addition, the beam needs to settle between the various subfield exposures which adds an extra amount of time. Given a runfile including all the necessary stage movements and alignments, NPGS can deliver an estimate of the entire time necessary to fully expose the pattern. For instance, for the first layer mask written at a magnification of 1000x at 500 $\mu C/cm^2$, the estimated write time is 5 hours and 30 minutes. The software estimated each stage movement would take 5 seconds and did not take any other delays into consideration.

4.5 Sources of Error in Pattern Writing

4.5.1 Fracturing, Stitching and alignment

As discussed, it is often necessary to break down a pattern destined to be written by e-beam lithography into many smaller patterns. This arises due to the field size of the lithography system and the fact that it is often smaller than that of an entire pattern. The field size depends inversely on the magnification at which the pattern is written: at higher magnifications, the field sizes are much smaller. In the SEM system being used in this process, a field size of approximately 90 µm is associated with a magnification of 1000x. So a larger pattern has to be broken up into sub-fields approximately 90 µm across. This process is referred to as fracturing. To minimize the number of fractures, it is desirable to work at the highest possible field size available. The lowest end of the high magnification spectrum of the microscope is around 500x. This thus ends up being the magnification of choice to perform lithography at.

To obtain perfect scaling between the SEM and NPGS at the writing magnification, the system has to be carefully calibrated. Calibration must be performed for each magnification within each project directory. To account for the angular difference between the stage translational axis and the SEM image, a rotation matrix is calculated. This is essential for stitching and alignment and must be performed every time before writing to a sample with an existing pattern such as, for instance, alignment marks. To accomplish rotation correction, three points on the existing pattern with known distances forming a straight angle are chosen by the user and used by the NPGS software to calculate the rotation matrix. The other component of the calibration pertains to absolute pattern size and is magnification dependent. In fact, the field size at the desired magnification must be measured to obtain the correct MagScale factor for use by the NPGS software. With the rotation matrix and the MagScale factor for the magnification of interest, the system is capable of accurately matching pattern coordinates to stage coordinates for alignment and stitching.

Fracturing a pattern into multiple writing fields is bound to introduce errors in the lithography. As the stage movements are imperfect, pattern matching errors can be introduced at each step. Minimizing the number of writing fields is clearly desirable to minimize the errors that can possibly be introduced in the pattern. This is why the magnification of 500x is preferable for writing than 1000x.

NPGS automatically fractures the layout if a runfile is created using the fracture mode. This mode allows the size of the write field to be specified by the user. Additionally, the user can define a border for the subfield. If a sufficiently large border is specified, patterns at the edge of the specified field do not get broken into the next one. Instead, if the entire pattern element can fit within the specified border, it does not need to be fractured. This feature can greatly minimize fracturing and stitching errors if the border size is properly chosen.

For the DOE layout, the horizontal direction (as defined in mask layouts depicted in chapter 3) has many fine features while the vertical direction is s continuous across the entire 1 mm length of the device in that direction. The different fracturing errors that may be introduced into the pattern as the stage steps horizontally and vertically are illustrated in figure 20. The solid squares indicate the different subfields while the dashed squares surrounding them indicate the borders. As seen between subfields one and two, the feature that does not fit within the subfield horizontally can fit within the specified border and hence does not get broken up. Meanwhile, between fields two and three, a vertical gap appears as the feature does not fit within the field or the border and has to be fractured. Whereas blank gaps can appear vertically, they will not appear horizontally if a sufficiently large border is specified. It is also possible for the vertical lines to align imperfectly between fields such as between subfields one and four. Clearly, no border can be specified to minimize fracturing errors along the continuous vertical features of the mask. However, a suitable border can be chosen such that the

pattern elements in the horizontal direction are never broken across subfields. As the feature sizes are quite small in this structure, the border does not need to be large. For the first layer mask, feature sizes do not exceed 400 nm, so a 1 µm border can ensure fitting the element within the field without breaking it. For the second layer mask, features do not exceed 800 nm so a 2 µm border should be specified to be safe. As the errors in the vertical direction cannot be compensated for in this manner, we can expect to see stitching errors in that direction. These errors are dependent on the accuracy of the stage. In the system in question, stitching errors on the order of around 200 nm can be expected. As some of the feature sizes in this design are around that size themselves, this error is likely to be problematic in the functionality of the device.

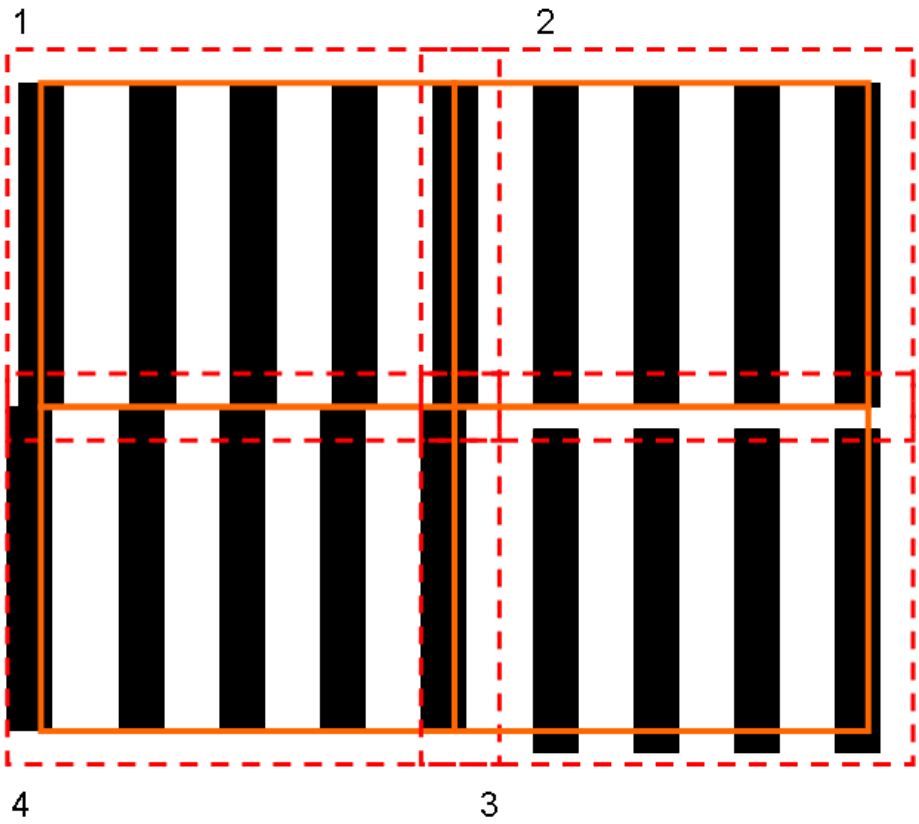


Figure 20 Stitching errors in different features as the stage steps horizontally and vertically. The solid squares represent the subfields and the dashed squares indicate the borders around each field

A different method of eliminating stitching errors is to take measures to specifically align the subfields to one another. For this to be accomplished, each field requires its own alignment marks. If such a mark exists within the field, the software can be directed to locate this alignment mark. For this purpose, a window has to be specified within each subfield containing an overlay mark. The overlay mark matches the alignment mark existing on the sample and the pair can be matched to ensure perfect pattern placement and error-free stitching. There are various problems associated with this procedure. One is that the necessary periodic alignment marks must somehow be created on the substrate prior to the e-beam lithography step. This requires additional processing and is often accomplished by photolithography. The mask necessary for photolithography must be fabricated which constitutes an additional cost. Aberrations and errors can be introduced during the optical lithography step that could compromise the alignment. Finally the finding of the alignment marks by the electron beam lithography system and the process of aligning to them constitutes additional steps and will increase both the complexity of the writing job and the total writing time.

Pattern overlay consists of the task of aligning a pattern to a previously existing one on the sample. Perfect alignment between layers for multilayer structures is one of the key parts of achieving a working device.

One demonstration of alignment between subsequent exposures using NPGS is discussed in [25]. The initial layer is positioned using a scratch across the sample and tick marks to further provide location indicators. Alignment features are written along with this layer's pattern. After development and etching, these marks can be used to align the second layer. Various alignment windows and overlays are defined in NPGS layout for the second layer. The windows are generally twice the size of the alignment marks

so that if any portion of the mark is visible through them, it can be positioned precisely against its corresponding overlay. This procedure provides quite precise alignment between marks written in the first layer and the second layer. It is necessary, however, for the windows to be roughly in the correct location to begin with for the software to be able to align the marks with the overlays. Manually locating these general locations will lead to the resist in this area to be exposed since the only method of locating features is by SEM imaging. To work around this problem, a sacrificial alignment pattern is also written during the first exposure in an unimportant area relative to the final device. This pattern can be found using SEM imaging and the microscope field can be rotated and aligned to these features. Once this is accomplished, the position of the actual pattern relative to these features is known and the stage can be moved to that location after the beam has been blanked to avoid exposing that area.

This method is similar to the one proposed in chapter three for the alignment of the second layer of the diffractive optical element in that a sacrificial alignment layer should also be written during the patterning of the first layer of the DOE. These alignment marks can then be located and the location of the pattern relative to them can be calibrated and defined. In this manner, the stage can be moved to the correct coordinates. This method is not likely to provide very accurate alignment. The accuracy of the stage is not sufficient to ensure that the perfect coordinates can be defined and located. The DOE pattern is a continuous layout covering an area of $2551 \times 1000\ \mu m^2$. Alignment marks cannot be written within this area itself as they will compromise the pattern of the structure and its operation. Therefore, once this layout broken into its various writing sub-fields, it is not possible to provide each field with its own alignment window and overlay to ensure that each subfield is perfectly aligned to the previous lithographic layout. It is possible, though, that the addition of alignment windows and overlays coupled with alignment marks around the edges of the device layout will improve alignment accuracy between the first and the second layer.

In summary, there are basically two components to alignment with e-beam lithography. The first is the correction for the placement and rotation of the piece with respect to the SEM and stage axes. The second is the correction within each subfield of the pattern. Figure 21 shows a set of alignment marks that can be patterned onto a sample by, for example, photolithography to be used during e-beam alignment. The marks are either etched into the sample or coated by metals such as gold, platinum or tungsten. The four marks around the edges, labelled 1, serve for global rotation and position correction. The L-shaped marks can be used within each subfield to position it absolutely relative to the adjacent fields. [24]

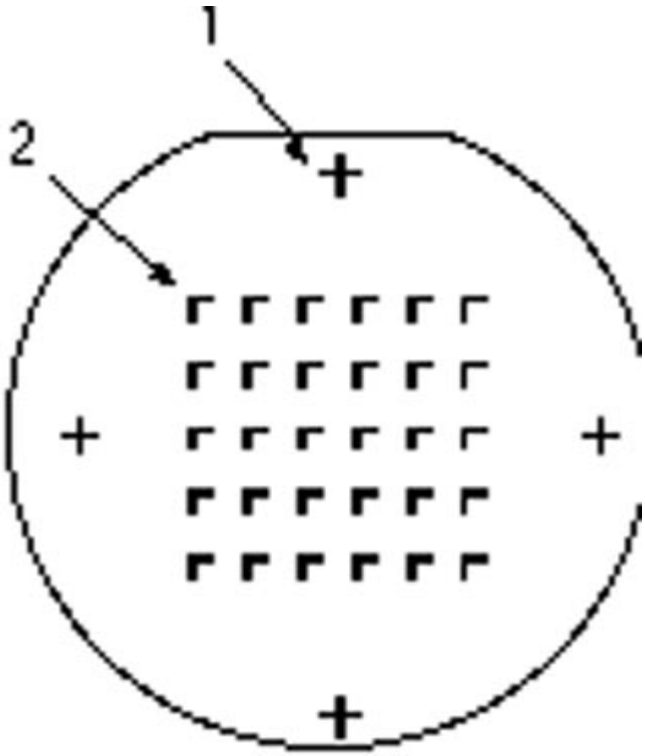


Figure 21 EBL alignment marks: (1) Global marks (2) Chip marks [24]

4.5.2 Charging Effects

Electrons are negatively charged particles. Unless they can easily and quickly find a path to ground, these particles will accumulate within the substrate. A negative charge accumulation can cause pattern writing and positioning errors: the negatively charged beam of electrons will be repelled by the negative charge accumulation. As a result, it may be moved from its correct position and an erroneous section of the resist may therefore get exposed.

The distance the electrons travel through the resist and subsequently the substrate is clearly directly proportional to electron beam energy. For a low energy beam, the particles will travel a shorter distance and are thus likely to accumulate within the resist. Unsurprisingly, the amount of accumulation increases with resist thickness: Thicker resist layers get more highly charged. For a higher energy beam, however, the particles will travel into the substrate. In this case, the more conductive the substrate is, the more easily can the electrons find a path to ground and thus discharge the sample. For a silicon substrate, this happens relatively quickly, while it is significantly slower for a quartz substrate.

It is desirable to provide these particles with a method of quickly accessing the ground in an attempt to minimize charging and as a result minimize charge-induced pattern distortion. For charge accumulation within the resist, a thin metal layer above or below this layer can provide the necessary conductive path for the electrons to use and eliminate their accumulation within the resist. This is because the particles are stopping close enough to the conductive layer. However, for electrons that travel deeper into the substrate, such conductive layers are of limited use as the particles do not stop close enough to access and use it. This means that a thin resist layer on a conductive

substrate is unlikely to charge significantly enough for a discharge layer to be required, while a thick layer on the same substrate will require a means of discharging.

4.5.2.1 Studies and Simulations

The effect of charging in insulating substrates was studied by Cummings et al in 1989. [26] They demonstrated that pattern deflection errors are significantly reduced when writing at 50 keV in comparison to writing at 20 keV.

In their 1995 paper, Liu et al study resist charging for beam energies for up to 10 keV for various conditions such as different resist thicknesses and exposure doses. They used a quartz substrate with chrome coating so their substrate itself should be considered conductive. Their findings demonstrate that for the same value of beam energy, a thicker resist layer will be charged more negatively than a thinner one. For the same resist thickness, the negative potential across the resist decreases as the beam energy is increased. In fact, they show that for each thickness, the negative potential approaches zero and after a certain beam energy, the resist becomes positively charged. It can be seen that at high energies, there will be a positive surface charge on the resist. They also demonstrated that the addition of a conductive layer on top of the resist effectively eliminates the resist surface potential meaning the layers successfully dissipates the electrons. [27]

Similar experiments were carried out on resist-coated silicon substrates by Bai et al in 1999. Their resist thicknesses varied from 0.15 to 1.3 µm and the same general trend of increasing negative surface potential after exposure with increasing resist thickness was observed. Similarly, higher electron beam energies also led to less negative surface potentials and these can in fact assume positive values. The electron beam energies used are 10 and 20 keV. It is found experimentally that the surface charging is dose-

independent for the 1-4 μC/cm2 dose values used in these trials. The authors also described and implemented a model for the charging that occurs in the resist to lead to the surface potential. This model agrees with the overall experimental results. [28]

Clearly the formation of a positive potential on the top layer of the resist is a surprising result. It is however quite consistently repeated in all experiments.

Calculations of the surface potential and the resultant beam deflection were carried out by Lee et al in their 2000 paper. [29] They show that electron beam deflection is minimum at the point of minimum surface potential. This then confirms the desirability of zero surface potential during electron beam exposure. The addition of a top surface conducting layer is deemed necessary to avoid the charging effect.

According to the simulation results in [30] and their comparison to various experimental results, the surface becomes more and more negatively charged with increasing resist thickness. For a given resist thickness, increasing the beam energy leads to a less negative surface potential. There is a point at which the zero surface potential condition is fulfilled. This means that for a certain resist thickness and at a certain beam energy, the surface charge will be zero. Deviating from this point will lead to either a positive or negative surface potential depending on the changes made on the aforementioned conditions. For PMMA thicknesses from 100 to 400 nm and beam energies up to 5 keV, simulation results demonstrate that the surface potential at any energy is always minimized for the thinnest resist layers. Meanwhile, increasing beam energy will always minimize the surface potential: for the simulated thicknesses, the surface potential approaches zero at 5 keV. The simulation results also show that beam deflection is minimized for higher beam energies.

Clearly charging effects are a lot more noticeable and problematic in lithography at the lowest voltages. As beam energy increases, the electron penetration depth increases. Thus at lower energies and for thicker resists, the electrons will have difficulty in penetrating through the resist and reaching the substrate. Thus for high energy exposure with relatively thin resist thicknesses on a grounded and conductive substrate, the charging in the resist will be negligible and will not lead to significant beam deflections resulting in pattern displacement or distortion. In 2003, Bai et al [31] performed experiments using PMMA thicknesses of 0.4 to 1 µm at beam energies of 10 and 25 keV on n-type silicon substrates and observed essentially zero surface potential and pattern displacements of less than 20 nm. Simulations showed that the maximum penetration depth of a 10 keV electron beam in PMMA is around 2.4 µm and around 12.5 µm for a 25 keV beam. These values are both much greater than usual PMMA thicknesses.

4.5.2.2 Charge Dissipation

A method of charge dissipation is required to enable the achievement of correct pattern placements and the elimination of errors attributed to substrate charging in electron beam lithography. The two approach taken to this end has been the addition of a conductive layer either above or below the resist layer and both polymer and metal conductors have been studied. As discussed, the amount of charge accumulated on and within the resist layer depends on many factors such as the layer thickness (single or multiple layers), substrate type and electron beam energy.

One method of dissipating the charge built up within the insulating resist layer was proposed and tested by Dobisz et al in 2003. [32] A process for coating approximately 15

nm Cu discharge layers unto insulating substrates was described. It was demonstrated that this layer effectively eliminates pattern placement errors when placed below the ~500-nm resist layer while writing at an electron beam energy of 50 keV.

A study of thin metal overlayers in 2008 [33] examined the effect of a thin metallic conductive layer over PMMA resist. Such a layer can be used as a discharging mechanism for the resist. However, it is important to characterise any possible effects the addition of such a layer would have on the lithography. The authors examine the effects of the addition of a 5 nm layer of Al, Cr, and Cu respectively. Electron beam energies from 2 to 30 keV were considered. They found that although the additional metallic layer increases the clearing dose for the PMMA resist, it has little adverse effects on resolution, linewidth and contrast, especially at beam energies higher than 5 keV.

Metallic overlayers are preferable to underlayers since they are more easily removed after exposure. Sandia National Laboratories uses a 5-10 nm Au layer over the PMMA resist as a charge dissipation layer. The Au can subsequently be etched chemically and the sample can then be developed. Although a metallic layer under the resist works quite well for dissipating accumulated electrons, it introduces extra complications into the process as the resist pattern has to be transferred into it. [22]

The use of electrically conductive organic polymers as a discharge layer for e-beam lithography was first described in 1989. [34] The authors make use of 200 nm of their conductive polymer under 1.2 µm of imaging resist and find that a conductivity of 10^{-4} S/cm is sufficient for fully discharging the charge built up within the resist. It is observed that this layer is sufficient to eliminate all pattern placement errors. The samples that did not use a discharging polymer, however, had pattern placement errors greater than 5 µm. It is important to note that the thick imaging resist layer used in this study is

prone to great charge build up. The electron beam energy used was 25 keV and the writing dose was 15 $\mu C/cm^2$. As these are conventional exposure conditions, the affectivity of the layer for charge dissipation in usual pattern-writing conditions is confirmed.

In another study, Novolak-based conductive polymer underlayers were synthesized for use with electron beam lithography in 2008. [35] The polymer can exhibit conductivities up to 10^{-4} S/cm. Also, products such as ESpacer from Showa Danko are water soluble conducting polymers that offer novel methods of eliminating substrate charging. [22] A water soluble conductive layer can be used either under or over the resist with equal ease. However, these polymers are generally a more costly solution and are not as readily available as metallic discharge layers which can be easily deposited using standard and readily available clean room tools.

Chapter 5: Pattern Transfer

Once a pattern has been written using some form of lithographic process, the pattern must in turn be transferred to the substrate. This can be accomplished in various ways depending on materials and applications. This chapter gives an overview of pattern transfer processes with emphasis on various methods of substrate etching.

The simplest mechanism for etching a surface is by wet chemical etching. This type of process relies upon the chemical reaction between the material to be etched and the substance used as etchant. The speed of the reaction between the two materials defines the etch rate. For wet etching to work, the material of the resist should not react with the etchant. Most chemical etches are isotropic; this means that the vertical and lateral etch rates are identical. This property leads to an effect known as under-cutting. If the target etch depth is larger than the opening in the resist, the final feature size will be larger than expected due to significant undercutting. This information can be taken into consideration during layout design to minimize the effect of the undercut. Moreover the timing of the etch is critical as overetching will lead to larger undercuts. The sidewalls in wet etching processes end up rounded. Wet etching can be used for patterning substrates or overlying layers. It can also be used to remove residues of sacrificial or mask layers completely. Hydrofluoric (HF) acid is an example of a wet chemical etchant for glass. In crystalline material, it is possible to use a wet etch for isotropic etching of the material. In this case, etch rates depend on crystal orientation. Silicon wafers can be etched anisotropically using potassium hydroxide (KOH).

It is often necessary to etch materials anisotropically. Sharp steps and smooth, straight sidewalls are the requirements in many designs including binary optical devices. For this

purpose, the method of choice is reactive-ion etching (RIE). This technique consists of bombarding the material surface with a chemically reactive plasma. The exact gases used depend on the material to be etched. Table 2 shows some of the etchants generally used for various substrates. [36, 37] The profile of the patterned layer used as etch mask influences the final etch profile: Photoresist with sloped sidewalls will lead to a sloped etch profile. The choice of masking material also depends on the substance to be etched and therefore the chemistry used to etch it.

Table 2 Etch gases for Common Microfabrication Material [36, 37]

Material	Gases
Silicon	CF_4, CF_4/O_2, CF_3Cl, CCl_4, SiF_4/O_2, NF_3, ClF_3
SiO_2	C_2F_6, C_3F_8, CF_4/H_2, CHF_3
Si_3N_4	CF_4/O_2, C_2F_6, C_3H_8, CF_3/H_2
Organic Materials	O_2, O_2/CF_6, O_2/CF_4
Al	CCl_4, CCl_4/Cl_2, $CHCl_3/Cl_2$, BCl_3, BCl_3/Cl_2, $SiCl_4$
Ti	CF_4, $CClF_3$, $CBrF_3$
Au	$C_2Cl_2F_4$, Cl_2
Cr	Cl_2/O_2, CCl_4/O_2

An important property of an etch is its selectivity. This defines the ability of the etching material to attack only the substance to be etched and leave the overlying and underlying layers untouched. In other words, the plasma etchant should be etching the target material at a much faster rate than the masking layer. Knowing the relative etch rates of the mask layer to the etching one, the necessary thickness of the mask layer can be determined for the target etch depth.

Many resists have poor resistance to plasma etching. In particular cases, the resist itself can be used as a masking layer for RIE. For instance, the Shipley S1813 positive photoresist which is used in photolithography can be used directly for the reactive-ion etching of silicon. This was tested using a HBr/Cl2 gas mixture. The etch rate is approximately 300 nm/min and the etch selectivity to resist is around 4:1. However, this same resist is not capable of acting as a mask for the etching of a glass substrate. For this reason, a different mask should be used for glass substrates. Fused silica can be etched using CHF_3. Using a chrome mask is a common solution. In general, the mask material used for RIE should be carefully selected to ensure adequate selectivity.

Before a metallic layer such as chrome can be used as a mask for RIE, the pattern from the resist will have to be transferred to it. This could be accomplished using wet chemical etching of the chrome, but this has the problems of etch depth accuracy and undercutting associated with it as previously discussed and is not generally desired for small feature sizes where the undercutting can be on the same order as the feature size itself. Although dry reactive-ion etching of chrome is also possible, a suitable mask must be found for that process as well.

The selectivity and etch resistance of the PMMA resist is very poor. PMMA itself can be dry etched by use of oxygen gas. The resist layer will therefore not serve as a suitable mask for RIE of either the glass substrate or a chrome mask. Therefore a different method for transferring the pattern into the chrome mask is needed. A different method of achieving this transfer is by means of a process known as lift-off wherein the patterned resist gets coated by a layer of metal and upon removing the resist, the sections of the metal over the resist get detached and removed along with it, leaving behind the segments covering the substrate itself. The solvent starts to dissolve the

resist starting at the edges and lifts off the metal along with it. It is therefore important that there be a gap between the metal and the resist where the solvent can reach it. This can be accomplished by methods of metal deposition where the metal is deposited on those areas where there is a direct line of sight from the source which is located above the sample. As a result, there is usually little or no deposition where there is a straight or inward sloping wall so these remain uncoated to allow the solvent to reach and dissolve the resist. Line-of-sight deposition methods include thermal and e-beam evaporation while sputtering is unsuitable for lift-off purposes as it often covers the side-walls and edges of the resist completely. Of course, line-of-sight deposition leads to shadowing and therefore a rounded profile which is certainly a disadvantage of the technique. [37]

To further facilitate lift-off, it is helpful to create undercutting or inward-sloping resist profiles. This is the purpose of layers such as the EL-11 copolymer for the PMMA or the LOR5B solution which is used in conjunction with the Shipley positive photoresists for liftoff with photolithography.

In summary, to allow the etching of a glass substrate, a metallic (chrome) mask is necessary. Transferring the pattern from the patterned e-beam resist to the chrome mask is best done using a lift-off process. For lift-off to be successful, the metallic layer should be deposited by evaporation and the resist profile should exhibit undercutting or inward-sloping walls. To fabricate such a profile, the e-beam sensitive resist should be undercoated by copolymer.

In an attempt to test lift-off, silicon samples were cleaned and coated with 500 nm of EL-11 copolymer and 50 nm of 950K A2 PMMA, softbaking each layer as needed. The samples were exposed with the wheel pattern previously discussed using a low beam

current but relatively high exposure doses. The samples were then developed as usual in a 1:3 solution of MIBK:IPA, post baked and dried with N2. At this point, the Denton sputterer was used to coat the samples with 150 nm of gold. As previously mentioned, however, sputtering is unsuitable for lift-off processes. However, as deposition by evaporation was at the time unavailable at the McGill microfabrication facilities, sputtering was used in testing the process. The substrates were then immersed in acetone. After approximately an hour of soaking, the samples were rinsed for several minutes by splashing acetone on them from a squeeze bottle. This process seemed to lift off most of the gold. The results were then observed using a dark field microscope. The image of one of the arrays on one of the samples appears in figure 22.

From the dark field images, it was evident that lift-off was incomplete. The samples were thus once again immersed in acetone for over another hour and once more rinsed thoroughly afterwards. They were then imaged using scanning electron microscopy (SEM). Results appear in figures 23 to 26.

The lift-off still appears to be incomplete. This confirms the fact that sputtering is unsuited to lift-off applications. Process development will continue by repeating the lift-off procedure using electron-beam evaporation to deposit the metallic layer. The time necessary for completion of the lift-off also needs to be characterized. Finally, upon completion, features must be measured to ensure the fidelity of the pattern transfer process.

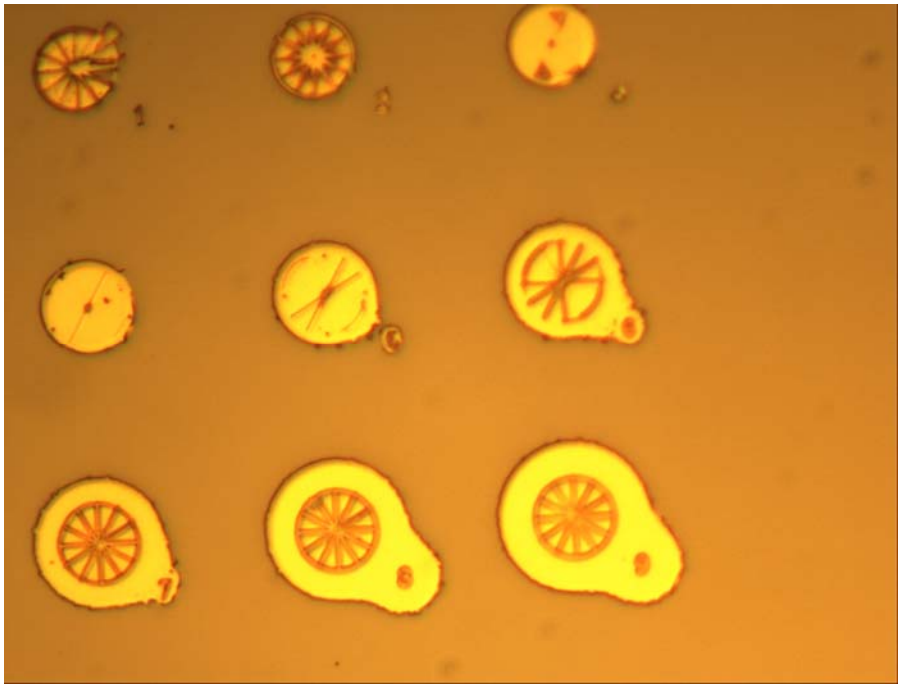


Figure 22 Dark field microscope image of array of pinwheels after lift-off

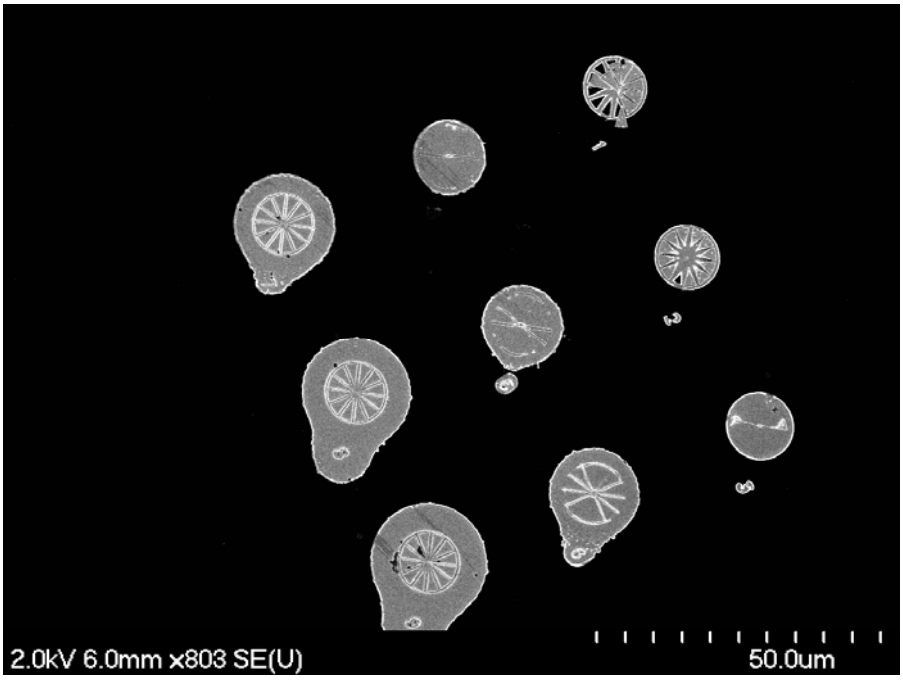


Figure 23 Array of pinwheels after lift-off on sample 1

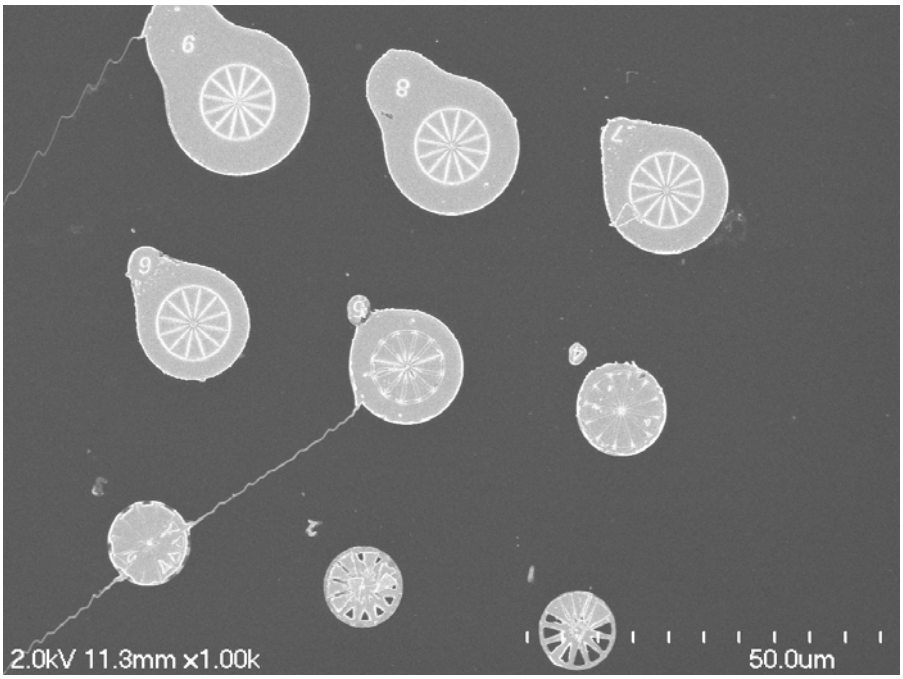


Figure 24 Array of pinwheels after lift-off on sample 2

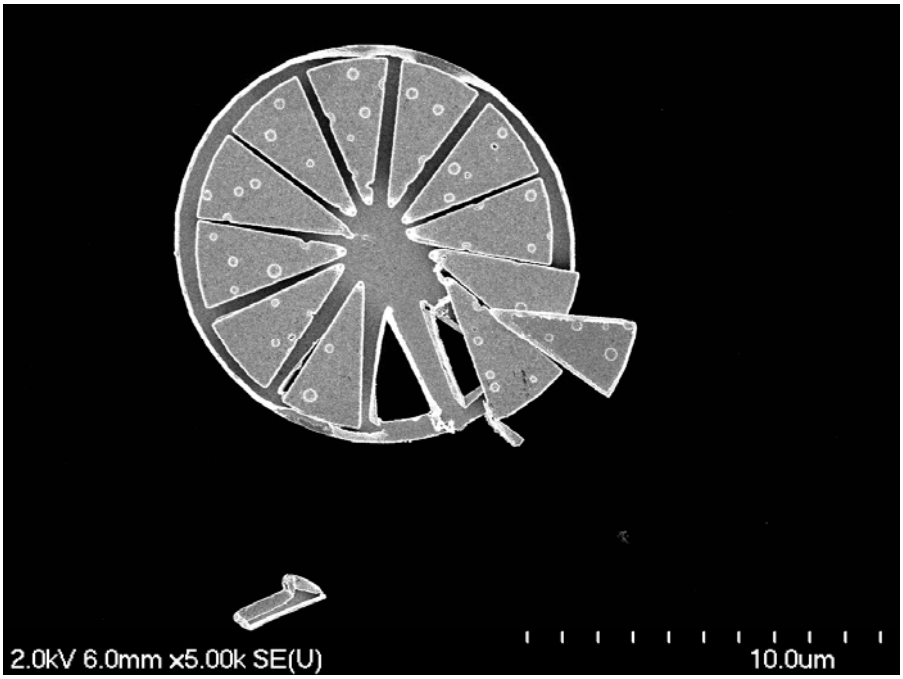


Figure 25 Example of incomplete lift-off from sample 1

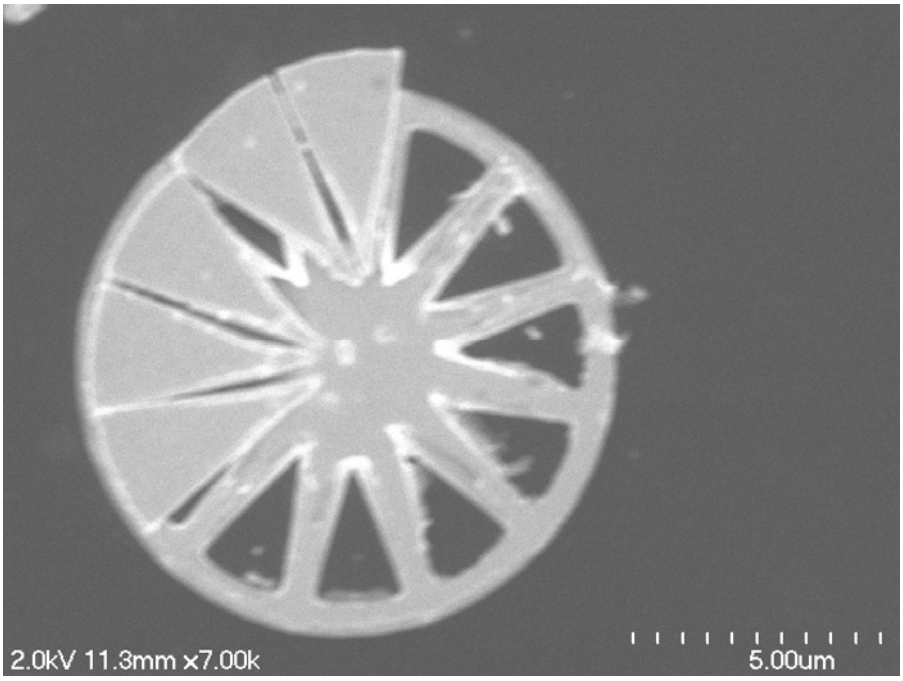


Figure 26 Example of incomplete lift-off from sample 2

Chapter 6: Conclusion

Integrated optical systems represent a highly desired solution to the demands of our present world where there is a distinct trend towards simplification and miniaturization of all systems. Integration leads to simplicity in that it reduces the number of elements in a system. At the same time, it leads to a more compact and lighter setup. As a result, it can be possible to create multiple channels where there was only one in a non-integrated system utilizing many components. Diffractive elements can be used to good advantage in reducing the number of necessary components. They are small and light-weight and an array of them can be tightly packed in a small area such that they can process many channels in parallel. This type of integration has been the main force behind the dreams embodied by microsystems such as the lab-on-a-chip.

Of course, the realization of such dreams has been heavily dependent on the ability to make optical elements with submicron critical features. Electron beam lithography systems have been instrumental in this success as the smallest feature dimensions attainable by optical lithography is fundamentally limited by the wavelength of light used. E-beam lithography therefore holds the key to the implementation of successful integrated microsystems.

Such considerations motivated the main goal of the project presented in this thesis. The aim was to develop a complete process for the fabrication of transmitting diffractive optical elements using electron beam lithography. The process was to use solely resources available within the McGill Nanotools microfabrication facility. Various challenges were met in achieving this goal. Foremost among these was the limitations of the EBL system including the size of the allowable exposure field and the inaccuracies

inherent to the stage movement. The combination of these two parameters led to the introduction of stitching errors arising from writing full elements that are much too large to fit within a single field of the microscope. As the pattern needed to be broken up into many smaller subfields, the stage was needed to move the sample from one exposure site to the next. This movement is prone to introduce pattern writing errors as the various subfields may not be perfectly aligned one to the other. In addition, the existence of multiple mask layers in the target design means that the second layer to be written needs to be aligned to the first one to a very high degree of accuracy. As each layer alone can accumulate its own share of stitching errors, the two layers in turn will have alignment errors between them due to the deviations of each layer from the perfect layout. Meanwhile, alignment errors may also be introduced in aligning the second mask to the alignment features deposited by the first.

It thus appears that a fair number of the challenges faced in this project are related to the limitations of the facilities available at McGill and in particular to the e-beam lithography system. As such, this thesis explains in detail the problems arising from this system and some methods of working around the difficulties that arise. For instance, it is advised to write the device pattern at the lowest possible magnification which corresponds to the largest possible field size for the available EBL system in an attempt to minimize stitching and alignment errors. These limitations are however inherent to the system and, although the conditions that minimize them have been identified and suggested as the optimal working conditions, they cannot be eliminated. The system itself uses an automated stage which goes a long way towards precise placement of the writing fields on the sample. Nevertheless, there are some system limitations that simply cannot be fully eliminated and must simply be taken into consideration in the design and process development for any device using the e-beam lithography system.

In this project, the continuous phase of the diffractive lens was broken up into four discrete levels. This particular number of levels was specifically chosen as it was deemed to be a reasonable compromise between diffraction efficiency of the lens and ease of fabrication, two design parameters which are inversely proportional one to the other. Structures best suited to fabrication by e-beam lithography would ideally consist only of two levels which can be attained by a single patterning steps. This reduces the processing complication significantly and removes some of the sources of errors in creating the device. The challenge would then arise in the design of a two-level structure which can exhibit high diffractive efficiency. Many of the processing steps developed in this project would be identical to any structure meeting the mentioned requirements and can thus be useful in this regards.

Meanwhile, the proposed process addresses many of the challenges faced in the application of other optical elements. For instance, many silicon-on-insulator technologies involve the fabrication of optical devices such as waveguides with feature sizes too small to be fabricated by optical lithography. Although the substrate may be different, the overall dimensions of such structures are comparable with that of a DOE. As such, the fabrication of these SOI structures will also face similar challenges as the DOE in pattern alignment and stitching. The solutions developed in this process can therefore be used for other similar processes with little or no modification. The development of a process addressing the details of fabricating nanooptical elements by electron beam lithography is a necessary and worthwhile effort which shall in time lead to many novel and interesting applications in integrated optics.

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