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High-Speed/Low-Cost Delta-Sigma Modulation Techniques for Analog-to-Digital Conversion

by

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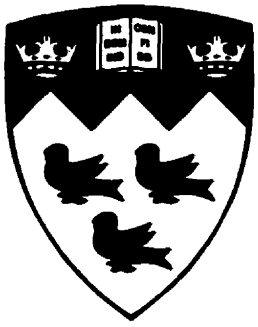

April 1998

A Thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Master of Engineering.

Abstract

As digital electronics becomes increasingly popular, the need for efficient data conversion to provide the link to our analog world grows all the more important. To sustain the current rate of technological advancement, the requirements on the data conversion systems are becoming more stringent. Wireless communication systems demand high speed, high performance analog-to-digital conversion front-ends. Furthermore, consumers demand quality electronics at low cost, which precludes the use of expensive analog processes.

This thesis investigates the potential of $\Delta\Sigma$ modulation techniques in addressing both of these issues through the design, implementation and experimentation of several prototype integrated circuits. Delta-Sigma modulation has recently become widely recognized for its ability to perform high performance data conversion without the use of high precision components. To extend these benefits to wireless applications, a novel eighth-order bandpass $\Delta\Sigma$ modulator for A/D conversion will be presented. The modulator design is developed beginning at the signal processing level and realized in a 0.8μ BiCMOS process using the switched-capacitor (SC) technique. To address the cost issue, the design of a data conversion system based on the $\Delta\Sigma$ modulation technique using an economical purely digital CMOS implementation is investigated. The distortion performance of experimental prototypes implemented using switched-capacitor (with capacitors realized using MOSFETs) and switched-current techniques is assessed.

This work therefore contributes to the ongoing drive to improve the performance and applicability of the $\Delta\Sigma$ modulation technique in meeting modern-day data conversion needs.

Résumé

Avec la popularité grandissante des circuits électroniques numériques, le besoin de convertir avec efficacité les données pour assurer le lien avec le monde analogique devient de plus en plus important. Afin de maintenir le rythme actuel de développement technologique, les exigences relatives aux systèmes de conversion de données deviennent plus sévères. Les systèmes de communication sans fil requièrent des circuits de conversions analogiques-numériques à grande vitesse et haute performance. De plus, les consommateurs exigent des composants électroniques de haute qualité à prix raisonnable, ce qui rend impossible l'utilisation de procédés analogiques coûteux.

Dans cette thèse, le potentiel de la modulation delta-sigma à solutionner les deux problèmes ci-haut mentionnés est étudié à l'aide de la conception, la fabrication et l'expérimentation de plusieurs prototypes de circuits intégrés. La modulation $\Delta\Sigma$ est récemment devenue largement reconnue grâce à sa capacité de convertir les données avec une grande qualité sans nécessiter de composants de haute précision. Pour étendre ces bénéfices aux applications de communication sans fil, un nouveau modulateur de huitième ordre à bande passante sera présenté. La conception du modulateur est expliquée à partir du niveau de traitement du signal jusqu'à la réalisation utilisant la technique des condensateurs-commutés à l'aide du procédé BiCMOS de 0,8 microns. Afin d'aborder la question du coût, la conception d'un système de conversion basée sur la technique de modulation $\Delta\Sigma$ qui utilise un procédé numérique est étudiée. Une analyse de la distorsion sur des prototypes expérimentaux employant des condensateurs-commutés (réalisés à l'aide de transistors à effet de champ MOSFETs) et des techniques de courants-commutés est aussi effectuée.

Cet ouvrage contribue donc à l'élan d'amélioration de la performance et de l'utilité des techniques de modulation $\Delta\Sigma$ dans le contexte des besoins présents de conversion de données.

Acknowledgements

The work described herein is a result of the generous contribution of knowledge, expertise, and support of several people.

To begin, I would like to express my gratitude to my supervisor, Professor Gordon Roberts. His endless enthusiasm and unparalleled teaching ability are largely responsible for my microelectronics career choice and success of this work. I greatly appreciate his technical insight and unwavering support throughout my degree.

I am grateful for the contributions of, and many useful technical discussions with Loai Louis, Choon Leong, Benoit Dufort, Mourad El-Gamal, Xavier Haurie, Vincent Leong, Benoit Veillette, Arman Hematy and for the good times spent together. I am very fortunate to have had such excellent company during my years at McGill. Nicolas Gagnon and John Walker were of great assistance in the development of the PCB boards. I am thankful for the around-the-clock efforts of the system administrators in keeping the computers running. I am also grateful for the work of the many MACS laboratory alumni who established the infrastructure that made this work possible.

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Chapter 1 : Introduction

This thesis is concerned with the use of delta-sigma modulation as a means of meeting the modern day analog-to-digital conversion (ADC) needs of high-performance and low-cost. This chapter will discuss the driving force behind these two industry demands, and outline how the work of this thesis is organized to address them.

1.1 Motivation

As digital processors are becoming ever more powerful and inexpensive, digital processing of information has replaced much of the traditional analog techniques used in the past. In addition due to the improved signal quality, ease of routing and added versatility, most information transmission in modern-day communication systems is also performed using digital means. In consequence, this has lead to the general processing scheme shown in Figure 1.1 below:

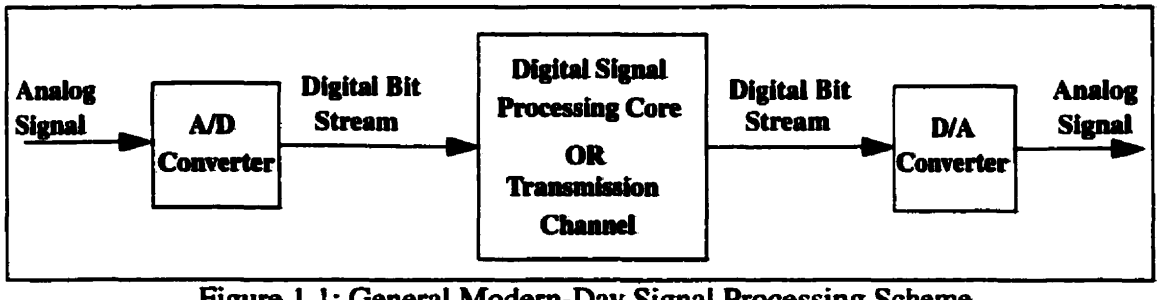


Figure 1.1: General Modern-Day Signal Processing Scheme

As real-world signals, such as speech or radio waves, are analog in nature, it is necessary to include A/D and D/A converters at the front and back ends of the system, respectively. These data converters contain both analog and digital components, and form the interface between analog real-world signals and the hardware that processes them.

The above scheme has become increasingly popular, however, it does have two major repercussions associated with it. These two repercussions are the motivating factor behind this work and will be discussed next.

1.1.1 The need for high-performance, high-speed data conversion

As we drive towards higher quality and greater operating speeds, increased demands are placed upon the processing hardware. Continually improving digital processors are paving the way for these increased demands. However, if the data converters shown in Figure 1.1 can not follow suit, they will become the bottle neck in the system. That is, their lower performance will dominate the system performance.

The need for high speed data conversion is further intensified by a growing trend in wireless communications. Systems that rely solely on analog modulation and demodulation schemes are being replaced by digital techniques or by hybrid solutions that allow the use of both analog and digital approaches. Digital systems allow the transfer of data as well as voice, are more easily routed and provide greater security for the user through channel encryption. A conventional (mostly) digital cellular receiver is depicted in Figure 1.2:

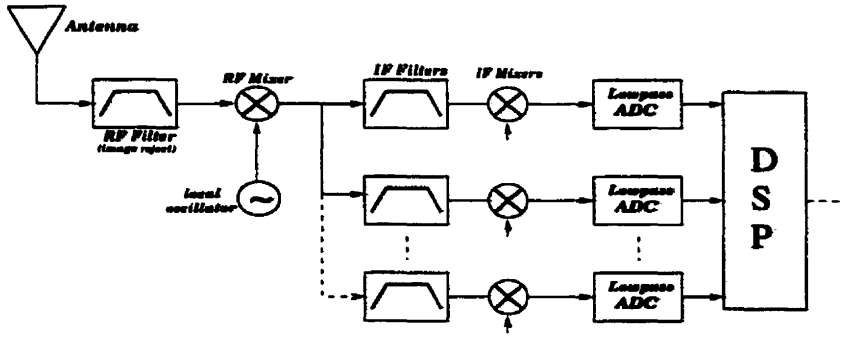


Figure 1.2: Simplified Conventional Wireless Receiver (Base Station)

Although not shown in the simplified base station architecture of Figure 1.2, the RF down-conversion is typically handled in multiple stages to ease the requirement on the image re-

jection filter. In the receiver of Figure 1.2, each channel uses an independent dedicated IF strip before the signal is brought down to baseband. Only then do the ADCs convert the signals to the digital domain, where processing can begin. This approach is costly due to the extensive use of analog components. In addition, each channel is fixed, and not adaptable to any changes made in transmission protocols. For these reasons, it is desirable to move the analog-to-digital converters as close to the front-end of the system as possible, ideally converting the entire RF spectrum with one single, wide-band ADC. This would alleviate the need for multiple expensive analog components, and make the system more versatile, as the digital hardware can easily be re-programmed and adapted to any new protocol. This latter approach, however, places extreme requirements on the data converter, in terms of both speed and resolution.

Further incentive for investigating high speed ADC can be understood by considering more closely the demodulation of a single channel, as in the handset receiver of Figure 1.3.

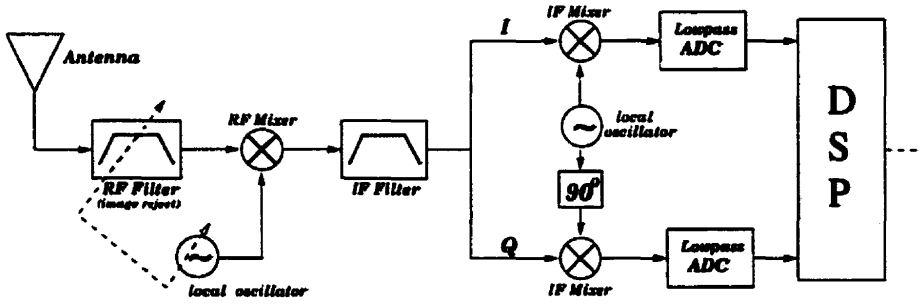


Figure 1.3: Simplified Handset Receiver Architecture

Once down-converted to baseband, the signal is split into in-phase (I) and quadrature (Q) components which are processed by separate channels, leaving the receiver susceptible to mismatch between the two. Furthermore, the lowpass ADC must be designed carefully to avoid DC offset and 1/f noise problems. Alternatively, these shortcomings could be avoided if a bandpass ADC were used to directly convert the IF signal and the I/Q split performed digitally. However, once again this places stringent demands on the data converter.

As will become evident shortly, $\Delta\Sigma$ modulation offers an attractive approach to realize the high-performance converters required. A major advantage of the $\Delta\Sigma$ technique is that it

does not require high precision analog circuitry, which is all the more important if one wishes to use a standard digital CMOS process.

1.1.2 The need for using a standard digital CMOS process

As the vast majority of IC's are currently realized using digital processing of information, fabrication processes have been tailored to optimize for digital circuitry. As such, pure digital CMOS, where no additional processing steps have been used, is by far the most economical technology in terms of fabrication cost.

However, analog circuitry often requires high performance features that are not found in a standard digital CMOS process. For example, the high gain and bandwidth associated with a BJT is often desirable, as is the high linearity of poly-poly capacitors. Although these features can be included through additional processing steps, as in current BiCMOS processes, this approach incurs extra costs.

In addition, in many systems, it is often desirable to include the usually small amount of analog circuitry together with the mainly digital core resulting in a mixed-signal IC. This is especially the case for data converters which often contain the only analog circuitry on the entire IC. If the analog circuits can not be designed using a purely digital CMOS process, the entire IC will have to be fabricated in a more expensive BiCMOS technology. Thus, although digital circuits can be produced quite inexpensively on their own, the relatively small amount chip area devoted to analog functions can contribute an unproportionate amount to the overall system cost.

Therefore, any circuit technique that would allow these analog circuits to be manufactured in the same inexpensive CMOS process as the digital core would be very valuable.

1.2 Thesis Overview

In Chapter 2, the concept of delta-sigma modulation for analog-to-digital conversion will be introduced. A basic second order lowpass modulator, implemented using the switched-capacitor (SC) technique has been fabricated in a 0.8μ BiCMOS process, and will be used

to demonstrate the technique through from specification to a physical IC. This illustration of the basic design process will serve to pave the way for the more elaborate work of Chapter 3, where a more complex eighth-order modulator will be investigated. It will also set the ground work for the ΔΣ modulator designs of Chapter 4, which are based on variations of the same second-order modulator.

Next, in Chapter 3, the concept of bandpass delta-sigma modulation will be introduced. The chapter illustrates a step-by-step design process for a novel, eighth-order bandpass delta-sigma modulator, designed to address the need for high speed, high performance data-converters discussed in Section 1.1.1. The discussion will detail the design from the DSP-level abstaction complete through to subtle, though crucial, implementation and layout considerations. The strategy used to verify the design at the various stages will also be presented. The design has been fabricated in a 0.8μ BiCMOS process producing the first working bandpass prototype of such high-order. Experimental results will be shown to illustrate the performance of the modulator.

Chapter 4 will be used to address the economic driving force discussed in Section 1.1.2 by studying the use of ΔΣ modulation in an all-CMOS data conversion system. Specifically, we will investigate sampled-data implementations of the ΔΣ modulator and filter components using two different circuit techniques that do not require the linear capacitors which are unavailable. One approach is to employ the switched-capacitor technique and use MOSFETs to implement the capacitors. The second approach is to use the technique of switched-currents which inherently does not require explicit capacitors all-together. In each case, an experimental prototype of a second order lowpass ΔΣ modulator as well as of a biquadratic filter has been fabricated to study the techniques. Experimental results of the four ICs will also be included in the chapter.

The thesis will conclude in chapter 5 with a summary of the work presented.

Chapter 2 : Basic Lowpass Delta-Sigma Modulation

In this chapter, the concept and background theory of lowpass ΔΣ modulation will first be introduced. Next, a second-order voiceband ΔΣ modulator will be used to illustrate the basic design process from initial specification through to a physical IC that has been fabricated in a 0.8μ BiCMOS process.

2.1 Background Theory

This section will first discuss how the analog-to-digital conversion using the ΔΣ method compares to other classes of data-conversion techniques. The basic principles of ΔΣ modulation will then be discussed in terms of both time domain and frequency domain behavior.

2.1.1 Delta-Sigma Modulation for Data-Conversion

The main A/D conversion techniques used today are summarized in Figure 2.1. The main distinction between converter classes is in the rate at which they sample the analog signal. Nyquist rate converters sample a bandlimited continuous-time signal at the Nyquist rate, f_N, which is twice the bandwidth of the analog signal. The sampling action must be preceeded by an analog lowpass filter to avoid any aliasing.

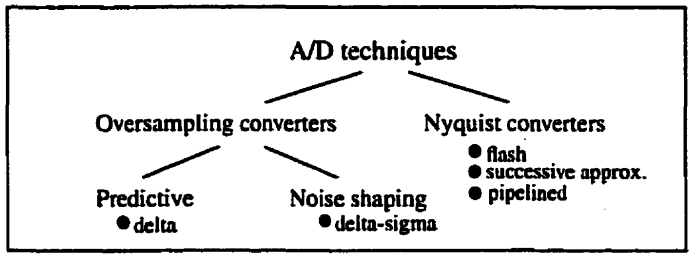


Figure 2.1: Main A/D conversion Techniques

Nyquist rate converters have two main disadvantages [1]. First, the anti-aliasing filter must have a very sharp roll-off which translates into a high-order, quite complex, analog filter. Second, the matching of components becomes a problem when the precision of the converter starts to increase. This is because in VLSI implementations, an N-bit quantizer achieves data-conversion by comparing the analog input signal to a set of reference voltages, and outputting the appropriate digital word. The precision of the converter depends on the spacing between these reference voltages which, from the implementation viewpoint, depends on the matching properties of the resistors or capacitors used. For a quantizer with 16-bit resolution or higher, the spacing of these reference levels must be in the microvolt range. Unfortunately, the matching tolerance of these elements (resistors or capacitors) is much lower than the above requirements. Therefore, unless expensive post-fabrication microsurgery is used, nyquist-rate converters are not well-suited for high-precision data conversion needs.

Oversampled converters sample the analog signal at a much higher rate, f_S. The amount of oversampling is quantified by the *oversampling ratio*, defined as

$$OSR = f_S / f_N \tag{2.1}$$

This class of converters avoids the aforementioned problems by exchanging the required resolution in amplitude for that in time. Furthermore, by oversampling, the specifications on the anti-aliasing filter are relaxed and a much coarser quantizer can be used. This is because in an oversampled system, the quantization noise will be spread over a much wider range, $[0,f_S]$ and subsequent filtering can eliminate the noise that is outside the signal band $[0,f_N/2]$. This results in an increased signal-to-noise-ratio (SNR). Specifically, the SNR will increase by 3 dB, every time the OSR is doubled [2].

The oversampling technique can be plainly applied to any waveform coding technique. However, coders that use oversampling usually use quantizers with fewer levels and employ an additional approach to reduce the quantization noise apart from pure oversampling. As will be seen in the next section, this is done in delta-sigma modulation by embedding the quantizer within a feedback loop. This allows the quantizer to be even more coarse (as low as one-bit) making these converters quite insensitive to circuit imperfections and component mismatch [3]. Thus, delta-sigma modulation can be viewed as a means of pushing the data-converter beyond component tolerances.

A simplified block diagram of an analog-to-digital converter that uses the delta-sigma modulation technique is shown in Figure 2.2. The analog input is first lowpass filtered to prevent aliasing from occurring when the signal is sampled at the clock rate, f_S. The delta-sigma modulator operates on the discrete time signal, x(n), producing a single-bit digital representation at the same rate, f_S. Next, the bit stream is decimated, producing a multi-bit digital word stream at the lower nyquist rate, f_N, which is now suitable for data storage or to be operated on by a DSP engine.

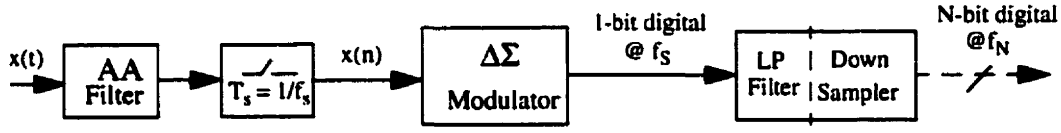


Figure 2.2: Elements of a Delta-Sigma Analog-to-Digital Conversion System

Next, the ΔΣ modulator, which forms the core of the data-converter, will be examined in more detail.

2.1.2 Basic ΔΣ Modulator Operation

In this section we investigate how a ΔΣ modulator single-bit output can effectively encode the discrete-time, multi-valued input signal. To begin, consider the DSP-level implementation of a first-order ΔΣ modulator shown in Figure 2.3.

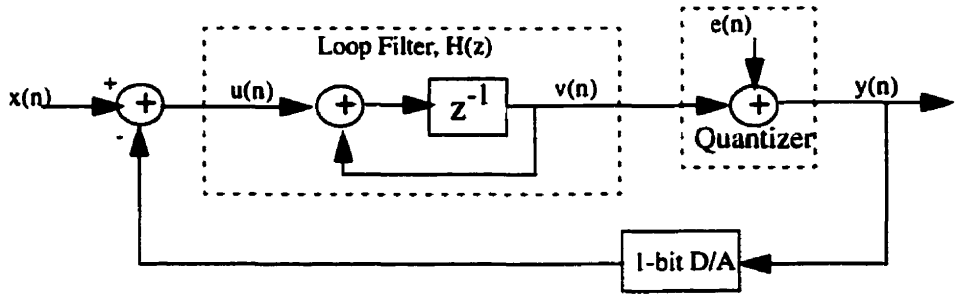


Figure 2.3: First-Order ΔΣ modulator with linear model of the quantizer

It consists of an analog delay element, z^{-1}, and summer stage in an internal feedback loop forming a simple integrator, H(z). This loop filter is followed by a 1-bit quantizer which will output +/-1 depending on whether the input, v(n), is above or below a certain threshold, usually defined midway between the supply rails. This quantizer has been modeled as a simple analog summer, with e(n) representing the error made when approximating the loop filter output, v(n), by the quantizer output, y(n). The quantity e(n) is referred to as the *quantization error*, and leads directly to the *quantization noise*, to be discussed shortly.

The quantizer output which also serves as the modulator output is feed back to the input through a 1-bit D/A converter. The feedback level is then subtracted from the modulator input signal to produce u(n), the loop filter input. The 1-bit D/A is necessary so that the subtraction can occur in the same (analog) realm, but does not otherwise affect the basic signal processing.

When employing a simple one-bit quantizer, the output y(n) can be either +/- 1. Consider the simple case for a 0 V DC input, x(n). If the output level is +1, the error u(n) will be negative, and negative values will accumulate in the integrator, producing v(n). Eventually, after enough clock cycles, enough negative values will accumulate, causing v(n) to go neg-

ative and the quantizer to produce y(n)=-1. The overall input-output error has been reduced, when averaged over time, because negative errors will cancel with previous positive ones

Consider next the case for a positive DC input signal, x(n). When y(n)=1, the magnitude of the error, u(n) would be less than when y(n)=-1. Therefore it would take more clock cycles for the integrator to accumulate enough error to cause y(n) to switch from 1 to -1 than from -1 to 1. Therefore, the output y(n) will spend most of it's time at y(n)=1. Similarly, for negative input signals, y(n) will spend most of it's time at y(n)=-1. In fact, when averaged over time, the output bitstream will approximate the DC input voltage, x(n).

Now, consider the case where x(n) is a sinusiodal input. Following the above reasoning, there should be more high output levels when the input is positive, and more low output levels when the signal is negative. This is confirmed by Figure 2.4 which shows the input-output time domain waveforms of a ΔΣ modulation system.

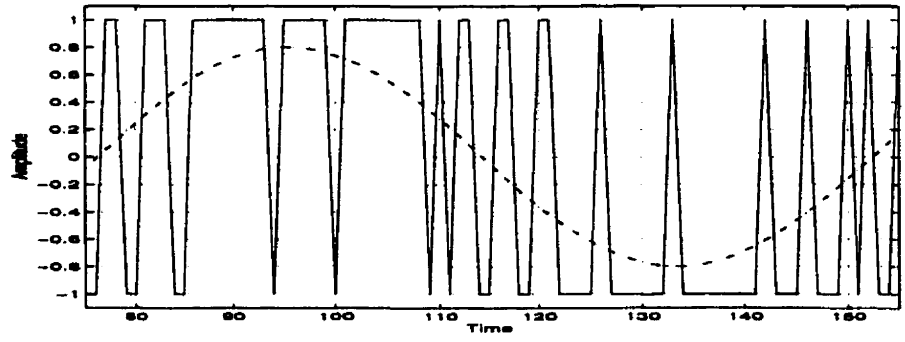


Figure 2.4: Input (sinusoid) and output (PDM) time-domain waveforms of a ΔΣM

With the input signal superimposed on the output signal, we see that the output signal toggles between the zero and one state in such a way that the input signal is encoded into the density of the one's in the output signal. In other words, when the input signal is very near the full scale value, the output is in the high state for many clock cycles. Conversely, when the input is near the other extreme, the output is in the zero state for many clock cycles. In both cases, the local average of the modulator output tracks the analog input. When the input is near the mid-range, the value of the modulator output varies rapidly between the low and high states in almost equal proportion.

This type of encoding is referred to as *Pulse Density Modulation* (PDM) [5]. By carefully averaging the output signal over many clock cycles, the input signal can be recovered as a multibit digital signal. This is the task performed by the decimator that was shown in Figure 2.2, resulting in multi-bit digital representation of the analog input.

2.1.3 Time Domain Analysis

A greater understanding of the modulator operation can be achieved by examining the time domain input-output relation of the structure. This can be easily obtain if the modulator of Figure 2.3 is modified slightly, without changing the functionality what so ever. The resulting signal flow graph is shown in Figure 2.5 below.

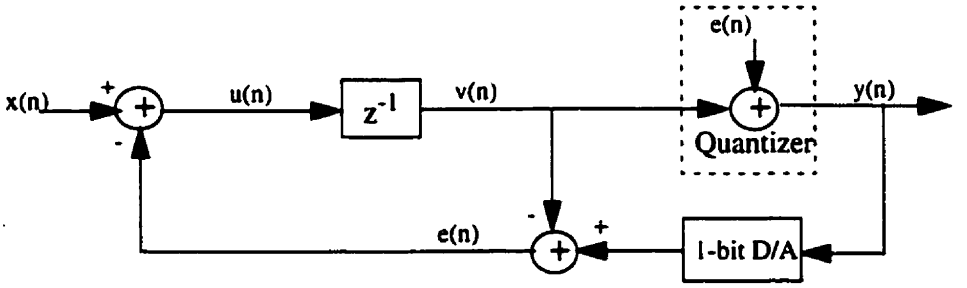


Figure 2.5: First-order ΔΣ modulator with modified signal flow graph

Referring to this modified representation of the modulator, it is easy to see that the quantization error, e(n), is being fed back and subtracted from the input signal. The time domain equation describing the circuit in Figure 2.5 can be easily found to be given by

$$y(n+1) = x(n) + [e(n+1) - e(n)] \tag{2.2}$$

As can be seen from Eq. (2.2), the output is the sum of the input, delayed by one clock cycle, plus the difference between the quantization error made on the current and previous cycles. Because the ΔΣ modulator loop is oversampled, adjacent samples of the internal signals will be highly correlated. Therefore, we can expect near perfect cancellation of the quantization errors, improving more so if the oversampling ratio is increased.

If instead of merely feeding back the quantization made on the last clock cycle, but rather a quantity dependent on multiple past errors (i.e. e(n), e(n-1), e(n-2)...) one could obtain a better estimate the sample error that would be made on the next phase. This approach al-

lows superior cancellation of the quantization errors and is the reasoning behind building higher-order modulators. In general, an Nth-order modulator will use N previous values of the quantization error on which to base estimate of the next.

2.1.4 Frequency Domain Perspective: Noise Shaping

Further insight can be obtained if the input-output relation of Eq. (2.2) is moved into the frequency domain by taking the z-transform as follows,

$$Y(z) = z^{-1}X(z) + [1 - z^{-1}]E(z) \tag{2.3}$$

The z-domain equation is usually analyzed in terms of the separate transfer characteristics experienced by the input signal and quantization noise. The *signal transfer function* (STF) of the above structure is given by

$$STF = \frac{Y(z)}{X(z)} = z^{-1} \tag{2.4}$$

indicating that the signal is only delayed in time. However, the quantization *noise transfer function* (NTF) is given by

$$NTF = \frac{Y(z)}{E(z)} = 1 - z^{-1} \tag{2.5}$$

which has a transmission zero at DC. Figure 2.6 illustrates the effect of this zero on the modulator output noise power spectral density (PSD), presented theoretically in [4][8]. It can be clearly seen that the lower frequency components of the noise will be suppressed while those at higher frequencies emphasized. Thus, the noise is "shaped" out of the signal band (at low frequencies) and into the high end of the spectrum.

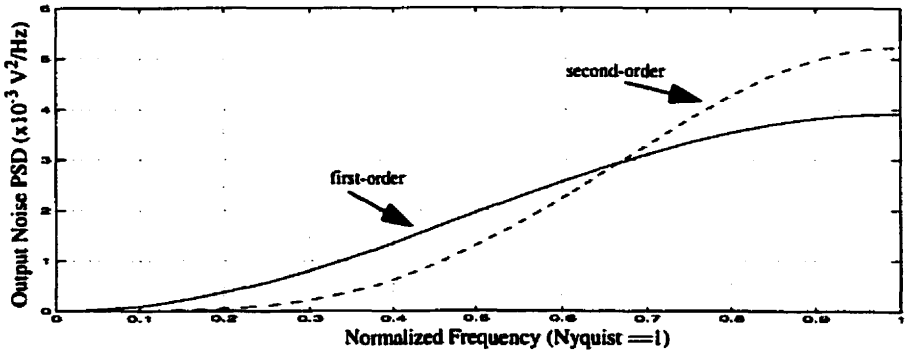


Figure 2.6: Output Noise PSDs corresponding to 1st and 2nd Order LP Modulators

The dashed line in Figure 2.6 illustrates the output noise PSD when a second order loop filter, H(z), is employed in Figure 2.3. Compared to the first order case, more of the quantization noise is pushed out of the signal band and into higher frequencies. This confirms the intuitive reasoning developed in the previous section. That is, in general, the higher the order of the converter, the more the noise will be shaped in the desired manner [6].

Regardless of the modulator order, the high frequency noise which occurs out of band must be removed in order to maintain signal quality. This is achieved by the subsequent lowpass filtering operation that occurs within the decimator.

As mentioned previously, the resolution of the modulator can be increased by increasing the oversampling ratio, defined in Eq. (2.1). The amount by which the SNR improves depends on the order of the modulator [5]. A general rule of thumb is that for every doubling of the OSR, the SNR will increase by 3 dB, in addition to 6 dB for every integrator in the loop filter [8]. Therefore, doubling the OSR would lead to a 9 dB increase in the SNR for a first order modulator, and 15 dB increase in the SNR for a second order converter.

2.1.5 A General Modulator Structure

To conclude our overview of ΔΣ modulation, consider the general (N^{th} order) modulator of Figure 2.7 consisting of a loop filter, quantizer and DAC in a negative feedback loop.

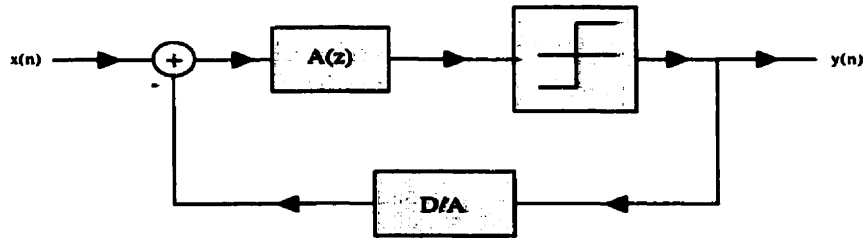


Figure 2.7: General ΔΣ Modulator Structure for A/D Conversion

In general, the quantizer need not be restricted to be a simple thresholder, as in the one-bit case. For the same OSR, multibit modulators have lower quantization noise (approximately 6 dB less per extra bit used [23]), are more easily stabilized, and ease the requirements on the decimation filter. Although this approach adds complexity to the quantizer, the major drawback comes from the D/A circuit, which must also be multi-bit to follow suit. Non-

linearities introduced from component mismatch in the multi-bit D/A circuit will lead directly to distortion at the modulator output as these errors, unlike those of the quantizer, will not be shaped by the modulator noise transfer function. Recently, however, research has emerged demonstrating that by using dynamic element matching techniques [74][75], the D/A errors can also be shaped, albeit at the expense of increased hardware. Therefore, although this work focuses on single-bit modulation, it should be noted that the multi-bit approach does show potential as well.

Referring again to Figure 2.7 and modeling the quantizer as an additive noise source allows the signal transfer function within this structure to be written as by

$$STF = A(z)/[1 + A(z)] \tag{2.6}$$

and the noise transfer function as

$$NTF = 1/[1 + A(z)] \tag{2.7}$$

To design a general modulator using the above structure, one must first determine how many bits of resolution are necessary for the specific application. This can be easily translated into an SNR requirement using Eq. (2.8)[23] below

$$SNR = (6.02 \cdot N + 1.76)\ dB \tag{2.8}$$

The above SNR requirement will place a constraint on the maximum allowable noise in the signal band. In brief, a mathematical NTF can then be derived that achieves the noise-shaping necessary to obtain the required noise suppression and thus SNR. As will be seen in the novel design presented in Chapter 3, this NTF can then be used in establishing the loop filter, A(z). It should also be mentioned that, especially when a 1-bit quantizer is used, $\Delta\Sigma$ modulators are highly nonlinear structures. Modeling the quantizer as an additive noise source, as usually done in practice, does not capture all its effects on the circuit. In particular, the stability of $\Delta\Sigma$ modulators (especially those of high-order) is not well understood and is generally addressed using rules of thumb [14].

Finally, as will be seen in the work that follows, although conceptually sound, $\Delta\Sigma$ modulators are not usually designed using the simple single-loop topology of Figure 2.7. Instead, multi-loop structures, which are better suited for circuit implementation will be used.

2.2 A Second-Order LowPass ΔΣ Modulator

In this section, a second-order lowpass modulator design will be used as an example to demonstrate the basic ΔΣ technique through from specification to a physical IC. It will set the stage for the more elaborate eighth-order design that will be investigated in Chapter 3. Furthermore, the work presented herein will also form the backbone of the ΔΣ designs in Chapter 4, which use the same signal processing-level topology.

2.2.1 Design Specifications

The modulator under investigation is intended for use in a voice-band analog-to-digital converter. The objective is to obtain at least 13-14 bits of resolution (or approximately 80 dB SNR) over the 0-4 kHz band.

The maximum expected SNR for a ΔΣ modulator can either be derived theoretically by modeling the quantization errors as an additive white noise source, as detailed in [5][8], or through empirical analysis, as described in [6]. Referring to the latter work, it was found that by using a 2nd-order modulator with coincident NTF zeros[1] and OSR of 128, up to 85 dB SNR can be expected. An OSR of 128 with inputs up to 4 kHz requires that the system be clocked at approximately 1 MHz, which is reasonable for the given technology. Therefore, a second-order modulator is well-suited to meet the intended specifications.

2.2.2 SFG-Level Design

Figure 2.8 shows the most popular topology for a second-order ΔΣ modulator, which is well documented in the literature [71].

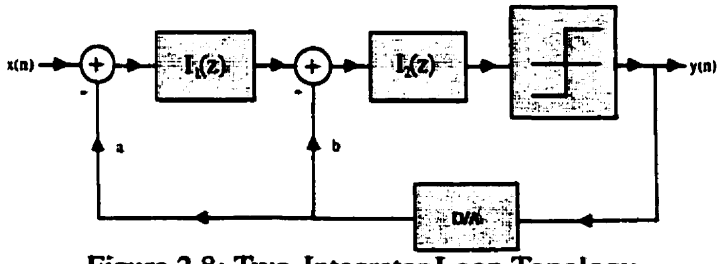


Figure 2.8: Two-Integrator Loop Topology

1. Alternatively, the NTF zeros could be spaced throughout the passband, though this will only improve the SNR by approximately 5 dB in the relatively low-order design of this chapter

It consists of two integrator loops with feedback coefficients, a and b, selected in such a way so as to ensure stability. The integrators, I_1 and I_2, may each either be delayed or non-delayed. Each combination has its own advantages and disadvantages. These will be discussed in the design of Chapter 3, where the implications are more severe. For these relatively low speeds and performance requirements, however, the choice is not crucial and we follow the approach used in [3]. That is, both integrators will be of the delayed type.

The resulting signal and noise transfer functions are given in Eqs. (2.9) and (2.10) below

$$NTF = \frac{(z-1)^2}{z^2 + (b-2)z + (1+a-b)} \tag{2.9}$$

$$STF = \frac{1}{z^2 + (b-2)z + (1+a-b)} \tag{2.10}$$

The corresponding SFG block level diagram is shown in Figure 2.9, with a=1 and b=2.

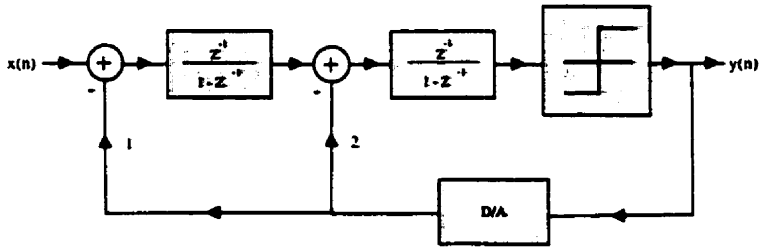
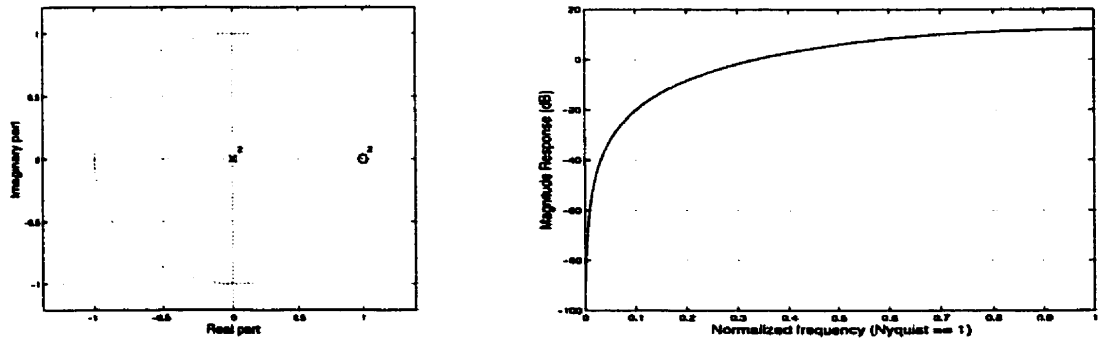


Figure 2.9: SFG level representation of the delayed, delayed combination

With his choice of feedback coefficients, the signal will propagate unaffected through the modulator in two clock cycles, while the quantization noise will be shaped according to the noise transfer function shown in Figure 2.10



(a) (b)

Figure 2.10: (a)Pole-Zero and (b) Frequency Response Plots of NTF for a=1, b=2

Although this does produce the desired noise shaping, the structure of Figure 2.9 is not best-suited for implementation. One reason for this is that the signal range required at the outputs of the two integrators is several times the maximum input range. This can represent a problem in VLSI circuit technologies where the dynamic range is limited. This effect can be avoided by slightly modifying the DSP representation to that shown in Figure 2.11 [3]. As will become apparent shortly, this representation also lends itself more easily to implementation than does the original of Figure 2.9.

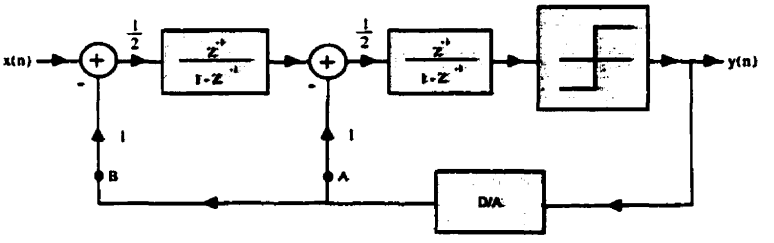
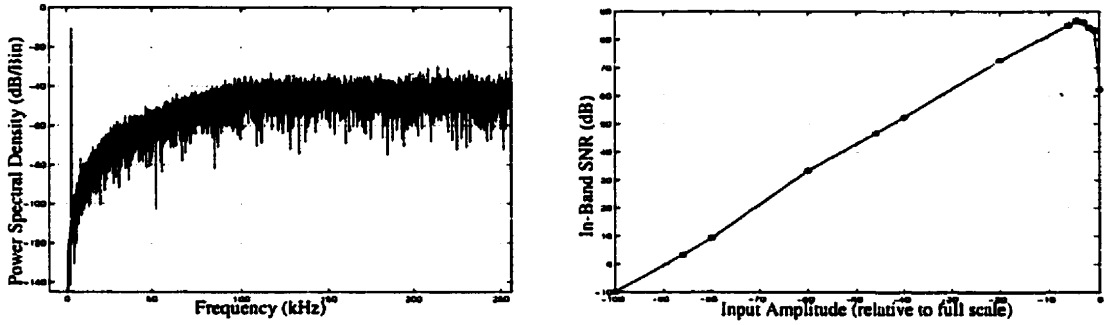


Figure 2.11: Alternate representation of the delayed, delayed combination

Referring to Figure 2.11, note that the feedback from point A to the output passes through one scaling factor of a half. However, the feedback from point B and the input both pass through two scaling factors of a half. Thus the feedback in the branch containing the point A is effectively twice that of the other branch, as in the original representation of Figure 2.9.

Before investigating IC realizations, design of Figure 2.11 was verified using Simulink, a SFG-level simulator. The circuit was stimulated with a sinusoid, whose frequency was carefully choose to ensure coherent sampling. The output PDM bitstream was sampled at a rate of one bit per clock cycle (1.024 MHz), for 32768 (2^{15}) cycles. Next, matlab was used to preform the FFT analysis, producing the spectra shown in Figure 2.13(a) with an equivalent resolution of 31 Hz/bin.



(a) Noise-Shaping Behaviour (b) SNR as a function of Input Level

Figure 2.13: Results of SFG-Level Simulation using Simulink

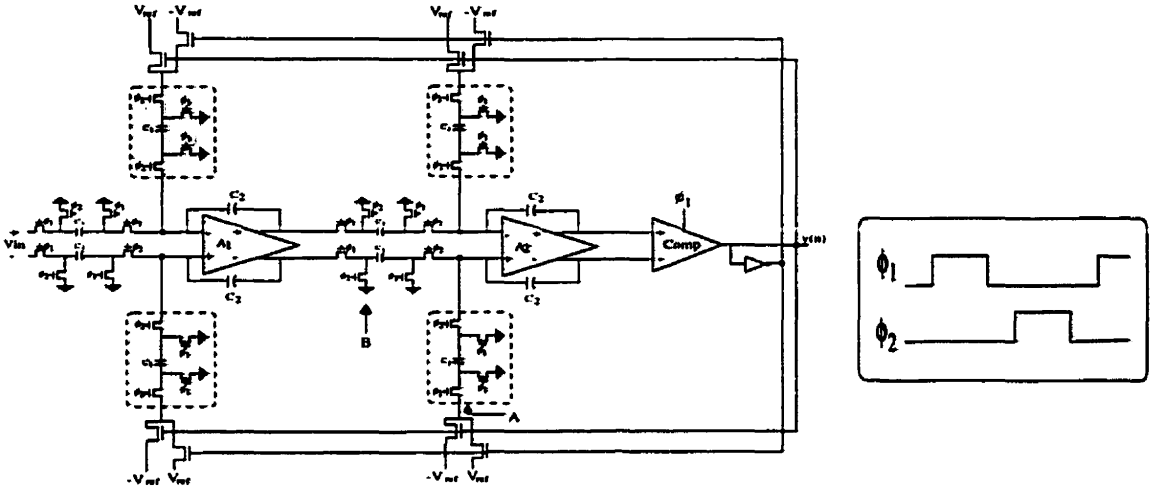
The maximum SNR in the 0-4 kHz bandwidth (corresponding to an OSR of 128) was found to be 86 dB.

In addition, this relatively fast simulator was used to investigate the behavior of the modulator for various input levels. The results are summarized in Figure 2.13(b). Initially, as the input level increases, the SNR follows suit, due to the increase in signal power. However, as the input approaches the feedback reference level of 0 dB, the SNR drops off rapidly. This behavior is typical to $\Delta\Sigma$ modulators and is due to stability problems which occur when large input voltages are allowed to accumulate in the integrators of the loop filter. The plot of Figure 2.13(b) illustrates that the modulator is useful in processing signals within a 90 dB dynamic range, that is the range in which the modulator attains a positive SNR.

2.2.3 Switched-Capacitor Realization

The switched-capacitor (SC) technique was chosen to implement the design due to its robustness, high degree of accuracy, and IC reusability. Because mixed-signal ICs suffer from relatively high noise, a fully differential SC implementation was used as it is less susceptible to electronic noise when compared with the single-ended implementation.

To map the SFG-level structure onto a SC design, each integrator in Figure 2.11 is directly realized by a conventional multi-input, stray-insensitive SC integrator of the delayed (non-inverting) type as shown in Figure 2.14(a).



(a) Switched-Capacitor Circuit (b) Two-Phase Clock

Figure 2.14: Lowpass Modulator Implementation

The switches are controlled by a two-phase non-overlapping clock whose phases are shown adjacently in Figure 2.14(b). The short time where both phases are low is necessary to avoid charge sharing in SC circuits. Feedback is implemented by the shaded sections, where the ratios of $(C_1/C_2)=1/2$ and $(C_3/C_2)=1/2$ specify the a and b coefficients respectively. The one-bit D/A block of Figure 2.11 is easily realized by switching in a positive or negative reference voltage, depending on the quantizer output level.

At this point, one advantage of the decision to use two delayed-type integrators in the SFG-level design becomes apparent. In this configuration, the amplifier A_1 is being driven at the beginning of ϕ_2, and has its output sampled at the end of ϕ_1. Therefore, on any given phase, the amplifier A_1 has only to settle an input transient or drive its capacitive load, but never both simultaneously. Had this integrator been non-delayed, the amplifier would have been driven at the beginning of ϕ_1, and the output would have been sampled at the end of that same ϕ_1, placing greater demand on the amplifier speed.

Another benefit of opting for the SFG-level design of Figure 2.11 is that, because $C_1=C_3$ in the corresponding implementation of Figure 2.14, the SC circuit can be optimized to

make more efficient use of the available silicon area. This can be accomplished by switch and capacitor sharing, as follows. Referring to Figure 2.14 and following the path from the label 'A' to the input of the second amplifier, one sees a switch controlled by ϕ_2, a capacitor of value C_1, and another switch controlled by ϕ_2, with switches controlled by ϕ_1 on either side of C_1. This is also true when following the path from the label 'B' to the input of this amplifier. Thus the whole feedback structure in the shaded area can be eliminated and node A can be connected to node B. This is also true for the other three shaded feedback structures. In addition, the D/A switches feeding analog V_{ref} and $-V_{ref}$ can also be shared since they perform the same function. Combining all of the above changes results in the circuit shown in Figure 2.15.

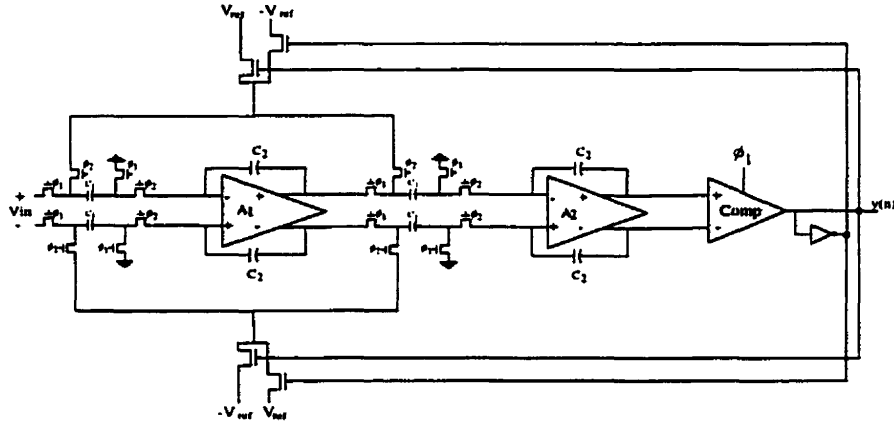


Figure 2.15: Area-efficient SC Modulator Implementation

After verifying the above topology using Switcap[68], a discrete-time simulator, the next task was to implement the SC design at the transistor-level.

2.2.4 Circuit Implementation

This section provides a brief discussion of how each of the components used in the schematic of Figure 2.15 is implemented using a BiCMOS technology.

(i) Amplifier and Comparator Circuits

The amplifier used in realizing the SC implementation was obtained from designers at Carleton University, where it was originally used in a similar bandpass application [7]. The

transconductance amplifier schematic is shown in Figure 2.16 where it can be seen that the design uses a folded-cascode topology. The pmos transistors of the input differential-pair provide a high input impedance and low 1/f noise, while the npn cascode transistors set the non-dominant pole near their unity gain frequency. The amplifier uses continuous-time CMFB circuitry to set the output DC level at analog ground. When compensated with 1pF load capacitors, the amplifier achieves a DC gain of 57 dB, a unity-gain frequency of 500 MHz, and a slew-rate of 1000 V/μs.

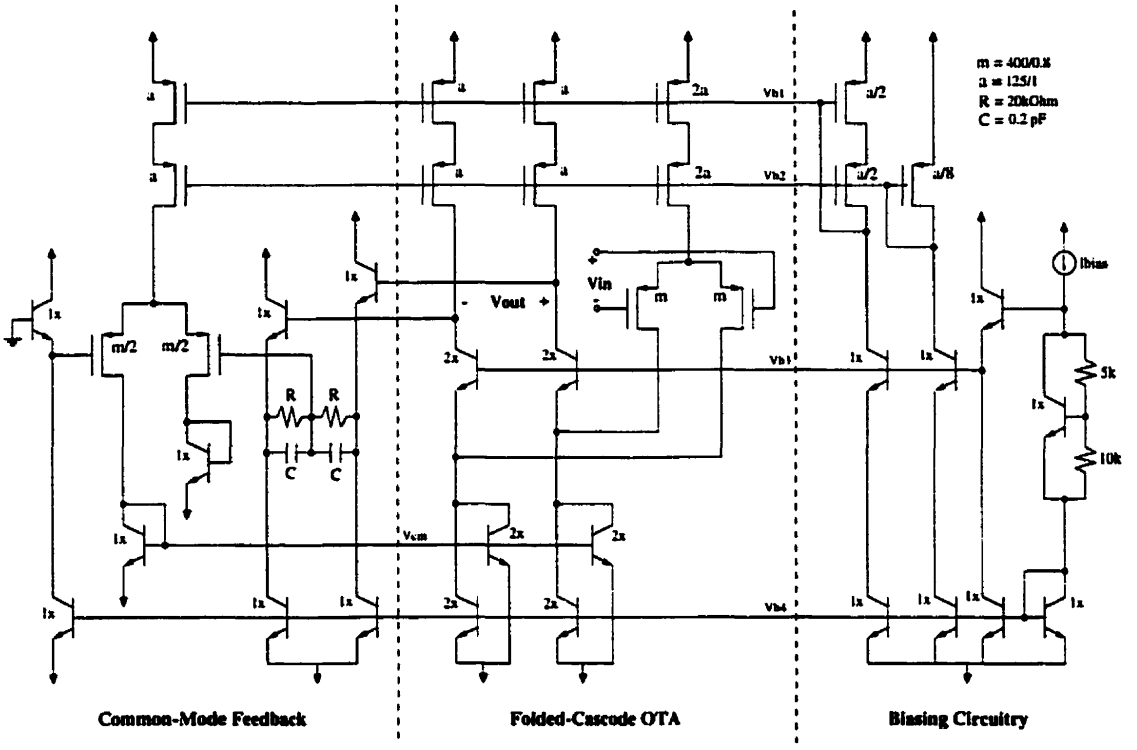


Figure 2.16: Fully-Differential Folded-Cascode OTA with CMFB and Bias Circuity

The comparator shown in Figure 2.15 can be realized simply by using the opamp in an open-loop configuration, followed by inverters to boost the gain. In addition, a D-type flip-flop can be used to provide the latching mechanism at the quantized output.

The performance of the amplifier is more than sufficient for the 1 MHz speed of this design. For the high-speed design of Chapter 3, however, capacitive loading will become a significant issue and will need to be investigated further.

(ii) Switches

The switches were realized using two-transistor transmission gates as shown in Figure 2.17. One benefit of this approach is that it increases the range of allowable signal levels in the circuit. For example, consider a singular nmos switch with a controlling voltage that swing between the +/- 2.5 volt rails. If a signal level of 2 V appears at the source of the nmos switch, the V_{GS} drop would be insufficient to conduct the signal. However, unlike a simple nmos switch, the transmission cell will always conduct when the controlling voltage (V_C) is positive. Specifically, if the node voltage at the source is such that the nmos does not conduct, it is guaranteed that the pmos will.

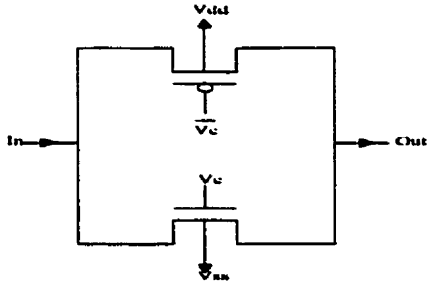


Figure 2.17: Transmission Cell

Another advantage of the transmission gate is that it can be carefully sized to control charge injection (CI). This effect can sometimes have a serious impact on SC circuit performance. However, at the speeds and precision required for this second-order modulator, CI was not a significant issue. Therefore, this topic will be further investigated in the more elaborate design of Chapter 3, where it plays an important role.

The transmission gate was simulated in HSPICE and found to have an on-resistance of 3.5k Ohms and off-resistance of 250 G Ohms. Considering that the capacitors will typically be in the picofarad range, the time constant during conduction will be on the order of nanoseconds. This effect is therefore not a concern in this design which is clocked at a frequency of 1 MHz.

(iii) Clock Phase Generator

The SC design to be implemented requires 4 clock phases. Of these, two are the non-overlapping controls, ϕ_1 and ϕ_2. In addition, their inverses are also needed to control the transmission gates. To produce these four phases from a single master clock, the well-known structure of Figure 2.18 was used. It is composed of an SR latch stretched out by an even number of inverters after the NOR gates. The length of the non-overlapping period is determined by the number of inverters in the feedback loop of the latch.

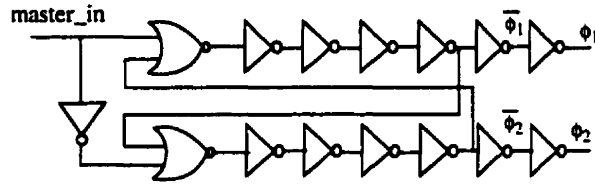


Figure 2.18: Schematic of Clock Phase Generator

(iv) Capacitors

The capacitors were formed by two layers of polysilicon available in the 0.8μ BiCMOS process used. Therefore, their linearity was not a concern in achieving the accuracy of this design. The actual sizes used were 1 pF and 2 pF for C_1 and C_2, respectively. They were chosen to be in the wide range where neither settling, charge-injection, or kT/C noise would become a serious issue. The exact choice is not critical at these speeds but will become significant for the high-speed design of Chapter 3, where it will be discussed in detail.

2.2.5 Experimental Results

Once the circuit was determined to function correctly through HSPICE simulations, the circuit layout was performed using a 0.8μ BiCMOS technology. The design was fabricated and the chip photomicrograph is shown in Figure 2.19.

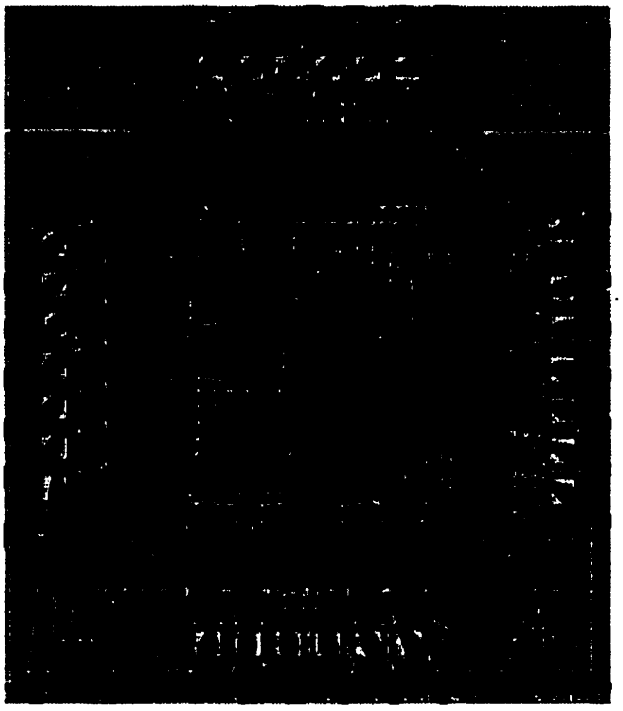
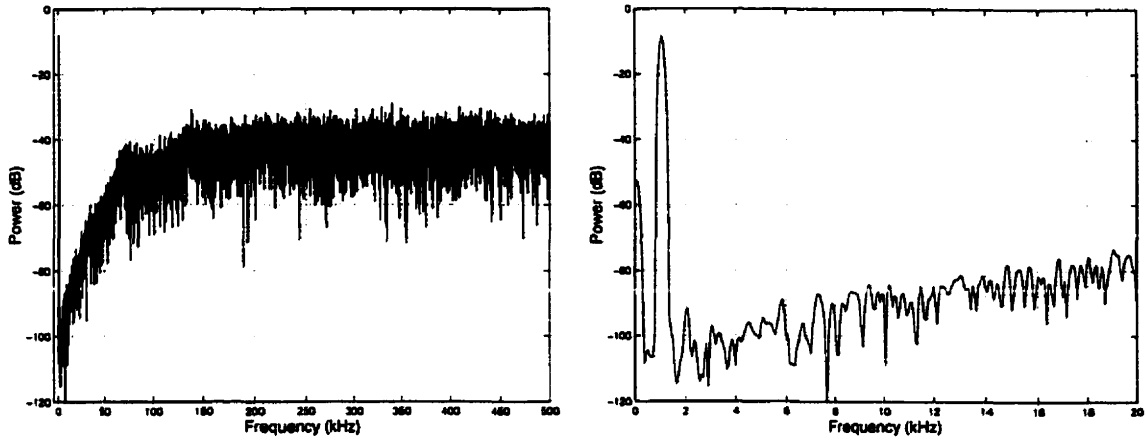


Figure 2.19: Chip Photomicrograph of Second-Order Lowpass ΔΣ Modulator

The chip occupies an active area of $0.51\mu m^2$ and consumes approximately 75 mW of power when clocked at a frequency of 1 MHz. Figure 2.20 illustrates the experimental results obtained from the prototype IC. A sinusoid in the voice-band was used as stimulus to the circuit and the output bit stream was captured digitally. Matlab was then used to perform a FFT analysis. The Nyquist band plot of Figure 2.20(a) is a result of 16384 (2^{14}) point FFT analysis (corresponding to a resolution of 61 Hz/bin) and clearly shows the quantization noise is being shaped as expected. The audio band zoom of Figure 2.20(b) reveals an additional tone at DC resulting from offset voltages in the lowpass modulator. This behavior is

expected and will not adversely affect the converter performance, as audio and voice band applications do not extend in frequency to DC.



(a) Nyquist Band (b) Audio Band

Figure 2.20: Experimental Results of the Fabricated IC

Over the voice-band, the peak signal-to-noise ratio (SNR)[1] was computed and found to be 82 dB, equivalent to approximately 13 bits of resolution. For input levels resulting in this peak SNR, the modulator achieves a spurious-free dynamic range (SFDR)[2] of 83 dB, limited by the third harmonic frequency component, visible in the audio-band output spectrum of Figure 2.20(b). The physical modulator therefore meets the design specifications outlined in Section 2.2.1 and is well-suited for the intended voice-band applications.

2.3 Conclusion

In this Chapter, the basic concepts of lowpass $\Delta\Sigma$ modulation for analog-to-digital conversion have been presented. A second-order voice-band modulator has been used to illustrate the basic design process from specification through to layout. Experimental results indicate the modulator is functioning correctly, and meets the desired specifications. We are now well prepared to investigate the novel eighth-order bandpass design of Chapter 3.

1. SNR defined as the ratio of the input power to the integrated noise floor over the signal band
2. SFDR defined as the ratio of the input power to the peak non-signal spectral component in the signal band (0-4kHz)

Chapter 3 : A Novel High-Order Bandpass ΔΣ Modulator

This chapter begins with an introduction to the bandpass modulation concept and its merits. The step-by-step approach that was used to design an eighth-order bandpass modulator will then be described. Implementation and layout considerations will prove be to key to overall performance and will be examined in detail. The methods used to test the modulator throughout the design process will also be investigated. The chapter will conclude with experimental results from a fabricated prototype.

3.1 The Bandpass Approach

Recall from Chapter 2 that a general ΔΣ modulator has the structure shown in Figure 3.1, repeated here for convenience.

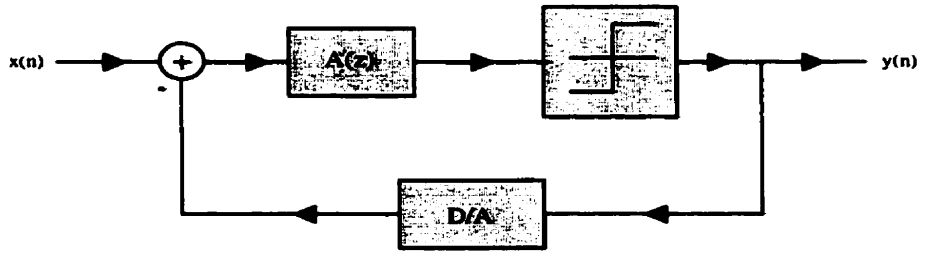


Figure 3.1: General Modulator Structure

In the previous lowpass case, the loop filter, A(z), was chosen so that the NTF shaped the quantization noise outside of the low frequency band. However, A(z) can be conveniently

chosen to shape the noise out of any desired band of operation. For example, one technique is to apply the lowpass-to-bandpass transformation described by Eq. (3.1) to the loop filter.

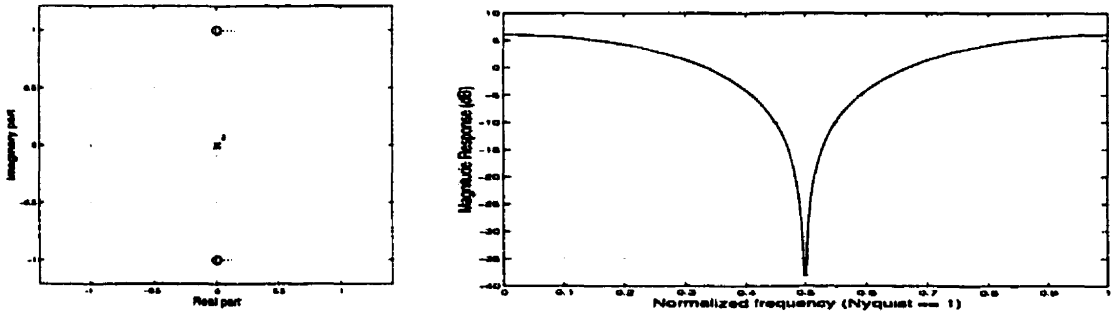
$$z \rightarrow -z^2 \tag{3.1}$$

This approach can be used without altering the stability characteristics of the modulator whatsoever[7]. That is, if the lowpass modulator is stable, so will be the bandpass equivalent. Applying this to the simple first order lowpass modulator of Section 2.1.3 yields the following signal and noise transfer functions:

$$NTF = (z^2 + 1)/z^2 \tag{3.2}$$

$$STF = -1/z^2 \tag{3.3}$$

As can be seen, the STF consists only of a a simple inversion and two pure delays. Therefore, it has linear phase and can be easily reconstructed without distortion. The new NTF, however, is vastly different and is shown in Figure 3.2.



(a) (b)

Figure 3.2: (a) pole-zero and (b) magnitude response plots of a BP NTF

Note that the NTF zeros are now centered about half the Nyquist frequency, not zero. Therefore, this modulator would be well suited to operate on signals with frequencies of one fourth the sampling rate.

The advantage of choosing a bandpass modulator over its lowpass counterpart comes when working on high frequency signals in a narrow bandwidth. With a bandpass modulator, it is only necessary to remove the noise from the narrow signal bandwidth, keeping the oversampling ratio (defined in Eq. (2.1)) high. This is because noise can be pushed onto both

sides of the band of interest. With a lowpass modulator on the other hand, the noise would need to be shaped out of the entire region $[0,f_{SIG}]$. Therefore the operational bandwidth would be much larger and the effective OSR greatly reduced. The only drawback of the bandpass approach is that for the same degree of noise shaping as a lowpass modulator, double the order is required. This is because each NTF pole and zero must have a complex conjugate in order to avoid having complex co-efficients in the loop filter.

In theory, delta-sigma modulators can be extended to an arbitrary high-order [6], to meet the continuously increasing requirements imposed on present-day A/D converters. Provided stability is achieved, high-order modulators have the advantage that the resolution and/or bandwidth obtained is considerably higher than low-order ones. Bandpass modulators allow the extension of these benefits to narrowband signals centered at higher frequencies. They are thus prime candidates for use in receiver front-ends, converting IF signals directly to digital form.

The eighth-order bandpass modulator design of this chapter is intended to meet the A/D conversion needs in the increasingly popular area of digital RF receivers. As depicted in Figure 3.3, the bandpass modulator is the key component in the A/D system that is used to convert the IF signal of a superheterodyne receiver directly to digital form. Any further processing, such as IF filtering and demodulation can now be handled digitally. This scheme makes the system more versatile, as the digital hardware can easily adapt to changing communication protocols. Furthermore, this approach does not suffer from DC offset and low frequency noise problems (when compared to mixing and lowpass conversion) and there is no I/Q mismatch in the quadrature demodulation since this step is performed in the digital domain[10].

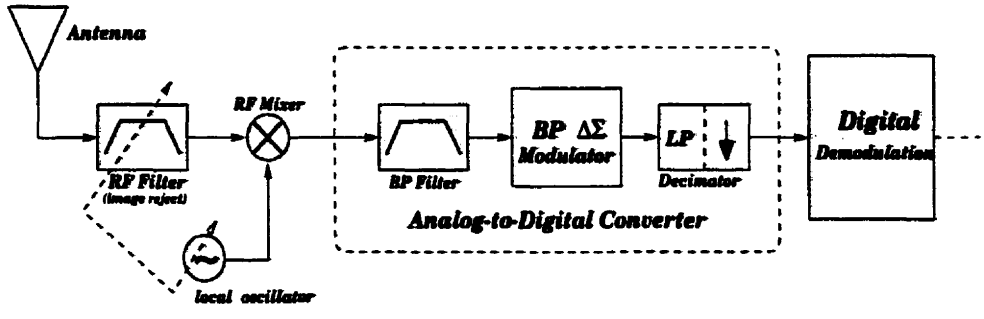


Figure 3.3: Simplified Digital RF Receiver

3.2 Modulator Design

This section will first briefly outline the specifications and goals of the design. A step-by-step procedure will then be given, outlining the design procedure that was followed.

3.2.1 Design Objectives

To address the need of digital radio, the modulator is designed to operate on signals within a 200 kHz bandwidth, centered at the commonly used IF of 10.7 MHz. When the IF signal band is centered at $f_S/4$, f_S being the clocking frequency, the circuit must be clocked at 42.8 MHz. However, because a high-order modulator is employed, it is also possible to centre the IF band at $3f_S/4$, allowing for either one third the clock rate (easing decimation), or processing of signals three times higher in speed (IF band centered at 32.1 MHz) while still achieving excellent results.

To achieve the high resolution required in modern-day wireless systems, an eighth-order modulator was chosen. Combined with the OSR of 107, derived from the above bandwidth and clock speed, a theoretical resolution of over 20 bits should be possible [6].

In addition to obtaining a working prototype of a future application, these ambitious design constraints will serve another purpose as well. The work will verify and further the design methods of high-order modulators; and help to understand and solve some of the problems encountered with them.

3.2.2 NTF Design for Desired Specifications

The mathematical expression for the NTF was established using DSMOD, a software tool developed at McGill for the design of ΔΣ modulators [11]. By specifying the modulator's passband, OSR, and various other parameters, the program produces an optimal NTF (butterworth with optimally placed zeros) which is a compromise between stability and SNR. The resulting NTF is given by Eq. (3.4) below.

$$NTF_{DSMOD}(z) = \frac{N_{DSMOD}(z)}{D_{DSMOD}(z)} = \frac{1 + 3.99926z^2 + 5.99852z^4 + 3.99926z^6 + z^8}{0.396502 + 1.9497z^2 + 3.646z^4 + 3.08274z^6 + z^8} \quad (3.4)$$

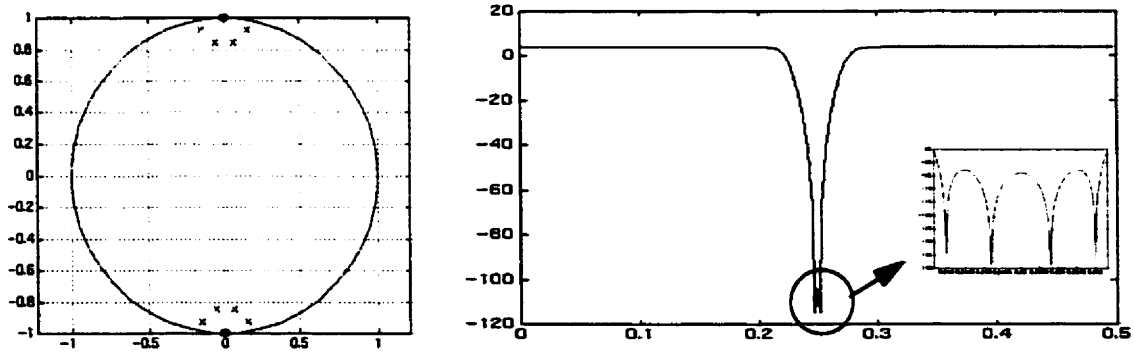
The expected specifications of a modulator characterized by the NTF of Eq. (3.4) are detailed in Table 3.1 which follows:

Specification	Value
Order	8
Center Frequency	0.250000
Oversampling Ratio	107.000
Lower passband Edge	0.247664
Upper passband Edge	0.252336
Bound on NTF	1.60000
Optimal Input Amplitude	0.50000
Maximum NTF Magnitude	1.58781
Expected SNR (estimate)	128.276

Table 3.1: Theoretical Modulator Specifications

One parameter that appears in Table 3.1 which has yet to be introduced is the NTF Bound. It specifies the maximum allowable level of the NTF amplitude. This factor plays an important role in ensuring the overall stability of the modulator. Specifically, the NTF bound is typically limited to a threshold determined by one of the many rules of thumb[6]. The DSMOD design program also attempts various NTF bounds and input signal amplitudes and returns with the NTF, the NTF bound, and the input level that maximize the SNR for the given specifications.

The corresponding pole-zero locations and magnitude response are shown in Figure 3.4, where the four NTF zeros and associated notches are clearly visible.



(a) Pole-Zero Plot (b) Magnitude Response

Figure 3.4: Pole-Zero and Magnitude Response Plots of NTF using DSMOD

It should be noted that the location of the poles in the design of the NTF for ΔΣ modulators is a compromise between stability and SNR. Placing the poles well inside the unit circle (i.e. close to the origin) will result in deep notches in the signal band (as a result of the zeros) and give excellent noise reduction there. However, remembering that the total noise power is constant, the noise outside the signal band will have to rise and will often exceed the practical stability limit of 2, proposed by Lee in [14] resulting in an unstable modulator. On the other hand, placing the poles too close to the zeros will ensure stability but decrease SNR as the noise in the signal band will rise due to the closely placed poles. Therefore, it is for this reason that an optimal location of the poles and zeros is usually found for a given NTF bound, as with the case of DSMOD.

As the current version of DSMOD is intended for ΔΣ oscillator applications, the STF returned by DSMOD is unfortunately restricted to be unity. As will become evident, this is neither a necessary nor desirable feature when the modulator is implemented with the SFG-level structure that follows. For this reason, the STF was designed separately as will be discussed in Section 3.2.5. However, the STF, does have the same denominator as the NTF (recall Eq. (2.6)), which considerably restricts the STF design.

3.2.3 Selecting a Structure

The next step in the design is to determine the physical structure that will implement the theoretical NTF and best meet the demands placed on the hardware such as matching accuracy and speed requirements. To begin, the fourth-order structure given in [12] can be extended to yield the general eighth-order structure shown in Figure 3.5.

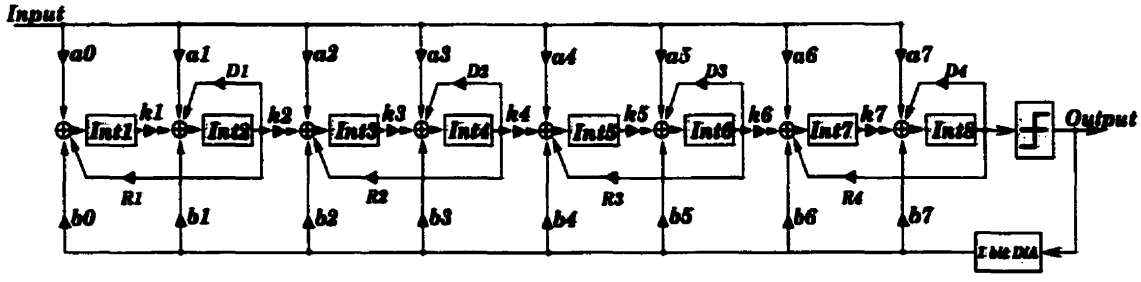


Figure 3.5: General Eighth-Order ΔΣ Modulator Structure

It is composed of a cascade of resonators, easily realizable in the SC technique, each forming an NTF complex zero pair. The local feedback paths weighted by the R_i and D_i coefficients (for i=1...4) specify the locations of these NTF zeros. The remaining feedback paths, from the output of the comparator, scaled by the b_i coefficients (for i=0, 1,...7) are used in conjunction with the above **R** and **D** coefficients (boldface is used to denote vector quantities) to define the NTF and STF pole's locations. Finally, the **a** coefficients (a_0...a_7) are used to establish the STF zeros, while the **k** coefficients (k_1...k_7) are used in scaling for maximum dynamic range.

One attraction of the above structure is that, being composed primarily of integrators, it lends itself quite easily to SC implementation. However, it has yet to be determined whether the integrators are of the delayed (non-inverting) or non-delayed (inverting) type. As will be discussed next, this small change in phasing can have a major impact on performance.

(i) The Lossless Digital Integrator (LDI) Structure

This popular structure used in [7] is one in which each second order section is composed of a LDI two-integrator-loop topology. That is the first and second integrators would be of the delayed and non-delayed types respectively, as shown in Figure 3.6.

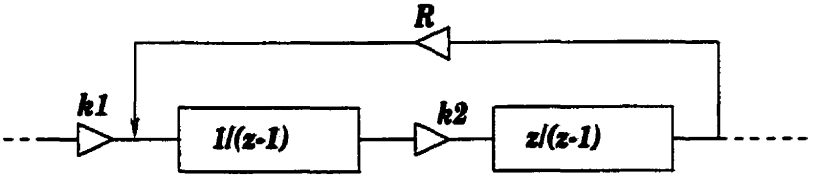


Figure 3.6: LDI Two-Integrator-Loop Topology

Each of the coefficients in Figure 3.6 directly represents a capacitor ratio when the LDI loop is implemented using the SC technique. The transfer function of this second order block is given as:

$$A(z) = \frac{k_1 k_2 z}{z^2 - (2 + k_2 R)z + 1} \tag{3.5}$$

The poles of this second order section will determine the NTF zeros in the overall structure, and are therefore crucial in achieving a high inband noise suppression. From Eq. (3.5), it

can be seen that the poles will lie on the unit circle, regardless of any capacitor mismatches, represented by k_1 and k_2. This is advantageous because it ensures that a deep notch will always exist in the overall NTF. However, note that k_2 can affect the phase angle of the poles of A(z), and thus shift the frequency of the notch slightly.

To understand the speed constraints this structure places on the amplifiers, refer to the SC implementation shown in Figure 3.7, ignoring at this point the parenthesized clock phases.

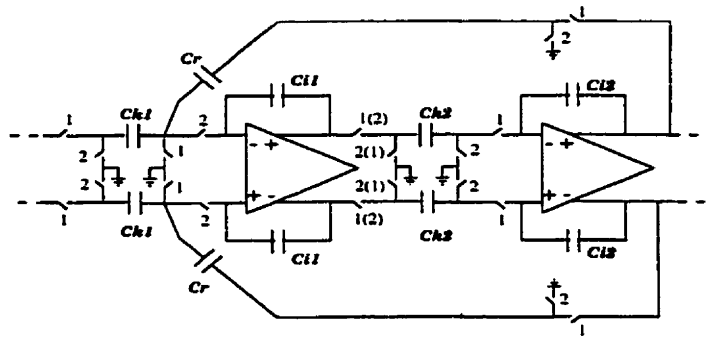


Figure 3.7: LDI and modified LDI (parenthesized clock phases) SC topologies

First note that the structure has a differential implementation, as will all the candidates under study. This is to cancel, to first order, the noise that the digital circuitry adds through the substrate. The integrators used are parasitic insensitive, and switch-sharing has been used in the usual manner. In the above, the capacitor ratio C_{k1}/C_{i1} forms the coefficient k_1, the ratio C_r/C_{i1} forms the ratio R, etc.

Referring to Figure 3.7, it is clear that on clock phase ϕ_1, the first amplifier must drive a load entering the second amplifier, which inturn must simultaneously settle the input transient and drive it's own load. This has a second order transient behavior due to the coupling of the two sections, an thus exhibits very poor settling[7].

(ii) The Modified LDI Structure

The modified LDI structure attempts to overcome the above mentioned problem associated with the basic LDI topology. There is a subtle change in the second integrator phasing, as seen in Figure 3.7.

Note that because the second stage is now non-inverting, it is necessary to feedback from the differential half-circuit counterpart, to ensure negative feedback.These small changes, however, do nothing to the overall transfer function given in Eq. (3.5). Therefore, this structure is also relatively insensitive to capacitor mismatch errors.

Referring to Figure 3.7, we see that on clock phase ϕ_1, the second amplifier has to simultaneously settle an input transient and drive its load, while the first amplifier remains idle. On ϕ_2, however, the situation is reversed. The first amplifier is overloaded, and the second is idle. Not only does this lead to poor settling behavior [7], with a large time constant on both phases, it is an inefficient use of hardware resources. Therefore although de-coupling the amplifiers improves the settling compared to the basic LDI structure, it is still insufficient for the speed requirements of this design.

(iii) Structures using the Unit Delay Cell

Rather than forcing the structure to be composed of integrators, much design freedom can be gained if instead, a unit delay cell [10] is used as a building block. With this approach, arbitrary SFG level designs can be quickly transferred to a SC implementation with ease. The unit delay cell is shown in Figure 3.8.

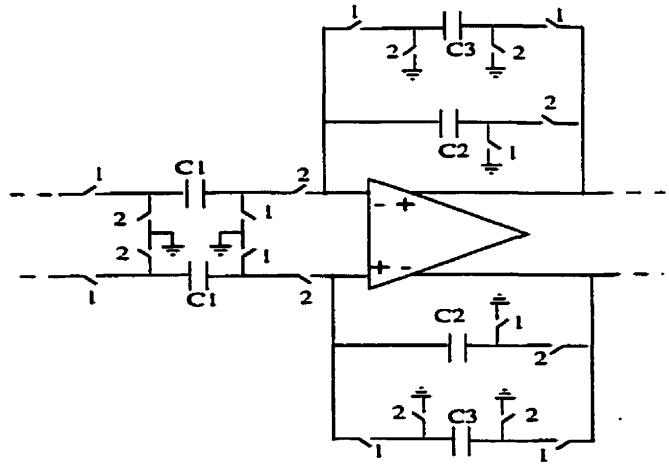


Figure 3.8: SC Implementation of the Unit Delay Cell

To obtain a full clock period delay, both the input and output voltages should be sampled on ϕ_1:

The transfer function of this basic cell depends on which clock phase the output is taken, as seen in Eqs. (3.6) and (3.7) below.

$$A(z) = (C_1/C_2) \cdot z^{-1/2} \quad (\textit{sampled on } \phi_2) \tag{3.6}$$

$$A(z) = (C_1/C_3) \cdot z^{-1} \quad (\textit{sampled on } \phi_1) \tag{3.7}$$

The drawback of the delay cell comes from its settling behavior. When these cells are cascaded, the amplifiers will have to settle their input transients and drive their loads simultaneously. Therefore, the settling behavior is expected to be in the same range as the modified LDI structure[7].

(iv) Forward Euler (FE) Structure

In this structure, each second order section is composed of a two-integrator FE loop, as shown in Figure 3.9.

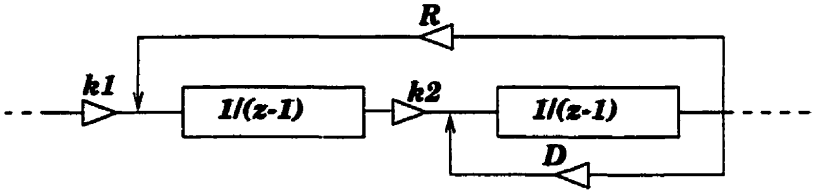


Figure 3.9: Basic FE Structure

Both integrators in this case are of the delayed (non-inverting) type. Again, each of the coefficients in Figure 3.9 would directly represent a capacitor ratio when the FE loop is implemented using the SC technique. The transfer function of this second order section is given as:

$$A(z) = \frac{k_1 k_2 z}{z^2 - (2 + D)z + (1 - k_2 R + D)} \tag{3.8}$$

From Eq. (3.8), we see that the poles will only lie on the unit circle provided k_2*R = D. This however, can not be guaranteed, as it depends on the matching accuracy of the capacitors. Therefore, the zeros of the overall NTF may stray off the unit circle causing the NTF notch to be shallower. In addition they may have a phase error, causing a frequency shift of the NTF notch, similar to the LDI case.

The advantage of using this structure, however, comes when operating at higher speeds. This can be seen by referring to the SC implementation shown in Figure 3.10.

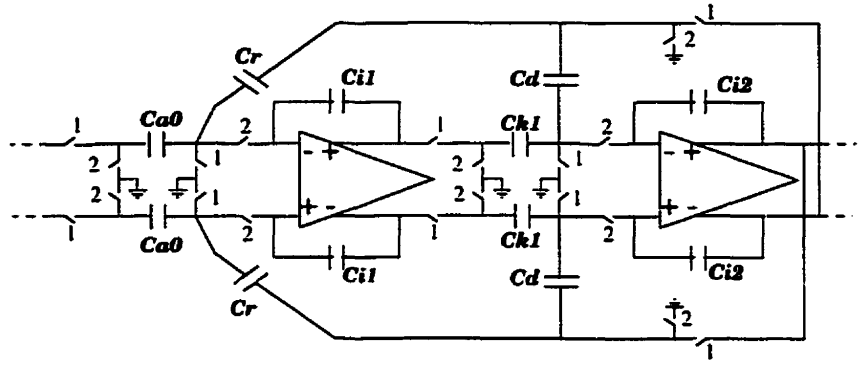


Figure 3.10: SC Implementation of the FE Structure

Observing Figure 3.10, it is evident that the amplifiers are not only de-coupled from each other, but from their loads also. That is on any given phase, each amplifier will only either have to settle an input transient or drive a load. This is the most efficient use of the available resources. One slight setback is that there is the extra capacitor, Cd, which further loads the second amplifier on ϕ_2. In spite of this, the FE structure still exhibits better settling behavior than any of the structures encountered thus far. Recall that the modified LDI would have a large time constant on *both* phases. Here, only the time constant on ϕ_2 is slightly degraded.

Further detail into the loading behavior of the circuit will be discussed in Section 3.3.1. At this point, it is evident that the FE structure will have the best settling behavior among all the other options. It is for this reason that it has been chosen to implement the eighth-order modulator, despite its greater dependence on capacitor matching. In addition, results from a second order modulator in [7] indicate that above 30 MHz, the FE structure outperforms its LDI counterpart.

3.2.4 Obtaining the Coefficients that control the NTF

Having decided to employ the FE loop as the basic second-order building block, the overall SFG-level structure can be redrawn with the knowledge that all integrators will be of the delayed-type. This is shown in Figure 3.11.

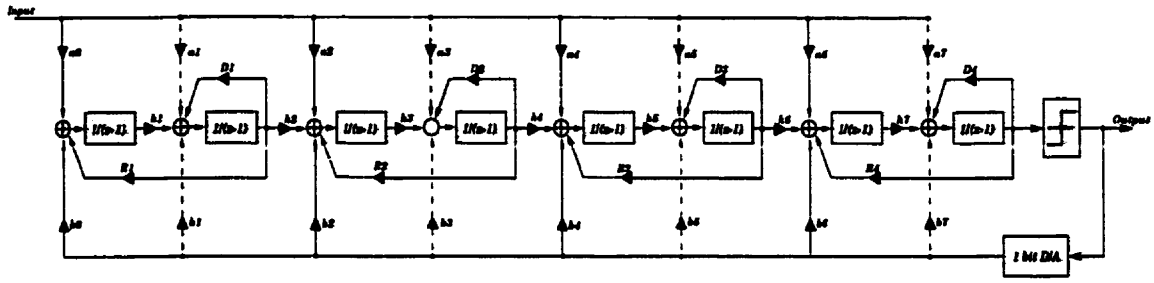


Figure 3.11: SFG-level Structure (based on FE loop)

In Section 3.2.3, it was already seen how each second-order section in Figure 3.11 forms a complex NTF zero pair via the **R** and **D** coefficients. This step in the design is concerned with finding the values of these coefficients that best meet the ideal NTF. In addition, we wish to find values for the **b** coefficients, which in conjunction with the above **R** and **D** coefficients will define the NTF and STF shared poles.

To determine numerical values for the coefficients controlling the NTF, the NTF of the SFG-level structure was first found in symbolic form.using IFAP [13]. Note that during this step, it is worthwhile to represent each of the coefficients in the structure's equations in such a manner so as to correspond directly to a capacitor ratio. This will allow the mapping from the SFG-level structure to the SC-structure to be simple and direct. The resulting NTF has the form shown in Eq. (3.9) below:

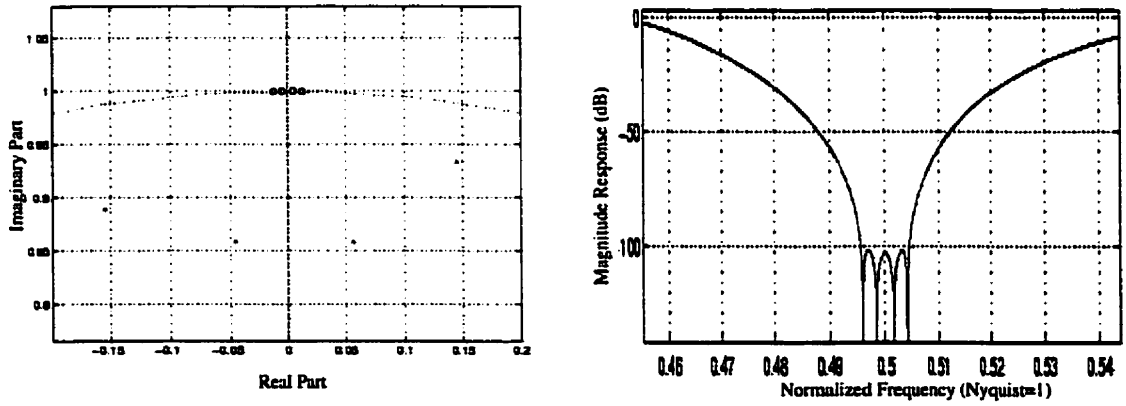
$$NTF_{sym}(R, D, b, k, z) = \frac{N_{sym}(R, D, k, z)}{D_{sym}(R, D, b, k, z)} \tag{3.9}$$

The symbolic NTF above produced using IFAP was then compared to the optimal numerical solution provided by DSMOD expressed in Eq. (3.4). By equating equal powers of z for each of the numerators and denominators, two sets of equations (consisting of 8 equations per set) are produced. Maple, a symbolic analysis program, was then used to help solve these equations in order to determine the structure coefficients. To simplify matters,

the **k** coefficients are temporarily set to unity as enough degrees of freedom exist to solve the equations without their use. Since the internal feedback coefficients (**R**'s and **D**'s) alone control the NTF's numerator, the equations controlling the NTF numerator, resulting from equating equal powers of z terms in both N_{DSMOD} and N_{sym} are solved first. This establishes values for the **R** and **D** coefficients. The denominator equations are then solved simultaneously for the remaining eight **b** coefficients, having replaced the **R** and **D** coefficients with their numerical values. Thus, DSMOD's NTF is mapped onto the modulator structure.

After noticing that some of the **b** coefficients (shown by dashed lines in Figure 3.11) were extremely small, it was decided to set these coefficients to zero, thus removing these feedback paths altogether. This will make implementation more practical by avoiding large spreads in capacitor values. Initially, this caused the structure to become unstable, however, after optimizing the remaining four **b**'s using Matlab, the original performance was re-established.

The optimization involved moving the poles formed by the remaining four **b**'s as close as possible to their original location (when all 8 **b**'s were used) under the constraint that the NTF bound remains below 1.6 and that none of the poles leaves the unit circle. The resulting NTF and its pole-zero plot are shown in Figure 3.12.



(a) pole-zero plot (b) magnitude response

Figure 3.12: Optimized NTF after 4 of the 8 **b**'s were set to zero

The **a** coefficients, which together with the above established **R**, **D** and **b**'s set the STF zeros, must also be determined. This task will be examined next.

3.2.5 Obtaining the Coefficients that control the STF

As previously mentioned, the STF poles are identical to those of the NTF, and are thus already determined at this point. We are therefore left to find the best location of the STF's zeros to achieve optimal magnitude and phase responses. The STF is not restricted to be unity, as in the structures of DSMOD intended for use in ΔΣ oscillator circuits. In fact, it is not possible to implement a unity-STF, as the 8th-order structure does not have any feedforward to the comparator which would require an extra summing circuit. It is also sometimes desirable to allow some freedom in the STF design, so as to help attenuate adjacent channels.

Matlab optimization routines were used to find the best set of feedforward coefficients (a0...a7 in Figure 3.11) to meet the design requirements. Of primary importance is that the phase remain linear in the signal band so that the signal can be reconstructed without distortion. The average delay distortion relative to the band center, as well as the intercept distortion were minimized by the optimizer. In addition, the magnitude of the STF was kept as flat as possible in the signal band.

As with the NTF design, during optimization, the odd coefficients shown as dashed lines in Figure 3.11 were set to zero, once again to render the SC realization more practical. The simplified structure after both the odd feedback and feedforward coefficients have been removed is shown below in Figure 3.13.

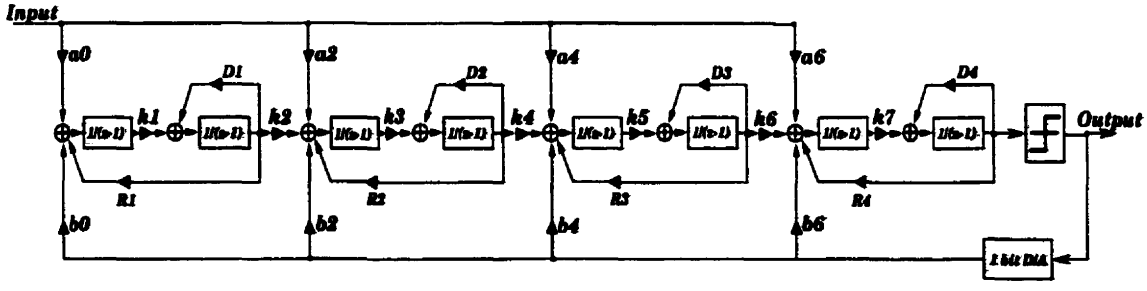
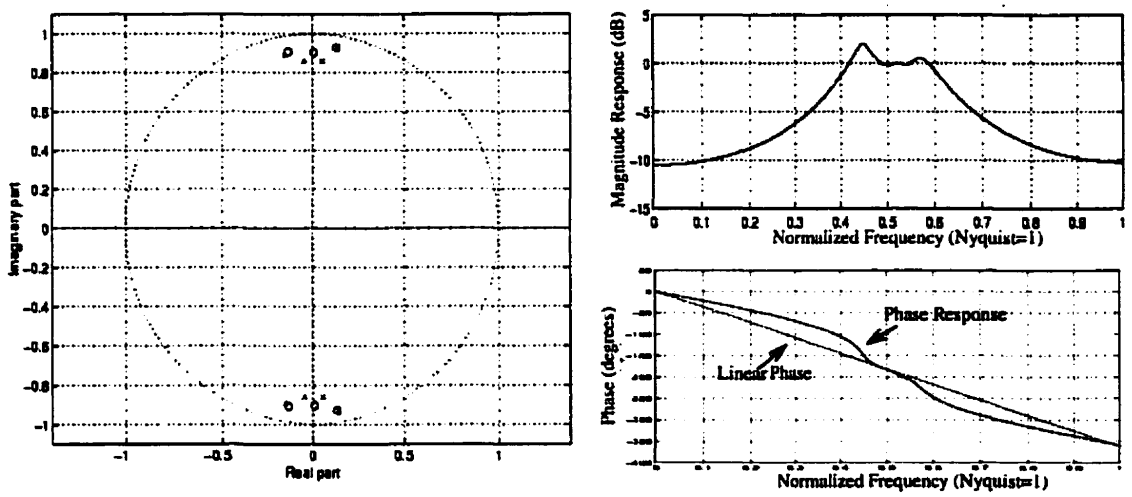


Figure 3.13: Modulator with odd feedforward coefficients set to zero

The new location of the STF zeros is shown in Figure 3.14(a). Note the poles have not changed, and were set by the NTF optimization. After optimization, the STF has the mag-

nitude and phase responses shown in Figure 3.14(b). While the magnitude response shows that the signal transfer function does provide some attenuation to most out of band signals, in the narrow passband the maximum ripple does not exceed 0.03 dB.



(a) Pole-Zero Locations (b) Magnitude and Phase Response

Figure 3.14: Optimized Signal Transfer Function Response

Much emphasis was placed on the phase, to ensure it remained linear in the band of interest, even without the odd feedforward coefficients. An extremely low average delay distortion value in the signal band was optimized for, resulting in phase linear to approximately 0.001 degree.

3.2.6 Scaling for Maximum Dynamic Range

At this point, numerical values of the coefficients of the final structure have been determined. The next step in the design is to scale the structure for maximum dynamic range (DR). This step involves finding the spectral peaks of all the transfer functions from input to integrator outputs and equating these peaks in magnitude to that of the overall transfer function. Recalling that an integrator is realized by an amplifier which has a limited swing, achieving the maximum possible dynamic range requires equalizing all the amplifier peaks. Otherwise, an amplifier that happens to have a high gain at a particular frequency would clip while all the other amplifiers functioned properly and cause distortion.

The DR scaling process was performed with the aid of Matlab's Simulink where the structure was first tested to ensure its proper operation. Next, a white noise source was used to simulate a swept sinusoidal input of constant amplitude. The transfer function at the output of each intgerator was then recorded using Simulink's averaging spectrum analyzer. With the spectral peaks of all the integrators obtained, dynamic range scaling was performed in the usual manner [15].

After the DR scaling was completed, it was noticed that two of the coefficients, namely k_2 and k_4 were too small and would result in a big spread in capacitor values. For this reason these two coefficients were scaled upward to a reasonable value and the necessary adjustments in the corresponding **R**'s and **k**'s were performed. For example, k_2 was multiplied by a factor of 3.2. So as not to affect the signal processing, the coefficient k_1 was divided by this factor, and R_1 multiplied by the same factor of 3.2.

After the above adjustments, two of the integrators peaked at less than the overall transfer function maximum gain. This compromise was necessary to ensure practical capacitor values given the technology of choice. Table 3.2 details the values of the structure coefficients after the DR scaling procedure and the above mentioned adjustments.

Coefficient	Value	Coefficient	Value
a_0	-0.302998	D_1	-1.9747
a_2	0.300026	D_2	-1.9901
a_4	-0.301294	D_3	-2.0099
a_6	0.311119	D_4	-2.0253
b_0	-0.309383	k_1	0.466009
b_2	0.338147	k_2	0.228715
b_4	-0.440347	k_3	0.778049
b_6	0.570072	k_4	0.376147
R_1	-4.23747	k_5	1.55714
R_2	-2.55781	k_6	0.355330
R_3	-1.29076	k_7	1.60163
R_4	-1.26453		

Table 3.2: Modulator Coefficients' Values After DR Scaling and Adjustments

3.3 Switched-Capacitor Implementation

At this point we wish to realize the SFG-level structure using the SC technique. The fully-differential design will make exclusive use of parasitic insensitive SC integrators, and share switches in the usual manner. Other issues that must be addressed will be discussed next.

3.3.1 Capacitor Sizing

Thus far we have determined the optimal structure coefficients, which are to be realized by capacitor ratios. In determining the absolute capacitor sizes, there are several issues that must be considered which set the upper and lower size limits.

(i) Upper-Bound Constraints

Typically, the capacitor arrays tend to consume a large portion of the silicon area in SC designs. Therefore, once the more crucial design constraints are satisfied, their size should be kept to a minimum. However, due to the high speeds of this particular design, amplifier loading and not area usage was the primary concern limiting the maximum capacitor size.

With a clock rate of 42.8 MHz, the largest transient in the circuit should settle within approximately 11.5 ns. The circuit time constants can be found quite easily since the amplifiers in the FE structure are de-coupled from each other, and from their loads.

The analysis is similar to that used in SC filters[15]. That is the time constant is given by

$$\tau = 1 / (\omega_t \beta) \tag{3.10}$$

where, in the above, β represents the feedback factor given by a simple capacitor divider. The factor ω_t represents the unity gain bandwidth of the transconductance amplifier and is given by

$$\omega_t = G_m / C_L \tag{3.11}$$

where, in the above, G_m represents the amplifier transconductance and C_L is the total load capacitance at the amplifier output. Thus, for example, consider the first amplifier in the complete SC circuit of Figure 3.19 on page 52. On ϕ_1, the time constant would be given by

$$\tau_{11} = \frac{C_{k1} + C_{lp} + (C_{i1} \| C_p)}{(C_{i1}/(C_{i1} + C_p))G_m} \tag{3.12}$$

where, C_p and C_{lp} represent the amplifier input and output load parasitics respectively.

To minimize the overall loading effect on the circuit, the following approach was taken. Firstly, the loading equations for each amplifier on each clock phase, 16 in total, were determined in the same manner as Eq. (3.12) above. As many of the capacitors appear in several of the amplifier loading equations, it would not be feasible to determine optimal values for them using hand analysis. Therefore, a Matlab script, using built-in optimization routines was employed. The eight integrator capacitor values were used to specify the eight degrees of freedom, as the other capacitors can be derived from them using the coefficient values listed in Table 3.2 on page 42. Therefore, the optimizer was used to vary the eight Ci's such that the maximum time constant associated with each clock phase, described by the amplifier loading equations, was minimized. This resulted in worst case time constants of 1.5 ns and 1.9 ns on ϕ_1 and ϕ_2 respectively.

Note that the same results would *not* be obtained by using the SC technique of scaling for minimum total capacitance. This is because there are fixed parasitic capacitances, C_p and C_{lp}, which do not scale. For example, in Eq. (3.12), if C_{i1} becomes very small compared to C_p, the time constant will start to increase. However, once the dominant time constants have been minimized, it is possible to scale non-dominant sections for minimum total capacitance as long as they do not cause a dominant time constant. This procedure was applied to amplifier sections four through seven in Figure 3.19.

(ii) Lower-Bound Constraints

One issue that can affect the minimum allowable capacitor size is amplifier stability, as the OTAs used in the design are uncompensated. Therefore, if the load capacitors are not large enough (approx 0.5 pF combined), a dominant pole may not be formed. As will be seen

shortly, this constraint was easily satisfied for every amplifier output node. Care must also be taken to ensure that the capacitors remain large enough such that matching accuracy is not a problem. Matching difficulties can arise as the capacitor size is reduced due to decreased area-to-perimeter ratio, as well as increased significance of routing parasitics.

The most serious limitation on the minimum allowable capacitor sizes of this design stems from their corresponding noise contribution. Capacitors themselves do not generate any noise, but rather store the sampled noise originating from switch resistances. As explained in [22], the total mean-squared noise resulting from a single switch is given by:

$$V_{n(rms)}^2 = kT/C \tag{3.13}$$

where k is Boltzmann's constant (1.38×10^{-23} JK^{-1}), and T is the temperature in Kelvins. In the eighth-order SC circuit (Figure 3.19 on page 52), each capacitor samples the noise from two sets of switches, one per clock phase, so the accumulated noise would actually be double that of Eq. (3.13).

To assess the effect of kT/C noise in the eighth order modulator, it is important to realize that not every capacitor in the circuit will contribute equally to the inband noise power. Specifically, only the noise from the input stage will propagate to the output without being shaped, to some extent, out of the signal band. Therefore, an estimate of the inband noise power can be obtained by input-referring the noise from the first stage capacitors. This procedure is shown in Eq. (3.14) which follows:

$$V_{n(rms)}^2 = \left[\frac{2kT}{C_{a0}} + \frac{2kT}{C_{r1}} \cdot \left(\frac{C_{r1}}{C_{a0}}\right)^2 + \frac{2kT}{C_{b0}} \cdot \left(\frac{C_{b0}}{C_{a0}}\right)^2\right] \cdot \frac{2}{OSR} \tag{3.14}$$

The extra multiplicative factor of two in Eq. (3.14) is included to account for capacitors on both differential halves of the circuit.

One would ideally choose the capacitors large enough such that kT/C noise is non-dominant. However, this approach would have led to excessive settling times, as described in the previous section. For this reason, the unit capacitor size had to be reduced to 0.1 pF as a compromise between matching, opamp stability, and settling. This choice results in a total

inband noise power of approximately -77 dB (with respect to the feedback references). Albeit not an optimal solution, it was deemed sufficient to assess the feasibility of the design structure through a first generation prototype.

(iii) Final Capacitor Values

After taking the above mentioned considerations into account and performing the Matlab optimization, the final values of the capacitors were obtained. These values which correspond to the complete SC circuit shown in Figure 3.19 on page 52, can be seen in Table 3.3.

Capacitor	Value (pF)	Capacitor	Value (pF)	Capacitor	Value (pF)
C_{a0}	0.1268	C_{k4}	0.1248	C_{d4}	0.8405
C_{a2}	0.1343	C_{k5}	0.3893	C_{i1}	0.4185
C_{a4}	0.1000	C_{k6}	0.1142	C_{i2}	0.4865
C_{a6}	0.1000	C_{k7}	0.6647	C_{i3}	0.4478
C_{b0}	0.1000	C_{r1}	1.7734	C_{i4}	0.3000
C_{b2}	0.1514	C_{r2}	1.1453	C_{i5}	0.3319
C_{b4}	0.1462	C_{r3}	0.4284	C_{i6}	0.2500
C_{b6}	0.1832	C_{r4}	0.4064	C_{i7}	0.3214
C_{k1}	0.2267	C_{d1}	0.9607	C_{i8}	0.4150
C_{k2}	0.1024	C_{d2}	0.5970		
C_{k3}	0.2334	C_{d3}	0.5025		

Table 3.3: Capacitor Values used in the SC structure

3.3.2 Switch Design

Transmission gates, of the form shown in Figure 3.15 (redrawn here for convenience), were used to implement the sampling switches in the SC design. This section will outline the factors that motivate the use of transmission gates before examining how two factors, on resistance and charge injection, influence the design of these switches.

(i) The Merits of Transmission Gates

One advantage of transmission gates, discussed in Chapter 2, is their ability to accommodate highly varying node voltages. Specifically, it was shown how a transmission gate will reliably conduct both high and low voltage levels, allowing a greater signal swing. A second benefit of using transmission gates, as opposed to a singular MOS-switch, stems from the reduced levels of charge injection (CI) produced. This is significant in that the CI mechanism can lead directly to harmonic distortion in SC circuits, as described next.

Recall that CI refers to the process whereby channel charge stored in a MOSFET switch during the conduction phase migrates into the circuit once the switch is turned off. The problem arises when this channel charge settles onto a sampling capacitor and becomes indistinguishable from the signal information. The injected charge is not necessarily related to the input voltage signal in a linear manner due to the non-linear C-V relation of the MOSFET switch, and more importantly the unpredictable nature with which the channel charge distributes once the switch turns off. Therefore, the error voltage on the sampling capacitor is a non-linear function of the input signal, which leads directly to harmonic distortion in the circuit output.

Of the many techniques that exist to minimize charge injection [17], the use of transmission gates with carefully sized MOS transistors was found to be the most effective. Referring to Figure 3.15 below, the composite switch combats CI by the fact that both the NMOS and PMOS conduct simultaneously when the switch is on. Therefore, when it turns off, the holes from the channel of the PMOS will theoretically cancel with the electrons from the NMOS. However, to reap these benefits without introducing other distortion mechanisms, the MOSFETs in the transmission gates must be carefully sized, as will be discussed next.

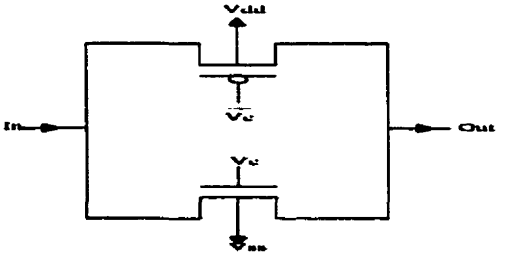
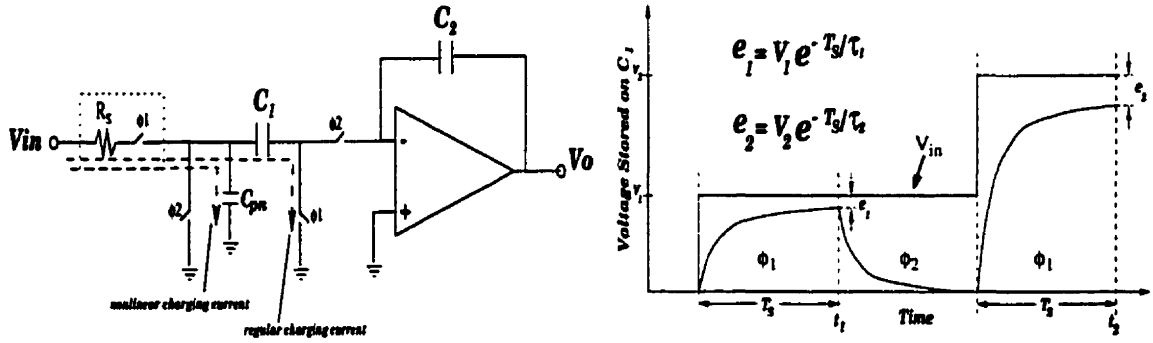


Figure 3.15: Transmission Gate

(ii) Transistor Sizing in the Transmission Gates

Of major concern in sizing the transmission gates is that they do not have a large on resistance. If the time constants associated with the switch conduction resistances contribute significantly to the overall settling behavior, a large distortion component will be introduced. This can be understood by considering the operation of the simple SC circuit in Figure 3.16(a), where the on resistance of the input switch has been explicitly shown, and referring to the voltage waveforms of Figure 3.16(b).



(a) Charging Currents in an SC Integrator (b) Settling Behaviour

Figure 3.16: Analysis of Settling Errors during the Charging Phase in SC circuits

Due to incomplete settling on the charging phase, ϕ_1, at the sampling instants t_1 and t_2, the voltage stored on the capacitor C_1 will be in error by amounts of e_1 and e_2 respectively. If these errors are constant, or related to the input signal in a linear manner, no distortion products will be produced. However, any non-linear variation in these errors will lead directly to harmonic distortion in the output. Referring to Figure 3.16(b), this can be caused by any variation whatsoever (be it linear or nonlinear) between the time constants, τ_1 and τ_2. These time constants are determined by the RC combination in the current charging path, as depicted in Figure 3.16(a).

The variation in settling rates can be attributed to the nonlinear junction capacitance, C_{pn}, and variation in the switch resistance, R_S, with the input signal level. This latter effect can be lessened by carefully sizing the relative aspect ratios between the nMOS and pMOS transistors in the transmission gate to account for the difference in carrier mobilities. By making $(w/l)_p \sim 3(w/l)_n$, the same resistance will be felt by positive signals (where the

nMOS is the primary conductor) as felt by negative signals (where the pMOS is the primary conductor).

The above approach helps alleviate the variation in resistance issue, however, it does not overcome the non-linear settling error problem completely. To do so requires reducing the switch resistance, R_S, such that the time constant associated with its settling is negligible compared to that of the OTA discussed previously. This typically corresponds to switch transistor aspect ratios in the range of 100 or more. At the time of fabrication, the importance of using large switches (especially at the input stage, where errors are not noise-shaped) was under-estimated. Instead, the switch size was reduced to compensate for the circuit's sensitivity to CI errors, resulting from the small unit capacitor size of 0.1 pF. As a consequence, the final design uses switches ranging from 4 to 16 times the minimum size, depending on the load capacitance seen by the particular switch.

Reducing the switch size might seem unnecessary under the premise that the CI is perfectly cancelled by the use of transmission gates. However, as will be described next, the CI is only eliminated for one specific signal voltage level. Assume for example that the areas of the nMOS and pMOS within a transmission gate have been carefully sized such that there is perfect cancellation of injected holes and electrons for signal levels near 0 V. Now for positive signals, the PMOS will be the primary conductor and thus have more holes under its gate than the NMOS has electrons. Therefore when the transistors turn off, there will be an excess of holes and the sampling capacitor will store a slightly higher voltage than the ideal case. Conversely, for negative signals the sampling cap will store a lower voltage than the ideal case. If one adjusts the relative areas of the MOSFETs to fix the positive input signal case, one degrades the situation for the negative input case, and vice-versa.

Therefore, overcoming charge injection effects through the use of composite switches is not a simple task and not always entirely effective. Although the use of transmission gates will cancel the majority of CI, we see it does have some shortcomings. It should be noted that the other major technique in existence, the use of dummy switches[17], might offer interesting alternatives for specific applications, but proved to be no better for the modulator

under design. In the next section, we investigate how the effects of CI can be lessened through an entirely different means, careful choice of clock phasing.

3.3.3 Clock Phasing

As discussed in Section 2.2.3, the conventional method of clocking a SC circuit is to use a simple two phase non-overlapping clock. This basic scheme, however, suffers from the fact that it leaves the circuit susceptible to signal-dependent charge injection. To overcome this problem, a more complicated clocking scheme[18], shown in Figure 3.17(a) can be used.

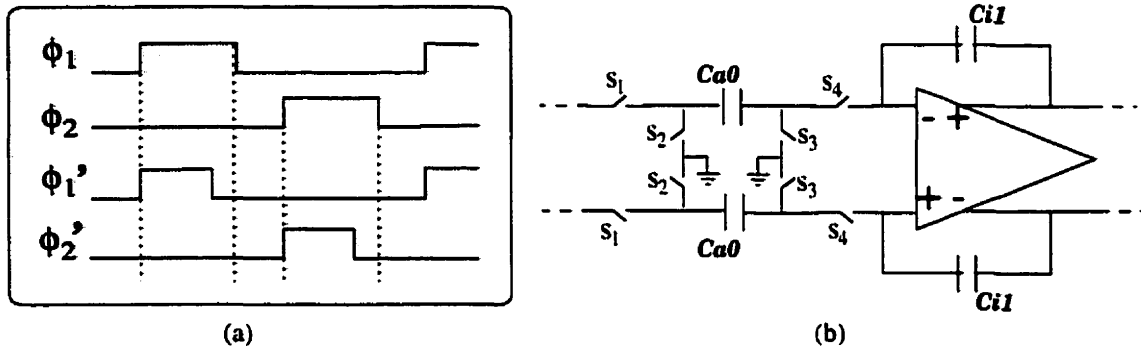


Figure 3.17: Four-Phase Clocking Scheme with Example Circuit

Referring to Figure 3.17(b), in this scheme the switch s_1 would still be controlled by ϕ_1, but s_3 would now be controlled by ϕ_1' not ϕ_1. Similarly, s_2 would be controlled by ϕ_2 and s_4 by ϕ_2'. Since when s_1 opens, s_3 is already open, the channel charge from s_1 that would normally be injected onto C_{k1}, is unable to settle onto the now floating capacitor. Therefore, no error voltage is produced by s_1, and similarly s_2. There is still however charge injected when s_3 (and s_4) open. However, unlike the charge from (s_1, s_2), the amount of this charge injected from (s_3,s_4) is not signal dependent. This is a direct consequence of the fact that both the drain and sources of these switches are always approximately at the analog ground level. Therefore, this CI is more acceptable, as it will not contain a signal dependency that would lead to harmonic distortion products.

The circuit used to produce the four phases is shown in Figure 3.18 which follows.

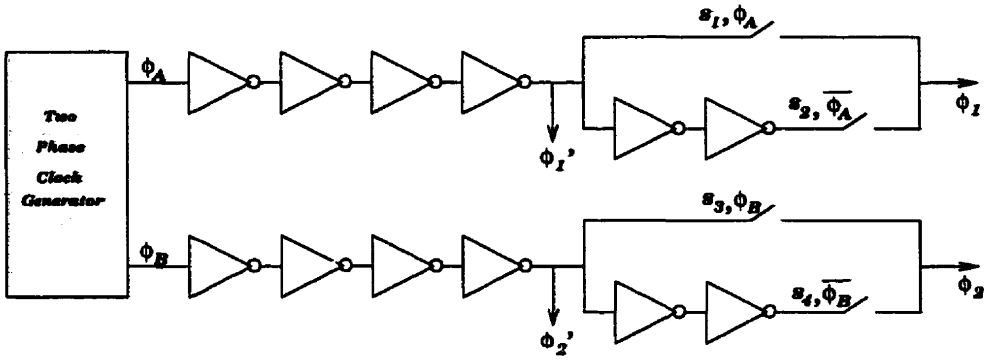


Figure 3.18: Digital Circuitry to Generate the Four Clock Phases

The two-phase clock generation circuit of Figure 2.18 on page 23 is first used to produce the non-overlapping phases, ϕ_A and ϕ_B. Next, we track how ϕ_A can be used to generate the control signals ϕ_1 and ϕ_1'. The controls ϕ_2 and ϕ_2' are produced by ϕ_B in a similar manner. The control signal ϕ_1' is simply a delayed version of ϕ_A. This delay allows the switches s_1 and s_2 to change state well before the leading edge ϕ_1'. Therefore, on a rising edge of ϕ_1', the top path controlled by s_1 will be already be conducting (ϕ_A high) and ϕ_1 will be identical to ϕ_1'. However, on a falling edge of ϕ_1', the bottom path will conduct (ϕ_A low) and ϕ_1 will be a delayed version on ϕ_1', producing the desired waveforms of Figure 3.17(a).

3.3.4 Amplifier and Comparator Circuits

The amplifier used to implement the modulator is the same as that used in the second-order lowpass design of Chapter 2, and was discussed therein. The one bit quantizer seen in was implemented using an amplifier in the open loop configuration followed by inverters to boost the gain and a flip-flop to latch the output. Although the approach is a relatively simple one, through HSPICE simulations which follow, it was not found to be a limiting factor in the overall performance. Therefore, alternative comparator designs were not pursued further.

3.3.5 D/A Scheme

The 1 bit D/A was achieved simply by switching in a positive or negative reference voltage, from an externally filtered voltage supply, depending on the comparator output. This can

be seen in Figure 3.19 which depicts the entire SC circuit. A single-bit DAC is inherently linear, and thus no elaborate circuit techniques were required in its implementation. Furthermore, since the DAC output will be sampled by the discrete-time SC circuit, a return-to-zero code is not necessary, as inter-symbol interference will not be an issue.

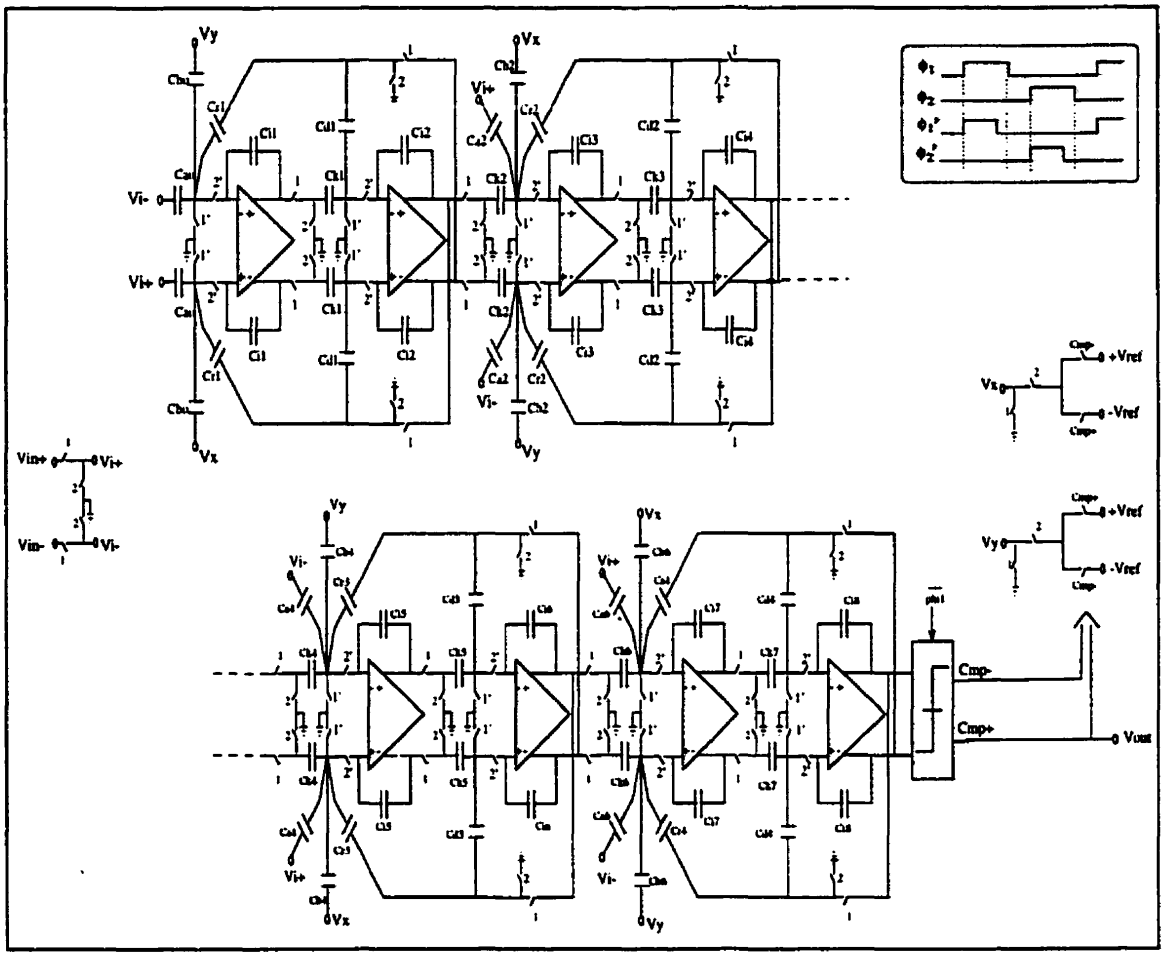


Figure 3.19: Complete Switched-Capacitor Circuit Implementation

3.4 Layout Considerations

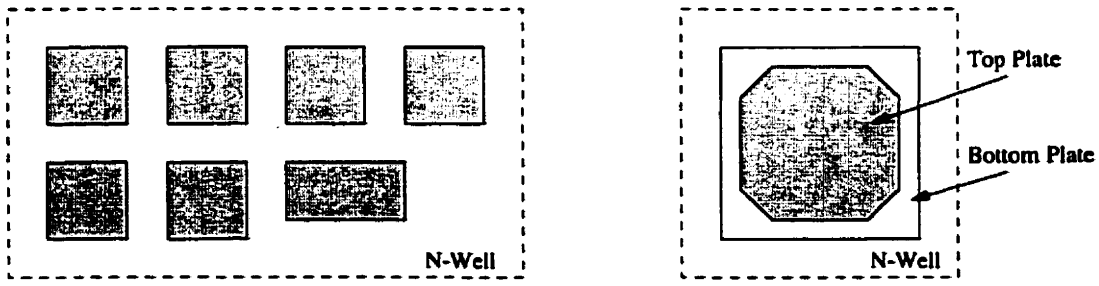
This is the final step in the design process and must be conducted very carefully if performance is not to be degraded. The main issues that must be taken into consideration will now be discussed.

3.4.1 The Capacitor Array

As the structure coefficients are formed by capacitor ratios, this is a very crucial part of the layout. The factors involved are as follows.

(i) Matching Concerns

As etching errors are inversely proportional to capacitor perimeter, to obtain the best capacitor accuracy, it is necessary to have as large an area-to-perimeter (A/P) ratio as possible. Moreover, all capacitors that are to be matched should have equal A/P ratios to achieve first-order cancellation of the etching errors. As a consequence, large capacitors must be composed of smaller unit elements connected in parallel so as to maintain a constant A/P ratio. It is also useful to make the *smallest* capacitor in the array in the shape of a square. Since the smallest capacitor will have a tendency to have the lowest A/P ratio, making it square will maximize the minimum A/P ratio. Since all capacitors will now be made with this unit element, this is the best way to maximize the A/P ratio over the entire array. Where the large capacitor is not a multiple of unit sized ones, the non-integer part was made using a rectangular section with the same A/P ratio, as shown in Figure 3.20(a).



(a) large capacitor composed of unit cells (b) unit capacitor

Figure 3.20: Basic Capacitor Layout

In order to obtain the best matching possible, capacitors from each section of the design were grouped together on the IC. In addition the capacitors from the positive half of the circuit were closely matched to their differential counterparts by interleaving them where possible. Note that a common-centroid geometry was not used as it was found that it introduced unacceptable routing parasitics which could change the absolute value of the small capacitors by up to 1%.

Dummy capacitors, not electrically connected to the circuit, were used to surround the array. This ensures that the environment of capacitors on the edge of the array will be no different than those in its interior. Therefore, the etching error, which depends heavily on what surrounds a capacitor, will be more uniform across the array and more effectively cancelled.

The entire array was next placed in a large Nwell biased to a quiet voltage, analog ground. This well isolates the capacitor array from any stray charge in the substrate that might migrate into the signal path through the bottom plate parasitics. Conversely, it prevents the signal dependent charge in the capacitor array from affecting the rest of the circuit through what would otherwise be a shared substrate.

(ii) Obtaining the Precise Capacitor Value

The coefficients in the design must be quite accurate. In addition, the capacitor values obtained from the loading optimization of Section 3.3.1 are quite small. Since the minimum grid snapping for the BiCMOS process in use is only 0.1μ, it becomes very difficult to obtain the desired capacitor value.

To increase the matching accuracy, the capacitors were not made as perfect squares or rectangles, instead 45 degree corners were used as shown in Figure 3.20(b). This approach has two distinct advantages. Firstly, this minimizes the fringing fields that would be present with 90 degree corners, and thus the capacitor value will be more predictable. Secondly, by varying each of these new smaller edges independently, it is possible to fine-tune the capacitor to the correct absolute value in the cases where non-unit elements are required. However, this process is quite involved, especially considering that the one must also keep

the A/P ratio within a reasonable limit of the average capacitor in the array. Therefore Matlab code was written that determines the shape which gives the most accurate capacitor values, while keeping the A/P ratio within 5% of the average.

3.4.2 Overall Floorplan

The floorplan must be designed with care, as this is a mixed analog-digital chip. Figure 3.21 is a simplified view of the complete layout that revels the floorplanning strategy used.

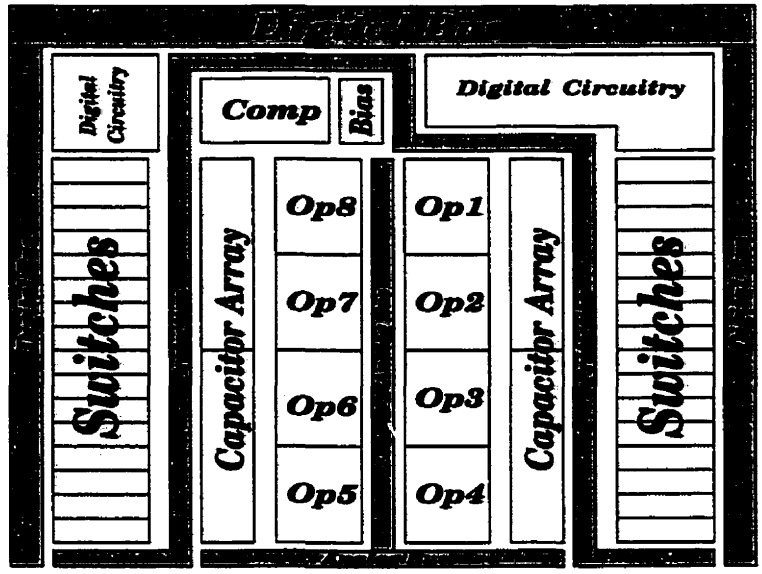


Figure 3.21: Overall Floorplan of the Layout

The most obvious feature is that the overall layout was carefully planned to make efficient use of silicon area. More importantly, it was designed so that it is never necessary to have an analog line cross over a digital line which carries a varying voltage. This avoids introducing harmful parasitics formed that could couple charge into the analog circuit.

The analog circuitry resides in the middle of the chip surrounded by a ring that protects these sensitive components from the digital circuitry. The protection is used to prevent any free charge carriers from the noisy digital substrate from migrating to the analog interior. This is achieved by biasing the substrate to negative analog supply and including an N-well biased to the positive supply, in order to capture the stray holes and electrons respectively.

In addition, the analog and digital circuitry uses separate power supplies which will be electrically de-coupled off-chip using π-filters.

Finally, all metal interconnect lines were sized wide enough such that the maximum current density limits [20] were respected.

3.5 Design Verification

This section discusses the test strategy used throughout the design process. At each stage of the design, appropriate simulations and tests were conducted to ensure the proper operation of the circuit. In the following, a chronological list of the various tests and simulations conducted will be given and briefly discussed.

3.5.1 SFG level verification

After the coefficients in the DSP-level structure were determined and dynamic-range scaled, the circuit was built in Matlab's Simulink and simulated. First, the basic operation of the circuit was verified. The points in the output digital bitstream were recorded for post-processing using Matlab. Figure 3.22 illustrates the results of a 16384-point FFT where the NTF zeros are clearly visible in the signal band.

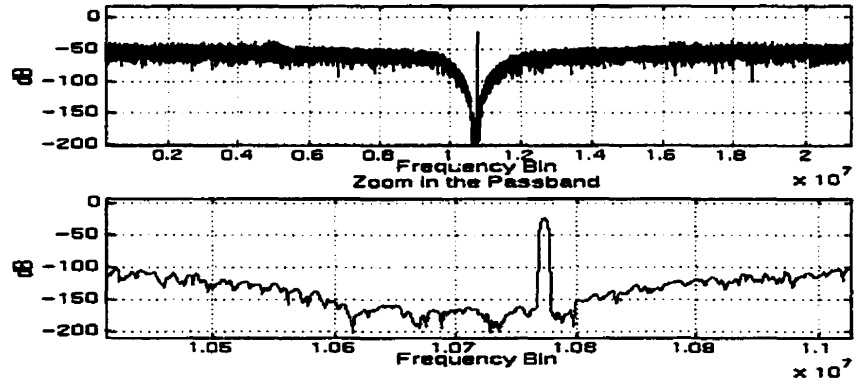


Figure 3.22: Spectrum of Modulator's Output, Simulated using Simulink

As the theory governing the stability of ΔΣ modulators (especially those of high order) is incomplete, this relatively fast simulator provides an attractive alternative to verify stability, at least in the short term. This was achieved by conducting lengthy simulations and

monitoring the signal levels at the outputs of the integrator outputs. If these signals remained bounded at their expected levels (stipulated during the dynamic-range scaling procedure), it would bode well towards, though not guarantee, a stable circuit. After a week-long simulation of the SFG-level structure on a SPARC-20 machine, the internal signals remained bounded at their predicted values, thereby increasing confidence in the design.

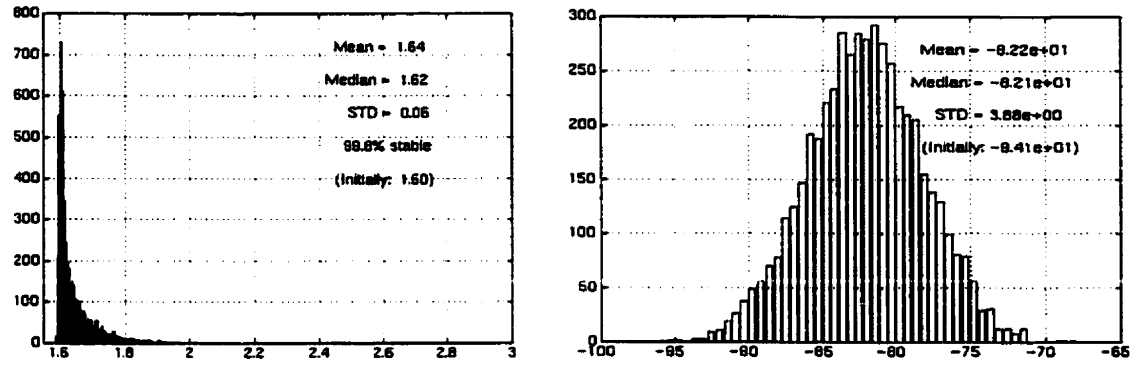
3.5.2 Performance Under Process Variation

This stage of verification was carried out in Matlab on the SFG-level representation of the circuit shown in Figure 3.13 on page 40. A script was written to alter the structure coefficients (which directly represent capacitor ratios) in a random manner, employing an independent uniform distribution for each. The reason a uniform random variable was used (as opposed to a Gaussian, for example) has to do with the nature of process variations. Provided careful, and barring a manufacturing disaster, the possible degree of inaccuracy in the ratio of two capacitors will be bounded to some percentage, known *a priori*. Therefore, it is logical to restrict the degree of variation in the random variables that represent the coefficients, making the uniform random variable a suitable choice.

The percent change in the coefficients should be representative of the expected capacitor matching (typically 0.1% - 1%). Therefore, a uniform random vector, 5000 elements long with this spread was used to represent each coefficient.The Matlab code was then executed, evaluating the noise and signal transfer functions for each of the 5000 sets of coefficients. The parameters that were focused on included NTF bound and location of poles to determine stability; relative noise floor to estimate resolution; and finally delay distortion, passband ripple and gain deviation to monitor linearity. A histogram of each of the results was then produced and analyzed.

For example, the histogram in Figure 3.23(a), along with the location of the poles, was used to give a reasonable prediction about stability. The resulting distribution of the NTF bound under 0.5% maximum coefficient change shows that 99.8% of the coefficient sets resulted in an NTF bound less than two. According to Lee's rule of thumb[14],this indicates a stable modulator. To confirm this approach, lengthy Simulink simulations using some of the ran-

domly generated coefficients were performed to verify stability or instability claims. The results were consistent with those of the NTF bound approach.



(a) NTF Bound Distribution (b) Relative Noise-Floor Distribution

Figure 3.23: Performance Under Process Variation

The relative noise floor was also observed to indicate the drop in performance due to process variation and is shown below in Figure 3.23(b) where it can be seen that its mean is now -82 dB, instead of the -94dB it was before process variation.

Similar histograms were obtained for the passband ripple, passband gain deviation, average relative delay distortion, and maximum relative delay distortion. The results of all these histograms confirmed that the structure would perform quite well under process variations and that a redesign of the structure was not necessary. Proceeding with the design process, the structure was mapped to its SC implementation where the next step of verification was performed.

3.5.3 Simulating the structure using SWITCAP2

Thus far, the tests and simulations were being carried out on a mathematical model of the circuit. Now, near ideal electrical components are introduced. SWITCAP2 allows testing of the SC topology to ensure the correct clock phasing, switch-sharing, and mapping from the SFG-level design. The circuit was run long enough such that 65536 (2^{16}) output data points, one per clock cycle, could be collected for FFT analysis. The results are displayed

in Figure 3.24, which has an effective resolution of 653 Hz/bin. The figure shows both the full Nyquist interval and a zoom around the signal band.

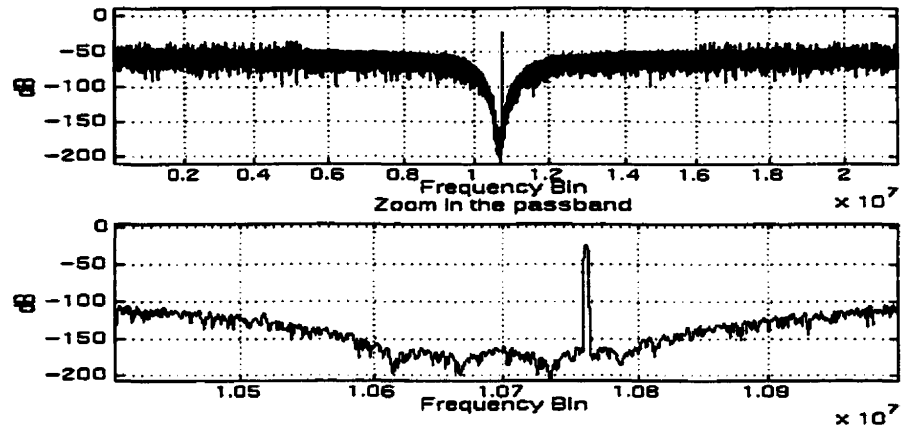


Figure 3.24: Spectrum of the Modulator Output, Simulated with SWITCAP2

The distinct noise-shaping behavior, including zeros visible in the passband, clearly indicate that the modulator is functioning correctly. The SNR, with noise integrated over the 200 kHz signal band was calculated to be 110 dB, equivalent to approximately 18 bits of resolution. Upon successful completion of Switcap2 simulations, it was possible to proceed with a circuit description that is closer to the transistor level.

3.5.4 Using HSPICE to Simulate the Circuit

As simulating transistor-level mixed-signal circuits is extremely time consuming, the digital circuitry was described using behavioral models wherever possible. Despite this, simulations are still problematic because in these sampled data circuits, simple AC analyses can not be used and more lengthy transient analyses are required. This is because on each clock phase, the SC circuit topology changes dramatically, as some switches become open circuits and others short. Therefore, no single operating point is the correct one about which to linearize the circuit for AC analysis. Therefore, a transient analysis must be performed for enough clock periods (typically in the order of 10000) so that a reasonable FFT can be computed on the pulse density modulated (PDM) output.

Adding to the simulation problem is the high order of this particular modulator, which means that for all practical purposes, a full transistor-level simulation is not feasible. For

this reason, idealized HSPICE elements were used whenever possible. The first step in importing the design into HSPICE was to obtain a working version of the circuit employing idealized switches (voltage controlled resistors), ideal amplifiers (VCVS's), an ideal latched comparator, and the actual values of the capacitors. The clock phases were generated using PULSE statements. Once this was accomplished, the comparator was replaced by a real amplifier in the open loop configuration followed by a D-type flip-flop (to implement the latching behavior of the comparator), both at the transistor level.

The simulation results are shown in Figure 3.25. It is no longer possible to see the notches in the passband because they are now being covered by noise resulting from the non-ideal implementation. However, the performance is still excellent and shows that using the proposed comparator setup will still give quality results.

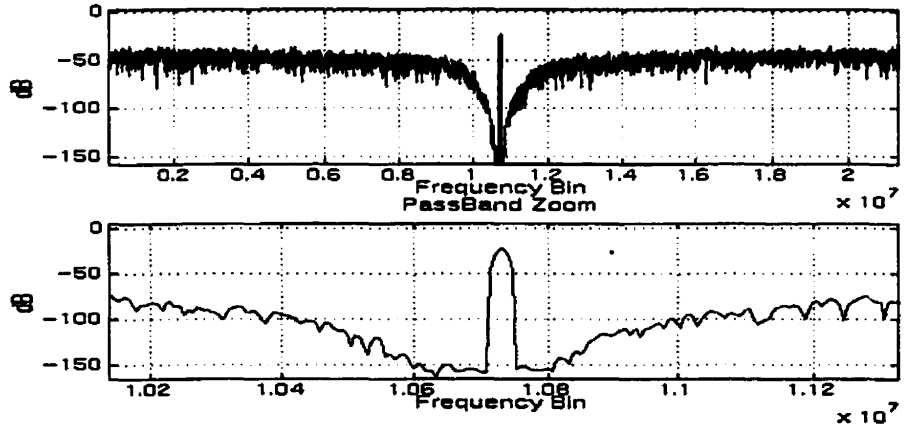


Figure 3.25: Spectrum of Modulator's output obtained from HSPICE simulation with everything ideal except the comparator

Following the addition of the real comparator, the ideal switches were replaced by transistor-level transmission gates. This of course made the simulation run much slower. After several design attempts where switches of different sizes were tried, a set of switches with the best performance was selected. Models capturing the important characteristics of the amplifier were then used instead of the ideal amplifiers as transistor-level amplifiers would have made the simulation prohibitively long. The trade-off, of course, is that the simulation accuracy has been compromised.

An alternative approach which was also used, is to keep all second-order sections ideal except for one. This one section could be represented with certain more realistic components. This approach allows one to judge the effect of multiple transistor-level components at the same time (for a given section) on the performance as one is still able to obtain a PDM output within a reasonable time frame. It is most insightful to implement the first section using transistor-level components, since errors from subsequent sections would be noise-shaped yielding an overly optimistic estimate of the circuit performance. However, each remaining section would still need to be separately replaced by a more realistic implementation to confirm that the transistor-level components can handle the different loading conditions of each section.

After extensively simulating the circuit, incorporating a mix of ideal, model and transistor level components, the circuit layout was performed.

3.5.5 Verifying the Circuit's Layout

An HSPICE netlist of the modulator including parasitic capacitances was obtained from the layout using the extraction tool provided with the CADENCE software. HSPICE was used to simulate the layout of the entire circuit in the time domain. It would take an excessively long time to obtain enough points for any FFT or SNR calculations. It was possible, however, to simulate long enough to recognize that the output waveform was indeed a PDM bitstream. This indicates that the layout was performed correctly, all components are powered up, and that no floating nodes exist.

In summary, we have seen that the actual behavior of the entire circuit with real components could not be completely obtained through simulation. This further justifies the need for fabrication of the ΔΣ modulator, as hardware testing is the only remaining option. The extensive simulations that were conducted, however, provide confidence in the success of the manufactured prototype.

3.6 Experimental Results

The IC was fabricated using a 0.8μ BiCMOS process. The chip, whose photomicrograph is shown in Figure 3.26, occupies and active area of 1.7mm x 1.7mm. The layout of the components directly follows the basic floorplan of Figure 3.21 on page 55, discussed previously in Section 3.4.

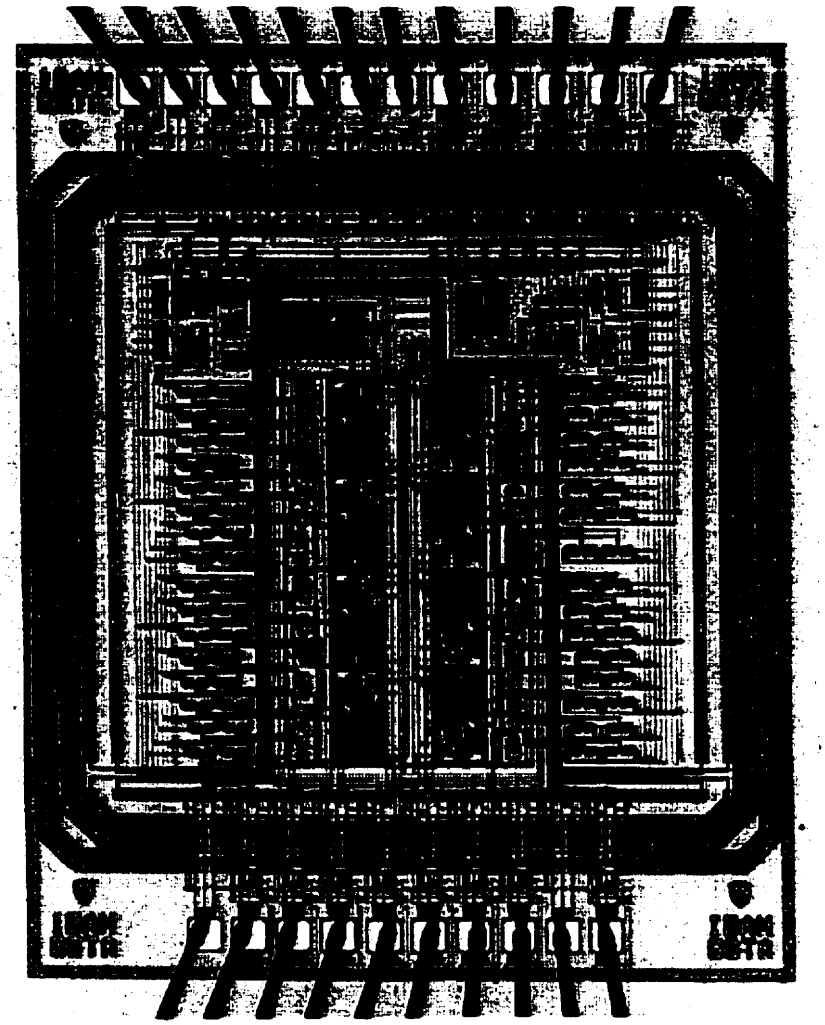


Figure 3.26: Die Micrograph of the 8th-order Bandpass Delta-Sigma Modulator

This section begins with an illustration of the environment and methods used to test the fabricated IC. The experimental performance of the design under various operating conditions will then be presented. Next, the summarized results will be evaluated with reference to, and shown to be comparable to, the current state-of-the-art in bandpass ΔΣ modulation. Fi-

nally, we will discuss some of the issues that would need to be addressed in order to further improve the modulator performance.

3.6.1 The Test Environment

After verifying the basic operation of the chip through a simple wire-wrap board, a cleaner, 2-layer PCB was constructed. The first step in its development involved producing a board layout using Cadence's Allegro software. The primary concerns in this step were ensuring a large ground plane and complete separation of analog lines from digital signals. In addition, π-filters, placed close to the chip, were used on all supply voltages. As described in [23] this is essential to minimize the noise that is coupled into the circuit. Once the board layout had been completed, high-quality transparencies, one for each board layer, were obtained using the Allegro output files. These were then used in a multi-step photochemical process to produce the boards shown in Figure 3.27.

Figure 3.27: Top View of PCB Boards

Two boards are shown because the modulator was also used as a component in a CODEC design developed at McGill University. The board on the left in Figure 3.27 was used to test the design in the system, while the board on the right was used solely to test the ΔΣ modulator itself.

The test setup that was used is shown in Figure 3.28. As seen in the diagram, the circuit was powered by +/- 2.5 volt supplies and external voltage references were used to realize the 1-bit D/A in the modulator feedback. The circuit was then clocked with an external generator and excited with a sinusoidal input.

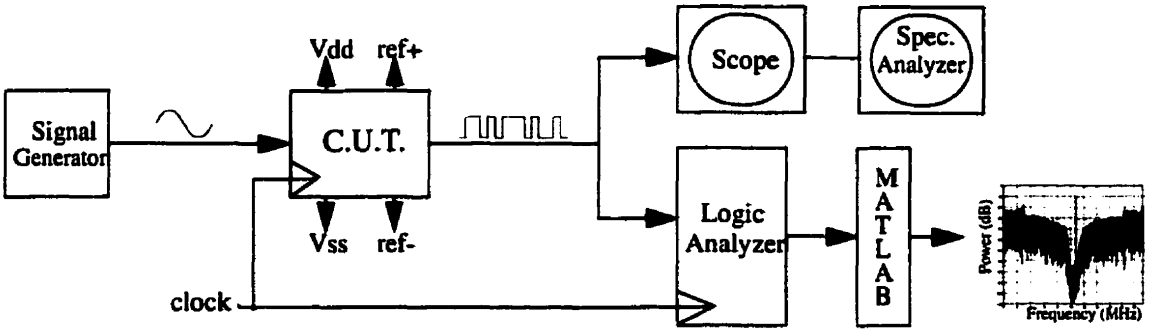


Figure 3.28: Experimental Setup used to Test the Modulator

The pulse density modulated output bitstream was then examined in two ways. The first consisted of using a conventional oscilloscope and an analog spectrum analyzer for diagnosing and debugging the circuit. The physical setup during this procedure is shown in Figure 3.29.

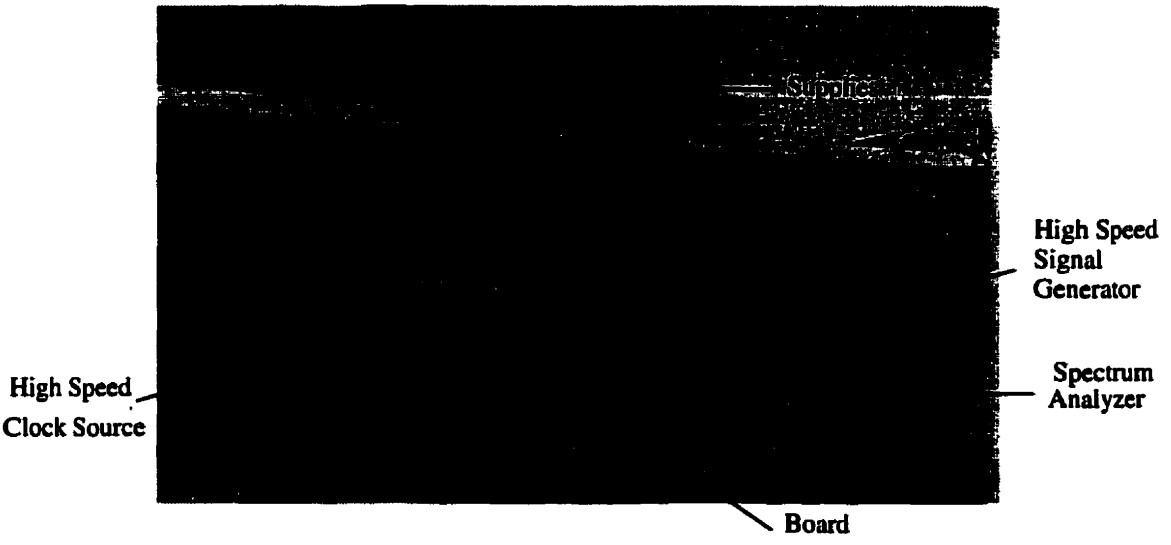


Figure 3.29: Physical Setup used in Diagnosing the Circuit

An alternative technique that was used to view the output spectrum was to capture the output time domain PDM digitally using a logic analyzer. By externally clocking the logic analyzer with the same clock that feeds the modulator, one can ensure that the data points are synchronously captured, one per clock cycle. Capturing the data digitally has the advantage that analog effects such as inter-symbol interference, and external noise coupling will not

be captured with the impulse sampling and therefore will not mask the true performance of the modulator. The data points were then transferred to a workstation for post-processing. Matlab was used to compute the FFT, and obtain values for performance metrics such as SNR. To obtain maximum information and accuracy from the FFT, the signal frequency was carefully chosen to ensure coherent sampling, as discussed in [72].

Another, more obvious difference between the FFT produced by Matlab and the spectrum analyzer trace is that, due to impulse sampling at the logic analyzer, the FFT spectrum will not experience a sin(x)/ x effect. This sinc(x) effect would be visible on the analog spectrum analyzer and could be misleading as this phenomenon would not occur in practice, as any further processing of the bitstream would be performed in the digital domain via impulse sampling.

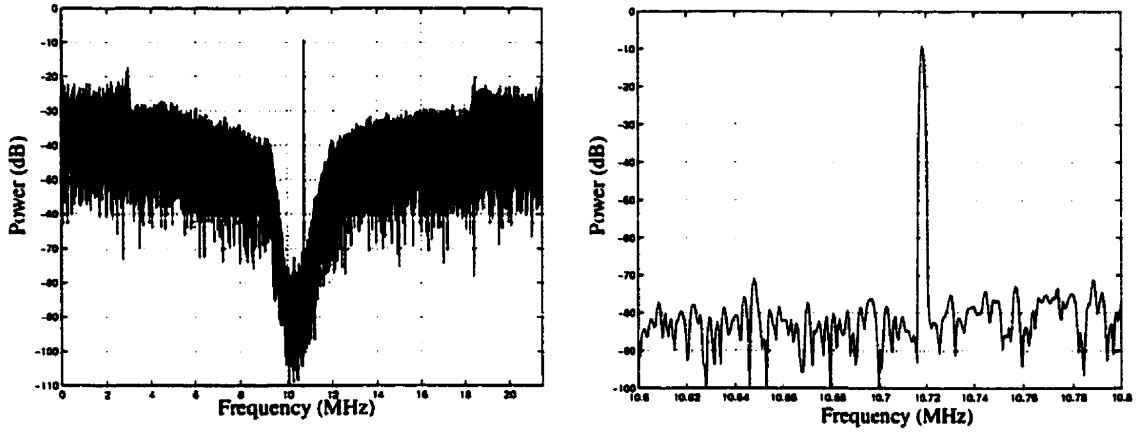
3.6.2 Experimental Performance

The modulator has been designed to operate on signals within a 200 kHz band, centered at an IF of 10.7 MHz. Under normal operating conditions, the IF band is centered at $f_S/4$, f_S being the clocking frequency, and the circuit is clocked at 42.8 MHz. However, as mentioned previously, it is sometimes advantageous to operate the modulator with the IF band centered at $3f_S/4$ by clocking at a lower rate of 14.3 MHz, in order to ease power and decimation requirements. The experimental performance under both of these operating conditions will be discussed next.

(i) IF band Centred at $F_S/4$

In this mode of operation, the chip is clocked at 42.8 MHz and consumes 227 mW of power. The experimental results seen in Figure 3.30 were obtained by conducting a 65536-point FFT (corresponding to a resolution of 653 Hz/bin) on the output PDM bitsream and demonstrate that the modulator is functioning correctly. Analysis of the FFT data reveals that the modulator achieves a signal-to-noise ratio of 52 dB over the originally specified band, shown in Figure 3.30(b). Close inspection of signal band zoom reveals the third harmonic of the input signal aliased back into the signal band at 10.65 MHz. After close observation,

the 5th harmonic is also visible at approximately 10.79 MHz, as expected. These tones limit the spurious-free dynamic range (SFDR) at approximately 62 dB, for input levels corresponding to peak SNR.



(a) Nyquist Band (b) Signal Band

Figure 3.30: Output spectra when clocked at 42.8 MHz

Closer inspection of the Nyquist band plot of Figure 3.30(a) reveals that the signal band is slightly shifted in frequency. That is, it is not exactly centered about 10.7 MHz, 1/4 of the 42.8 MHz clock frequency. Nevertheless, the design still achieves very respectable results. This is due to the fact that the 10.7 MHz tone is near the edge of a band that extends far beyond the 200 kHz it was originally designed for. In fact the band is actually centered at 10.5 MHz, and has a width of approximately 800 kHz-1 MHz. The extra bandwidth is a result of the noise floor being above the theoretical -130 dB/Hz, for which the 200 kHz bandwidth was designed. Of course, at higher levels of noise, an extension of the original bandwidth is expected.

The frequency shift can be attributed to magnitude and phase errors in the integrator building blocks. These are a result of incomplete settling at high frequencies and coefficient mismatch errors. A similar problem was reported in [7] which used the same integrator structure and amplifier in a 2nd-order bandpass ΔΣ modulator.

The band can be re-centered about the IF of 10.7 MHz if the modulator is calibrated by adjusting the clock frequency. This is reasonable provided the modulator does not share the same clock with a surrounding system, whose clock frequency can not change. When the

clock is increased to 44.8 MHz, the band centered around 10.7 MHz, attains a width of approx 800 kHz without increasing the noise floor. This can be seen below in Figure 3.31, which is the result of a 65536-point FFT.

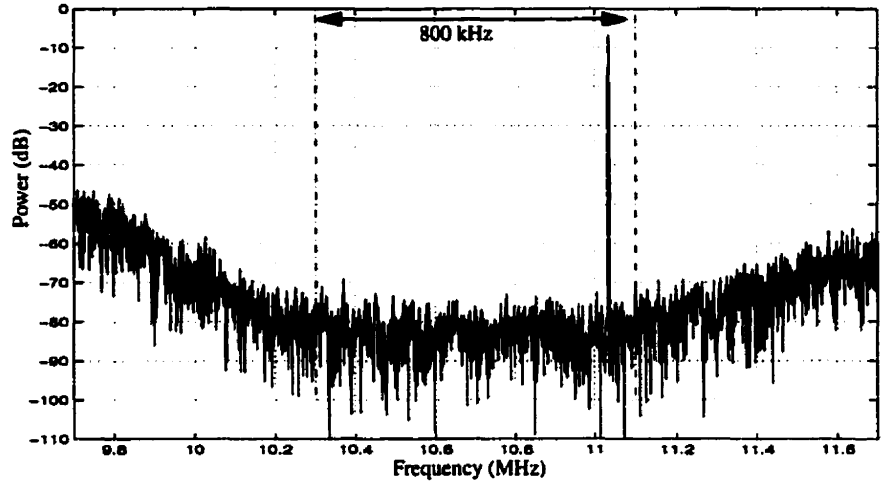


Figure 3.31: IF band when clocked at 44.8 MHz

To determine the useful range of operation of the modulator, the input signal was varied in amplitude and the output signal-to-noise ratio measured with and without the harmonic distortion components included. The results of this test are shown in Figure 3.32, where full scale corresponds to the reference feedback level. The dynamic range, defined as the range of inputs resulting in a positive SNR, can be seen to be approximately 58 dB.

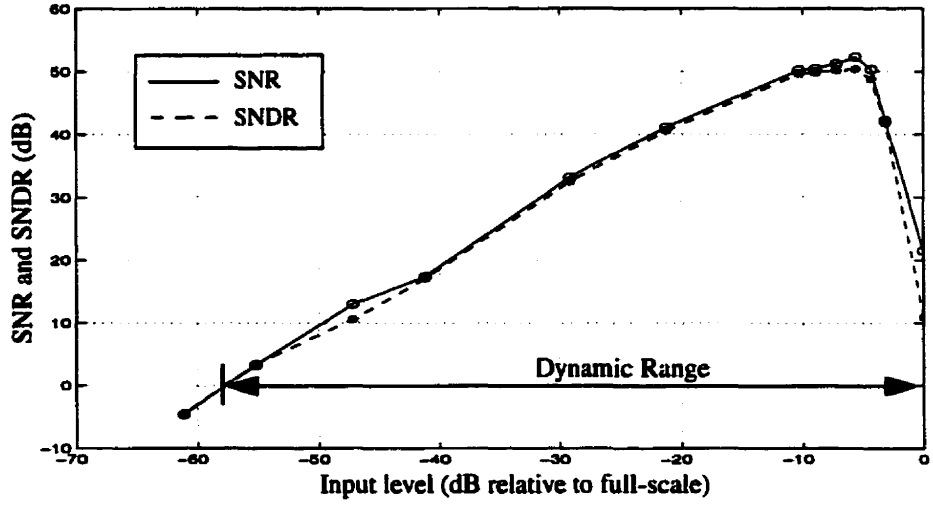
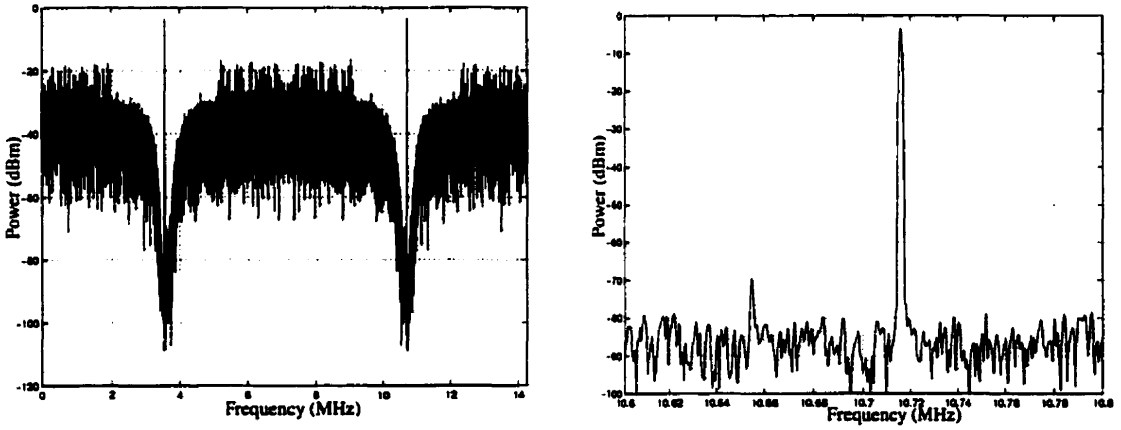


Figure 3.32: SNR and SNDR as a function of input level

(ii) IF Band Centred at 3Fs/4

Next, we consider the modulator performance when clocked three times lower in speed, at 14.3 MHz. The signal band is still centered about the originally specified 10.7 MHz, which is now at 3/4 the clock frequency, f_S. However, because the inherent sample-and-hold at the input stage of the SC circuit, the $3f_S/4$ band is immediately aliased to $f_S/4$ and the signal processing is no different than in the previous case.

In this mode of operation, the power consumption has been reduced from 227 mW in the previous case, to 157 mW. The PDM bitstream data points were collected and a 65536-point FFT computed. Figure 3.33 illustrates the results in the entire 0-f_S band, and the 200 kHz signal band.



(a) Entire 0-Fs Band (b) Signal Band Zoom

Figure 3.33: Output Spectra when clocking at 14.27 MHz

A drawback one might initially expect as a consequence of the lower clock rate is reduced OSR. While it is true that the OSR has dropped three-fold, due to the high-order of the modulator, one can still achieve excellent results. In fact, with the noise integrated over the 200 kHz signal band, the SNR was calculated to have a peak value of 59 dB. For this input amplitude, the SFDR is 66 dB, limited by the third harmonic which aliases back into the signal band. The dynamic range in this mode of operation was found to be 67 dB. These results are actually approximately 5-10 dB better than the previous $f_S/4$ case, due to the increased settling time.

Finally, due to the fact that in frequency aliasing the IF band has been mirrored about $f_S/2$, care must be taken when recovering the original signal. This can be easily taken care of digitally, when the signal is brought to base-band. Specifically, instead of down-converting the $f_S/4$ signal to baseband, as usually done in practice, the $-f_S/4$ signal, which has the correct orientation is up-converted via the complex exponential, e^(+j*2*pi*n*T*fs/4) which has the discrete values of 1,j,-1,-j, 1,... etc.

3.6.3 Performance Evaluation

Table 3.4 which follows summarizes the highlighted experimental performance of the modulator presented in this chapter.

Specification	Value
Modulator Design	8th-order Bandpass
Technology	0.8μ BiCMOS
Active Area	1.7mm x 1.7 mm
Power Consumption	157 mW
Clock Frequency	14.3 MHz
Signal Band	10.6 MHz - 10.8 MHz
peak SNR	59 dB
SFDR (@ peak SNR)	66 dB
Dynamic Range	67 dB

Table 3.4: Summary of Experimental Results

In Table 3.5 which follows, a chronological summary of previously reported fabricated bandpass (BP) ΔΣ modulators is provided. It is meant to outline the evolution of BP modulators over the last few years and to illustrate how the 8th-order modulator of this thesis compares to previously designs. The modulator achieves a dynamic range of 67 dB over a wide bandwidth of 200 kHz centered at 10.7 MHz. This is accomplished without having to resort to very high clocking rates, which would render decimation more difficult, and without requiring an expensive process. Overall, for the given technology and signal band frequency, the modulator demonstrates performance comparable to the current state-of-the-art while keeping power consumption within acceptable limits. Moreover, this is the first re-

ported working 8th-order BP modulator, and demonstrates that high-order, single-bit modulators can be made to be stable and are thus a viable means of meeting the stringent demands placed on present-day A/D converters.

Ref. # & year	DR (dB)	SNR (dB)	BW (kHz)	IF; f_{clk} (MHz)	Mod. Order	Power (mW)	Process
8th-order	67	59	200	10.7 ; 14.3	8	157	0.8 um BiCMOS
[25], 1997	75*	75*	200	20 ; 40	4, 2 path	72	0.3 um CMOS
[26], 1997	NA	92	366	55.5 ; 4000	2	1400	AlInAs/InGaAs HBT
[27], 1997	67	62	200	3.75 ; 10	4, complex	130	0.8 um BiCMOS
[28], 1996	84	NA	NA	5 ; 160	4	1000	0.8 um BiCMOS
[29], 1995	69	56	30	2 ; 8	4, 2 opamps	NA	2 um CMOS
[7], 1995	NA	57	200	10.7 ; 42.8	2	60	0.8 um BiCMOS
[12], 1993	NA	63	8	0.455; 1.82	4	210	3 um CMOS
[12], 1993	15 bits	75	30	1.8 ; 7.2	4	NA	1 um CMOS
[30], 1993	NA	55	200	6.5 ; 26	2	150	1.2 um BiCMOS

*: extrapolated, NA : Not Available

Table 3.5: Previously Reported Fabricated Bandpass ΔΣ Modulators

3.6.4 Performance Limitations

Although the modulator performance is very respectable, further refinement in the following areas could enhance the accuracy of a second generation design.

(i) OTA Design: Settling

Recall that when the chip is clocked at the lower rate of 14.3 MHz instead of 42.8 MHz, the performance improved by approximately 5-10 dB despite the reduced OSR. This clearly indicates that the quantization noise floor is not the limiting factor of the circuit performance. Rather, circuit implementation and specifically settling time is a significant factor. That is, when clocked at 14.3 MHz, the modulator amplifiers have more time to settle and

there is no longer any shift of the NTF band center. With the band correctly centered about the IF frequency, greater quantization noise suppression could be achieved. Next, we will see how the constraints imposed by the amplifiers have far wider reaching implications than settling itself.

(ii) Capacitor Sizing: kT/C Noise

As a consequence of the settling problems described above, the capacitors were forced to be as small as 0.1 pF. The resulting kT/C noise is not a limiting factor during $f_S/4$ operation (that is when clocked at 42.8 MHz) due to the higher OSR and more severe settling problems at these speeds. However, with the circuit clocked at 14.3 MHz for $3f_S/4$ operation, the lower estimate for the total inband noise power calculated using Eq. (3.14) from Section 3.3.1 is approximately -72 dB (relative to the reference signals). Therefore, the kT/C noise is likely to be contributing significantly to the experimentally observed level.

(iii) Switch Design: Harmonic Distortion

As discussed in Section 3.3.2, it is desirable to make the switches wide enough such that the time constants associated with their on resistance are negligible. However, the excessive charge injected from large switches leads to significant voltage errors when stored across the small capacitors used in the design. As previously mentioned, the switches were therefore decreased in size to the point where the time constants associated with their on resistance were in the same order as the time constants associated with the OTA settling.

Recall from Section 3.3.2, that this approach unfortunately leaves the circuit susceptible to harmonic distortion. This mechanism is thought to be responsible for the odd order distortion products (approx 60^+ dB below the signal) that were observed to be folding back into the signal band during experimentation.

(iv) Test Environment: Noise, Coupling

Clearly, to obtain performance in the range of 18 bits, one must have a test environment capable of producing and measuring high quality signals. Although external filters were

used on all circuit inputs and a two layer PCB was built to house the chip, the signal quality was still insufficient. For example, the external reference voltages were observed to contain noise at a level of approximately -115 dBm/Hz, which is in the range of that observed in the output PDM when examined on the spectrum analyzer. Finally, a random noise level of approximately 50 mV could be observed on the board ground plane, which is clearly unacceptable.

3.6.5 Recommendations for Improvement

A second spin of the design could benefit most from modifications made at the implementation level. To begin, one should take advantage of the newly available 0.35μ process to design an OTA with improved settling behavior. This will in turn allow the use of larger capacitors, thereby reducing the kT/C noise problem. Larger capacitors will also lessen the sensitivity to CI effects, allowing the use of bigger switches. Larger switches, especially at the input, will of course reduce the distortion. This latter adjustment should be made regardless of the CI problem, as CI should be adequately controlled with a four phase clocking scheme. Furthermore, when testing the fabricated IC, it is important to take precautions to avoid coupling problems as described in [24] including the use of a multi-layer board. In addition, the use of external supplies to provide the feedback voltages is not recommended, as on chip references could be used to provide cleaner DC levels. Finally, the high quality test stimuli required for the input signal could be produced using the ΔΣ modulated bitstream approach [73] and appropriate on chip filtering.

If above requirements can not be easily met, it might be wiser to design the modulator for a wider bandwidth instead of high resolution which becomes very difficult to test. A wide bandwidth can be useful in simultaneously converting multiple IF channels to digital form.

3.7 Conclusion

This chapter began with an introduction to the bandpass approach to delta-sigma modulation. It was shown that using a bandpass modulator can be beneficial in many applications that require processing of narrowband signals at high frequencies. The modulator is intended for use in an RF receiver, performing the analog-to-digital conversion on signals in the IF band which has numerous advantages. The detailed procedure that was used in designing a novel eighth-order bandpass modulator, intended for use in digital radio, was presented. The work began a mathematical transfer function level progressed to a complete SFG-level design. Next, issues involved in mapping the SFG structure onto a SC implementation, such as capacitor sizing, switch design and clock phasing were thoroughly investigated. This was followed by a examination of the issues that must be taken into account at the layout level, so as to not degrade the modulator performance. Having completed the discussion of the design process, verification strategy that was used throughout the design was brought to attention. Various simulations were conducted at each level of design, with promising results that warranted fabrication of a prototype modulator. Experimental investigations of the IC revealed that the modulator achieves approximately 11 bits of resolution over a 200 kHz bandwidth centered at 10.7 MHz. This performance was shown to be comparable to the current state-of-the art in bandpass ΔΣ modulation. Furthermore, insight was provided into how these results could be further improved through implementation refinements in a second generation design. This is the first reported fabricated 8^{th}-order BP modulator, and demonstrates that high-order, single-bit modulators can be made to be stable, and are a viable solution to meet the continuously increasing demands imposed on present-day A/D converters.

Chapter 4 : All-CMOS Data Conversion using ΔΣ Modulation

Thus far, we have investigated how delta-sigma modulation can be used to meet the industry demand for high-performance data conversion. The next issue that will be addressed is how to provide these solutions at low cost.

4.1 Introduction

As the vast majority of integrated circuits are digital in nature, fabrication processes have been tailored to optimize for digital electronics. Therefore, the most economical approach to producing data converters is to fabricate the entire design in a standard digital CMOS process. However, this excludes the possibility of having extra processing steps to provide linear capacitors or bipolar transistors for the precise analog components. The latter is no longer as major a concern, as high-gain stages can be made without the use of BJTs [31]. This work will therefore focus on the effect the lack of linear capacitors has on the data conversion systems of Figure 4.1.

Referring to Figure 4.1, the decimator, interpolator and ΔΣ modulator in the D/A case are all digital in nature and are thus easily implemented in a CMOS process. Next, the design constraints on the analog anti-aliasing filter are usually quite relaxed due to the high oversampling rate used in the ΔΣ modulator that follows. This continuous-time filter can thus be realized by a simple off-chip passive RC filter or alternatively on-chip, employing only

MOSFETs[31].The analog reconstruction filter, however, must remove quantization noise which can rise sharply just outside of the signal band, especially when a high-order ΔΣ modulator is used. Therefore, the reconstruction filter, along with the ΔΣ modulator in the A/D case are the components most affected by the lack of linear capacitors. To better understand the implications of using a purely digital CMOS, this chapter will study the implementation of these components without the use of linear capacitors.

(a) Analog-to-Digital Conversion

(b) Digital-to-Analog Conversion

Figure 4.1: Basic Elements of Data Conversion systems based on ΔΣ Modulation

These two components can be implemented using either continuous-time or sampled-data approaches. Typically, the ΔΣ modulator is implemented using sampled-data techniques, however continuous-time realizations, based on transformations of discrete-time structures, have recently been reported[33]. The reconstruction filter on the other hand, would generally be implemented using a continuous-time approach. Nevertheless, in certain applications, it can be advantageous to use a precise sampled-data filter in combination with a simple continuous-time filter, instead of using a solely continuous-time approach. Sampled-data filters have the advantage of higher precision, and greater robustness. Albeit, to produce a purely analog signal, they must be followed by a continuous-time filter to remove clock tones and image signals. Due to the high oversampling rates involved in the ΔΣ modulators, however, this last step is a relatively easy one. In many cases the lowpass filtering inherent in the stage following the reconstruction filter might be sufficient to suppress higher frequencies. This would definitely be the case for the voice/audio band application of this chapter, where the reconstruction filter would be followed by a speaker.

For the purposes of this thesis, the sampled-data approach is used for the investigations concerning both the ΔΣ modulator and reconstruction filter blocks. Specifically, two entirely different sampled-data circuit techniques, those of Switched-Capacitor (SC) and Switched-Current (SI), will be studied and used to implement each of the above two components.

The SC approach has already been used in previous chapters, where linear capacitors were available. Next, in Section 4.2, we will investigate how the SC approach can be used to implement the above mentioned reconstruction filter and ΔΣ modulator blocks, employing MOSFETs to realize the capacitors. In Section 4.3, the SI approach, which inherently does not require linear capacitors, will be introduced and used to implement the same two data-conversion components. The above investigations therefore involve the fabrication and experimentation of four prototype ICs. As such, this chapter will provide insight into the issues involved in the design and expected performance of an all-CMOS data conversion system that employs the ΔΣ modulation technique.

4.2 The Switched-Capacitor Approach

This section will begin with a background on the effects of using MOS transistors to implement the capacitors in a SC structure. Next, we will examine different SC topologies that can be used to overcome these effects. Once this ground work has been layed, we will examine the design and implementation results of two fabricated prototypes that use these techniques. As previously mentioned, the two designs are the key analog components in data conversion systems of Figure 4.1, namely the reconstruction filter for the D/A case and ΔΣ Modulator for the A/D scheme.

4.2.1 Using MOSFETS to Realize Capacitors

(i) Process Alternatives

The usual method of realizing linear capacitors for analog circuit functions involves adding additional processing steps to provide an extra layer of polysilicon. This allows the use of

polysilicon-to-polysilicon capacitors, which have both a high degree of linearity and a high capacitance-to-area ratio. In a purely digital CMOS process, however, these capacitors are not available. One alternative is to use metal1-to-poly or metal2-to-metal1 capacitors. Although these capacitors will have good linearity[36], they occupy an excessively large area and exhibit poor matching properties[34]. The other alternative is to make use of the gate-to-channel capacitance inherent in a MOSFET. Due to the thin gate-oxide which acts as a dielectric, they generally will also have a greater capacitance per unit area than even the poly-to-poly capacitors. Furthermore, due to the greater controllability of the gate oxide relative to the field oxide, this approach results in capacitors that are more accurately matched than the traditional poly-to-poly class[35][37], with relative mismatches as low as 0.02% having been reported[38]. The only drawback to using MOS transistors to implement the capacitors is that they exhibit a large voltage dependence, as will be discussed next.

(ii) MOS-Capacitor Voltage Dependence

To understand the origins of the MOSFET-capacitor voltage dependence, consider the basic N-type MOS structure shown in Figure 4.2(a). This two-terminal device consists of a thin dielectric sandwiched between a metallic plate and a silicon substrate. Adjacent to the basic MOS-capacitor is a sample block charge diagram for the device [16]. This diagram will serve as a useful visualization aid by providing information concerning the approximate charge distribution within the MOS structure.

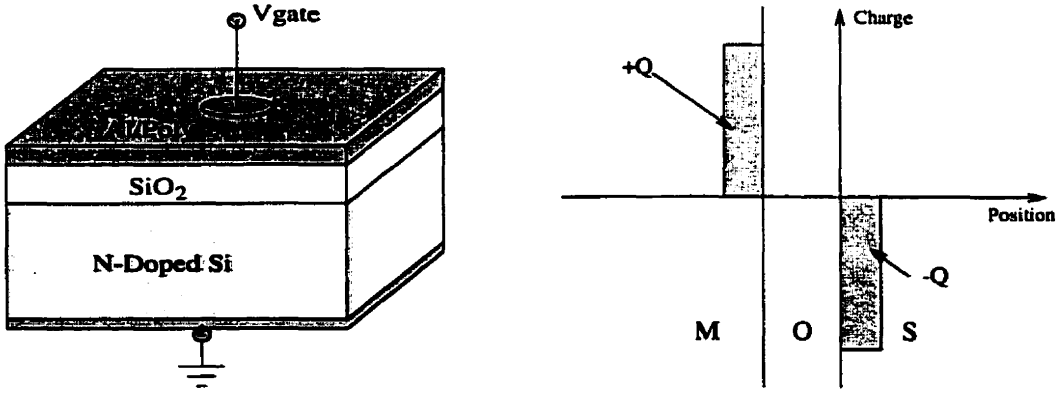


Figure 4.2: (a) Basic MOS Capacitor and (b) Sample Block Charge Diagram

When there is no applied gate voltage, equilibrium conditions prevail and there will be no charge within the device. Figure 4.2(b) depicts the distribution in the case where a positive DC voltage is applied at the gate, resulting in an accumulation of charge at the metal-oxide interface. Note that in order to satisfy Gauss' law, an equal amount of negative charge must accumulate in the semiconductor.

Next, to determine the capacitance of the MOS-C under different DC biasing conditions, we examine the effect an AC fluctuation in the gate voltage has on each DC charge distribution [16].

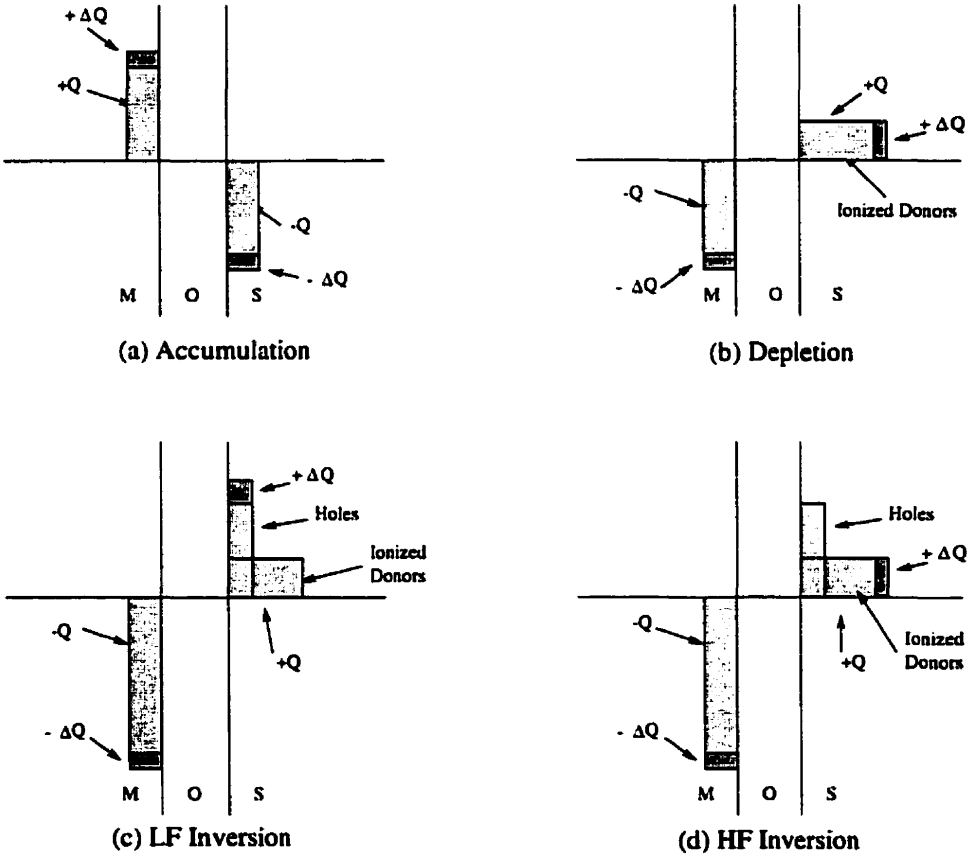


Figure 4.3: Charge Fluctuations within a MOS-C structure subject to an AC gate voltage, under four different DC bias conditions

Figure 4.3(a) illustrates the case when the MOS-C is biased in its accumulation region. That is, a positive gate voltage is applied and majority carriers within the semiconductor (electrons for the N-type semiconductor under investigation) *accumulate* at the oxide inter-

face. As this gate voltage is varied about its DC bias, there will be a corresponding fluctuation in charge distribution as shown in Figure 4.3a. This behavior is much like that of a parallel plate capacitor, with capacitance given by Eq. (4.1), where A_G and x_o represent the gate area and oxide thickness respectively.

$$C_o = \frac{k_o \varepsilon_o A_G}{x_o} \tag{4.1}$$

Next, Figure 4.3(b) illustrates the case when the MOS-C is biased in its depletion region. A small negative gate voltage ($|V_G| < |V_T|$) is applied which, conceptually, repels the electrons away from the oxide. This *depletion* of majority carriers (electrons) leaves their positively charged donor sites exposed. As the gate voltage is varied, there will be a fluctuation in the width of this depletion region, with charge distributions as depicted in Figure 4.3b. The total capacitance can be represented by the oxide capacitance, C_O, in series with a semiconductor capacitance, given by Eq. (4.2)

$$C_S = \frac{k_s \varepsilon_s A_G}{W} \tag{4.2}$$

As the DC gate voltage becomes more negative, the width of the depletion region, W, increases, decreasing the overall capacitance.

Figures 4.3c and 4.3d illustrate the case when the MOS-C is biased in its inversion region. In this case, a large negative gate voltage ($|V_G| > |V_T|$) is applied, which *inverts* the semiconductor at the oxide interface from N-type to P-type. In this situation, once the depletion region reaches its maximum width, W_T, the additional positive charge required to maintain conservation originates from newly available extra holes, not ionized donors.

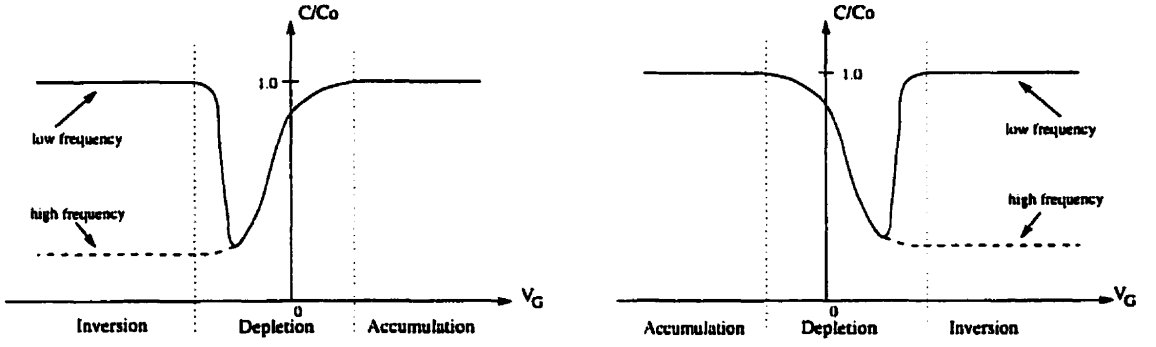
Now, when a low-frequency AC signal is superimposed on the DC gate bias, the resulting charge fluctuations will be as shown in Figure 4.3(c). The charge variation in the semiconductor is due to the generation/recombination of minority carriers (holes), at the oxide interface. The capacitance under these conditions can thus be simply expressed by Eq. (4.1). Alternatively, if a high frequency (typically > 10 Hz [16]) signal is applied at the gate, the minority carrier variations can not follow, so the charge variation will stem from the majority carrier effect (modulation of the depletion region width) as seen in Figure 4.3(d). In

this case, the total capacitance can be described as a series combination of C_S and C_O, as seen in Eq. (4.3).

$$C_T = \frac{C_S C_O}{C_S + C_O} \tag{4.3}$$

This situation is similar to the depletion case, except that here, the depletion region width has reached its maximum value, W_T, and will not change with varying DC voltage. Therefore, the capacitance will remain constant.

Combining the analysis from each of these four situations together results in the approximate capacitance-voltage characteristics shown in Figure 4.4. A typical plot for both the N-type MOS-C discussed above, and the complimentary P-type MOS-C are shown.



(a) N-Type MOS-C (b) P-Type MOS-C

Figure 4.4: Capacitance-Voltage Characteristics of N-type and P-type MOS-Cs

(iii) MOS-Capacitor Implementation

Now that the basic MOS-C structure is well understood, we will examine how the more practical MOSFET device can realize a capacitor, and the C-V characteristic associated with it.

As discussed in [40], there exists many ways in which a capacitor can be realized in a single-well process. The most practical techniques are those where the capacitor is isolated in its own well. In this case, neither terminal is forced to be connected to a supply voltage, and a floating capacitor is possible. The MOSFET-capacitor structure that was used in the single n-well process available is shown in Figure 4.5.

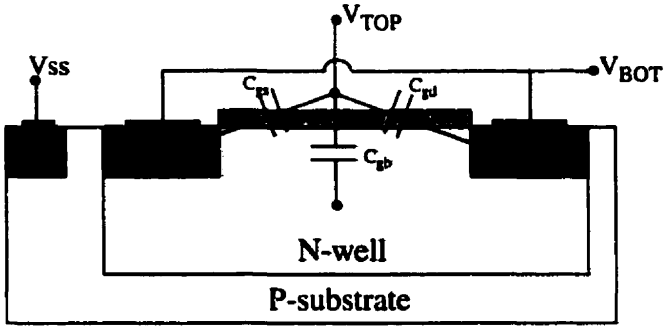


Figure 4.5: P-MOSFET Structure used for Capacitor Implementation

It consists of a basic PMOS transistor whose gate forms the capacitor top plate and whose body, drain and source are connected together to form the bottom plate. For any given DC bias, the total capacitance seen between these two plates is given by:

$$C_T = C_{gs} + C_{gd} + C_{gb} \tag{4.4}$$

The gate-body capacitance component, C_{gb}, behaves in the same manner as the basic MOS-C structure of the previous section. The linear overlap capacitances present in a actual device appear in parallel with C_{gs} and C_{gd}. When biased in inversion, C_{gb} will take on the high-frequency characteristic of Figure 4.4(a), as any frequencies below 10 Hz are not relevant for the audio-band applications discussed here.

For negative DC biases ($V_{TOP} < V_{BOT}$), the PMOS is in its strong inversion region. In this case the total capacitance is dominated by a capacitor whose top plate is formed by the gate poly and bottom plate by the channel charge. The P+ drain and source regions provide a means for connecting to this channel charge, thereby establishing a strong ($C_{gs} + C_{gd}$) component. The gate-body component has little effect on the overall capacitance in this region, as it takes on the HF characteristic shown in Figure 4.4(a).

For positive DC biases ($V_{TOP} > V_{BOT}$), the PMOS is in its accumulation region. The capacitances C_{gs} and C_{gd} contribute little to the overall capacitance because it is not possible to contact the channel charge through the reverse biased PN junction formed between the P+ regions and the N-type channel. Therefore, the positive-biased gate-body capacitance (shown in Figure 4.4(a)) will dominate the overall capacitance.

One advantage of choosing a MOSFET structure, as opposed to the simple MOS-C structure of Figure 4.2, is that the device electrical representation can be extracted and simulated from layout. The approximate C-V characteristic can be obtained either by applying an AC gate voltage and examining the imaginary component of the current, or by using the DC-CAP feature in HSPICE [41]. The results are shown in Figure 4.6.

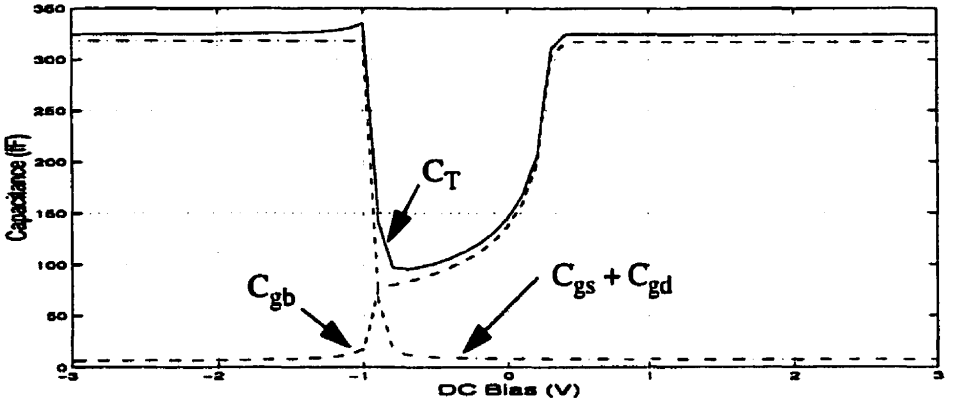


Figure 4.6: Capacitance-Voltage Characteristic for the P-MOSFET Structure

As evidenced by the abrupt junctions and unrealistically flat accumulation and inversion regions [40], the HSPICE results are not accurate. Moreover, the results vary considerably depending on the MOS gate capacitance model used [41]. Nevertheless, it is important that the structure can be simulated from layout, so that at least the overall circuit functionality can be confirmed before fabrication.

Another advantage to using the structure of Figure 4.5 is that its C-V characteristic is insensitive to the body effect, which can delay the onset of inversion. That is, no distortion will arise due to a C-V curve shift caused by a varying source-body voltage as shown in [42], since in this case, V_{sb} is fixed at 0 V. As will become evident in the SC circuits that follow, an additional advantage to using the structure of Figure 4.5 is that all three regions of operation can be investigated with this single device, depending on the DC bias conditions.

(iv) Distortion in SC Integrators

To understand how the voltage dependence discussed above can result in non-linearities in SC circuits, consider the basic non-inverting SC integrator, depicted in Figure 4.7 in its single-ended, stay-insensitive configuration.

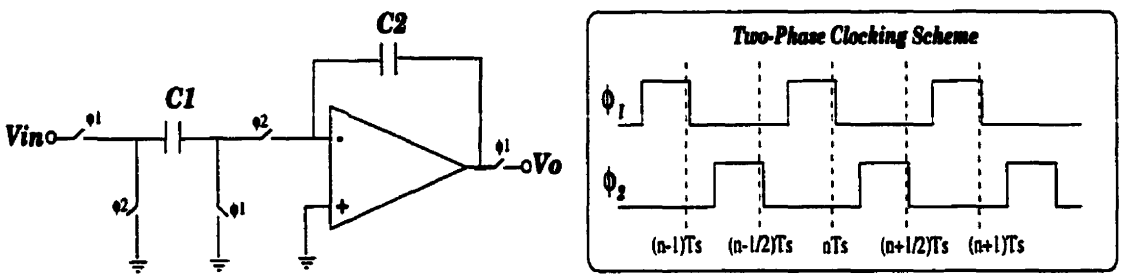


Figure 4.7: Basic SC integrator to illustrate effect on capacitor non-linearities

First consider its operation under ideal conditions. At the end of ϕ_1, a charge of $Q_1 = C_1 * V_{in}$ will be stored across the input capacitor, C_1. During ϕ_2, this charge will be transferred onto the integrating capacitor, C_2 as described in the charge balance relation,

$$Q_2(n) = Q_1(n-1) + Q_2(n-1) \tag{4.5}$$

where T_s represents the sampling period corresponding to the waveform of Figure 4.7. If the charge-voltage relation for C_2 is given by $Q_2 = C_2 * V_o$, the output voltage will be given by Eq. (4.6),

$$V_o(n) = \left(\frac{C_1}{C_2}\right) V_{in}(n-1) + V_o(n-1) \tag{4.6}$$

which clearly illustrates the integrating function is linear. Next consider the case when each capacitor is described by a non-linear function that can be expanded into a Taylor series,

$$C_i(v) = C_{o_i}(1 + a_1 v + a_2 v^2 + \ldots), \quad i = 1, 2 \tag{4.7}$$

where v represents the voltage across the capacitor, C_o is the nominal capacitance under quiescent conditions and a_1 and a_2 represent the linear and quadratic coefficients of capacitance, respectively. Note that to simplify matters it has been assumed that capacitors C_1 and C_2 are matched, resulting in the same voltage coefficients for both. Next, substituting

Eq. (4.7) into the charge balance relation of Eq. (4.6) will result in the input-output relation described below:

$$C_{o_2}\left\{1+a_1V_o(n)+a_2[V_o(n)]^2+\ldots\right\}V_o(n) = C_{o_1}\left\{1+a_1V_{in}(n-1)+a_2[V_{in}(n-1)]^2+\ldots\right\}V_{in}(n-1)+ C_{o_2}\left\{1+a_1V_o(n-1)+a_2[V_o(n-1)]^2+\ldots\right\}V_o(n-1) \quad (4.8)$$

Since the voltages $\{V_o(n), V_o(n-1), V_{in}(n-1)\}$ are not generally equal, the non-linear, bracketed terms will not cancel. Therefore, Eq. (4.8) can not be easily separated into the classic integrator form of Eq. (4.6). Depending on the level of the input and output voltages, the effective capacitor values will differ, producing variations in the integrator gain which lead to harmonic distortion at the output. As discussed in [39], a rough approximation of the level of the first two distortion components can be obtained by solving Eq. (4.8) for the sinusoidal case, employing three term truncated polynomials. These results are shown in Eqs. (4.9) and (4.10), below:

$$HD_2 \approx \frac{a_1}{2}\sqrt{V_o^2+\left(\frac{V_{in}}{2}\right)^2} \quad (4.9)$$

$$HD_3 \approx \frac{a_2}{4}\left(V_o^2+\frac{V_{in}^2}{3}\right) \quad (4.10)$$

The difficulty in using the above estimates is in determining the voltage coefficients of capacitance, as the precise C-V relation can be difficult to obtain. Furthermore, as will be seen next, not every integrator in an SC circuit will lead to overall distortion, regardless of the fact that it may be non-linear itself.

(v) Distortion in Multi-Stage SC Circuits

To determine how capacitor non-linearities affect multistage SC circuits, consider the SC circuit from a charge-processing point of view. As explained in [43], as long as the bias across any capacitor is controlled by only a single node voltage (as is most often the case), an SC circuit will realize linear charge processing. That is, a SC circuit will have the same

charge transfer function, regardless of the capacitor realization. It is thus possible, to represent a SC circuit as in Figure 4.8.

Figure 4.8: The SC Technique from a Charge Processing Point of View

The only requirement for overall linearity with respect to voltage is that the input and output blocks are also linear. In a conventional SC integrator as in Figure 4.7, the input capacitor, C_1, inherently performs the V-to-Q conversion. Similarly, the integrating capacitor, C_2, performs the Q-to-V conversion. Therefore, regardless of the order of the SC circuit, if the input capacitors to the first integrator, and the integrating capacitor of the output integrator are linear, the entire circuit will be linear.

As an example, consider the SC circuit shown in Figure 4.9, where capacitors C_2 and C_4 have non-linear C-V relationships. For clarity, consider the case where all capacitors have a zero initial condition. Let us track the flow of charge from input to output.

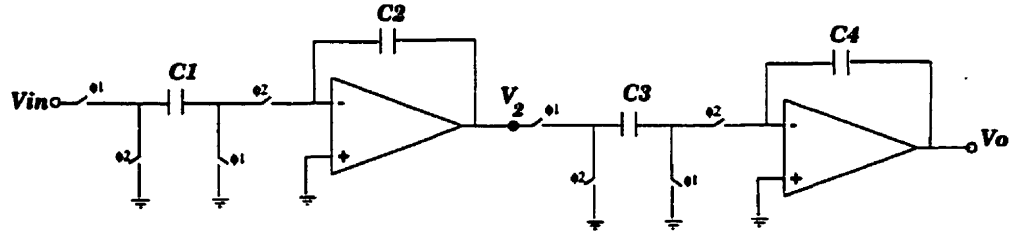


Figure 4.9: SC Circuit to Demonstrate Linear Charge Processing

During ϕ_1, capacitor C_1 is charged linearly by the input voltage. Adopting the timing reference used in the previous section (recall Figure 4.7(b)), results in a final charge given by:

$$Q_1(n-1) = C_1 \cdot V_{in}(n-1) \tag{4.11}$$

Next, on ϕ_2, this charge is completely transferred onto the non-linear capacitor, C_2, by means of the opamp ground. This charge will set up a voltage at node V_2, given by:

$$V_2(n) = \frac{Q_1(n-1)}{C_{o_2}\{1 + a_1 V_2(n) + a_2[V_2(n)]^2 + \ldots\}} \tag{4.12}$$

On the next phase of ϕ_1, this voltage will charge up capacitor C_3, to a value of:

$$Q_3(n) = C_{o3}\{1 + a_1 V_2(n) + a_2[V_2(n)]^2 + \ldots\} \cdot V_2(n) \tag{4.13}$$

Since C_2 and C_3 are assumed to be matched, including their non-linear terms, and share the common node voltage, V_2, their non-linear voltage dependent terms are identical. Therefore, when Eq. (4.12) is substituted into Eq. (4.13) above, these terms cancel, resulting in:

$$Q_3(n) = \frac{C_{o_3}}{C_{o_2}} \cdot Q_1(n-1) \tag{4.14}$$

Thus the first opamp, with capacitors C_2 and C_3 connected to its output node performs the operation of a linear charge mirror [43], independent of capacitor technology. During the next phase of ϕ_2, this charge is completely transferred to the linear capacitor C_4, resulting in an output voltage given by:

$$V_o\left(n+\frac{1}{2}\right) = \frac{Q_4\left(n+\frac{1}{2}\right)}{C_4} = \frac{(C_{o_3}/C_{o_2}) \cdot Q_1(n-1)}{C_4} \tag{4.15}$$

Finally, substituting Eq. (4.11) into Eq. (4.15) the input-output relation in terms of voltage is obtained as:

$$V_o\left(n+\frac{1}{2}\right) = \left(\frac{C_{o3} \cdot C_1}{C_{o2} \cdot C_4}\right) \cdot V_{in}(n-1) \tag{4.16}$$

If the output is sampled on the next ϕ_1, the input will have incurred two delays when propagating through the circuit, one for each non-inverting integrator, as expected. From Eq. (4.16), it is clear that the output voltage is a linearly scaled version on the delayed input signal. It is therefore evident that for any SC circuit, the non-linearity of the internal capacitors will have no effect, as long as all capacitors connected to the same opamp output node are governed by the same non-linearities [43], which is a reasonable assumption.

This realization has strong implications when realizing ΔΣ modulators in particular. To see this, consider the basic ΔΣ modulator structure of Figure 4.10, implemented using a SC loop filter, represented from a charge processing point of view.

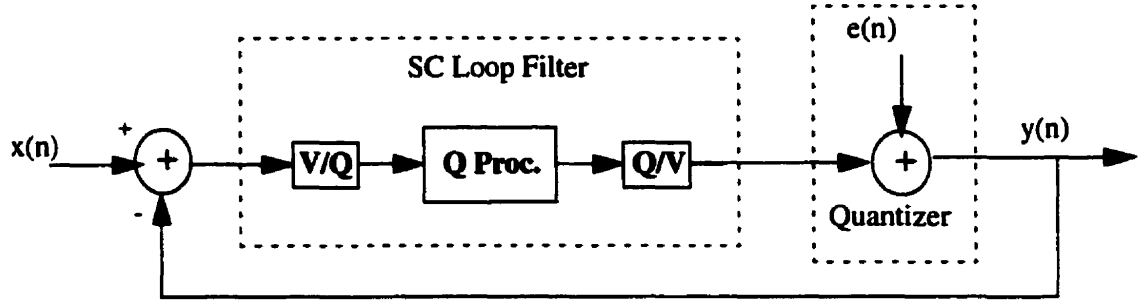


Figure 4.10: SC ΔΣ Modulator from a Charge Processing Perspective

Any distortion caused by non-linearities in the output Q-to-V stage appear just before the quantizer. These errors will thus be shaped by the modulator noise transfer function, in the same manner as the quantization noise. Therefore, in a SC ΔΣ modulator, the primary source of distortion will be from the input capacitors of the first integrator.

Now that it has been seen how MOS-capacitors can cause distortion in SC circuits, next we shall investigate how the non-linearity from any individual MOS-capacitor can be reduced.

4.2.2 Reducing the MOS-Capacitor Non-Linearity

(i) Use of Additional DC Biasing

One way to reduce the non-linearity introduced by the MOS-capacitor is to bias the device in one of the flatter regions of its C-V characteristic. This was first proposed in [44] for the single-ended lossy integrator of Figure 4.11.

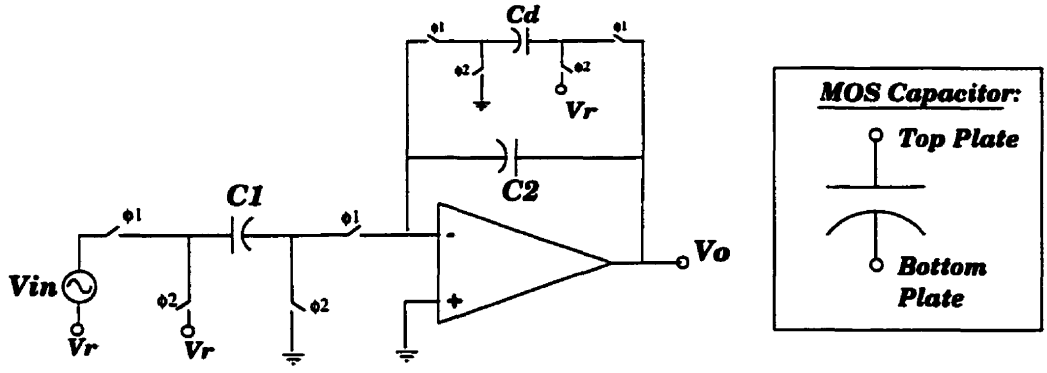


Figure 4.11: Configuration used to Bias PMOS-Capacitors in Accumulation

By applying a positive reference voltage, V_r, at key points in the SC circuit, one is ensured that on both clock phases, a DC bias equivalent to V_r will always exist across the MOS capacitor. As discussed previously, biasing the capacitor in the accumulation region greatly reduces its voltage dependence. The drawback of the setup shown in Figure 4.11 is that unless the opamp has a DC output level equal to V_r, damping is required to maintain the bias across the integrating capacitor, C_2. That is, the amplifier itself does not inherently provide different input and output common mode levels to bias C_2. Therefore, C_d is necessary to establish an output common mode level of V_r, and thus impose a DC bias on C_2. To overcome this constraint, the alternate configuration of Figure 4.12 can be used [40]. This setup does not require damping regardless of the opamp DC output level.

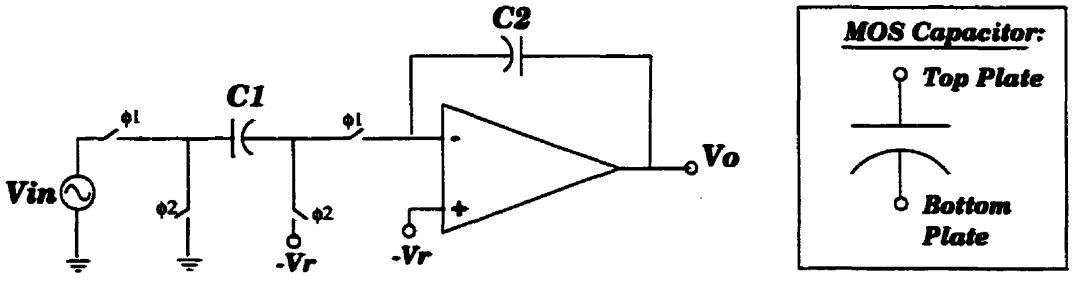


Figure 4.12: Alternate DC Biasing Configuration

As previously discussed, it is desirable to use a differential structure in any SC implementation. Figure 4.13 illustrates a DC biasing scheme for a differential integrator structure that will ensure the biasing of the MOS-capacitors is controllable. A similar approach was used in [42] in biasing the MOS-capacitors of a SC delay cell.

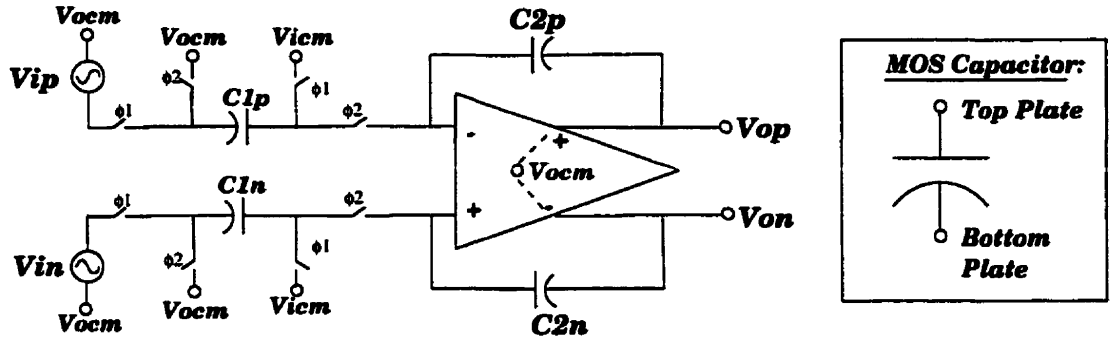


Figure 4.13: DC Biasing Scheme for a Differential SC Integrator

In this case, the differential amplifier has a non-zero output common mode level, V_{ocm}, that is controllable by varying the reference voltage in its common-mode-feedback circuit. The amplifier common-mode input level will be forced to the DC reference level, V_{icm}, by the SC topology. Therefore, on either clock phase, a DC bias of (V_{icm}-V_{ocm}) will be present across each MOS-capacitor. This will not affect the settling behavior or parasitic-insensitivity of the structure.

As long as the amplifier has sufficient input and output common-mode ranges, the DC bias voltages, V_{icm} and V_{ocm}, can be varied to bias the MOS-capacitors in any desired region of its C-V characteristic.

(ii) Use of Composite MOS-Capacitors

In some applications however, the extra biasing required in the previous section may not be desired. For example, in low-voltage circuits where headroom is limited, it might be necessary to simply operate the MOS-capacitors in their depletion regions. In this case, one of the composite capacitor structures of Figure 4.14 could be used to reduce the distortion.

(a) Parallel (b) Series

Figure 4.14: Structures to Reduce Non-Linearity, without DC Biasing

The idea behind the parallel structure seen in Figure 4.14(a) is that because the two constituent capacitors have opposite voltage polarities across their plates (v_2=-v_1), their voltage-dependent non-linearities will cancel when the two capacitances are summed in parallel. In fact, this simple circuit has been patented [45], and shown to cancel the odd order harmonic distortion components produced by the capacitor non-linearities.

In the series structure in Figure 4.14(b), the two capacitors also have opposite polarities across their plates. In addition the voltage that appears across either of the constituent capacitors is only half the magnitude of the voltage across the composite capacitor. As a result, the severity of the C-V dependence is lessened considerably. Figure 4.15 illustrates the C-V characteristics for each of the series capacitors and the composite capacitance, C_T.

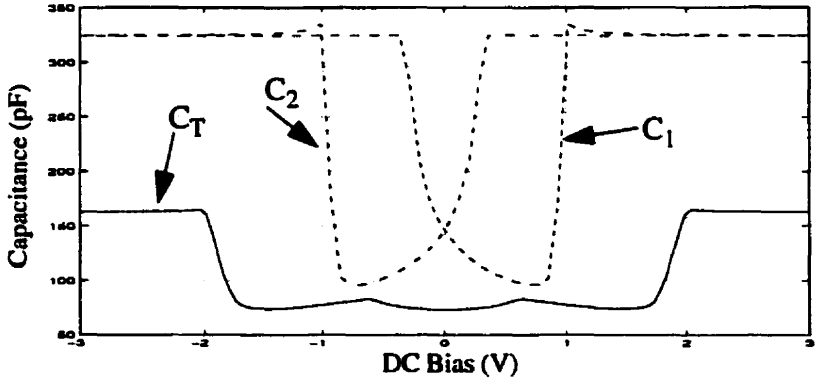


Figure 4.15: C-V Characteristics for the Composite Series Branch

An alternate approach to improving the capacitor non-linearity can be applied at the layout level, as shown in Figure 4.16. The basic structure is that of pmos capacitor where the gate poly forms the top plate, and the bulk forms the other. The MOS has been modified slightly by adding extra highly-doped P+ diffusion regions in the N-well.

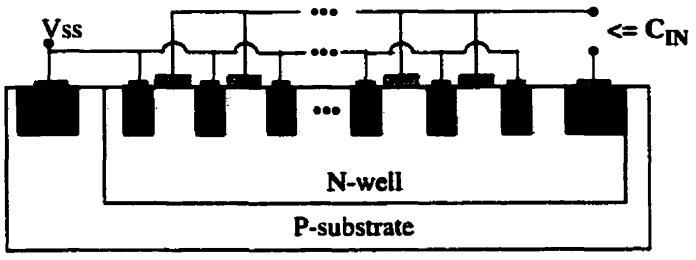


Figure 4.16: MOSFET Layout to Reduce Non-linearity

To understand the reasoning behind this structure, consider the following. Recall that the reason the C-V curve decreases in the depletion region is due to the fact that the width of the depletion region under the gate oxide increases with decreasing gate voltage. In doing so, it exposes ionized donor sites, which provide the positive charge necessary to satisfy Gauss' Law of charge conservation throughout the device. The extra p-doped sites of Figure 4.14c, are meant to provide this charge directly, so that the depletion width modulation is not necessary, and the C-V characteristic will remain flatter.

(iii) Use of DC-Biased, Composite MOS-Capacitors

Next, consider the two techniques shown in Figure 4.17 which bias the MOS-capacitors in their flatter accumulation regions, as well as using composite structures similar to those of Figure 4.14. These specific schemes were first proposed in [46], although similar circuits have been independently proposed in [47].

In the first scheme, shown in Figure 4.17(a), two additional capacitors, denoted C_H, are used in conjuction with the parallel combination of two signal-path capacitors, denoted C_S. On clock phase ϕ_1, all capacitors are biased in their accumulation regions via the reference voltages, V_{bp} and V_{bn}. On the next phase, the holding capacitors, C_H, maintain the DC bias across the signal capacitors while the input signal is applied. Therefore, this scheme will cancel distortion products as did the scheme of Figure 4.14(a), in addition to lowering the overall distortion to begin with by biasing the MOS-capacitors in their accumulation regions. Figure 4.17(b) illustrates another technique referred to as series compensation. On ϕ_1, the bias voltage, V_b sets each of the MOS-capacitors in their accumulation regions. On the next phase, it can be shown [46] that the charge delivered by the SC branch is linear

with respect to the applied input voltage, to a first order approximation. One obvious, but minor drawback of these approaches, is that they each require approximately four times the capacitance area compared to a standard SC branch.

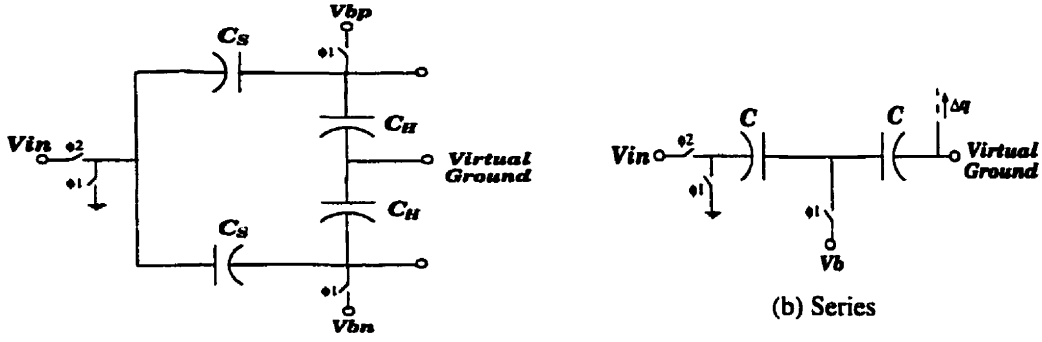


Figure 4.17: Composite SC Branches proposed in [46]

The above two compensation schemes have been used in conjunction with correlated-double-sampling techniques[48], to produce amplifiers with up to 70 dB dynamic range[49][50]. More recently, these techniques have been used to linearize the input capacitor of a ΔΣ modulator [51], and achieve up to 16 bits of resolution. As discussed in Section 4.2.1(v), this is the one dominant source of distortion in SC ΔΣ modulators, therefore these results are not surprising. In ΔΣ modulators, it is only necessary to linearize the input capacitor, which is why 16-bits of resolution is possible, even though the other capacitors are not linearized to the same extent.

Unfortunately, the above two schemes are not applicable to any SC circuit in general. In cases where the capacitor can not be reset to a bias voltage on every alternate phase, the two composite branches can not be applied. This case exists in general for any integrator-based design, where the integrating capacitor can obviously not be reset.

In the following sections, we examine two prototype integrator-based SC circuits: A biquadratic filter and ΔΣ modulator. The designs use the first two strategies discussed in this section. As mentioned above, the last technique is not applicable to the biquadratic filter, and although it would likely improve the performance of the ΔΣ modulator, it was not applied. The research concerning its use in ΔΣ modulators only surfaced after the prototype modulator had been sent for fabrication.

4.2.3 Prototype Filter

This is the first of the two SC prototypes employing MOS-capacitors that will be investigated. Switched-Capacitor filter design is a well understood and developed field. Therefore, to obviate reinventing the wheel, we begin our discussion directly with the second-order lowpass filter originally designed in [52]. The basic structure is shown in Figure 4.18 in its single-ended configuration for simplicity.

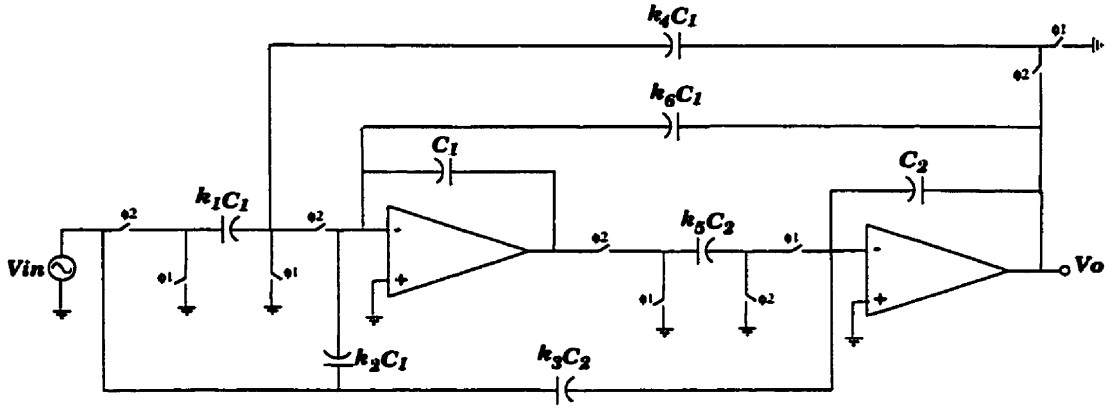


Figure 4.18: Second-Order Lowpass SC Filter Prototype

The circuit consists of two stray-insensitive integrators in a loop, with feedforward (k_2, k_3) and feedback (k_4, k_6) paths clearly visible. The discrete time transfer function of this topology is given by,

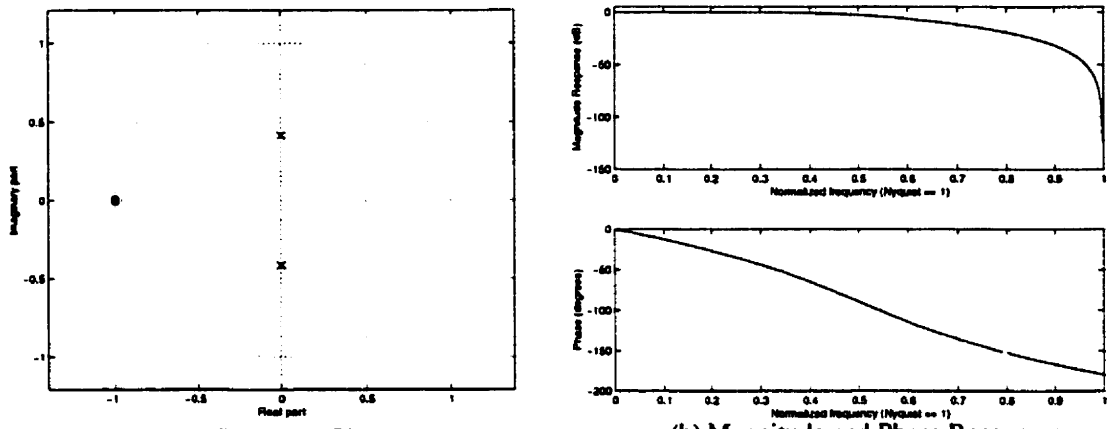
$$\frac{Vo}{Vi}(z) = -\left[\frac{k_3z^2 + (-2k_3 + k_1k_5 + k_2k_5)z + k_3 - k_2k_5}{z^2 + (-2 + k_4k_5 + k_5k_6)z + 1 - k_5k_6}\right] \tag{4.17}$$

The dynamic-range scaled coefficient values of Table 4.1 were used to obtain a lowpass filter response with a 3 dB point of one quarter the clock frequency and a maximally flat passband region. The wide, flat passband will facilitate experimental measures of Spurious-Free Dynamic Range (SFDR), as calibration will not be necessary.

Coefficient	Value
k_1	1.0824
k_2	0
k_3	0.2929
k_4	1.0824
k_5	1.0824
k_6	0.7654

Table 4.1: Dynamic-Range Scaled Coefficient Values for the SC Filter

For the coefficient values listed in Table 4.1, the ideal pole-zero plot and frequency response of the filter are shown in Figure 4.19.



(a) Pole-Zero Plot (b) Magnitude and Phase Responses

Figure 4.19: Ideal SC Filter Response

The filter was implemented using the differential integrator structure of Figure 4.13, using the MOSFET-capacitor structure of Figure 4.5. The DC voltages, V_{icm} and V_{ocm}, can be varied to bias the MOSFET-capacitor either in its accumulation, inversion or depletion regions, while ensuring that the DC bias does not cause the amplifier to exceed its input and output common-mode ranges. Note that due to area constraints, it was not possible to implement the structures of Figure 4.14 with the filter aswell. However, they will be investigated in the ΔΣ modulator prototype that follows. In the ΔΣ design, there are fewer capacitors and the coefficients have less of a spread, therefore the area constraint is less critical.

Other issues such as matching, absolute capacitor sizing, transmission gate sizing, and floorplanning were dealt with in much the same manner as discussed in Chapter 3. Next, the layout of the filter was performed in a double-poly process, allowing for the flexibility to multiplex between MOSFET-capacitors and the traditional linear poly-poly type. An HSPICE netlist was extracted from the layout and the filter functionality was verified. However, as discussed previously, the simulation results are not useful to assess the filter performance due to inadequate modeling and excessive simulation times. The prototype filter was fabricated in a 0.8μ BiCMOS process on the same IC as the prototype ΔΣ modulator that follows. The chip photomicrograph is shown in Figure 4.20, where the filter section of the IC consumes an active area of approximately 0.67 mm^2.

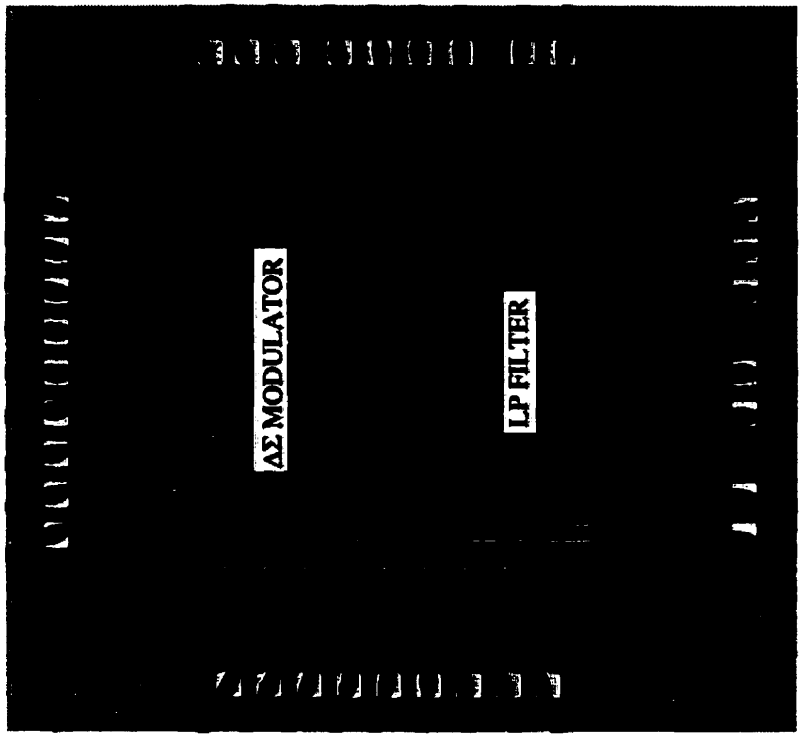


Figure 4.20: Chip Micrograph of SC Circuits employing MOSFET-capacitors

To test the filter, it was necessary to add an input stage to apply the DC offsets (V_{icm}, V_{ocm}) and perform the single-ended to differential conversion of the input stimuli. In addition, an output stage was required to interface between the differential filter output and the single-ended test equipment. The overall test setup is shown in Figure 4.21.

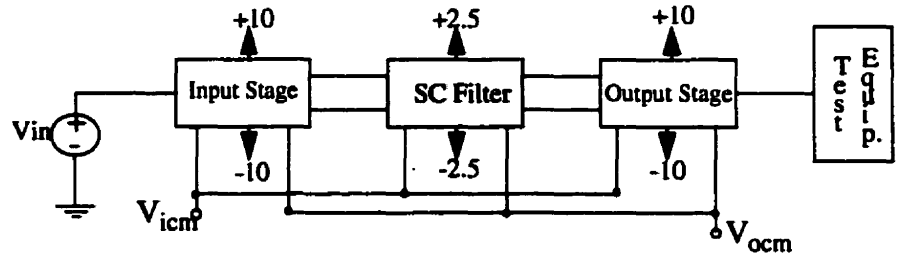
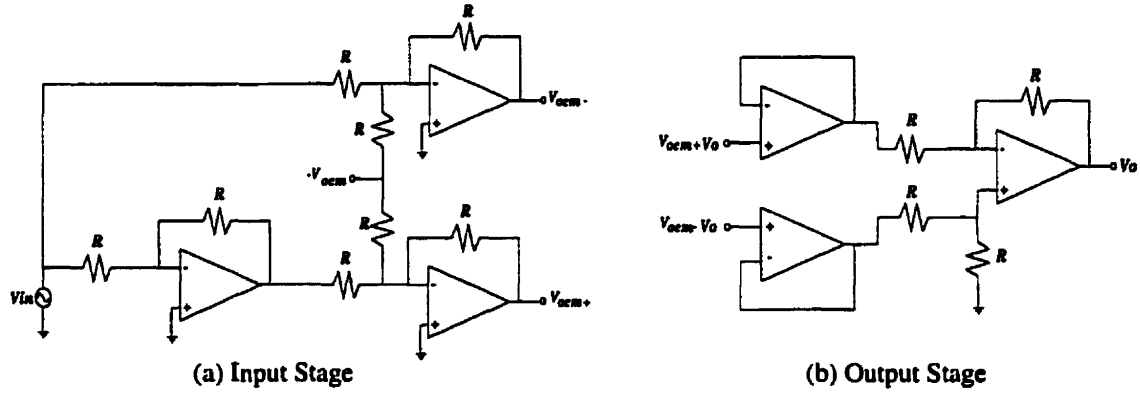


Figure 4.21: Overall Filter Test Setup

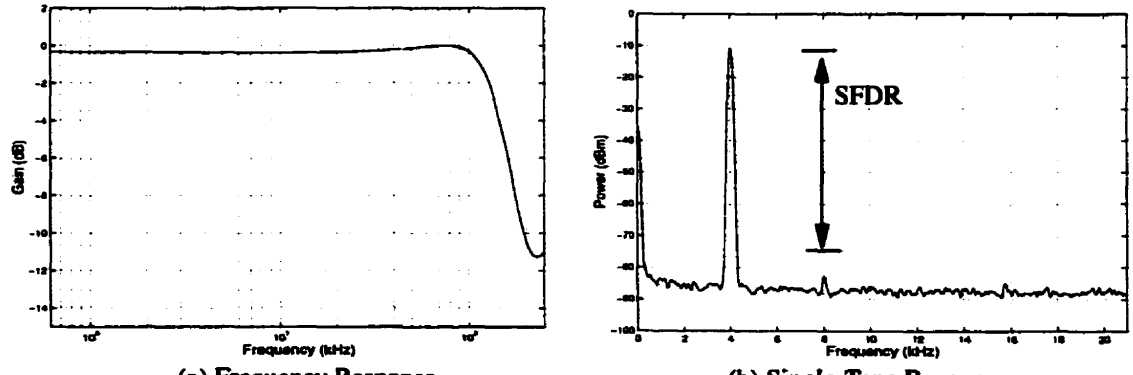
The input and output stages consist of standard opamp circuits [59] that were assembled off-chip to conserve silicon area, using discrete components as shown in Figure 4.22 below:



(a) Input Stage (b) Output Stage

Figure 4.22: Input and Output Stages Required in the Overall Test Setup

Next, the basic SC filter, employing standard poly-poly capacitors was connected in the configuration shown in Figure 4.21 above. When clocked at a frequency of 500 kHz, the filter dissipates approximately 50 mW of power and has the behavior shown in Figure 4.23



(a) Frequency Response (b) Single-Tone Response

Figure 4.23: Experimental Filter Behavior, employing Poly-Poly Capacitors

The frequency response exhibits a 3-dB point of 137 kHz approximately one-quarter the clocking frequency. In the interval between the 3-dB point and the Nyquist frequency (250 kHz), the filter attenuates the signals at a rate of approximately 12 dB per octave as would be expected from a second-order filter. The single-tone response shows an SFDR of approximately 72 dB in the test environment used.

Next, the filter was tested with the standard poly-poly capacitors replaced by MOSFET ones. In this case, the overall frequency response was not noticeably affected, however, the distortion performance in response to a single tone input depended heavily on how the MOS-capacitor was biased. This effect can be seen by the plot of Figure 4.24 which illustrates how the SFDR is affected as a result of varying the DC Bias (V_{icm}-V_{ocm}) over a 6 volt range.

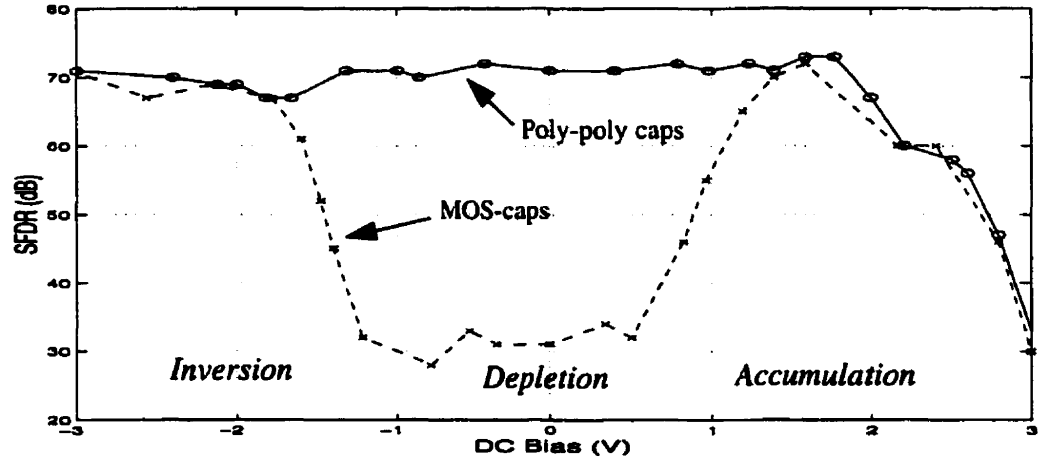


Figure 4.24: Effect of Capacitor DC Bias on the Filter SFDR

In all cases, the measurements were performed with respect to a constant differential input voltage level of 1 V. The top-to-bottom plate capacitor bias is determined by varying the difference between the DC bias voltages (V_{icm}-V_{ocm}), that are applied to each integrator, as shown in Figure 4.13. With no DC bias applied, the MOSFET-capacitors operate in their depletion regions, where the C-V characteristic is highly non-linear. It is therefore not surprising that the SFDR is only in the 30 dB range, limited by a strong third harmonic.

However, as little as 1.4 V is enough to bias the MOS-capacitors in their accumulation regions and attain an SFDR of over 70 dB, equal in performance to the reference case where poly-poly capacitors were used. When biasing the MOS-capacitors in their inversion re-

gion, slightly more bias (1.8 V) is required to attain equal performance. This fact is consistent with the simulation results obtained for the MOSFET-capacitor structure, which are shown in Figure 4.6. Finally, note that the performance degradation when more than 2 volts of DC bias is applied is expected and occurs regardless of the type of capacitor in use. This limit is imposed by the diminishing amplifier output voltage swing as its output common mode level (V_{ocm}) approaches the circuit rails.

Unfortunately, the performance of the filter that employs standard poly-poly capacitors was itself no better than approximately 70 dB. It is therefore not possible to ascertain whether the MOSFET-capacitors, when adequately biased, are indeed limiting the performance of the filter under investigation. However, this work does show that an SFDR of at least 70 dB is attainable with ease, by performing some simple modifications on existing SC structures.

4.2.4 Prototype ΔΣ Modulator

Next, we examine the second of the two prototype switched-capacitor circuits implemented using MOSFETs as capacitors. The design of the modulator is based on the second-order lowpass ΔΣ modulator which was examined in Chapter 2. The SFG-level signal flow graph is shown again in Figure 4.25 below for convenience.

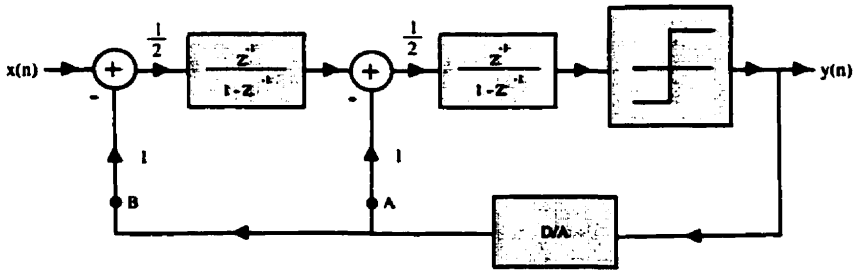


Figure 4.25: SFG-Level Structure for Prototype ΔΣ Modulator

The obvious advantage of using this structure is that it has already been used successfully in the modulator of Chapter 2. In addition, recall that it does not require a large signal range at the output of the integrators [3]. This has particular relevance when MOSFETs are used to implement the capacitors. Reducing the output voltage swing will help keep the ampli-

fiers from leaving their linear regions and keep the MOS capacitors biased in their desired regions for a greater range of signal levels.

The two integrators were implemented using the differential SC structure of Figure 4.13 where the DC bias voltage, V_{icm} and V_{ocm}, are tunable. As with the prototype filter, this allows the MOS capacitors to be biased in either their accumulation, inversion or depletion regions. In addition, it is also of interest to access the merits of using the three composite structures of Section 4.2.2. Therefore each capacitor of the SC circuit was actually replaced by a bank of capacitors, anyone of which could be active at a given time through simple multiplexing.

Due to the area constraints and number of capacitor types, it was necessary to use a smaller unit size capacitor than in the design of Chapter 2. Table 4.2 details the various capacitor structures under investigation and the approximate area a unit capacitor of that type would occupy to achieve the nominal value indicated.

Capacitor Type	Dimensions	Nominal Value	Reference Figure
Poly-Poly	19.5μ x 23.2μ	300 fF	-
Basic MOS(inv/accum)	20μ x 17.2μ	325 fF	Figure 4.5
Basic MOS(depletion)	20μ x 17.2μ	~150 fF	Figure 4.5
Parallel MOS	2x(20μ x 17.2μ)	~300 fF	Figure 4.14a
Series MOS	2x(20μ x 17.2μ)	~75 fF	Figure 4.14b
Extra-Dopant MOS	20.0μ x 50.8μ	~150 fF	Figure 4.14c

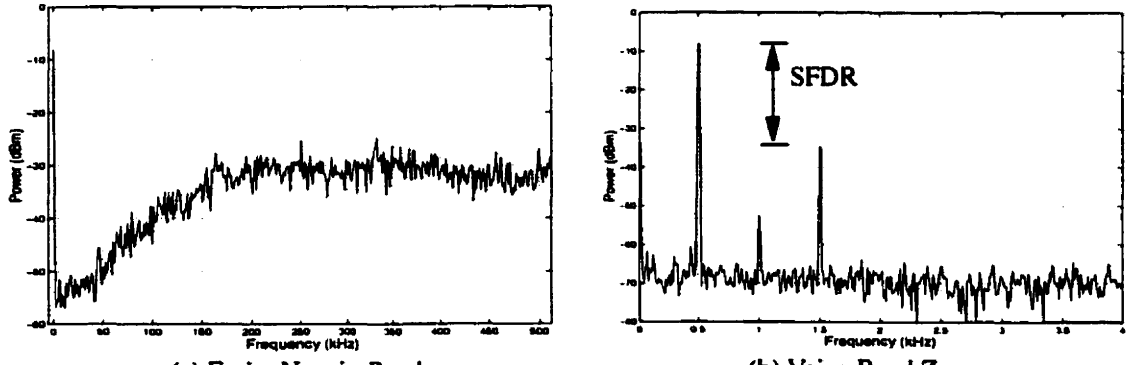
Table 4.2: Implemented Capacitor Structures and Area Requirements

When biased in its accumulation or strong inversion region, the basic MOS capacitor has a higher capacitance per unit area than the standard double-polysilicon counterpart (1.97 fF/μ^2 compared to 1.15 fF/μ^2 [20]). However, due to the extra overhead imposed by the drain and source regions, it occupies only slightly less area. The last four capacitor types above are intended for use without any additional biasing whatsoever, operating in their depletion regions. In the case of the basic MOS capacitor, the nominal capacitance value for a given area is approximately halved. The series and extra-dopant structures are the most demand-

ing on area, requiring four to five times that of the traditional double-poly type to achieve the same capacitance values.

Complete simulation of the transistor level design was prohibitively long. However, by using idealized models where possible and a lower clocking rate, the basic circuit functionality was able to be verified, warranting fabrication. The chip micrograph is shown in Figure 4.20. The ΔΣ modulator occupies an active area of approximately 0.88 mm^2 and consumes approximately 75mW of power when clocked at 1 MHz.

It has already been seen in Chapter 2 that the ΔΣ modulator functions correctly when realized with poly-poly capacitors. Next, we examine how the use of non-linear MOSFET capacitors affects the distortion performance. Specifically, the SFDR will be used as a metric, and monitored under different circuit conditions. Figure 4.26 below illustrates the modulator operation when basic MOSFETs are used to implement the capacitors without any biasing whatsoever.



(a) Entire Nyquist Band (b) Voice-Band Zoom

Figure 4.26: Experimental Performance using Non-Biased MOSFET Capacitors

Although the noise shaping behavior is apparent, there is significant distortion evident in the signal band zoom. In this case, the MOSFETs were biased in their depletion regions and one would therefore expect the performance to be poor. However as seen in Figure 4.27, when a DC bias (V_{icm}-V_{ocm}) is applied across the capacitors, the harmonic distortion drops considerably. Note that in all cases the SFDR was measured for a maximum-stable differential input amplitude of 0.6 V. This is slightly below the maximum-stable level (using reference levels of +/- 0.5 V) so that one can be sure that the distortion tones are not a result of instability

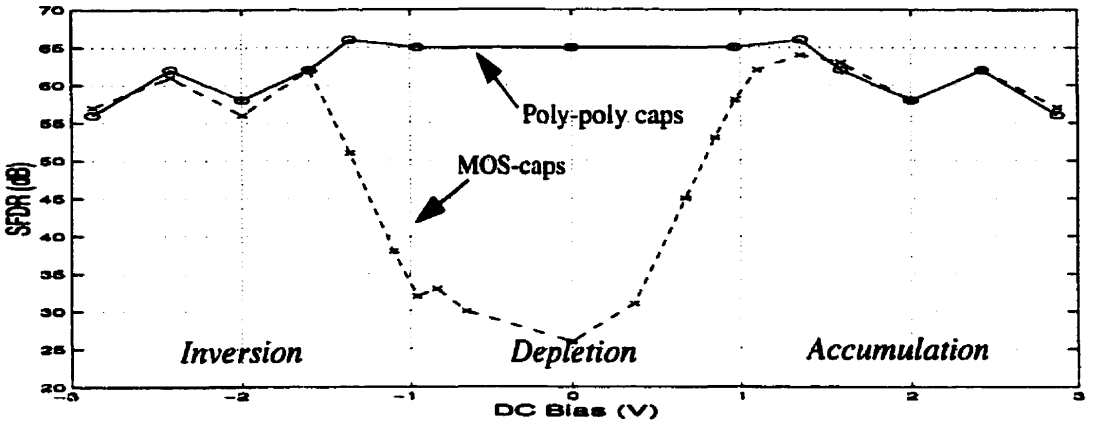


Figure 4.27: Effect of Capacitor DC Bias on the Modulator SFDR

.Consider first the reference case where poly-poly capacitors are used. The decrease in SFDR with respect to the modulator of Chapter 2 is thought to be due to the smaller capacitor sizes used, especially at the input stage, which leaves the modulator more susceptible to non-linear charge injection. As previously mentioned, smaller capacitor sizes were used to accommodate the many different capacitor types.

Figure 4.27 shows that as little as 1.4 V is sufficient to bias the MOS capacitors in their accumulation region and attain an SFDR of approximately 65 dB, equivalent to that of the reference case. As with the prototype filter, slightly more bias is required when operating the MOS capacitors in their strong inversion regions.

Next, we consider more closely the situation where no additional bias is applied to the capacitors. Table 4.3 details the measured SFDR for the various MOSFET capacitor structures investigated. Once again, all measurements were taken at a constant differential input amplitude of 0.6 V.

Capacitor Type	SFDR (dB)
Poly-Poly	65
Basic MOS	26
Parallel MOS	26
Series MOS	32
Extra-Dopant MOS	32

Table 4.3: Maximum SFDR Attainable with Non-Biased MOSFET Capacitors

The results indicate that when no bias is used, it is only possible to achieve an SFDR in the range of 32 dB. Moreover, this only occurs when the *series* or *extra-dopant* structures are used which require much greater area. Therefore, it is doubtful that the use of non-biased MOSFET capacitors would be feasible for the vast majority of applications.

Next, we consider a entirely different approach to realizing the analog components of a ΔΣ modulation system in a purely digital CMOS process, namely that of switched-currents.

4.3 The Switched-Current Approach

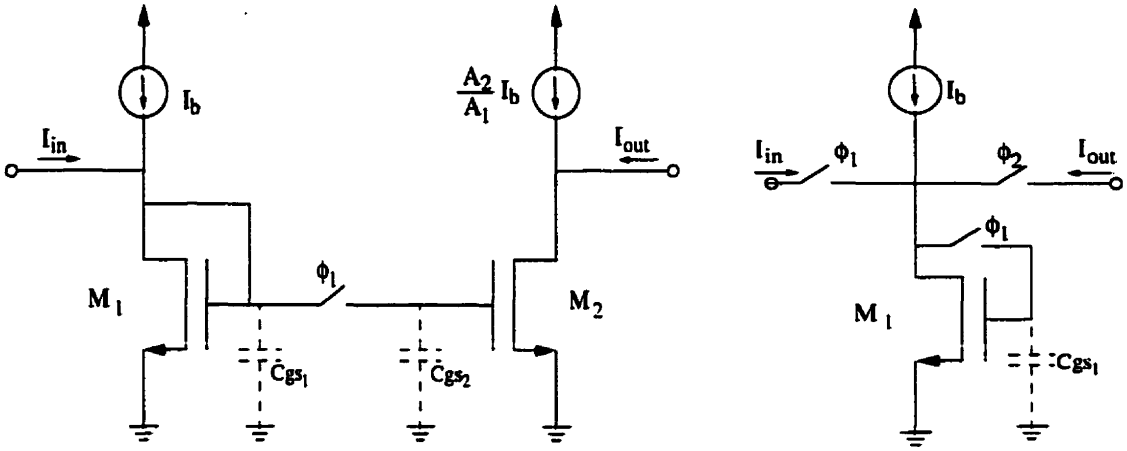
This is the second of the two sampled-data circuit techniques under investigation that can be implemented without the use of linear capacitors which require an extra layer of poly-silicon in fabrication. In fact, as will become apparent shortly, the switched-current (SI) approach does not require any explicit capacitors whatsoever. Before examining two prototype ICs design using this approach, the SI technique itself will first be discussed.

4.3.1 Implementation using the SI Technique

We begin our discussion with an introduction to the basic SI building block, the memory cell. Thereafter, we will consider some of the most important implementation issues involved in designing SI circuits. The section will conclude by outlining a basic procedure for designing circuits using the SI technique.

(i) Basic Functionality

The fundamental building block used in SI circuits is the memory cell. To understand its operation, consider the first-generation SI memory cell proposed in [53][54], shown in Figure 4.28(a).



(a) First-Generation (b) Second-Generation

Figure 4.28: Basic SI Memory Cells

Note that the two capacitors, Cgs_1 and Cgs_2, are implicit to the MOSFET itself, and thus no external capacitors are required. The input and bias currents sum to form the drain current of M_1, and corresponding gate-source voltage. When the switch closes, this Vgs is imposed on M_2, and sets the drain current of M_2. If the transistors are matched, KCL dictates that the resulting output current will be equal to the input current. When the switch opens, the output current is held constant by means of Cgs_2. By adjusting the aspect ratios of the two transistors, a gain factor can be introduced, resulting in the transfer function given by Eq. (4.18).

$$T(z) = \frac{(W/L)_2}{(W/L)_1} \cdot z^{-1/2} \tag{4.18}$$

Figure 4.28b depicts the second-generation memory cell first proposed in [55]. It operates in much the same manner, but has the advantage that for unity gain, only one transistor is required. This eliminates mismatch effects, however, as discussed in [56] the second-generation cell introduces more harmonic distortion than its first generation counterpart.

Continuing with the first-generation cell, Figure 4.29 shows how it can be used to realize an integrator by cascading two memory cells to form a complete delay, and then applying feedback around it.

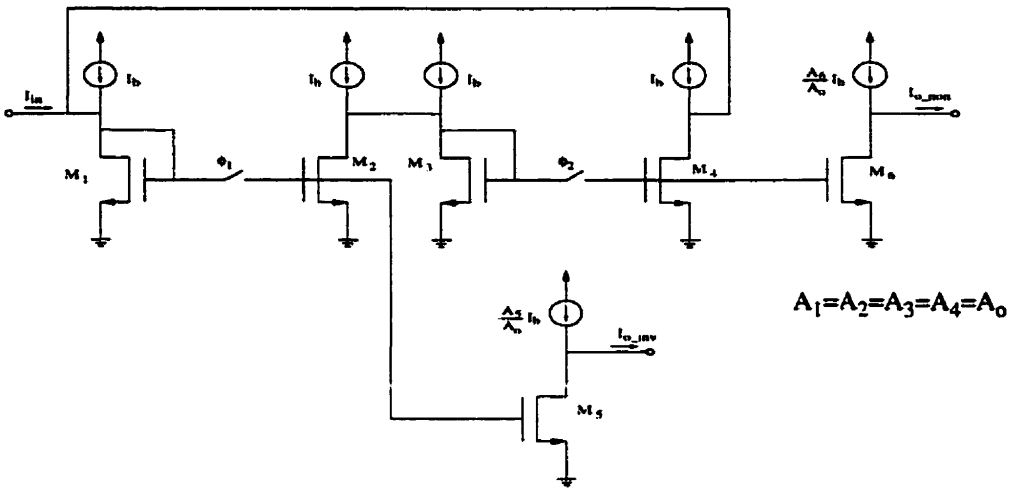


Figure 4.29: SI Integrator based on First-Generation Memory Cells

As with the SC technique, the circuit requires a two-phase non-overlapping clock to control the switches. Depending on where the output is taken, either a non-inverting or inverting integrator function is obtained, as described by Eqs. (4.19) and (4.20) respectively.

$$\frac{Io_{non}}{Iin}(z) = \frac{A_6}{A_o} \cdot \frac{z^{-1}}{1-z^{-1}} \tag{4.19}$$

$$\frac{Io_{inv}}{Iin}(z) = -\frac{A_5}{A_o} \cdot \frac{z^{-1/2}}{1-z^{-1}} \tag{4.20}$$

Note that these equations have the same form as those of traditional SC integrators and can thus be used to build more complex circuits in a similar manner.

(ii) Implementation Issues

In this section, we will briefly outline the three main factors that contribute to distortion in the above circuits and examine how their effect can be lessened.

The most obvious factor is the finite output resistance of the memory cell. This channel length modulation effect will directly lead to a output current variation depending on the

signal level. As explained in [57], the percentage current variation can be expressed in terms of the drain-source voltage variation,

$$\frac{\Delta I}{I} = \Delta V_{DS} \cdot \lambda \tag{4.21}$$

which can be used to approximate the constraint on resolution as:

$$n \approx \log_2\left(\frac{OSR}{\Delta V_{DS} \cdot \lambda}\right) \tag{4.22}$$

For example, for an oversampling ratio of 64, if λ=0.05 and ΔV_{DS}=1v, only about 10 bits can be expected. Alternatively, substituting $r_{out}=1/\lambda I$ into Eq. (4.22), one can express the requirement on output resistance in terms of the desired resolution:

$$r_{out} > \frac{2^{n+1}}{Ib_{min} \cdot OSR} \tag{4.23}$$

The next two issues have to do with errors in the final value of the voltage stored on the gate-source capacitance of the memory transistor. Charge injected from the sampling switch, as well as incomplete settling during the memorization phase of the SI memory cell will lead to errors in this voltage, and the corresponding memorized output current. Moreover, even if this V_{GS} error is a constant or linear one, since the I_D-V_{GS} relation is itself non-linear, it will still result in distortion seen in the current output. Note that this later shortcoming is specific to SI circuits, as linear and DC errors would not cause harmonic distortion in SC circuits.

To alleviate some of these problems, consider replacing each transistor in the SI circuit with the regulated-cascode (RC) equivalent [57] shown in Figure 4.30.

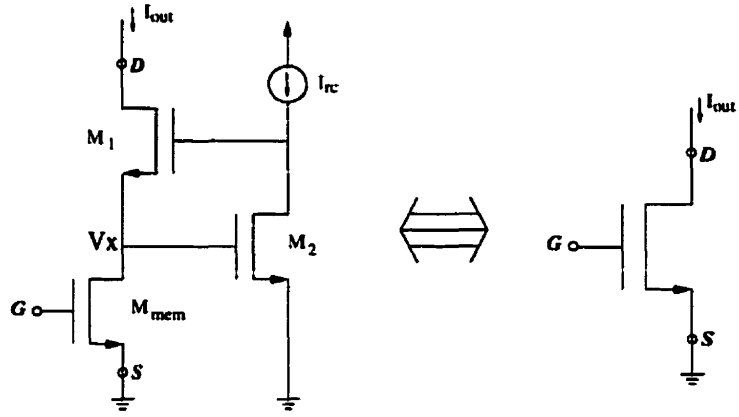


Figure 4.30: Regulated Cascode "Super-Transistor"

It consists of two extra transistors, M_1 and M_2, in addition to the main memory transistor, M_{mem}. Transistor M_1 acts as a current buffer, as in any cascode configuration. M_2 is used to fix the drain voltage of M_{mem} at a constant voltage so as to avoid the effects of channel length modulation. The cell is very efficient due to its negative feedback operation. If V_X increases, causing an increase in I_{OUT}, V_{GS2} also increases. Due to the constant current source, I_{RC}, the additional drain current associated with the increase in V_{GS2} will be drawn from the gate of M_1. This will thereby reduce V_{GS1} and I_{OUT}, offsetting the initial increase. During the constant current phase, the output resistance is given by

$$r_{out} = gm_1 ro_1 \cdot gm_2 ro_2 \cdot rds_{mem} \tag{4.24}$$

which is typically in the 100 M Ohm range, more than sufficient for our applications.

Due to the strong negative feedback mechanism, the RC cell will maintain a high output resistance even when M_{mem} enters the triode region. This is extremely useful for SI circuits, because when M_{mem} is operated in its triode region, its I_D-V_{GS} characteristic is linear, eliminating distortion of the current output introduced from constant and linear errors in V_{GS} discussed above. Furthermore, during the memorization phase of the SI memory cell, the input resistance with M_{mem} operating in triode is a constant (given by Eq. (4.32) to follow). With the settling time constant given by

$$\tau \approx 2 \cdot C_{GS} \cdot r_{in} \tag{4.25}$$

the variation in settling error with signal level is thereby reduced (though still affected by the non-linear C_{GS}), reducing the overall distortion.

In order to reap the full benefit of the increased output resistance of the RC cell, the current sources in the SI circuit must have equivalently high output resistance. One suitable choice is the high-swing double-cascode source [61] of Figure 4.31

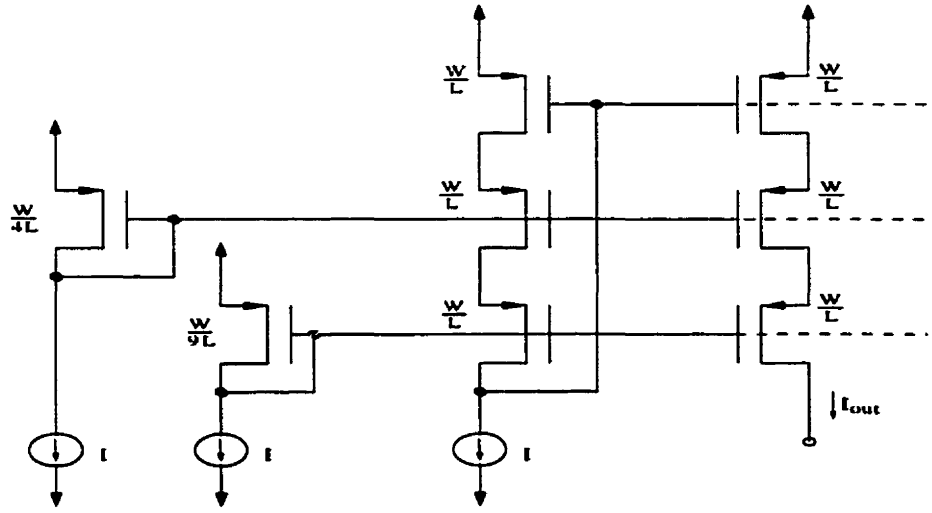


Figure 4.31: High-Swing Double-Cascode Current Source

The current source achieves a high output resistance by virtue of the double cascode. The three current sinks could be provided off-chip or via another mirror. A large output voltage swing is achieved because the cascode transistors are not diode connected. Instead, the two transistors on the left are used to bias the cascode transistors just at the edge of their saturation regions, thereby saving a V_{GS} drop in output swing for each cascode level.

(iii) Design Procedure

Before working at the transistor level, one must first arrange the signal-flow graph such that it is easily realized in terms of SI integrator blocks. Once this has been achieved, the next step in designing SI circuits involves finding the range of gate voltages that can appear on the SI memory transistor while keeping it in its triode region. With M_2 of the RC cell holding V_X at approximately Vt, triode operation will be maintained provided that, as explained in [64],

$$2V_t < V_{GS} < 3V_t \tag{4.26}$$

This constraint places a corresponding limit on the minimum and maximum allowable drain currents, given by Eqs. (4.27) and (4.28) respectively.

$$Imin = (1/2) \cdot \mu_n C_{ox}(W/L) \cdot V_t^2 \tag{4.27}$$

$$Imax = (3/2) \cdot \mu_n C_{ox}(W/L) \cdot V_t^2 \tag{4.28}$$

Next, we wish to ensure that the effects of thermal noise do not affect the accuracy of the design. One can estimate the SNR by dividing the RMS value of the input signal by the kT/C noise sampled on the gate-source capacitance of the memory transistor as in [60]. For example, in a data converter design with n bits accuracy, one must satisfy

$$\frac{[(3V_t - 2V_t)/2]/\sqrt{2}}{\sqrt{kT/(Cgs \cdot OSR)}} > 2^{n+1} \tag{4.29}$$

This will set a lower bound on the gate-source capacitance of the memory transistor, Cgs_{min},and thus set the following constraint on the memory transistor size:

$$W_n L_n > \frac{Cgs_{min}}{C_{ox}} \tag{4.30}$$

The next step is to ensure that the memory cell time constant is such that the SI circuit settles to within the desired accuracy of the overall design. Specifically, assuming a single time constant settling behavior, for an n-bit data converter one requires:

$$e^{-T_s/2\tau} < \frac{1}{2^{n+1}} \tag{4.31}$$

where Ts represents the sampling period and τ denotes the time constant given in Eq. (4.25). The resistance in Eq. (4.25) is that seen by the sampling capacitor and is dominated by the diode-connected RC transistor. With M_{mem} biased in its triode region, the resistance is given by

$$r_{in} = \frac{1}{g_m} = \frac{1}{\mu_n C_{ox}(W_n/L_n)V_t} \tag{4.32}$$

Substituting Eqs. (4.25) and (4.32) into Eq. (4.31) results in the following constraint on the size of the memory transistor:

$$\frac{W_n}{L_n} > \frac{4Cgs_{min}\ln(2^{-(n+1)})}{\mu_n C_{ox} V_t} \tag{4.33}$$

Combining this latter constraint with that of Eq. (4.30) yields the dimensions of the minimum sized memory transistor to satisfy both noise and settling concerns. These can then be substituted into Eqs. (4.27) and (4.28) to quantify the allowable range of drain currents. For maximum allowable signal swing, the bias current should be then set midway between these values:

$$Ib = (Ib_{min} + Ib_{max})/2 \tag{4.34}$$

It remains to determine the sizes of the feedback transistors in the RC cell, and bias current, I_{RC}. As previously noted, it is desired to bias the cell with V_X just slightly above Vt. With V_X = 1.1*Vt, from Figure 4.30, it is clear that this restricts the aspect ratio of M_2 to be:

$$\left(\frac{W}{L}\right)_2 = \frac{I_{RC}}{(1/2)\mu_n C_{ox} \cdot (0.1V_t)^2} \tag{4.35}$$

As explained in [64], I_{RC} is usually chosen much less than I_{BIAS} in order to decrease power dissipation and avoid parasitics from the unduly large feedback transistors.

Finally, we need to determine the allowable range of input currents we can apply to the circuit while maintaining linear operation. From signal flow graph analysis, one can determine the maximum gain from the input to integrator outputs, which we denote as G_j, where j represents the j^{th} integrator output. One must then ensure that the maximum output peak current, $G*Iin_{max}$, does not exceed the allowable current swing of $(Ib_{max}-Ib_{min})/2$. This limits the maximum input current as

$$Iin_{max} = \frac{Ib_{max} - Ib_{min}}{2 \cdot max(G_j)} \tag{4.36}$$

Note that for a ΔΣ modulator, this limit would be further restricted to satisfy stability issues. Next, we investigate two SI circuits that have been designed using the above procedure.

4.3.2 Prototype Switched-Current Filter

The filter which follows was previously designed in [65], although never successfully implemented therein. Therefore, this section will only briefly discuss the design process, and rather focus on the results obtained after implementing and fabricating the design.

The theoretical SI prototype filter has exactly the same characteristics as its SC counterpart of Section 4.2.3, chosen purposely to ease experimental comparisons. The SFG of the SI filter was first obtained by transposing that of the corresponding SC filter. As explained in [63], this allows the circuit to be easily realized in terms of SI integrator blocks, without changing the filter behavior. The resulting SI filter circuit is shown in Figure 4.32.

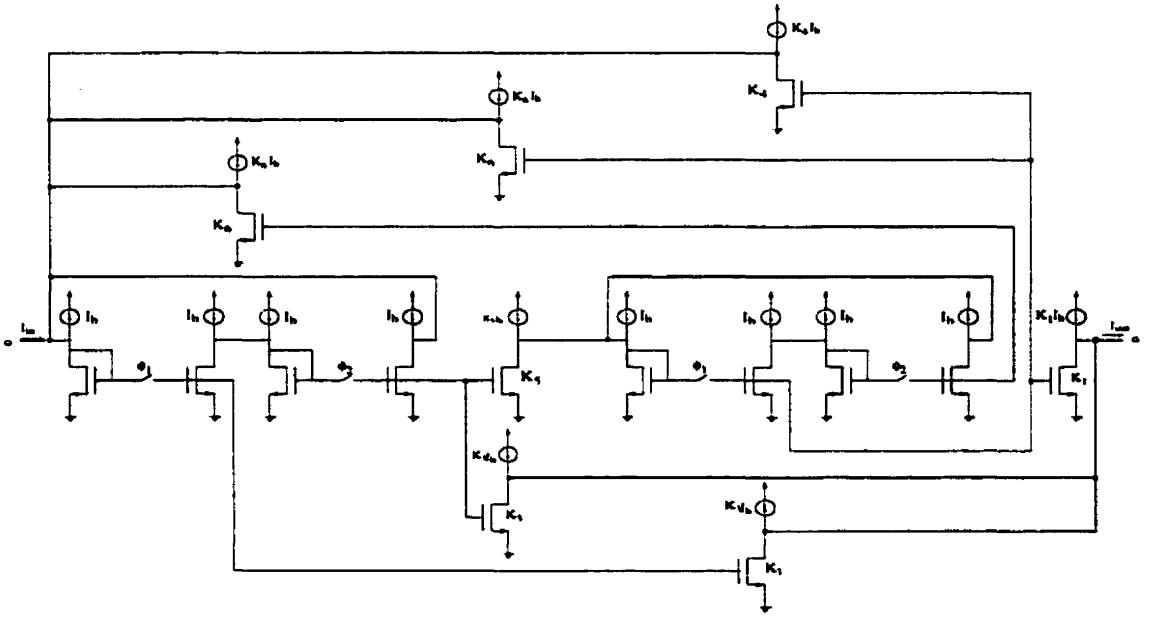
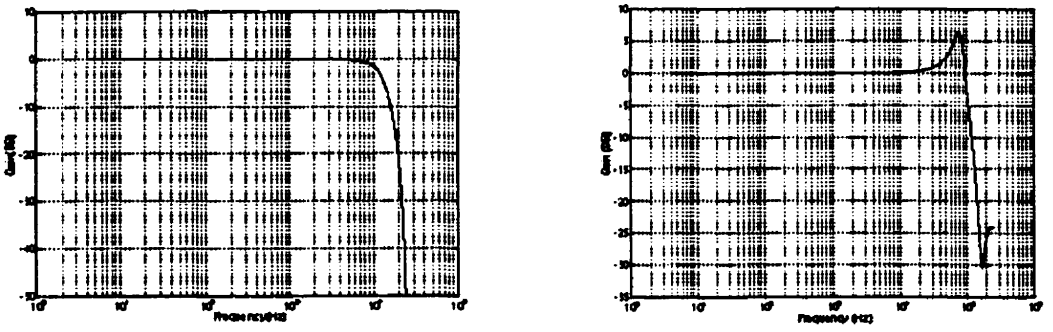


Figure 4.32: A Second-Order Lowpass SI Filter Circuit

The filter is composed of two first-generation SI integrators with feedforward (K_2, K_3) and feedback (K_4,K_6) paths clearly visible. The coefficient values are identical to those of the counterpart SC filter, detailed in Table 4.1. Each of the transistors in Figure 4.32 was implemented using a regulated-cascode composite device and the current source was realized using the design of Figure 4.31. Further detail into device sizing and current levels are explained in the work of [65], where the filter was designed.

To simulate the design, an HSPICE netlist was first extracted from the circuit layout. Next, and in-house tool, Snapper [66], was used to convert the netlist to one recognizable by WATSNAP [1][67]. This discrete-time simulator linearizes the transistors about their operating point, and deals with those intended to be used as switches as such. The results of this simulation are shown in Figure 4.33 below:



(a) fclk=50 kHz (b) fclk = 500kHz

Figure 4.33: Simulated Frequency Response of SI Filter using WATSNAP

When clocked at 500 kHz, the simulation shows a slight shift in the 3-dB frequency from the intended $f_{clk}/4$, aswell as obvious signs of Q-enhancement. In the work of [65], this was attributed to an oversimplification of the models used in sizing the memory transistors.

The above simulation approach provides a relatively fast means of simulation, without the convergence problems often encountered when using HSPICE on mixed-signal designs. However, this discrete-time simulation ignores subtle analog issues such as those related to switch design. Unfortunately, as will be seen shortly, these effects are crucial to the performance of the SI design.

After simulation, the chip was fabricated in 1.2μ CMOS process and the photomicrograph is shown in Figure 4.34 above. The filter occupies an active area of approximately 0.47 mm^2 and consumes 1.1mW of power when clocked at 500 kHz. Figure 4.35 illustrates typical measured responses of the SI filter. Referring to Figure 4.35a, for a 50 kHz clock, the

1. WATSNAP differs from Switcap2 in that it provides a greater variety of circuit elements with which to construct a network model.

filter behaves as expected, with a 3dB point at one approximately quarter the clock rate. However when clocked at 500kHz, the performance degrades considerably.

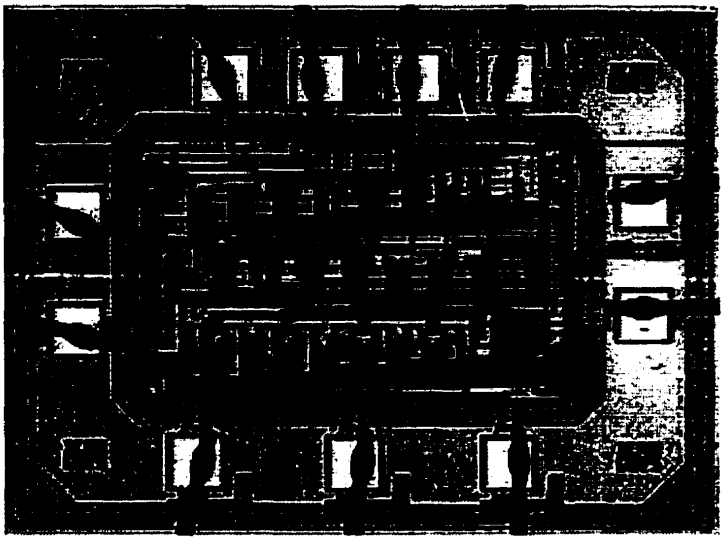
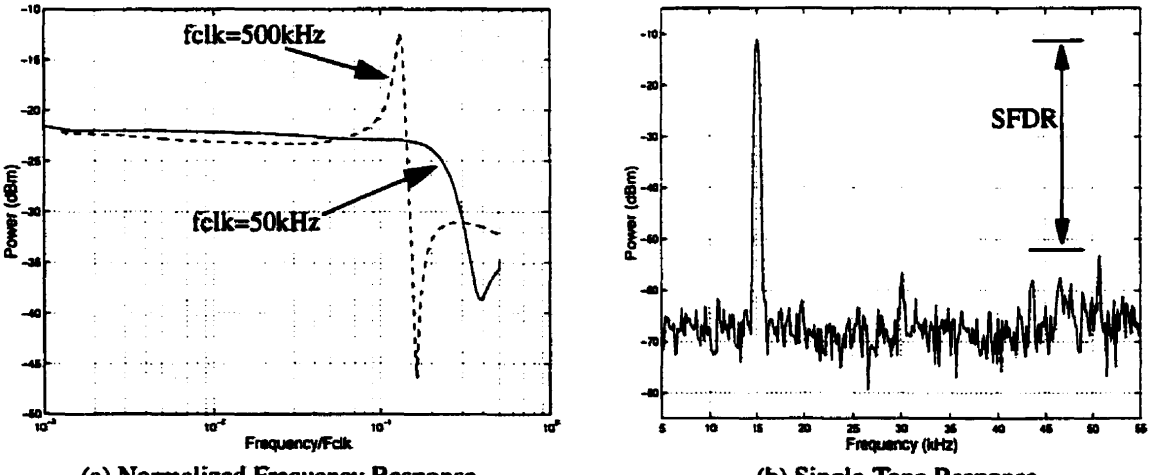


Figure 4.34: SI Filter Chip Photomicrograph

Although some Q-enhancement was detected in simulations, it was not nearly as severe. The discrepancy is thought to be due to excessively large time constants associated with the switch on resistances in the original design of [65]. Since WATSNAP replaces transistor-level switches with idealized ones, this effect was not apparent from simulation alone. Nonetheless, the filter prototype is still useful in providing insight into the distortion behavior. Specifically, at frequencies unaffected by the apparent Q-enhancement, an SFDR of 49dB was achieved for signal levels up to -10 dBm.



(a) Normalized Frequency Response (b) Single-Tone Response

Figure 4.35: SI Filter: Measured Experimental Performance

4.3.3 Prototype Switched-Current ΔΣ Modulator

Next we focus our attention on the second of the two prototype SI circuits under investigation, a second order lowpass delta-sigma modulator. The SFG-level structure of the SI modulator is shown in Figure 4.36 below.

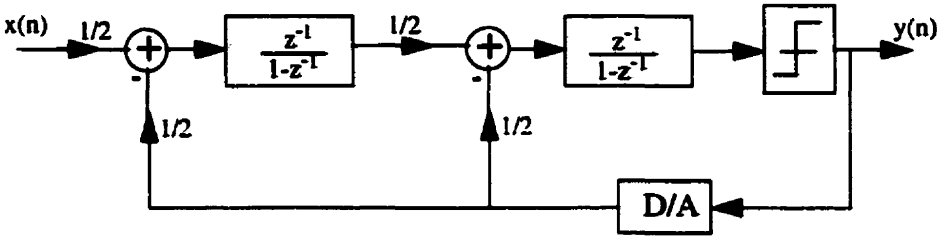


Figure 4.36: DSP-level Structure of SI Modulator

Comparing the above structure to that of Figure 4.25, we see that in order to ease comparisons, the SI modulator has been based on the same SFG-level structure as the 2nd order SC modulators previously discussed. The only difference it that the scalar gains of (1/2) have been factored out. This slight modification will not affect the NTF or STF but is necessary to allow direct implementation with SI integrator cells.

The SI integrators were implemented using the 1st-generation SI memory cells, as shown in Figure 4.29. To improve accuracy, all memory transistors were implemented using the regulated-cascode cell of Figure 4.30, and the current sources using the high-swing, double-cascode configuration of Figure 4.31. To realize the quantizer and 1-bit DAC, the transistor level implementations shown in Figure 4.37 were used. Referring to Figure 4.37(a),

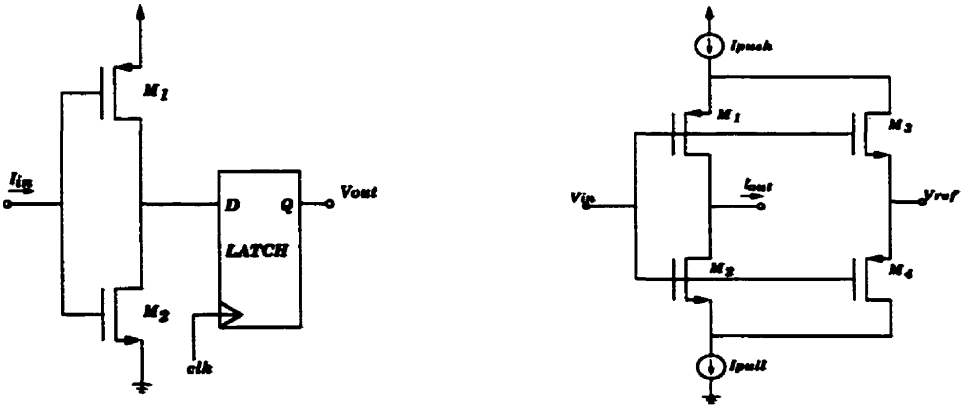


Figure 4.37: (a) Quantizer and (b) 1-bit DAC implementations

the input current to the quantizer will charge (discharge) the gate-source capacitances of M_1 and M_2 forcing the inverter output to Vss (Vdd). The voltage is then latched on the correct clock phase to ensure correct synchronization with the rest of the modulator. Referring to Figure 4.37(b), the voltage input to the DAC will turn on either M_1 or M_2 causing a current to either be pushed into or pulled from the output node. The transistors M_3 and M_4 are only used to keep the current sources in saturation when not connected to the output, thereby reducing the large current spikes that would occur during their off-on transition. The exact value of V_{ref} is not crucial, as it merely acts to provide a throw-away point for the current sources.

The overall ΔΣ modulator schematic is shown in Figure 4.38. The two integrators in the loop are clearly visible, as is the quantizer and DAC feedback currents. The switches were implemented using transmission gates, sized as explained in Chapter 3. The initial sizing of the regulated-cascode memory transistors was performed as per the procedure outlined in Section 4.3.1.

Unfortunately, despite the use of transmission gates, simulations revealed that charge injection was limiting the circuit performance. To overcome this problem, the value of the gate-source capacitance can be increased. However, in order to keep the settling time unchanged requires lowering the input resistance of the memory cell by increasing the aspect

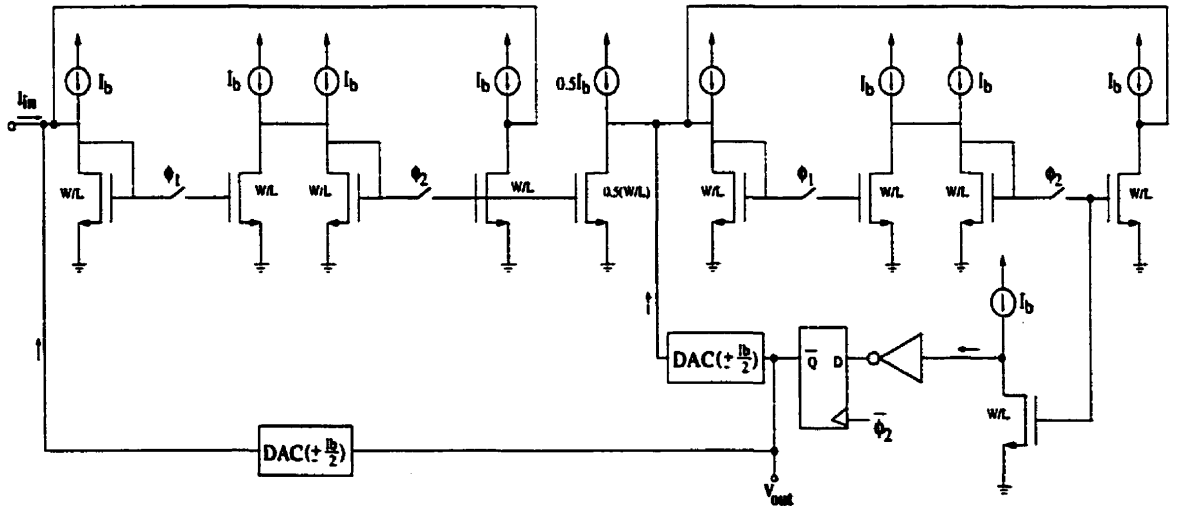


Figure 4.38: Simplified SI Delta-Sigma Modulator Schematic

ratio of the memory transistors. This in turn requires an increase in the bias current so as to keep the memory transistors biased in their triode regions (recall Eq. (4.27)). Therefore we see that charge injection can be reduced, only at the expense of increased area and power consumption.

It has already been shown[64] that approximately 9-bits of accuracy is achievable for power in the mW range. Therefore, it was decided to try to improve the performance of the SI modulator at the expense of power and area so long as they did not exceed that of its SC counterpart previously examined. An upper limit on Cgs was encountered when the time constant associated with the switch on-resistance begins to dominate the settling behavior. Increasing the memory transistor aspect ratio thereafter no longer offsets the increase in Cgs, and incomplete settling results. Table 4.4 outlines the final design values chosen to achieve the best compromise between these factors.

Unit Transistor Sizes		Nominal Current Levels	
Memory	300μm x 125μm	Memory Bias	600 μA
Reg. Cascode	125μm x 1.5μm	Reg. Cascode Bias	25 μA
DAC	5μm x 0.8μm	DAC Feedback	50 μA

Table 4.4: Nominal Design Values for SI Delta-Sigma Modulator

Before fabricating the IC, the design was simulated as best possible. We have already seen that simulation with discrete time simulators such as WATSNAP can be misleading and thus a continuous-time simulator such as SPICE is necessary to capture the full effects of transistor implementation. Unfortunately, these simulators do not handle the switching instants separately, leading to excessively long simulation times for mixed-signal designs. Moreover, when combined with the current-mode nature of the signal processing, the circuit suffers from serious DC and transient convergence problems.

In order to access the modulator performance, the SI design was implemented using the purely digital part of a 0.8μ BiCMOS process. The chip micrograph is shown in Figure 4.39 where the modulator occupies an active area of approximately 1395μm x 375μm.

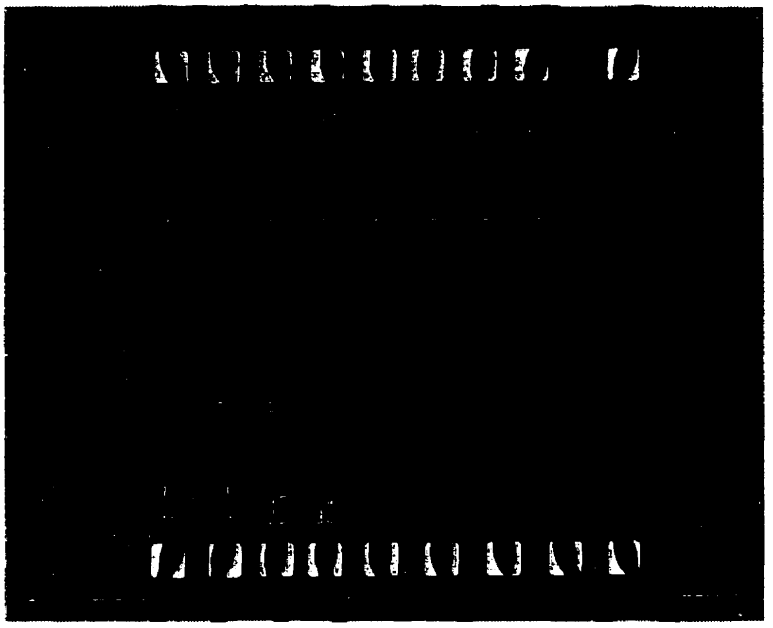


Figure 4.39: SI Delta-Sigma Modulator Chip Photomicrograph

As the modulator works in current-mode, and since the IC contains no explicit V-to-I converter itself, it was necessary to include one off-chip. Figure 4.40 below illustrates the well-known design[59] that was used, based on a negative-impedance converter(NIC).

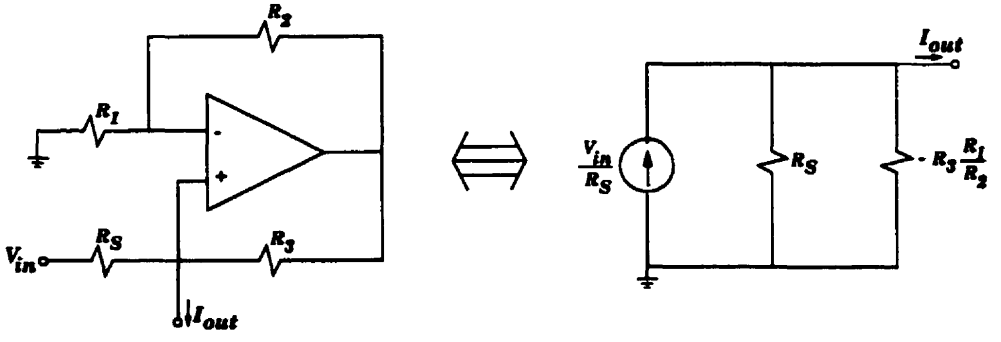
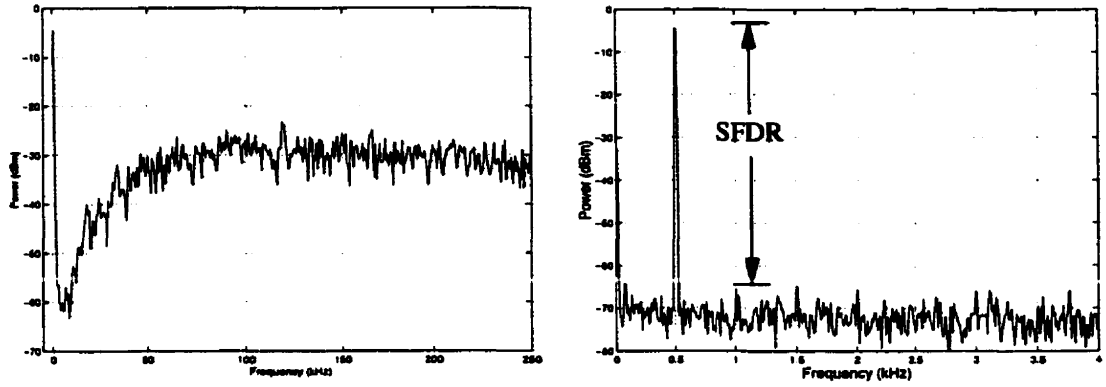


Figure 4.40: V-to-I Converter Based on a Negative-Impedance Converter

If the resistor R_S is made equal to $R_3(R_1/R_2)$, an ideal current source results. In practice, it was found that the output resistance was limited to be in range of 10 - 100 MegaOhms. Referring to Eq. (4.23), this will not impose a constraint unless the SNR is greater than 90 dB, and is therefore more than sufficient for the purposes of the modulator under test. The current signal was observed by measuring the voltage drop across a test resistor, using an opamp in the unity-gain configuration as a buffer.

Applying the current input to the modulator and operating it at a clock frequency of 500 kHz, the SI prototype has the behavior shown in Figure 4.41.



(a) Entire Nyquist Band (b) Voice-Band Zoom

Figure 4.41: Experimental Performance of SI ΔΣ Modulator

For maximum-stable input levels, the corresponding spurious-free dynamic range was found to be 62 dB. Note also that is was possible to reduce the clock rate to 256 kHz (for an OSR of 32 in the voice-band), and bias current as low as 300 μA (for a power consumption of 19 mW) without affecting the circuit performance whatsoever. Therefore, the modulator was clearly not limited by the theoretical constraint (imposed by OSR), but rather by the circuit implementation effects, such as charge injection, etc. Nevertheless, the 62 dB SFDR performance of the SI modulator is sufficient for many A/D conversion needs.

4.4 Conclusion

This chapter addressed the design of an all-CMOS data conversion system based on the delta-sigma modulation technique. The focus of the work concentrated on the two key analog components that would be most affected by the use of a purely digital CMOS process. Specifically, the construction of a sampled-data filter proceeding the reconstruction filter and of the ΔΣ modulator for use in an A/D converter were investigated.

Two entirely different circuit techniques for building each of these components without the use of traditional poly-poly capacitors were studied. The first involved the use of various configurations of non-linear MOSFET-capacitors in conjunction with the standard

switched-capacitor technique. The second approach, that of switched-currents, requires no explicit capacitors whatsoever.

In order to obtain a better understanding of the design issues involved, a prototype filter and ΔΣ modulator were implemented using each of these two approaches. The experimental results and operating conditions of the four fabricated ICs are summarized in Table 4.5.

	Prototype Filters		Prototype Modulators	
	SC, MOScaps	SI	SC, MOScaps	SI
Active Area	0.67 mm^2	0.47 mm^2	0.88 mm^2	0.52 mm^2
Supply Voltages	+/- 2.5v	0 - 5v	+/- 2.5v	0 - 5v
Clock Frequency	500 kHz	50 kHz	1 MHz	500 kHz
3-dB point / Bandwidth	137 kHz	12.5 kHz	4 kHz	4 kHz
Power Consumption	50 mW	1.1 mW	75 mW	19mW
SFDR (no bias)	32 dB	49 dB	26 - 32* dB	62 dB
SFDR (1.4 V bias)	> 72 dB	--	> 64 dB	--
*MOS-capacitor structure dependent				

Table 4.5: Summary of Experimental Results for the Four Prototype ICs

All the ICs were fabricated using only the CMOS components of a 0.8μ BiCMOS process, except the SI filter, which used a 1.2μ CMOS process. Although the SC designs operate between +/- 2.5 V supplies, they can just as easily be made to operate from a single 5 V supply, as the SI designs. Despite the fact that extremely large memory transistors were used to alleviate charge-injection problems, the SI designs still consume less power and area than their SC counterparts, as they do not require operational amplifiers.In terms of distortion, with no DC bias permitted across the MOSFET-capacitors (in low-voltage conditions, for example), the SI designs exhibit greater accuracy. However, when this constraint is removed, the SC circuits, with MOSFET-capacitors biased preferably in accumulation, out-perform those implemented with the SI technique. Moreover, one can not ignore the relative ease with which these SC circuits can be implemented, requiring only slight modification to an existing SC design.

Further pursued, both of the techniques investigated herein possess the potential of producing improved results with respect those above. For example, it has very recently been demonstrated in [51], that by using the SC technique with DC-biased composite MOS-capacitors (as discussed in Section 4.2.2), it is possible to obtain high linearity performance. Specifically, a ΔΣ modulator with distortion more than 90 dB below signal levels was reported, although further research is required to attain such performance for SC circuits in general. In terms of the SI approach, performance is also being improved. Most recently, a third-order ΔΣ modulator was reported[69] with approximately 12 bits of accuracy, although the corresponding SFDR was still limited to 63 dB. Research is currently ongoing to further enhance the linearity of the basic memory element, with the S^3I technique[70] being most recently introduced.

Again, it should be emphasized that neither of the techniques discussed in this chapter require any additional processing steps normally used in forming linear poly-poly capacitors. Therefore, regardless of their increased distortion with respect to conventional approaches, they are both highly desirable from an economic perspective. This is especially the case in the mixed-signal environments seen by the data conversion circuits investigated herein, where the majority of the IC would be occupied by digital electronics. Moreover, we have seen that the distortion performance exhibited by circuits using these techniques is more than adequate for many applications.

Chapter 5 : Conclusion

The work in this thesis was concerned with the use of delta-sigma modulation techniques to meet the present day demands placed on data converters. One issue that was addressed is the need for high-performance, high-speed A/D converters for use in wireless applications. The second issue which was explored is how $\Delta\Sigma$ data converters can be provided at low cost by using a purely digital CMOS process.

The work began by studying the basics of the $\Delta\Sigma$ modulation technique and the concept of noise shaping from both a time domain and frequency domain perspective. The $\Delta\Sigma$ approach was then further explored through the design and implementation of a second-order lowpass prototype. The voice-band design was fabricated in a 0.8μ BiCMOS process and achieved approximately 13-bits of resolution.

Once the fundamentals had been discussed, a novel eighth-order bandpass $\Delta\Sigma$ modulator was presented. The modulator design, intended for using in a digital RF receiver, was discussed beginning at the SFG level through to details of the SC implementation and layout considerations. Simulation results, highlighting the effects of process variation, were provided and the experimental performance of the modulator described. The fabricated prototype exhibits stable behavior and achieves a dynamic range of 67 dB over a 200 kHz bandwidth centered at the commonly used IF of 10.7 MHz. The work therefore demonstrates the viability of high-order single-bit bandpass delta-sigma modulation as a means of

meeting the stringent performance requirements demanded from present-day A/D converters.

To address the cost issue, the design of data conversion systems using the $\Delta\Sigma$ technique which can be fabricated in a digital process were studied. Specifically, sampled-data implementations of the $\Delta\Sigma$ modulator and filter components were studied, as these are the most affected by the lack of linear capacitors, unavailable in a digital CMOS process. One approach investigated was the use of the SC technique with MOSFETs used to implement the capacitors. The second approach was that of switched-currents, which inherently does not require external capacitors all together. In each case, a prototype IC was fabricated to better study the technique and understand the design issues involved. In general, it was noted that the SI approach requires less chip area and consumes less power, however, the design process is more complex and distortion less controlled compared to the SC counterparts. The experimental results which were discussed demonstrate that either technique could be of value depending on the intended application.

In conclusion, this thesis has provided insight into the applicability of the $\Delta\Sigma$ technique in the design of quality high speed data converters and of converters developed in a low-cost digital process.

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