A Coherent Subsampling Test System Arrangement with Amplitude and Phase Noise Measuring Capabilities

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Abstract

This thesis presents a coherent subsampling test system arrangement that can be configured to measure the amplitude response of an analog or sampled-data channel, or the instantaneous phase response of a time-based channel such as a phase-locked loop, using a sampling rate that is established based on the incoming signal bandwidth rather than the highest frequency contained in the measured signal. Such test systems are applicable to a wide range of applications from RF to optical communication systems and can be constructed using off-the-shelf components. Four coherent subsampling system will be presented, each handling a different type of input such as single-tone, multi-tone, phase-modulated signals, as well as the zero-input conditions used for making intrinsic noise measurements. Simulation results are obtained using MATLAB/Simulink and experiments are conducted on a Teradyne Flex tester to validate the proposed coherent subsampling principles.

Résumé

Cette thèse présente un ensemble cohérent de systèmes de test de sous-échantillonnage pouvant être configuré pour mesurer la réponse en amplitude d'un canal analogique ou de données échantillonnées, ou la réponse en phase instantanée d'un canal temporel, tel qu'une boucle à phase asservie, au moyen d'un taux d'échantillonnage déterminé à partir de la bande passante du signal entrant, au lieu de la plus haute fréquence contenue dans le signal mesuré. Ces systèmes de test peuvent correspondre à un vaste champ d'applications, allant des radiofréquences aux systèmes de communication optiques, et peuvent être élaborés à partir de composants courants. Quatre systèmes cohérents de sous-échantillonnage seront présentés : monovoie, multivoie, à signal en modulation de phase, ainsi que leurs mesures intrinsèques. Les résultats de ces simulations sont obtenus grâce à MATLAB/Simulink, et ces expériences sont menées sur un testeur Teradyne Flex, afin de valider la cohérence des principes de sous-échantillonnage proposés.

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List of Acronyms

ADC – Analog to Digital Converter

ASK - Amplitude Shift Keying

ATE – Automatic Test Equipment

AWG – Arbitrary Waveform Generator

BIST – Built-In Self Test

BPF – Band-Pass Filter

CP – Charge Pump

CW – Continuous Wave

DAC – Digital to Analog Converter

DFT – Design For Testability

DIG – DIGitizer

DPSK – Differential Phase Shift Keying

DSP – Digital Signal Processing

DUT – Device Under Test

FFT – Fast Fourier Transform

FPLL– Fractional Phase-Locked Loop

FSK - Frequency Shift Keying

FSR – Full Scale Range

Gbps – Gigabits per second

HF - High Frequency

IC – Integrated Circuit

IIR – Infinite Impulse Response

IMDD – Intensity Modulation/Direct Modulation

IoT – Internet of Things

LO – Local Oscillator

LPF – Low-pass Filter

ODSP – Optical Digital Signal Processing

OFDM – Orthogonal Frequency Division Multiplexing

OSNR – Optical Signal-to-Noise Ratio

PFD – Phase Frequency Detector

PLL – Phase-Locked Loop

PM - Phase Modulated

PSK – Phase Shift Keying

QAM – Quadrature Amplitude Modulation

RF – Radio Frequency

RMS – Root Mean Squared

SNR – Signal-to-Noise Ratio

Tbps – Terabits per second

TDC – Time to Digital Converter

UTP – Unit Test Period

VCDL – Voltage Controlled Delay Line

VCO – Voltage Controlled Oscillator

WDM – Wavelength Division Multiplexed

Chapter 1

Introduction

IC (integrated circuit) manufacturers produces many chips a day and Analog/Mixed-Signal testing has been used along with automatic test equipment (ATE) to test devices to verify manufactured chips working condition within designed specifications. The chips that are made in a silicon chip foundry are subject to manufacturing errors such as process defects and variations that can make two identical transistors act differently or output different results with same set of inputs. Manufactures want minimum variability; unfortunately, this cannot be guaranteed. Subsequently, component testing needs to be applied to every device that has been produced with the manufacturing process. Otherwise, bad products, or what is referred to as escapes, will end up

Figure 1.1: Early ATE which can be programmed using knobs and dials.

in the customer's hands and lead to their product failures. Secondary product failures are certainly more costly than primary IC chip failures, however, the more critical issue facing the IC vendor is its reputation for producing quality products (i.e., defect-free products). For manufactured chips to obtain the pass condition in the component testing process, it needs to pass all the test that the test engineer has setup; for example, testing with known input and comparing the measured and expected output for a go or no-go test. Hence, the test engineer plays a vital role in setting-up a rigorous test plan. However, it is impossible to test all possible inputs to ensure 100% working condition, thus, it is test engineer responsibility to propose the test plan that has the best trade-off between minimum escapes and test time.

In the early 1980's, the ATE industry introduced the ***DSP-Based Test Platform*** that was more programmable and adaptable to the ever-changing manufacturing environment. This test platform was constructed using hundreds of analog-to-digital (DACs) and digital-to-analog (ADCs) converters. Such a system construction enable the test engineer to write software programs to emulate standard bench-top instruments. This significantly increased the versatility

of the ATE. Moreover, through clever mathematical techniques, such an approach provided a means to make accurate measurements in near-minimum test time. To understand the test technology, prior to this development, ATE was constructed using specialized hardware configurations with knobs and dials to set the appropriate test conditions and limits. Figure 1.1 is an illustration of one of these old electronic testers for testing radio circuits made by Precision Apparatus Company. On the left side is a set of sockets where the device-under-test is insert for subsequent testing.

The conversion resolution of data converters in the early eighties were limited to about 12 bits and this increased slowly according to [1] by approximately 1.5 bits over an eight-year time-span from the late eighties to about 1997. Today we are seeing data converters in the consumer market that have resolutions as high as 24 bits.; low noise 24 bit ADC, such as ADS 1231 is available by Texas instrument in the market. These are being used in a multitude of products and systems, from instrumentation, to portable personal devices like tablets and smart phones, to the equipment used create the infrastructure behind cloud computing and storage, and the internet-of-things (IoT).

Today's digital and optical communication technology is operating at extremely high data rates, in excess of 100 Gbps in advanced fiber optic channels, and these rates are expected to increase even further in the very near future. As these data rates exceed the present day operating limits of existing data converters, traditional ATE and DSP techniques will not be adequate to meet the needs for testing optical data communication systems. The main reason is due to the Nyquist-Shannon sampling theorem which states that the sampling rate must be greater than twice the highest frequency contained in the incoming signal, and that these frequencies are approaching 100's, if not 1000's of GHz. According to [2], there are future challenges that needs to be solved

before high data rates can be realized. Such challenges includes, high-speed ADC and DSP, tunable narrow bandwidth local oscillator, and fiber non-linearity. Before we present the solution to such challenges, we would first like to present some background information about present-day optical data communication systems and the main system performance metric called phase noise.

1.1 Optical Digital Communication Systems

This section will explain the background of optical communication by looking at various technologies and techniques that have been used to overcome challenges that optical communication industry have faced and are facing today. This section will help the reader to understand the needs for accurate test measurements method at low costs for very high-speed circuits that are being used in optical communication systems.

Network traffic has been growing rapidly since the personal computer has been introduced and it has been growing even further by the introduction of smartphones where consumers can connect to the network from anywhere and at any time. From Figure 1.2, we can observe that the demand for bandwidth increased exponentially from 2001 to 2011, for both developing and developed countries. Developing countries demand for bandwidth is slowly increasing compare to a developed country, but the trend will soon to be increasing rapidly as the more affordable hand-held devices are pushed into this market. In 1948, C. Shannon introduced the term *capacity of a channel* [3]. Shannon capacity describes the asymptote of the rate of transmission that is possible with arbitrarily low error rate. Such capacity is no more than a signal-to-noise ratio (SNR) where signal quality will degrade for long-haul transmissions; one of the reason for this degradation is due to the nonlinearity of the fiber channel. For the most part, optical communication research sets out to identify how to maximize the SNR between the transmitter and receiver. In the early eighties,

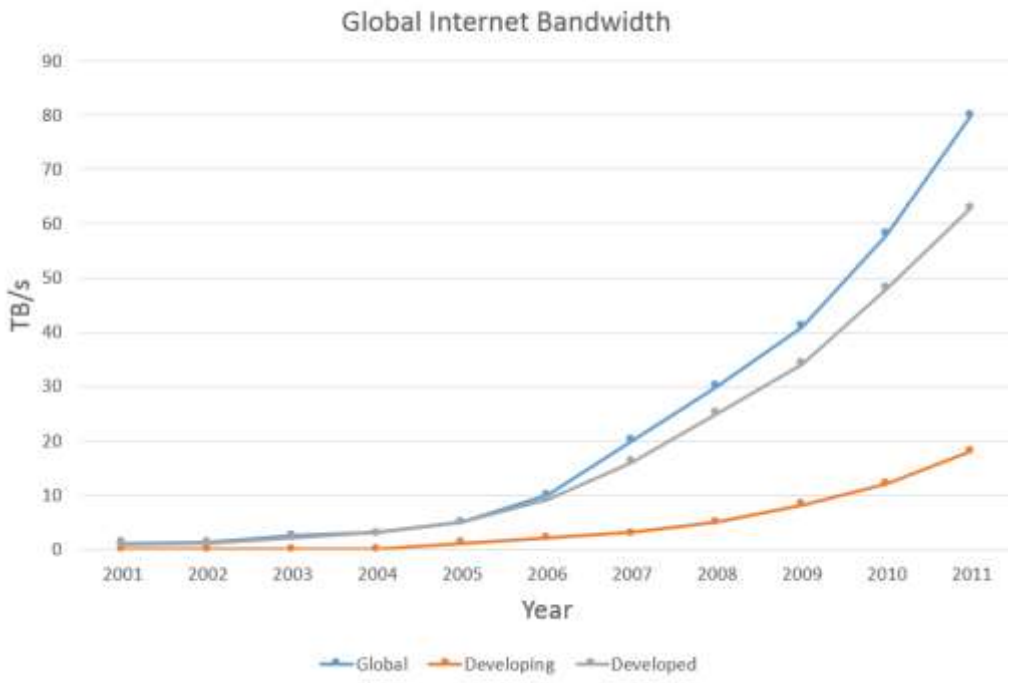

Figure 1.2: Global bandwidth demands [5]**.**

the concept of a coherent optical transmission system was introduced; Coherent optical transmission is a technique that uses a modulation of amplitude, phase, and polarization to transmit information through fiber optics. Such a system relied heavily on the use of digital signal processing (DSP). However, at the time, this was simply too expense to deploy and the fact that the existing paradigm involving wavelength division multiplexed (WDM) systems provided ample capacity at the time. Today, though, with the advancement of CMOS IC technology DSP technology is widely available. Thus, coherent optical systems are now widely deployed in the development of the internet communication networks and the corresponding cloud technologies. Coherent optical fiber technology has become the main driver of high-speed data transmission in excess of 100 Gbps, as it enables more effective modulation schemes, such as M-ary phase shift keying (PSK) and quadrature amplitude modulation (QAM) [2].

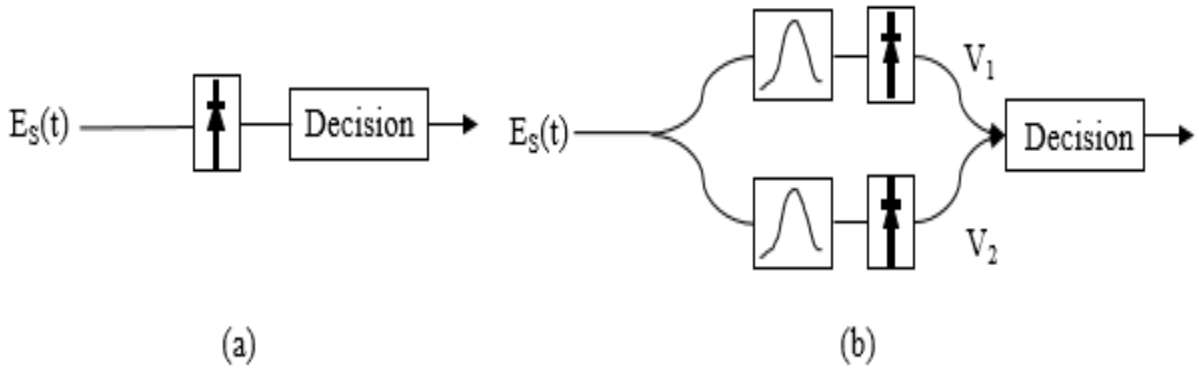

Figure 1.3: Non-coherent receivers: (a) ASK, and (b) FSK.

Optical transmission development started with intensity modulation/direct modulation (IMDD) which reached data rates as high as 10 Gbps. This was changed to a differential shift keying (DPSK) modulation method which enabled data transfer speeds as high as 40 Gbps. To reach even higher speeds, coherent detection with optical digital signal processing (ODSP) was introduced [4]. Currently, 100 and 400 Gbps coherent detection transceivers are deployed across the globe. Without coherent detection and ODSP, data rates over 100 Gbps would not had been possible. ODSP corrects for the chromatic dispersion, polarization rotation, polarization-mode dispersion, and fiber nonlinear impairments that arise from the fiber. Fiber dispersion is the major source of timing jitter in an optical communication link; timing jitter depends on the link length and one of the ways to correct the errors from the optical dispersion, is to compensate in the electrical domain after the photo-detector [5].

Take a look at few receiver configurations along with its modulation formats. In Figure 1.3, two non-coherent detection method are illustrated. In part (a), an amplitude shift keying (ASK) detection method is shown. Here optical signals are converted to electrical signals using the photo-detectors and a decision is made using an electrical signal rather than using an optical signal. In

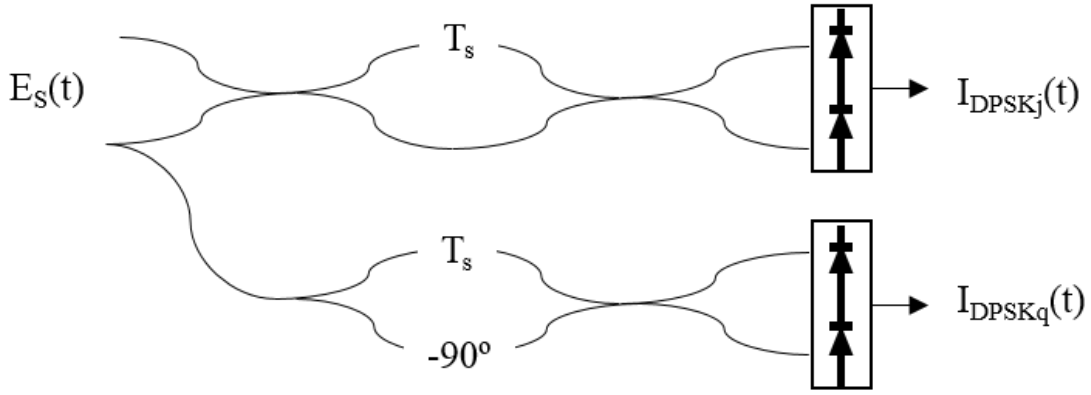

Figure 1.4: Differential coherent phase detection of M-DPSK.

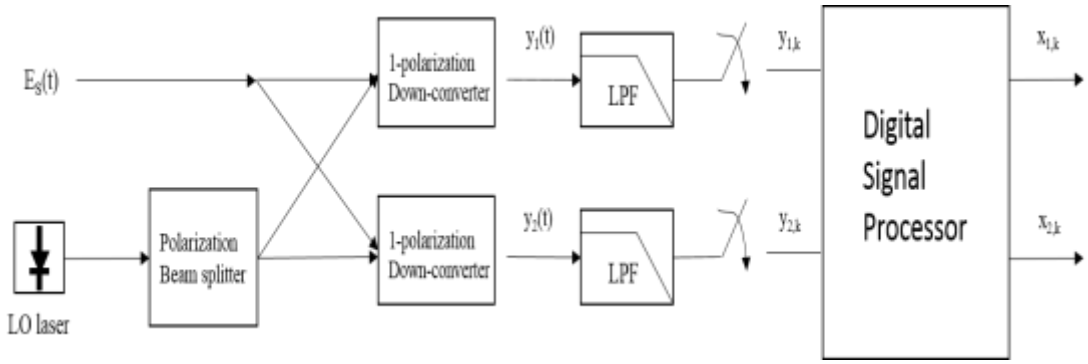

Figure 1.5: Coherent receiver system implementation.

part (b) of Figure 1.3, illustrates the detection method using binary frequency shift keying (FSK). Here the process is similar to ASK, but the difference is that further signal manipulation takes place in the optical domain. Specifically, the optical signal is split then band-pass filtered to remove any noise that can degrade the purity of the optical signal. A decision is then made by measuring the signal energy at the receiver [6].

In contrast, the differential coherent receiver shown in Figure 1.4 uses a differential phase shift keying (DPSK) technique. Here $E_S(t)$ is the received signal and T_S represents the delay symbol period; only one received signal, $E_S(t)$, exist and this received signal undergoes two different routes, where one route has no phase shift while the other route has -90°. In a differential coherent detection, the receiver makes a decision based on the phase difference between the symbol of interest and a reference symbol. The reference symbol is provided by the previous symbol. In other words, without the information of previous symbol phase, current symbol phase cannot be determined.

A coherent receiver implementation is illustrated in Figure 1.5. Here, a coherent receiver receives the transmitted signal, $E_S(t)$, and a 1-polarizaiton down-converter recovers the baseband modulated signal. This signal is then passed through a low-pass filter to attenuate the unwanted signal power. Afterwards, DSP is used to extract the *k-th* transmitted symbol x_k. For coherent detection, it takes the product of the modulated light signal along with the output from a continuous wave local oscillator (LO) to transmit the information from point A to B. In this system, a coherent detection system makes a decision by recovering both the amplitude and phase information of the full electric field that is received from the light signal. As the coherent receivers needs the information of the carrier phase, the received signal is demodulated using the LO which serves as a reference phase.

Using coherent detection, more complex modulation schemes can be used, such as the orthogonal frequency division multiplexing (OFDM) scheme which uses a set of carriers instead of a system consisting of a single carrier one using another format, such as frequency division multiplexing (FDM). OFDM is a popular modulation format for long-haul and wireless communication applications [7]. OFDM can transmit a much larger amount of data as a single

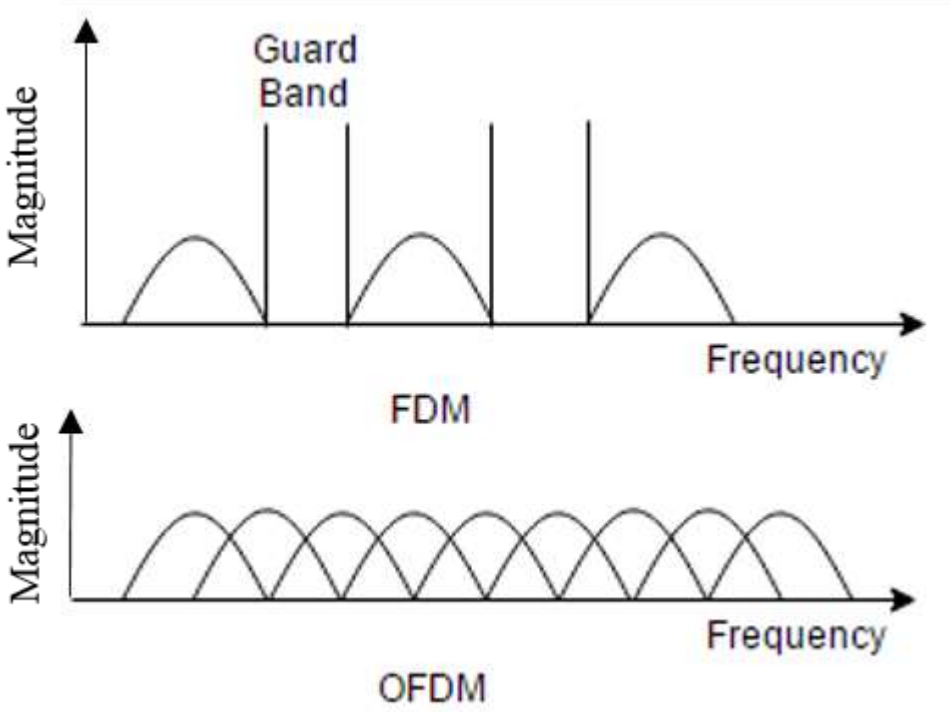

Figure 1.6: Difference between FDM versus OFDM.

carrier system and can be designed to meet a wide range of system requirements, such as bandwidth efficiency, performance, spectrum shaping, and sensitivity to various impairments [8]. The advantage of using OFDM over FDM can be seen from Figure 1.6. To avoid frequency leakage effects, guard bands are required between adjacent frequency bands in a FDM signal, as shown in the upper diagram of Figure 1.6. This reduces the amount of bandwidth available to transmit data and lowers data throughput. In contrast, for the OFDM situation depicted in the lower diagram of Figure 1.6, signal information can overlap adjacent bands, as the signal information can be recovered using the orthogonality principle. Thus, utilizing the available bandwidth more efficiently.

QAM (Quadrature Amplitude Modulation) is another widely-used modulation format and according to [9], has reached a maximum capacity of 101.7 Tbps. In this format, two carrier signals are set at the same frequency but separated in phase by 90°. At the receiver end, these signals are separated and the data is extracted; one signal can be represented as a sine-wave and the other as a cosine-wave. An example of a QAM constellation consisting of 128 points is shown in Figure 1.7. The constellation diagram is a representation of maximum number of possible symbols that the modulation scheme can choose in the complex plane. Hence, with higher order, more bits per symbol can be carried, resulting in higher data rate. It is worth noting that a QAM scheme can use a more complex constellation. However, a large constellation sets require larger amount of optical power. For example, doubling the size of the constellation increases the SNR of the optical system by two orders of magnitude. Such an increase is impractical over large distances due to the nonlinear effects of the optical fiber [10]. Therefore, increasing the constellation points to increase the data rate is not desirable as it needs impractical levels of optical SNR. Meanwhile, increasing the carrier frequency to increase the size of the constellation set introduces a new set of challenges. One such challenge is the need for data converters with high resolution and fast sampling rates. The coherent subsampling principle that is proposed in this thesis will go a long way at solving the problem of high resolution - high sampling rates by removing the need for high sampling rates in the data conversion operation encountered in the equipment used during test. One type of test that will figure prominent in this thesis is the measurement of phase noise.

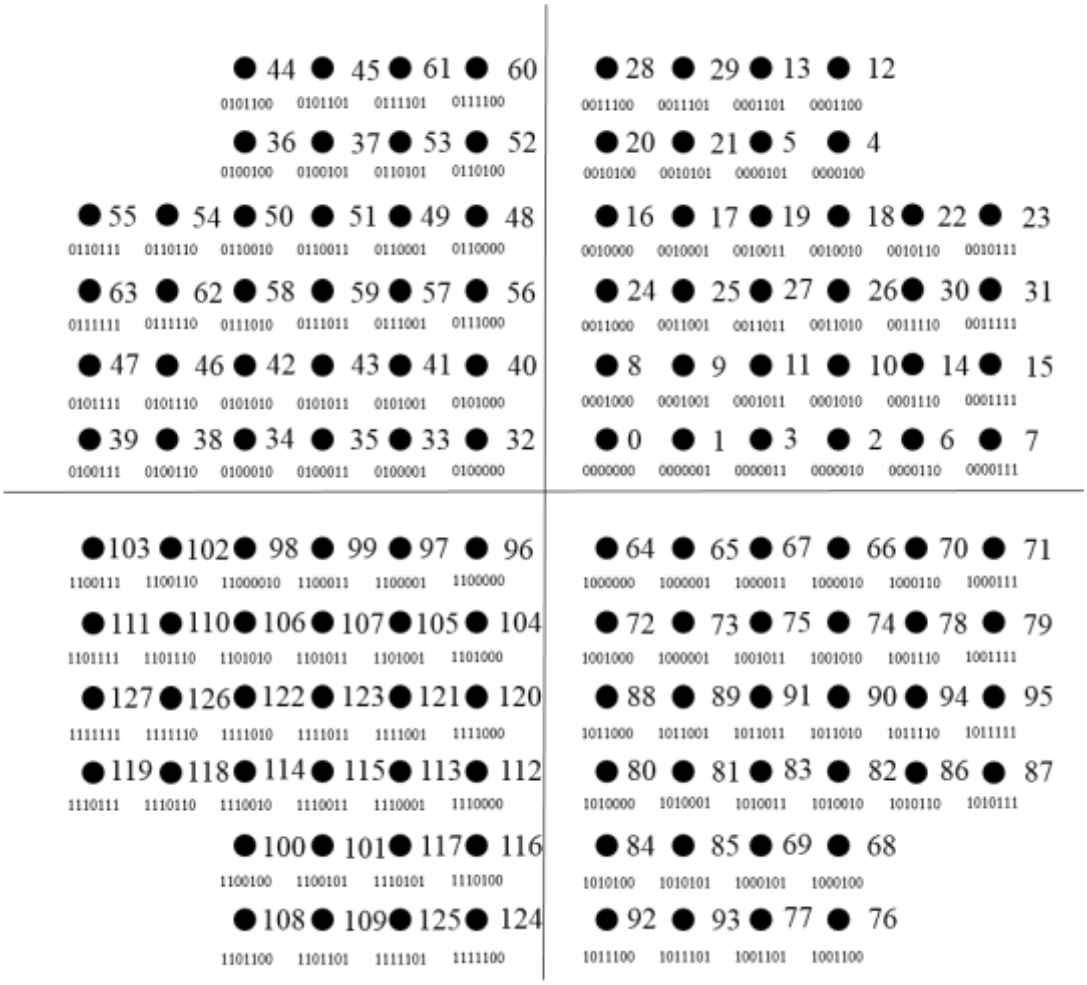

Figure 1.7: Illustrating the 128-QAM constellation points.

1.2 Phase Noise Measurement Methods

A phase noise measurement collect information about the random phase shifts that occurs within a periodic signal. Figure 1.8 attempts to illustrate these timing errors by comparing the low-to-high transition time between two step-like signals called ideal and actual. The yellow shaded area on the actual signal signify the magnitude of this phase error. Here, one can observe the random phase shifts that are occurring in the actual signal. These random phase errors are caused

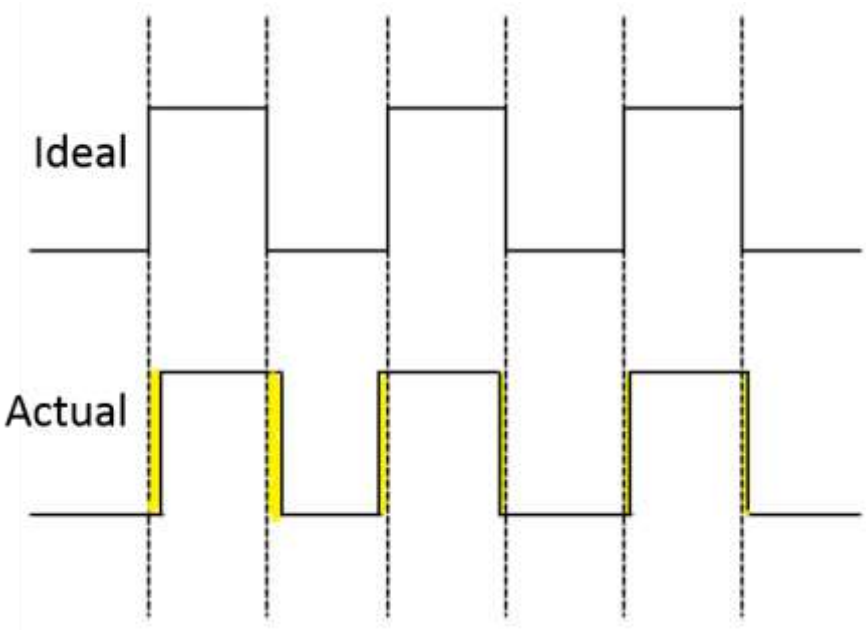

Figure 1.8: Illustrating the timing errors (highlighted in yellow) which is referred as phase noise.

by internal thermal noise effects and external environment conditions like steady voltage supply level variations, temperature changes, etc.. In reality, phase noises are inevitable and cannot be completely removed, but can be minimized by selecting the appropriate circuit topology.

The most direct way to obtain phase noise information from a periodic signal like a sine-wave or clock is to use spectrum analyzer and observe the corresponding frequency-domain characteristic [11]. Figure 1.9 describes the basic diagram of spectrum analyzer where the input signal is first low-pass filtered to attenuate unwanted frequency components. After the input filter, the signal is mixed with a local oscillator. The signal then passes through the filter labelled "resolution bandwidth filter" and subsequently is amplified and compressed in a logarithmic way; the bandwidth of the "resolution bandwidth filter" is controllable by the user to increase the accuracy of the result. The signal is then rectified and again further filtered with video filter. Lastly,

the signal is captured with an ADC and DSP is applied to calculate the amount of phase noise that is residing in the test signal.

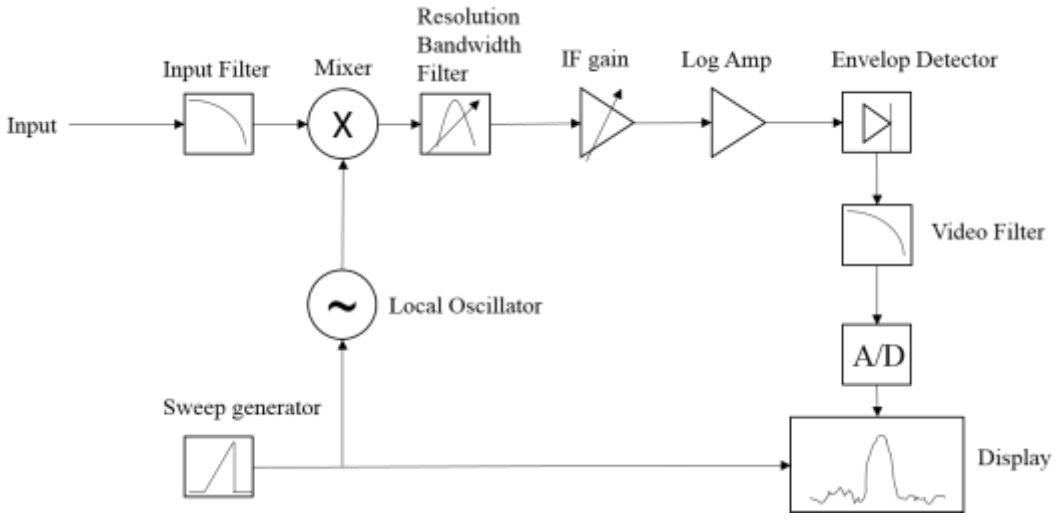

Figure 1.9: Diagram of spectrum analyzer.

The Figure 1.10 illustrates a typical frequency-domain characteristic of a sine-wave. Here the power of the signal is centered at f_c and has power dispersed about its sides. The units of power is expressed in dBm. If the sinusoidal signal were ideal, then the power of the signal would appear as a sharp tone (much like an impulse) centered at f_c; it would not have any sideband power. It is the presence of this power dispersion about f_c that introduces phase noise. Phase noise at a frequency offset Δf from the carrier frequency is denoted by the symbol $\pounds(\Delta f)$. It is expressed in dBc/Hz when normalized with respect to the carrier power and spectrum analyzer bandwidth BW, i.e.,

$$\pounds(\Delta f)[dBc/Hz] = P_{SSB,offset}[dBm] - P_{carrier}[dBm] - 10\log(BW) \quad (1.1)$$

where $P_{SSB,offset}$ is the power level offset by Δf from the carrier, $P_{carrier}$ is power of the carrier, and BW is the resolution bandwidth of the spectrum analyzer. Note that the measurement variability can be reduced by capturing multiple time window frames and averaging the results. Result of

the phase noise plot is shown in Figure 1.11. From the phase noise plot, the RMS quantity in radians can be found by integrating over some frequency range as

$$\sigma_{\emptyset}|_{rad} = \sqrt{2\int_{f1}^{f3} £(\Delta f)\mathrm{d}\Delta f} \tag{1.2}$$

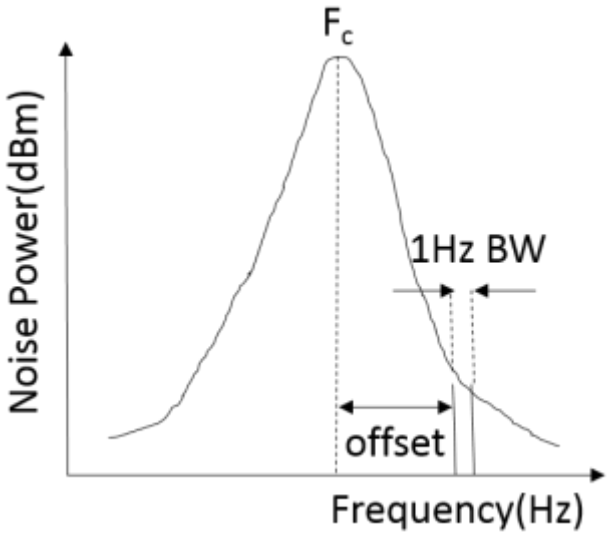

Figure 1.10: Illustrating the phase noise that is offset from the carrier, FC.

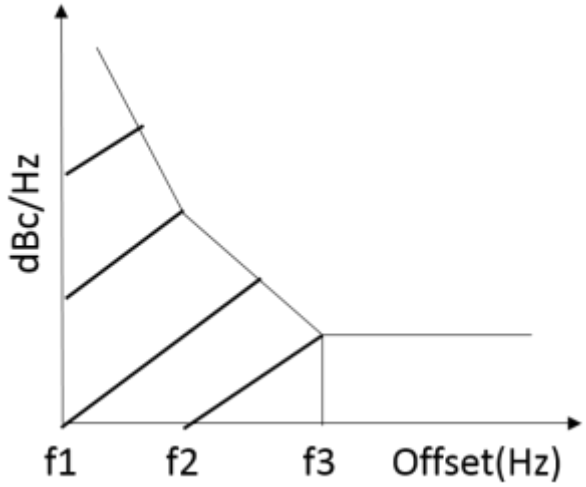

Figure 1.11: Illustrating the phase noise plot in units of dBc/Hz vs. offset from the carrier.

Another way to measure the phase noise associated with a digital signal is to use sampling involving a time-to-digital converter (TDC), filter, and peak detection block [12], which is illustrated on the Figure 1.12. This method uses an all-digital method where the cost of implementation is kept to a minimum. The TDC is used to measure a zero-crossing point of an incoming signal while the infinite impulse response (IIR) filter is used to emulate a one-point DFT operation. By using an IIR filter, it eliminates the needs for storing the whole waveform before the calculation can be processed.

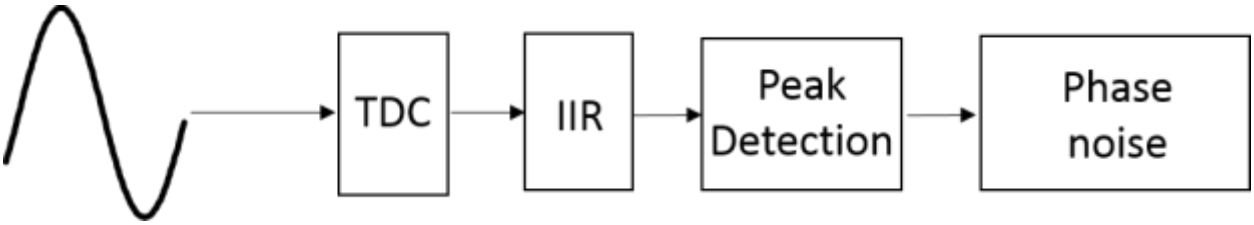

Figure 1.12: Phase noise measurement method using TDC.

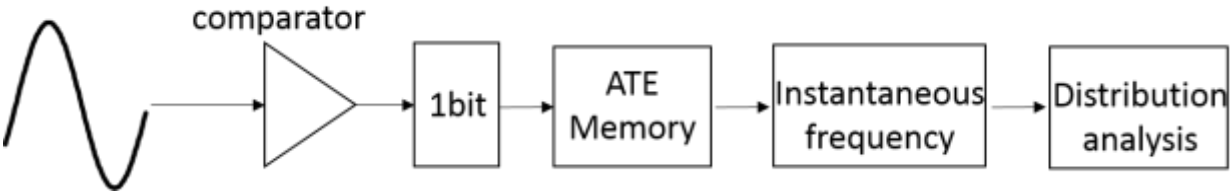

Figure 1.13: Illustrating the phase noise testing using comparator and DSP technique, such as computing instantaneous frequency and analyzing the distributions.

Similarly, using the inverse of the time between each zero-crossing (equivalent to the instantaneous frequency) of the incoming signal provides another way to extract its phase noise [13]. Such a test system is illustrated in Figure 1.13. Here the incoming signal is oversampled using the front-end comparator and the output is converted to a 1-bit digital signal. Subsequently, the bit stream is analyzed using DSP techniques. An analysis of the zero-crossings of the corresponding digital signal is used to determine the instantaneous frequency of the incoming

signal. In the case of an ideal sine-wave without phase noise, the same zero-crossing will occur periodically, whereas the incoming signal with phase noise will have different zero-crossing points.

Two methods to measure a phase noise that has been explained previously are all based on off-chip measurements using ATE instruments. These instruments can have high initial costs and its size are large with large parasitic, and cannot be used out in the field to test the device in system operation. Hence, many researchers have been exploring an on-chip solution for phase noise measurements. Figure 1.14 illustrates a test setup where a low-noise voltage-controlled delay line (VCDL) and mixer is used to extract the phase noise information in the baseband [14]. Here, the system uses a VCDL along with a mixer that mixes a delayed clock along with system input. After the mixer, the signal passes through a low pass filter (LPF) and is then amplified using a low-noise amplifier. Once the signal has been amplified, the signal is digitized and DSP performed to extract the phase noise. This measurement technique is similar to what a bench-top equipment uses to measure the jitter of a system with a spectrum analyzer; spectrum analyzer uses sampled data and apply an FFT on the captured data and uses these results to calculate the phase noise associated with the signal. A programmable phase-frequency detector (PFD), charge pump (CP), and delay-line can also be used to perform an on-chip phase-noise/jitter measurement [15]. Both [14] and [15] do not requires an external reference clock, which reduces the overhead of the chip design. In this techniques, rather than using an external reference clock, it uses a delayed version of the clock to extract the jitter using accumulated period jitter.

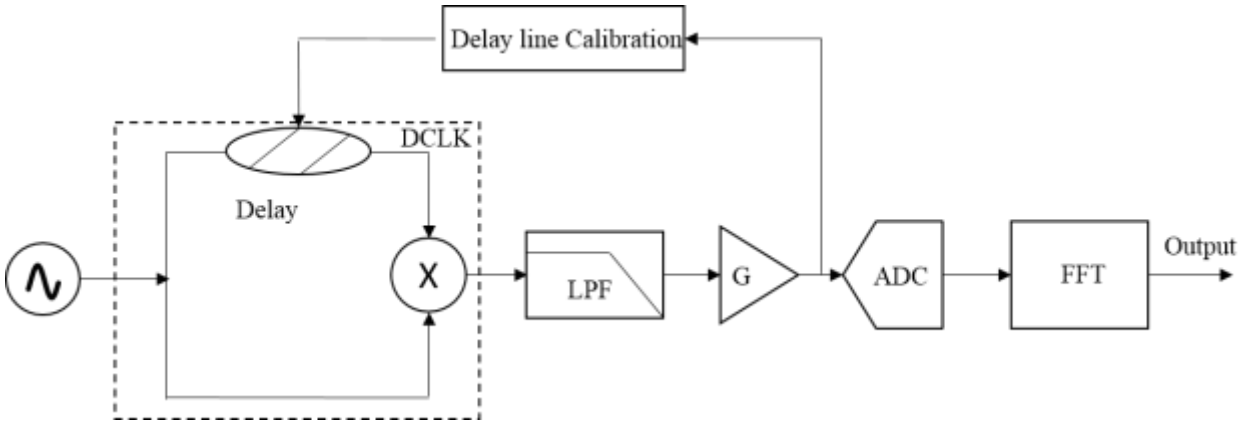

Figure 1.14: Phase noise measurement using VCDL and mixer.

Opposed to using a delayed version of the clock, an additional external reference can be used to design an on-chip solution of the phase noise measurement capabilities. A reference clock is used to sample its timing jitter of the DUT and convert it to a voltage signal using a PLL, or delay lines and phase interpolators, which reference [16] refers to as jitter measurement macro. With the converted voltage signal, the power spectral density expressed in V^2/Hz can be used to extract the jitter spectrum in rad^2/Hz.

Another on-chip measurement technique is shown in Figure 1.15 where it uses a reference and measured signal which passes through a 4-phase clock generator along with micro-measurement macro. Micro measurement macro suppresses the noise such as quantization noise, thermal noise, and process variation by using oversampling, delay line, and feed-forward calibration [17]. Note that the micro measurement macro are being controlled by the oversampling-rate controller to achieve the required resolution of the measurement. For any of the designs that uses a PLL for the phase noise measurement setup, such as Figure 1.14 and Figure 1.15, can be further improved by using a self-calibration feature to improve the accuracy of its measurements [18]. By using a BIST technique, to measure and correct for phase errors, it enables the low noise designs that can further improve the noises from the process variations.

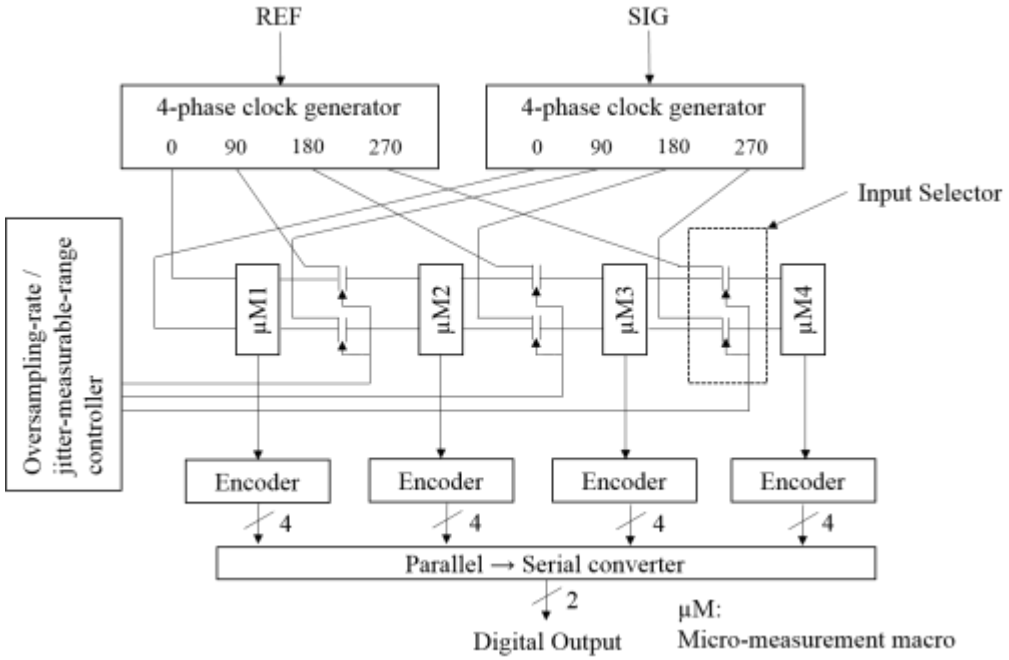

Figure 1.15: Jitter measurement using four phase interpolated clock and oversampling.

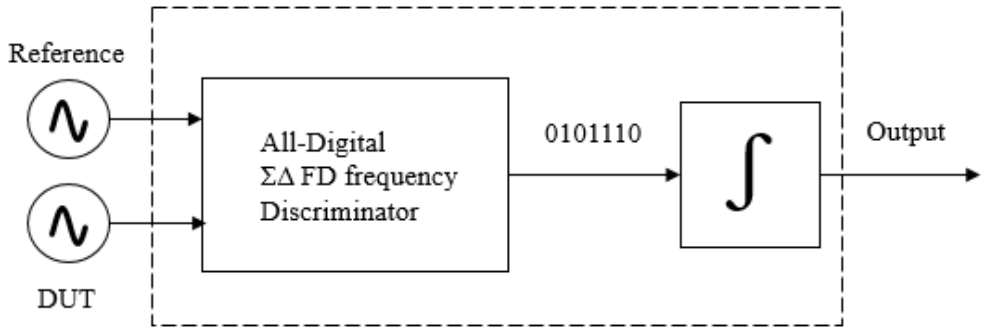

Figure 1.16: Illustrating all digital phase noise measurement method.

An all-digital solution is also available to measure a phase noise using the *ΣΔFD* discriminator proposed in [19] is shown in Figure 1.16. Using the *ΣΔFD* discriminator, it extracts the signal from the DUT and compares it to a reference signal, which then produces a digital bit

stream whose average value contains the average frequency error between the DUT signal and the reference signal [20]. A digital filter that follows the *ΣΔFD* discriminator will reveal the corresponding phase noise of the DUT.

1.3 Motivation

The cost of test for mixed signal devices is dominated by the costs associated with analog testing. It has been estimated that the cost of analog test can be as high as 50 percent of the total cost to manufacture a device [21] where current and future costs trends between manufacturing, analog test, and digital test are shown in Figure 1.17. Manufactures are eager to reduce the cost of test and they might take a route where less tests are performed. However, it is well known in the industry that such an approach will simply pass-on more test costs to the buyer by increasing the amount of wasted product, as well defocusing the engineering teams on delivering value to their

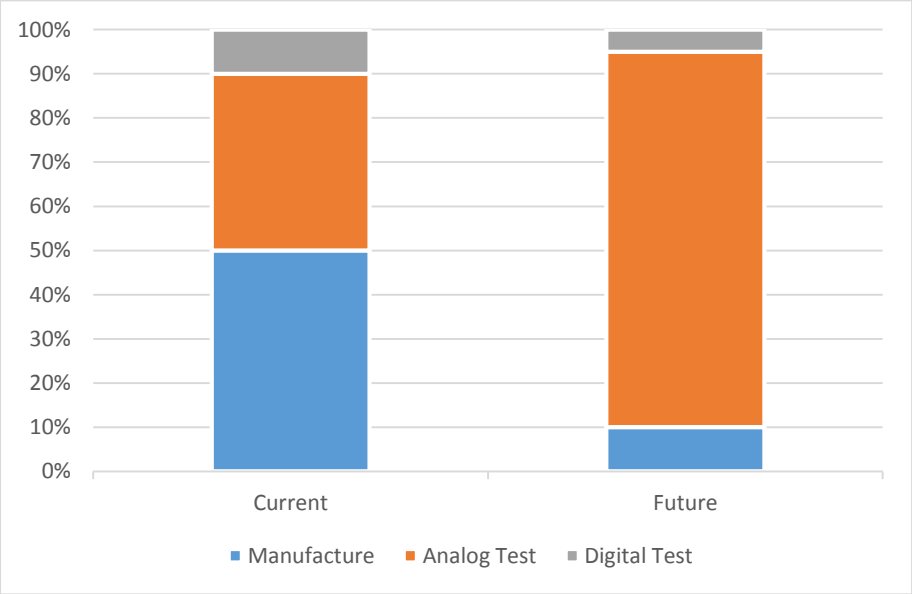

Figure 1.17: Current and Future trend in Manufacturing costs of a device *[21]*.

employer by wasting more time of customer support.

One approach to reduce the cost of test is to make use of various Design-For-Test (DFT) and/or Built-In Self-Test (BIST) strategies. DFT is a methodology where test engineers make a test plan at the beginning of the design cycle and influence the present IC design or manufacturing system, so as to reduce the overall test costs. The DFT engineer may suggest a BIST solution whereby a virtual test instrument is incorporated directly in to the IC. BIST, if executed correctly, can provide improved test times, more accurate measurements and simpler ATE interfacing [22], [23].

As it has been mentioned before, the demand for higher bandwidth and data rates is ever increasing and this presents new test challenges to those products that are incorporated into such systems, e.g., optical digital communications. In point of view of testing, higher data rates generally require very expense bench-top equipment to be incorporated into the ATE in a sub-optimum manner. One where the sources and data capture measurement processes must operate in a non-coherent manner. As a result, the test times are long – not only from the measurement perspective but also from a data transfer perspective. Instead, a coherent sampling system has proven itself to be an extremely flexible test system that can approach near-minimum test times. Unfortunately, for high-speed digital and optical communication systems, the sampling rates exceed all possible data converter technology known to exist today. It is therefore the objective of this thesis to demonstrate that a ***coherent subsampling system*** can perform similar measurements as a coherent sampling system but with existing data converter technology. In fact, using off-the-shelf products that are available in large quantities and at low cost. As the reader will soon see, the trade-off will be longer test times.

1.4 Thesis Outline

In this thesis, a coherent subsampling method will be presented whereby the sampling rate is determined based on the desired signal bandwidth instead of the highest frequency contained in the signal, allowing for a much lower sampling rate. Such a test system is relatively inexpensive to construct and can be built today using off-the-shelf components. One of the objectives of this thesis is to identify the sampling conditions for a subsampling process that is synchronized with the incoming test signal, herein referred to as a coherent subsampling system. Another objective of this work is to demonstrate how such a test system can be used to measure a wide range of analog and sampled channels using single-tone and multi-tone signals, and channels that require phase-modulation (PM) type test signals, such as phase-locked loop and delay-locked loops.

This thesis is organized as follows: **Chapter 2** will explain the coherent system and its advantages over non-coherent sampling systems, as well as coherency conditions and constraints that needs to be met, in order to eliminate any intermodulation signal masking and amplitude peaks in the signal.

Chapter 3 describes a new proposal of the general sampling considerations for a system to be coherent when subject to subsampling; this will include signal conditions for single-tone, multi-tone, and phase-modulated signals, and systems undergoing a noise measurement with no external excitation signal.

Chapter 4 presents subsampling techniques that can be used to measure the intrinsic voltage and phase noise of a DUT. The method involves converting the subsampled data set into an analytic signal using a Hilbert transform then extracting its instantaneous phase, which is the background we rely on to extract the phase noise of the DUT.

Chapter 5 will provide the circuit used to create the sampling clocks of the coherent subsampling system. In addition, a brief look at the time and frequency resolution of a coherent subsampling system will be provided, together with a look at the impact of an ADC finite resolution on a measurement.

Chapter 6 will provide a detailed summary of the MATLAB/Simulink simulation results and the ability of the coherent subsampling system to make accurate measurements. Some system limitations such as ADC resolution will be investigated in this chapter.

Chapter 7 will provide experimental measurement results using a Teradyne Flex ATE and bench-top equipment. The results will confirm the theory presented in this dissertation.

Finally, **Chapter 8** will provide a summary of the conclusions.

Chapter 2

A Coherent Sampling System: Review

The previous chapter explain why the application of coherency became the break-through technique for present-day optical communication systems. In this chapter, we will first explain the importance of coherent sampling by looking at the problem of the non-coherent sampling approach. This will be presented in the context of the measurement accuracy of an RMS meter when subject to a sine-wave of with arbitrary frequency. The basics of sampling and reconstruction of a signal will be presented. This will lead to the constraints on using a coherent sampling approach for both single and multi-tone signals as first developed by M. Mahoney [24].

2.1 Needs for Coherency

As stated in Chapter 1, the revolution in the testing industry was when ATE manufactures moved from an analog-based approach to one involving the use of platform consisting of hundreds of data converters (i.e., analog-to-digital and digital-to-analog converters). By doing so, digital signal processing (DSP) could be used to process measurement information.

One of the drawback of analog testing approach was its long test time. This stems from the fact that the signal source and measurement instrument are independent of one another, i.e., unsynchronized, or in the context of this thesis, referred to as non-coherent. To appreciate this fact, consider the role of a RMS voltmeter. The RMS value of a signal *x(t)* is defined according to the following integral equation,

$$X_{RMS} = \sqrt{\frac{1}{T_2 - T_1}\int_{T_1}^{T_2} |x(t)|^2 \, dt} \tag{2.1}$$

where X_{RMS} is defined over an interval of $T1 \leq t \leq T2$. If x(t) is a sine-wave with period that is a non-integer multiple of *T2* - *T1* then the RMS value will not be the correct value as depicted in Figure 2.1 for a sine wave that completes only 1.5 cycles over the time interval *T2* - *T1*. Although multiple measurement will converge to a correct RMS value, but the downside of such a measurement is long test time. However, if the period of the signal is an integer multiple of *T2* - *T1* then the RMS value is exact. The later situation is depicted in Figure 2.2 for a sine-wave that completes two complete cycles. This example highlights the advantage of a non-coherent sampling system to one that is coherent.

In next section, we will discuss the basics of sampling and reconstruction. This is important to understand the principles of a coherent subsampling system.

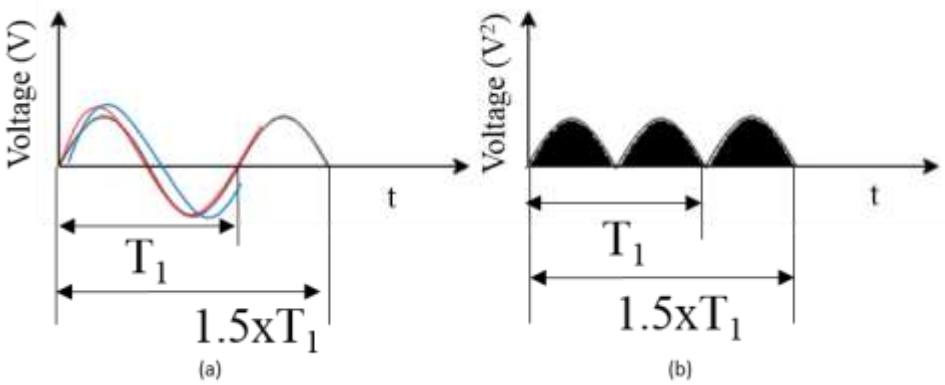

Figure 2.1: RMS value for coherently sampled sine-wave. a) sine-waves with two periods, one 1.5 times larger than the other, and (b) sine-wave with 1 ½ period where sampled signal has been squared.

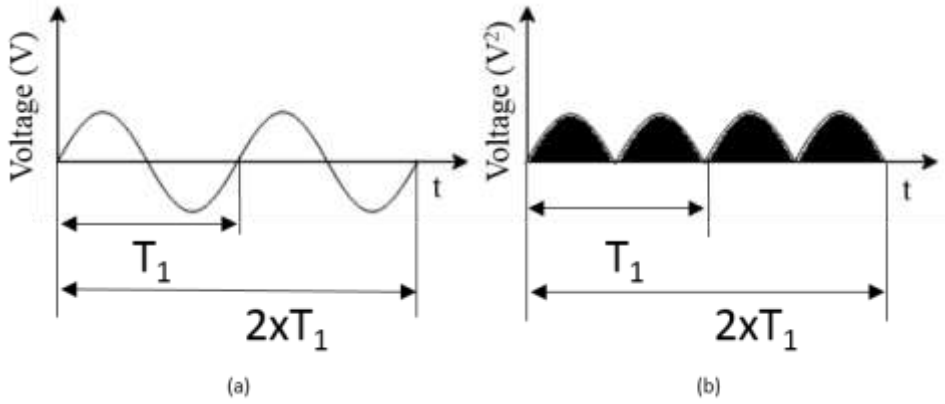

Figure 2.2: RMS value for coherently sampled sine-wave. (a) sine-wave with 2 periods consisting of positive and negative voltage, and (b) sine-wave with 2 periods where sampled signal has been squared.

2.2 Sampling and Reconstruction

Sampling and reconstruction are two processes that are at the heart of the proposed coherent subsampling test system. A continuous signal can be described as

$$v(t) = A \cdot \sin(2\pi ft + \phi) \tag{2.2}$$

where A is the amplitude of a sine-wave, f is the frequency, t is function of time, and ϕ as phase

term. When such continuous signals are sampled with an ADC, it is converted to a discrete-time signal described as

$$v[n] = A \cdot \sin(2\pi \frac{f_T}{f_s} n + \phi) \tag{2.3}$$

where f_T is test signal frequency and f_s is sampling rate and n is the time integer index. Signals that are described in discrete domain, such as in Equation (2.3), can be saved in ATE memory and the sampled data can be used for further DSP analysis. Now, we have converted the continuous time signal to a discrete time signal, we can also perform the opposite conversion. A DAC is the device that converts discrete-time signals into continuous-time signals through a process called *reconstructing*. Reconstructing is an operation that involves an interpolating function, denoted here as $p(t)$, and the discrete-time signal $v[n]=v(nT_s)$. The role of the interpolating function is to fill in the signal value between the sample instants, according to the convolution operation, i.e.,

$$v(t) = \sum_{-\infty}^{\infty} v(nT_s)\, p(t - nT_s)\,. \tag{2.4}$$

In practice, the DAC creates a sample-and-hold effect at its output as illustrated in Figure 2.3. This can be viewed as a stair-case continuous-time signal. Due to the stair-case effect, the DAC output contains undesired high-frequency signals. To eliminate these unwanted frequency components, an anti-imaging filter is placed at the output of the DAC in cascade as shown in Figure 2.3. Although, in theory with ideal inputs, perfect reconstruction is possible with infinite duration pulses $p(t)$, in reality, perfect reconstruction cannot be realized. During the DAC reconstruction process, errors are introduced, such as aperture effect and, magnitude and phase errors.

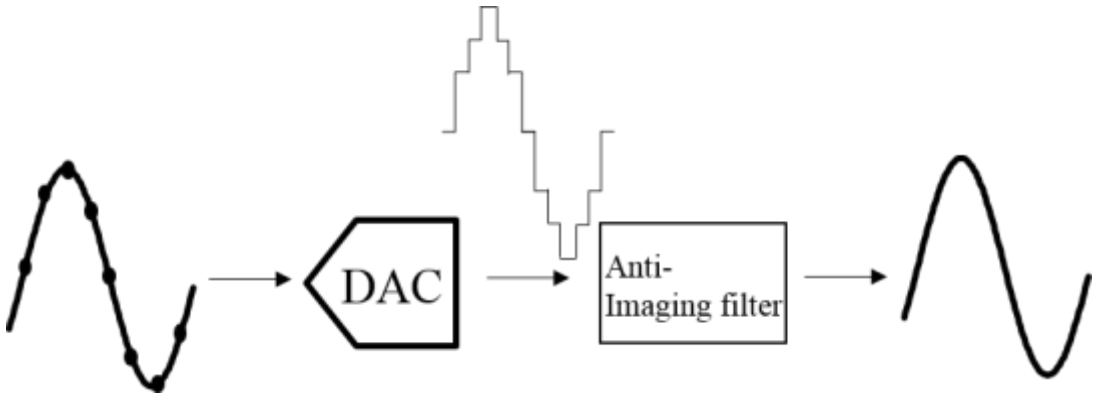

Figure 2.3: Illustrating the reconstruction process of a DAC.

2.3 Coherent Sampling System

Today's high speed optical communication uses principles of coherency [2], where it was been first formulated by M. Mahoney in the context of mixed-signal testing [24]. As it has been stated before, most system today use data converters to convert between analog and digital signals. DSP-based testing uses finite sample sets to excite a DUT. By using repetitive sample sets, a test signal can be generated that can maintain its spectral purity indefinitely.

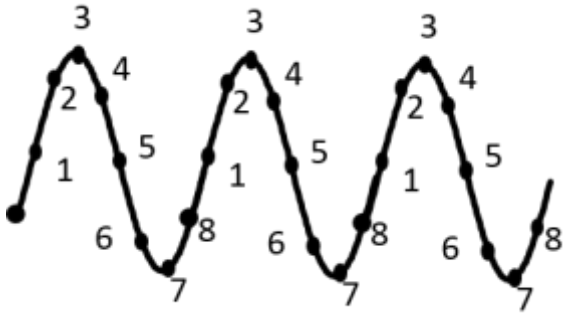

Figure 2.4: Repeated sample set that is coherent with respect to the sampling period.

The example waveform displayed in Figure 2.4 is an illustration of a sample sets that consists of 8 data samples that repeat for three cycles. Notice how the 8 samples has smooth transition from last point (numbered 8) to start (numbered 1) of the new sample sets. Such smooth transition is referred as *coherence*. The term coherence is the most important aspect of DSP-based testing which allows quick and accurate testing. If one does not coherently sample a signal, it may look like Figure 2.5. The sampled set that is shown here does not exhibit a smooth transition from sample-to-sample, unlike that which we seen in Figure 2.4.

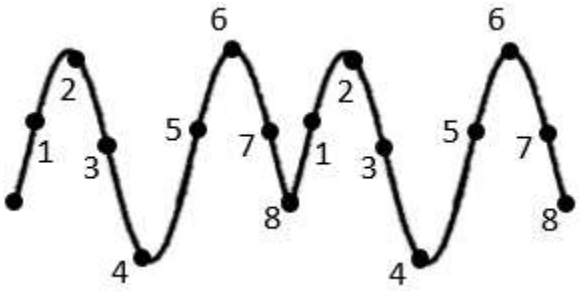

Figure 2.5: Repeated sample set that is non-coherent with respect to the sampling period.

A coherently sampled signal such as that shown in Figure 2.4 consist of exactly 8 unique points; these points simply repeat cycle-after-cycle giving rise to the perfect-looking sine wave signal. In general, a coherent signal can be constructed from N unique points over a full period called the *Unit-Test-Period* (*UTP*). Assuming the time interval between samples is equal to the reciprocal of the sampling frequency F_S, then the UTP can be quantified as

$$UTP = \frac{N}{F_S}. \tag{2.5}$$

Conversely, the inverse of the *UTP* is referred to as the *primitive frequency*, F_P, i.e., the lowest frequency signal whose period coincides exactly with the UTP, i.e.,

$$F_P = \frac{1}{UTP} = \frac{F_S}{N} \tag{2.6}$$

In order to satisfy the coherency requirement mentioned above, i.e., smooth transition at the wrap-around point, it has been proven by [24] that only those signals whose frequency F_T are an integer multiple of the primitive frequency will be coherent. Mathematically, it can be stated as

$$F_T = \frac{M}{N} F_S \tag{2.7}$$

where M is an arbitrary integer.

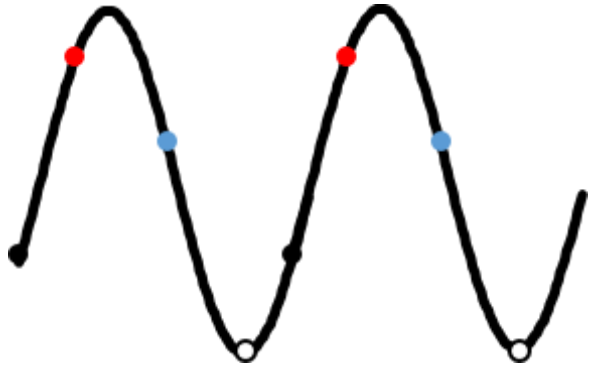

Figure 2.6: Non-mutually prime number selected as a bin, where the same sampling points are illustrated using colors.

In order to avoid non-coherence effects, the test engineer needs to keep the ratio of F_T/F_S and M/N as the ratio of two integer numbers [25]. Usually, N is chosen to be power of 2's, because of the periodicity and the computation time of the FFT, and M should be either odd or prime whichever makes the M and N relationship to be *relatively prime*; relatively prime or mutually prime number means M and N have no common divisors other than 1. If a non-mutually prime number has been chosen for M, it leads to periodic errors that can be seen in Figure 2.6.; periodic errors means, sampled data are not unique to each other, hence, some of the sampling points will contain repeated sample sets. Here, the sampled points are identical for both cycles of a sine-wave

and following conditions can be achieved by applying M=2 and N = 8. By having the ratio of *M* and *N* being non-relatively prime, the sampled points will be repeating after the first 4 sample points; the repetition of the samples are highlighted in different colors. The same colored samples indicate that the sampling instance are exactly identical to each other, hence, leading to periodic errors which has been explained previously.

Aside from periodic errors, there are other handful of reasons to use mutually prime numbers, such as distortion effect like intermodulation. Intermodulation is the term that is being used to define the mix of two frequencies that lands on a bin of interest and change the desired measurement value. Here, bin represents the index of the FFT algorithm. While choosing mutually prime numbers does not guarantee no intermodulation. It will, however, greatly reduce the likelihood of having an intermodulation and harmonics that can land on the bin of interest, which in term will alter the result of the measurement. Therefore, even though the mutually prime number rule has been used, it is important to verify that the any kinds of distortion does not lands on a bin of interest.

Another reason to use mutually prime number bin (*M*) is related to asymmetrical peaks in the time domain signal. From Fig. 2.7(a), the signals are symmetrical relative to DC offset where multi-tone signal has been generated using bins 3, 5, and 7. On the other hand, Fig. 2.7(b), shows asymmetrical along the DC offset, where the generated multi-tone signal uses spectral bins that are non-mutually prime which are 2, 5, and 7. Hence, the non-mutually prime bin selection gives rise to asymmetrical peaks that has different maximum and minimum values. Such tests result in very poor DUT coverage as it does not exercise the full range of the DUT; one side of the range is higher than the other. The problem of asymmetrical peaks cannot be solved by simply increasing the signal swing, since one side of the signal swing will be over the limit of DUT input range, thus,

loss of original signal information. Hence, it is best to use mutually-exclusive prime numbers for *M* and *N* in all instances when selecting a bin for generating multi-tone signals.

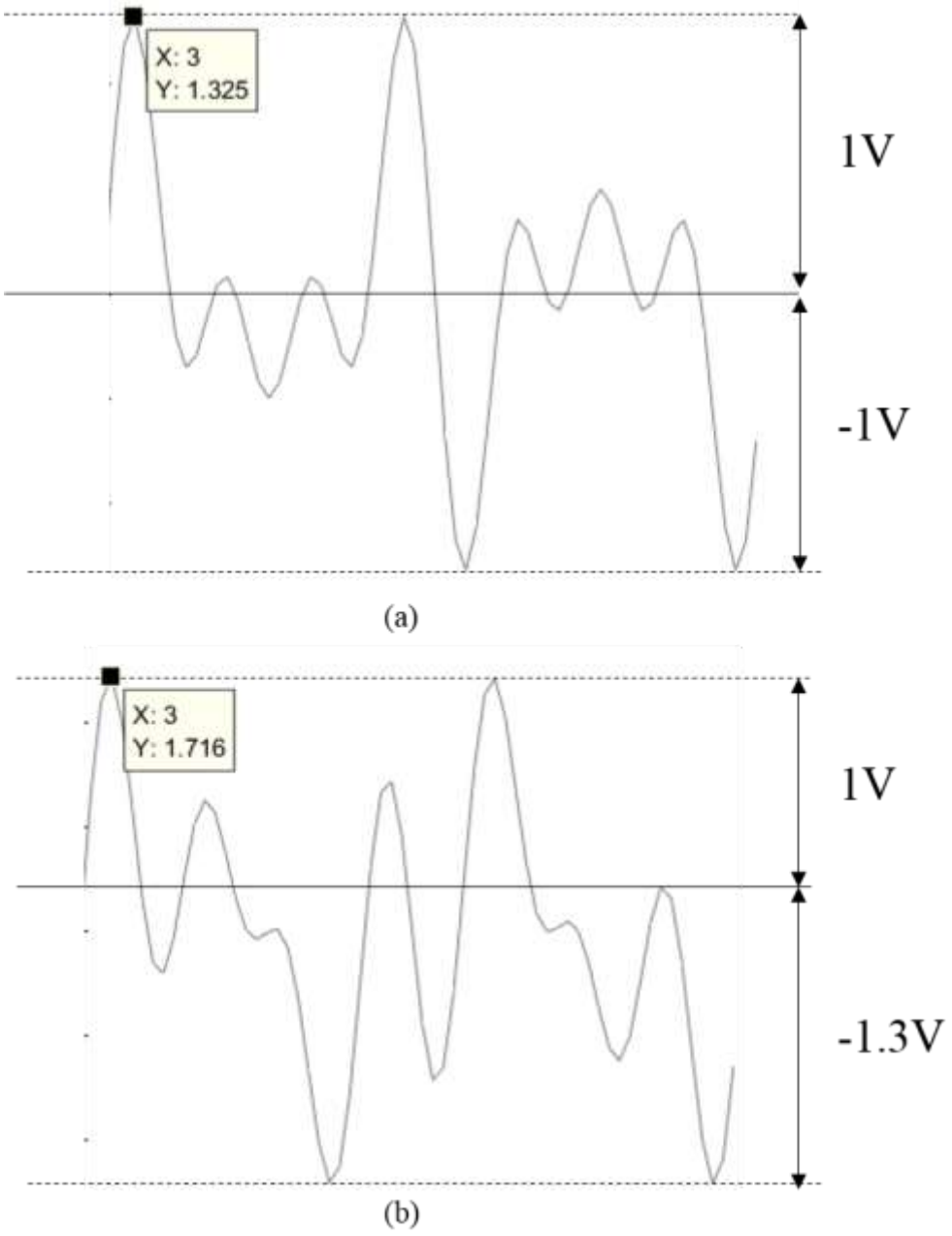

Figure 2.7: Non-mutually prime bin selection can lead to asymmetrical peaks relative to DC offset of a signal: (a) mutually prime multi-tone signal, (b) non-mutually prime multi-tone signal.

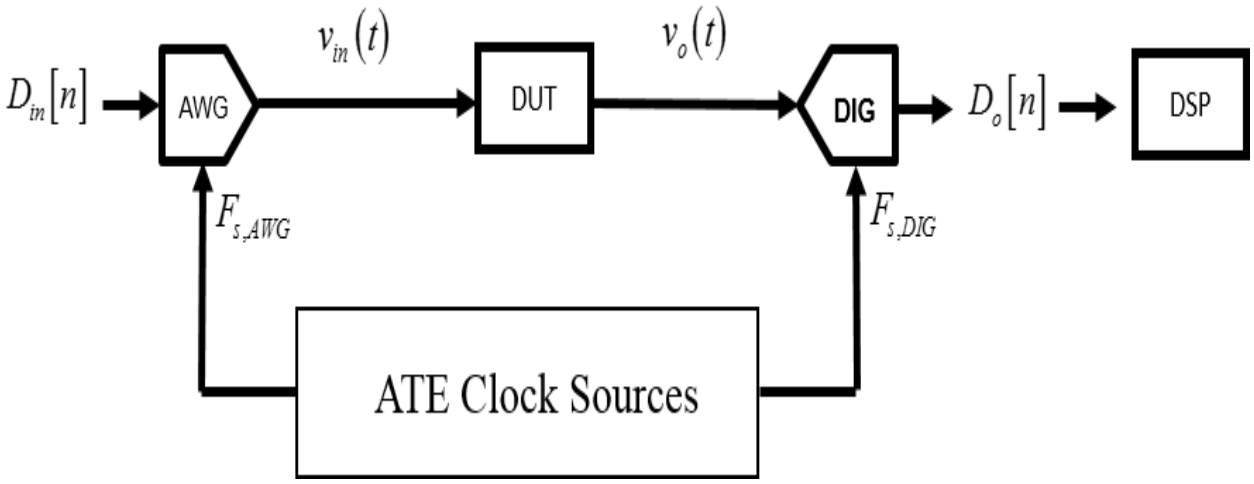

Figure 2.8: General coherent sampling system.

The general coherent sampling system is shown in Figure 2.8 without any filter at this stage, as the emphasis is on clock synchronization requirements; subsequent chapters will include the filters as well as its role in details. The signal, denoted as $v_{in}(t)$, is generated by the AWG using a predefined set of data points stored in the ATE memory. This signal is used to excite the DUT. The sampling rate of the AWG is denoted as $F_{S,AWG}$. Subsequently, the output response of the DUT will be sampled using a digitizer (DIG) at sampling rate $F_{S,DIG}$ where a set of sampled points are saved to an ATE memory for further analysis. Note in cascade with the AWG output but not shown is an anti-imaging filter. Likewise, in front of the DIG is an anti-aliasing filter. These filters are used to remove any high-frequency components associated with the AWG/DIG process. The sampling frequencies of both the AWG and DIG are derived from the ATE clock source block. This blocks serves to generates two independent frequencies $F_{S,AWG}$ and $F_{S,DIG}$ from a common clock source reference. These signal frequencies are derived from a Phase-Lock Loop (PLL), whose parameters are established by integer-valued divider blocks.

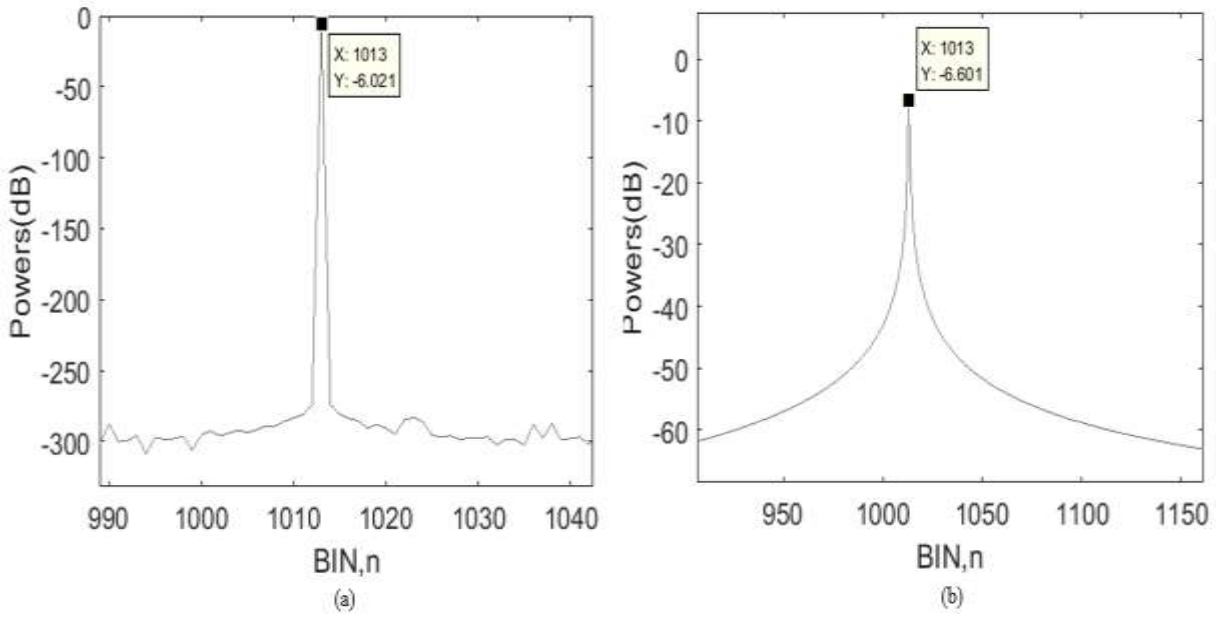

Figure 2.9: Comparison of two different sampling system of single-tone signal: (a) Coherently sampled signal, and (b) Non-coherently sampled signal. (N=4096).

Now that we have explained the general coherent system, we are now able to sample a signal coherently and its result are shown in Figure 2.9 where both coherent and non-coherently sampled signal results are illustrated. From Figure 2.9(a), the coherently sampled signal has a very low noise floor with an impulse-like tone. No spectral leakage is present in the FFT result of the sampled signal, as it has satisfied the Equation (2.5) where the ratio of F_T/F_S and M/N are rational numbers. On the other hand, for the case for a non-coherently sampled signal shown in Figure 2.9(b), spectral leakage can be observed where a single-tone sine-wave has skirting around the fundamental tone. To overcome the issue of leakage, windowing needs to be used where it alters the actual sampled data. Additionally, for different tests requirements, test engineer needs to select windowing that suits the needs. Hence, coherent sampling is very useful method to preserve the spectral purity of the sampled signal.

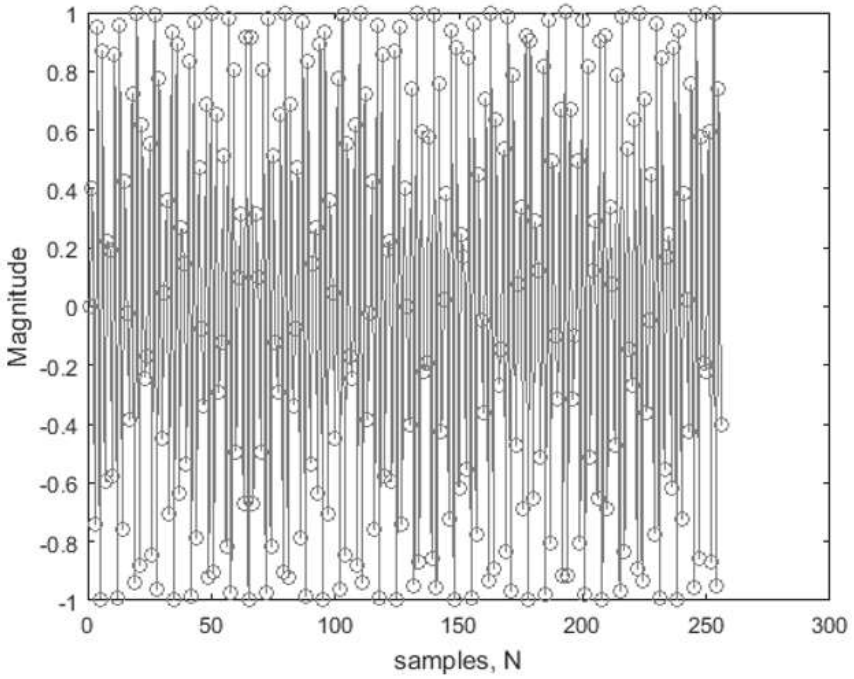

Figure 2.10: Visualization problem when M approaches to N/2. (M=111, N=256).

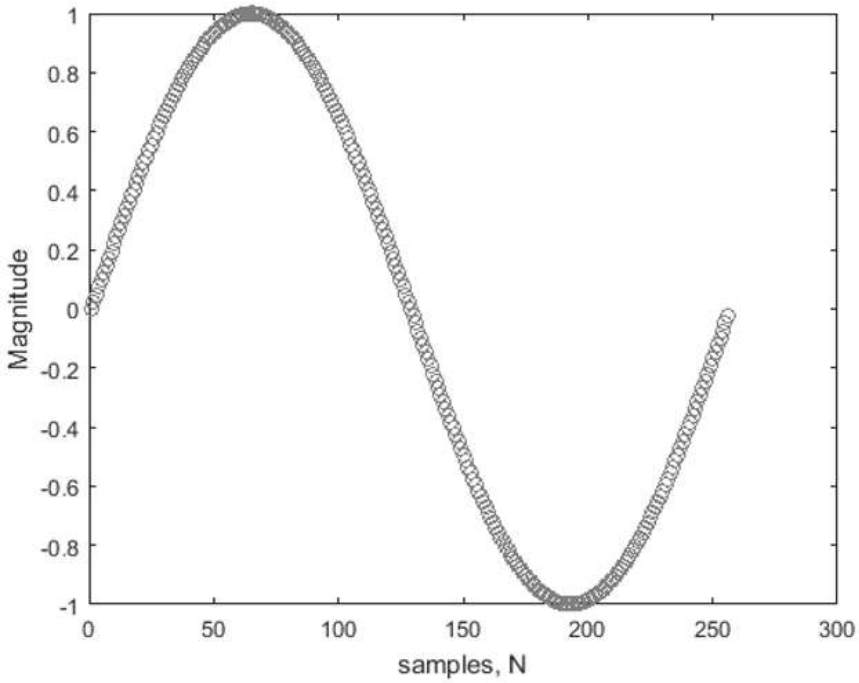

Figure 2.11: Result of modulo time plot algorithm applied to sampled data shown in Figure 2.10.

One might ask how can we determine whether the sampled data is coherent or not? Conventional methods would use spectral analysis and/or histograms which provides some information, but a technique called the *Modulo Time Plot* gives a quick visualization of system performances, such as dynamic range, error plot, and timing errors [26]. The modulo time plot technique is more commonly used when *M* approaches *N/2*. In such situations, there are too few points per cycle of the sine-wave. This creates a visualization problem. Such problem can be seen from Figure 2.10 for a sine-wave generated with sampling parameters *M=111* and *N=256*. From this plot, it is impossible for one to conclude that the sample signal is in fact a single-tone sine-wave. Instead, to aid the visualization process, one can apply the modulo time plot technique and produce the result shown in Figure 2.11. As can be seen from this figure, a single-cycle of the sine-wave is now evident which gives a visualization that the sampled signal from the Figure 2.10 is indeed a sine-wave signal. A modulo time plot is created by mapping a set of ordered pairs (x,y) from the original data set to a new set of order pairs according to

$$(x,y) \text{ - > } (x',y) \text{ where } x' = (n*M) \bmod N = N \cdot f_r(\frac{n*M}{N}) \tag{2.8}$$

where *n* is the index of the sample, *M* is an integer $0<M<N/2$, and $f_r(a)$ indicates the fractional part of the argument *a*.

2.4 Coherent Sampling of a Multi-Tone Signal

A signal consisting of multiple sine-waves with different frequencies, called a *multi-tone signal,* can be a very useful test signal. Consider a circuit that operates over a frequency range from 1 kHz to 20 kHz. To measure its frequency response, a sine wave at 1 kHz would be applied

with a known input RMS level and the RMS value of the corresponding output measured. The ratio of the output to input RMS values would provide information about the gain of the circuit at 1 kHz. This procedure would then be repeated for signal frequencies ranging from 1 kHz to 20 kHz, in small frequency increments, say 1 kHz frequency steps. If we assume that *P* individual frequencies were involved in the frequency response test and each single-frequency test took T_{ST} seconds to complete, then the total test time will be $P \times T_{ST}$ seconds. A multi-tone approach would combine all *P* sine-wave together into one signal by simply adding the individual tones with frequencies $F_{T,i}$ according to

$$v(t) = \sum_{i=1}^{P} A_i \cdot \sin(2\pi f_i t + \phi_i) \tag{2.9}$$

where each tone is assumed to have an arbitrary amplitude A_i and phase ϕ_i. Sampling the multi-tone signal with sampling frequency F_S leads to the following discrete-time signal v[n],

$$v[n] = \sum_{i=1}^{P} A_i \cdot \sin(2\pi \frac{F_{T,i}}{F_S} n + \phi_i) . \tag{2.10}$$

Here, $F_{T,i}$ represents multiple test-tone frequency which has different frequency component and F_S represents the sampling frequency. If the ratio of each individual frequency to sampling frequency $F_{T,i}/F_S$ can be expressed as the ratio of two integers, specifically, M_i/N, where M_i is the number of cycles the *i*-th sine wave completes in *N* points, then the entire sample set will be coherent, e.g.,

$$v[n] = \sum_{i=1}^{P} A_i \cdot \sin(2\pi \frac{M_i}{N} n + \phi_i) . \tag{2.11}$$

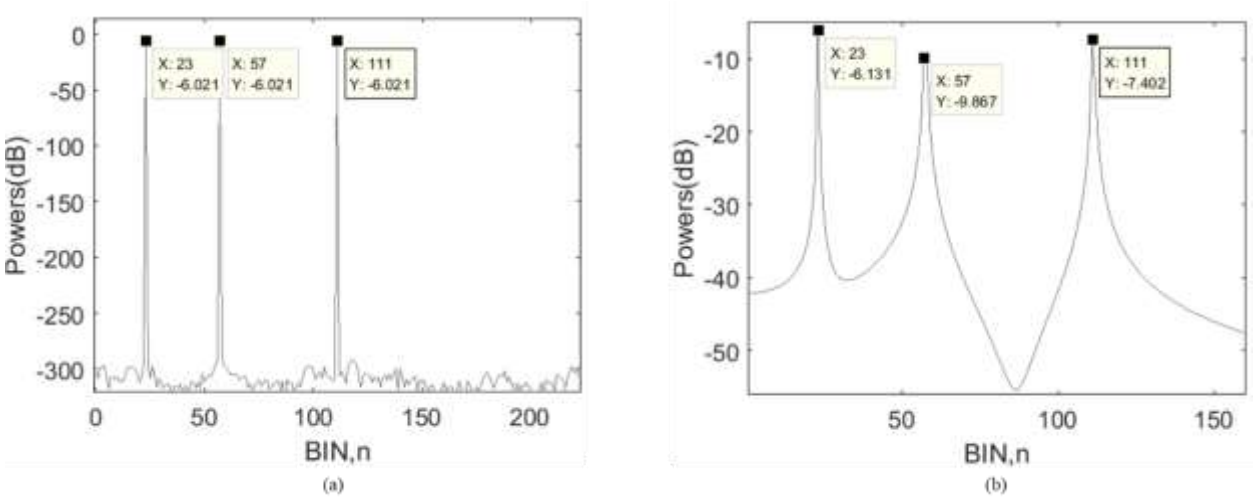

Figure 2.12: Comparison of two different sampling system of multi-tone signal: (a) Coherently sampled signal, and (b) Non-coherently sampled signal. (N=4096).

A 4096-point FFT of a three-tone multi-tone signal with M_i of 23, 57 and 111 can be seen in Figure 2.12(a). As can be seen, three impulse-like tones are present in bins 23, 57 and 111. All other bins contain a very low-level noise component. It is interesting to compare the FFT result of a multi-tone signal that is non-coherent with the sampling rate. The Figure 2.12(b) were generated using the same N and F_S, but with non-integer bins such as 23.1, 57.5, and 111.3. As can be seen from Fig. 2.12(b), in much the same way that was seen for the non-coherent single-tone signal, large amounts of spectral leakage is present.

While a multi-tone signal can save immense test time when compared to a test involving a single-tone, there are some cautions that one must take. In particular, the peak-to-RMS ratio of the multi-tone signal must be held in check. If this ratio is too large, then it signifies that most of the signal power is concentrated around a single time instant, with very little signal power elsewhere. As a result, it can cause undesirable effects, such as: (1) saturate the DUT and drive it out of its linear operation, and (2) the low-power region of the signal will be masked out by external noise sources. To avoid a high peak-to-RMS ratio, the phase of the individual tones that make up the

multi-tone signal require different phases with little correlation between. By selecting the individual phases randomly using a pseudorandom number generator to uniformly distribute the power over the UTP helps to remove any peaks in the signal. Observing from Figure 2.13(a), 7-tone multi-tone signal has been generated with equal phase and it is showing an energy concentrated at one instance of time pointed out by the two red circles. As it has been stated before, these kinds of concentrated power can cause undesirable effects. Now, let's take a look at Figure 2.13(b), this multi-tone signal has been generated using a iterative process to find a random phase that reduce the peak to a predefined range set by the user. By randomizing the phase of 7-tones, the power that has been concentrated at one time instance has been distributed throughout the UTP, therefore, removing spikes of the waveform that was apparent in the equal phase scenario. Hence, when creating a multi-tone signal, it is a good practice to randomize the phase of each tones, which distributes the power across the signals UTP that can reduce the undesirable effect during the DUT testing. Once the random phase are found, such phase can be used to test different chips, as long as the signal parameters are unchanged.

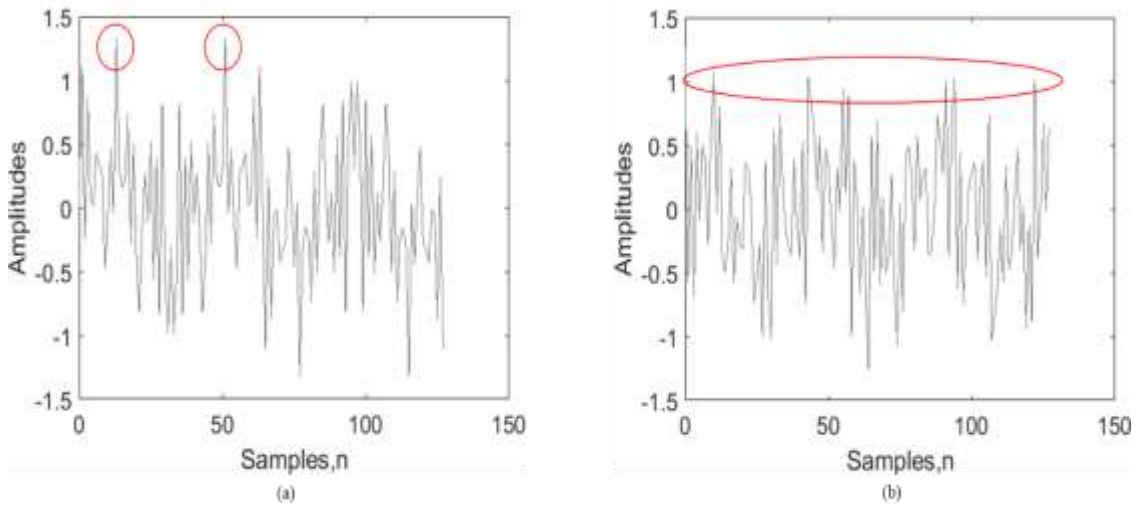

Figure 2.13: Peak-to-RMS control for multi-tone testing: (a) equal phases, and (b) random phases.

2.5 Summary

In this chapter, we have first described the problem of RMS meter with its non-coherent sampling approach and presented a solution where an integer multiple periods are needed to be sampled to accurately measure the RMS value of a signal. Then, we have introduced the term *coherent sampling* along with its coherent system, and described the F_T/F_S and M/N ratio which needs to be rational number in order to satisfy the coherent sampling condition. Moreover, selecting the mutually prime bin number to avoid the undesirable effects has been discussed, such as, periodic errors, asymmetrical peaks, and intermodulation. Aside from the single-tone, multi-tone signal also has been discussed in details and its advantages as a test signal. Lastly, comparison between equal phase and random phases of multi-tone signal has been discussed. In next chapter, we will now present a new coherent subsampling system that can be very useful sampling technique, which can be used to test high-speed digital communication systems.

Chapter 3

A Coherent Subsampling System: New Proposal

In this chapter, the principle of the coherent subsampling theory will be explained. A coherent subsampling system involving ADC/DACs will be presented along with their coherency requirements. Three different input signal conditions, single-tone, multi-tone, and phase modulated (PM) signals, will be considered.

3.1 Introduction to Coherent Subsampling

To illustrate the principle of subsampling, consider the diagram shown in Figure 3.1 involving a sine wave with period T_T, or frequency $1/T_T$.

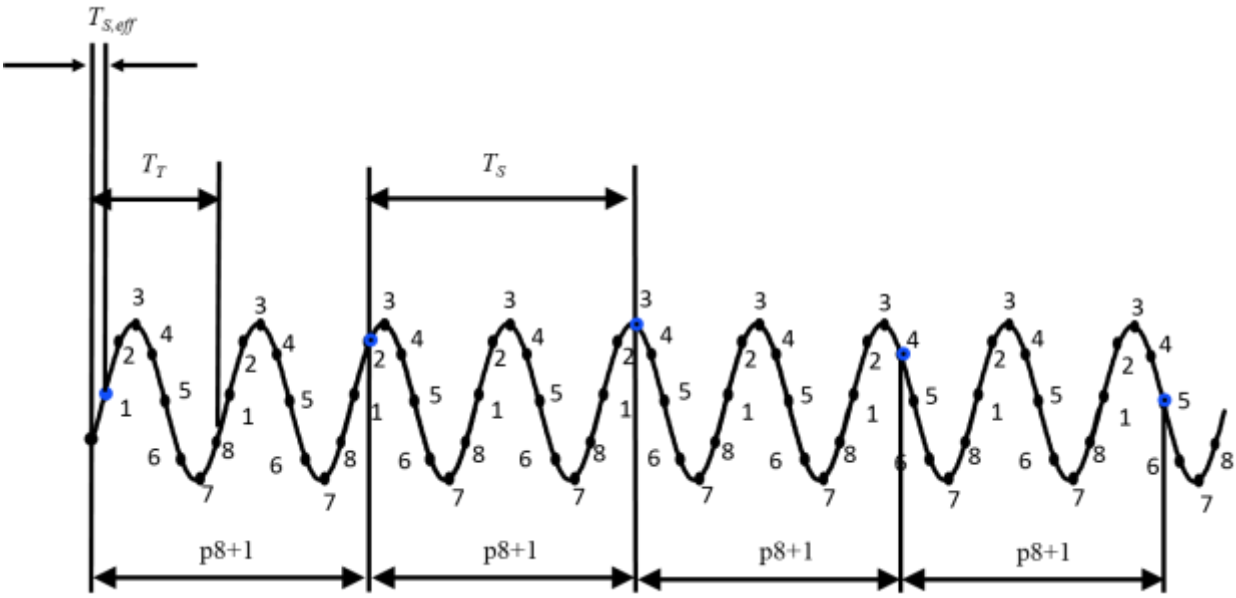

Figure 3.1: Highlighting the principle of subsampling on a sine-wave signal consisting of 8 sample points whose sample set is periodic.

This particular sine-wave has been sampled at a sampling rate that results in 8 points, labeled 1, 2, 3, … 8, being collected over a single period of this waveform. On account of the specifics of this sampling rate, the sampling of the next cycle of the sine-wave results in the exact same sample set, and the next and the next and so on. Because of the periodic extension property of the sample set, the sample points can be collected at a much slower rate, and in any order. For instance, once the first point labeled 1 has been sampled, the second point can be found by delaying the next sampling instant by some time corresponding to $p8+1$, where p is an arbitrary integer representing the number of cycles the sine-wave has completed fully before the next sample point. So, for $p=1$, the delay would be equal to 9, for $p=2$, the delay would be 17, etc. Using the same delay, the third point can be collected. Repeating this process, all 8 points could then be found using a sampling rate much lower than the original sample set.

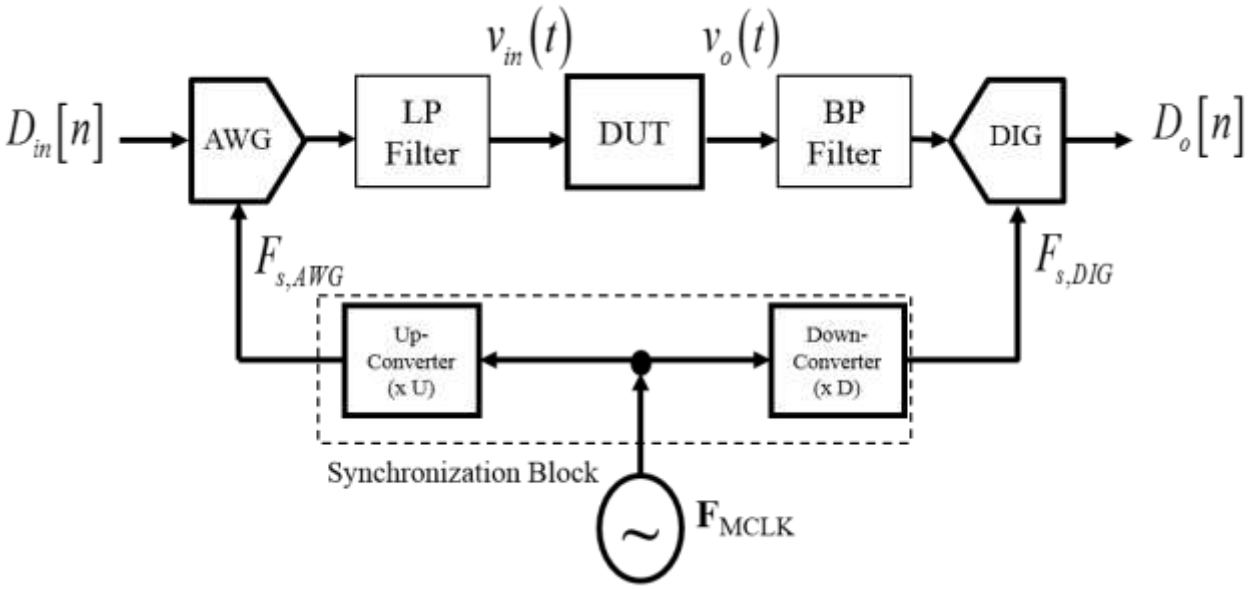

Figure 3.2: Proposed coherent subsampling test system for up-converting system using a band-pass, digitizer, and a phase-locked synchronization network.

3.2 General Sampling Consideration

The proposed coherent subsampling test system for the up-converting system is shown in Figure 3.2. Here an arbitrary waveform generator (AWG) receives a digital signal D_{in} from the source memory of the ATE and produces a base-band test signal $v_{in}(t)$ over some bandwidth BW_{AWG}. Subsequently, this signal is used to excite the DUT and its response, described by $v_o(t)$, is filtered by a band-pass (BP) response with bandwidth BW_{DIG} and then digitized using the DIG. The corresponding sample values D_o are then delivered to the capture memory of the ATE. The AWG and DIG is assumed to be clocked with a frequency $F_{S,AWG}$ and $F_{S,DIG,}$ respectively. The sampling clocks are derived from a synchronization network involving a master reference clock with frequency F_{MCLK}, and two internal timing blocks called the up- and down-frequency converters.

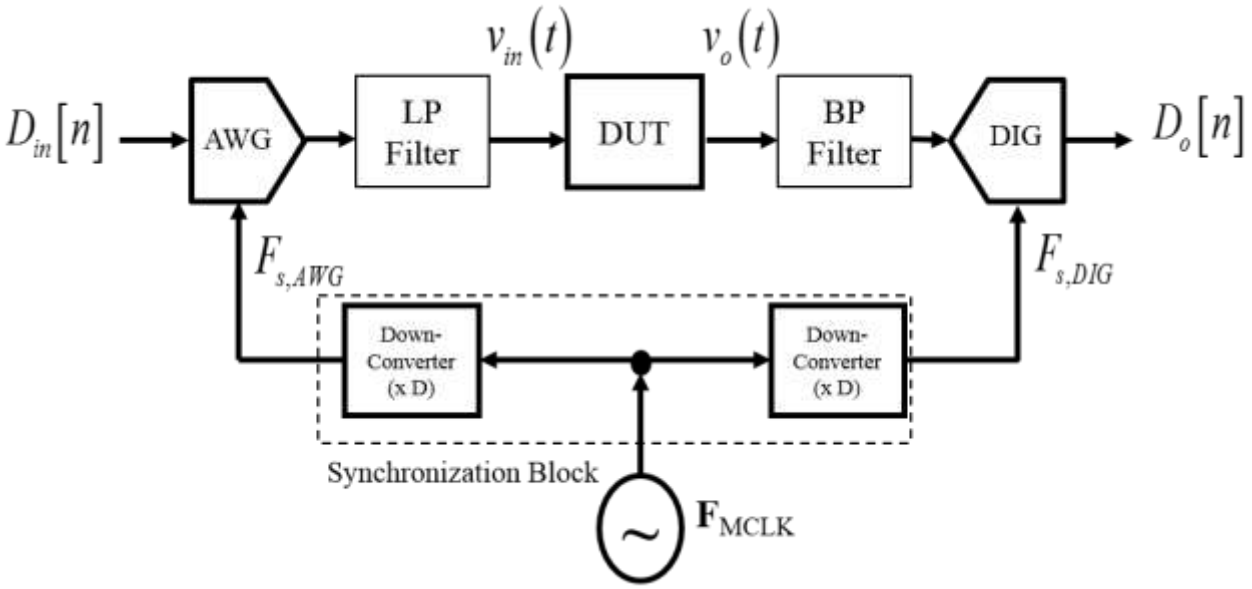

Figure 3.3: Proposed coherent subsampling test system for down-converting system using a band-pass, digitizer, and a phase-locked synchronization network.

Another coherent subsampling test system is shown in Figure 3.3. The block diagram illustrates a subsampling system similar to the one shown in Fig. 3.2 but whose blocks inside the synchronization section consists of only down converters – i.e., has no up-converters. In other words, $F_{S,AWG}$ and $F_{S,DIG}$ are restricted to frequencies that are less than reference clock signal F_{MCLK}.

The up and down-converters are realized using an integer PLL and a fractional PLL (FPLL). A PLL/FPLL is a widely used block in telecommunications and electronics. A PLL is a system that generates an output signal whose output frequency is related to the input reference frequency by the ratio of two integer value (see Fig. 3.4). In contrast, a FPLL is a similar device, but one that produces an output frequency that is again the product of the ratio of two integers and the reference frequency, whereas FPLL uses a fractional number and an integer number (Fig. 3.5). The increased dynamic range is made possible through the use of a sigma-delta modulator. A more detailed description of the PLL and FPLL will be presented in Chapter 5.

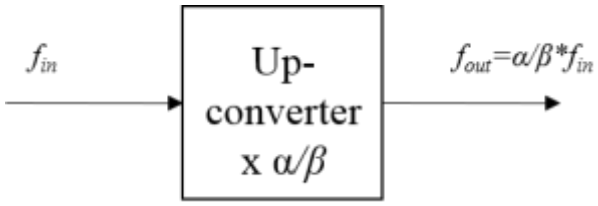

Figure 3.4: Block diagram of an up-converter; the output frequency is the product of the ratio of two integers α/β and the incoming frequency f_{in}.

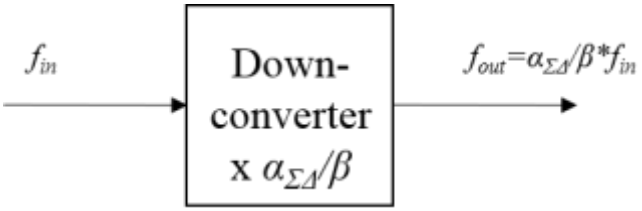

Figure 3.5: Block diagram of a down-converter; the output frequency is the product of input frequency and $\alpha_{\Sigma\Delta}/\beta$

By design, the sampling rate of the AWG is much greater than the sampling rate of the digitizer,

$$F_{S,AWG} >> F_{S,DIG} \tag{3.1}$$

so that the DIG subsamples or under-samples the incoming signal $v_o(t)$. The AWG is assumed to generate a base-band signal according to the principles of coherency, i.e.,

$$F_T = \frac{M_{AWG}}{N_{AWG}} F_{S,AWG} \tag{3.2}$$

where N_{AWG} represents the number of samples values used in the source memory of the AWG and M_{AWG} represents the number of cycles a sinusoidal will complete in the time period $N_{AWG}/F_{S,AWG}$. In contrast, the DIG is assumed to sample an aliased version of this tone, i.e.,

$$F_{S,AWG} > F_T > F_{S,DIG} > F_{T,alias} \tag{3.3}$$

then, according to the principles of coherency, i.e.,

$$F_{T,alias} = \frac{M_{DIG}}{N_{DIG}} F_{S,DIG} \tag{3.4}$$

where N_{DIG} represents the number of samples values used in the capture memory of the DIG and M_{DIG} represents the number of cycles a sinusoidal will complete in the time period $N_{DIG}/F_{S,DIG}$.

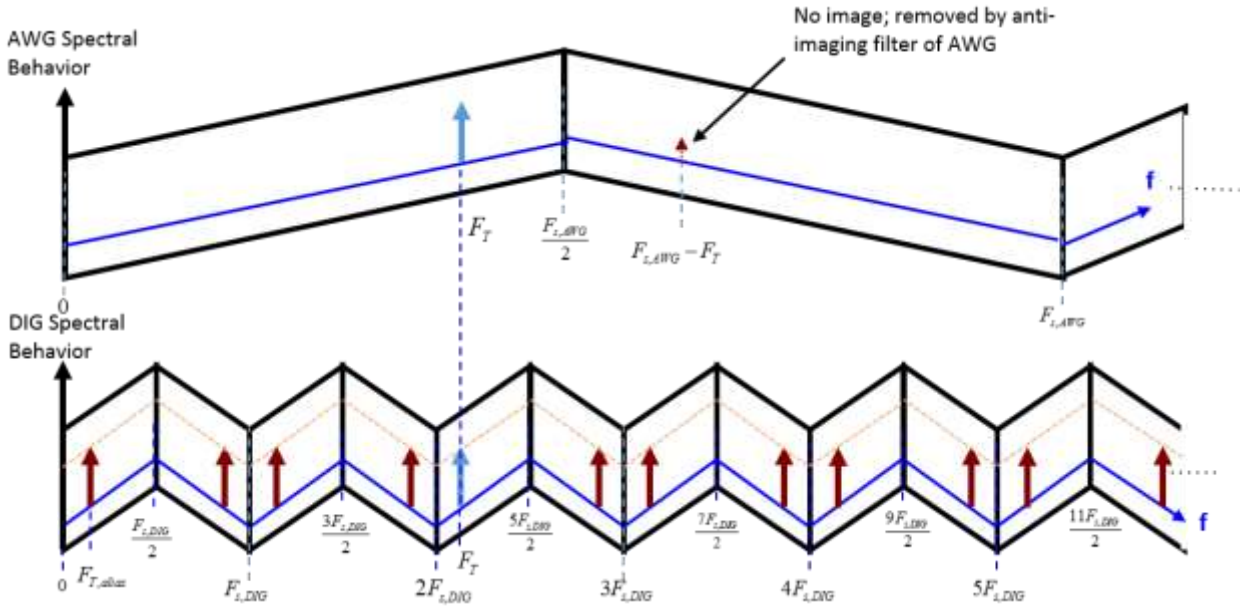

Figure 3.6: Illustrating the relative spectral periodicity of the AWG versus the DIG for a single sinusoidal. The blue vectors indicate original signal and the dark red vectors indicated an image signal.

Figure 3.6 provides an illustration of the spectral behavior of the AWG versus the DIG under the assumed subsampling conditions for a single-tone sine-wave. As both the AWG and the DIG are sampled systems, the spectral behavior in both cases are periodic in frequency, but the DIG exhibits a much smaller period. Of further consideration is the fact that any one period of the frequency spectrum consists of an even and odd part that are fold-symmetric [27]. It is also important to note the response of the AWG is low-pass in nature, whereas the DIG has a band-pass response. Here it is shown that the bandwidth of the DIG is set equal to $F_{S,DIG}/2$, it need not

be. It can, in principle, be made much larger than the AWG bandwidth without violating the conditions of Equation (3.3).

Using a DIG sampling rate that is much lower than its incoming signal frequency can be advantageous when trying to capture signal information associated with high-frequency (HF) analog/mixed-signal systems. Three separate coherent subsampling test arrangements will be described that can be used to make the following measurements:

1) RMS value of a HF single-tone sine-wave.
2) RMS values of individual frequency components of a HF multi-tone sine-wave
3) RMS value of the individual phase frequency components of a PM signal
4) RMS value of the phase noise using intrinsic measurement

In all of the above listed cases, the sampling conditions will be described in following subsection.

3.2.1 Subsampling a Single-Tone Signal

Consider a sinusoidal signal with amplitude A_{in} that is coherently generated by the AWG without any phase signal component as follows

$$D_{in}[n] = A_{in} \cdot \sin(2\pi \frac{M_{AWG}}{N_{AWG}} n). \tag{3.5}$$

As Equation (3.5) must satisfy the AWG coherency requirements, we can rewrite the above equation in terms of the test frequency and AWG sampling rate as

$$D_{in}[n] = A_{in} \cdot \sin(2\pi \frac{F_T}{F_{S,AWG}} n). \tag{3.6}$$

Now, assume that this signal is applied to the DUT input and the output signal is sampled by the DIG. Assuming the frequency of the output signal remains the same and the bandwidth of the BP filter is sufficient to pass the test signal with little attenuation, the DIG output signal can be written as

$$D_o[n] = A_o \cdot \sin(2\pi \frac{F_T}{F_{S,DIG}} n) \tag{3.7}$$

where A_o represents the amplitude of the DUT output signal. As the frequency of the output signal is related to the coherency parameters of the AWG described by Equation (3.2), one can re-write Equation (3.7) as

$$D_o[n] = A_o \cdot \sin(2\pi \frac{M_{AWG}}{N_{AWG}} \frac{F_{S,AWG}}{F_{S,DIG}} n). \tag{3.8}$$

The relationship between the original tone frequency F_T and the aliased tone frequency $F_{T,alias}$ can be summarized as

$$F_T = \begin{cases} p \cdot F_{S,DIG} + F_{T,alias}, & \text{even image} \\ p \cdot F_{S,DIG} - F_{T,alias}, & \text{odd image} \end{cases} \tag{3.9}$$

where p is an arbitrary integer representing the number of cycles of the digitizer spectrum encompassed or nearly encompassed by the incoming tone frequency. For example, in Figure 3.6, two cycles of the DIG spectrum are encompassed by the tone frequency. Substituting the AWG and DIG coherency relationships, specifically, Equations (3.2) and (3.4), into Equation (3.9) leads to

$$\frac{M_{AWG}}{N_{AWG}} F_{S,AWG} = p \cdot F_{S,DIG} \pm \frac{M_{DIG}}{N_{DIG}} F_{S,DIG} \tag{3.10}$$

or, when re-arranged,

$$\frac{F_{S,AWG}}{F_{S,DIG}} = \begin{cases} \dfrac{p + M_{DIG}/N_{DIG}}{M_{AWG}/N_{AWG}}, & \text{even image} \\ \dfrac{p - M_{DIG}/N_{DIG}}{M_{AWG}/N_{AWG}}, & \text{odd image} \end{cases} . \tag{3.11}$$

The above relationship identifies the synchronization condition between the sampling rates of the AWG and the DIG. To convince oneself that the above sampling conditions indeed satisfy the coherency requirements, consider substituting Equation (3.11) back into Equation (3.8) and re-arrange, i.e.,

$$\begin{aligned} D_o[n] &= A_o \cdot \sin(2\pi \frac{M_{AWG}}{N_{AWG}} \frac{F_{S,AWG}}{F_{S,DIG}} n) \\ &= A_o \cdot \sin(2\pi \frac{M_{AWG}}{N_{AWG}} (\frac{p + M_{DIG}/N_{DIG}}{M_{AWG}/N_{AWG}}) n) \\ &= A_o \cdot \sin(2\pi p \cdot n + 2\pi \frac{M_{DIG}}{N_{DIG}} n) \\ &= A_o \cdot \sin(2\pi \frac{M_{DIG}}{N_{DIG}} n) \end{aligned} . \tag{3.12}$$

To set up the subsampling coherent system, four parameters must be chosen by the user: M_{AWG}, N_{AWG}, M_{DIG} *and* N_{DIG}. Subsequently, for a given AWG sampling rate, $F_{S,AWG}$, both the test frequency F_T and DIG sampling rate $F_{S,DIG}$ would be determined from Equations (3.2) and (3.11), respectively.

3.2.2 Subsampling a Multi-Tone Signal

For a multi-tone signal, further sampling restrictions can be introduced to simplify the bookkeeping. Consider the source memory of an AWG is loaded with samples derived from a signal described by

$$D_{in}[n] = \sum_{i-1}^{P} A_{in,i} \cdot \sin(2\pi \frac{M_{AWG,i}}{N_{AWG}} n). \tag{3.13}$$

Here D_{in} is a multi-tone signal consisting of P orthogonal sine-waves completing $M_{AWG,i}$ number of integer cycles in the time period $N_{AWG}/F_{S,AWG}$ with amplitudes $A_{in,i}$. Following the subsampling development similar to the single-tone development in Section 3.2.1, one can write the expression for the samples captured by the digitizer as

$$D_o[n] = \sum_{i-1}^{P} A_{o,i} \cdot \sin(2\pi \frac{M_{AWG,i}}{N_{AWG}} \frac{F_{S,AWG}}{F_{S,DIG}} n). \tag{3.14}$$

Equation (3.11) provides the subsampling rule for a single sinusoidal. For a multi-tone signal, there are many choices in which to select the subsampling frequency $F_{S,DIG}$. The easiest choice, and one with the easiest booking, is to select the subsampling frequency based on the primitive frequency of the AWG and DIG. This occurs when $M_{AWG} = M_{DIG} = 1$. Subsequently, the subsampling constraint becomes

$$\frac{F_{S,AWG}}{F_{S,DIG}} = \begin{cases} \dfrac{m + 1/N_{DIG}}{1/N_{AWG}}, & \text{even image} \\ \dfrac{m - 1/N_{DIG}}{1/N_{AWG}}, & \text{odd image} \end{cases} \tag{3.15}$$

where m is a positive integer that relates the number of cycles of the DIG spectrum that is encompassed by the original tone, i.e., $p = mM_{AWG}$. Thus, substituting Equation (3.15) back into Equation (3.14) results in

$$
\begin{aligned}
D_o[n] &= \sum_{i=1}^{P} A_{o,i} \cdot \sin(2\pi \frac{M_{AWG,i}}{N_{AWG}} \frac{F_{S,AWG}}{F_{S,DIG}} n) \\
&= \sum_{i=1}^{P} A_{o,i} \cdot \sin\left[2\pi \frac{M_{AWG,i}}{N_{AWG}} \left(\frac{m + 1/N_{DIG}}{1/N_{AWG}} \right) n \right] \\
&= \sum_{i=1}^{P} A_{o,i} \cdot \sin\left[2\pi M_{AWG,i} m \cdot n + 2\pi \frac{M_{AWG,i}}{N_{DIG}} n \right] \\
&= \sum_{i=1}^{P} A_{o,i} \cdot \sin\left(2\pi \frac{M_{AWG,i}}{N_{DIG}} n \right)
\end{aligned}
\qquad (3.16)
$$

The above result is clear: The number of cycles completed in the DIG sampled spectrum will be equal to the same number of cycles completed in the AWG spectrum even though their respective time periods are different, i.e., $N_{AWG}/F_{S,AWG}$ vs. $N_{DIG}/F_{S,DIG}$, provided $M_{AWG,i} < N_{DIG}/2$ for all *i*. Violating this condition will lead to additional aliasing effects.

A second condition requires the BP filter of the DIG to be large enough to encompass all the tones of interest coming from the DUT, as depicted in Figure 3.7. For example, if an AWG has generated a multi-tone signal consisting of three frequencies, say F_T, $2F_T$ and $3F_T$, then the bandwidth of the BP filter in front of the DIG must be at least $2F_T$ to ensure sufficient signal energy reaching the DIG. Through the appropriate subsampling selection, i.e., Equation (3.15), the three tones will appear as harmonic aliases.

3.2.3 Subsampling a Phase-Modulated (PM) Signal

Often the frequency response behavior of a time-sensitive channel such as phase-locked loop (PLL) is to be measured. To do so, requires the AWG to generate a multi-tone signal

embedded in the phase of a sine-wave signal acting as the carrier. The proposed coherent subsampling system can be used to perform this measurement.

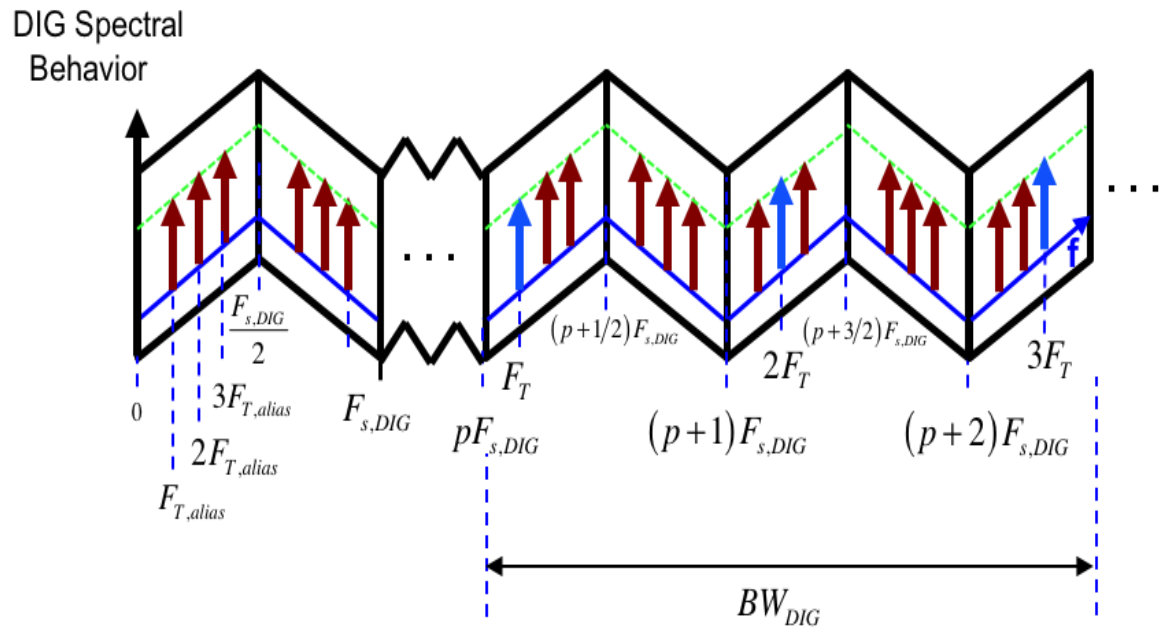

Figure 3.7: Illustrating the spectral periodicity of a multi-tone subsampled DIG signal consisting of a fundamental, second and third harmonic signals (in blue. All other signals (dark red) are images.

Consider the following PM signal equation used to produce the samples for the AWG source memory,

$$D_{in}[n] = A_{c,in} \cdot \sin\left(2\pi \frac{M_{AWG,c}}{N_{AWG}} n + \sum_{i=1}^{P} A_{\phi,in,i} \cdot \sin\left(2\pi \frac{M_{AWG,\phi,i}}{N_{AWG}} n \right) \right). \tag{3.17}$$

Here $A_{c,in}$ represents the amplitude of the carrier signal, and $A_{\phi,in,i}$ are the amplitudes of the individuals phase tones. Here it is assumed that P-tones are used. The carrier and phase tone frequencies are assumed to be coherent with the AWG sampling rate $F_{S,AWG}$ satisfying

$$F_c = \frac{M_{AWG,c}}{N_{AWG}} F_{S,AWG} \tag{3.18}$$

Likewise, the frequencies of the individual phase tones are given by

$$F_{\phi,i} = \frac{M_{AWG,\phi,i}}{N_{AWG}} F_{S,AWG} \cdot \tag{3.19}$$

Correspondingly, the samples collected by the digitizer have the familiar form,

$$D_o[n] = A_{c,o} \cdot \sin\left(\begin{array}{l} 2\pi \dfrac{M_{AWG,c}}{N_{AWG}} \dfrac{F_{S,AWG}}{F_{S,DIG}} n \\ + \displaystyle\sum_{i=1}^{P} A_{\phi,o,i} \cdot \sin\left(2\pi \dfrac{M_{AWG,\phi,i}}{N_{AWG}} \dfrac{F_{S,AWG}}{F_{S,DIG}} n \right) \end{array} \right) \tag{3.20}$$

where $A_{c,o}$ represents the amplitude of the carrier signal and $A_{\phi,o,i}$ are the amplitudes of the individuals phase tones seen at the DIG. Substituting the sampling constraint provided in Equation (3.15) leads to the final result,

$$D_o[n] = A_{c,o} \cdot \sin\left(\begin{array}{l} 2\pi \dfrac{M_{AWG,c}}{N_{DIG}} n \\ + \displaystyle\sum_{i=1}^{P} A_{\phi,o,i} \cdot \sin\left(2\pi \dfrac{M_{AWG,\phi,i}}{N_{DIG}} n \right) \end{array} \right). \tag{3.21}$$

In much the same way as the multi-tone subsampling situation, both the carrier and its sidebands are mapped to the DIG spectrum in the exact same sequence provided $M_{AWG,c}$ and $M_{AWG,\phi,I}$ for all i are less than $N_{DIG}/2$. Moreover, the bandwidth of the DIG must allow for enough sidebands to pass to the DIG unchanged but remove any other higher frequency components to avoid these aliasing into the Nyquist band. Figure 3.8 depicts the sample spectrum of the PM signal just described. All of the coherent constraints for the subsampling method for single-tone, multi-tone, and PM signals are summarized in Table 3.1.

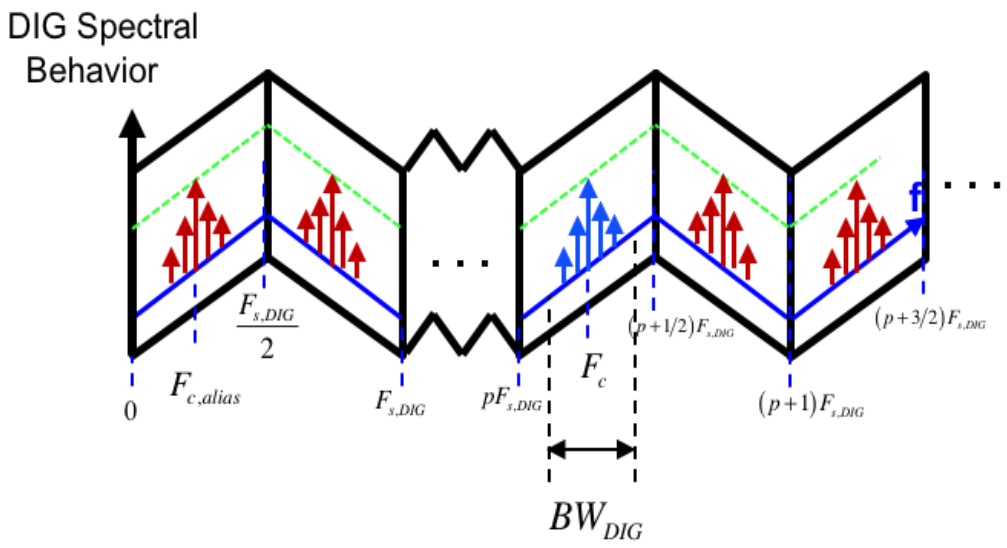

Figure 3.8: Illustrating the aliasing effect of a PM signal with carrier frequency F_C.

Table 3.1: Summary of coherent constraints for single-tone, multi-tone, and PM signals.

	Coherency Constraint
Single-tone Signal	$\frac{F_{S,AWG}}{F_{S,DIG}} = \begin{cases} \frac{p + M_{DIG}/N_{DIG}}{M_{AWG}/N_{AWG}}, & \text{even image} \\ \frac{p - M_{DIG}/N_{DIG}}{M_{AWG}/N_{AWG}}, & \text{odd image} \end{cases}$
Multi-tone Signal	$\frac{F_{S,AWG}}{F_{S,DIG}} = \begin{cases} \frac{m+1/N_{DIG}}{1/N_{AWG}}, & \text{even image} \\ \frac{m-1/N_{DIG}}{1/N_{AWG}}, & \text{odd image} \end{cases}$
PM Signal	$\frac{F_{S,AWG}}{F_{S,DIG}} = \begin{cases} \frac{m+1/N_{DIG}}{1/N_{AWG}}, & \text{even image} \\ \frac{m-1/N_{DIG}}{1/N_{AWG}}, & \text{odd image} \end{cases}$

3.4 Summary

In this chapter, a coherent subsampling system has been introduced, as well as the subsampling constraints for single-tone, multi-tone, and PM signals has been derived. Note that Equations (3.11), (3.15), and (3.27) needs to be satisfied to coherently subsample a signal. The next chapter will describe how to make intrinsic voltage and phase noise measurements.

Chapter 4

Intrinsic Noise Measurements Using Subsampling

In this chapter, subsampling techniques that can be used to measure the intrinsic voltage and phase noise of a DUT will be presented. The method involves converting the subsampled data set into an analytic signal using a Hilbert transform then extracting its instantaneous phase. As the Hilbert transform can be applied in either the time or frequency-domain, both approaches will be explained.

4.1 Voltage-Based Noise Measurement

A voltage-based intrinsic noise measurements of a DUT (no input signal present) can be performed with a subsampling digitizer with arbitrary subsampling frequency $F_{S,DIG}$, provided the digitizer (DIG) bandwidth satisfies the following condition

$$BW_{DIG} < \frac{F_{S,DIG}}{2} \tag{4.1}$$

and the center frequency f_o of the BP filter meets the condition

$$f_o = p \cdot F_{S,DIG} \pm \frac{F_{S,DIG}}{4}. \tag{4.2}$$

By doing so, the base-band spectral coefficients of the DIG sample set will correspond one-to-one with those that fall within the frequency region bounded by the BP filter. Alternatively, if the DIG bandwidth is much greater than its sampling frequency $F_{S,DIG}$ or the center frequency is not aligned with the sampling frequency then aliasing will occur. In the case of the center frequency being aligned according to Equation (4.2) but the DIG bandwidth is much greater $F_{S,DIG}$, then the noise power will increase on account of the aliases present by the following factor,

$$\gamma = \frac{BW_{DIG}}{F_{S,DIG}/2}. \tag{4.3}$$

Any other situation will depend on the specifics and no general answer can be provided a priori.

4.2 Phase-Based Noise Measurement

Phase-based intrinsic noise measurements, such as those associated with a PLL, or similar type of device, can be measured using the coherent subsampling approach described in Chapter

3.2.3 where it has explained coherent subsampling constraint for PM signals. A reference signal would be generated by the AWG operating at a clock rate of $F_{S,AWG}$ without PM modulation and applied to the DUT. The DUT output would then be digitized at a subsampling frequency $F_{S,DIG}$ given by Equation (3.15) and the corresponding sample sets are collected. The technique that will be used to extract the excess phase within a subsampled signal of a DUT compare to a reference signal, will be presented in Section 4.3, where it will present coherent phase extraction method using a Hilbert transform.

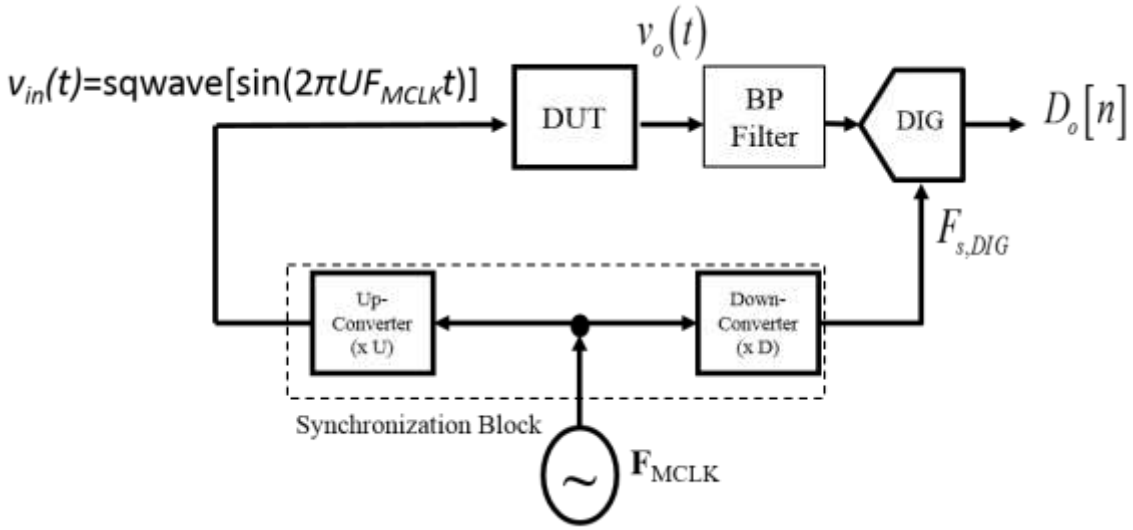

Figure 4.1: Proposed intrinsic phase noise measurement test setup with input reference signal taken directly from the up-converter block.

An alternative approach is one that removes the AWG as the source of the reference signal and, instead, takes the reference signal directly from the up-converter block as shown in Figure 4.1. In this case, the input signal to the DUT can be described as

$$v_{in}(t) = sqwave\left[\sin(2\pi \cdot U \cdot F_{MCLK} \cdot t)\right] \tag{4.4}$$

where the *sqwave* operation simply maps the sine wave signal into a square wave signal with the same frequency, UxF_{MCLK}. Here F_{MCLK} is the frequency of oscillation of the master clock and U

is the up-conversion factor. Similar to the up-converting intrinsic noise measurement setup, the down-converting intrinsic noise measurement is shown in Figure 4.2. There is very little difference between the two setups. Other than the reference clock signal, F_{MCLK}, is down-converted by an arbitrary integer; all other operation and blocks are identical.

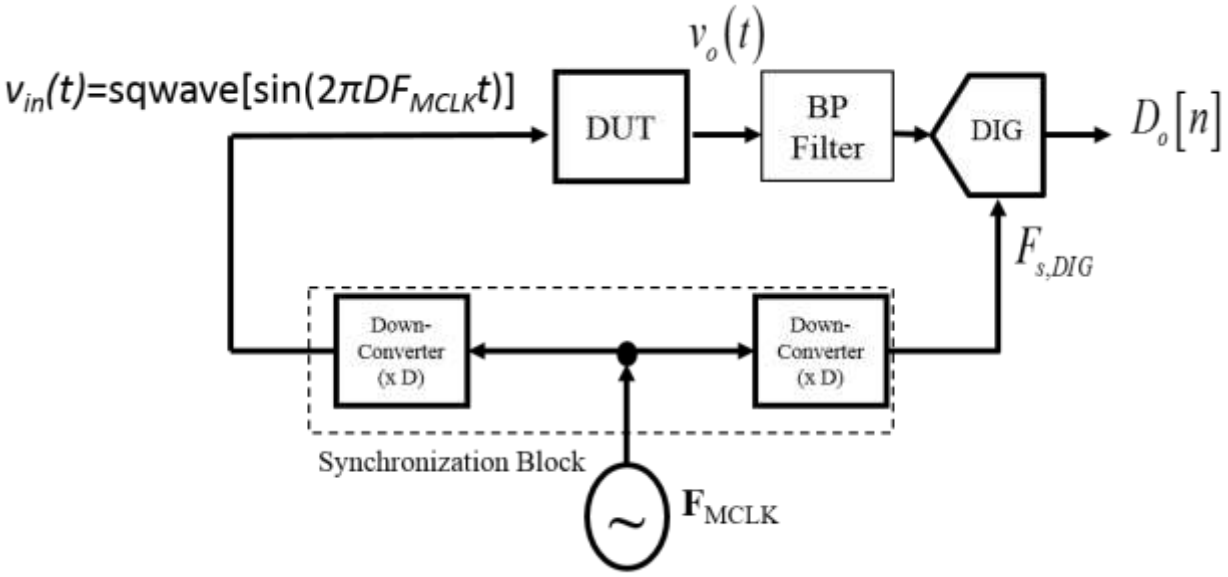

Figure 4.2: Proposed intrinsic phase noise measurement test setup with input reference signal taken directly from down-converter block.

Returning to the subsampling system depicted in Figure 4.1, on passing the DUT output through the BP filter and subsampling the output at a sampling rate of $F_{S,DIG}$, the DIG samples appearing in the capture memory can be then be described as

$$D_o[n] = \sin\left(2\pi \cdot U \cdot \frac{F_{MCLK}}{F_{S,DIG}} n\right). \tag{4.5}$$

With the sampling constraint,

$$\frac{F_{MCLK}}{F_{S,DIG}} = \begin{cases} m + 1/N_{DIG}, & \text{even image} \\ m - 1/N_{DIG}, & \text{odd image} \end{cases}. \tag{4.6}$$

Equation (3.26) can be reduced to

$$D_o[n] = \sin\left(2\pi \frac{U}{N_{DIG}} n\right). \tag{4.7}$$

Here the reference clock signal will appear in FFT bin U provide $U < N_{DIG}/2$. All other bins of the DIG FFT will therefore contain components of the noise.

4.3 Instantaneous Phase Signal Extraction Using Subsampling

The instantaneous phase of the output signal from the DUT $v_o(t)$ can be extracted from subsampled captured digital signal $D_o[n]$. Here the method of analytic signal representation is used [28]. The basic idea is to create a complex signal representation from the captured data through the application of the Hilbert transform, i.e.,

$$D_o[n] = D_o[n] + jDHT\{D_o[n]\} \tag{4.8}$$

where $DHT\{D_o[n]\}$ represents the Hilbert transform of $D_o[n]$ described by

$$DHT\{y[n]\} = \frac{2}{\pi}\begin{cases} \sum_{k=odd} \frac{y[k]}{n-k}, & \text{n even} \\ \sum_{k=even} \frac{y[k]}{n-k}, & \text{n odd} \end{cases}. \tag{4.9}$$

Consequently, the instantaneous phase [27] of the captured signal is found from

$$\theta_o[n] = \theta_o[n-1] + \tan^{-1}\left(\frac{DHT\{D_o[n]\}}{D_o[n]}\right) - \tan^{-1}\left(\frac{DHT\{D_o[n-1]\}}{D_o[n-1]}\right). \tag{4.10}$$

Often our interest lies with the instantaneous phase difference between the $D_o[n]$ and some reference signal, say $D_{ref}[n]$, referred to as the excess instantaneous phase, i.e.,

$$\phi_o[n] = \theta_o[n] - \theta_{ref}[n]. \tag{4.11}$$

As the DIG system is coherent with the sampling clock, the reference signal has an instantaneous phase that can be described as

$$\theta_{ref}[n] = 2\pi \frac{M_{AWG,c}}{N_{DIG}} n. \tag{4.12}$$

Hence, the excess instantaneous phase can be written as

$$\phi_o[n] = \theta_o[n] - 2\pi \frac{M_{AWG,c}}{N_{DIG}} n. \tag{4.13}$$

Alternatively, the Hilbert transform can also be performed in the frequency domain using the FFT [27] and [29]. Performing the Hilbert transform in the frequency domain is much more efficient than a time domain calculation, which is a computationally expensive process. To calculate the Hilbert transform using the frequency domain signal description, first apply a FFT according to

$$D_{out}(k) = FFT\{d_{out}\}, \text{ where k = 0...N-1}. \tag{4.14}$$

Next, compute a $D_{OUT,analytic}$ according to the following description

$$D_{out,analytic}(k) = \begin{cases} D_{out}(k), & \mathrm{k} = 0 \\ 2 \cdot D_{out}(k), & \mathrm{k} = 1,\ldots \frac{\mathrm{N}}{2} - 1 \\ 0, & \mathrm{k} = \frac{\mathrm{N}}{2},\ldots,\mathrm{N} - 1 \end{cases} \tag{4.15}$$

where the DC component of D_{out} is copied to k=0, then from k=1 to N/2-1 D_{out} will contribute twice the value of its corresponding coefficients. In other words, the spectral coefficients of the first images of D_{out} are summed with coefficients of the Nyquist Interval of D_{out} and the remaining bins in the first image set to zero. Similarly, $D_{OUT,reference}$ only needs to include its fundamental as

$$D_{out,reference}(k)=\begin{cases}2\cdot D_{out}(k), & \mathrm{k=M}\\ 0, & \text{otherwise}\end{cases}. \tag{4.16}$$

Once the two analytic signals are found, an inverse-FFT (IFFT) is performed and the real and imaginary parts of the analytic signal are found according to

$$d_{out}[n]=\mathrm{Re}\{IFFT(D_{out,analytic})\},\mathrm{n}=0,\ldots,\mathrm{N}-1. \tag{4.17}$$

and

$$\bar{d}_{out}[n]=\mathrm{Im}\{IFFT(D_{out,analytic})\},\mathrm{n}=0,\ldots,\mathrm{N}-1. \tag{4.18}$$

The instantaneous phase of the subsampled signal can then be found using Equation (4.10) where the instantaneous unwrapped phase, $\theta[n]$, can be found from

$$\theta[n]=\begin{cases}\theta[n-1]+2\pi+\tan 4q^{-1}(\dfrac{\bar{x}[n]}{x[n]})-\tan 4q^{-1}(\dfrac{\bar{x}[n-1]}{x[n-1]}), & \begin{array}{l}\bar{x}[\mathrm{n}-1]<0,\ x[\mathrm{n}]>0,\ \bar{x}[\mathrm{n}]>0\\ \text{or}\\ x[\mathrm{n}-1]>0\ \bar{x}[\mathrm{n}-1]<0,\ \bar{x}[\mathrm{n}]>0\end{array}\\ \theta[n-1]+\tan 4q^{-1}(\dfrac{\bar{x}[n]}{x[n]})-\tan 4q^{-1}(\dfrac{\bar{x}[n-1]}{x[n-1]}), & \text{otherwise}\end{cases} \tag{4.19}$$

where $\tan4q^{-1}(y/x)$ is the four-quadrant inverse tangent function defined according to

$$\tan 4q^{-1}(\frac{y}{x})=\begin{cases}\tan^{-1}(\dfrac{y}{x}), & x\geq 0, y\geq 0\\ \pi-\tan^{-1}(\dfrac{y}{-x}), & x<0, y\geq 0\\ \pi+\tan^{-1}(\dfrac{-y}{-x}), & x<0, y<0\\ 2\pi-\tan^{-1}(\dfrac{-y}{x}), & x\geq 0, y<0\end{cases}. \tag{4.20}$$

A conventional two-quadrant inverse tangent performs a one-to-many mapping that are separated by multiples of $\pm2\pi$. This creates a discontinuity in the computed phase and make this phase extraction method unusable.

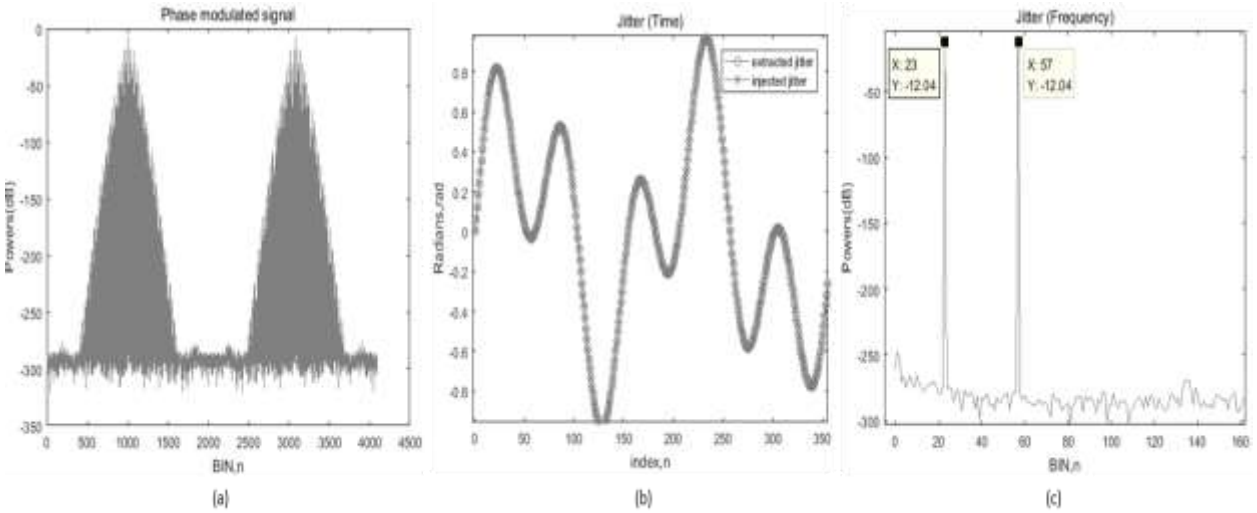

Figure 4.3: Various signals associated with a two-tone PM signal: (a) FFT of coherently captured signal from AWG, (b) extracted instantaneous phase signal, and (c) FFT of instantaneous phase signal.

There are other strategies to determine the excess instantaneous phase; details can be found in [27]. Reference signal that is generated from the AWG, may experience phase shift, therefore, it is always better to extract the reference signal phase using the sampled signal data from the receiver rather than relying on the generated signal parameters from the AWG. As an example, Figure 4.3 illustrates the various signals asscoiated with a two-tone PM signal generated by the AWG with paraemters N=4096, $M_{AWG,c}$ = 1013, $M_{AWG,\phi,1}$=23 and $M_{AWG,\phi,2}$=57. In part (a) the FFT of the AWG samples is shown. Here the fold-symmertric spectrum is shown, as well as the rich side bands about a carrier. In part (b), the instantaneous phase signal as a function of the time index, n, is shown and the corresponding frequency domain description is provided in part (c). Clearly, two tones in bins 23 and 57 are present.

4.4 Summary

In this chapter, subsampling techniques that can be used to measure the intrinsic voltage and phase noise of a DUT was explained. The method involves converting the subsampled data set into an analytic signal using a Hilbert transform then extracting its instantaneous phase.

Chapter 5

Implementation Issues

This chapter will provide the circuits used to create the sampling clocks of the coherent subsampling system. In addition, a brief look at the time and frequency resolution of a coherent subsampling system will be provided, together with a look at the impact of the ADC finite resolution on measurements.

5.1 Generating Coherent Sampling Frequencies

The general test setup for coherent subsampling system has be presented in Chapters 3 and 4. Here, we would like to describe the up and down-convert blocks that will be used to realize the sampling clocks for AWG and the DIG. A high-level description of these timing blocks was first presented in Section 3.1. Here we will look at these timing blocks in more detail.

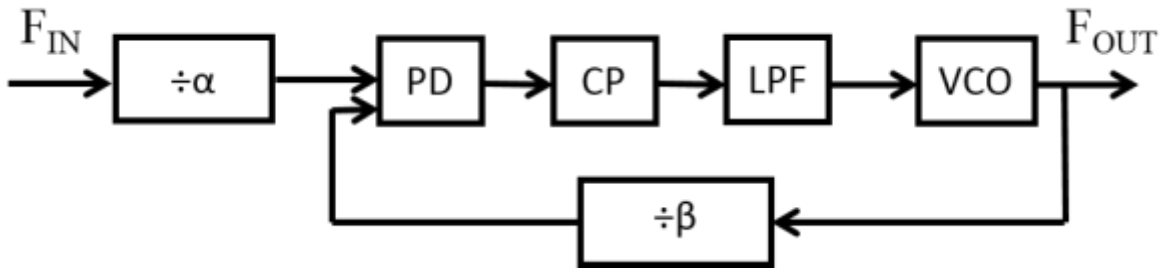

Figure 5.1: Block diagram of the PLL.

A circuit that generates an output frequency that is higher than the incoming reference frequency is the integer-based phase-lock loop (PLL) shown in Figure 5.1. The individual blocks that make up the PLL are as follows. The PD is short form for phase detector. It is used to detect the phase difference between its two inputs and produce a voltage signal in proportion to the phase difference. CP is short form for a charge pump. It is a device that has converts the output voltage signal from the PD into one of two possible current levels, $\pm I_O$; it essentially acts a one-bit D/A converter. This current is then applied to a low-pass filter block denoted by (LPF). The output of this filter is then applied to the input of a voltage-controlled oscillator (VCO) to generate the output clock signal. Two divider, i.e., counters, are present. One is placed in cascade with input signal and divides the input frequency by a factor of α. The other is placed in the feedback loop and divides the output frequency by a factor of β. The relationship between the output frequency and the input reference frequency is

$$F_{out} = \frac{\beta}{\alpha} \times F_{in} \tag{5.1}$$

As the dividers are essentially counters consisting of m flip-flops, the count range of each divider ranges from 0 to 2^m-1. This implies that β and α can take on any integer value between 0

and 2^m-1 in steps of unity. The highest frequency resolution of the PLL can be then be described as

$$\Delta F = \frac{F_{in}}{2^m - 1} \tag{5.2}$$

A fractional-N PLL(FPLL) is another PLL that utilizes a divider that divides by an integer P or P+1 depending on the selection value set at shown in Figure 5.2.

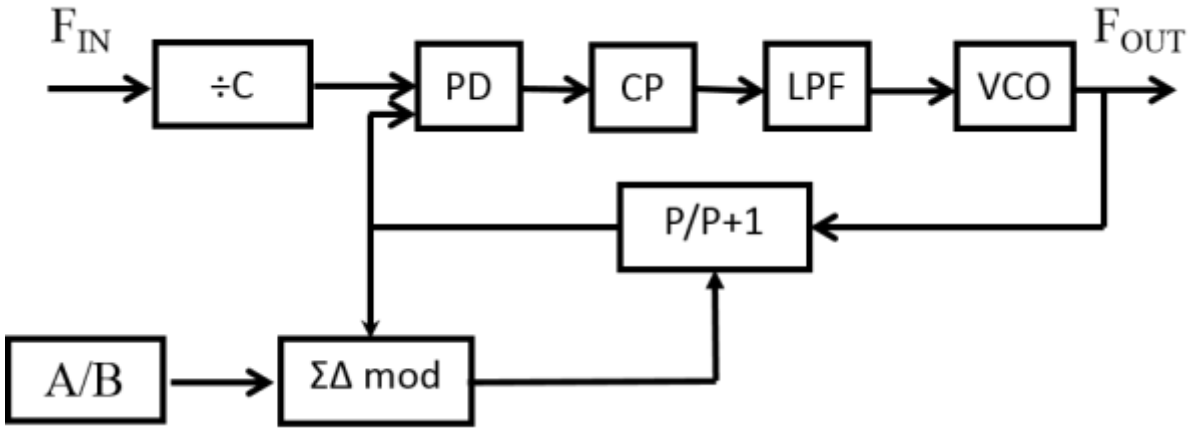

Figure 5.2: Block diagram of a FPLL with ΣΔ modulator

The selection value is driven by the output of a sigma-delta (ΣΔ) modulator with an input control variable set by an input integer value C. On doing so, the FPLL can provide an output frequency given by

$$F_{out} = \frac{average\{P, P+1\}}{C} \times F_{in} \tag{5.3}$$

As the ΣΔ modulator is a digital system working with n-bit wide words, the denominator term in Equation (5.3) can be expressed as the ratio of two integers, A and B, i.e.,

$$average\{P, P+1\} = \frac{A}{B} \tag{5.4}$$

Substituting back into Equation (5.3), the output frequency can be written as

$$F_{out} = \frac{A}{B \times C} \times F_{in} \tag{5.5}$$

If

$$\beta = A \quad \text{and } \alpha = B \times C \tag{5.6}$$

then Equation (5.5) can be written in the same form as Equation (5.1). The frequency resolution of the FPLL can be then be described as

$$\Delta F = \frac{F_{in}}{\alpha} = \frac{F_{in}}{B \times C} \tag{5.7}$$

As C takes on a maximum value of 2^m-1 and B takes on a maximum value of 2^m-1, then the frequency resolution of the FPLL is

$$\Delta F = \frac{F_{in}}{\left(2^m - 1\right) \times \left(2^m - 1\right)} \tag{5.8}$$

Here the FPLL clearly has a higher frequency resolution than the integer PLL.

5.2 Clock Synchronization Details

A coherent subsampling system relies directly on the ability of the clock network to generate the appropriate sampling clocks for the AWG and DIG. In Figure 3.2 and 3.4, the

synchronization subsystem consists of two main components: an up-converter and a down-converter. The up-converter takes the incoming master clock signal and scales its output frequency by an integer factor *U* to drive the AWG, i.e.,

$$F_{S,AWG} = U \cdot F_{MCLK} . \tag{5.9}$$

Conversely, the down-converter takes the incoming master clock signal and scales its output frequency by some factor *D* that can be expressed as the ratio of two factors, β and α, to drive the DIG, i.e.,

$$F_{S,DIG} = D \cdot F_{MCLK} = \frac{\beta}{\alpha} F_{MCLK} . \tag{5.10}$$

The rational for this choice lies with the circuits used to realize the up and down conversion blocks. The up-conversion clock component would be realized using an integer PLL with a frequency divider with gain U. The down-converter clock component would be realized using a FPLL, which can set the output frequency as the ratio of two integers, e.g., Equation (5.5).

As the ratio of the AWG to DIG sampling frequency for the single-tone test case must satisfy Equation (3.11), one can write

$$\frac{F_{S,AWG}}{F_{S,DIG}} = \frac{U \cdot F_{MCLK}}{\frac{\beta}{\alpha} F_{MCLK}} = \frac{p + M_{DIG} / N_{DIG}}{M_{AWG} / N_{AWG}} . \tag{5.11}$$

Solving for β and α, one finds

$$\beta = U \cdot M_{AWG} \cdot N_{AWG} \tag{5.12}$$

and

$$\alpha = N_{AWG}(p \cdot N_{DIG} + M_{DIG}). \tag{5.13}$$

Similarly, for multi-tone and multi-tone PM signal measurements ratio of the AWG and DIG can be found by using Equations (3.15) and (5.10),

$$\frac{F_{S,AWG}}{F_{S,DIG}} = \frac{U \cdot F_{MCLK}}{\frac{\beta}{\alpha} F_{MCLK}} = \frac{m + 1/N_{DIG}}{1/N_{AWG}}. \tag{5.14}$$

Solving for β and α, one finds

$$\beta = U \cdot N_{DIG} \tag{5.15}$$

and

$$\alpha = N_{AWG}(m \cdot N_{DIG} + 1). \tag{5.16}$$

Intrinsic noise measurement also follows a similar reasoning using Equations (3.27) and (5.10), i.e.,

$$\frac{F_{S,AWG}}{F_{S,DIG}} = \frac{U \cdot F_{MCLK}}{\frac{\beta}{\alpha} F_{MCLK}} = m + 1/N_{DIG}. \tag{5.17}$$

Solving for β and α, one finds

$$\beta = U \cdot N_{DIG} \tag{5.18}$$

and

$$\alpha = M_{DIG}(m \cdot N_{DIG} + 1) \tag{5.19}$$

where M_{DIG} has been added in to account for the number of cycles that the DIG samples. Condition for the two proposed subsampling systems are summarized in Table 5.1.

Table 5.1: Synchronization block parameters for up-converting timing system.

Function	PLL		FPLL	
	β	**α**	**β**	**α**
single-tone, Fig. 3.2	U	1	$U\,M_{AWG}\,N_{DIG}$	N_{AWG} $(pN_{DIG}+M_{DIG})$
multi-tone, Fig. 3.2	U	1	$U\,N_{DIG}$	$N_{AWG}\,(mN_{DIG}+1)$
Multi-tone PM with AWG, Fig. 3.2	U	1	$U\,N_{DIG}$	$N_{AWG}\,(mN_{DIG}+1)$
Intrinsic phase noise, Fig. 4.2	U	1	$U\,N_{DIG}$	$M_{DIG}\,(mN_{DIG}+1)$

Similar to up-converting system, down-converting system parameters are slightly different to each other. Down-converting system, down-converts a F_{MCLK} by an integer D, U variable needs to be replaced by $1/D$. Summarized of the synchronization block parameters for down-converting system are shown in Table 5.2.

5.3 Timing, Frequency, and Data Resolution

A periodic signal with unit-test period UTP_{SIG} generated by a signal generator (arbitrary or otherwise) applied to a digitizer with sampling period $T_{S,DIG}$ collects N samples over some time period, which will be called the DIG unit-time period, i.e.

Table 5.2: Synchronization block parameters for down-converting timing system.

Function	PLL		FPLL	
	β	**α**	**β**	**α**
single-tone, Fig. 3.3	*1*	*D*	$M_{AWG}\,N_{DIG}\,/\,D$	$N_{AWG}\,(pN_{DIG}+M_{DIG})$
multi-tone, Fig. 3.3	*1*	*D*	$N_{DIG}\,/\,D$	$N_{AWG}\,(mN_{DIG}+1)$
Multi-tone PM with AWG, Fig. 3.3	*1*	*D*	$N_{DIG}\,/\,D$	$N_{AWG}\,(mN_{DIG}+1)$
Intrinsic phase noise, Fig. 4.2	*1*	*D*	$N_{DIG}\,/\,D$	$M_{DIG}\,(mN_{DIG}+1)$

$$UTP_{DIG} = N \cdot T_{S,DIG} \tag{5.20}$$

Due to the periodic nature of the incoming signal, the samples collected are equivalent in y-axis value to another set within the unit-time-period of the signal, UTP_{SIG}, described by

$$UTP_{SIG} = N \cdot \Delta T \tag{5.21}$$

or

$$\Delta T = \frac{UTP_{SIG}}{N} \tag{5.22}$$

where ΔT is the effective time resolution of the subsampling process.

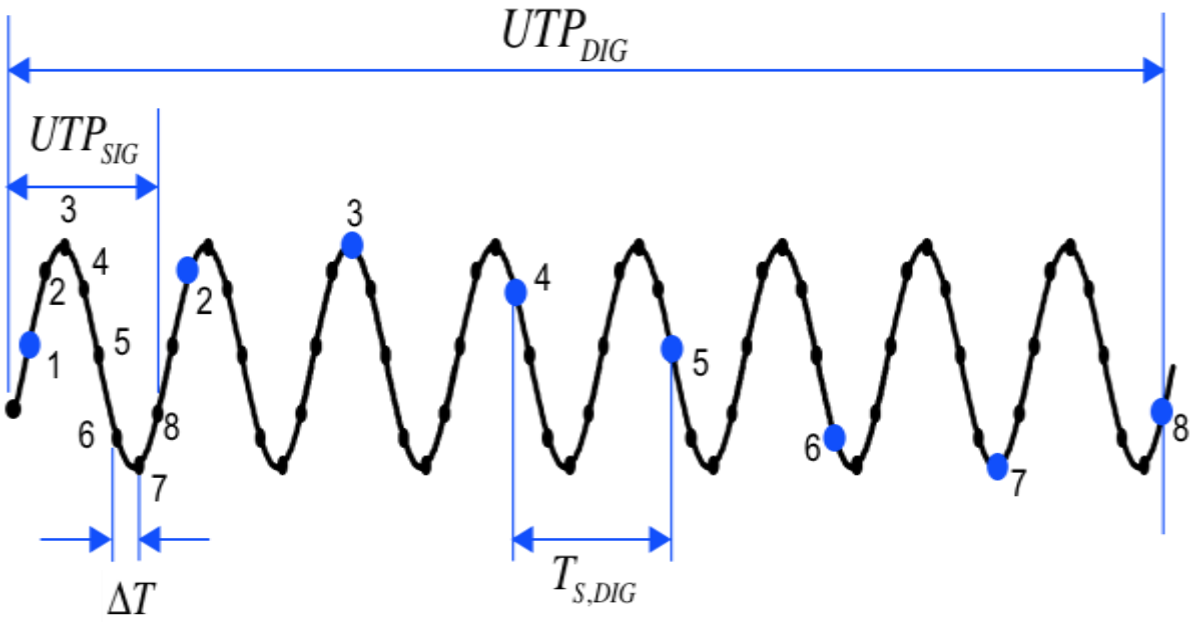

Figure 5.3: Subsampling provides an effective timing resolution much greater than the sampling period of the digitizer.

For example, in Figure 5.3, a signal with period UTP_{SIG} is produced and applied to a DIG with sampling period $T_{S,DIG}$. Here the DIG collects 8 samples over a time-period UTP_{DIG}. These are represented by the larger blue dots, labelled from 1 to 8. As is evident, these samples are equivalent to another set within the unit test period (UTP) of the signal, also labelled from 1 to 8.

It is common practice to refer to the reciprocal of the time resolution ΔT as the effective sample rate $F_{S,eff}$, i.e.,

$$F_{S,eff} = \frac{1}{\Delta T} \quad . \tag{5.23}$$

Substituting Equation (5.22) into Equation (5.23), one finds

$$F_{S,eff} = \frac{1}{\Delta T} = \frac{N}{UTP_{SIG}} . \tag{5.24}$$

For a given periodic signal, coherent subsampling provides an effective sampling rate $F_{S,eff}$ that

increases with the number of sample points, *N*.

Post-processing of the sample set involving an FFT will provide a frequency resolution describe by

$$\Delta F = \frac{F_{S,DIG}}{N} \tag{5.25}$$

The larger the size of the sample set, *N*, the finer the frequency resolution. It is interesting to note that both the time and frequency resolution increases with increasing *N*. In other words, the longer the test time the greater the amount signal information captured by the subsampling coherent process.

Another concern is the quantization error produced by the digitization process involving a D-bit ADC. The lower the ADC resolution, the greater the quantization error that is incorporated with the sample set. For example, the RMS quantization error of the ADC is

$$V_{q,RMS} = \frac{1}{\sqrt{12}} \frac{FSR}{2^D - 1} \tag{5.26}$$

where FSR is the full-scale range. As we shall see shortly, quantization issues will figure prominently in our measurements and it must be dealt with.

5.4 Summary

In this chapter the method in which to generate the sampling clocks was described. Two types of timing blocks were described. One involving an integer PLL and the other a fractional-N PLL. The integer PLL would be used to construct the up-conversion timing block and the

fractional-N PLL would be used to create the down-conversion timing block. In addition, the timing, frequency and data resolution has also been explained. It is interesting to note that both timing and frequency resolution can be improved by simply increasing the number of sampled that is being collected by the DIG. The next chapter will verify the four proposed coherent subsampling systems MATLAB/Simulink.

Chapter 6

Coherent Subsampling System Simulations

The various forms of the subsampling coherent test systems proposed in this thesis will be investigated using MATLAB/Simulink. The focus is to verify that the proposed sampling considerations leads to the correct output signal conditions, and secondly, to investigate the impact that the finite ADC resolution has on the captured signal.

6.1 Verifying the Coherent Subsampling Conditions

In Chapters 3 and 4, four separate subsampling conditions were derived for single-tone, multi-tone, a PM signal and an intrinsic noise test; three of them can be found listed in Table 3.1.

In this section, these sampling conditions will be investigated. In this section, the DIG will be assumed to be implemented with an ADC with infinite resolution, i.e., no quantization error.

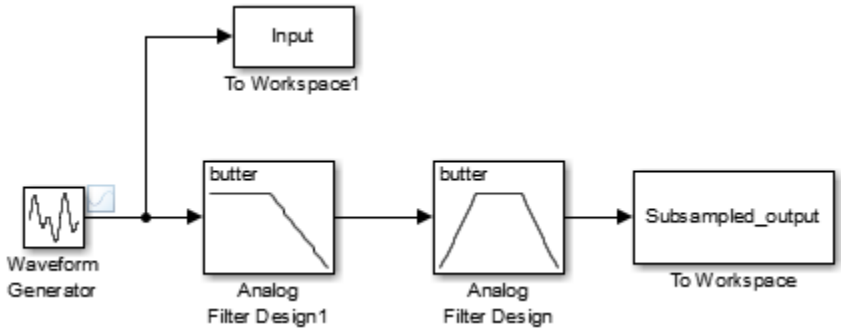

Figure 6.1: Illustrating the Simulink simulation setup of the AWG/DIG arrangement using subsampling. The low-pass filter acts as the anti-imaging filter of the AWG and the band-pass filter acts as the anti-aliasing filter for the DIG.

6.1.1 Subsampling Single-Tone Signal

To simulate the subsampling conditions for a single-tone signal using Simulink, a waveform generator is used to generate a 9.21875 MHz sine-wave with parameters M_{AWG} = 59 and N_{AWG} =256 using a sampling rate of $F_{S,AWG}$ of 40 MHz. The single tone was then passed through the anti-imaging low-pass filter with a 3-dB bandwidth of 15 MHz, and subsequently through the band-pass anti-aliasing filter with a 3-dB bandwidth of 78 kHz centered at 10.22 MHz before entering the sub-sampler. The setup used in Simulink is shown in Figure 6.1. The experiment was repeated for a wide range of amplitudes beginning with 1 μV and ending with 1 V.

The sampling clock was derived from a master clock of 10 MHz using a PLL with an up-conversion ratio of U=4. The sampling rate of the DIG was selected according to Equation (3.11) using N_{DIG} = 1024 and m = 1, resulting in $F_{S,DIG}$ = 8.7165MHz. In this way, the tone corresponding

to the DIG FFT will fall in the same bin as the AWG bin. The FPLL clocking parameters β and α were found from Table 5.1 to be 241,664 and 277,248, respectively.

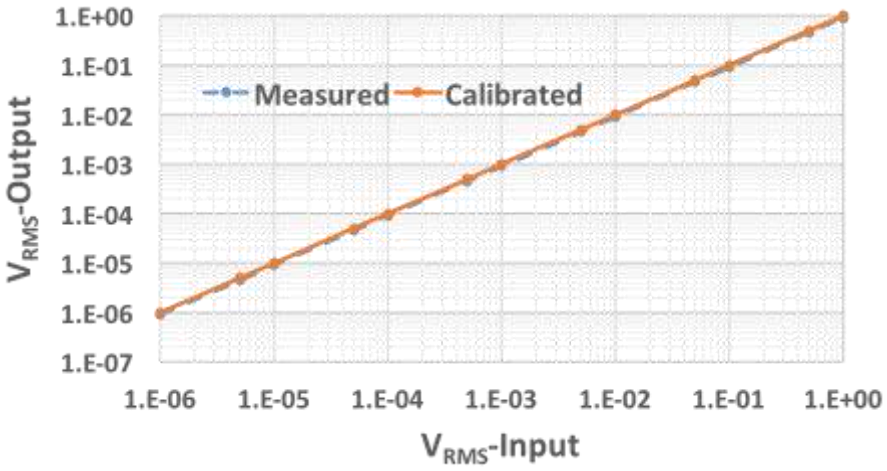

Figure 6.2: Input-Output transfer characteristic of the coherent subsampling test system for a single sine-wave at 9.21875MHz plotted on a log-log scale.

The results of the simulations are displayed in Figure 6.2 on a log-log scale before and after channel calibration. Calibration is used to correct for the power loss caused by the BP filter. As is evident from the plot, the transfer characteristic is very linear over the full range.

6.1.2 Subsampling a Multi-Tone Signal

The multi-tone signal test setup is the same as that shown in Figure 6.1 with the only difference being that the waveform generator will generate a multi-tone signal. Samples from a multi-tone signal consisting of three equal-amplitude sine waves were loaded into the AWG having parameters $M_{AWG,1}$ = 23, $M_{AWG,2}$ = 43, $M_{AWG,3}$ = 59, N_{AWG} =256 and $F_{S,AWG}$ = 40 MHz. The same DIG set-up was used as for the single-tone signal, i.e., N_{DIG} = 1024, m=1 and $F_{S,DIG}$ = 156.1 kHz

and the same front-end BP filter. The clock synchronization parameters are calculated using Equation (3.15).

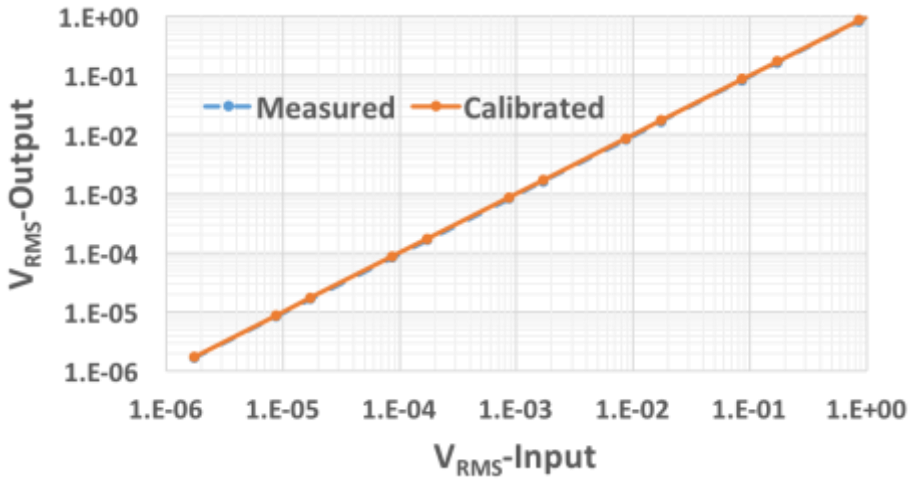

Figure 6.3: Input-Output transfer characteristic of the coherent subsampling test system for a 3-tone multi-tone signal plotted on a log-log scale.

The RMS value of each of the 3 tones were set equal, beginning with 1 μV then increased to 1 V, corresponding to a total RMS value √3 times larger. The results of the simulations are displayed in Figure 6.3 on a log-log scale before and after channel calibration. As is evident, the transfer characteristic for the multi-tone signal capture remains quite linear.

6.1.3 Subsampling a Multi-Tone PM Signal

Similar to multi-tone signal simulation test, a multi-tone PM signal simulation will use same test setup shown in Figure 6.1, except that the signal will be generated from the waveform generator. Samples from a multi-tone PM signal consisting of six equal-amplitude sine waves were loaded into the AWG having parameters $M_{AWG,\phi}$ parameters: 1, 7, 11, 17, 23 and 29, N_{AWG} =256 with $F_{S,AWG}$ = 40 MHz. The carrier frequency is set to 9.21875 MHz. The amplitude of the carrier

was set to 1 V and the RMS value of each phase tone was set to 0.01 rads. The DIG set-up has N_{DIG} = 1024 and m=1, resulting in $F_{S,DIG}$ = 156.1 kHz. A band-pass filter precedes the DIG with a 78 kHz bandwidth centered at 10.22 MHz. Using the analytic phase extraction method described in Section 4.3, the spectral coefficients of the instantaneous phase of the captured signal is shown in Figure 6.4.

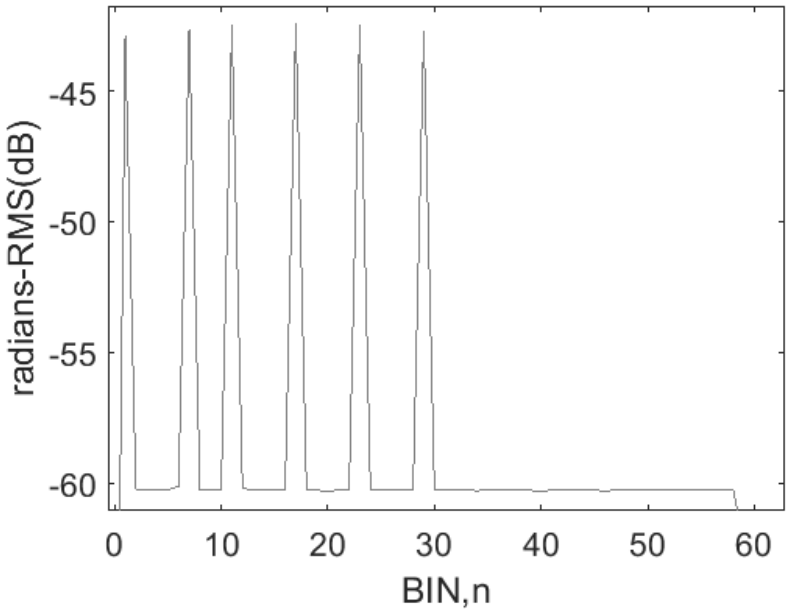

Figure 6.4: Magnitude of the spectral coefficients of the phase modulation signal.

As is evident, six tones in the appropriate FFT bins are present, with almost equal phase levels of about -43 dB. There is a slight roll-off present on account of the front-end filter. Through a calibration procedure, this error can be removed. In order to calculate the calibration factor, an input is created by generating an equal magnitude multi-tone signal and taking the ratio between input and output powers as shown in Figure 6.5. The plot is showing the magnitude response of the system, which can be used to calibrate the subsampled data that has been acquired by a data converter.

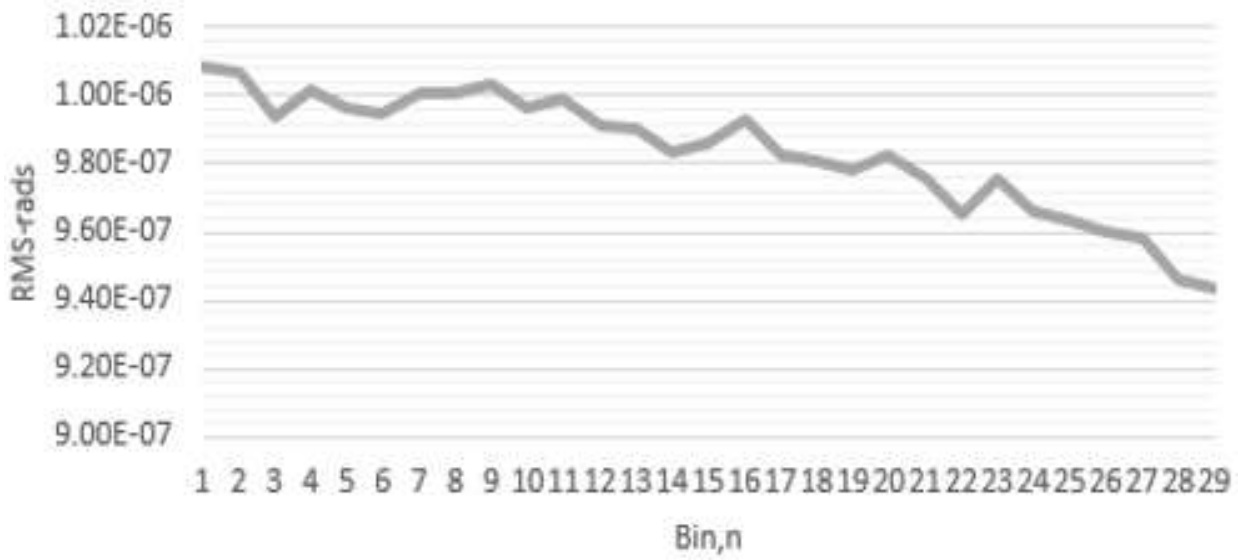

Figure 6.5: System response to equal magnitude multi-tone signal which will be used to calibrate the subsampled data.

6.1.4 Subsampling a PM Noise Signal

For PM noise signal simulation, an integer PLL was used as the DUT and band-limited noise signal was injected into the VCO input node. The VCO will take this noise and phase modulated it with respect to the input reference. A block diagram of the test setup is shown in Figure 6.6 and the corresponding Simulink test bench is provided in Figure 6.7. Since a conventional bench-top waveform generator has a PM input, this same setup is used in our simulations here. A diagram of the Simulink model used here is shown in Figure 6.8, together with the phase-modulated noise source.

An output signal produced by a PLL acting as the DUT was simulated using MATLAB/Simulink. The PLL produced an output frequency of 40 MHz according to the test setup shown in Figure 4.1 using a clock reference of 10 MHz. A wide range of white noise power was injected into the voltage control port of the PLL to simulate the noise that would be carried by the

PLL output signal. The result of this simulation is shown in Figure 6.9, together with a linear regression line to account for the repeatability of the noise measurement. As is evident, the system is behaving quite linear.

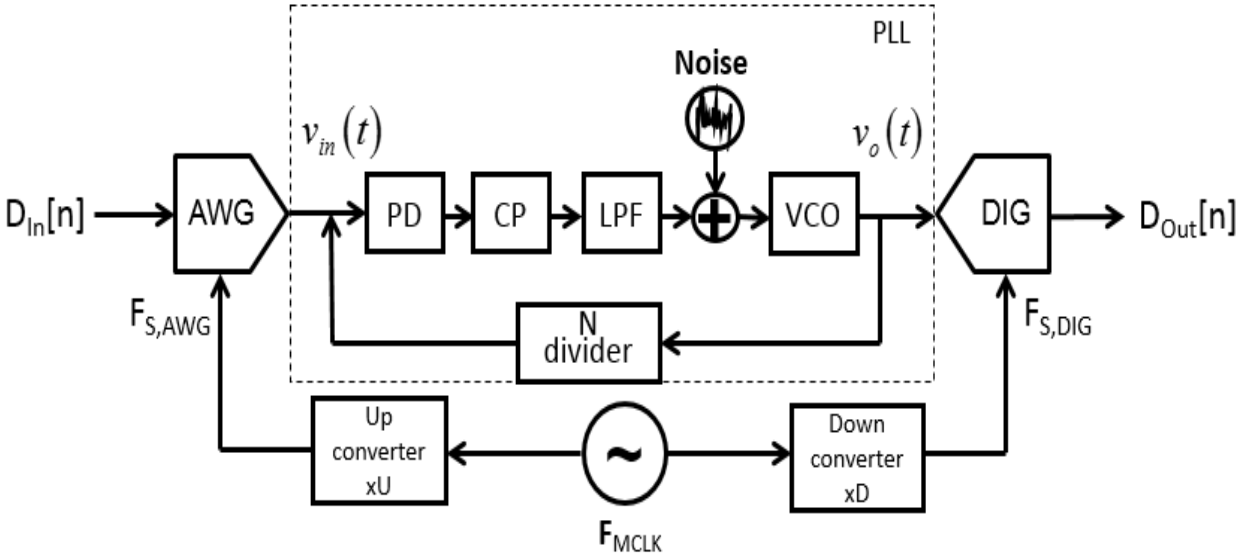

Figure 6.6: Illustrating the PM noise signal test setup with PLL as a DUT.

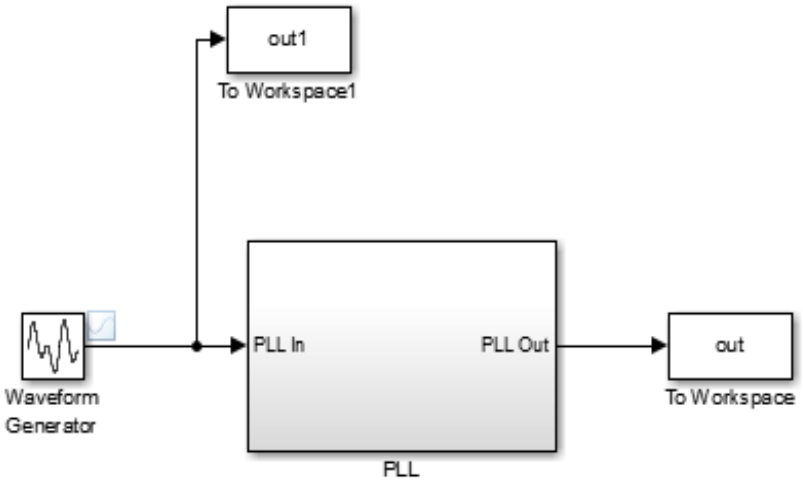

Figure 6.7: Simulink simulation setup with PLL acting as a DUT.

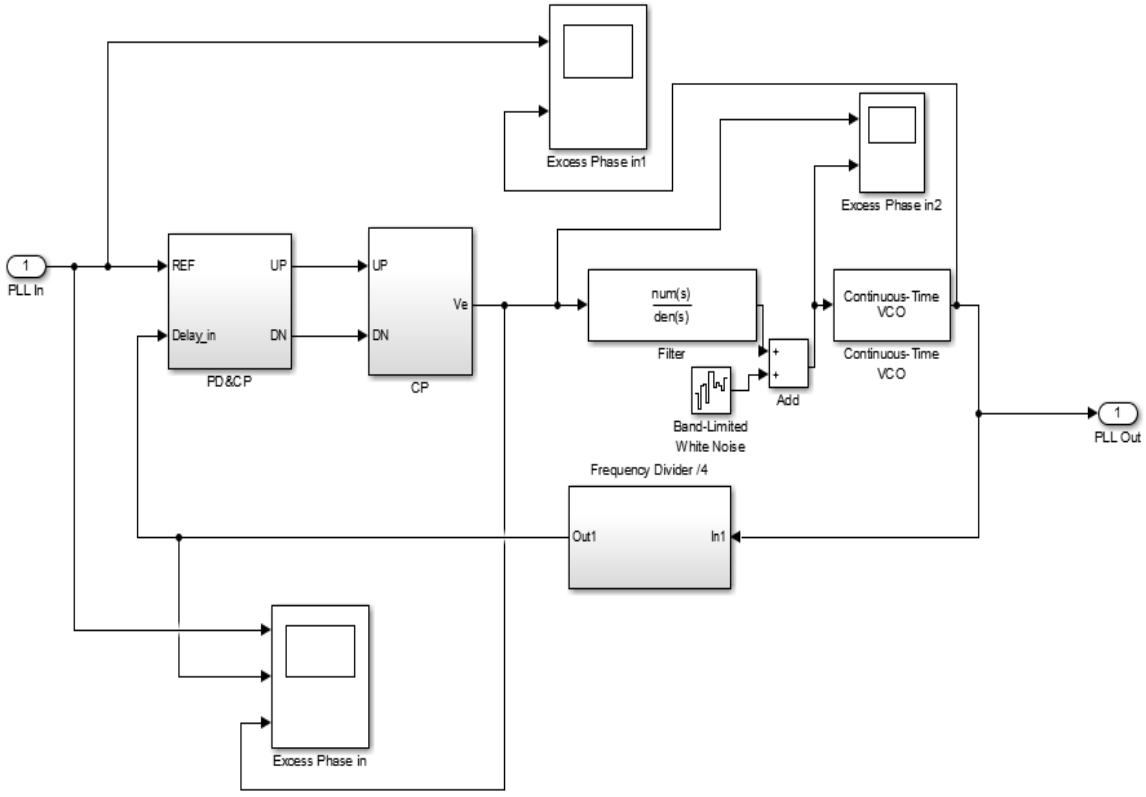

Figure 6.8: Detail view of the inside of the PLL block used in Simulink.

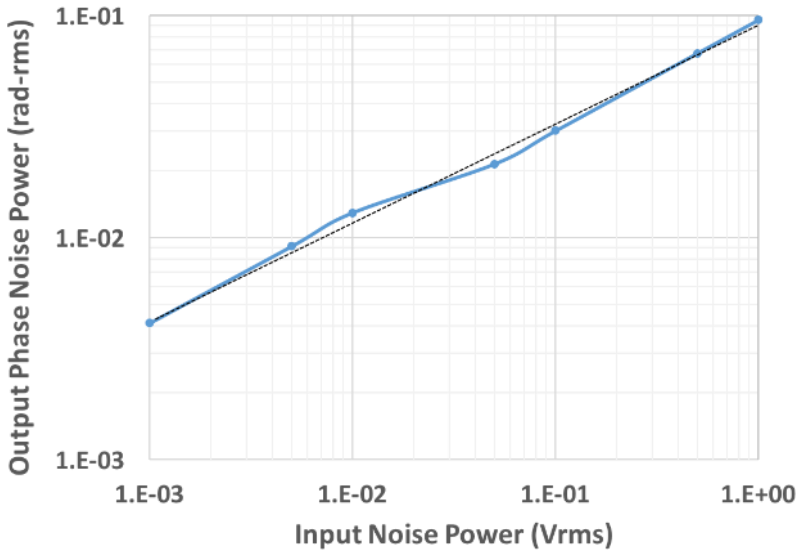

Figure 6.9: Input-Output phase noise transfer characteristic of the coherent subsampling test system.

6.2 Effects of Finite ADC Resolution on DIG Operation

Practically, a digitizer will be implemented with an ADC with finite resolution and the quantization error introduced in the measurement will impact the quality of the signal captured. In this section, the effects of ADC resolution on the measurement of a PM signal will be investigated. A PM signal is much more sensitive to ADC quantization error than a single or multi-tone signal.

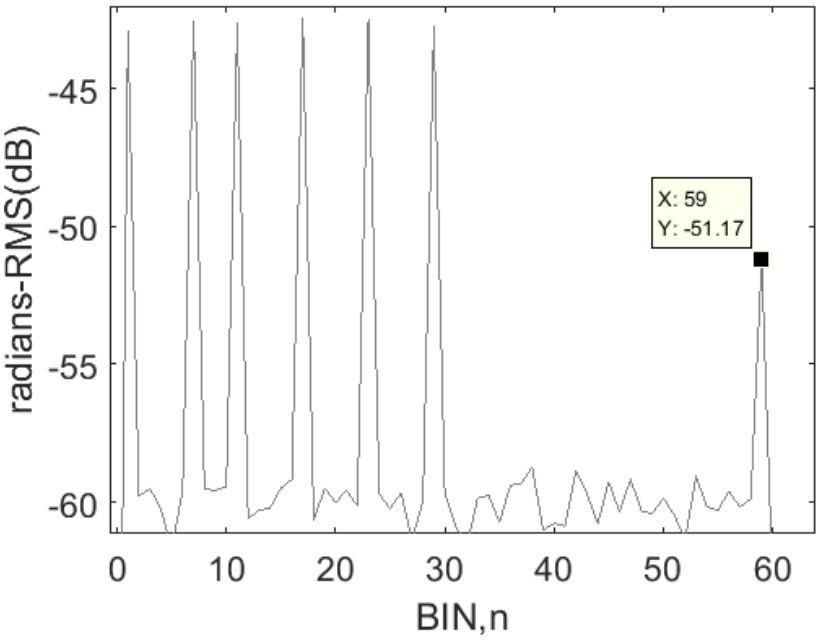

Figure 6.10: Illustrating the carrier leakage that appears in the spectrum of the phase component of the PM signal when an 8-bit ADC is used.

Using the test condition parameters used previously in Chapter 6.1.3 of this section, the spectral coefficients of the instantaneous phase of the captured signal is shown in Figure 6.10 for an ADC resolution of 8 bits. A very large tone appears in the bin where the carrier was placed ($M_{AWG,c}$ = 59). This tone will be referred to as *carrier feed-through*. The magnitude of this feed-through decreases with increasing ADC resolution. As the AWG and DIG are synchronized to the

master clock, this carrier feed-through is localized to a single bin and has no effect on the other tones. Through separate simulations, it was revealed that the measured relative error of any single tone is about 3% for a 6-bit ADC, 1% for an 8-bit ADC, and essentially 0% error for a 10-bit or higher resolution ADC.

Table 6.1: Illustrating the effect of varying sampling length on relative error.

N	ADC resolution	Programmed Aphi (V_{RMS})	Measured Aphi (V_{RMS})	Relative error (%)
512	10	0.0245	0.0285	16.3%
1024	10	0.0245	0.0257	4.9%
2048	10	0.0245	0.0246	0.41%

It is interesting to note that increasing N_{DIG} improves the relative accuracy of the measurement of the tone. For the situation depicted in Table 6.1 with a 10-bit ADC, with N_{DIG} set to 512, the relative error is about 16% without calibration and decreases to less than 1% when N_{DIG} is increased 2048 or higher.

In the case of PM noise signal, one finds the performance of the DIG is also affected by the quantization level of the ADC, but improves with sample size. For instance, in Figure 6.11, a plot of the output phase noise in rad-RMS versus the input noise level in V-RMS for data lengths of 1024 and 4096 when the DIG has 6-bits of resolution. The bandwidth was assumed to be 10 kHz. This is also compared to the infinite resolution case for N=4096. As is evident, the results greatly improve with sample length, *N*.

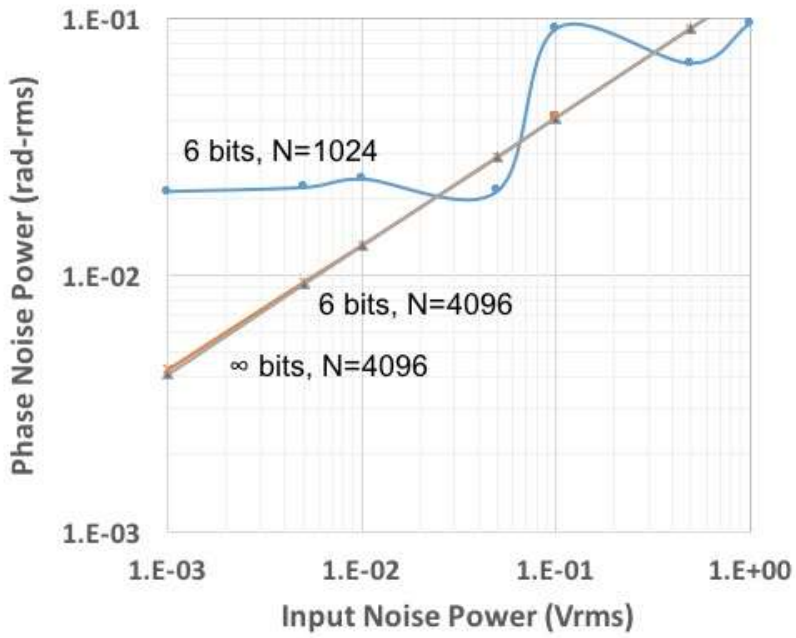

Figure 6.11: Comparison of the transfer characteristic for a DIG with 6-bits of resolution and different sample lengths, 1024 and 4096, and one with infinite resolution with 4096.

In addition, the effects of the finite ADC resolution and number of samples, *N*, has been simulated for both up-conversion and down-conversion system depicted in Figure 4.1 and 4.2, where results are shown in Figure 6.12 and Figure 6.13. In Figure 6.12, it shows that as ADC resolution increases, the relative error improves as expected, since a higher resolution ADC has lower quantization noise, resulting in less error compare to the initial input noise power. Interestingly, in Figure 6.13, a plot shows that increasing the sample length has similar effect compare to increasing the ADC resolution. Simulation results shows that increasing the sample length, can improve the resolution of the sampled signal rather than using a higher resolution ADC. .

Similar to an up-converting timing system simulation, the results of the down-converting timing system simulations are shown in Figure 6.14 and 6.15. Here one sees similar results to those found for the up-converting system simulations. The down-converting timing system also showed

improvement when the sample length *N* was increased. When the ADC resolution increased from 6 bits to 8 bits, the relative error fell to 0%. In addition, when the number of samples collected was increased, the relative error had fallen to 0% for N=2048 or higher. The relative error seems to be flat at 1% for N ranging between 256 and 1024.

6.3 Summary

In this chapter, simulation results for the four versions of the coherent subsampling system was provided. In all cases, the systems exhibited excellent linearity and the equation for selecting the sampling frequencies were confirmed to be correct. The effects of finite ADC resolution as well as finite sample lengths on measurement accuracy was investigated. The results show that higher ADC resolution or longer sample sets improve measurement accuracy; both independent on one another.

In next chapter, experimental results performed on a commercial Flex mixed-signal tester by Teradyne will be provided together with some results collect on the bench using a noise source and signal generator.

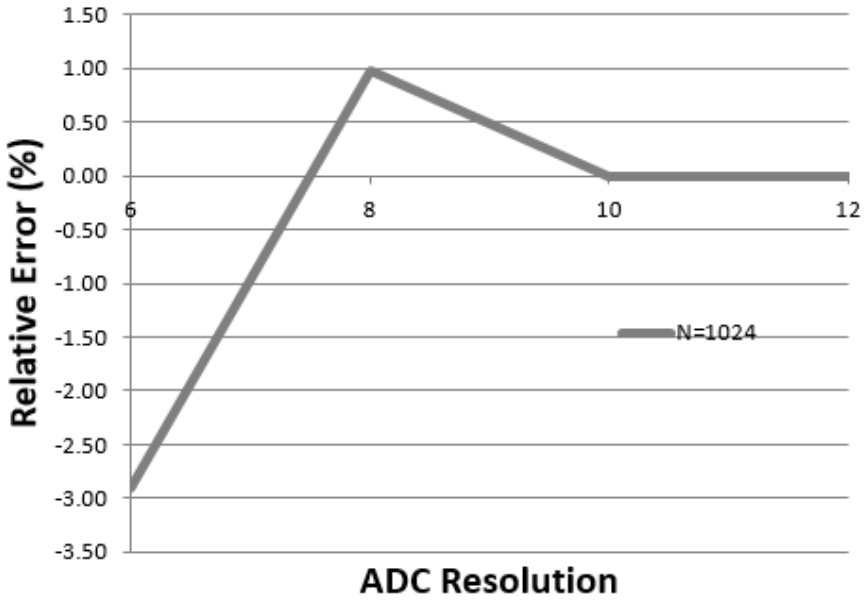

Figure 6.12: Illustrating the effects of the ADC resolution on the single-tone PM signal for up-converting system. (N=1024).

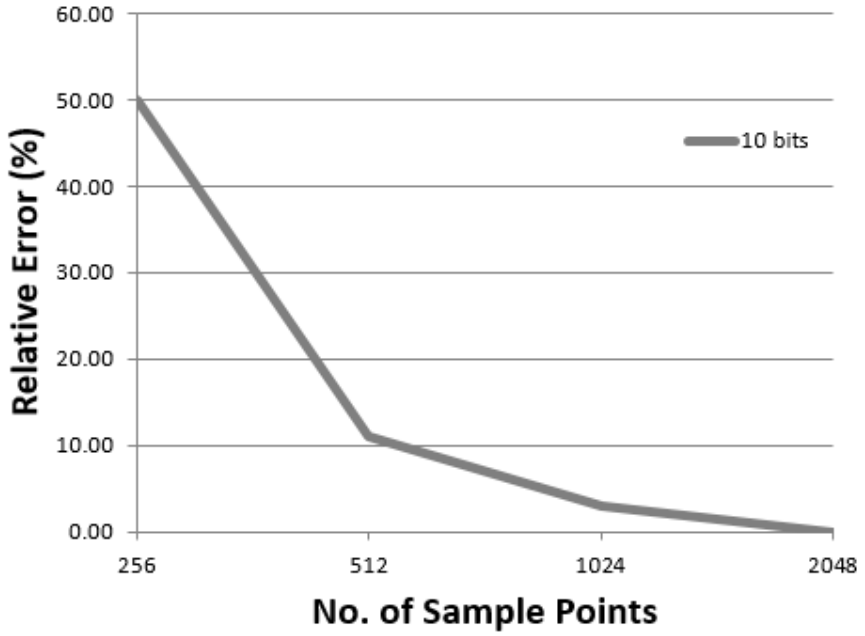

Figure 6.13: Illustrating the effects of number of sample points on sampled data resolution for single-tone PM signal for up-converting system.

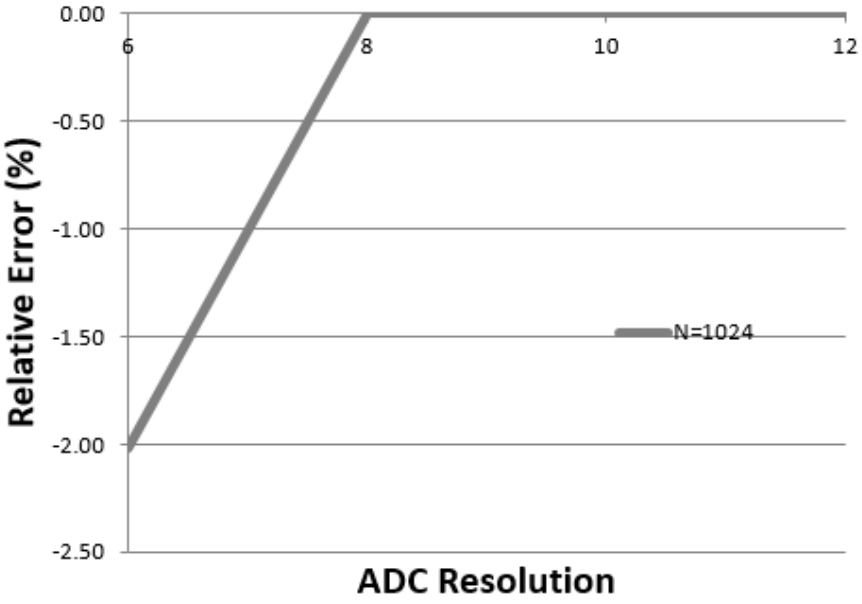

Figure 6.14: Illustrating the effects of the ADC resolution on the single-tone PM signal for down-converting system. (N=1024)

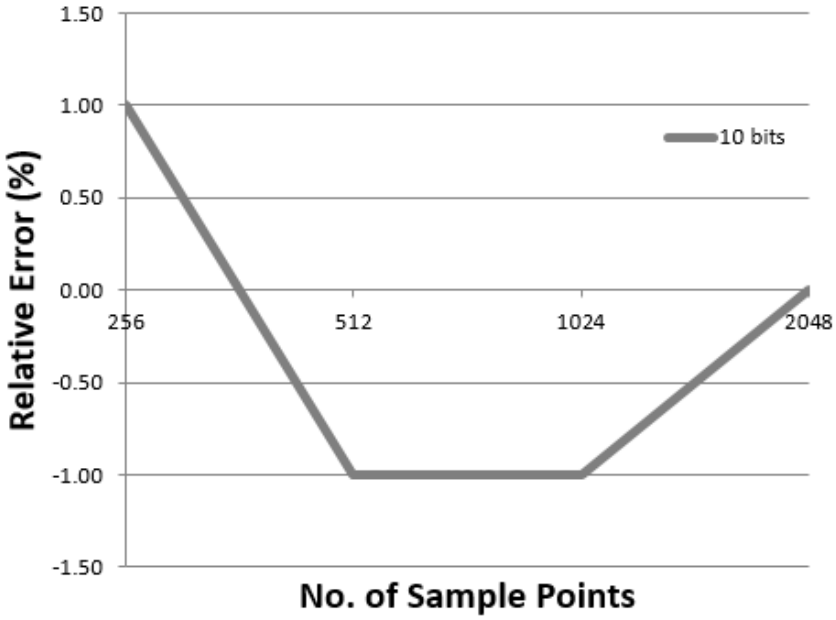

Figure 6.15: Illustrating the effects of number of sample points on sampled data resolution for single-tone PM signal for down-converting system.

Chapter 7

Experimental Validation

In this section the proposed coherent subsampling system proposed here will be experimentally investigated. Measurements will be performed using a Teradyne Flex Tester. The Flex tester uses a 16-bit DAC in the AWG and a 14-bit ADC in the DIG. A picture of this test setup is shown in Figure 7.1.

The sampling frequencies of each block is derived from the internal clocking section of the ATE. The test setup is similar to that shown in Figure 7.2. The filter after the AWG is a low-pass anti-imaging filter whose characteristics are set by the signaling conditions. This is internally set by the ATE. A BP filter is inserted in the signal path in front of the DIG; this is separate from the anti-aliasing incorporated in the DIG of the ATE. To account for the frequency response behavior of these filters, a calibration procedure is run prior to the start of any measurement. In our tests, a short circuit between the AWG and the DIG acts as the DUT. In this way, the proposed theory can be verified without any DUT concerns.

Figure 7.1: Teradyne Flex Tester used for the experimental validation measurement for the coherent subsampling method.

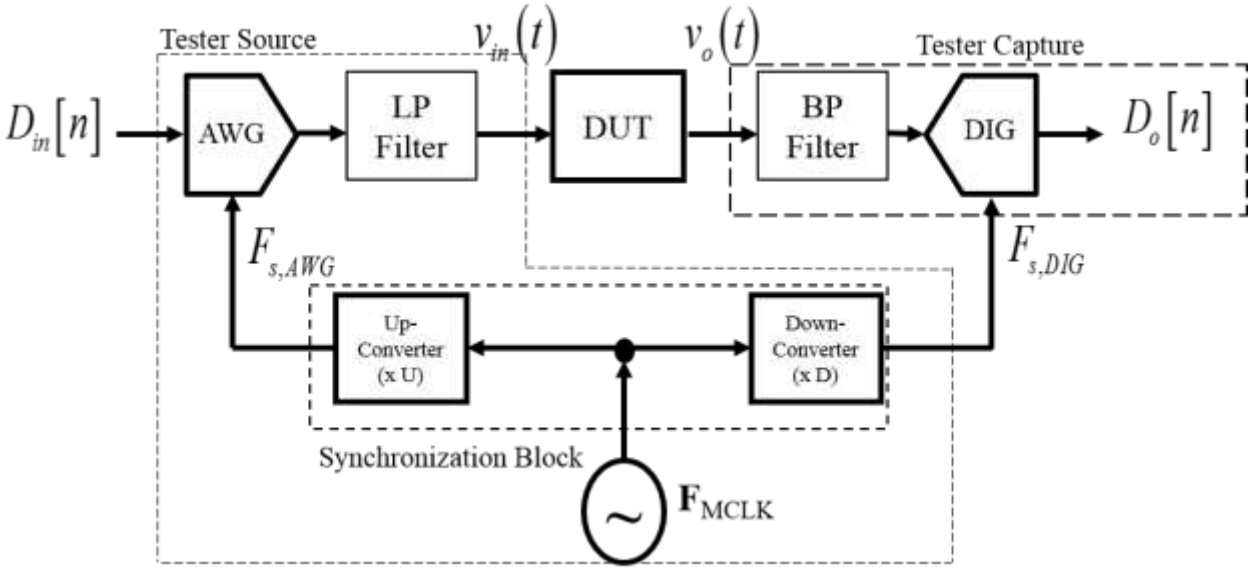

Figure 7.2: Test diagram using Teradyne tester that source and capture the signal

7.1 Subsampling a Single-Tone Signal

In this test, a single-tone sine-wave was loaded into the source memory of the AWG with the exact same parameters described previously in the simulation section. Here a tone was established in bin 59 of the AWG with a 10 mV RMS value having a sampling rate of 40 MHz. This 9.21875 MHz signal was then applied to the DIG with a sampling rate of 156.1 kHz and 1024 samples were collected in its capture memory. The subsampled signal plotted in time domain is shown in Figure 7.3 where it shows that with increase of sample length from the DIG, the time resolution of the signal increases (more definition can be seen in the plot on the right than that seen on the left).

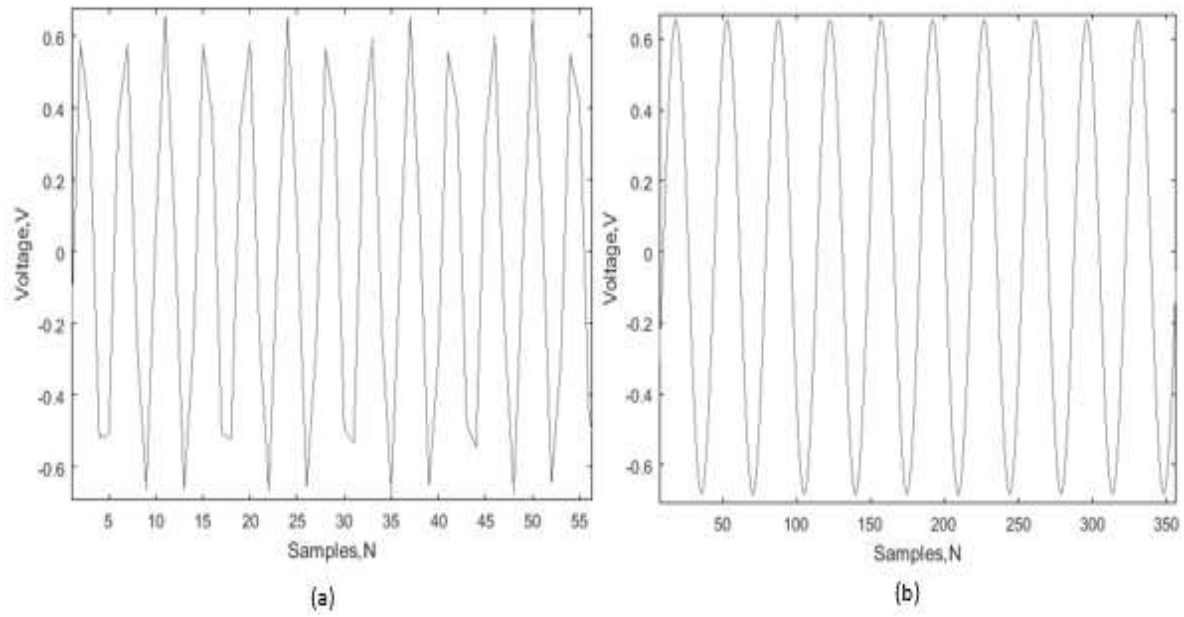

Figure 7.3: Subsampled signal plotted in time domain: (a) N=256, (b) N=2048.

The spectral coefficients of the subsampled signal over its Nyquist interval is shown in Figure 7.4. As is evident from this plot, a single tone is present in bin 59, identical to the AWG bin position, thus again confirming the proposed subsampling theory. Next, the RMS value of the

sine wave was varied from 1 mV to 1 V by the AWG and captured by the DIG. A post-processing analysis reveals the nonlinearity to be less than 1% over this input range.

7.2 Subsampling a Multi-Tone Signal

Using the same AWG and DIG clocking as the single-tone case except that the AWG is loaded with three tones in bins 23, 43 and 59 having equal amplitudes of 10 mV RMS each. The spectral coefficients of the captured signal are shown in Figure 7.5. As is evident, all three tones are present in the appropriate bins.

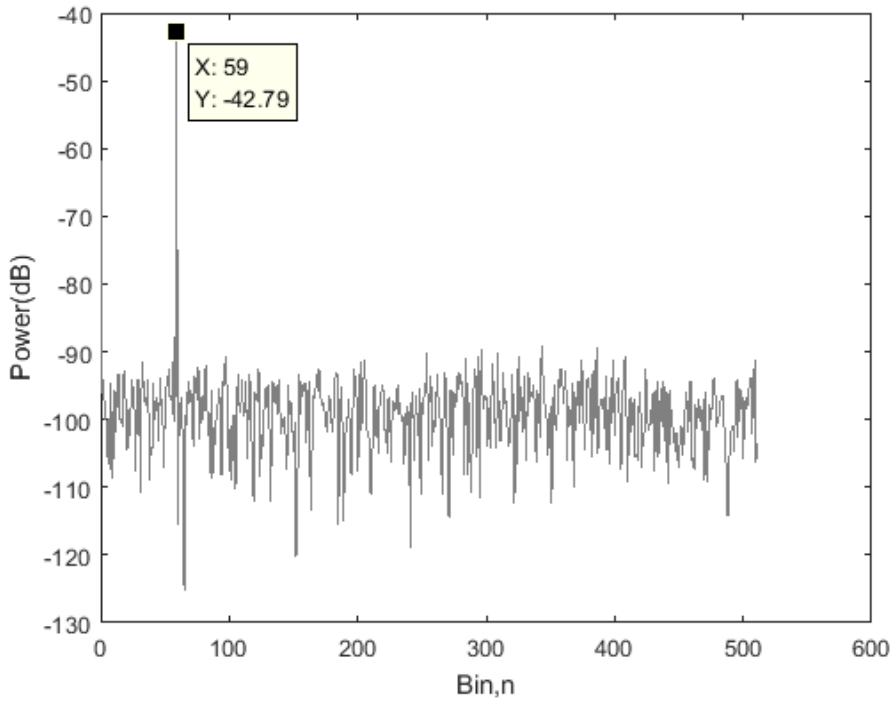

Figure 7.4: The measured spectral coefficient of a 10 mV-RMS single-tone sine-wave over its Nyquist interval (N=1024).

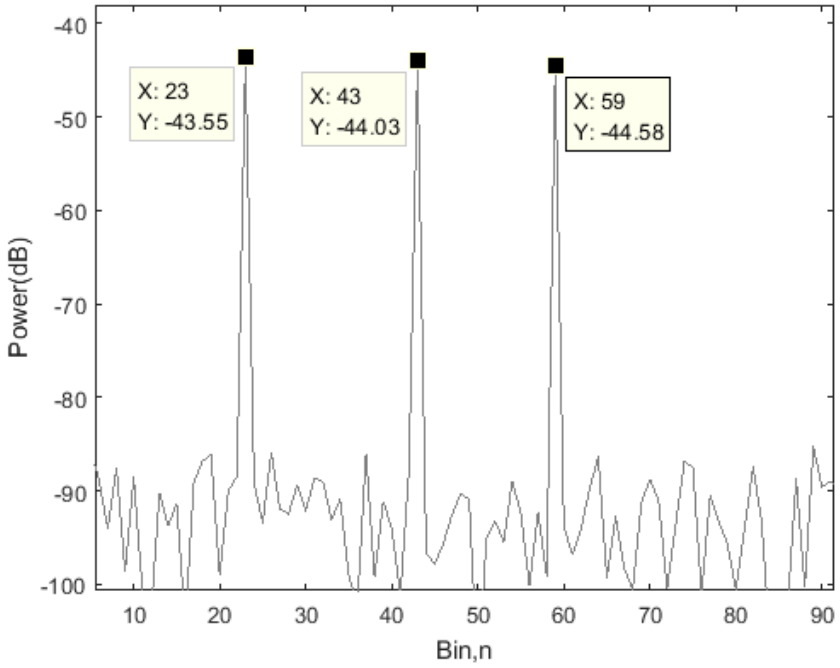

Figure 7.5: The measured coefficient of a multi-tone signal in bins 23, 43, and 59 (N=1024).

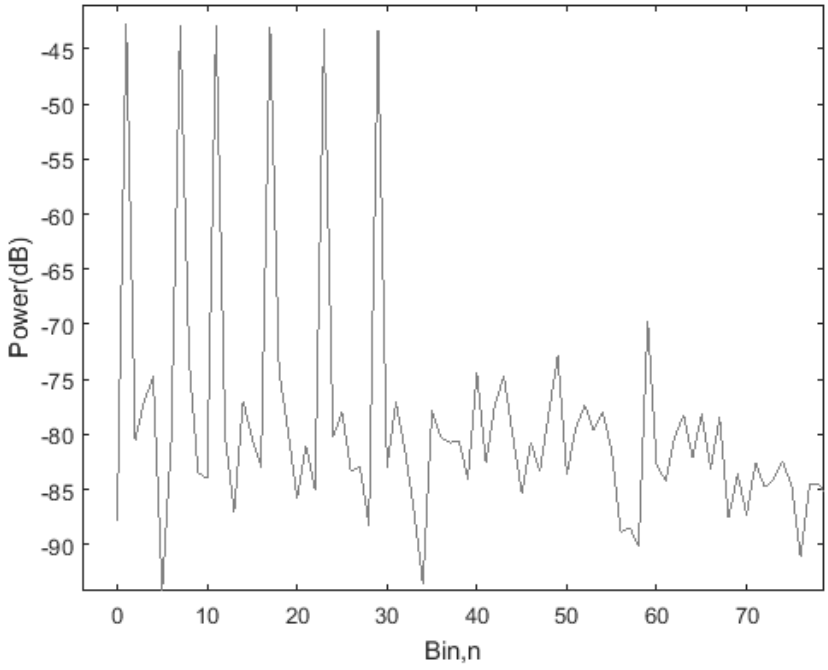

Figure 7.6: The measured spectral coefficients of a multi-tone PM signal with phase components in bins 1, 7, 11, 17, 23, and 29. The carrier was placed in bin 59 where a small carrier feed-through can be seen (N=1024).

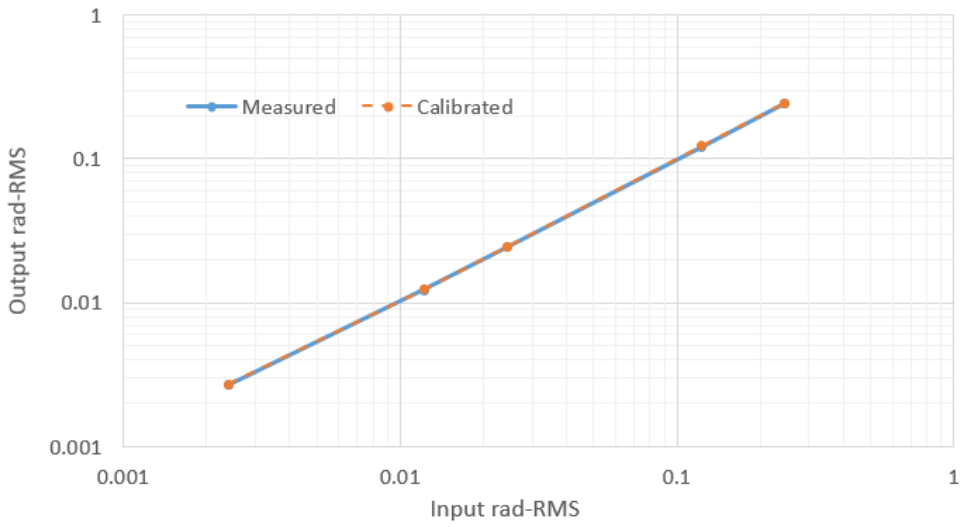

Figure 7.7: Sweep of input rad-RMS from 1 mrad-RMS to 100 mrad-RMS per tone of multi-tone PM signal.

7.3 Subsampling a Multi-Tone PM Signal

This next test involves a six-tone multi-tone PM signal. Using the same clocking parameters as for the single- and multi-tone case above, a PM signal was loaded into the source memory of the AWG with carrier bin 59 and phase tones located in bins: 1, 7, 11, 17, 23 and 29. An analysis of the spectral properties of the instantaneous phase of the DIG captured signal is shown in Figure 7.6. As is evident, all six phase components are clearly visible in their appropriate bins. A small carrier-feed-through is present in bin 59. This leakage is quite small as the ADC resolution used by the DIG is equal to 14 bits. A sweep of the input rad-RMS value of each phase component was made over a range of 1 mrad-RMS to 100 mrad-RMS per tone and the results are captured by the DIG and its relative error has been calculated. From the Table 7.1, we can observe that as PM noise V_{RMS} values increases the relative error also improves. The Figure 7.7 illustrates a very linear range of operation when multi-tone PM noise has been swept from 1 mrad-RMS to 100 mrad-RMS per tone.

Table 7.1: The comparison of programmed versus measured rad-RMS values of the multi-tone PM signal.

N	M	p	Programed Aphi (rad-RMS)	Measured Aphi (rad-RMS)	Relative error	Calibrated Aphi (rad-RMS)	Relative error
1024	59	1	0.0024	0.0027	12.5%	0.0027	12.5%
1024	59	1	0.0122	0.0123	0.81%	0.0124	1.64%
1024	59	1	0.0245	0.0244	-0.41%	0.0246	0.41%
1024	59	1	0.1225	0.1214	-0.9%	0.1226	0.08%
1024	59	1	0.2449	0.2426	-0.94%	0.2448	-0.04%

7.4 Subsampling a PM Noise Signal

Detailed diagram of the setup is shown in Figure 7.8. Here, signal is capture either using a Teradyne tester for proposed coherent sampling method or the spectrum analyzer for comparison between two results. Note that when spectrum analyzer is used to obtain the results, sampling process is not using the proposed subsampling method.

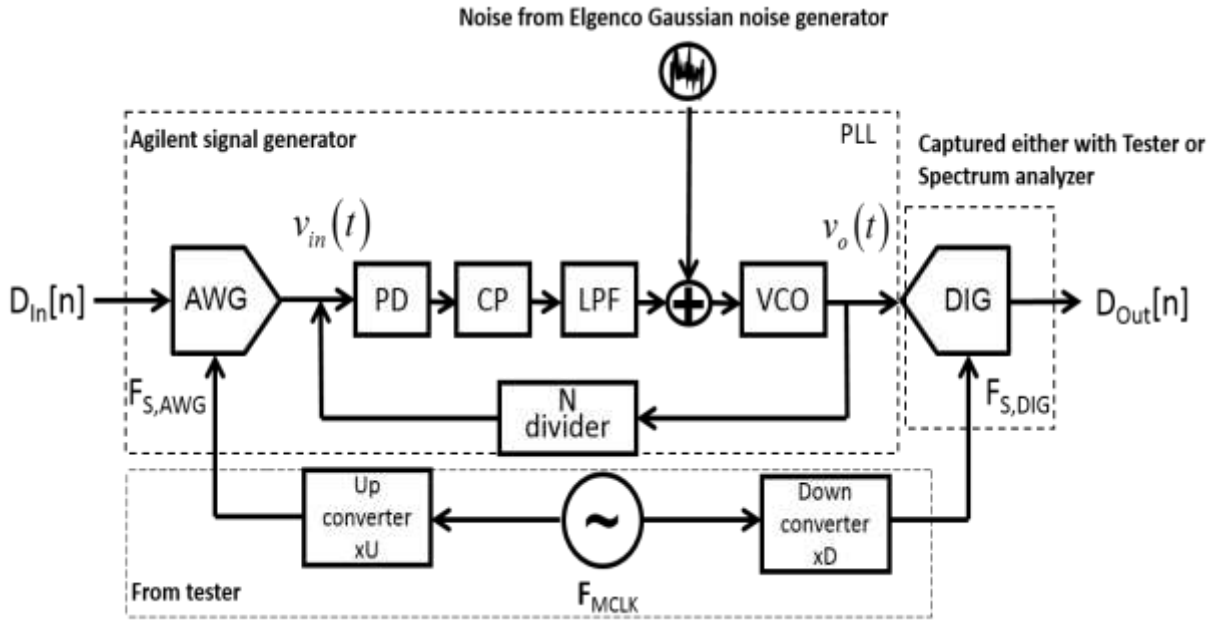

Figure 7.8: Diagram of testing no-input case where signal are captured using either the Tester or spectrum analyzer.

An Agilent 33220A signal generator (Figure 7.9) was set up to produce a PM signal with a carrier of 20 MHz with its phase modulation input connected to random noise generator. The generator was random noise signal from a Type 603-A noise generator made by Elgenco Inc. as shown in Figure 7.10. The noise signal was used to modulate the carrier ranging over an RMS range of 1 mV to 1 V. The resulting signal was then measured on an Agilent MXA N9020A Spectrum analyzer (Figure 7.11).

The corresponding output PM signal was then applied to the coherent subsampling system for measurement. Two different data lengths were used. One with a sample set of 512 points and another consisting of 2048 points. The results for these two cases are displayed in Figure 7.12.

Figure 7.9: Agilent 33220A signal generator with Modulation input.

Figure 7.10: Elgenco Inc. Model 603-A Gaussian Noise Generator.

Figure 7.11: Agilent MXA N9020A Spectrum analyzer.

For the longer data set, linear operation can be observed from about two decades of change in the input/output noise level. For inputs less than 10 mV, the output measurement saturates at an output noise level of about 30 ps. For shorter data lengths, the output saturation noise level is much higher at 300 ps and the linear range of operation reduces to a single decade change. The change in the saturation limit/linear range of operation is attributed to jitter-induced quantization noise effects associated with the digitizer.

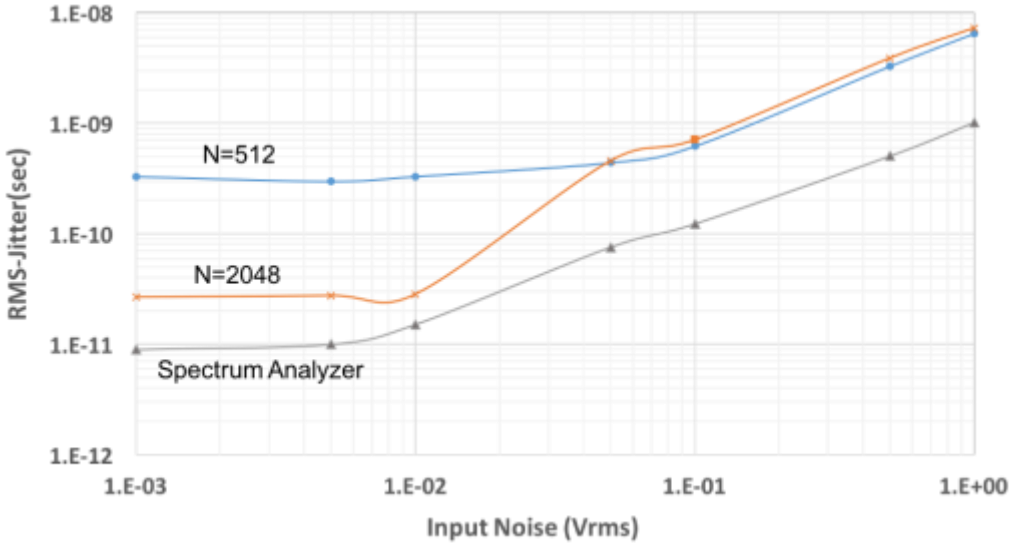

Figure 7.12: Output RMS phase noise power (jitter) versus input noise power injected into VCP port of an Agilent 33220A voltage-controlled oscillator and measured using the proposed coherent subsampling technique. The results are also compared to those found using the results captured by a spectrum analyzer.

For comparison, the phase noise over a 10-kHz bandwidth associated with each PM signal was measured using an Agilent MXA N9020A spectrum analyzer. While the absolute noise levels are different, the shapes are almost identical. Calibrations can be used to fix these differences.

7.5 Summary

In this chapter, we have measured single-tone, multi-tone, multi-tone PM, and intrinsic noise signals using coherent subsampling along with the phase extraction method. Throughout the chapter, the results were close to what we have seen in with the simulations. There still exists difference in phase noise results between spectrum analyzer versus subsampling with phase extraction method, which should be investigated in more detail in the future.. Despite the differences, similar linear behavior has been observed between the two methods, which shows promising future for the coherent subsampling method for high-speed signal measurements for both amplitude and phase noise based measurements tests.

Chapter 8

Conclusion

8.1 Conclusion

In this thesis, coherent subsampling test system has been proposed very first time. This system was shown to be able to measure a wide range of signal types, such as a single-tone or multi-tone sine-waves and PM noise signals. Coherent sampling system has been explained in **Chapter 2**, where many useful practices was presented, such as selecting a mutually-prime bins, randomizing the phase for multi-tone signal, and modulo time plot. The latter can greatly help to visualize the signal whose fundamental bin is close to N/2. A coherent subsampling was presented in **Chapter 3**. Here, it was shown how single-tone, multi-tone, and multi-tone PM signals could be measured in an accurate manner. Coherent constraints for different signal types was formulated. If such conditions are not fulfilled, then it will lead numerous errors such as aliasing, frequency leakage, timing resolution. In **Chapter 4**, an intrinsic noise measurement has been discussed with analytic signal, using a Hilbert transform, which can be used to calculate the excess instantaneous

phase of a periodic signal. This technique is extremely valuable for measuring the phase noise of a signal, i.e. jitter. **Chapter 5**, outline the circuits used to create the sampling clocks of the coherent subsampling system. This involved the application of an integer-based PLL and a fractional-N PLL. In addition, a brief look at the time and frequency resolution of a coherent subsampling system was provided, together with the impact of ADC finite resolution on a measurement. It was interesting to observe that the improvement of time resolution can be increased by using a larger sized data set, N. The effect of quantization noise can be improved by using a higher resolution ADC. Finally, **Chapters 6 and 7** provided validation data in the form of numerical simulations using MATLAB/Simulink together with experimental data derived from a production-oriented mixed-signal tester. With the obtained results from both simulation and experimental, we can conclude that the proposed coherent subsampling can be very useful in testing high-speed communications systems.

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