Lateral Liquid-Phase Epitaxy Growth of SiGe Epilayers on Si with Asymmetric Strain and Low Threading Dislocation Densities

Andrew O'Reilly

Department of Mining and Materials Engineering
Faculty of Engineering
McGill University
Montreal QC Canada

December 13, 2017

A thesis submitted to McGill University in partial fulfilment of the requirements of the degree of Doctor of Philosophy

Abstract

The replacement of Si as the material for high mobility channels in next-generation MOSFETS is required to ensure continued device improvement as the benefits from further miniaturisation are diminishing. Uniaxially strained $Si_{1-x}Ge_x$ channels have been proposed as a replacement material for high mobility channels since SiGe has lower electron hole effective masses than Si, which increases the carrier mobility. In addition, uniaxial compressive strain further increases the hole mobility in pMOSFET devices, and the strain enhanced mobility effect is more pronounced for uniaxial strain than bi-axial strain. However, there is not a well-established technique for the fabrication of a high quality SiGe virtual substrates with compressive uniaxial strain. Previously proposed techniques to deposit uniaxially strained $Si_{1-x}Ge_x$ epilayers on Si (001) substrates require multiple deposition steps and only yielded thin strips of uniaxially strained films.

In this thesis, a novel lateral liquid-phase epitaxy (LLPE) technique was developed which allows for the growth of SiGe epilayers on Si (001) substrates with asymmetric strain and low threading dislocation density. The lateral growth produces arrays of parallel misfit dislocations, aligned in the [110] growth direction through the distinction of the critical thicknesses for dislocation glide (h_G) and nucleation (h_N). Dislocations are nucleated in a seed region where the epilayer thickness is greater than h_N and h_G such that the epilayer is relaxed by a combination of dislocation nucleation and glide which forms an orthogonal network of <110> misfit dislocations. As the film is propagated laterally, the thickness is reduced below h_N, such that misfit dislocations which were nucleated in the seed region can glide into the laterally propagating film but the nucleation of new dislocations is inhibited, which results in an array of parallel misfit dislocations. This permits, for the first time, the observation of separate critical thicknesses for the two strain relaxation mechanisms.

The parallel array of misfit dislocations results in asymmetric strain relaxation, where the film is fully strained in the [110] direction and 31 % strain relaxed in the $[1\bar{1}0]$ direction. This is the first report of asymmetric strain relaxation in a blanket film on Si (001). In addition, the inhibition of dislocation nucleation favours the formation of long misfit dislocations by glide, which reduces the threading dislocation density to $10^3/cm^2$, which is two orders of magnitude lower than the seed area.

Sommaire

Afin de permettre l'amélioration continue des transistors MOSFETs à haute mobilité d'électrons, le remplacement du silicium comme matériau composant les canaux des transistors est nécessaire puisque les améliorations de performance venant de la miniaturisation diminuent. Le $Si_{1-x}Ge_x$ sous tension uniaxiale a été proposé comme matériau de remplacement au silicium puisque le SiGe possède une masse effective de trous plus faible que le silicium ce qui contribue à augmenter la mobilité des porteurs de charge. De plus, une tension uniaxiale compressive contribue également à l'augmentation de la mobilité des trous dans des dispositifs pMOSFET. Cependant, il n'existe pas de technique de fabrication bien établie permettant la croissance de substrats virtuels de SiGe de haute qualité possédant une tension compressive. À ce jour, les techniques proposées afin de déposer une couche épitaxiale de $Si_{1-x}Ge_x$ sous tension uniaxiale, sur substrat de Si (001), requiert plusieurs étapes de déposition qui n'ont seulement résulté en la fabrication de bandes minces de film.

Dans cette thèse, une nouvelle technique de croissance épitaxiale latérale en phase liquide est développée et permet la croissance de couches minces de SiGe en tension asymétrique possédant une faible densité de dislocations traversantes sur substrat de Si (001). La croissance latérale produit des rangées parallèles de dislocations inadaptées alignées dans la direction de croissance [110] via la distinction entre l'épaisseur critique de couche minces pour le glissement (h_G) ou la germination (h_N) d'une dislocation. Les dislocations sont d'abord créées dans un site de germination où l'épaisseur de la couche épitaxiale est plus grande que h_G et h_N permettant ainsi de relaxer la couche via une combinaison de germination et de glissement de dislocations, formant ainsi un réseau orthogonal de dislocations inadaptées <110>. Lorsque le front de croissance de la couche se propage, l'épaisseur de la couche diminue et atteint éventuellement une épaisseur plus petite, h_N; à ce stade, les dislocations créées dans la zone de germination peuvent encore glisser mais la production de nouvelles dislocations n'est plus possible résultant alors en la formation de rangées parallèles de dislocation inadaptées. Ceci permet, pour la première fois, l'observation d'épaisseurs critiques différentes pour ces deux mécanismes de relaxation de tension.

Le réseau parallèle de dislocations inadaptées résulte en une relaxation asymétrique de la tension où le film est sous tension dans la direction [110] mais relaxée par 31% dans la direction $[1\bar{1}0]$. Ceci représente la première observation de relaxation asymétrique d'un film épitaxial sur Si (001).

De plus, l'inhibition de la germination de dislocations avantage la formation de longues dislocations inadaptées par glissement ce qui réduit la formation de dislocations traversantes à une densité de $10^3/cm^2$, soit deux ordres de grandeurs plus petit que dans la zone de germination.

Acknowledgments

I would first like to thank my supervisor, Professor Nate Quitoriano, whose support and guidance was essential to the completion of this thesis. Thank you for all our meetings, for the countless drafts that you revised and for all the advice and encouragement that you provided throughout this project. There were significant hurdles to overcome; without your patience and encouragement, this work would not have been possible.

I would like to thank my research group colleagues, Jerome LeBoeuf, Alexandre Horth, Jun Wang, Wheizhen Wang, Han Wang and Moshen Keshavarz for their input, questions and support. Jerome provided the initial design of the LPE system that was modified for my LLPE system. Alexandre provided the French translation of the thesis abstract. Special thanks go to Jun, with whom I developed and shared the LPE furnace and who developed the etch pit density process, as well as long discussions on techniques, characterization and results.

I would also like to thank the following members of the McGill staff for their advice, support and knowledge. Graduate Coordinator Barbara Hanley for all of her assistance navigating the graduate student life. Monique Riendeau for access to the wet benches for chemical etching. Florence Paray for their training and support on the scanning electron microscope. Don Berry and Jun Lee of the McGill Nanotools Microfab for their assistance with technique and know-how on vacuum pumps, leak detection and other techniques. Mohini Ramkaran for training and assistance on the atomic force microscope. Nima Nantegi, from École Polytechnique for training and assistance on the X-ray diffractometer.

I would like to thank McGill University and NSERC for providing my funding.

Most importantly, I would like to thank my family and friends for supporting me through this long journey. To my parents, Lorie and Richard O'Reilly, who supported and encouraged my academic aspirations from the very beginning, and my wife Kate and son William, who shared with me the exciting times of new discoveries and optimism and supported me through the most difficult days of failed experiments and broken equipment, it is to them, for their unconditional love and support, that I dedicate this work.

Table of Contents

List of Figures

List of Tables

List of Acronyms

AFM	**A**tomic **F**orce **M**icroscopy
BSE	**B**acks**s**cattered **E**lectrons
BOX	**B**uries **O**xide **L**ayer
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CMP	**C**hemical **M**echanical **P**olishing
CVD	**C**hemical-**V**apour **D**eposition
EDS	**E**nergy **D**ispersive **S**pectroscopy
ELO	**E**pitaxial **L**ayer **O**vergrowth
EPD	**E**tch **P**it **D**ensity
FM	**F**rank-van der **M**erwe
HELO	**H**etero**e**pitaxial **L**ayer **O**vergrowth
IEE	**I**nterfacial **E**nergy **E**pitaxy
ITRS	**I**nternational **T**echnology **R**oadmap for **S**emiconductors
LPE	**L**iquid-**P**hase **E**pitaxy

LLPE	**L**ateral **L**iquid-**P**hase **E**pitaxy
MBE	**M**olecular **B**eam **E**pitaxy
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
RLP	**R**eciprocal **L**attice **P**oint
RMS	**R**oot **M**ean **S**quare
RSM	**R**eciprocal **S**pace **M**ap
SE	**S**econdary **E**lectrons
SEM	**S**canning **E**lectron **M**icroscopy
SGOI	**S**trained Silicon-**G**ermanium **o**n **I**nsulator
SIMOX	**S**eparation-by-**Im**plantation of **Ox**ygen
SK	**S**transki-**K**rastanov
SOI	**S**ilicon **o**n **I**nsulator
SSOI	**S**trained **S**ilicon **o**n **I**nsulator
TEM	**T**ransmission **E**lectron **M**icroscopy
XRD	**X**-**R**ay **D**iffraction
VLS	**V**apour-**L**iquid-**S**olid
VPE	**V**apour-**P**hase **E**pitaxy
VW	**V**olmer-**W**eber

Contribution of Authors

This thesis was written entirely by A. O'Reilly and reviewed by N. Quitoriano. Part of the work presented in this thesis has been, or will be, published elsewhere. Parts of each publication are reproduced in Chapter 5, the experimental results from each publication are reproduced in Chapter 7 and Chapter 8, respectively.

1. A. O'Reilly, N. Quitoriano, *Asymmetric, compressive, SiGe epilayers on Si grown by lateral liquid-phase epitaxy utilizing a distinction between dislocation nucleation and glide critical thicknesses.* Journal of Crystal Growth, 2018. **482**: p. 15-22.
2. A. O'Reilly, N. Quitoriano, *Reduction of Threading Dislocation Density in SiGe Epilayer on Si (001) by Lateral Growth Liquid-Phase Epitaxy*. Journal of Crystal Growth, (Accepted December 7, 2017).

In 1, A. O'Reilly designed the LLPE system, performed the crystal growth experiments, did the XRD, AFM and SEM characterization, analysed the results and wrote the paper. N. Quitoriano provided guidance and co-wrote the paper.

In 2, A. O'Reilly designed the LLPE system, performed the crystal growth experiments, did the XRD, AFM, EPD and SEM characterization, analysed the results, and wrote the paper. N. Quitoriano provided guidance and co-wrote the paper.

Statement of Originality

This thesis provides important contributions to the field of strain relaxation in heteroepitaxial growth of SiGe virtual substrates. The four primary contributions are listed here:

1. A lateral liquid-phase epitaxy (LLPE) growth technique has been designed, assembled and developed to deposit large area lattice mismatched epilayers. Previous lateral growth techniques required the overgrowth of epilayers on a masked substrate, such as epitaxial layer overgrowth. Direct lateral growth of lattice mismatched materials has previously only been accomplished by guiding the lateral growth of nanowires. The lateral growth is accomplished by coupling the slider of a modified sliding boat LPE system to a stepper motor, such that the growth substrate is moved slowly through the growth solution during growth. This creates a growth front which propagates laterally across the substrate.
2. LLPE growth on Si (001) produces a epilayer which transitions from an orthogonal network of <110> misfit dislocations to an array of parallel misfit dislocations aligned in the [110] growth direction due to a thickness gradient in the growth direction which allows the distinction of the critical thickness for dislocation nucleation and the critical thickness for dislocation glide. This is the first report of the direct observation of these two critical thicknesses and provides a pathway to determine the energetics and mechanism of the dislocation nucleation processes.
3. The array of parallel misfit dislocations provides asymmetric strain relaxation given that the misfit strain is only relaxed in the direction perpendicular to the dislocation line direction. As a result, the epilayer is fully strained in the [110] growth direction and strain relaxed in the $[1\bar{1}0]$ direction. This is the first report of an array of parallel misfit dislocations on a Si (001) substrate and the first report of asymmetric strain in a blanket film on Si (001).
4. The inhibition of dislocation nucleation permits the glide of long misfit dislocations. As a result of the long misfit dislocations, the threading dislocation density in the lateral growth region is two orders of magnitude lower than in the seed area. This shows, for the first time, that lateral growth can be used to grow high-quality lattice mismatched films over a large area.

Chapter 1

Introduction

1.1. Motivation

For the past several decades, the steady miniaturisation of metal-oxide-semiconductor, field-effect transistors (MOSFETs) has driven the continual improved performance of integrated circuits (ICs). The MOSFET miniaturisation and performance trend was first observed in Moore's law [1, 2]. However, as the transistor gate length reduced to sub-micron lengths, significant hurdles to increasing device performance have emerged, such as short-channel effects, velocity saturation, large leakage current and dielectric breakdown [3]. Increasing the mobility of carriers in strained MOSFET channels has been identified as an important technique to continue device performance improvements. The strain-enhanced mobility increases the injection carrier velocity and results in higher drive current at velocity saturation [4].

Strain-enhanced-mobility channels were adopted for the 90 nm node technology. Compressive strain was introduced into the channel by substituting SiGe as the source and drain material. Given the larger lattice constant of partially relaxed SiGe, the source and the drain exert a compressive stress on the channel. The impact on mobility from the processed-induced strain was significant. For example, uniaxial compressive stress increased the hole mobility by a factor of 2 at the 65 nm node technology [5]. As IC technology progresses beyond the 14 nm node, introduced in 2014, towards sub 10 nm nodes, significant technological challenges must be addressed. As the current

density continues to increase with each generation, the demand for lower resistance channel materials increases. Enhanced mobility in Si from process-induced strain is expected to saturate and the replacement of strained Si with a higher mobility channel material is required to further improve device performance.

The International Technology Roadmap for Semiconductors (ITRS) highlights Ge as the preferred replacement for high mobility channels [6]. Ge has a lower electron effective mass than Si, as well as lower heavy and light hole effective masses. As a result, Ge has higher carrier mobility than Si. Recently, uniaxial-strained Ge was shown to have the highest observed hole mobility of any p-type material [7]. However, due to the large cost and smaller size of single crystal Ge substrates, $Si_{1-x}Ge_x$ and Ge virtual substrates on Si are required to lower the device cost.

SiGe epilayers on a Si (001) substrate with lattice mismatch of less than 2 % are known to relax by the nucleation and glide of 60˚ dislocations which form an orthogonal network along the <110> directions [8]. This forms the crosshatch morphology, characterized by an orthogonal network of ridges and troughs which lies above the underlying misfit dislocation network. In contrast to misfit dislocations which create the crosshatch morphology, a threading dislocation is the segment extending from the substrate/film interface where a misfit dislocation resides to the film/ambient interface. Threading dislocations do not contribute significantly to misfit strain relaxation and their density must be kept below $10^6/cm^2$ [9] to allow for proper device performance given that these defects act as scattering sites and recombination sites for electrons and holes.

Strategies to reduce the threading dislocation density include the fabrication of graded buffers [10, 11], epitaxial layer overgrowth (ELO) [12-14] and small area growth [15]. Graded buffers, with their small lattice mismatch at each layer, reduce the threading dislocation density by encouraging the misfit dislocations to glide along the interface of low misfit layers. ELO films are nucleated in a seeding window and grow laterally over a masking oxide layer. Misfit and threading dislocations are confined to the seeding window which allows for defect-free films which lie above the oxide mask. The small area growth technique deposits a misfit epilayer on a patterned substrate, such that the distance for a misfit dislocation to glide to the edge of the epilayer is small. This allows the dislocations to terminate at the edge of the epilayer and not as a threading dislocation. However, these techniques have their disadvantages. Graded buffers require thick films, often ~10 μm to accommodate a 4% lattice mismatch, ELO sacrifices the epitaxial connection between the epilayer

and the substrate and the useful surface is limited by the patterning required for ELO and small area growth.

1.2.Scope and Organization

The objective of this thesis is to develop a lateral liquid-phase epitaxy growth technique to deposit high-quality SiGe thin films with asymmetric strain over large areas. This thesis introduces a novel lateral liquid-phase epitaxy (LLPE) technique which was constructed and developed at McGill. The LLPE technique was developed to deposit SiGe films with asymmetric strain and low threading dislocation densities on Si (001) substrates.

An in-depth review of the relevant literature for the development and understanding of the LLPE technique is presented in the first four chapters of the thesis. First the theory of misfit strain relaxation in the SiGe system is presented in Chapter 2, including the theory of dislocation nucleation. Second, the benefits of uniaxial strain in SiGe for continued MOSFET improvement and the techniques used to produce SiGe virtual substrates with uniaxial strain is presented in Chapter 3. Chapter 4 provides an overview of the field of SiGe LPE growth, from the development of the technique to important milestones and challenges in the field.

The proposed lateral growth mechanism and the development of the LLPE growth technique is provided in Chapter 5. A brief overview of the important characterization techniques used to characterise the epilayers grown by LLPE is presented in Chapter 6. The key findings of this work are presented in Chapters 7 & 8, which provide the results of LLPE growth for asymmetric strain and threading dislocation reduction, respectively. The conclusions from this work are provide in Chapter 9, along with suggestions for future work.

Chapter 2

Misfit Strain Relaxation in SiGe

This chapter provides an overview of the strain relaxation mechanisms in the SiGe binary system. First, the primary slip systems at play are introduced followed by a discussion of the mechanisms and sources for misfit dislocation nucleation. Lastly, threading dislocation minimization strategies are discussed.

2.1.Slip Systems in SiGe

The large lattice-misfit between Ge and Si (4%) is the overriding factor in the epitaxial growth of SiGe on Si. Lattice misfit is defined as the elastic strain introduced to the lattice of a crystal which is grown epitaxially onto a crystal with a different lattice constant (Figure 2-1a). The total misfit, *f*, is [15]:

$$f = \frac{(a_s - a_0)}{a_0} = \epsilon + \delta$$

Equation 2-1

Where a_0 is the lattice constant of the epilayer and a_s is the lattice constant of the substrate. ϵ and δ are the elastic and plastic strain in the epilayer, respectively. This assumes that the epilayer is thin compared to the substrate, such that all the strain is accommodated within the epilayer.

When an epilayer with a lattice-constant larger than the substrate, such as SiGe on Si, is grown, the lattice misfit is originally compensated entirely by compressive elastic strain (Figure 2-1b).

The strain is anisotropic, this results in a larger lattice-constant perpendicular (out-of-plane) to the growth interface ($a_{\perp}$) then the lattice constant parallel (in-plane) to the interface ($a_{//}$). As the thickness of the epilayer increases, the strain energy in the pseudomorphic crystal increases as well. Beyond the critical thickness, h_c, it becomes energetically favourable to nucleate a misfit dislocation to relieve the strain (Figure 2-1c).

The energy of a dislocation is proportional to the square of the magnitude of the dislocation Burgers vector (b^2), thus the dislocations with the shortest Burgers vector have the lowest energy. As a result, dislocations in Ge and Si (001) epilayers, which have a diamond crystal structure, form an orthogonal dislocation network along the <110> directions which lie on {111} planes, which are the planes and directions of highest density [15, 16]. Thus, the primary slip system in SiGe crystals is the {111}<110> slip system, where {111} is the slip plane and <110> is the line direction of the dislocation.

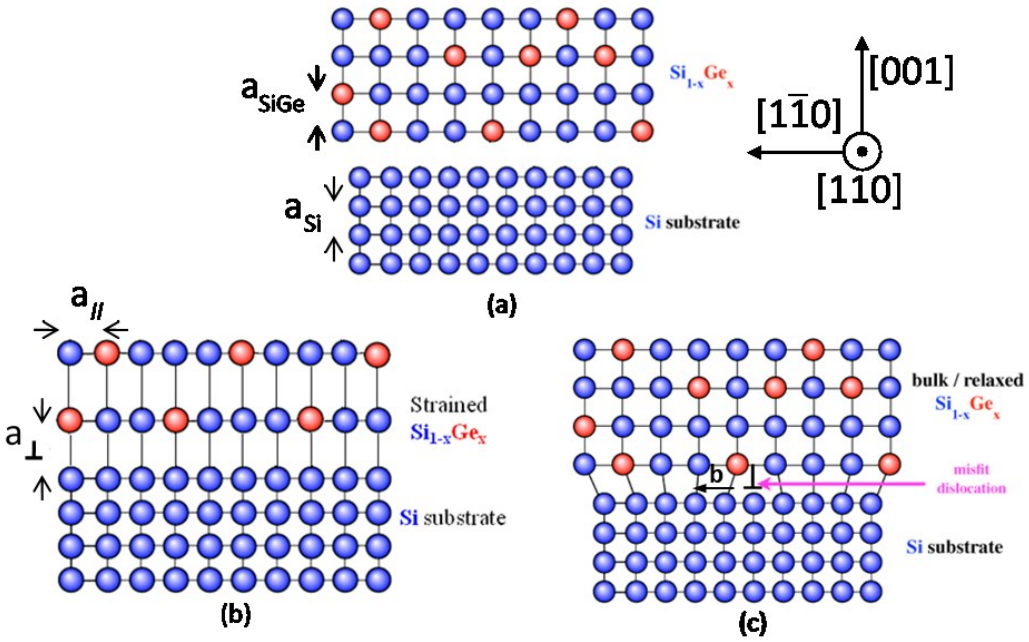


Figure 2-1. Schematic of lattice mismatch between SiGe and Si. a) A SiGe thin film is deposited on a Si substrate with a smaller lattice constant. b) The lattice misfit strains the SiGe epilayer asymmetrically. c) Beyond the critical thickness, misfit dislocations

Misfit dislocations only relieve the misfit strain in the direction perpendicular to the dislocation line, as shown in Figure 2-1. The Burgers vector (b) direction is $[1\bar{1}0]$, which is orthogonal to the [110] dislocation line, which represents an edge dislocation. Thus, 90° edge dislocations are the most efficient strain relieving dislocations since their Burgers vectors lie along the heteroepitaxial interface and the entirety of the Burgers vector, which lies in the <110> direction perpendicular to the dislocation line, contributes to strain relaxation. However, 90° dislocations exist in the {100}<110> slip system, which is not the primary slip system. The 90˚ dislocations are thus sessile, that is, they cannot glide, which results in short misfit dislocation lengths, the segment of a dislocation which exists at the heteroepitaxial interface and contributes to misfit strain relief (Figure 2-2), which increases the number of dislocations required to relieve the lattice strain. Short misfit dislocations are undesirable since a dislocation must terminate at a surface. The component of dislocation that terminates at the surface of the epilayer is termed a threading dislocation (Figure 2-2). A threading dislocation does not contribute to the misfit strain relief and acts as scattering and recombination site for electrons and hole, which is detrimental for future devices constructed atop the epilayer. It is preferable to have long misfit dislocations, which form through dislocation glide, at the heteroepitaxial interface to maximise the strain relief and reduce the number of threading dislocations.

Strain relaxation using the {111}<110> primary slip system is achieved with glissile 60° which glide on {111} planes (Figure 2-2). These dislocations have a <110> Burgers vector that is tilted 60° from the dislocation line [15]. Given that 60˚ have a mixed edge and screw components, and only the edge component of the Burgers vector contributes to strain relaxation, 60˚ are less efficient than 90˚ for strain relaxation per unit length of the dislocation. However, since 60˚ dislocations can glide on the primary slip system, they form long misfit dislocations which allows them to relieve more strain per threading dislocation. 60° dislocations are the dominant misfit dislocation in systems with low lattice misfit (<1%), whereas 90° dislocations are dominant in high misfit systems (>3%) [17].

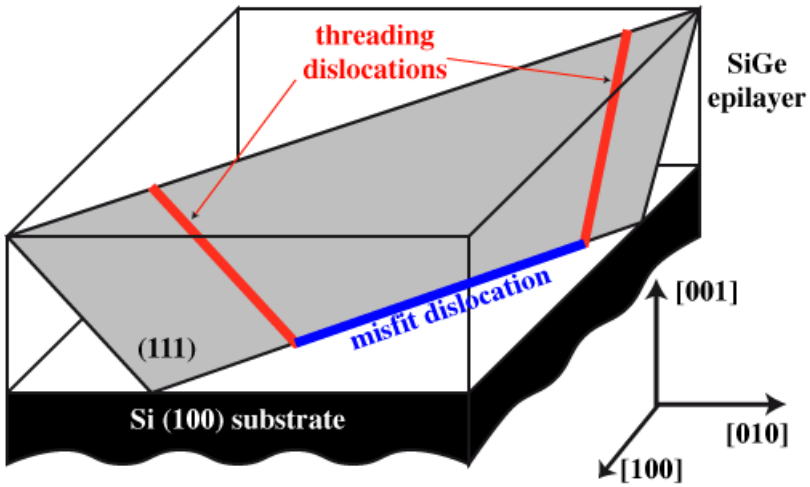


Figure 2-2. Schematic of 60° dislocations on Si (001) [18]. The misfit dislocation, which contributes to strain relaxation is shown in blue. The threading dislocation segments, which do not contribute to strain relaxation and are detrimental to device performance are shown in red.

2.2. Misfit Dislocation Sources

As discussed above, misfit dislocations are nucleated to relieve the misfit strain when the epilayer reaches a critical thickness (h_C) where it is energetically favourable to nucleate a misfit dislocation. The strain energy (E_ϵ) in a lattice mismatched epilayer is given in Equation 2-2 [15]:

$$E_\epsilon = \epsilon^2 Y h$$

Equation 2-2

where Y is Young's modulus under biaxial stress and h is the thickness of the film.

The energy per area of an isotropic array of misfit dislocations at the interface (E_d) is given by Equation 2-3:

$$E_d = D\left(\frac{b}{b_{eff}}\right)(1 - \nu\cos^2\alpha)(f - \epsilon)\left[ln\left(\frac{R}{b}\right) + 1\right]$$

Equation 2-3

where D is the average shear modulus of the interface, b_{eff} is the effective Burgers vector (the component of the vector which lies in the interface-plane), ν is the Poisson ratio, α is the angle between the angle between the dislocation line and the Burgers vector and R is the outer cut-off radius of the dislocation energy.

The total energy of the misfit layer is the sum of the strain and dislocation energies ($E_\epsilon + E_d$). The critical thickness can be determined by finding the minimum energy of the system by setting the derivative of the total energy to zero and solving for h (Equation 2-4).

$$h_C = \frac{D(1-\nu\cos^2\alpha)\left(\frac{b}{b_{eff}}\right)\left[ln\left(\frac{h_c}{b}\right)+1\right]}{2Yf}$$

Equation 2-4

This provides a first estimate of the critical thickness; however, this derivation does not provide any insight into the nucleation sources of the misfit dislocations. The lowest energy source for misfit dislocations are threading dislocations inherited from the substrate. Consider a pseudomorphic SiGe epilayer grown on a Si (001) substrate. If a threading dislocation is present at the surface of the substrate, the dislocation will thread through the film to the epilayer surface (A in Figure 2-2). Matthews proposed that the stress in the epilayer from the lattice misfit applies a force on the threading dislocation [15, 19-21]. The resolved lateral force, in the direction of dislocation glide, from the misfit on the threading dislocation is given in Equation 2-5:

$$F_e = 2G\frac{(1+\nu)}{(1-\nu)}\epsilon bh(\cos\lambda)$$

Equation 2-5

where G is the shear modulus, h is the height of the epilayer and λ is the angle between the Burgers vector and line in the film plane which is perpendicular to the intersection of the glide plane with the epilayer surface.

The lateral force on the dislocation is opposed by the line tension (F_l) (Equation 2-6) which, qualitatively, is proportional to the energy required to create a new length of misfit dislocations, and prevents the glide of the dislocation.

$$F_l = \left[Gb^2\frac{1-\nu\cos^2\alpha}{4\pi(1-\nu)}\right]\left[ln\left(\frac{h}{b}\right)+1\right]$$

Equation 2-6

As the epilayer thickness increases, F_e increases proportionally to h, and at a critical thickness F_e exceeds F_l, at which point the lateral force causes the dislocation to glide, which creates a misfit

dislocation segment at the heteroepitaxial interface (B in Figure 2-2). By balancing the Equation 2-5 and 2-3, the critical thickness for the nucleation of a misfit dislocation by the glide of a threading dislocation can be determined (Equation 2-7).

$$h_C = \frac{b(1 - \nu \cos^2 \alpha)\left[ln\left(\frac{h_c}{b}\right) + 1\right]}{8\pi\epsilon(1+\nu)\cos\lambda}$$

Equation 2-7

Thus, once the epilayer exceeds h_C, the misfit strain in the epilayer is relieved by the glide of threading dislocations inherited from the substrate. However, the threading dislocation density in commercial Si wafers is very small (less than 10^3 cm^{-2} [22]) and will not contribute significantly to the strain relaxation. The nucleation of additional dislocations is required to fully relax a strained epilayer.

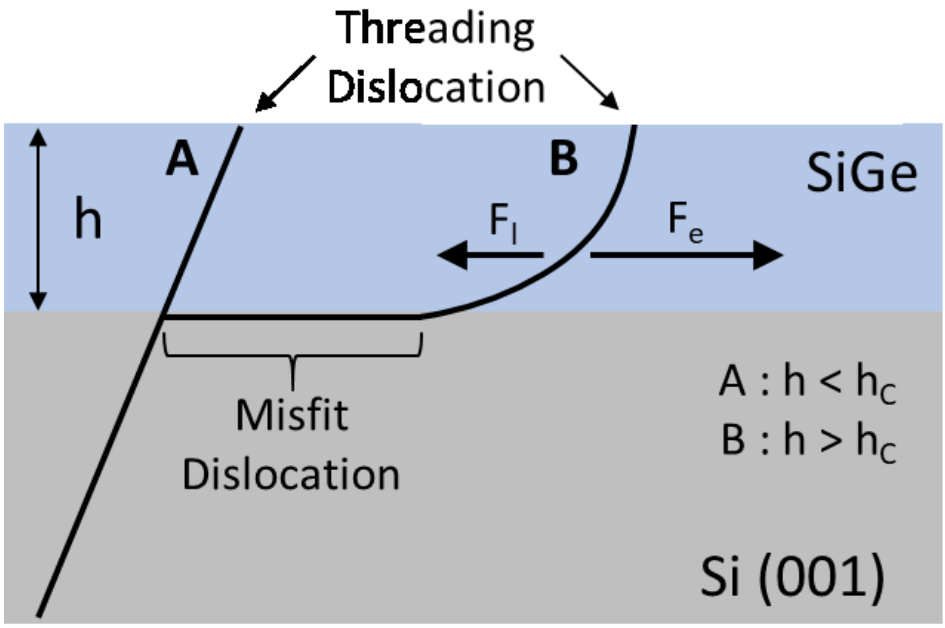


Figure 2-2. Schematic of the nucleation of a misfit dislocation from the glide of a threading dislocation.

The simplest nucleation mechanism to model for new dislocations is the surface half-loop nucleation mechanism, which was first modeled by Matthews [20]. The mechanism considers a dislocation half-loop which nucleates at the epilayer surface and glides to the heteroepitaxial interface on the glide plane (Figure 2-3a). There are three energy considerations for dislocation nucleation, the energy required to create a dislocation half-loop (E_l)(Equation 2-8) is, the strain

energy relieved by the half-loop (E_s)(Equation 2-9) and the surface energy released by the removal of surface steps (E_S)(Equation 2-10) [23].

$$E_1 = \frac{Gb^2R}{8}\left[\frac{(2-\nu)}{(1-\nu)}\right] ln\left(\frac{8\eta R}{e^2 b}\right)$$

Equation 2-8

$$E_\epsilon = \pi R^2 \left[Gb\frac{(1+\nu)}{(1-\nu)}\right] \epsilon\, cos\lambda\, cos\varphi$$

Equation 2-9

$$E_s = \frac{Gb^2}{4}\sin\alpha$$

Equation 2-10

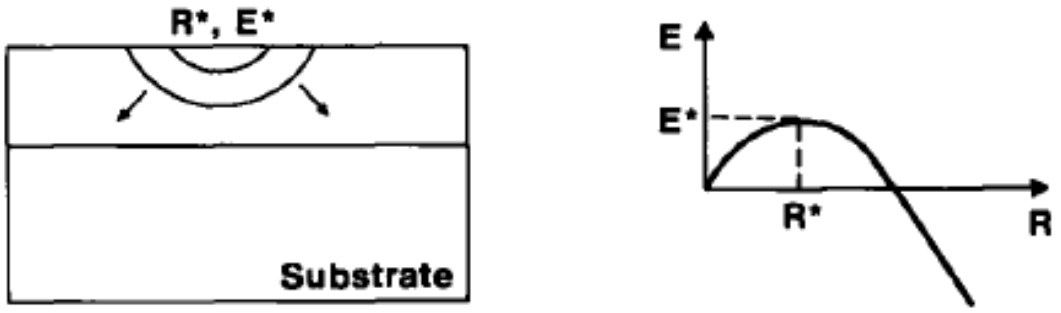
Where R is the radius of the dislocation, ν is the Poisson ratio, η is the core parameter (η=4 is true for most diamond structures [15]) and cosλcosφ is the Schmid factor which resolves the stress of the over layer onto the slip plane.

The energy difference (ΔE) for the nucleation of a dislocation half-loop is the difference between the energy required to nucleate the dislocation (E_1) and the sum of the strain (E_ϵ) and surface (E_s) energy released by the dislocation (Equation 2-11).

$$\Delta E = E_1 - (E_\epsilon + E_s)$$

Equation 2-11

If ΔE is plotted as a function of the half-loop radius (Figure 2-3b), it is observed that the nucleation of a dislocation increases the energy of the system. As the dislocation grows, so does the energy of the system, until a maximum energy (E*) is achieved, at which point the dislocation spontaneously grows since it reduces the energy of the system. E* is the activation energy for the nucleation of a dislocation by the half-loop mechanism [23].



a) b)

Figure 2-3. Schematic of homogeneous dislocation half-loop nucleation. a) Nucleation of a dislocation requires the spontaneous formation of a dislocation of radius R* to overcome the energetic barrier E* (b) [15].

However, the predicted strain energy to homogeneously nucleate a misfit dislocation is much higher then what is experimentally observed [15]. Heterogeneous half-loop nucleation from particulates, impurities or surface roughness can lower the activation energy for dislocation nucleation [22] and is more likely to occur then homogeneous nucleation.

The half-loop nucleation theory requires that the dislocation be nucleated at the epilayer surface and glide to the heteroepitaxial interface. Since 90° dislocations cannot glide on the {111}<110> primary slip system, they cannot be nucleated in this manner. Instead, the 90° dislocation nucleation occurs during three-dimensional (3D) Stranski-Krastanov (SK) growth. Due to the large lattice misfit, Ge will grow in the SK mode on Si (001) [24, 25], which will be discussed in Chapter 4.6.

The misfit strain is the driving force for both dislocation glide and nucleation. The kinetics of these two processes are thermally activated and can be described by an Arrhenius equation [26, 27]. The velocity of nucleation glide (v) is governed by the excess stress in the epilayer (σ_{ex}) and the activation energy for dislocation glide (E_v), as shown in Equation 2-12,

$$v = v_0 \left(\frac{\sigma_{ex}}{\sigma_r}\right)^n e^{\frac{-E_v}{KT}}$$

Equation 2-12

where v_0 is the velocity prefactor, σ_r is a reference stress, n is the exponent that describes the contribution of the excess stress, k is the Boltzmann constant and T is the epilayer temperature.

The nucleation rate (N'_1) is governed by the excess stress in the epilayer and the thermal nucleation activation energy (E'), as shown in Equation 2-13,

$$N'_1 = N' \left(\frac{\sigma_{ex}}{\sigma_r}\right)^m e^{\frac{-E'}{KT}}$$

Equation 2-13

where N' is the nucleation prefactor and m is the exponent that describes the contribution of the excess stress.

From the energetics and kinetics, we see that the strain relaxation processes depend on two factors: the misfit strain in the epilayer, which increases with film thickness and the misfit, and the activation energy of the processes, which is representative of the strain relaxation mechanism. Dislocation glide is the lowest energy mechanism, thus will have the lowest activation energy. This energy can be predicted by models. The activation energy for homogeneous surface half-loop nucleation can also be predicted by models, however, the energy is too high to be activated. Heterogeneous half-loop nucleation is a more likely candidate for dislocation nucleation, however the activation energy cannot be predicted, though it is expected to be greater than the activation energy for dislocation glide.

2.3. Crosshatch Morphology

Strain relaxation in low misfit systems ($f < 2\%$) on Si (001) substrates occurs by the nucleation and glide of 60° dislocations, as discussed in the previous section. These low misfit films and are known to have surface undulations or crosshatch morphology [28-30]. The crosshatch morphology is extensively reported for SiGe films grown by VPE [31-34].

There are two proposed models for the formation of the crosshatch morphology. The first proposes that the crosshatch morphology arises from surface diffusion due to the inhomogeneous strain fields created by the misfit dislocation network [35]. Albrecht *et al.* reported the crosshatch morphology of SiGe epilayers on Si substrates deposited by LPE and demonstrated that the crosshatch morphology is a result of both plastic (dislocation nucleation) and elastic (surface undulations) relaxation mechanisms [8, 36]. They deposited $Si_{0.97}Ge_{0.03}$ films of varying thicknesses on a Si (001) substrate from an In solution and proposed that the crosshatch morphology is developed in 4 steps:

1) Pseudomorphic planar growth begins. As the dislocation-free layer grows, the misfit strain induces surface undulations in the <100> directions. The shear stress is increased in the troughs and is greatest at the edges of the substrate.
2) Misfit dislocations are nucleated at the edge of the substrate to partially relieve the misfit strain. The dislocations are glissile 60° dislocations in the primary slip system.
3) The deposition rate is increased in the relaxed areas lying above the misfit dislocations [37]. This creates ridges in the <110> directions.
4) Remaining misfit strain is relieved by preferential misfit dislocation deposition and nucleation in the troughs. This increases the growth rate in the troughs and promotes a flat epitaxial layer.

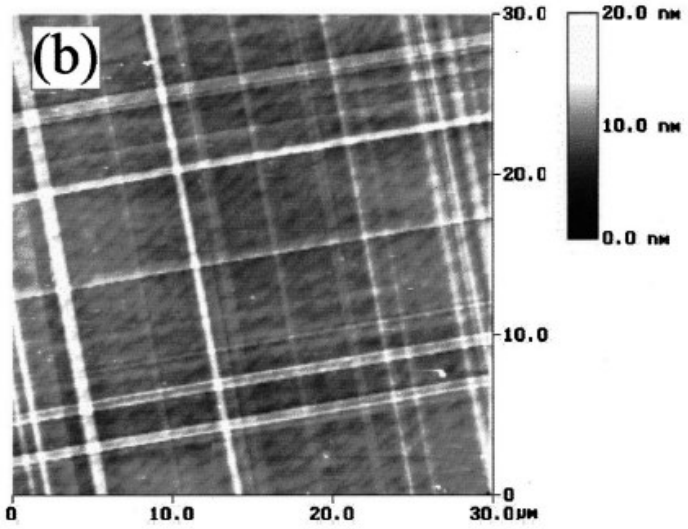


Figure 2-4. Atomic force microscopy (AFM) image of a $Si_{0.75}Ge_{0.25}$ layer on Si (100) substrate grown by MBE, showing the crosshatch morphology [32].

The second phase of dislocation nucleation in the troughs is driven by the high shear stress in these regions. The shear stress will push the dislocations into the substrate and act as a Frank-Read dislocation multiplication source [38].

Lutz *et al.* proposed an alternative mechanism, where the crosshatch morphology arises from surface steps created where the dislocation glide plane intersects the epilayer surface [39]. AFM imaging of the surface of thin $Si_{0.85}Ge_{0.15}$ films on Si (001) revealed surface steps whose height corresponded to the expected surface displacement of a 60˚ dislocation. These original misfit

dislocations are multiplied by Frank-Reed multiplication which creates dislocation pile ups and increases the surface undulations. However, it is likely that this mechanism is only valid for the early stages of the crosshatch evolution and that the strain field proposal is the most likely explanation for the crosshatch morphology [40].

2.4. Threading Dislocation Reduction

As discussed in Chapter 2.1, threading dislocations are detrimental to device performance, and must be minimised. The following chapter outlines strategies employed to reduce the threading dislocation density in SiGe epilayers.

2.4.1. Graded Buffers

Graded buffer layers are the primary technique to grow relaxed, lattice mismatched heteroepitaxial films with low threading dislocation densities [41-45]. High misfit layers (>1.5 %) are known to nucleate a large number of misfit and threading dislocations [15]. For example, pure Ge on Si growth results in a dislocation density of $10^9/cm^2$ [46]. Low misfit layers (<1.5 %) can have very low dislocation densities [47] due to the reduced strain energy, which is the primary driving force for misfit dislocation nucleation.

Since dislocation nucleation is reduced in low misfit systems, a low Ge content $Si_{1-x}Ge_x$ layer is grown on Si. The Ge content (x) is then slowly increased for subsequent layers, such that the misfit strain between each layer is small. The top layer should be a fully relaxed $Si_{1-x}Ge_x$ virtual substrate of the desired composition and with low dislocation density. Fitzgerald *et al.* demonstrated that for typical graded buffer growth temperatures (550°C), the initial $Si_{1-x}Ge_x$ layer is elastically relaxed [46]. The mismatch between the first and second layer will then be nearly the same as the mismatch between the substrate and the second layer, which increases the dislocation density.

Fitzgerald *et al.* proposed that there are two main criteria for the growth of strain-relaxed, low-defect density, graded $Si_{1-x}Ge_x$ buffers [46, 48]. First, the dislocation nucleation rate must be minimised and second, the dislocation glide must be maximised. If these criteria are met, the threading dislocations that are nucleated in the initial SiGe layer can glide in the second layer and fully relax the layer without the nucleation of additional misfit dislocations, as shown in Figure

2-5a. Since dislocation glide is thermally activated, and the dislocation rate increases with the lattice mismatch, high-quality $Si_{1-x}Ge_x$ graded buffer layers with low defect densities can be grown with Ge content up to 100 % [46], if the layers are grown at high temperature (>750°C) and the composition gradient is low (<10% Ge/μm). Figure 2-5b shows a TEM micrograph of a relaxed SiGe layer grown above a fully relaxed step graded buffer layer. The dislocation density does not increase throughout the graded buffer which indicates that the dislocations can glide in to the subsequent layers. In addition, the relaxed top layer is defect free.

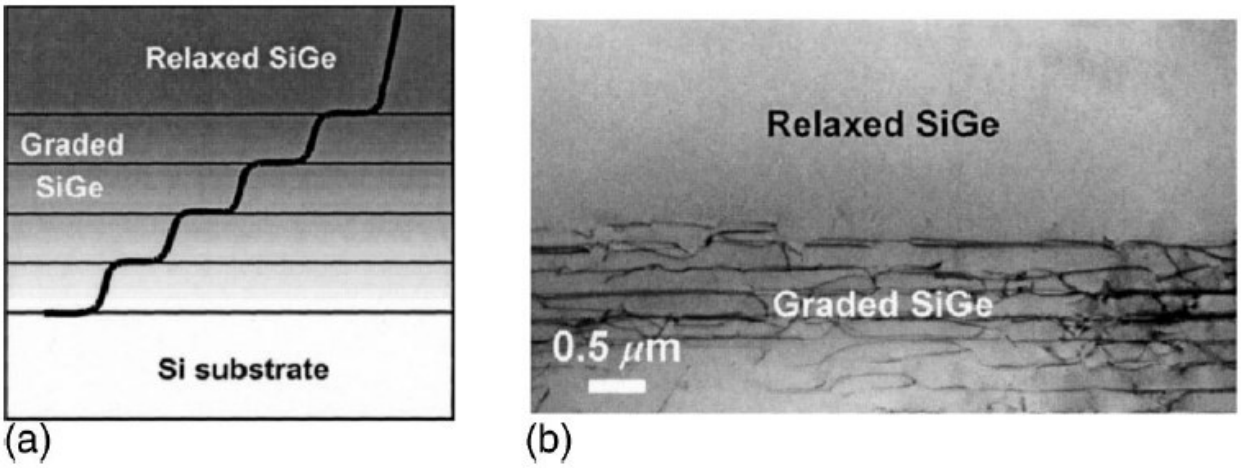


Figure 2-5. a) Schematic of a SiGe step-graded buffer. b) TEM micrograph of a relaxed SiGe top layer on a step graded SiGe buffer [48].

2.4.2. Dislocation Pile-Up

As discussed is the preceding section, low threading dislocation densities are achieved in graded buffers by extending the misfit dislocations by glide to prevent the nucleation of additional dislocations. Dislocation pile-ups act as kinetic barriers to dislocation glide since dislocations in a pile-up can no longer glide, thus new dislocations must be nucleated [11]. Paine *et al.* observed that the glide of a dislocation could be blocked by the strain field of an orthogonal misfit dislocation and Freund proposed that the driving force for dislocation glide was lost in the strain relaxed region lying above the perpendicular dislocation [49]. The stress field around a misfit dislocation decays as a function of 1/r, where r is the distance from the misfit dislocation. As a result, a threading dislocation must pass through a channel which lies above the strain field of an orthogonal misfit dislocation and below the epilayer surface [40], as shown in Figure 2-6.

However, trenches in the crosshatch morphology, which form above a cluster of misfit dislocations can locally reduce the film thickness and eliminate the channel through which the threading dislocation can pass, resulting in dislocation pile-up. If the dislocation cannot pass over the orthogonal misfit dislocation, the glide of the dislocation is exhausted, and additional dislocations must be nucleated to relax the misfit strain.

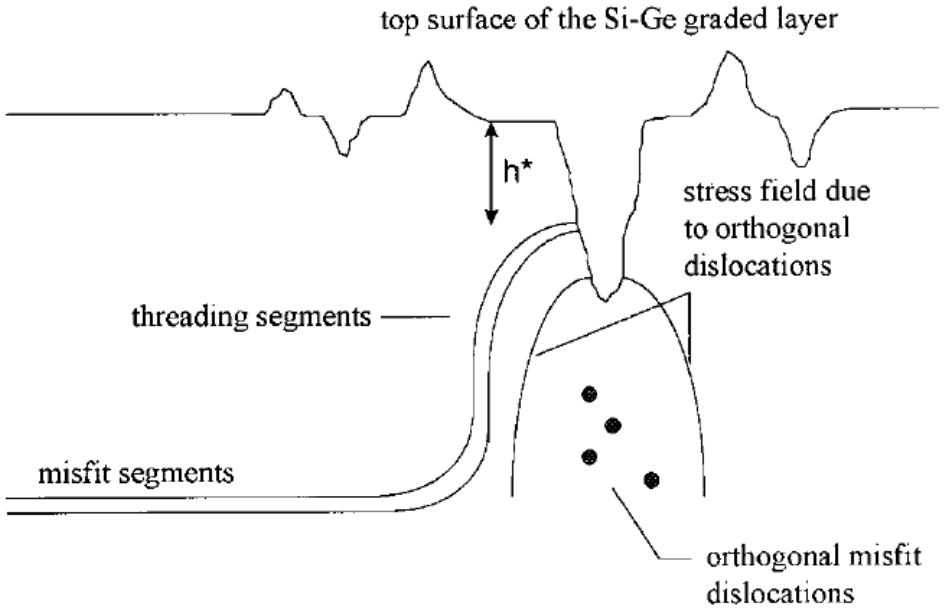


Figure 2-6. Schematic of the interaction between the glide of a dislocations and blocking dislocations and surface morphologies [40].

Thus, dislocation pile-ups can significantly increase the threading dislocation density in lattice mismatched films by creating short misfit dislocation lengths. In SiGe graded buffers grown at high temperature, dislocation pile-ups occur due to the surface roughness caused by the crosshatch pattern [40]. Currie *et al.* demonstrated that dislocation pile-ups can be removed in a continuously graded SiGe buffer layer by removing the crosshatch surface roughness by intermittent chemical mechanical polishing (CMP) [11]. The removal of the surface roughness reduces the formation of dislocation pile-ups. As a result, the threading dislocation density in a linearly graded buffer on Si (001) to 100 % Ge, was reduced by one order of magnitude (10^7 cm^{-2} to 10^6 cm^{-2}) by the addition of the single CMP step at $Si_{0.5}Ge_{0.5}$.

2.4.3. Epitaxial Layer Overgrowth

The growth of defect-free semiconductor crystals on oxide films (SOI) has many technological applications, such as the realisation of three dimensional integrated circuits [50, 51]. Epitaxial layer overgrowth (ELO) is a technique used to produce defect free Si thin films on SiO_2. ELO growth occurs on a Si substrate that has been masked with an insulating SiO_2 film, as shown in Figure 2-7. Seeding windows are selectively etched through the insulating layers. The epitaxial layer is nucleated in the seeding window and grows to fill the window. Vertical growth continues until the thickness of the epilayer exceeds the thickness of the masking oxide layer, at which point the epilayer grows laterally over the insulating layer. ELO by VPE was developed in the 1960's [52], however Si on insulator ELO suffered from low lateral to vertical growth ratios of up to 2:1. Bergmann *et al.* [12] applied the ELO technique to grow defect free Si single crystal films on SiO_2 with aspect ratios of 40:1 on Si (111) substrates. They demonstrated that ELO growth produces hexagonal crystals, bounded by {111} facets in the <110> directions. ELO growth on Si (001) substrates resulted in pyramidal growth and low aspect ratios [53]. The electron mobility of MOS transistors fabricated on Si SOI layers by LPE ELO were superior to the mobility of similar devices fabricated on Si SOI layers by VPE [54]. The increase in mobility is attributed to the superior crystal quality of the defect free LPE ELO layers.

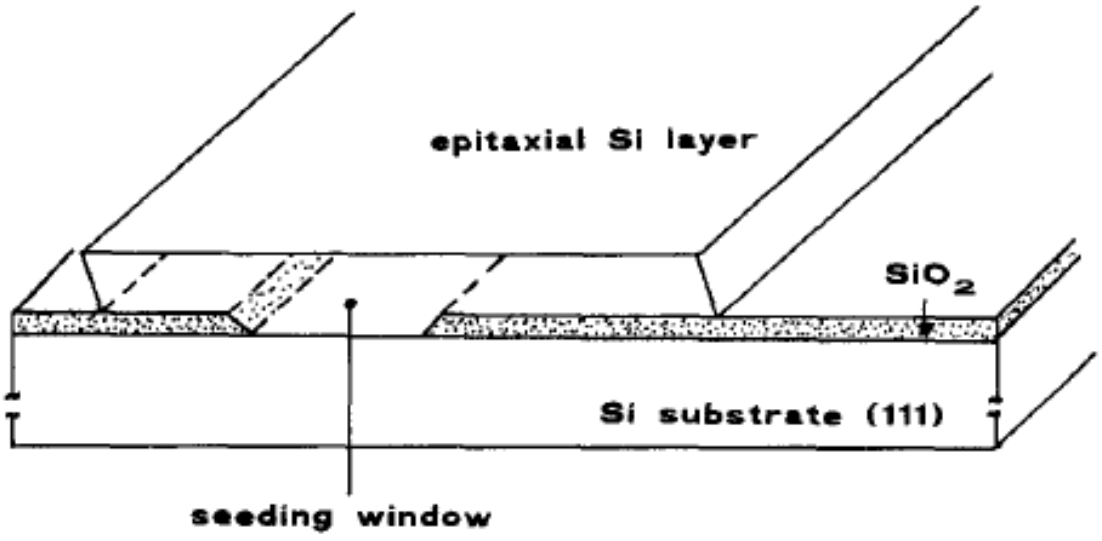


Figure 2-7. Schematic of epitaxial layer overgrowth on Si (111) [50].

Banhart *et al.* observed defective ELO growth which resulted in a high density of dislocations in the SOI layer [50]. They determined that residual stresses resulting from the thermal expansion mismatch between Si and SiO_2 induced strain into the Si epilayer. 60° dislocations were nucleated to relieve the strain, similar to the nucleation in low lattice mismatched LPE growth.

Homoepitaxial layer overgrowth (ELO) provides high quality single crystal Si on SiO_2 for transistor applications. Heteroepitaxial layer overgrowth (HELO) provides the further benefit of relaxed and defect free SiGe films. Hansson *et al.* applied HELO to high Ge content SiGe on Si (111) [13, 14]. The lattice mismatch is accommodated in the seeding area by the nucleation of misfit dislocations for film thicknesses greater than h_c. As discussed above, the strain relaxation mechanism results in a rough surface morphology. A $Si_{0.2}Ge_{0.8}$ HELO layer on Si (111) is shown in Figure 2-8. The center of the layer lies above the seeding window and shows a rough surface morphology. The overgrown areas (i.e. above the SiO_2 film) are smooth. Characterisation by cathodoluminescence and TEM indicated that the overgrown films with 90 at. % Ge were dislocation free, though stacking faults were observed [14]. The aspect ratio of SiGe ELO (11:1 [13]) was significantly lower than Si ELO. This is likely due to the formation of steps and facets from misfit dislocation nucleation, as was seen in defective Si ELO [50].

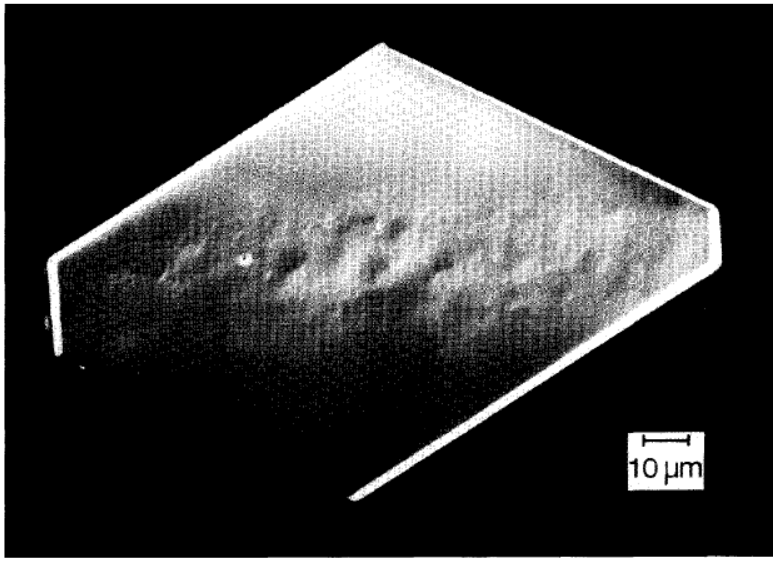
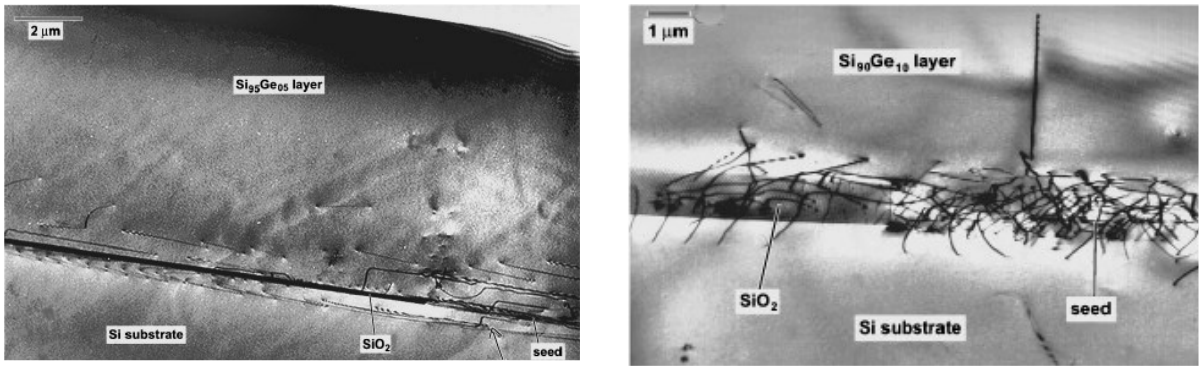


Figure 2-8. Nomarski differential interference contrast (NDIC) micrograph of $Si_{0.2}Ge_{0.8}$ ELO layer on Si(111) [13]

Banhart and Gutjahr [55] demonstrated that there are two dislocation nucleation mechanisms in HELO growth which depend on the critical thickness of the epilayer exceeding the thickness of the masking layer. In the first case, the critical thickness of the epilayer is greater than the thickness of the masking layer. Later growth over the oxide layer occurs without plastic strain relaxation. However, the stresses at the edges of the oxide mask promote heterogeneous nucleation of dislocations which are pinned at the oxide interface and form Frank-Read multiplication, which are an important relaxation mechanism in low lattice misfit systems [56]. The TEM micrograph in Figure 2-9 shows the dislocations extending along the (111) planes parallel to the heteroepitaxial interface in both the substrate and epilayer. However, no threading dislocations are observed in the epilayer above the oxide.



a) b)

Figure 2-9. TEM cross-section micrographs of HELO SiGe on Si (111) [55]. a) $Si_{0.95}Ge_{0.5}$ epilayer which does not present misfit dislocations, and b) $Si_{0.9}Ge_{0.1}$ epilayer which presents a high density of misfit dislocations at the heteroepitaxial interface within the seeding window.

The second dislocation nucleation mechanism occurs when the critical thickness of the epilayer is less than the thickness of the oxide mask. Misfit dislocations will nucleate in the epilayer before lateral growth across the oxide film. The misfit dislocations form hexagonal networks, as observed previously in the low misfit systems [25]. The oxide mask acts as a barrier to dislocation glide into the SiGe layer above the oxide, which results in a lower dislocation density in the layer above the oxide, as seen in Figure 2-9b. No threading dislocations were found in the ELO layers for all compositions studied (up to 14 at.% Ge)

Miyao *et al*. [57-59] presented a modified ELO growth which produced long, single crystal strips of Ge on Si. They deposited 100 nm thick strips of amorphous Ge by MBE on a thermally oxidized Si wafer on which seeding windows were opened by wet etching (Figure 2-10). Rapid thermal annealing (1000°C for 1s) was applied to quickly melt and solidify the amorphous Ge. It was found that the Ge strips crystallised at the seeding window and the single crystal was propagated across the entire length of the original amorphous strip. Though this growth system is closer to melt growth then traditional LPE, it is important that they successfully grew lateral, single crystal, strips with lengths of 400 μm with different seed crystal orientations: (001), (110) and (111) [59].

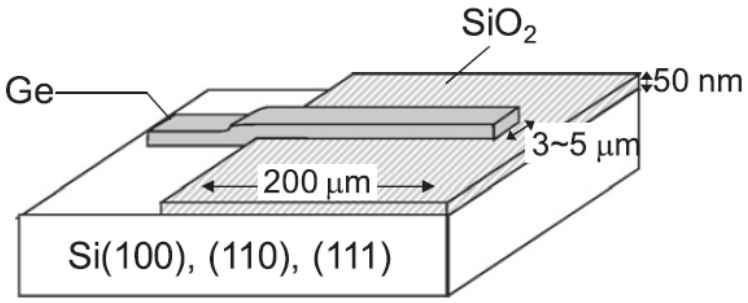


Figure 2-10. Schematic of the lateral-overgrowth experiments by Miyao *et al*. [59]. The amorphous Ge strip was deposited by MBE onto a Si substrate with a SiO_2 mask.

2.4.4. Lateral Nanowire Growth

The lateral growth of lattice mismatched layers is a potential solution to grow high quality semiconductor films with low threading dislocation densities. The lateral growth of SiGe epilayers on oxide layers has been demonstrated using ELO, as discussed in Chapter 2.4.3. However, these techniques are not suitable for the lateral growth of a SiGe epilayer on a lattice mismatched Si substrate. The growth of high quality Ge nanowires on amorphous [60]and lattice mismatched Si substrates [61] has been reported previously using a guided vapour-liquid-solid growth (VLS) technique. The fabrication of the guided nanowires is illustrated in Figure 2-11. First a Si (001) substrate with a buried oxide layer (BOX) is capped with a Si_3N_4 layer, and stripes were etched down to the BOX layer (Figure 2-11a). The oxide layer was then etched such that the top Si layer was undercut and a gold catalyst was placed under the Si overhang (Figure 2-11b). Si or Ge nanowire growth was activated by VLS. The nanowire initially grew in its preferred [111] direction until it reached the oxide layer, which then guided the nanowire to grow laterally in the [110]

direction (Figure 2-11c). The lateral growth was terminated when the nanowire reached the end of the etched stripe (Figure 2-11c).

The growth of a lattice mismatched Ge nanowire on Si showed that the misfit dislocations were confined to the heteroepitaxial interface and did not thread to the surface of the nanowire [61]. Misfit dislocations could nucleate at the edge of the Ge nanowire, give the that the diameter of the nanowires was less than 200 nm, which eliminates the need to thread to the top surface of the Ge.

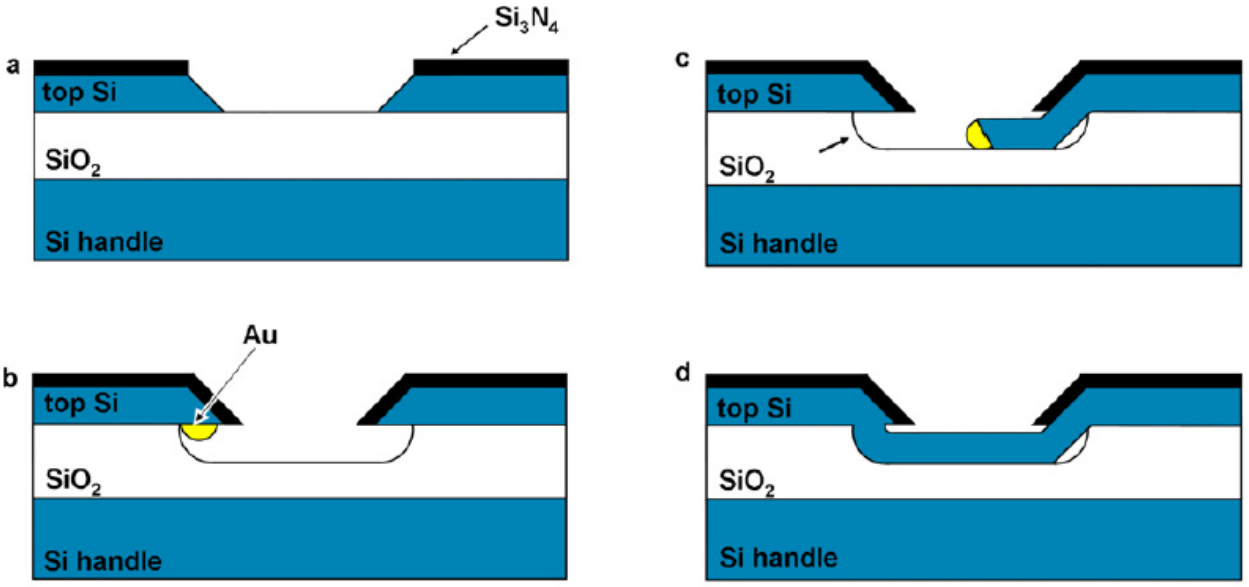


Figure 2-11. Schematic of the fabrication process for guided NW growth on an oxide layer [60].

Lateral growth has the potential to deposit thin, high-quality, lattice mismatched films over a large area by confining the misfit dislocations to the heteroepitaxial interface. In Chapter 5.1, a novel lateral growth technique by liquid-phase epitaxy (LPE) which produces large-area epilayers with long misfit dislocations and low threading dislocation densities. The results of the reduction of the threading dislocation density is presented in Chapter 8.

Chapter 3

Uniaxial Strain

For the past few decades, the continual miniaturisation of metal-oxide-semiconductor field effect transistors (MOSFET) has driven the continual improvement of the performance of integrated circuits (IC). The roadmap for MOSFET miniaturisation was envisioned in Moore's law, which observed that the number of transistors on a chip doubled every two years [1, 2]. The doubling of the number of transistors led to MOSFET device improvements since smaller devices had smaller gates and the devices were limited to how fast the electrons traveled under the gate. However, as the transistor gate length reduced to sub-micron lengths, significant hurdles to increasing device performance were presented, such as short-channel effects, velocity saturation, high leakage current and dielectric breakdown [3]. Increasing the mobility of carriers in strained MOSFET channels has been identified as an important technique to continue device performance improvements.

The following chapter explores the field of uniaxial strain in Si and SiGe. First the origin and the benefits of compressive strain are described. In the following sections, multiple techniques will be discussed to fabricate strained $Si_{1-x}Ge_x$ layers for MOSFET applications. In the first section, we will discuss techniques for biaxial strained layers. These include traditional graded buffers and techniques to fabricate SiGe on-insulator substrates for increased MOSFET performance. In the second section, novel techniques are proposed for the fabrication of uniaxial strained SiGe layers.

3.1.Strained Si

Strained channels were first adopted by Intel for the 90 nm node technology in 2004 after they observed greater than expected performance enhancement when they embedded SiGe as the source and drain material in the early 2000's. The increase in performance was attributed to the stresses induced in the channel by the implanted SiGe [62] and prompted significant interest in the effect of strain on MOSFET performance.

Enhanced mobility in biaxial tensile-strained Si on SiGe was reported as early as 1982 by Manasevit *et al.* [63]. The enhanced strain mobility was explained by Abstreiter *et al.* in 1985 [64]. They postulated that the increased strain mobility was caused by the strain-induced offset of the type-II band, which repopulates electrons into the lower effective mass band (discussed below). Despite the promise of higher carrier mobility, strained Si applications were limited due to the high defect densities (10^8-10^{10}/cm^2) of the strain relaxed SiGe graded buffers layers on which they were fabricated [48]. The development of fully strain relaxed SiGe buffers in the early 1990's reduced the defect density in SiGe layers to 10^6/cm^2 [48]. Within a year, the superior quality of the SiGe buffer layer allowed the electron mobility in strained Si to be increased from 19 000 to 170 000 cm^2/Vs [65]. In 1993, compressively strained Ge layers on a SiGe buffer demonstrated the highest hole mobility for group IV semiconductors [66]. The research community then had the tools to envision the next generation of MOSFETs utilising high mobility tensile strained Si n-channels and compressive strained Ge p-channels.

3.1.1. Carrier Mobility Enhancement

The mechanism for strain enhanced mobility in Si was first proposed by Abstreiter *et al.* in 1985 [64]. In bulk Si, the conduction band is composed of six degenerate valleys in the <100> direction, as shown in Figure 3-1. The effective mass is anisotropic for each ellipsoidal valley. The transverse mass (m_{trans}=0.19m_0) is smaller than the longitudinal mass (m_{long}=0.98m_0) [5]. Under unstrained conditions in bulk Si, the contributions of each degenerate valley are expressed as a single conductivity effective mass of electrons [67].

Under biaxial tensile strain, the degeneracy of the 6 valleys is broken. Tensile strain in the <110> direction will cause the energy of the Δ2 subband to shift down and the energy of the Δ4 subband to shift up. The band splitting causes the electrons to repopulate into the lower energy Δ2 subband, which is shown schematically in Figure 3-1, where the Δ2 subbands grow at the expense of the Δ4 subbands. Because the effective mass of Δ2 ($0.19m_0$) is less than the effective mass of Δ4 ($0.315m_0$), the average effective mass of the strained Si is reduced [3]. In addition to the reduction of the average effective mass, the band splitting reduces the intervalley phonon scattering [68, 69], which results in increased electron mobility.

It should be noted that the mobility enhancement in strained MOSFET channels is not identical to the enhancement observed in bulk Si. The six valley degeneracy is broken, even for unstrained Si, by the electric field confinement in the channel [3]. In addition, the mobility is limited by the surface scattering. It is expected that the strain enhancement of the electron mobility in a MOSFET channel is less than the effect on bulk, strained Si.

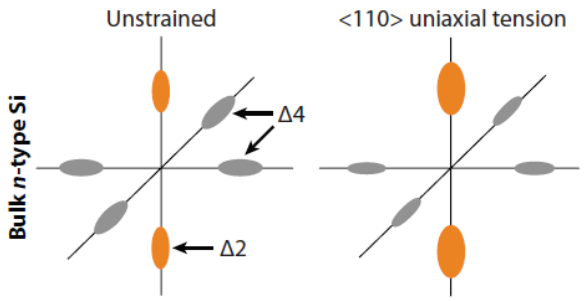


Figure 3-1. Simplified schematic of the band structure of Si. The six degenerate valleys in bulk Si are shown on top [3].

The hole mobility can also be increased by strain, though the mechanism differs significantly from the electron mobility. In unstrained Si, the heavy hole and light hole bands are degenerate at the Γ point. The majority of the holes (80%) occupy the heavy hole band ($0.59m_0$), the remainder occupy the light hole band ($0.15m_0$) [3]. Under compression along the <110> directions, the degeneracy is broken as the light hole band is warped and shifted upwards (Figure 3-2). Repopulation of the holes into the light hole band reduces the hole effective mass thereby increasing the hole mobility. At room temperature, and under low strain (<1GPa), uniaxial strain induces more band warping than biaxial strain [70]. Thus, uniaxial compressive strain is more effective than biaxial compressive strain to increase mobility in short channels.

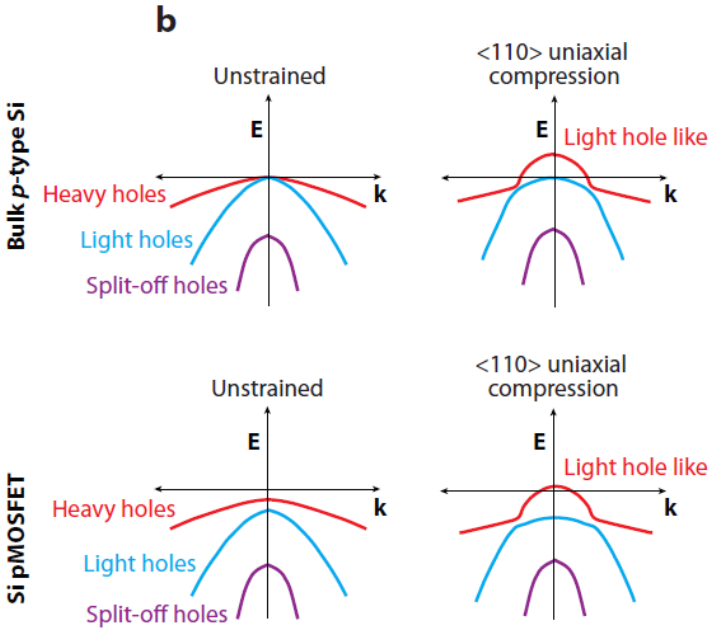


Figure 3-2. Schematic of the valence band structure of Si [3].

3.1.2. Current Technology

Strain enhanced mobility channels were adopted for the 90 nm node technology. A primary challenge for the fabrication of high mobility devices, is the integration of tensile strained nMOSFET and compressive strained pMOSFET on a single device. Processed induced uniaxial stress, as opposed to biaxial stress from lattice mismatched layers, was selected as the strain source for various reasons, including increased hole mobility at low strain [71], avoiding dislocations and defects from lattice mismatched layers, larger drive current in short-channel devices [72] and smaller threshold voltage shifts in nMOSFETs [73].

Process induced uniaxial strain requires two process flows to produce integrated tensile nMOSFETs and compressive pMOSFETs. Compressive strain is introduced into the channel by substituting SiGe as the source and drain material. Given the larger lattice constant of relaxed SiGe, the source and the drain exert a compressive strain on the channel. Uniaxial tensile strain in nMOSFET devices is introduced via a tensile nitride capping layer. The effect of a strained nitride

layer on MOSFET performance was first reported by It *et al.* [74] in 2000 and Shimizu *et al.* [75] in 2001.

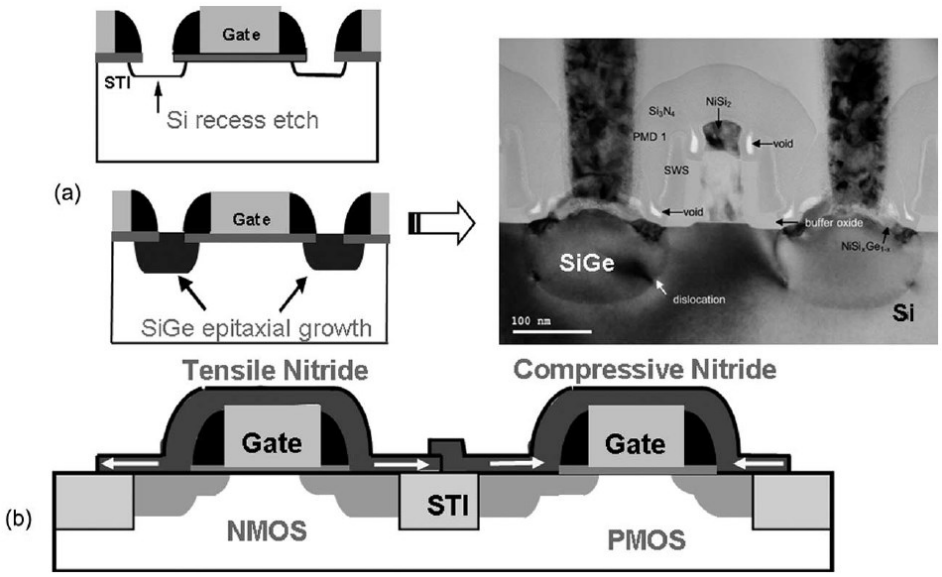


Figure 3-3. a) Process flow for strained pMOSFET. b) Dual stress liner with tensile and compressive nitride capping layers [72].

Thompson *et al.* introduced the process to fabricate compressive strained pMOSFET and tensile strained nMOSFET devices on a single wafer and is illustrated in Figure 3-3 [72]. By selective etching and deposition, SiGe is grown in the pMOSFET source and drain regions. (Figure 3-3a) Then, tensile silicon nitride is selectively deposited above the nMOSFET devices (Figure 3-3b). TEM crossections of complementary transistors are shown in Figure 3-4. The large SiGe source and drain, which exert the compressive strain are clearly visible in the pMOSFET, whereas the tensile nitride layer is visible in the nMOSFET as is the absence of the compressive SiGe source and drain. Uniaxial processes-induced strain provided the primary source of mobility improvement down to the 45 nm node. For example, uniaxial compressive stress increased the hole mobility by a factor of 2 at the 65 nm node technology [5].

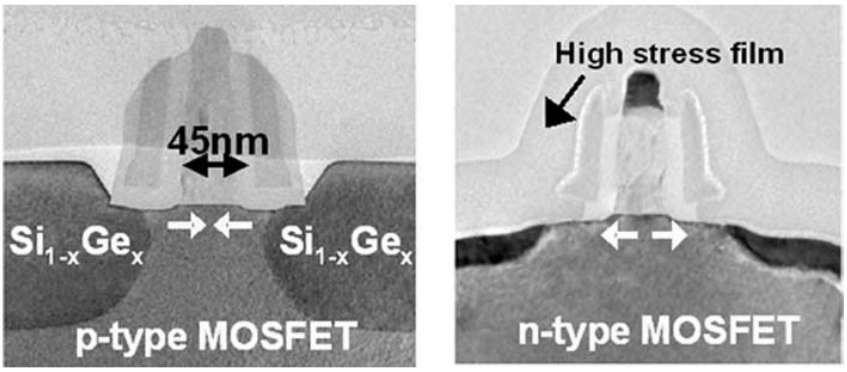


Figure 3-4. TEM micrographs of a 45 nm pMOSFET (left) with a compressed channel from the SiGe source and drain effect. nMOSFET (right) which is tensile strained by a SiN capping layer [76].

3.1.3. SiGe Channels

As IC technology progresses beyond the 14 nm node, introduced in 2014, towards sub 10 nm nodes, significant technological challenges must be addressed. As the current density continues to increase with each generation, the demand for lower resistance channel materials increases. Enhanced mobility in Si from process induced strain is expected to saturate and the replacement of strained Si with a higher mobility channel material is required to further improve device performance.

The International Technology Roadmap for Semiconductors (ITRS) highlights Ge as the preferred replacement for high mobility channels [6]. Ge has a lower electron effective mass than Si, as well as lower heavy hole and light hole effective mass (Table 3-1). As a result, Ge has higher carrier mobility than Si.

Ge and SiGe layers demonstrate similar mobility enhancements to bulk Si under biaxial strain. The mobility enhancement effect from uniaxial strain saturates at much higher levels of stress in Ge and SiGe layers when compared to Si, such as the Si hole effective mass which saturates at 2-3 GPa, as shown in Figure 3-5. Thus, Ge strained channels are expected to provide significant carrier mobility improvement and device performance.

	Si	Ge
Electrons		
m_{long}	0.98	1.59
m_{trans}	0.19	0.0815
$m_{effective}$	0.26	0.12
Holes		
m_{lh}	0.16	0.043
m_{hh}	0.49	0.33

Table 3-1. Effective mass, as a function of m_0, for Si [77] and Ge [78].

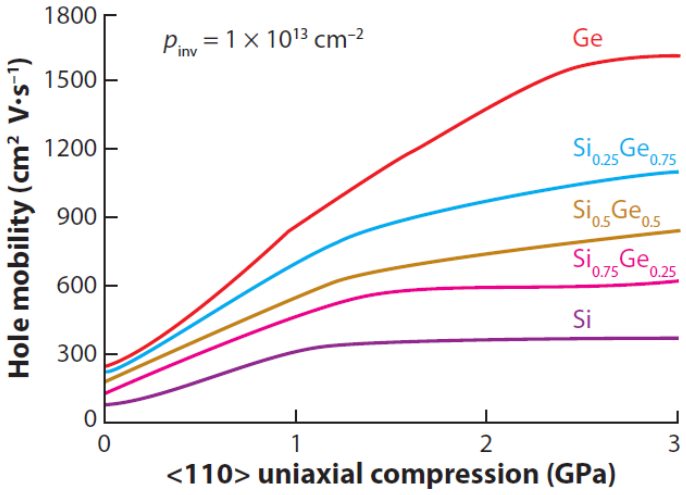


Figure 3-5. Hole mobility of $Si_{1-x}Ge_x$ vs uniaxial compression stress at different Ge contents [3].

3.2. Biaxial Strain Techniques

Lattice mismatched heteroepitaxial growth is the simplest technique to fabricate biaxial strained Si layers. If the thickness of the epilayer is less than the critical thickness for dislocation nucleation, the lattice constant of the epilayer will conform to the lattice constant of the substrate [15]. If the epilayer lattice constant is less than that of the substrate, the epilayer will have biaxial tensile strain, for example, tensile-strained Si on relaxed SiGe. If the epilayer lattice constant is greater than that of the substrate, the epilayer will have biaxial compressive strain, for example, compressively

strained SiGe on Si. In this way, the biaxial strain can be controlled by the difference in lattice constant of the epilayer and substrate. That is, the degree of biaxial strain in a strained Si epilayer can be controlled by the composition of the $Si_{1-x}Ge_x$ substrate.

Since it is difficult to grow high-quality and compositionally uniform, single-crystal, SiGe substrates, it is convenient to grow SiGe virtual substrates on Si substrates. However, given the lattice mismatch between Si and Ge, it is necessary to nucleate misfit dislocations to have a strain-relaxed SiGe epilayer on a Si substrate. Graded buffers are the primary solution to achieve strain-relaxed SiGe virtual substrates, as discussed in Chapter 2.4.1. Early attempts to fabricate strained-Si on SiGe buffers did not significantly increase the electron mobility in the stained-Si top layer since the buffer layers suffered from incomplete strain relaxation and high defect densities ($10^8/cm^2$). The fabrication of high-quality, low defect density, graded $Si_{1-x}Ge_x$ buffers has allowed the deposition of high mobility, strained-Si layers, as shown in Figure 3-6.

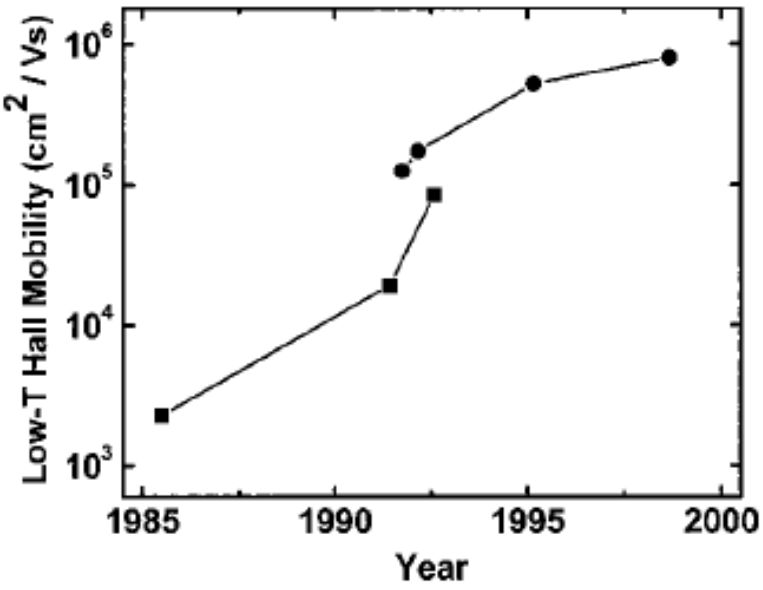


Figure 3-6. Evolution of record low-temperature (<4.2 K) electron mobility in strained-Si on SiGe heterostructures. Circles represent results from fully relaxed graded buffers and squares represent results from other buffer techniques [79]

3.2.1. Strained Si & SiGe on Oxide

Previous IC node technologies have been implemented on silicon on insulator (SOI) substrates. The buried oxide layer (BOX) eliminates most parasitic capacitance which reduces power consumption and is the substrate of choice for high speed, low power and low voltage applications [5]. Multiple techniques have been proposed for the fabrication of strained Si on insulator (SSOI) and strained SiGe on insulator (SGOI) substrates.

The separation-by-implantation of oxygen (SIMOX) process is a well-established technique to fabricate SOI substrates. The SIMOX process forms a BOX layer by ion implantation of oxygen which is subsequently annealed to form a buried oxide layer and to heal defects caused by the ion implantation [80, 81]. The natural extension of the SIMOX process is the fabrication of SGOI substrates.

Early attempts to fabricate SiGe BOX layers required the growth of a SiGe graded buffer atop an ultrathin SOI substrate [82, 83]. The primary concern with this process is the required thickness of the graded buffer which increases the depth of the BOX layer. The first successful fabrication of a BOX layer in a SiGe graded buffer directly by the SIMOX process was reported by Fukatsu *et al.* in 1998 [84]. Low energy (25 kV) O^+ ions were implanted in a strain relaxed $Si_{0.82}Ge_{0.18}$ virtual substrate on top of a SiGe buffer layer. The O^+ dose was kept low ($2x10^{17}/cm^2$) to reduce the number of defects formed in the top layer of the virtual substrate layer, which was initially dislocation free. Following ion implantation, the substrate was annealed in N_2 at 1280°C for 6 hours.

Figure 3-7b shows a TEM crossection of a 30 nm (BOX) layer below a 25 nm $Si_{0.82}Ge_{0.18}$ top layer. The authors investigated the structure of the BOX layer at various O^+ doses. The optimized condition is presented in Figure 3-7. If the dose was reduced to $1x10^{17}/cm^2$ (Figure 3-7a), precipitates of SiO_2 were formed, but a continuous BOX could not form due to insufficient oxygen atoms in the SiGe. If the dose was increased to $3x10^{17}/cm^2$ (Figure 3-7c), parasitic SiGe islands were formed [85]. Interestingly, no Ge was found in the BOX. The Ge atoms diffused to the SiO_2/SiGe interface, which was rougher than a typical SiO_2/Si interface in an SOI interface.

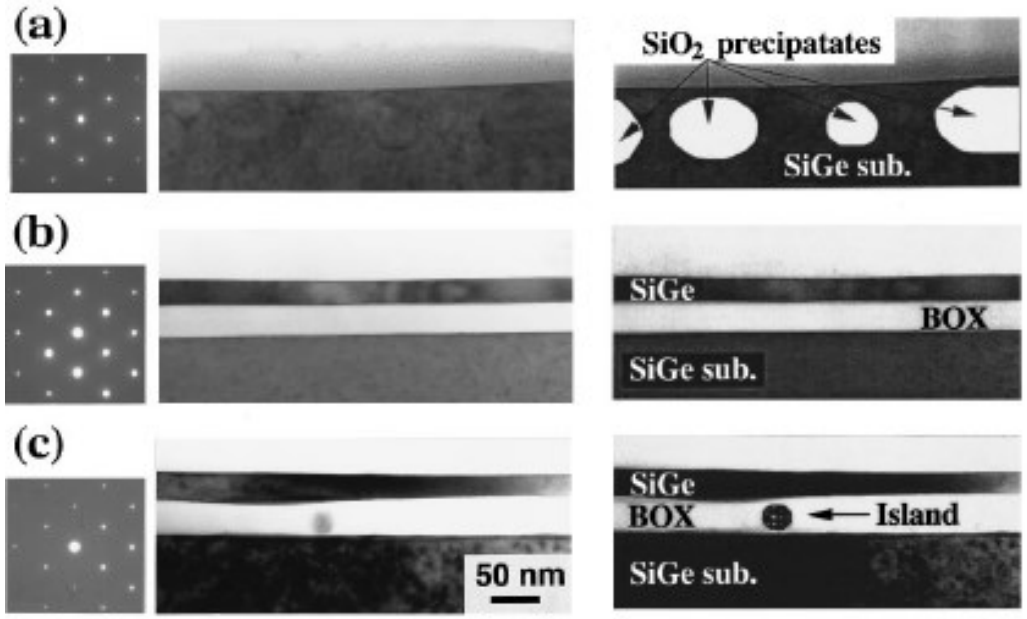


Figure 3-7. TEM crossection of a buried oxide layer in a SiGe virtual substrate by the SIMOX process at different O^+ doses [84]. a) $1x10^{17}/cm^2$, b) $2x10^{17}/cm^2$, c) 3x1017/cm^2.

A challenge for the implementation of nMOSFETs on SSOI fabricated by the SIMOX process is the thickness of the relaxed SiGe buffer and the strained, defect-free, Si layer. In addition, the presence of the SiGe buffer layer reduces the thermal budget of the process due to the Ge segregation at high temperatures, higher leakage current, enhanced dopant diffusion and a high level of dislocations and defects [5]. To alleviate these concerns, Langdo *et al.* proposed a process to remove the SiGe from SSOI substrates [86].

The process to fabricate SiGe-free SSOI substrates is illustrated in Figure 3-8. A 54 nm thick strained-Si layer is grown on a $Si_{0.68}Ge_{0.32}$ graded buffer. Hydrogen ions (H_2^+) are implanted through the strained Si layer, into the SiGe buffer layer. The implantation energy is adjusted to induce a cleave plane, approximately 350 nm below the strained Si. The strained Si is then bonded to the handle wafer with a 100 nm thick oxide layer. The substrate is annealed to remove the graded buffer (Figure 3-8b). The transferred SiGe layer is then removed by a combination of low temperature steam oxidation and HF etching. Since the $Si_{0.68}Ge_{0.32}$ steam oxidation rate is 120 times greater than the rate of Si oxidation [87], the SiGe layer is fully oxidized and selectively

stops at the strained Si interface. In this way, a high quality strained SSOI substrate is fabricated with controlled strained-Si and SiO_2 layer thickness. Raman spectroscopy and X-ray diffraction (XRD) confirmed that the tensile strain in the Si layer was preserved following the removal of the SiGe buffer layer.

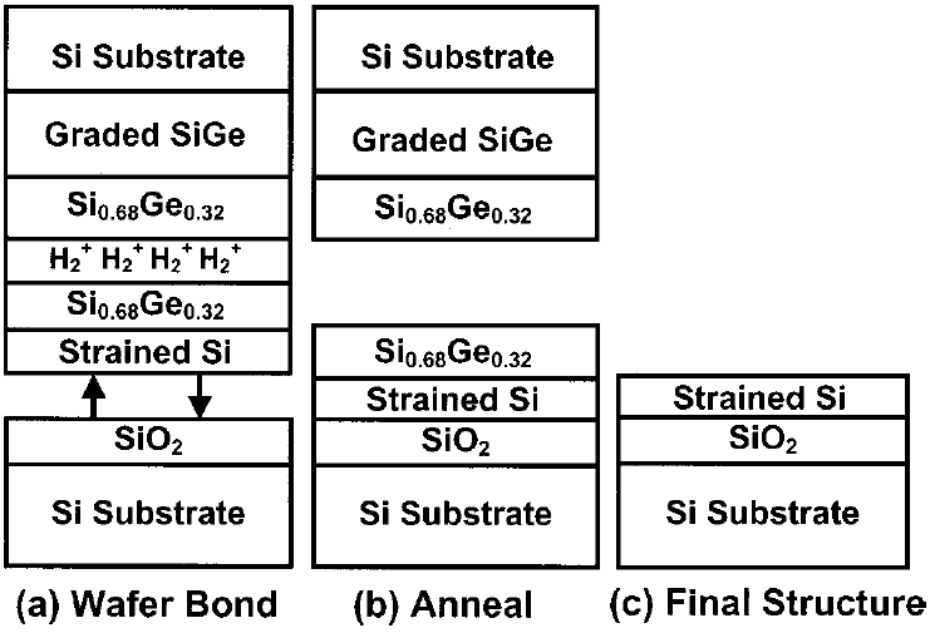


Figure 3-8. SiGe-free SSOI fabrication process [86].

The bond-and-etch back technique to fabricate SSOI can be extended to fabricate SGOI. Gomez *et al*. fabricated ultrathin strained-Si/strained-Ge/strained-Si layers on insulator by using the bond and etch-back process illustrated in Figure 3-9 [88]. A SiGe graded step buffer is first grown on a Si (100) substrate. A strained Si etch stop layer is then deposited, followed by a relaxed SiGe etch stop layer. Lastly, the strained-Si/strained-Ge/strained-Si multilayer is deposited. All layers were deposited by low pressure chemical vapour deposition (LPCVD). A SiO_2 bonding layer was then deposited and the multilayer structure was bonded to an oxidized handle wafer. Chemical mechanical polishing (CMP) removed the original Si substrate. A series of chemical etches removed the SiGe graded buffer and Si etch stop layers (Figure 3-9b). The final structure is composed of an 8.5 nm thick strained-Si top layer, a 4.2 nm strained-Ge layer and a 3 nm strained-Si layer on BOX.

The thermal budget must be carefully managed when fabricating ultrathin strained Si/Ge multilayer structures to avoid strain relaxation and the inter-diffusion of Si and Ge. The SiO_2 top layer is deposited at low temperature and densified for 2 hours at 600°. In addition, the post-bond anneal is kept low (T<550°). Raman and XRD analysis of the strained layers indicate that the strained-Ge layer contains 93 at.% Ge, indicating inter-diffusion between the layers during the bonding process. The strain relaxation in the Ge layer was calculated to be 12 %. This technique successfully fabricated thin, strained Si/Ge/Si heterostructures on BOX, though the thermal budget must be strictly regulated to avoid increased strain relaxation and inter-diffusion.

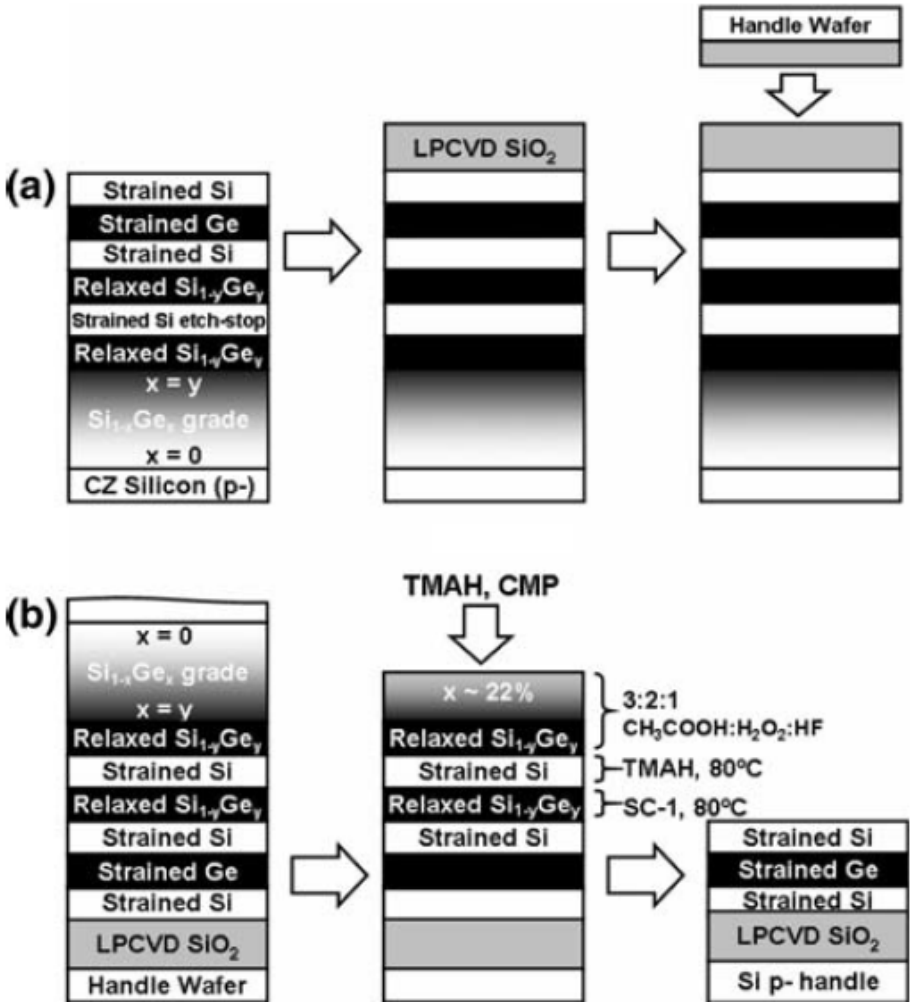


Figure 3-9. Schematic of the bond and etch-back process. a) Epitaxial growth, planarization and bonding, b) substrate grinding and etch back. A series of chemical etches are used to remove SiGe buffer and etch stop layers [88].

3.3. Uniaxial Strain Techniques

Uniaxial strain has been shown to provide greater carrier mobility enhancement when compared to biaxial strain, as discussed in Chapter 3.1.1. The following section introduces the current techniques which produce uniaxial strain in SiGe epilayers without the use of external tensors. Theses techniques include the selective strain relaxation by substrate patterning and ion implantation as well as the fabrication of strained nanowires.

3.3.1. Patterning Induced Lateral Strain Relaxation

In 2006, Irisawa *et al.* proposed a novel fabrication technique to induce uniaxial strain in a SiGe layer by lateral relaxation [89]. The fabrication process is outlined in Figure 3-10. A biaxial compressive SGOI substrate, with 20 at.% Ge, is patterned by anisotropic etching into rectangular strips. Elastic strain relaxation occurs at the free edges of the channels. No dislocations were observed in the SGOI layer, indicating that the relaxation was entirely elastic. If the channel width is narrow with respect to the channel length, the SiGe can fully relax along the narrow dimension, but not along the length of the channel.

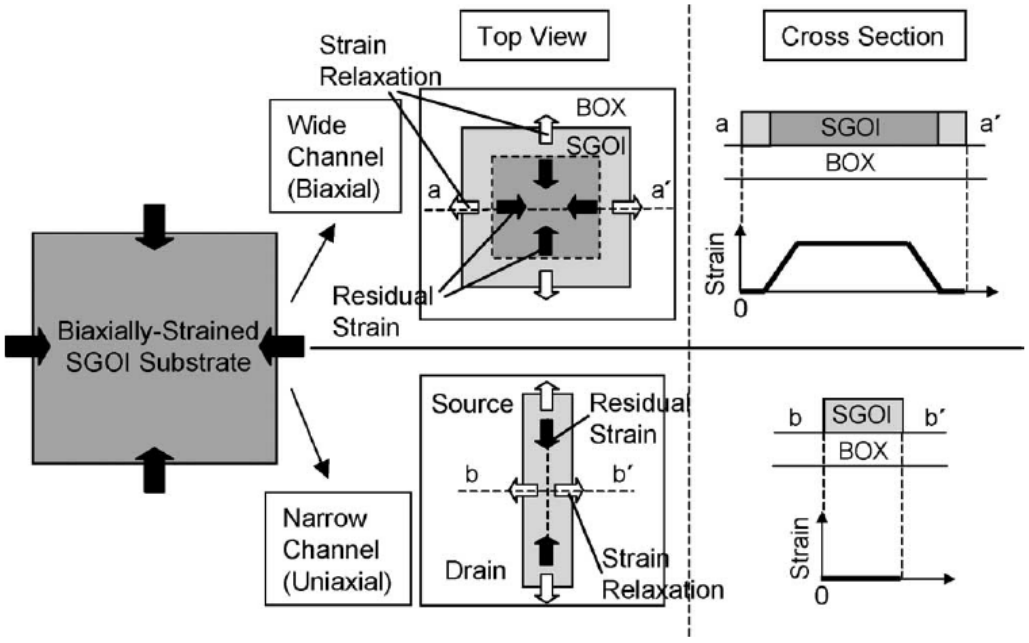


Figure 3-10. Schematic of the lateral relaxation process to create uniaxial strain in narrow channels patterned on biaxially strained SGOI. [89].

The strain in the channel was investigated by nanoelectron-beam diffraction (NBD) in each direction. Figure 3-11 summarizes the strain measurements of a channel with length of 10 μm (*x* direction), width of 0.3 μm (*y* direction) and thickness of 80 nm (*z* direction). The strain along the channel length was -0.9%, which is comparable to a fully strained $Si_{0.8}Ge_{0.2}$ layer on Si (-0.8%). This indicates that the channel is fully strained in the *x* direction. The strain in the *y* and *z* directions was +0.4% and +0.5%, respectively. This indicates that the lattice constant of the $Si_{0.8}Ge_{0.2}$ layer is larger than its equilibrium bulk lattice constant. The increase in the lattice constant is in response to the deformation caused by the compressive strain in the *x* direction. The results demonstrate that the channel exhibits uniaxial strain along the length of the channel.

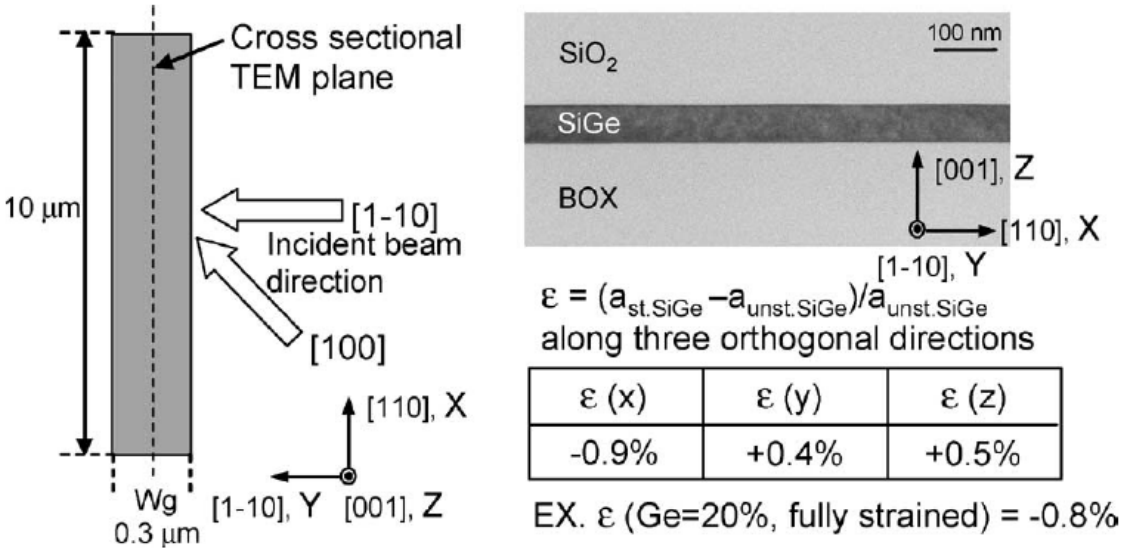


Figure 3-11. Schematic of the NBD strain measurements and summary of the strain in each direction [89].

Electrical characterization demonstrated that very little (approximately 10%) enhancement in hole mobility was achieved in large width channels when compared to control channels on SOI substrates. The small enhancement is due only to the increased Ge content in the channels, and not due to strain enhancements since the large-width channels are biaxially strained. However, as the channel width is reduced from 10 μm to 0.2 μm, the drain current of a pMOSFET fabricated on the channels is increased by 80 % (Figure 3-12).

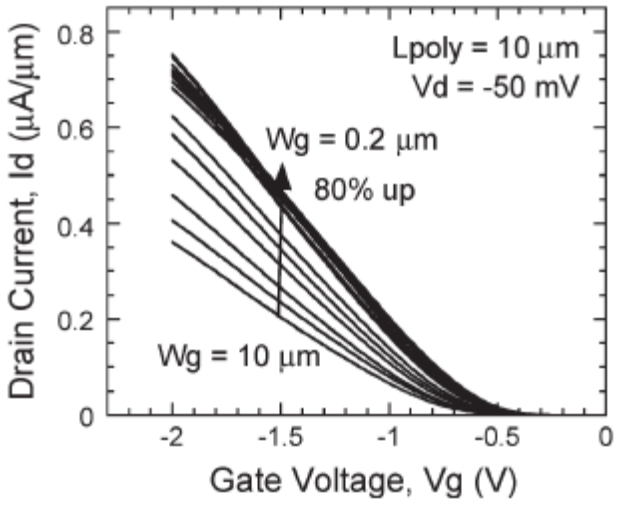


Figure 3-12. Drain current of holes with respect to the applied gate voltage in a pMOSFET fabricated on laterally strain relaxed SGOI. The length of the channel is 10 µm and the channel width (W_g) is reduced from 10 µm to 0.2 µm [89].

Irisawa *et al.* extended the lateral relaxation technique to fabricate high mobility nMOSFET devices [90]. Trigate nMOSFETS were fabricated on a uniaxial tensile SSOI, which was fabricated by the same process as the compressively strained pMOSFET SGOI devices described above. The mobility of the uniaxial strained nMOSFET was two times greater than the mobility of a control device fabricated from an unstrained SOI wafer.

The patterned lateral strain relaxation technique was extended to SiGe epilayers directly on Si by Uhm *et al.* [91-94]. The authors deposited a 25 nm, pseudomorphic film of $Si_{0.6}Ge_{0.4}$ on a Si (001) substrate by CVD followed by a strained Si cap. A hard SiO_2 mask was then deposited and the stripes were patterned by photolithography and etched by reactive ion etching (Figure 3-13a). The strain in the stripe was investigated by Raman spectroscopy using a visible (λ=488 nm) and a UV (λ=325 nm) laser. The use of two different wavelengths was essential to characterize the strain in the stripe as the visible laser will penetrate into the SiGe layer whereas the UV laser will not penetrate the Si capping layer if the thickness exceeds 4 nm [92]. In this way, the contribution to the strain relaxation from the Si capping layer can be decoupled from the SiGe layer. To further improve the accuracy of the Raman spectroscopy, a screening layer was deposited, as shown in Figure 3-13b, to eliminate signals from the Si substrate.

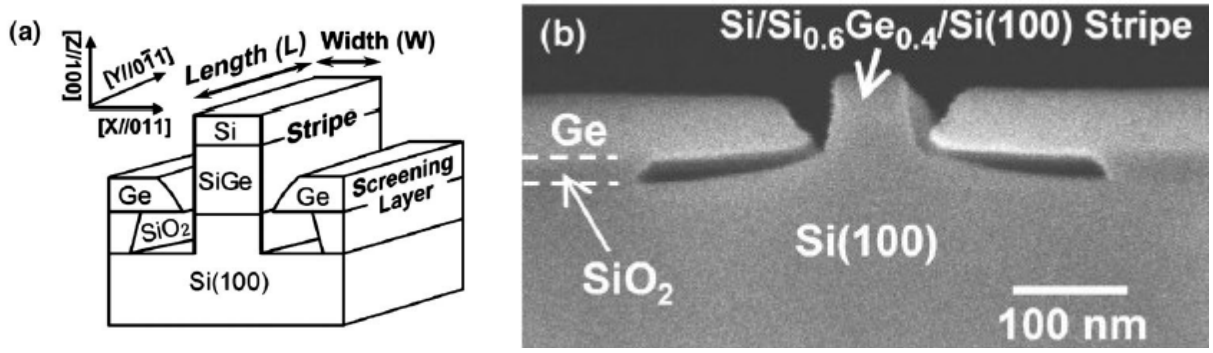


Figure 3-13. a) Schematic diagram and b) SEM micrograph of a stripe patterned Si/$Si_{0.6}Ge_{0.4}$ structure.

Raman spectroscopy confirmed that strain relaxation occurred in the SiGe stripes. The total relaxation increased from 20 % to 100 % as the stripe width was reduced from 600 nm to 20 nm [91]. However, the authors were unable to show that the strain in the channel was uniaxial. The effect of the Si capping layer thickness was also investigated. The Si layer is under tension, which counteracts the compressive strain in the SiGe layer. As a result, the Si capping layer hinders the complete relaxation of the SiGe layer. The strain relaxation in the SiGe layer was increased as the Si cap thickness was decreased from 10 nm to 5 nm [91]. This provides an additional tool to control the strain in the SiGe layer.

Hashemi *et al.* extended the lateral strain technique to high-Ge-content thin films, to fully exploit the mobility enhancement of Ge and bring the device dimensions closer to that of current transistors [95]. A Si/Ge/Si on insulator structure was fabricated using the bond and etch back technique described in Chapter 3.2.1. The Ge layer was 5 to 7nm thick and was under 1.8 % biaxial compression. The Si capping layer was 4 nm thick and was under 1.8 % biaxial tension. The pseudomorphic layers were grown on a strain-relaxed $Si_{0.5}Ge_{0.5}$ virtual substrate. The channels were patterned with widths of 300 to 30 nm. The strain relaxation was investigated by UV Micro-Raman spectroscopy, using a 325 nm He-Cd source. However, due to the small size of the channels, the low signal output of the samples required the use of a large spot size to sample multiple stripes simultaneously. In addition, Raman spectroscopy is unable to differentiate asymmetry in the relaxation. Thus, the calculated strain relaxation in the channels was modeled as biaxial. Using the biaxial strain model, Hashemi *et al.* showed that the strain relaxation increased from 10 % to 45 % as the stripe width was reduced from 300 nm to 30 nm.

Recently, Chen *et al.* reported a record high hole mobility in a pMOSFET device under high vertical field conditions [7]. Starting with a 10 nm thick SGOI layer [88] with 2.5% biaxial strain and a 3.5 nm thick strained Si capping layer, strips of various widths, from 0.425 to 15 µm, were patterned , as shown in Figure 3-14. In addition, strips were patterned in the <110> and <100> directions to investigate the impact of orientation on hole mobility. The effective hole mobility of the pMOSFET devices fabricated on the patterned strips increased as the strip width decreased, as shown in Figure 3-15. This is due to the increase in the uniaxial strain effect. However, the authors observed that strip widths up to 2 µm displayed mobility enhancement of 20 % over a biaxial control device, indicating that uniaxial relaxation occurs even at large widths. 15 µm wide strips did not display mobility enhancement, indicating that the device is biaxially strained. The narrowest strip investigated (425 nm) displayed a mobility enhancement of 50 % when compared to the biaxially strained control. The measured mobility of 955 cm^2/Vs is the largest hole mobility reported for strained Si/Ge pMOSFET devices.

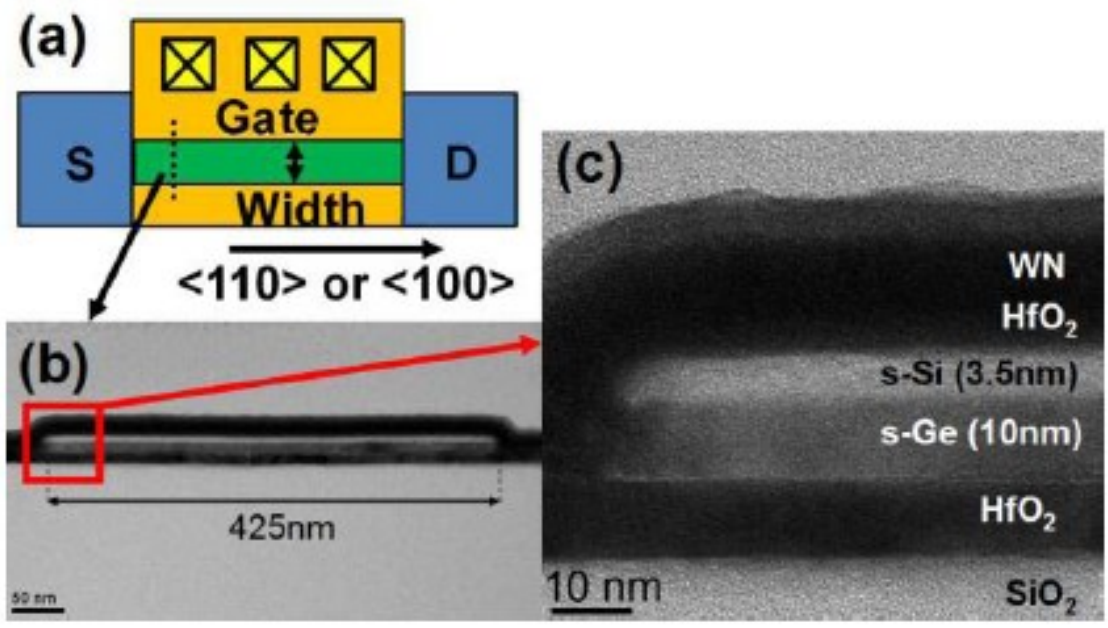


Figure 3-14. a) Schematic of the top-view of a p-MOSFET fabricated on a uniaxially strained Ge strip. b) Cross-sectional TEM micrograph of a 500 nm patterned width strip. c) High resolution micrograph of the p-MOSFET structure [7].

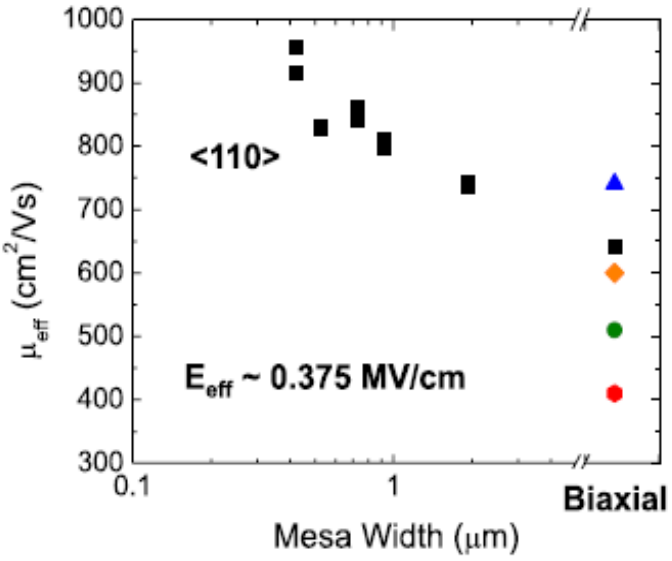


Figure 3-15. Effective hole mobility (μ_{eff}) vs. the mesa width for <110> oriented channels [7]. Benchmark hole mobilities for previously reported high-*k*/metal gate strained-Si capped strained-Ge devices at equivalent E_{eff} [96-98].

3.3.2. Uniaxial Strain by Selective Ion Implantation

A novel technique to pattern areas of uniaxially strained SiGe was developed by the group of Shiraki in Japan which utilized ion implantation to selectively relax SiGe epilayers. Hollander *et al.* have shown that the strain relaxation of a pseudomorphic SiGe epilayer on a Si substrate could be enhanced by ion implantation [99]. A 200nm $Si_{83.5}Ge_{16.5}$ epilayer was grown on a Si (100) substrate by MBE. The layer was shown to be fully strained by XRD. Hydrogen ions were implanted with an energy of approximately 25 keV and created a highly defective layer approximately 30 nm below the heteroepitaxial interface. Subsequent annealing of the sample promoted the nucleation of misfit dislocations. The ion implantation had two important effects on the strain relaxation of the epilayer. First, the defects caused by the ion implantation acted as nucleation sites for dislocation nucleation. This significantly increased the misfit dislocation density, and thus the total strain relaxation of the epilayer. The ion implanted samples showed 90% strain relaxation, compared to 55 % relaxation in samples without ion implantation. Secondly, the ion implanted samples showed two orders of magnitude fewer threading dislocations. The reduction in threading dislocations is attributed to the observation that the misfit dislocations would terminate at hydrogen induced cavities below the heteroepitaxial interface.

The previous observations were extended to induce uniaxial strain in a $Si_{0.73}Ge_{0.27}$ epilayer by selectively exposing strips of the substrate to Ar+ ion implantation [100-103]. In their process, a Si (001) substrate is patterned into strips using a SiO_2 hard mask. Ar^+ ions are then implanted in the unmasked regions at 25 keV. Following ion implantation, the oxide mask was removed and the substrate was annealed to recrystallize the damaged areas which ensures that defects are restricted to the selected areas. A pseudomorphic SiGe layer was then grown by MBE above the patterned substrate at 500 °C. The epilayer was then annealed at 900 °C to promoted strain relaxation.

Misfit dislocation nucleation is favoured in the regions lying above the ion-implantation strips due to the presence of defects at the interface, compared to the regions without defects. This results in an alternating pattern of relaxed and strained strips, as shown in Figure 3-16. The regions with greater strain relaxation have a larger in-plane lattice constant which causes these regions to impart a compressive strain on the non-relaxed strips. Thus, the regions lying above the un-implanted stripes exhibit uniaxial strain in the direction perpendicular to the strips.

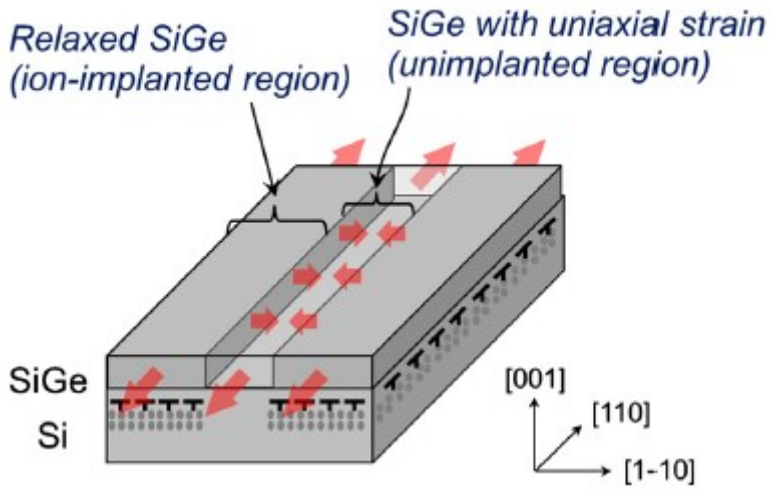


Figure 3-16. Schematic of a SiGe epilayer which is grown above a selectively ion-implanted Si substrate and the direction of the applied stresses [102].

The reciprocal space maps (RSM) shown in Figure 3-17 demonstrate the uniaxial strain effect. In Figure 3-17a, the X-ray beam is directed perpendicular to the strip direction, the resulting RSM

shows that the SiGe peak has the same reciprocal lattice constant, which indicates a fully strained layer. In Figure 3-17b, the SiGe peak is broader and shifted to smaller reciprocal lattice size, which indicates a relaxed layer. The researchers found that the degree of strain relaxation in the direction perpendicular to the strips is close to zero and up to 40 % in the direction of the strips [102].

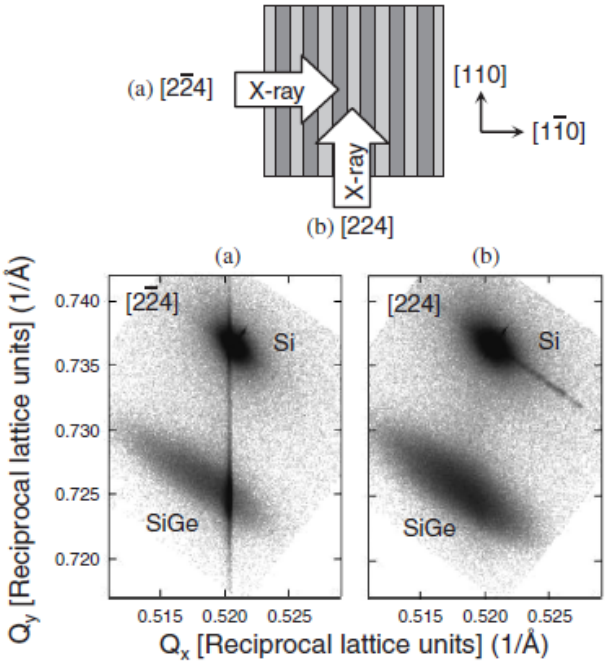


Figure 3-17. XRD reciprocal space map of the 224 asymmetric reflection of a $Si_{0.73}Ge_{0.27}$ epilayer on Si(100) in the direction a) perpendicular to the stripe pattern and b) parallel to the stripe pattern [100].

3.3.3. Strained Nanowires

As demonstrated above, as the aspect ratio of a strained channel is increased, lateral relaxation is favoured at the free edges which results in uniaxial strain along the channel length. To maximise this effect, strained nanowires have been proposed as the ideal structure for uniaxial strain and high mobility channels.

Feste *et al.* demonstrated that a strained nanowire is the ideal structure for uniaxial strain. They performed 2D finite element simulations of rectangles with various aspect ratios under tension

[104]. The simulations are presented in Figure 3-18. The simulations showed that the tensile strain in the y-direction of a rectangle spreads homogeneously throughout the shape at low aspect ratios (Figure 3-18a). At an aspect ratio of 8:1, the tensile strain is homogenous across the entire area. The strain relaxation in the x-direction is observed at aspect ratio of 8:1 (Figure 3-18b). However, complete and homogenous strain relaxation required higher aspect ratios, greater than 24:1. Thus, Feste *et al.* concluded that uniaxially strained tensile nanowires would be the ideal high mobility channel for nMOSFETs.

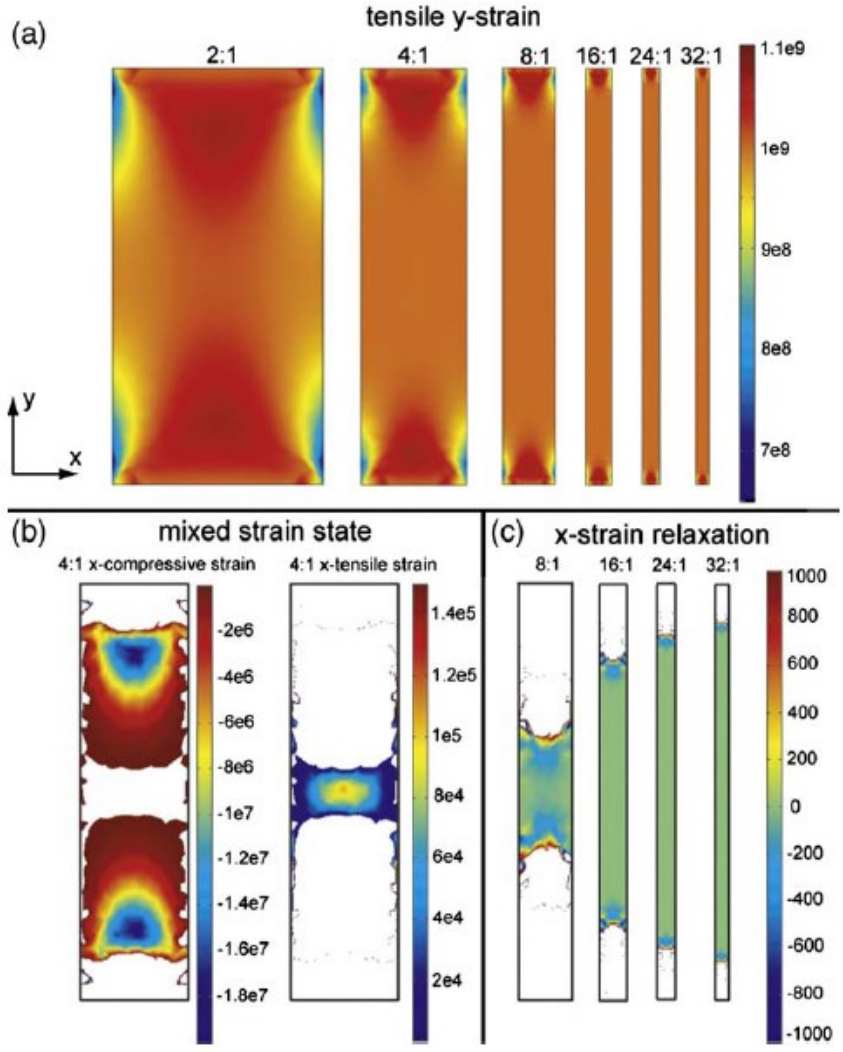
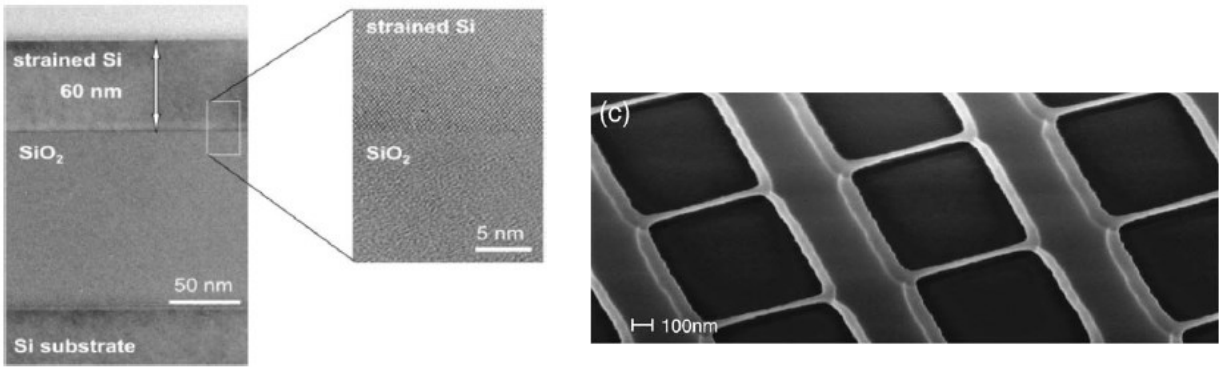


Figure 3-18. 2D Finite element simulations of the strain state in rectangles of different aspect rations is the y-direction (a), x-direction (c). The mixed tensile and compressive strain is illustrated in b) for a 4:1 aspect ratio rectangle.

The challenge to develop strained nanowire devices is the fabrication and integration of the nanowires. Feste *et al*. proposed a top-down solution to fabricate strained nanowires [104, 105]. Beginning from a SSOI substrate (Figure 3-19a), the nanowires were patterned by photolithography and etched by RIE. The buried oxide layer was then under-etched using diluted HF acid. Lastly, the nanowire side walls were smoothed by a sacrificial oxidation followed by HF etching. The resulting strained nanowires are shown in Figure 3-19b. It was determined by simulation that 80% of initial the biaxial strain (1.2 GPa) was retained as uniaxial strain along the nanowire length.



a) b)

Figure 3-19. a) TEM crossection of the 60 nm thick strained Si on SiO_2 which is above a Si substrate [105]. b) SEM image of strained Si nanowires with smooth side walls after oxidation and etching. Nanowire diameter is 30 nm [104].

nMOSFETS were fabricated from the strained nanowires described above. The performance of strained nanowire nMOSFETs was compared to control devices fabricated on an unstrained SOI substrate. The mobility in the strained nanowire nMOSFET was increased by a factor of 2.8 over the unstrained nMOSFET [105]. A shortcoming of this technique is the lack of hole mobility enhancement for pMOSFET devices. However, the authors concluded that the orientation of the wires was an important parameter for controlling MOSFET performance. Nanowires aligned along the <110> direction on a (100) substrate reduced the difference between the performance of nMOSFET and pMOSFET devices since hole mobility is highest in the <110> direction [106].

An alternative method to fabricate strained nanowires was proposed by Najmzadeh *et al. [107, 108]*. The strain in the nanowires is induced during thermal oxidation. The method utilises a top-down approach that is fabricated from a bulk silicon wafer which is illustrated in Figure 3-20.

A summary of the strained nanowire fabrication process follows:

1. A hard SiO_2 and Si_3N4 mask is deposited on a Si (001) substrate. The Si mesas are then etched by RIE. The Si is etched by sacrificial oxidation and HF etching to undercut the hard mask. A Si_3N_4 layer is then deposited on the Si sidewall.
2. An isotropic dry Si etch undercuts the Si_3N_4 mask on the Si sidewalls which creates a narrow Si neck below the mask.
3. The Si neck is removed by sacrificial oxidation and HF etching. This creates the floating nanowires. The nanowire thickness can be further reduced by subsequent oxidation and etching steps.
4. The free space below the nanowires is back filled with low temperature oxide.
5. Deposition of the ploy-Si gate.
6. Metallisation of the device contacts.

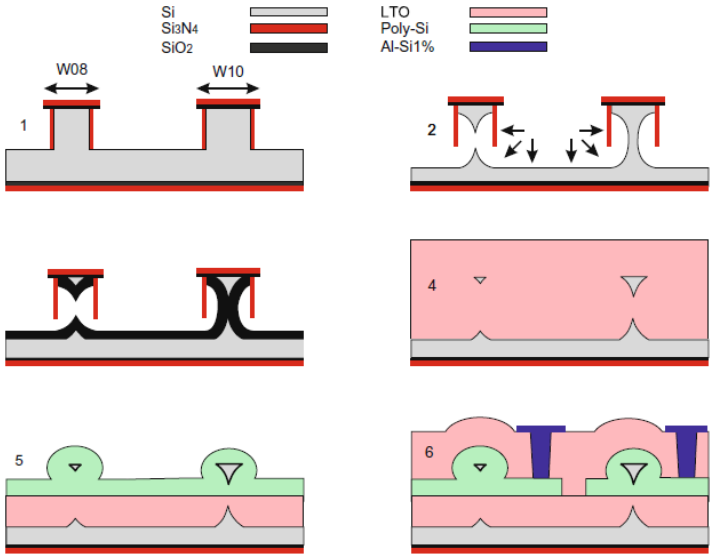


Figure 3-20. Schematic of the process flow to fabricate strained Si nanowires [108]. W08 and W10 represent the initial widths of the nanowires, 0.8 and 1.0 µm.

The initial Si substrate is unstrained and the strain is introduced into the nanowires during processing. This provides a process that is more compatible with traditional CMOS fabrication since it does not require the fabrication of a strained-silicon-on-insulator substrate.

The nature of the strain in the nanowires was investigated by Najmzadeh *et al*. They observed that the nanowires buckled after the SiO_2 layer undercutting due to the induced tensile strain from the Si_3N_4 hard mask. Raman spectroscopy was used to quantify the strain in the nanowires, as shown in Figure 3-21. Oxidation of the nanowires induces biaxial strain in the nanowires, which reduces the overall tensile strain. Lastly, after the oxide and hard mask layers were removed, the nanowires elongate to relieve the stored mechanical potential energy from the oxidation step. This increases the uniaxial tensile strain in the nanowires by a factor of 3-5. The total tensile stress following processing can reach up to 2.6 GPa [107], which is significantly greater than the stress achieved in the previously described methods.

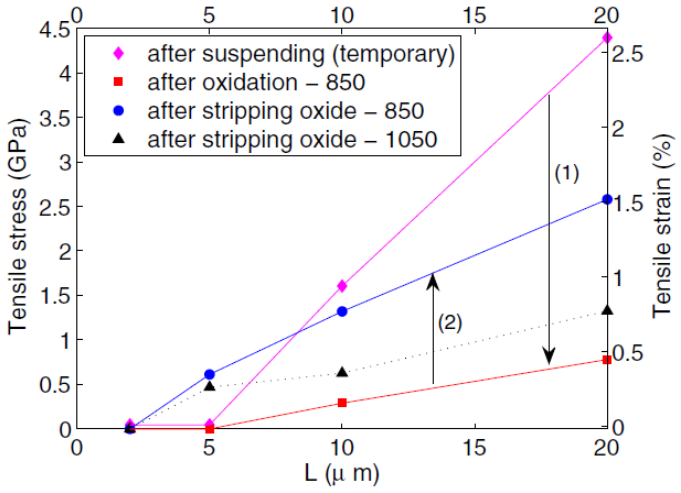


Figure 3-21. Variation in the stress vs. the nanowire length at the different steps of the fabrication process: 1) The stress in the suspended nanowire, 2) The stress in the nanowire after the wet oxidation at 850°C and 3) The stress in the nanowire after removal of the hard mask and grown oxide [107].

The strained nanowires fabricated by Najmzadeh *et al.* were used to fabricate gate-all-around nMOSFETs. The strained devices displayed a 64% electron mobility enhancement. The average electron mobility was 525 cm^2/Vs, which represents a 64 % increase over an unstrained control device fabricated from an SOI substrate.

A third technique to induce uniaxial strain in nanowires was reported by Singh *et al.* [109]. The authors observed severe deformation of unstrained nanowires, fabricated from an SOI wafer, upon deposition of a high-k dielectric and TaN metal layers, as shown in Figure 3-22. From measurements on bulk Si, the deposited TaN layer is compressively strained, with a compressive stress of approximately 200 MPa. When deposited on unstrained Si nanowires, the nanowires increase in length by up to 4%, which corresponds to a tensile stress of greater than 4 GPa. This is the largest reported tensile stress reported in Si nanowires for nMOSFET applications.

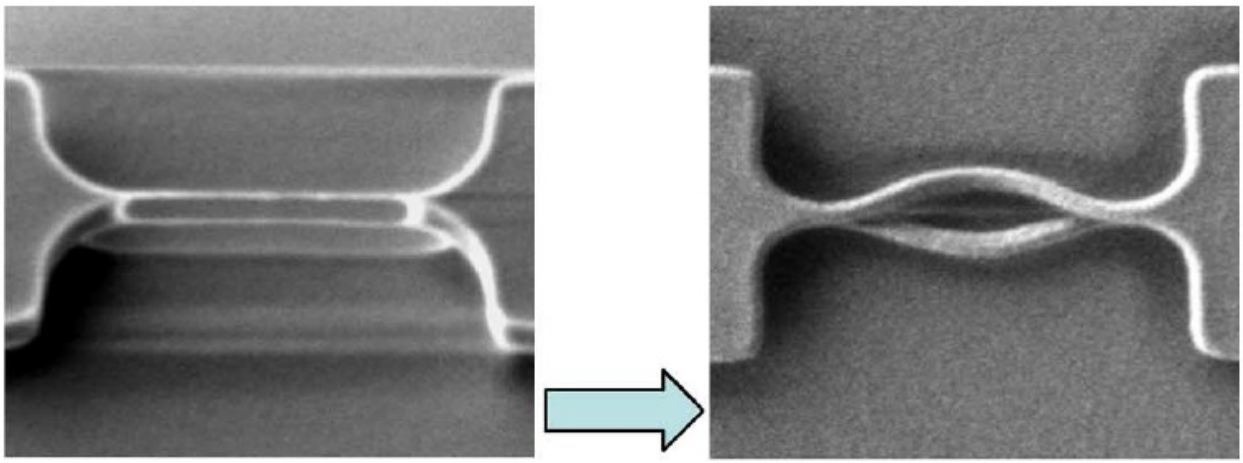


Figure 3-22. Tilted SEM micrograph of two suspended Si nanowires before (left) and after (right) deposition of a high-k dielectric and TaN metal layers [109].

The techniques described in the chapter have fabricated Si and SiGe structures with uniaxial tensile and compressive strain and which have demonstrated record-breaking carrier mobilities. However, these techniques have their limitations. The uniaxial compressive strain achieved by selective relaxation, either by substrate patterning or ion-beam implantation, is restricted to narrow strips and requires multiple photolithographic, deposition and etching processes. The strained nanowires provide exceptional tensile strain improvements, but are not suitable for compressive strain. A novel lateral growth technique will be introduced in Chapter 5 which can deposit uniaxial compressive strained SiGe epilayers on Si (001) in a single step and which is not limited to narrow strips.

3.3.4. Uniaxial Strain on Si (110)

Uniaxial strain relaxation of SiGe on Si (001) substrates can only be achieved, so far, by reducing the symmetry of the epilayer, as discussed in the preceding section, to induce preferential strain relaxation in a given [110] direction. Uniaxial strain can be achieved on Si (110) substrates without patterning due to the unique orientation of the slip planes with respect to the substrate surface. SiGe growth on Si (110) was first reported by Hull *et al.* in 1991 [110]. As discussed in Chapter 2.1, strain relaxation in SiGe epilayers occurs primarily with dislocation nucleation and glide in the {111}<110> primary slip system. On a Si (001) substrate, four {111} planes intersect the substrate surface along the orthogonal <110> directions (Figure 3-23) which allows for misfit dislocation nucleation and glide in both <110> directions. The orthogonal misfit dislocation network produces isotropic strain relaxation. On a Si (110) substrate only two {111} planes intersect the substrate in a <110> direction (Figure 3-23). Since both planes intersect in the [1$\bar{1}$0] direction, misfit dislocations can only be nucleated and glide in this direction. The result is an array of parallel misfit dislocations aligned in the [1$\bar{1}$0] direction [27], as shown in Figure 3-24.

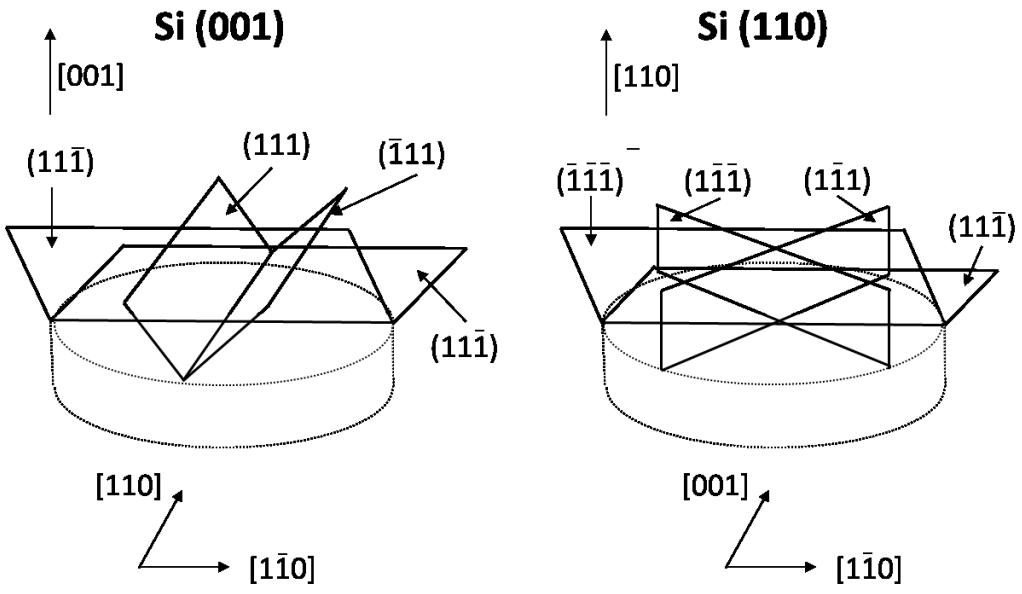


Figure 3-23. Schematic of the {111} glide planes on Si (001) and Si (110) substrates. Modified from [110].

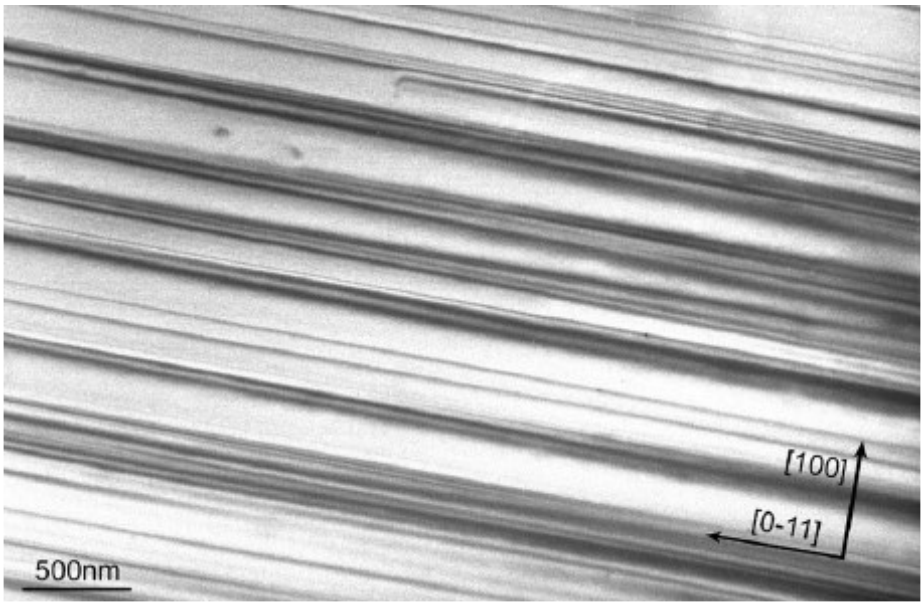


Figure 3-24. TEM micrograph of an a array of parallel misfit dislocations aligned in the [0$\bar{1}$1] direction on a Si (100) substrate [111].

Since the strain relaxation occurs in the perpendicular direction of a misfit dislocation, plastic strain relaxation on Si (110) is confined to the [001] direction. Strain relaxation does not occur in the [1$\bar{1}$0] direction as a result of plastic deformation from the array of misfit dislocations. Figure 3-25 shows the reciprocal space maps (RSM, which are explained in detail in Chapter 6.1) of an 80 nm thick pseudomorphic $Si_{0.8}Ge_{0.2}$ epilayer grown by MBE on a Si (110) substrate [112]. The in-plane relaxation can be determined from the (260) maps (Figure 3-25 a & c) which represent the strain relaxation in the [1$\bar{1}$0] direction and the (062) maps (Figure 3-25 b & c) which represent the strain relaxation in the [001] direction. The RSMs for the pseudomorphic epilayer (Figure 3-25 a & b) show that the $Si_{0.8}Ge_{0.2}$ epilayer peak lies directly below the Si substrate, which indicates that the epilayer is fully strained in both the [1$\bar{1}$0] and [001] in-plane directions. Following a 900 ˚C anneal which promoted the nucleation and glide of an array of parallel misfit dislocations, the RSM shows strain relaxation in the [001] direction (Figure 3-25d), whereas the epilayer remains fully strained in the [1$\bar{1}$0] direction (Figure 3-25c). This demonstrates that the array of parallel misfit dislocations produces an asymmetrically strained epilayer. Further strain relaxation in the [001] direction, aided by increased misfit dislocation nucleation from ion implantation, can produce an epilayer with uniaxial strain [111].

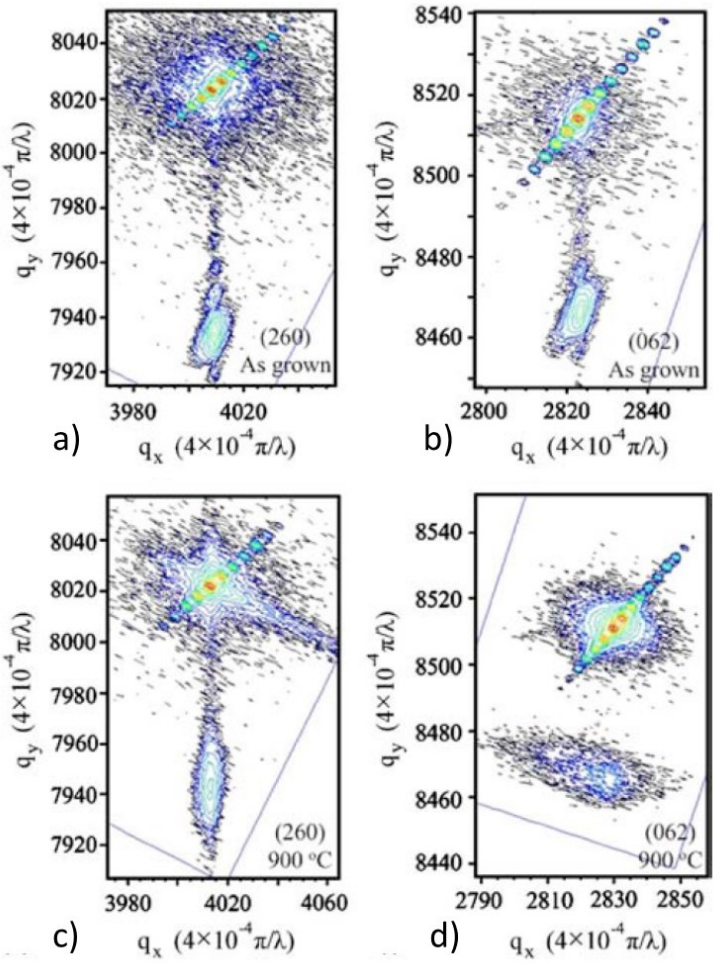


Figure 3-25. Reciprocal space maps of a $Si_{0.8}Ge_{0.2}$ epilayer on a Si (110) substrate. a) (260) map of the pseudomorphic layer which shows the strain relaxation in the [1$\bar{1}$0] direction, b) (062) map of the pseudomorphic layer which shows the strain relaxation in the [001] direction, c) (260) map of the epilayer after a 900 °C anneal and c) (062) map of the epilayer after a 900 °C anneal. Modified from [112].

The growth of SiGe epilayers on Si (110) allows for the deposition of a blanket film with asymmetric strain due to the formation of an array of parallel misfit dislocations, which cannot be accomplished by current techniques on Si (001) substrates due to the symmetry of the crystal structure. A novel technique to fabricate a blanket film with asymmetric strain due to the formation of an array of parallel misfit dislocations on Si (001) substrates is introduced in Chapter 5 and the strain asymmetry in SiGe epilayers is reported in Chapter 7.

Chapter 4

Liquid-Phase Epitaxy

Liquid phase epitaxy (LPE), also known as solution growth, is a semiconductor growth technique in which a crystal is formed by the precipitation of solute semiconductor atoms onto a crystalline substrate from a metallic solvent. LPE is distinguished from melt growth by the composition and temperature of the liquid growth medium. Melt growth occurs at temperatures near the melting point of the semiconductor whereas LPE growth occurs from a dilute eutectic growth solution which must be heated to significantly lower temperature than the semiconductor melting point. In addition, LPE is distinguished from vapour phase epitaxy (VPE) techniques by the transport of the semiconducting precursors or atoms to the substrate which occurs in a liquid solvent, as opposed to the gas or vapour phase, as is the case for chemical vapour deposition (CVD) and molecular beam epitaxy (MBE).

The following chapter provides an overview of the development of LPE as well as the various experimental setups developed for this technique. The primary considerations and challenges for LPE growth are also outlined to provide the conditions for optimal growth. First the aspects of LPE which are applicable to any epitaxial system are presented, followed by the specifics of LPE for SiGe on Si heteroepitaxy.

4.1. Development of LPE

LPE was first reported by Nelson in 1963 [113] and quickly became the technique of choice for the deposition of GaP, GaAs and AlGaAs and other III-V, II-VI and IV-VI compound thin films [114, 115]. The rapid adoption of LPE is in part due to the challenges associated with the epitaxial growth of these compounds at the time by CVD. In the 1960's, Si CVD epitaxy was a well established epitaxial growth technique, however, III-V CVD epitaxy was plagued by non-stochiometric deposition which produced, for example, a large number of Ga vacancies or As antisite defects in GaAs. In addition, the hydride or halide precursors used for AlGaAs compounds posed significant challenges due to aluminum's affinity for oxygen [52]. Early development of LPE was driven by its ability to produce III-V thin films with excellent stoichiometry, crystal quality and low defect densities.

The ability to grow thin films with excellent stoichiometry is illustrated by the binary phase diagram of a III-V semiconductor system (Figure 4-1). At temperature T_1 and composition X_1, the solution lies on the liquidus line. As the solution is cooled to T_2, the liquid composition will follow the liquidus line until it reaches composition X_2. However, the crystallised solid phase will be the stochiometric AC line compound. The composition of the solid phase does not vary with temperature. In this way, stochiometric GaAs thin films can be grown from a Ga solution that is saturated with As.

The high crystal quality and low defect density of LPE thin films is a result of the crystal growth occurring very near thermodynamic equilibrium. The driving force for deposition in LPE is the difference in chemical potential, $\Delta\mu$, between the saturated solvent phase μ_0 and the solid crystalline phase μ established by undercooling the solution below the liquidus temperature [116].The driving force for deposition in LPE is the difference in chemical potential, $\Delta\mu$, between the saturated solvent phase μ_0 and the solid crystalline phase μ established by undercooling the solution below the liquidus temperature [116]. If $\Delta\mu = \mu - \mu_0 < 0$, then there is a thermodynamic driving force for crystal growth. In LPE, the undercooling can be controlled such that $\Delta\mu < 0$ for crystal growth, $\Delta\mu = 0$ for thermodynamic equilibrium and $\Delta\mu > 0$ for etching. The resulting chemical potential can be engineered to be very small. For this reason, LPE is often called an equilibrium deposition technique. There is a three orders of magnitude difference in the relative

Gibbs free energy between the reactants and products (i.e. the magnitude of the driving force for crystal growth) between LPE, CVD and molecular beam epitaxy (MBE) is shown in Figure 4-2. The near-equilibrium growth of LPE results in epitaxial layers with the greatest crystal perfection and lowest defect densities, when compared to the VPE techniques [117].

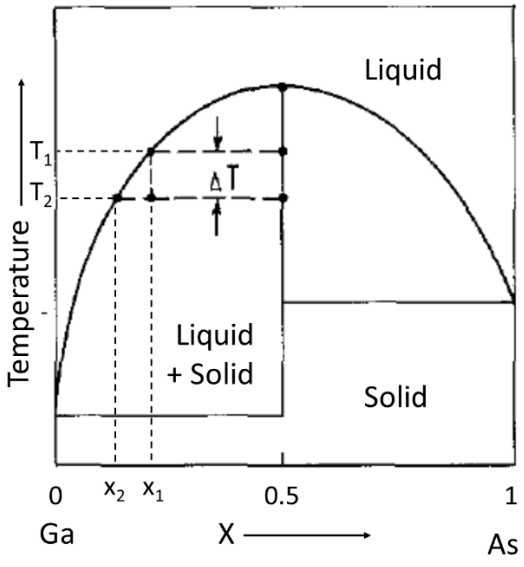


Figure 4-1. Binary phase diagram of Ga-As system [118].

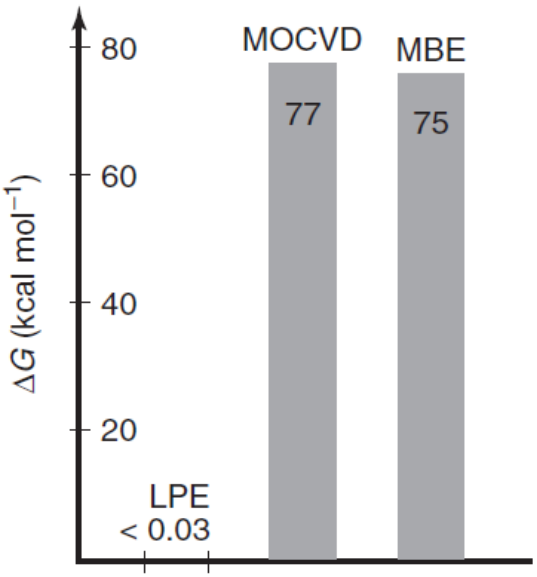


Figure 4-2. Estimated Gibbs free energy between reactants and products in semiconductor epitaxy techniques [7]

A typical LPE temperature profile is shown in Figure 4-3. Undercooling is achieved by cooling the growth solution according to one of two different cooling profiles. The first is equilibrium cooling (Figure 4-3, solid line). In equilibrium cooling the substrate is introduced to the solution at the saturation temperature (T_S), the temperature at which the solution is saturated with the semiconductor solute, and is then cooled at a constant rate to the final temperature (T_f), after which the substrate is removed from the solution and cooled to room temperature. A constant driving force for crystal growth is maintained throughout the deposition. The second cooling profile is termed supercooling (Figure 4-3, dashed line). In supercooling growth, the substrate is introduced to the solution at T_U, where T_S-T_U=ΔT represents the initial undercooling of the solution. The solution is then cooled at a constant rate until T_f. The initial undercooling will yield a higher initial growth rate and can modify the growth morphology of the crystal as discussed in Chapter 4.7.

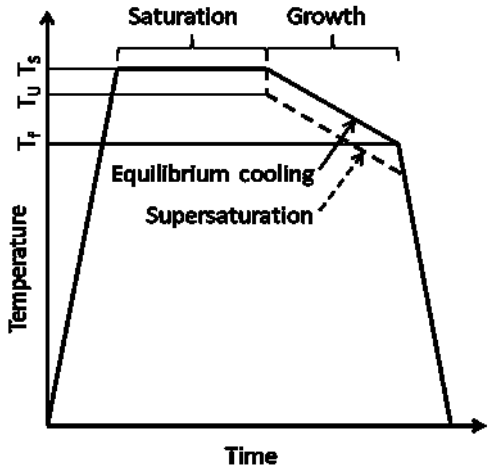


Figure 4-3. Temperature profiles for LPE growth. Equilibrium cooling is shown with a solid line and supersaturation cooling is shown with a dashed line.

The high crystal quality and the ability to deposit stochiometric III-V epitaxial layers by LPE were essential to numerous important advancements in optoelectronic devices. In particular, the deposition of $Al_{1-y}Ga_{1-x}As$ compounds, as demonstrated by Rupprecht, Woodall and Pettit at IBM Laboratories in 1967 [119], was achieved by LPE. The ability to deposit, lattice matched, $Al_{1-y}Ga_{1-x}As$ double heterostructures, was previously impossible due to the instability of AlAs [120]. This led to the development of the first GaAs/AlGaAs double-heterostructure laser diode continuous-wave lasing at room temperature [121]. , for which, in part, Zhores I. Alferov was awarded the Nobel Prize in physics in 2000. An extended list of optoelectronic achievements using LPE is provided in Kuphal's review paper [118].

In addition to the advantages discussed above, LPE is an economical epitaxial growth technique. The capital cost of an LPE system can be up to 10 times less than a CVD or MBE system [118, 122]. The low capital cost is due to the technological simplicity of an LPE system which operates at atmospheric pressure and does not require the ultra-high vacuum systems necessary for CVD and MBE operation. In addition, LPE does not require the use of expensive, toxic and pyrophoric gas precursors which require expensive safety mechanisms.

The deposition rate of LPE is significantly greater than the VPE techniques (1 μm/min [52]) which further improves LPE's economic advantage and allows for the deposition of thick layers, up to 100 μm. The deposition efficiency of LPE is very high. In binary systems where the solvent is re-

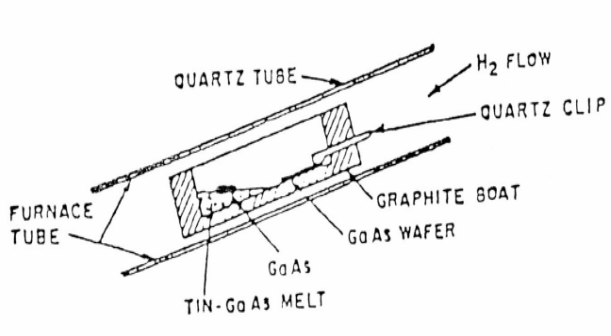
used, the deposition efficiency can approach 100% [118] . In addition to the high efficiency, the reuse of the solvent eliminates the solid waste produced by solidified spent growth solutions, which is the only waste product produced by LPE.

4.2.LPE Growth Techniques

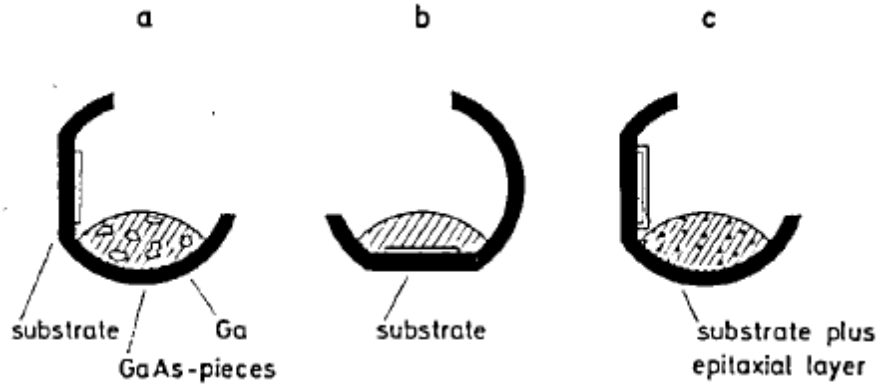
The original LPE experiments by Nelson in 1963 used a tipping boat to deposit GaAs [113]. In Nelson's design, the substrate was placed at one end of a graphite crucible and the growth solution at the opposite end as shown in Figure 4-4a. To initiate the growth, the entire furnace was tipped such that the solution flowed onto the substrate. To terminate the growth, the furnace was tipped in the opposite direction and the solution flowed off the substrate. The tipping boat design was significantly improved by Bauser's rotating boat in 1974 [123]. In this design, the substrate is placed on the boat sidewall, as shown in Figure 4-4b, the boat is rotated along the longitudinal axis to cover the substrate with the growth solution. The boat is then rotated back to its original position to terminate the growth. The rotating boat method does not require the entire furnace and quartz tube to be tipped to initiate and terminate growth, which greatly reduces the complexity of the LPE system.

An important development to the rotating boat LPE systems was the introduction of the sliding boat by Kaufmann and Heime in 1977 [124]. This design contains multiple chambers, one for each growth solution. The substrate is placed on a slider and can be introduced into each chamber and brought into contact with the growth solution by rotating the boat, as in Bauser's design. In this way multilayer growth can be achieved.

The primary advantage of the tipping/rotating boat design is that the contact time between the substrate and growth solution can be accurately controlled since there is no risk of solution carry-over [125, 126]. In addition, there are no moving parts within the boat which eliminates contamination from graphite particles and damage to the substrate by abrasion. However, thickness variations are common due to uneven substrate coverage and two dimensional diffusion [118].



a)



b)

Figure 4-4. Schematic of tipping boat LPE systems. a) Nelson's tipping boat [113], b) Bauser's rotating boat [123].

An alternative LPE technique is the dipping LPE system. The growth solution is contained in a graphite crucible within a vertical furnace. Growth is initiated by lowering the substrate into the growth solution, as shown in Figure 4-4. This was technique was used by Rupprecht, Woodall and Pettit at IBM Laboratories in 1967 to deposit $Al_{1-y}Ga_{1-x}As$ p-n junctions on GaAs substrates [119]. The doping was achieved by counter doping the growth solution. Dipping LPE does suffer from thickness variations due to two dimensional diffusion and solute transport by convection, though convection problems can be minimized by rotating the substrate [127].

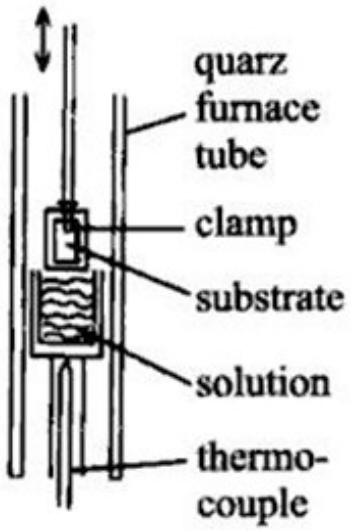


Figure 4-4. Schematic of a dipping LPE system [128].

Dipping LPE is the most suitable technique for the mass production of LED wafers, for which thickness homogeneity is not critical. Holmes and Kamath developed the infinite solution LPE technique in 1982 [129]. Using a growth solution up to 1 kg (compared to growth solutions of a couple of grams in standard LPE set-ups), numerous substrates can be dipped sequentially. Industrially, this can be scaled up such that hundreds of wafers can be dipped simultaneously [118].

The most commonly used LPE system is the multi-bin sliding boat technique. The graphite boat contains multiple chambers and the substrate is placed on a graphite slider, as shown in Figure 4-5. The substrate is introduced into each chamber sequentially by lateral motion of the slider which is activated by hand or by a computer controlled for precise movement and growth times. This technique was used by Panish *et al.* to fabricate the first GaAs/AlGaAs double-heterostructure laser diode continuous-wave lasing at room temperature [121]. The sliding boat technique is the preferred method to deposit multilayered structures by LPE since it does not require rotational motion, such as the rotating/sliding boat of Kaufmann and Heime [124].

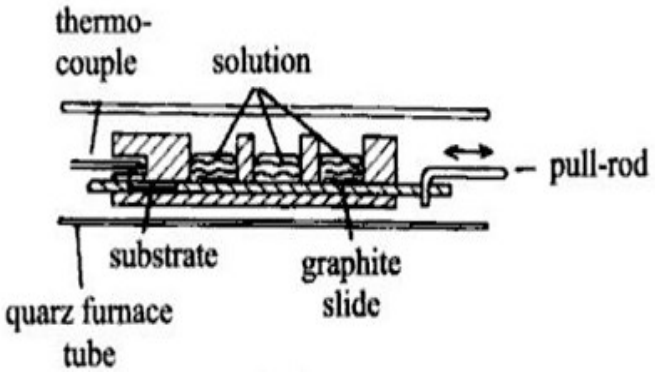


Figure 4-5. Schematic of a horizontal multi-bin, sliding boat, LPE system.

4.3. LPE Growth Challenges

Thin film growth by LPE in a multi-bin sliding-boat LPE system presents many challenges, many of which are common to all LPE systems. The following section will discuss these challenges and present solutions in the context of a multi-bin, sliding boat, configuration.

Solution carry-over is the primary concern in sliding-boat LPE systems. Solution carry-over occurs when the solution is not entirely removed from the substrate surface as it is removed from the growth well. The entrained solution can, in the case of multi-layer growth, contaminate the subsequent wells or, in the case of single-layer growth, act as an undesirable source of secondary deposition while the substrate is cooled to room temperature, which reduces thickness control. It has been shown that 3D island growth on top of the deposited epilayer can be nucleated from the entrained growth solution during the secondary growth phase [130].

Solution carry-over is a function of the gap between the well and substrate (S_2 in Figure 4-6), the solution height and the velocity of the substrate [131]. Depending on the contact angle between the solution and substrate, the optimal S_2 height has been shown to be as low as 20 μm [118]. If S_2 is too small, the lateral motion of the substrate and slider may cause abrasion between the graphite parts and between the graphite and the substrate. The abrasion particles act as growth defects during crystal growth. Abrasion can be minimised with the use of high-quality graphite parts. Wilson *et al.* [131, 132] showed that in addition to minimizing the gap S_2, solution carry-over can be minimised by reducing the solution pressure head and increasing the pull velocity. The

solution pressure forces the solution into the channel between the substrate and the well. This pressure is proportion to the height of the solution and can thus be minimised by lowering the solution height. The pull velocity is the speed at which the substrate is removed from the growth solution. Solution carry-over was shown to be reduced with increasing pull velocity, perhaps due to wafer edge effects or dynamic wetting effects. Lastly, the surface morphology will influence the solution carry-over. Non-planar surfaces, such as etch pits and ridges caused by a melt-back step or 3D features such as pyramidal island growth, will increase the solution carry-over.

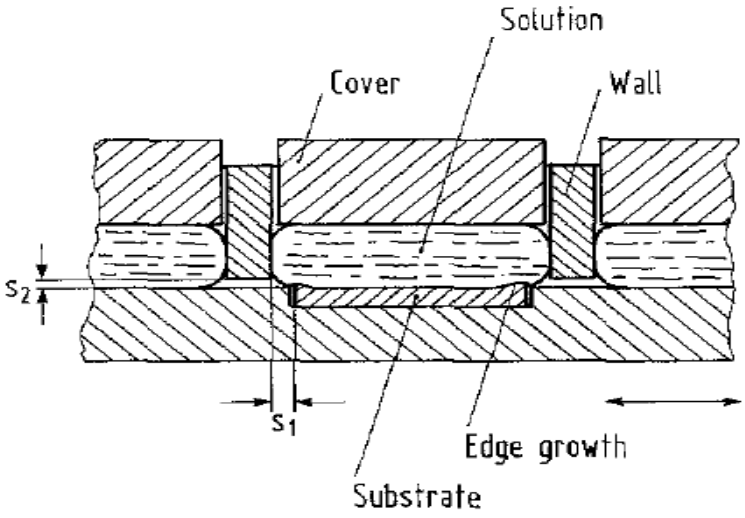


Figure 4-6. Schematic of the growth wells of a multi-bin sliding boat LPE system [115]. The height S_2 between the substrate and solution is indicated.

Edge growth is a second concern in a sliding boat system. Edge growth reduces the uniformity of the epilayer as the growth rate that the edges may be significantly greater than in the centre of the substrate [133]. Edge growth may be caused by thermal convection, orientation-dependant growth at the substrate edge, two-dimensional solute diffusion in the well and growth effects related to the solution surface tension [118]. Thermal convection occurs when a temperature gradient exists within the solution-well. This can be minimised by reducing the cooling rate [134]. Orientation effects can be eliminated if the solution contact area is smaller than the substrate. Two-dimensional diffusion and surface tension effects can be minimised by capping the solution and ensuring that the solution height is smaller than the contact width of the solution (Figure 4-6). If the temperature gradient in the solution is small and the solution height and the radius of curvature of the solution are smaller than the substrate, the LPE growth process can be modeled as a one dimensional

diffusion process [118]. Since LPE is near-equilibrium, the growth rate of the crystal is a function of the transport of the solute through the boundary layer perpendicular to the substrate.

The control and homogeneity of the epilayer thickness is a significant challenge for LPE, when compared to VPE techniques. Traditional LPE techniques are not well suited for the growth of thin and abrupt junctions required for quantum well devices. Thin layers can be grown by careful control of the supersaturation [135]. However, in practice, precise control of the supersaturation is difficult. The linear rapid slider boat technique was developed for the deposition of thin epitaxial layers by minimizing the contact time between the growth solution and the substrate. A schematic of a rapid linear slider boat is shown in Figure 4-7. The width of the contact area between the growth solution and the substrate can be varied and reduced to less than 1 mm [136]. In addition, the slider is moved at high speed (up to 1 m/s) such that the contact time is on the order of milliseconds [137]. The rapid slider techniques has been shown to grow epilayers with thicknesses on the order of 10^2 Å or less for AlGaAs [138], InGaAsP [139] and InAsSb [140] alloys. Using this technique, a multilayer structure can be deposited in a single run. This allows multilayered devices, such as quantum well lasers to be deposited in a couple of minutes, as opposed to several hours by MBE [141].

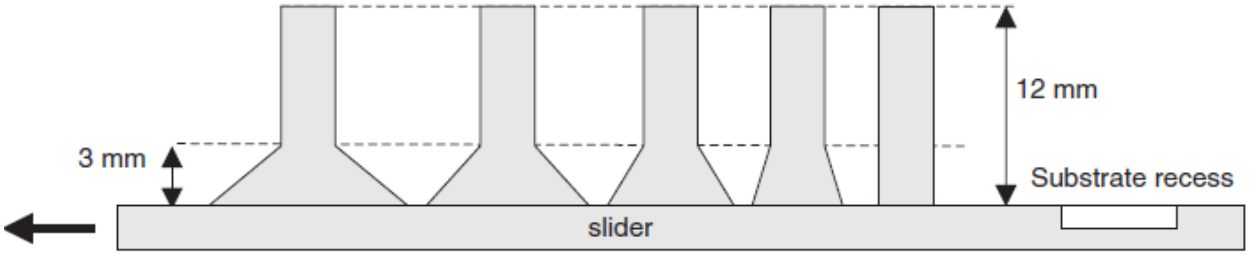


Figure 4-7. Schematic of the cross-section of a linear rapid slider boat [141].

Rezek *et al.* [137] demonstrated that the growth rate of epilayers grown by the rapid slider technique with contact time less than 200ms do not follow the $t^{1/2}$ relationship of a diffusion limited deposition [142], as shown in Figure 4-8. This result is expected as the short contact time prohibits the system from reaching equilibrium. Further investigation by Garbuzov *et al.* [143] showed that for very short contact times (<10 ms) the growth rate was independent of the contact time. In addition, the growth rate increased with the width of the slot of the solution chamber (i.e. the

contact area). These results indicate that the growth rate for short contact times is not limited by diffusion or attachment kinetics, but rather by the convective mass transport of the solutes in the solution caused by the flow of the growth solution induced by the rapid movement of the slider [141].

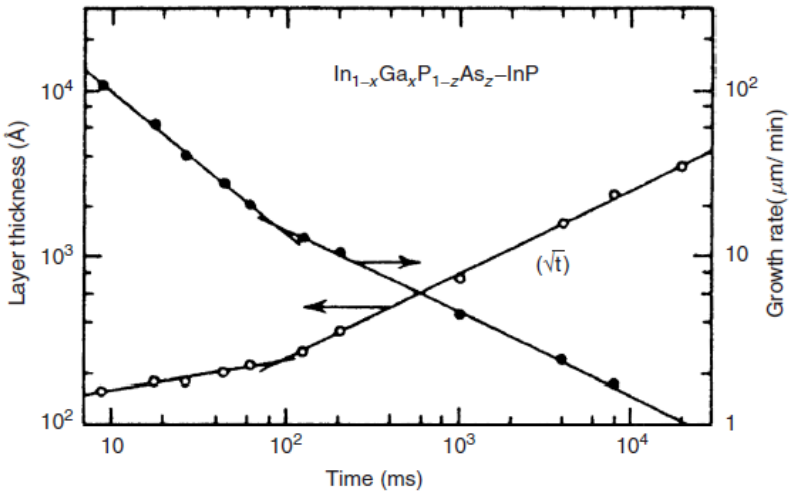


Figure 4-8. Variation of the epitaxial layer thickness and growth rate as a function of the contact time between the growth solution and the substrate [137].

Lastly, LPE deposition occurs at atmospheric pressure. This is an advantage for LPE growth over the VPE techniques since it reduces the equipment cost and complexity. However, without the benefit of a high vacuum environment, LPE is very sensitive to the growth parameters and environment. LPE typically occurs in a high purity H_2 environment which prevents the oxidation of the substrate and decomposition of the graphite boat [118]. It has been shown that changing the ambient gas from hydrogen to argon, for example, will change the contact angle between the silicon substrate and the solution[144] and can, in the case of epitaxial lateral overgrowth, reduce the aspect ratio of the crystal [145].

Growth on Si substrates is particularly sensitive to the presence of oxygen or moisture. Incomplete removal of the native oxide layer prevents smooth layer growth and can result in 3D island growth [146]. The Si native oxide layer is typically removed by an HF wet etch prior to loading the sample into the furnace. The removal of any oxide that may regrow due to trace amounts of oxygen in the furnace can be removed by hydrogen reduction in the in H_2 environment at temperatures greater

than 930°C [147]. In addition, the native oxide layer may be removed by the addition of trace amounts of high purity Al to the solvent. The etching reaction is given below [145]:

$$4Al_{(l)} + 3SiO_{2(s)} \rightarrow 3Si_{(l)} + 4Al_2O_{3(s)}$$

4.4. Development of SiGe LPE

Si and Ge deposition from a metallic solution predates LPE and CVD epitaxy technologies. Keck and Broder [148] and Carman *et al.* [149] demonstrated that high quality junctions could be created by depositing a bead of metal on a Si or Ge substrate. The substrate was heated above the metal-semiconductor eutectic temperature to melt the metallic bead. The liquid metal dissolved the semiconductor substrate until the solubility limit of the solution was achieved. Upon cooling the solution, the semiconductor recrystallized on the substrate as an epitaxial layer with trace amounts of the metallic solvent incorporated as dopants. This technique, known as *alloying* or *meltback* was the primary technique to fabricate diodes and bipolar transistors until 1960 [52].

LPE growth on a Si substrate was first reported by Donnelly and Milnes in 1966 [150]. The primary challenge which delayed the development of LPE growth on Si was the difficulty in obtaining an oxide free Si surface. Donnelly circumvented the oxide problem by cleaving a Si bar *in-situ* which exposed an oxide free surface for heteroepitaxial growth, on which a 127 μm thick Ge epilayer was deposited from a Sn solution.

As discussed above, LPE development was driven by the need to deposit stochiometric, epitaxial, III-V films with high crystal quality for the development of optoelectronic devices, which was unachievable by CVD at the time. Si deposition by CVD was demonstrated in the 1950's , and was a well established deposition technique by the time LPE was introduced [52]. In addition, LPE deposition of Si and Ge LPE does not provide the benefit of stochiometric deposition. The Si-Ge binary phase diagram is shown in Figure 4-9. Si-Ge forms a complete solid solution across the entire composition range, unlike the III-V semiconductors which have stochiometric compounds. In addition, the metallic solution is a constituent element of the deposited III-V semiconductor (i.e. Ga solution for GaAs LPE), whereas for SiGe, the metallic solution will incorporate into the epilayer as a dopant, with a concentration equivalent to its solubility in the crystal at the growth temperature, as shown in Figure 4-10.

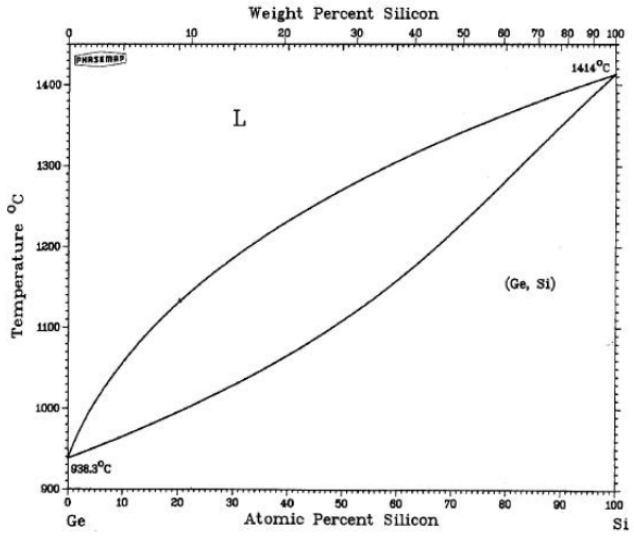


Figure 4-9. Si-Ge binary phase diagram [151].

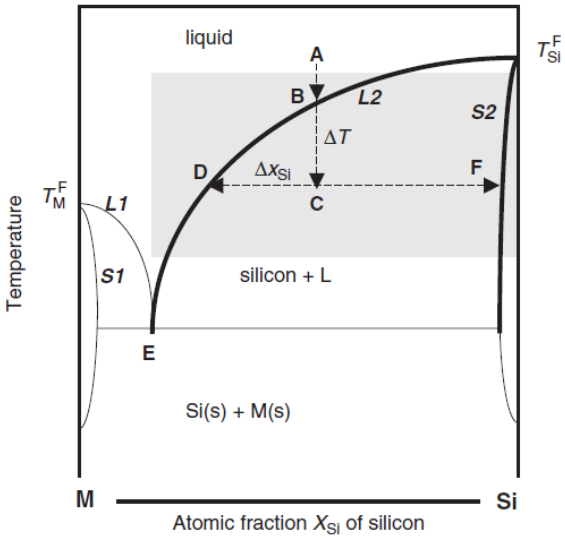


Figure 4-10. Typical Si-Metal phase diagram [52].

As result, there was no interest in SiGe LPE until the end of the 1980's, when interest in high quality and low cost SiGe epilayers on Si substrates for solar cell applications developed. The early leaders in this field were the researchers at the Max-Plank-Institut fur Festkorperforschung in Stuttgart, Germany.

In 1987, Alonso and Bauser first reported SiGe growth on Si by LPE. They successfully grew smooth SiGe layers from an In solvent with Ge contents up to 75 at. % on Si (111) substrates. Their work provided the initial thermodynamic information required for composition control in addition to some basic growth parameters. Composition control is determined by two parameters: the saturation temperature T_{sat} and the germanium content in the solution x_{Ge}. T_{sat} is defined as the isotherm at which the solution is saturated with Si and Ge. For a given T_{sat}, the ratio of mole fractions of Ge (x_{Ge}) and Si (x_{Si}) can vary, as shown in Figure 4-11a. At a given T_{sat}, the Ge content in the deposited thin film (x) increases as x_{Ge} increases, as shown in Figure 4-11b. The composition of SiGe epilayers for different x_{Ge} and T_{sat} is shown in Figure 4-11c. It is observed that the Ge content can also be controlled by varying T_{sat} for a given x_{Ge}. As T_{sat} is lowered, the Ge content in the solid increases due to the lower solubility of Si in the solvent.

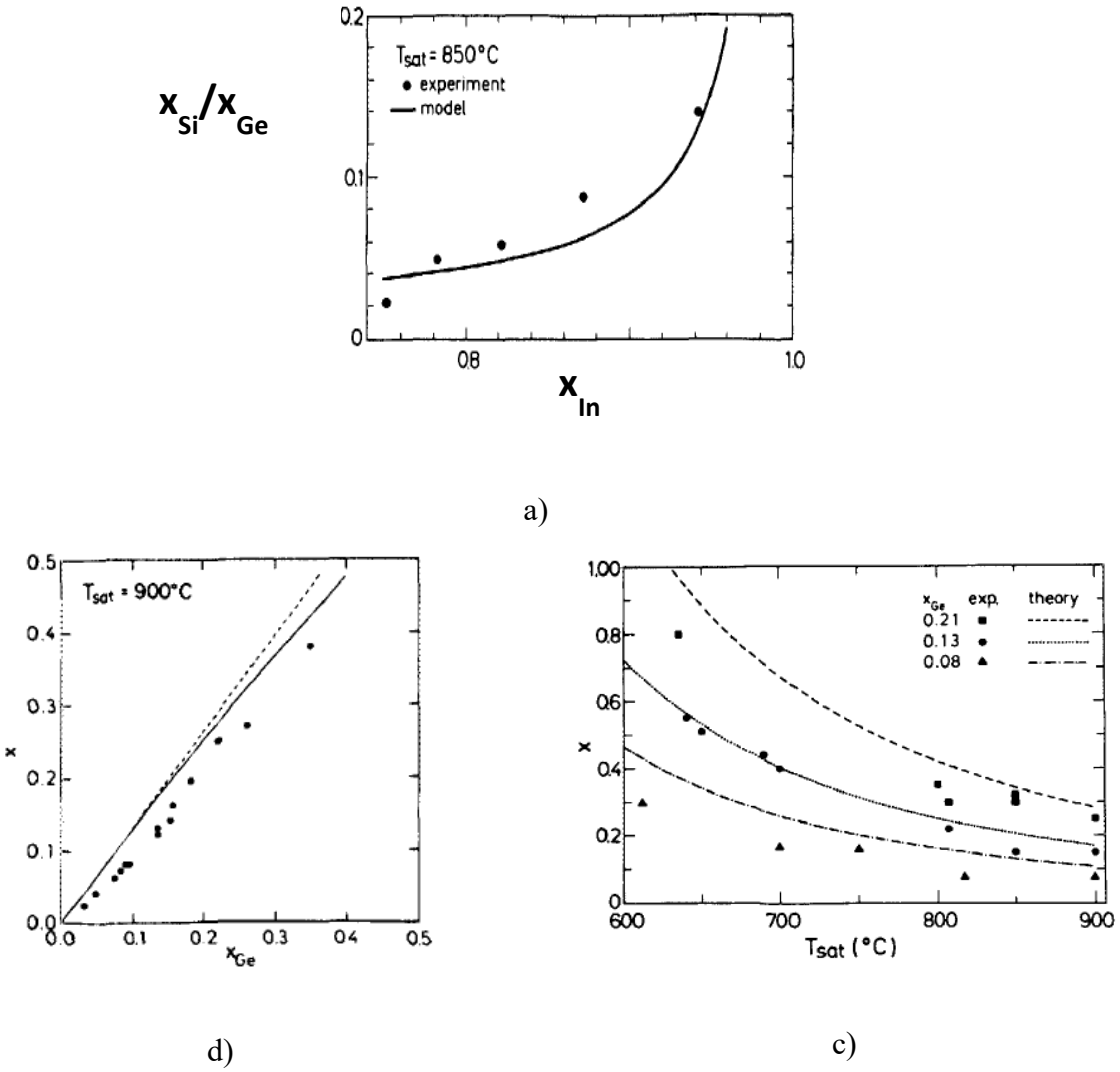
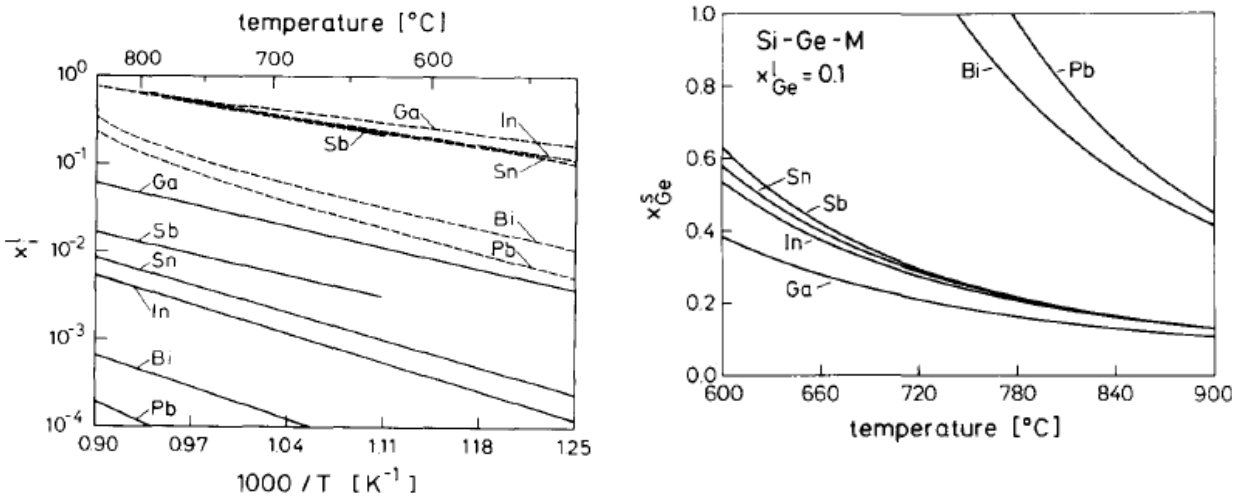


Figure 4-11. Thermodynamic treatment of the Si-Ge-In system by Alonso and Bauser [125]. a) Liquidus compositions of the isotherm T_{sat} of the ratio of Si to Ge in solution to the mole fraction of Indium in the solution. b) Solidus composition x as a function of the Ge mol fraction in the solution (x_{Ge}) at a saturation temperature of 900°C. c) Solidus composition x ($Si_{1-x}Ge_x$) as a function of the liquidus temperature T_{sat} for different Ge mole fractions x_{Ge} in the solution.

In 1990, Trah published an important paper on SiGe LPE growth [115]. Trah calculated the solubility of Si and Ge in various metallic solvents (Figure 4-12a) and their effect on the final composition (Figure 4-12b). To deposit high Ge content thin films, the Ge solubility must be greater than the Si solubility in the solvent at a given temperature. Following the solubility criteria; In, Ga, Sb, Sn, Bi and Pb were identified as potential solvents for SiGe LPE growth (Figure 4-12a). The solubility of Si in Bi and Pb is lower than the solubility of Si in the other identified solvents,

by at least an order of magnitude, which allows SiGe thin film deposition with the Ge content approaching 1 (Figure 4-12b). Trah selected Bi as the ideal solvent for high Ge content SiGe LPE growth. The composition of thin films deposited from a Bi solution were in good agreement with the predicted Ge content (+/- 3 at. %.).



a) b)

Figure 4-12. a) Solubility of Si (solid line) and Ge (dashed line) in various metallic solvents. b) Ge content in the deposited crystal (x^s_{Ge}) as a function of the saturation temperature from a growth solution containing 10 at.% Ge for various metallic solvents [115].

Shortly following Trah's publication, Hansson *et al.* published the first detailed characterization of SiGe LPE films [152]. They deposited high germanium content (at. % Ge > 70 %) thin films from a Bi solution on Si (111) substrates. The composition and strain were calculated by XRD characterization of the symmetric (111) and asymmetric (511) reflections. In addition, the areal dislocation density (N) was determined from the full width at half maximum of the XRD peak ($\Delta\omega$), where b is the Burgers vector.

$$N = \left(\frac{\Delta\omega}{4b}\right)^2$$

Equation 4-1

A dislocation density of $3x10^7$ cm^{-2} was calculated for a film with 68 at. % Ge and a lattice strain of 2.7×10^{-2}. The dislocation density was confirmed by etch pit density measurements using the Billig etch.

Optical characterization of the SiGe thin films showed that the measured photoluminescence line widths (5-8 meV) were the smallest reported for SiGe epitaxial films deposited by LPE or VPE [153, 154], and comparable to bulk crystals grown by the Czochralski method [155]. Electrical characterization of the resistivity and Hall mobility determined that the SiGe layers were *n*-type, due to the incorporation of Bi atoms from the growth solution. The carrier concentration was approximately equal to the solubility of Bi in SiGe at the growth temperatures (approximately 10^{16} cm^{-3}). The room temperature Hall mobility (maximum 3.4×10^2 cm^2/V s) was approximately 50% of the experimentally determined mobility of polycrystalline SiGe and 20% of the mobility of single crystal SiGe. The dislocation density was identified as the primary reason for the reduction in Hall mobility.

Concurrently, Sukegawa *et al.* developed a novel LPE technique, the Yo-Yo solute feeding method, to deposit thick SiGe films on Si substrates [156-158]. The Yo-Yo technique is illustrated in Figure 4-13. A Sn-Ge-Si solution is placed between two Si wafers; the lower wafer is called the source, and the upper wafer the substrate. Initially, the system is heated below the source wafer which increases the solubility of Si in the solution and causes the dissolution of the source wafer. Given that the specific gravity of the solute is less than the metallic solvent, the density of the solution is reduced at the interface with the source wafer. The Si rich solution (i.e. lower density) is transported to the upper substrate wafer by convection. The solution is then saturated at the substrate interface. The temperature of the solution is then lowered and the solute is deposited on the substrate wafer. By cycling the temperature of the solution, alternating feeding and growth cycles allow the growth of thick SiGe films of constant composition. This is not easily achieved by conventional LPE given the finite volume of the growth solution.

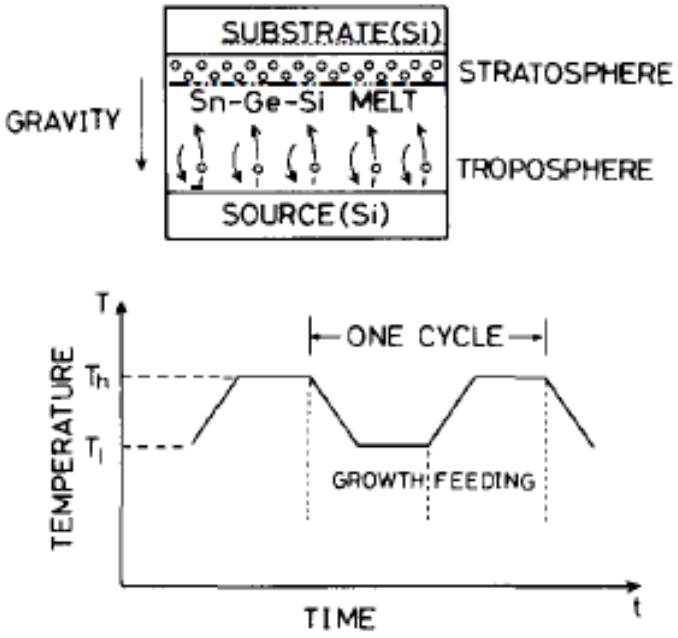


Figure 4-13. Schematic of the Yo-Yo solute feeding method by Sukegawa et al. [31].

4.5. Morphology of SiGe LPE films

The reports by Alonso and Bauser, and Trah provided the thermodynamic and processing conditions required for compositional control of SiGe epitaxial growth. However, both papers reported surface roughness and varying growth morphologies. Alonso and Bauser observed that the growth morphology was dependant on T_{sat} and x_{Ge} [125]. They determined that smooth layers could be grown up to a critical germanium content at a given T_{sat}, which increases as T_{sat} decreases. In addition, for a given composition, there is an optimum growth temperature interval for which smooth layers can be deposited, so long as they are thinner than their critical thickness and the germanium content is less than 75 at. %. Growth at temperatures above the optimum interval resulted in three-dimensional growth.

Trah observed differences in the growth morphology when growing high Ge content films on Si (111) and Si (001) substrates [115]. Growth on Si (111) substrates resulted in a terraced morphology due to the slight misorientation of the substrate. Growth on Si (001) substrates did not have a terraced morphology and showed significant surface roughness. The substrate dependant

morphology was illustrated by growing SiGe films with 98 at.% Ge from a Bi solution onto Si substrates that had been partially masked with an oxide. Square holes were opened in the oxide mask. The substrate dependant growth morphologies are shown in Figure 4-14. The SiGe crystals are faceted by {111} planes, since they are the morphologically stable slow growth planes [159]. The Si (111) morphology shows flat islands faceted by {111} faces (Figure 4-14a) whereas the Si (001) substrate shows pyramidal islands (Figure 4-14b).

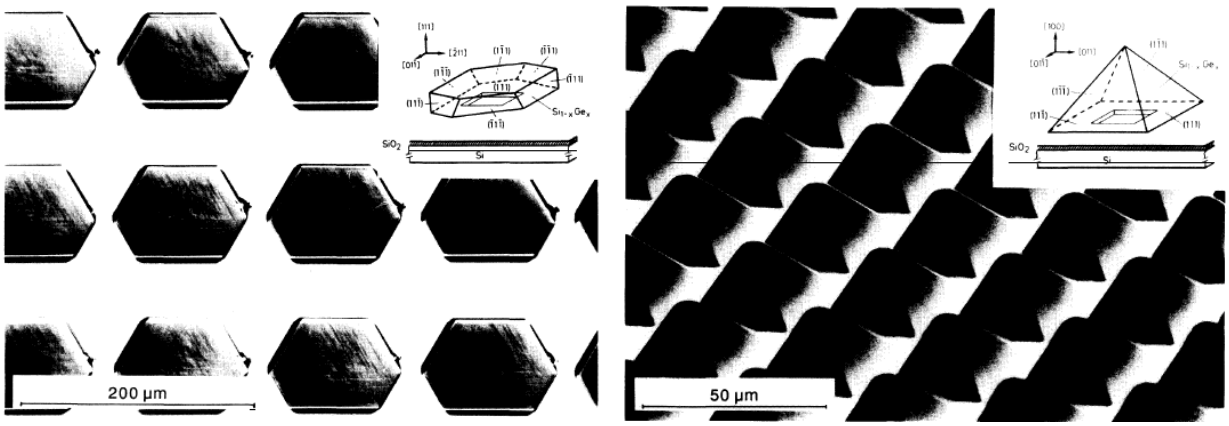


Figure 4-14. Growth morphology of $Si_{0.03}Ge_{0.97}$ deposited on masked Si substrates by LPE a) Si (111) substrate and b) Si (001) substrate [115].

4.6.SK growth mode of SiGe and the self assembly of strain induced islands

The equilibrium growth mode can be determined by considering the surface free energies of the substrate γ_s, the epitaxial layer γ_e and the interface γ_i, as determined by Bauer [160]. Two dimensional Frank-van der Merwe (FM) growth [161] occurs if the sum of the epitaxial layer surface free energy and the interface energy is less than the substrate surface free energy:

$$\gamma_e + \gamma_i \leq \gamma_s$$

Equation 4-2

If Equation 4-2 does not hold, then 3D Volmer-Weber (VW) growth will occur. Qualitatively, FM growth occurs when the interfacial energy is high and the solution wets the substrate and VW growth occurs when the interfacial energy is low and the solution does not wet the substrate.

The Stranski-Krastanov (SK) growth mode is an intermediate between FM and VW growth modes and occurs when the interfacial energy and strain energy are high, such as SiGe deposition by LPE if the lattice misfit is greater than 2 % [128]. Marée modified Bauer's equation to account for the lattice misfit by adding the misfit strain energy, σ [162].

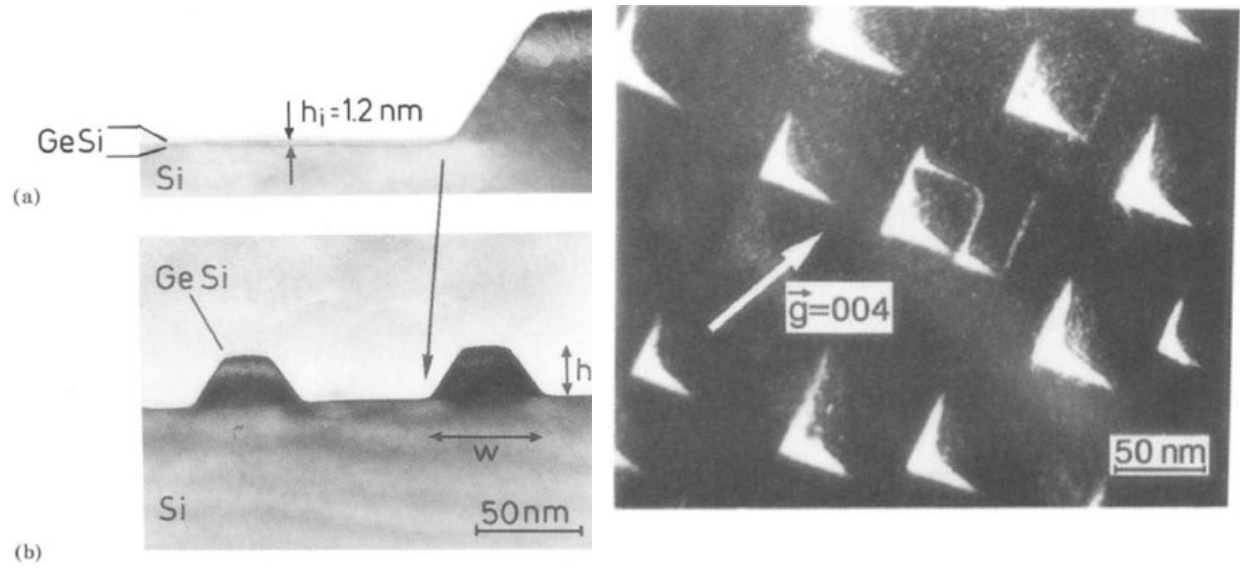
$$\gamma_e + \gamma_i + \sigma \leq \gamma_s$$

Equation 4-3

The high interfacial energy allows for initial FM 2D layer-by-layer growth. As the layer thickness increases, the stain energy in the epitaxial layer increases until Equation 4-3 no longer holds and the growth mode transitions to VM 3D island growth.

SK growth accommodates the elastic strain in the initial 3D growth stages which allows pseudomorphic growth beyond the theoretical critical thickness [163]. However, misfit dislocations are ultimately required to fully relieve the misfit strain. Since the islands are very short, 90° dislocations can be nucleated at the edge of an island and climb to the heteroepitaxial interface [15]. However, after the islands coalesce, the edge dislocations can no longer climb to the interface and 60° dislocations are nucleated to relieve the remaining strain.

In a series of papers [116, 164], Hansson *et al.* investigated the early growth stages of high Ge content SiGe thin films on Si (001) substrates. In the first paper [164], the early growth stages were observed by using very short growth times (approximately 1 s) and negligible undercooling. They termed this growth technique as "equilibrium growth." A continuous $Si_{0.15}Ge_{0.85}$ thin film with a thickness of 1.2 nm was observed on the surface of the substrate in addition to randomly distributed truncated pyramid islands, as shown in Figure 4-15a. The islands were formed by {111} facets and aligned in the <110> directions. The 2D to 3D transition thickness of 1.2 nm corresponds to 8 monolayers. These results confirm that the epilayers grew in the SK growth mode. Misfit dislocation nucleation occurred within the pyramidal islands which were taller than 30 nm [164] as shown in Figure 4-15b. This thickness is an order of magnitude greater than the critical thickness predicted by Matthews' mechanical equilibrium theory [21]. The increase in pseudomorphic layer thickness is attributed to the strain reduction from the islands and a kinetic barrier to dislocation nucleation [164].



a) b)

Figure 4-15. TEM micrograph of a $Ge_{0.85}Si_{0.15}$ layer deposited on a Si(100) substrate. Growth time of 1.5 s at 800C from a 0.2 K supercooled Bi-Ge-Si growth solution [164]. a) Cross-section showing a 1.2 nm 2D SiGe layer and 3D pyramids. b) Weak-beam dark-field plan view of SiGe islands. A single misfit dislocation is observed in the middle.

Hansson *et al.* developed a novel LPE technique, "interfacial energy epitaxy" (IEE), to further investigate the early growth stages of high Ge content SiGe thin films on Si (001) substrates [116]. IEE utilizes the reduction of the interfacial free energy between the growth solution and the substrate as the driving force for crystal growth, even in conditions of under saturation. The energy balance for LPE crystal growth is:

$$\Delta G = \Delta\gamma_{int} + \Delta\mu$$

Equation 4-4

Where ΔG is the difference in Gibbs free energy of the system, $\Delta\gamma_{int}$ is the difference in interfacial free energy and $\Delta\mu$ is the thermally induced chemical potential. As discussed above, LPE crystal growth is driven by the thermally induced chemical potential ($\Delta\mu < 0$). Hansson *et al.* demonstrated that under small undersaturation ($\Delta\mu > 0$), crystal growth can be driven by the reduction of the interfacial free energy if it is greater than the undersaturation ($\Delta\gamma_{int} > \Delta\mu$). IEE growth is closer to thermodynamic equilibrium and provides very slow growth rates or 2 monolayers/s, which allows

precise thickness control. No misfit dislocations were observed in islands up to 100 nm in thickness, which are three times thicker than previously reported [164]. This indicates that the growth morphology is dependent on the driving force and distance from equilibrium.

Dorsch *et al.* provide a rigorous description of the nucleation and growth of the SK growth mode in high Ge content SiGe by IEE [24]. The first stage of growth is the deposition of 4 monolayers, layer-by-layer, driven by the reduction of the interfacial free energy. Following the initial growth, the solution no longer interacts with the interface and the driving force for epitaxial growth is reduced. However, the lattice mismatch between $Si_{0.15}G_{0.85}$ and the substrate is 3.5%. As the initial monolayers are deposited, the strain energy in the thin film increases. Epitaxial growth stops when the reduction in interfacial free energy and the increase in strain energy are equal:

$$\Delta\gamma_{int} + \Delta\sigma = 0$$

Equation 4-5

Further epitaxial growth is then driven by the reduction of the strain energy by island formation. Islands nucleate on the 2D pseudomorphic film and grow laterally as new monolayers are nucleated on top. This continues until the islands are faceted by {115} planes. Lateral growth of the islands is terminated and further growth is driven by the reduction of the surface energy of the islands towards lower energy {111} faceted islands. Schade *et al.* [165] determined the variation in composition of Ge in SiGe islands along the vertical <100> direction by electron energy loss spectroscopy (EELS). The Ge composition showed a sharp change in composition and gradient at 1/3 of the island height, which corresponds to the observed transition from {115} to {111} faceted islands. In a subsequent publication, Dorsch *et al.* showed that the width of the islands is inversely proportional to the lattice mismatch (i.e. Ge content) and is not dependent on the growth temperature or growth rate [166].

Following the works of Hansson and Dorsch, a divide is created in SiGe LPE literature. Two main avenues of research are established. The first investigates the growth and self-assembly of SiGe islands on Si substrates. The second investigates the planar growth of SiGe on Si and minimization of defects for solar cell applications. A summary of the research to date on island growth by LPE is provided below. The reader is referred to the recent and comprehensive review by Aqua *et al.*,

Growth and Self-Organisation of SiGe nanostructures [167], on the current state of SiGe island growth and assembly research for all epitaxy techniques.

Island growth of SiGe on Si offers some interesting applications as self-assembled quantum wells. Quantum wells can be created by lithographic techniques, but the critical thickness of high misfit systems is not suitable for such techniques [168]. Self-assembly by SK growth is an attractive technique for the formation of defect free, epitaxial quantum wells. Control of the island morphology, size, ordering and aerial density is necessary for device engineering.

Schimdbauer *et al*. [168] observed that island ordering varied with island density. At low island densities (approximately 1 island per μm^2) the islands are randomly distributed, however, local clusters showed some alignment in the <100> direction. As the island density was increased, the ordering of the islands increased also. Medium density islands showed preferential alignment in the <100> direction and high density islands were arranged in a square lattice with strong alignment in the <110> and lesser alignment in the <100> directions. Hanke *et al.* [169, 170] showed that the increase in ordering with island density is the result of preferential nucleation sites from the strain induced wetting layer depression [171, 172] surrounding an island. The strain field decays quicker in the <100> directions than the <110> directions, which *su*ggests the preferred nucleation direction, though they were unable to show that the strain distribution created low energy sites for island nucleation. Induced near-island nucleation along the elastically soft <100> direction was demonstrated by Monte-Carlo simulations [173].

It was also shown that as the growth conditions moved further from thermodynamic equilibrium the island size and formation moves away from the equilibrium {111} faceted islands. Hanke *et al.* [147] applied a high cooling rate of 10K/min to promote non-equilibrium growth. The resulting islands were smaller, by more than a factor of 2, than islands grown near-equilibrium. In addition, the islands showed only local interactions during self-assembly, with less long range order.

4.7. Planar SiGe LPE growth and misfit strain relaxation

Planar growth of SiGe can be divided into two streams, low misfit systems ((f < 1%) and high misfit systems (f > 1.5%). Each system exhibits unique strain relaxation mechanisms as discussed below.

4.7.1. Strain relaxation in high misfit systems

Following the early SiGe LPE work of Alonso, Trah and Hansson, Chen *et al.[174]* investigated the dislocation morphology of relaxed, high Ge content SiGe epilayers. High Ge content films (80 – 100 at. % Ge) with corresponding lattice mismatches of 3.3% to 4% were deposited on Si (111) substrates from a Bi solution. Multiple defects were observed, including misfit and threading dislocations, microtwins and stacking faults. The dislocations were characterised by TEM using the two-beam condition for Burgers vector analysis. It was determined that a significant fraction of threading dislocations did not lie in the primary slip system and could not have been formed by the half-loop nucleation mechanism. They observed threading dislocation-free cells within the film and postulated that these cells correspond to the formation of 3D islands during the early stages of SK growth. As the islands grow and coalesce, Chen *et al.* proposed that the misfit dislocations will thread into the epitaxial film at the interface of two islands, as shown in Figure 4-16. A dislocation spacing of approximately 50 nm in the cell walls is an order larger than the predicted spacing of 5 nm, which suggests that a significant portion of threading dislocations terminate at nodes near the heteroepitaxial interface, further reducing the threading dislocation density at the surface.

The threading dislocation density decreased with decreasing cooling rate and initial supersaturation. At 0°C initial supersaturation and a cooling rate of 20°C/h, a threading dislocation density of 1.5×10^8 cm^{-2} was observed. At 3°C initial supersaturation and a cooling rate of 30°C/h, a threading dislocation density of 5.0×10^8 cm^{-2} was observed. It is difficult to determine the individual impact of supersaturation and cooling rate from the results. However, both parameters increase the driving force for epitaxial growth which will increase the nucleation rate of islands and threading dislocations, according to the proposed model. It should be noted that threading dislocation densities lower than 10^6 cm^{-2} in relaxed SiGe are required for integration with III-V optical devices [41].

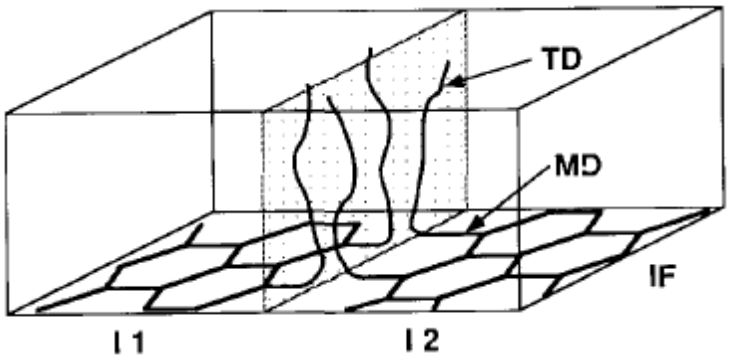


Figure 4-16. Threading dislocation model proposed by Chen [174].

Albrecht *et al.* [16] observed the nucleation of misfit dislocations within pyramidal islands ($Si_{0.14}Ge_{0.86}$), confirming the work of Hansson *et al.* [164], and identified the dislocations as 90° edge dislocations lying in the secondary {110}<110> slip system. Due to the large strain energy, the secondary slip system is activated and the dislocations glide to the heteroepitaxial interface. Using the models described by Matthews [19, 175] they calculated that at high misfit strain (f > 3%), the critical thickness is lower for the {110}<110> slip system then the primary {111}<110> slip system [176]. As the misfit strain is relieved by dislocation nucleation, the secondary slip system is deactivated.

Füller *et al. [25]* demonstrated that the misfit strain relaxation mechanism is dependent on the substrate orientation. The surface free energy of Si and Ge {001} and {111} faces are provided in Table 4-1. The surface energy of {111} faces is lower than {001} faces, which indicates that {001} faces are unstable and which promotes the {111} faceted pyramid growth on Si (001) substrates.

Table 4-1. Surface energies for {111} and {100} faces of relaxed Si and Ge, and strained Ge [177].

		{100}		{111}	
	Lattice constant	eV/atom	J/m^2	eV/atom	J/m^2
Si	a_{Si}	1.97	2.14	1.1	1.38
Ge	a_{Ge}	1.57	1.57	0.98	1.13
	a_{Si}	1.57	1.70	0.98	1.23

As a result of the lower surface energy, Si (111) substrates are better suited for planar growth of high Ge content SiGe films by LPE [178]. Pseudomorphic growth on Si (111) occurs by the lateral propagation of monoatomic steps. The step growth mode allows for strain relaxation at the free edge of the step. As successive pseudomorphic layers are nucleated, misfit dislocations are nucleated at the step edges, which is the first area to exceed the critical thickness. The TEM micrograph of a $Si_{0.6}Ge_{0.4}$ epilayer on a Si (111) substrate (Figure 4-17) shows the laterally propagating step edges. Hexagonal dislocation networks are visible at the step edges, which indicates that they are nucleated at the edge of a step and glide into the epilayer [25]. Ernst *et al.* determined that misfit dislocations in $Si_{0.15}Ge_{0.85}$ on Si (111) form hexagonal networks of 90° partial dislocations, which cannot be formed by the half-loop nucleation model [179, 180].

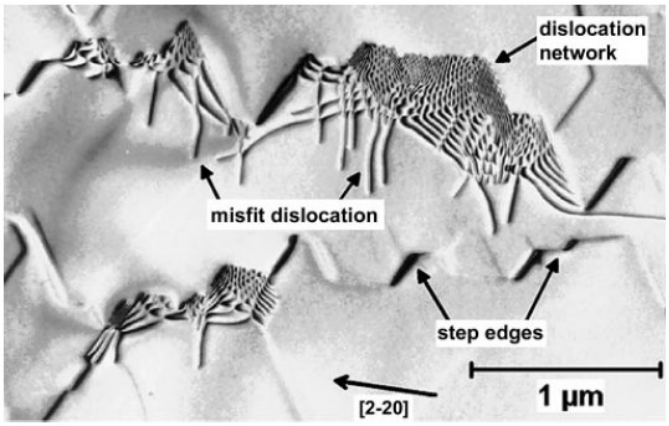


Figure 4-17. Plan-view TEM micrograph of $Si_{0.6}Ge_{0.4}$ epilayer on a Si (111) substrates[25]. Hexagonal misfit dislocation networks are visible at the step edges.

4.7.2. Strain relaxation in low misfit systems

Low misfit systems ($f < 2\%$) on Si (001) substrates do not grow in the SK growth mode and are known to have surface undulations or crosshatch morphology, as discussed in Section Crosshatch Morphology2.3. This section outlines the growth parameters for the growth of high-quality and smooth SiGe epilayers by LPE.

The rough surface of the crosshatch morphology is undesirable for the deposition of multilayers and for photolithographic techniques. However, the nucleation of dislocations and the resulting crosshatch morphology is necessary to relax the misfit strain. Crosshatch morphology is

characterized by two parameters: the wavelength of undulations (λ) and the root mean square (RMS) value of roughness (Rq). Sembian *et al.* demonstrated that relaxed and smooth SiGe films could be deposited by increasing λ [181-183]. As discussed above, the ridges in the crosshatch morphology are formed from the increased deposition rate in the relaxed portion of the film above a misfit dislocation. Thus, to increase λ, the distance between misfit dislocations must be increased, that is, to decrease the misfit dislocation density. Sembian *et al.* demonstrated that the dislocation density can be reduced by decreasing the Ge content in the epitaxial layer, as shown in Figure 4-18 [181]. This is a trivial result, as reducing the Ge content reduces the misfit strain, which is the root cause of dislocation nucleation and the crosshatch morphology. More importantly, they showed that λ can be increased by decreasing the cooling rate [181, 182]. Figure 4-19 shows the variation of λ and the etch pit density as a function of the cooling rate for $Si_{0.976}Ge_{0.034}$ epitaxial layers on Si (100) substrates. The etch pit density, a measure of the threading dislocation density, increases as λ decreases which indicates that the crosshatch morphology is a result of the nucleation of dislocations.

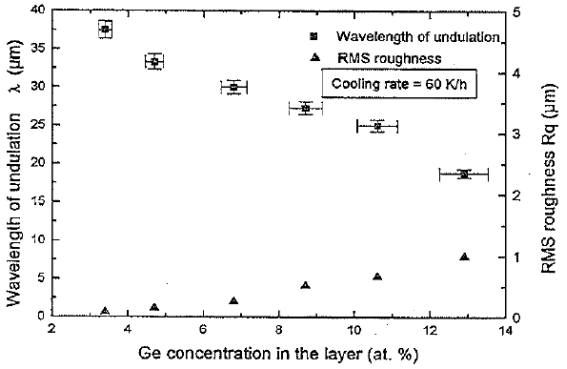


Figure 4-18. Variation of the wavelength of undulation (λ) and RMS roughness (Rq) with Ge concentration in the epitaxial film on Si(100) [181].

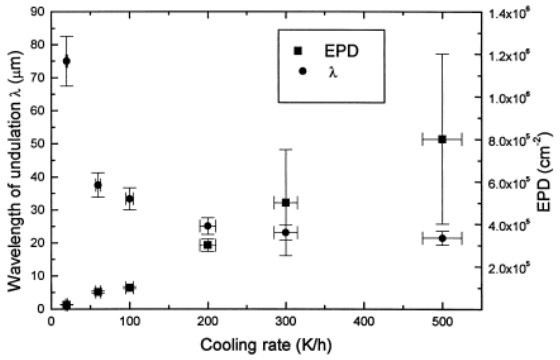


Figure 4-19. Variation of the wavelength of undulation (λ) and etch pit density with the cooling rate in $Si_{0.976}Ge_{0.034}$ film on Si(100) [182].

The increase in dislocation nucleation with increasing cooling rate is explained from kinetics. As the cooling rate is increased, the driving force and deposition rate increase. In addition, the surface mobility of the adatoms decreases with increasing cooling rate [182]. This combination may lead to local accumulations in the epitaxial layer, which locally increases the misfit strain, and promotes dislocation nucleation. The etch pit density increased from $2x10^4$ to $8x10^5$ cm^{-2} as the cooling rate was increased from 20 to 500 K/h, respectively, for $Si_{0.976}Ge_{0.034}$. In addition, the etch pit density

increased from $8x10^4$ to $7x10^6$ as the Ge content increased from 3.4 to 12.9 at. %, respectively. Smooth, relaxed, SiGe epitaxial layers were grown using low cooling rates with Ge contents up to 13 at. %, above which the growth mode transitioned to island growth [181].

Gutjahr *et al.* [126] demonstrated that smooth layers up to 27 at. % could be deposited using graded buffers. As discussed above, the solubility of Si in LPE metallic solvents is an order of magnitude lower than the solubility of Ge (Figure 4-12b). In LPE growth from a finite solution, the Si is depleted quicker than Ge, thus the composition will vary through the thickness as shown in Figure 4-20 which facilitates the deposition of graded buffers. Gutjahr demonstrated that the threading dislocation density in $Si_{0.9}Ge_{0.1}$ epilayers is two orders of magnitude lower if a graded buffer is grown compared to an epilayer of the same composition grown directly on a Si substrate ($5x10^7$ to $7x10^5$ cm^{-2}) [126]. They also showed that the graded buffer profile could be varied by the cooling rate (Figure 4-20) given the differences in the diffusion coefficients of Si and Ge. However, they did not observe a change in threading dislocation density between epilayers with different cooling rates.

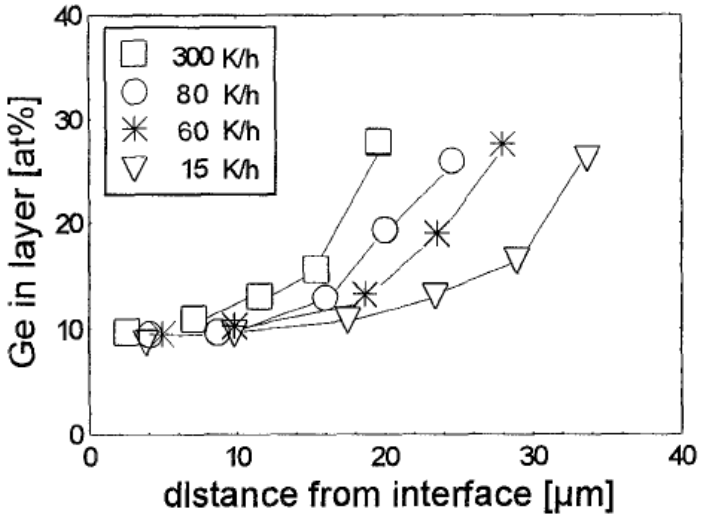


Figure 4-20. Variation of Ge content in SiGe epilayer grown at 950°C from an $In_{0.9}Ge_{0.08}Si_{0.02}$ growth solution [126].

Chapter 5

Lateral Liquid-Phase Epitaxy

This chapter will describe the design and functioning of the LLPE furnace and the LLPE growth technique. The important experimental conditions and improvements of the process will be discussed.

5.1. Lateral Growth Proposal

The lateral growth of lattice mismatched layers is a potential solution to grow high quality semiconductor films with low threading dislocation densities. The growth of high quality Ge nanowires on amorphous [60]and lattice mismatched Si substrates [61] has been reported previously using a guided vapour-liquid-solid growth. The growth of a lattice mismatched Ge nanowire on Si showed that the misfit dislocations were confined to the heteroepitaxial interface and did not thread to the surface of the nanowire. Lateral growth has the potential to deposit thin, high-quality, lattice mismatched films over a large area by confining the misfit dislocations to the heteroepitaxial interface.

Fitzgerald *et al.* proposed that there are two main criteria for the growth of strain-relaxed, low-defect density, graded $Si_{1-x}Ge_x$ buffers [48, 184]; the dislocation nucleation rate must be minimised while the dislocation glide must be maximised. If these criteria are met, dislocations that nucleate in the initial SiGe film can glide in the second layer and fully relax the layer without nucleating more misfit dislocations; this process can be repeated with successive films each with slightly increasing Ge content.

These two criteria were applied to a novel lateral liquid-phase epitaxy (LPE) growth technique, lateral LPE (LLPE), which can deposit a SiGe epilayer with reduced threading dislocation density in a single step. Dislocation nucleation and glide are governed in part by the strain energy in the epilayer originating from the lattice misfit. As a pseudomorphic epilayer is grown, the strain energy increases until a critical thickness is reached at which point it is energetically favourable to nucleate misfit dislocations to relieve the strain energy. There are different nucleation sources for misfit dislocations, with corresponding activation energies, and thus, different critical thicknesses. If a threading dislocation is present at the substrate surface prior to heteroepitaxial deposition, the dislocation will thread through the growing epilayer. When the epilayer reaches the critical thickness for dislocation glide (h_G), the threading dislocation can glide along the heteroepitaxial interface and create a misfit dislocation. This is the lowest energy source for the nucleation of a misfit dislocation[23]. If the film cannot completely relax via the glide of threading dislocations inherited from the substrate, the nucleation of new dislocations will occur by the half-loop nucleation and multiplication mechanisms when the critical thickness for dislocation nucleation (h_N) is exceeded. These mechanisms have higher activation energies than that for dislocation glide, thus h_N is expected to be greater than h_G.

The difference in activation energies for the misfit dislocation formation can be exploited to promote dislocation glide and minimize the threading dislocation density. The proposed lateral growth mechanism is shown schematically in Figure 5-1. A strained epilayer is grown on a Si (001) substrate and a misfit dislocation is nucleated (Figure 5-1a). The left side of the misfit dislocation threads to the surface, whereas the right side of the misfit dislocation ends along the interface at the free edge of the epilayer. As the epilayer is grown horizontally in the [110] direction, the misfit dislocation which terminates along the interface at a free edge of the epilayer (Figure 5-1a), can propagate laterally, as shown in Figure 5-1c. If the thickness of the laterally grown epilayer is greater than the critical thickness for dislocation nucleation h_N and nucleation is favorable, the epilayer will be relaxed by dislocation nucleation and glide which is characterized by misfit dislocations extending along the substrate/film interface (Figure 5-1b). This will result in the creation of new threading dislocations. On the other hand, if the thickness of the epilayer is kept below h_N but above the critical thickness for dislocation glide (h_G) (where the nucleation of dislocations is unfavorable), the misfit strain in the epilayer will be relieved largely by the glide of existing misfit dislocations (Figure 5-1c). Under these conditions of inhibited dislocation

nucleation, no new threading dislocations are introduced to the epilayer, yet the misfit strain is still relieved with a network of parallel misfit dislocation lying in the growth direction and results in partially relaxed films with very low threading dislocation density.

An additional benefit of a parallel misfit dislocation network is the prevention of dislocation pile-up. Misfit dislocations and crosshatch ridges and trenches in the $[1\bar{1}0]$ direction act as barriers to dislocation glide in the [110] direction and are sources of dislocation pile-up [11, 49, 185], which increases the threading dislocation density. The absence of misfit dislocations in the $[1\bar{1}0]$ direction, allows the [110] misfit dislocations to glide and form long misfit dislocations with low threading dislocation density.

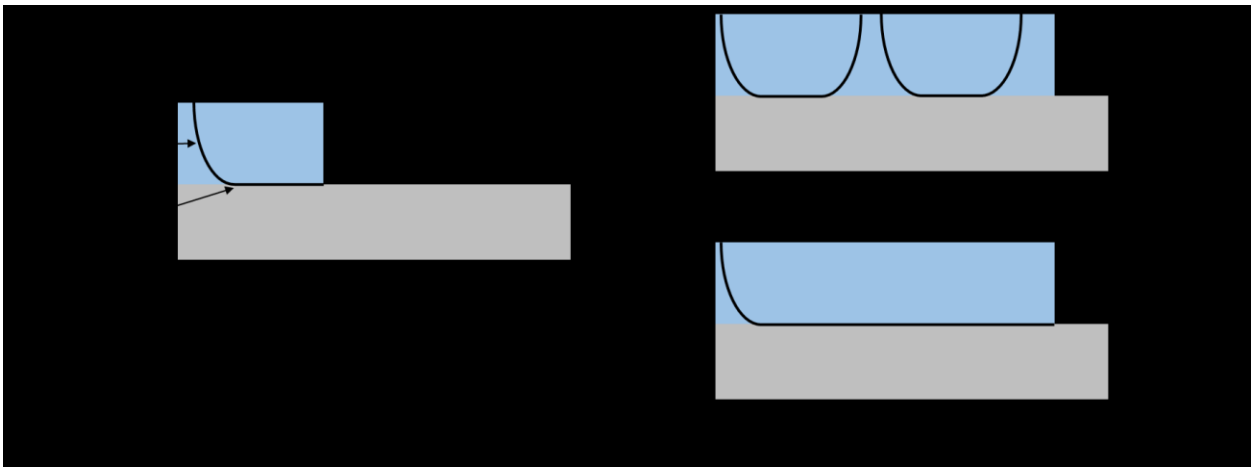


Figure 5-1. Schematic of dislocation propagation in LLPE growth. a) A dislocation with a misfit and threading segment is nucleated in a SiGe epilayer. b) If the film thickness is greater than h_N a combination of dislocation glide and nucleation is used to relieve the misfit strain as the epilayer is propagated laterally. c) If the film thickness is below h_N, but above h_G, the misfit strain is relieved by the glide of the misfit dislocation.

5.2. Fabrication of the LLPE Furnace

LLPE film growth was performed in a custom designed and constructed liquid-phase epitaxy furnace (Figure 5-2) which was supplied with a high purity gas supply from a custom-built manifold (Figure 5-3). The primary components are identified on the pictures and listed here:

1. Cylindrical Watlow ceramic fiber heaters Furnace Controller.
2. Watlow Ez-Zone controller
3. Furnace mounted wheels and rails for lateral travel.
4. Furnace stepper motor.
5. Quartz tube.
6. Quartz-to-metal seals.
7. Fan to cool the quartz-to-metal seals
8. Custom bellows.
9. Slider stepper motor
10. Trap to remove volatised metallic impurities from the gas exhaust.
11. Gas exhaust and isolation valve
12. Hydrogen Micro-Torr gas purifier.
13. Nitrogen Micro-Torr gas purifier.
14. MKS M100B mass flow controller.
15. PURA in-line hygrometer
16. K-type thermocouple.
17. Thermocouple reader.
18. Isolation valve.
19. Leak detection port.

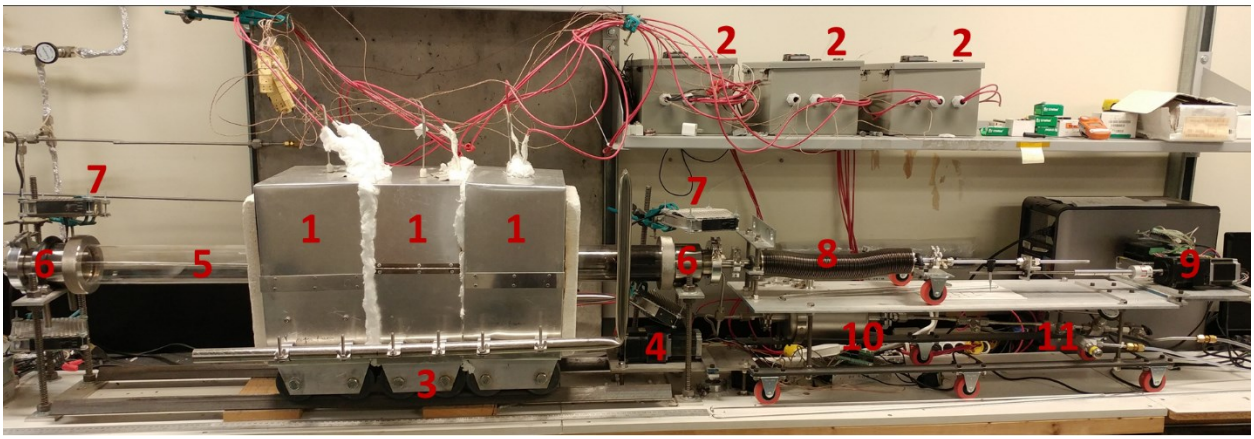


Figure 5-2. Picture of the LLPE furnace.

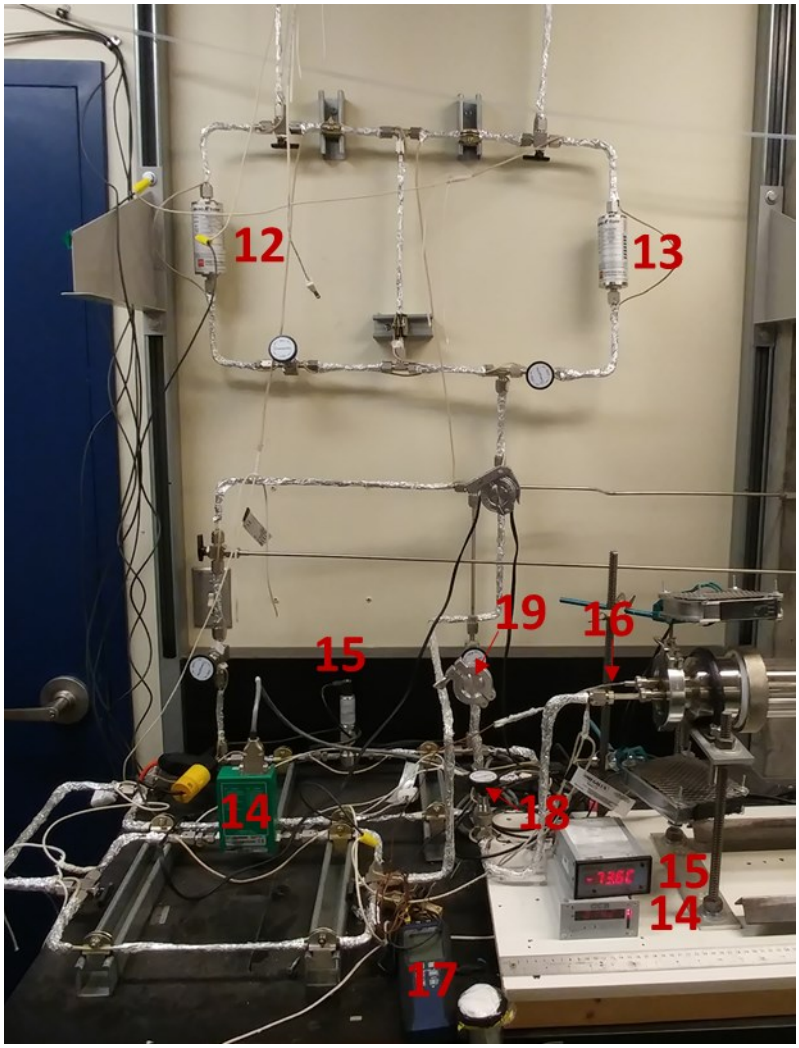


Figure 5-3. Gas manifold for LLPE furnace

The crystal growth was housed in a custom graphite boat, which will be discussed in detail in the following section. The graphite boat was contained in a quartz tube which was sealed at either end with custom quartz-to-metal compression seals, as shown in Figure 5-4. High purity gas (N_2 or H_2) was flowed through the quartz tube at all times to maintain a clean environment for crystal growth. When the furnace was in operation, high purity H_2 (99.999%) was flowed to maintain a reducing environment to remove any oxide that may regrow during the loading of the furnace.

When the furnace is not in operation the gas is switched to, high purity N_2 gas, from a liquid N_2 for cost and safety concerns. To help minimize the presence of oxygen and moisture in the furnace, the gas is filtered through Micro-Torr gas purifiers from SAES Pure Gas Inc., and the moisture is monitored with an in-line PURA hygrometer from Michell Instruments. The gas flow is controlled by an MKS M100B mass flow controller from CCR.

A three-zone furnace was assembled from three cylindrical Watlow ceramic fiber heaters (120V, 900 W), each controlled by a Watlow Ez-Zone controller. The independent control of the furnaces enabled the establishment of a temperature gradient across the furnace. The furnaces were mounted on rails and coupled to a stepper motor via a ball-screw. This allowed for slow and precise movement of the furnaces which, combined with the established temperature profile, allowed to cool the graphite boat at a controlled rate and provide the driving force for crystal growth.

A second stepper motor was coupled to the graphite slider with a hooked quartz push-rod. Lateral motion of the push-rod was permitted with the use of custom designed bellows. The slider stepper motor controlled the movement of the graphite slider, which allowed for LLPE growth.

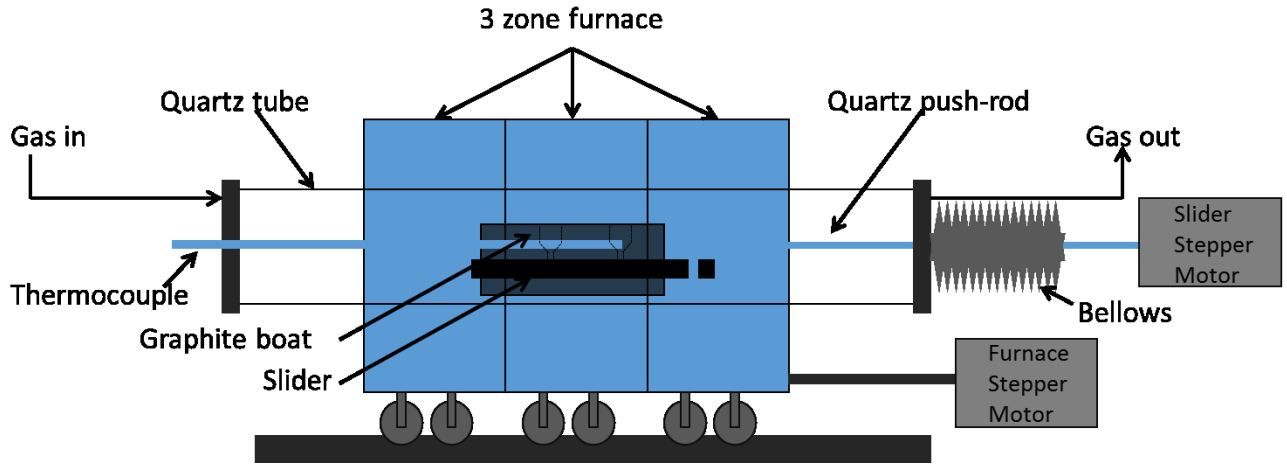


Figure 5-4. Schematic of the LLPE system.

5.3.Graphite Boat Design

The graphite boat was designed to accommodate both traditional LPE growth as well as LLPE growth. The boat design consisted of 5 components that were machined from high quality Sigraform HLM graphite from SGL Group: the well-block, the slider, the holder, the lid and the inserts (Figure 5-5). Detailed drawings of the assembly are provided in Appendix B.

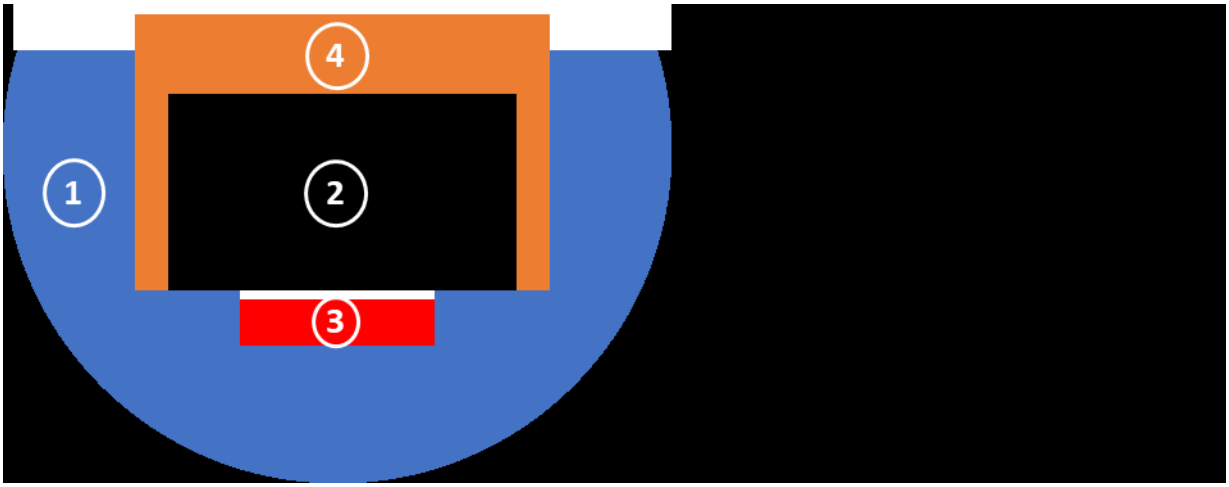


Figure 5-5. Side view schematic of the graphite boat pieces.

The graphite well-block was designed to hold the liquid metal solution. Detailed drawings for the well-block are provided in Appendix B. The well-block contained three sets of wells (Figure 5-6). The first set of wells were designed to house graphite inserts which enabled variations in well-openings of 2, 3 or 4 mm. The second set of wells were designed to house molybdenum inserts which could further reduce the opening to 0.1 mm. The third set of wells were rectangular for traditional LPE growth. The separation between two identical wells was the same for each of the three well types, such that the two identical wells could be used simultaneously during a given growth experiment.

Two thermocouple bores were drilled into the well-block to monitor the temperature of the wells. The bores terminated at the wells for graphite holders, one at each of the identical wells. Two additional bores were added to secure the well-block to the holder and lid.

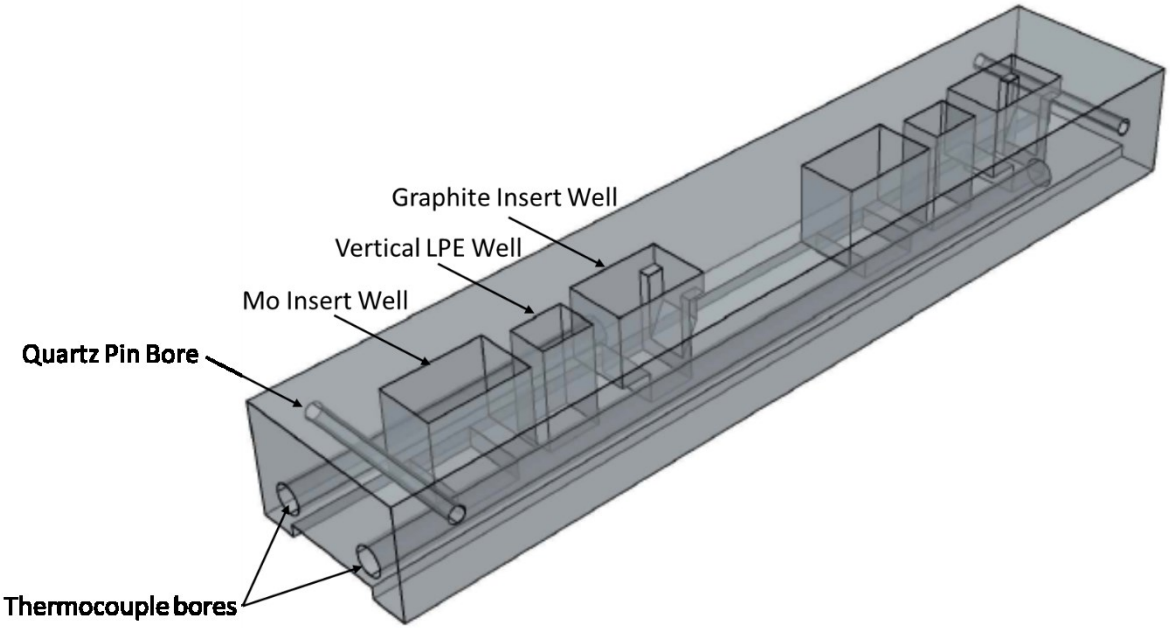


Figure 5-6. Isometric view of the graphite well-block.

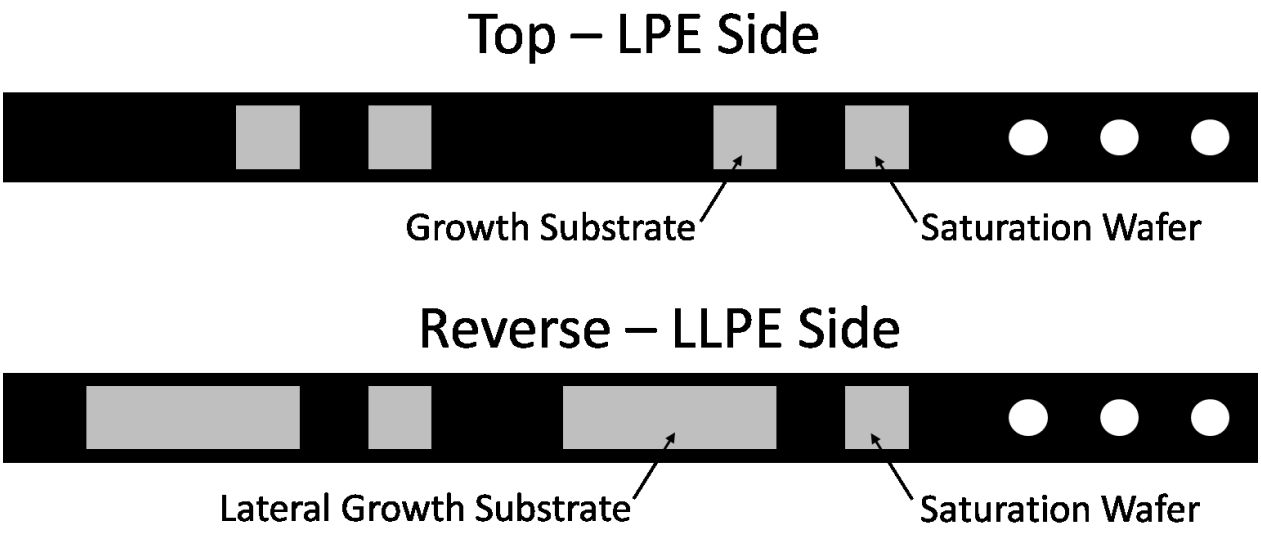


Figure 5-7. Schematic of the graphite slider. Top side was used for traditional vertical LPE growth. The reverse side had a longer growth substrate slot for LLPE growth.

The graphite slider was designed to hold the growth and saturation wafers for LPE and LLPE growth (Figure 5-7). The detailed drawings for the slider are given in Appendix B. The top side of the slider has four slots for Si wafers, two for saturation and two for growth wafers. The slots were spaced to allow for two growths using the LPE wells in a single experiment. Each slot could hold a wafer that is 12 mm x 12 mm. The reverse side of the slider has two slots for saturation wafers

(12 mm x 12 mm) and two long slots for lateral growth wafers (12 mm x 30 mm). The depth of the slots is 500 µm to allow for a 500 µm Si wafer to lie flush with top of the slider. Three holes were drilled into the leading edge of the slider to allow coupling with the quartz slider. Each hole allows access to a different set of wells.

The graphite holder was machined from a cylinder of diameter 5.56 cm, out of which was machined slots for the well-block, slider and lid. The assembly is held together with two quartz dowels. The slot for the well-block is designed to sit above the slider with a gap of 20 µm to help minimize solution carry-over.

5.4. Experimental Conditions

Prior to growth, the metallic solution was homogenised to prevent the Ge and Si powders from floating on the surface of the metallic solution and agglomerating. The wells of the graphite boat were loaded with high purity In shot and powder, followed by Ge powder. The shot and powder were all 99.999% pure and were supplied by Super Conductor Materials Inc. The concentration of Ge (X_{Ge}) in the solution can be varied to control the Ge concentration in the epilayer [115, 125]. The solution was not saturated with Si during the homogenisation step. The solution was then placed in the LPE furnace under H_2 atmosphere and heated to 1000 ˚C for two hours.

Si (001) ± 0.1˚ prime grade wafers were used as the growth and saturation wafers. The wafers were cleaned before growth. Organic impurities were removed with a self-heating piranha solution (1:1 = H_2SO_4:H_2O_2) for fifteen minutes. Metallic impurities were then removed with an acid etch (1:1:6 = HCl:H_2O_2: H_2O) heated to 80°C for fifteen minutes.

The Si (001) wafers were cleaved into growth and homogenisation substrates. The sacrificial homogenisation substrates were cut into 12 mm x 12 mm squares. The growth substrates were cut either into 12 mm x 12 mm squares or long 30 mm x 12 mm rectangles. The substrates were dipped in a 10:1= H_2O:HF solution for thirty seconds to remove the native oxide layer and then immediately placed on the graphite slider and the appropriate wells were loaded with a pre-homogenised growth solution. The graphite boat was then placed immediately in the furnace to prevent re-growth of the native oxide layer.

Once the boat was sealed in the furnace, the quartz tubbed was pumped to 100 millitorr, with the use of a turbo pump, and purged with N_2. After four pump and purge cycles, the gas was switched

to high purity H_2 and the temperature was raised above 950 ˚C. The substrates were baked for 2 hours to remove any remaining oxide [146]. The furnaces were then set to the saturation temperature (T_s) and once the temperature stabilized, a sacrificial Si wafer was introduced to the In solution for two hours to saturate the solution with Si.

Following saturation, the sacrificial wafer is removed. Prior to inserting the growth into the solution, the temperature is adjusted to the initial growth temperature, which is either T_S or the solution is undercooled (T_U) (Figure 4-3). In traditional (planar) LPE, the substrate is fully inserted into a square well, and the growth solution covers the entire substrate. The solution is cooled at a constant rate to initiate and continue growth. When the desired cooling interval (ΔT) is reached, the substrate is fully removed from the growth solution to terminate the growth.

For LLPE, a tapered well with an opening width of 3 mm is used to restrict the contact area between the solution and the substrate (Figure 5-8). The substrate is introduced to the solution such that the well is completely covering the leading edge of the growth substrate. The furnace stepper motor was then activated to cool the solution at a constant rate. The slider stepper motor is then activated to pull the substrate through the solution at a constant rate, ranging from 0.1 to 1 mm/min.

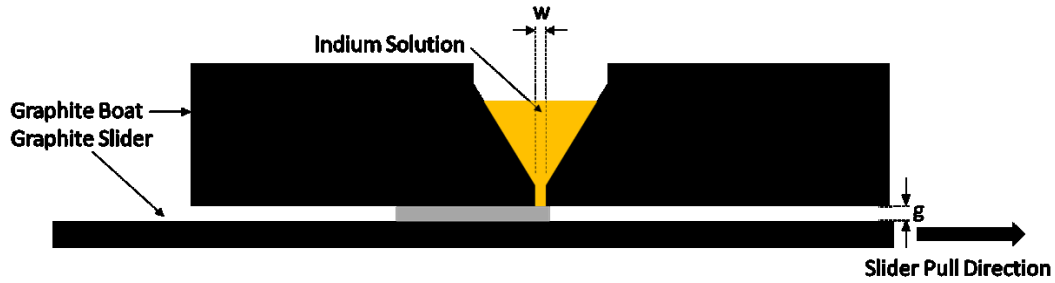


Figure 5-8. Schematic of the custom graphite boat for LLPE.

5.5.Native Oxide Removal

It is essential to remove the Si native oxide layer prior to epitaxial growth since SiGe growth on Si (001) substrates is very sensitive to oxide removal. Failure to remove the oxide layer prevents epitaxial growth whereas the incomplete removal of the oxide layer leads to a masked-growth effect which results in island growth [146]. Figure 5-9 shows the importance of the complete removal of the native oxide layer. The region in the lower half of the micrograph, which is indicated as “Complete oxide removal” shows epitaxial film growth, which indicates that the oxide was completely removed from the interface. The film is characterized by the crosshatch

morphology, above which high Ge content islands nucleated along the <110> directions due to solution carry-over, as discussed in the following section. The is a transition from ordered islands in the <110> directions to disordered islands as the growth moves into the regions marked as "Incomplete oxide removal". The disordered islands grew out of random holes in the oxide layer and indicate that there was an incomplete removal of the native oxide in this region.

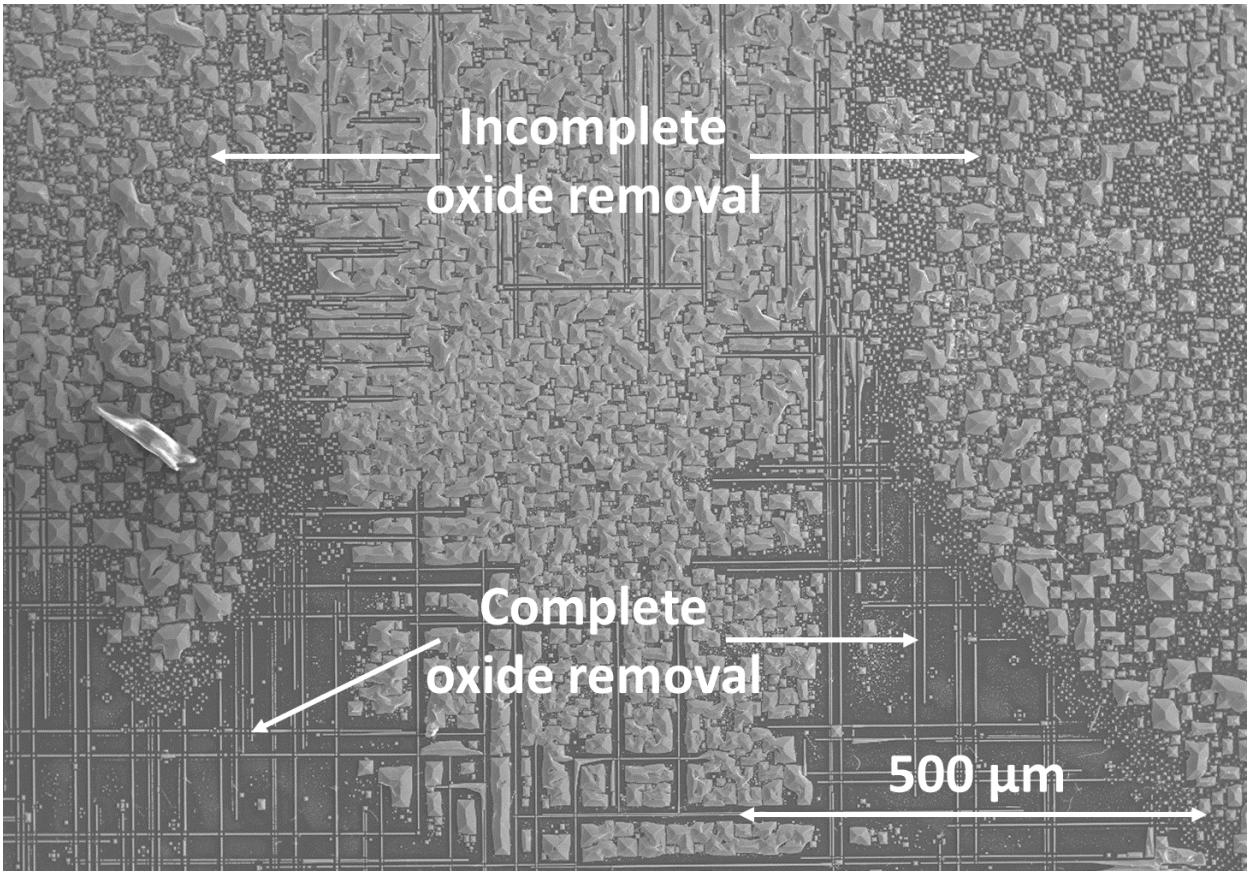


Figure 5-9. SEM micrograph which illustrates the importance of complete removal of the native oxide from the Si substrate surface. Areas where the oxide where the oxide were completely removed show complete film growth and ordered island growth, whereas areas with incomplete removal show random island growth.

Multiple steps were taken to remove the native oxide from the Si substrates. The first step was a wet HF etch, as described above, of the growth and saturation substrates, which removed the oxide layer by the following reaction:

$$SiO_{2(s)} + 6HF_{(l)} \rightarrow H_2SiF_{6(aq)} + H_2O_{(l)}$$

The HF etch provides a Hydrogen-terminated surface which prevents the oxide regrowth for approximately 15 minutes. To prevent oxide-regrowth, the substrates must be loaded into the

graphite boat, along with the metallic solvent, and sealed in the LLPE furnace in an N_2 atmosphere as quickly as possible. A typical load time was under 12 minutes. Given the relatively long time required to place the etched substrates in an inert atmosphere, the risk of oxide regrowth is significant. Initial experiments either did not produce any SiGe growth due to complete oxide coverage of the substrate, or produced disordered island growth. Multiple deoxidation strategies were investigated and implemented to remove any oxide regrowth that occurred during the loading of the furnace and to prevent further regrowth. The successive improvement

The first strategy to produce an oxide free substrate surface was to employ two deoxidation steps to remove any native oxide that regrew during the loading of the furnace. The first, a high temperature bake in a H_2 reducing environment, was used for every growth experiment. The substrates were baked at 1000 ˚C for more than two hours, and the oxide layer was reduced, per the reaction below:

$$SiO_{2(s)} + H_{2(g)} \leftrightarrow SiO_{(v)} + H_2O_{(v)}$$

The second deoxidation step required the addition of 0.4 wt. % Al to the metallic solution. The Al removed the native oxide layer and produce aluminum oxide [145], which floats to the surface of the metallic solution, as per the reaction:

$$4Al_{(l)} + 3SiO_{2(s)} \rightarrow 3Si_{2(l)} + 4Al_2O_{3(s)}$$

The use of Al as a deoxidant was avoided since the addition of Al to the In solvent made the solvent adhere more strongly to the graphite boat, which made it more difficult to remove the solid solvent from the boat after growth. This in turn caused scratches to the graphite, which in turn allowed for greater mechanical adhesion of the solvent to the graphite.

The deoxidation steps improved the film growth, however it was determined that they resulted in an incomplete removal of the native-oxide regrowth. When the graphite boat was loaded into the furnace, the quartz tube had to be opened to the ambient atmosphere which introduced O_2 and moisture into the tube, which contributed to the oxide regrowth. Since it was not feasible to install a load-lock to the system to reduce eliminate the introduction of ambient air into the quartz tube, content of ambient gas was reduced by cyclically pumping the quartz tube to 100 millitorr with a turbo pump and purging with N_2 gas. Four cycles were required to reduce the ambient content in the tube to below 1 ppm, which is lower than the high purity gas content. In addition, the quartz

tube and graphite boat were periodically baked at high temperature (1000 ˚C for more than 2 hours) to help remove any moisture from their surfaces. In addition, the graphite boat was stored within the quartz tube, under a N_2 atmosphere, whenever it was not in use.

Lastly, the it was necessary to further remove O_2 and H_2O from the high purity N_2 and H_2 before they entered the quartz tube. Two solutions were adopted; heaters were attached to the gas to bake the lines periodically and drive off any adhered moisture, and gas filters were installed. The combination steps significantly reduced the moisture content of the high purity gas, as evidenced by the reduction of the dew point from -60˚C to below as -120˚C, which is below the detection limit of the hygrometer. It was observed that epitaxial film growth required an atmosphere with a dew point below -100˚C.

5.6.Solution Carry-Over

Solution carry-over, or entrainment, is a significant problem in LPE growth. It occurs when the liquid growth solution is entrained onto the growth substrate as the substrate is removed from the growth solution. Entrained solution on the growth substrate has a significant impact on the composition and morphology of the final crystal. The first impact of solution carry-over is the continued growth after the removal of the substrate from the well. Since the substrate remains covered in the solution as the furnace is cooled to room temperature, epitaxial growth continues until the supply of solute (Si and Ge) is exhausted. This makes it impossible to study the growth rate and composition of the desired film, since it cannot be determined which part of the film was grown during the controlled deposition phase, and which part was deposited from the entrained solution during the furnace cool down phase. The amount of entrained growth is dependant on the quantity of solution which is entrained, which varies from run to run.

Since Ge has a higher solubility limit than Si, LPE growth at low temperatures favours the growth of high Ge content crystals. Given the large misfit between high-Ge-content SiGe and the low-Ge-content films grown in the controlled deposition phase, as the entrained solution is cooled to room temperature, high-Ge-content islands grow by the SK growth mode overtop of the low-Ge-content film. The islands are aligned in the <110> directions along the crosshatch ridges of the low-Ge-content film. Figure 5-10 demonstrates the impact of solution-carry over. The left side of the

micrograph shows a $Si_{98}Ge_2$ film which is characterized by an orthogonal network of ridges and trenches, the crosshatch morphology. On the right side of the micrograph, bright Si_7Ge_{93} islands are aligned above the crosshatch pattern of the $Si_{98}Ge_2$ film. The island growth on the right side was caused by the entrainment of the growth solution. The boundary between the entrained and non-entrained areas is dramatic as the island growth ends abruptly at edge of the entrained area.

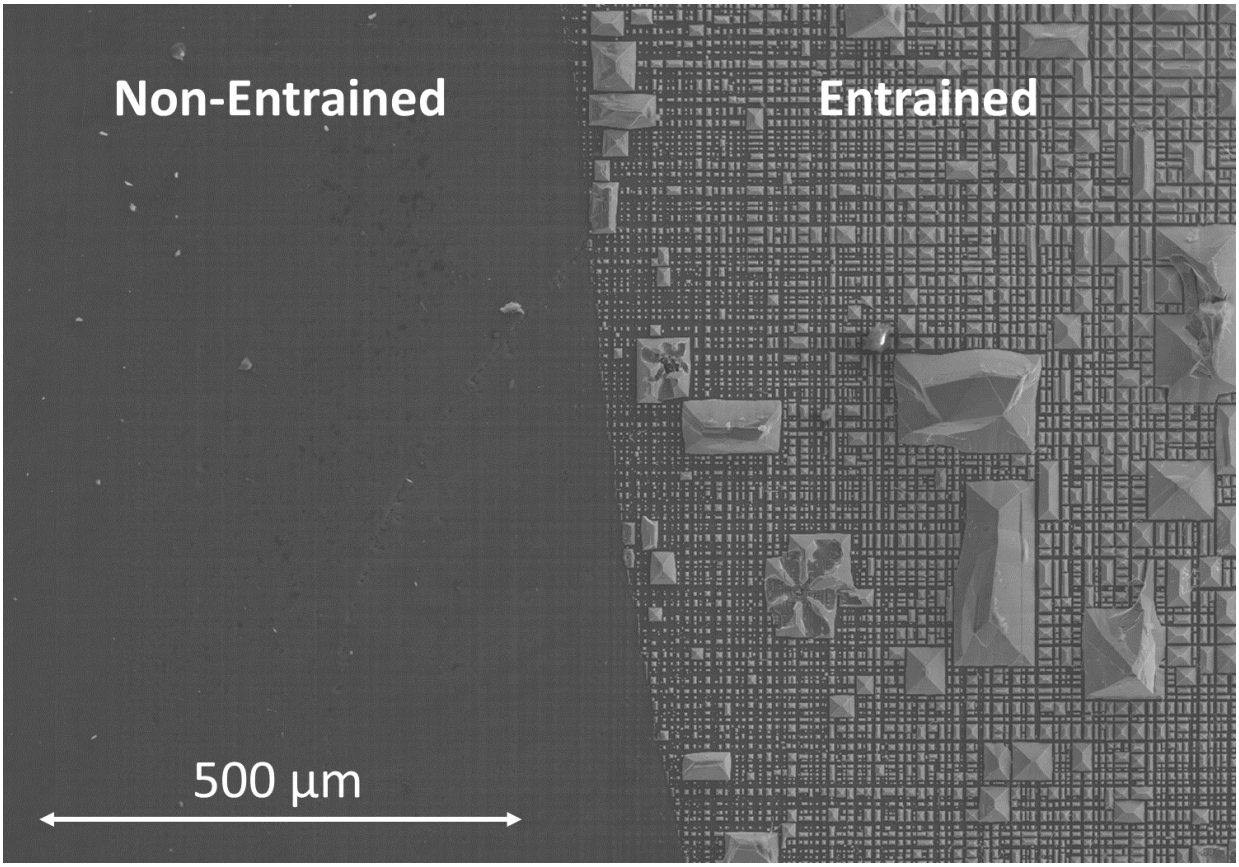


Figure 5-10. SEM micrograph of a $Si_{98}Ge_2$ epilayer grown by LPE which demonstrates the impact of solution carry-over. The left side of the micrograph was not entrained and is characterized by the crosshatch morphology. The right side of the micrograph shows an area in which there was entrainment. Si_7Ge_{93} islands were grown above the epilayer by the entrained solution.

The solution carry-over occurs due to the preference of the growth solution to wet the Si substrate over the graphite and its presence or amount is a function of the gap between the substrate and graphite boat, the height of the growth solution and the pull speed, as discussed in Chapter 4.3. To minimise the solution carry-over the gap between the substrate and the graphite boat was set at 20 µm. To keep the head pressure of the solution as low as possible, the growth solution was limited to 3 g (about 5 mm above the bottom of the graphite well). To terminate the growth, the substrate was pulled out of the solution as fast as possible.

Solution carry-over was particularly problematic for lateral growth for LLPE growth on long growth substrates (3 cm long). The long length of the substrate provided a channel for the growth solution to escape the growth well and flow into an adjacent well where it can reduce its surface free energy by beading to avoid the graphite surface, as shown in Figure 5-11. This prevents consistent lateral growth since the contact time between the growth solution and the substrate cannot be controlled. A redesign of the graphite boat is required to reduce the problem of the solution carry-over. This redesign would require a tighter gap between the solution and the substrate as well as the elimination of the additional wells such that the long growth substrate remains covered by graphite at all times, before and after growth.

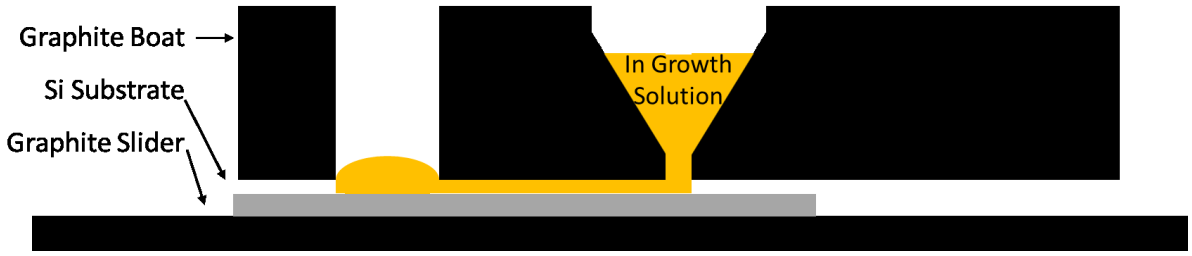


Figure 5-11. Schematic of the graphite boat for LLPE growth which demonstrates the issue of the solution short-cutting to an adjacent well causing solution carry-over.

Chapter 6

Characterization Techniques

The characterization techniques used in this thesis are summarised in the chapter. The author was responsible for the operation of each instrument and the analysis of the results. The following techniques were used to asses four criteria of the epilayers grown by LLPE; composition was determined by X-ray diffraction (XRD) and energy dispersive spectroscopy (EDS) with the scanning electron microscope (SEM), strain was determined by XRD, film thickness was determined by cross section imaging in the SEM and pit depth analysis with the atomic force microscopy, the threading dislocation density was determined by etch pit density (EPD) measurements with the SEM.

6.1.X-Ray Diffraction

X-ray diffraction XRD was the primary technique used to characterise the strain and composition of the SiGe epilayers grown by LLPE. All XRD measurements were performed on a Brucker D8 at École Polytechnique. The following section describes the theory of the collection and analysis of the XRD data to determine the composition and strain of SiGe epilayers on Si (001) substrates.

X-ray waves are elastically scattered by the atoms in a crystal lattice. If the path difference of two scattered waves on two neighbouring crystal planes is equal to $2d\sin\Theta$, then the waves will constructively interfere, as shown schematically in Figure 6-1. The condition for constructive interference is known as Bragg's law:

$$2d \sin\theta = n\lambda$$

Equation 6-1

Where *d* is the spacing between planes, Θ is the angle of incidence of the wave, λ is the wavelength of the X-rays and *n* is the order of the reflection. Thus, for a known wavelength and angle of incidence, the lattice spacing of the crystal can be determined. However, in lattice misfit systems, the lattice constant of the epilayer will conform to the lattice constant of the substrate, if no misfit dislocations are nucleated (Figure 2-1b). The lattice constants of the epilayer are then different from the bulk lattice constant. If the composition of the epilayer is known, the strain in the epilayer can be calculated from the experimentally determined lattice spacing, or the composition can be calculated if the sample is assumed to be fully relaxed [115]. If neither the composition nor the strain are known, the epilayer cannot be characterised by simply applying Bragg's Law.

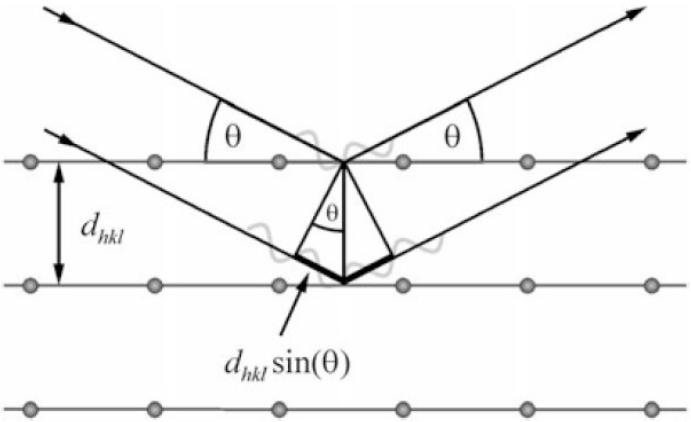


Figure 6-1. Constructive interference condition of the diffraction of two rays on neighbouring planes [186].

The construction of a reciprocal space map (RSM) by triple-axis diffraction can provide a complete characterization of the strain and composition of the epilayer. A crystal lattice can be defined by three vectors, a_1, a_2 and a_3, the corresponding reciprocal lattice is defined by the vectors b_1, b_2 and b_3 , where:

$$b_1 = \frac{1}{V}(a_2 \times a_3)$$

Equation 6-2

$$b_2 = \frac{1}{V}(a_3 \times a_1)$$

Equation 6-3

$$b_3 = \frac{1}{V}(a_1 \times a_2)$$

Equation 6-4

and V is the volume of the unit cell [187]. b_1, b_2 and b_3 are normal to the (100), (010) and (001) planes, respectively, and their lengths are equal to the reciprocal spacing of the respective planes. The reciprocal lattice is shown in Figure 6-2, where the lattice points indicate a crystallographic plane which has a corresponding reciprocal lattice vector G_{hkl} (Equation 6-5), which points from the origin (000) to the lattice point [186].

$$G_{HKL} = hb_1 + kb_2 + lb_3$$

Equation 6-5

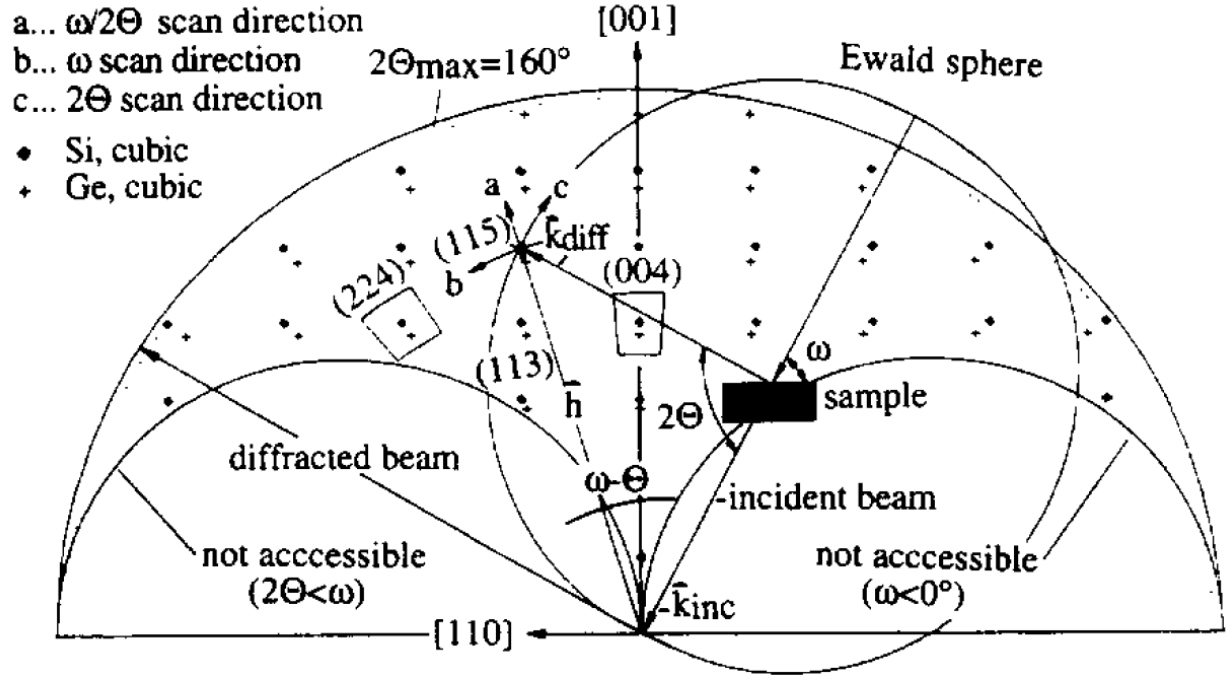


Figure 6-2. Reciprocal space map of the Bragg reflections accessible for an incident X-ray with a wave vector of length k_0 [186].

The *von Laue* condition (Equation 6-6) provides the conditions for constructive interference in the reciprocal lattice, where k_{inc} is the wave vector of the incident wave and k_{diff} is the wave vector of the diffracted wave:

$$(k_{inc} - k_{diff}) = G$$

Equation 6-6

Since the waves are elastically scattered, the magnitude of the incident and diffracted wave vectors are equal.

The Ewald construction represents the conditions for constructive interference. As shown in Figure 6-2, the incident wave vector, k_0, is drawn such that the tip of the vector points to the origin. The diffracted wave vector, k, is drawn beginning at the centre of the sphere defined by k_0. Any lattice points that lie on the surface of the sphere satisfy the *von Laue* condition. For example, in Figure 6-2, k-k_0=ΔK is equal to the lattice vector of the (004) plane (G_{004}) [186].

A triple-axis diffractometer is required for high resolution scans in reciprocal space. The triple-axis refers to the three rotation axes of the setup: the Bragg angle of the monochromator crystal, the sample and of the analyzer crystal. The important scan directions in triple-axis diffraction are illustrated in Figure 6-3a. The components of the diffracted vector ΔK are [188]:

$$q_{\parallel} = k(\cos\alpha_f - \cos\alpha_i)$$

Equation 6-7

$$q_{\perp} = k(\sin\alpha_f + \sin\alpha_i)$$

Equation 6-8

Where α_i is the angle of incidence with respect to the surface of the sample, which is typically described by the goniometer angle (ω), and α_f is the angle of the diffracted beam with respect to the sample surface such that

$$2\theta = \alpha_i + \alpha_f$$

Equation 6-9

In this way, α_i and α_f can be measured by scanning ω and 2Θ [186].

The strain in the epilayer can be determined from reciprocal space maps, as shown in Figure 6-4. The vertical axis represents the [001] reciprocal lattice vector ($k_\perp$) , which is proportional to the out-of-plane lattice constant ($a_\perp$) by Equation 6-10. The horizontal axis represents the [110] reciprocal lattice vector ($k_\parallel$), which is proportional to the in-plane lattice constant ($a_\parallel$). The symmetrical (004) reciprocal lattice point (RLP) of a relaxed Si substrate (Si^r in Figure 6-4) lies on the vertical [001] axis. A fully relaxed Ge epilayer has a larger lattice constant than Si, thus the Ge^r (004) RLP lies below Si. A pseudomorphic Ge epilayer on Si has a larger out-of-plane lattice constant than relaxed Ge, thus the Ge^p (004) lies below Ge^r. The strain relaxation path between Ge^p and Ge^r is shown by the arrow connecting the two RLPs. Since all of the (004) RLPs lie on the vertical axis, only $a_\perp$can be determined from an (004) RSM. If the composition of the epilayer is known, then the strain of the epilayer can be determined from an (004) RSM. However, since $a_\perp$and $a_\parallel$ are not equal in a strained epilayer, the asymmetric (224) RSM must be collected to fully characterize the composition and strain of the epilayer.

The relaxed Si^r and Ge^r RLPs both lie on the [224] reciprocal lattice vector since their Bragg planes are parallel [186], as shown on the left side of Figure 6-4. A fully strained pseudomorphic layer will have the same lateral component of the scattering vector ($k_\parallel$) as the substrate because the epilayer lattice constant parallel to the interface ($a_\perp$) is equal to the substrate lattice constant (a_s). The strained epilayer RLP lies directly below the substrate RLP, as seen in Figure 6-4, where the Ge^p (224) lies below Si^r (224). Relaxation path between Ge^p and Ge^r is shown by the arrow between the two RLPS.

$$a_\perp = \frac{4}{k_\perp}$$

Equation 6-10

$$a_\parallel = \frac{2\sqrt{2}}{k_\parallel}$$

Equation 6-11

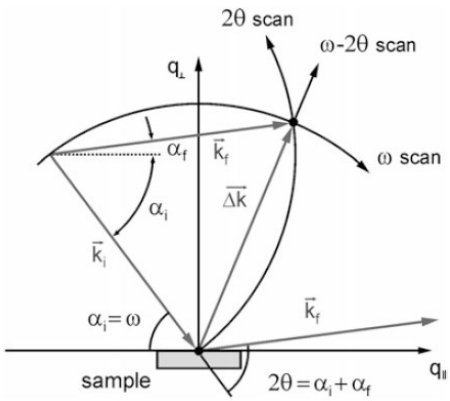


Figure 6-3. Scan directions in reciprocal space [186]

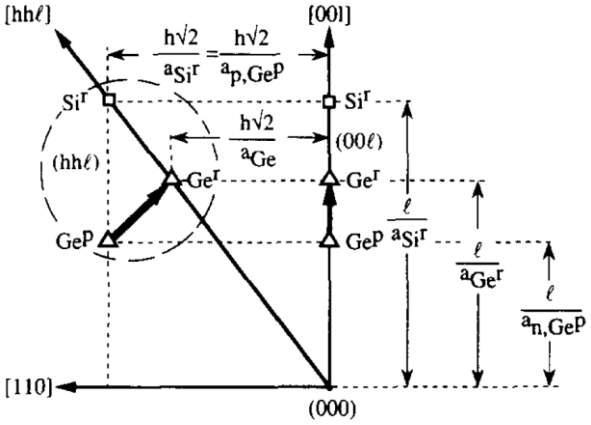


Figure 6-4. Reciprocal space of SiGe [189]

If the composition of the epilayer is not known (i.e. the reciprocal-lattice points of the strained and unstrained layers is not known), the derivation of Leitz and Bulsara [190], adapted from the works of van der Sluis [191] and of Matney and Goorsky [192], provides compositional and strain results from symmetric (004) and asymmetric (224) RSM. The components of the scattered wave vector for the glancing incident (224) scan are given by:

$$k_{/\!/} = \frac{2}{\lambda}\sin\left(\theta_{B,224} + \Delta\theta_{224}\right) \cdot \cos\left(\frac{\pi}{2} - \left(\varphi - \Delta\omega_{224} + \Delta\omega_{004}\right)\right)$$

Equation 6-12

$$k_{\perp} = \frac{2}{\lambda}\sin\left(\theta_{B,224} + \Delta\theta_{224}\right) \cdot \sin\left(\frac{\pi}{2} - \left(\varphi - \Delta\omega_{224} + \Delta\omega_{004}\right)\right)$$

Equation 6-13

Where $\Theta_{B,224}$ is the Bragg angle of the substrate and $\Delta\Theta_{224}$ is the angular difference between the substrate and film peak. $\Delta\omega_{224}$ and $\Delta\omega_{004}$ are the angular difference between the substrate and film peaks. Lastly, φ represents the angle between the (224) and (004) planes (φ=35.264°).

From the calculated components of the wave vectors, the lattice constants of the epilayer can be determined:

$$a_r = \frac{(-a_\perp - (\nu \cdot a_\parallel)}{-1 - \nu}$$

Equation 6-14

Where a_r is the lattice of a fully relaxed film of the measured composition. The determination of the lattice constants, the composition, misfit and % relaxation of the epilayer can be calculated:

$$composition = \frac{a_\parallel - a_r}{a_r}$$

Equation 6-15

$$misfit = \frac{a_s - a_r}{a_r}$$

Equation 6-16

$$\%relaxation = \left(1 - \frac{|strain|}{|misfit|}\right) \times 100$$

Equation 6-17

In this way, RSM obtained by high resolution, triple-axis diffraction provides quantitative information on the composition and strain of SiGe epilayers on Si substrates [193-195]. In addition, the full width at half maximum of the peaks provide information on the crystal quality and defect density [196-198].

6.2.Scanning Electron Microscopy

Scanning electron microscopy (SEM) was the primary imaging technique used to qualify the SiGe film growth as well as complementary technique to XRD for compositional analysis by energy dispersive spectroscopy (EDS). SEM imaging was performed on a Hitachi SU-3500 SEM. All micrographs in the thesis were imaged with an accelerating voltage of 20 keV and a working distance of 10 mm, which are the required conditions for EDS analysis.

The primary consideration for SEM imaging for this thesis is to resolve the crosshatch morphology, which provides the density and symmetry of the misfit dislocation network. The crosshatch pattern can be resolved by the selection of the appropriate imaging mode. Three imaging modes were available on the Hitachi SU-3500 and each mode provides different

information. Secondary electron (SE) imaging is the most common SEM imaging technique. SE are low-energy electrons which are ejected the imaged material by incoming, high-energy beam electrons. The SE are collected are attracted by a magnetic field and are collected by an Everhart-Thornley detector, which is mounted on the side of the SEM chamber. The intensity of the SE micrograph represents the number of electrons collected at each pixel. The number of SE generated in each area is dependant on the topography and the elemental composition. As a result, an SE micrograph provides both topographical and compositional information. A SE micrograph of a SiGe epilayer with a crosshatch morphology is shown in Figure 6-5a. The crosshatch morphology is a network of ridges and troughs which can be seen in the SE micrograph, though it is difficult to resolve individual ridges. In the top right corner of the micrograph is a ridge of high-Ge content islands which appear lighter due to the increased topography and Ge content.

Backscattered electron (BSE) imaging allow to decouple the compositional and topographical effects. BSE are high-energy beam electrons which have undergone sufficient elastic scattering events to escape back through the film surface. BSEs are collected by an annular ring detector mounted around the electron beam at the top of the SEM chamber. The number of BSE generated by a material increases with increased atomic number (Z) [199]. This allows for compositional imaging, where low atomic number elements appear dark due to low backscattering, and high atomic number elements appear bright. This behaviour can be observed in Figure 6-5b, where the high-Ge content islands appear bright white compared to the low-Ge content crosshatch film. The crosshatch morphology us slightly visible due to the slight variations in composition across the crosshatch pattern. However, it is more difficult to resolve the crosshatch pattern in BSE composition mode than by SE imaging.

The most effective mode to resolve the crosshatch morphology is the BSE topography mode. The BSE detector is divided into four quadrants, by subtracting the signal from opposing quadrants, as opposed to summing the signal in compositional mode, the topography of the surface is revealed due to the high take-off angle of the BSE. The micrograph in BSE topographic mode is shown in Figure 6-5. The variations in topography are highlighted and the crosshatch morphology is clearly visible. BSE topography mode allows for determination of the ridge density and symmetry.

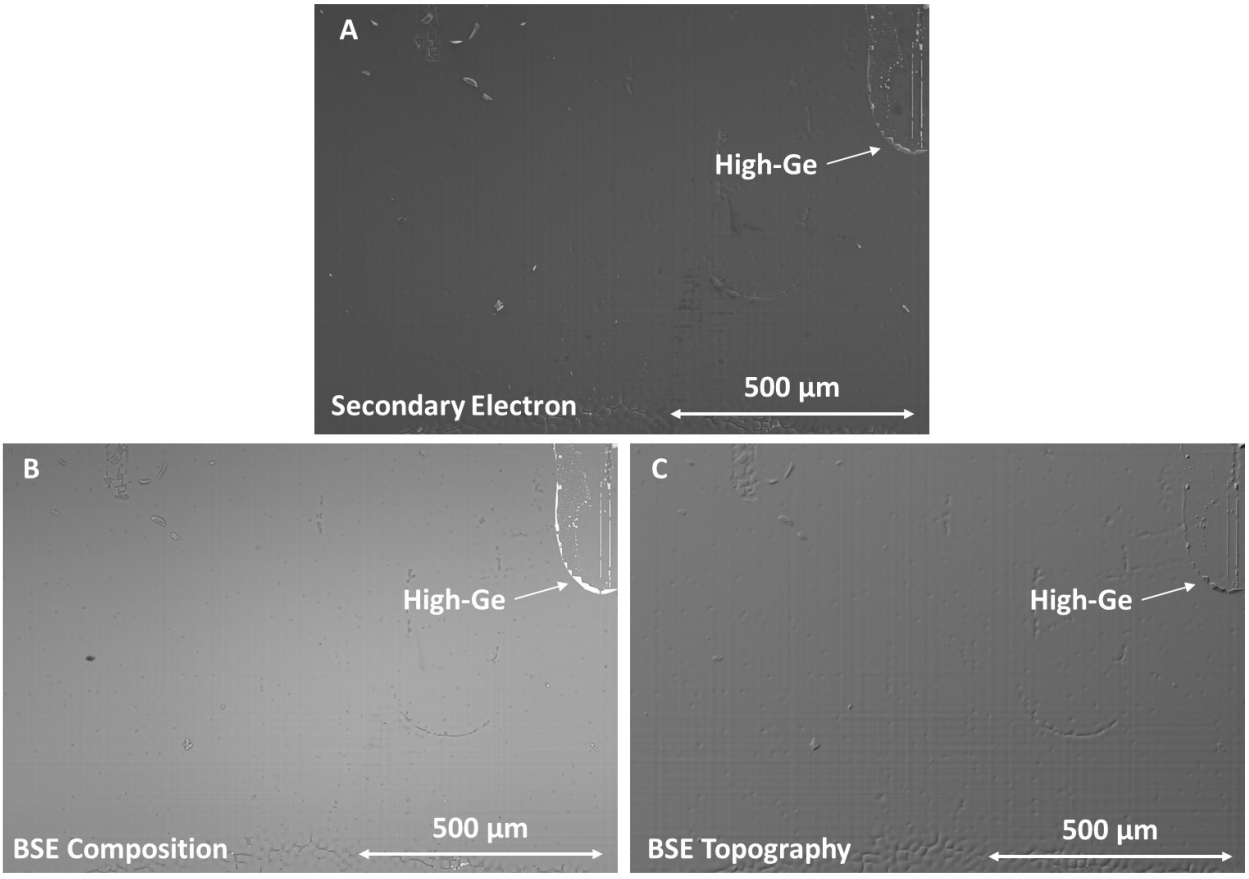


Figure 6-5. Three scanning electron micrographs of the same area using different imaging modes: a) secondary electron imaging mode, b) backscattered electron composition mode, and c) backscattered electron topography mode.

6.3.Etch Pit Density

Etch pit density (EPD) was the primary technique used to determine the aerial threading dislocation density in this thesis. When a threading dislocation intercepts the surface, there are dangling bonds which increases the energy of the film in the vicinity of the threading dislocation. With the selection of an appropriate etchant, the etch rate of the film at a threading dislocation will be greater than the etch rate of the film. This results in the formation of pits which can be observed and counted by SEM imaging.

The etching solutions used to determine the EPD of Si composed of three parts. First, an oxidising agent is used which converts the Si site into a soluble oxide. For Si and SiGe etchants, the oxidising agent is typically Cr^{6+}. Second, a fluoride compound, typically HF acid, is used to dissolve the

oxide. Third, a solvent, such as water, is used to dilute the etchant in order to control the etch rate [200].

There are three primary etchants used to reveal defects in Si and low-Ge SiGe epilayers [201]: the Sirtl etch, which reveals defects on (111) surfaces , and the Secco and Schimmel etchants which reveal defects on (001) surfaces.

The Schimmel etchant was developed for EPD measurements of Si (001) films [202] and uses CrO_3 as the oxidising agent. It was developed to replace the Secco etch, which uses $K_2Cr_2O_7$ as the oxidising agent, since it does not require ultrasonic agitation, which reduces damage to the epilayer from cavitation, and the etch pit time is half that of the Secco etch. The Schimmel etchant is appropriate for both n and p-type Si.

Given the composition of the low-Ge content SiGe epilayers is close to pure Si, the Schimmel etchant was adapted for EPD measurements of the epilayers grown by LLPE. The etchant was mixed with the following ratios:

$$1\text{g } CrO_3 : 35 \text{ mL } H_2O : 20 \text{ mL HF}$$

The samples were etched for 1 minute without agitation and then rinsed with water. The etch pit density was determined by counting the pits by SE imaging in the SEM and averaging the density across several images.

6.4. Atomic Force Microscopy

Atomic force microscopy (AFM) was used to quantify the film thickness to determine the critical thicknesses for dislocation glide and nucleation. An Asylum MFP3D AFM was used in contact mode for imaging all the samples. AFM provides topographical information by scanning a cantilever probe, which is in contact with the surface, across the surface and measuring the deflection of the cantilever. In an AFM image, as shown in Figure 6-6, the variation in film height due to the crosshatch morphology can be imaged, where the bright areas represent the elevated ridges, and the dark represent the troughs.

Film thickness was determined by investigating the depth of pits in the SiGe epilayer. The pits are formed due to incomplete film coalescence in areas where the re-growth of the native oxide prevents epitaxial growth. An example calculating the film thickness via a pit is given in Figure

6-6. The pit is highlighted by the red circle. A line scan of the height variation along the red line shows that the pit depth is approximately 200 nm. To determine the film thickness, the surface undulations from the crosshatch morphology, which vary the film height by almost +/- 50 nm, must be considered. The average height is shown by the black dashed line, which conveniently places the average height at 0 in this case. As a result, the film thickness is approximately 200 nm in this region.

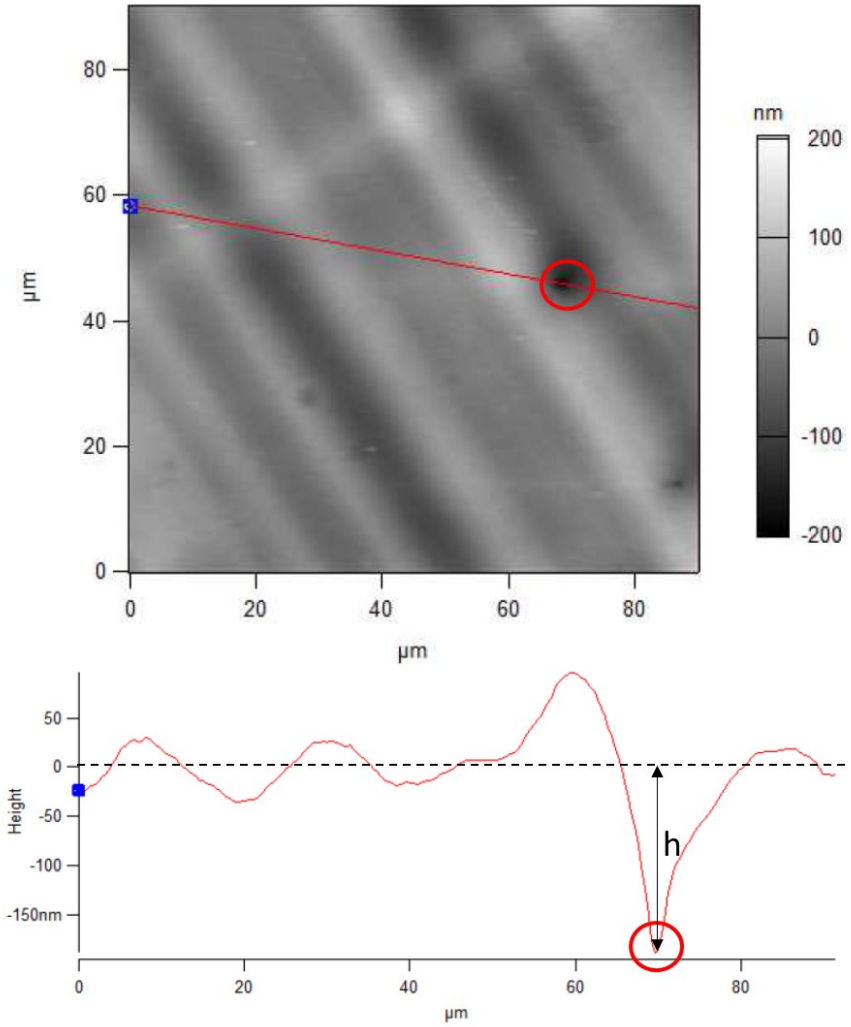


Figure 6-6. AFM scan of a SiGe crosshatch film with the depth profile of a pit of film thickness measurement.

Chapter 7

Growth of SiGe Epilayers with Asymmetric Strain

The following chapter presents the growth of a SiGe epilayer on a Si (001) substrate by traditional LPE and by LLPE. The origin of parallel arrays of misfit dislocations is described and the resulting asymmetric strain relaxation is characterised. The body of this chapter was reproduced from the article "Asymmetric, compressive, SiGe epilayers on Si grown by lateral liquid-phase epitaxy utilizing a distinction between dislocation nucleation and glide critical thicknesses" which is published in the Journal for Crystal Growth [203].

7.1. Liquid-Phase Epitaxy Growth

A SiGe thin film was grown by planar LPE on a Si (001) substrate (without lateral motion) with the following parameters: X_{Ge}=2 at. %, T_{sat} = 975˚C, ΔT= 260 ˚C, cooling rate of 20˚C/min. At the edge of the graphite well, a small amount of the In solution could leak out of the well into the small gap between the substrate and the graphite boat (g in Figure 5-8) due to the preference of the solution to wet the Si substrate over the graphite. As a result, a thickness gradient formed at the edge of the film due to the limited solute transport to the solution at the edges. The edge of the epilayer, is shown in Figure 7-1. On the right of the micrograph, the bulk $Si_{0.974}Ge_{0.026}$ epilayer,

which grew beneath the graphite well is present which displays the typical crosshatch morphology with dislocation glide along both the [110] and [1$\bar{1}$0] directions. The edge of the film, which grew beneath the gap is shown on the left of the micrograph and is characterised by the thickness gradient (lower part of Figure 7-1). The thickness of the film along the dashed line in the upper part of Figure 4 was determined by measuring the depth of the nearby pits by atomic force microscopy. The pits are formed from incomplete film coalescence in regions where native oxide re-growth on the substrate prevented film growth. As the epilayer thins from the bulk (1.2 µm) to the edge, the crosshatch ridges are observed only in the [110] direction, towards the edge of the film. The ridges in the [1$\bar{1}$0] direction are not present at thicknesses much below 500 nm. The ridges in the [110] direction are present in the epilayer to a minimum thickness of 150 nm. The transitions from an orthogonal crosshatch morphology to unidirectional ridges and then to a ridge free morphology shows that there are two critical thickness with different activation energies. The two critical thicknesses are shown here for the first time as the critical thicknesses for dislocation nucleation (h_N) and for dislocation glide (h_G).

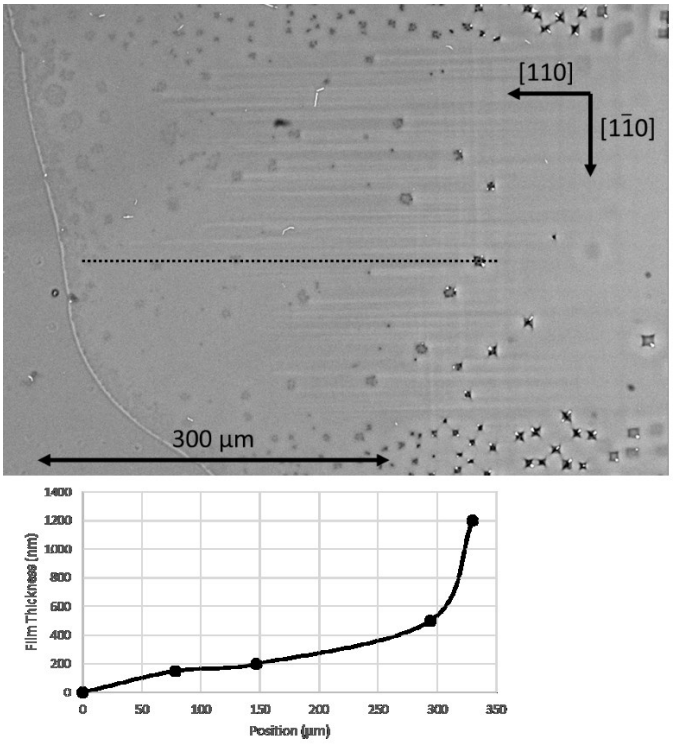


Figure 7-1. Electron micrograph in backscattered electron topographic mode of the edge of a $Si_{0.974}Ge_{0.026}$ epilayer on Si (001) grown by traditional LPE. The film thickness along the dashed line is shown in the chart below. The film thickness was measured by AFM evaluation of the pit depth at select locations. The line passing through the points was fitted to help guide the reader.

The critical thickness for dislocation glide (h_G) is defined as the thickness at which the glide of threading dislocations is activated, which creates misfit dislocation segments at the interface. A force is resolved onto a threading dislocation, in the direction of the dislocation slip from the shear stress introduced to the epilayer by the lattice mismatch. If the force on the threading dislocation is greater then the line-tension force, which is proportional to the energy required to create a misfit dislocation, the threading dislocation will glide and create a misfit dislocation segment at the interface. This thickness, 150 nm, is equal to the predicted critical thickness from Matthews and Blakeslee [15, 19, 20], given the lattice mismatch is 0.11 %, which assumes that the threading dislocation segment is inherited in the epilayer from the substrate. This is the lowest energy source for misfit dislocation nucleation, and thus corresponds to the lowest predicted critical thickness.

The critical thickness for dislocation nucleation (h_N) is defined as the thickness required to nucleate misfit dislocations through, for example, surface half loop nucleation mechanisms or dislocation interaction and multiplication mechanisms. These mechanisms have higher activation energies and thus have higher predicted critical thicknesses [15]. However, the nucleation of dislocations is kinetically limited [26] and h_N will be dependant on the growth conditions, such as temperature, growth rate and surface roughness, in addition to the misfit strain energy (i.e. film thickness).

The two critical thicknesses can be identified in Figure 7-1. There is a transition from an orthogonal crosshatch morphology to single direction ridges at a film thickness of approximately 500 nm. The extinction of ridges in the $[1\bar{1}0]$ direction suggests that there is insufficient strain energy to nucleate new dislocations, thus $h_N \sim 500$ nm for $Si_{97.4}Ge_{2.6}$. The dislocations that are present at thicknesses below h_N were nucleated in the epilayer, where the thickness is greater than h_N, and then glided towards the edge of the film until they reach h_G (150 nm). At this point, the force on the threading dislocation from the strain energy is equal to the line-tension force of the dislocation and the dislocation ceases to glide. In this region, the dislocations glide hundreds of microns, from the bulk towards the edge of the epilayer. The long misfit dislocations either terminate at a pit or as a threading dislocation when the glide is exhausted. This supports the hypothesis that the dislocations nucleate in the bulk, and not at the edge of the film, since there are no dislocations that extend from the edge of the film which terminate before reaching the bulk or which glide in the $[1\bar{1}0]$ direction in this region with thickness between 150 and 500 nm.

These results show that the activation energy for the formation of misfit dislocations by glide of threading dislocations is lower than the activation energy for the nucleation of a new dislocation. Assuming there is no plastic deformation prior to misfit dislocation nucleation, the strain energy at a film thickness h_N is 3.3 times greater than the strain energy at h_G. In this way, long misfit dislocations, which are nucleated above h_N can be propagated through an epilayer if the thickness of the layer is less than h_N, but greater than h_G.

7.2.Lateral Liquid-Phase Epitaxy Growth

LLPE was performed to further extend the propagating dislocations by ensuring that the lateral growth film thickness was kept below h_N and above h_G. Lateral growth was performed with the following parameters: X_{Ge}= 2 at. %, T_{sat}= 790˚C, ΔT = 20˚C, cooling rate of 20˚C/hour, and a lateral pull rate of 4 mm/min. The epilayer contained 2.6 at. % Ge, the same as the planar LPE epilayer discussed above.

Three morphological regions can be identified on the LLPE sample, as illustrated schematically in Figure 7-2. The growth is initiated in Region I (Figure 7-3a) which displays the typical isotropic crosshatch morphology. The epilayer was propagated laterally into Region II (Figure 7-3b) which shows ridges aligned only in the [110] lateral growth direction. Lastly, the lateral growth continued into Region III (Figure 7-3c) which does not display any ridges.

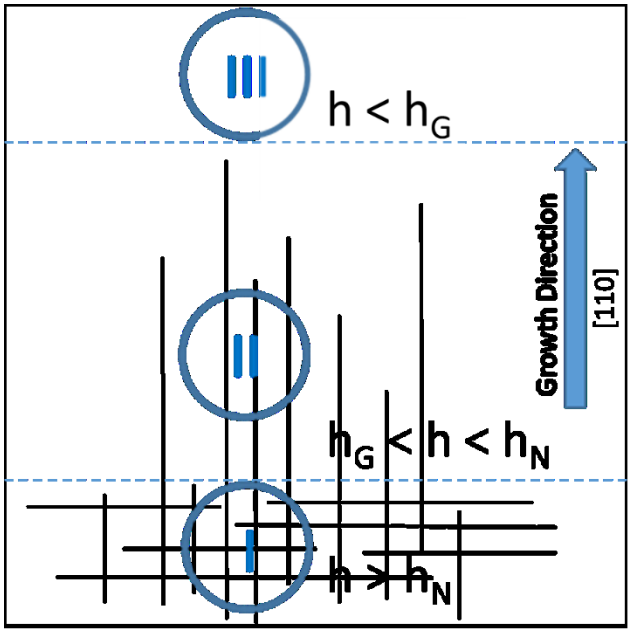


Figure 7-2. Schematic of lateral LPE growth

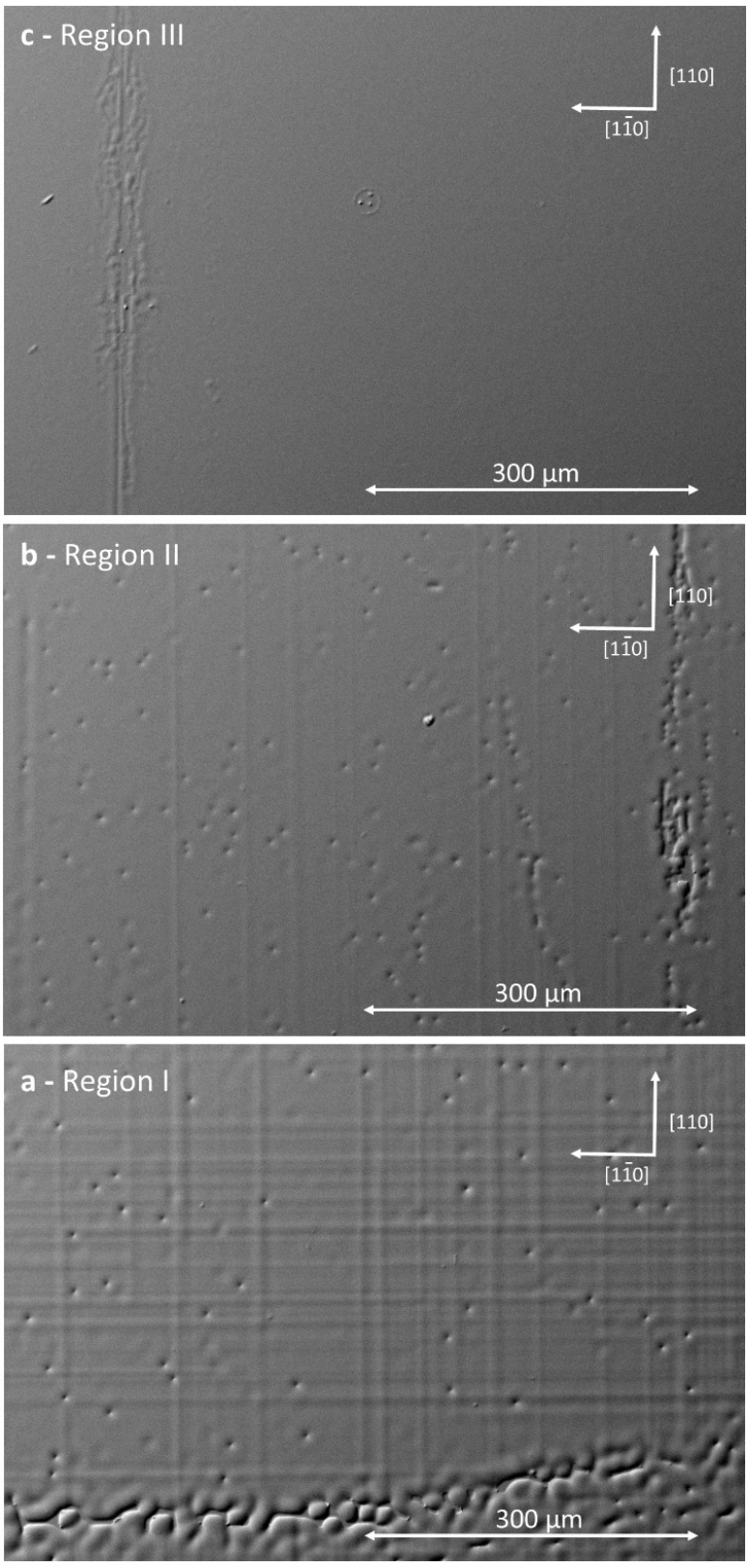


Figure 7-3. Electron micrographs in backscattered electron topographic mode of the three Regions illustrated in Figure 7-2: Region 1 (a), Region II (b) and Region III (c)

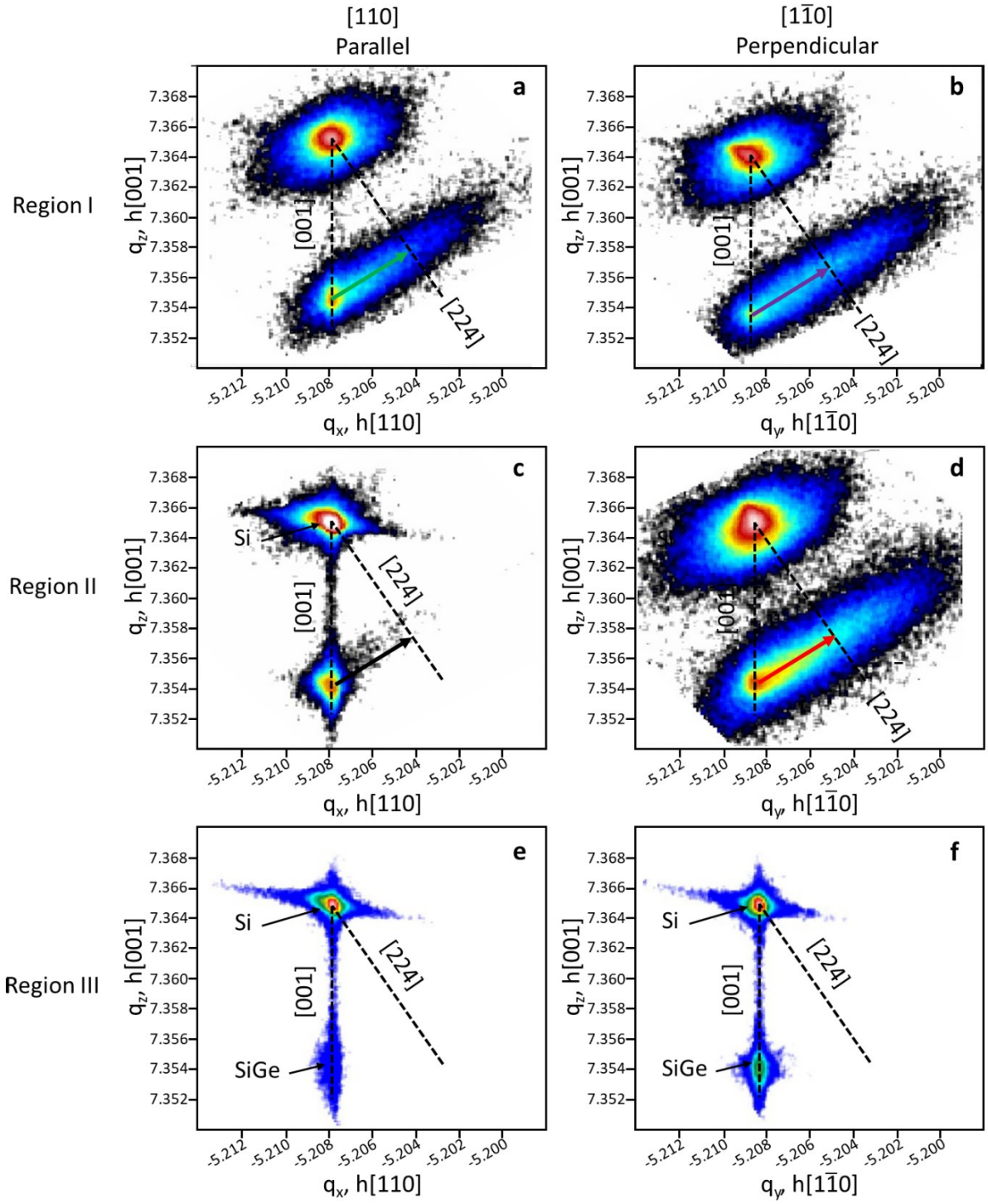


Figure 7-4. Reciprocal Space Maps of the 224- reflections taken at 90° from each other for Region I (a & b), Region II (c & d) and Region III (e & f). Scans in the [110] analysis direction, parallel to the growth direction (a, c, & e) and scans in the [1$\bar{1}$0] analysis direction, perpendicular to the growth direction. The colour bar intensities are identical for a, b, c & d.

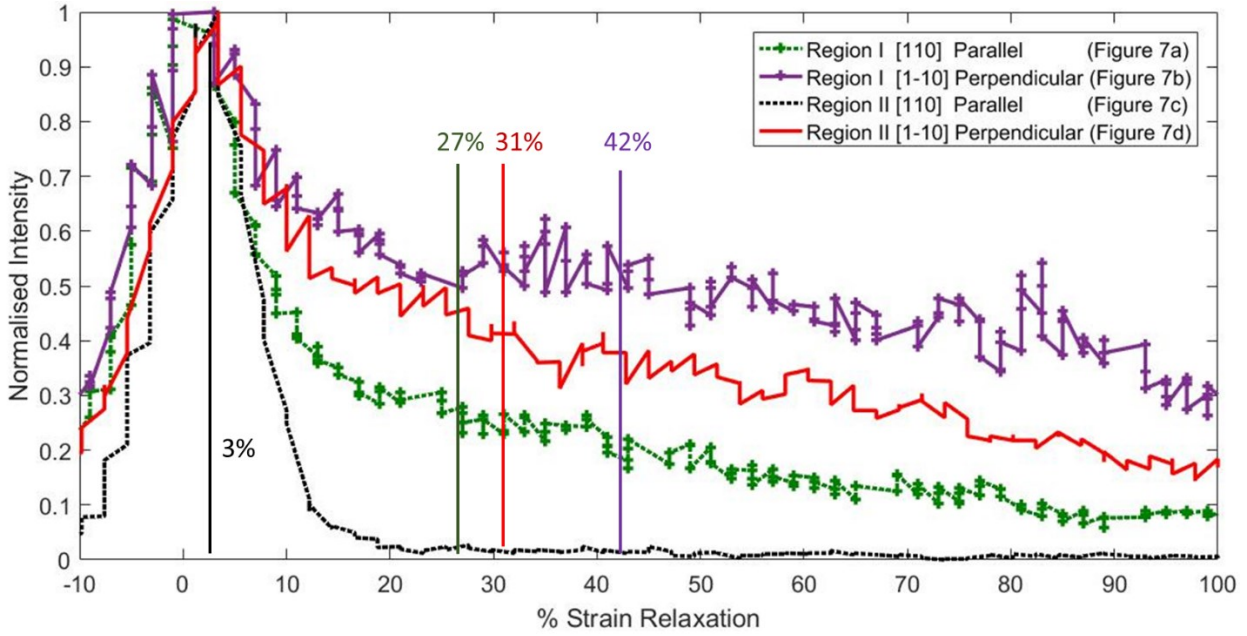


Figure 7-5. Plot of the normalised intensity from the RSMs in Region II as a function of the degree of strain relaxation along the strain relaxation path.

Since the crystal growth first nucleated in Region I, there were no initial misfit dislocations in this region, the film thickness was greater than h_N (1.5 μm), so dislocations nucleated in both orthogonal directions to relieve the misfit stress, as shown in the SEM micrograph in Figure 7-3a. Reciprocal space maps were collected in both orthogonal <110>-type directions to quantify the strain relaxation in Region I. The 224 glancing incidence RSM, whose plane of analysis (the plane that contains the incident and diffracted X-ray beams) intersects the substrate surface in the [110] direction (the analysis direction which in this case is parallel to the lateral growth direction), is shown in Figure 7-4a. This RSM shows the out-of-plane lattice constant (q_z) on the vertical axis, and the in-plane lattice constant (q_x) on the horizontal axis. The epilayer peak is broad which indicates the onset of plastic strain relaxation from the nucleation and glide of misfit dislocations. However, the peak of highest intensity lies directly below the substrate peak, which indicates that a significant portion of the epilayer is fully strained. The RSM in the [1$\bar{1}$0] analysis direction (perpendicular to the growth direction) is shown in Figure 7-4b. The epilayer peak is slightly broader than in the [110] direction, though the peak of highest intensity remains below the substrate peak.

The strain relaxation follows the relaxation path shown in the RSMs, which begins at the fully strained point, which lies below the substrate peak on the [004] reciprocal lattice vector, and follows the arrow to the fully relaxed point which lies along the [224] reciprocal lattice vector. The variation in intensity of the RSMs along the relaxation path is plotted in Figure 7-5 for both <110> directions for Regions I and II. The intensity was normalised to the peak intensity for each RSM. The peak intensity for the curves associated with Region I lies above the fully strained point (0 % strain relaxation) and the curves decay as the strain relaxation increases. This indicates that there is a variation in strain relaxation across the sample, from fully strained to fully relaxed, though the plurality of the film remains fully strained. The weighted average of the strain relaxation along the relaxation path in Region I is 27 % and 42 % in the [110] and [1$\bar{1}$0] directions, respectively. The difference in strain relaxation between the <110> directions can be attributed to the slight increase in the density of ridges lying in the [110] direction, as opposed to the [1$\bar{1}$0], as summarised in **Error! Reference source not found.**, due to the onset of the lateral growth behaviour.

	[110] Parallel			*[1$\bar{1}$0] Perpendicular*				
	Strain (%)	% Strain Relaxation	Ridge Density (μm^{-1})	Strain (%)	% Strain Relaxation	Ridge Density (μm^{-1})	Δ % Strain Relaxation	Δ Strain (%)
Region I	-0.080	27	0.06	-0.064	42	0.04	15	0.016
Region II	-0.107	3	0.02	-0.076	31	0.002	28	0.031
Region III	-0.110	0	0	-0.110	0	0	0	0

Table 7-1. Summary of the strain relaxation in each region.

As lateral growth progressed, the film thickness slowly decreased until the film thickness reached h_N at which point, there was not sufficient strain energy to nucleate new dislocations. The SEM micrograph for Region II (Figure 7-3b) shows crosshatch ridges which lie only in the [110] direction, parallel to the lateral growth direction. These ridges extend millimeters in length and indicate the presence of underlying misfit dislocations. Ridges are not observed in the direction perpendicular to the lateral growth direction since misfit dislocations did not nucleate in the [1$\bar{1}$0] direction in Region II. The film thickness in this region is approximately 175 nm ($h_G < h < h_N$).,

The 224 glancing incidence RSM in the [110] analysis direction, (Figure 7-4c), shows that there is no strain relaxation in the epilayer, since the epilayer peak lies directly below the substrate peak, which indicates that the in-plane lattice constant of the epilayer conforms to the lattice of the substrate. This is expected given the absence of misfit dislocations in the [1$\bar{1}$0] direction. The 224 glancing incidence RSM in the [1$\bar{1}$0] analysis direction, perpendicular to the misfit dislocations (Figure 7-4d), on the other hand, shows a broad $Si_{0.974}Ge_{0.026}$ peak, similar to the epilayer peak observed in Region I (Figure 7-4a and 7b), which indicates the onset of plastic relaxation. The peak of highest intensity remains below the substrate peak, like in Figure 7-4a & 7b. The anisotropic strain relaxation in Region II is highlighted in Figure 7-5. The weighted average of the strain relaxation is 3 % in the [110] direction and 31 % in the [1$\bar{1}$0] direction. The difference of 28 % between the <110> directions indicates the presence of asymmetric strain.

It is important to observe the large variation in strain relaxation along the relaxation path for Region II. The relaxation curve in the [1$\bar{1}$0] has a peak of greatest intensity centered around 0 % strain relaxation, which is identical to the total strain relaxation in the [110] direction, which demonstrates that a significant portion of the epilayer does not undergo plastic deformation from the gliding dislocations. However, the long tail to the right of the peak shows that there is a broad distribution of strain relaxation throughout the epilayer. The inhomogeneity of strain relaxation is expected since strain mapping has shown that strain relaxation from dislocations is localized to the vicinity (~micrometers) of dislocations [204]. The average dislocation separation in Region II is 50 μm, which is too low to fully relax the epilayer in the [1$\bar{1}$0] direction. This indicates that Region II has uniaxial compressive strain in the vicinity of the aligned dislocations, and isotropic compressive strain in the regions between the dislocations.

The film thickness continued to thin as the lateral growth progressed across Region II. When the film thickness reached h_G, dislocation glide ceased, which demarcates the beginning of Region III. In the SEM micrograph from Region III (Figure 7-3c) there are no ridges in either of the <110> directions, which is expected given that the film thickness does not allow for the nucleation of glide of misfit dislocations. AFM investigation confirmed the absence of ridges in this region. The epilayer thickness in this region is less than 120 nm ($h < h_G$), which is comparable to the thickness at which dislocation glide was terminated in the LPE growth discussed above (Figure

7-1). In this region, both 224 RSMs are identical (Figure 7-4e & f). The epilayer peaks are directly below the substrate peaks, which indicates a fully strained epilayer.

7.3. Conclusions

These results provide a pathway to the development of a growth technique to deposit a blanket film with uniaxial compressive strain in a single step on Si (001). First, misfit dislocations are nucleated in a seed area, where the thickness is greater than the critical thickness for misfit dislocation nucleation and glide. Secondly, the film thickness is reduced below h_N, but greater than h_G, as the epilayer is propagated laterally in the [110] direction, such that the glide of misfit dislocations is promoted while the nucleation of new misfit dislocations is inhibited. This allowed the observation of distinct h_N and h_G for the first time.

In this way, a $Si_{0.974}Ge_{0.026}$ epilayer was grown with asymmetric compressive strain. The epilayer was essentially fully strained in the direction of the lateral crystal growth, and was 31 % strain-relaxed in the orthogonal direction. The difference in strain relaxation of 28 % is slightly lower than the 37 % reported previously [103], however this technique has the potential to increase both the strain asymmetry and the magnitude of the strain. The magnitude of the strain is low, due to the low Ge content. Film growth of SiGe on Si (001) substrates by LPE has been reported for Ge contents up to 13 % [182], after which the growth transitions to 3D island growth. Thus, SiGe epilayers grown by LLPE are expected to produce a blanket film of uniaxial strain of at least 0.52 %.

To achieve a blanket film with uniaxial strain the misfit dislocation density must be increased. As the density of misfit dislocations (which lie in the [110] growth direction) is increased, the strain relaxation can approach 100 % in the orthogonal direction. This will simultaneously increase the homogeneity of the strain distribution, since the distance between misfit dislocations will be less than the radius of plastic relaxation from a single misfit dislocation. The misfit dislocation density can be increased by increasing the cooling rate during growth of the seed area [183] or by introducing defects into the substrate below the seed area by ion implantation which can significantly increase the strain relaxation [99].

Chapter 8

Reduction of the Threading Dislocation Density in SiGe Epilayers by LLPE

The following chapter presents the reduction of the threading dislocation density in a SiGe epilayer grown by LLPE. The body of this chapter is reproduced from the article "Reduction of Threading Dislocation Density in SiGe Epilayer on Si (001) by Lateral Growth Liquid-Phase Epitaxy" published in the Journal for Crystal Growth.

8.1. LLPE Growth

LLPE was performed in a custom liquid-phase epitaxy (LPE) furnace. The construction of the furnace and the growth procedure have been reported previously [203]. The furnace was loaded with In as a solvent with 1.8 at. % Ge solute. The solution was saturated with Si at 792˚C then an undercooling of 6˚C was established prior to introducing the Si (001) growth substrate to the

solution. After the introduction of the growth substrate, the solution was cooled at 0.27˚C/min while the substrate was pulled through the solution at a velocity of 0.12 mm/min. The growth was terminated when a cooling interval of 30˚C was reached and the sample was removed from the solution. The growth substrate dimensions were 12 mm x 12 mm and lateral growth was achieved across the length of the substrate and approximately 6 mm of the width.

The composition and strain state of the SiGe films were determined by high-resolution, triple-axis, X-ray diffraction using a Bruker D8 Discovery X-ray diffractometer. To quantitatively determine the composition and strain of the epilayer, an asymmetric (224) reflection was collected in each region. By using the asymmetric (224) scan, the in-plane and out-of-plane lattice constants can be deduced. In this work, the (224) glancing incidence reflection was collected such that the plane of analysis (the plane that contains the incident and diffracted X-ray beams) intersects the substrate surface in the $[1\bar{1}0]$ direction (the analysis direction which in this case is perpendicular to the misfit dislocation line direction grown by LLPE), thereby enabling the strain relaxation from the misfit dislocations which lie in the [110] growth direction to be quantified.

The film thickness was determined by measuring the depth of the nearby pits by atomic force microscopy, and confirmed by scanning electron micrographs (SEM). The pits are formed from incomplete film coalescence in regions where native oxide re-growth on the substrate prevented film growth.

The aerial threading dislocation density was determined by measuring the etch pit density (EPD). The epilayer was etched for 1 minute in a 1g CrO_3 : 35 mL H_2O : 20 mL HF etchant [202] to preferentially etch the areas in the vicinity of threading dislocations. The etch rate at a threading dislocation was approximately 1 μm /min which is approximately an order of magnitude greater than the etch rate of the epilayer. The etch pit density was determined by counting the pits after taking SEM images, each with an area of $5x10^4$ μm^2. The total measurement area for each region was $9x10^5$ μm^2. In addition, to qualify the misfit dislocation density, the linear ridge density was measured and is defined here as the number of crosshatch ridges which lie in the [110] direction (the growth direction), and is calculated by counting the number of ridges in the SEM micrographs which intersect a line of a given length in the $[1\bar{1}0]$ direction.

Results & Discussion

A $Si_{0.973}Ge_{0.027}$ epilayer was grown by LLPE. Three morphological regions can be identified on the LLPE sample, as illustrated schematically in Figure 8-1. The growth was initiated in Region I, which displays the typical isotropic crosshatch morphology, as shown in the SEM micrograph (Figure 8-2). The thickness of the epilayer is 1.2 μm, which is greater than h_N. Consequently, dislocations nucleated and glided in both orthogonal directions, displaying the typical cross hatch morphology, to relieve the misfit stress. The linear ridge density in the [110] direction is 700 ± 200 cm^{-1}.

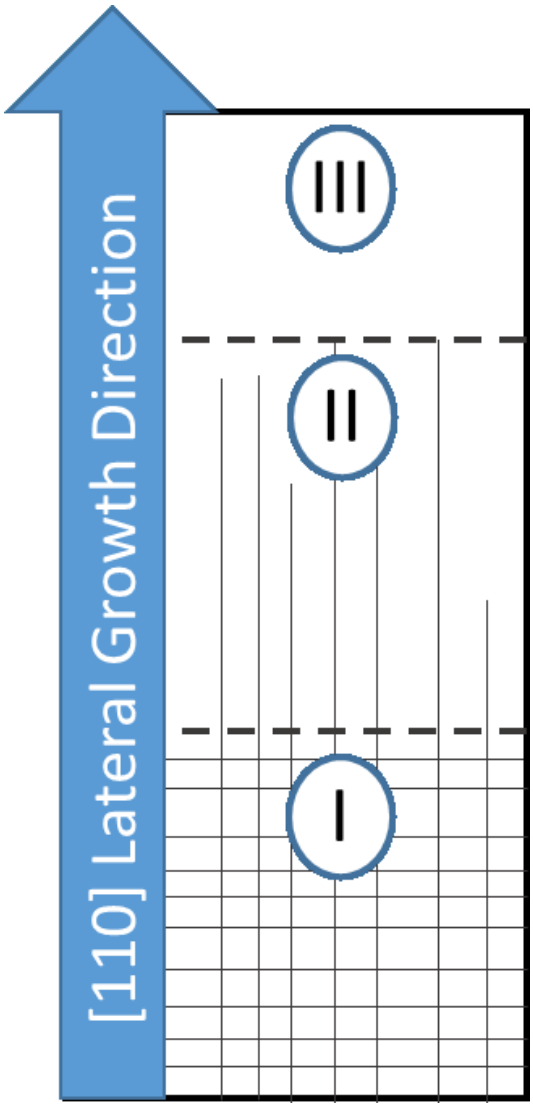


Figure 8-1. Schematic of an LLPE growth sample, illustrating the three regions with different crosshatch morphologies.

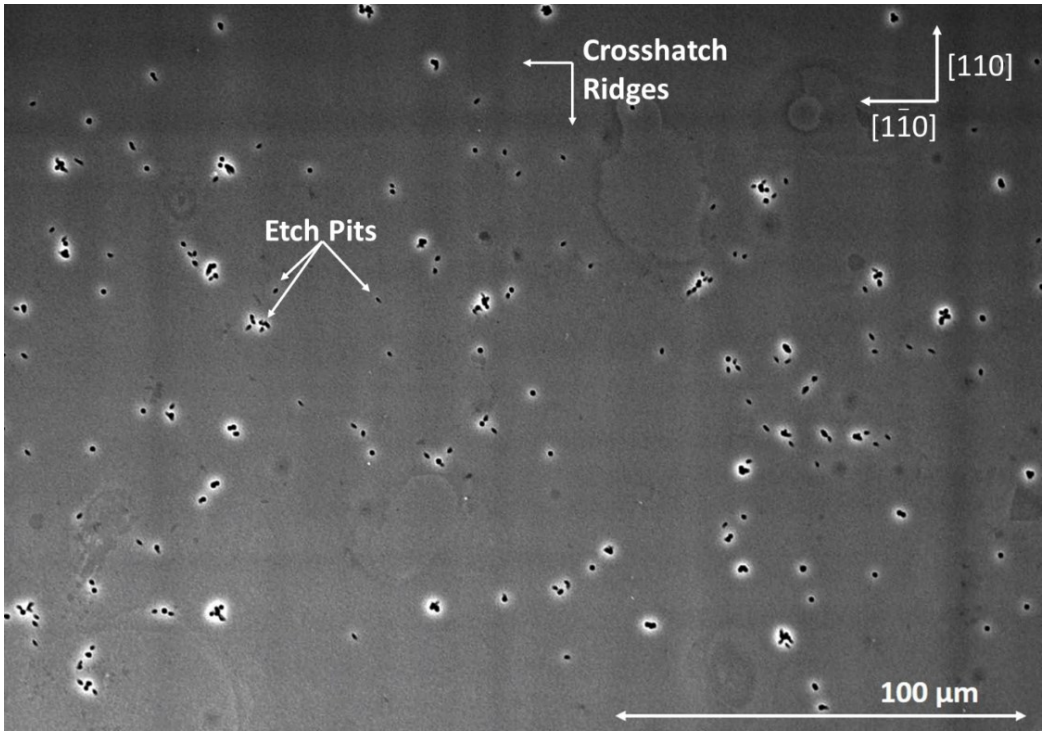


Figure 8-2. SEM micrograph of Region I. The dark spots marked by the arrows are etch pits. The orthogonal crosshatch network is aligned in the <110> directions, and can be seen in the background of the image, as indicated by the arrows.

The epilayer thickness was reduced as the film was propagated laterally in the [110] direction. At a thickness of approximately 170 nm, the crosshatch pattern ceased, which indicates that the nucleation of dislocations is inhibited (h_N=170 nm), and was replaced by an array of ridges parallel to the [110] direction. This marked the beginning of Region II. As a result, only misfit dislocations which already nucleated in Region I could glide along the [110] growth direction into Region II. This can be observed in Figure 8-3, where the epilayer thickness is 100 nm and only ridges lying in the [110] direction are present. The ridge density in the [110] direction in Region II is 600 ± 200 cm^{-1}, which is comparable to the ridge density in Region I, as expected since the misfit dislocations in Region II originated from Region I.

As the lateral growth progressed into Region III, the film thickness decreased further and became lower than 50 nm, which inhibited both the nucleation and glide of misfit dislocations (h_G = 50 nm). As a result, there were no crosshatch ridges in either direction, which can be observed in Figure 8-4.

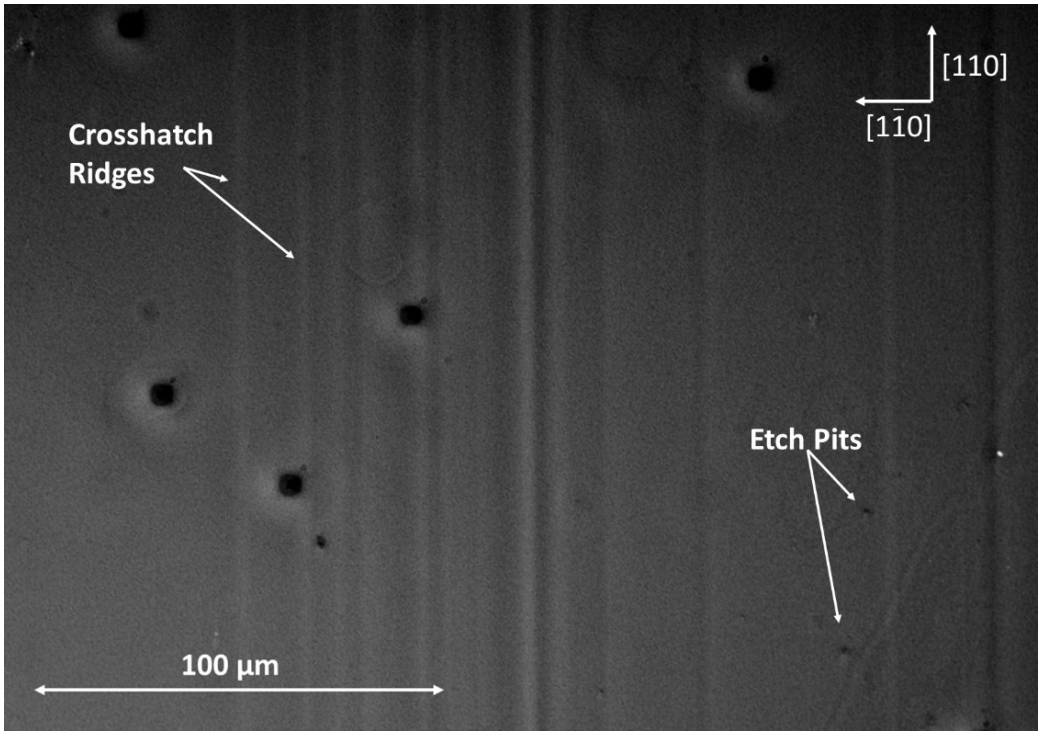


Figure 8-3. SEM micrograph of Region II. The dark spots marked by the arrows are etch pits. The orthogonal crosshatch network is aligned in the <110> directions, and can be seen in the background of the image, as indicated by the arrows. The large dark squares are film discontinuities.

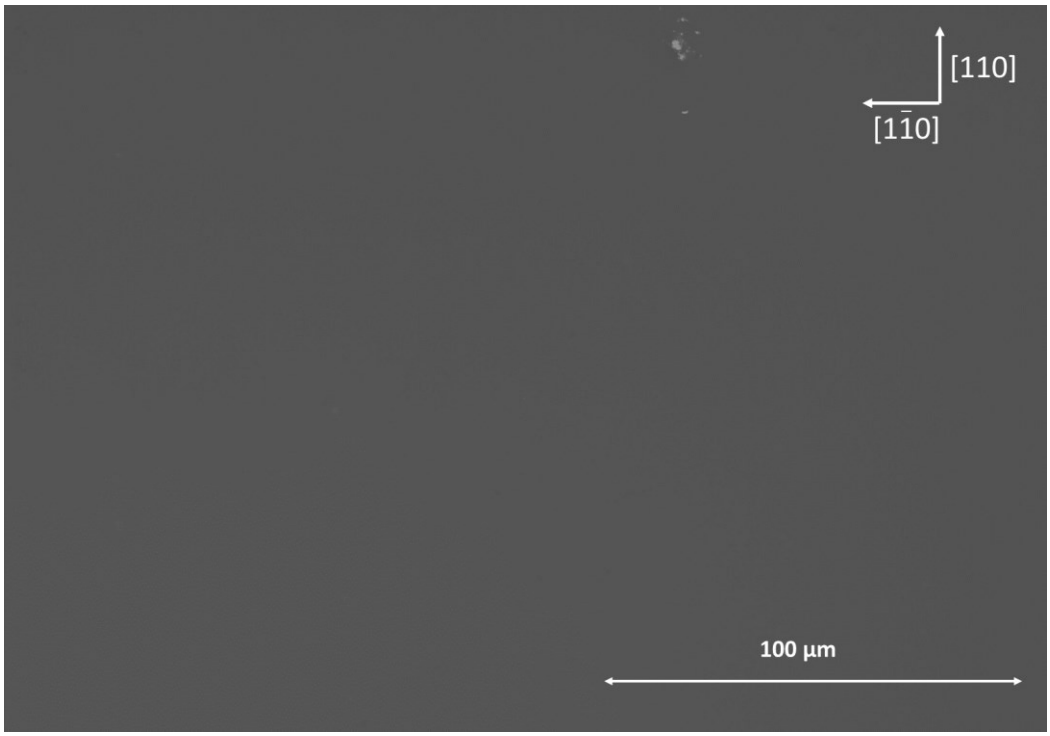


Figure 8-4. SEM micrograph of Region III. There are no ridges or etch pits visible.

Etch pits are clearly visible, as indicated in Figure 8-2, and are either present as individual pits, or in clusters of up to eight pits. The etch pit density in Region I is $6x10^5 \pm 5x10^5$ cm^{-2}, as shown in Table 8-1. The error represents one standard deviation. There is a significant reduction in etch pits in Region II, as seen in Figure 8-3. The large square pits existed prior to EPD and were formed during film growth due to incomplete film coalescence caused by incomplete oxide removal. The etch pit density in Region II is $5x10^3 \pm 1x10^4$ cm^{-2}, two orders of magnitude lower than the density in Region I. The large error associated with the etch pit density in Region II is due to the inhomogeneous distribution of the etch pits, given that some sampled regions had no etch pits, while others had as many as 10^4 cm^{-2}.

The etch pit density in Region III, where there are no misfit dislocations, was determined to be $7x10^2 \pm 2x10^3/cm^2$, which is on the order of the defect density expected from prime grade Si substrates. This suggests that the threading dislocations in this region were inherited from the substrate.

	Threading Dislocation Density (cm^{-2})	*Misfit Dislocation Density [110] (cm^{-1})*	*Strain Relaxation (%)*	*Misfit Dislocation Length [110] (mm)*
Region I	$6x10^5 \pm 5x10^5$	3.6×10^4	63	2.4
Region II	$5x10^3 \pm 1x10^4$	1.0×10^4	18	10.5
Region III	$7x10^2 \pm 2x10^3$	0	0	/

Table 8-1. Summary of the dislocation densities in each region.

The density of misfit dislocations which lie in the [110] direction ($\rho_{MD\ [110]}$) in each region was calculated from Equation 8-1 [15], where δ is the plastic strain relieved by the misfit dislocations and b_{eff} is the effective Burgers vector of the misfit dislocation. The effective Burgers vector is equal to $a/\sqrt{8}$ for 60˚ misfit dislocations, where a is the lattice constant of the epilayer [205].

$$\rho_{MD\,[110]} = \frac{\delta}{b_{eff}}$$

Equation 8-1

The plastic strain relaxation was determined by X-ray diffraction. The 224 glancing incidence reciprocal space map (RSM) for Region I is shown in Figure 8-5a. This RSM shows the out-of-plane lattice constant (q_z) on the vertical axis, and the in-plane lattice constant (q_y) on the horizontal axis. The center of the $Si_{0.973}Ge_{0.027}$ peak corresponds to 83 % strain relaxation. However, the broadness of the peak indicates that there is a range of strain relaxation in the epilayer, from fully strained to fully relaxed. As discussed previously [203], the strain relaxation is symmetrical in both <110> directions in Region I. The weighted average of the strain relaxation is 63 %, which gives a misfit dislocation density in the [110] direction of $3.6x10^4$ cm^{-2} (Table 8-1).

The RSM for Region II is shown in Figure 8-5b. The broadness of the peak shows the onset of plastic relaxation. However, the peak of highest intensity is directly below the substrate peak, which indicates a significant portion of the epilayer is fully strained. The weighted average of the strain relaxation is 18 %, which corresponds to a misfit dislocation density in the [110] direction of $1.0x10^4$ cm^{-2} (Table 8-1).

To ensure that the reduction in threading dislocation density was due to the promotion of misfit dislocation glide and the inhibition of dislocation nucleation, and not to a decrease in the misfit dislocation density, the average misfit dislocation length ($\langle l \rangle$) was calculated from Equation 8-2 [15] each region, and is shown in Table 8-1. The misfit dislocation length was increased by an order of magnitude from Region I to II, which further supports the assertion that the reduction in threading dislocation density is attributed to the misfit dislocation glide, and not a change in misfit dislocation density.

$$\rho_{TD} = 4\rho_{MD}\left(\frac{1}{\langle l \rangle} - \frac{1}{L}\right)$$

Equation 8-2

As discussed previously [203], the strain relaxation is asymmetrical in Region II, as there is no strain relaxation in the [110] direction. The difference in the RSMs between Regions I and II can be attributed, in part, to the slight decrease in misfit dislocation density in Region II. An important source for the difference in the RSMs may be due to the inhomogeneous distribution of the misfit

dislocations. In Region I the crosshatch ridges are evenly distributed across the surface of the epilayer, which results in a broad and symmetrical epilayer peak. However, in Region II, the spacing between ridges is inhomogeneous. A misfit dislocation will only relax the epilayer within the vicinity of a couple micrometers [204]. Thus, the large spacing between misfit dislocations in Region II (approximately 1 µm) shows that the epilayer is not homogeneously relaxed, with strain relaxed regions lying above the misfit dislocations, and strained regions between.

This results in large areas without misfit dislocations which are fully strained and areas with a higher density of misfit dislocations which are strain-relaxed. Given that the X-ray spot size is approximately 300 µm in diameter (the width of the SEM micrographs is 253 µm), the fully strained and strain-relaxed areas are both sampled by the X-ray. Increasing the misfit dislocation density in Region II is required to increase the strain relaxation as well as to improve the strain homogeneity, this can be accomplished by increasing the nucleation of misfit dislocations in Region I. The misfit dislocation density can be increased by increasing the cooling rate during growth of the seed area [183] or by introducing defects into the substrate below the seed area by ion implantation which can significantly increase the strain relaxation [99]. It is expected that as the misfit dislocation density is increased in Region II, so too will the threading dislocation density. However, given that misfit dislocation length is an order of magnitude longer in Region II, as shown in Table 8-1, and the absence of orthogonal misfit dislocations which act as dislocation pile-up sources, the threading dislocation density is expected to remain significantly lower than in Region I.

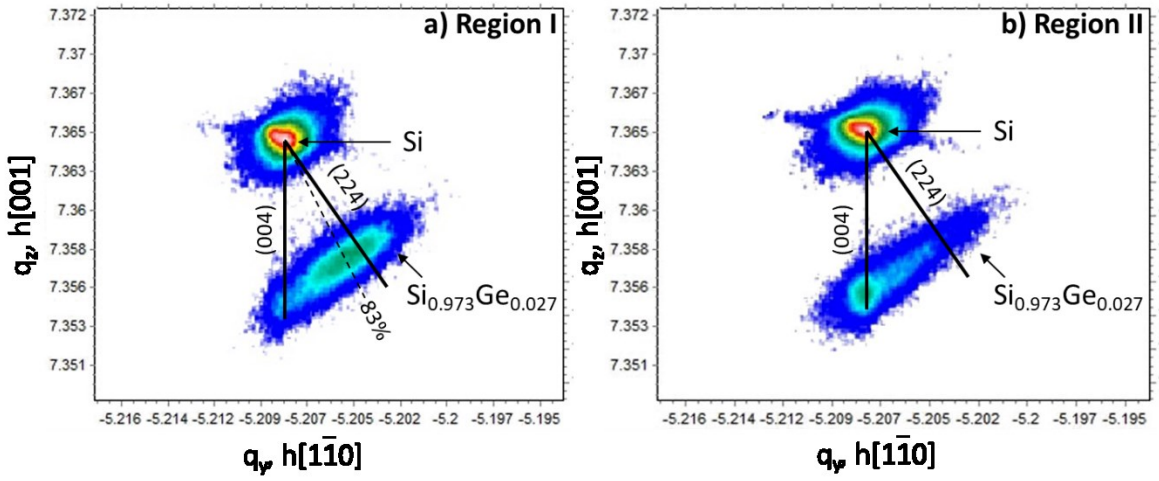


Figure 8-5. Reciprocal space maps of the 224 glancing incidence reflection in the [1$\bar{1}$0] analysis direction for a) Region I and b) Region II.

8.2. Conclusions

A $Si_{0.973}Ge_{0.027}$ film was grown laterally on a Si (001) substrate using the LLPE growth technique. The threading dislocation density was reduced by two orders of magnitude between the seed area (Region I), with thickness greater than h_N, and the lateral growth area (Region II), with thickness less than h_N but greater than h_G. The lateral growth and inhibition of dislocation nucleation in Region II favoured the formation of an array of long parallel misfit dislocations through the glide of dislocations nucleated in Region I. This demonstrates, for the first time, that lateral growth is a potential technique to grow low-defect density lattice-mismatched films over a large area. However, the misfit dislocation density must be increased to fully relax the epilayer and improve the strain homogeneity.

Chapter 9

Conclusions and Future Work

9.1. Conclusions

Lateral growth has been previously proposed as a technique to produce high-quality lattice mismatched films with low threading dislocation density. In this thesis, a lateral growth mechanism was proposed in Chapter 5.1 through which large area films could be deposited laterally which can produce long misfit dislocations in the lateral growth direction. A novel LLPE growth technique was developed to grow SiGe epilayers laterally on a Si (001) substrate. Lateral growth was achieved in a custom designed and built furnace by pulling the Si substrate through the growth solution at a controlled rate with the use of a stepper motor, as described in Chapter 5.2. Multiple design iterations were required to achieve epitaxial film growth. Most importantly, the graphite boat design was modified to allow for lateral growth and minimise solution carry-over, and strategies were implemented to reduce the native oxide regrowth.

SiGe films with low Ge content (< 3 at. % Ge) were grown laterally on Si (001) substrates. The lateral growth by LLPE yielded epilayers with a thickness gradient, with thick films ($h > 1$ μm) in the initial growth area and decreasing film thickness in the lateral growth direction. The thickness gradient allowed, for the first time, the direct observation of separate critical thickness for dislocation nucleation (h_N) and dislocation glide (h_G). The critical thickness for dislocation glide matches well with Matthews' model for strain relaxation by the glide of threading dislocations inherited from the substrate. The mechanism for dislocation nucleation remains undetermined, as such there is no model in the literature for the critical thickness for dislocation nucleation. The

lateral growth technique provides a pathway to determine the energetics of misfit dislocation nucleation since it filters out the contribution of dislocation glide.

When the thickness of the epilayer is between h_N and h_G dislocation nucleation is inhibited whereas the glide of dislocations, which were nucleated in a region where $h > h_N$, is permitted. This results in an array of long parallel misfit dislocation aligned in the [110] lateral growth direction. There are two benefits to the array of parallel misfit dislocations. The first benefit is the asymmetric strain relaxation, discussed in Chapter 7. The misfit dislocations only relieve the misfit strain in the direction orthogonal to the dislocation line, i.e. the $[1\bar{1}0]$ direction. As a result, the epilayer was fully strained in the [110] direction and 31 % strain relaxed in the $[1\bar{1}0]$ direction. Previously, arrays on parallel misfit dislocations were only achievable on Si (110) substrates and asymmetric strain relaxation on Si (001) could only be achieved by patterning a biaxially strained epilayer into thin stripes. LLPE provides the first technique to deposit a blanket film of asymmetrically strained SiGe on Si (001).

The second benefit of the array of parallel misfit dislocations is the significant reduction of the threading dislocation density when compared to the seed region with an isotropic dislocation network, as discussed in Chapter 8. The threading dislocation density in the seed area with an isotropic dislocation network ($h > h_N$) was on the order of $10^5/cm^2$ which is two orders of magnitude greater than the density in the laterally grown region with a parallel array of misfit dislocations ($10^3/cm^2$). The reduction in the threading dislocation density is attributed to the growth of long misfit dislocations through glide, given that dislocation nucleation is inhibited and the glide is not inhibited by orthogonal dislocations. Long misfit dislocations are preferable since they relieve more strain per threading dislocation arm than short misfit dislocations.

These results show that lateral growth is a potential solution to grow large area films on lattice mismatched substrates with asymmetric strain and low threading dislocation density. These materials could be used as a virtual substrate for the fabrication of pMOSFETs given that the hole mobility is increased in channels with uniaxial compressive strain.

9.2. Future Work

The conclusions in this thesis raise some interesting research questions. In particular, two potential avenues of research can be pursued: the extension of the LLPE growth process to SiGe epilayers with higher Ge content and different orientations, and the investigation of the energetics of dislocation nucleation and glide to provide insight into the dislocation nucleation mechanisms.

Extending lateral growth to higher Ge content poses the significant challenge of the introduction of 90˚ edge dislocations which are predominant in high misfit systems. The edge dislocations do not lie in the primary slip system, and are thus sessile. Thus, parallel arrays of long misfit dislocations are not expected to be produced by dislocation glide. However, lateral growth may provide a pathway to long edge dislocations. As described in Chapter 5.1, dislocations which nucleate in a seed area may terminate at the free edge of the epilayer at the heteroepitaxial interface. If the seed area is small, there is a greater chance of an edge dislocation terminating at the free edge. The lateral propagation of the epilayer could then propagate the otherwise sessile edge dislocation at the free edge of the epilayer.

The growth of strain relaxed SiGe layers with low threading dislocations was demonstrated in Chapter 8. However, the film was asymmetrically strained. If an isotropically strain-relaxed film is required, the nucleation of misfit dislocations in the orthogonal $[1\bar{1}0]$ direction is necessary. Since the lateral growth technique only extends the misfit dislocations in the [110] direction, the result is long misfit dislocations in the [110] direction and short misfit dislocations in the $[1\bar{1}0]$ direction (Figure 9-1a). The short misfit dislocations will increase the threading dislocation density. A potential solution to grow isotropically strain relaxed epilayers with low threading dislocation density is to rotate the substrate orientation by 45˚, such that the lateral growth direction is [100]. In this way, the misfit dislocations could be propagated laterally in both the <110> directions (Figure 9-1b).

As discussed in Chapter 4.3, LPE growth has some significant challenges and suffers from poor thickness and composition control, which make LPE an unattractive choice for the thin film growth, when compared to VPE techniques. For the LLPE system, in particular, poor temperature and position control cause poor reproducibility. More importantly, the native-oxide regrowth (Chapter 5.5) and solution-carry over (Chapter 5.6) problems provide significant hurdles to the LLPE growth, such that result of every growth is unpredictable and successful growth is rare.

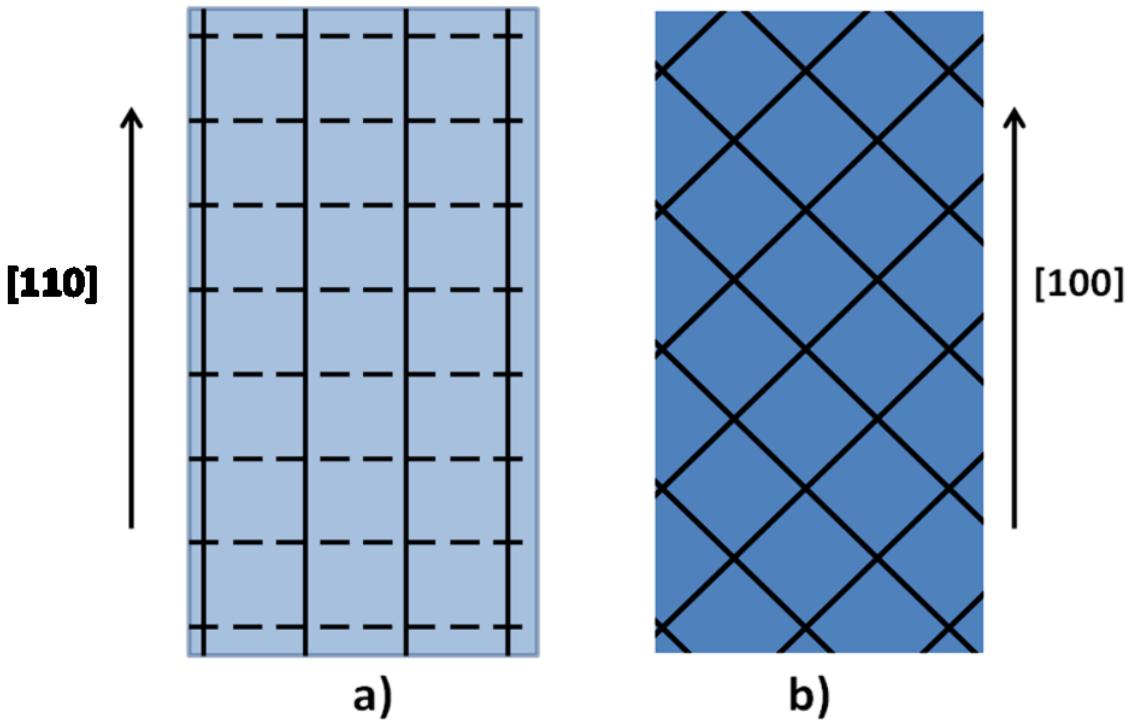


Figure 9-1. Schematic of isotropically strain-relaxed epilayers which are grown in the a) [110] directions and b) [100] direction.

Due to the low success rate and poor reproducibility of the LLPE growth technique, it is preferable to grow lateral SiGe films by either CVD or MBE. Lateral growth has been accomplished in the vapour phase using the VLS growth mechanism (Chapter 2.4.4), but requires multiple fabrication steps and only produces thin stripes of useful epilayer. Blanket films with asymmetric strain could be deposited by MBE using a travelling mask set-up, as shown in Figure 9-2. A plate with a slit is placed above a Si substrate which is coupled to a motor which can pull the substrate under the mask. Under high vacuum, the flux of atoms from the MBE target is parallel, and only the area below the slit will be exposed to the atomic flux. The substrate is pulled to slowly expose new areas to the atomic flux, thus controlling the lateral growth velocity. The film thickness can be controlled by either varying the pull speed, which will increase the exposure time of a given area, or by varying the atomic flux.

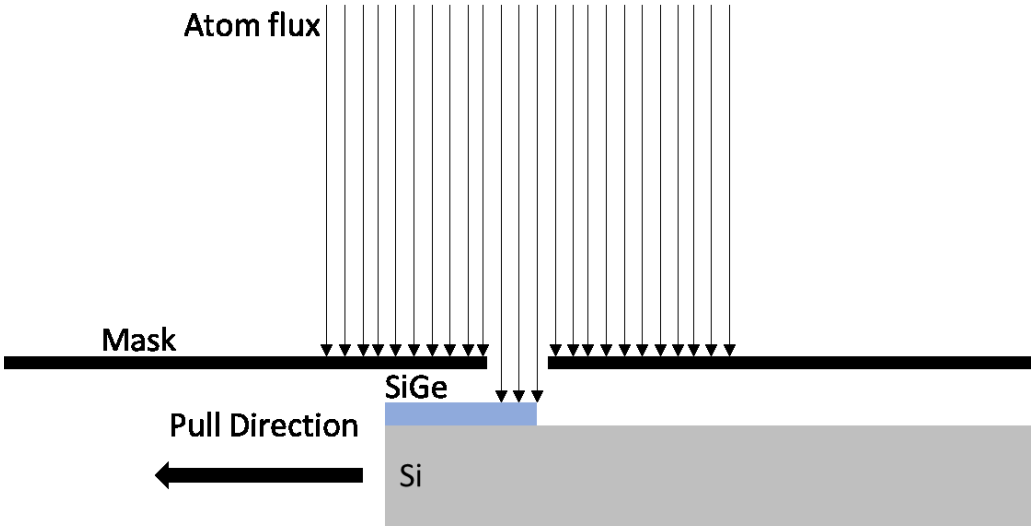


Figure 9-2. Schematic of the traveling-mask set-up.

The lateral growth technique could be a useful technique to provide the energetics of dislocation nucleation, which remains an important topic of argument in heteroepitaxy. To provide useful information on the kinetics, the critical thickness for dislocation nucleation should be determined over a range of compositions. A simple approach to produce films with a thickness variation to filter h_G and h_N is an etch-and-anneal process. First, a pseudomorphic SiGe epilayer is grown on a Si (001) substrate with thickness greater than h_N such that the epilayer is fully strained and free of misfit dislocations. The thickness gradient is produced by vertically dipping narrow strips of the pseudomorphic epilayer into an etchant which etches the SiGe epilayer (Figure 9-3). A stepper motor controls the rate at which the substrate is dipped which controls the thickness gradient by controlling the time that the sample is exposed to the etchant.

The etched epilayer is then annealed to nucleate and glide misfit dislocations, which creates 4 distinct regions (Figure 9-4). In Region 1, where the epilayer is not etched ($h > h_N$), dislocation nucleation and glide are active and an isotropic crosshatch network is formed. In Region 2, the film thickness begins to decrease until it reaches h_N. In this region, the driving force for misfit dislocation nucleation is slowly reduced, which lowers the nucleation rate, as evidenced in the increased dislocation spacing in the [110] direction. In Region 3, the film thickness is less than h_N which inhibits dislocation nucleation, but greater than h_G which allows for dislocation glide. Thus, misfit dislocations which are aligned in the [110] can glide from region 2 into region 3, and there are no misfit dislocations in the $[1\bar{1}0]$ direction. In Region 4, the thickness is below h_G so

dislocation glide is inhibited, no misfit dislocations are expected in this region. By measuring the epilayer thickness at the transition between regions 2 & 3, h_N can be determined. Similarly, h_G can be determined by the thickness at the transition between regions 3 & 4.

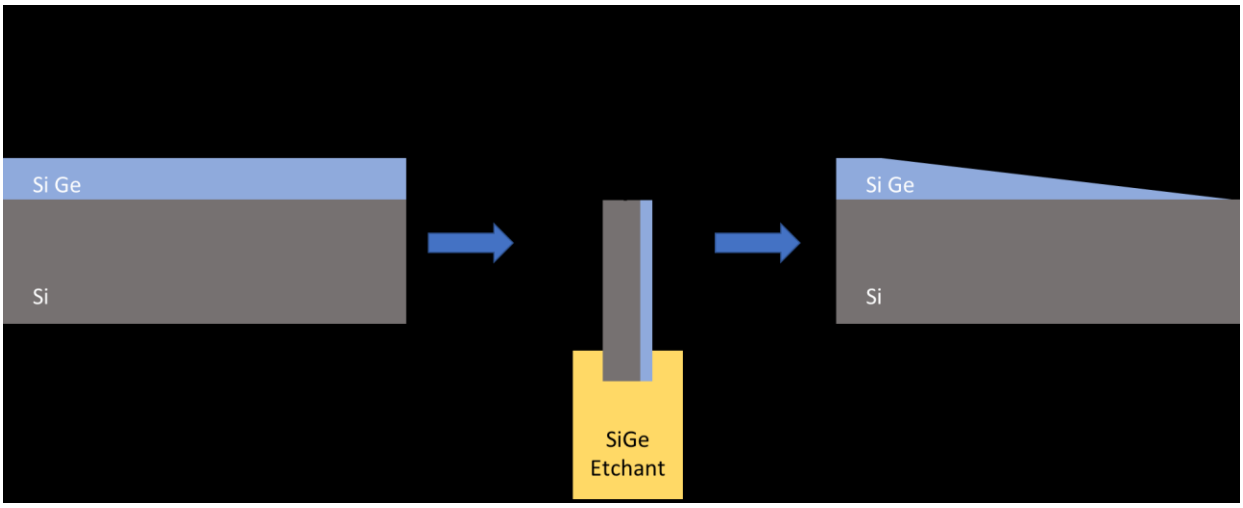


Figure 9-3. Schematic of the etching process to fabricate a pseudomorphic epilayer with a thickness gradient.

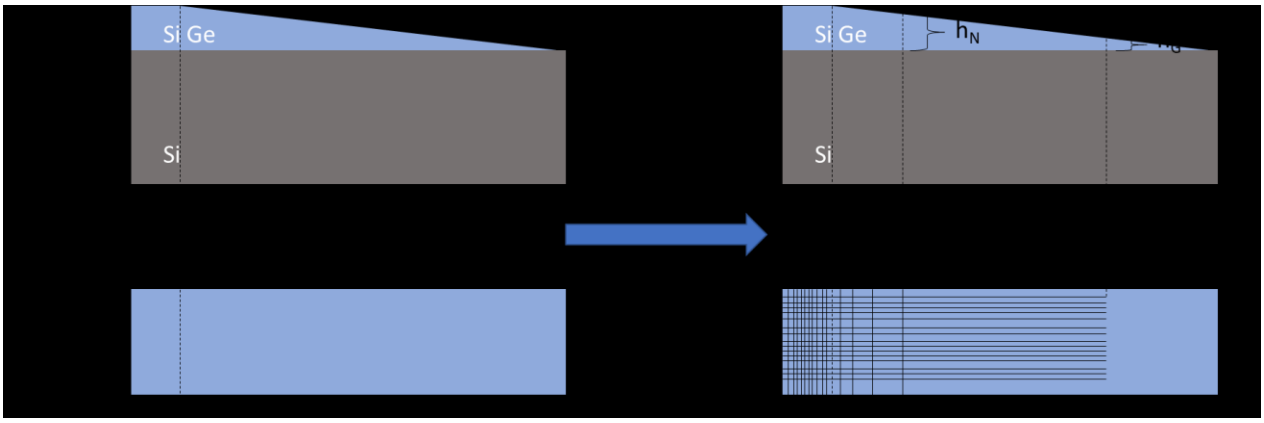


Figure 9-4. Schematic of the annealing step to fabricate a SiGe epilayer with an array of parallel misfit dislocations.

References

1. Thompson, S.E. and S. Parthasarathy, *Moore's law: the future of Si microelectronics.* Materials Today, 2006. **9**(6): p. 20-25.
2. Mac, K.C.A., *Fifty years of Moore's law.* IEEE Transactions on Semiconductor Manufacturing, 2011. **24**(2): p. 202-207.
3. Chu, M., et al., *Strain: A solution for higher carrier mobility in nanoscale mosfets*, in *Annual Review of Materials Research*. 2009. p. 203-229.
4. Rim, K., J.L. Hoyt, and J.F. Gibbons, *Fabrication and analysis of deep submicron strained-Si n-MOSFET's.* IEEE Transactions on Electron Devices, 2000. **47**(7): p. 1406-1415.
5. Kang, E., F.K.A. Hamid, and R. Ismail, *Future of nanoscale strained Si/SixGe1-x Metal-Oxide Semiconductor Field-Effect Transistor for performance metric evaluation: A review.* Journal of Nanoelectronics and Optoelectronics, 2014. **9**(3): p. 317-326.
6. ITRS, *The International Technology Roadmap for Semiconductors - Process Integration, Devices and Structures Summary.* 2013.
7. Chern, W., et al., *Record hole mobility at high vertical fields in planar strained germanium on insulator with asymmetric strain.* IEEE Electron Device Letters, 2014. **35**(3): p. 309-311.
8. Albrecht, M., et al., *Surface ripples, crosshatch pattern, and dislocation formation: Cooperating mechanisms in lattice mismatch relaxation.* Applied Physics Letters, 1995. **67**: p. 1232.
9. Fitzgerald, E.A. and S.B. Samavedam, *Line, point and surface defect morphology of graded, relaxed GeSi alloys on Si substrates.* Thin Solid Films, 1997. **294**(1): p. 3-10.
10. Fitzgerald, E.A. and S.B. Samavedam, *Line, point and surface defect morphology of graded, relaxed GeSi alloys on Si substrates.* Thin Solid Films, 1997. **294**(1-2): p. 3-10.
11. Currie, M.T., et al., *Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing.* Applied Physics Letters, 1998. **72**(14): p. 1718-1720.
12. Bergmann, R., E. Bauser, and J.H. Werner, *Defect-free epitaxial lateral overgrowth of oxidized (111) Si by liquid phase epitaxy.* Applied Physics Letters, 1990. **57**(4): p. 351-353.
13. Hansson, P.O., R. Bergmann, and E. Bauser, *Heteroepitaxial lateral overgrowth of GexSi1−x over SiO2/Si structures by liquid phase epitaxy.* Journal of Crystal Growth, 1991. **114**(4): p. 573-580.
14. Hansson, P.O., et al., *High quality GexSi1-x by heteroepitaxial lateral overgrowth.* Journal of Crystal Growth, 1992. **121**(4): p. 790-794.
15. Fitzgerald, E.A., *Dislocations in strained-layer epitaxy: theory, experiment, and applications.* Materials Science Reports, 1991. **7**(3): p. 87-140.
16. Albrecht, M., et al., *Misfit dislocation formation and interaction in Ge(Si) on Si (001).* Journal of Crystal Growth, 1993. **128**(1-4): p. 327-330.
17. Quitoriano, N.J. and E.A. Fitzgerald, *Alternative slip system activation in lattice-mismatched InP/InGaAs interfaces.* Journal of Applied Physics, 2007. **101**(7): p. 073509-10.
18. Paul, D.J. *Misfit Dislocations*. [cited 2013 January 14]; Available from: http://userweb.eng.gla.ac.uk/douglas.paul/SiGe/misfit.html.
19. Matthews, J.W., S. Mader, and T.B. Light, *Accommodation of Misfit Across the Interface Between Crystals of Semiconducting Elements or Compounds.* Journal of Applied Physics, 1970. **41**(9): p. 3800-3804.
20. Matthews, J.W., A.E. Blakeslee, and S. Mader, *Use of misfit strain to remove dislocations from epitaxial thin films.* Thin Solid Films, 1976. **33**(2): p. 253-266.
21. Matthews, J.W. and A.E. Blakeslee, *Defects in epitaxial multilayers. I. Misfit dislocations.* Journal of Crystal Growth, 1974. **27**(C): p. 118-125.

22. Perovic, D.D., et al., *Heterogeneous nucleation sources in molecular beam epitaxy-grown GexSi1-x/Si strained layer superlattices.* Thin Solid Films, 1989. **183**(1 -2 pt 1): p. 141-156.
23. Fitzgerald, E.A., et al., *Nucleation mechanisms and the elimination of misfit dislocations at mismatched interfaces by reduction in growth area.* Journal of Applied Physics, 1989. **65**(6): p. 2220-2237.
24. Dorsch, W., et al., *Early growth stages of Ge 0.85Si 0.15 on Si(001) from Bi solution.* Surface Science, 1995. **331-333**(PART B): p. 896-901.
25. Füller, T., et al., *Critical thickness of silicon-germanium layers grown by liquid phase epitaxy.* Applied Physics A: Materials Science and Processing, 1999. **69**(6): p. 597-603.
26. Houghton, D.C., *Strain relaxation kinetics in Si1-xGex/Si heterostructures.* Journal of Applied Physics, 1991. **70**(4): p. 2136-2151.
27. Andersen, D. and R. Hull, *Effect of asymmetric strain relaxation on dislocation relaxation processes in heteroepitaxial semiconductors.* Journal of Applied Physics, 2017. **121**(7).
28. Cullis, A.G., et al., *The characteristics of strain-modulated surface undulations formed upon epitaxial Si1−xGex alloy layers on Si.* Journal of Crystal Growth, 1992. **123**(3–4): p. 333-343.
29. Dutartre, D., et al., *Defect-free Stranski-Krastanov growth of strained Si1-xGex layers on Si.* Journal of Crystal Growth, 1994. **142**(1-2): p. 78-86.
30. Fitzgerald, E.A., et al., *Dislocations in Relaxed SiGe/Si Heterostructures.* physica status solidi (a), 1999. **171**(1): p. 227-238.
31. Sawano, K., et al., *In-plane strain fluctuation in strained-Si/SiGe heterostructures.* Applied Physics Letters, 2003. **83**(21): p. 4339-4341.
32. Chen, H., et al., *<title>Crosshatching on a SiGe film grown on a Si(001) substrate studied by Raman mapping and atomic force microscopy</title>.* Physical Review B, 2002. **65**(23): p. 233303.
33. Hartmann, J.M., et al., *Strain-balanced Si/SiGe short period superlattices: Disruption of the surface crosshatch.* Journal of Applied Physics, 1999. **86**(2): p. 845-849.
34. Bauer, M., et al., *Relaxed SiGe buffers with thicknesses below 0.1 μm.* Thin Solid Films, 2000. **369**(1–2): p. 152-156.
35. Hsu, J.W.P., et al., *Surface morphology of related GexSi1−x films.* Applied Physics Letters, 1992. **61**(11): p. 1293-1295.
36. Dorsch, W., et al., *The transition from ripples to islands in strained heteroepitaxial growth under low driving forces.* Journal of Crystal Growth, 1998. **183**(3): p. 305-310.
37. Albrecht, M., et al., *Locally varying chemical potential and growth surface profile: a case study on solution grown Si(Ge)Si.* Journal of Crystal Growth, 1996. **167**(1–2): p. 24-31.
38. Albrecht, M., S. Christiansen, and H.P. Strunk, *The driving force for dislocation multiplication in the substrate of misfitting heteroepitaxial systems.* physica status solidi (a), 1995. **150**(1): p. 453-461.
39. Lutz, M.A., et al., *Influence of misfit dislocations on the surface morphology of Si1−xGex films.* Applied Physics Letters, 1995. **66**(6): p. 724-726.
40. Samavedam, S.B. and E.A. Fitzgerald, *Novel dislocation structure and surface morphology effects in relaxed Ge/Si-Ge(graded)/Si structures.* Journal of Applied Physics, 1997. **81**(7): p. 3108-3116.
41. Fitzgerald, E.A. and S.B. Samavedam, *Line, point and surface defect morphology of graded, relaxed GeSi alloys on Si substrates.* Thin Solid Films, 1997. **294**(1–2): p. 3-10.
42. Mooney, P.M., et al., *Strain relaxation and mosaic structure in relaxed SiGe layers.* Applied Physics Letters, 1993. **62**(26): p. 3464-3466.
43. Leitz, C.W., et al., *Dislocation glide and blocking kinetics in compositionally graded SiGe/Si.* Journal of Applied Physics, 2001. **90**(6): p. 2730-2736.
44. LeGoues, F.K., et al., *Mechanism and conditions for anomalous strain relaxation in graded thin films and superlattices.* Journal of Applied Physics, 1992. **71**(9): p. 4230-4243.

45. Lee, M.L., D.A. Antoniadis, and E.A. Fitzgerald, *Challenges in epitaxial growth of SiGe buffers on Si (111), (110), and (112).* Thin Solid Films, 2006. **508**(1-2): p. 136-139.
46. Fitzgerald, E.A., et al., *Totally relaxed GexSi1-x layers with low threading dislocation densities grown on Si substrates.* Applied Physics Letters, 1991. **59**(7): p. 811-813.
47. Jung, K.H., Y.M. Kim, and D.L. Kwong, *Relaxed GexSi1-x films grown by rapid thermal processing chemical vapor deposition.* Applied Physics Letters, 1990. **56**(18): p. 1775.
48. Lee, M.L., et al., *Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors.* Journal of Applied Physics, 2005. **97**(1): p. 011101.
49. Freund, L.B., *A criterion for arrest of a threading dislocation in a strained epitaxial layer due to an interface misfit dislocation in its path.* Journal of Applied Physics, 1990. **68**(5): p. 2073-2080.
50. Banhart, F., et al., *Dislocation generation in silicon grown laterally over SiO₂ by liquid phase epitaxy.* Applied Physics A: Materials Science & Processing, 1991. **53**(4): p. 317-323.
51. Silier, I., et al., *Solution growth of epitaxial semiconductor-on-insulator layers.* Journal of Crystal Growth, 1996. **166**(1–4): p. 727-730.
52. Mauk, M.G., *Silicon, Germanium and Silicon-Germanium Liquid Phase Epitaxy*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic Materials*. 2007, John Wiley & Sons, Ltd. p. 109-178.
53. Bergmann, R., *Model for defect-free epitaxial lateral overgrowth of Si over SiO2 by liquid phase epitaxy.* Journal of Crystal Growth, 1991. **110**(4): p. 823-834.
54. Bergmann, R., et al., *MOS transistors with epitaxial Si, laterally grown over SiO₂ by liquid phase epitaxy.* Applied Physics A: Materials Science & Processing, 1992. **54**(1): p. 103-105.
55. Banhart, F. and A. Gutjahr, *Stress relaxation in SiGe layers grown on oxide-patterned Si substrates.* Journal of Applied Physics, 1996. **80**(11): p. 6223-6228.
56. Tuppen, C.G., et al., *Misfit dislocation multiplication processes in Si1-xGe x alloys for x<0.15.* Applied Physics Letters, 1990. **56**(1): p. 54-56.
57. Miyao, M., et al., *Giant Ge-on-insulator formation by Si-Ge mixing-triggered liquid-phase epitaxy.* Applied Physics Express, 2009. **2**(4): p. 0455031-0455033.
58. Tanaka, T., et al., *Giant growth of single crystalline Ge on insulator by seeding lateral liquid-phase epitaxy.* Thin Solid Films, 2010. **518**(6 SUPPL. 1): p. S170-S173.
59. Ohta, Y., et al., *Growth-direction-dependent characteristics of Ge-on-insulator by Si-Ge mixing triggered melting growth.* Solid-State Electronics, 2011. **60**(1): p. 18-21.
60. Quitoriano, N.J., W. Wu, and T.I. Kamins, *Guiding vapor-liquid-solid nanowire growth using SiO2.* Nanotechnology, 2009. **20**(14).
61. Quitoriano, N.J., *Lateral, high-quality, metal-catalyzed semiconductor growth on amorphous and lattice-mismatched substrates for photovoltaics.* Applied Physics Letters, 2010. **97**(13).
62. Thompson, S., et al. *A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 um2 SRAM cell*. in *Technical Digest - International Electron Devices Meeting*. 2002.
63. Manasevit, H.M., I.S. Gergis, and A.B. Jones, *Electron mobility enhancement in epitaxial multilayer Si-Si 1-xGex alloy films on (100) Si.* Applied Physics Letters, 1982. **41**(5): p. 464-466.
64. Abstreiter, G., et al., *Strain-induced two-dimensional electron gas in selectively doped Si/SixGe1-x superlattices.* Physical Review Letters, 1985. **54**(22): p. 2441-2444.
65. Schaffler, F., et al., *High-electron-mobility Si/SiGe heterostructures: Influence of the relaxed SiGe buffer layer.* Semiconductor Science and Technology, 1992. **7**(2): p. 260-266.
66. Xie, Y.H., et al., *Very high mobility two-dimensional hole gas in Si/GexSi 1-x/Ge structures grown by molecular beam epitaxy.* Applied Physics Letters, 1993. **63**(16): p. 2263-2264.

67. Lee, M.L., et al., *Strained Si, SiGe, and Ge channels for high-mobility metal-oxide- semiconductor field-effect transistors.* Journal of Applied Physics, 2005. **97**(1).
68. Fischetti, M.V., et al., *Six-band k·p calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain, and silicon thickness.* Journal of Applied Physics, 2003. **94**(2): p. 1079-1095.
69. Sun, Y., S.E. Thompson, and T. Nishida, *Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors.* Journal of Applied Physics, 2007. **101**(10).
70. Sun, G., et al., *Hole mobility in silicon inversion layers: Stress and surface orientation.* Journal of Applied Physics, 2007. **102**(8).
71. Thompson, S.E., et al. *Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs*. in *Technical Digest - International Electron Devices Meeting, IEDM*. 2004.
72. Thompson, S.E., et al., *Uniaxial-process-induced strained-Si: extending the CMOS roadmap.* Electron Devices, IEEE Transactions on, 2006. **53**(5): p. 1010-1020.
73. Fossum, J.G. and W. Zhang, *Performance projections of scaled CMOS devices and circuits with strained Si-on-SiGe channels.* IEEE Transactions on Electron Devices, 2003. **50**(4): p. 1042-1049.
74. Ito, S., et al. *Mechanical stress effect of etch-stop nitride and its impact on deep submicron transistor design*. in *Technical Digest - International Electron Devices Meeting*. 2000.
75. Shimizu, A., et al. *Local mechanical-stress control (LMC): A new technique for CMOS-performance enhancement*. in *Technical Digest - International Electron Devices Meeting*. 2001.
76. Thompson, S.E., et al., *A logic nanotechnology featuring strained-silicon.* IEEE Electron Device Letters, 2004. **25**(4): p. 191-193.
77. NSM. *Silicon - Band structure and carrier concentration*. 19/12/2015]; Available from: http://www.ioffe.ru/SVA/NSM/Semicond/Si/bandstr.html#Masses.
78. NSM. *Germanium - Band structure and carrier concentration*. 12/19/2015]; Available from: http://www.ioffe.ru/SVA/NSM/Semicond/Ge/bandstr.html#Masses.
79. Lander, R.J.P., et al., *On the low-temperature mobility of holes in gated oxide Si/SiGe heterostructures.* Semiconductor Science and Technology, 1997. **12**(9): p. 1064-1071.
80. Diem, B., et al., *SOI 'SIMOX'; from bulk to surface micromachining, a new age for silicon sensors and actuators.* Sensors and Actuators: A. Physical, 1995. **46**(1-3): p. 8-16.
81. *Method of fabricating SOI substrate*, U.P. Office, Editor. 1999, Atsushi Ogura: USA.
82. Powell, A.R., S.S. Iyer, and F.K. Legoues, *New approach to the growth of low dislocation relaxed SiGe material.* Applied Physics Letters, 1994. **64**(14): p. 1856-1858.
83. Mizuno, T., et al., *Electron and hole mobility enhancement in strained-Si MOSFET's on SiGe-on-insulator substrates fabricated by SIMOX technology.* Electron Device Letters, IEEE, 2000. **21**(5): p. 230-232.
84. Fukatsu, S., et al., *SiGe-based semiconductor-on-insulator substrate created by low-energy separation-by-implanted-oxygen.* Applied Physics Letters, 1998. **72**(26): p. 3485-3487.
85. Prabhakaran, K., et al., *Bonding partner change reaction in oxidation of Ge on Si(001): Observation of two step formation of SiO2.* Applied Physics Letters, 1994. **64**(14): p. 1839-1841.
86. Langdo, T.A., et al., *SiGe-free strained Si on insulator by wafer bonding and layer transfer.* Applied Physics Letters, 2003. **82**(24): p. 4256-4258.
87. Liu, W.S., et al., *Wet oxidation of GeSi at 700°C.* Journal of Applied Physics, 1992. **71**(8): p. 4015-4018.
88. Gomez, L., M. Canonico, and M. Kim, *Fabrication of Strained-Si/Strained-Ge Heterostructures on Insulator.* Journal of Electronic Materials, 2008. **37**(3): p. 240-244.

89. Irisawa, T., et al., *High-performance uniaxially strained SiGe-on-insulator pMOSFETs fabricated by lateral-strain-relaxation technique.* IEEE Transactions on Electron Devices, 2006. **53**(11): p. 2809-2815.
90. Irisawa, T., et al., *Device design and electron transport properties of uniaxially strained-SOI tri-gate nMOSFETs.* IEEE Transactions on Electron Devices, 2008. **55**(2): p. 649-654.
91. Uhm, J., M. Sakuraba, and J. Murota, *Strain relaxation by stripe patterning in Si/Si1 − xGex/Si(100) heterostructures.* Thin Solid Films, 2006. **508**(1–2): p. 239-242.
92. Uhm, J., M. Sakuraba, and J. Murota, *Local strain in Si/Si0.6Ge0.4/Si(100) heterostructures by stripe-shape patterning.* Thin Solid Films, 2008. **517**(1): p. 300-302.
93. Uhm, J., M. Sakuraba, and J. Murota, *Strain control and electrical properties of stripe-patterned Si/Si 1-xGex/Si(1 0 0) heterostructures.* Semiconductor Science and Technology, 2007. **22**(1): p. S33-S37.
94. Murota, J., J. Uhm, and M. Sakuraba. *Strain control of Si and Si1-xGex layers in the Si/Si1-xGex/Si heterostructures by stripe-shape patterning for future Si-based devices*. in *ECS Transactions*. 2007.
95. Hashemi, P., et al., *Asymmetric strain in nanoscale patterned strained-Si/strained-Ge/strained- Si heterostructures on insulator.* Applied Physics Letters, 2007. **91**(8).
96. Hashemi, P. and J.L. Hoyt, *High hole-mobility strained-Ge/Si 0.6Ge 0.4 P-MOSFETs with high-κ/metal gate: Role of strained-Si cap thickness.* IEEE Electron Device Letters, 2012. **33**(2): p. 173-175.
97. Bedell, S.W., et al., *Mobility scaling in short-channel length strained Ge-on-insulator P-MOSFETs.* IEEE Electron Device Letters, 2008. **29**(7): p. 811-813.
98. Nicholas, G., et al., *High mobility strained Ge pMOSFETs with high-κ metal gate.* IEEE Electron Device Letters, 2007. **28**(9): p. 825-827.
99. Holländer, B., et al., *Enhanced strain relaxation of epitaxial SiGe layers on Si(1 0 0) after H+ ion implantation.* Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 1999. **148**(1–4): p. 200-205.
100. Kentarou, S., et al., *Introduction of Uniaxial Strain into Si/Ge Heterostructures by Selective Ion Implantation.* Applied Physics Express, 2008. **1**(12): p. 121401.
101. Hoshi, Y., et al., *Line width dependence of anisotropic strain state in sige films induced by selective ion implantation.* Applied Physics Express, 2011. **4**(9).
102. Sawano, K., et al., *On the origin of the uniaxial strain induced in Si/Ge heterostructures with selective ion implantation technique.* Journal of Crystal Growth, 2013. **378**: p. 251-253.
103. Sawano, K., et al., *Uniaxially strained SiGe(111) and SiGe(100) grown on selectively ion-implanted substrates.* Journal of Crystal Growth, 2014. **401**: p. 758-761.
104. Feste, S.F., et al., *Fabrication of uniaxially strained silicon nanowires.* Thin Solid Films, 2008. **517**(1): p. 320-322.
105. Feste, S.F., et al., *Silicon nanowire FETs with uniaxial tensile strain.* Solid-State Electronics, 2009. **53**(12): p. 1257-1262.
106. Zhang, L., et al., *Uniaxial strain effects on electron ballistic transport in gate-all-around silicon nanowire mosfets.* IEEE Transactions on Electron Devices, 2011. **58**(11): p. 3829-3836.
107. Najmzadeh, M., et al., *Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs.* Microelectronic Engineering, 2010. **87**(5–8): p. 1561-1565.
108. Najmzadeh, M., et al., *Investigation of oxidation-induced strain in a top-down Si nanowire platform.* Microelectronic Engineering, 2009. **86**(7–9): p. 1961-1964.
109. Singh, N., et al., *Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High-κ/Metal-Gate Device Structures.* Electron Device Letters, IEEE, 2007. **28**(7): p. 558-561.
110. Hull, R., et al., *Growth of GexSi1-x alloys on Si(110) surfaces.* Applied Physics Letters, 1991. **59**(8): p. 964-966.

111. Minamisawa, R.A., et al., *Uniaxial strain relaxation in He+ ion implanted (110) oriented SiGe layers.* Applied Physics Letters, 2009. **95**(3): p. 034102.
112. Elfving, A., et al., *Asymmetric relaxation of SiGe/Si(110) investigated by high-resolution x-ray diffraction reciprocal space mapping.* Applied Physics Letters, 2006. **89**(18).
113. Nelson, H., *Epitaxial Growth from the Liquid State and Its application to the Fabrication of Tunnel and Laser Diodes.* RCA Review, 1963. **24**.
114. Nelson, H., *Liquid-phase epitaxy—its role in crystal growth technology.* Journal of Crystal Growth, 1974. **27**(0): p. 1-5.
115. Trah, H.P., *Liquid phase epitaxy in the ternary system Si-Ge-Bi.* Journal of Crystal Growth, 1990. **102**(1-2): p. 175-182.
116. Hansson, P.O., et al., *Interfacial energies providing a driving force for Ge/Si heteroepitaxy.* Physical Review Letters, 1994. **73**(3): p. 444-447.
117. Scheel, H.J., *Introduction to Liquid Phase Epitaxy*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic Materials*. 2007, John Wiley & Sons, Ltd. p. 1-19.
118. Kuphal, E., *Liquid phase epitaxy.* Applied Physics A Solids and Surfaces, 1991. **52**(6): p. 380-409.
119. Rupprecht, H., J.M. Woodall, and G.D. Pettit, *Efficient visible electroluminescence at 300°K from Ga 1-xAlxAs p-n junctions grown by liquid-phase epitaxy.* Applied Physics Letters, 1967. **11**(3): p. 81-83.
120. Alferov, Z., *Double heterostructure lasers: early days and future perspectives.* Selected Topics in Quantum Electronics, IEEE Journal of, 2000. **6**(6): p. 832-840.
121. Panish, M.B., I. Hayashi, and S. Sumski, *Double-heterostructure injection lasers with room-temperature thresholds as low as 2300 A/cm2.* Applied Physics Letters, 1970. **16**(8): p. 326-327.
122. Mauk, M.G. and J.B. McNeely, *Equipment and Instrumentation for Liquid Phase Epitaxy*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic Materials*. 2007, John Wiley & Sons, Ltd. p. 85-108.
123. Bauser, E., et al., *Substrate orientation and surface morphology of GaAs liquid phase epitaxial layers.* Journal of Crystal Growth, 1974. **27**(C): p. 148-153.
124. Kaufmann, L.M.F. and K. Heime, *A new graphite boat construction for the LPE growth of thin GaAs layers with a new technique.* Journal of Crystal Growth, 1977. **42**(C): p. 321-327.
125. Alonso, M.I. and E. Bauser, *Growth of Si[sub 1 - x]Ge[sub x] on silicon by liquid-phase epitaxy.* Journal of Applied Physics, 1987. **62**(11): p. 4445-4449.
126. Gutjahr, A., et al. *SiGe layer structures for solar cell application grown by liquid phase epitaxy*. in *Photovoltaic Specialists Conference, 1997., Conference Record of the Twenty-Sixth IEEE*. 1997.
127. Pohl, U., *Methods of Epitaxy*, in *Epitaxy of Semiconductors*. 2013, Springer Berlin Heidelberg. p. 275-313.
128. Herman, M.A., W. Richter, and H. Sitter, *Epitaxy : physical principles and technical implementation*. 2004, Berlin; New York: Springer.
129. Holmes, D.E. and G.S. Kamath, *Growth of InP by infinite solution LPE.* Journal of Crystal Growth, 1981. **54**(1): p. 51-58.
130. Dutt, B.V., R.A. Ludwig, and F. Ermanis, *The origin and elimination of Si pyramids in (Ga, Al)As: Si LEDs.* Journal of Crystal Growth, 1983. **62**(1): p. 21-26.
131. Wilson, R.B., P. Besomi, and R.J. Nelson, *INVESTIGATION OF MELT CARRY-OVER DURING LIQUID PHASE EPITAXY.* Journal of The Electrochemical Society, 1985. **132**(1): p. 172-176.
132. Besomi, P., R.B. Wilson, and R.J. Nelson, *INVESTIGATION OF MELT CARRY-OVER DURING LIQUID PHASE EPITAXY - II. GROWTH OF INDIUM GALLIUM ARSENIC PHOSPHIDE DOUBLE HETEROSTRUCTURE MATERIAL LATTICE-MATCHED TO INDIUM PHOSPHIDE.* Journal of The Electrochemical Society, 1985. **132**(1): p. 176-179.

133. Astles, M.G., H. Hill, and V.W. Steward, *An experimental investigation of edge-growth effects in the LPE growth of GaAs and GaAlAs.* Journal of Crystal Growth, 1983. **62**(1): p. 61-66.
134. Tamargo, M.C., C.L. Reynolds Jr, and R.I. Kunkel, *Thermal effects on LPE layer thickness.* Journal of Crystal Growth, 1985. **71**(2): p. 421-426.
135. Becher, S., et al., *Characterization of lattice-matched single In1-xGaxAsyP1-y quantum wells grown by conventional liquid phase epitaxy.* Semiconductor Science and Technology, 1994. **9**(8): p. 1558-1563.
136. Alferov, Z.I.G., D. Z.; Arsent'ev, I. N.; Ber, B. Ya.; Vavilova, L. S.; Krasovskii, V. V.; Chudinov, A. V., *Auger profiles of composition and luminescence studies of liquid-phase-grown InGaAsP heterostuctures with (1.5-5)x10-6 cm active regions.* Soviet Physics: Semiconductors, 1985. **19**(6): p. 679-683.
137. Rezek, E.A., et al., *Thin-layer liquid phase epitaxy of InGaPAs heterostructures in short intervals (< 100 ms): Non-diffusion-limited crystal growth.* Journal of Electronic Materials, 1981. **10**(1): p. 255-285.
138. Bantien, F., K. Kelting, and E. Bauser, *Liquid phase epitaxy of GaAs quantum well structures.* Journal of Crystal Growth, 1987. **85**(1–2): p. 194-198.
139. Benchimol, J.L., et al., *InGaAsP superlattices grown by liquid-phase epitaxy.* Journal of Applied Physics, 1986. **59**(12): p. 4068-4072.
140. Krier, A. and X.L. Huang, *Mid-infrared electroluminescence from InAsSb quantum dot light emitting diodes grown by liquid phase epitaxy.* Physica E: Low-dimensional Systems and Nanostructures, 2002. **15**(3): p. 159-163.
141. Krier, A., X.L. Huang, and Z. Labadi, *Liquid Phase Epitaxy of Quantum Wells and Quantum Dots*, in *Liquid Phase Epitaxy of Electronic, Optical and Optoelectronic Materials*. 2007, John Wiley & Sons, Ltd. p. 227-257.
142. Traeger, G., E. Kuphal, and K.H. Zschauer, *Diffusion-limited LPE growth of mixed crystals: Application to In1-xGaxAs on InP.* Journal of Crystal Growth, 1988. **88**(2): p. 205-214.
143. Garbuzov, D.Z., et al., *On the peculiarities of the short-time (tg < 10 ms) solid solution LPE growth onto the moving substrate.* Journal of Crystal Growth, 1991. **110**(4): p. 955-959.
144. Olchowik, J.M., et al., *Analysis of ambient gas influence on silicon layers crystallized by means of LPE.* Journal of Non-Crystalline Solids, 2008. **354**(35-39): p. 4423-4425.
145. Jozwik, I. and J.M. Olchowik, *The epitaxial lateral overgrowth of silicon by two-step liquid phase epitaxy.* Journal of Crystal Growth, 2006. **294**(2): p. 367-372.
146. Bergmann, R. and J. Kurianski, *The role of hydrogen in silicon liquid phase epitaxy.* Materials Letters, 1993. **17**(3-4): p. 137-140.
147. Hanke, M., et al., *Size, shape, and ordering of SiGe/Si(001) islands grown by means of liquid phase epitaxy under far-nonequilibrium growth conditions.* Applied Physics Letters, 2005. **86**(14): p. 1-3.
148. Keck, P.H. and J. Broder, *The solubility of silicon and germanium in gallium and indium.* Physical Review, 1953. **90**(4): p. 521-522.
149. Carman, J.N., P.E. Stello, and C.A. Bittmann, *Regrowth of silicon through a low melting zone of silicon-gold eutectic [4].* Journal of Applied Physics, 1954. **25**(4): p. 543.
150. Donnelly, J.P.M., A. G., *The Epitaxial Growth of Ge on Si by Solution Growth Techniques.* Journal of The Electrochemical Society, 1966. **113**(3): p. 297-298.
151. Dost, S. and B. Lent, *Chapter 2 - Fundamentals and phase changes*, in *Single Crystal Growth of Semiconductors from Metallic Solutions*, S.D. Lent, Editor. 2007, Elsevier: Amsterdam. p. 15-25.
152. Hansson, P.O., et al., *Liquid-phase epitaxy and characterization of Si1-xGex layers on Si substrates.* Journal of Applied Physics, 1990. **68**(5): p. 2158-2163.
153. Weber, J. and M.I. Alonso, *Near-band-gap photoluminescence of Si-Ge alloys.* Physical Review B, 1989. **40**(8): p. 5683-5693.

154. Lyutovich, A.S., et al., *Radiative Recombination at Centres in Germanium–Silicon Solid Solutions.* physica status solidi (b), 1985. **129**(1): p. 313-320.
155. Mitchard, G.S. and T.C. McGill, *Photoluminescence of Si-rich Si-Ge alloys.* Physical Review B, 1982. **25**(8): p. 5351-5363.
156. Sukegawa, T., M. Kimura, and A. Tanaka, *Gravity effect on dissolution and growth of silicon in the In-Si system.* Journal of Crystal Growth, 1988. **92**(1-2): p. 46-52.
157. Sukegawa, T., et al., *Growth of GeSi thick alloy layers by the yo-yo solute feeding method.* Journal of Crystal Growth, 1990. **99**(1–4): p. 274-277.
158. Sukegawa, T., et al., *Growth of a GeSi thick alloy layer on a Si substrate by liquid phase epitaxy.* Journal of Crystal Growth, 1991. **109**(1–4): p. 186-190.
159. Hartman, P. and W.G. Perdok, *On the relations between structure and morphology of crystals. I.* Acta Crystallographica, 1955. **8**(1): p. 49-52.
160. Bauer, E. and J. van der Merwe, *Structure and growth of crystalline superlattices: From monolayer to superlattice.* Physical Review B, 1986. **33**(6): p. 3657-3671.
161. Frank, F.C. and J.H. van der Merwe, *One-Dimensional Dislocations. II. Misfitting Monolayers and Oriented Overgrowth*. Vol. 198. 1949. 216-225.
162. Marée, P.M.J., et al., *Thin epitaxial Ge–Si(111) films: Study and control of morphology.* Surface Science, 1987. **191**(3): p. 305-328.
163. Christiansen, S., et al., *Reduced effective misfit in laterally limited structures such as epitaxial islands.* Applied Physics Letters, 1995. **66**(5): p. 574-576.
164. Hansson, P.O., et al., *Dimensionality and critical sizes of GeSi on Si(100).* Thin Solid Films, 1992. **216**(2): p. 199-202.
165. Schade, M., et al., *Investigation of the chemical composition profile of SiGe⁄Si(001) islands by analytical transmission electron microscopy.* Applied Physics Letters, 2007. **90**(26): p. -.
166. Dorsch, W., et al., *Strain-induced island scaling during Si1-xGex heteroepitaxy.* Applied Physics Letters, 1998. **72**(2): p. 179-181.
167. Aqua, J.N., et al., *Growth and self-organization of SiGe nanostructures.* Physics Reports, 2013. **522**(2): p. 59-189.
168. Schmidbauer, M., et al., *Ordering of self-assembled Si_{1-x}Ge_{x} islands studied by grazing incidence small-angle x-ray scattering and atomic force microscopy.* Physical Review B, 1998. **58**(16): p. 10523-10531.
169. Hanke, M., et al., *Island chain formation during liquid phase epitaxy of SiGe on silicon.* Applied Physics Letters, 2003. **83**(24): p. 4927-4929.
170. Hanke, M., et al., *SiGe/Si(001) Stranski-Krastanow islands by liquid-phase epitaxy: Diffuse x-ray scattering versus growth observations.* Physical Review B - Condensed Matter and Materials Physics, 2004. **69**(7): p. 753171-753177.
171. Denker, U., et al., *Trench formation around and between self-assembled Ge islands on Si.* Applied Physics Letters, 2001. **78**(23): p. 3723-3725.
172. Liao, X., et al., *Transmission-electron microscopy study of the shape of buried quantum dots.* Physical Review B, 1998. **58**(8): p. R4235-R4237.
173. Meixner, M., et al., *Formation of island chains in SiGe/Si heteroepitaxy by elastic anisotropy.* Physical Review B - Condensed Matter and Materials Physics, 2001. **64**(24): p. 2453071-2453074.
174. Chen, J.X., et al., *Liquid phase epitaxy of GeSi on {111} Si substrates: lattice defect structure and electronic properties.* Journal of Crystal Growth, 1992. **118**(3–4): p. 452-460.
175. Matthews, J.W., *DEFECTS ASSOCIATED WITH THE ACCOMMODATION OF MISFIT BETWEEN CRYSTALS.* J Vac Sci Technol, 1974. **12**(1): p. 126-133.
176. Albrecht, M., et al., *Dislocation glide in {110} planes in semiconductors with diamond or zinc-blende structure.* Applied Physics Letters, 1993. **62**(18): p. 2206-2208.

177. Mercer, J.L. and M.Y. Chou, *Energetics of the Si(111) and Ge(111) surfaces and the effect of strain.* Physical Review B, 1993. **48**(8): p. 5374-5385.
178. Kotulak, N.A., et al., *Toward a tandem gallium phosphide on silicon solar cell through liquid phase epitaxy growth.* Thin Solid Films, 2014. **556**: p. 236-240.
179. Ernst, F., P. Pirouz, and E. Bauser, *Lattice mismatch accommodation at GeSi/{111}Si interfaces grown by liquid phase epitaxy.* physica status solidi (a), 1992. **131**(2): p. 651-662.
180. Ernst, F., *Interface dislocations forming during epitaxial growth of GeSi on (111) Si substrates at high temperatures.* Materials Science and Engineering: A, 1997. **233**(1–2): p. 126-138.
181. Sembian, A.M., et al. *Surface morphology of LPE SiGe layers grown on (100) Si substrates*. in *Materials Research Society Symposium - Proceedings*. 1998.
182. Sembian, A.M., et al., *Defect distribution and morphology development of SiGe layers grown on Si(100) substrates by LPE.* Thin Solid Films, 1998. **336**(1-2): p. 116-119.
183. Sembian, A.M., et al., *Influence of cooling rate on the dislocations and related luminescence in LPE SiGe layers grown on Si (100) substrates.* Thin Solid Films, 2000. **372**(1–2): p. 1-5.
184. Fitzgerald, E.A., et al., *Totally relaxed GexSi1−x layers with low threading dislocation densities grown on Si substrates.* Applied Physics Letters, 1991. **59**(7): p. 811-813.
185. Shiryaev, S.Y., et al., *Nanoscale Structuring by Misfit Dislocations in ${\mathrm{Si}}_{1-\mathit{x}}{\mathrm{Ge}}_{\mathit{x}}/Si$ Epitaxial Systems.* Physical Review Letters, 1997. **78**(3): p. 503-506.
186. Pohl, U., *Structural Properties of Heterostructures*, in *Epitaxy of Semiconductors*. 2013, Springer Berlin Heidelberg. p. 11-77.
187. Cullity, B.D., *Elements of x-ray diffraction*. 1978, Reading, Mass.: Addison-Wesley Pub. Co.
188. Ferrari, C. and C. Bocchi, *Strain and composition determination in semiconducting heterostructures by high-resolution x-ray diffraction*, in *Characterization of Semiconductor Heterostructures and Nanostructures*. 2008. p. 93-132.
189. Bauer, G., J. Li, and E. Koppensteiner, *X-ray reciprocal space mapping of Si Si1-xGex heterostructures.* Journal of Crystal Growth, 1995. **157**(1-4): p. 61-67.
190. Leitz, C.W. and M.T. Bulsara, *Guide to Reciprocal Space Mapping*.
191. van der Sluis, P., *Determination of strain in epitaxial semiconductor structures by high-resolution X-ray diffraction.* Applied Physics A Solids and Surfaces, 1994. **58**(3): p. 129-134.
192. Matney, K.M. and M.S. Goorsky. *New approach for determining epilayer strain relaxation and composition through high resolution x-ray diffraction*. in *Materials Research Society Symposium - Proceedings*. 1995.
193. Chen, X., et al., *Large Area and Depth-Profiling Dislocation Imaging and Strain Analysis in Si/SiGe/Si Heterostructures.* Microscopy and Microanalysis, 2014. **20**(05): p. 1521-1527.
194. Shah, V.A., et al., *Reverse graded strain relaxed SiGe buffers for CMOS and optoelectronic integration.* Thin Solid Films, 2012. **520**(8): p. 3227-3231.
195. Franco, N., et al., *XRD analysis of strained Ge-SiGe heterostructures on relaxed SiGe graded buffers grown by hybrid epitaxy on Si(0 0 1) substrates.* Materials Science and Engineering B: Solid-State Materials for Advanced Technology, 2005. **124-125**(SUPPL.): p. 123-126.
196. Dommann, A. and A. Neels, *The role of strain in new semiconductor devices.* Advanced Engineering Materials, 2009. **11**(4): p. 275-277.
197. Jang, J.H., et al., *Structural characterization of strained silicon grown on a SiGe buffer layer.* Semiconductor Science and Technology, 2008. **23**(3).
198. Yousif, M.Y.A., et al., *Direct assessment of relaxation and defect propagation in different as-grown and in situ post-growth annealed thin Ge/Si and step-graded Si1-xGex/Si buffer layers.* Solid-State Electronics, 2001. **45**(11): p. 1869-1874.

199. Goldstein, J.I., et al., *Electron Beam–Specimen Interactions*, in *Scanning Electron Microscopy and X-ray Microanalysis: Third Edition*. 2003, Springer US: Boston, MA. p. 61-98.
200. Jenkins, M.W., *A New Preferential Etch for Defects in Silicon Crystals.* Journal of the Electrochemical Society, 1977. **124**(5): p. 757-762.
201. Abbadie, A., J.M. Hartmann, and F. Brunier. *A review of different and promising defect etching techniques: From Si to Ge*. in *ECS Transactions*. 2007.
202. Schimmel, D.G., *Defect Etch for <100> Silicon Evaluation.* Journal of the Electrochemical Society, 1979. **126**(3): p. 479-483.
203. O'Reilly, A.J. and N. Quitoriano, *Asymmetric, compressive, SiGe epilayers on Si grown by lateral liquid-phase epitaxy utilizing a distinction between dislocation nucleation and glide critical thicknesses.* Journal of Crystal Growth, 2018. **482**: p. 15-22.
204. Zoellner, M.H., et al., *Imaging Structure and Composition Homogeneity of 300 mm SiGe Virtual Substrates for Advanced CMOS Applications by Scanning X-ray Diffraction Microscopy.* ACS Applied Materials & Interfaces, 2015. **7**(17): p. 9031-9037.
205. Ferrari, C., G. Rossetto, and E.A. Fitzgerald, *Misfit dislocation and threading dislocation distributions in InGaAs and GeSi/Si partially relaxed heterostructures.* Materials Science and Engineering: B, 2002. **91-92**(Supplement C): p. 437-440.

Appendix A – Stepper Motor Control Code

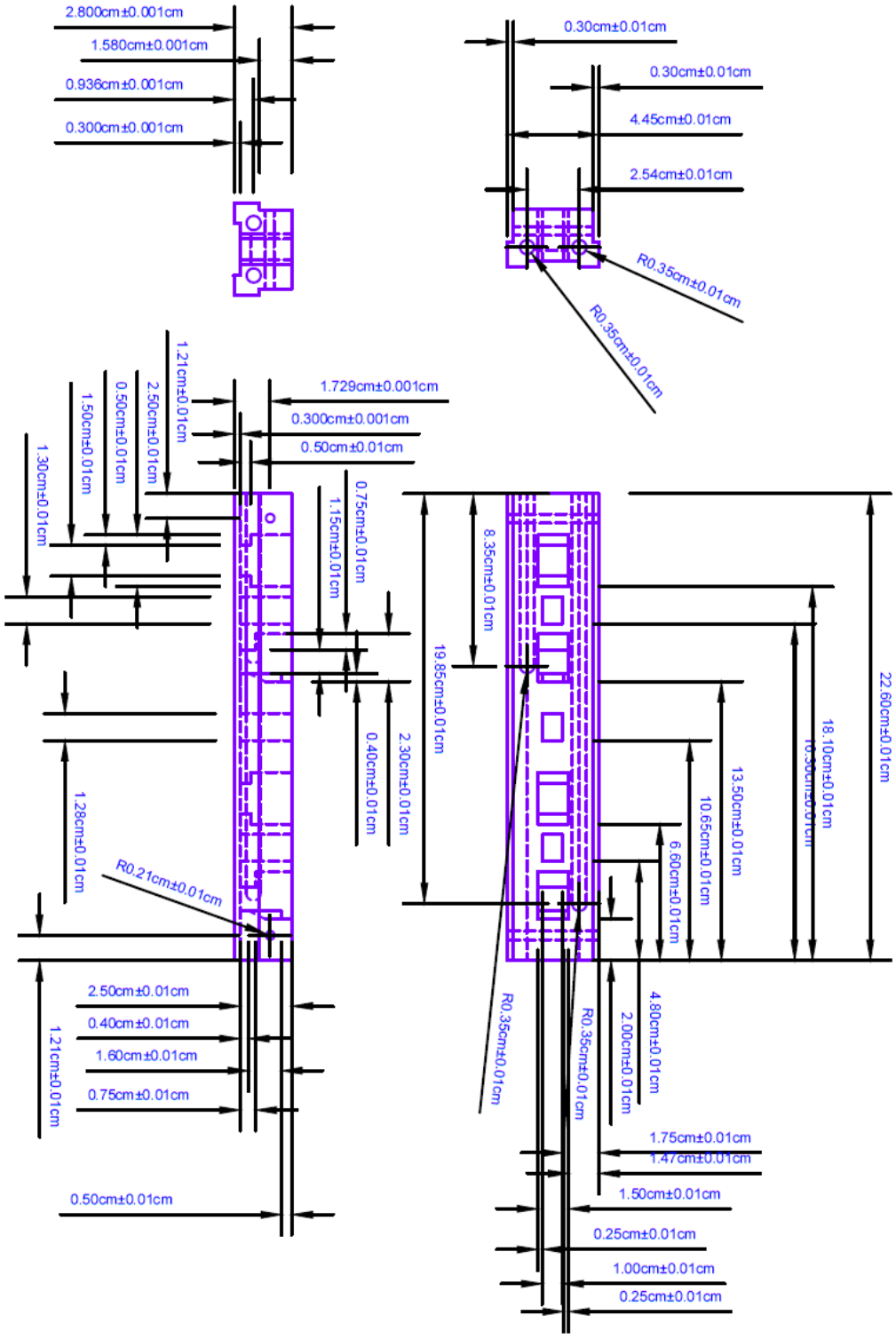
```
//***********************
//Displacement Variables

float distmm=60;//Distance in mm
float timeM=120;// in mins
boolean left=false;
//***********************
//Time variables

float timeS;
float timeMS;
float timeUS;

//diplacement feedback
float stepCount;
float stepCal;

//Pulse and control variables
float lastTime;
float speedmm;
float period;
float ratio=12;
float steps=1600;
float beginTime;
int pul= 2;
int dir=3;
int en=4;
int enableControl=5;
boolean done=false;
float totalTime;
float presentTime;

void periodCal(){
  speedmm=distmm/timeUS;
   period =pow((speedmm*steps*ratio),-1);
   //Serial.print("period: ");
   //Serial.println(period,6);
 }
 void pulse(){
  digitalWrite(pul,HIGH);
  //delayMicroseconds(5);
```

```
  digitalWrite(pul,LOW);

 }
 void timeCal(){
  timeS=timeM*60.0000;
  timeMS=timeS*1000.00000;
  timeUS=timeMS*1000.00000;
  //Serial.print("timeUS: ");
  //Serial.println(timeUS);
 }
 void stepCalculate(float distancemm){

  stepCal=distancemm*steps*ratio;
  //Serial.print("stepCal: ");
  //Serial.println(stepCal);
  stepCount=0;
   }

void setup(){
   Serial.begin(9600);
   pinMode(pul, OUTPUT);
   pinMode(dir, OUTPUT);
   pinMode(en, OUTPUT);
   pinMode(enableControl,INPUT);
   timeCal();
   stepCalculate(distmm);
   periodCal();
     if(left){
   digitalWrite(dir, LOW);
    }else{digitalWrite(dir,HIGH);
        }
    digitalWrite(en,HIGH);
    lastTime=micros();

    Serial.println("Type 'go' to begin");
  while(!Serial.find("go"));
  beginTime=millis();
   }

 void loop(){
     presentTime=micros();
     if((presentTime-
lastTime)>period&&digitalRead(enableControl)==HIGH&&!done||presentTime-lastTime<0){
          lastTime=presentTime;
```

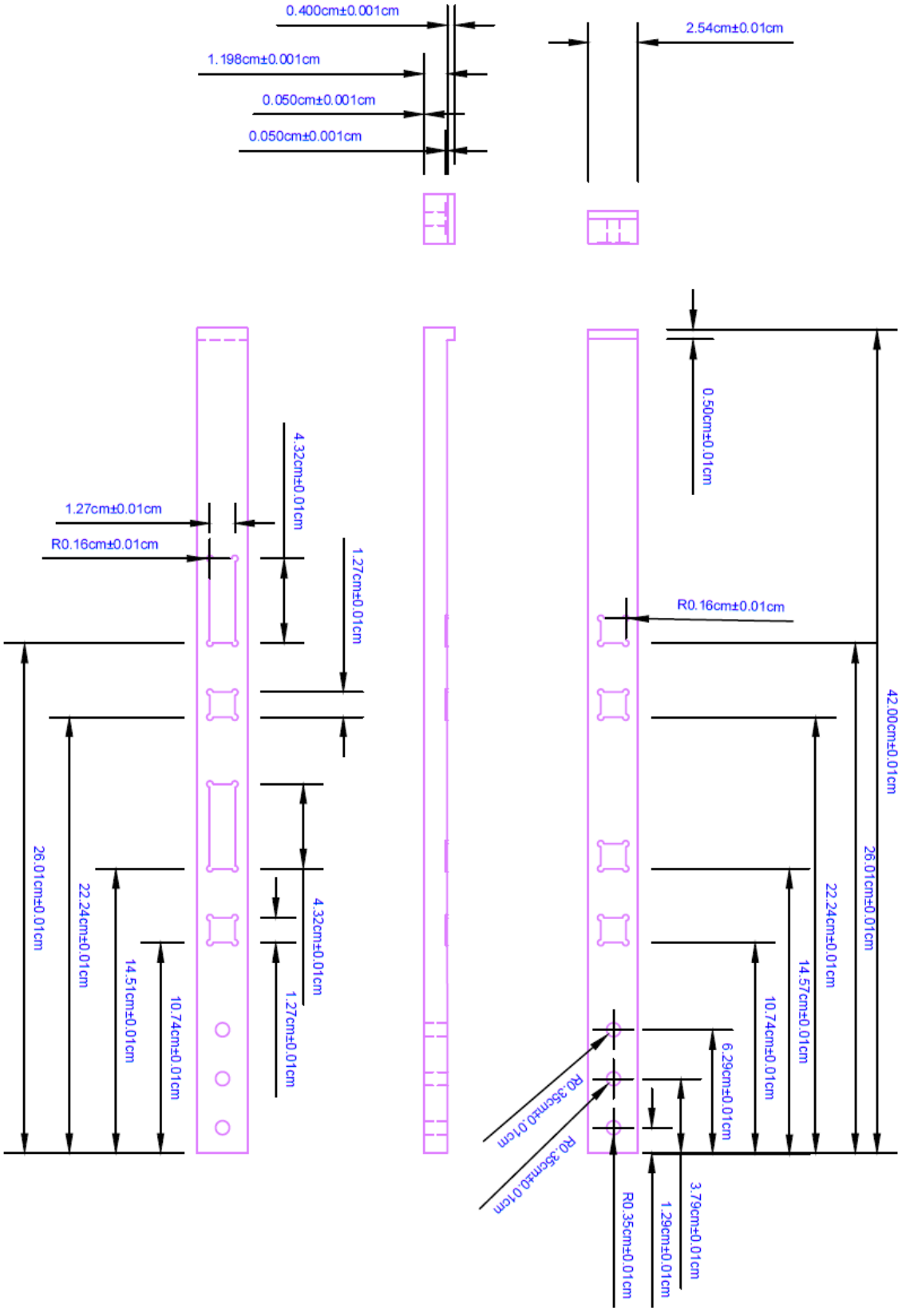
```
        stepCount++;
        pulse();
       }
    if(stepCount>=stepCal&&!done){
        done=true;
        totalTime= (millis()-beginTime)/60000;
        Serial.println("Final Report");
        Serial.print("stepCal: ");
        Serial.println(stepCal);
        Serial.print("stepCount: ");
        Serial.println(stepCount);
        Serial.print("speed(mm/min: ");
        Serial.println(speedmm*60000000);
        Serial.print("period: ");
        Serial.println(period);
        Serial.print("totalTime: ");
        Serial.println(totalTime);
       }
      //Serial.println("loop");
}
```

Appendix B – Graphite Boat Technical Drawings

Well-Block drawings



Graphite Slider Drawings



Graphite Assembly Drawings