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Transceiver Arrays for Optically Interconnected Electronic Systems

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A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfilment of the requirements of the degree of Doctor of Philosophy

to my Mom and Dad

Abstract

This dissertation investigates the design of optical receivers and transmitters for VLSI chips. The receivers discussed here run at a moderate speed (100's Mb/s) and they need to be relatively sensitive. However, unlike a traditional fiber communication receiver, a low power and area consumption are very important design considerations. The challenge in designing these receivers comes from satisfying simultaneously all the above requirements. The design of VLSI optical transmitters based on reflection-mode modulators is also discussed. Three optoelectronic technologies, namely FET-SEED, MQW diodes flip-chipped onto CMOS, and epitaxy-on-electronic designs were used to design arrays of transceivers.

Current-Mode and buffering techniques are introduced into the design of VLSI-optoelectronic receivers. These techniques enable the integration with the receiver of larger and hence more alignable detectors. The design of a misalignment tolerant array of receivers is proposed and discussed. A time-differential receiver is introduced. It provides the good dynamic range of a dual-rail encoded receiver, but with only half the number of beams. In addition transmitters are optimized to drive large alignable modulators (reflection devices). For this purpose, BiCMOS drivers are also considered and discussed. Low-power adiabatic modulator drivers are proposed.

The designs discussed are multi-purpose and generic to all optical interconnect systems. However, the discussion is performed in the context of the design of a high-capacity free-space optical backplane. An overview of three demonstrator backplanes is given. To guide the design of optical interconnect systems such as a backplane, a model is proposed. It takes into account the important design parameters of the transmitter and receiver. The system model relates the bit error rate (BER) with the optical power of the interconnection (its sensitivity) at any given bit rate for a *given* design. The model also predicts the power consumption of the interconnect.

Résumé

Cette dissertation fait l'étude de la conception des récepteurs et des transmetteurs optiques pour des circuits à très haute densité d'intégration. Les récepteurs sont conçus pour des vitesses de transmission modérées (centaines de Mb/s) et pour être relativement photosensibles. La conception de ces récepteurs procède d'une manière très differente de celle des systèmes de communication de longue distance basées sur la fibre optique. Contrairement aux récepteurs pour les systèmes de télécommunication, il est très important de réduire la consommation en puissance et la surface qu'occupe les récepteurs abordés dans cette dissertation. Cette thèse discute aussi de la conception de transmetteurs construits à partir de modulateurs MQW en mode de réflection. Trois technologies opto-électroniques sont utilisées pour l'implementation des circuits de réception et de transmission: la technologie FET-SEED, la technologie diode MQW 'flip-chipper' sur CMOS (MQW diodes onto CMOS), et l'épitaxie-sur-électronique (epi-on-electronics).

Une technique 'current-mode' est utilisée pour concevoir des récepteurs dont la performance est indépendante de l'aire du photodétecteur. Ceci permet une augmentation de la tolérance d'alignement faisceau-détecteur. Une technique pour améliorer la tolérance d'alignement d'une matrice bi-dimensionelle est presentée. Un récepteur 'time-differential' est proposé pour augmenter la dynamique du signal utile sans requérir a un deuxième faisceau comme c'est le cas d'un récepteur 'dual-rail'. La conception de transmetteurs utilisant des modulateurs avec une grande surface active est réalisé avec une méthode d'optimization et la technologie BiCMOS. La grande surface active du modulateur facilite l'alignement du faisceau qui est refléchi par le modulateur. Une nouvelle méthode de commutation adiabatique est utilisée pour la conception des transmetteurs afin de réduire leur consommation en puissance à un niveau très faible.

La méthode de conception est générale mais elle est ici appliquée à des récepteurs et des transmetteurs pour des systèmes de fond de panier qui utilisent des matrices bi-dimensionelles de récepteurs et de transmetteurs. La thèse discute de la conception et la réalisation de trois fonds de panier. Pour assister la conception de ces systèmes d'interconnection optique, un modèle est construit pour prédire la probabilité d'erreur et la consommation en puissance de l'interconnection.

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Chapter 1: Introduction

There is an increasing demand for asynchronous transfer mode (ATM), parallel processing, video and real-time image processing, and other bandwidth hungry applications [1.1]. The computing and switching hardware handling those applications are now facing serious performance limitations. Although the processor speed has been increasing steadily over the past few years, the ability to communicate between processor nodes has not, and a communication bottleneck is being observed at various points in the interconnection hierarchy of the system. The bottleneck arises because of the physical limitations of electrical packaging and interconnections which limits the bandwidth and connectivity of systems. The introduction of optics in digital processing systems not only provides a solution to the limitations of electrical packaging and interconnections, but also enables new high-performance architectures that optimally exploit the optical bandwidth and the fan-out, and the third interconnection dimension of free-space [1.2, 1.3]. A complete analysis and comparison between optical and electrical interconnect technologies can be found in [1.4, 1.5]. From the system point of view, the bottleneck is nowhere more apparent than at the backplane level [1.6, 1.7]. The optical solution allows a higher degree of *scalability*, and *aggregate* throughputs unachievable by electrical backplanes. To fully exploit the optical connectivity, two-dimensional, free-space [1.8] optical interconnects have been proposed for the implementation of these connection-intensive digital systems.

Figure 1.1 shows the aggregate bandwidth requirements of future high-performance digital systems, and the potential of electrical and optical technology. Already traditional long-haul telecommunication systems have exploited the large temporal bandwidth (y-axis of Figure 1.1) and 'transparency' of fiber optics [1.9]. Within computing systems, however, the designer wants to capitalize on the large connectivity and spatial bandwidth (x-axis of Figure 1.1) of free-space optics [1.8]. Consequently a large number of receivers and transmitters (hundreds) are needed unlike long-haul telecom systems which only need one of each. Due to the large number, their implementation would be impossible with discrete components and a hybrid package is often the approach for telecom receivers and transmitters. An optoelectronic technology which integrates the optical and the electronic devices together is needed. Many integrated optoelectronic technologies have been proposed and developed over the past 18 years with the first reported demonstration of such technology made in 1979 [1.10]. The yield and

manufacturability has generally been poor. It is only recently that the appearance of technologies "good enough" for system use has been witnessed. Today optoelectronic technologies with very large scale integration (VLSI) are available to the system designer. Optical interconnections are normal to the VLSI chip, and directly terminated onto it. These VLSI optoelectronic chips are essential for the implementation of 2-D optical interconnections.

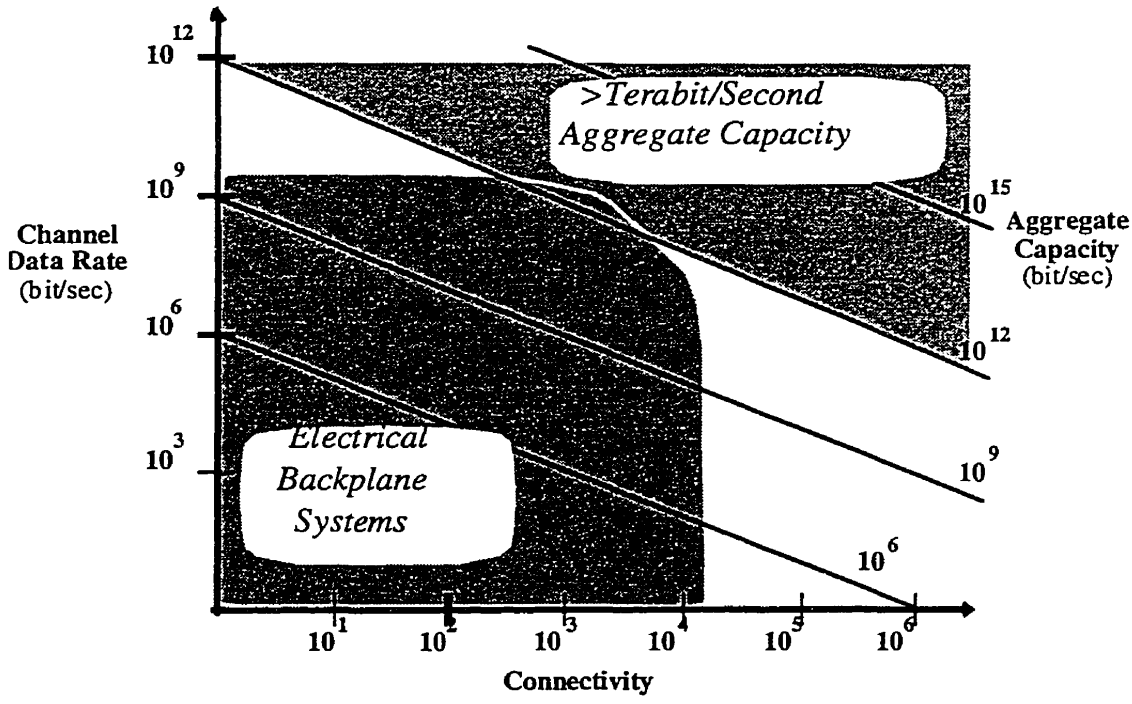

Figure 1.1: Future bandwidth requirements of digital systems

This chapter first motivates the use of optics inside digital computing and switching systems. Then, it motivates the research into optical transceivers for such systems and set the stage for the work presented in this dissertation: the design of 2-D arrays of optical transceivers for short-haul digital processing systems. The final two sections outline the content and the author's contributions. A large body of work has been performed on optical transceivers for long-haul communication systems (see for example [1.11]). The transceivers discussed in this dissertation are, however, very different because they are subjected to very different *system requirements*. The work presented in this dissertation is multi-disciplinary in nature and involves three distinct disciplines, namely optoelectronic technologies, circuit design, and systems. The emphasis is put on transceiver design for systems with large 2-D spatial bandwidth. The key contributions of this thesis reside in

the novel design approaches for VLSI optoelectronic receivers for systems such as a backplane.

1.1 Why optical interconnections?

As suggested in the introductory remarks, the physical advantages of optics will contribute along with an efficient architecture to the realization of systems that have performance unequaled by all-electrical ones. Optical interconnections offer several advantages over electrical interconnections [1.4, 1.5]. These advantages include:

- **Higher aggregate bandwidth.** The inherent parallelism of optics enables a larger connectivity than for electrical lines. This is so for two main reasons: 1) the planar geometry prevalent in electronic fabrication restricts the number of pin-outs and 2) the density is limited by the EM crosstalk and interference. For example current backplane technology cannot support much more than 2500 pin-outs per board. On the other hand, 2-D optoelectronic used in conjunction with free-space optics have the potential of several 1000's of pin-outs perpendicular to the board. The RC charging time of electrical lines increases with its length, and limits its bandwidth. Whereas in optical interconnects, the bandwidth is only limited by the receiver and transmitter circuits. The bandwidth is thus independent of the interconnect length. The net result is a much larger aggregate throughput when optical technologies are used.

- **Lower power consumption.** It has been shown that there is a break even length beyond which an optical interconnection would consume less power than an electrical one [1.4, 1.5,1.12, 1.13]. This occurs when the power consumption used to switch the electrical line becomes larger than the power consumption of the optical overhead (i.e. inefficiency of the electrical-to-optical and optical-to-electrical conversion). The power to switch an electrical line is proportional to the length of the interconnect whereas for an optical interconnect this power is basically constant over the interconnect length since optical losses are negligible compared to the overhead for the length of interest. Furthermore the optical interconnect doesn't need impedance matching. In electrical lines impedance matching is required to eliminate reflections at high-speed. Termination of electrical lines consume a very large amount of power. For example a BTL backplane connection consumes in excess of 200mW of power per line at a rate of 150Mb/s. Almost the totality of this dissipation occurs in its 50 ohm

termination. Optical interconnects on the other hand are directly terminated on-chip [1.12, 1.16].

- **Less skew.** Manufacturing process variations result in sizeable variation in the RC time constant of electrical lines. This leads to unpredictable delays and skew [1.14]. Optical interconnects are less susceptible because there is no line charging and the RC time constants of an optical receiver and transmitter are short.

- **Low cost.** Free-Space optical interconnects is potentially low cost since no medium is required. The cost per line can be very small because 1000s of links can be aligned at the same time by a single alignment procedure. This is its attraction over fiber links.

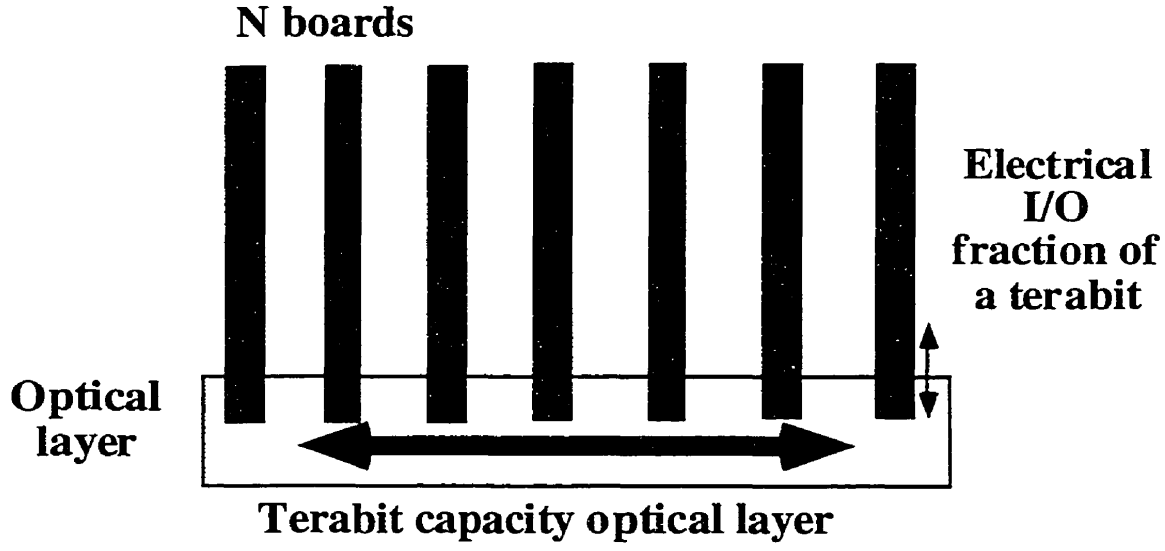

Figure 1.2: Firehose architecture

The large aggregate bandwidth provided by optics has stimulated research in computing and switching architectures [1.15]. Several architectures have been proposed to exploit fully the large optical bandwidth. The challenge is to make use of the large optical bandwidth provided by the VLSI optoelectronic chip without being limited by the small electrical pin-out of the chip [1.16]. An interesting class of architectures that addresses this issue is the firehose [1.16] of which a backplane is one example. A backplane is schematically depicted in Figure 1.2. A number of taps or boards inject and retrieve data at a fraction of the total capacity at the optical layer. Typically a PCB has a throughput of 1-

10Gb/s [1.17]. Each board contributes to filling the optical bandwidth. The boards are about 30cm apart which is comparable to the break even length mentioned above. Optics can provide a 10 boards backplane with the required 100Gb/s throughput. An active backplane architecture was proposed [1.18] to regulate the traffic from the boards in such a way that the optical bandwidth is used optimally. Another application of optical interconnections can be found in the switching fabric [1.8] which uses 2-D fiber bundles at both input and output. Optics can also be used when intensive sorting and exchanging of data is required [1.19]. In all these three systems, the optical bandwidth between the processing chips is orders of magnitude above the electrical bandwidth of the chip.

The implementation of the optical solution must be considered carefully in order to fully take advantage of optics. Optoelectronic and transceiver design are key to enable optically interconnected electronic systems. Optoelectronic technologies and transceiver design techniques are now reviewed.

1.2 VLSI Optoelectronic Technologies

The implementation of 2-D interconnects requires an optoelectronic technology with the following characteristics:

- A high optical-to-electrical and electrical-to-optical conversion efficiency
- VLSI electronic intimately integrated with the optical devices (detectors, and emitters or modulators)
- High device yield and uniformity
- High reliability
- Moderate speed (100's of Mb/s)

Yield, uniformity and reliability similar to that obtained in current integrated circuits (ICs) are desirable. Integration avoids the need for a hybrid package that results in the implementation of the optical solution consuming a large electrical power. Hybrid packaging is often used for long-haul telecommunication transceivers. However the power consumption in those systems is not as big of a concern as in the digital processing systems treated here. Furthermore receivers and transmitters are often interlaced on the VLSI chip

plane so that an integrated technology is required. A large number of integrated optoelectronic technologies have been proposed and demonstrated [1.20].

Integrated optoelectronic technology appears in two forms: monolithic and hybrid integration. In a monolithic technology, both optical and electronic devices are grown "simultaneously" and share a common semiconductor substrate. Whilst in a hybrid technology, the devices are grown separately on separate substrates. The devices are brought into intimate contact afterwards with a technique such as self-aligned flip-chip solder bonding. Flip-chip solder bonding was developed in the early 1960s by IBM [1.21]. It is used because 1) a large number of bonds can be formed simultaneously, 2) the resistance, capacitance and inductance are one or two orders of magnitude lower than wirebonds used in a hybrid package, and 3) it allows pin-outs in the center of the chip rather than be confined to its perimeter. The first demonstration of flip-chip solder bonding of optoelectronic devices was in 1989 [1.22]. Large arrays of GaAs Multiple Quantum Well (MQW) diodes flip-chip onto CMOS have been demonstrated [1.23, 1.24]. The electro-absorption devices are PIN diodes with a multiple quantum well (MQW) stack grown in the intrinsic region. The device can be used as a detector or as a modulator. Modulators use the Quantum Confined Stark Effect to shift the exciton peak of the MQW structure, and consequently alter the absorption of the device at a fixed wavelength. An example of backside illumination photodiodes flip-chip on a substrate is found in [1.25].

Another technology which exploits commercial foundry electronics can be found in the epi-on-electronic technology proposed by Fonstad's group at MIT. In this technology, optoelectronic devices are grown onto commercial GaAs electronics [1.26]. The use of this technology for a system is explored in Chapter 3. Finally a purely monolithic technology is found in the FET-SEED [1.27]. This technology provides intimate integration of modulators and photodetectors with LSI GaAs electronics. The poor integration density, non-uniformity and low yield of this technology makes it less attractive for system use. The details of this material are explored in Chapter 2.

Vertical-Cavity Surface-Emitting Lasers (VCSEL) are attractive, and show great promise for the future. Due to its geometry it naturally provides the 2-D arrays needed for free-space interconnects such as the backplane. It has a small footprint and emits a low-divergence circular beam. Large arrays of VCSELs with operating current low enough to allow simultaneous operation of all the lasers in the array appeared only recently. An 8X8 array with a threshold of 1mA has been reported [1.28]. Researchers are currently working

on reducing the threshold of VCSELs. High reflectivity distributed Bragg reflector (DBR) mirrors can be fabricated. The resistance of the DBR has been reduced and current confinement methods have been proposed to increase the efficiency of the device and reduce its threshold. The monolithic integration of VCSELs with electronics is currently under development [1.29, 1.30]. VCSELs can also be integrated with electronics using flip-chip bonding. Direct on-chip integration of VCSELs is still a technology that is not readily available to the system designer. Hybrid packaging of VCSELs with electronics and detectors provides a temporary solution. An example of hybridization is found in the MSM/VCSEL demonstrator described in Chapter 6. Another example of hybridization is found in [1.31]. The transceivers implemented with this technique consume a large power and the system is not scalable to large parallelism.

Currently the best temporary solution of a technology that integrates optoelectronic devices directly on-chip is found in the hybrid CMOS technology described above. The use of MQW technology is appropriate whenever the number of transmitters required in a system is around 1000, and the bit rate is below 1Gb/s [1.32]. The MQW device has a saturation intensity which limits the output power of a transmitter based on this technology. The insertion loss is also high (typically 3dB). Their use often requires sensitive receivers. Modulators need an extra alignment of the read beam onto the device. Consequently, this makes modulator-based system optomechanics more involved and system alignment more difficult [1.16]. On the other hand, arrays of VCSELs with a low threshold and high output power (10mW) would permit the implementation of high-throughput systems more easily and more cost effectively than a modulator-based technology. A complete comparison between the two has been reported [1.33].

1.3 A New Class of Optical Receivers

The amplification of optical signals and the driving of emitters or modulators need to be considered carefully. The receivers and drivers are the interface between the analog (power amplitude) optical signal and the on-chip VLSI digital electronics. Their efficiency drives the break-even distance for which optical interconnections are advantageous over an electronic implementation. A large transceiver power consumption contributes to lengthening the break-even distance. This can be significant when compared to the short length of the interconnects that are typically required in computing systems. The

performance of the transceivers determines whether or not a given system architecture can be implemented using a specific optoelectronic technology.

As noted in the introductory remarks, the different system constraints make the design of the long-haul and the short-haul optical receivers very different from each other [1.9, 1.34]. Research into the design of VLSI optoelectronics is relatively new. It has emerged from a class of digital processing systems that exploit optical interconnects e.g. in optical backplanes or a switching fabric. In long-haul systems, optical attenuation makes the signal to be detected very weak. Thus sensitivity in traditional long-haul receivers has been the main design goal. Furthermore a large dynamic range (20-30dB) is required to handle the wide variation in signal levels. Automatic gain control (AGC) circuitry is needed to achieve the required dynamic range. The sensitivity and dynamic range requirements result in high electrical power consumption (which is a few Watts in those systems) and area (1000s mm^2). In VLSI optoelectronic receivers this is unacceptable. A VLSI optoelectronic receiver is typically part of a large 2-D array with interlaced processing electronics. It is important to minimize the power and area consumption. The challenge in the design of these receivers comes from satisfying the following requirements simultaneously:

- Compact (e.g. 0.0025 mm^2 or 50μmX50μm). To make the receiver compact, no AGC circuitry is used. Consequently the dynamic range is small (<a few dB). Larger dynamic range can be provided by a differential approach (see section 4.7).
- Low power consumption (<5mW). Power consumption in the analog front-end of the receiver dominates over that consummed by the thresholder and the digital part of the receiver.
- Reasonable sensitivity (-20dBm). The receiver sensitivity is noise-limited in long-haul fiber optic receivers. Whereas in the VLSI optoelectronic receiver it is limited by gain. The amount of gain that these receivers provide is limited because of the power consumption and area constraints. Furthermore the sensitivity is often sacrificed in order to tolerate process and external parameter variations, and digital switching noise that arises in large arrays [1.35].
- Moderate bandwidth (be able to run at 100's Mb/s). No bandwidth is allocated to data encoding and the receiver is DC coupled.
- Digital output. The analog and the digital part are intimately integrated together.

The transceivers can encode and decode a single beam (single-rail) or a pair of differential beams (dual-rail). The dual-rail configuration was adopted because of the low contrast ratio of modulators (1:10 at best [1.36]) for the voltage swings that are normally available on integrated circuits. Dual-rail interconnects are less sensitive to fluctuations in the received optical power than single-rail. Thus, dynamic range can be improved to some extent without any AGC circuitry. The drawback of the dual-rail interconnect is that two beams are needed instead of one. This can complicate the alignment of the system and increases the optical power required by the interconnects. This dissertation will present a novel receiving scheme that improves the dynamic range of VLSI receivers without this drawback (see Chapter 4).

1.4 Contents

Chapter 1 gives a brief introduction to the content of this thesis.

Chapter 2 present a model and a simulator for the FET-SEED technology. With these tools, a transceiver array is designed and characterized for an optical backplane.

Chapter 3 explore the epi-electronic technology for backplane use. It presents the design dynamic receivers and a LED driver.

Chapter 4 shows how alignment tolerance of the interconnect can be increased with proper circuit design techniques. Current-mode and buffer design of VLSI optoelectronic receivers are proposed, and demonstrated. This chapter also examines technique to improve the dynamic range of VLSI receivers. Furthermore low-power modulator drivers using adiabatic switching are proposed.

Chapter 5 presents an optical interconnect model that relate the BER with the sensitivity and the bit rate for a given design.

Chapter 6 outlines the backplane systems that have been constructed.

Chapter 7 summarizes the thesis and makes concluding remarks.

1.5 Contributions

The material presented in chapter 2 and 6 is derived from a publication of the author of this dissertation [1.37], and on publications that he co-authored [1.38, 1.39, 1.40, 1.41]. All the material in Chapter 3 and 5 are based on original but unpublished work performed by the author. Most of the material in chapter 4 was presented by the author for the first time at major technical conferences, except for the work on adiabatic modulator drivers (section 4.8.4) which is original unpublished work. Except for the concept of the alignment tolerant array (section 4.6) and the time-differential receiver (section 4.7) which were Frank Tooley's ideas, the work in Chapter 4 emanated from the author's original ideas. The current-mode sense amplifier based receiver was invented independently by the author and by T.K Woodward from Lucent Techonology, Bell laboratories. Two full journal papers are under preparation. One reports the VLSI optoelectronic receiver design using a current-mode approach, and the other reports the model of a 2-D interconnect. This thesis makes the following contributions:

- Introduce a current-mode approach for designing VLSI optoelectronic receivers (U.S. patent disclosure filed). Two examples of this approach, namely the current-conveyor based receiver and the current-mode-sense-based receiver are proposed, and designed (Chapter 4).
- Introduce analog buffering techniques for designing VLSI optoelectronic receivers (Chapter 4).
- Propose adiabatic modulator drivers for zero energy switching (Chapter 4).
- Propose and design of low-power dynamic GaAs receivers (Chapter 3).
- Establish a system-level model that relates BER with incident optical power and bit rate for a given receiver design (Chapter 5).
- Develop CAD tools and modeling for a novel FET-SEED technology (Chapter 2).
- Make contributions as a *team member* to three successful backplane demonstrators (chapter 6).

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Chapter 2: FET-SEED Modeling, Design and Characterization

The work presented in this chapter was completed under the supervision of Professors D.V. Plant and H.S. Hinton in the fall of 1993 and during 1994. This chapter is derived from two publications [2.1, 2.2] of the author. In this chapter the design, modelling and characterization of FET-SEED transceiver arrays are discussed. The FET-SEED technology *monolithically* integrates in a custom batch fabrication process [2.3] GaAs based field-effect transistors with PIN detectors and normal-incidence modulators which use the quantum confined Stark effect in a multiple-quantum-well (MQW). A single optical device namely a p-i(MQW)-n diode, can be used as a detector or a modulator.

A cross sectional view is shown in Figure 2.1. The p^+-layer is contacted and tied to the source of the GaAs FET on the right of Figure 2.1. This layer helps to shield the FET against backgating [2.4, 2.5]. However it increases the parasitic capacitance of the diode. In general it is difficult, if not impossible, to optimize all the devices on a monolithic platform. In addition to the MQW diodes and depletion FET, the FET-SEED process offers Schottky diodes to the designer. Enhancement FET can be produced by applying a bias to the p layer to shift the threshold to a positive voltage. A forward biased MQW diode can be used as a LED. However, none of these devices are optimized.

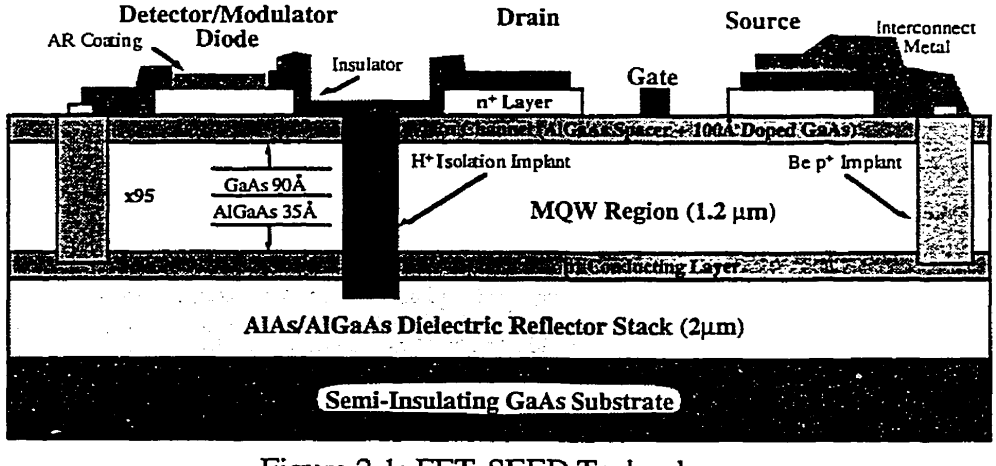


Figure 2.1: FET-SEED Technology

In the following section a model for the FET-SEED technology is proposed. In section 2.2 a high-speed optoelectronic test bed is discussed. The test bed is used to

characterize transceivers. In section 2.3 the characterization of the FET-SEED transceivers are presented.

2.1 FET-SEED Modeling

The GaAs FET is modeled with a PSPICE based Raytheon or Statz model [2.6, 2.7]. A discussion of various MESFET models can be found elsewhere [2.6, 2.8, 2.9]. The values of the model parameters are extracted. Ideally wafer uniformity and the run-to-run uniformity need to be characterized in order to provide the FET-SEED circuit designer with a robust model. Typically, the threshold voltages vary radially on the surface of wafer. They are around -0.8V, while in the center of the wafer they increase to around -1.1V [2.3]. The variation slope is typically 10mV/mm of wafer edge and can be as large as 100mV/mm [2.3]. This radial variation is due to the variations in thickness of the nominal 900Å AlGaAs spacer layer that exists between the n-doped GaAs channel and gate, and it is a result of the poor quality achieved in the MBE growth process [2.3]. An HP 4145B semiconductor parameter analyzer is used to measure the I-V curves of a few FET samples. The values of the Statz model parameters are extracted from those measurements [2.1], and are shown in Table 2.1.

MESFET Parameter Values:
LEVEL=2 (to select the Raytheon model)
VTO (pinch-off voltage) = -1.4 V
ALPHA (saturation voltage parameter) = 1.67 V^{-1}
BETA (transconductance coefficient) = 8.6E-5 A/V^2
LAMBDA (channel-length modulation) = 0.03 V^{-1}
B (doping tail extending parameter) = 0.73 V^{-1}
TAU (conduction current delay time) = 0 sec
RG (gate ohmic resistance) = 0 Ω
RD (drain ohmic resistance) = 1500 Ω
RS (source ohmic resistance) = 1500 Ω
IS (gate junction saturation current) = 1.0E-14 A
N (gate pn emission coefficient) = 2.2
VBI (gate junction effective built-in potential) = 0.8 V
M (gate junction grading coefficient) = 0.5
CGD (zero-bias gate-drain junction capacitance) = 0.1E-15 F
CGS (zero-bias gate-source junction capacitance) = 1.0E-15 F
FC (forward-bias depletion capacitance coefficient) = 0.5
CDS (drain-source capacitance) = 0.4E-15
EG (bandgap voltage (barrier height)) = 0.69 eV

Table 2.1: Parameter values for the PSPICE based Raytheon model

Figure 2.2 shows a fit of the model generated I-V curves and those obtained experimentally. Typical measured DC currents of the transistors at V_{gs} = 0 V were 75.5 mA/mm at V_{ds} = 2.0 V, and the measured transconductance at V_{gs} = 0 was 93.5 mS/mm. The measured threshold voltages were - 1.2 V, and the drain-source breakdown voltages were greater than 8 volts. The MESFET current gain bandwidth, f_t , was calculated using $\frac{g_m}{2\pi(C_{gs}+C_{gd})}$ where g_m is the model predicted FET transconductance, and C_{gs} and C_{gd} are the modeled gate-source and gate-drain capacitances respectively at the operating point of the MESFET. Using values of C_{gs} = 9.51 fF and C_{gd} = 1.1 fF [2.10], we calculated an f_t of 13.5 GHz, which is in good agreement with an experimentally measured f_t of 10 GHz [2.4].

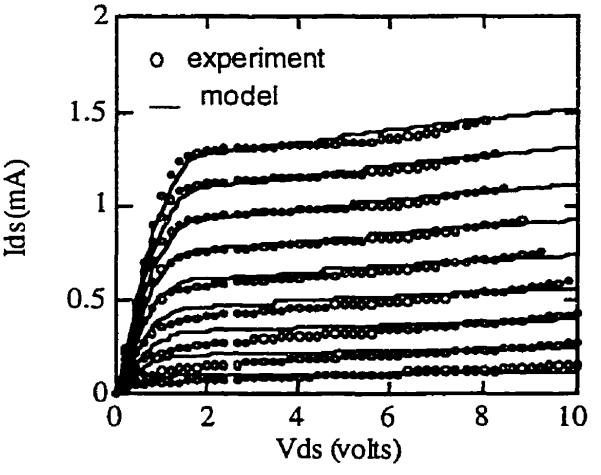
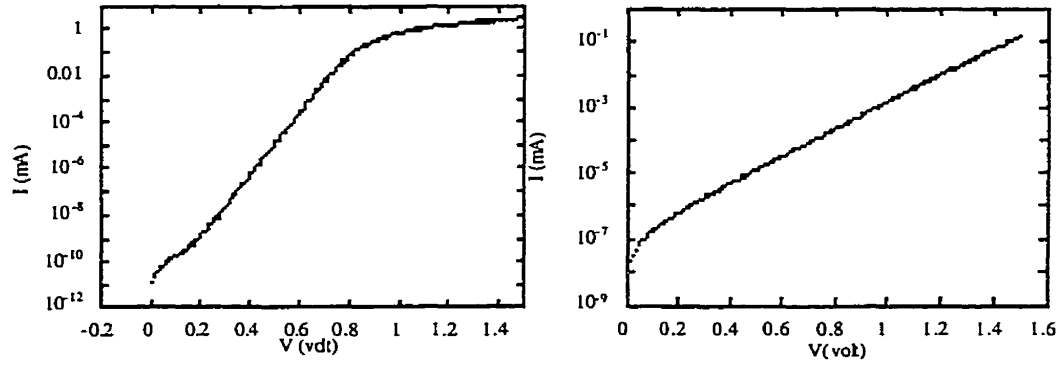


Figure 2.2: 10μm FET I-V characteristics
(-1V≤Vgs≤+0.6V by 0.2V steps)

The diode I-V modeling (Schottky diodes and PIN junction diodes) was done using the standard PSPICE™ based model for diodes. The measured I-V characteristics are shown respectively in Figure 2.3a and b. The extracted values of the PSPICE™ parameters [2.1, 2.7] are shown in Table 2.2 and in Table 2.3. The provide a good fit for the range of interest. However, discrepancies are observed for very low currents and voltages. The PIN diode optical characteristics are also of interest. The device is modelled with a current source that depends linearly on the optical power, and with a capacitance to simulate its AC characteristics. The L-V characteristic is described using a simple look-up table [2.11], and the capacitance is assumed to be 0.115fF/μm^2 [2.12]. Figure 2.4 shows a plot of the typical diode responsivity and reflectivity versus voltage at 850 nm. Individual modulators

exhibited a reflectivity change of 45% to 15% with -7.5 volts of applied bias, and modulator pairs in the transmitter circuit exhibited a 2 (60%) to 1 (30%) reflectivity contrast ratio. The detectors had a responsivity of ~0.5 A/W over a large range of applied voltage.



(a) (b)

Figure 2.3: (a) Schottky Diode (b) PIN Diode I-V characteristics

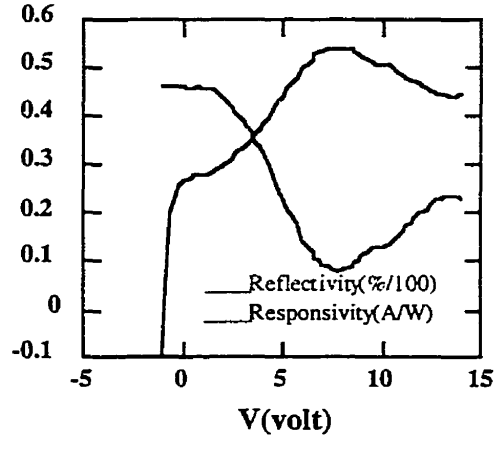


Figure 2.4: Optical Characteristics of p-i(MQW)-n Diodes at 850nm

In addition to FETs and diodes, we also modeled the trace lines and the bond pads. The trace lines were modeled as RLC distributed networks with characteristic impedance Z_o, resistance R_o, inductance L_o, and capacitance C_o per unit length. The values of these parameters were calculated assuming a conventional microstrip geometry for metal interconnects[2.5]. For the FET-SEED technology, the metal interconnects are 300nm thick gold with $\rho = 2.2X10^{-16}$ Ω-cm. The receiver signal interconnects are 4 μm wide and the

transmitter signal interconnects are 5μm wide. The parameter values of the RLC distributed model were calculated to be $R_0 = 0.0183\ \Omega$/cm, and $C_0 = 0.549$ pF/cm $L_0 = 14.3$ nH/cm. For the 75 μm x 75 μm bond pads, the loading capacitance was calculated to be 13.8 fF. The validity of this model is confirmed by experiments described in the next sections.

Schottky diode parameters:
IS (saturation current) = 1.16E-16 A
N (emission coefficient) = 1.26
ISR (recombination current parameter) = 0 A
NR (emission coefficient for ISR) = 2
IKF (high-injection 'knee' current) = infinite A
BV (reverse breakdown 'knee' voltage) = infinite V
IBV (reverse breakdown 'knee' current) = 1E-10 A
NBV (reverse breakdown ideality factor) = 1
IBVL (low-level reverse breakdown 'knee' current) = 0 A
NBVL (low-level reverse breakdown ideality factor) = 1
RS (parasitic resistance) = 3693 Ω
TT (transit time) = 0 sec.
CJO (zero-bias pn capacitance) = 0 F
VJ (built-in potential) = 0.75V
M (grading coefficient) = 0.333
FC (forward-bias depletion capacitance coefficient)= 0.5
EG (bandgap voltage (barrier height))= 1.4 eV
XTI(IS temperature exponent) = 2
RL (Leakage resistance)=infinite Ω

Table 2.2: Values of the parameters for the Schottky diode

MQW pin diode parameters:
IS (saturation current) = 1E-13 A
N (emission coefficient) = 3.2
ISR (recombination current parameter) = 0 A
NR (emission coefficient for ISR) = 2
IKF (high-injection 'knee' current) = infinite A
BV (reverse breakdown 'knee' voltage) = infinite V
IBV (reverse breakdown 'knee' current) = 0 A
NBV (reverse breakdown ideality factor) = 1
IBVL (low-level reverse breakdown 'knee' current) = 0 A
NBVL (low-level reverse breakdown ideality factor) = 1
RS (parasitic resistance) = 4061 ohm
CJO (zero-bias pn capacitance) = 0.1E-15 F
VJ (built-in potential) = 0.8V
M (grading coefficient) = 0.5
FC (forward-bias depletion capacitance coefficient)= 0.5
EG (bandgap voltage (barrier height))= 0.69 eV
XTI(IS temperature exponent) = 2

Table 2.3: Values of the parameters for the PIN diode

2.2 FET-SEED Transceiver Array Design

Arrays of individually addressable FET-SEED dual-rail transmitters and receivers are fabricated using the batch fabrication process made available through the ARPA - Consortium for Optical and Optoelectronic Technologies for Computing (CO-OP) and AT&T [2.13]. The purpose of this design is two-fold: 1) to facilitate the development of a FET-SEED model, and 2) to design transceivers for a backplane system. Using the FET-SEED technology, a 4 x 4 array of electrically addressable, amplified differential modulators, and a 4 x 4 array of diode clamped, optical receivers with off-chip drivers are designed [2.14]. Figure 2.5 shows the 2mmX2mm chip. The transmitter array is located in the upper left corner, and the receiver array is located in the lower right corner. In both arrays the p-i(MQW)-n diodes have a 25 x 25 μm active area. The two diodes constituting a dual-rail link are separated by 50 μm, and each dual-rail link is pitched at 200μm.

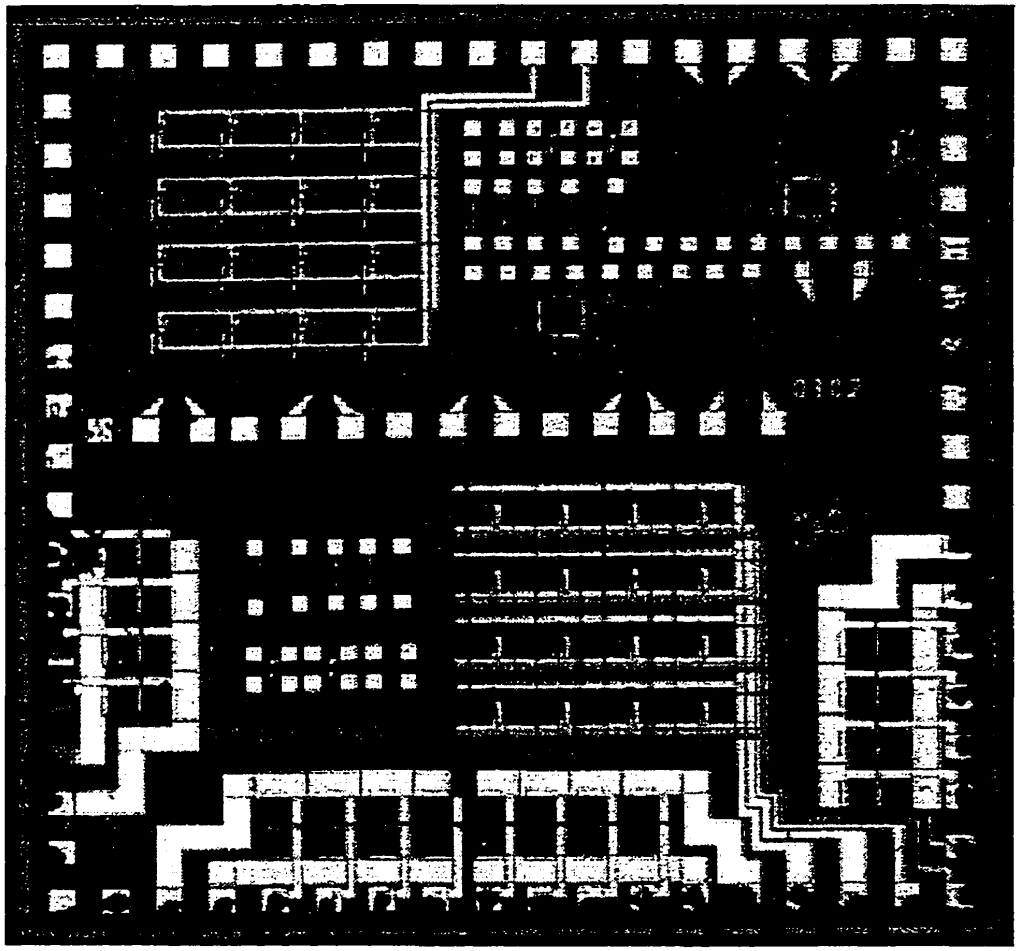


Figure 2.5: FET-SEED chip

The transmitter circuit operates by electrically modulating the voltage drop across the series MQW diode pair, subsequently modulating the reflectivity of the diodes [2.15]. Both the load and switching MESFET transistors were 25μm wide. The receiver circuit operates by demodulating dual rail optical signals which are detected using a series connected detector-diode pair to form a diode-clamped receiver [2.16, 2.17]. The input node (gate of the input DFET) is charged and discharged as a function of the state of the incident optical power. The series diodes push and pull the photocurrent in and out of the input node. A pair of clamping diodes (biased at +/-Vcl) limits the voltage at the input. The demodulated optical signal drives a 3-stage amplifier circuit. The first two stages form a series pair of inverters with a total of four load and active transistors, each transistor being 6 μm wide. The third stage (shaded) is a 375 μm power FET designed to drive 100 ohm transmission lines. The receiver and the transmitter circuit and layout are shown in Figure 2.6.

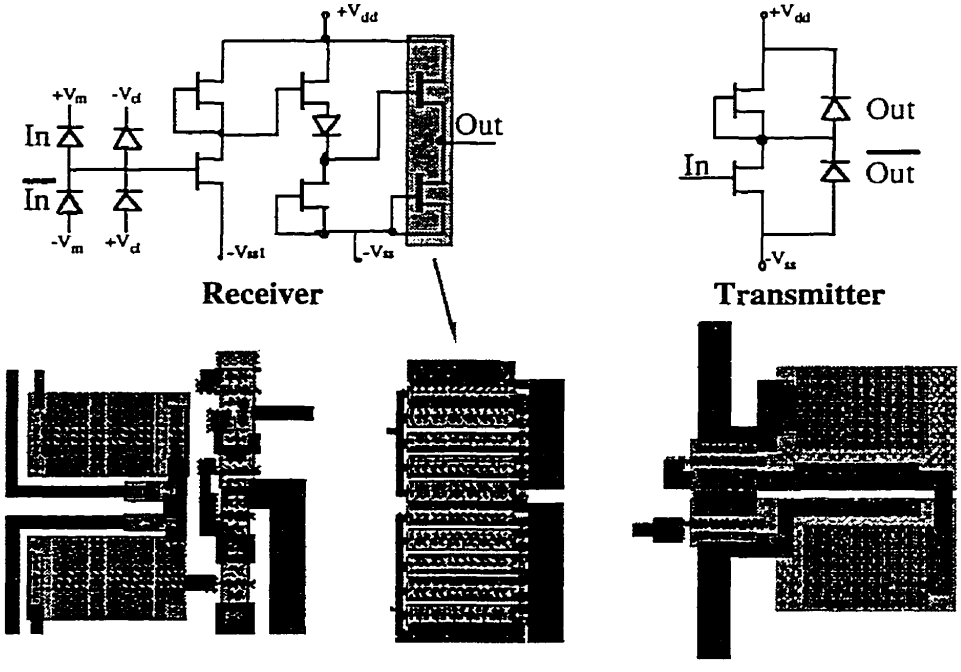


Figure 2.6: Single Receiver and Transmitter

The diode-clamped receiver is similar to a high-impedance front-end [2.18]. To achieve a high-speed, high-impedance front-end normally necessitates equalization [2.18]. For the diode-clamped receiver, diodes are used to clamp the voltage at the input. This allows high-speed operation of a high-impedance front-end by limiting the integration of charge on the input node. Furthermore by properly biasing the clamping diodes the input node voltage swing can be adjusted to the most sensitive point of the amplifier. The bias of

the amplifier can also be adjusted for that purpose. The amplifier in this design uses BFL [2.5]. The drawback of this receiver includes the area consumed by the clamping diodes, additional bias lines, and a moderately high electrical power consumption (2.8mW).

In addition to the 4 x 4 arrays, individual FETs, PIN junction diodes, and Schottky diodes are included on the die for DC probing purposes. The I-V curves of these discrete devices is measured and the data was used to develop the device models described in the section 2.1.

2.3 High-Speed Optoelectronic Tester

This section presents a generic VLSI optoelectronic receiver tester. It provides a high-speed optical input to the receiver under test, and extracts a high-speed electrical output. The tester can supply both a single-ended and differential optical input to the receiver under test. A DC beam of light and a modulated one are focused onto the device plane. When testing differential input receivers, the modulated beam power level swings about the unmodulated one. This technique for testing dual-rail receiver is simple and does not necessitate the use of an additional modulator and their synchronization.

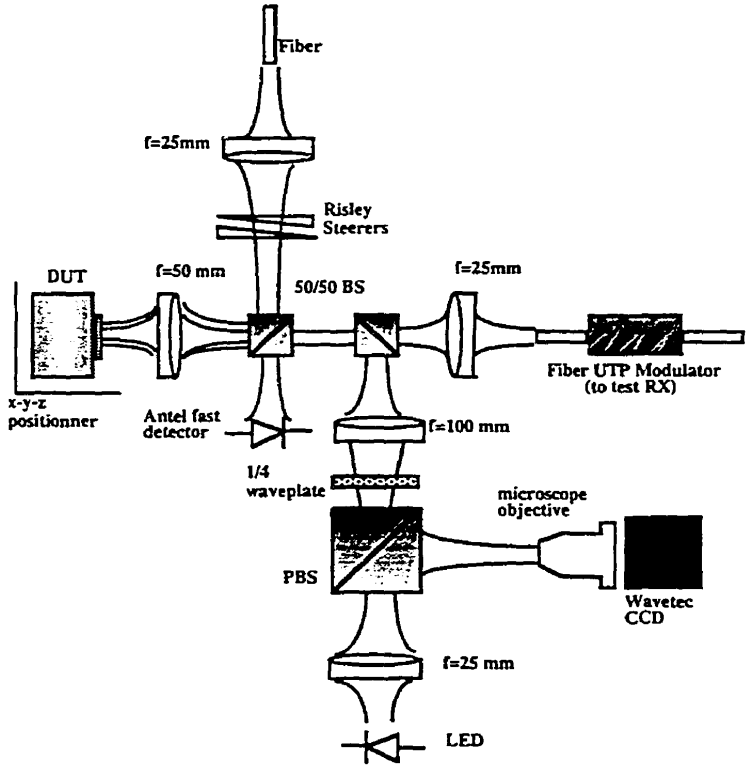


Figure 2.7: Optoelectronic Tester

The optoelectronic tester is shown in Figure 2.7. A Schwartz SEO tunable Ti:sapphire laser pumped with a Coherent argon laser is used as the source. The wavelength is tuned to the operation wavelength of the MQW diodes which is 850 nm. The laser output is split into two paths as shown in Figure 2.7. One path is modulated by a UTP Mach-Zehnder amplitude modulator [2.19]. In the other path, Risley steerers (two glass wedges) are used to position one beam with respect to the other. Both beams are focused on the device plane of a 4f system with a 25 and 50mm lens. This choice of lens yields the desired spot size on the device plane. The 4f relay theoretically provides a spot diameter, $2\omega_0$ of 10.2 μm. However due to optical aberrations and misalignment the measured diameter is approximately 20μm. However this spot diameter still results in more than 99% of power coupling into the detector. The spot size is measured with a Merchantek PC-Beamscope Profiler with a series 3 probe style head. Table 2.4 shows the results of the spot diameter (e^{-2} power) $2\omega_0$, the Gaussian fit and standard deviation for 34 samples at various optical powers for an X and a Y scan.

Power (mW)	Gaussian Fit (%)	Diameter (μm)	Standard Deviation
1	96.2	17.85	0.23
2	96.4	18.06	0.14
3	96.4	18.57	0.21
4	96.4	18.79	0.24
5	96.0	18.92	0.31

(a)

Power (mW)	Gaussian Fit (%)	Diameter (μm)	Standard Deviation
1	96.6	17.88	0.06
2	96.3	18.03	0.07
3	96.4	18.54	0.05
4	96.2	18.84	0.16
5	96.1	18.93	0.33

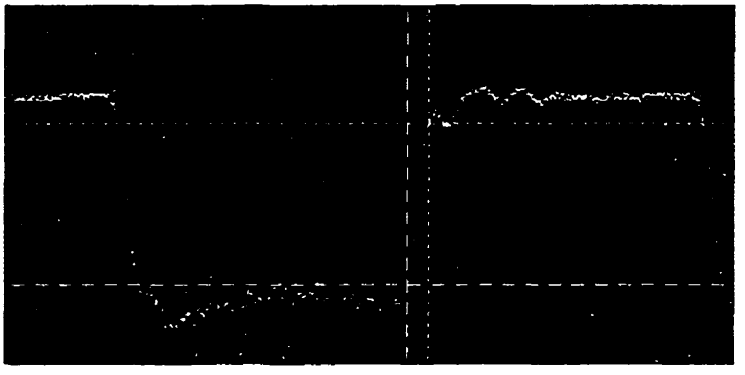
(b)

Table 2.4: Spot size of test beam (a) X-scan (b) Y-scan

The UTP modulator has a fiber input and output. The maximum contrast ratio is measured to be 14 dB for a bias voltage of 2.4V. The inherent insertion loss of the modulator is 4.6 dB (37%throughput) but there is only a 60% coupling efficiency which results in an overall throughput of 20% of the input power.

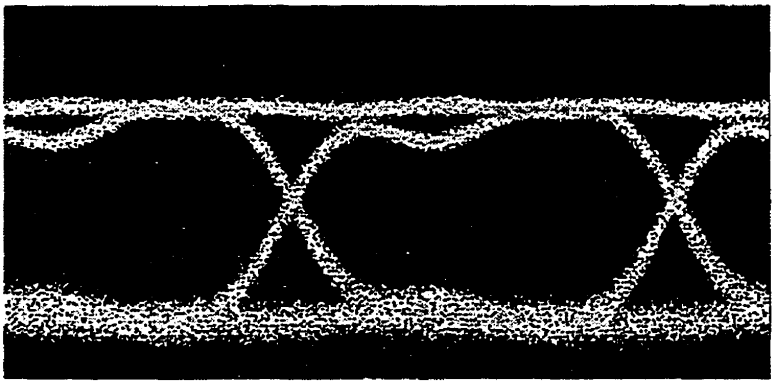
To view the device plane, a LED based illumination and a 4f imaging system is incorporated into the set-up as shown in Figure 2.7. Off-the-shelves Spindler and Hoyer™ optomechanics are used to hold the optics and define the optical axis.

The UTP modulator has a 3dB bandwidth of 12GHz [2.19]. It is driven by a HP80000 digital data generator which has a 150psec risetime. Test bit patterns can thus be provided. The risetime of the modulated input is characterized with an Antel ARX-SA avalanche photodetector. This fast detector is incorporated in the tester to provide a continuous monitor of the modulated beam as shown in Figure 2.7. The detector and its sampling head have a risetime of 210 psec and 7 psec, respectively. The measured risetime is 289.4 psec as shown in Figure 2.8. Deconvolving the detector and sampling head risetime, the risetime of the modulated beam is found to be 200 psec. Eye diagrams are also obtained and a typical eye is shown in Figure 2.9. This eye can be used as a baseline to quantitatively compare the performance of different receivers.



1 nsec / div

Figure 2.8: Tester Unconvolved Risetime (289.4 psec)



200 psec / div

Figure 2.9:Tester Eye Diagram (unconvolved)

Table 2.5 summarizes the characteristics of the tester. It provides a high-speed optical input with a good contrast ratio to the receiver under test. The power available to the receiver under test is limited by the maximum input power allowed by the modulator. An alternative way to provide a differential input is currently being pursued. In that tester, two lasers are used and can be modulated independently. The optics in that set-up are packaged with custom optomechanics into a permanent laboratory set-up.

Spot size (μm)	Power (mW)	Contrast Ratio (dB)	Risetime (psec)
20	7	14	200

Table 2.5: Summary of tester characteristics

2.4 Characterization Results

The characterization of the transceiver array is now described, and the validity of the model is experimentally verified. The FET-SEED transceiver circuits are wire bonded into high speed multilayer ceramic Quad Flat Packages (QFP) capable of carrying forty signals with 2:1 signal-to-ground ratios. These packages are further integrated onto PCBs using a pressure based, solderless disconnect which had 50 ohm impedance matching capabilities. By appropriately tuning the package to board impedance, these QFP/PCB packages were capable of supporting forty, 3 GHz signal lines. In order to verify the bandwidth properties of these packages, network analyzer measurements were conducted on the assemblies. The 3 dB point of the QFP/PCB assembly was measured to be greater than 3 GHz, with a 0.1 dB transmission loss over the 5 KHz - 100 MHz range. All optical and electrical measurements of the FET-SEED electronics described in the following sections are performed on devices packaged at the PCB level using these assemblies. The receivers are characterized with the tester described in the previous section.

2.4.1 Characterization of the Receiver Array

The optical properties of the detector is measured using an 850 nm source, the λ_1 operating point for these SEED structures. Figure 2.4 shows a plot of the typical diode responsivities versus voltage at 850 nm. The detectors had a responsivity of 0.5 A/W. Both optical and electrical, high frequency receiver circuit measurements are performed, and compared to predicted performance. In the case of the optical measurements, the optoelectronic tester described in the previous section is used to measure the rise and fall

The high frequency electrical measurements could be accomplished owing to the fact that the devices were packaged using high bandwidth signal lines for DC biasing. Using a bias tee, the clamping diodes could be biased to their optimum operating point, and then either digital or analog signals could be applied to the input transistor of the three stage amplifier. Because all the clamping diodes on the die are electrically tied to two inputs (one for $+V_{cl}$ and one for $-V_{cl}$), the measurement results described below represent a response of the entire 16 element array being driven simultaneously (not including the power FETs). Digital measurements are performed by modulating the circuit input using a 150 psec risetime source, and measuring the output using a digitizing scope. Figure 2.12 the experimental set-up for all the electrical measurements, and a plot of a typical measured response (dashed line), yielding a rise time of 2.87 nsec for a circuit biased to an optimum operating point. The correlation between the optical and electrical measurements is very good. They agree on a response time of the amplifier of around 2.7nsec.

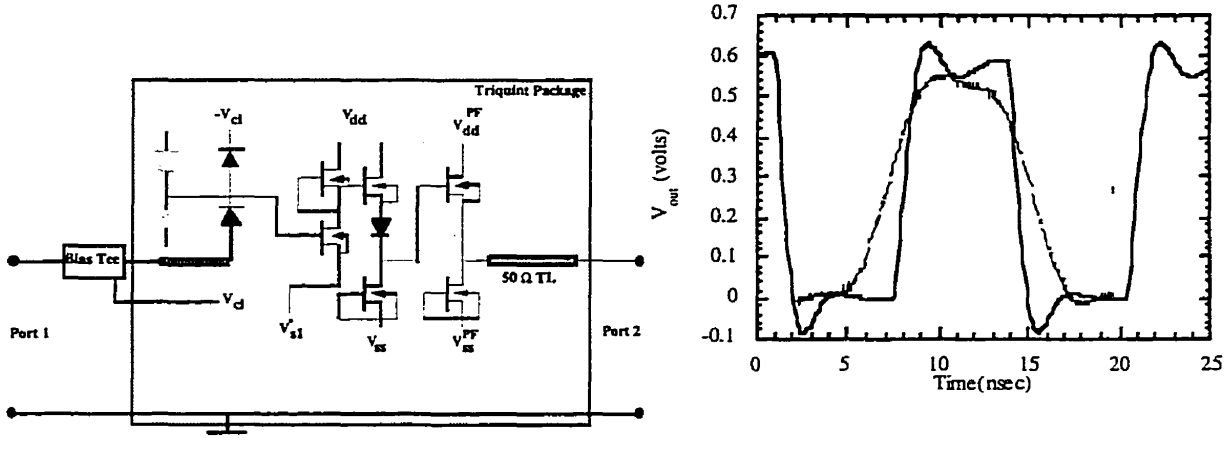


Figure 2.12: Receiver all-electrical measurements

S-parameter measurements on the array are also performed using a 5 kHz - 3.0 GHz network analyzer. In order to de-embed the circuit performance from the combined circuit plus package performance, the network analyzer was calibrated using a modified QFP/PCB calibration package. The calibration package contained a 50-Ohm termination, a short circuit termination, an open circuit termination, and a straight through connection. A complete set of S-parameters is taken on five of the 16 channels, and this data is used to calculate the properties of the circuit including the current gain, h_{21}. In addition, the data is used to measure the array uniformity. Figure 2.13a shows a plot of the measured circuit

current gain, h_{21} for 5 of the channels. From these measurements, an average f_t = 440 MHz is found. The data oscillates over the first 400 MHz. The oscillations are not due to improper impedance matching to the network analyzer, the input and output impedances are matched to 50 and 100 ohms respectively. Using the above models, the predicted h_{21} (solid) is also shown in Figure 2.13b, with a predicted f_t = 691 MHz. As is expected based on the above digital measurements, the agreement between measured and predicted f_t is off by a factor of approximately 1.57.

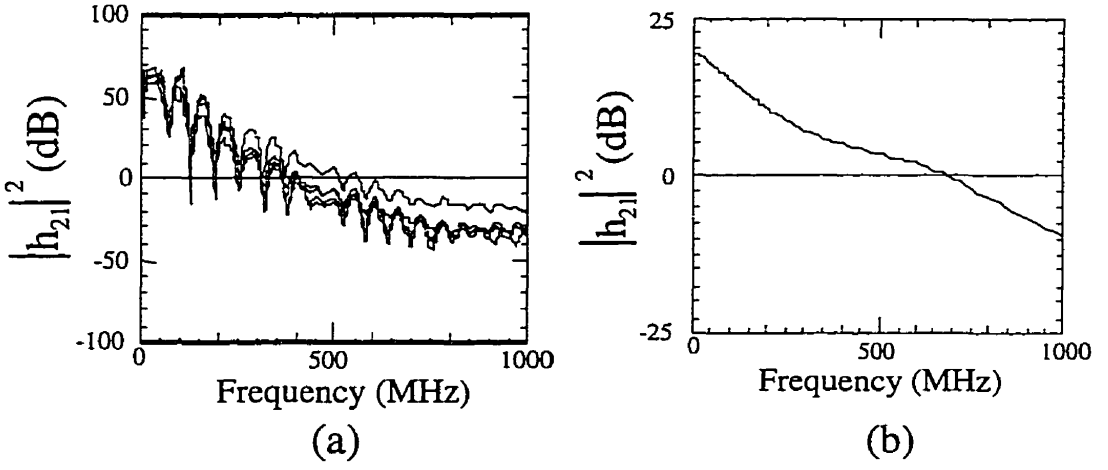
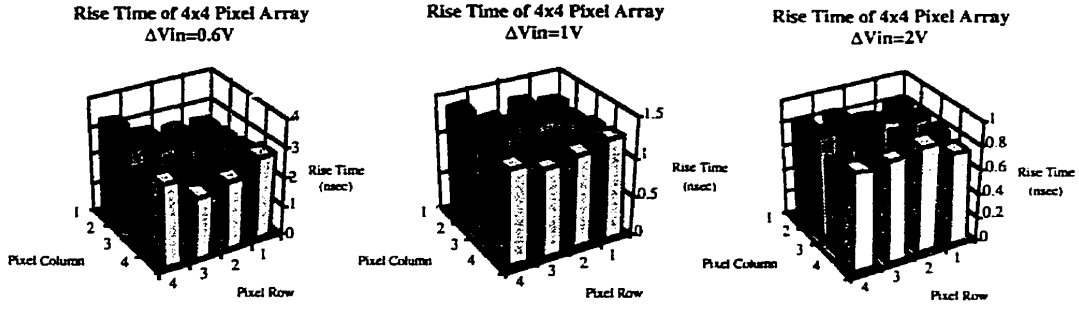


Figure 2.13: (a) Measured h21 values for 5 receivers and (b) model prediction

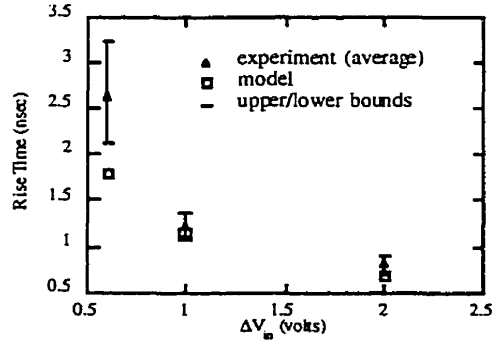
2.4.2 Characterization of the Modulator Array

High frequency measurements are performed on the transmitter circuits by applying 400 MBit/sec digital signals to the gate of the switching transistor. Individual optical beams are used to read out the state of the modulator pair, the reflected light being focused onto a fast photodiode (t_{rise} = 21 nsec) to monitor the switching speed. For these measurements, the 4x4 array is biased at V_{dd} = 7.3 volts and V_{ss} grounded, and the incident power on the transmitter modulators is 290 μW. The 400 MBits/sec input signal is applied at three voltages, 0.6, 1.0 and 2.0 volts peak-to-peak. The experimentally measured rise times of the 16 modulators in the array are shown in Figure 2.14a for the three different input voltages. Figure 2.14b shows the bound of the risetime variations for the three input voltage swing after deconvoluting the appropriate detector response. The variation in risetimes across the array can be as much as +/-20% of the average value. From Figure 2.14, it can be seen that $t_{rise,ave}$ = 1.22 nsec, and $t_{rise,ave}$ = 0.84 nsec at V_g = 1.0 V, and 2.0 V, respectively. The 3 dB bandwidths, calculated using $f_{3dB} = 2.2/2t_{rise}$, is found to be f_{3dB} = 291 MHz, and f_{3dB} = 432 MHz at V_g = 1.0 V, and 2.0 V, respectively, and the unity gain bandwidth is determined to be f_o = 1.51 GHz, and f_o = 2.04 GHz, assuming an output

swing of 7 volts and input swing of V_g = 1.0 V and V_g = 2.0 V, respectively. These measurements are in close agreement with values obtained by Lentine et al [2.20]. The rise times presented in this paper are approximately 3 times larger than those of [2.20], primarily due to the larger modulator size (25 x 25 μm versus 10 x 10 μm). Using the model described by Lentine et al., it can be shown that the rise time is given by CV_o/DI_{FET} (if photocurrent is ignored) where C is the total output capacitance, V_o is the output voltage across a MQW, and DI_{FET} is the difference in current between the load and switching transistors as the output begins to change state. The capacitance in this experiment is approximately 12 times greater due to the larger modulators, but the difference in current was approximately 4 times larger owing to the fact that the transistors are equally sized. Combining these two differences, the rise time is expected to be approximately 3 times larger than [2.20], as measured.



(a)



(b)

Figure 2.14: Risetimes versus input swing

This circuit is modeled using the device and interconnect models described in section 2.1. Figure 2.15 shows both the experimentally measured (solid) and modeled (dashed) reflectivity change of a modulator driven at 1 GHz with 2.0 V peak-to-peak drive

voltage. In addition to the electronics, we modeled the SEED devices with a current source in parallel with a capacitance. The current source depended linearly on the optical power thus the I-V characteristic could be described using a simple look-up table [2.11], and the capacitance was assumed to be $0.115 fF/\mu m^2$ [2.12]. The transmitter is simulated with a 100μW optical input on both modulators. Based on this model, the predicted rise times where as follows: t_{rise} = 1.14 nsec for V_g = 1.0 V, and t_{rise} = 0.68 nsec for V_g = 2.0 V. Using these values, the following are found: a 3 dB bandwidth of f_{3dB} = 307 MHz and f_{3dB} = 515 MHz, and unity gain bandwidths of f_o = 1.53 GHz and f_o = 1.65 for V_g = 1.0 V and 2.0 V respectively. As can be seen, these results are in good agreement with the experimentally measured circuit rise times, 3 dB bandwidths, and unity gain bandwidths cited above.

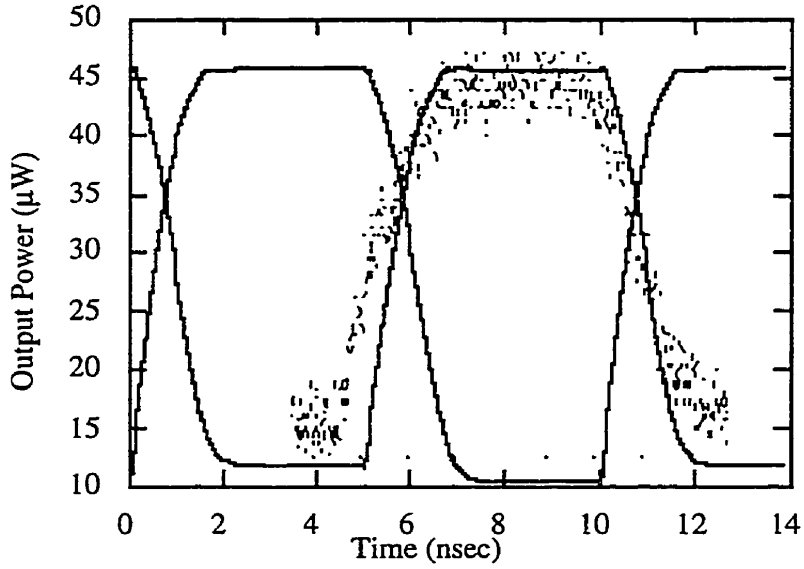


Figure 2.15: Typical measured (solid) and modeled (dashed) reflectivity change

The array was also tested for electrical crosstalk in order to measure the electrical isolation between adjacent on-die trace lines. This measurement is performed by driving one transmitter circuit and measuring the voltage crosstalk on the adjacent addressing trace line. A 2.0 V square wave is applied to a transmitter, and this transmitter's nearest neighbor input is monitored using a 50 ohm terminated digitizing scope. 20 mV spikes are induced by these addressing signals. This voltage crosstalk is attributed to parasitic crosstalk in adjacent signal lines. Similar measurement are performed on next-nearest neighboring lines, but no detectable voltage crosstalk is found.

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Chapter 3: Epitaxy-on-Electronic Transceivers

This chapter discusses the use of epitaxy-on-GaAs technology to design 2-D arrays of optical transceivers. Epitaxy-on-(GaAs) Electronic (E-o-E) technology is a monolithic technology developed at the Massachusset Institute of Technology (MIT) [3.1]. Unlike the FET-SEED technology discussed in the previous chapter, the fabrication of the optical devices and of the electronic devices occur almost independently. GaAs/AlGaAs optical devices are grown lattice matched on fully processed commercial VLSI GaAs fabricated at Vitesse Semiconductor Corporation. Studies have shown that the degradation of the electronic devices is minimal after the growth of the optical devices [3.2]. Thus commercial VLSI GaAs is fully taken advantage of in the creation of VLSI optoelectronics. E-o-E VLSI optoelectronics is produced in four steps [3.3]. The first step involves the design of the circuits and the definition of selected areas reserved for epitaxial growth. The second step is the fabrication of the GaAs electronics at Vitesse, and the etch of the selected areas to expose the GaAs surface. Cuts are opened where selected in the overglass of the standard Vitesse GaAs. The Vitesse process has a passivation etch to remove the top overglass protective layer and a scribe line etch [3.4]. Both etches are used and an additional cleaning etch is performed resulting in the exposure of the GaAs surface. These cuts are called Dielectric Growth Wells or DGW [3.3]. During the third step, the epitaxial layers are then grown in the DGW. Materials are deposited everywhere on the chip by molecular beam epitaxy (MBE). However, epi-layers are grown only in the DGW where they are seeded by the GaAs surface. A polycrystalline material is deposited everywhere else (on the top of overglass and bond pads). Finally, after a planarizing polycrystalline etch, the optical devices are formed, and interconnection with electronic circuits are made.

The following devices can be grown in the DGWs [3.2]: light emitting diodes (LEDs) [3.5], long wavelength (>870nm) metal-semiconductor-metal (MSM) detectors (this is in addition to the shorter wavelength MSMs available on the standard Vitesse run), vertical-cavity surface-emiting lasers (VCSELs), and modulators. This potential flexibility makes the E-o-E technology attractive for the design of VLSI optoelectronic systems. This chapter focuses on the first step, namely the design. It presents the design of E-o-E circuits that may eventually be used in an optical interconnection system such as a backplane. The details of the other steps can be found elsewhere [3.3].

In this chapter test circuits designed for the OPTOCHIP [3.6] project are described. In the next section, the OPTOCHIP project is described. In section 3.2, the design of dynamic receivers is discussed, and compared with other GaAs receivers such as the diode-clamped (discussed in chapter 2), and the TIA receiver. In section 3.3, the design of a LED-based transmitter is presented. Finally, section 3.4 summarizes and concludes.

3.1 The Designs on OPTOCHIP

OPTOCHIP [3.6] is a multi-project chip that offers E-o-E optoelectronics to circuit and system designers. The devices available to the designers are: E-o-E integrated LEDs, Vitesse HGaAsIII standard process MSMs and OPFETs, and VLSI GaAs E/D MESFETs. The OPTOCHIP is divided into nine user groups each receiving a 2mmX2mm sub-chip for optoelectronic circuit design. A sub-area is reserved for DGWs for characterization, and for other cells for process control monitor. The following lists the projects which were implemented [3.6]:

"Optoelectronic Neural Array"
Jean-Jacques P. Drolet and Demetri Psaltis
California Institute of Technology, Pasadena, CA

"An OPTOCHIP for an Optoelectronic Connectionist Correlation Network"
Carl W. Wilmsen, Mahmood Azimi, Rick Snyder, and Eric Hayes
Colorado State University, Fort Collins, CO

"Integrated Source/Detector Array for Free-space Optical Interconnection Prototype Demonstration Systems"
Michael W. Haney, Marc P. Christensen, and Shaktish Acharya
George Mason University, Fairfax, VA

"Dynamic Smart Pixels for high-capacity backplanes"
Alain Shang and Frank Tooley
McGill University, Montreal, Canada

"Controller Interface for a Distributed Ensemble of Remote Sensors"
Lily Cheng, Edward Kolesar, and Stephen Weis
Texas Christian University, Fort Worth, TX

"Optoelectronic Error Diffusion Neural Network"
Barry L. Shoop, Eugene Ressler, Andre Sayles, James Loy,
Gergory Tait, Daniel C. Gray, Bryan S. Goda, and
James H. Wise
United States Military Academy, West Point, NY

"Optical Multi-channel Interconnection Network Interface using Monolithic Optoelectronic Integrated Circuits"
Timothy Pinkston
University of Southern California, Los Angeles, CA

"Smart Pixel Array Systems for Parallel Data Processing"
Alexander A. Sawchuk and Charles Kuznia
University of Southern California, Los Angeles, CA

"Multiplicative Lateral Inhibition Neural Networks (NLINN)"
W. Randall Babbit
University of Washington, Seattle, WA

The "Dynamic Smart Pixels for high-capacity backplanes" project is described here. The goal of this project is to explore the suitability of E-o-E technology for the implementation of large transceiver arrays for a high throughput backplane system. Such a system requires large 2-D arrays of digital transceivers which are efficiently and intimately interfaced with in-situ digital processing electronics. The I/Os perform processing tasks such as encoding/decoding, route multiplexing, control structures, ATM header processing, communication protocol handling and so on. Smart detectors and circuitry that implements alignment strategies can also be introduced into the 'smart pixel' (see Chapter 4). The scalability of the array is an important issue for the implementation of large cross-section bandwidth systems. The sensitivity and electrical power consumption of these interconnects are usually traded off. For moderate sensitivities (1-10's of μW), the major impediment to scalability becomes power consumption. Therefore it is important to reduce the electrical power consumption of transceivers. Low-power receivers and associated circuits have been designed for the OPTOCHIP.

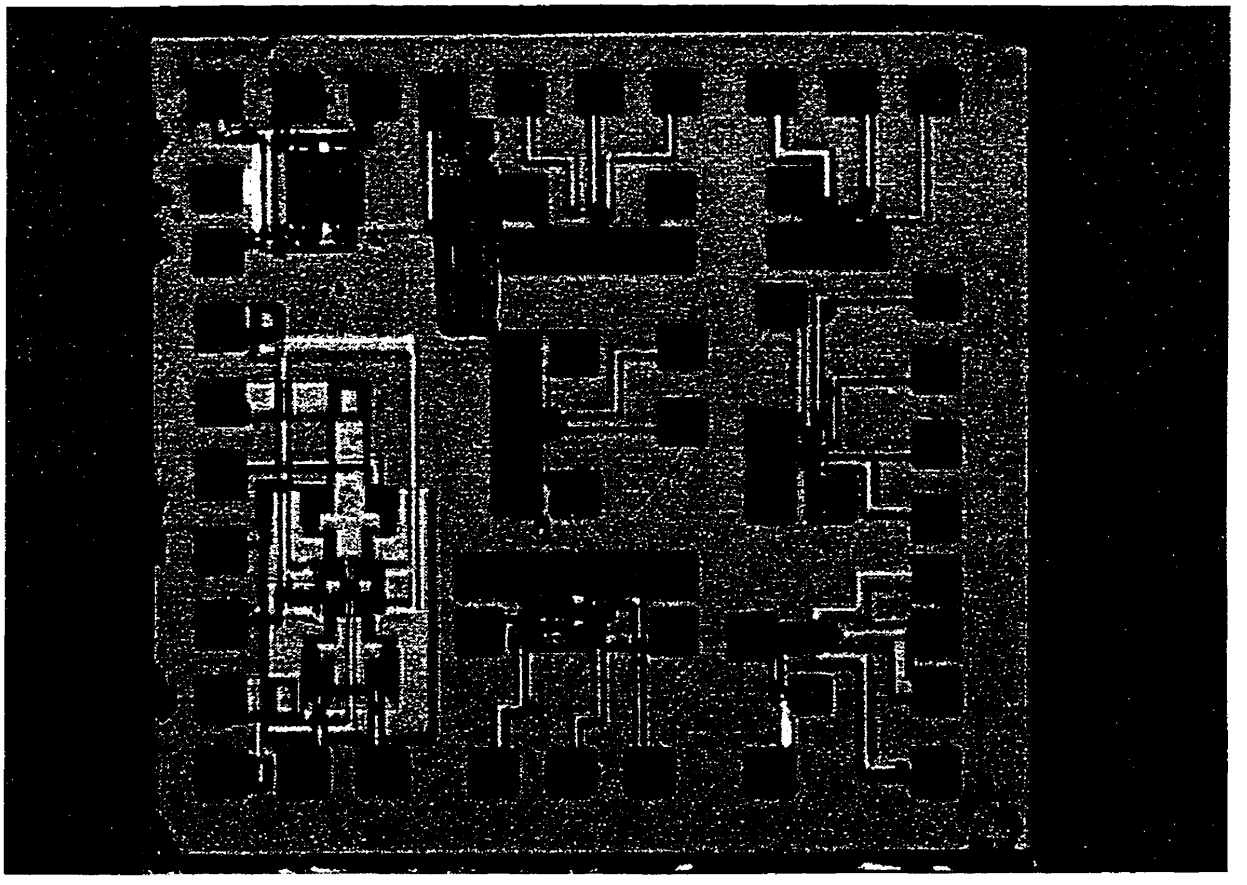


Figure 3.1: Photomicrograph of the OPTOCHIP (sub-chip)

An array of receivers and transmitters, and six test circuits are designed. Figure 3.1 shows the sub-chip. The test cells include two designs of dynamic receivers, a clock driver, two designs of transimpedance amplifier (TIA) receiver, and one of a LED driver. The dynamic and TIA receiver cells are layed out in two ways: 1) electrical IN and OUT (see for example Figure 3.2), and 2) optical IN and electrical OUT (see for example Figure 3.3). The power supply pads are not shown in Figure 3.2 and Figure 3.3. The optical input is provided by a 20μmX20μm MSM as shown in Figure 3.3. Such layouts enable the full testing and characterization of the receiver both electrically and optoelectronically. The IN and OUT pads are 100μmX100μm and they are each 150μm apart from a ground pad. This pitch is chosen to match that of a CASCADE™ high-speed probe with signal/ground pitched at 150μm. The power is supplied to each cell independently. Power and ground pad exist for each test cell. Integrated MSM photodetectors serve as the optical inputs. Off-chip photodetectors can also be wirebonded to the IN pad.

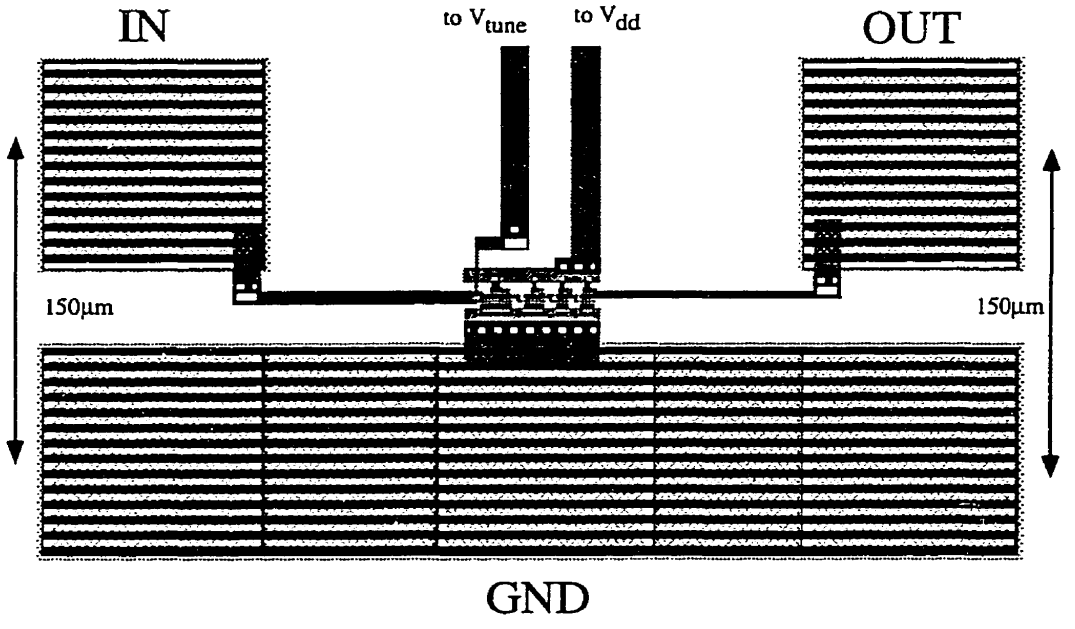


Figure 3.2: All-Electrical Cell

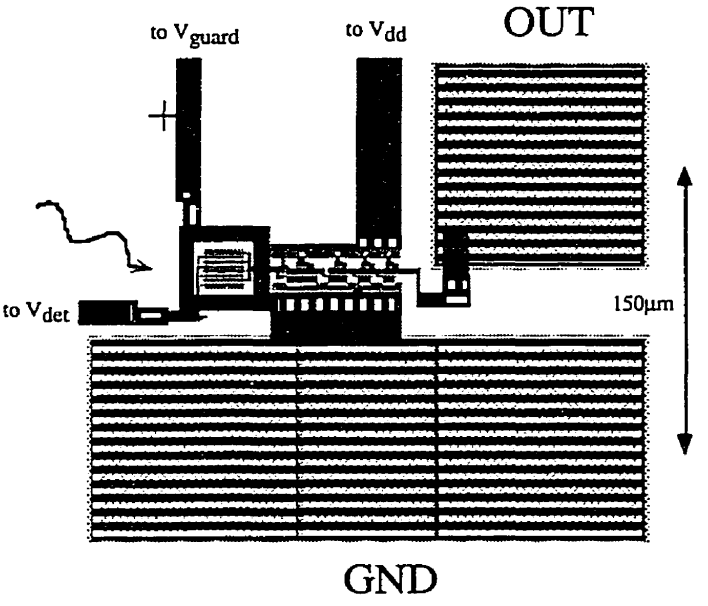


Figure 3.3: Opto-Electronic Cell

In addition, a receiver and a transmitter array are designed:

1) A 2X2 MSM array is pitched at 90μm. The MSMs are 20μmX20μm. The TIA receivers are each followed by a SBFL driver that can drive a few femtofarads of capacitive load.

2) A 2X2 LED array is pitched at 90μm to match that of the receiver. The driver consists of a switch FET connected in series with the LED.

The layout of these arrays are shown in Figure 3.4 and in Figure 3.5, respectively. The LEDs and MSM are designed to implement a clustered interconnect. In the following sections the design of the test receivers and transmitters are discussed.

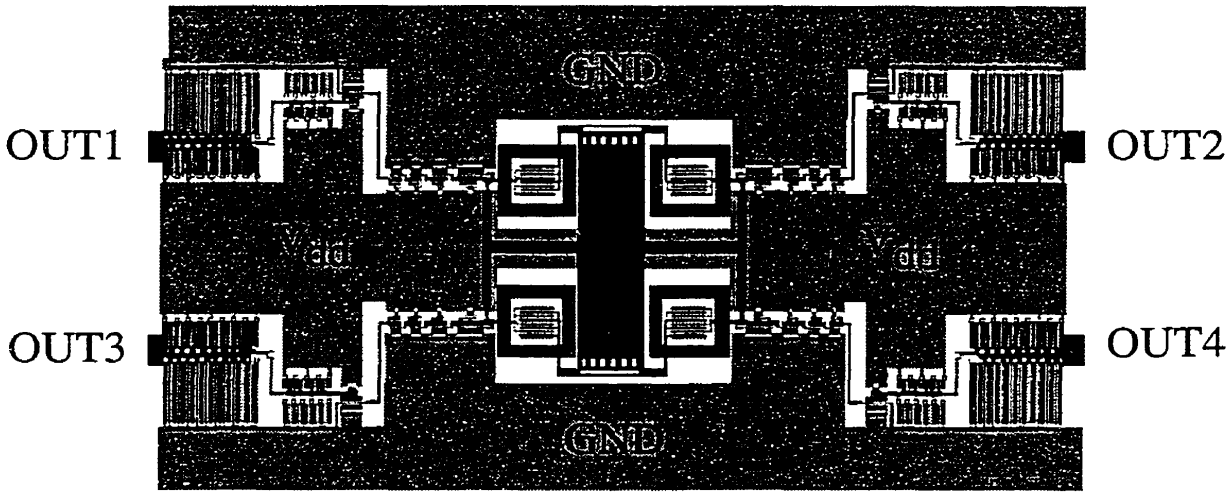


Figure 3.4: MSM array

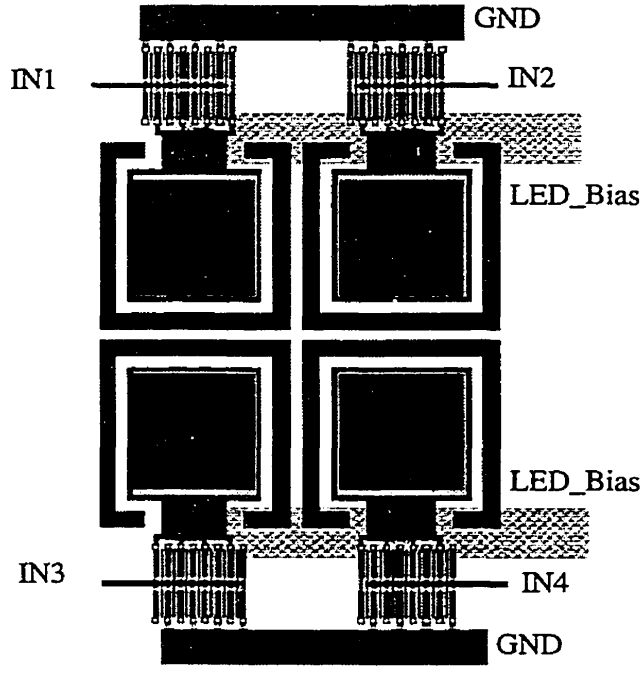


Figure 3.5: LED array

3.2 GaAs Receiver

The receiver provides amplification and serves as an interface between the optically encoded data and a GaAs digital logic such as DCFL [3.7] or BFL [3.7]. The optical signal is converted into a photocurrent by the detector, and fed into the input of the receiver which converts the photocurrent into a voltage, and amplifies it. In this section the design of a MSM photodetector is discussed. Following that, three receivers are presented. The discussion of the receiver mainly focuses on the power consumption. Power consumption is important for two main reasons: 1) it is key for array scalability and 2) it has been one of the major drawbacks of GaAs receivers [3.7].

3.2.1 MSM Detectors

Optical FETs (OPFETs) can be used as a high-gain (e.g. sensitivity of 2000A/W) detector. However this bandwidth is very low (few KHz bandwidth [3.3]). Since speed is very important for a backplane receiver, metal-semiconductor-metal (MSM) photodetectors are preferred since they are typically high-speed. The MSM is fabricated with the standard Vitesse process steps (GaAs/AlGaAs) and it is sensitive to wavelength≤880nm (the bandgap of GaAs ~870nm). It is made by interdigitating two sets of metal fingers to form Schottky-barrier contacts to the underlying GaAs. The finger widths and spacings are optimized for light collection efficiency and responsivity. To maximize the light collection efficiency, the fingers are typically narrow. The metal electrodes are not transparent although some transparent [3.8] and semi-transparent [3.9] fingers have been proposed. On the other hand, to increase the responsivity and lower the bias voltage of the device, the fingers are closely spaced to yield a high E-field between fingers. For semi-insulating GaAs, a low bias (2V) can fully deplete the regions between the fingers. For the Vitesse HGaAsIII process, all active areas receive an ion implantation. Consequently a higher bias (~5V) is required to deplete the regions between the fingers. An additional mask step could shield the MSMs from the implantation [3.10]. This mask was not available at the time of the design.

Concurrently, the finger widths and spacings are designed to optimize the 3dB bandwidth which is given by

$$\frac{1}{2\pi\sqrt{t_{tr}^2 + (RC)^2}}$$

where t_{tr} is the transit time across the fingers and RC is the RC time constant of the MSM structure. To optimize the bandwidth, both the transit and the RC time need to be reduced together [3.11]. If the finger width is too small, the structure becomes highly resistive, and the bandwidth suffers. On the other hand, decreasing the spacing reduces the transit time, t_{tr} but increases the capacitance, C and decreases the bandwidth.

The MSM used for the receivers has seven 1.2μm wide fingers with a 1.6μm spacing covering an active area of 20μmX21.2μm. This fabricated device has a low parasitic capacitance of 0.1 to 0.2fF, a dark current of <100nA, a good quantum efficiency of 35-40%, and a sensitivity of 0.27-0.37 A/W for wavelength < 870nm. Although MSMs can have high-responsivity, a good percentage of the active area is covered by the metal fingers. In this design example about 40% of the active area is hidden by the fingers. The risetime (delay) due to the MSM is shorter than 0.3 nsec [3.12]. A guard ring surrounds the MSM to isolate it from the rest of the chip, and protect it from backgating [3.3, 3.7].

3.2.2 DCFL Receiver

The main drawback of the BFL diode-clamped receiver discussed in the previous chapter is its high power consumption. Receivers which consume a lower power have been proposed, an example can be found in the DCFL resistive load receiver [3.13]. Power consumption (and incidentally the area consumption) is lower when using DCFL rather than BFL [3.7]. However their sensitivity is generally not as good as a diode-clamped receiver. A receiver with a better sensitivity can be found in the transimpedance amplifier-based (TIA) receiver. The design of a TIA is described in section 3.2.4. Its power consumption is comparable to the resistive load receiver. To achieve a high-speed (i.e. nsec and sub-nsec response), MSMs are used. A *clocked DCFL receiver* with a MSM at its input is proposed here. Figure 3.6 shows the receiver topology. M1 is an EFET, and M2 and M3 are DFETs. A clock signal is used to reset the gate of M1 at every clock cycle in a way similar to AROEBICS receivers [3.14]. The input impedance of this receiver, like the diode-clamped one, is very high when CLK2 is low (M3 is off). During that time, the photocurrent provided by the MSM charges the gate capacitance to a voltage that switches the input EFET M1. When CLK2 is high, M3 is on and the gate of M1 is grounded. The timing diagram for this receiver is shown in Figure 3.7. This is to be contrasted with the resistive load receiver where the input resistance is much lower, or with the TIA which has

an impedance value in between the resistive load and the high-impedance receivers. Usually a high-impedance front-end requires equalization [3.15] to achieve a high bandwidth. In the case of the diode-clamped and clocked DCFL receiver, bandwidth is achieved by limiting the input voltage rather than using area and power hungry equalization filters. Instead of using diode-clamps to limit the input voltage, the clocked DCFL receiver limits the voltage by shorting at every clock cycle the input node to ground using a pass transistor M3 (see Figure 3.7).

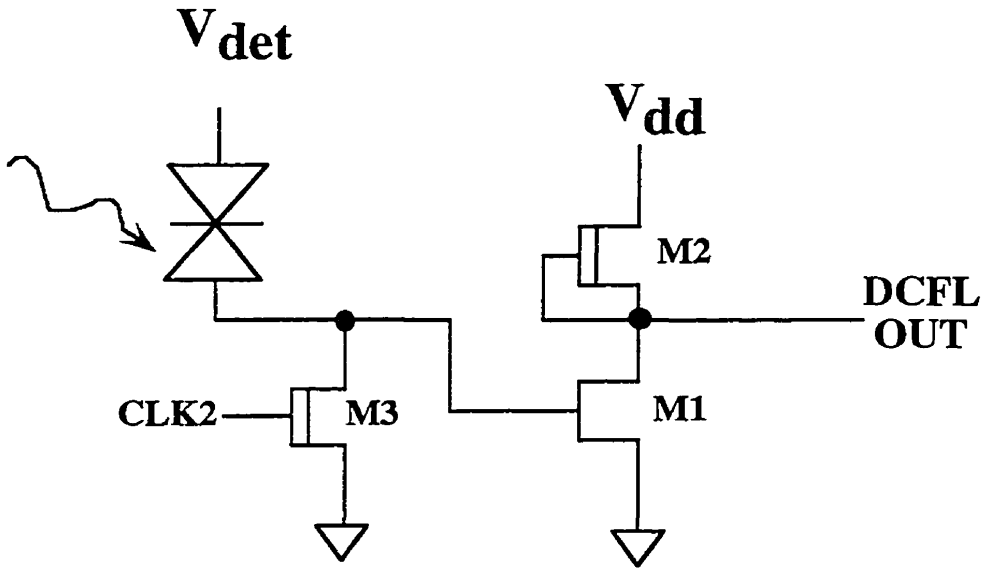


Figure 3.6: Clocked DCFL receiver

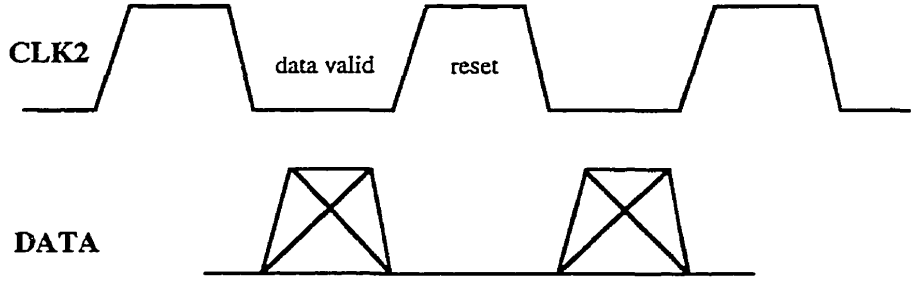
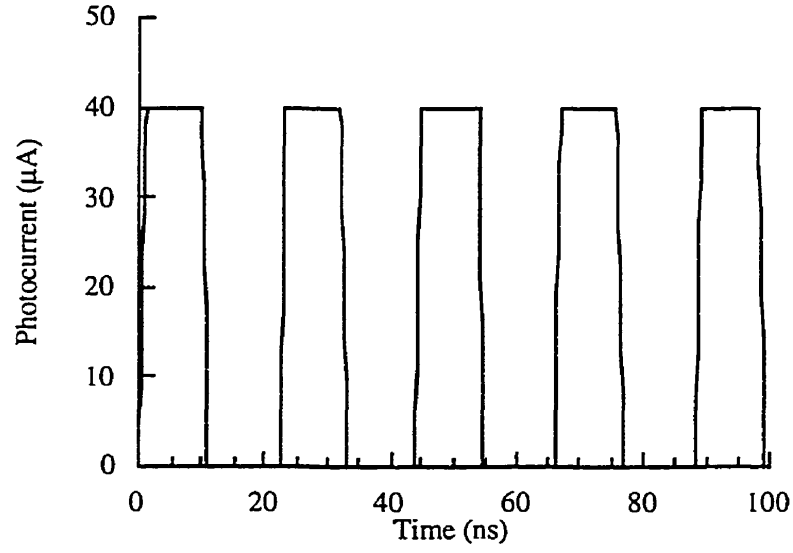


Figure 3.7: Timing diagram of DCFL receiver

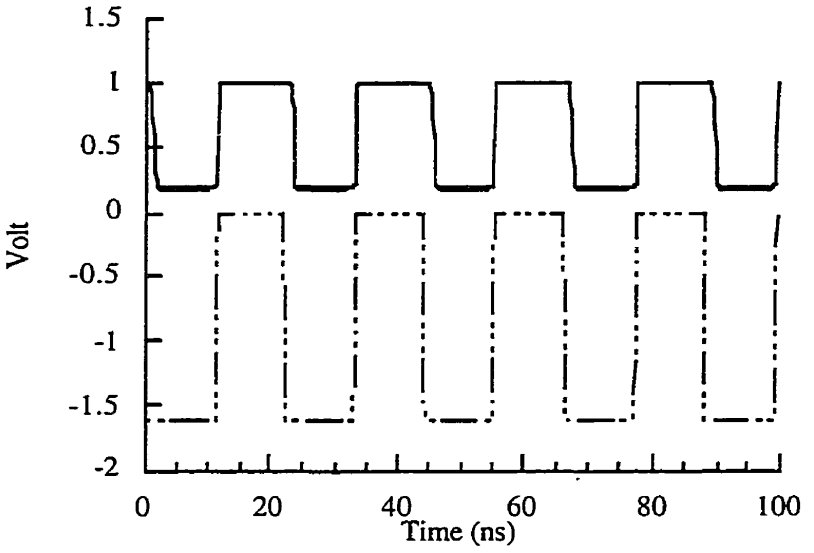
The diode-clamped and the dynamic receiver achieve high sensitivity using the attribute of an integrating input node. The sensitivity of a diode-clamped receiver can be adjusted with the diode-clamp biases. They properly bias the input voltage swing with respect to the amplifier switching point, and control the input voltage bias point and its swing. Similarly the clock signal in the clocked DCFL receiver ensures that the voltage swing at the input

gate of M1 is returned to ground at each clock cycle, and that the swing is limited. Thus the clocked DCFL receiver has a similar (and even for some case lower) sensitivity compared to that of the BFL diode-clamped receiver. In general, there is a sensitivity dependence on bit rate or speed due the finite time to (dis)charge the input node capacitance.

The clocked DCFL receiver consumes a low power which is similar to that of the DCFL resistive load receiver. The DCFL clocked receiver is more compact than the diode-clamped receiver due to the absence of diodes. The area can be as small as $1000\mu m^2$ with a GaAs technology compared to $4480\mu m^2$ for a FET-SEED diode-clamped receiver. The overhead of the clock is mitigated if the same clock (or an easily derived one) can be used to run the digital electronics. The other drawback of a clocked receiver is the reduction in bit rate caused by assigning a portion of each clock cycle to reset the voltage at the input node. In general, all clocked receivers have this drawback (see next section on dynamic receivers, and the current-mode sense amplifier based receiver in Chapter 4). A simulation of the clocked DCFL receiver at 50Mb/s is shown in Fig.3.8. The output (solid line in Figure 3.8) is resetted at each clock cycle to ~1V. The input bit is always 'high' and the output of the receiver is pulled to 'low'. The power consumption is 0.45mW. The sensitivity is 40μW at a speed of 155Mb/s.



(a)



(b)

Figure 3.8: Simulation of the clocked DCFL receiver (a) Input data (b) Received data (solid line) and clock (dashed)

3.2.3 GaAs Dynamic Receivers

Although the receivers discussed above consume an electrical power 3 to 6 times less than that of the diode-clamped receiver , the power consumption can still be prohibitive for a large array (e.g. 32X32). The main contributor to the electrical power consumption is the static flow of current in the analog front-end and in the GaAs digital static logic gates. The alternative to static GaAs logic is dynamic logic. For example two-phase Dynamic FET Logic (TDFL) [3.16], differential Pass-Transistor Logic (DPTL) [3.17], or domino logic [3.18] have been used to design low-power VLSI digital circuitry. Some GaAs dynamic logic families consume 10 times less power than their static counterparts, and 0.8μm linewidth, 5V CMOS [3.16].

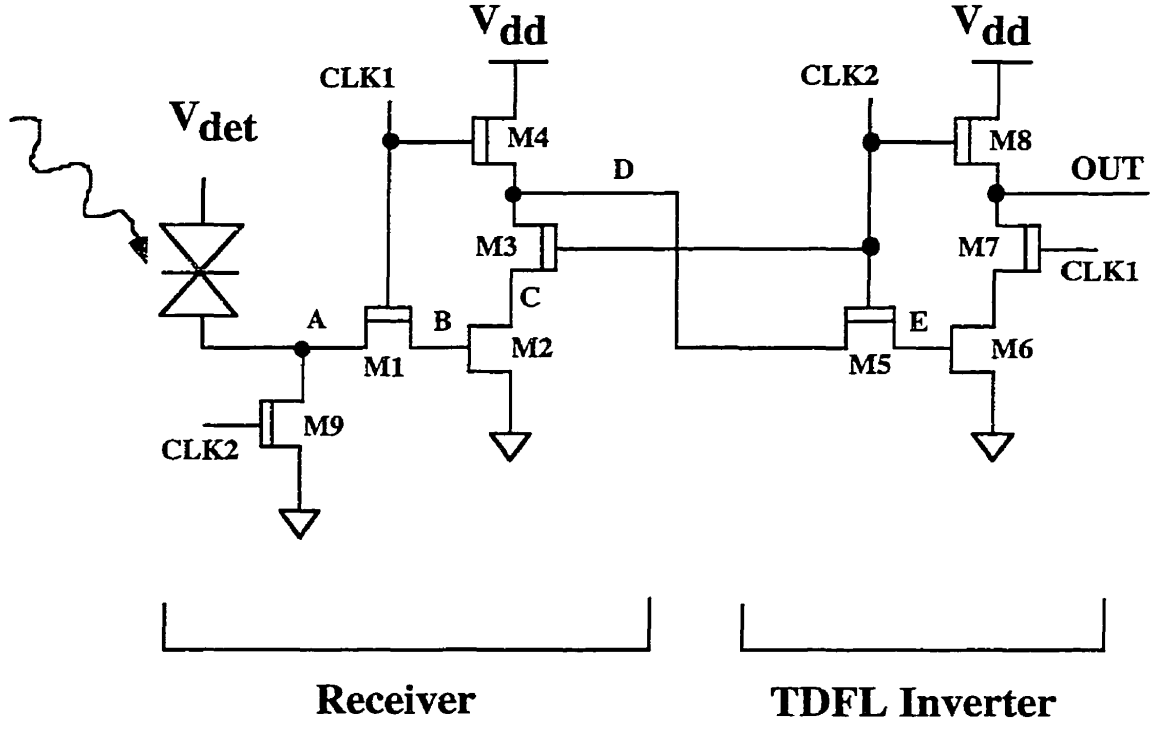


Figure 3.9: Dynamic (clocked) receiver

Here *dynamic (clocked) receivers* are proposed in order to eliminate the static power dissipation in the analog front-end. The dynamic receiver consumes less power and less area than their static counterparts. Figure 3.9 shows a design inspired by a TDFL gate. The front-end is similar to the receiver discussed in the 3.2.1. However the receiver instead of using a DCFL gate uses a TDFL gate. The TDFL receiver works as follows. Clocks CLK1 and CLK2 are 180 degrees out of phase. Consider the receiver front-end of Figure 3.9. The DFET have a threshold voltage of -1.1V and the EFET of +0.05V. When the CLK1 is high, CLK2 is low and M1 and M4 conducts. M3 is off, cutting the path to ground. M5 in the second stage is also off and it isolates the first from the second stage. The output of the receiver at node D is charged up to about V_{dd}. Nodes A and B in the meantime are charged to about 0.5V (the barrier potential) if there is photocurrent, or kept at 0V if there is no photocurrent. Node A has been discharged to ground in the preceding clock cycle when CLK2 was high. Now when CLK1 goes low, CLK2 goes high and M3 and M5 conduct. If node B had been charged high when CLK1 was high then M2 conducts, and the output at D is discharged. On the other hand if node B had been low, then M2 is off and the output remains high. Note however that the high is determined by the gate-to-source conduction of the EFET of the next stage, M6. This potential is about

0.5V. Charge sharing between node C and E also plays a role in determining this voltage [3.16].

Since dynamic receivers store charges on isolated circuit nodes, the design of nodal capacitance becomes a key issue in dynamic designs. When the node D is charged up to high, a charge $Q_D=C_DV_{dd}$ is brought onto that node. When CLK1 becomes low and CLK2 high, this charge is shared by node C and E. So that the voltage becomes

$$V_H = \frac{Q_D}{\left(C_C + C_D + C_E + C_{gsM6}\right)} = \frac{C_D V_{dd}}{\left(C_C + C_D + C_E + C_{gsM6}\right)} \tag{3. 1}$$

where C_i is the capacitance at node i, and C_{gsM6} is the gate-to-source capacitance (of the Schottky barrier). Assuming that there is no gate diode leakage, a high is close to V_{dd} if and only if:

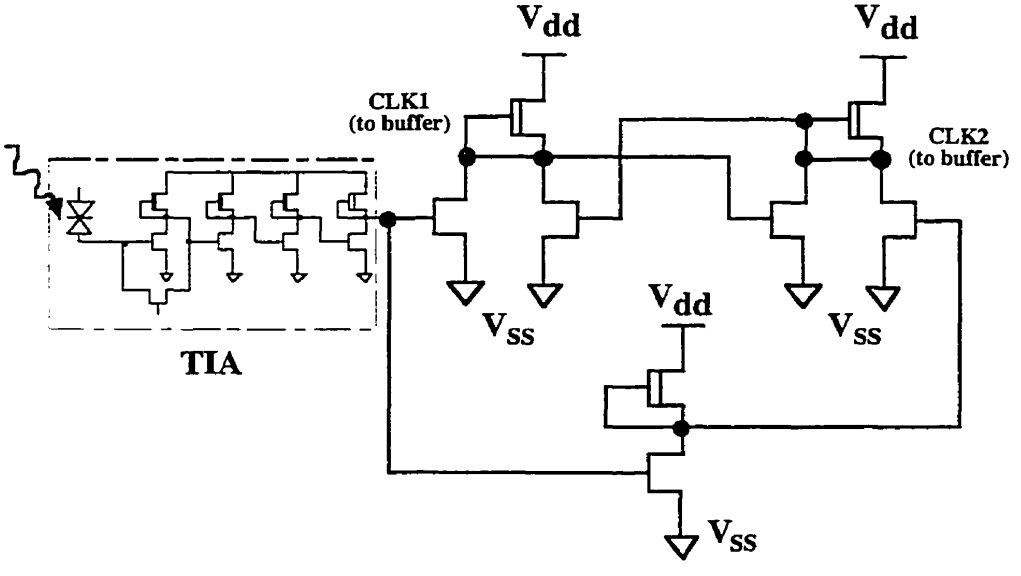
$$C_D \geq C_C + C_E + C_{gsM6} \rightarrow 0 \tag{3. 2}$$

However the final potential is determined by the charge leakage through M6, and settles at about 0.5 or 0.6 volts. It is important to maximize the voltage swing as much as possible. The larger the input voltage swing is, the lower the drain-to-source resistance of the input EFET M6 thus decreasing the RC time of the second stage. A large EFET width suggests a short discharge RC time for the ouput node D, while charge sharing concerns suggest a narrow width EFET. If the capacitive load at node D is large, charge sharing is not an issue, and a large EFET can be used to minimize the RC discharging time. Charge sharing will become an issue for a certain EFET width. The charging DFETs M4 (and M8) are minimum size but may be larger for large output loads.

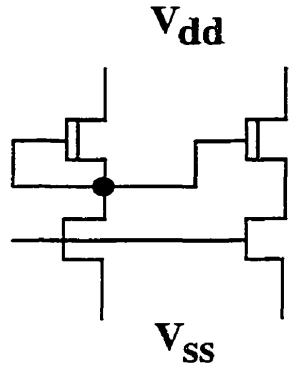
Another design issue is raised by the capacitive coupling between the clocks and the isolated nodes of the gate (e.g. node B). When node B has been charged to 0.5V and CLK1 goes low, a displacement current through the capacitance existing between node B and node CLK1 produces a voltage drop on B. To minimize this drop, the input pass transistor M1 is minimum sized to decrease the coupling capacitance between node B and

CLK1. On the other hand, when node B is discharged and CLK1 goes low, the displacement current pulls the potential at B below 0V. This reduces the subthreshold current in M2 and turns it off completely.

To operate the receiver, two clocks need to be generated. A two-phase optical clock driver is designed to drive a 200fF capacitive load. This driver can supply clock signals to 40 receivers each loading the clock driver with a characteristic minimum gate capacitance of 5fF. The clock is generated optically and the driver generates the two phases for the operation of the dynamic receiver. The clock driver consists of a TIA receiver at the front-end followed by cross-coupled NOR gates and a buffer that drives the fanout load to all the receivers. The design is shown in Figure 3.10. The bias rail V_{dd}=0V and V_{ss}=-1.5V. The biasing is chosen according to the DFET pass transistor threshold which is -1.1V. The TIA is the same design as described below. DCFL is used to design the cross-coupled NOR gate which generates the two complementary phases, CLK1 and CLK2. The SBFL [3.7] or a BDCFL [3.4, 3.7] driver can be used for driving large capacitive loads. For this design, a SBFL driver is modified slightly to pull the output up to V_{dd}. The modification involves replacing the pull-up EFET in the second stage of the SBFL driver by a DFET. A simulation of the optical clock driver with modified SBFL drivers is shown at 500Mb/s in Figure 3.11. The power consumption is about 1mW. There is in fact a power overhead of about 25μW per TDFL receiver. The effect of this overhead can be amortized if this clock can be shared with the VLSI digital logic clock(s).

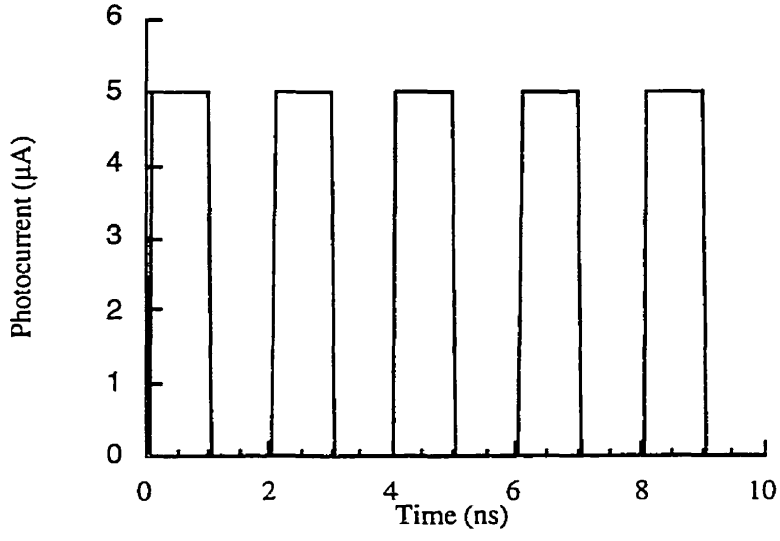


(a)

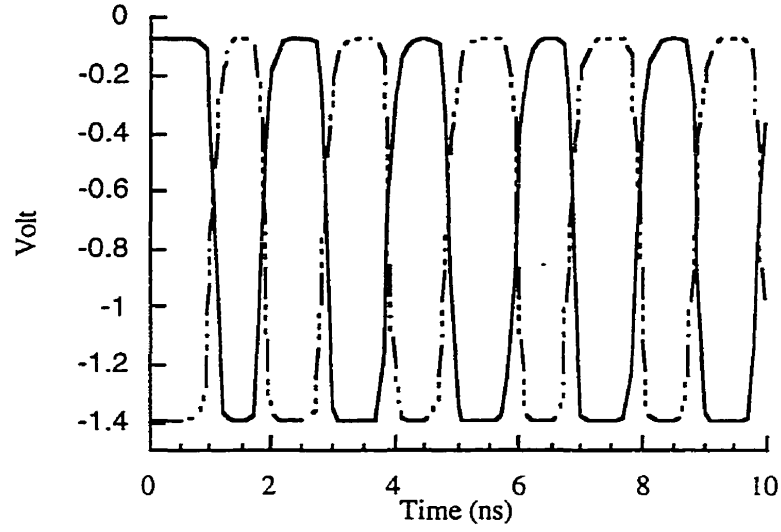


(b)

Figure 3.10: (a) Optical clock generator (b) Output buffer.



(a)

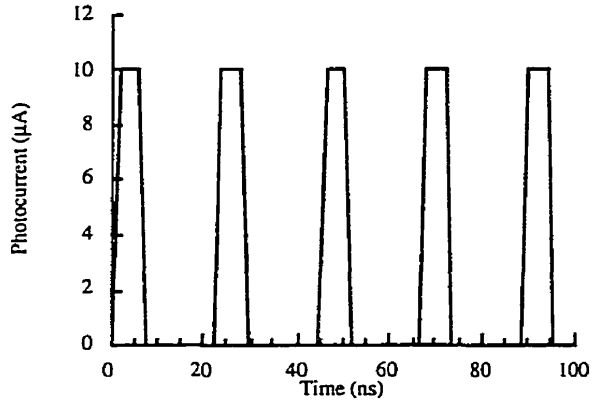


(b)

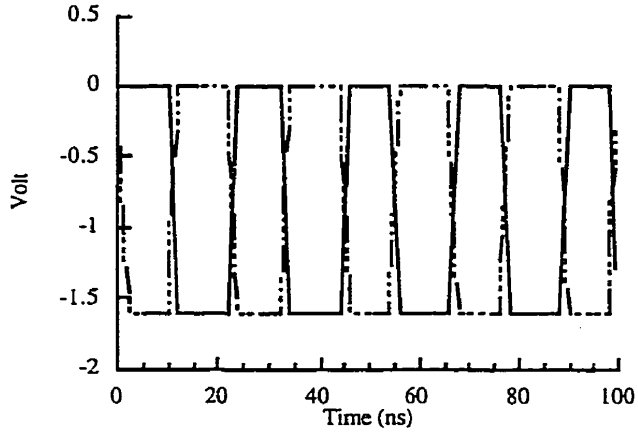
Figure 3.11: Simulation of optical clock generator (a) optical clock signal (b) electrical output (two phases)

Figure 3.12: Photomicrograph of the dynamic receiver

A fabricated one-stage dynamic receiver is shown in Figure 3.12. The MSM on the left of the photograph has an area of 20μmX20μm, and a capacitance of ~50fF. The area of the receiver is 47μmX47μm. A simulation of the TDFL receiver at 50Mb/s is shown in Figure 3.13. The power consumption is only due to switching and it is 40μW at 155 Mb/s. The sensitivity at that speed is around 5μW.



(a)



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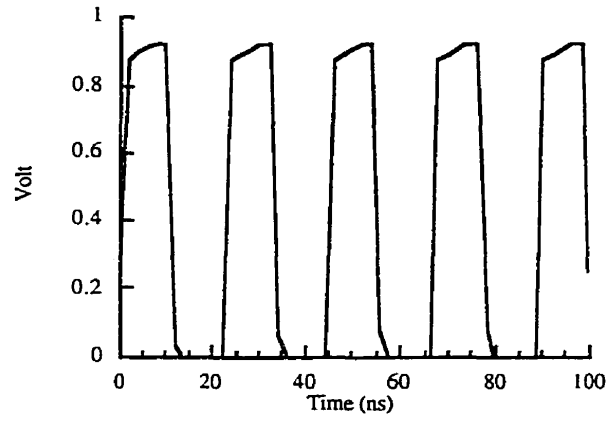


(c)

Figure 3.13: Simulation of the dynamic receiver (a) input (b) 2 phase-clock (c) output

3.2.4 TIA Receivers

A transimpedance amplifier (TIA) is used to provide a wider bandwidth and dynamic range than an integrating front-end [3.15]. It also has a good sensitivity. However the TIA consumes more electrical power than the dynamic receivers.

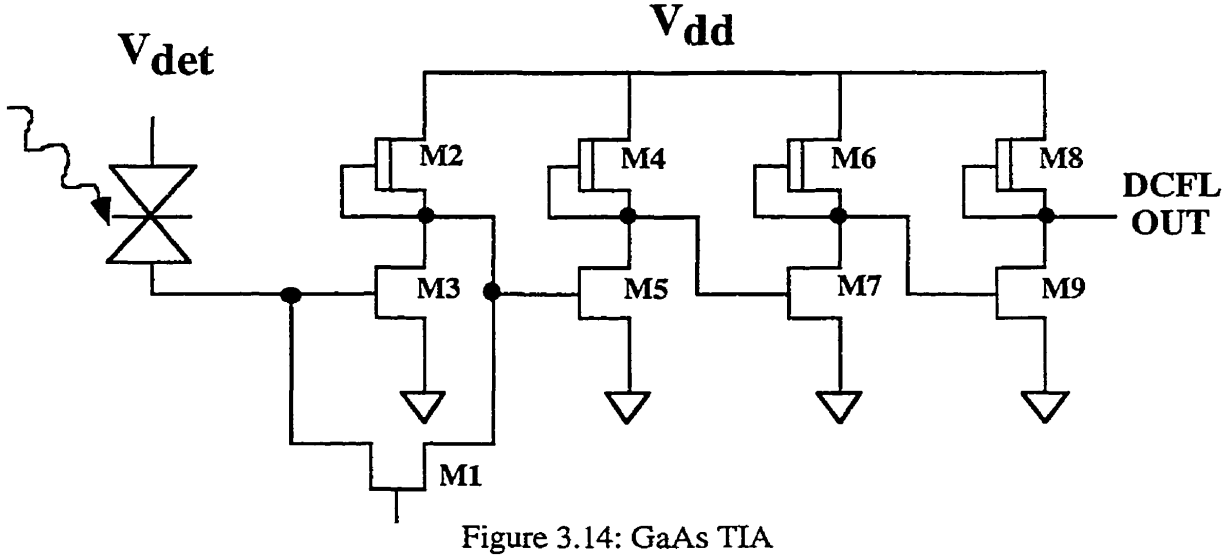


Figure 3.14: GaAs TIA

This section presents a high-sensitivity TIA. The TIA design is shown in Figure 3.14 (V_{dd}=1V). The fabricated receiver is shown in

Figure 3.15. The width to gate length ratio (W/L) of DFETs M4, M6, and M8 are 2μm / 2μm. The W/L for the EFETs M5, M7, and M9 are 10μm / 1μm. The EFET M3 and DFET M2 have W/L=14μm/1μm, and 4μm/2μm, respectively. The TIA has an active feedback in a EFET 2μm wide with a 2μm gate length. The total layout area of the TIA is about 30μmX70μm. The bias at the gate permits the tuning of the transimpedance to some extent. Since there is not space for a sophisticated AGC circuitry, the active feedback provides enough dynamic range when used with a controlled optical source. The layout is extracted and simulated. The results of the simulation is shown in Figure 3.16 demonstrating 500Mb/s operation. At 155Mb/s, the power consumption for this receiver is about 600μW and the sensitivity at this rate is 5μA of photocurrent.

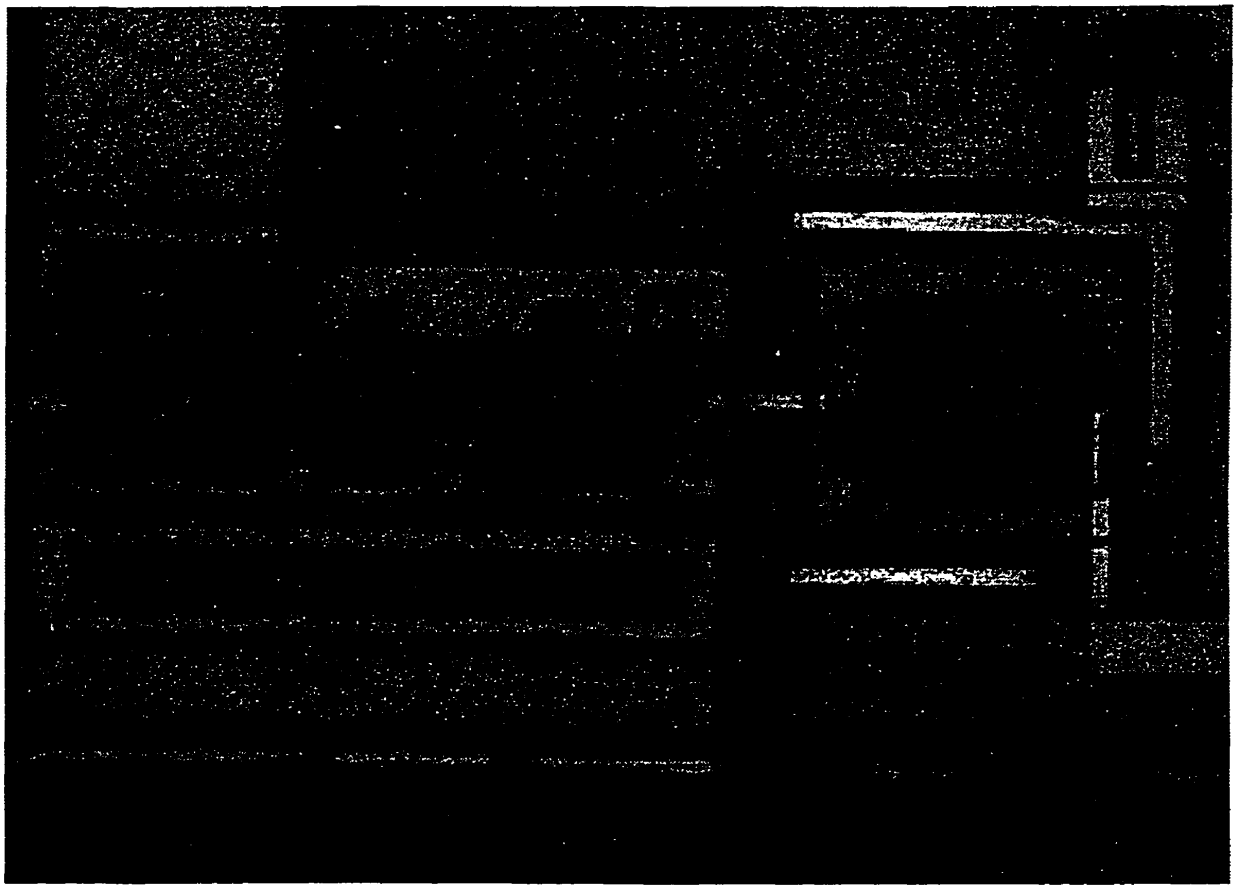


Figure 3.15: Photomicrograph of TIA-based receiver

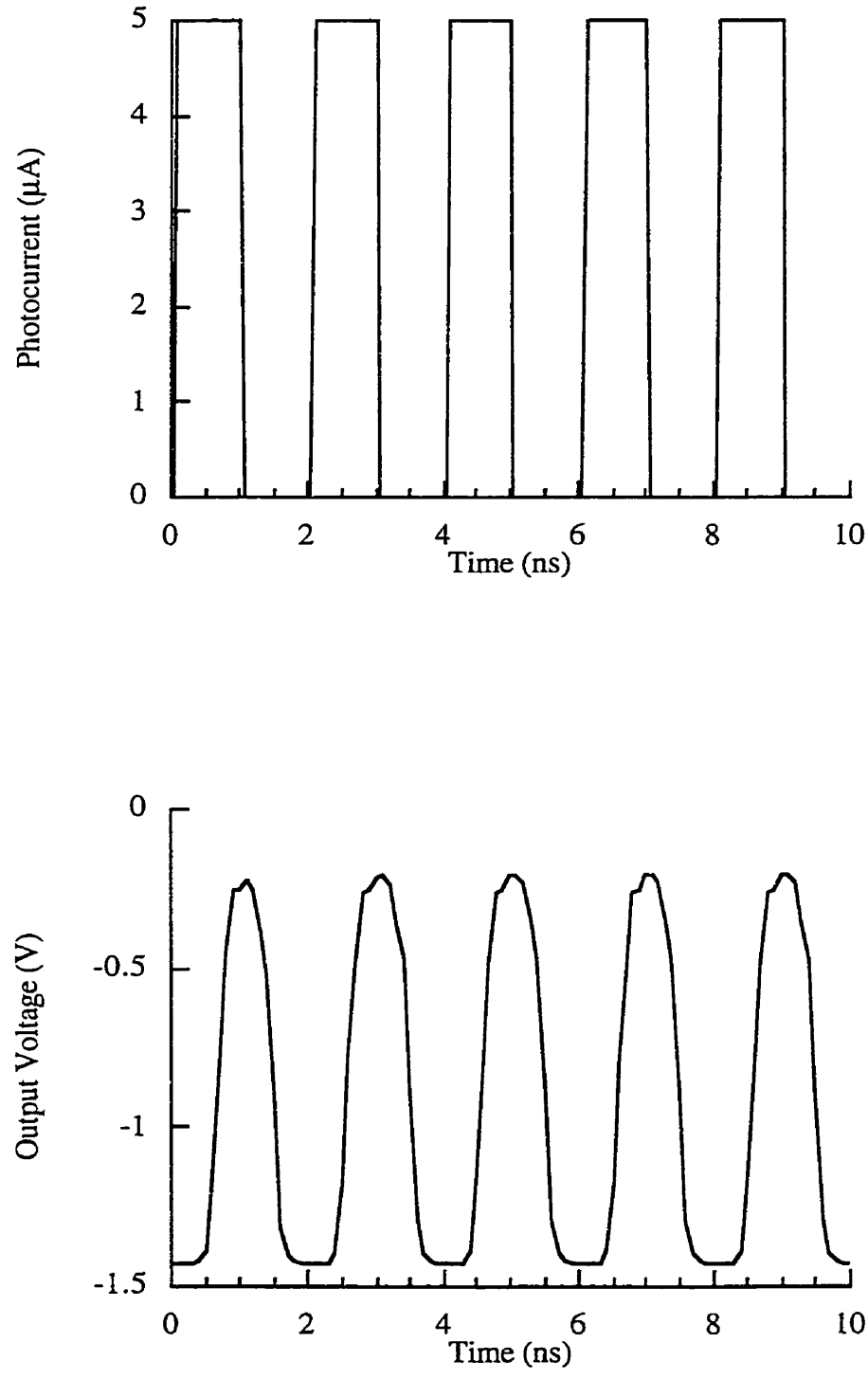


Figure 3.16: Simulation of GaAs TIA

3.3 LED based transmitters

LEDs are grown in 50μmX50μm DGWs. A fabricated LED is shown in Figure 3.17. The actual size of the device is slightly smaller. MIT provides the 'optical bond pads' [3.6] which can be dropped in anywhere in the layout. The only additional design rule to the Vitesse rules [3.4] specifies that nothing can be less than 5 μm away from the DGW [3.12]. The LED is a GaAs/InGaP double hetrostructure [3.2]. The emission comes from spontaneous emission in the GaAs core. The bandgap of GaAs is 1.42eV which corresponds to a 873nm emission wavelength. The LED spectrum is shown in Figure 3.18.

Figure 3.17: Fabricated LED

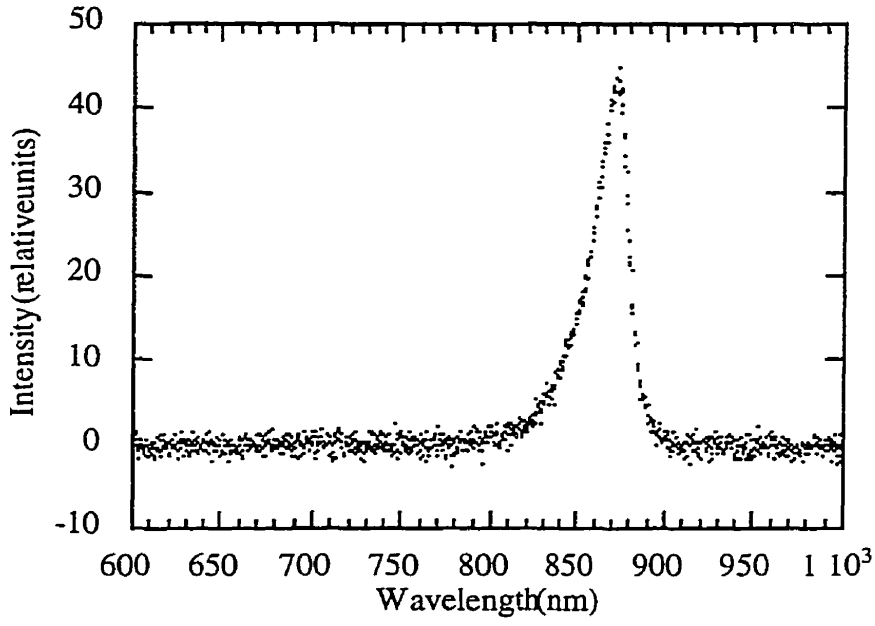


Figure 3.18: LED spectrum

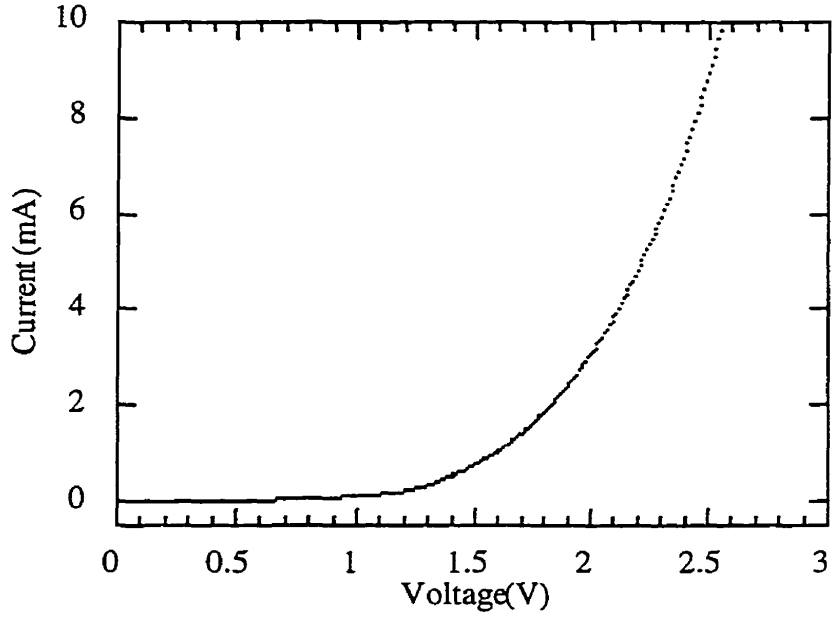
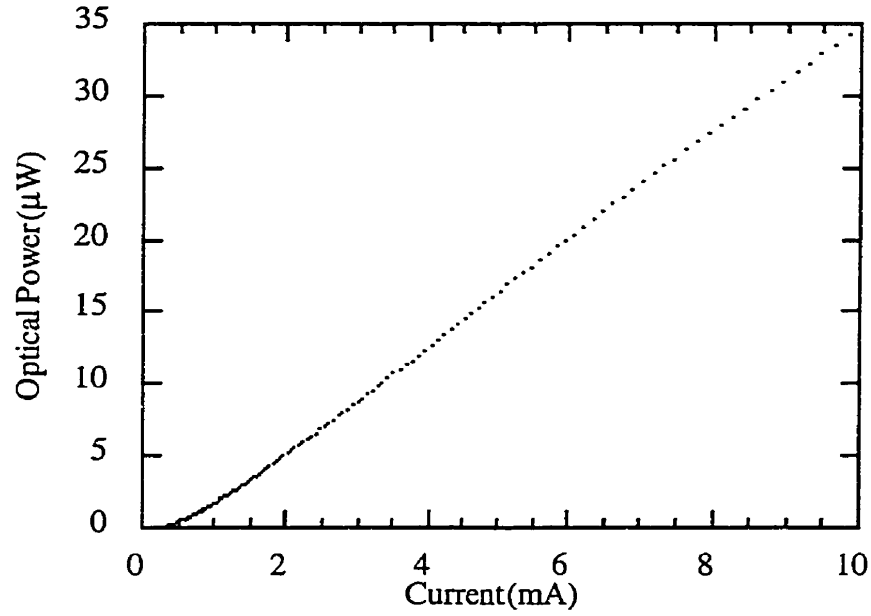


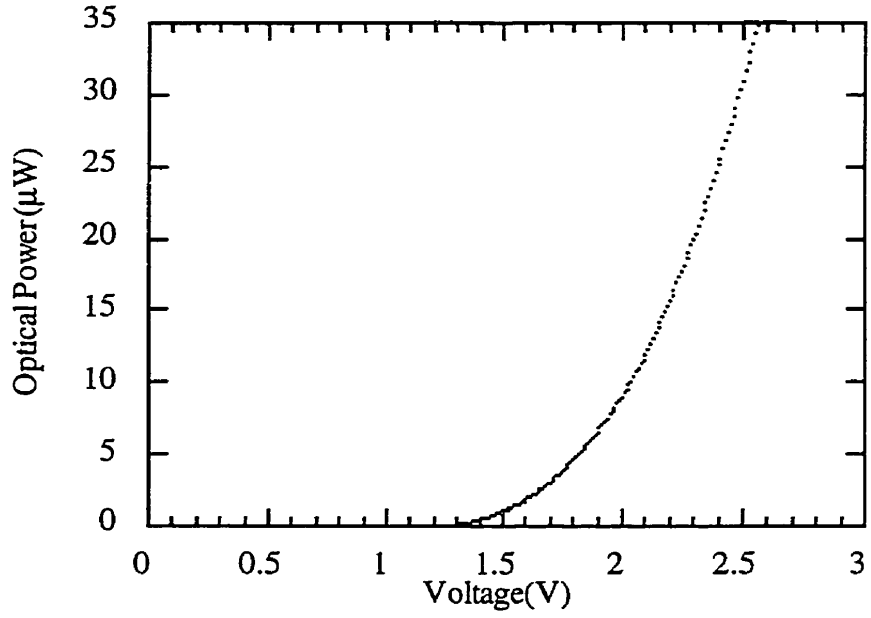
Figure 3.19: LED I-V characteristics

The I-V characteristic is shown in Figure 3.19. For simulation purposes, the LED I-V characteristics can be modelled by a resistor in series with a DC turn-on voltage. It is deduced from Figure 3.19 that the turn-on voltage is 1.2V and the resistance is about 100Ω-140Ω. A wider ohmic contact to the LED makes the "turn-on" sharper because of a lower resistance. The LED used here has a 3μm wide ohmic contact [3.12]. Since the LED

can be voltage or current driven, it is instructive to consider the LED's L-I and L-V curves. These are shown respectively in Figure 3.20a and b.



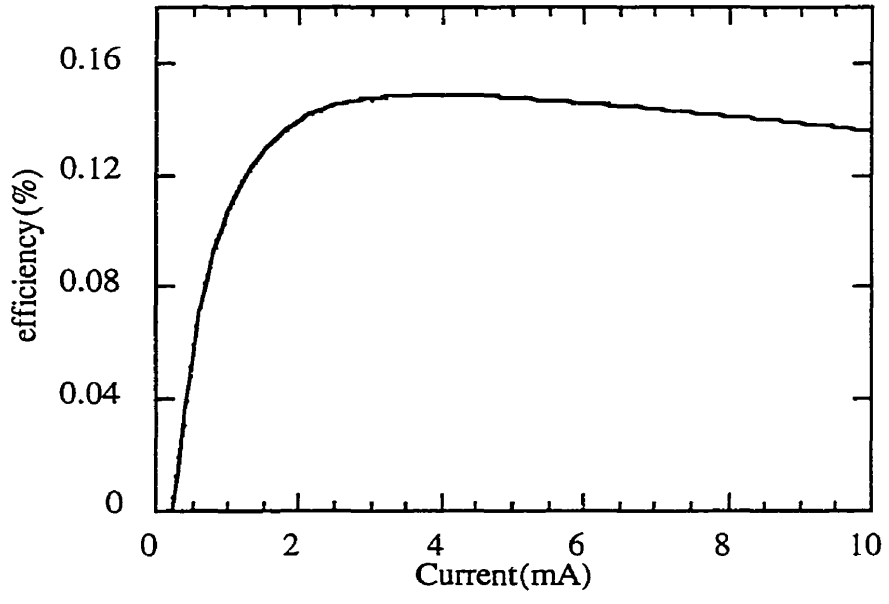
(a)



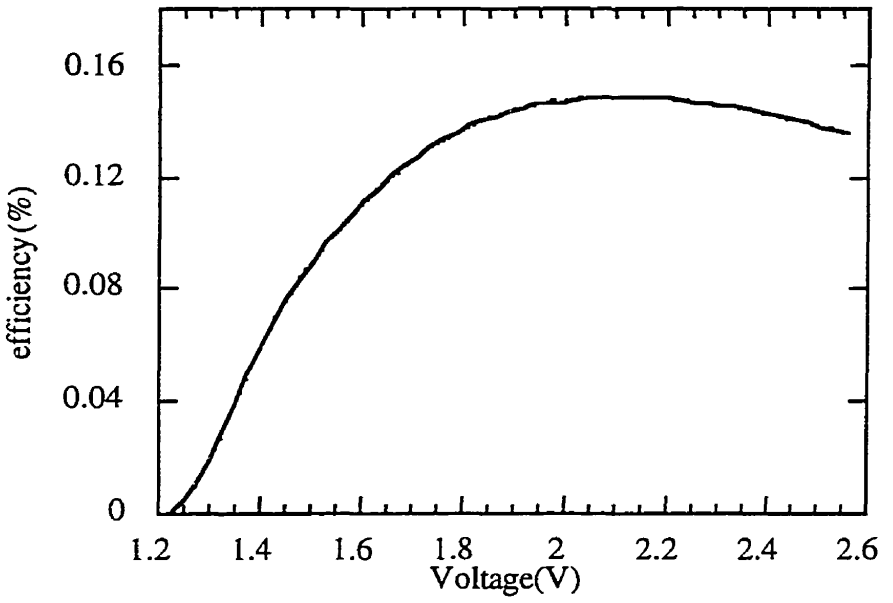
(b)

Figure 3.20: LED output optical power

The power efficiency as a function of voltage and current is shown in Figure 3.21. The efficiency is optimum for a drive current of 3.9mA or a voltage of 2.1V. The power consumption corresponding to the drive current and voltage is shown in Figure 3.22. For the optimum efficiency (i.e. 0.148%), the power consumption is 8.3 mW, and the optical power is 12.3μW. This optical power is however too little since optical power in excess of the receiver sensitivity (1-10s of μW) is required to compensate for the optical interconnect and the misalignment losses. The power consumption of these transmitters do not compare favorably with modulator-based ones (see Chapter 4). The average on-chip electrical power consumption of a transmitter based on a quantum confined stark effect modulator is ~1mW/Gb/s [3.19]. Thus, the low efficiency of this LED makes the implementation of large arrays difficult. Furthermore the Lambertian beam divergence complicates the collection of light and may introduce optical crosstalk in dense arrays. These LEDs may find a application in a single point-to-point link with a small optical losses and a high-sensitivity receiver.

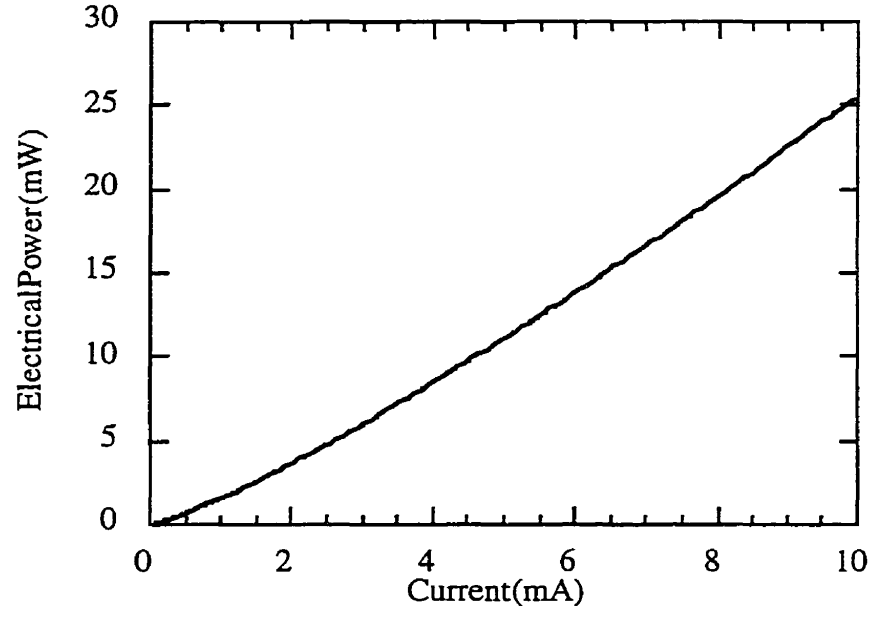


(a)

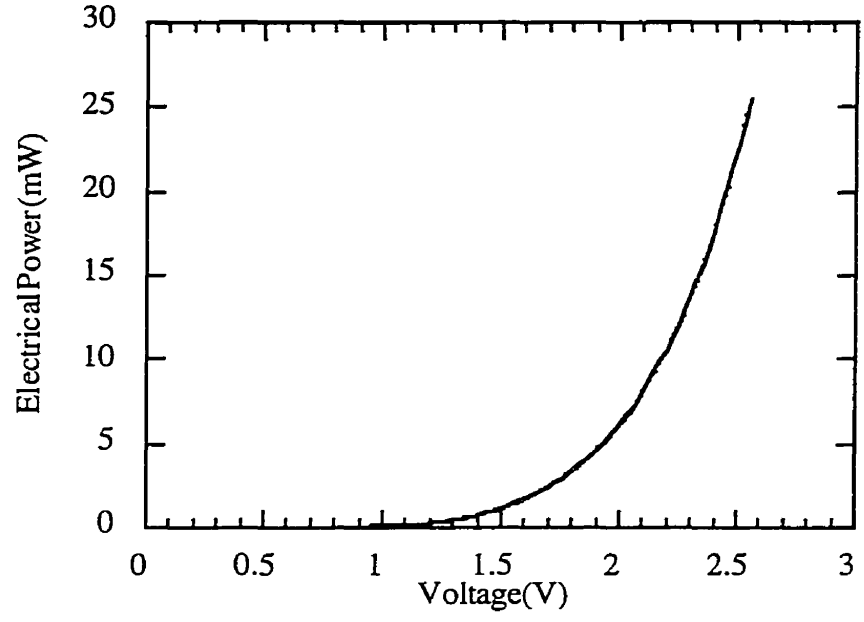


(b)

Figure 3.21: LED efficiency



(a)



(b)

Figure 3.22: LED electrical power dissipation

A digital driver is shown Figure 3.23. It consists of a pull-down EFET which swiches the LED on and off. A simulation of this driver is shown in Figure 3.24.

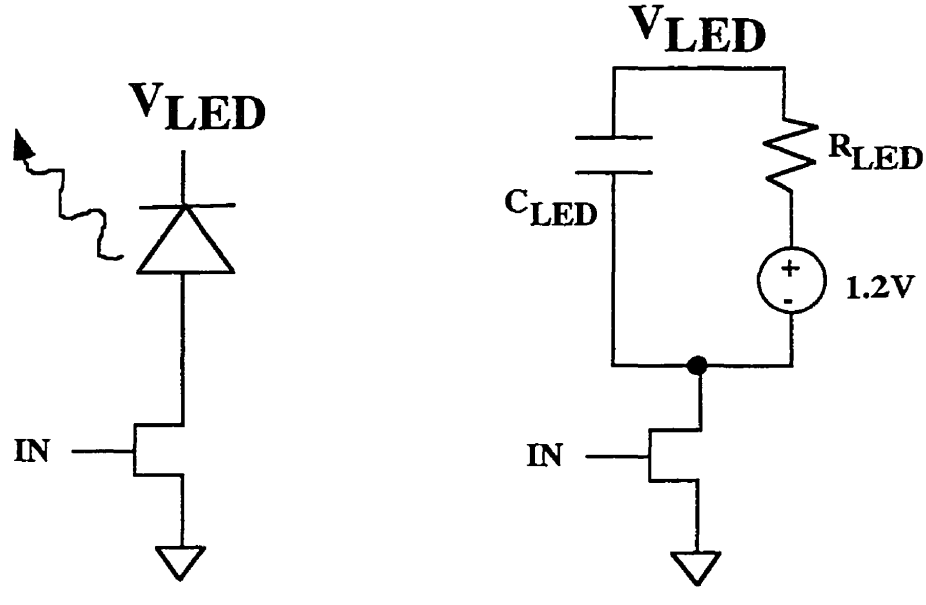


Figure 3.23: LED driver(s)

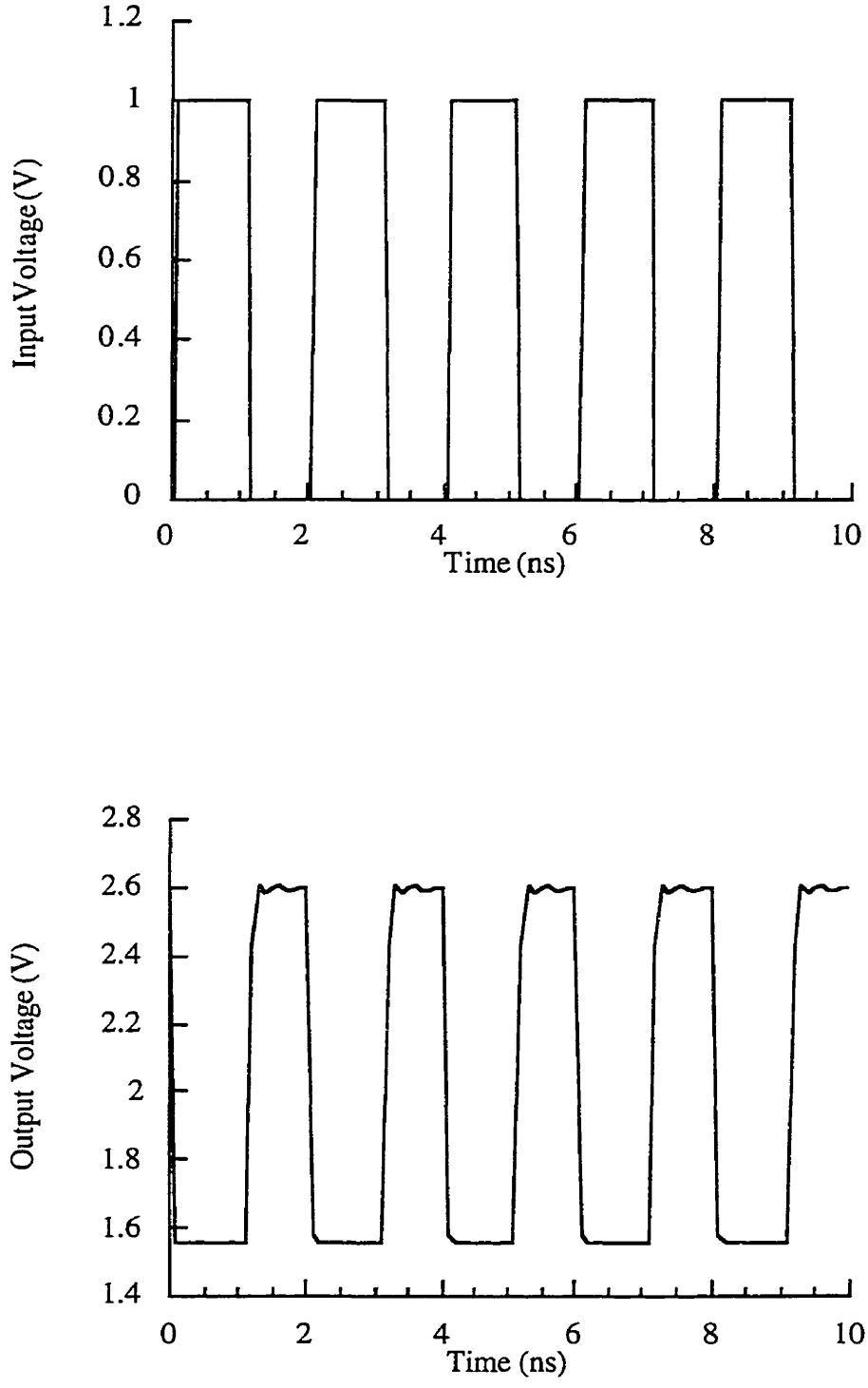


Figure 3.24: Driver simulation

3.4 Conclusions

To conclude, the clock dynamic receivers can reduce the power dissipation significantly of each receiver in the array. The clock that is needed for the operation of these receivers is a small overhead. Its sensitivity is high, second only to the TIA receiver. Moreover this receiver is compact. In non-feedback receivers, the sensitivity comes with the integrating front-end. The reduction in electrical power consumption is achieved by using lower power gate families such as DCFL, and by using a dynamic approach cutting the static current path to ground. In the TIA, the sensitivity is improved over all the non-feedback ones. Table 3.1 summarizes the receivers key characteristics for backplane applications. All receivers have a bandwidth which allows them to operate at moderate bit rates (100's Mb/s to Gb/s). The bandwidth is quite high for all of them due to their simplicity. The bandwidth is highest for the low-impedance resistive load receiver. The bandwidth of the TIA is next highest. The other receivers are high-impedance and consequently a small bandwidth is expected if no equalization is provided. However the diode clamps and the clock allows the receiver to operate at a speed comparable to the two previous receivers, and without equalization. In terms of sensitivities, the highest sensitivity receiver are the high-impedance receivers (diode-clamped, clocked and dynamic DCFL) and the lowest is the low-impedance resistive load receiver. The TIA normally has a sensitivity between the high and the low impedance front-end. Because the high-impedance receiver limits their voltage at the input, the sensitivity is not as high as it would be for a normal high-impedance front-end. It turns out that they are lower than the TIA.

GaAs Receiver	Power Consumption (mW)	Sensitivity (μW)	Area (μm^2)
Resistive Load (DCFL) [3.13]	0.5	94	1280
Diode-Clamped (BFL)	2.8	66	4480
Clocked DCFL	0.45	40	1000
Dynamic TDFL	0.04	10	2209
TIA	0.6	5	2100

Table 3.1: GaAs receiver comparison for a bit rate of 155 Mb/s .

The LED output optical power is too low and its electrical power consumption too high for reliable application for a backplane. Furthermore its wide beam divergence makes

the collection and focusing of emitted light difficult, and crosstalk is too high. A higher optical power LED would be desirable, and integrated VCSEL with a low threshold would be ideal for the application considered here.

The chip has been designed with testing in mind. The test cells can be easily probed and characterized electrically and optically. Wirebond pads have been used to attach photodetectors to their receiver or LEDs to their driver. Pads have also been used to take the high-speed signal on and off the chip. Typically these pads rather than the VLSI transceivers will limit the operating speed if on-board or inter-chip signal communication is needed.

3.5 References

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Chapter 4: Hybrid Optoelectronic CMOS Transceivers

In this chapter, the design of VLSI optical I/Os using GaAs Optoelectronics-onto-CMOS is presented. The technology employed consists of a flip-chip attach of p-i(MQW)-n diodes (reflective mode) to CMOS circuitry with a subsequent removal of the GaAs substrate [4.1]. This technology takes advantage of the low-power and the high density of CMOS, and the mature flip-chip (C4 attach) technology. Being a hybrid technology, the design of the optoelectronic devices can be optimized independently from the electronic circuitry. These characteristics of the technology help, with appropriate transceiver design, to implement the large 2-D arrays of optical I/O required by the high-capacity interconnect systems.

This chapter focuses on circuit techniques, and on electronics to achieve a larger alignment tolerance for the interconnect. To do so, this chapter proposes the use of oversized detectors with *current-mode* receivers, and misalignment arrays which reroute the misaligned optical data stream. It introduces a generalized detector buffering technique for VLSI receivers. It also proposes techniques to improve the dynamic range of VLSI receivers.

This chapter is divided into two parts. Sections 4.1-4.7 discuss the *receiver design*, while section 4.8 discusses the *transmitter design*. In the next section, optical VLSI receivers design is briefly reviewed. In section 4.2, the concept of a current-mode receiver is introduced. Section 4.3 analyzes a particular implementation of a current-mode receiver: the current-conveyor-based receiver. In section 4.4, the buffering of optical VLSI receivers is discussed. Section 4.5 discusses another implementation of a current-mode receiver: the current-mode sense amplifier. Section 4.6 presents the implementation of an alignment tolerant array. Section 4.7 discusses the advantage of differential schemes, and introduces the time-differential receiver. In the last section modulator drivers are discussed.

4.1 Optical VLSI Receivers

A typical receiver has one of the three front-ends shown in Figure 4.1. These topologies have been discussed in the context of long-haul fiber optic preamplifiers [4.2]. Here these are considered for VLSI receivers for large and dense arrays of on-chip optical inputs and outputs. These voltage-mode front-ends convert the optical power, ΔP_{opt} into a voltage signal, ΔV according to:

$$\Delta V = S\Delta P_{opt} R \tag{4. 1}$$

where S is the photodetector responsivity and R the input impedance. The dominant pole of the voltage-mode receiver is at its input node and limits its response time. To the first order, the response time associated with these structures is given by

$$\Delta t \ \alpha \ \frac{\Delta VC}{S\Delta P_{opt}} = RC \tag{4. 2}$$

In the case of the transimpedance amplifier (TIA),the bandwidth is proportional to the feedforward gain, A, and is given by $\sim \frac{A+1}{2\pi RC}$ where C the total capacitance. Electrical power is dissipated mainly in the load, R in the case of the high and low impedance receiver. Static power due to bias current dominates in a TIA.

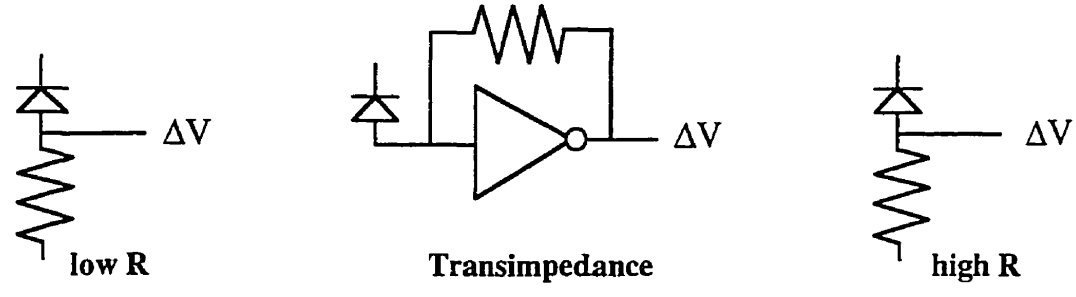


Figure 4.1: Voltage-mode front-ends

An amplifier is designed to increase the optical sensitivity of the receiver. There are two main categories of amplifier suitable for optical VLSI receivers: 1) asynchronous linear amplifiers and 2) synchronous sense amplifiers [4.3,4.4].

1) The analog amplifier brings ΔV to the digital rail. It effectively acts as a digital thresholder. It is implemented with a string of properly sized inverters.

2) The receiver based on a sense amplifier is by nature optically and electrically differential. However it can be operated in a single-ended fashion if an optical or electrical reference is provided. Moreover, it uses a clock to increase its sensitivity. It determines the time to sense (data valid) and the time to reset (data not valid). During data valid, the input is regenerated to the digital rails through positive feedback. Hence, the electrical power consumption is typically low and the area small. The bit rate, however, is reduced by the time required during each period to reset the sense amplifier.

4.2 Current-Mode Receivers

The alignability of the optical inputs is an important system issue. Many optical methods exist to improve the alignability of the interconnect [4.5]. On the other hand, electronic solutions can alleviate the problems of optics just like optics alleviates the problems of electronics [4.6]. This thesis introduces *current-mode techniques* to alleviate this problem. Normally, the input capacitance of the receivers should be minimized. This means that the detectors area needs to be inconveniently small, and hence the detectors are difficult to align to incoming signals. Oversizing the detecting or active area would be accompanied by an increase in the input capacitance. A 700 nm thick MQW PIN diode has a capacitance of 0.11 fF/ μm^2. A 20 μm square detector therefore has a capacitance of around 50 fF. An additional capacitance of around 20 fF is introduced into the input stage of a receiver through the flip-chip process [4.7]. A larger input capacitance leads to a decrease in bandwidth and sensitivity, and an increase in power consumption. This problem can be solved with a judicious circuit design.

By *limiting* the voltage swing at the input of the receiver, oversized detectors may be used without any detrimental effect to the receiver speed, sensitivity and power

consumption. The diode clamped receiver discussed in Chapter 2 is an example of how a limited voltage swing enhances performance. More examples are considered in this chapter. When the voltage swing is eliminated, current rather than voltage is used for signalling. Such designs are termed *current-mode* [4.8]. The current-mode circuit (CMC) input impedance, R is *designed* to be ideally zero (in practice very low). Voltage swings, ΔV are thus eliminated (reduced) at the high-capacitance input node. The response time therefore tends to zero as the input impedance is reduced because the time associated with charging and discharging the input capacitance is eliminated. In fact, current-mode approaches have been used in the design of high-speed amplifiers [4.9]. Moreover, the current-mode front-end (CMFE) sensitivity is increased and power consumption reduced when R and ΔV goes to zero to achieve a true I-mode operation. Table 4.1 shows the dependence of sensitivity, response time, and power on C for voltage-mode (V-mode) and current-mode (I-mode) front-ends (B is the bit rate). Thus the detector area can be increased to be whatever is convenient to capture all the signal light even in the presence of large misalignment and poor optical quality components. The detector area may be limited only by optical crosstalk considerations.

	V-mode	I-mode
Optical Sensitivty	~ΔVBC/S ~ΔV/SR	~ΔI/S
Response Time	α RC	independent of C as R->0
Electrical Power	ΔV^2 BC + static	0 + static

Table 4.1: A comparison between Current and Voltage-mode

The proposed receiver configuration consists of a current-mode front-end (CMFE) which is followed by a current-to-voltage (I-V) converter as shown in Figure 4.2. The I-V converter provides a digital logic output. The CMFE consists of a photodetection device connected to a current-mode circuit (CMC). The CMC amplifies directly the input photocurrent rather than converting it to a voltage first (as is the case for the receivers discussed previously). Voltages are created incidentally but are not used as the processing variable. In the proposed configuration, the current out of the CMC is converted to a voltage since most

digital logic are voltage-mode. The purpose of the CMFE is to buffer the high input capacitance from the low-capacitance digital node.

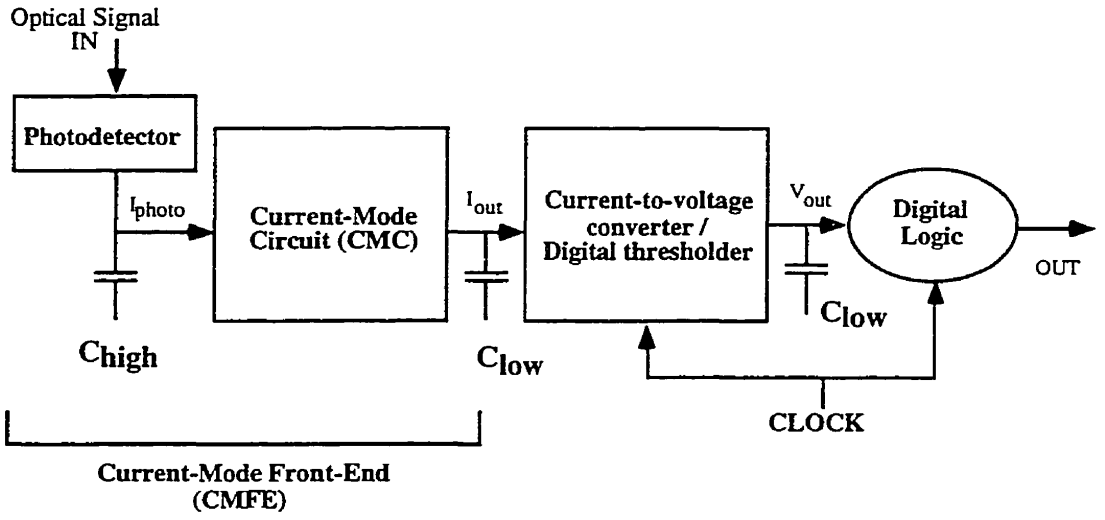


Figure 4.2: Proposed VLSI receiver configuration

The performance of the proposed receiver is therefore independent of the input capacitance. This characteristic introduces design freedom:

1) It enables an increase in the photodetector active area without a loss in receiver performance. Larger areas ease the design of the optics and the alignment of the optical interconnect as discussed above.

2) A photodetector can also be placed distant from its receiver without a penalty being incurred due to an increase in the input capacitance due to the line between the detector and its receiver. This kind of detector placement is used for a clustered pixel configuration [4.10].

3) Large electrical fan-in from multiple optical inputs [4.11] can be implemented with a CMFE.

Another advantage of a CMFE is that its performance is not as quickly degraded when the voltage supply is scaled down. This is true as long as all the transistors are biased in their saturation region. For example, a low-voltage current-mode sense amplifier has been demonstrated for a RAM design. Scaling the voltage down is advantageous for low-power operation [4.12].

This chapter discusses the design and implementation of two receivers with a CMFE. The first receiver uses a push-pull current conveyor (CCI) as its CMC. The second is based on an inherently current-mode sense amplifier (CMSA). Topologically, photocurrent is fed into the low resistance drain or source of the FET rather than into its high input resistance gate hence reducing the input impedance.

4.3 Current-Conveyor based receiver

The current conveyor-based receiver is now examined. The current-mode circuit (CMC) for this receiver is a current conveyor (CC). The ideal current conveyor [4.13] conveys with a unity gain an input photocurrent to its output (which is the input node of the I-V converter in Figure 4.2). An ideal current conveyor of the type CCI is schematically defined in Figure 4.3. In this figure, the IV characteristic of the single ellipse element (called a nullator) is V=0 and I=0. The double ellipse (called a norator) has an arbitrary I-V relationship (that is, the current and voltage are independent). Thus the following relationships hold:

$$I_Y = I_X = I$$

$$V_X = V_Y$$

$$I_Z = \pm I$$

The subscripts refer to the labelled node in Figure 4.3. A virtual short exists at the inputs, X and Y producing a zero input resistance. The input current is transported or conveyed to the output, Z, almost instantaneously since the current conveyor is a current-mode circuit.

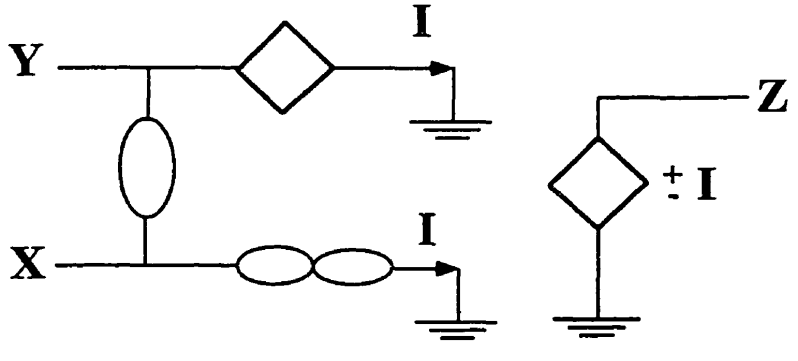


Figure 4.3: The current conveyor

4.3.1 CMOS Current Conveyor

The implementation in CMOS of a CCI current conveyor is shown in Figure 4.4 [4.14, 4.15]. The corresponding X,Y and Z ports of the current conveyor are shown. The diodes on the left hand side of the circuit diagram (D1 and D2) represent the photodetectors. The encoding of the optical input is assumed to be spatially differential (see section 4.7). The photodetector combination supplies a bipolar current to the input node, X of the current conveyor. The current conveyor is composed of a simpler upper (M1 to M4) and a lower (M5 to M8) current conveyor [4.16] which are stacked one on top of the other. Each simpler CC is composed of a p current mirror (M1 and M2, or M5 and M6), and an n current-mirror (M3 and M4, or M7 and M8). The current conveyor transports the photocurrent to the input of a current-to-voltage (I-V) thresholder. The complete receiver consists of the CCI front-end and the I-V converter. A TIA is used to convert the conveyed current into a digital voltage as suggested in Figure 4.4.

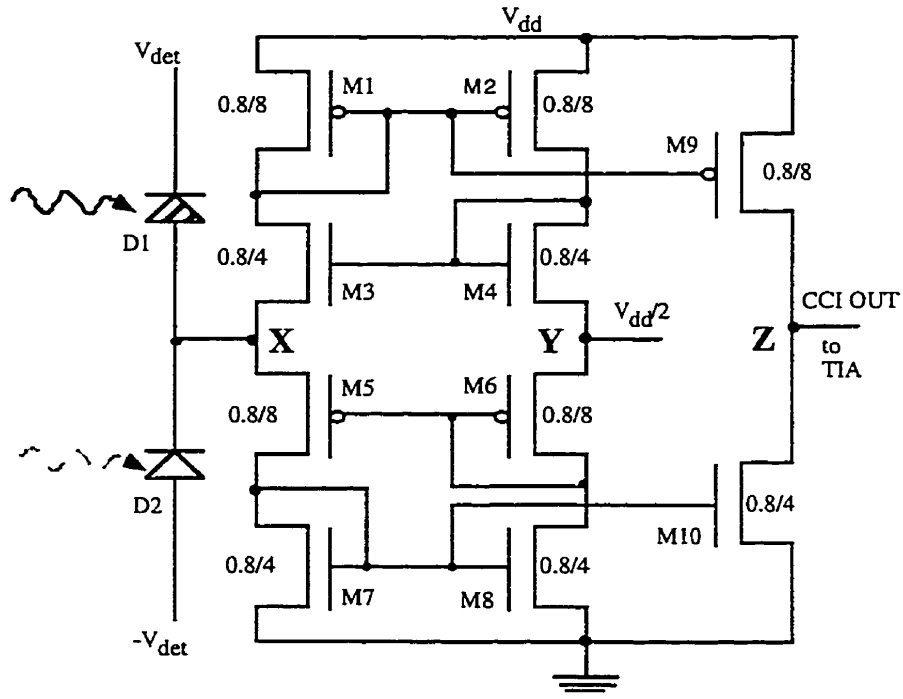


Figure 4.4: CMOS current conveyor front-end

The following analysis is a small-signal analysis which assumes linearity in the neighborhood of a given bias point. All transistors are biased in their saturation region and all the transistors are matched. Due to the matching of currents in the two branches of the CC, the voltages at the source of M3 and M4 (for the upper), and M5 and M6 (for the

lower) are also equal hence virtually shorting the input voltage, v_{in} to $V_{dd}/2$ ($\Delta v_{in} = \left| v_{in} - V_{dd}/2 \right| = 0$).

Each simpler CC (upper and lower) positively feeds back the photocurrent with a gain, $A_{ICC} \leq 1$. These gains are given respectively for the upper and lower CC as follows:

$$A_{ICCu} = \left(\frac{g_{m3}}{g_{m4} + g_{d2} + g_{d4}} \right) \left(\frac{g_{m2}}{g_{m1} + g_{d1} + g_{d3}} \right)$$

$$A_{ICCl} = \left(\frac{g_{m5}}{g_{d8} + g_{d6} + g_{m6}} \right) \left(\frac{g_{m8}}{g_{d5} + g_{d7} + g_{m7}} \right) \tag{4. 3}$$

From Equation (4. 3), the total input current is found:

$$\Delta I + \Delta I A_{ICCi} + \Delta I (A_{ICCi})^2 + \ldots + \Delta I (A_{ICCi})^n + \ldots = \frac{\Delta I}{1 - A_{ICCi}} \tag{4. 4}$$

Therefore the input resistance is $R_{ini} = \dfrac{\Delta V}{\Delta I / (1 - A_{ICCi})}$ where i=u,l referring to the upper or the lower CCI. Their respective input resistances are given by

$$R_{inu} = \frac{1 - A_{ICCu}}{g_{m3}}$$

$$R_{inl} = \frac{1 - A_{ICCl}}{g_{m5}} \tag{4. 5}$$

The input resistance of the push-pull CCI is effectively $R_{in} = R_{inu} \| R_{inl}$. From (4. 5), the input impedances are

$$Z_{inl} = R_{inl}\frac{\omega_0^2\left(1+s/\omega_{fet}\right)}{s^2+s\frac{\omega_0}{Q}+\omega_0^2} \text{ and } Z_{inu} = R_{inu}\frac{\omega_0^2\left(1+s/\omega_{fet}\right)}{s^2+s\frac{\omega_0}{Q}+\omega_0^2} \tag{4. 6}$$

The input impedance is $Z_{in} = Z_{inu} \| Z_{inl}$, $\omega_0^2 = \omega_{det}\omega_{fet}$ and $Q = \sqrt{\frac{\omega_{det}}{\omega_{fet}}}$. The frequencies $\omega_{det} = 1/\left(R_{in}C_{in}\right)$ and $\omega_{fet} = 1/\left(R_{fet}C_{fet}\right)$ are the components of the pole frequency associated with the input (C_{in}) and FET (C_{fet}) or parasitic capacitance. R_{in} is the input resistance of the CCI. For complex and stable poles, the response is underdamped with a damping time proportional to $\frac{2Q}{\omega_0} = \frac{2}{\omega_{fet}}$. The input impedance approaches zero when the gain approaches unity. The zero input impedance limits the voltage swing.

The transfer function of the CCI is:

$$H(s) = \frac{|H_0|\omega_0^2}{s^2+s\frac{\omega_0}{Q}+\omega_0^2} \tag{4. 7 }$$

where

$$|H_0| = \left(\frac{g_{m3}}{g_{m1}+g_{d1}+g_{d3}}\right)\left(\frac{g_{m9}}{g_{m4}+g_{d2}+g_{d4}}\right) = \left(\frac{g_{m10}}{g_{d5}+g_{d7}+g_{m7}}\right)\left(\frac{g_{m5}}{g_{d8}+g_{d6}+g_{m6}}\right) \tag{4. 8}$$

is the DC gain. The current conveyor and in general, a current-mode circuit have a large bandwidth that is independent of gain (see section 4.5 for further discussions). This is clear if the transfer function (Equation (4. 7)) is examined for physical frequencies:

$$H(j\omega) = \frac{|H_0|}{1-\frac{\omega^2}{\omega_0^2}+j\omega\frac{1}{Q\omega_0}} \tag{4. 9 }$$

The frequency response is independent of ω (flat) if the pole frequency, ω_0 is high. This can be achieved with a R_{in} that tends to zero (unity gain bandwidth for the individual FET is usually very high i.e. many GHz). The amount of gain is limited by the process (the transconductance of the devices- see Equation (4. 7)).

The gain can be increased with an output stage. The output stage is composed of M9 and M10 (refer to Figure 4.4). It provides a current gain to the CCI. The DC current gain at the output stage (M9 and M10) is [4.14, 4.16]

$$|H| = (W/L)_{M_9} / (W/L)_{M_2} = (W/L)_{M_{10}} / (W/L)_{M_8} \tag{4. 10}$$

The current conveyor gain, H contributes to increasing the sensitivity. Since gain is independent of bandwidth as described above, the sensitivity can be increased with a minimal penalty in the bandwidth. This decrease cannot be indefinite since the gain for this simple structure is limited. The increase in gain also results in an increase in noise therefore contributing to reducing the sensitivity. However for the values of gain considered here, the noise level is typically low compared to the signal level (see next section).

Thus the CCI does not incur a penalty in the bandwidth and the optical power requirements of the receiver but the CC-buffer adds electrical power consumption. To quantify this excess power consumption, let I_q be the total quiescent current in the CCI. The quiescent current is divided into equal parts in the three branches of the CCI. Input photocurrent is forced into or drawn out of the input node. The input current flows into or out of the upper and the lower CCI (away or towards the input node). It is assumed that the magnitude of the current into or out of the upper and lower CCI are equal. The current from the drain of M9 is therefore $|H|\left(I_q/3 \mp i_{in}/2\right)$ and the current into the drain of M10 is $|H|\left(I_q/3 \pm i_{in}/2\right)$. The output current is the difference between these two currents i.e. $i_{out} = Gi_{in}$. Assuming that $|G| = 1$, the power consumption is [4.15]

$$P \sim \left(I_q + i_{in}/2\right)V_{dd} \tag{4. 11 }$$

The power consumption of the CC is therefore independent of frequency since consumption associated with switching power is non-existent in a current-mode circuit.

Now consider the I-V converter which is a TIA (see Figure 4.1). The output current of the CC is the input photocurrent, ΔI_{photo} to the TIA. The optical power requirements and bandwidth of the receiver is limited by that of the TIA. The TIA transfer function can be expressed as follows [4.17]:

$$Z_{Tia}(j\omega) = \frac{\Delta V(j\omega)}{\Delta I_{photo}} = \frac{-R_f\left(\frac{A_{vTia}}{1+A_{vTia}}\right)}{1+j\omega R_f\left(C_f + \frac{C_g}{1+A_{vTia}}\right)} \tag{4. 12 }$$

where $A_{vTia} = \dfrac{-g_{mtia} + \frac{1}{R_f} + j\omega C_f}{\frac{1}{R_o} + \frac{1}{R_f} + j\omega\left(C_f + C_o\right)}$, g_{mtia} is the transconductance of the input FET, and I_l is the input FET gate current leakage. R_f and C_f are the feedback resistance and capacitance. R_o and C_o are the output resistance and capacitance, and C_g is the input capacitance of the TIA. Its optical power requirements and bandwidth are given by (4. 1) and (4. 2), respectively.

From Equations (4. 9) and (4. 12), the overall transfer function becomes:

$$T = H(j\omega)Z_{Tia}(j\omega) \sim |H_0|Z_{Tia}(j\omega) \tag{4. 13}$$

The bandwidth of the receiver is typically determined by that of the TIA. The overall performance of the receiver is independent of C_{in}, and the capacitances C_g and C_f are usually small (a few femtofarads).

4.3.2 Noise Analysis and sensitivity

This section presents a noise analysis to evaluate the sensitivity of a receiver. The previous section treated optical power requirements without considering noise. An increase in input capacitance may result in an increase in noise and thus an increase in the optical power required to achieve a given BER (see Chapter 5). The analysis presented here quantifies the additional amount of noise introduced by the CCI as a function of the input capacitance.

The noisy CCI is modelled by an ideal (noiseless) CCI with noise sources referred to its input. Figure 4.5 shows those noise sources. The current spectral noise density of the photodiodes is $\frac{d\langle i_{nd}^2\rangle}{df}$. The current and the voltage spectral noise density of the CCI are $\frac{d\langle i_{na}^2\rangle}{df}$ and $\frac{d\langle v_{na}^2\rangle}{df}$. They are given as follows :

$$\frac{d}{df}\langle i_{nd}^2\rangle = \frac{d}{df}\langle i_{GR}^2\rangle + 2eI_{dark} \tag{4. 14}$$

$$\begin{aligned}\frac{d\langle i_{na}^2\rangle}{df} = &\left[4kT\zeta\left(g_{m1}+g_{m3}\right)+2e\left(I_{l1}+I_{l2}+I_{l9}\right)+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]+\\ &+\left[4kT\zeta\left(g_{m5}+g_{m7}\right)+2e\left(I_{l7}+I_{l8}+I_{l10}\right)+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]\\ &+2\sqrt{\left[4kT\zeta\left(g_{m1}+g_{m3}\right)+2e\left(I_{l1}+I_{l2}+I_{l9}\right)+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]}\\ &\times\sqrt{\left[4kT\zeta\left(g_{m5}+g_{m7}\right)+2e\left(I_{l7}+I_{l8}+I_{l10}\right)+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]}\end{aligned} \tag{4. 15}$$

$$\frac{d}{df}\langle v_{na}^2\rangle = A^2\left(\frac{1}{g_{m6}^2}\left[4kT\zeta(g_{m6}+g_{m8})+2e(I_{l5}+I_{l6})+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]\right)$$
$$+B^2\left(\frac{1}{g_{m4}^2}\left[4kT\zeta(g_{m2}+g_{m4})+2e(I_{l3}+I_{l4})+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]\right) \quad (4.\ 16)$$

where $A=\frac{g_{m5}}{g_{m5}+g_{m3}}$ and $B=\frac{g_{m3}}{g_{m5}+g_{m3}}$ and ζ=0.7 for silicon technologies [4.2]. I_{li} is the gate leakage current of FETi. K_F is the flicker noise coefficient. I_{dq} is the quiescent drain current. AF is the flicker noise exponent. L_{eff} is the effective gate length. C_{ox} is the field oxide capacitance, and f is the low frequency corner frequency. The spectral density for the generation-recombination, $\frac{d}{df}\langle i_{GR}^2\rangle$, and shot noise due to a dark current I_{dark} is taken into account in Equation (4. 14). In Equations (4. 15) and (4. 16) the first terms in the square bracket are the contribution from the FET channel noise, the second terms are due to gate leakage currents, and the third terms take into account the 1/f noise [4.18]. All spectral densities are assumed to be white over the band of interest.

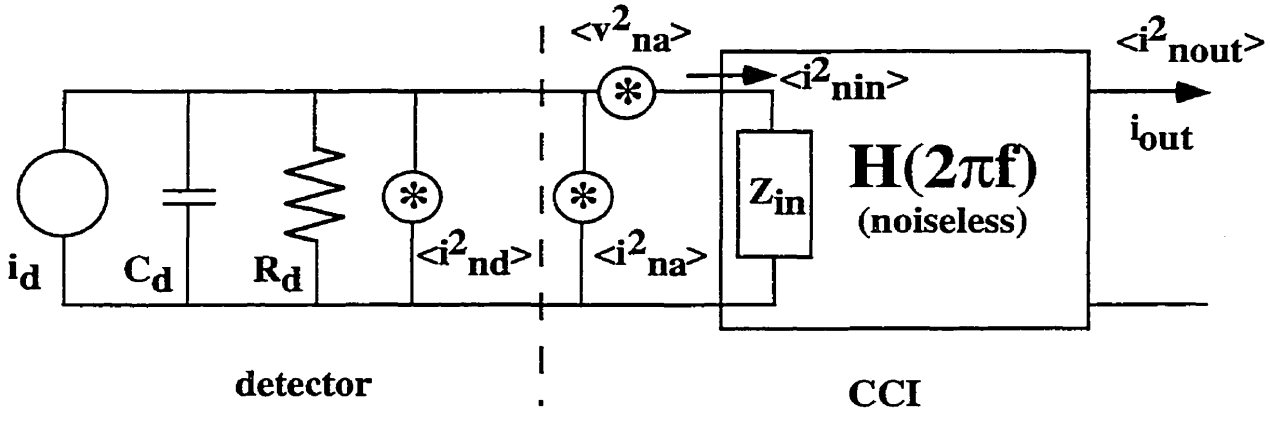


Figure 4.5: Noise equivalent model

The noise sources shown in Figure 4.5 can be replaced by a single equivalent current noise source referred to the input given by (see 4.10 Appendix for derivation of Equation (4. 17)) [4.18]:

$$\frac{d<i_{ni}^2>}{df}=\frac{d<i_{nd}^2>}{df}+\frac{d<i_{na}^2>}{df}+\left[\frac{d<v_{na}^2>}{df}|Y_d|^2\right]+2\chi\left[\sqrt{\frac{d<i_{na}^2>}{df}}\sqrt{\frac{d<v_{na}^2>}{df}}|Y_d|\right] \tag{4. 17}$$

where $|Y_d|^2=\frac{1}{|Z_d|^2}=\frac{1}{R_d^2}+\omega^2C_d^2$ and $\omega=2\pi f$ is the frequency in radians. The last term in Equation (4. 17) arises if there is any correlation between the current and voltage sources $-1\le\chi\le1$. If they are independent, $\chi=0$.

The output spectral noise density for the CCI is therefore:

$$\frac{d<i_{nout}^2>}{df}=\frac{d<i_{ni}^2>}{df}|K_{CCI}(j\omega)|^2 \tag{4. 18}$$

where $|K_{CCI}(j\omega)|^2=\left[\frac{Z_d}{Z_d+Z_{in}}\right]^2|H(j\omega)|^2$.

Including the noise from the TIA I-V converter, $\langle i_{ntia}^2\rangle$, the total noise for the receiver is (the output is divided by the DC gain to refer the total noise to the input):

$$\langle i_{TOT}^2\rangle=\frac{\langle i_{ntia}^2\rangle}{|K_{CCI}(0)|^2}+\int_0^\infty\frac{d\langle i_{ni}^2\rangle}{df}\frac{|K_{CCI}(f)|^2}{|K_{CCI}(0)|^2}\frac{|Z_{Tia}(f)|^2}{|Z_{Tia}(0)|^2}df \tag{4. 19}$$

where Z_{Tia} is given by Equation (4. 12) and,

$$\langle i_{ntia}^2\rangle=\left[\frac{4kT}{R_f}+2eI_l+\frac{4kT\zeta\left(g_{mn}+g_{mp}\right)}{g_{mn}^2R_f^2}\right]\int_0^\infty\frac{|Z_{Tia}(f)|^2}{|Z_{Tia}(0)|^2}df+\frac{4kT\zeta\left(g_{mn}+g_{mp}\right)}{g_{mn}^2}\left(2\pi C_g\right)^2\int_0^\infty f^2\frac{|Z_{Tia}(f)|^2}{|Z_{Tia}(0)|^2}df \tag{4. 20}$$

The integrals in Equation (4. 19) are found to be [4.17]:

$$\int_0^\infty \frac{|Z_{Tia}(f)|^2}{|Z_{Tia}(0)|^2} df = \frac{1+g_{mtia}R_o}{4\left[R_o\left(C_g+C_o\right)+R_f\left(C_f+C_g\right)+g_{mtia}R_oR_fC_f\right]}$$

$$\int_0^\infty f^2 \frac{|Z_{Tia}(f)|^2}{|Z_{Tia}(0)|^2} df = \frac{\left(1+g_{mtia}R_o\right)^2}{16\pi^2\left[R_o\left(C_g+C_o\right)+R_f\left(C_f+C_g\right)+g_{mtia}R_oR_fC_f\right]\left[R_oR_f\left(C_f\left(C_g+C_o\right)+C_gC_o\right)\right]}$$

(4. 21)

As shown in Equations (4. 19) and (4. 17), the total noise is C_d^2 dependent, as expected. This dependence arises because the detector admittance Y_d is proportional to its capacitance, C_d, and the total spectral noise density is proportional to $|Y_d|^2$(see Equation (4. 19)). Knowing the amount of noise in the receiver, the sensitivity as defined at the beginning of this section can be calculated as a function of BER (see Chapter 5). The sensitivity is inversely proportional to C_d. This is because the noise level rises when input capacitance increases.

4.3.3 Measurements of receiver performance

CCI-based receivers were designed and tested, 0.8μm and 0.5μm CMOS were used. One design is shown in Figure 4.4. A simulation of the design at 333 Mb/s is shown in Figure 4.6 for +/-4μA photocurrent input. The fabricated receiver shown in Figure 4.7, occupies an area of 50μm by 70μm. A metal pad at the input of the receiver is laid out for wirebonding a photodetector. On-chip PN silicon detectors were wirebonded to the input of the receiver. The responsivity of the photodetector is <0.1A/W. The total input capacitance is estimated to be ~20pF. The test bed described in Chapter 2 is used to test the receiver. The output of the receiver is buffered, and it was found that the buffer limited the speed of the receiver. Figure 4.8 shows the output of the receiver for an optical power of -20dBm (10μW) at a rate of 3Kb/s and 10Mb/s input. For the design under consideration, the power consumption is less than 3mW.

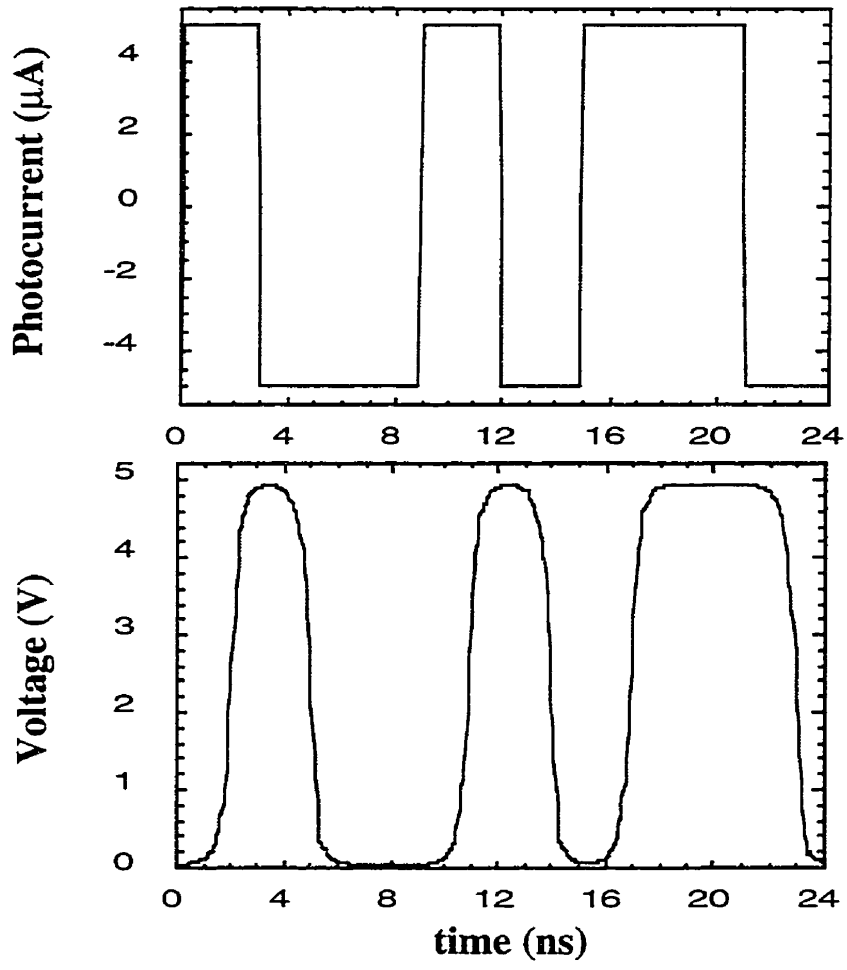


Figure 4.6: Simulation of the CC-based receiver

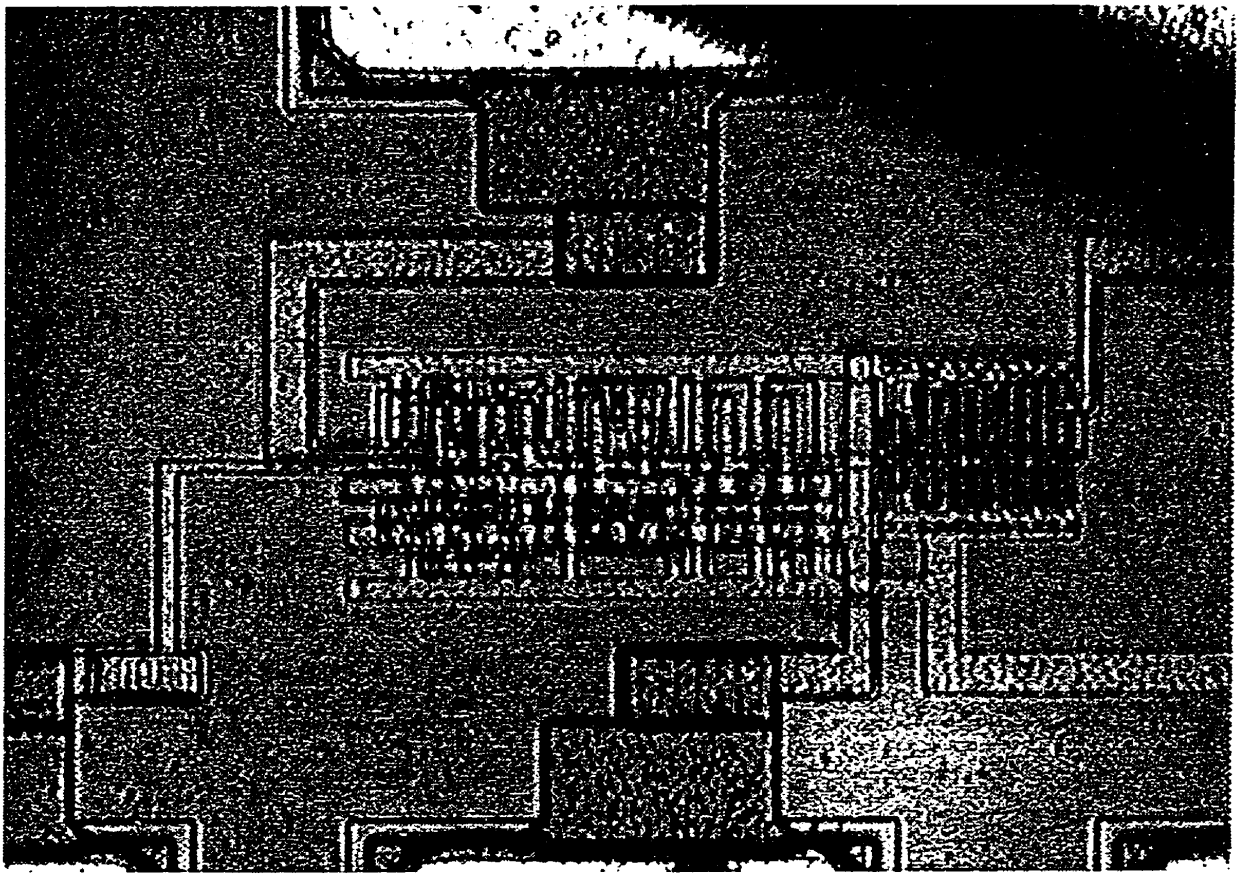
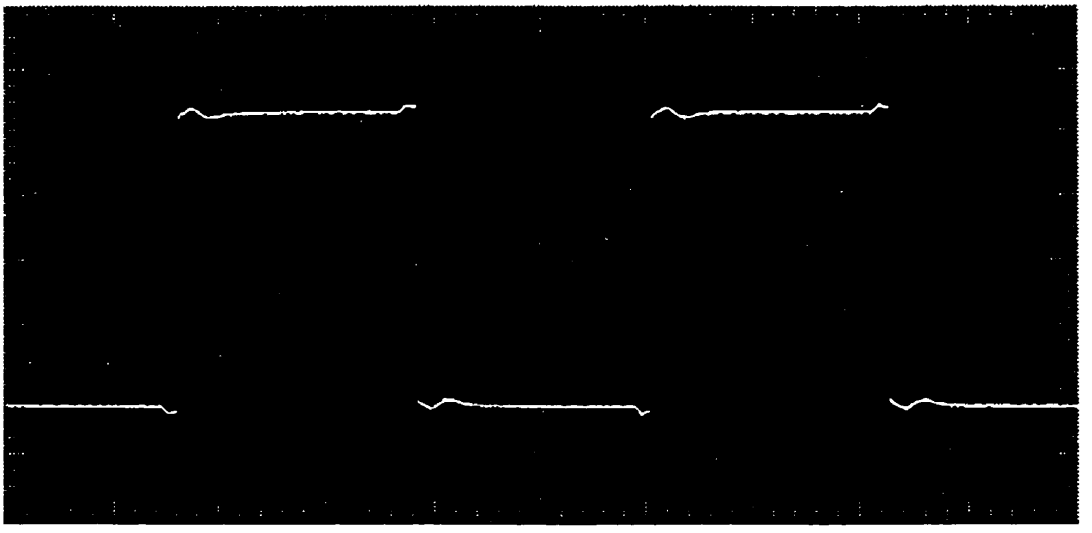
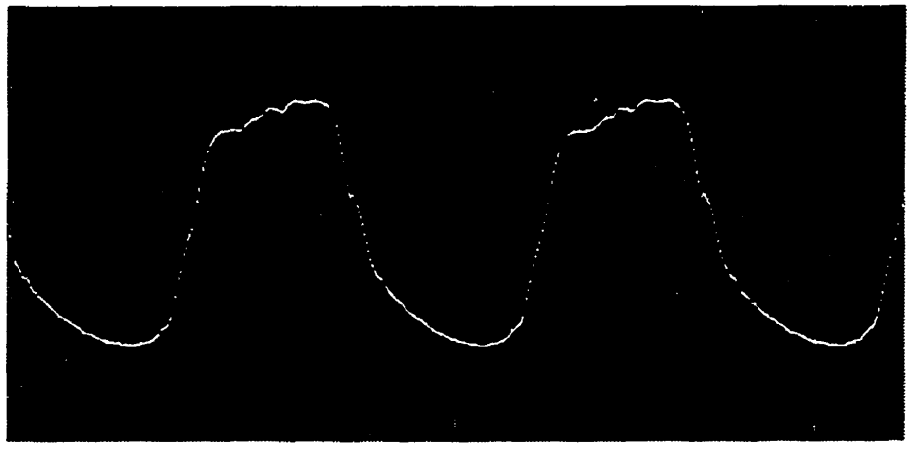


Figure 4.7: Fabricated current conveyor-based receiver



(a)



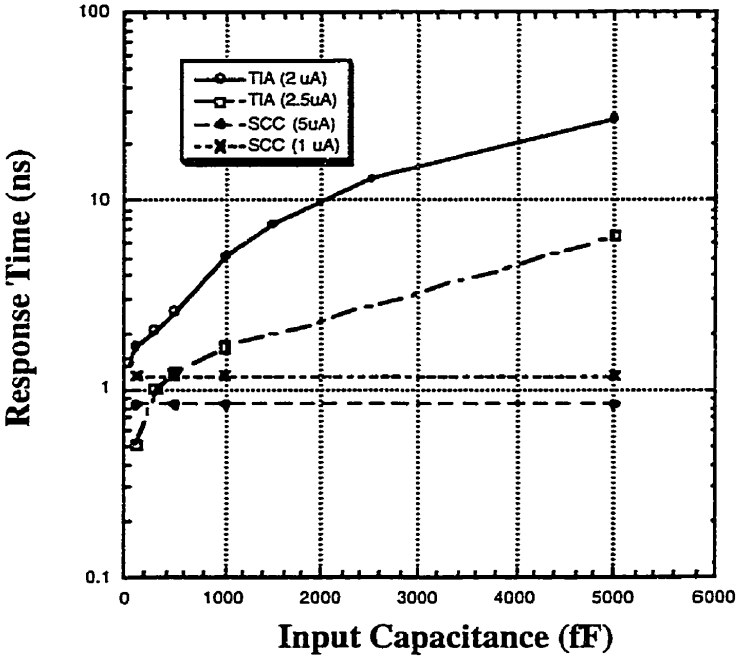
(b)

Figure 4.8: Experimental output of CC-based receiver (a) at 3 Kb/s (b) at 10Mb/s

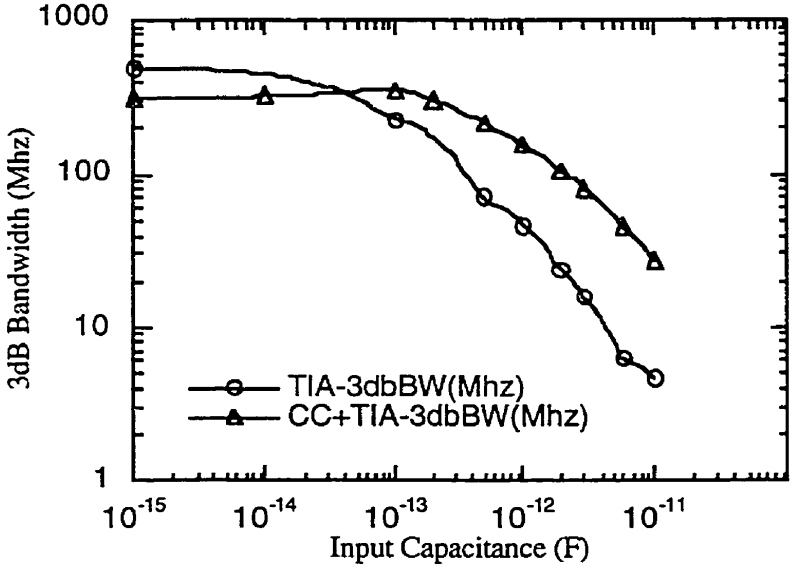
Figure 4.9a shows the edge times versus input capacitance. The response time is independent of the input capacitance over many picofarads. For comparison, the response time for a TIA-based receiver without the CC at the front-end is shown in that figure for two different input photocurrent levels. Figure 4.9b shows the bandwidth as a function of input capacitance. Table 4.2 summarizes the comparison.

	CCI $H(j\omega)$	TIA $Z_{tia}(j\omega)$	CCI/TIA $H(j\omega)Z_{Tia}(j\omega)$
3dB BW	independent of C_{in}	dependent on C_{in}	independent of C_{in}
Power Consumption	independent of C_{in}	dependent on C_{in}	independent of C_{in} sum of the CCI and TIA power
Sensitivity (noise)	α $1/C_{in}$ (αC^2_{in})	α $1/C_{in}$ (αC^2_{in})	α $1/C_{in}$ (αC^2_{in}) noise of CCI and TIA are summed
Area	small	small	sum of that of CCI and TIA

Table 4.2: A comparison between buffered and unbuffered receivers



(a)



(b)

Figure 4.9: Speed versus Input Capacitance (a) edge speed (b) 3dB bandwidth

Figure 4.10 shows the total spectral noise density (input referred-see Equation (4. 17)) as a function of frequency for $\chi = 1$, C_{in}=1pF and R_{in}~756Ω. The spectral density has the same square dependence on the detector capacitance, C_d. The total output noise is found by integrating the spectral density over *all* frequencies. Figure 4.11 shows the result of a calculation of the integrated noise at the output of the current conveyor for a range of input capacitance values and various values of R_{in}. The noise level increases with the value of capacitance for a low R_{in}. However for the design under consideration (R_{in}=756 ohms), noise decreases for higher values of capacitance because there is a finite noise bandwidth that drops at high values of capacitances. Figure 4.12 shows the calculated noise bandwidth of the CCI-based receiver. The total noise for the TIA is about ~1e-13 A^2 [4.17] following essentially the same trend as in Figure 4.11. Its noise level is lower because the noise bandwidth is smaller as shown in Figure 4.12. In conclusion, we find that decreasing R_{in} increases bandwidth but it also increases noise. For a low input resistance design, bandwidth can be extended over that of the TIA while keeping the CCI noise at levels comparable to the TIA's.

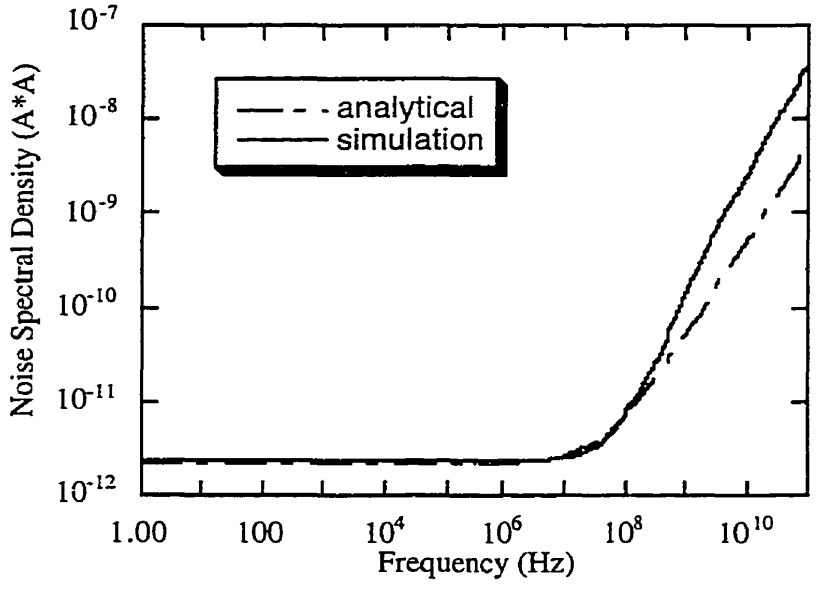


Figure 4.10: Spectral noise density

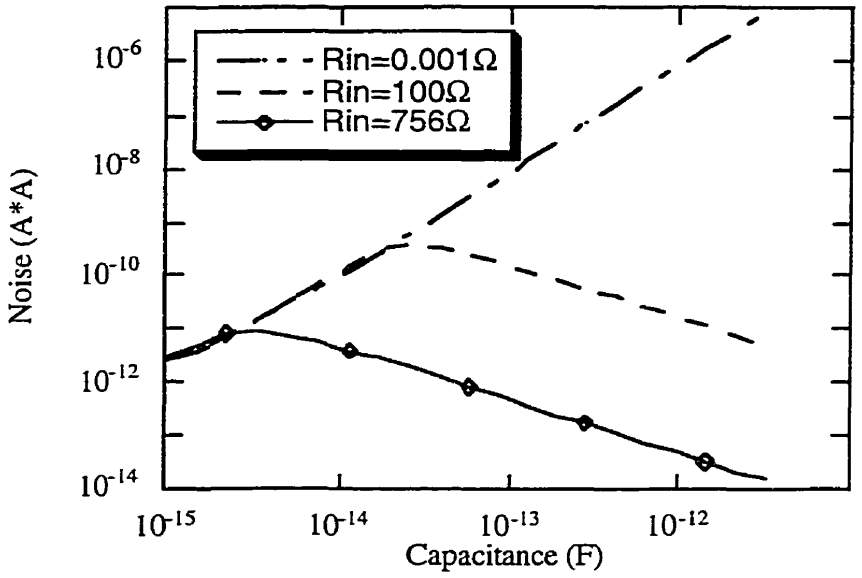


Figure 4.11: Output noise for various input resistances

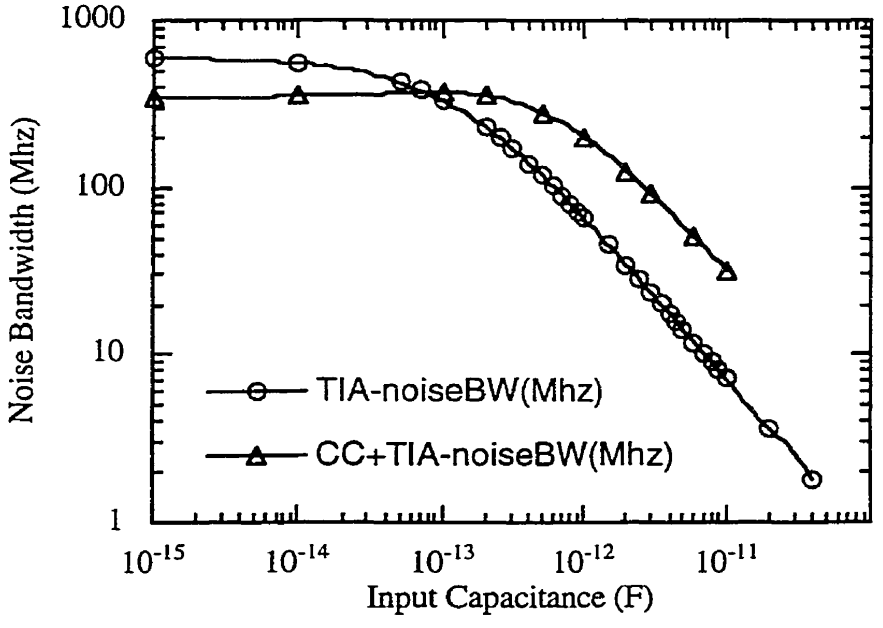


Figure 4.12: Noise Bandwidth

4.4 Buffering of receivers

As discussed in section 4.3, the current-conveyor buffers the input of the I-V converter from the detector to achieve a receiver performance that is independent of the capacitance of its detector. In this section, the buffering of receivers are discussed further and the technique is generalized. Where required, buffers are used at the input and/or output of the analog receiver. This section considers the buffering of receivers that have a transimpedance configuration. Receivers with feedback are considered because they have a better bandwidth and dynamic range than high-impedance receivers, and a better noise performance and sensitivity than low-impedance receivers. TIA based receivers have been widely used (see for example [4.19, 4.20]). They invariably use a voltage controlled voltage source (VCVS) open-loop amplifier. This configuration may not be optimal. The transimpedance topology is *generalized* to include *all* open-loop amplifiers from the Tellegen ideal set [4.21]. This set approximates the behavior of all practical amplifiers:

1) Voltage Controlled Voltage Source (VCVS) with a voltage gain A_{ov}
2) Current Controlled Current Source (CCCS) with a current gain A_{oi}
3) Current Controlled Voltage Source (CCVS) with a transimpedance Z_{ot}
4) Voltage Controlled Current Source (VCCS) with a transconductance G_{ot}

Ideally, a voltage input has an infinite impedance, and a current input a zero impedance. A voltage output has zero impedance, and a current output an infinite impedance.

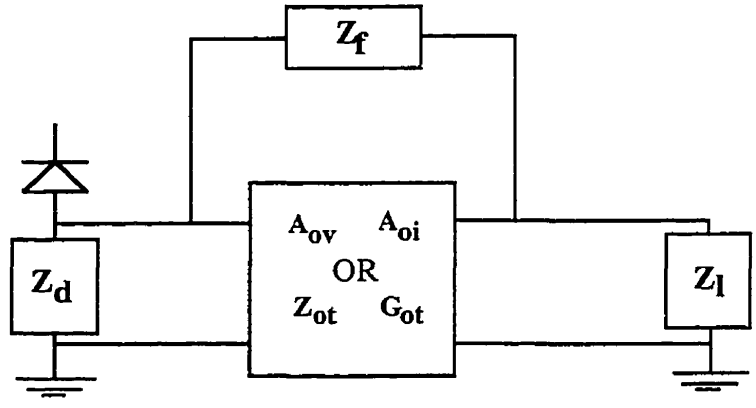
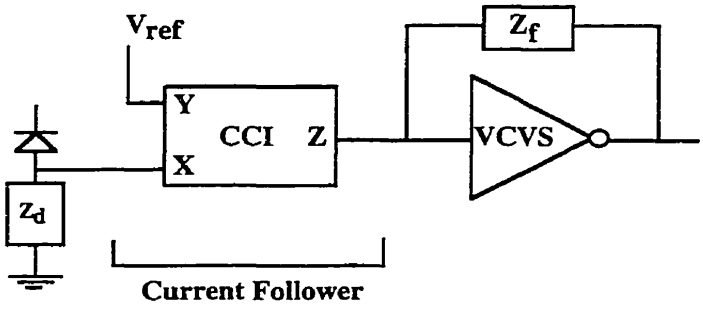
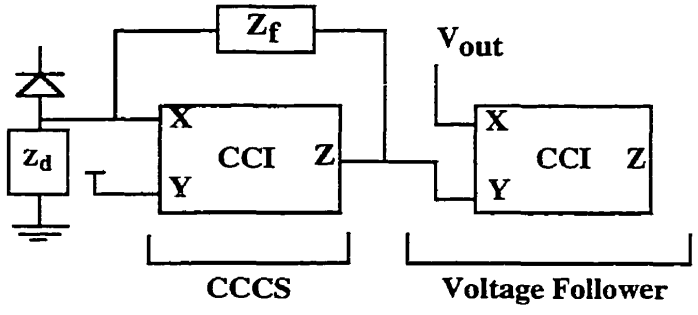


Figure 4.13: Generalized TIA-based receiver

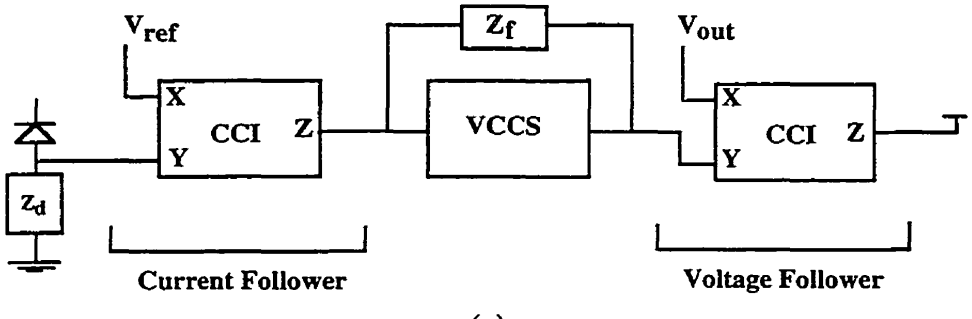
Now consider the three remaining cases in Table 4.3. With buffering, the dependence on the input and output impedance is removed ($\Psi \rightarrow 1$) and the fixed gain-bandwidth product is broken [4.24]. This is accomplished by buffering the input of a VCVS transimpedance configuration, the output of a CCCS configuration or both in the case of the VCCS. The three buffered receivers are shown in Figure 4.14. As discussed in the section 4.3, a VCCS TIA is buffered by connecting a current follower (CF) to the input of the TIA (Figure 4.14a). In the case of a CCCS TIA, a voltage follower (VF) is connected at the ouput of the TIA (Figure 4.14b). Finally the VCCS requires a CF and a VF at the TIA input and output, respectively (Figure 4.14c).



(a)



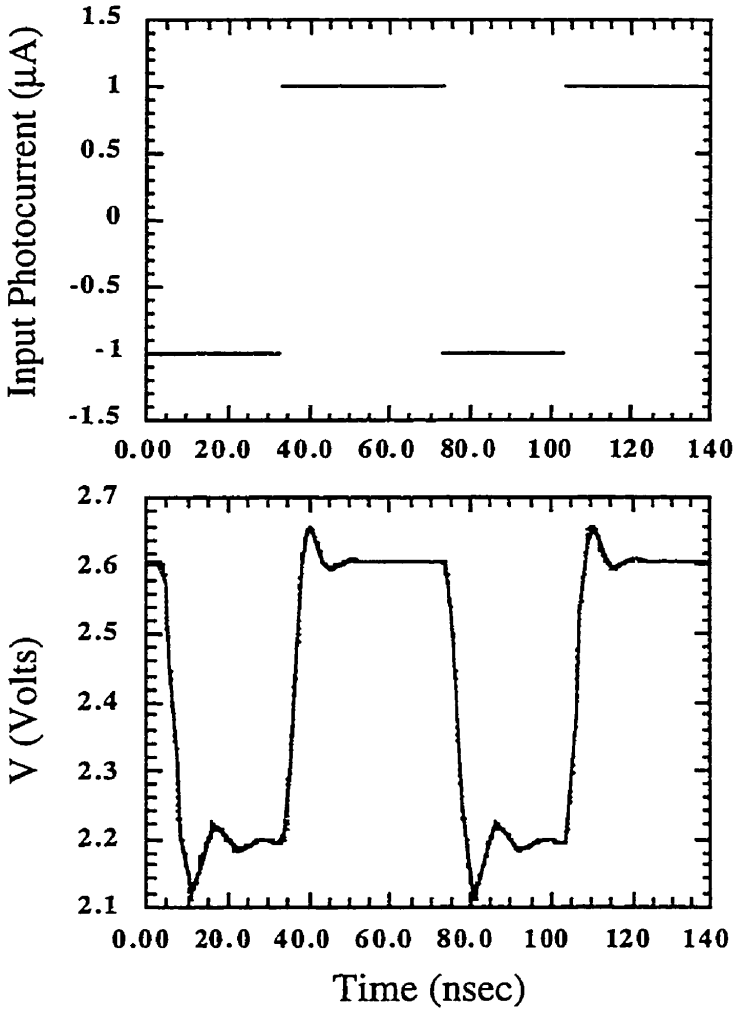
(b)



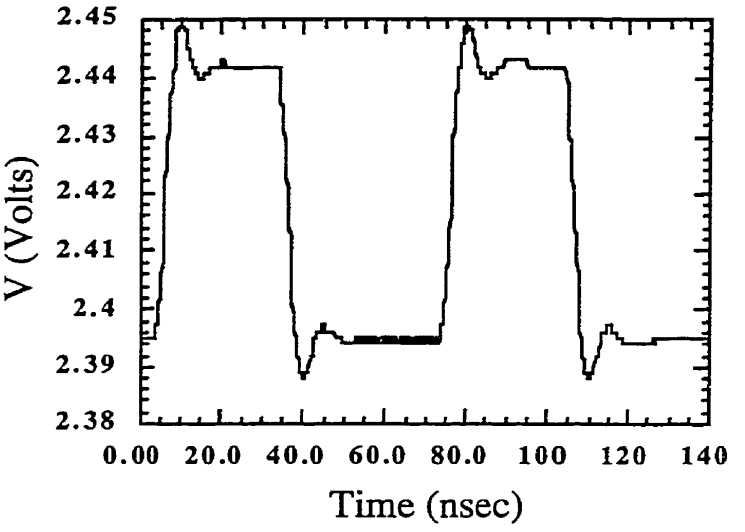
(c)

Figure 4.14: Buffered TIA-based receivers

CF and VF are designed and implemented with CMOS current conveyors (CCI). A CMOS CF was discussed in section 4.3. A VF can be implemented with the same circuit. The voltages on ports Y and X follow each other because of the existence of a virtual short (see Figure 4.3). The design shown in Figure 4.14a and b are now presented and discussed. Their respective analog output voltages are shown in Figure 4.15. Both receivers have an input capacitance of 1pF, and the input photocurrent is +/-1μA. Their risetimes are respectively 2.57nsec, and 2.63nsec. The ringing is introduced by the second order CCI (see the discussions in section 4.3) while the TIA alone is designed to give a maximally flat response. The ringing reduces when the feedback impedance is increased.



(a)



(b)

Figure 4.15: Simulation of buffered receivers

In the second design (Figure 4.14b), the voltage follower serves two purposes: 1) to produce a bandwidth that is not dependent on Z_l (see Table 4.3), and 2) to convert the output current of the TIA into a voltage for further digital processing. The performance and bandwidth do not depend on Z_d since this design has a current-mode input (see section 4.2).

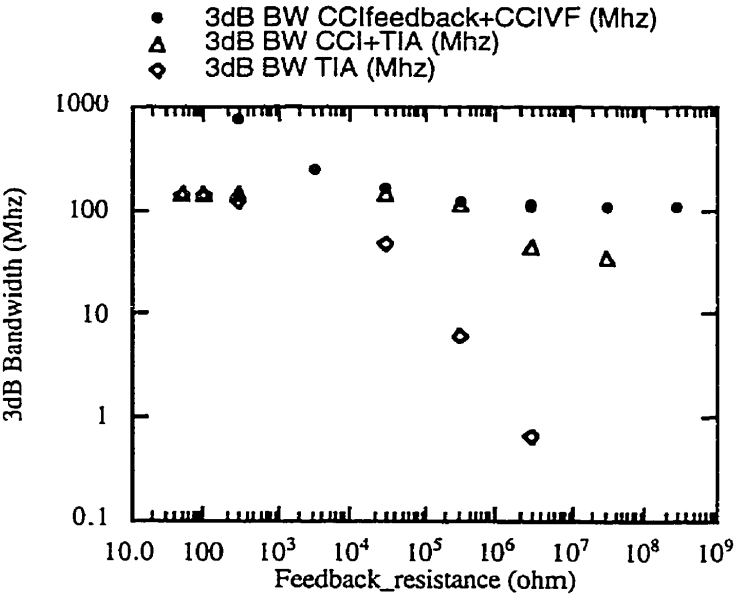


Figure 4.16: Bandwidth versus gain

The gain bandwidth for these two designs as compared with the unbuffered VCCS TIA is presented in Figure 4.16. The transimpedance can be increased over a large range with a small penalty in bandwidth. This is not the case for the unbuffered case. Transimpedances of 10's of kΩ are not uncommon with a small active resistor made of FETs. Larger transimpedance may be more difficult to achieve in technologies such as 0.8 or 0.5 μm CMOS without it being physically large.

Buffering techniques enable the design of receivers which are less dependent on input and output impedance. The resulting designs have bandwidth that is independent of gain and sensitivity.

4.5 Current-Mode Sense Amplifier-based receiver

In this section, the design of a current-mode receiver implemented with a sense amplifier is described. A sense amplifier is normally used for VLSI memory design [4.25]. The circuit low-power consumption and compactness is also very attractive for the implementation of VLSI optoelectronic receivers. The receiver is constructed with a current-mode sense amplifier (CMSA) which is a sense amplifier with a current-mode input [4.26]. The CMSA replaces the current-mode front-end (CMFE), and the current-to-voltage converter and the digital thresholder of Figure 4.2. This implementation results in a very compact current-mode input digital receiver. Moreover the sense receiver is optically differential like the CC-based receiver (discussed in 4.3) but it is also electrically differential. Being fully differential, the sense amplifier-based receiver has the advantage of common noise rejection and a reduction in switching noise (see section 4.7).

Figure 4.17 shows a CMOS implementation of the CMSA-based receiver [4.3, 4.4]. The receiver consists of a pair of cross-coupled inverters (M1-M4 and M2-M3), and voltage clamps (M8 and M9) that are biased in the linear region (by adjusting the voltage at the source of M7 and M8). Pass n-transistors, M5 and M6 are used to equalize the potential on the input and output nodes. The diodes represent the MQW PIN detectors which are biased with a single power supply rail V_{det}. Consider the timing diagram of the CMSA shown in Figure 4.18. When the clock is high, the output of the CMSA (CMSA_out) is forced into a metastable state by shorting the outputs. The inputs are also shorted providing

a zero input impedance just before the clock falls. As the clock goes low, the sense amplifier becomes more and more sensitive to differential noise. An infinitesimally small difference at the inputs initiates the positive feedback provided by the cross-coupled inverters, and a digital output (differential) is reached in ΔT_r after the start of the fall of the clock (see Figure 4.18). The difference in output voltages initially increases exponentially and then saturates.

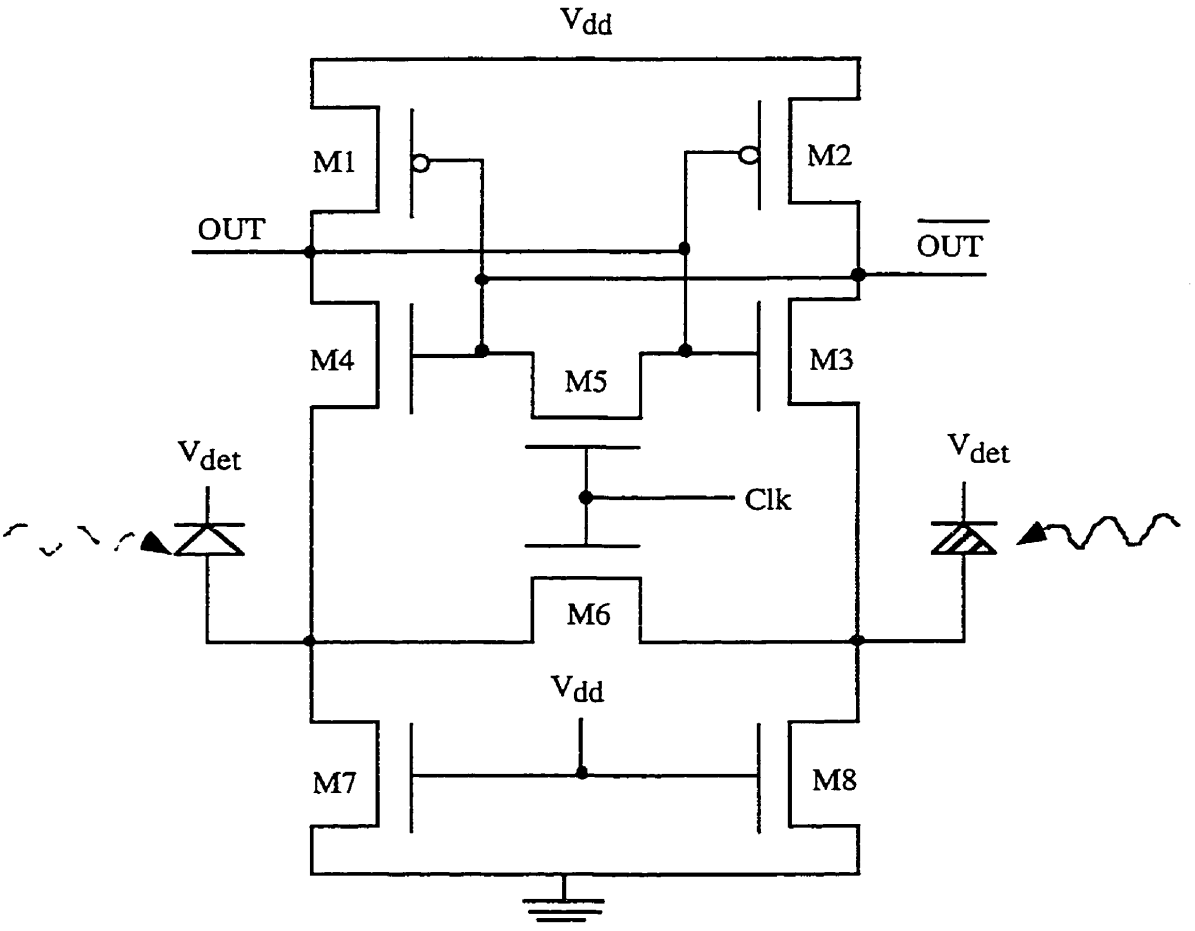


Figure 4.17: Current-mode sense amplifier-based receiver

The analog optical input uses a space differential encoding (dual-rail). The differential optical input must be stabilized when the clock starts to fall and kept stable until the output is completly switched to the rails. After this occurs, the CMSA_out is stable against all *small* differential inputs. The differential noise limits the receiver sensitivity. Process variations and asymmetry in the differential arms also contributes to the differential noise. This noise is produced by independent noise on the input beams. Common-mode noise, on

the other hand, is eliminated with the fully differential configuration of the CMSA-based receiver.

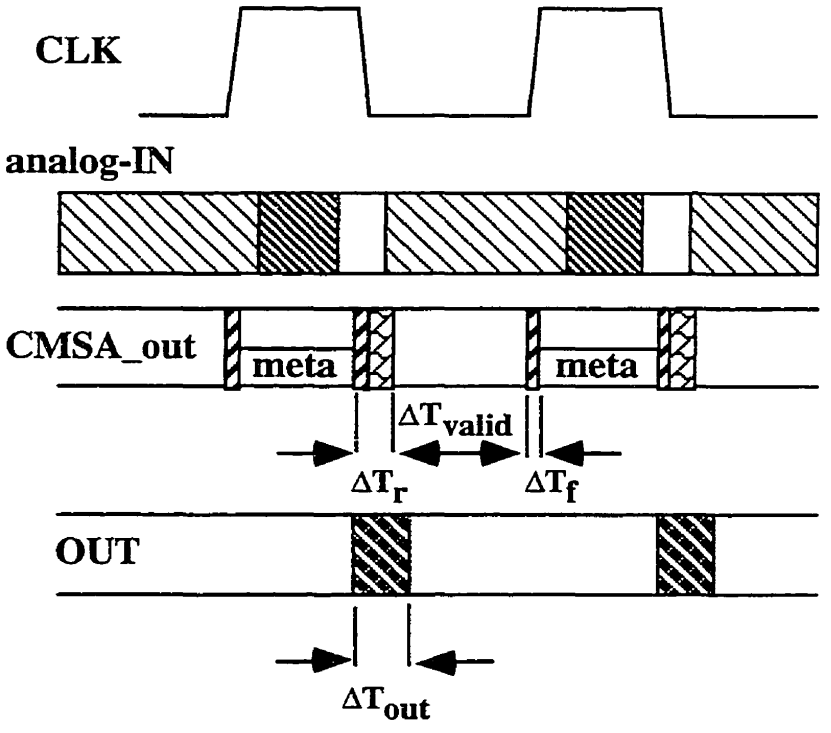


Figure 4.18: CMSA timing diagram

Another version of the CMSA [4.27] is shown in Figure 4.19. The inputs are equalized in the same fashion as before but the outputs are equalized or precharged to 0 V instead of ~$V_{dd}/2$ as described above. When the clock falls low, P1 and P2 conduct and charge the output nodes. M3 and M4 are initially off as their gates were precharged to 0 V but they turn-on when the output nodes are charged to the input voltage plus one threshold voltage. At which time the input has become clearly defined and the sense amplifier starts operating. In effect, the output is resolved only after the input is stabilized. In the timing diagram the output of the modified CMSA is shown. The input is again shown at the top. The CMSA receiver is compatible with precharged and domino logic. When the clock is high, the CMSA-based receiver is precharging the output nodes. When the clock is low, the receiver evaluates its inputs. The receiver is in effect a p-block precharge-evaluate gate with analog inputs but digital outputs, and it can be cascaded with an n-block precharge-evaluate and domino logic [4.28]. It is also compatible with dynamic edge-triggered flip-flops and latches that are clocked with a true single-phase clock (TSPC) [4.28].

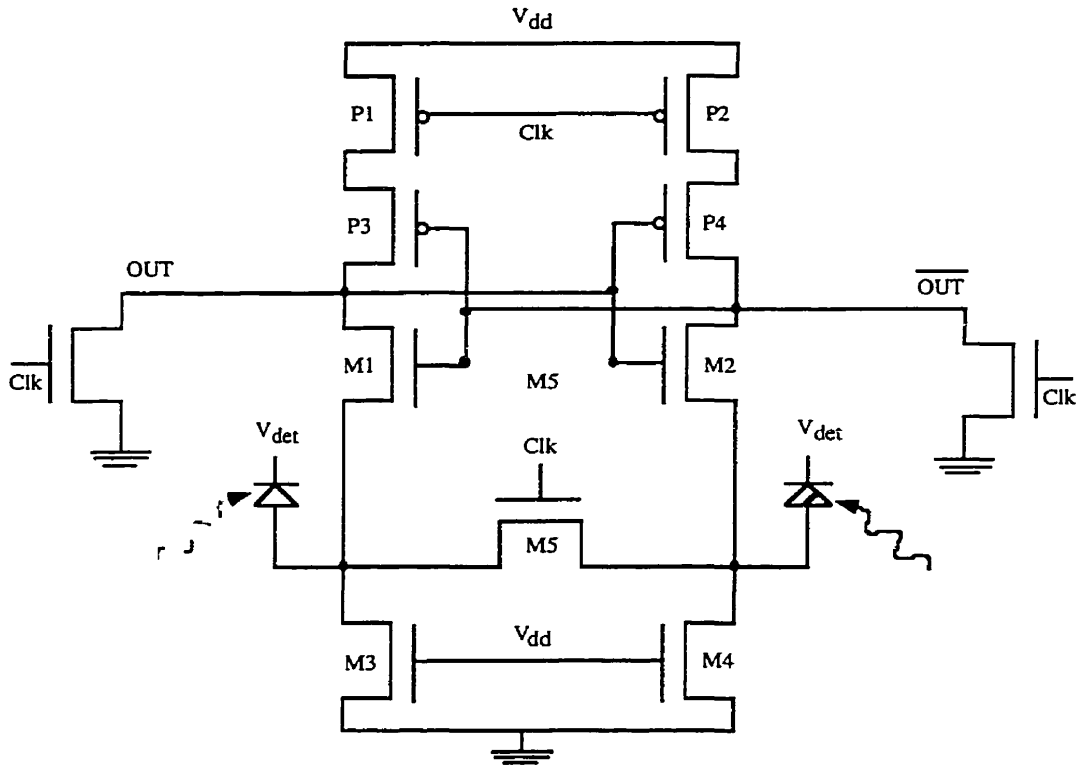


Figure 4.19: Modified CMSA-based receiver

The CMSA-based receiver is synchronous. In fact, this receiver is a compact clocking element with an analog optical input and a digital output. Such an element is key in the implementation of high-density optical inputs for clocked digital links and pipelines. It is the key element in the implementation of an optical-to-electronic digital demultiplexer [4.29].

The maximum bit rate is

$$B = \frac{1}{\Delta T_r + \Delta T_f + \Delta T_{meta} + \Delta T_{valid}} \qquad (4.23)$$

where the rise and fall times are ΔT_r and ΔT_f respectively, and ΔT_f is the time the outputs are not changing (see Figure 4.18). ΔT_{meta} is the time taken at each period to put the receiver in its metastable state. The bit rate is predominantly determined by the bandwidth

of the cross-coupled inverter, rather than the RC time constant of the input nodes [4.30]. To increase the bit rate, the duty cycle of the clock can be varied. The duty cycle is

$$\eta = \frac{\Delta T_{meta}}{\Delta T_r + \Delta T_f + \Delta T_{meta} + \Delta T_{valid}} = \Delta T_{meta} B \tag{4. 24}$$

The bit rate can also be increased by reducing ΔT_r and ΔT_f. The edge time is $\Delta T_r = \frac{C_{out}\Delta V}{I_{charging}}$ where ΔV is the voltage swing at the outputs, and $I_{charging}$ is the charging current for the output capacitance which is typically the capacitance of the gate of a buffer or of digital logic. It is important to notice that these times are not dependent on the input but on output nodes capacitance. The rise and fall times are reduced by increasing the sizes of the cross-coupled inverters (M1-M4 in Figure 4.17). However doing so increases the electrical power consumption of the receiver by increasing the metastable current I_{meta} and contributes to a higher switching power.

The power consumption for the CMSA-receiver is expressed as follows:

$$P_{elec} = \eta V_{dd} I_{meta} + 2C_{out}\Delta V^2\left(\frac{1}{\Delta T_r} + \frac{1}{\Delta T_f}\right) + 2C_g V^2 B \tag{4. 25}$$

Notice that in this equation the electrical power consumption is not dependent on the input node capacitance. The first term accounts for the power consumed by the metastable current. The second term is contributed by the switching power of the two output nodes. The last term represents the switching power of the cross-coupled inverters.

4.5.1 Measurements of fabricated test circuits

CMSA-based receivers were designed. The design topology is shown in Figure 4.17. A simulation of one CMSA receiver at 333 Mb/s is shown in Figure 4.20. CMSA-based test receivers have been fabricated in 0.8 and 0.5μm CMOS, and tested. Receivers with integrated silicon photodetectors, and receivers with electrical pads at the inputs were

designed and layed out in a similar fashion as described in Chapter 3. These pads are layed out to receive a flip-chipped detector, or a wirebond from a separate photodetector. Integrated PN junctions for photodetection with an area of 20μmX20μm have been designed. A PN photodetector is formed with p+ and n-well, and with n+ diffusion or n well in a p substrate, these have both been fabricated and tested. The responsivity of these detectors is less than 0.1A/W. The pads also facilitate all-electrical testing of the CMSA. Wirebonds to package pins or on-chip probes were used to supply the electrical input to the receiver, and monitor its output.

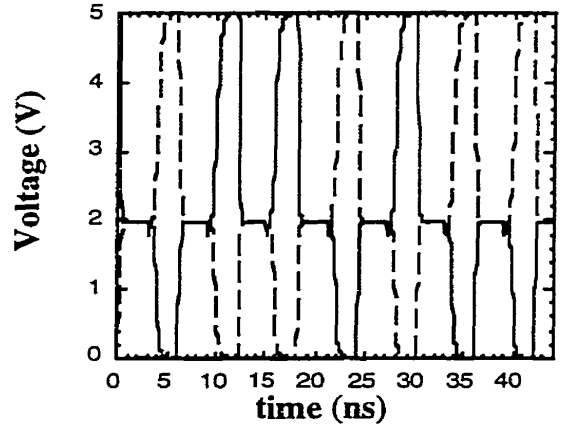


Figure 4.20: Simulation of the CMSA-based receiver

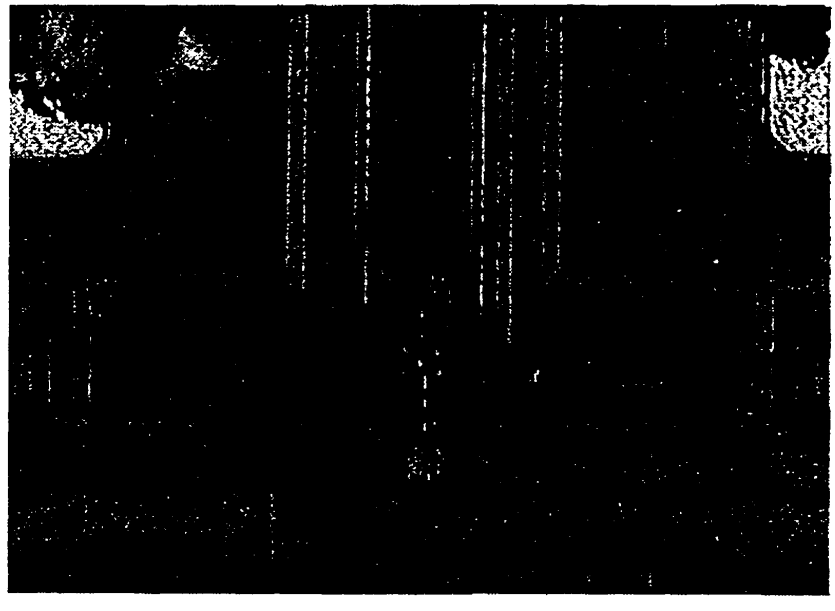


Figure 4.21: Photomicrograph of fabricated CMSA-based receiver

A fabricated CMSA receiver is shown in Figure 4.21. The receiver occupies a 50μmX50μm area. Two integrated silicon detectors can be seen on the right and left of Figure 4.21. Figure 4.22 shows a high-speed electrical test that has been performed at 25Mb/s. The risetime from the metastable voltage is about 1.5nsec. This suggests that the receiver can easily run at many hundreds of Mb/s. The metastable voltage agrees well with the simulation, and it is ~2V. The CMSA-based receivers have been tested optically in the set-up described in Chapter 2. Figure 4.23 shows a typical output at 3kHz. The input pattern is a repetition of 'high' 'low' 'high'. The minimum differential optical power to switch the receiver is 10μW, and it is mainly due to mismatch in the differential arm. When this level is exceeded, the switching to a full digital rail is initiated. The eye pattern for the receiver is always wide open. Error-free operation is achieved with the synchronization of data and clock. The minimum optical power to switch is independent of input capacitance and is not expected to vary with bit rate. The average power dissipated by the current mode receiver is 0.8 mW. The power consumption is independent of input capacitance. Each of the three photodetectors described above were wirebonded to the input pads of a CMSA and their bandwidth were measured by measuring the risetimes. Our experiments show that the bandwidth is not degraded. Figure 4.24 shows the edge time versus the input capacitance. The performance of the optical VLSI receiver is not affected over many picofarads. As in Figure 4.9a, the TIA-based receiver is used as a comparison. It is seen from Figure 4.24 that the TIA-based receiver edge speed is faster for higher optical powers whereas the CMSA-based receiver output risetimes are not dependent on optical input power above a given level. This level is determined by the degree of imbalance in the differential arms. Figure 4.9 and Figure 4.24 show that there exists a value of capacitance above which it is more advantageous to use a current-mode receiver than the conventional TIA-based receiver.

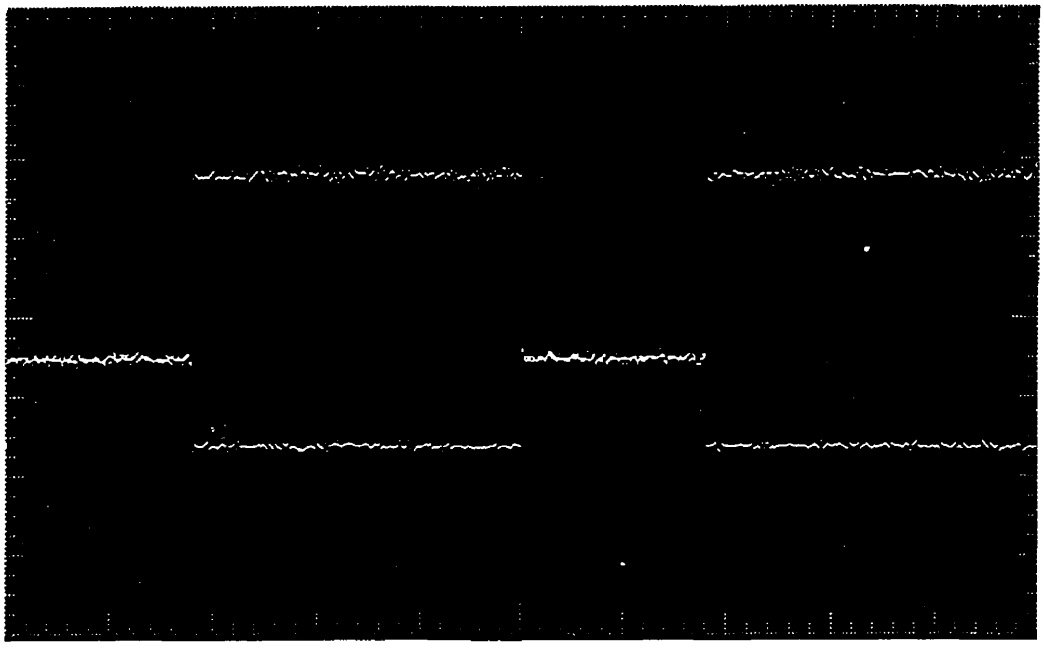


Figure 4.22: All-electrical test of CMSA-based receiver (8nsec /div).

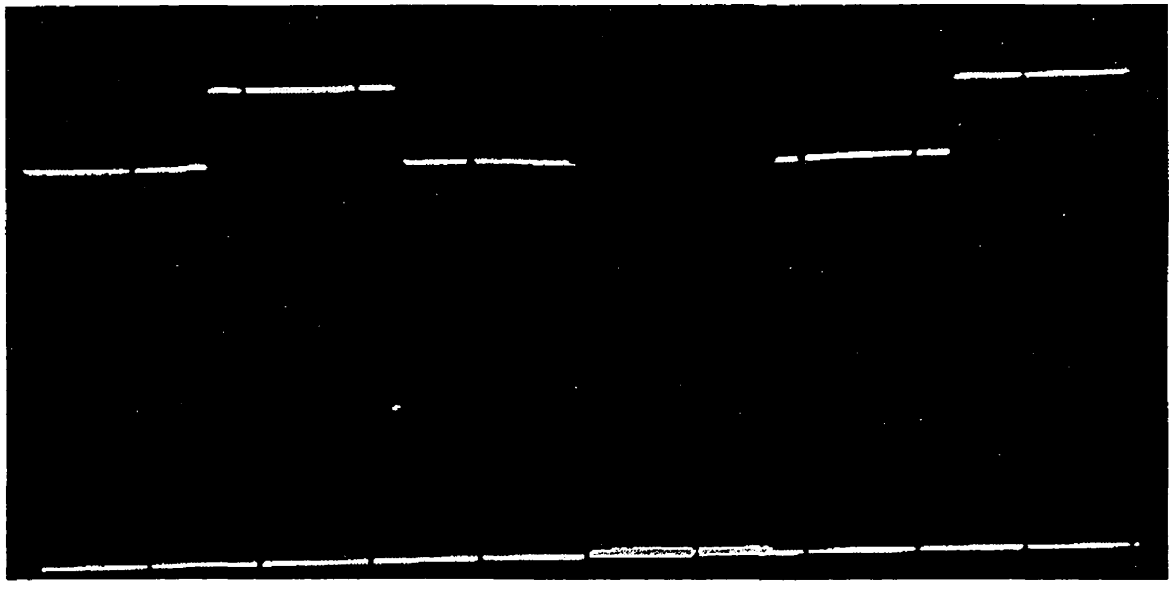


Figure 4.23: Optical test of CMSA-based receiver (output is inverted) at 3kb/s

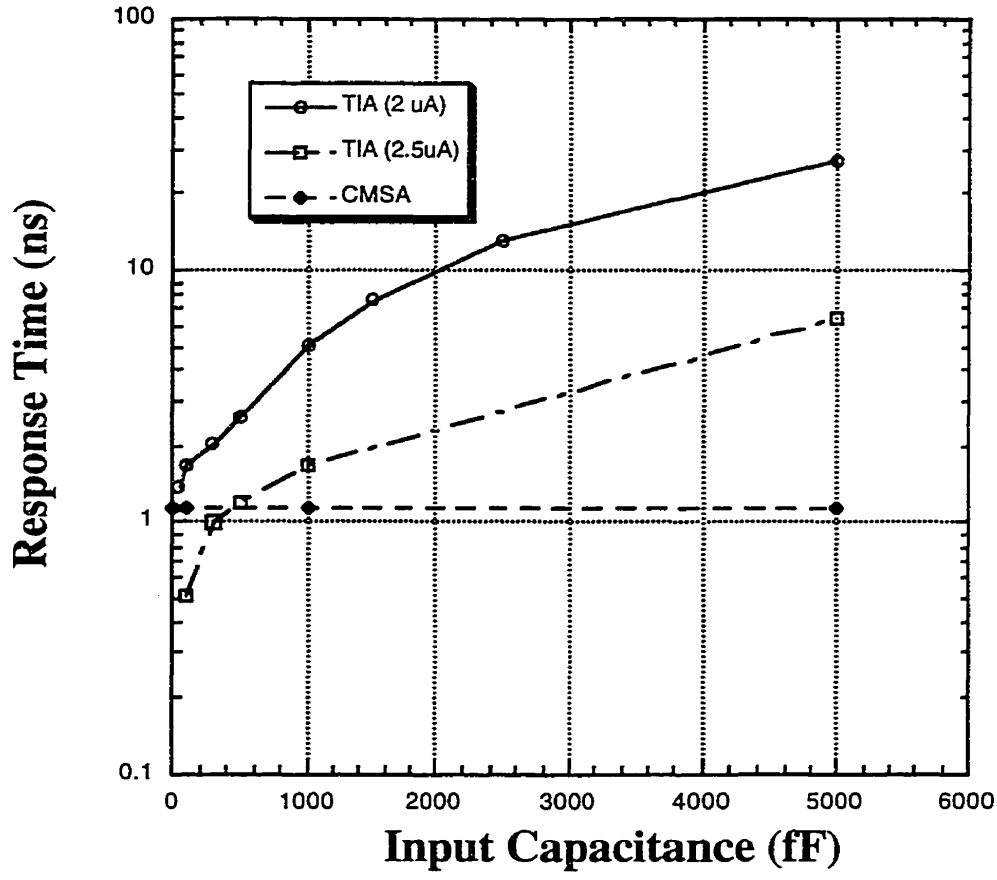


Figure 4.24: Simulated edge speed versus input capacitance

4.6 Misalignment Tolerant Array

The optomechanics of free-space systems can position an array with micron precision and maintain this precision for months with a rigid structure. In all free-space systems however, the active arrays must be removable for repairs and upgrade [4.31]. The separability of device planes from the optical interconnect layer is a desirable feature of optical systems and is critical in the design of optical backplanes as evidenced by this feature being incorporated into the waveguide-based POINT[4.32] and Honeywell [4.33] optical backplanes. The re-insertion time needs to be short to minimize the data loss in an operating system (assuming the repairs must be done on the live backplane). These requirements make micron precision costly and difficult if not impossible to achieve and maintain.

Fortunately, the optomechanics does not need to have micron precision for the system to operate. The alignment tolerance can be relaxed with oversized detectors and arrays used in conjunction with microlens concentrators. Oversized detectors can be connected to current-mode receivers the sensitivity and bandwidth of which are independent of the detector size [4.34] as discussed in section 4.3 and 4.5. The alignment tolerance can approach the pixel pitch when microlens concentrators are used [4.5]. To exceed this tolerance, an oversized smart pixel array that reroutes electrically the misaligned optical data to the correct channel is proposed here. The rerouter constitutes an overhead but as is shown below, it can be simple and compact. With this technique the alignment tolerance can be increased to an integer number of the pixel pitch.

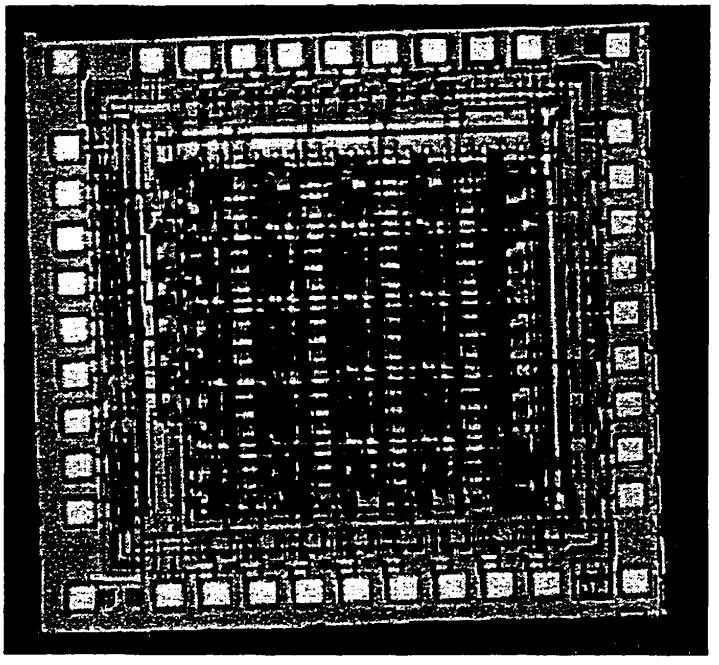


Figure 4.25: Photomicrograph of fabricated misalignment tolerant array

Two misalignment tolerant array chips were designed and implemented. Each chip consists of a 3X3 channel array in the middle of an oversized 5X5 array [4.35]. One array was implemented using GaAs PIN detectors flip-chipped onto CMOS electronic, and the other was implemented with a 2 μm CMOS technology with integrated PN detectors. The photomicrograph of the GaAs PIN detectors on CMOS chip is shown in Figure 4.25. The detectors are placed in a regular square array pitched at 250 μm and 300 μm. A hexagonal layout was also considered. This has the advantage that each detector has only 6 instead of

Position of Array	Control Bit (datapath select)
Aligned	A'BCD'
NW misalignment	AD
N misalignment	A'BD
NE misalignment	B'D
E misalignment	B'CD'
SE misalignment	B'C'
S misalignment	A'BC'
SW misalignment	AC'
W misalignment	ACD'

Table 4.4: Generation of the data path select bit

The design of one pixel is shown in Figure 4.26. Multiplexers sets up the datapath between the misaligned input and the correct electrical output. The 'data path select' bits have to be preset before data can go through the link. Figure 4.27 shows an array of 5x5 detectors (white boxes) illuminated by a 3x3 array of beams represented by dots. There are 9 possible positions in which the array of beams can fall on the detectors. The smart pixel corrects for misalignment by re-routing the signal electrically to the correct pixel output. Nearest-neighbor electrical connections are made between every pixel (8 connections: N, NE, E, SE, S, SW, W, NW). The misalignment, if any, is monitored using the data from 4 pixels at the edge of the field (detectors A, B,C and D in Figure 4.27) are used to determine the array position within the oversized array. The 'data path select' bits are generated with combinatorial logic as shown in Table 4.4 for each of the possible array position. This is used to control a 9-way router (a 9:1 multiplexer) at each pixel. An input can fall on any of 9 locations and is shifted by the router to its correct location. The electrical output from the pixel, is restored to its correct position by this process. The scheme can be extended given an appropriate change in the control and routing hardware.

There are some overheads associated with increasing the alignment tolerance in this way. Added latency comes from the time that is needed to stabilize these control signals and to establish the path through the selected passgate. In addition to this setup time, the signals experience an additional delay from a driver with a fanout of 9, and a passgate. The setup time can be slow (ms-μs) since only an occasional reset may be needed to compensate for the slow drift in the alignment. Otherwise the latency is minimal. The added power per pixel is estimated to be less than 1mW per pixel (including the monitoring and control circuit). Most of the power comes from the driver with a 1-to-9 fan-out at each pixel.

Minimal power is consumed by the alignment monitoring circuit (6 gates and 4 D-Flip-Flops (DFFs), and control line drivers) since it is operating at a low speed. Furthermore an additional (N+2)X(N+2)-NXN pixels are required, introducing additional power consumption and area. The router area and that due to the rerouting paths connecting the pixels to one another may be significant if extremely complex and small pitch pixels are used. In this design the pixel pitches are 250 and 300 μm. They consumed 3 to 4 times more area than that of a pixel without misalignment tolerant schemes.

Whereas this scheme works for lateral misalignment of integer pixel pitch which cause the same correction to be needed across the array, a potential problem is that roll causes misalignment at the edge of the device array but no misalignment of the pixels in the center of the device array. This problem can be worked around using more complex control of the router. Another potential 'fix' for this is the use of non-regular pixel layout. There is no requirement that the pitch and active area in the center of the device array be the same as that on the edge of the device array.

A problem with this technique is associated with fill-factor; if the beam falls in the region between active areas, the scheme will not work since little or no light will be detected or similar power will fall on a detector from two different signals (or on two detectors from the same signal). For the case of random alignment, a 20 μm diameter beam, 250 μm pitch and 240 μm active area, and an acceptable additional loss due to 'clipping' of 3 dB, this will occur 8% of the time, this problem may be reduced using non-regular layout of pixels and redundancy [4.5]. Some solutions such as redundancy [4.5] have been proposed to solve this problem.

4.7 Differential and Single-Ended Receivers

In the previous sections, the bandwidth, the sensitivity, the power consumption and the area were considered in the design of VLSI optical receivers. This section discusses the dynamic range which becomes an additional consideration. Dynamic range for a receiver is required so that it can operate in a range of input level. This range is determined by the degree the transmitter output optical power can be controlled. The dynamic range of a receiver must exceed the variation in the optical power incident on it. These variations are

the result of process non-uniformity at the transmitter array. The receiver must also compensate for process variations in the receiver manufacture process, and for variation in power supply voltage. This variation can be caused by switching or Δ-I noise [4.36] or when the voltage supply is reduced to decrease power consumption [4.3]. These non-uniformities invariably result in a shift in the threshold with respect to the high and low power levels ('1' and '0'). There is a limit to how much the threshold can vary with respect to the input signal level before the receiver stops working. This range defines the dynamic range. Within the dynamic range, these variations create pulse width distortion (PWD). PWD can be detrimental to the operation of a system [4.37]. Figure 4.28 shows the origins of PWD. PWD arises because the analog signal before the thresholder has a finite edge time. Any fluctuations from the input power level (e.g. IN and IN'), and in the threshold (e.g.Thresholdi, I=1,2,3) result in a variation in output pulse width. It is noted that a variation in optical power leads to a variation in the level and in the edge speed of the signal that is presented to the thresholder. Both effects contribute to PWD. Furthermore these variations lead to an increased bit error rate (see Chapter 5).

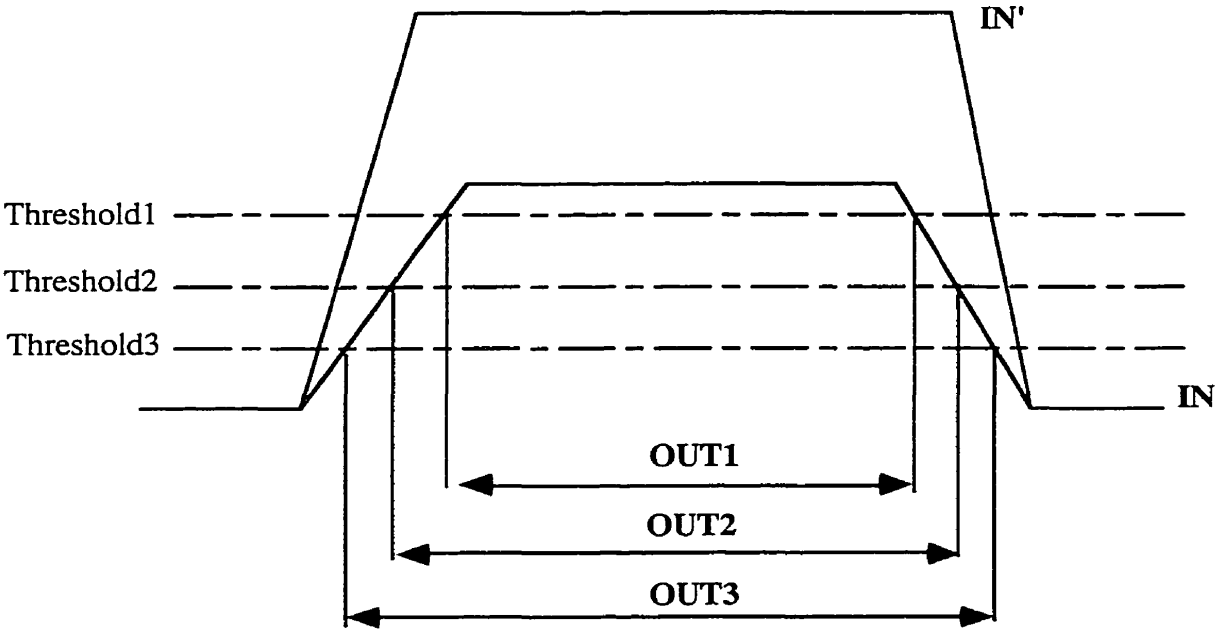


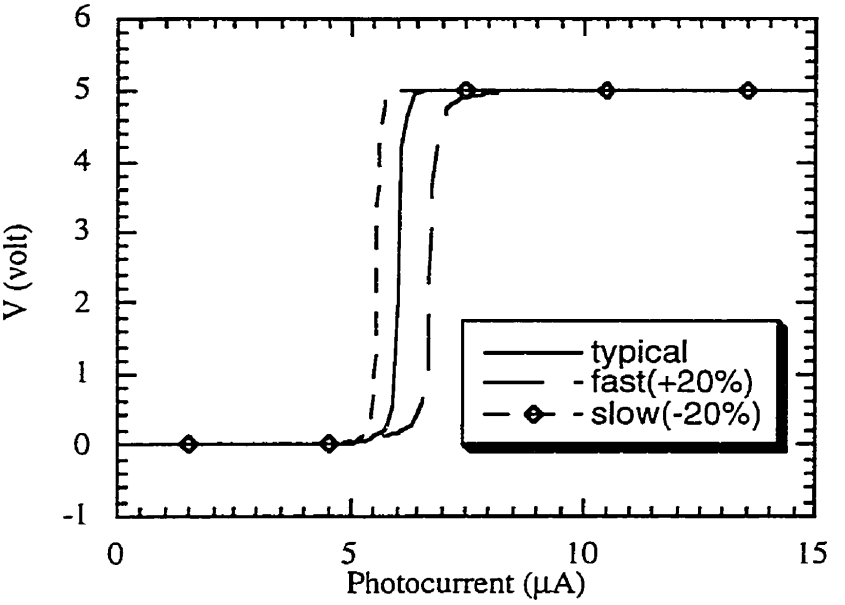
Figure 4.28: Origins of pulse width distortion

A good dynamic range can be achieved using fine tuning of the circuit after system assembly, automatic gain control (AGC) and/or setting the threshold from the average signal level. This flexibility may require an unacceptably complex receiver circuit which is impractical if large arrays need to operate simultaneously due to latency, area and electrical

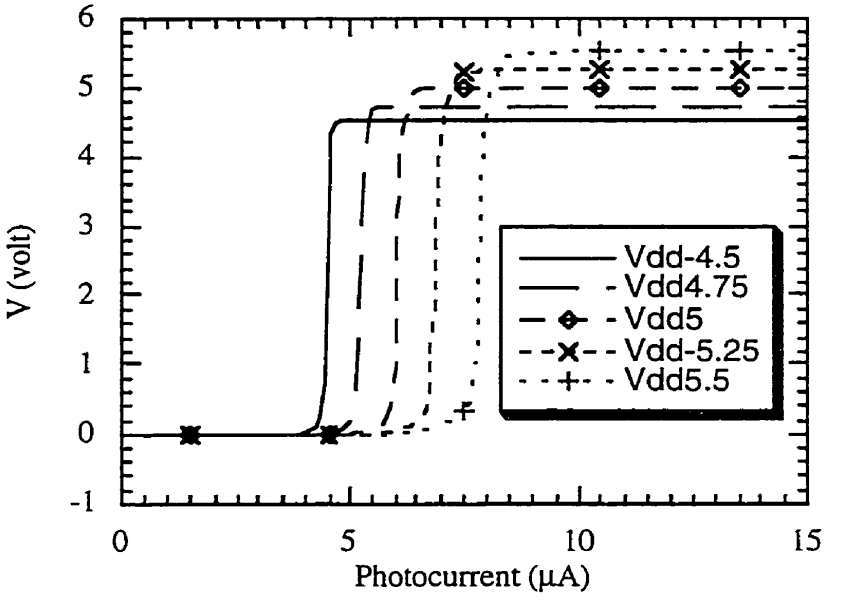
power consumption constraints. For example, a commercial Vitesse VSC7810 MSM/GaAs MESFET photodetector/TIA has a dynamic range of 19.4dB [4.38]. The receiver has an automatic gain control mechanism. The receiver occupies a 1.2X1mm die and consumes a power of 130mW. This is clearly unacceptable for designing large transceiver arrays. To gain some dynamic range without AGCs, a differential approach is taken. This can be used in conjunction with simple FET feedback loads [4.39] that improves the dynamic range further. Table 4.5 shows the choices that are available for the implementation of VLSI receivers. They are divided into three different groups depending upon their topology and the data encoding used. The receiver can be space (or optically), electrically or time differential. Each receiver in Table 4.5 is described below.

	Optically/ Space Differential	Electrically Differential	Time Differential
Single-rail TIA [4.19]	no	no	no
Dual-rail TIA [4.40]	yes	no	no
Differential TIA [4.41]	yes	yes	no
Sense Amplifiers [4.3]	yes	yes	no
Time-Differential receiver [4.42]	no	partially	yes
Active threshold receiver [4.42]	no	partially	no

Table 4.5: VLSI optical receiver choice



(a)

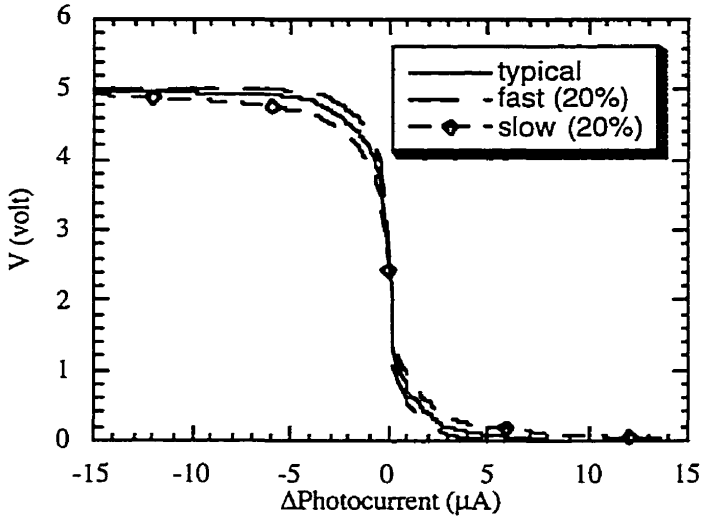


(b)

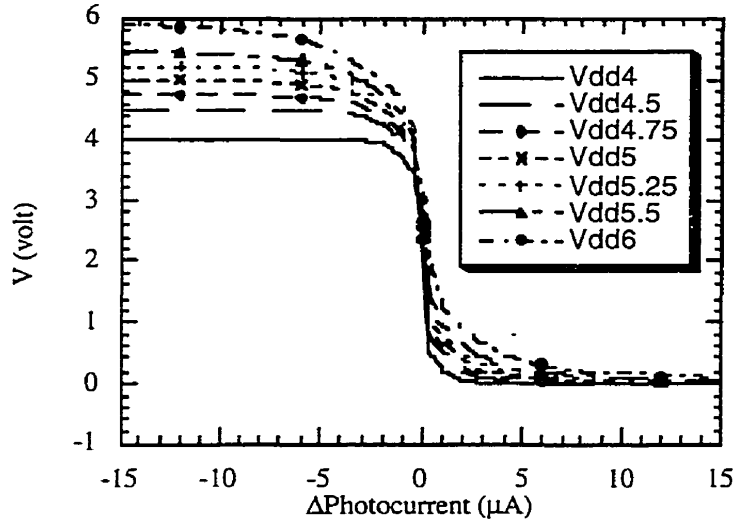
Figure 4.29: DC transfer functions under (a) process variations, and (b) Vdd fluctuations for single-rail TIA-based receiver.

The single-rail TIA receiver is not robust against optical power fluctuation, process variation, supply voltage fluctuation and common mode noise. Thus it is not suitable for complex system applications, as it imposes stringent requirements on other system components. This receiver necessitates a high contrast ratio signal in order for it to work. Figure 4.29 shows the DC characteristics under process and power supply variations. Under a +/-20% process variation, the threshold varies by as much as ~2μA, and for a +/-0.5V supply voltage fluctuation from the optimized one, the threshold can vary by as much as ~4μA. The sensitivity thus varies.

The dual-rail receiver uses two beams to encode the data. The polarity of the difference in optical power between the two beams is used for signalling. The receiver is designed to accept a bipolar input current that is supplied by two detectors in series. This type of signalling does not necessitate a high contrast ratio and is very tolerant to fluctuation in the optical power that comes from a single source. This results in a dynamic range much larger than the single-ended TIA. This also makes the receiver easier to design than the single-rail one since the threshold need not be accurately positioned since the differential input is always about the threshold. It is also found that this receiver threshold is very tolerant to process and power supply variations as shown in Figure 4.30.



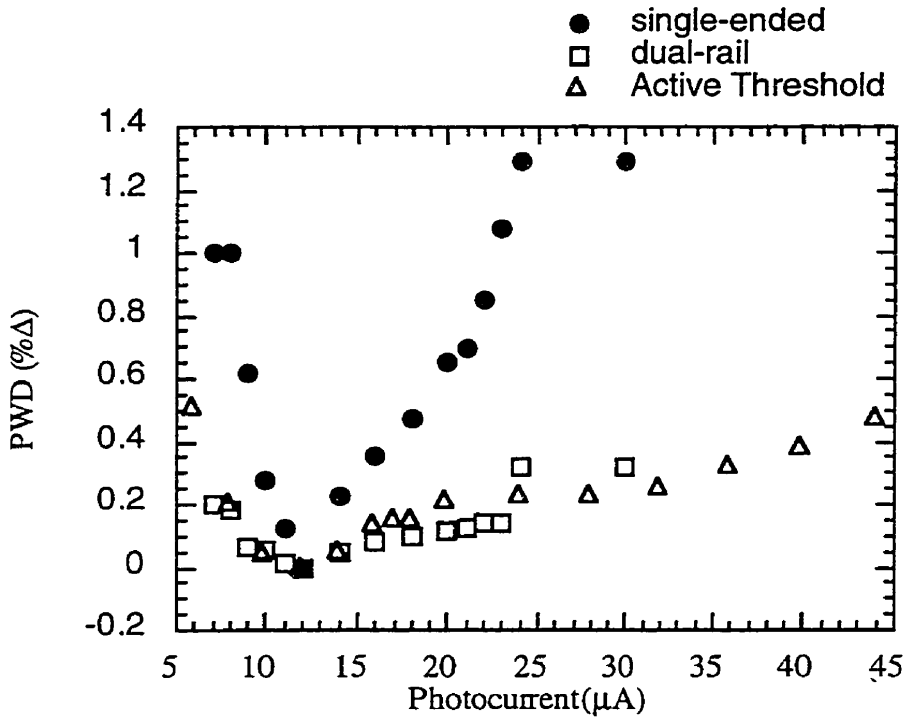
(a)



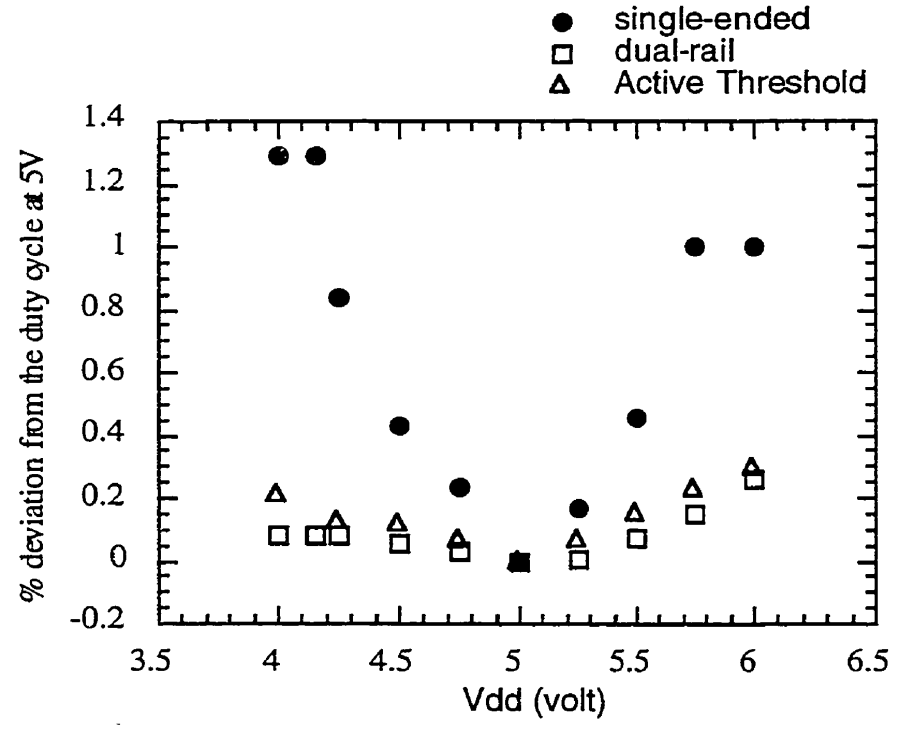
(b)

Figure 4.30: DC transfer functions under (a) process variations, and (b) V_{dd} fluctuations for dual-rail TIA-based receiver.

The optical power and threshold variation lead to pulse width distortion (PWD). Figure 4.31 shows a comparison between the PWD of a single and dual-rail receiver resulting from variation in the input levels and in the power supply. The contrast ratio of the modulators is assumed to be fixed at 3:1, and the input level is defined as the sum of the optical power in the 'high' and in the 'low' beam. The PWD in Figure 4.31a and b are respectively defined as percentage deviation from the duty cycle at an input level 12μA (9μA:3μA), and the percentage deviation from the duty cycle at V_{dd}=5V. For the single-ended case, the PWD is constant for low and high input levels as shown in Figure 4.31. The receiver stops working for those ranges. The dynamic range for the single-ended receiver is only 16μA, and it cannot tolerate a variation in the power supply of more than 1.5V. If the input level is below ~8μA, the swing is always below the threshold, and thus the receiver does not work. The dual-rail receiver always works for the range of interest.



(a)



(b)

Figure 4.31: Pulse Width Distortion (PWD) for (a) input and (b) power supply variations

A spatially differential receiver can be single-ended (TIA) or differential (sense amps) electrically. An electrically differential TIA has also been proposed by Novotny [4.41]. In addition to being robust against non-local power fluctuations, process and supply voltage variation, the sense amplifier-based receiver eliminates common mode noise, reduces switching noise and is more tolerant to process variation than the dual-rail TIA [4.43, 4.44]. The problem of PWD does not arise in synchronous receivers such as the current-mode sense amplifier-based receiver. The clock controls the length of the bit.

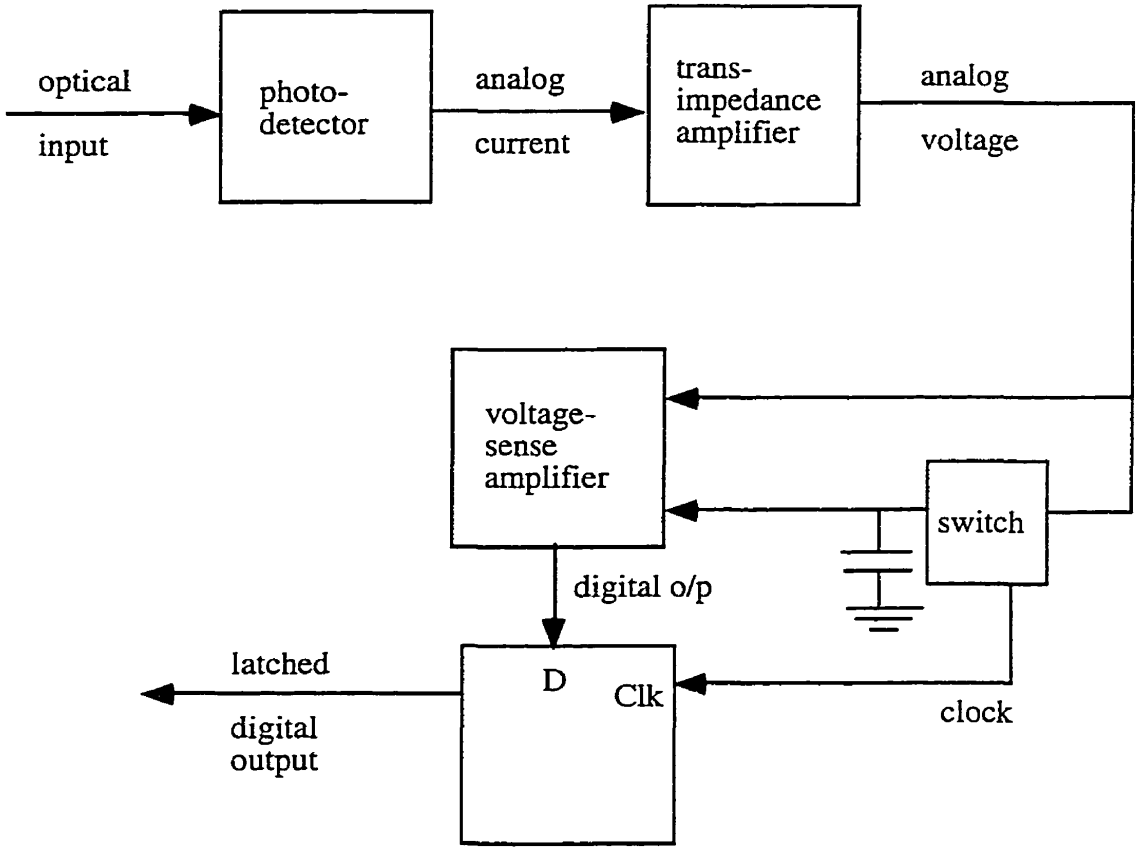


Figure 4.32: Implementation of a time-differential receiver

Spatially differential receivers need twice as many transmitters and detectors, and twice the optical power. To solve this problem and preserve the advantages of a differential scheme a time-differential receiver is proposed. In a time differential scheme, the single-

ended input (optical) is fanned out into two paths after reception. One path is delayed by one period with respect to the other, and then compared *before* it is thresholded and converted to a digital level. The polarity of this difference in *analog voltage* is decoded with a voltage sense amplifier. This receiver uses the biphase Manchester encoding scheme. The implementation of this concept is shown in Figure 4.32. The receiver is spatially and optically single-rail but is differential in the time domain. The signal at one clock period is dynamically stored and compared with the signal level at the next clock period.

The receiver is immune to power fluctuations that are slow compared to the clock speed, and to process variations since the input levels and process fluctuations in the single-ended TIA affects both delayed and undelayed paths equally. The sense amplifier is electrically differential thus it is robust against process variation and common mode noise. Therefore the dynamic range is large. The receiver is synchronous and has a speed overhead i.e. data can only be half as fast as the clock, thus one of two clock cycles is wasted. A simulation of the implementation is shown in Figure 4.33. The receiver was fabricated in 0.8μm CMOS, and tested. The receiver was found to decode properly at low frequencies (10's of Kb/s). The speed was limited by the off-chip driver. The minimum optical power needed to switch the receiver was measured to be 2μW for an integrated silicon photodetector with a responsivity of 0.1A/W at 850nm.

A higher data rate can be achieved with a receiver with active threshold adjustment. Instead of comparing the level during two distinct clock phases, the incident signal is compared with its DC level. A low-pass filter (LPF) is used to derive this DC level. The level is assumed to vary very slowly compared to the signal rate. The dynamic range of this receiver is thus large since the threshold is continuously derived and compared with the incoming signal. In general, the derived threshold is data-dependent. Long strings of '0's or '1's will produce non-optimal values of threshold. One solution is to use Manchester encoding which ensure data-independent average (DC) power. But this makes the data rate half of the clock. A better solution is to use bit scrambling [4.45] which can be used to operate at a full data rate and yet to a large extent guarantees a data-independent average power level. A bit scrambler encoder is easily implemented at the transmitter. The power consumption for both the time-differential and the active threshold receiver is about 10mW. The PWD is comparable to the differential receiver as shown in Figure 4.31. It is also, like the differential receiver very tolerant to process parameter variations. Thus the active threshold receiver appears to be a better option. It has the good dynamic range of

differential receivers but needs only one input beam, and it has a comparable power consumption to the time-differential receiver.

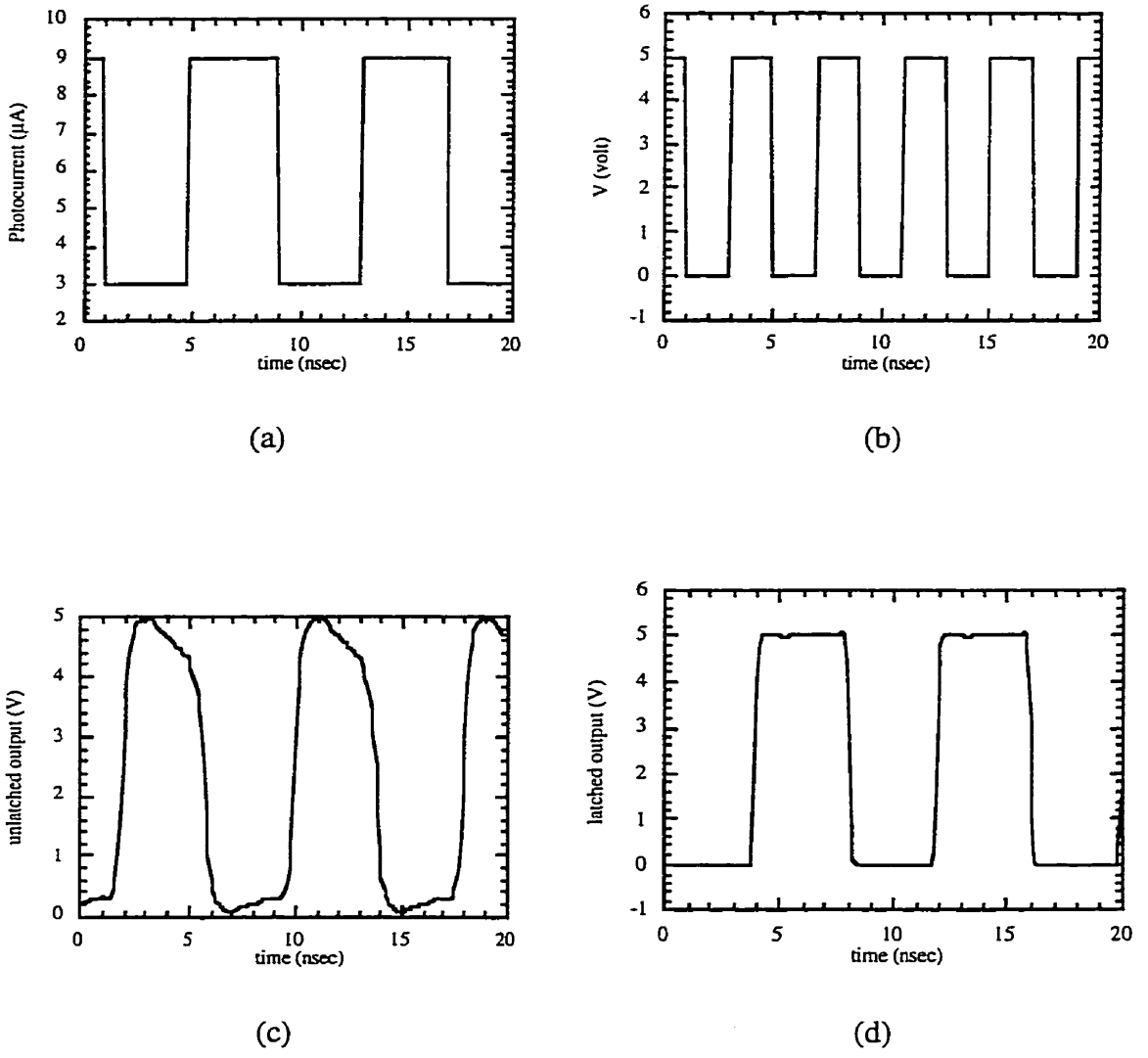


Figure 4.33: Simulation of a time-differential receiver

4.8 Transmitters

The VLSI optoelectronic transmitter consists of a pair of modulators, a modulator driver and a voltage swing converter (see Figure 4.34a). The driver switches the field across the modulator to produce a change of absorption in the device, and consequently a change in the reflected and output optical power. The driver is designed to supply the switching current required to (dis)charge the transmitter to achieve a given bit rate. The contrast ratio of the QCSE modulator is maximized when the voltage swing provided by the driver is around 7-8 volts for a wavelength of 850nm. A voltage swing converter interfaces between the high voltage driver and the CMOS logic levels (5V, 3.3V or lower) as shown in Figure 4.34. A voltage converter such as push-pull circuits [4.46] can directly drive the modulators but that arrangement is not optimal. The insertion of the driver permits the optimization of the transmitter area, speed and power. Optimization is needed when driving devices with capacitances that are an order of magnitude larger than the minimum gate capacitance of VLSI digital processing logic. Large modulator area makes the alignment of the read beams easier. Since capacitance is directly proportional to modulator area, it is thus important to optimize the design for the required alignment tolerance. The converter and the driver share the same bias rail. This is separated from the bias of the modulators and that of the digital logic so independent bias tuning can occur. Tuning is required to compensate for changes in temperature or non-uniformity in the fabrication process.

Figure 4.34b shows the model of the transmitter. A current source models the driver and a RC load models the modulator capacitive load. Typically, the RC constant of the modulator is a few hundreds of picoseconds [4.47]. This corresponds to a 20μm by 20μm active area MQW diode. Larger active modulator area results in an increase in alignment tolerance of the power beams onto the active area. However it also results in larger capacitive loads. To drive these loads, the design of the driver borrows from electronic line or pad driver designs, and adapts them for driving modulators. The modulator driver should be able to drive large modulators but still have a [4.48]:

- compact area (less than 30μmX30μm)
- moderate bit rate and a short delay (hundreds of Mb/s-a few Gb/s)
- low electrical power consumption
- good contrast ratio (large voltage swing output)

In the next sections, the design and optimization of the driver is presented. CMOS and BiCMOS driver design are investigated in section 4.8.1 and 4.8.2, and low-power adiabatic drivers in section 4.8.3.

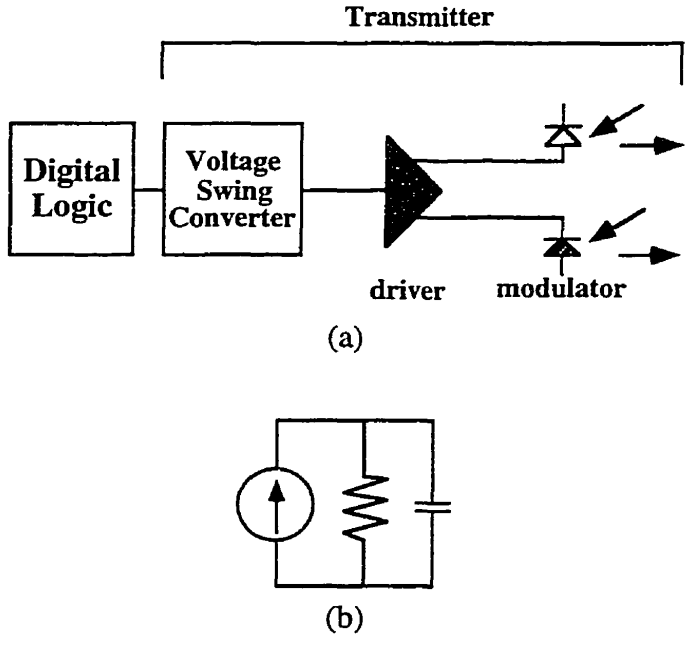


Figure 4.34: a) Modulator-based transmitter b) Transmitter model

4.8.1 CMOS driver

In this section the design and optimization of a tapered buffer (or superbuffer) for driving the modulators is discussed. CMOS devices provide the switching current for the load. For large capacitances or large area modulators, the area of the driver is increasingly large. There is a basic design trade-off between area and delay [4.49]. In order to drive a large capacitive load at a specified speed, the designer can increase the size of the device in order to provide a larger charging current. In doing so, the gate and parasitic capacitances also increase thus contributing to lengthen the delay. There is a lower limit to the delay when device sizes are increased. In a N-stage cascaded design, the gate capacitance of the stage connected to the load contributes to slowing down the (N-1)th stage. One may be tempted to increase its size. But increasing its size slows down the (N-2)th stage. Thus there is a trade-off between the number of stages (and area) and the delay. The optimum design is shown in Figure 4.35. The design consists in N cascaded stages. The size of each

stage is increasingly larger (tapered). A fixed ratio, a, between stages is kept. Unequal ratios have been used but with only slight improvements [4.50]. Design optimization consists of determining this ratio and the number of stages, N, that would result in a design with minimal delay and area.

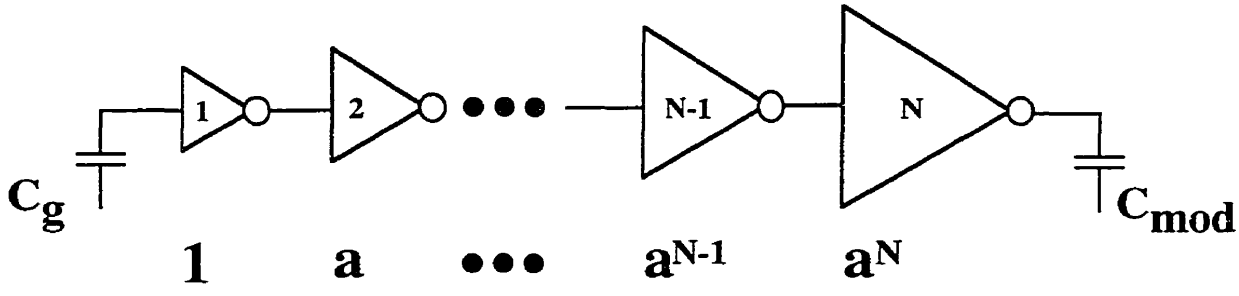


Figure 4.35: Tapered buffer

The delay is $\tau = Na\tau_{min}$. It can be shown that [4.49, 4.50, 4. 51]

$$N = \frac{\ln(C_{lr})}{\ln(a)} \tag{4. 26}$$

where C_{lr} is the ratio of the load capacitance to the minimum gate capacitance for a FET, C_g, and τ_{min} is the delay for a minimum sized inverter. From (4. 26), the delay is found:

$$\tau = \ln(C_{lr})\left(\frac{a}{\ln(a)}\right)\tau_{min} \tag{4. 27}$$

The delay is optimum when a=e~2.72. If a> e then the delay is longer but the number of stages, N is smaller for a given C_{tr}. Thus the area is decreased. If a<e, the delay is shorter but the number of stages and the area increases. When the drain or intrinsic output capacitance, C_d is taken into account, the optimum a is given by $a(\ln(a)-1) = \frac{C_d}{C_g}$ and it varies between 2.3 and 5 depending on the process [4.51].

Most of the total power consumed in the transmitter is due to switching. The static power is small. There is a static power dissipation associated with the constant read beams that are incident on the modulator. It can be minimized if highly sensitive receivers are used, or if the read beams are pulsed [4.52]. The power consumed in switching the load capacitance C_{load} is:

$$P_{load} = C_{load} V_{dd}^2 f \tag{4. 28}$$

where f is the bit rate or switching frequency and V_{dd} is the power supply voltage. In addition to the power dissipated in the load, there is the power consumed by the CMOS driver. The ratio of power consumed by the driver, P_{tot} to that by the load (P_{load}) is given by [4.49, 4.50]:

$$\frac{P_{tot}}{P_{load}} = \frac{\left(1+\frac{C_d}{C_g}\right)\left(1-\frac{1}{C_{tr}}\right)}{(a-1)} \tag{4. 29}$$

This ratio (or the total power consumption by the transmitter) can be decreased by increasing a. Doing so initially decreases the delay but for large a, the delay increases with it. The number of stages, N (see Equation (4. 26)) becomes smaller and individual devices larger. An optimization of the power-delay shows that there exists a lower bound just like in the optimization of the delay. The two optimums are related as follows [4.50]:

$$a_{power*delay} = \left(a_{delay}\right)^{\eta} \tag{4. 30}$$

where $\eta \cong 1.44$.

A CMOS driver was designed with a~2.7-2.8. The design is shown in Figure 4.36. Circular active area for the modulators are used to reduce their capacitance. The voltage converter (not shown) drives the input (IN). The voltage swing and the power supply V_{dd} of the driver are adjusted to drive the modulators at their highest contrast ratio. MQW

modulators are represented on the right of Figure 4.36 by diodes. This design is used as a comparison with the BiCMOS drivers described in 4.8.2. The use of BiCMOS for high-performance but compact modulator drivers is now considered.

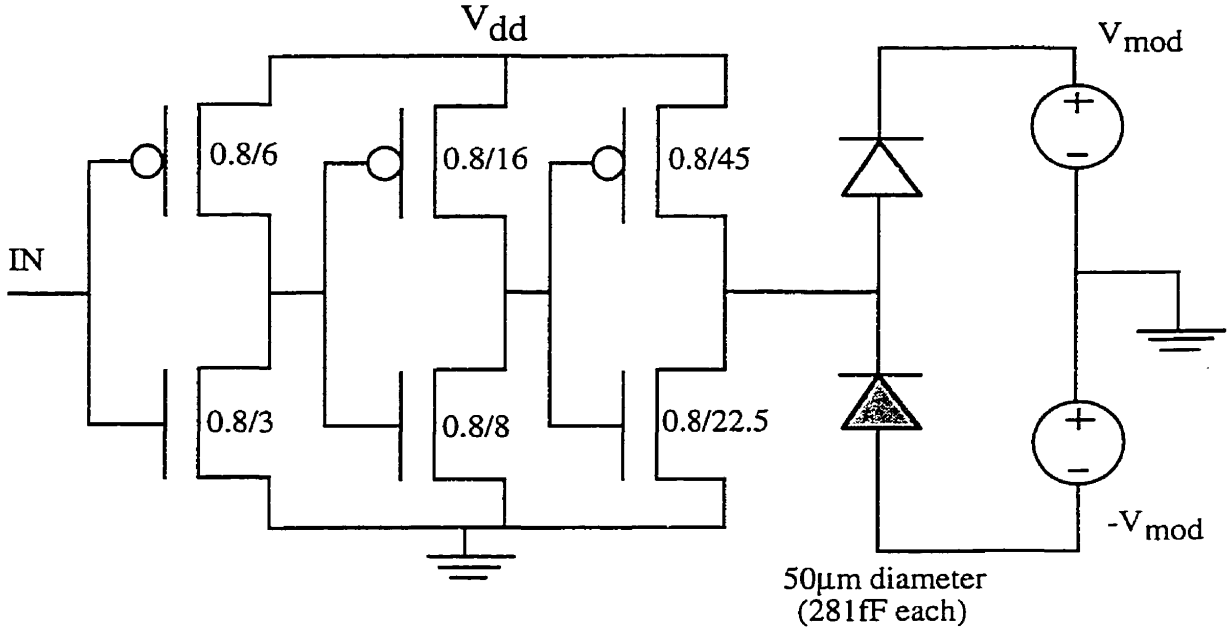


Figure 4.36: CMOS Transmitter

4.8.2 BiCMOS Transmitter Drivers

CMOS is recognized for its low power dissipation and its noise immunity [4.51, 4.53]. Its driving capabilities are poor. Bipolar devices on the other hand have superior performance with respect to driving capabilities [4.54]. The superior driving capabilities come about because the transconductance (or current per unit input voltage) of a bipolar device is exponentially related to the input voltage, while for a MOSFET it is linearly related. This results in a greater current per unit area for the bipolar devices. BiCMOS technology integrates both MOSFETs and bipolar devices onto the same platform, hence bringing the best of both worlds to the designer. Different applications would demand a different amount of CMOS and of bipolar circuitry. For example, bipolar devices have been introduced into mainly CMOS designs such as a memory system [4.55] in order to enhance its performance. On the other hand, CMOS has been introduced into high-performance bipolar designs for the implementation of low-power circuitry. The advantage of BiCMOS

over CMOS reveals itself when an optimization procedure is performed [4.56]. By way of example, a BiCMOS circuit can drive a 1pF load at 200 MHz at a supply voltage of 1.5V.

The driving capabilities of BiCMOS are exploited here to drive VLSI modulators. This technology has already been considered to implement modulator drivers [4.57]. However the devices in the work by Mansoorian were not optimized for speed. BiCMOS modulator drivers are considered here for high-speed data transmission [4.48, 4.54, 4.58]. BiCMOS drivers are typically faster than CMOS drivers when driving a capacitive load larger than a so-called crossover capacitance [4.54]. The advantage of BiCMOS over CMOS thus becomes clear when driving modulators with large active areas. Large active areas enable the improvement of the alignment tolerance of the read beams onto the reflective modulator.

A BiCMOS driver is potentially smaller than its CMOS counterpart when both are designed for the same delay and speed. It is smaller mainly because of the BJT's superior driving capabilities and consequently the absence of a tapered buffer as required for a CMOS transmitter. In the case of equal size CMOS and BiCMOS driver, the BiCMOS driver has a shorter delay and is faster than its CMOS counterpart. The power consumption is however about the same [4.54].

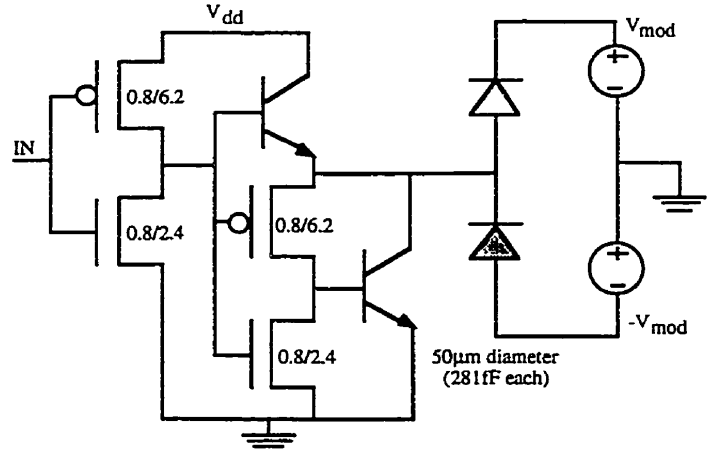
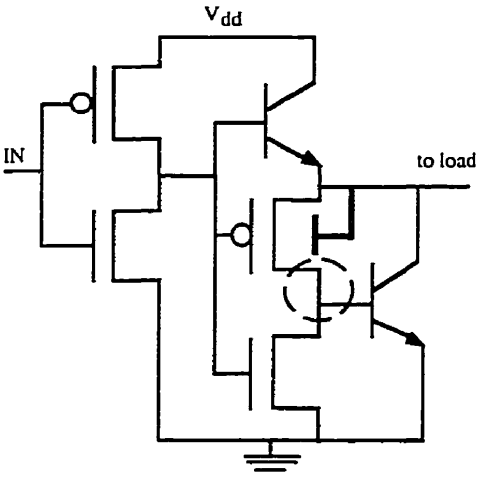


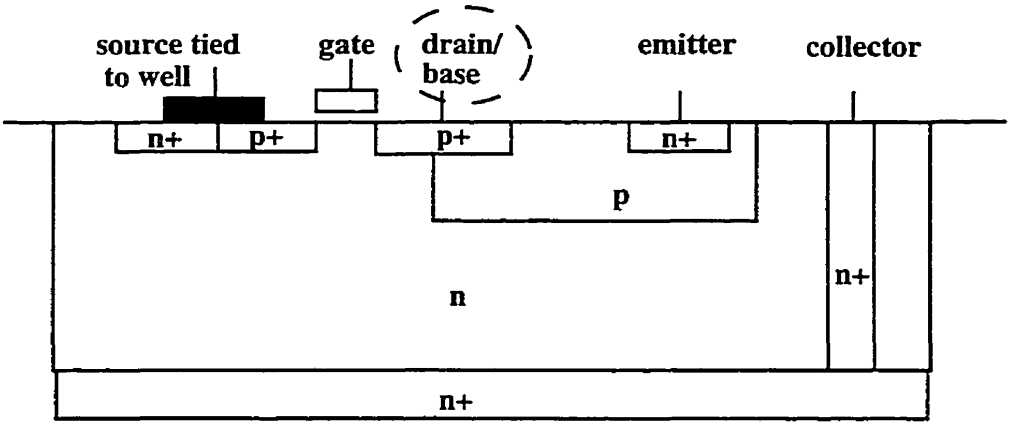
Figure 4.37: BiCMOS Transmitter

Figure 4.37 shows the design of a BiCMOS inverter. This driver however does not provide a full-swing to the modulators. The bipolar transistor junction voltage V_{BE} limits the swing. A full swing design can be implemented with complementary bipolar junction

transistors [4.59, 4.60, 4.61]. Simulations shows that at the same operating speed the peak switching current is 5mA per driver compared to 6mA for the CMOS driver. The load is 562 fF (two 55μm diameter MQW modulators).



(a)



(b)

Figure 4.38: Merged BiCMOS driver

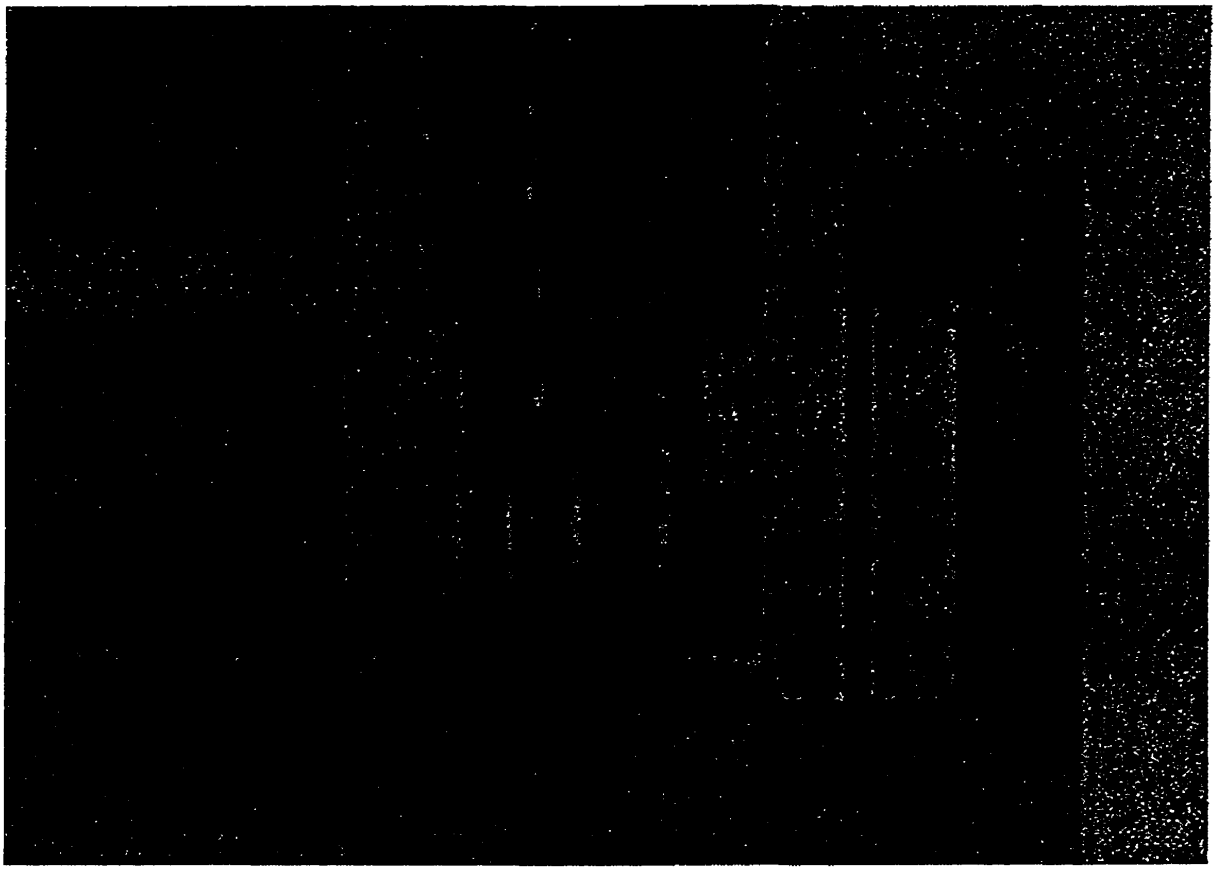
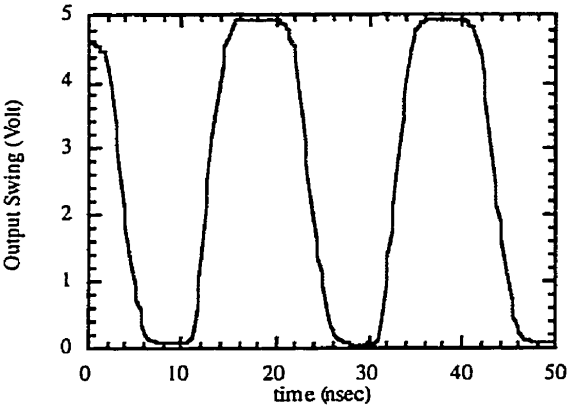


Figure 4.39: Fabricated BiCMOS modulator driver

To reduce the driver's size further, a merged layout is used [4.62, 4. 63]. The design of the merged structure is shown in Figure 4.38. The drain of the PMOS and the base of the NPN BJT are merged thus leading to a more compact layout. Both devices also share the same n-well. The source of the PMOS is tied to the well. The capacitance of the combined structure is reduced, and the speed improved. The improvement in delay and speed becomes more significant at low power supply voltages [4.58, 4.64]. The fabricated transmitter is shown in Figure 4.39. Figure 4.40 shows the experimental and simulated output voltage when driving a ~20pF load at 100Mb/s. The voltage swing does not fully go to the rails (ground and V_{dd}=5V) as expected of such a BiCMOS technology that does not have complementary bipolar junction transistors.

5 nsec / div

(a)



(b)

Figure 4.40: Driver output voltage swing (a) experimental (b) simulated.

4.8.3 Adiabatic Modulator drivers

As discussed in the previous section, the power consumption of CMOS and BiCMOS drivers are comparable. The question now is how can their power consumption be reduced. Speed can be traded off for power consumption in two ways (refer to Equation (4. 28)): 1) by reducing the voltage swing delivered to the modulator and 2) by decreasing the modulator capacitance. It would be difficult to decrease the voltage swing without sacrificing the contrast ratio. Careful modulator design may improve the contrast ratio [4.47] but as a general rule the electric field change required to provide an adequate exciton shift does not scale down easily. A tapered design described in the previous sections can be used without reducing the voltage swing. But the energy per switch never goes below CV^2. Secondly, the reduction in capacitance would be difficult because the capacitance of

the modulator is fixed by the device design, and because larger modulators are preferred for a better system alignability.

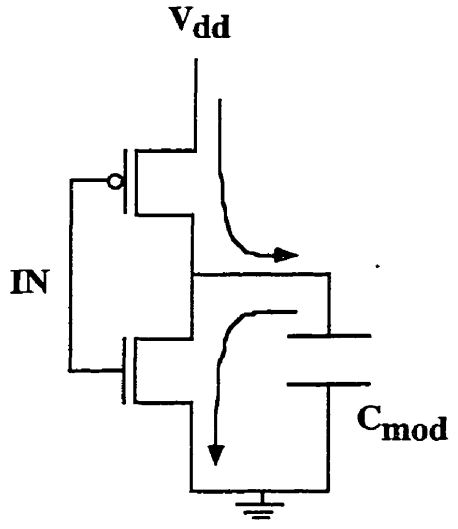


Figure 4.41: Conventional modulator driver

By operating the transmitter adiabatically, speed can be traded off for power consumption without decreasing the voltage swing. Figure 4.41 shows a conventional modulator driver. In that figure, the charging and discharging path are shown. When the power supply is suddenly switched on, the voltage at the output of the modulator driver rises exponentially in time to V_{dd}. During this same time, the drain-source potential of the PMOS reduces exponentially from V_{dd} to a voltage close to zero hence turning the device on. The time for the signal to reach equilibrium and to settle is proportional to the RC_{mod} constant, where R is the on-resistance of the PMOS and C_{mod} is the capacitance of the modulators. The energy supplied to the driver is $C_{mod}V_{dd}^2$. Half of this energy is dissipated in the PMOS, and half is stored in the capacitor. The stored energy is dissipated in the NMOS when it is discharged (when the input goes high). Therefore the totality of the supplied energy is dissipated.

The energy dissipated by a charging or discharging event can be reduced below CV^2 if the rate of charge transfer from the supply to the modulator capacitance is controlled [4.65, 4.66, 4.67, 4.68]. The transfer is slow and in the limit *adiabatic*. Two methods exist for controlling the charging: 1) by stepwise charging and 2) by ramping the voltage supply.

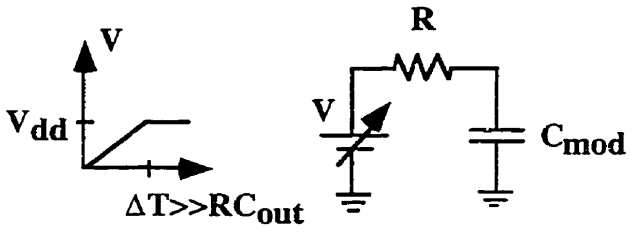


Figure 4.42: Model for load charging and discharging

Consider the RC network shown in Figure 4.42 which models the charging (through the PMOS) and discharging (through the NMOS) of the modulator(s). In that figure, R represents the on-resistance of the channel, and C_{out} the output capacitance (dominated by the modulator capacitance). The power supply voltage is slowly ramped up to V_{dd} in a time $\Delta T >> RC_{mod}$. The slow voltage rise keeps the voltage across the PMOS small and most of the ramp voltage appears across the capacitor (capacitor reactance is high when switching transient is slow). Since v_C is the ramp voltage appearing across the capacitor, the charging current is $i = C_{out}\frac{dv_C}{dt} = I$=constant when $0<t<\Delta T$, and zero any other time (pulse of current ΔT long). The total charge supplied to the output capacitive node is

$$Q_{\text{supplied}} = \int_0^{\infty} i\,dt = I\Delta T = C_{out}V_{dd} \tag{4.31}$$

so that $I = C_{out}V_{dd}^2/\Delta T$. The energy dissipated in the PMOS is hence [4.65, 4.69]

$$\begin{aligned} E_{idissipated} &= (I^2R)\Delta T = \left(\frac{C_{out}V_{dd}}{\Delta T}\right)^2 R\Delta T \\ &= \left(\frac{RC_{out}}{\Delta T}\right)C_{out}V_{dd}^2 \end{aligned} \tag{4.32}$$

$\bar{\rho}$ is a weighted average of each node (passgate) time constant, m is the number of time constants required for each charging step and, $T=NmR_iC_{mod}$ is the time available for one full charging (risetime). The corresponding energy dissipation is

$$E_{opt} = \frac{3}{2}\sqrt[3]{\frac{4m\bar{\rho}}{T}}C_{mod}V^2 \qquad (4.35)$$

The data to be transmitted is fed to a circuit that initiates the charging/discharging cycle (closing the passgates in-turn). A finite state machine turns on the passgates in succession at each clock cycle. The first circuit is a simple shift register that open the passgates in turn with the aid of a clock. The voltage swing of the input can be that of the digital logic as long as the swing is large enough to close and open the passgates. Thus the voltage swing converter can be eliminated. The overhead should be carefully evaluated . A large capacitive load would be more advantageous.

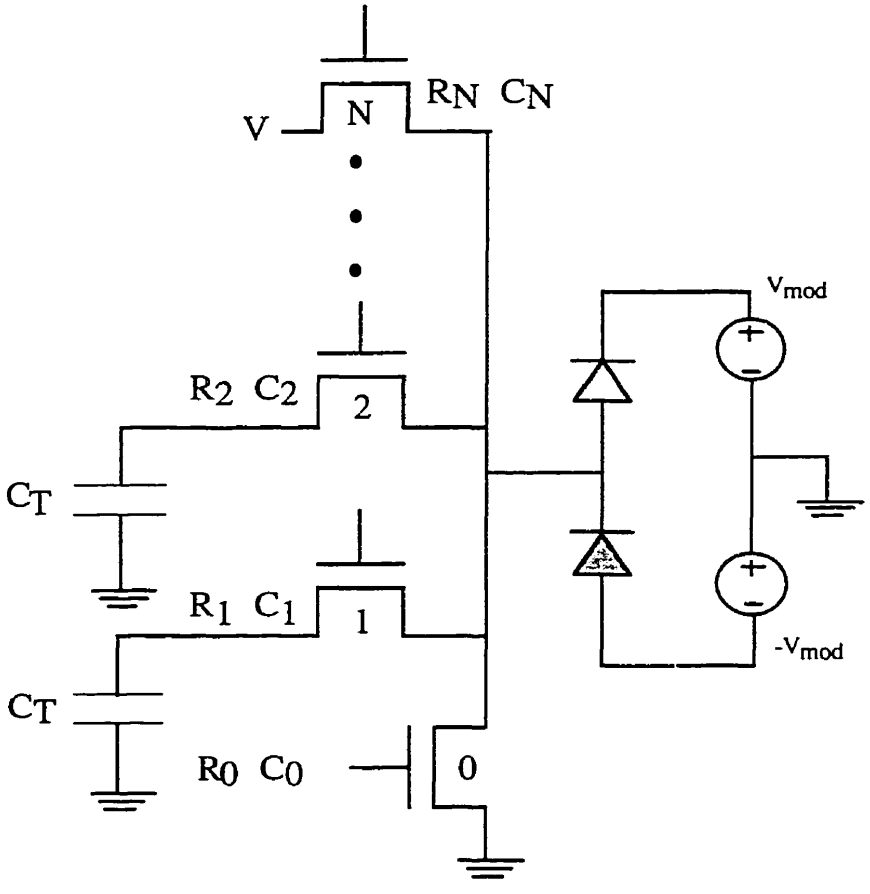


Figure 4.43: Stepwise charging

In both the resonant power supply and stepwise charging approach, energy dissipation per switch is reduced below the conventional CV^2 by sacrificing speed. By increasing T, the energy per switch decreases. The amount of the slow down necessary to retain the advantage of adiabatic switching depends on the modulator capacitance, and the overhead circuitry. In any event, parallelism can be used to conserve the data throughput [4.3] (see Figure 4.44). By demultiplexing high-speed input data onto N transmitter with sub-CV^2 switching energy, the overall power consumption of the transmitter can be reduced. This comes with a penalty in the area.

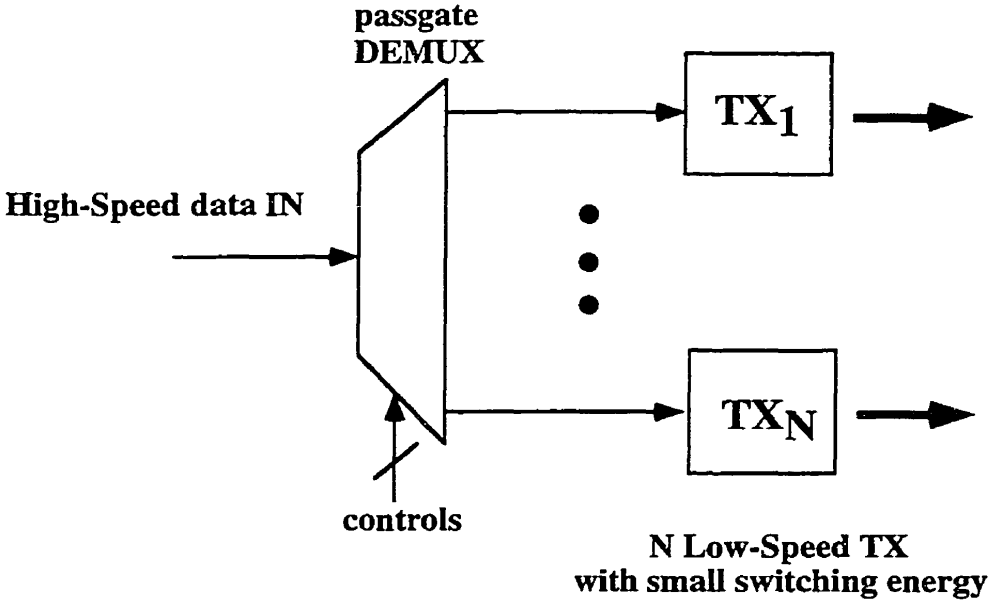


Figure 4.44: Parallelism for low-power

4.9 Conclusions

In this chapter, a hybrid CMOS technology that flip-chips p-i(MQW)-n diodes onto commercial CMOS was presented. The diodes can act as a detector or a modulator for receivers and transmitters. CMOS VLSI transceivers were designed, and tested. Four aspects of the VLSI receiver were the point of focus: 1) its alignability, 2) its power consumption, 3) its sensitivity and bandwidth, and 4) its dynamic range. Current-mode designs of VLSI receivers were introduced. With this technique, the receiver can have a performance that is minimally affected by increasingly large detectors. Oversizing the

detectors constitutes a way to increase the alignment tolerance of the receivers. Furthermore a misalignment tolerant array was proposed to increase the alignment tolerance by one full receiver pitch. The design of a current-conveyor and a current-mode sense amplifier-based receiver were presented as two implementations of current-mode designs. The sense amplifier is attractive because of its compactness and its low-power consumption. Another analog technique that was successfully used for the design of VLSI receivers was buffering the input and/or the output of the receiver. With this technique, a gain independent of bandwidth is achieved. Finally techniques were considered to increase the dynamic range of receivers without the use of automatic gain control circuits (AGC) which are area and power consuming.

This chapter also considered the design of modulator drivers. Compact drivers were designed to drive large modulators. Modulators were oversized to increase the alignment tolerance of the read beams onto the modulators. The drivers were optimized for speed and power consumption. BiCMOS was also considered for improving the drivability of large modulators.

4.10 Appendix

Derivation of $\frac{d\langle i_{na}^2 \rangle}{df}$

Summing all the independent noise sources at the input of the small-signal noise equivalent circuit for the upper CC yields:

$$\frac{d\langle i_{nau}^2 \rangle}{df} = \left[4kT\zeta\left(g_{m1} + g_{m3}\right) + 2e\left(I_{l1} + I_{l2} + I_{l9}\right) + 2\frac{K_F I_{dq}^{AF}}{fC_{ox} L_{eff}^2} \right] \tag{4. 36}$$

Similarly referring the noise sources to the input of the lower CC, it is found that:

$$\frac{d\langle i_{nad}^2 \rangle}{df} = \left[4kT\zeta\left(g_{m5} + g_{m7}\right) + 2e\left(I_{l7} + I_{l8} + I_{l10}\right) + 2\frac{K_F I_{dq}^{AF}}{fC_{ox} L_{eff}^2} \right] \tag{4. 37}$$

The three terms represent respectively the contribution by the channel noise of the input transistors, by the gate leakage currents and by the 1/f or flicker noise. We note that at high frequencies, the channel noise of each FET is conducted to its gate through its gate-to-drain capacitance. The effective gate current noise increases by the square of the frequency. The gate and channel noise is correlated since they both originated from thermal fluctuations in the channel.

The noise sources in the upper and in the lower CC contribute to the total input referred noise for the push-pull CC thus the total noise is the sum of Equations (4. 36) and (4. 37),

$$\frac{d\langle i_{na}^2\rangle}{df}=\left[4kT\zeta\left(g_{m1}+g_{m3}\right)+2e\left(I_{l1}+I_{l2}+I_{l9}\right)+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]$$
$$+\left[4kT\zeta\left(g_{m5}+g_{m7}\right)+2e\left(I_{l7}+I_{l8}+I_{l10}\right)+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]$$
$$+2\chi\sqrt{\left[4kT\zeta\left(g_{m1}+g_{m3}\right)+2e\left(I_{l1}+I_{l2}+I_{l9}\right)+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]}$$
$$X\sqrt{\left[4kT\zeta\left(g_{m5}+g_{m7}\right)+2e\left(I_{l7}+I_{l8}+I_{l10}\right)+2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]}$$

The last term is a correlation term between the two noise sources. $-1\le\chi\le 1$ quantifies this correlation.

Derivation of $\frac{d\langle v_{na}^2\rangle}{df}$

The potential at the input node of the receiver circuit (point X in Figure 4.4) is given by

$$v_{in}=\frac{v_{g5}g_{m5}+v_{g3}g_{m3}}{g_{m5}+g_{m3}} \tag{4. 38}$$

where g_{mi} is the transconductance of the FET I. Differentiating Equation (4. 38), and assuming that the noise on the gate of M3 and M5 are independent and uncorrelated,

$$\frac{d<v_{in}^2>}{df}=\frac{d}{df}\left\langle(v_{g5}A+v_{g3}B)^2\right\rangle=A^2\frac{d}{df}\left\langle v_{g5}^2\right\rangle+B^2\frac{d}{df}\left\langle v_{g3}^2\right\rangle \tag{4. 39}$$

where $A=\frac{g_{m5}}{g_{m5}+g_{m3}}$ and $B=\frac{g_{m3}}{g_{m5}+g_{m3}}$. Here it is assumed that the transconductances, g_m are not frequency dependent. Furthermore,

$$\frac{d\langle v_{na}^2\rangle}{df} = \frac{d\langle v_{in}^2\rangle}{df}$$

(4. 40)

It is assumed that a noiseless reference is provided at the source of M4 and M6. Therefore

$$\frac{d\langle v_{g3}^2\rangle}{df} = \frac{d\langle v_{g4}^2\rangle}{df} = \frac{1}{g_{m4}^2}\left[4kT\zeta(g_{m2}+g_{m4}) + 2e(I_{l3}+I_{l4}) + 2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]$$

$$\frac{d\langle v_{g5}^2\rangle}{df} = \frac{d\langle v_{g6}^2\rangle}{df} = \frac{1}{g_{m6}^2}\left[4kT\zeta(g_{m6}+g_{m8}) + 2e(I_{l5}+I_{l6}) + 2\frac{K_F I_{dq}^{AF}}{fC_{ox}L_{eff}^2}\right]$$

(4. 41)

where k is Boltzmann's constant, T the temperature in Kelvin and $\zeta = 0.7$ for silicon FETs [4.2].

Derivation of $\frac{d\langle i_{ni}^2\rangle}{df}$

Consider the transformed signal source I_d and the output current I_{out} in Figure 4.5. The CCI front-end *noiseless* gain is defined:

$$K_{CCI} = \frac{I_{out}}{I_d}$$

(4. 42)

By the current divider rule, the output current:

$$I_{out} = I_d \frac{Z_d}{Z_d + Z_{in}} H$$

(4. 43)

Therefore the overall CCI transfer function is given by

$$K_{CCI} = \frac{Z_d H}{Z_d + Z_{in}} \tag{4. 44}$$

Now consider the noise sources $\frac{d\langle i_{nd}^2 \rangle}{df}$, $\frac{d\langle i_{na}^2 \rangle}{df}$ and $\frac{d\langle v_{na}^2 \rangle}{df}$. The current noise into the CCI, $\frac{d\langle i_{nin}^2 \rangle}{df}$ is:

$$\frac{d\langle i_{nin}^2 \rangle}{df} = \left(\frac{d\langle i_{nd}^2 \rangle}{df} + \frac{d\langle i_{na}^2 \rangle}{df} \right) \left| \frac{Z_d}{Z_d + Z_{in}} \right|^2 + \frac{\frac{d\langle v_{na}^2 \rangle}{df}}{\left| Z_d + Z_{in} \right|^2} \tag{4. 45}$$

and

$$\frac{d\langle i_{nout}^2 \rangle}{df} = |H|^2 \left[\left(\frac{d\langle i_{nd}^2 \rangle}{df} + \frac{d\langle i_{na}^2 \rangle}{df} \right) \left| \frac{Z_d}{Z_d + Z_{in}} \right|^2 + \frac{\frac{d\langle v_{na}^2 \rangle}{df}}{\left| Z_d + Z_{in} \right|^2} \right] \tag{4. 46}$$

By dividing Equation (4. 46) by the gain of the CCI (Equation (4. 44)) squared, the input referred noise is found:

$$\frac{d\langle i_{ni}^2 \rangle}{df} = \frac{\frac{d\langle i_{nout}^2 \rangle}{df}}{|K_{CCI}|^2} = \frac{d\langle i_{nd}^2 \rangle}{df} + \frac{d\langle i_{na}^2 \rangle}{df} + \frac{d\langle v_{na}^2 \rangle}{df} |Y_d|^2 \tag{4. 47}$$

where $|Y_d|^2 = 1/|Z_d|^2$.

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Chapter 5: Optical Interconnect Modeling

A model is an indispensable tool that improves the efficiency of the design process and aids in the reduction of the cost of a finished system or product. The purpose of a model is at least three-fold: to provide a methodology 1) for the design and optimization of a system, 2) to quantitatively evaluate the performance before the system is built, and 3) in assessing how reality agrees with the model and better understand the operation of the system. A model is especially needed when designing a system with a large number of interacting components.

In this chapter, a novel model of an optical interconnect is proposed. The model takes into account the key design parameters of the receivers and the transmitters. If this model was fully implemented, the designer would be:

- able to explore the impact of the scaling and the limits of current technologies on system performance, and suggest directions for technology improvement (the model is independent of technology and the values of the parameters chosen accordingly).
- able to explore parameter design space and performance optimization.
- able to predict the behavior of a *particular* design under various operating conditions (sub-optimal) such as varying bit rate, optical input power, and power supply voltage.

Most models only satisfy the first and second requirement but not the third. Examples of such models can be found in [5.1] and [5.2, 5.3], respectively. The third point is important because operating conditions are not always optimal, and a design should be versatile and re-useable. A design is often used in a wide variety of systems even though it is not necessarily optimal.

The optical interconnect that is modeled here has its transceivers integrated in a large 2-D array (for example 32 by 32). These transceivers are optical inputs and outputs (I/Os) to VLSI digital logic providing direct on-chip terminations [5.4]. Consequently, the transceivers must be small and have a low electrical power consumption. To achieve these requirements, the receivers do not have automatic gain control (AGC) circuitry and the transmitters do not have power and temperature control circuitry. The design of these

transceivers is significantly different from that of a traditional long-distance fiber link [5.5]. The receivers for these interconnects are typically gain rather than noise limited [5.1, 5.5] and the gain and electrical power consumption are traded-off for optical power. Various models to determine the optical power requirements of gain-limited receivers have been proposed (see for example [5.2]). VLSI Transmitter models have also been investigated [5.6]. However, no interconnect model based on VLSI transceivers [5.5] predicts the optical and electrical power consumption under varying bit error and bit rates. The model presented in this chapter estimates the optical and electrical power consumption for a given bit error rate (BER) that defines an "error-free" operation, and bit rate.

5.1 Model of the Optical Link

The interconnect consists of an array of receivers, an array of transmitters and optics to connect them point-to-point. The model takes into account the following link performance measures:

- Sensitivity (optical power required to overcome noise and process non-uniformities to achieve a given bit error rate or BER)
- Operating and maximum bit rate
- Link delay
- Electrical power consumption

Receiver:

The receiver consists of an analog front-end that converts the input optical power into a voltage. The front-end is followed by a thresholder or a decision circuit, and a multi-stage amplifier to obtain a digital output (rail-to-rail). The receiver model is shown in Figure 5.1. The receiver optical input can be single or dual-rail. The front-end can be an amplifier without feedback or a transimpedance amplifier (TIA). Receivers based on comparators such as sense amplifiers are not considered here. Refer to Chapter 4 for a detailed discussion of such receivers. The following design parameters are taken in consideration by the model:

S: responsivity of the photodetector(s)

R_f feedback or input load resistance

C: input capacitance of receiver

A_{vTia}: open-loop gain of front-end analog amplifier

δV_{sens}: thresholder sensitivity

A_v: gain of post-amplifier

V_{dd}: power supply voltage

σ: standard deviation of the parameter

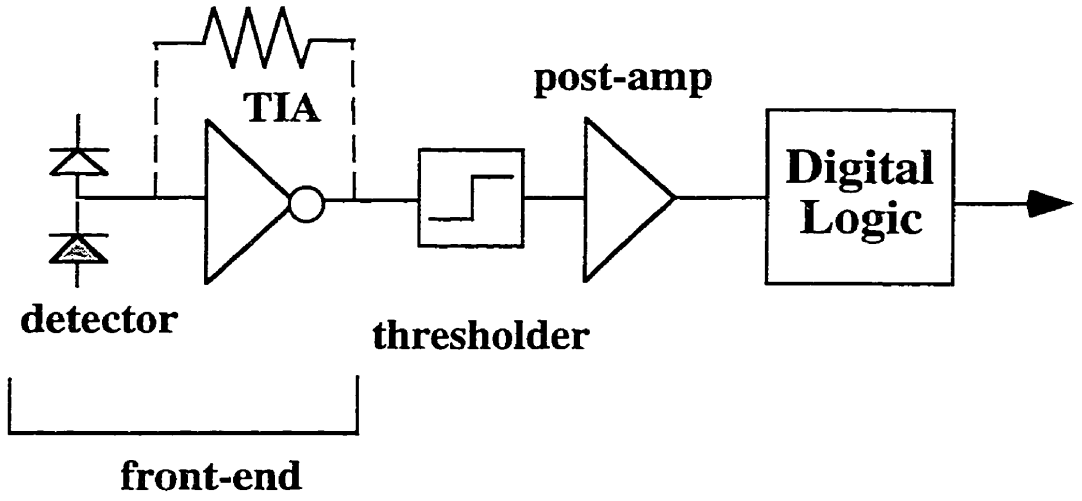


Figure 5.1: The VLSI receiver

Transmitter:

The transmitter consists of a modulator(s) and a driver. A constant beam of power P_0 is incident on the modulator. The modulator has a finite contrast ratio C_R and it is assumed to be the maximum contrast ratio of the devices [5.7]. The transmitter is shown in Figure 5.2. Refer to section 4.8 for a complete discussion of modulator drivers. The optical power attenuation from transmitter to receiver is modeled with an attenuation factor α.

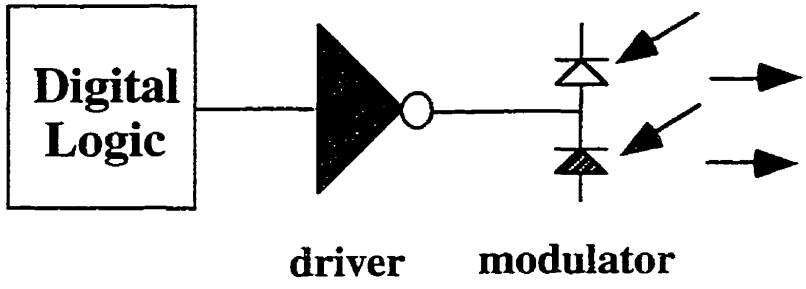


Figure 5.2: The VLSI transmitter

5.1.1 Sensitivity

The receiver sensitivity is defined as the minimum optical power necessary to achieve a given bit error rate (BER). Received bits have a finite probability of error caused by a statistical deviation in the difference between the signal levels at the output of the front-end, and the decision threshold set by the thresholder (see Figure 5.1). This statistical deviation is caused by noise (on the signal), and by process variations, σ. The process variations produce a statistical variation in the threshold and in the output signal levels of the front-end. The statistical deviation may be produced from run to run, and across a chip or wafer. Other factors that lead to a statistical deviation include cross-talk between adjacent receivers, power supply noise [5.8] and optical noise (from the lasers supplying the read beams to the modulators).

The effective signal needed at the input of the thresholder is:

$$\delta V_{eff} = (V_0 - \sigma_{V0}) - (V_1 + \sigma_{V1}) \tag{5. 1}$$

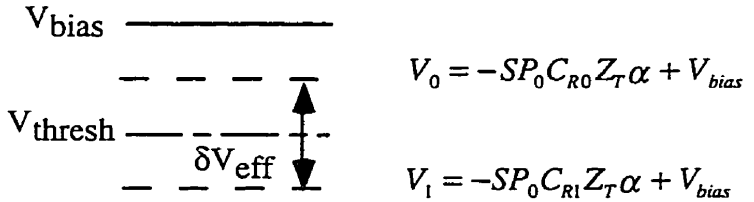
where V_1 is the output voltage associated with 'bright' beam and V_0 is associated with a 'dim' beam. An inversion usually occurs at the front-end (see below). The difference in Equation (5. 1) should be

$$\delta V_{eff} \geq 2QZ_T\sqrt{\langle i_n^2 \rangle} + \delta V_{sens} + 2\sigma_{V_{thresh}} \tag{5. 2}$$

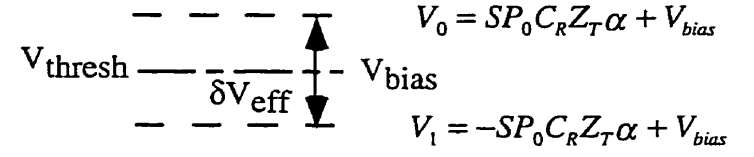
in order to achieve a bit error rate (assuming a Gaussian statistics) of

$$BER = \frac{1}{\sqrt{2\pi}}\int_Q^\infty \exp(-x^2/2)dx$$
$$= \frac{1}{2}erfc(\frac{Q}{\sqrt{2}}) \sim \frac{1}{\sqrt{2\pi}}\frac{e^{-(Q^2/2)}}{Q} \tag{5. 3}$$

where $Q = \frac{V_{thresh} - V_{0,1}}{\sigma_{0,1}}$. $V_{0,1}$ are the expected value of received signals for a digital 0 and a digital 1, and δV_{sens} is the threshold sensitivity. σ is the standard deviation of the quantity subscripted due to process variation, and $\langle i_n^2 \rangle^{1/2}$ is the rms value of noise referred to the output of the front-end.



(a)



(b)

Figure 5.3: Analog signal levels (a) for a single and (b) a dual-rail receiver.

The TIA front-end is considered here. The signal levels at the output of the front-end are shown in Figure 5.3 for (a) single and (b) dual rail inputs. The signal levels for the single-rail front-end are:

$$V_1 = -SP_{opt,1}Z_T + V_{bias}$$

$$V_0 = -SP_{opt,0}Z_T + V_{bias} \tag{5. 4}$$

where S the photodetector responsivity, $P_{opt,1}$ and $P_{opt,0}$ ($P_{opt,1}>P_{opt,0}>0$) are the associated optical power levels coupled into the detector of the receiver, $Z_T = R_f\left(\frac{A_{vTia}}{1+A_{vTia}}\right)$ is the DC transimpedance gain (R_f is the feedback resistance and A_{vTia} is the open-loop gain of the TIA- see Equation (4. 12)), and V_{bias} is the bias or reference voltage. For the transmitter shown in Figure 5.2, the optical power levels are $P_{opt,0} = P_0C_{R0}\alpha$ and $P_{opt,1} = P_0C_{R1}\alpha$ for a single-rail receiver, or $P_{opt,0} = -P_0C_R\alpha$ and $P_{opt,1} = +P_0C_R\alpha$ for a dual-rail receiver, where P_0 is the probe beam power, C_{Ri} is the associated reflectivity of the modulator, $C_R=C_{R1}-C_{R0}>0$ is the difference in reflectivity of the modulator, and α is the attenuation of the link. The levels for the dual-rail front-end are self-thresholded (see section 4.7), and they are shown in Figure 5.3b. The standard deviation, σ for the voltage level i, i=0,1 due to process variations are given by [5.3]

$$\sigma_{Vi} = SP_0C_{Ri}Z_T\alpha\left(\left(\frac{\sigma_S}{S}\right)^2 + \left(\frac{\sigma_{P0}}{P_0}\right)^2 + \left(\frac{\sigma_{CRi}}{C_{Ri}}\right)^2 + \left(\frac{\sigma_{ZT}}{Z_T}\right)^2 + \left(\frac{\sigma_\alpha}{\alpha}\right)^2\right)^{1/2} \tag{5. 5}$$

assuming that each quantity has a Gaussian distribution. From Equations (5. 1), (5. 4) and (5. 5) the voltage swing at the input of the thresholder is therefore

$$\delta V_{eff} = \theta S P_o Z_T C_R \alpha - \sigma_{V_0} - \sigma_{V_1}$$
$$= S Z_T \left[\left(P_{opt,1} - P_{opt,0}\right) - \left(P_{opt,1} + P_{opt,0}\right) \left(\left(\frac{\sigma_S}{S}\right)^2 + \left(\frac{\sigma_{P0}}{P_0}\right)^2 + \left(\frac{\sigma_{CRi}}{C_{Ri}}\right)^2 + \left(\frac{\sigma_{ZT}}{Z_T}\right)^2 + \left(\frac{\sigma_\alpha}{\alpha}\right)^2 \right)^{1/2} \right]$$

(5. 6)

where θ=1 or 2 for a single or dual-rail link. The BER is improved by a factor of two for a dual-rail scheme. The reason for that comes from the push-pull configuration. The effective input swing to the TIA is bipolar and its magnitude is doubled for a fixed contrast ratio. Furthermore this scheme increases the dynamic range since the difference in rather than the absolute power at each detector is important. The drawbacks include that an additional detector and bias line are required.

After thresholding, δV_{eff} is amplified by the gain A_v of the post-amp (see Figure 5.1). It is assumed that the probability of error in the post-amp stages is negligible compared to that in the front-end. Errors are more likely to occur before the amplification of the signal. Therefore only the front-end noise and process non-uniformity are considered for calculating the sensitivity. The minimum optical power $\Delta P_{opt} = P_{opt,1} - P_{opt,0}$ required to obtain a full digital swing, ΔV_{dd} at the output is such that:

$$\left(A_v Z_T\right) S \Delta P_{opt} = \Delta V_{dd}$$

(5. 7)

The output voltage is typically limited by the gain, $(A_v Z_T)$ and not by noise. The gain limitation resides in the simplicity of the receiver that is generally used in large spatial bandwidth systems. The optical power, ΔP_{opt} has been assumed lower. Some authors have used ΔP_{opt} as the definition for sensitivity, and have neglected the BER dependence on input optical power [5.2].

5.1.2 Bit rate

Increasing the gain increases the sensitivity but reduces the receiver front-end bandwidth due to a fixed gain-bandwidth product in most designs. Neglecting parasitic feedback capacitance, the bandwidth is given by (see Equation (4. 12))

$$f_{3db} \sim \frac{A_{vTia}+1}{2\pi R_f C} \tag{5. 8}$$

where R_fC is the time constant associated with the dominant pole of the front-end. On the other hand, the transimpedance gain, Z_T is directly proportional to R_f. In a typical front-end design, the bandwidth and the gain are traded off [5.2].

The *operating* bit rate is defined by:

$$B = \frac{\xi}{\left(t_r + t_f\right)} \tag{5. 9}$$

t_r and t_f are the rise and fall times and they are taken to be approximately equal for simplicity. ξ is the allowed percentage of the bit period that the rise and fall time take without significant signal degradation [5.9]. The rise and fall times are inversely proportional to the 3 dB bandwidth. For a receiver front-end with a linear transfer function

$$t_{rf-e} = \frac{K}{f_{3dB}} \tag{5. 10}$$

where K~0.35 for a single-pole transfer function. Substituting Equation (5. 10) into Equation (5. 9) defines the *maximum* possible bit rate of the receiver.

The total rise time found at the output of the receiver is given by:

$$t_r = \sqrt{t_{rf-e}^2 + \sum_i t_{rp-ai}^2}$$

(5. 11)

t_{rf-e} and t_{rp-ai} are the risetime for the front-end (given in (5. 10)), and for the following stages (post-amp). The permissible bit rate is usually lower than the *maximum* one because of the non-zero response time associated with the post-amp. When the edge times incurred at the transmitter, t_{TX} are included in Equation (5. 11), the delay in the link is:

$$\Delta t = \sqrt{t_{rf-e}^2 + \sum_i t_{rp-ai}^2 + t_{TX}^2} + t_{flt}$$

(5. 12)

where t_{flt} is the time of flight.

The bandwidth and the edge times are determined by the receiver circuit parameters. The edge times are normally independent of the input amplitude or levels. However they are dependent on inputs under two distinct circumstances: 1) when the input controls the resistance in the charging and discharging paths (e.g. FET) of the output node (voltage-mode circuits such as an inverter) and 2) when a positive input current I is charging (and a negative current is discharging) a purely capacitive load. These situations can be modelled with a capacitance C that is (dis)charged to a voltage ΔV. The risetime is then $t_r = \frac{C\Delta V}{I}$.

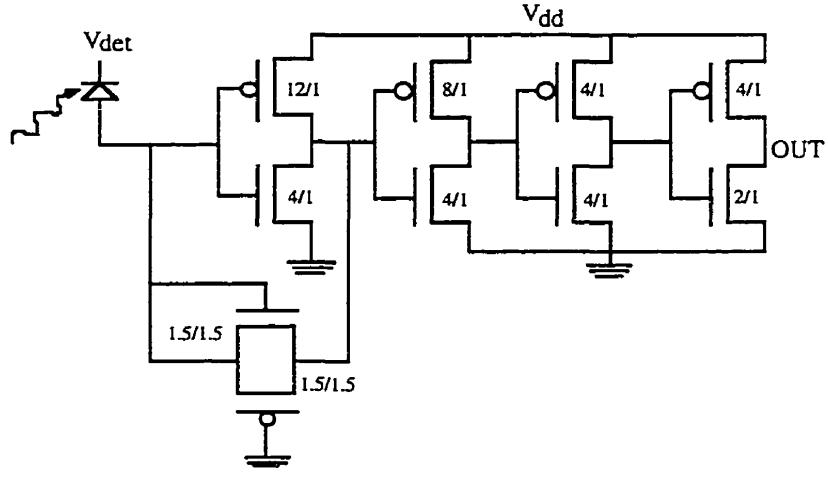


Figure 5.4: CMOS TIA-based receiver

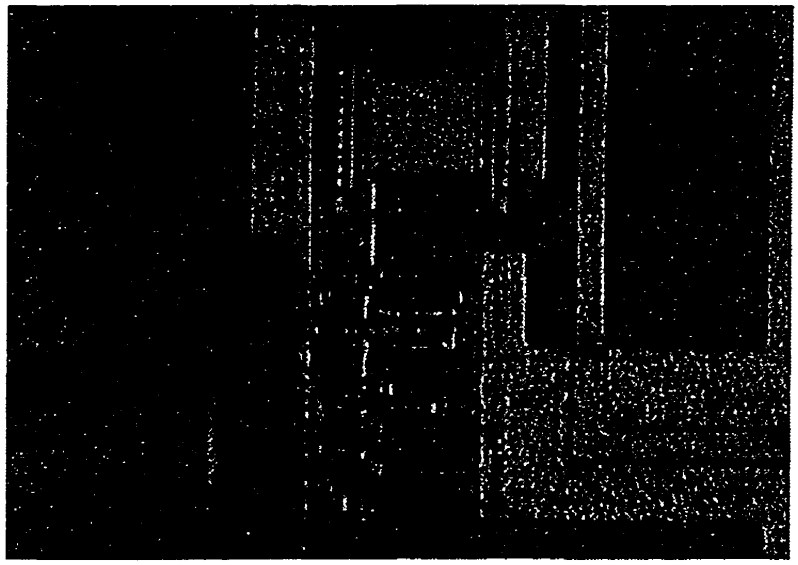


Figure 5.5: An example of fabricated TIA with integrated detector (top).

An example of each situation is found in 1) CMOS TIA receiver [5.10] (see Chapter 4), and 2) FET-SEED diode-clamped receiver [5.11] (see Chapter 2). The CMOS TIA is shown in Figure 5.4, and a photomicrograph of a fabricated TIA is shown in Figure 5.5. The fabricated TIA is less than 50μmX50μm. The inverters act as the thresholder and the post-amplifier. Although the edge time associated with the front-end is independent of the input levels, the edge time associated with the ith inverter stage, t_{rp-ai} in Equation (5. 11) and (5. 12) depends on their input level V_1 and V_0. The edge times (rise and fall) for those stages are [5.12]

$$t_{rp-ai} \sim (2\pi K)\frac{C_{out}}{\beta_p\left(V_{dd} - V_1 - \left|V_{Tp}\right|\right)} \text{ and } t_{fp-ai} \sim (2\pi K)\frac{C_{out}}{\beta_n\left(V_0 - V_{Tn}\right)} \tag{5. 13}$$

An increase in P_0 would increase the swing δV_{eff} (refer to Equations (5. 1) and (5. 6)) and consequently reduce the edge times associated with the post-amp. Thus the receiver would be able to be operated at a bit rate closer to the *maximum* one (see Equation (5. 9)).

The FET-SEED diode-clamp receiver shown in Figure 2.6 is now considered. It has a high-impedance integrating front-end (see Chapter 2). The photocurrent charges the input capacitance to a voltage high enough to switch the input FET. The edge time is

proportional to the input photocurrent level. The voltage has to be clamped to prevent the voltage from rising too high or falling too low in the case of a string of '1's or '0's.

5.1.3 Power Consumption

The number of gain stages, m and hence the receiver power consumption (and area) can be traded-off for sensitivity. Power consumption is also proportional to the bit rate. The total power for one link, P_{link} is the sum of the power consumed by the receiver, the transmitter and the in-situ logic i.e. $P_{link} = P_{RX} + P_{TX} + P_{\substack{in-situ \\ logic}}$. The power dissipation of the receiver, P_{RX} is the sum of power dissipated in the analog amplifier front-end and the following stages.

The power in a CMOS TIA can be expressed as follows:

$$P_{RX} = nV_{bias}I_{bias} + \sum_{i}^{m} V_i I_i + kC_g V_{dd}^2 B \tag{5. 14}$$

The first term is the static power consumed in the feedforward amplifier, and is proportional to V_{bias}^3 (n is the number of stages in the feedback-loop[5.13]). The second term accounts for the static power consumed in the following stages (m being their number), and the third term describes the dynamic switching power of the digital receiver.

The power consumed by the transmitter is:

$$P_{TX} = \frac{SP_o V_{\text{mod}}}{2} + P_{\substack{driver \\ static}} + kC_{\text{mod}}\Delta V_{CR}^2 B \tag{5. 15}$$

The first term represents the power dissipated in the modulators due to a constant beam with power P_o incident photocurrent. The second term accounts for the static power dissipated in the driver and the final term models the switching power (dynamic). The dynamic power in the transmitter is more important than in the receiver and accounts for the main part of the total consumption (see Section 4.8). Since the optical power is externally

supplied, the electrical power consumption is independent (if the first term in Equation (5. 15) is neglected) of the output optical power for modulator-based transmitters. For an interconnect based on an emitter technology, the total power consumption depends the output optical power and sensitivity of the receiver. The on-chip driving power consumption increases due to higher driving currents.

The power consumption for the in-situ digital logic is taken into account by the model. It is $P_{\substack{in-situ \\ logic}} = kn_s C_g V_{dd}^2 B$. n_s is the 'smartness' parameter. 'Smartness' is the number of gates or the amount of processing required by one link. k is the activity factor. Intelligent receivers and transmitters have been termed 'smart pixels'. The logic performs processing functions such as address recognition, and multiplexing and demultiplexing data.

5.2 Array of Transceivers

The performance of one link has been modelled in the previous section. This section discusses a few issues related to the design of the array, namely aggregate bandwidth and on-chip channel density, skew and switching noise.

The density of electronics is $D_e = \frac{n_s}{A} \leq D_{e/\max}$ where $D_{e/max}$ is the maximum density. The density of the electronic can be limited in two ways: 1) heat removal limited [5.14], or 2) wire-limited (area constrained) [5.14]. For example, a smart pixel requiring in addition to optical I/Os, a large number of electrical I/Os and control lines would be wire-limited. If the chip is heat removal limited then $D_{e/\max} = \frac{W}{kC_g V_{dd}^2 B}$ where W is the heat removal capability.

The optical I/O density, D_o is usually not limited by the density of VLSI receivers and transmitters that can be packed on a chip but by the optics. Diffraction represents a limit but in practice is not reached. The placements of the detectors and modulators (or emitters) on the chip plane, and the optical system providing the array of beams need to be designed in conjunction to optimize the link density given the constraints of the optics. Figure 5.6 shows two examples of optical I/O layout: a) regular b) clustered. The optical detectors and

modulators reside right on top of electronics. The arrays of receivers and transmitters can be physically disjoint or interlaced. Typically the receivers and the transmitters are interlaced with one receiver and one transmitter per pixel.

The total optical power is limited in a system. This puts a limit on the number of link that can be interconnected. If the maximum power available is P_{TOT} then this maximum number of links is

$$N_{link/\max} = \frac{\alpha\left(\frac{C_{R1} + C_{R0}}{2}\right)P_{TOT}}{\Delta P_o} \tag{5. 16}$$

where ΔP_0 is defined by Equation (5. 7).

(a) (b)

Figure 5.6:Optical I/O layout (shaded areas) (a) regular (b) clustered array.

It is important to consider skew between each link. The skew is mainly limited by process variations at the receiver and transmitter. Another source of skew comes from the differential on-chip metal interconnect lengths from the receivers and transmitters to and from the edge of the chip. The edge times of the front-end, the post-amp, and the transmitter in Equation (5. 12) are strongly dependent on the process or circuit parameters. This is so because of the simplicity of the receiver and transmitter design as small areas are required. Circuit design have been used to reduce the effect of process variations without too much area and power consumption overhead [5.13]. With the parameters in Table 5.1, it is found that the delays associated with the transmitter and the receiver account for about

half of the total link delay. On the other hand, the time of flight is directly proportional to the distance. In a backplane this distance is typically 30 cm which makes the time of flight about 1ns long.

Since the analog and the digital section coexist on the same chip (all transceivers share analog and digital bias lines), switching noise may become important for large arrays. Solutions to reduce this effect include the use of differential amplifiers [5.8, 5.15, 5.16] decoupling of bias lines and optical powered smart pixels [5.17].

5.3 Results

The receiver is shown in Figure 5.4. The transmitter use modulators with 3:1 contrast ratio. The reflectivities are 45% and 15%. Substituing Equation (5. 8) into (5. 10), and (5. 10) into (5. 9), the *maximum* bit rate is calculated to be 550Mb/s. The DC switching optical power is found with Equation (5. 7) to be 3.4μW (-24.7dBm). This level constitutes the minimum input to obtain a full digital output swing. An additional amount of optical power is required to overcome noise and process variations. The optical power required to overcome noise and process variations to achieve a given BER is calculated using Equations (5. 2), (5. 3) and (5. 6) for that maximum bit rate. The edge times required to run at a given bit rate are found with Equation (5. 9). With Equations (5. 10) and (5. 11), the edge times associated with the post-amp are calculated. The input optical power to obtain these edge times are calculated with Equations (5. 4) and (5. 13). The results of this calculation are presented in Figure 5.7. Calculations verified with simulations, show that a 2μW and 3μW reduction in ΔP_{opt} slow the bit rate from the *maximum* to 375Mb/s and 250 Mb/s, respectively. These reductions are the same for any given BER, and indicates a slower post-amp edge. For a BER=10^{-9}, the sensitivity is -19.6 dBm at maximum speed i.e. 550 Mb/s. At a bit rate of 375 Mb/s, the sensitivity is -20.6 dBm. At a bit rate of 250 Mb/s, the sensitivity if -21.1 dBm. These compare favorably with the measured sensitivities [5.10], hence validating the model.

The power consumption is calculated with Equation (5. 14). The input gate capacitance is estimated at 10fF and C_g=3*10fF since there are three stages (m=3 and n=1). k=1 for NRZ signalling. A static power of 4.5mW is estimated. A dynamic power of 400

μW, 300μW, and 200μW are calculated for 550 Mb/s, 375 Mb/s, and 275 Mb/s operation. Therefore the total power is 4.9 mW at 550 Mb/s, 4.8 mW at 375 Mb/s, and 4.7mW at 250 Mb/s. These values agree with the measured power consumption [5.10].

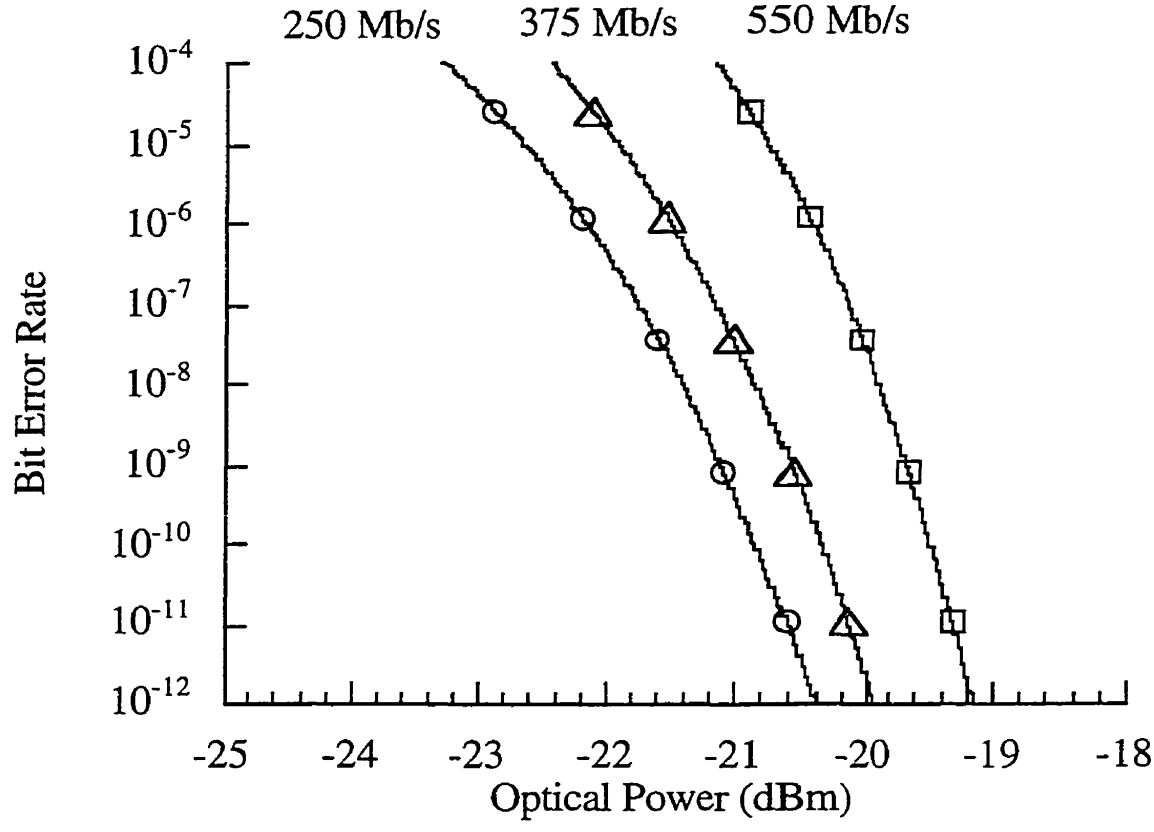
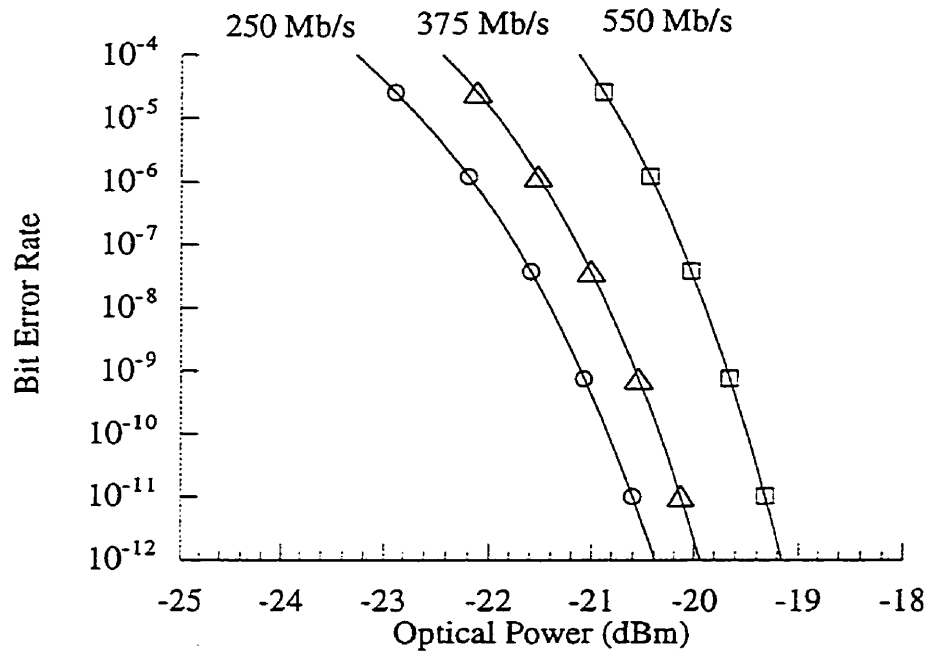


Figure 5.7: BER versus optical power for three bit rates.


250 Mb/s
375 Mb/s
550 Mb/s
Bit Error Rate
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
-25
-24
-23
-22
-21
-20
-19
-18
Optical Power (dBm)

Parameter	Value
A_{vTia} Open-loop gain for the feedforward amplifier of the TIA	5
R_f Feedback Resistance of TIA	28619Ω
C Input capacitance of receiver front-end	52fF [5.18]
ξ Percentage of the bit period that the edge times take	0.6 [5.9]
A_v Gain of post-amp	125 (3 stages each with gain=5)
S Responsivity of the detector	0.5A/W
ΔV_{dd} Power supply volltage	5V
C_{R1} Reflectivity for a 'high' beam	0.45
C_{R0} Reflectivity for a 'low' beam	0.15
α Optical link attenuation	1
σ(process) Standard deviation of the process	1.8%
$\sigma_{Vthresh}$ Standard deciation of the threshold voltage	10mV
δV_{sens} Sensitivity of the thresholder	20mV
$<i_n^2>$ Noise in the front-end	10^{-13} A^2

Table 5.1: Values of the parameters.

5.4 Conclusions

A model for optical interconnect based on VLSI-optoelectronic transceivers was proposed. The model can be used to estimate the optical power required by the interconnect for any BER or to ensure error-free operation. Circuit noise and process variations are taken into account in the model. It also predicts its power consumption, and the interconnect delay. Table 5.2 summarize the model predictions and compares them with measurements.

There is a general trade-off between optical and electrical power consumption in a modulator-based interconnect. This is due to the fact that more sensitive receivers require larger gain that consumes more electrical power. On the transmitter side, the power consumption is only weakly dependent on the output optical power. For an emitter-based interconnect, a larger optical power entails a larger power consumption at the transmitter so that the total power consumption of the interconnect is not necessarily reduced with the use of less sensitive receivers.

Bit Rate (Mb/s)	Measured Sensitivity (dBm) [5.10]	Predicted Sensitivity (dBm)	Receiver Power Dissipation (mW) [5.10]	Predicted Receiver Dissipation (mW)
250	-21.5	-21.1	4.7	4.7
375	-20.9	-20.6	4.8	4.8
550	-19.4	-19.6	5	4.9

Table 5.2: Comparison between model and measured sensitivities (BER=10^{-9}) and power consumption.

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Chapter 6: Backplane Demonstrators

The work presented in this chapter was undertaken under the supervision of Profs. D.V. Plant and H.S. Hinton during the period spanning from the spring of 1994 to the spring of 1995. The author was working in a team that was building backplane systems [6.1, 6.2]. His main contribution resides in the design and optoelectronic packaging of the transceiver arrays used in these systems. As pointed out in the introduction of this thesis, optical interconnections and 2-D optoelectronic arrays may find an important application at the backplane level [6.3, 6.4] where there is an electronic bottleneck at the printed circuit board (PCB) to backplane interface [6.5]. In this chapter, three backplane demonstrators are described. The demonstrator approach is used to identify the critical research issues in photonic backplane systems. Three main fields of expertise are called upon when building a photonic backplane: 1) 2-D optoelectronic technology and circuit design, 2) optics and optomechanics, and 3) packaging and system assembly and integration. This chapter examines how the three fields work together in implementing an optical backplane as depicted conceptually in Figure 6.1.

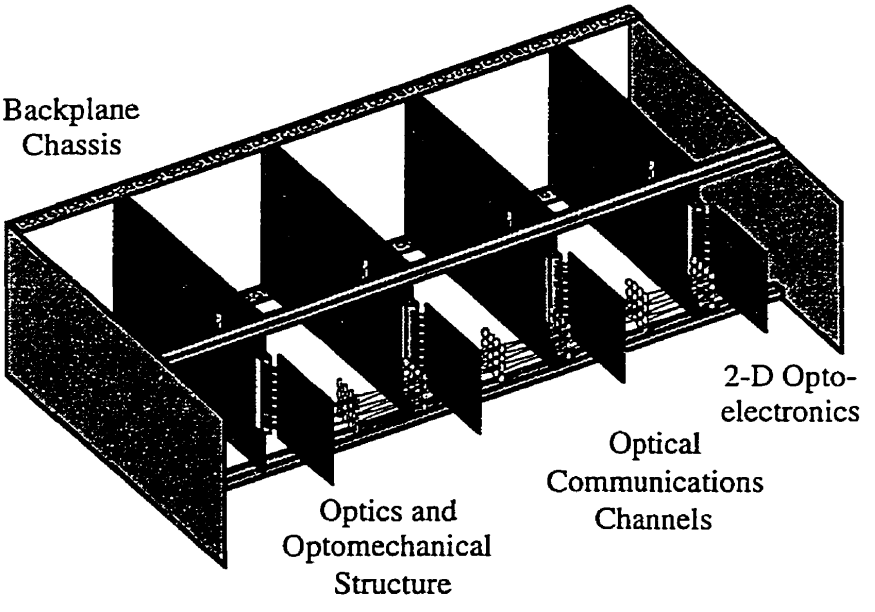


Figure 6.1: Conceptual Optical Backplane

The function of the backplane is to communicate data between PCBs. The photonic backplane exploits VLSI 2-D optoelectronics and free-space optics to achieve the high spatial bandwidth. The backplane consists of 2-D arrays of VLSI optoelectronic

transceivers interconnected through free-space optics. A VLSI optoelectronic transceiver acts as an interface between the optical data (in an analog form) and the digital logic on the VLSI chip and/or on the board. The design of a transceiver is discussed in Chapters 2 to 4. Functionalities such as header processing and address recognition can be added to each transceiver in the array. The added processing electronics produces 'intelligent' optical input and output [6.6]. One important goal in building those demonstrators is to test these 'intelligent' transceiver arrays, and see how well they behave in a system environment. The CMOS/SEED system described below implements a portion of the hyperplane architecture [6.7]. This architecture uses 'intelligent' I/O to direct traffic between a multi-boards backplane.

Another important goal is in developing the optomechanics and packaging of photonic backplanes, more particularily of free-space systems. This is to provide a good long-term stability and ease of alignment. Techniques in designing the receiver and the array discussed in Chapter 4 may help the alignability and the tolerance of the system, but rugged mechanical support is still needed. The approaches to all the demonstrators have been to use:

- thermally and mechanically stable optomechanics.
- modular design for automatic manufacturing.
- passive alignment with no adjustments once the system is built.
- removable daughter boards.
- an integration of optics into a standard VME [6.8] backplane chassis.

The concept of the kinematic daughter board is illustrated in Figure 6.1. The daughter board is a small board on which the optoelectronic arrays are mounted. It is mechanically decoupled from the rest of the board (the mother board) to ease alignment. A high-speed connector is used between the daughter and the mother board. This optomechanical approach has made the system alignment much easier to achieve.

The third component of the backplane is the optics. The challenge in the design of the optics resides in providing a scaleable interconnect between multiple boards. The efficiency of the links is an important design issue. Furthermore, the optics may provide diagnostic tools to aid alignment and assembly of the system. In the next section, a FET-SEED-based demonstrator is described. In section 6.2 the MSM/VCSEL backplane is discussed. Section 6.3 presents the hybrid CMOS system, and the final section summarizes and give conclusions.

6.1 FET-SEED based demonstrator backplane

A uni-directional PCB-to-PCB optical interconnection is designed and constructed. The demonstrator is based on a 4X4 FET-SEED receiver and a transmitter array, PCB level optoelectronic packaging, conventional optics or diffractive microoptics, and baseplate optomechanics. The design, packaging, and characterization of the transceiver arrays are described in Chapter 2. The board-to-board optical interconnection is achieved using a two-sided PCB approach. The optical system establishes the communication between the PCBs and it is implemented in two ways: 1) with conventional optics and 2) with diffractive microoptics. The conventional optical system is shown in Figure 6.2 (all numbers in mm; RBS=Risley Beam Steerers and BPG=Binary Phase Grating). The rectangle at the top labelled OPS in Figure 6.2 is the optical power supply. It supplies an 8X4 array of vertically polarized light spots to the modulators on the right-handside board. The OPS is similar to that of the microoptic based interconnect and is described below. A conventional optical system relays the modulated beam from the modulator array to the receiver array on the left-handside PCB. Although the conventional optical system is easier to align, it is not as compact as the microoptic-based interconnect.

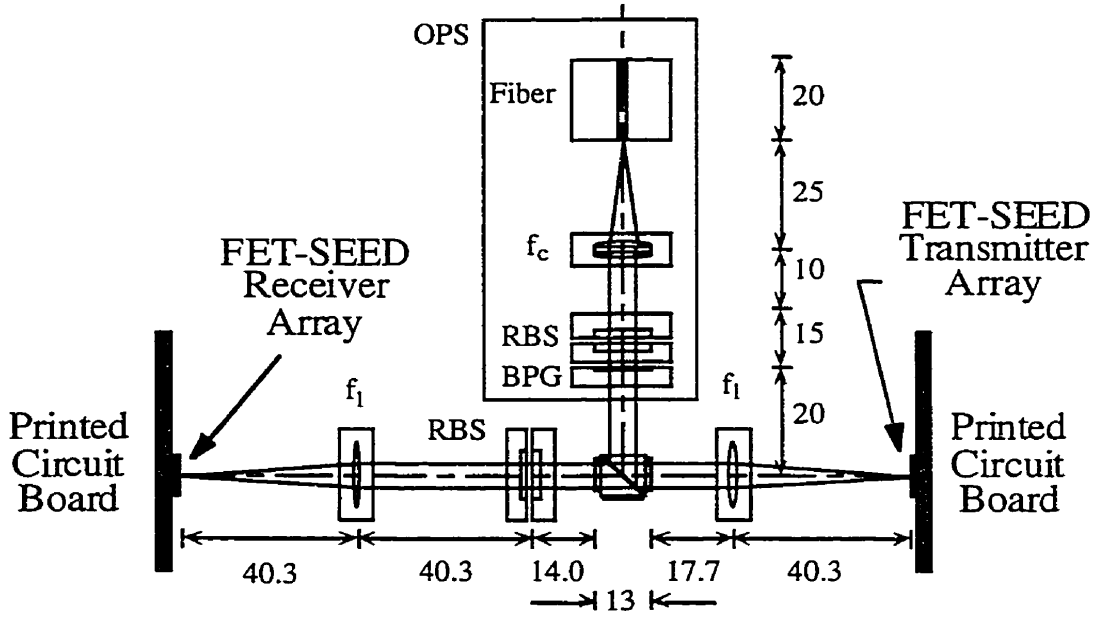


Figure 6.2: Conventional Optical System Layout

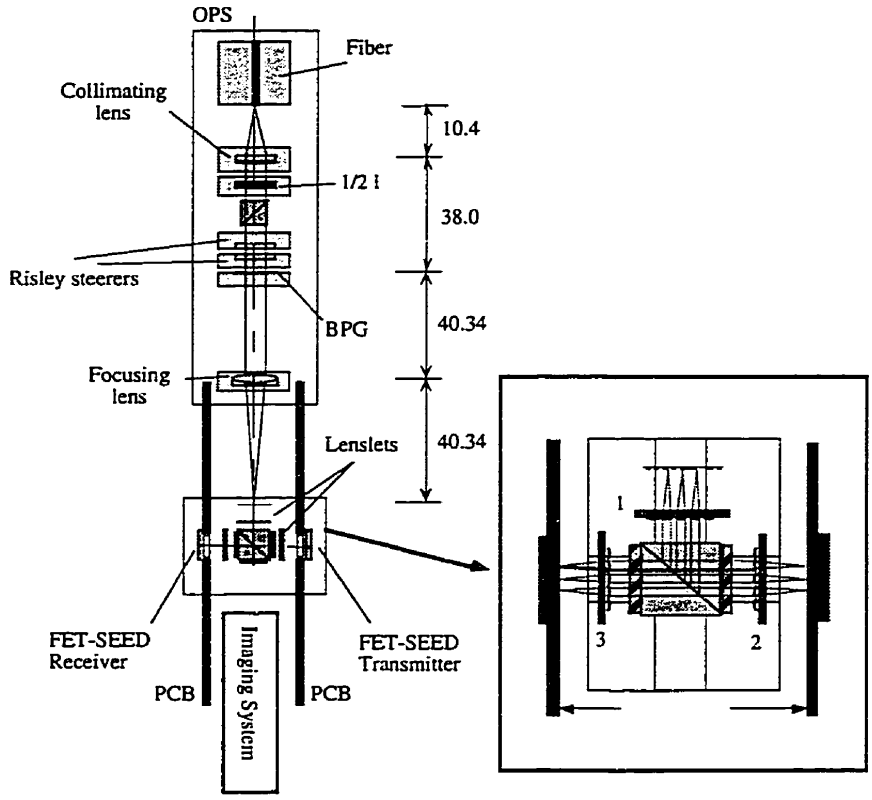


Figure 6.3: Microoptic-based Interconnect

Microoptic lens arrays are used to implement the board-to-board relay to produce a system that is scalable and to obtain a board spacing that is comparable to current electronic systems [6.5]. Figure 6.3 shows a schematic of the optical system (all numbers in mm). The OPS is shown in the rectangle. The optical power is delivered from a 850 nm single frequency, argon ion pumped Ti:sapphire laser coupled into single mode, polarization maintaining fiber and collimated with a 10 mm focal length lens at the fiber output. The system spot array generator consisted of a binary phase grating and a 40.34 mm achromat lens to produce the required 32 spot pattern. The efficiency of the binary phase grating is measured to be 67%. Fine adjustment of the beam positioning is accomplished using Risley beam steerers packaged with ball bearings for ease of rotation. Two 4f relays are established using three 6.5mm focal length, 8 level diffractive microlens, and a 5 mm polarizing beam splitter as shown in the Figure 6.3 insert. The first relay is setup between the power plane and the transmitter array with microlenses labelled 1 and 2, and the second relay with microlenses 2 and 3. The microlens have a measured throughput efficiency of 90%. The total optical loss of the system is measured to be 20.7% from the fiber output to the transmitter array, and 70.5% from the transmitter array to the receiver array. The

system is typically operated with 0.5 mW per diode (1.0 mW per dual-rail channel) on the transmitter array, and an average of 0.35 per diode on the receiver array.

The optomechanical system is constructed using a slotted magnesium baseplate and pre-aligned optical components mounted into one inch holders. The components are held in place by a stacked magnet/steel bar combination which allowed for tailoring the strength of the retaining force. The PCBs are mounted onto five axis positioning stages secured to the baseplate. The optical system is designed and operated with 10 micron mechanical tolerancing. The system demonstrated excellent long term stability, and remained aligned over several days. Figure 6.4 shows a photograph of the demonstrator. The transmitter board is again on the right and the receiver board on the left of the photograph. The imaging system has been removed and placed on the right hand of the backplane (top right in the photo).

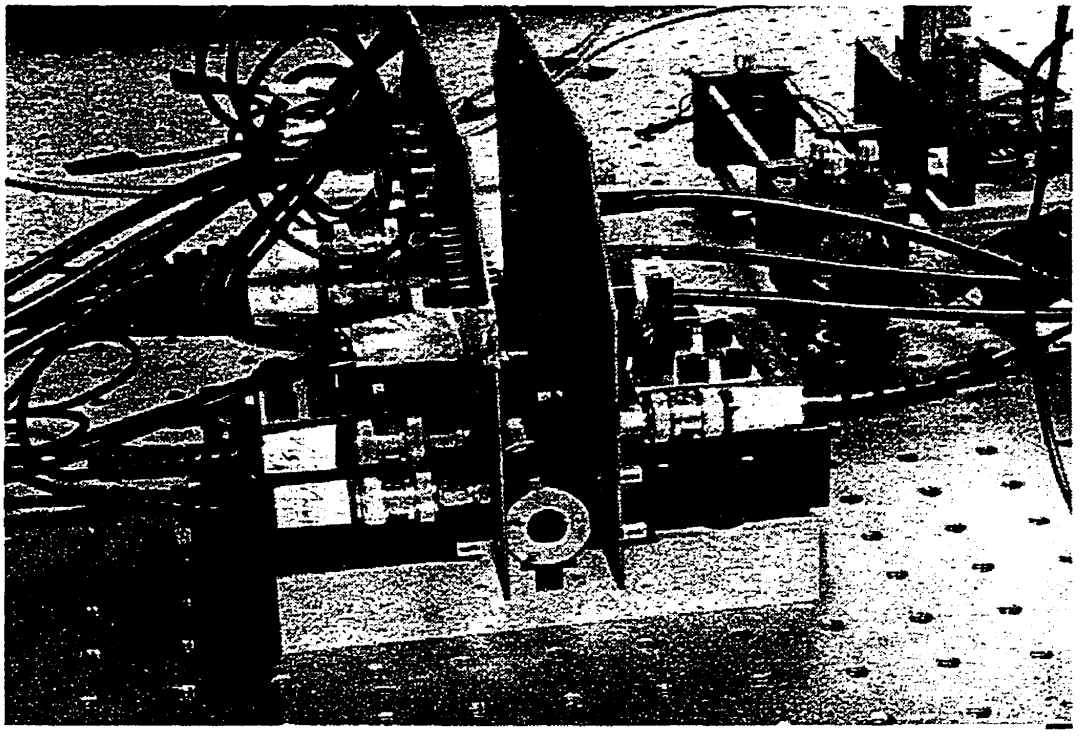
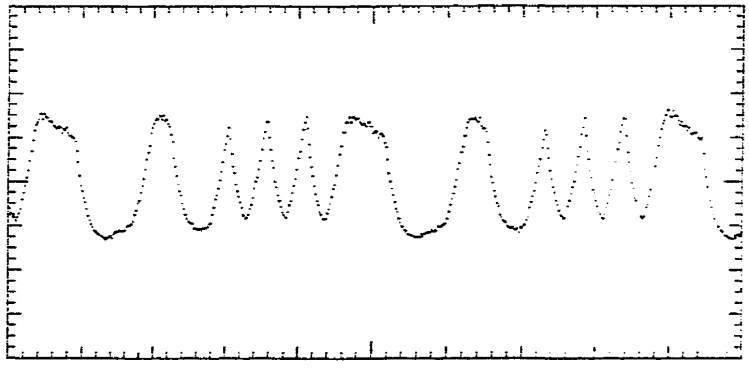


Figure 6.4: Photomicrograph of the FET-SEED based backplane

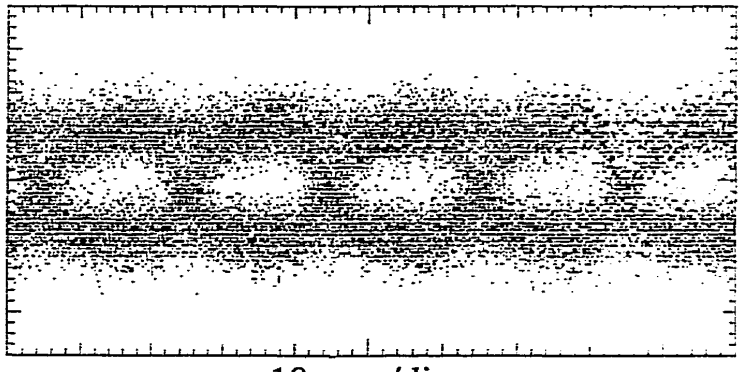
The system is operated in two configurations. Based on the 600 μm center-to-center spacing of the lenslets arrays, in the first configuration the 4 corners of the transmitter/receiver smart pixel arrays are interconnected optically. Figure 6.5 shows the results of transmitting data from board to board over one of these micro-optical channels.

In this configuration, each lenslet supported one dual rail optical channel. The system is operated in this configuration at data rates up to 75 Mb/s on an individual channel. Based on the received optical power, and the bias voltages of the diode clamped receiver circuit, the switching energy is calculated to be 50 femtojoule/bit. This was the first time a single lenslet based optical interconnect was used to support differential optical signals. Multiple channel operation was also investigated, however the data rates were somewhat slower owing to cross talk on the FET-SEED circuit electronics. The crosstalk appeared in the form of electrical pick-up on adjacent trace lines most likely due to non-optimum circuit metalization. However no measurable significant optical crosstalk in the system is detected.



75 nsec/div

(a)



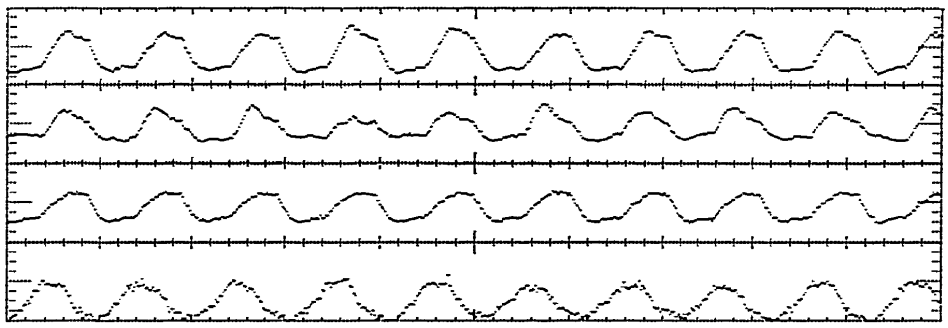
10 nsec/div

(b)

Figure 6.5: 16 bit patterns and a PRBS at 50Mb/s

In the second configuration, a single lenslet (600 μm in diameter) is used to support four dual rail optical channels, a total of eight optical channels, in a cluster pixel configuration. This is possible due to the robustness of the lenslet design. In this optical configuration, 2 X 2 transceiver subarrays are used. In particular, a 2 x 2 modulator array

(center-to-center spacing 200 μm) in the center of the 16 element array is interconnected with the center 2 x 2 sub-array on the receiver chip. Figure 6.5 shows a typical recording of the output of the system with all four channels being driven simultaneously at 25 MBits/sec. This result is significant in that it demonstrates an effective channel density of 2222 channels/cm^2, and points toward the scalability of free space interconnects at the backplane level of the interconnection hierarchy.



75 nsec/div

Figure 6.6: Cluster Pixel output at 25Mb/s

A larger number of clustered channels may be handled by the lenslet. The optimization of the connection density with the design of the lenslet has been studied [6.9] and the results of the analysis is reported in [6.10].

6.2 MSM/VCSEL based demonstrator

A system demonstrator is built based on Vertical Cavity Surface Emitting Lasers (VCSELs), Metal Semiconductor Metal (MSM) detectors, PCB level optoelectronic device packaging, a conventional optical relay, and novel barrel/PCB optomechanics. The entire system is constructed using a standard VME electrical backplane chassis [6.8] and operated at > 1.7 Gb/s of aggregate data flow. In addition to describing the component technologies developed, this section describes operational testing and characterization of the demonstrator.

Figure 6.7 is a picture of the demonstration system. The large PCBs are mechanically decoupled from a smaller board on which the optoelectronic chip is packaged. Because the requirement of connectivity into or out of the board is a fraction of the information flowing between them, a scaleable high speed flexible 50 ohm connector is chosen to connect between the two boards. The extraction and insertion of the PCB can

thus occur with a minimal impact on the alignment of the optoelectronics. This approach resulted in the concept of mother boards which resided in a conventional manner inside the VME chassis, and daughter boards which are part of the optical interconnect layer. In addition to optomechanical advantages, the daughter boards provided the first and second level packaging for the optoelectronics and their associated support electronics. The 2-dimensional device arrays used to provide the optical link between the daughter boards are VCSELs for the transmitter, and MSMs for the receiver. The light is relayed from the VCSEL plane to the MSM plane through a 4f telecentric imaging system, with external viewing capabilities.

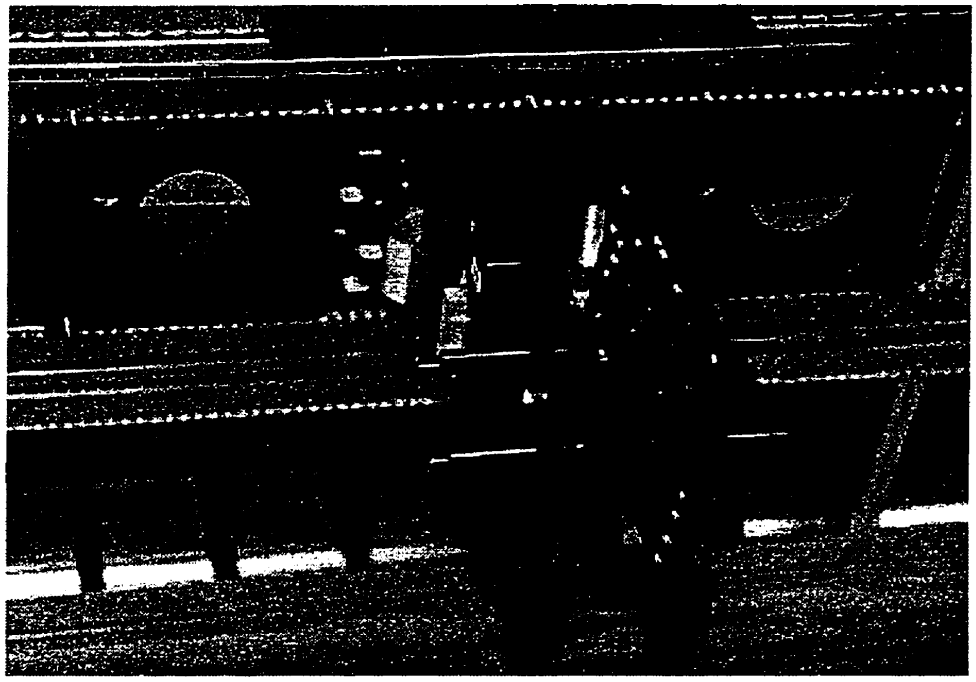


Figure 6.7: MSM/VCSEL Backplane Demonstrator

Parameter	Symbol (Unit)	Min.	Typical	Max.
Optical Output	P_{out} (mW)	1.0	-	-
Peak Wavelength	λ (nm)	835	850	865
Full Angle @ Half Maximum	θ (degree)	10.0	13.0	15.0
Pitch	125 μm x 125 μm			
Array	4 x 4 array			

Table 6.1: Optical Characteristics for PRI's VCSEL (TA = 25 °C, cw operation)

The transmitter daughterboard includes a 4x4, 850 nm VCSEL array (device pitch, 125μm) packaged in a Pin Grid Array (PGA) chip carrier. The VCSEL characteristics are shown in Table 6.1. The beam waist is specified to be from 1.189 μm to 1.853 μm (3ω is 3.566 μm to 5.558 μm). PCB level packaging of the PGA is accomplished using custom, impedance controlled, 4 layer PCBs. In addition, a TE cooler is mounted on the back of the PGA in order to allow for active cooling of the VCSEL array. This is accomplished by leaving a hole in the VCSEL daughterboard. In order to avoid the problem of slow drive electronics, each individual VCSEL is operated through a dedicated bias tee mounted on the mother board.

On the receiver daughterboard, a 4x4 MSM array (fabricated by McMaster University) is hybridly packaged in a 68 pin PGA with commercially available HP silicon MMIC transimpedance amplifier chips. The responsivity of the MSM is 0.2 A/W at 5V bias. The pitch size is designed to match that of the VCSEL. The active area of a MSM receiver is 50x50 μm. The ratio of the finger width and finger spacing inside an active window is 1:1, thus, roughly 50% optical power onto MSM is reflected by metal and a further 30% of the remaining light reflected by the GaAs. Table 6.2 summarizes the optical parameters of the MSM receivers. To minimize long leads and unwanted inductive parasitics, the transimpedance amplifier chips are mounted directly into the PGA, adjacent to the detector array chip. The output of each MSM is wire bonded to an amplifier chip. The outputs of the transimpedance amplifier chips are then wire bonded to the PGA outputs. These amplifier outputs are fed into variable gain amplifiers which are surface mounted on the receiver daughterboard and configured as limiting amplifiers to achieve ECL voltage levels. In both cases, the daughter boards are connected to the mother boards through high speed connectors.

Pitch	125 μm x 125 μm
Active window	50 μm x 50 μm
Finger width	2 μm
Finger Spacing	2 μm
Reflection from MSM	~ 80%

Table 6.2: Optical parameters for the MSM

The optical interconnect is accomplished using a 4-f telecentric imaging system which employs two inexpensive injection molded glass aspherical lenses (f = 6.24 mm).

Risley beam steerers are used for fine adjustment of the optical beams, and a 4 mm beamsplitter cube is used to provide a view port. The resulting spot radius on the MSMs is calculated to be 27 μm. The optical power throughput is 43% but since only 40% of the power is coupled into the MSM, a 17% efficiency is found.

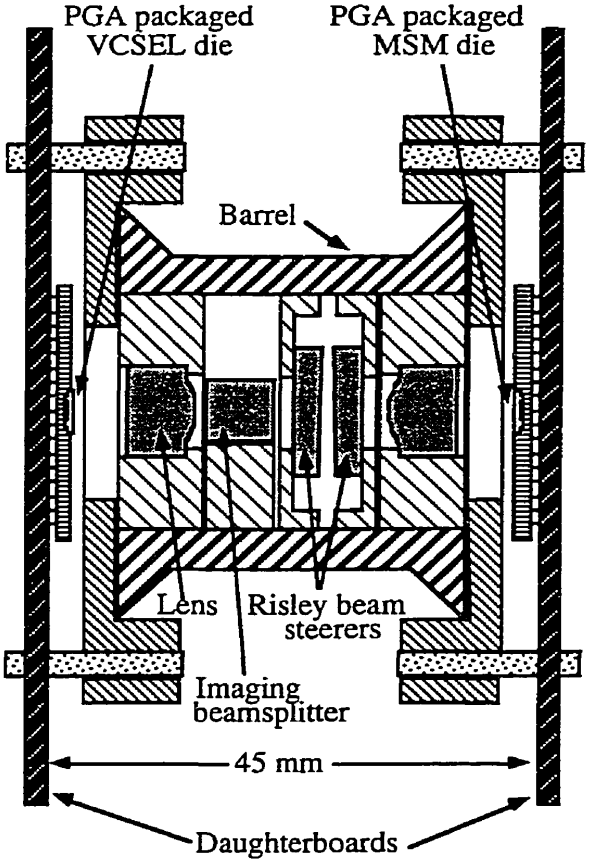


Figure 6.8: Barrel Optomechanic

Figure 6.8 shows a schematic of the optics and optomechanics. The objective of this approach is to design and build a compact, low-cost, stable, and rapidly assembled optomechanical support structure which can be integrated into an industry standard VME 6U chassis. The barrel had two 45° bevels, one on each side. These served to support the daughter board barrel adapters which acted as an interface between the daughter boards and optomechanical components. The barrel itself is fixed in position relative to the VME chassis, and the optomechanical interface permitted motion of the daughter boards relative to the barrel. The utility of a flexible connector between daughter and mother boards is key because the daughter boards are required to move independently relative to the chassis. Neither the die to package nor the package to board alignment tolerances are critical to the

alignment of the system as the daughterboard optomechanics are designed to compensate for these misalignments. During assembly, the optomechanics allow spots generated by the VCSEL array to be positioned to within 50 μm of their required location. Additional alignment is provided by the Risley steerers which have a range of 80 μm and resolution in the micron range. The physical separation between two PCBs is 28.8 mm. Finally, in addition to TE cooling the optoelectronics, two cooling fans are bolted to the VME chassis support spine as is shown in Figure 6.7. This spine also served to support the rod and barrel optomechanics; thus these fans are directly mechanically coupled to the chassis. These fans blew air directly onto the daughter boards and provided an additional heat removal mechanism. During all the operational testing described below, not only is the VME chassis freestanding but also the two cooling fans are on at all times.

The system is operated in a number of different modes. Each of the 16 channels is individually operated at data rates up to 500 Mb/s on the best channels. Figure 6.9 shows eye diagrams of six of the channels operating at 155 Mb/s. In the parallel mode of operation, the VCSEL array performance is degraded by thermal coupling between adjacent VCSELs. Only 11 channels can operate simultaneously. In this mode, these 11 channels are operated at 155 Mb/s, with < 2ns edges and high signal quality. This represents greater than 1.7 Gb/s of aggregate data flow. The stability and robustness of the system is excellent. The system remained aligned for over 21 days and showed under 2 μm of transverse (x-y) misalignment. In addition, the system was tested under mother board insertion and extraction, showing no misalignment after over 30 insertion and extraction cycles. Finally, both the introduction of mechanically coupled fans to the chassis and shock on the daughter boards show no effect on the alignment of the system.

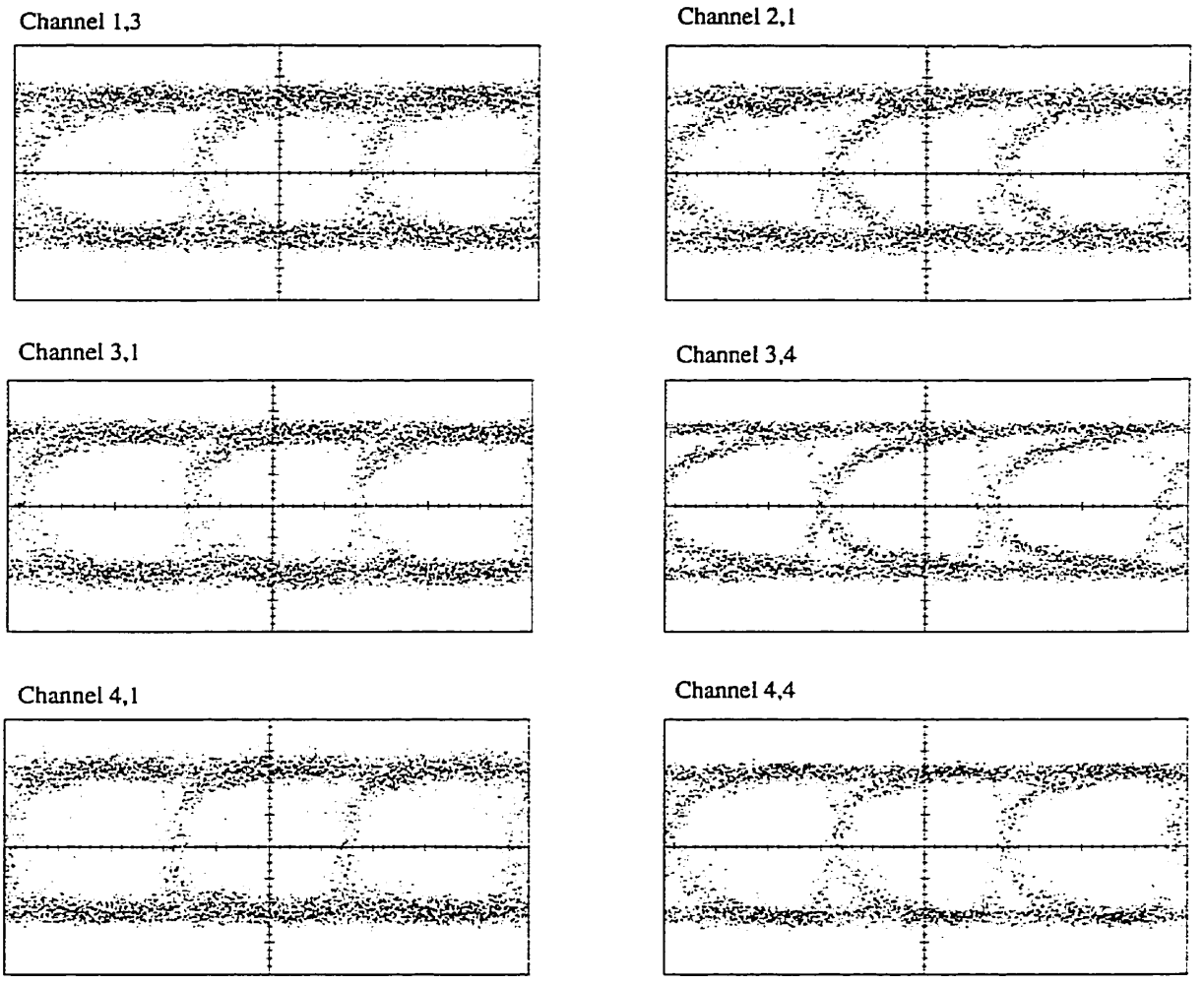


Figure 6.9: MSM/VCSEL system eye diagram at 155 Mb/s

6.3 CMOS/SEED based demonstrator

The system implements four 4-bit wide parallel unidirectional rings that interconnect four boards or stages. Each board has associated with it a 4-bit wide address. The transmitting board sends out packets with an address header that specifies the destination board. The implementation is based on CMOS/SEED VLSI optoelectronics arrays, a hybrid (lenslet+conventional optics) optical system [6.11], a baseplate and barrel optomechanics [6.12] and daughter/mother board and chip-on-board packaging [6.13]. The whole is integrated in a VME backplane chassis. Figure 6.10 shows a photograph of the completed system.

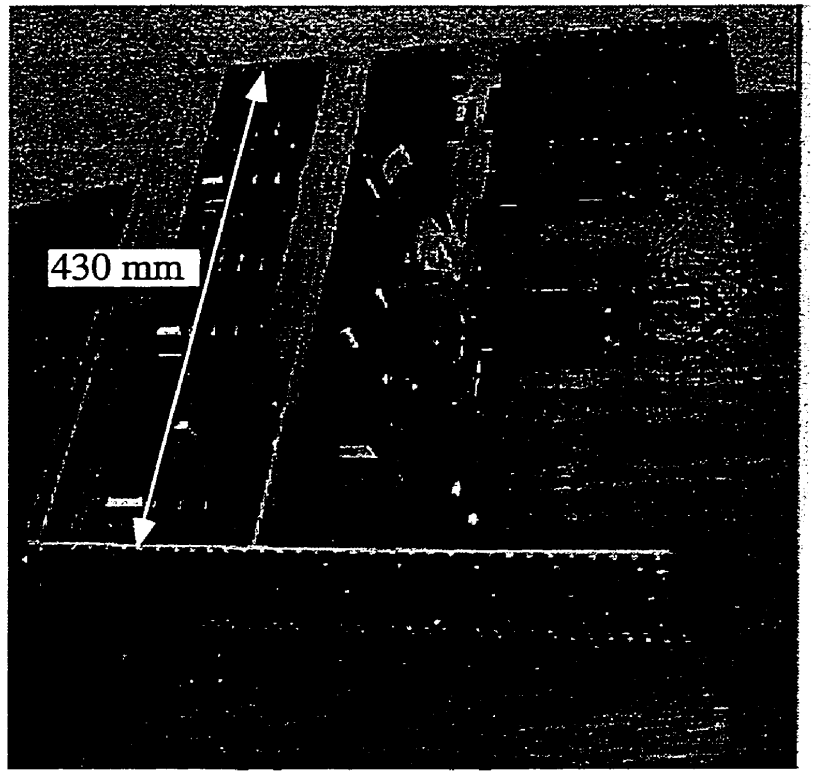
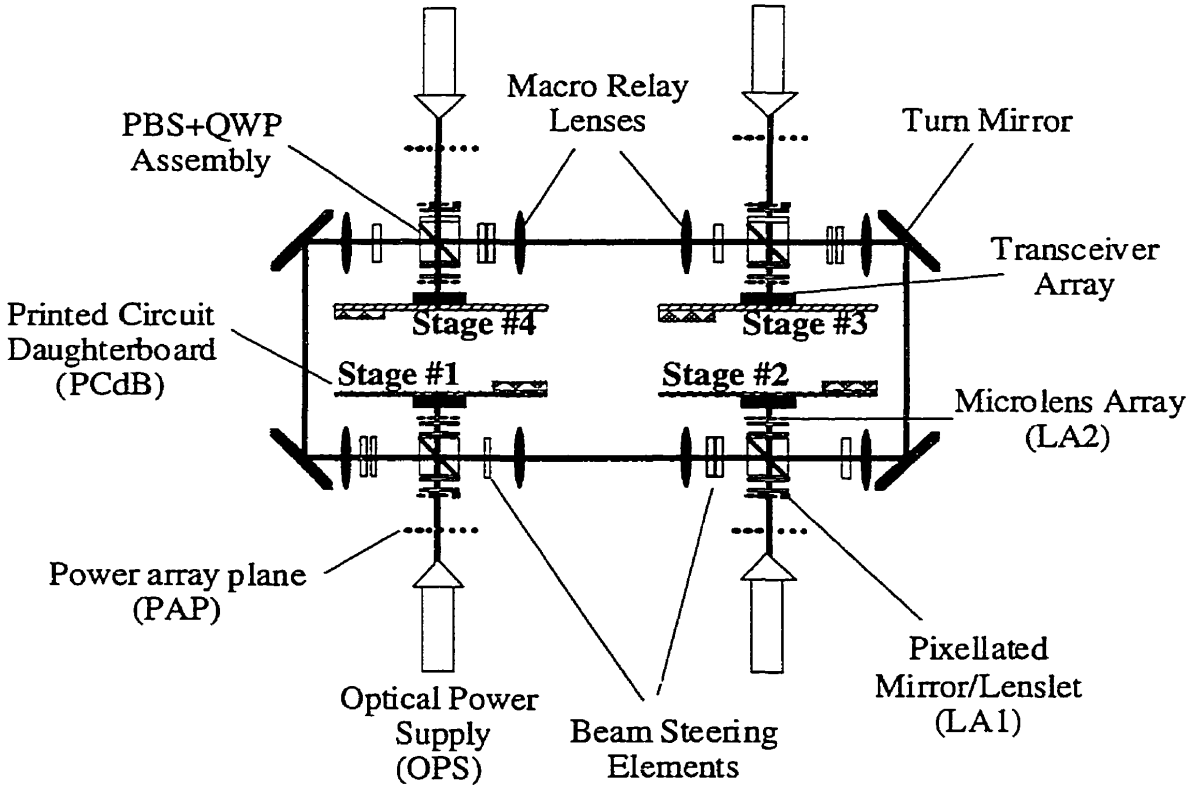


Figure 6.10: CMOS/SEED based backplane

The 4 stage system allows for data to be brought on and off the backplane via the CMOS/SEED array [6.14]. The hybrid-SEED technology was made available through ARPA/COOP/AT&T Hybrid SEED workshop. A 4X4 array of pixels each with one receiver and one transmitter was designed. The receiver and the transmitter operate in a differential mode (two MQW diodes per receiver and per transmitter). A dual-rail TIA receiver is used. Ten microwatts of optical power is required to operate the array at 2Mb/s. The receiver and transmitter are isolated from the digital logic to reduce the effect of digital switching noise on the analog circuitry. Four pixels make one 4-bit channel. Each one of the four 4-bit channel has an address recognition circuit that compares the incoming header address with the board address. The address encoding scheme is such that there is a broadcast capability. The array can operate in one of three modes; transmit mode which allows for data to be clocked onto the backplane, receiver mode which allows for extraction of data from the backplane and transparent mode which allows data to propagate to the next node in the system.

The optical system is based on three major subassemblies and forms a unidirectional optical interconnect. The first section is the optical power supply (OPS) similar to the modulator-based system (FET-SEED) described earlier. The OPS is a fiber

optic based delivery system which employs binary phase gratings, conventional lenses and risley steerers to take the output from a single laser (500mW) and uniformily distribute it into four 4X8 spot arrays. There is one OPS for each board. The light is then delivered to the active areas of the modulators using a lenslet relay system which employs diffractive lenslets. A polarizing beam splitter (BPS) quarter wave plate (QWP) assembly and pixellated mirrors are used for routing and interconnecting the optical beams from stage-to-stage. In addition, two conventional lenses are arranged in a telecentric relay configuration to complete the stage-to-stage connection. A schematic of the optical layout is shown in Figure 6.11. The custom optomechanics are based on a barrel and baseplate system, and are designed to be simple, compact and efficient. The slotted optomechanics is similar to the one discussed for the FET-SEED based system described above. The barrel optomechanics is similar to that of the MSM/VCSEL described earlier. One drawback of this design is that latency would increase with the number of boards thus limiting the scalability of the system. The contrast ratio of the modulators were measured to be less than one, and they were unusable for transceiving.



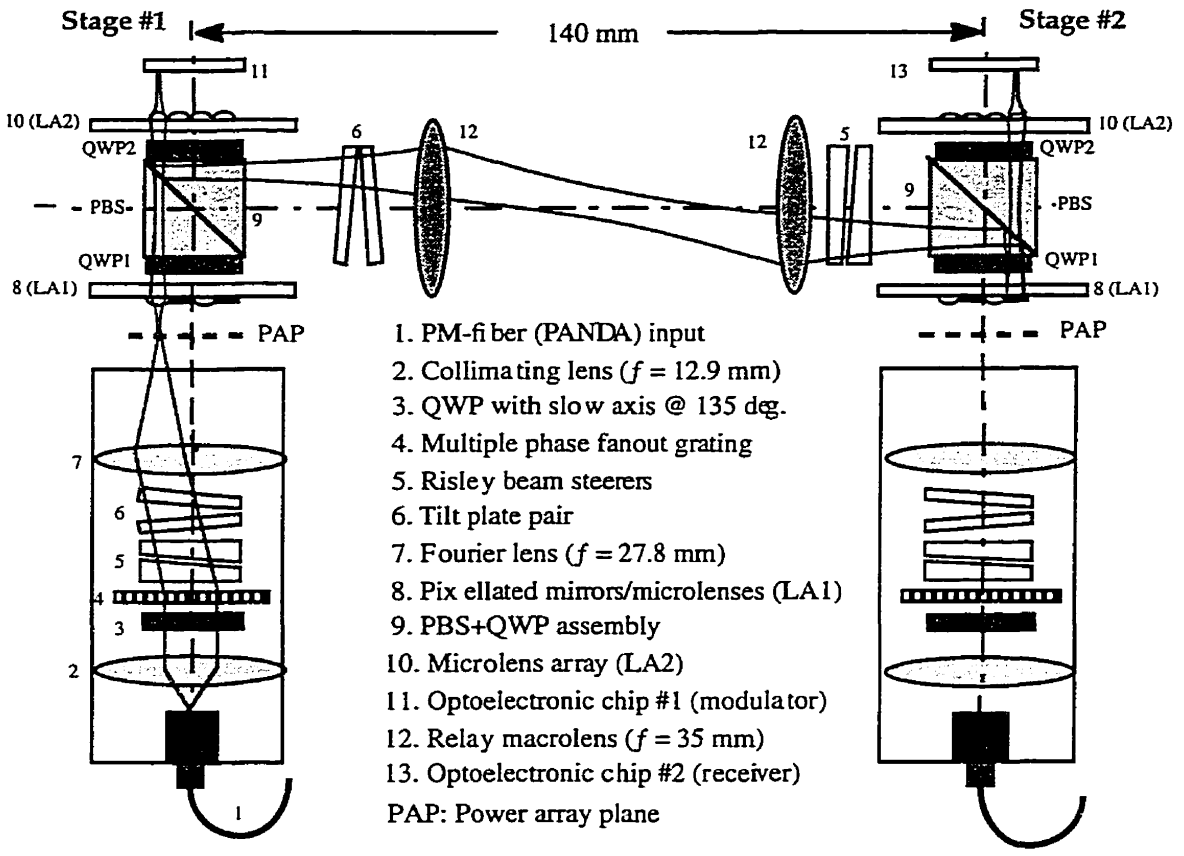


Figure 6.11: Optical ring interconnect

6.4 Summary and conclusions

Three backplanes have been designed and constructed. The first one was based on FET-SEED technology. The free-space optical communication channels were established using binary diffractive gratings, multilevel diffractive microlenses, polarizing optics, all integrated onto a slotted baseplate. Operational testing of the system in two modes was performed at data rates of 150 MBits/sec for individual channels, and 75 Mb/s for multiple channels. A single lenslet based interconnect was used to support four differential, eight total, optical channels, each operating at 25 Mb/s. This result points to the scalability of backplane level, free space optical interconnects for future, large switching and computing systems. The second system had VCSELs as the transmitter and MSMs as the detector. The demonstration system was capable of > 1.7 Gb/s of aggregate data capacity with up to 500 Mb/s operation on individual channels. The effective connection density of the system is > 6000 channel/cm^2. Using custom rod and barrel optomechanics and a daughter board/mother board assembly, the system demonstrated excellent robustness and stability.

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Chapter 7: Conclusions and Future Work

7.1 Conclusions

This thesis has discussed the design and implementation of VLSI optoelectronic receivers and transmitters for optical 2-D interconnects. Although mainly focused on transceiver design, this dissertation touches three disciplines as mentioned in the introduction. Therefore conclusions are drawn on three fronts:

- on the choice of the optoelectronic technology
- on the circuit design method
- on the packaging and system integration approaches.

Firstly, three optoelectronic technologies were considered, namely 1) the FET-SEED 2) the epi-electronic and 3) the hybrid CMOS technology. The FET-SEED technology has three major drawbacks. It has a high power dissipation, a low device yield and a high non-uniformity. The high power consumption originated with the use of static GaAs logic, and the effect of the underlying p-layer that increases the device parasitic capacitance leading to a higher power-delay product. The p-layer can cause up to a 60% penalty in the delay [7.1]. This is a typical trade-off for monolithic technologies that tolerate a non-optimized device to accommodate another (in this case the MQW diodes). Epi-electronic, on the other hand, provides more flexibility for the simultaneous optimization of optical and electrical devices. Optical devices are grown on top of commercial GaAs electronics that possesses a good (commercial) yield and uniformity that are better than for the FET-SEED. A mask was added to the commercial GaAs process to fabricate metal-semiconductor-metal (MSM) detectors that have a higher responsivity than the one formed by the normal process. Unfortunately only LEDs were available at the time of this research. The power they emitted was too low for reliable (low BER) transceiving high-speed data. The best technology of the three considered was the hybrid CMOS with which large arrays of VLSI transceivers can be produced. System designers have used them because of its impressive spatial bandwidth, and its availability. There are however problems that make this technology difficult to use in a system. Although the optical power can easily be tuned by the external lasers that supplies the read beams to the modulators, the output from those

transmitters is limited by the exciton intensity saturation, and a high insertion loss. Furthermore being a modulator-based technology (like the FET-SEED) the optics and optomechanics are complex. Modulator-based technologies require that an extra set of beams be provided compared to emitter based systems. This makes the assembly and manufacturing of such system more difficult than an emitter based system. However the on-chip power consumption for emitter technologies is currently high, and large arrays (i.e. 16X16) have not yet been available readily to the system designer.

Secondly, system performance improvement can also come from circuit design as was shown in this dissertation. The transceiver circuit design is important for implementing an optical solution that offers a marked advantage over electrical technologies. It can also make up for the deficiencies of the current optoelectronic technology. To help the circuit design, a circuit simulator was configured for the FET-SEED technology. This tool was used to design receivers, and transmitters for a backplane system. A main theme in this dissertation is that careful circuit design and layout can improve the alignment tolerance of an optical interconnect. Current-mode techniques were examined for the implementation of VLSI optoelectronic receivers. With a current-mode approach, the performance of receivers becomes less dependent on the capacitance, and the size of the detector. Consequently alignment tolerance can be achieved with a minimal impact on the receiver performance by oversizing the detectors. This dissertation introduces a misalignment tolerant array. A misalignment tolerant array improves the misalignment tolerance of an entire array by using more detectors than required, and by rerouting electrically (on-chip) misaligned optical inputs to the proper electrical chip output. Other circuit techniques were introduced to improve the performance of the interconnect. Receivers with gain and sensitivity that are weakly dependent on the bandwidth were achieved with buffers. Time-differential receivers were proposed to enlarge the dynamic range, and increase the tolerance on process variations and voltage supply fluctuations with a minimal amount of area and power consuming circuitry. Dynamic GaAs receivers were introduced for low-power transceiving. On the transmitter side, techniques were mainly investigate for reducing the switching power of modulator drivers, and improve the alignability of the read beam onto the modulator active area. In that regard, BiCMOS modulator driver promises high-speed and compactness when driving large misalignment tolerant modulators. Moreover the adiabatic operation of modulator drivers can dramatically reduce the power consumption compared to traditional charging. The overhead for such scheme was low and taken into account when making the comparison.

Finally, a simple 2-D interconnect model was proposed. The model takes into account all the transceivers design parameters. This model makes performance predictions for the system given a transceiver design. It helps to evaluate the impact of the transceiver design on the overall system performance. For a given receiver and transmitter design, it predicts the sensitivity for any given bit error rate (BER) at given data transmission rates.

A demonstrator approach was used to understand the design issues of an optical backplane. Systems using the FET-SEED and the hybrid CMOS technology, and a MSM/VCSEL technology have been designed and built. Chapter 6 summarized the performance of each. Although they demonstrated an aggregate bandwidth that was not up to the full potential of the optical solution, the packaging solution for such systems was demonstrated. Compact and sturdy optomechanics was designed for each demonstrator, and their long-term stability demonstrated. It was shown that the mother-daughter board and chip on board packaging ease the assembly and the alignment of the system. Also, the integration of optics and optomechanics into a standard VME backplane chassis was demonstrated.

7.2 Future Work

The future work lies in the three areas mentioned above. Device technology improvement and availability are required for the implementation of systems. More work should be done to continue the effort initiated in this dissertation on circuit techniques to improve the optical interconnect and the system performance. Finally more system demonstrators are needed to prove the worth of free-space technologies.

1) Emitter technology is needed. Flip-chip of VCSELs onto commercial silicon electronic would be desirable. Epi-electronics that integrates VCSEL is currently under development. The technology should be made readily available to system designers through CO-OP and workshops.

2) The work in this thesis was aimed at providing new analog techniques for designing transceivers used for a 2D optical interconnect system. Novel receivers were tested and characterized. Future work include their integration into a system and an assessment of their contribution to improving the system performance. This has already been tackled to some extent. Currently an 'intelligent' transceiver array of CMSA-based receivers have been designed and will be used in the next system demonstrator. Two clocks have been

used. One clock is used to operate the sense amplifier and the other is used to clock the data through the pipeline. A single-clock can be used with a modified CMSA and dynamic logic. This is an example of how proper circuit design can simplify the clocking of the array, and that of the system. The clocking of the backplane is a general problem that should be addressed more closely in the future. A low-power adiabatic VLSI optoelectronic transmitter is currently being designed, and a future demonstration is planned.

3) Alignment is the most important issue in considering large 2-D interconnect based systems such as a backplane. Thus, additional demonstrators are needed to demonstrate the alignability of the system. The misalignment tolerant array technique introduced here, and other techniques [7.2] ought to be used in conjunction to achieve a demonstration of an easily alignable system.

7.3 References

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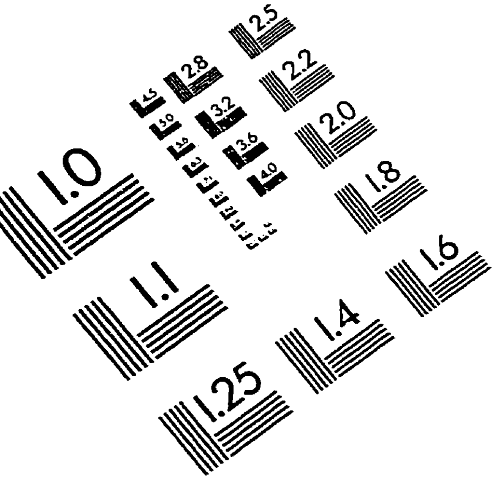
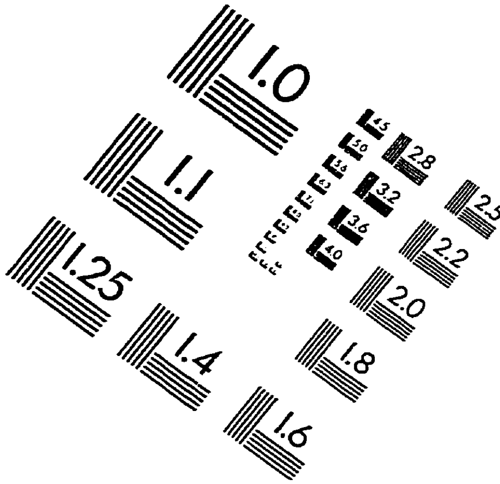
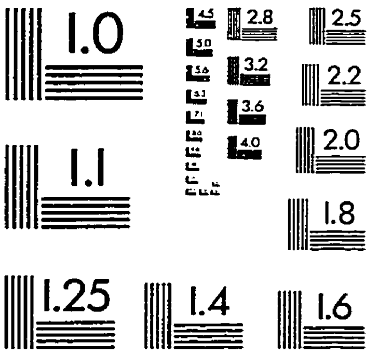
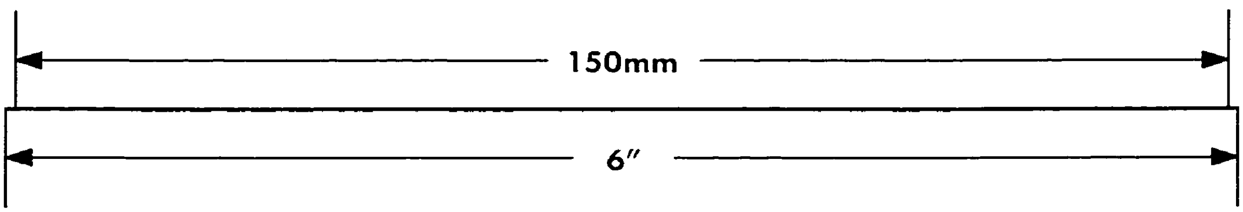
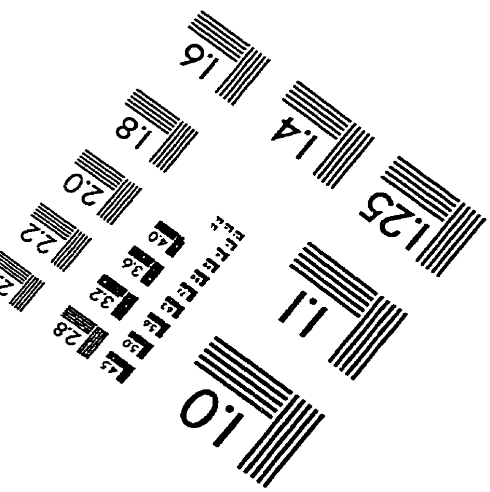
IMAGE EVALUATION TEST TARGET (QA-3)

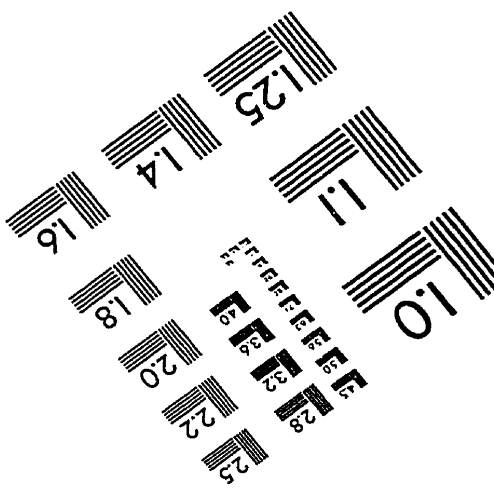












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