Reprogrammable Optical Phase Array

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ABSTRACT

The evolving needs of network carriers are changing the design of optical networks. In order to reduce cost, latency, and power consumption, electrical switches are being replaced with optical switching fabrics at the core of the networks. An example of such a network is an Agile All-Photonic Network (AAPN).

This thesis presents a novel device that was designed to operate as an optical switch within the context of an AAPN network. The device is a Reprogrammable Optical Phase Array (ROPA), and the design consists of applying multiple electric fields of different magnitudes across an electro-optic material in order to create a diffractive optical element. The configuration of the electric fields can change to modify the properties of the diffractive device.

Such a device has a wide range of potential applications, and two different ROPA designs are presented. Both designs are optimized to function as 1xN optical switches. The switches are wavelength tunable and have switching times on the order of microseconds. The ROPA devices consist of two parts: a bulk electro-optic crystal, and a high-voltage CMOS chip for the electrical control of the device. The design, simulation, fabrication and testing of both the electrical and optical components of the devices are presented.

SOMMAIRE

L'évolution des besoins des fournisseurs de réseau apporte des changements dans la conception des réseaux optiques. Afin de réduire les coûts, les délais et la puissance consommée, les commutateurs optiques remplacent leurs équivalents électriques au cœur des réseaux. Un réseau de type "Agile All-Photonic Network " (AAPN) en est un exemple.

Cette thèse présente un nouveau dispositif conçu pour servir de commutateur optique dans un réseau AAPN. C'est un réseau de diffraction à commande de phase reprogrammable (Reprogrammable Optical Phase Array ou ROPA) basé sur l'application à un matériau électro-optique de champs électriques multiples, d'amplitude variable, de manière à créer un diffracteur optique. Les champs électriques peuvent être reconfigurés de manière à modifier les propriétés du diffracteur.

Un tel dispositif se prête à des applications très diverses, et cette thèse présente deux structures de ROPA. Les deux concepts sont optimisés de manière à servir de commutateur optique 1xN. Ces commutateurs peuvent être ajustés en fonction de la longueur d'onde, et leur temps de commutation est de l'ordre de quelques microsecondes. Chaque dispositif ROPA a deux composants : un cristal électro-optique, et un circuit intégré CMOS générant les signaux électriques à haut voltage contrôlant le cristal. La conception, la simulation, et le test des composants électriques et optiques sont présentés.

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ACRONYMS

AAPN	Agile All-Photonic Network
DAC	Digital to Analog Converter
DNL	Differential Non-Linearity
DOE	Diffractive Optical Element
EO	Electro-Optic (as in material)
EO	Electrical-to-Optical (as in conversion)
ER	Extinction Ratio
FPGA	Field Programmable Gate Array
HV	High-Voltage
IL	Insertion Loss
INL	Integral Non-Linearity
ITO	Indium-Tin-Oxide
LSB	Least Significant Bit
MEMS	Micro-Electro-Mechanical Systems
OE	Optical-to-Electrical
OEO	Optical-Electrical-Optical
OPA	Optical Phase Array
OPL	Optical Path Length
PCB	Printed Circuit Board
PDL	Polarization Dispersion Loss
RCWA	Rigorous Coupled-Wave Analysis
ROPA	Reprogrammable Optical Phase Array
SA	Simulated Annealing
SEM	Scanning Electron Microscope
SOA	Semiconductor Optical Amplifier
TEC	Thermo-Electric Cooler

CHAPTER 1. INTRODUCTION

Over the past decade, there has been an evolution in the design of optical networks to match the evolving needs of Internet carriers. Networks are now designed not only to increase the available bandwidth, but also to decrease the overall network cost and to increase the flexibility of the network. One way to achieve these goals is to reduce the number of optical-electrical-optical (OEO) conversions and electrical switches by replacing them with optical switching fabrics to reduce cost, latency, and power consumption, as well as to make the switches data rate and protocol independent [1-4]. By introducing the requirement for very fast optical switching in the core, dynamic provisioning is possible, as is packet level switching.

Most currently available optical switching technologies are too slow for such dynamic provisioning, e.g. thermal-optical switches and Micro-Electro-Mechanical Systems (MEMS). In contrast, electro-optic switching holds great promise for use in optical networks due to its high-speed and lack of moving parts. However, it is also hampered by two drawbacks: if a waveguide structure is used the coupling losses tend to be high [5-7], but if a bulk structure is used then the voltage levels are close to 1kV [8-11]. This thesis presents an optical switch that is fast and uses voltage levels that are less than 300V.

The design consists in applying multiple electric fields of different magnitudes across an electro-optic material in order to create a Diffractive Optical Element (DOE). The configuration of the electric fields can change to modify the properties of the DOE. Such a device is referred to as a reprogrammable diffractive optical element, or a Reprogrammable Optical Phase Array (ROPA). The inherent flexibility of a reprogrammable diffractive element leads to many potential applications. This thesis focuses on using the ROPA device as an optical switch within an agile all-photonic network, as described in the next

section, but other applications include multiple spot generation, beam shaping, corrections to free-space misalignment, and a variable focus-length lens.

1.1 Agile All-Photonic Switch Requirements

Agile All-Photonic Networks (AAPNs) are a potential solution to the growing and changing needs of internet carriers [12]. An all-photonic network is defined as one in which the data remains optical and is never converted to an electrical signal in between the ingress and egress points, referred to as edge nodes, of the network. The term all-photonic is used to contrast with the alternate definition of an all-optical network, where both the data and the control signals remain in optical form. An agile network has an optical switching technology at the core that is very fast, allowing for a reconfigurable non-blocking fabric capable of packet level or time slot switching. Such an optical fabric presents unique performance requirements.

The elimination of OEO conversions leads to significant challenges in the way the network is designed. For the foreseeable future, there are no commercially available optical buffers or memory. Therefore once all electrical conversions are eliminated, there is no longer any ability to store data for traffic management or congestion control. A way to get around this limitation is to move the network control to the edge of the network, as in an all-photonic star configuration [13-15]. A star configuration also has the advantage of being easily scalable.

In the Agile All-Photonic Network (AAPN) research network, a star configuration is proposed. Figure 1 is a schematic of the proposed star architecture, indicating edge node and core node points.

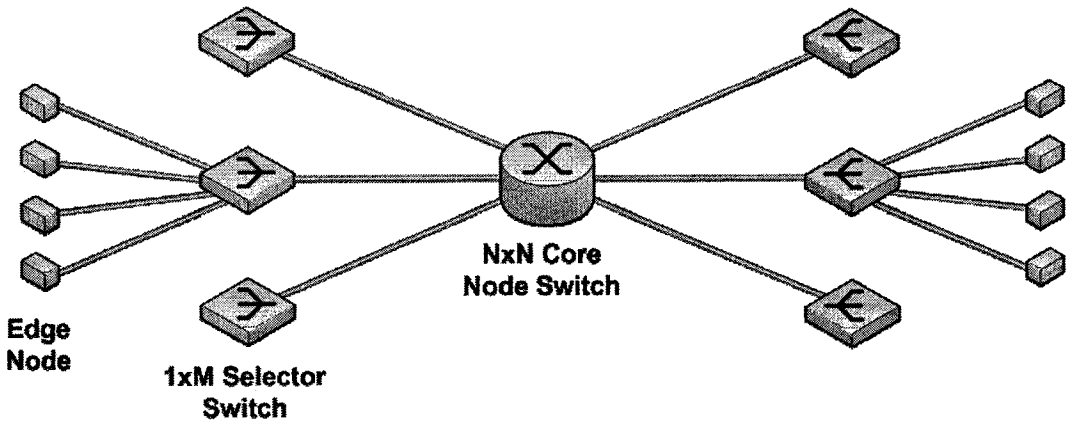


Figure 1. AAPN star network configuration

At the center of the star is an optical space switching fabric operating at a single wavelength. Multiple stars, each operating at a different wavelength, can be overlaid to provide redundancy and increased bandwidth. Figure 2 is a representation of a lambda-layered NxN switch fabric. All of the electrical-to-optical (EO) and optical-to-electrical (OE) conversions are performed at the edge nodes. All of the control, including traffic management and the determination of the core switch configuration, is also performed at the edge nodes, eliminating the need for optical memory or buffers. In order to avoid contention issues at the core, time slot switching is employed. At each time slot, the optical fabric in the core can be reconfigured.

The performance requirements for the switching core in such an AAPN network are very specific. First of all, the optical switching fabric must be fast to accommodate time slot switching with a very high granularity. Secondly, it must be low-loss and low-crosstalk since there is no signal regeneration from an OEO transponder. Finally, it must have a large port count to accommodate the star configuration of the network. For the AAPN architecture, the design target is an optical switching fabric capable of sub-1μs switching times, a 64x64 port count, and less than 10dB insertion loss.

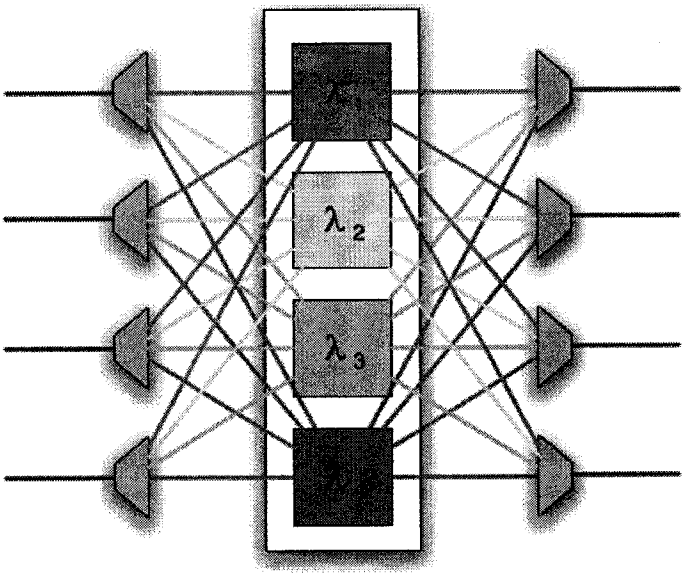


Figure 2. λ-layered NxN switch fabric

Regardless of the choice of architecture, fast optical switching technology represents a key enabler. For the purposes of this thesis, we define an optical switch as follows: a space switch device that is optically transparent, has N input ports and M output ports (e.g. 1x2, 1x4), and that is reconfigured via an applied electric signal (voltage or current).

1.2 ROPA Switch

Multiple optical switches have been demonstrated that are either fast, or low-loss, or high-port count, or wavelength independent. To our knowledge, there exist no optical switches that have all of those features simultaneously. The ROPA switch that is presented in this thesis has the following properties:

- Capable of nanosecond switching times.
- Based on bulk electro-optic properties, and therefore low-loss compared to waveguide electro-optic switches.
- Can be programmed as a 1xN port switch, suitable for use in a star configuration.

- Wavelength tunable, in that by applying different voltages to the electrodes, a different wavelength can be sent through the device and switched appropriately.
- Polarization dependent due to the EO material properties.

We propose two distinct ROPA designs: a 2-D array and a 1-D array. The 2-D array is more flexible; the 1-D array is simpler but more limited in its functionality. Both create 1xN fast electro-optic switches, and both are electronically controlled though flip-chipping to a high-voltage CMOS chip.

1.2.1 2-D array

In this configuration, the ROPA is a diffractive optical element operating in reflection mode as shown in Figure 3 below. The electro-optic crystal is flip-chipped to a CMOS chip. The incoming signal goes through the electro-optic material and reflects off the CMOS chip, or more specifically, off the electrodes in between the Electro-Optic (EO) material and the CMOS chip.

The EO material is sandwiched between a transparent grounded Indium-Tin-Oxide (ITO) electrode and an array of reflective metal electrodes. When the correct voltages are applied to the metal electrodes, a pattern of different refractive indices is created in the electro-optic material. This creates a diffractive element that can be reconfigured by changing the applied voltages.

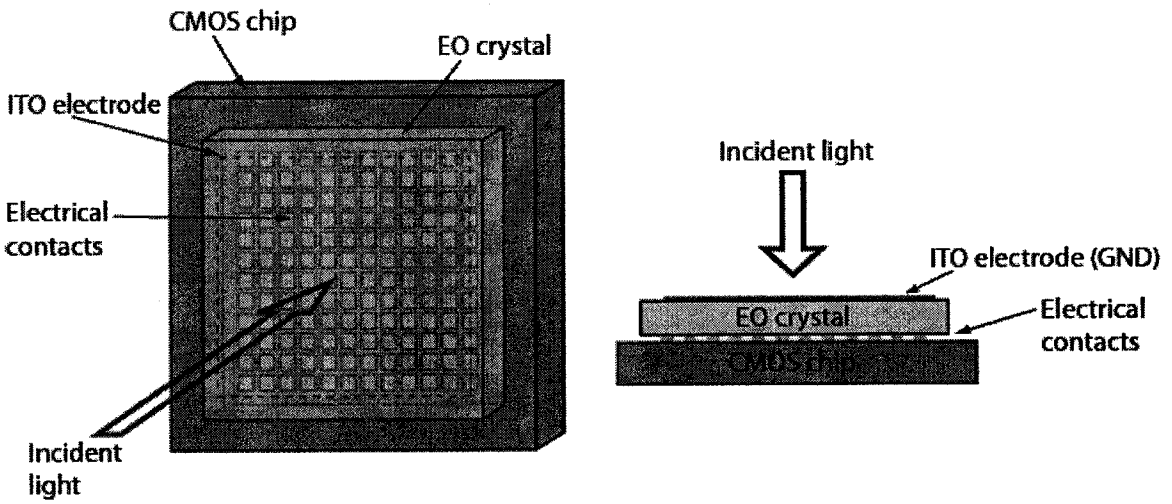


Figure 3. 2-D Optical Phase Array

The CMOS chip controls the voltages that are applied to the electrodes "underneath" the EO crystal. A computer in turn controls this CMOS chip. The CMOS chip is made from a high-voltage CMOS process capable of both low voltage and high-voltage digital design. The technology used for the CMOS chip is described in more detail in section 1.2.3.

An alternative design for the 2-D array, which simplifies the CMOS design, is shown in Figure 4 below. This design both reduces the number of independent voltages required and allows for a tighter spacing of the electrodes since the logic controlling each electrode can be placed on the periphery of the chip. The drawback is that since the voltages vary across only one dimension of the EO material, the incoming beam can only be steered in one dimension. However, this simplified design provides an excellent proof of concept.

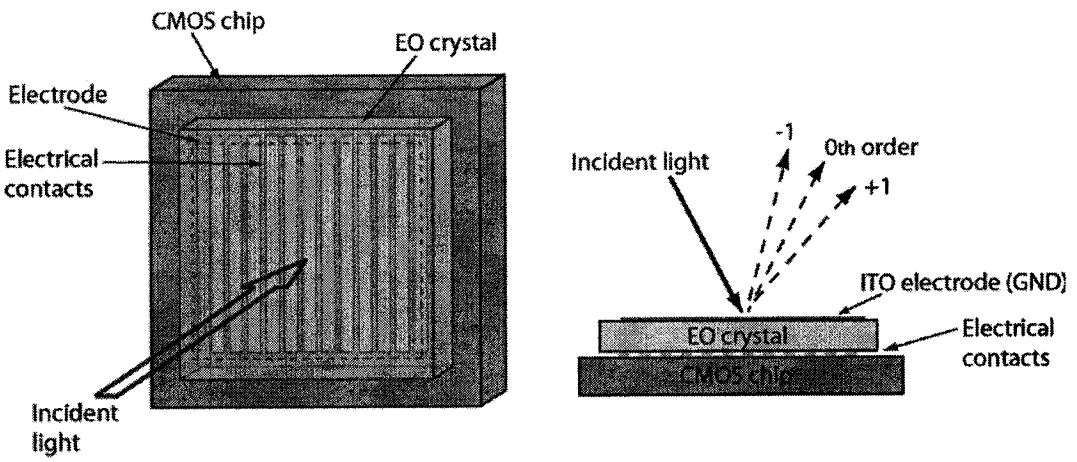


Figure 4. 1-D Simplified 2-D array for 1-D beam steering

1.2.2 The 1-D array

An alternative design for the ROPA is the 1-D array shown in Figure 5 below. This structure is very similar to other existing Optical Phase Arrays (OPAs) as discussed in greater detail in section 2.3. The difference between this design and the existing similar OPAs is that by providing the voltage through flip-chipping many more electrodes can be controlled, leading to lower losses. Also, the electro-optic crystal used will be neither $LiNbO_3$ nor $LiTaO_3$ but SBN:61 as discussed in section 3.1.2. The disadvantage of such a design is that the beam can only be steered in one-dimension. Its advantage over the 2-D array is that since the input signal propagates through a long length of EO material instead of just through its thickness, the electro-optic coefficient can be much lower and still produce a 2π phase shift for the same applied voltage.

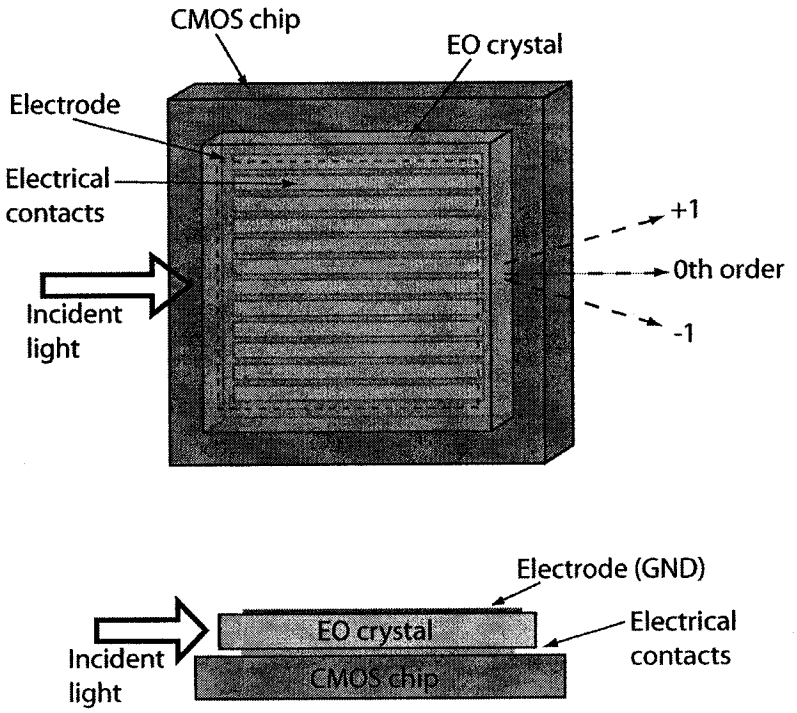


Figure 5. 1-D Optical Phase Array

Another significant difference between this design and the 2-D array is that since the signal propagates under the top electrode instead of through it, the top electrode no longer needs to be transparent and can be a simple grounded metal electrode.

1.2.3 High-voltage CMOS chip

In order for the ROPA switch to be compact and heterogeneously integrate both the optical and electrical components, a novel high-voltage CMOS process provided by DALSA Semiconductor is exploited. The process is the C08G quadruple well, three metal layer, epitaxial silicon process. This process combines 0.8 μm low-voltage transistors with high-voltage transistors on the same chip [16]. The high-voltage transistors can handle voltages of up to 300 V. The chip designed for the ROPA switch was fabricated through collaboration with the Canadian Microelectronics Corporation (CMC) in the first ever publicly available run by DALSA. Therefore, the ROPA switch represents the first

attempt to harness the capabilities of this new CMOS process and integrate it with an electro-optic material to create an optical device.

The main function of the chip is to provide independent voltages from 0 to 300 V to each of the electrodes on the EO crystal. To accomplish this, the architecture consists of an array of Digital-to-Analog Converters (DACs). Since the high-voltage transistors are quite large, a significant design challenge lay in minimizing the number of high-voltage transistors required, while maintaining the voltage resolution and accuracy needed to maximize the optical performance. Additionally, the design layout must be consistent with the flip-chipping requirements.

1.3 Original contributions

The work presented in this thesis is in many instances the result of the collaborative efforts of several people. This section outlines their efforts and then presents the original contributions to the field of optical switch design that are included in this thesis.

The concept of the ROPA design was the work of the author and her supervisor Professor David Plant, with Eric Bisaillon and Julien Faucher providing many brainstorming sessions to work out several of the details of the design.

The design of the CMOS chip was shared by the author and Ehab Shoukry. Mr. Shoukry was responsible for the implementation of the design and the simulation of the performance of the chip. Mr. Shoukry also designed the printed circuit board used to test the chip. The author, Mr. Shoukry and Christopher Ostafew all shared in the task of testing the chip. Mr. Ostafew also implemented all of the LabView interfaces that greatly simplified the testing of the devices.

The optical simulations of the ROPA device that were performed by the author were in a large part aided by Eric Bisaillon. Mr. Bisaillon's expertise in the field of optical simulations was invaluable in defining several of the algorithms used and in verifying the accuracy of the results.

The electrode deposition process that was developed specifically for this project was the result of the efforts of the author, Professor Keith Goossen from the University of Delaware, Professor Vincent Aimez from the University of Sherbrooke, and Etienne Grondin, also from the University of Sherbrooke. All of these researchers spent many long hours perfecting the metal deposition process that was critical to the project.

Professor Keith Goossen performed all of the flip-chipping of the EO crystals to the Si chips. In order to do so, he fine-tuned the process to deposit the flip-chip bumps in order to be compatible with the ROPA design.

The setup to measure the reflectivity of the electrodes was designed by Eric Bisaillon who also aided the author in modifying it to suit the testing requirements of the ROPA device.

The optical testing methods, optical testbeds, and all of the associated hardware (test chips and printed circuit boards) were the work of the author. Marie-Claude Nadeau developed the vacuum chuck system that was used by the author within the optical testbeds.

The original contributions presented in this thesis are:

- Concept of the ROPA design itself. This device is a compact, flexible, reprogrammable diffractive optical element, suitable for many applications. This thesis focuses on using the ROPA device for optical space switching applications.
- Development of simulation techniques for the optical performance of the ROPA device. In order to maximize the diffraction efficiency of the device, an iterative simulated annealing method was used to determine the optical voltage configuration for a particular desired device performance.
- Design of high-voltage chip architecture using a new semiconductor process. To our knowledge, this work is the first time a high-voltage CMOS technology has been used to create an array of digital-to-analog converters, useful for many high-voltage applications.
- Development of an electrode deposition process suitable for the needs of the ROPA design. The primary requirements were that the electrodes

adhere well to the chosen EO crystals, that they be reflective at telecommunication wavelengths, and that they be compatible with the subsequent flip-chipping process.

- Heterogeneous integration of an EO crystal to a high-voltage CMOS chip to create a compact reprogrammable diffractive optical element. To our knowledge, this is the first time such an integration has been attempted.
- Development of testing methodology for ROPA device that decouples the electrical and optical performances of the device.

Evidence of the impact of these contributions can be found in various published, accepted for publication, and submitted journal articles and conference papers, as well as a US provisional patent: [17-22].

1.4 Structure of thesis

This thesis comprises 6 chapters. Chapter 2 explores the current state-of-the-art optical switch technologies, and compares them to the ROPA switch for use within an agile all-photonic network. Chapter 3 discusses the optical design and simulations. This includes the choice of electro-optic material to be used for the ROPA switch, and the impact of the material choice on the design and the simulations. Chapter 4 discusses the design and simulation of the CMOS chip, and discusses the particularities of working with high-voltage transistor technology that imposed certain restrictions on the design. Chapter 5 presents the fabrication processes that were developed, and the experimental results for both the high-voltage chip testing and the testing of the optical performance of the ROPA device. Chapter 6 concludes and discusses future work.

CHAPTER 2. STATE OF THE ART SWITCH TECHNOLOGIES

This chapter explores and compares multiple space-switching technologies to evaluate their suitability for use within an Agile All-Photonic Network (AAPN). A set of switch parameters to be used for comparison is first defined, then several switch technologies are briefly described. Emphasis is placed on studying switches that fulfill the switching speed requirements of an AAPN. Afterwards, other optical phase array devices are presented and compared to the ROPA device.

2.1 Switch Parameters

In discussing switches for agile all-photonic networks, the most important parameter is arguably switching speed. In order to have a dynamically reconfigurable fabric for every time slot, switching speeds must be very fast. In the case of AAPN, we are proposing a network that switches timeslots that are 10μs long [12]. If the packets become much longer than 10μs then the network latency becomes significant. In order to have an efficient network the switching time should not exceed 10% of the timeslot length. For AAPN, this leads to a nominal switching time of less than 1μs. This switching time includes the time for the input to be redirected to a different output, the locking time necessary for the optical receivers at the edge nodes, as well as any required guard bands.

In general, optical switching technologies are either fast, with switching times in the tens of nanoseconds, or they are relatively slow with switching times that are over several hundred microseconds. These speeds are determined by the technology and cannot be significantly improved without migrating to an entirely different technology platform.

The next two parameters that are of roughly equal importance are the insertion loss and crosstalk values of the switching technology. Both of these parameters degrade the quality of the optical signal and cause errors to appear at the optical receiver. If the switch fabric is made up of small port count switches,

such as 1x2 switches, then the insertion loss and crosstalk parameters of the individual switching elements must be very low to be able to scale up to a large port count fabric with reasonable insertion losses. As a starting point for the AAPN network, a maximum insertion loss of 10dB is defined for a 64x64 optical fabric. This number allows for the use of standard output power lasers, and will not cause the optical signal to drop below the sensitivity of the receiver for a 10Gb/s signal.

Another parameter to consider when evaluating switching technologies includes the polarization dependence of the switch. If a switching technology is polarization dependent, then the cost of the star network becomes much higher since the size of the optical fabric needs to be doubled to handle each polarization state separately. Other parameters that can be considered include power consumption, the physical size of the fabric, and the cost.

2.2 Switching Technologies

As discussed in the previous section, since speed is the most important parameter in evaluating switches for use in an agile all-photonic network, certain switching technologies can be eliminated as candidates for the switching fabric. These include switches that are based on mechanical motion (e.g. MEMS) [23-29], thermal effects [30-35], liquid crystals [36-39], and acousto-optic effects [40-42]. All of these switching technologies have switching times that range from several microseconds to several milliseconds, as shown in Figure 6 below. The ideal switch for an AAPN is represented by a small square and is labelled "Target switch."

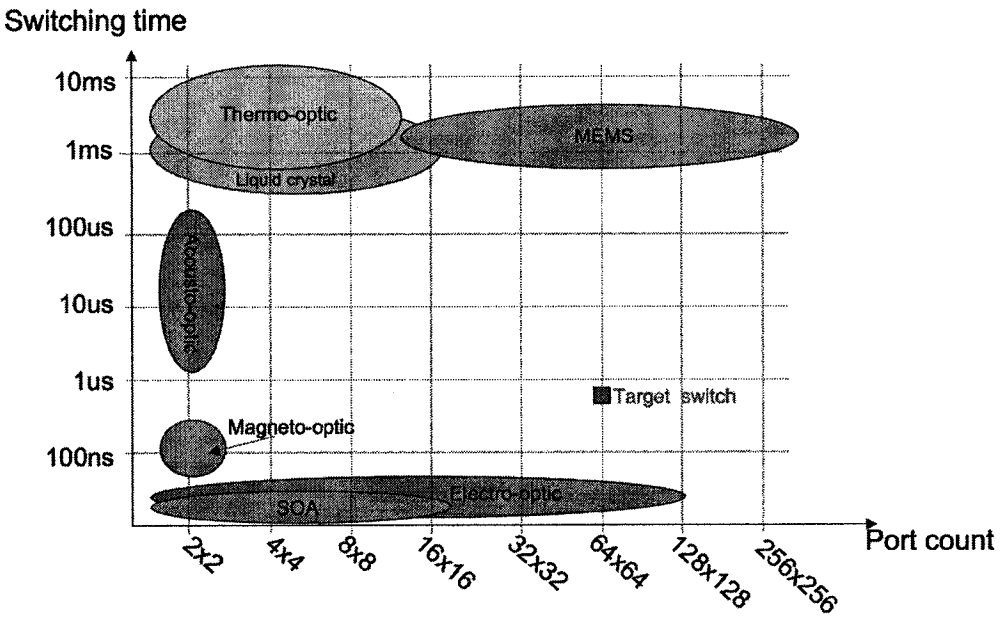


Figure 6. Comparison of switch technologies based on switching time and port count

The switching technologies that are inherently fast enough for an agile all-photonic network are based on semi-conductor optical amplifiers (SOAs), electro-optic (EO) effects, and magneto-optic effects. These three technologies have switching times that range from less than a nanosecond to several hundred nanoseconds, all of which are appropriate for an agile all-photonic network. These technologies are described in more detail in the following sections.

2.2.1 Electro-Optic (EO) Switches

The electro-optic effect occurs when a voltage is applied to a crystalline material, resulting in a change in the index of refraction. This change in index occurs very rapidly, usually limited in speed by the electronic circuitry, but is unfortunately strongly polarization dependent. There are four distinct technologies that exploit the electro-optic effect: bulk switches, waveguide switches, holographic switches, and optical phased arrays.

Bulk EO switches use the electro-optic effect to either refract or reflect a light beam [8, 43-47]. The switches are implemented in electro-optic materials such as $LiNbO_3$ or $LiTaO_3$. These crystalline materials are initially poled to create domain-inverted regions. When a voltage is afterwards applied to the

entire crystal, there is an opposite change in index between the inverted regions and the non-inverted regions. This creation of a Δn between regions can be used to refract the beam, or to reflect the beam through total internal reflection. The main limitations of such a technology are the very high voltages required to create a sufficiently strong E-field though the bulk material to get the required Δn, and the low port counts that are typically achieved.

Waveguide switches are based on the same electro-optic principles as the bulk electro-optic switches, but they confine the light to a narrow waveguided region [6, 48-51]. Given this geometry, much smaller voltages are required to obtain E-fields of similar strength. Since the voltages are smaller, switching speeds on the order of nanoseconds can be achieved. Three types of EO waveguide switches are typically built: directional couplers, interferometric switches, and digital optical switches (Y-branch). All of these configurations can be used to create 1x2 and 2x2 switches. Large port count switches can be built only by cascading multiple stages of these switches.

Holographic EO switches are based on the principle that electrically or optically controlled index changes in a material cause the diffraction of a beam to the appropriate output port [9, 52]. These switches can be implemented using a slower response material such as liquid crystals, but can also be implemented in faster materials such as $LiNbO_3$ or KLTN. The main limitation of this technology is that poor diffraction efficiencies lead to high insertion losses, though large port counts are feasible.

Optical phased arrays are one dimensional arrays in an electro-optic material with optical path lengths that are voltage controlled [53-56]. The resultant diffraction redirects the beam to any of several output ports. However, since each path is controlled by a separate electrode, there are necessarily gaps between the electrodes which lead to a reduction in the diffraction efficiency. These phased arrays can be implemented in a bulk EO crystal, or using waveguides in an EO crystal, or using liquid crystals. A more detailed discussion of optical phase arrays can be found in section 2.3.

2.2.2 Semiconductor Optical Amplifier (SOA) switches

SOA based switches are essentially on/off modulators that are controlled with a bias voltage. By creating a population inversion in the semiconductor using a bias voltage, amplification is achieved. Without a bias voltage, and therefore without a population inversion, the signal is absorbed. By using the SOAs in combination with passive waveguide couplers, low port count single-stage switches can be created [57-61]. One significant difference between the SOA switches and other optical switches is that noise is introduced along with the signal amplification. Noise factor values can be greater than 5dB. Therefore, even though the insertion loss of the switch can be very low, or even provide gain, it cannot be compared to an optical switch with equally low insertion loss but no amplification.

2.2.3 Magneto-Optic Switches

Magneto-optic switches use an orthoferrite crystal to rotate the polarization state of a linearly polarized input beam [62, 63]. The orthoferrite crystal, typically yttrium iron garnet (YIG), is controlled using a magnetic field instead of an electric one, as for the electro-optic switch technologies. When such crystals are used in combination with polarization beam splitters, a 2x2 switch is achieved. Though the theoretical switching time is less than 100 ns, in practice the switching times are closer to 300 μs. This is because while switching, the domains of the YIG crystal display random fluctuations that are not easily eliminated and need time to settle [62].

2.2.4 Comparison of Fast Switch Technologies

The following table summarizes the typical performance of the various fast optical switch technologies. The table is based on experimentally demonstrated devices, not on future projected performances or on theoretical results.

Table 1. Comparison of fast switching technologies

	SOA	Electro-optic				Magneto-optic
		Bulk	Waveguide	Optical phased array	Holographic	
Port count	2x2, 4x4	1x2, 1x4, 2x2	1x2, 1x4, 2x2	1x16, 1x32, 1x64	1x2, 4x4	1x2, 2x2
Insertion loss	0-5dB	3-5 dB	<4 dB	>8 dB	>4 dB	1 dB
Crosstalk	Good	Good	Good	Poor	Average	Good
PDL	Low	High	Low	High	High	Low
Wavelength dependence	High	Low	High	High	High	Low
Number of stages for 64x64 fabric	High	High	High	Low	Low	High

2.3 Optical phase arrays

Optical phase arrays have been proposed for use in optical switching or beam steering for several decades. Experimentally demonstrated OPAs, designed primarily for beam steering, are summarized in this section. As will be shown, they suffer from several drawbacks. In particular, they are either limited to steering the beam in only one dimension, or they are based on a liquid crystal design and therefore have slow switching speeds, or they have a small number of electrodes which results in very high optical losses.

2.3.1 OPA with all electrodes on one side of the EO material

A plane wave is normally incident onto a PLZT crystal with electrodes deposited on the front surface [53, 64, 65]. The electrodes are not transparent (i.e. chrome-gold electrodes), so they block the incoming beam, which greatly reduces the overall diffraction efficiency of the device. The electrode voltages alternate between a high voltage and ground. The area in between the electrodes experiences an E-field that varies the index of the material. The beam can only be steered in one dimension.

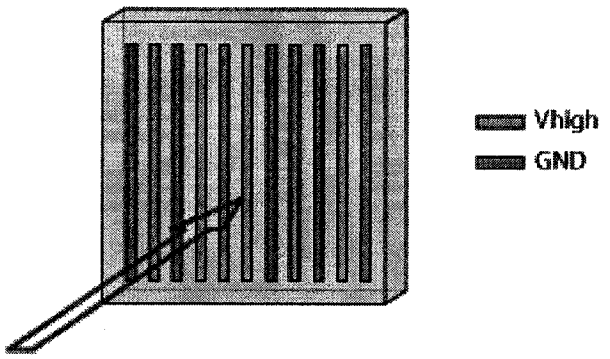


Figure 7. OPA with electrodes on one side

2.3.2 Liquid crystal based OPA

A plane wave is normally incident onto a material with discrete electrodes deposited on the front surface, and one large ground electrode on the back [38, 66, 67]. This device is used in reflection mode. If the electrodes are not transparent, they block the beam, causing insertion loss. Liquid crystals are used as the electro-optic material, which means that the switching time is on the order of a millisecond.

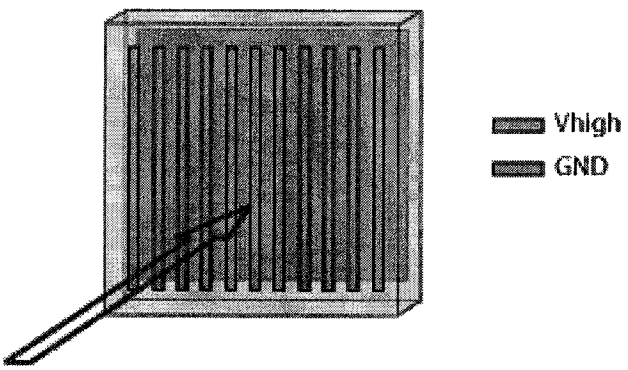


Figure 8. Liquid crystal OPA

2.3.3 Beam propagation parallel to the electrodes

A highly elliptical beam is incident onto the side of a $LiNbO_3$ or $LiTaO_3$ crystal with discrete electrodes deposited on the front surface, and one large ground electrode on the back [55, 56, 68]. The beam is not blocked by the electrodes, but propagates underneath them. Few electrodes are used (4 to 46)

leading to poor efficiencies due to low periodicity. As the electro-optic coefficients of both $LiNbO_3$ and $LiTaO_3$ crystals are not very high, large voltages are required ($\approx$ 600 V) for crystals about 350 μm thick.

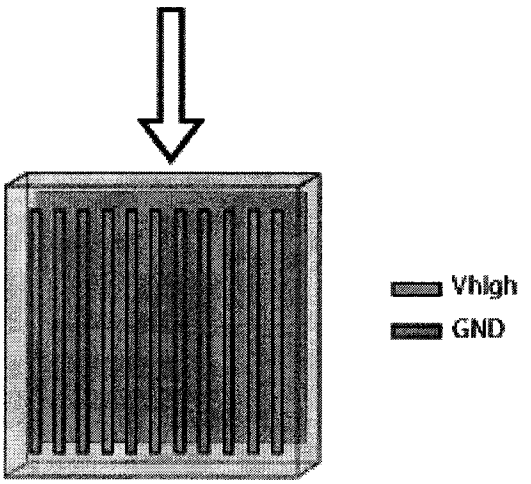


Figure 9. Beam parallel to the electrodes

2.3.4 Waveguide based

A beam is coupled into a 1-D array of waveguides, using free-space optics or input and output coupling gratings [7, 54, 69, 70]. Individual electrodes are deposited over each waveguide channel (or triangular electrodes over a group of channels), with a ground electrode on the other side of the substrate. The effective index of each waveguide is changed through an applied E-field. Since waveguides are used, the voltages required are small ($\approx$ 10 V) but the insertion losses are high (> 15 dB).

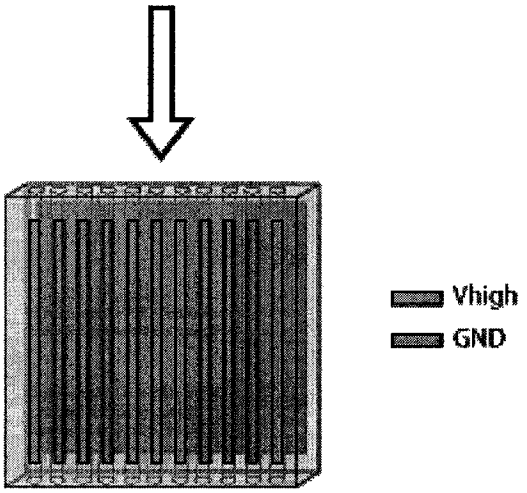


Figure 10. Waveguide OPA

2.4 Summary

In the field of optical space switches, there is an extremely diverse set of technologies that can be used to implement a switch. Inherently, certain switch technologies, such as MEMS or thermo-optic switches, have switching speeds that are too low to be considered for use within an AAPN. The most significant technologies that are fast enough include electro-optic devices and SOA devices. Of the electro-optic switching technologies, they either suffer from high insertion loss, low port count, or very high voltage requirements (> 1 kV). SOA devices are low port count, but they are unique in that they can provide gain as opposed to insertion loss.

Also explored within this chapter was the subset of switches consisting of optical phase arrays. Of these switches, the most similar to the 2-D ROPA design are the liquid crystal based switches described in section 2.3.2. These switches are very flexible and can create large port count switches, but the liquid crystal technology limits the switching speed. The most similar to the 1-D ROPA design are the ones with the light propagating parallel to the electrodes and within a bulk EO crystal as described in section 2.3.3. The most significant difference between these and the 1-D ROPA design is that the ROPA switch provides a higher diffraction efficiency by using a larger number of electrodes with a tighter pitch.

CHAPTER 3. OPTICAL DESIGN AND SIMULATIONS

This chapter covers the design and simulations of the optical component of the ROPA design. It begins with the choice of electro-optic material for both the 1-D and 2-D designs. The requirements for the two designs are different, and therefore two different materials are chosen. After the EO material has been chosen and the optical properties are known, the simulation techniques are discussed. Again, as the two designs are quite different optically, two different simulation techniques are used, though both are based on rigorous coupled wave analysis. As the optical performance is intrinsically tied to the voltages used to define the diffraction grating, an iterative technique is used to fine-tune the voltages and maximize the diffraction efficiency.

3.1 Electro-optic materials

The choice of an electro-optic material is critical to the design of the ROPA device. Many factors must be considered, and the five most important are listed here in decreasing order of importance.

Strength of the electro-optic coefficient

The most important factor when choosing the electro-optic material is arguably the strength of the electro-optic coefficient. A higher electro-optic coefficient means in practice that a lower voltage is needed to get a 2π phase shift in the optical path length. When a 2π phase shift occurs, the optical path length has shifted by an entire wavelength:

$$\lambda = \Delta nL \tag{3.1}$$

where L is the length of the electro-optic material through which the signal propagates, and Δn is the change in index of refraction of the material when a voltage is applied. This is a necessary condition to diffracting the incoming beam of light using the device.

Transparency to infrared

The optical losses of the material are significant since they will directly affect the fiber-to-fiber losses of the device. As the ROPA device is designed to operate within an AAPN network, it must be transparent to telecommunication wavelengths. In particular, it must be transparent to 1300 nm light through to 1600 nm. Fortunately, most materials surveyed satisfied this condition with very low losses (dB/cm) at telecommunication wavelengths. Additionally, in the 2-D ROPA design the light passes though roughly only 1 mm of material, leading to low overall losses even if the losses per centimeter were high.

Response time

The requirement for a very fast response time highlights the advantages of electro-optic materials over other technologies such as MEMS and liquid crystals. Electro-optic crystals in general have response times on the order of nanoseconds, and the final speed of the device will most likely be limited by the electronics and not by the response time of the material.

Curie temperature

The device will need to operate below the Curie temperature of the electro-optic material. If the crystal is heated above its Curie temperature, it goes through a phase transition and loses molecular polarization. Therefore the material will either need to have a Curie temperature that is higher than the operating temperature, or the device will need to be cooled.

Cost and availability

The cost and availability of the EO materials varies greatly. These factors are considered on a case-by-case basis.

The next two sections discuss the specific EO requirements for the 2-D and the 1-D ROPA designs. The five factors mentioned above will determine the material choices.

3.1.1 EO crystal for the proposed 2-D ROPA design

The primary consideration when choosing a material is the strength of the electro-optic coefficient in the desired direction. For the 2-D design, the E-field will be applied across the device, in the direction of propagation of the light, meaning that the E-field of the incoming light will be *perpendicular* to the applied electric field. Therefore a crystal must be found for which the electro-optic coefficient is such that the index change is perpendicular to the applied E-field, i.e. parallel to the direction of the E-field of the light. Consider the following tensor for the electro-optic coefficients:

$$r_{ij} = \begin{bmatrix} r_{11} & r_{12} & r_{13} \\ r_{21} & r_{22} & r_{23} \\ r_{31} & r_{32} & r_{33} \\ r_{41} & r_{42} & r_{43} \\ r_{51} & r_{52} & r_{53} \\ r_{61} & r_{62} & r_{63} \end{bmatrix} \tag{3.2}$$

When multiplied by an E-field, we get:

$$\begin{bmatrix} \Delta\left(\frac{1}{n^2}\right)_1 \\ \Delta\left(\frac{1}{n^2}\right)_2 \\ \Delta\left(\frac{1}{n^2}\right)_3 \\ \Delta\left(\frac{1}{n^2}\right)_4 \\ \Delta\left(\frac{1}{n^2}\right)_5 \\ \Delta\left(\frac{1}{n^2}\right)_6 \end{bmatrix} = \begin{bmatrix} r_{11} & r_{12} & r_{13} \\ r_{21} & r_{22} & r_{23} \\ r_{31} & r_{32} & r_{33} \\ r_{41} & r_{42} & r_{43} \\ r_{51} & r_{52} & r_{53} \\ r_{61} & r_{62} & r_{63} \end{bmatrix} \begin{bmatrix} E_x \\ E_y \\ E_z \end{bmatrix} \tag{3.3}$$

The changes in refractive indices can then be used in the index ellipsoid:

$$\left(\frac{1}{n^2}\right)_1 x^2 + \left(\frac{1}{n^2}\right)_2 y^2 + \left(\frac{1}{n^2}\right)_3 z^2 + 2\left(\frac{1}{n^2}\right)_4 yz + 2\left(\frac{1}{n^2}\right)_5 xz + 2\left(\frac{1}{n^2}\right)_6 xy = 1 \tag{3.4}$$

Therefore, the electro-optic coefficients r_{ij}, for which i=j, do not contribute at all towards creating an index change in a direction perpendicular to the E-field. They only create an index change in the same direction as the applied E-field. The coefficients r_{12}, r_{13}, r_{21}, r_{23}, r_{31}, and r_{32} all create an index change in the desired perpendicular direction. However, none of the materials surveyed (such as $LiNbO_3$, $LiTaO_3$, SBN, PLZT, etc...) had large enough electro-optic coefficients in those positions in the tensor to allow for their use while still using voltages below 300 V.

This leaves the "off-axis" coefficients: r_{ij} for which i > 3. The material $BaTiO_3$ has the following electro-optic tensor:

$$r_{ij} = \begin{pmatrix} 0 & 0 & 12 \\ 0 & 0 & 12 \\ 0 & 0 & 112 \\ 0 & 1920 & 0 \\ 1920 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{3.5}$$

where the units of the coefficients are in pm/V. This material is tetragonal with a 4 mm form. When there is no applied electric field, the x and y axes both have an index of refraction n_o=2.37 (at 800 nm), and the z axis has the index of refraction n_e=2.32 (at 800 nm) [71].

Let us assume that the crystal is used with the following orientation:

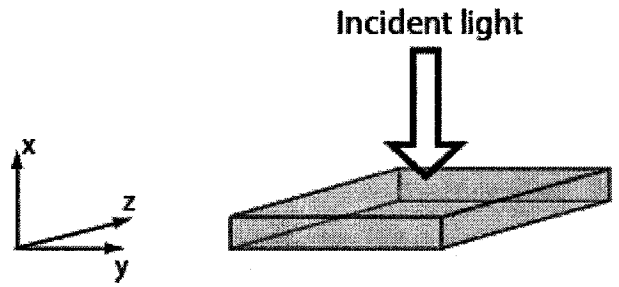


Figure 11. Orientation of crystal with respect to incoming light

The electric field is applied along the x-axis. The resultant index ellipsoid is:

$$\frac{x^2}{n_o^2}+\frac{y^2}{n_o^2}+\frac{z^2}{n_e^2}+2r_{51}E_x xz=1 \tag{3.6}$$

Since there is no index change along the y-axis for a non-zero electric field, we can consider only the xz plane. If we graphically plot the index ellipsoid for both $E_x = 0$ (dashed line) and $E_x >> 1$ (solid line), we get:

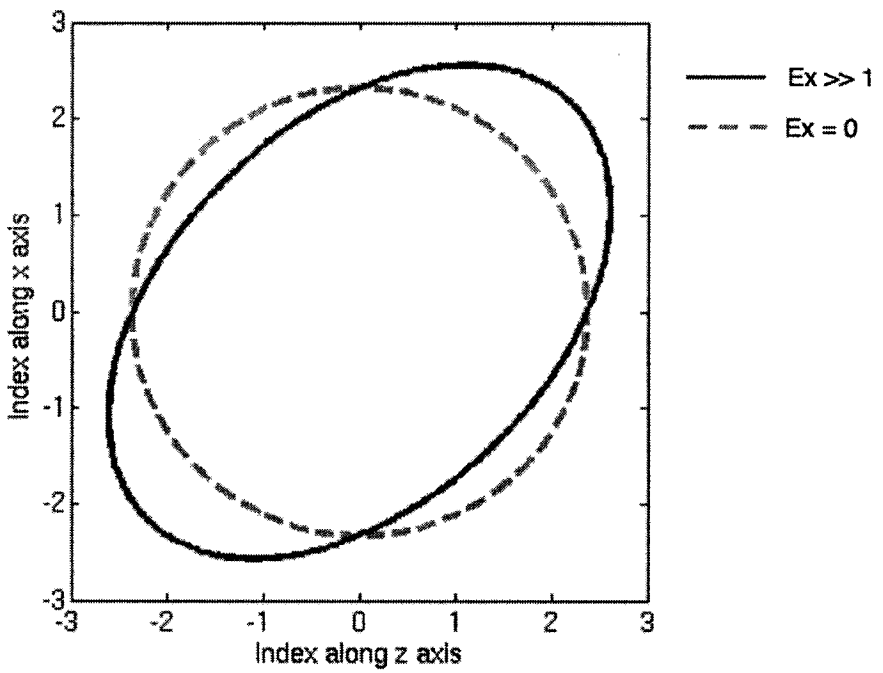


Figure 12. Index ellipsoid when voltage is applied along the x-axis

As can be seen in Figure 12, to benefit from the large r_{51} coefficient when applying an electric field along the x-axis, the incident light must be propagating along the x = z direction. This means the incident angle (within the crystal) must be 45°. There are two ways to achieve this. The first is to use a 45°-cut $BaTiO_3$ crystal. With a crystal with such an orientation, the incident light arriving perpendicularly to the top surface of the crystal would propagate along the x = z axis within the crystal, as shown in the figure below.

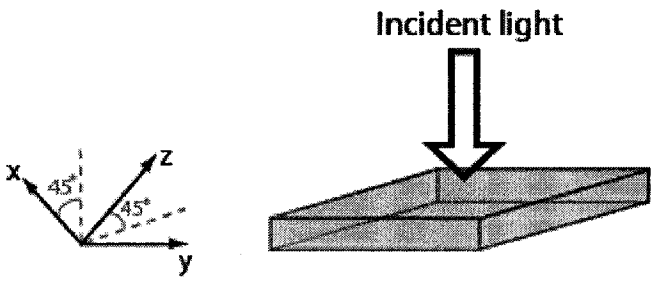


Figure 13. Light incident on 45° cut $BaTiO_3$

It is difficult to obtain a $BaTiO_3$ crystal cut at 45° [72], and quite expensive. Therefore, an alternative way of using the crystal has been explored. Due to the high index of refraction of the crystal, it is not possible to have the incident light refract within the crystal with an angle higher than the critical angle given below:

$$\theta_c = \arcsin\left(\frac{n_{air}\sin(90^o)}{n_{crystal}}\right) = \arcsin\left(\frac{1}{2.35}\right) = 25.2^o \qquad (3.7)$$

Note that the value of $n_{crystal} = 2.35$ used is the index on the index ellipsoid when x = y, and when there is no applied E field.

Therefore, with the crystal cut as shown in Figure 11 above, the direction of propagation of the light within the crystal cannot exceed an angle of 25.2°. However, for a given voltage under 300 V, there is still a sufficient index change at smaller angles to obtain a 2π phase shift.

Consider the following geometry, showing the orientation of the incoming light with respect to a $BaTiO_3$ crystal:

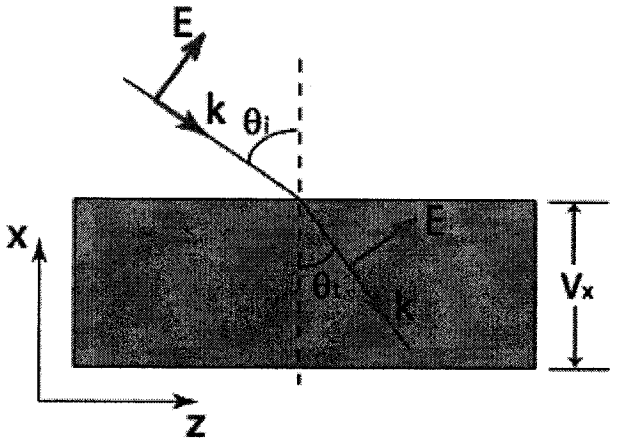


Figure 14. Light incident on crystal with voltage applied along the x-axis

Let θ_t define the direction of the propagation of the light within the crystal, and let θ define the direction of propagation of the E-field within the crystal. When there is no electric field applied to the crystal ($E_x = 0$), the index of refraction sampled by the incoming light is:

$$n = \frac{\left(\frac{1}{(\tan\theta * n_o)^2} + \frac{1}{n_e^2}\right)^{-1/2}}{\sin\theta} \tag{3.8}$$

When there is an electric field applied to the crystal along its x-axis, the index of refraction becomes:

$$n_{E_x} = \frac{\left(\frac{1}{(\tan\theta * n_o)^2} + \frac{1}{n_e^2} + \frac{2r_{51}E_x}{\tan\theta}\right)^{-1/2}}{\sin\theta} \tag{3.9}$$

The change in refractive index seen by the light can be determined by subtracting equation 1 from equation 2, i.e. $\Delta n = n_{E_x} - n$.

If we consider a piece of $BaTiO_3$ that is 500 μm thick and oriented as shown in Figure 14, then with the light going all the way through the crystal (transmission mode) we get the following change in index of refraction:

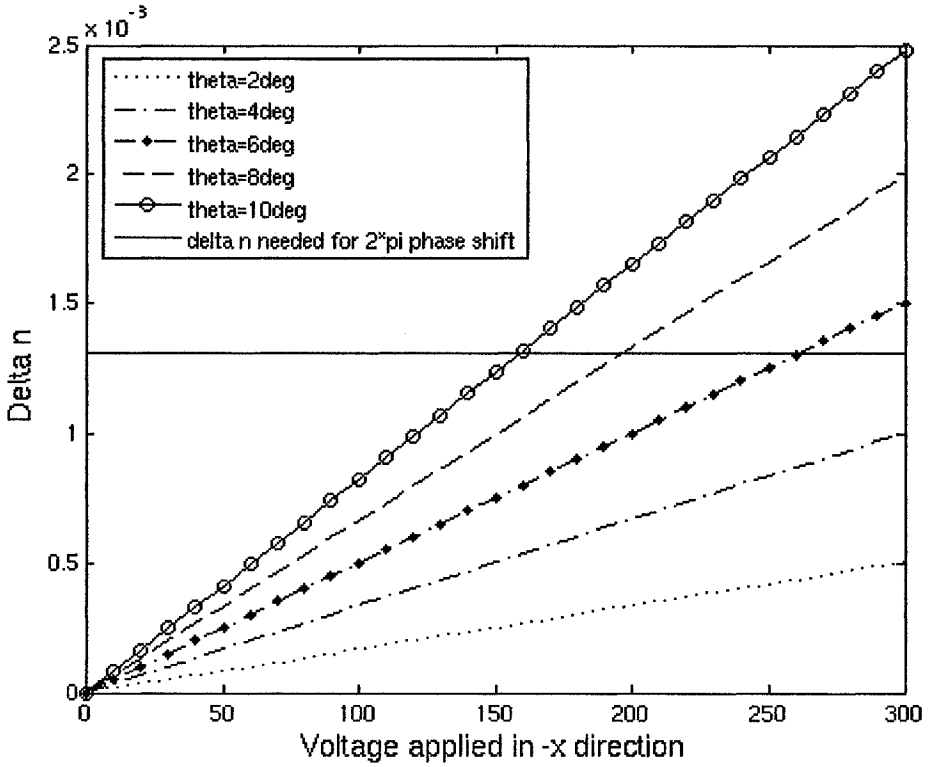


Figure 15. Voltage required to get a 2π phase shift, in transmission mode

The dashed line in Figure 15 above is the change of index required to get a 2π phase shift for light at 1310 nm. For $\theta = 10°$, only a little over 150 V is required. However, one must consider that in the 2-D ROPA design, the crystal is used in reflection mode, not in transmission mode. One would initially think that only half the index change is required since the light is propagating through twice the thickness and would experience the change in index twice. This is in fact not the case. After the light reflects off the electrodes on the bottom of the crystal, the light propagates through the crystal at a different angle with respect to the index ellipsoid, and experiences a different change in index. Consider the same 500 μm thick piece of $BaTiO_3$ crystal with the same orientation but with the light reflecting off the bottom electrodes as shown in Figure 16.

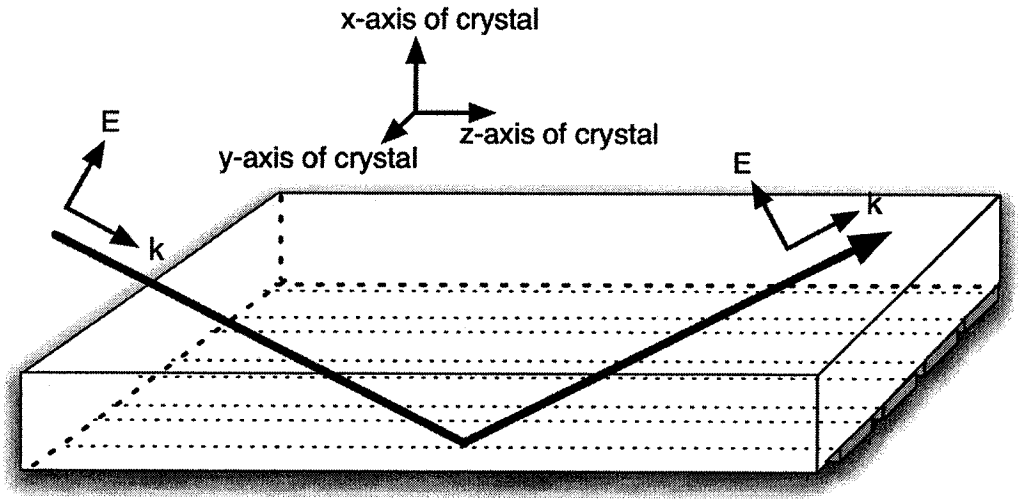


Figure 16. Orientation of electrodes that does not lead to a 2π phase change

For the configuration shown above, the normalized Optical Path Length (OPL) change seen by the light when 300 V is applied to the electrodes, as opposed to when 0 V is applied, is 0.084. To get a 2π phase shift, a normalized OPL of 1 is required. Figure 17 shows the results of a simulation that was run for a grating with a periodicity of 12 electrodes, and with the incidence angle of the light set to 70°. Though the shape of a blazed grating can be seen in the figure, the change in OPL is obviously much too small to create an efficient diffraction grating.

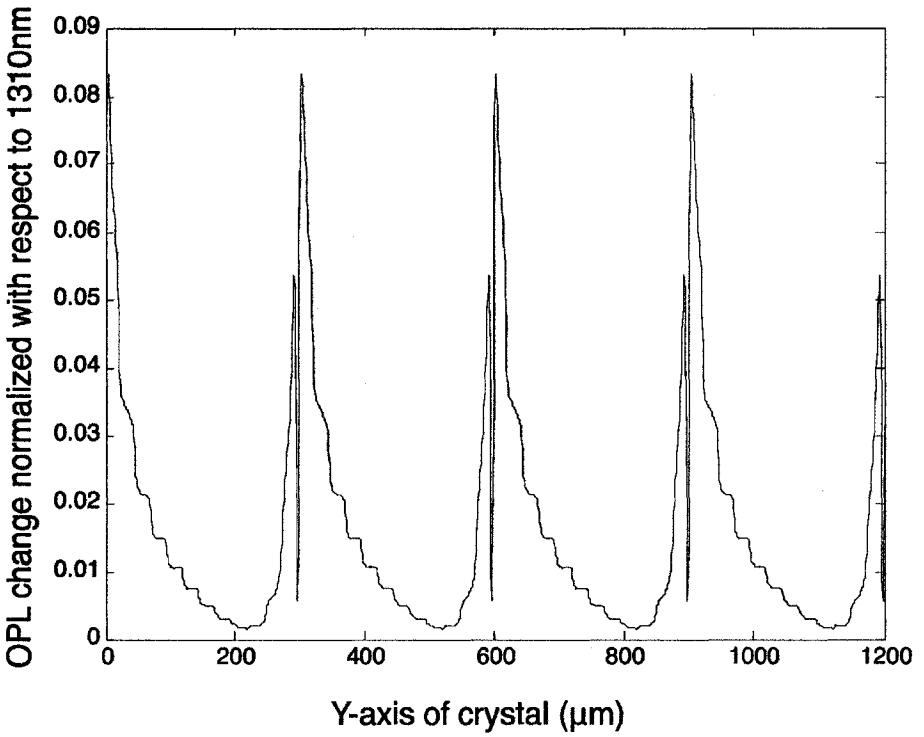


Figure 17. Change in OPL when electrodes have same orientation as reflection plane

However, if the orientation of the electrodes is rotated with respect to the crystal axes, as illustrated in Figure 18, then the situation is much more complex as the light passes over several electrodes and hence through multiple different indices of refraction. The technique used to simulate this more complex situation is described in detail in section 3.2, but to illustrate the impact of rotating the electrodes, an example of the change in optical path length in shown in Figure 19. The normalized change in OPL is obtained when a periodic pattern of four voltages (0, 200, 280, 250 V) is applied to the electrodes and the light is incident at 50° with respect to the normal.

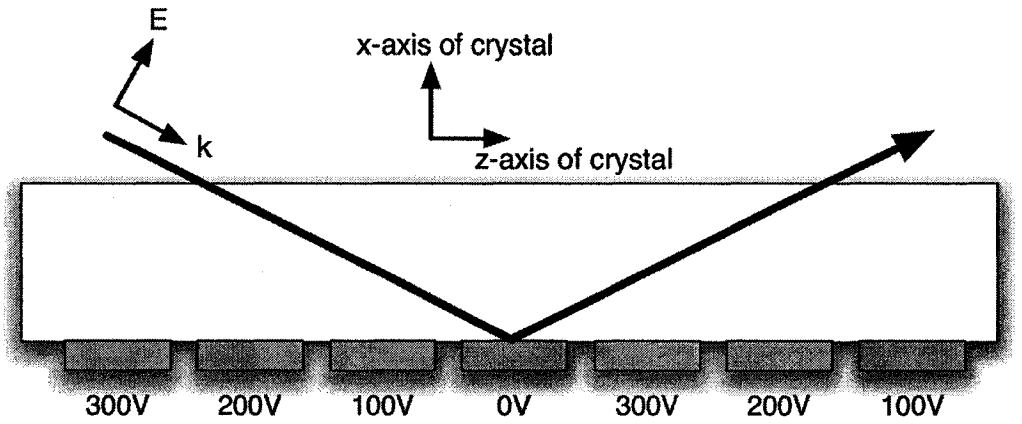


Figure 18. 2-D ROPA device used in TM configuration

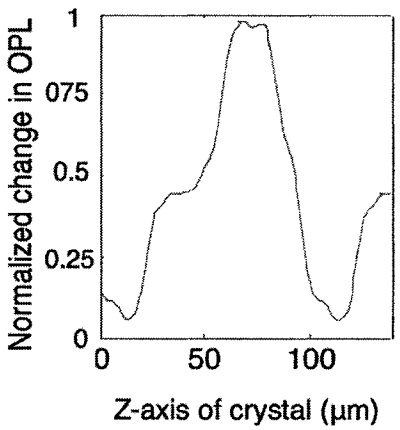


Figure 19. Change in OPL when electrodes are perpendicular to the reflection plane

Therefore, to obtain the desired change in index, the device must operate with light polarized in a TM configuration with the electrodes perpendicular to the reflection plane. It is interesting to note here the reflections obtained off the top surface of the $BaTiO_3$ crystal in such a situation. The Fresnel equations that govern the reflectivity off the top surface of the $BaTiO_3$ crystal are:

$$r_{TE} = \frac{n_{air}\cos\theta_i - n_{crystal}\cos\theta_t}{n_{air}\cos\theta_i + n_{crystal}\cos\theta_t}$$
$$r_{TM} = \frac{n_{crystal}\cos\theta_i - n_{air}\cos\theta_t}{n_{air}\cos\theta_t + n_{crystal}\cos\theta_i} \qquad (3.10)$$

In Figure 20 below, the reflectance is plotted with respect to the incident angle for the air crystal interface for both the TE and TM configurations. By working in the TM configuration near the Brewster angle, the reflectance is close to zero, which reduces the insertion loss of the device.

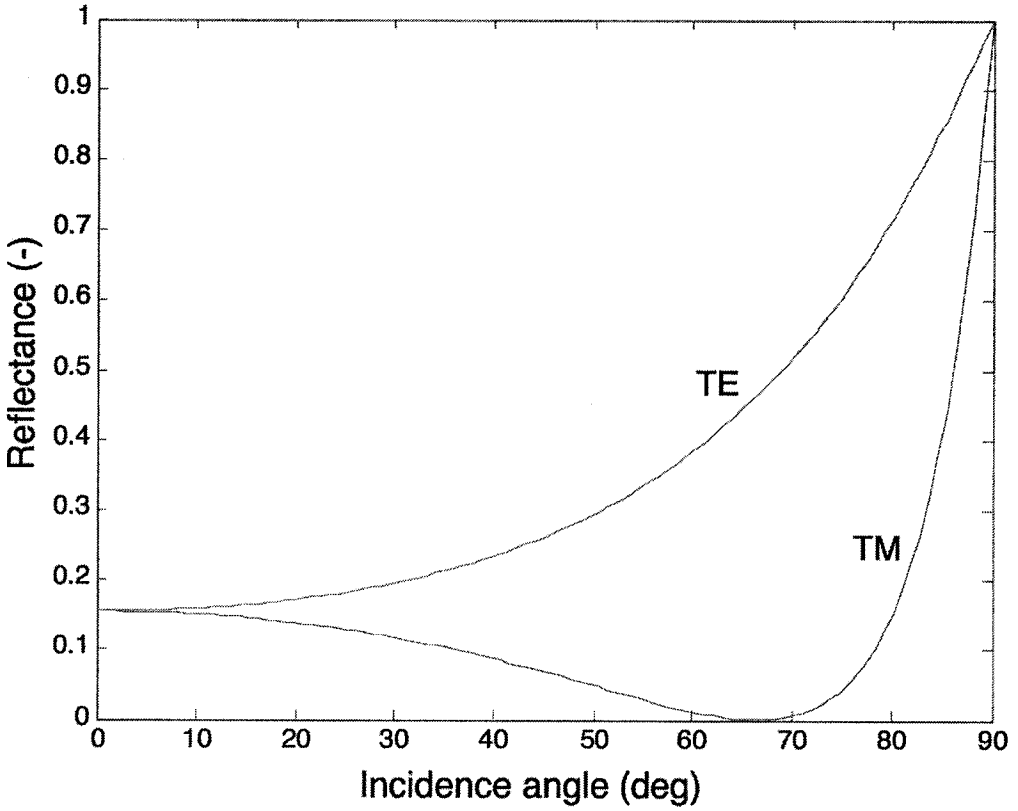


Figure 20. Reflectance of TE and TM waves off top of $BaTiO_3$ crystal

Given the above results, in view of the strength of the r_{51} electro-optic coefficient, the crystal $BaTiO_3$ was chosen as the EO crystal to be used in the 2-D ROPA design. No other electro-optic crystals were found with electro-optic coefficients that allowed for a 2π phase shift with less than 300V applied to the crystal.

Here are some other material properties of $BaTiO_3$ [73], including the transmission wavelengths, which include the entire infrared telecommunications range:

Table 2. Material properties of $BaTiO_3$

Crystal structure	Tetragonal (4mm) **for 13°C<T<125°C**
Growth method	Top seeded solution growth
Cell parameters	a=3.99Å, c=4.04Å (at 26°C)
Melting point	1600°C
Density	6.06 g/cm^3 (at 26°C)
Specific heat	0.527J/g·k (at 300 K)
Thermal conductivity	6 W/m·k (at 300 K)
Thermal expansion	15.7 //a, 6.2 //c ($x10^{-6}k^{-1}$)
Dielectric constant (ε_r)	ε_a=3000, ε_c=800
Hardness (Mohs)	4.5
Index of refraction (at 800nm)	n_o = 2.3681, n_e = 2.3235
Transmission wavelengths	430nm – 6300nm

One significant drawback of using $BaTiO_3$ as the electro-optic material for the switch is that the tetragonal $BaTiO_3$ single crystal will change phase to orthorhombic when the temperature is lower than 13°C, or to cubic when it is higher than 125°C. When it returns to its tetragonal state at room temperature, it has lost molecular polarization and is unusable without re-poling. It is therefore necessary to keep its temperature within the tetragonal range during its processing steps, usage, storage and transportation. The change in the crystalline structure of the crystal for different temperatures is shown in Figure 21 [74].

Related to the change in phase of the crystal is the temperature dependence of the electro-optic coefficients. The graph in Figure 22, taken from [75], shows the temperature dependence of the r_{42} coefficient (or r_{51} coefficient) for $BaTiO_3$, compared to the r_{22} coefficient for $LiNbO_3$. This further reinforces the need for temperature control of the crystal.

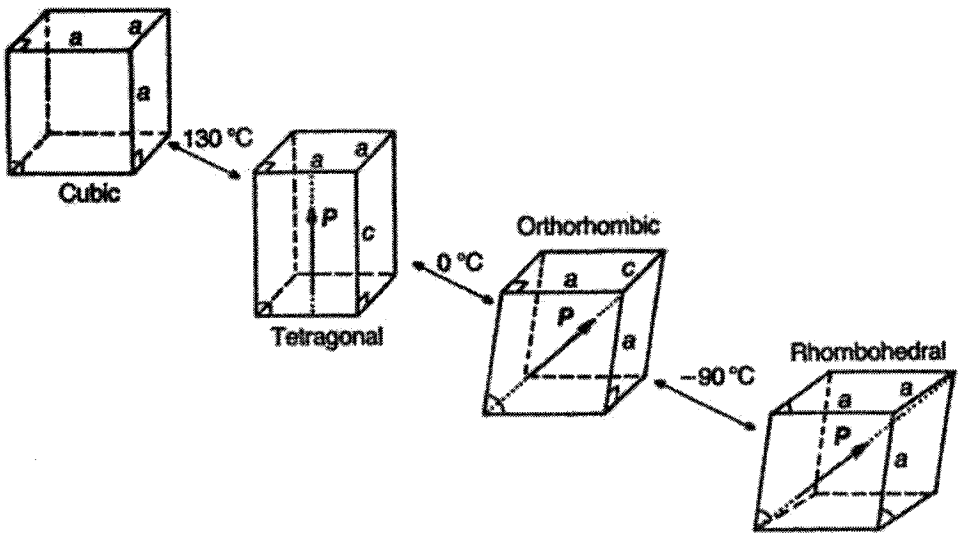


Figure 21. Phase transitions of crystalline structure of $BaTiO_3$

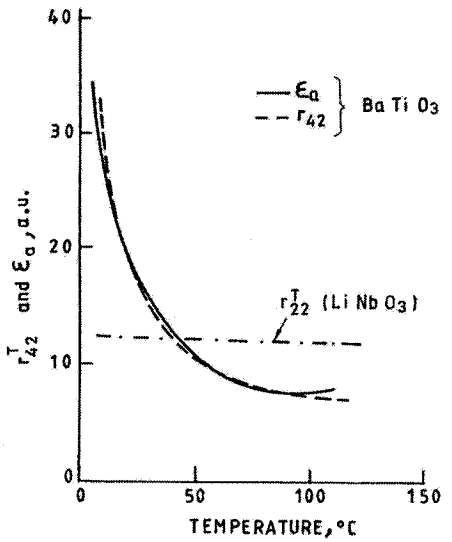


Figure 22. Correlated resonance enhancement of r^T_{42} near 9°C for $BaTiO_3$, and slight nonresonant dependence of r^T_{22} on temperature for $LiNbO_3$ [75]

The other difficulty in working with $BaTiO_3$ is its cost and availability. There are very few suppliers of bulk $BaTiO_3$ crystals and the cost is quite high. To obtain a single 5 mm x 5 mm x 500 μm crystal that has been cut, polished, and poled with the required crystal orientation, the cost ranges from 200$ to 400$ (USD). The lead-time for such a crystal can be as long as 6 months.

3.1.2 EO crystal for the proposed 1-D ROPA design

There are two significant differences when considering an EO material for the 1-D as opposed to the 2-D design. The first is that the E-field of the light is now *parallel* to the applied electrical E-field, as the light is vertically polarized and propagates though the length of the crystal. Therefore, the electro-optic coefficients r_{11}, r_{22}, and r_{33}, now become the most significant coefficients. This makes the choice of EO material much simpler, as the r_{33} coefficient is usually quite strong. The other significant difference is that the electric field is applied across the thickness of the device, whereas the light propagates along the length of the device. As the length is much longer than the thickness, much smaller voltages are required to get a 2π phase shift.

Assuming a linear electro-optic effect (Pockels effect), and given that the E-field of the light propagates in the same direction as the electric field, the resulting index change is:

$$\Delta n = \frac{1}{2} n_e^3 r_{33} \frac{V_{2\pi}}{d} \tag{3.11}$$

where d is the thickness of the device. Recalling that a 2π phase shift is required, and given that L is the length of the device:

$$\lambda = \Delta n L \tag{3.12}$$

Then, substituting (1) into (2) and solving for the voltage,

$$V_{2\pi} = \frac{2\lambda d}{n_e^3 r_{33} L} \tag{3.13}$$

With equation (3.13), the voltage required for a 2π phase shift can be easily calculated for different EO materials with different lengths and thicknesses. If we consider a quadratic electro-optic material (Kerr effect) where the change in index is given by:

$$\Delta n = \frac{1}{2} n^3 s \left(\frac{V_{2\pi}}{d} \right)^2 \tag{3.14}$$

then for the same 1-D configuration we get:

$$V_{2\pi} = d \sqrt{\frac{2\lambda}{n^3 sL}} \tag{3.15}$$

Table 3 below lists some common electro-optic materials and their parameters [71, 76, 77]. All of these materials have a linear electro-optic effect except for PLZT (Lead-Lanthanum-Zirconate-Titanate), which has a quadratic electro-optic effect.

Table 3. Comparison of electro-optic materials

	n_e	r_{13} (pm/V)	r_{33} (pm/V)	s (m^2/V^2)	Curie Temp (°C)	Transparency (nm)
PLZT (8.5/65/35)	≈ 2.5	NA	NA	38.60×10^{-6}	100	1310/1550
PLZT (9/65/35)	≈ 2.5	NA	NA	3.80×10^{-6}	70	1310/1550
$LiNbO_3$	2.2	10	32.6	NA	606	350 - 5000
$LiTaO_3$	2.18	8	33	NA	606	400 - 5000
SBN:61	2.30	37	237	NA	75	370 - 6000
SBN:75	3.32	67	1340	NA	56	350 - 6000
Polymer (Pacific Wave)	≈ 1.5	NA	90	NA	NA	1310/1550

Thought the electro-optic polymer mentioned in Table 3 has a relatively large r_{33} coefficient, it can only be deposited in thin layers onto a substrate and is therefore suitable for a waveguide configuration rather than a bulk device. Using the values given in Table 3 for the remaining EO materials, as well as the equations (3.13) and (3.15), Table 4 was created for the remaining materials.

Table 4. Voltages required for 2π phase shift for a device 3 mm long and 500 μm thick

EO material	Volts (V) for 1310nm	Volts (V) for 1550nm
PLZT (8.5/65/35)	60.2	65.4
PLZT (9/65/35)	192	209
$LiNbO_3$	1327	1570
$LiTaO_3$	1277	1511
SBN:61	141	167
SBN:75	25.1	29.7

Though the PLZT crystals both required low voltages to get a 2π phase shift, they have the disadvantage of having a depolarizing effect on the light when such strong E-fields are applied [78]. The SBN (Strontium Barium Niobate) crystals stand out due to their very high electro-optic coefficients and therefore low voltage requirements. SBN is a photo-refractive material, so it is often used to make holograms and for other non-linear effects such as four-wave mixing. However, its absorptive range is well below infrared wavelengths, and since the intensity of the incoming light is very low ($\approx$ 1 mW) compared to the intensities used in non-linear optics, the electro-optic effect will dominate over the photo-refractive effect. SBN:75 unfortunately has a Curie temperature of only 56°C, compared to 85°C for SBN:61. As mentioned previously, if the crystal is heated above its Curie temperature, it goes through a phase transition and loses molecular polarization.

The electro-optic polymer would be an interesting material for the 1-D design, but since only thin layers can be deposited it would have to be used in a waveguide configuration, leading to large coupling losses to fibers. In order to minimize such losses, the OPA 1-D design uses a bulk crystal, not a waveguide, at least for the time being.

Given these factors, SBN:61 was chosen as the EO crystal to be used in the 1-D ROPA design. As with the $BaTiO_3$ crystal, it is procured cut, polished, and poled. The cost of the SBN crystals is quite high, with a 5 mm x 5 mm x 500 μm crystal costing over 800$ (USD). The lead-time is usually greater than three months.

3.1.3 Processing steps for the electro-optic crystal

The processing of the crystals, both $BaTiO_3$ and SBN, involves cutting, polishing, poling, and then depositing the electrodes. As much as possible, the process that was developed was designed to be the same for both crystal types, to avoid needing to optimize two separate processes.

The cutting and the polishing must be performed before poling, due to the fact that the compressive stress experienced during polishing can induce

reorientation of the 90° domains in the BaTiO3 crystal [79]. Therefore the crystals are first cut to 5mm x 5mm x 0.5mm, then polished. After polishing, temporary metal electrodes are deposited onto the required surfaces of the crystals. The poling electrode locations are shown in the figures below. In both cases the crystals are poled along their z-axis. The poling electrodes are a silver conductive epoxy, removable with acetone.

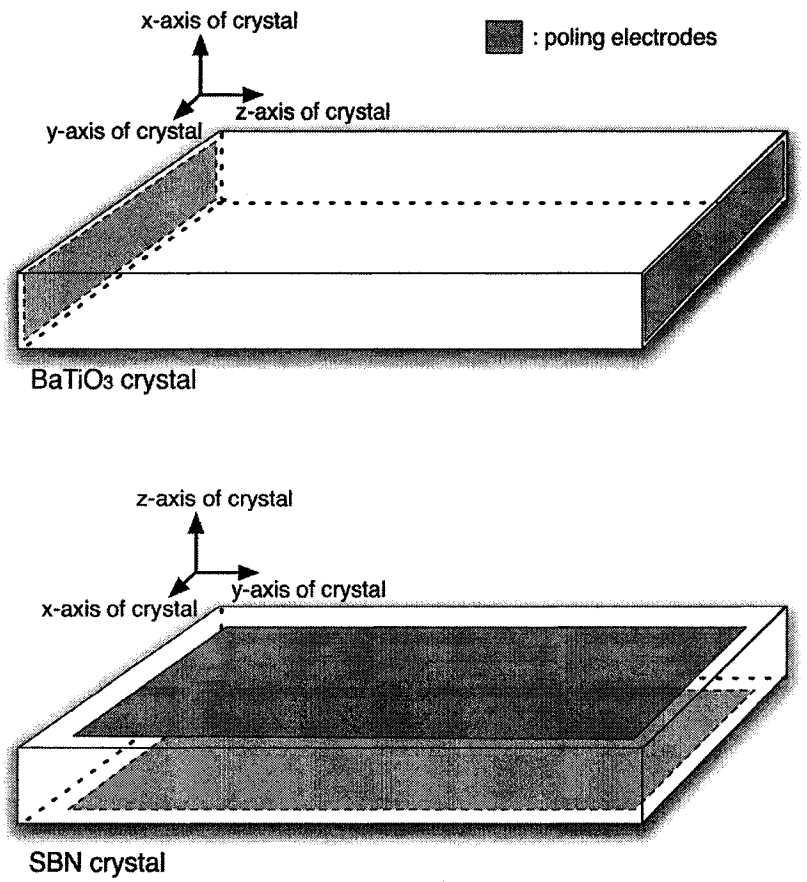


Figure 23. Poling electrode locations for both $BaTiO_3$ and SBN crystals

The poling of the $BaTiO_3$ crystal is performed by applying an electric field of 1.5 kV/mm, while slowly decreasing the temperature from 135°C to room temperature [79]. The SBN crystal was poled at room temperature with an electric field greater than 2.4 kV/cm [80].

After poling, the poling electrodes are removed and the final electrodes are deposited onto the crystal. The electrodes need to adhere to the crystal, to be compatible with the flip-chip process, and to be highly reflective at 1310 nm. The

reflectivity requirement is only needed for the 2-D design, but for simplicity the same electrode deposition process is used for both ROPA designs. Aluminium (Al) is highly reflective at telecom wavelengths (97% at 1310 nm), but unfortunately does not adhere well to the EO crystals. Therefore, a thin layer of titanium (Ti) is necessary between the crystal and the Al electrode. This layer reduces the reflectivity of the electrodes, so it is chosen to be as thin as possible, i.e. 50 Å. In order to be compatible with flip-chipping, a thick layer of gold (>3000 Å) needs to be deposited as the top layer of the electrodes. A second layer of Ti is necessary to act as a barrier layer between the Al and the Au layers. The final stack-up of the electrodes is Ti/Al/Ti/Au with thicknesses of 50/500/500/6000 Angstroms respectively. Figure 24 and Figure 25 below show the variation in reflectivity as the Ti adhesion layer thickness is varied [81]. As can be seen in the figures, for a Ti thickness of 50 Å, the reflectivity of the electrodes is 90% at 1310 nm, and it is 89% at 1550 nm. The process used to deposit these metal layers is described in greater detail in section 5.1.

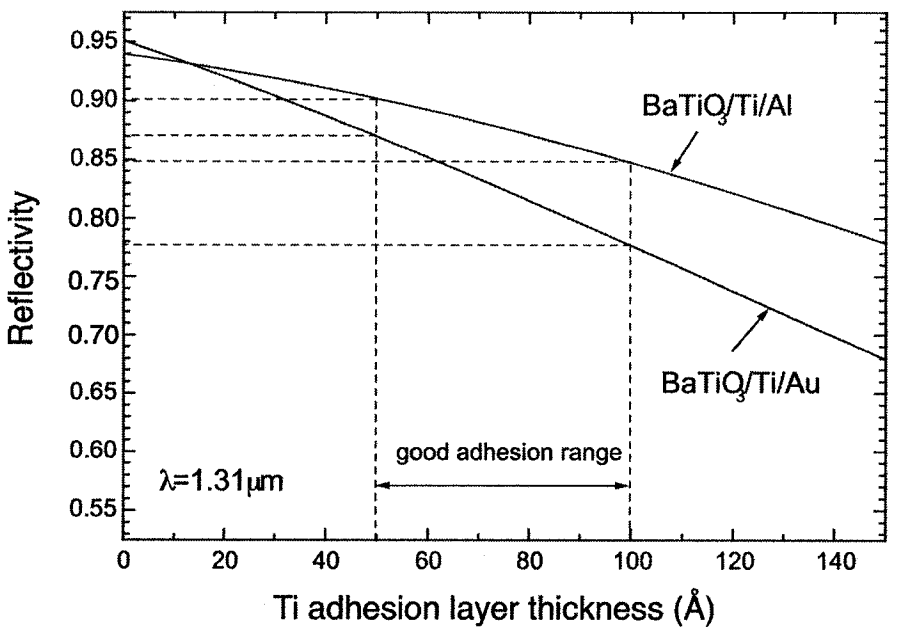


Figure 24. Reflectivity as a function of the adhesion layer thickness at 1310 nm

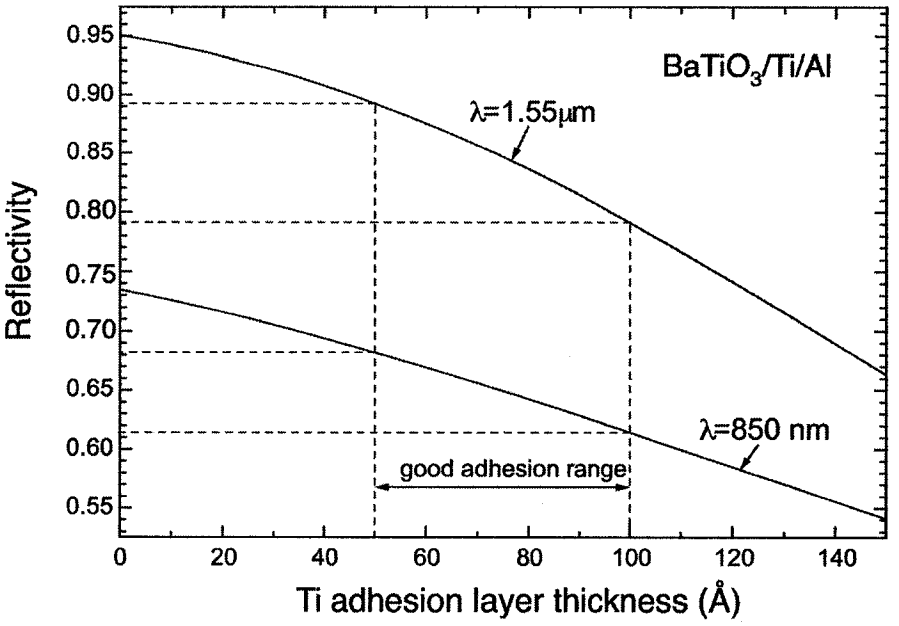


Figure 25. Reflectivity as a function of the adhesion layer thickness at 1550 nm

When considering the spacing between the electrodes there are conflicting requirements. To maximize the diffraction efficiency, there would ideally be no gap between the electrodes at all. However, a large enough electrode spacing is required to ensure that there will be no voltage breakdown between the electrodes. If one considers the phenomena of gaseous breakdown voltage versus gap spacing, then according to the Paschen curve [82] there will be no breakdown regardless of gap spacing as long as the voltages are kept below 360 V. The mechanism that governs the Paschen curve is the Townsend avalanche within an ionized gas. Indeed, there is no gaseous breakdown at regular air pressure below 360 V, but for small dimensions there can be electron field emission that can lead to voltage breakdown at lower voltages. The electrode spacing that is at the transition point between the two phenomena is 5 μm. If the spacing is further shrunk to dimensions smaller than 2 nm, then tunneling of electrons can become significant. Experiments were performed by [83] and [82] to determine the breakdown voltage for micron scale electrode spacings. In both cases, a voltage breakdown of 300 V is obtained for spacings ranging from 1.5 to 3 μm. Since the ROPA devices operate at voltages up to 300 V, the spacing between the electrodes was designed to be 5 μm.

When defining the width of the electrodes, again there are conflicting requirements. To get the largest possible control over the optical performance of the device, very narrow electrodes would be used with a correspondingly small period. However, the pitch of the electrodes defines the pitch of the flip-chip points between the EO crystal and the high-voltage chip. Additionally, the width of the electrodes defines the width of the flip-chip bumps. Figure 26 below illustrates the layout of the electrodes and the flip-chip points. In the center of the figure, we can see the 64 electrodes that are each 3 mm long and 20 μm wide on a pitch of 25 μm. With this electrode configuration, the electrodes provide a coverage of 80%. This coverage will be taken into account when measuring the reflectivity of the electrodes in section 5.1.

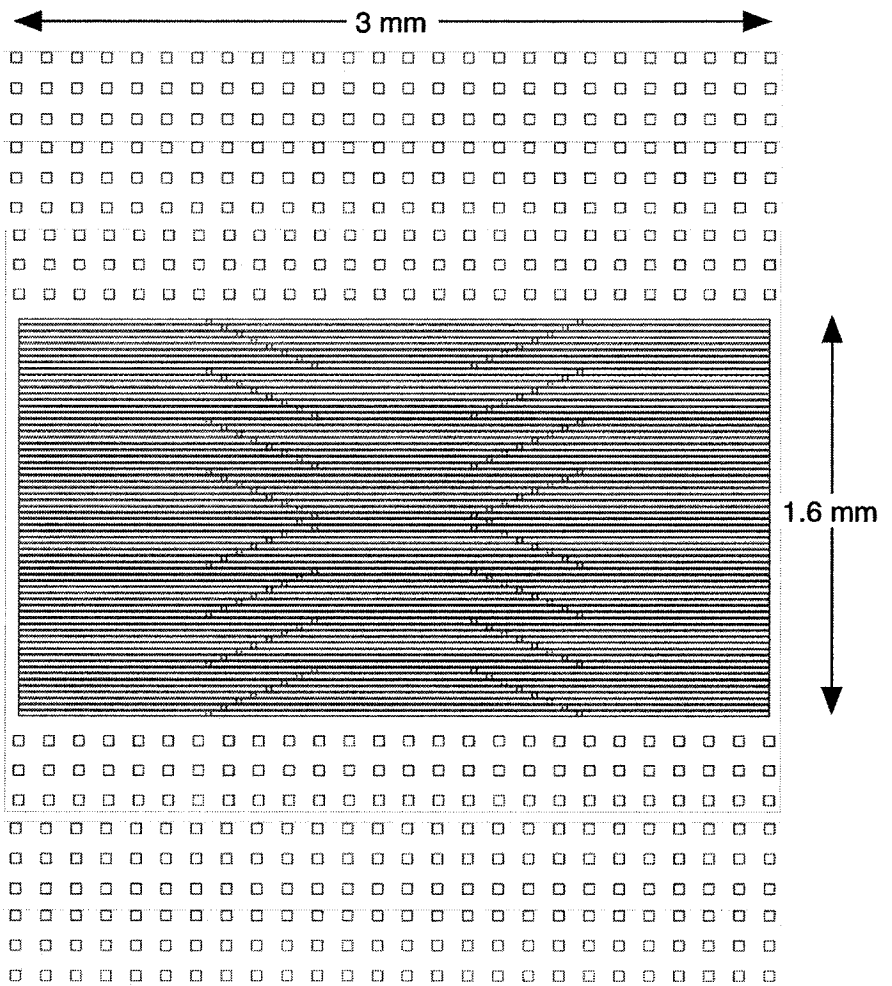


Figure 26. Pattern of electrodes and flip-chip points

Each flip-chip bump connecting the electrode to the high-voltage chip is 20 μm x 20 μm. In Figure 26 above, the flip-chip bumps are represented as little squares underneath the 64 long electrodes in the center of the figure. In order to minimize the chance of shorting between the flip-chip bumps, they are horizontally distributed across the electrodes. There are two flip-chip points for each of the 64 electrodes for redundancy, in case one of the bumps fails. Above and below the 64 electrodes, there are large arrays of electrodes that are 40 μm x 40 μm. These electrodes will also be used as flip-chip points to the high-voltage chip and will be grounded. Their purpose is mostly to provide extra flip-chip points for greater mechanical strength and stability between the crystal and the high-voltage chip.

The other side of the electro-optic crystal, the top side, must have a large ground electrode deposited on it. If the device is used in the 1-D configuration, then an ordinary metal electrode is fine. If the device is used in a 2-D configuration, than an Indium-Tin-Oxide (ITO) electrode must be used [84, 85]. This type of electrode is transparent to infrared wavelengths. Possible ways to ground the top electrode include wirebonding, and gluing a wire with conductive epoxy.

3.2 Optical simulations

The simulation of both the 2-D and the 1-D design is critical in predicting the behavior of the final devices. As well as calculating the diffraction efficiencies of the devices it is important to determine the number of resolvable spots, as this limits the number of possible output ports.

3.2.1 Simulation techniques

The method used to simulate the ROPA device is Rigorous Coupled Wave Analysis (RCWA). RCWA is a rigorous electro-magnetic modeling technique [86, 87]. As opposed to the scalar approach, RCWA can fully solve the electro-magnetic problem in the case of grating diffraction. Given a periodic structure and a plane wave incident source condition, RCWA divides the structure into a

series of vertically homogeneous layers. The technique decomposes the index distribution in each layer using a series of spatial harmonics. The electro-magnetic field distribution is then solved for each of the layers, and a propagation matrix is applied to the layer set. Using the boundary condition at each layer interface, the electro-magnetic problem is then solved for the periodic structure, and a series of reflected and transmitted diffraction efficiencies is produced. The method can be implemented in two and three dimensions and can account for incident wave polarization. Although the method allows for a fully anisotropic (bi-axial) material definition, most common implementations of the technique require the use of an isotropic material. Adapting one of these implementations to deal with the uniaxial properties of the materials used for the ROPA device will be discussed in section 3.2.3 (for the 2-D ROPA case) and section 3.2.4 (for the 1-D ROPA case).

Additionally, since the voltages on the electrodes can be tuned to optimize the diffraction efficiency of the device, a custom iterative thermal annealing method was developed, to be used in conjunction with the commercial RCWA software. The efficiency of the desired diffraction order is the merit function and the variation of the voltages on the electrodes is linked to the simulated annealing temperature parameter.

3.2.2 Switch deflection angles

The gratings that are produced using the ROPA designs are first order multilevel gratings. The voltages that are applied to the electrodes define the periodicity of the grating. Using scalar theory [88], and the grating equation:

$$d \sin \theta_m = m\lambda \tag{3.16}$$

and if we assume the electrodes are 25 μm wide with no gaps between them, then the following table can be generated:

Period (in μm)	# of levels in grating	Deflection angle @1310 nm	Deflection angle @1550 nm	Efficiency η
50	2 (binary)	±1.50°	±1.78°	40.5%
75	3	1.00°	1.18°	68.4%
100	4	0.75°	0.89°	81.1%
125	5	0.60°	0.71°	87.5%
150	6	0.50°	0.59°	91.2%
175	7	0.43°	0.51°	93.5%
200	8	0.38°	0.44°	95.0%
225	9	0.33°	0.39°	96.0%
250	10	0.30°	0.36°	96.8%

Table 5. Scalar properties of multi-level gratings

It is important to note that since the blazed angle can be created in either direction and assuming the incoming light has a normal incidence angle, the angles of possible deflection will actually be ± θ. So, if the electrodes are 25 μm wide, then for a 4-level grating the deflection angles will be ± 0.75° at 1310 nm.

Given these results, placing the electrodes on a 25 μm pitch (20 μm electrodes with a 5 μm gap between them) gives reasonable deflection angles in view of building an optical switch. If one always assumes at least 3 levels will be used to create the grating but no more than 10 levels, then potentially 14 output spots can be generated (7 in each direction). However, in order to determine whether or not all of the spots are resolvable, the angular spectrum of the incident wave must be considered, as well as the non-infinite periodicity of the grating.

The finite number of periods in the ROPA device results in a larger angular width of the diffracted order angles. In our case, the number of periods is dependent on the periodicity of the grating, i.e. the number of electrodes used per period. Additionally, the RCWA simulations assume plane wave incidence, whereas the incident beam for the 2-D ROPA device is a Gaussian beam with a waist of 640 μm. The incident beam for the 1-D ROPA at the crystal plane is an elliptical Gaussian beam with a vertical waist of 100 μm and a horizontal waist of 700 μm. In terms of calculating the number of resolvable outputs, the horizontal

waist of the beam is the one of interest as the deflection of the beam is in the horizontal direction. However, as the waist for the 2-D ROPA is smaller than the horizontal waist for the 1-D ROPA, it has a larger divergence angle and is the therefore the one used to calculate the number of resolvable spots.

Taking both the finite number of periods and the smaller Gaussian beam waist into account yields the angular beam width ($1/e^2$) shown in Table 6 below, where θ is the angle of diffraction given by the scalar grating equation.

Table 6. Angular beam width for finite periods and incident Gaussian beam

# of electrodes per period	Period of grating	# of periods	θ	Angular beam width
8	**200μm**	**8**	**0.59°**	**0.48° to 0.70°**
7	175μm	9	0.67°	0.56° to 0.78°
6	150μm	10	0.78°	0.67° to 0.90°
5	**125μm**	**12**	**0.94°**	**0.83° to 1.06°**
4	100μm	16	1.18°	1.07° to 1.29°
3	**75μm**	**21**	**1.58°**	**1.47° to 1.70°**

In order to minimize crosstalk, a 1×6 switch is realized by tuning the electrode voltages for either the +1 or -1 orders, for a grating consisting of 3, 5, or 8 electrodes per period. The corresponding entries in the table are shown in bold. The 0^{th} diffraction order is not used for the switch, as that output port would suffer from high crosstalk. This is especially true when switching light to the 1^{st} order using only 3 electrodes per period, as that is the configuration that suffers from the lowest diffraction efficiency.

3.2.3 Simulation of 2-D ROPA device

In order to simulate the optical performance of the ROPA we exploit the quasi-periodic nature of the device by using the rigorous coupled wave analysis (RCWA) technique [86]. In addition to the conventional implementation of RCWA, we have developed a novel iterative modeling algorithm for uniaxial periodic electro-optics materials. This algorithm, described in the following sections, involves calculating and segmenting the index profile of the crystal,

determining the diffraction efficiency of the grating, and then using a simulated annealing technique to iteratively tune the electrode voltages to improve the diffraction efficiency.

Determining refractive index profile

Electrode voltages are applied as boundary conditions to the electro-optic crystal and the electric field distribution is subsequently computed using a finite-difference modeling method. The region between the top and bottom electrodes of the crystal is meshed into a 1 μm grid, and an initial voltage distribution is assumed for each point in the mesh. Then a new voltage is calculated for each point in the mesh based on the average value of its neighbors. This is done iteratively until every voltage value in the mesh has stabilized. From the mesh of voltages, a mesh of electric field values is computed.

Once the electric field distribution has been found, the resulting indices of refraction are calculated at each point in the crystal using the electro-optic tensor, for a given optical path through the material. Due to the anisotropic nature of the crystal, the index sampled by light once reflected from the bottom electrodes will be different from that before reflection. In order to circumvent this added difficulty in the subsequent simulations, the post-reflection path through the structure is unfolded in the model yielding a pure transmission structure, through which light propagation is unidirectional. The unfolded index profile for a single grating period consisting of 4 electrodes (a period of 100μm), with voltages 0, 100, 200, and 300V, is shown in Figure 27 below.

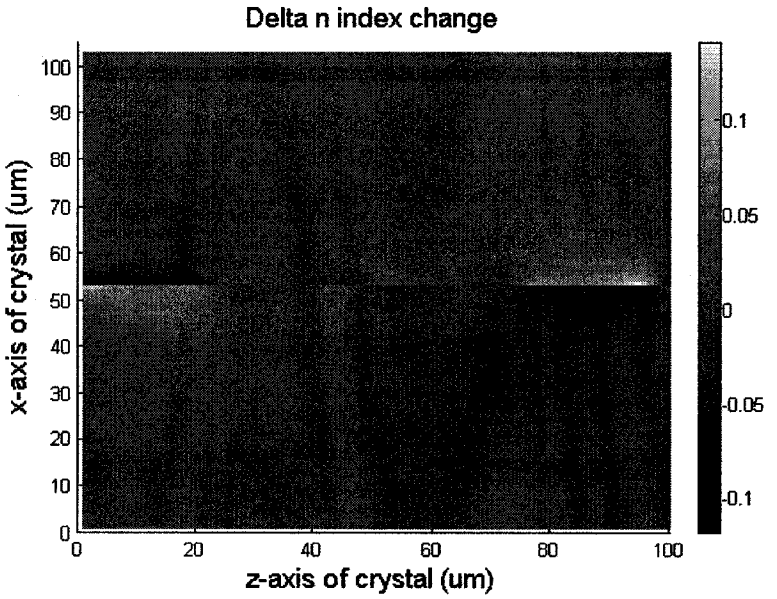


Figure 27. Index change (Δn) of center of unfolded $BaTiO_3$

Segmentation of index profile

The computed index profile for the unfolded structure is transferred into a two-dimensional rigorous coupled wave analysis (RCWA) algorithm. This index profile is segmented in both spatial directions into segments of uniform index. The number of segments in both the vertical and horizontal directions depends on the index profile, such that there are more segments in areas of larger index variation. Care is taken to ensure that for a given number of segments the computation is convergent. The transmission efficiencies of the structure are obtained in the RCWA.

Optimization of diffraction efficiencies

In order to optimize the voltages applied to the structure, the entire model is executed in a simulated annealing (SA) optimization process [89]. This optimization uses the efficiency in the desired order as the merit function with the voltage variation linked to the SA temperature parameter. The initial voltage distribution across the electrodes is chosen to be a linear distribution from 0 to 300 V. The SA optimization can be applied to all of the electrodes

simultaneously or to one electrode at a time, and this can be done repeatedly for a further refinement of the design. Figure 28 below shows the optimization of the diffraction efficiency of the 1st order over 240 iterations for a period of 3 electrodes (75 μm).

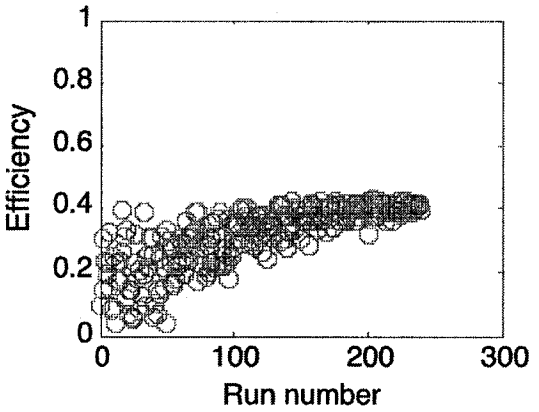


Figure 28. Optimazation of diffraction efficiency

Figure 29 shows the simulated optimal diffraction efficiencies of the ROPA device, working at 1310 nm, which range from 37% to 63%. The x-axis indicates the number of electrodes in one period of the grating. As the number of electrodes increases, the ability to tailor the profile of the grating increases, leading to greater diffraction efficiencies. However, an increasing period leads to a reduction in the deflection angle. When using 3 to 8 electrodes per period, the deflection angles range from ±0.38° to ±1.0° about the zero order reflection. For a crystal thickness of 500 μm, the voltage needed for a 2π phase shift is 295 V. When working at 1550 nm, as shown in Figure 30, the diffraction efficiencies range from 39% to 62%, but the required maximum voltage is 355 V.

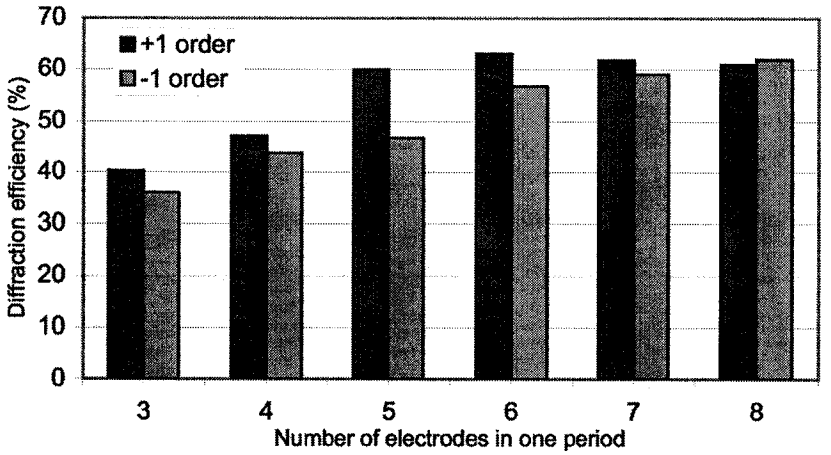


Figure 29. Diffraction efficiencies of 2-D ROPA at 1310 nm

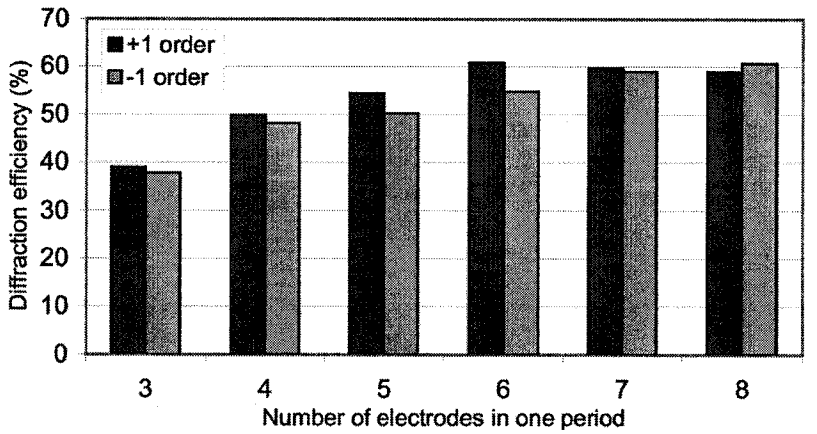


Figure 30. Diffraction efficiencies of 2-D ROPA at 1550 nm

As can be seen in the figures above, the diffraction efficiencies for the +1 order mode are slightly higher than for the –1 order mode. This is due to the fact that the light is not normally incident to the crystal but has an angle of 50°, which breaks the symmetry of the device.

3.2.4 Simulation of 1-D ROPA device

The algorithm used to simulated the 1-D ROPA device is similar to the one used for the 2-D ROPA. First, the electric-field distribution is calculated within the crystal using the same finite-difference modeling method. Then the resulting changes in the indices of refraction are calculated at each point in the crystal using the following expression:

$$\Delta n = \frac{1}{2} n_e^3 r_{33} E \tag{3.17}$$

where E = electrical field at each mesh point = V/m

n_e = extraordinary index of refraction = 2.30

r_{33} = electro-optic coefficient = 237 pm/V

Calculating the index of refraction is simpler for the 1-D ROPA device than for the 2-D device, as there is no reflection within the device and the light passes straight through the device parallel to the electrodes. There is therefore a single index of refraction instead of two for each point within the crystal for the incoming vertically polarized light. An example of the distribution of the potential through a vertical cross section of two periods of the induced grating is shown in Figure 31 below. In this figure, each period comprises four electrodes with the following voltage distribution: 300 V, 200 V, 100 V, 0 V. The top electrode of the device is grounded.

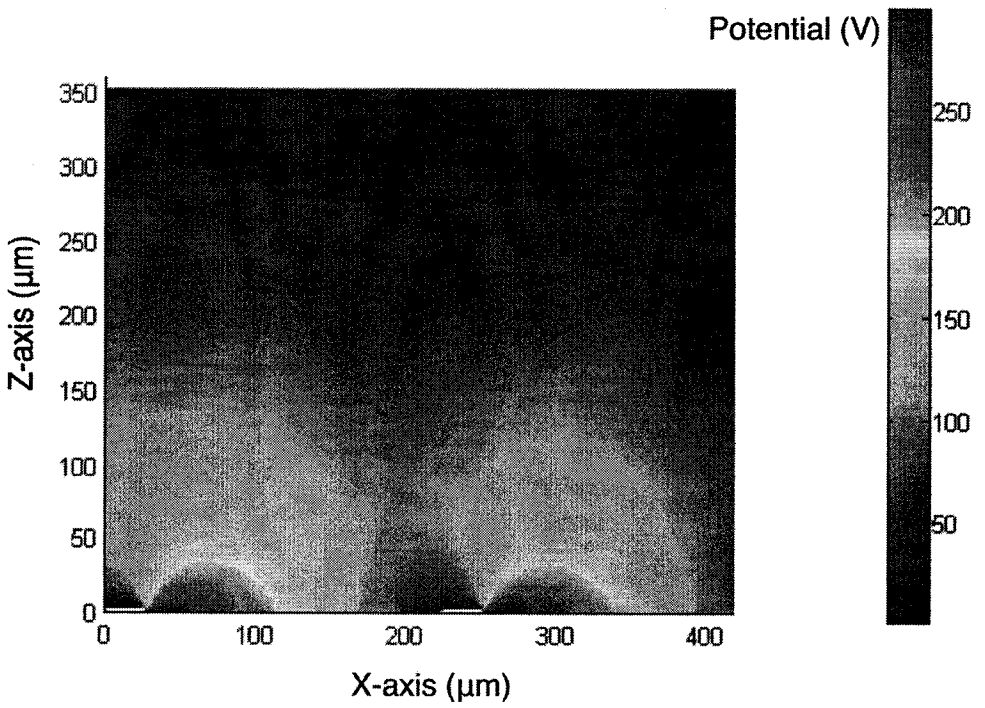


Figure 31. Potential distribution through the lower 350 μm of an SBN crystal

Once the index of refraction is found for each point within the crystal, this index profile is segmented in both spatial directions into uniform index segments. Because the index profile is smooth and continuous, and due to the sheer size of the device in terms of number of wavelengths, a two-dimensional implementation was chosen. That is to say, the three-dimensional problem is solved in two-dimensional slices, and a Gaussian overlap integral is applied to calculate the overall diffraction efficiency. The two-dimensional simulations are performed one at a time on a horizontal slice (5 μm thick) along the z-axis of the crystal. An illustration of the slice used in the simulation is shown in Figure 32 below.

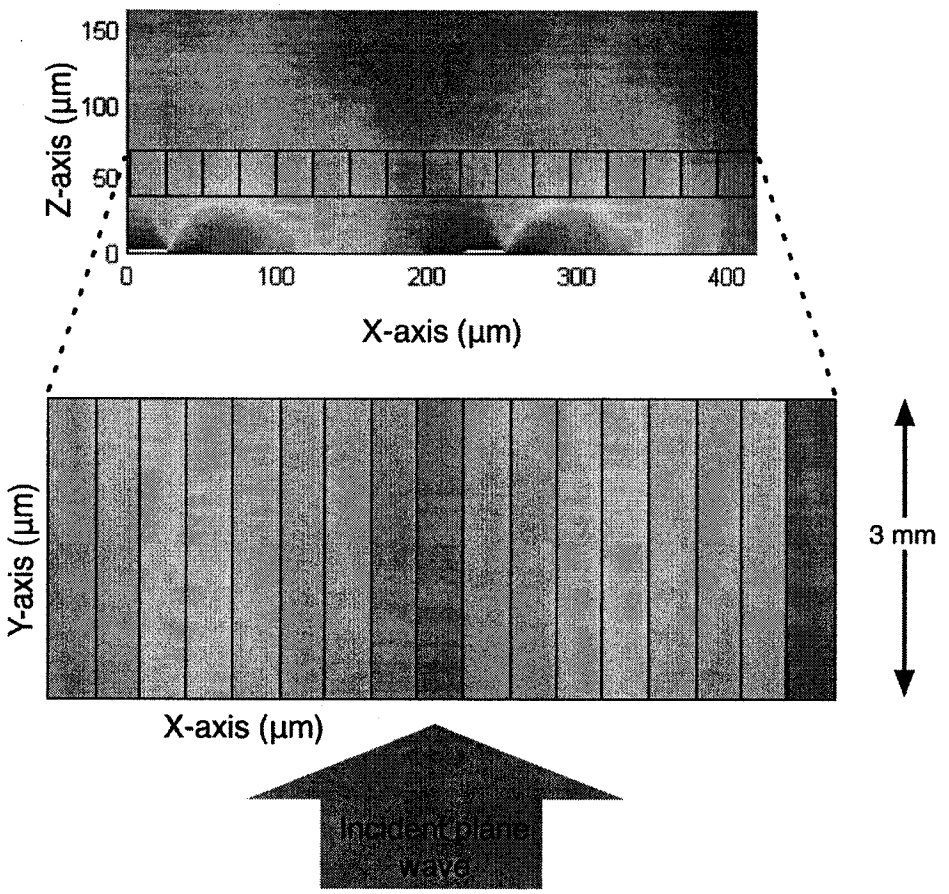


Figure 32. Simulation of a single horizontal slice of the index profile of the crystal

Figure 32 is somewhat misleading in that it shows the horizontal segmentation of the index profile to be uniform. In fact, the segmentation

algorithm increases the number of segments in areas where there is a large index change, and uses larger segments in areas of almost continuous index profile.

The thermal annealing algorithm is used to optimize the voltage distribution across the electrodes while using the efficiency of the slice corresponding to the center of the input beam location as the merit function. This horizontal slice is referred to as the primary slice. Table 7 below shows the diffraction efficiencies for the primary slices of the 1-D ROPA device, at both 1310nm and 1550 nm.

Table 7. Optimized diffraction efficiencies for the primary slice of the crystal

Number of electrodes per period	1310 nm diffraction efficiency	1550 nm diffraction efficiency
3	22.59%	21.82%
4	24.25 %	26.11%
5	31.64%	33.29%
6	46.55%	45.96%
7	48.85%	49.20%
8	47.52%	48.2%

There are two main factors contributing to the relatively low diffraction efficiencies. First, unlike the 2-D ROPA situation where the light is incident at an angle close to the Brewster angle, in the 1-D ROPA case there are significant Fresnel reflections at both surfaces of the SBN crystal. Recalling that the extraordinary index of refraction for an SBN:61 crystal is n_e=2.3 :

$$\text{Total reflection} = 2 \times \left(\frac{n_e - n_{air}}{n_e + n_{air}} \right)^2 = 2 \times \left(\frac{2.3 - 1.0}{2.3 + 1.0} \right)^2 = 31\% \qquad (3.18)$$

Therefore, if an ideal grating were induced within the crystal, the diffraction efficiency would be at best 69% if no anti-reflection coating were used on the crystal. This corresponds to a minimum insertion loss of 1.61 dB.

The second reason for the lower diffraction efficiencies is that the light propagates roughly through the center of the crystal, whereas most of the index change is near the electrodes as can be seen in Figure 31. In the 2-D ROPA situation, the light reflects off the electrodes, and therefore benefits from the relatively high changes in index of refraction near the electrodes.

Once the voltages have been optimized for the center slice, the diffraction efficiency of every slice within the crystal is calculated. In Figure 33 below, the simulated diffraction efficiencies for the 100 horizontal slices of a grating with a periodicity of four electrodes are plotted (each slice is 5 μm thick for a total crystal thickness of 500 μm).

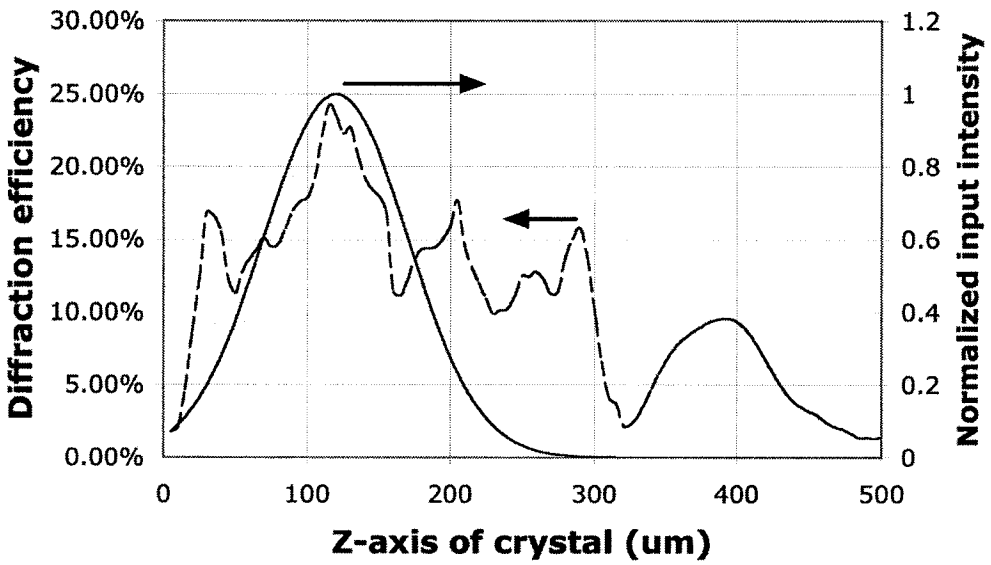


Figure 33. Diffraction efficiency for each slice across the thickness of the crystal

The dashed curve plots the diffraction efficiencies calculated for the individual slices, and the black curve represents the input profile of the Gaussian input beam. The beam is defined to have a vertical beam waist of 100 μm, and as is shown in Figure 33, does not propagate through the exact center of the crystal. In order to maximize the diffraction efficiency, the beam propagates as close to

the electrodes as possible, while not introducing too much loss through beam clipping. The center of the beam is assumed to be 120 μm above the electrodes.

In order to estimate the total diffraction efficiency for each periodicity of the 1-D ROPA device, an overlap integral is applied between the Gaussian beam and the diffraction efficiencies obtained for the slices. The resulting total 1st order diffraction efficiencies are given in Table 8 below.

Table 8. Total simulated diffraction efficiencies for the 1-D ROPA device

Number of electrodes per period	1310 nm diffraction efficiency	1550 nm diffraction efficiency
3	16.31%	15.74%
4	16.96%	17.12%
5	17.44%	17.86%
6	19.38%	18.65%
7	21.21%	22.63%
8	19.34%	21.63%

Unlike the 2-D ROPA case, there is no difference in diffraction efficiency for the +1 and –1 diffraction orders, since the incident input beam is normal to the crystal surface creating a perfect symmetrical case for the two diffraction orders.

Similar to the 2-D ROPA situation, the voltages required for to maximize the diffraction efficiency at 1550 nm go as high as 315V. The 1-D ROPA device is therefore tunable around 1310 nm with the current design.

3.3 Summary

The electro-optic crystals that were chosen for the ROPA device were $BaTiO_3$ for the 2-D configuration, and SBN for the 1-D configuration. Both of these crystal types have high enough electro-optic coefficients in the desired crystal axis that a potential of 300V can introduce a 2π phase shift in 1310 nm incident light. In the 2-D ROPA situation, the change in index is related to the incidence angle to the top face of the crystal. In order to maximize the change in

index and minimize the reflections off the top surface of the crystal, the angle of incidence is chosen to be close to the Brewster angle. For both these crystal types, the index of refraction is temperature dependent, which means that the ROPA device will need to be temperature controlled.

For the 2-D ROPA device, the metal electrodes that are deposited onto the crystal need to be highly reflective at telecom wavelengths, need to adhere to the crystal, and need to be compatible with the flip-chipping process. The electrode stack-up that satisfied all of these requirements was Ti/Al/Ti/Au with thicknesses of 50/500/500/6000 Angstroms respectively. For simplicity when processing the crystals, the same metal stack-up is used for the 1-D ROPA device, though the reflectivity is no longer required in that configuration.

When defining the dimensions of the electrodes, there are competing requirements. In order to maximize the reflectivity of the device, the smallest possible gap between the electrodes would be ideal. However, to prevent arcing a large enough gap must exist between the electrodes. To satisfy these requirements, a gap of 5 μm was defined. Similarly, in order to maximize the control over the optical performance of the device, a small pitch for the electrodes would be required. However, in order to be compatible with the flip-chipping process, the electrodes must be large enough to contain the flip-chip bumps used to bond the electrodes to the high-voltage chip. An electrode width of 20 μm was thus defined.

Once the electrode dimensions were defined, the output deflection angles were calculated. In order to minimize crosstalk, at most an 1×6 switch can be realized by tuning the electrode voltages for either the +1 or -1 orders, for a grating consisting of 3, 5, or 8 electrodes per period.

In order to simulate the performance of the devices, rigorous coupled wave analysis was used in conjunction with an iterative simulated annealing technique to optimize the performance of the devices. For the 2-D ROPA device, diffraction efficiencies range from 37% to 63% and for the 1-D ROPA device, the diffraction efficiencies range from 16% to 21%.

CHAPTER 4. HIGH-VOLTAGE CMOS CHIP

The ROPA device comprises two distinct parts that are flip-chipped together: the EO crystal and the CMOS chip used to control the voltages on the electrodes. The previous chapter focused on the design issues surrounding the EO crystal and the simulations of the optical performance of the electrically induced diffraction grating. This chapter deals with the design challenges and simulations of the CMOS chip [90].

For the electric control of the ROPA device, a key enabling technology is a new chip process developed by DALSA Semiconductor. It is the C08G quadruple well, three metal layer, epitaxial silicon process. This process combines 0.8 μm low-voltage transistors with high-voltage transistors on the same chip [16]. System integration of high-voltage and low-voltage digital circuitry on a single die is desirable for many applications besides optical switching, such as biomedical applications and plasma display drivers [8, 91-94]. In all of these cases, using a single die for all the electrical circuitry results in reliability, cost, and size improvements.

For the ROPA device, the main design requirement for the chip is that it be able to produce 64 independent voltages ranging from 0 to 300 V. The circuitry therefore consists of a fully integrated array of 64 high-voltage Digital-to-Analog Converters (DACs) independently operating up to 300 V [17, 21]. To our knowledge, this is the first time such a design has been attempted in this process.

4.1 High-voltage chip technology

Double Diffused Metal Oxide Semiconductor (DMOS) transistors are the most popular means of obtaining high-voltage integrated circuits. In order to combine low-voltage and high-voltage circuitry on the same chip, a technique called RESURF (REduced SURface Field) allows drain breakdown voltages of up to 600V [16, 95]. In an n-type DMOS device as shown in Figure 34, a lightly

doped P-Top region inside the N-Well is used in-between the P-base and the drain in order to withstand the high drain-source voltage. For high drain voltages, the P-Top region will deplete as the N-Well region depletes [95].

These high-voltage transistors have certain specifications that influence the design choices. The main parameter to affect the design is V_{GS}. For N-type transistors, the breakdown voltage is 15 V (nominally 5 V) whereas for a p-type transistor, the V_{GS} must be larger than –16 V (nominally –5 V). Thus, assuming a p-type device attached to a 300 V supply, its gate voltage will have to be between 295 V and 300 V. This becomes an important design challenge, as conventional current-to-voltage conversion using op-amps is no longer a straightforward approach. This is discussed in more detail in section 4.2.3.

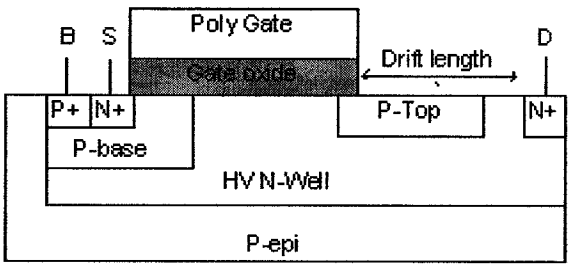


Figure 34. Cross-section of an HV NMOS transistor

It is important to note that the high-voltage transistors are quite large: 90 μm x 112 μm. The number of high-voltage transistors used on-chip will therefore be the main factor controlling the overall die size.

4.2 Chip architecture

In order to provide full electric control to the electro-optic switch, 64 independent voltages ranging from 0 to 300 V are required [19], which means that 64 digital-to-analog converters (DACs) are needed on chip. The larger the number of bits per DAC, the greater the control over the voltages, which maximizes the optical performance. 6-bit DACs were therefore designed, which

gives a voltage resolution of 4.7 V over 300 V. The 64 DACs are laid out in an 8 x 8 array. The overall chip architecture is shown in Figure 35 below.

In order to provide the 6-bit independent inputs to each DAC, 384 (6 x 64) input pads would normally be required. This unrealistic port count is overcome by using four serial input registers, thus requiring only four input pads for the 384 digital inputs. On the right-hand side of Figure 35, a blow-up of the architecture of a single DAC is shown. It consists of a row and column decoders and a current cell matrix. These structures are described in the next sections.

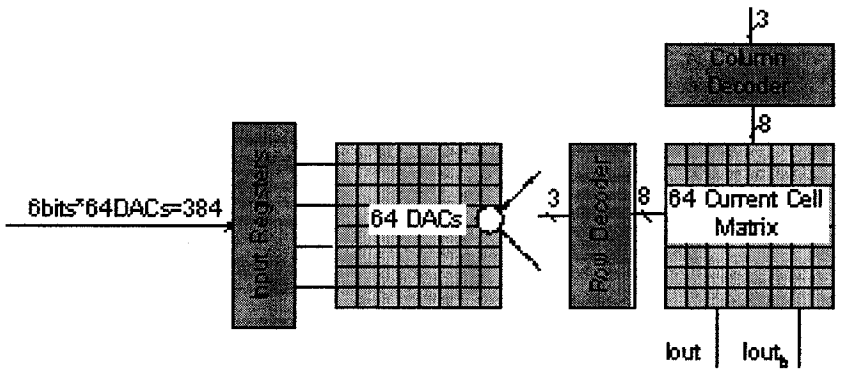


Figure 35. Chip architecture

4.2.1 Current cell matrix

The current cell matrix for each DAC consists of 64 individual current cells. Each current cell can steer a fixed current I_{out} to the output of the cell. The maximum current output for the entire current cell matrix of a single DAC is therefore 64 x I_{out}, and has a resolution of I_{out}. The individual currents from all the current cells are summed together before undergoing current-to-voltage conversion, as described in section 4.2.3, to provide the final output voltage of the DAC. This type of DAC architecture is called a thermometer coded DAC.

For a thermometer coded DAC, when the 6-bit input is increased by one Least Significant Bit (LSB), an additional current source in the current cell matrix is turned on. This architecture ensures monotonicity, low glitch energy, and relaxed matching requirements on the current sources when compared to a binary weighted DAC [96, 97]. In contrast, in a binary weighted DAC, every switch

switches an output current that is twice as large as the previous LSB. Though this architecture may be simple, a larger Differential Non-Linearity (DNL) error ensues and the overall static and dynamic performances of the converter are compromised.

As mentioned above, the implementation of the thermometer coded DAC requires 64 (2^6) current cells, each connected to digital logic. A single current cell is shown in Figure 36 below.

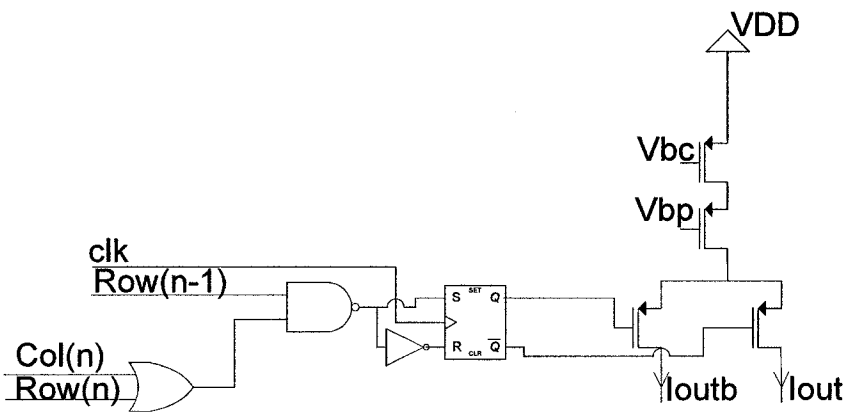


Figure 36. A single current cell

The current is either steered to the output I_{out}, and is then summed to the outputs of the other current cells, or is steered to I_{outb}, and then to ground.

4.2.2 Input registers

In order to provide the 6-bit digital inputs to each DAC, 384 input pads would normally be required. This unrealistic port count is overcome by using four scan chains (96 bits each), hence requiring only four input pads for the digital inputs. A schematic of a scan chain is shown in Figure 37 below. The scan_en strobe on the scan chain is asserted once all 96 inputs have been scanned in. Four scan chains are used as opposed to a single 384 bit scan chain, to reduce input delay.

After being scanned in, the input bits are sent to the individual row and column decoders for each DAC, as illustrated in Figure 35. The three most significant bits drive the column decoder, while the three least significant bits

drive the row decoder. The output bits of the decoders control whether the current from a current cell is steered towards output I_{out} or I_{outb}.

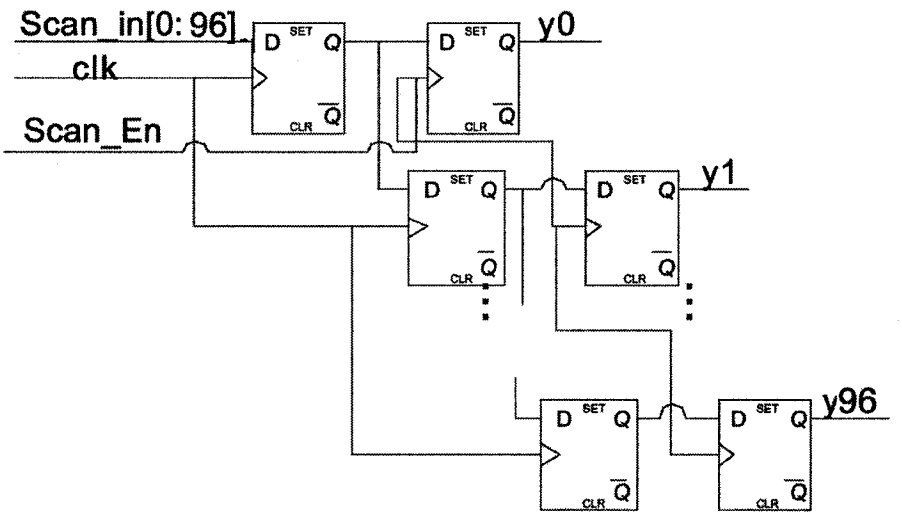


Figure 37. Scan chain for the digital input bits of the DAC array

4.2.3 Current-to-voltage conversion

The currents flowing from each current cell, shown in Figure 36, are summed to generate the total DAC current. Due to the peculiarities of the high-voltage transistors, standard current-steering DACs in which the current-to-voltage conversion is done using an output resistor or an op-amp, cannot be used. This section will explain the limitations of the standard designs and discuss the solution for high-voltage (HV) situations. The standard designs using an output resistor for the current to voltage conversion are shown in Figure 38.

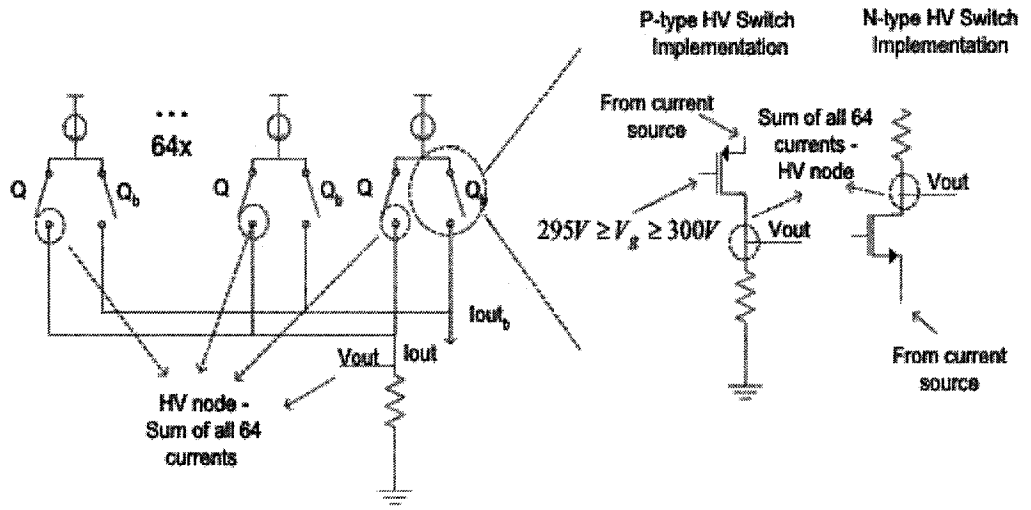


Figure 38. Standard I-V conversions for a current-steering DAC

When using an output resistor to convert the current to a voltage, the design is impractical because the current summation node would be a HV node, thus requiring all current switches in the current cells to be HV transistors. On the right-hand side of Figure 38, two methods of implementing the high-voltage current switches are shown. In the N-type implementation, the main drawback is the elevated number of HV transistors, and therefore area, required. The HV transistors are quite large (90 μm x 112 μm), such that using 128 of these (two for each of the 64 current cells) would require a prohibitively large die size. Using the P-type alternative entails a method of providing the required gate voltages to these HV transistors (295 V ≥ V_G ≥ 300 V), for example by using level-shifters, and this also results in using many HV transistors.

An alternative way of implementing the current-to-voltage conversion is by using an op-amp. However, this method is also difficult to implement due to the V_{GS} constraint discussed in section 4.1. Figure 39 depicts a simple two-stage op-amp configuration.

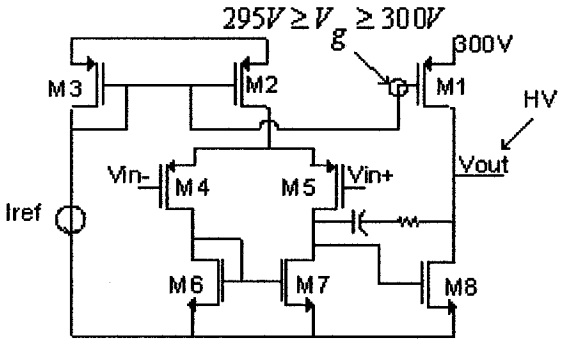


Figure 39. Two-stage CMOS op-amp implementation

Transistors M1 and M8 must be high-voltage transistors in order to produce the desired HV signal. However, P-type HV transistors require that their gate voltage be within 5V of the source voltage. This constraint triggers a domino effect, in the sense that transistors M2 and M3 must now be HV transistors since their gates are connected to that of M1. This implies that I_{ref}, if implemented on-chip, would also consist of HV circuitry. It is therefore evident from this simple implementation that the output stage of a typical op-amp is not the optimal solution to provide the current-to-voltage conversion, as the area quickly increases with the number of HV transistors.

One effective alternative for the current-to-voltage conversion, which we implemented in our application, is to use a high-compliance current mirror [98] and to replace the output transistor by HV transistors, as shown in Figure 40. In this approach, the current is copied to the output node with a worst-case error of 0.53 %, thus decoupling the current switches from the HV node. This particular implementation sources 2 mA to the capacitive load of the electrodes deposited on the EO crystal. This technique considerably reduces the number of HV transistors in each DAC unit from a potential high of 128 transistors, down to 6. This therefore results in a great savings in die area, though the frequency response of the DAC is lower.

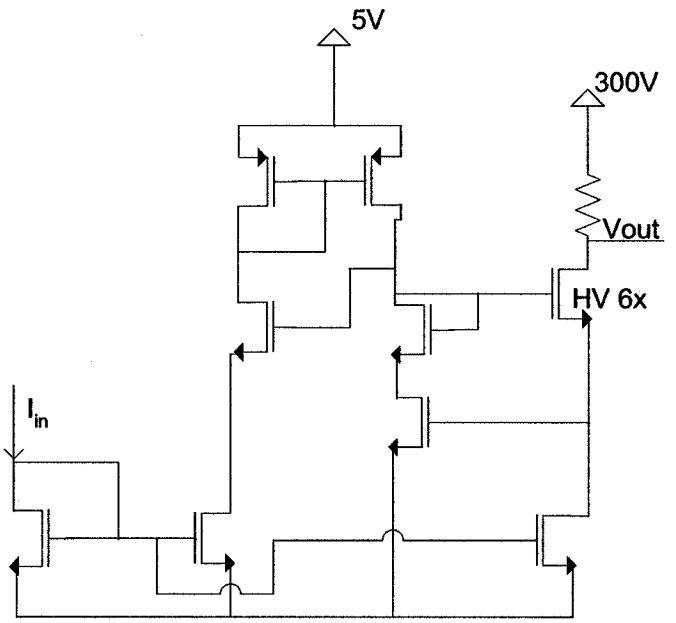


Figure 40. High output impedance current mirror

4.2.4 Layout of chip

When designing the layout of the chip, the optical path of the light must be considered. When the high-voltage chip is used in the 1-D ROPA configuration, there must be no wirebonds, and hence no wirebond pads, blocking the path of the light. Also, to increase the mechanical robustness, the EO crystal should be centered as much as possible on the chip. This implies that the flip-chip pads must be close to the center of the chip. The layout of the chip is shown in Figure 41 below. With the orientation of the chip given in Figure 41 the optical path is vertically oriented and there are no wirebond pads in the path.

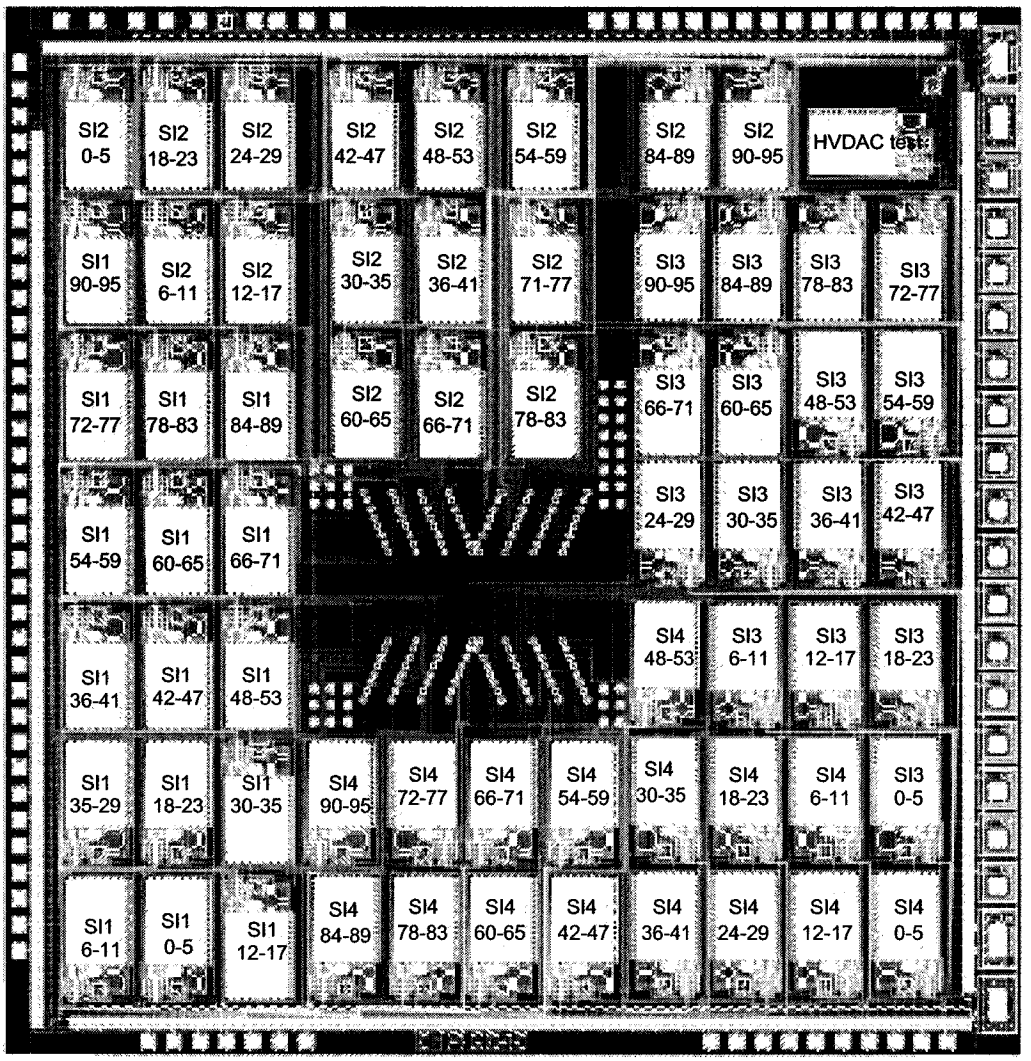


Figure 41. Layout of chip showing the 64 DACs and their controlling scan chain bits

Also shown in Figure 41 is the location of all 64 DACs. For each DAC, the input scan chain used is indicated by the notation "SIn" where "n" is the scan chain number from 1 to 4. The bits within each scan chain used to control that particular DAC are also indicated.

Due to the large size of the high-voltage transistors, the final die size is quite large: 8.1 mm x 8.1 mm. This translates to a large cost for fabricating the die. However, the manual handling of the die during the flip-chipping process is simplified.

In Figure 42, a packaged chip is shown with one of the 64 DACs highlighted, as well as the location of the flip-chip pads. In this figure, the optical path for the 1-D ROPA design is from left to right.

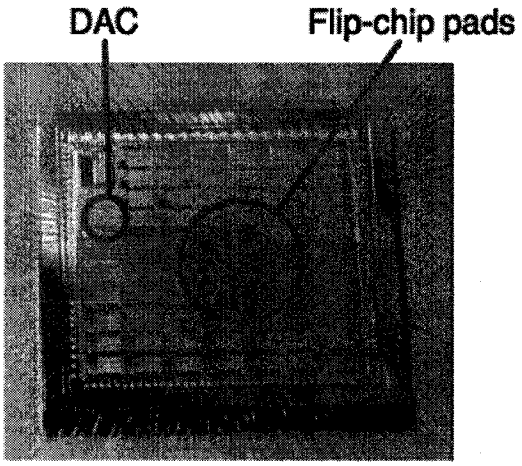


Figure 42. Packaged chip with flip-chip pads highlighted

4.2.5 Capacitive load

The switching speed of the CMOS chip is partially dependent on the capacitance of the electrodes. The electrodes essentially act as parallel plate capacitors, with a capacitance given by:

$$C = \frac{\varepsilon_r \varepsilon_o A}{d} \qquad (5.1)$$

Since each electrode is 3 mm long and 20 μm wide, the area A of one electrode is 6×10^{-8} m^2. The thickness of the device, d, is 500 μm. The electric permittivities for the two crystals are:

$\varepsilon_r = 3700$ for $BaTiO_3$ [73]

$\varepsilon_r = 2000$ for SBN [99]

Given that ε_o = electric permittivity of free space = 8.84×10^{-12} F/m, then the capacitances of the electrodes are:

$C = 3.9 \times 10^{-12}$ F = 3.9 pF for $BaTiO_3$

$C = 2.1 \times 10^{-12}$ F = 2.1 pF for SBN

As a larger capacitance means a slower response time for the chip, the larger capacitance for the electrodes across the $BaTiO_3$ crystal was used in the electrical simulations in order to simulate the worst-case scenario. These simulations are presented in the next section.

4.3 Simulations of performance of chip

The chip was simulated using Spectre. The output voltage was simulated for each of the 64 possible input codes. The resulting output voltages are shown in Figure 43. To quantify the performance of a DAC, two important figures of merit can be extrapolated from the simulated output voltages. These are the Differential Non-Linearity (DNL) and the Integral Non-Linearity (INL). When the input to the DAC varies by one bit, or one input code transition, the DNL measures the output deviation produced by the DAC with respect to the ideal Least Significant Bit (LSB) step of 4.7 V. For example, if the ideal output voltage for a particular input code transition is supposed to go from 10 V to 14.7 V (1 LSB), and the simulated output goes from 10V to 12.35 V (0.5 LSB), the deviation corresponds to half of an LSB step (half of 4.7 V). In other words, DNL = 0.5. The DNL is shown in Figure 44 below, and always has a magnitude less than 0.4.

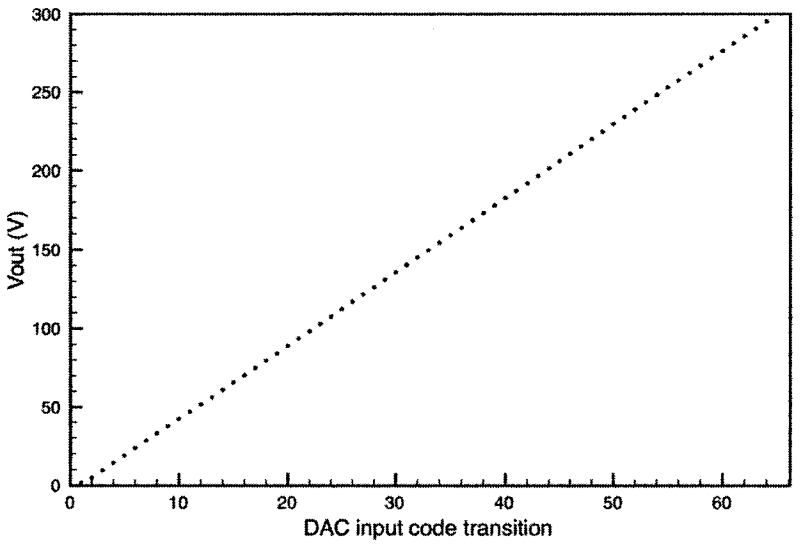


Figure 43. DAC output voltage level versus input code

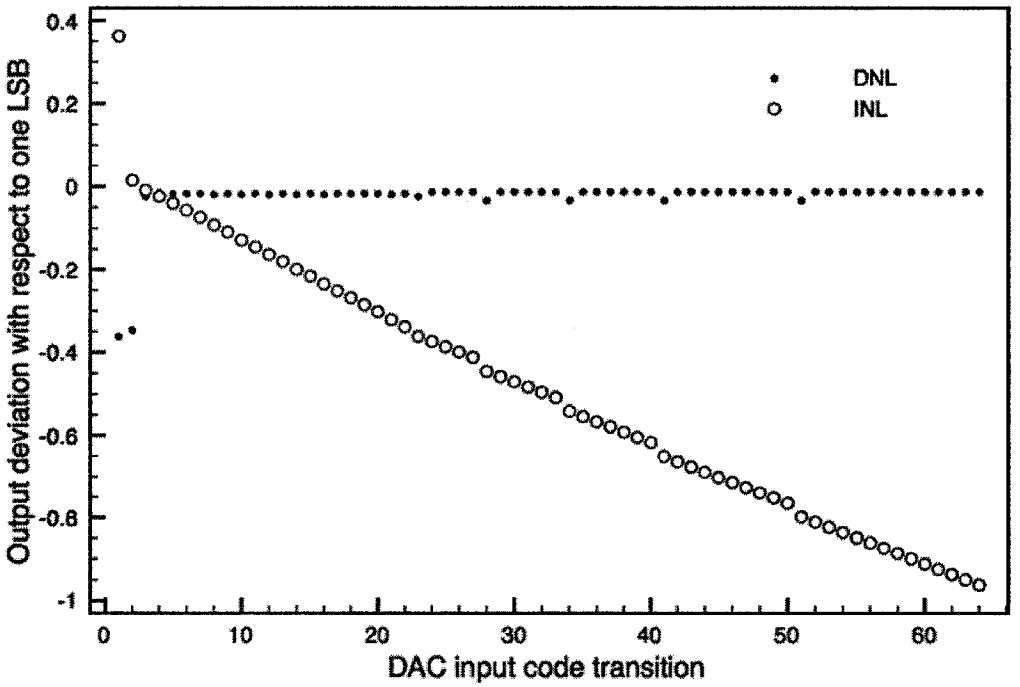


Figure 44. Simulated DNL and INL over all input codes

The other important figure of merit mentioned above is the INL. The INL shows how much the DAC transfer characteristic deviates from the ideal, in LSB units. For example, if the ideal output voltage for a particular input code is 10 V and the simulated output is 12.35 V for the same input code, the deviation corresponds to half of an LSB step (half of 4.7 V). In other words, INL = 0.5. The worst-case simulated INL was -1.0 LSB, and is shown above in Figure 44.

Another important parameter for the DAC performance is the switching time. The switch time is measured for the case when the DAC is providing the maximum output voltage swing. The worst-case capacitance of each electrode being driven by the DAC is 3.9pF. For this capacitance, the simulated 10-90% rise time is 1.2 μs and the fall time is 0.9 μs. The switching time is illustrated in Figure 45.

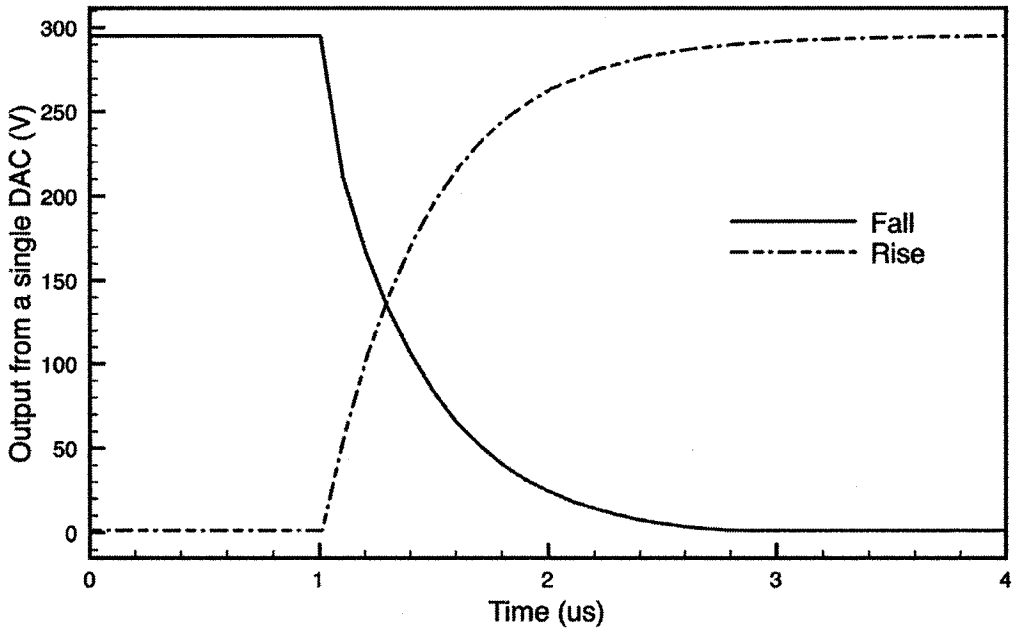


Figure 45. Simulated output of a DAC switching from 0 V to 300 V

These switching times are fast enough to satisfy the requirements of an AAPN network.

4.4 Summary

The ROPA design exploits the new mixed high and low-voltage transistor process developed by DALSA Semiconductor. With this technology, it is now possible to construct a chip capable of providing all of the independent voltages required for the ROPA devices. As a consequence, the ROPA switches are compact devices, as opposed to being electro-optic crystals controlled by multiple, bulky, external voltage supplies.

The overall high-voltage chip architecture consists of an array of 64 transistors. Each DAC has a thermometer-coded architecture consisting of 64 identical current cells. The sum of the currents from the current cells undergoes a current-to-voltage conversion using a high-compliance current mirror. This method of current-to-voltage conversion was chosen in order to minimize the number of high-voltage transistors used, and to thus minimize the area of the die. The simulated DNL, INL, and switching times were presented.

CHAPTER 5. EXPERIMENTAL RESULTS

This chapter covers all of the experimental results obtained for the ROPA device. It begins with describing the electrode deposition process that was developed specifically for this project, and the testing of the reflectivity of the resulting electrodes. The effect of the electrode deposition process on the optical performance is also investigated. Afterwards, the electrical testing of the high-voltage chip is presented. As the performance of the high-voltage chip differed significantly from the simulated results, two different testing methodologies were developed to decouple the optical performance of the chip from the performance of the high-voltage chip. These testing methodologies were applied to both the 1-D and the 2-D ROPA devices.

5.1 Electrode deposition process

Before the electrode deposition process, the crystals are cut to the correct dimensions (5 mm x 5 mm x 500 μm) and are polished. Temporary poling electrodes made of conductive epoxy are then deposited onto the crystal, as described in section 3.1.3, and the crystal is poled. The poling electrodes are removed using acetone and the crystals are cleaned to prepare them for the electrode deposition. The cutting, polishing and poling steps were performed by the crystal manufacturers.

In order to save on polishing costs, the $BaTiO_3$ crystals were only polished to an optical grade on the two large top and bottom surfaces of the crystal. Since in the 2-D ROPA design the light does not go through the sides of the crystal, those surfaces do not require more than a rough polish. The SBN crystals, on the other hand, were fully polished on all surfaces. Though the light in the 1-D ROPA design does not go through the top and bottom surfaces, these surfaces were still polished in order to provide a high-quality surface for the electrode deposition.

As discussed in section 3.1.3, the deposited electrodes need to be compatible with flip-chipping, to be highly reflective at 1310 nm, and to adhere

well to both $BaTiO_3$ and SBN. The electrode stackup that filled these requirements was found to be Ti/Al/Ti/Au, with thicknesses of 50/500/500/6000 Å respectively. As both SBN and $BaTiO_3$ crystals are quite expensive, the deposition process was developed using mechanical samples of $LiNbO_3$. As mentioned in sections 3.1.1 and 3.1.2, the crystals' temperatures cannot be raised above their phase transition point without needing to re-pole the crystals afterwards. The phase transition point for $BaTiO_3$ is 125°C, and for SBN:61 it is 85°C. As a single processing procedure was desired for reasons of simplicity, this implied that the crystal temperature could not exceed 85°C. In order to have a safety margin, a process was developed that never exceeds 75°C.

Cleaning

To prepare the crystals for the deposition, they are first cleaned with the solvent Remover 1165 by Microchem. Afterwards, they are cleaned with acetone and finally with isopropyl alcohol while drying them with nitrogen.

Photolithography

The first step is to spin coat a > 1.5 μm thick layer of photoresist 9245. As the electrodes are 0.705 μm thick (50 + 500 + 500 + 6000 Å), the photoresist layer must be at least twice as thick to get complete liftoff after the metal deposition.

Since the crystal area is only 5 mm x 5mm, a significant edge bead forms around its perimeter when the photoresist is spin coated onto it. This edge bead must then be removed in order to get the photomask close enough to the top surface of the crystal. This removal is possible as the electrode pattern was designed to occupy the center 3 mm x 3 mm area of the crystal, leaving a 1 mm wide area around the edge of the crystal that does not require photoresist. After the edge bead removal, the photoresist is left for at least an hour to cure at room temperature.

The photoresist is then exposed to UV light using a contact aligner and a chrome photomask. After the UV exposure, the photoresist is developed in AZ 400K 1:4. It is then baked at 75°C for 15 minutes.

Metal deposition and liftoff

The metal stackup is created using Electron-beam (E-beam) evaporation. During the evaporation, the temperature of the crystal is monitored using a thermocouple placed right next to it in the chamber. The evaporation is suspended when the temperature reaches 65°C and is resumed when the crystal has cooled to 30°C. The thick gold layer (6000 Å) is deposited in three passes.

The liftoff step is performed in Remover 1165, which is heated to 65°C. The final cleaning of the crystal is done using acetone and then isopropyl alcohol.

5.1.1 Results of electrode deposition

The resulting electrodes are shown in Figure 46 below. Due to the removal of the edge bead, there is a ring of metal around the periphery of the crystal as shown in Figure 47. This extra ring does not hinder any of the next processing steps. In Figure 47, the copper tape that is visible through the crystal is just used to hold the crystal within its packaging and is not part of the processing.

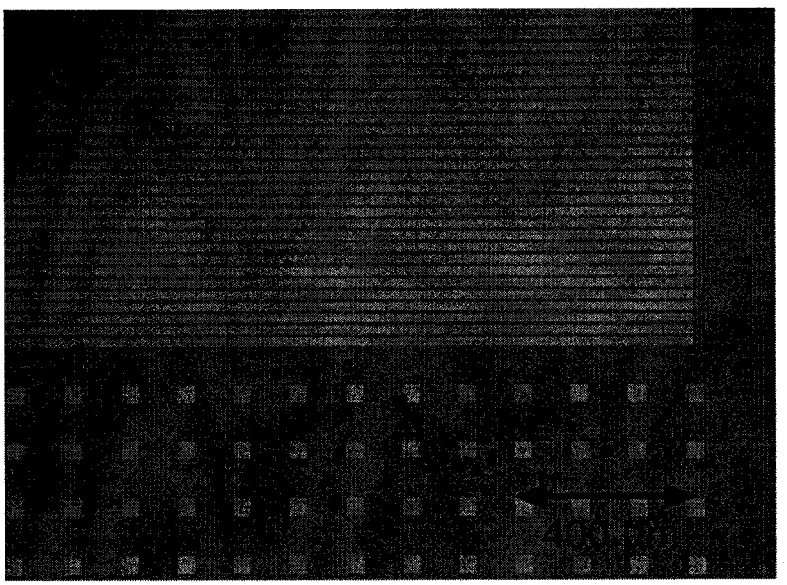


Figure 46. Electrodes deposited onto SNB crystal

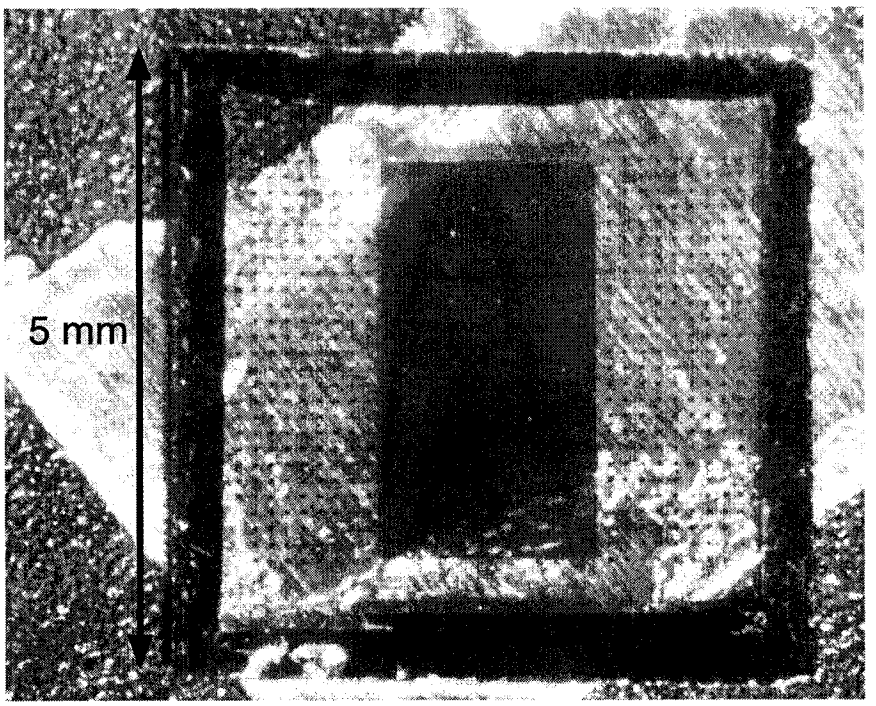


Figure 47. Top view of SBN crystal after electrode deposition

Before the electrode deposition process, 1310 nm light was sent through an SBN crystal, parallel to the electrode surface. The input beam at the front

surface of the crystal was elliptical with a waist diameter of 1.52 mm x 0.24 mm. The optical setup for the test is shown in Figure 48 below, and the resulting horizontal cross-section of the beam at the camera plane is shown in Figure 49 below. As can be seen in the figure, there is no noticeable beam distortion. After the electrode deposition onto an SBN crystal, light was sent through the crystal, once again parallel to the electrodes. The horizontal cross-section of the beam is shown in Figure 50. In this post-deposition case, side-lobes to the beam are clearly visible at the camera plane. It is important to note that this test could only be performed on an SBN crystal as the sides of the $BaTiO_3$ crystals were not polished, and therefore light could not be sent through the $BaTiO_3$ crystal parallel to the electrode surface.

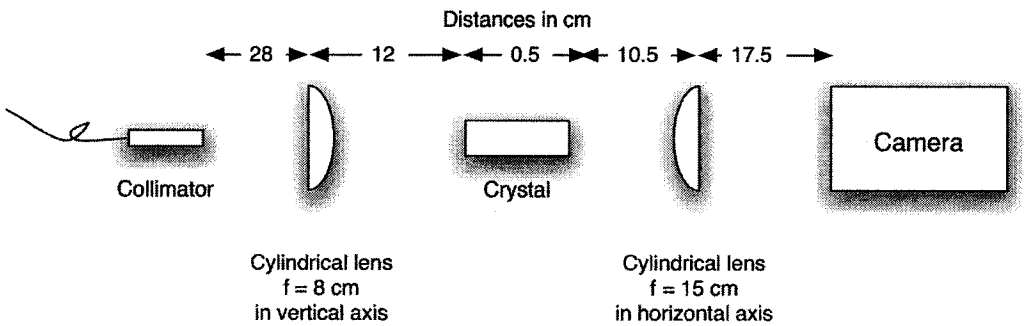


Figure 48. Setup to measure impact of electrode deposition

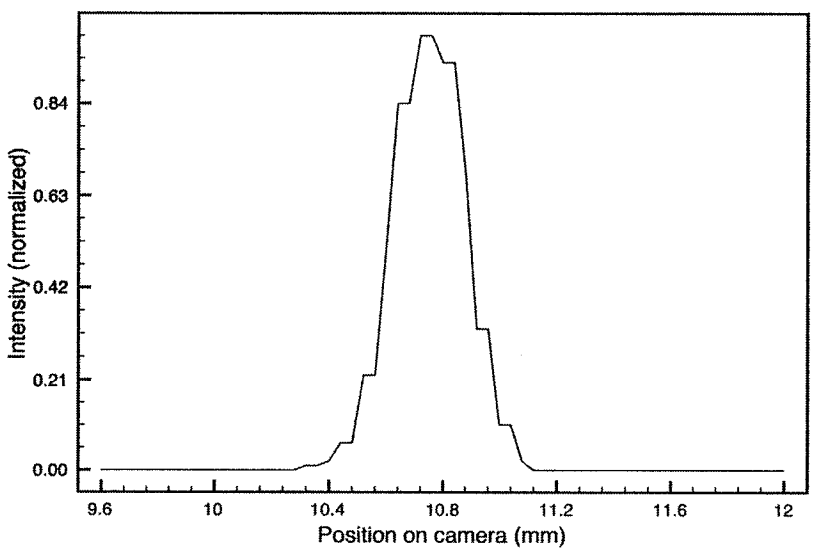


Figure 49. Cross-section of light beam through SBN crystal before electrode deposition

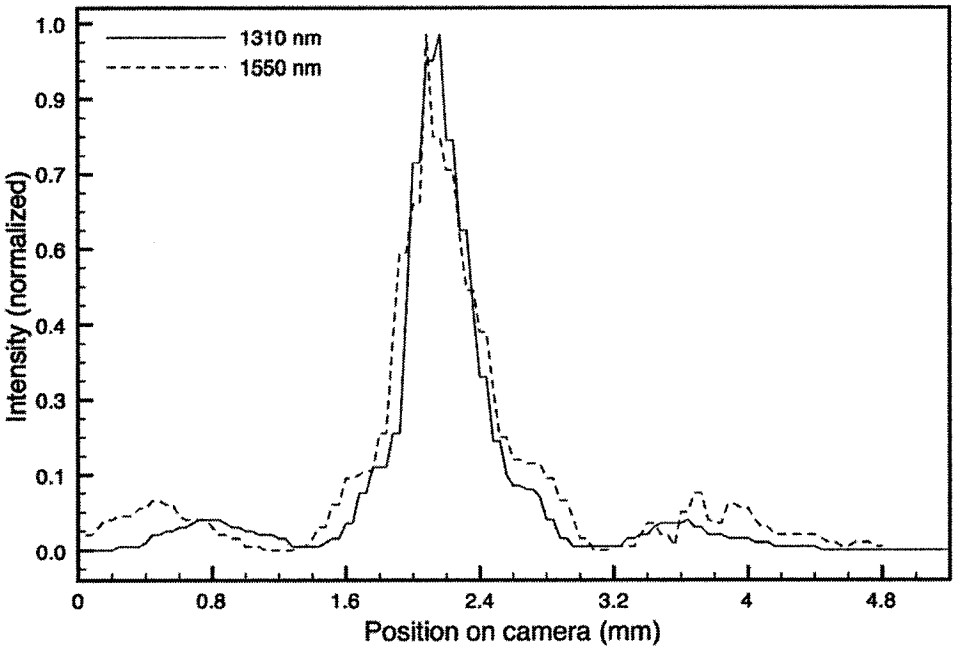


Figure 50. Cross-section of light beam through SBN crystal after electrode deposition

From Figure 50 we conclude that the process to deposit electrodes, or the electrodes themselves, causes mechanical stresses in the SBN crystal that affect the index of refraction. In order to further analyze the stress, the measurement of the output beam profile was done at both 1310 nm and 1550 nm. The location of the side-lobes at the camera plane was compared to the displacement that would occur from a binary grating within the crystal. The period of the grating within the crystal that would cause the displacement measured is 145 μm. This is shown in Table 9 below.

Table 9. Comparison of theoretical and measured deflections for a grating period of 145 μm

Wavelength (nm)	Theoretical Δx displacement (mm)	Measured Δx displacement (mm)
1310	1.42	1.4
1550	1.68	1.7

Had the locations of the side-lobes been consistent with a grating periodicity of 25 μm, one could have concluded that the stresses were highly localized above each individual electrode. As it stands, one can say that there are

stresses that create a grating effect, but the stresses are not clearly linked to the electrode locations.

5.1.2 Reflectivity of electrodes

For the 2-D ROPA design, the reflectivity of the electrodes is very important as it directly impacts the insertion loss of the final device. Figure 51 shows a block diagram of the setup used to measure the reflectivity of the electrodes, and Figure 52 shows a photo of the setup.

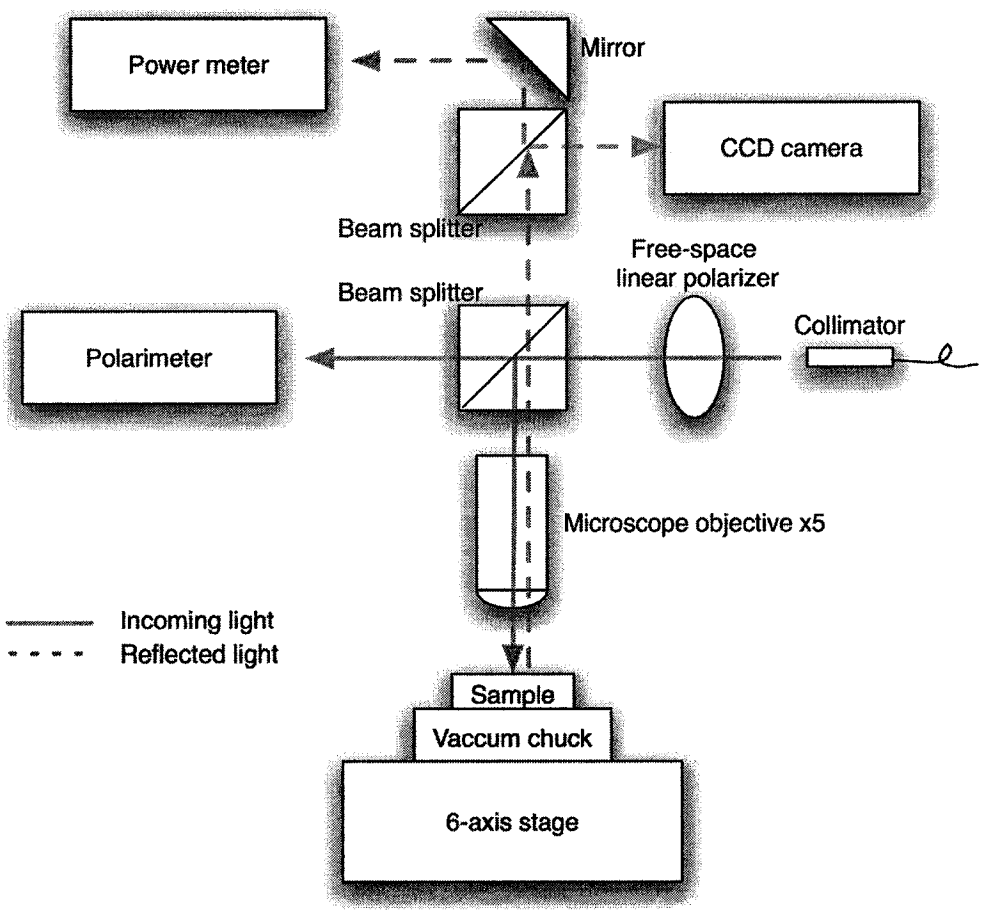


Figure 51. Setup to measure reflectivity of electrodes

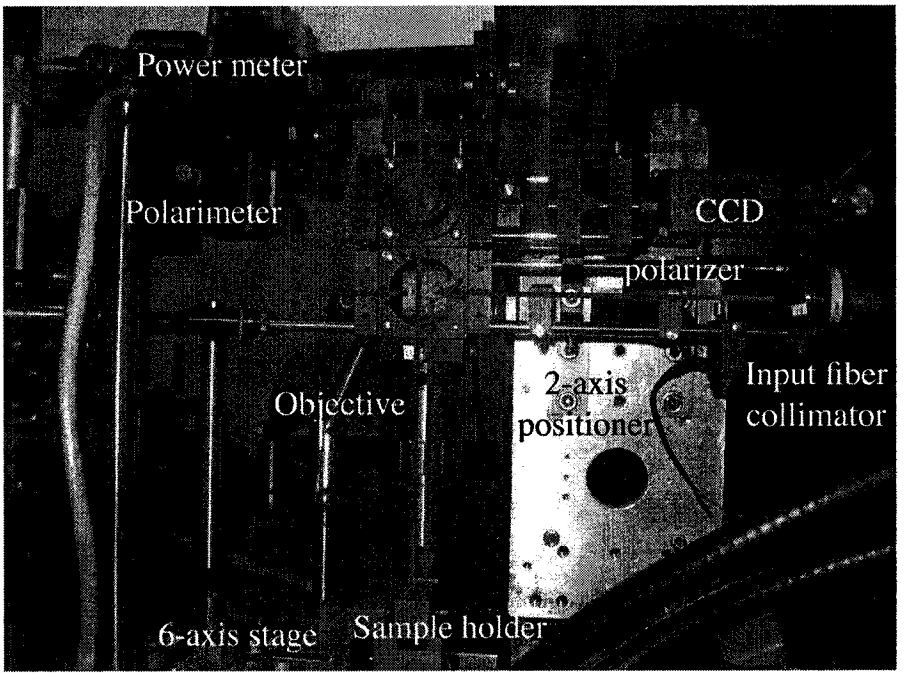


Figure 52. Photo of setup to measure reflectivity of electrodes

The light is launched from a collimator and goes through a free-space linear polarizer. The light is vertically polarized (ER > 35 dB) with respect to the horizontal electrodes on the sample. In order to verify the polarization, the light is split using the center 50/50 beam splitter and then measured with a polarimeter. The light then goes through a x5 microscope objective and is reflected off the sample being tested. The sample is mounted on a vacuum chuck that is itself mounted on a 6-axis stage. The reflected light is split by a second 50/50 beam splitter, located towards the top of the setup. Half the light goes to a CCD camera for alignment purposes, and the other half to a power meter to measure the reflected power.

As this setup requires a reference measurement, a gold mirror was used as the reference. The reflectivity of the gold mirror (Thor Labs part number PF10-03-M01) is specified to be 98% for wavelengths ranging from 1300 nm to 1600 nm. The measured reflectivities for a $BaTiO_3$ sample are shown in Table 10. The reflectivity in the center column shows the reflectivity measured with the setup. The column on the right hand side shows the calculated reflectivity of the

electrodes, given that the electrodes cover 80% of the area of the crystal as described in section 3.1.3.

Table 10. Reflectivity of electrodes on $BaTiO_3$ sample

Wavelength used (nm)	Measured reflectivity of sample	Reflectivity of electrodes	Theoretical reflectivity
1310	58.4%	73.1%	90%
1550	51.4%	63.3%	89%

The experimental error on the measured reflectivity is 8%. One of the main reasons for the lower than theoretically predicted reflectivities is the surface roughness of the electrodes that scatters the incoming light. This scattering is to be expected, and though it increases the insertion loss it should not otherwise adversely affect the performance of the device.

5.2 High-voltage chip

The testing of the high-voltage chip was performed before flip-chipping. Once the flip-chipping is performed, there is no access to the top surface of the chip in order to monitor the output voltages, and the optical and electrical performances can no longer be decoupled.

5.2.1 Experimental test bed

The chip is wirebonded into a 144-pin surface mount gull-wing ceramic carrier. This carrier is soldered onto a custom Printed Circuit Board (PCB) shown in Figure 53 below. The main functions of the PCB are to connect the digital inputs of the chip to a computer controlled digital input/output card, and to provide the DC supply voltages and currents to the chip and to all the test circuitry on chip. The layout of the board was designed to not impede the light path for the 1-D ROPA design.

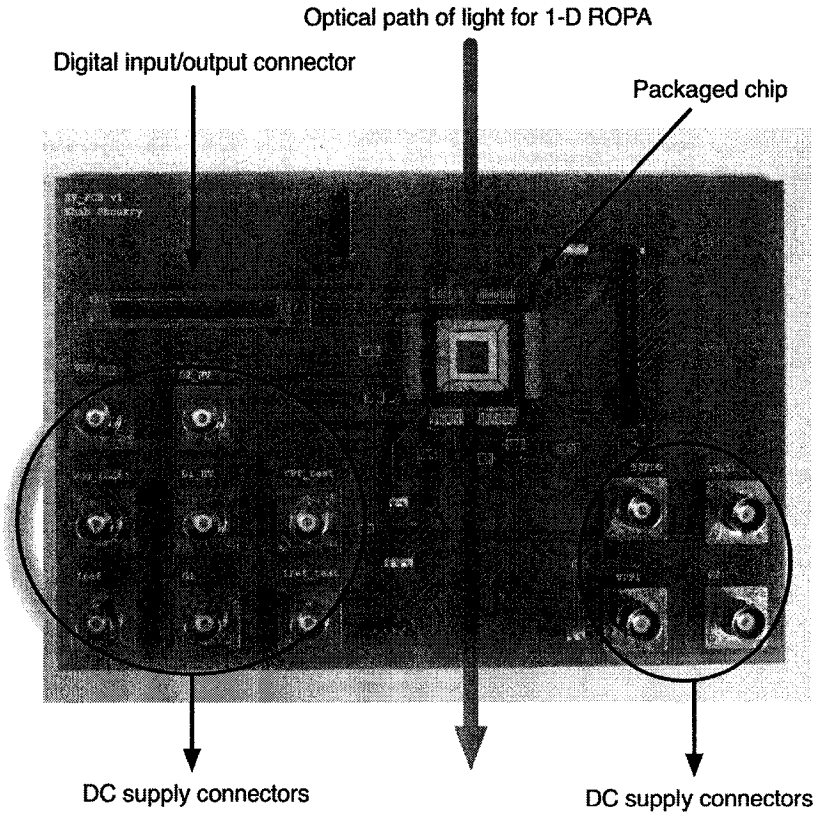


Figure 53. PCB used for high-voltage chip testing

Due to the high worst-case power dissipation of the chip (6W), the chip is temperature cooled using a Thermo-Electric Cooler (TEC) to 35°C. When not cooled, the operating temperature of the chip rises to over 90°C and logical errors appear at the output of the input row and column decoders. Also, since the EO crystal is flip-chipped to the chip and will be at approximately the same temperature as the chip, for the sake of the optical performance of the crystal it is best to maintain it as close to room temperature as possible. In order to accommodate the TEC and to place it up against the backside of the ceramic carrier, a hole was drilled into the PCB under the carrier. This is shown schematically in Figure 54. A heat sink is placed on the other side of the TEC to help with the heat dissipation. A thermistor is glued to the top side of the carrier, next to the chip, in order to provide temperature feedback to the TEC controller. In Figure 55, the thermistor is visible on the top side of the chip, with alligator clips connected to its leads.

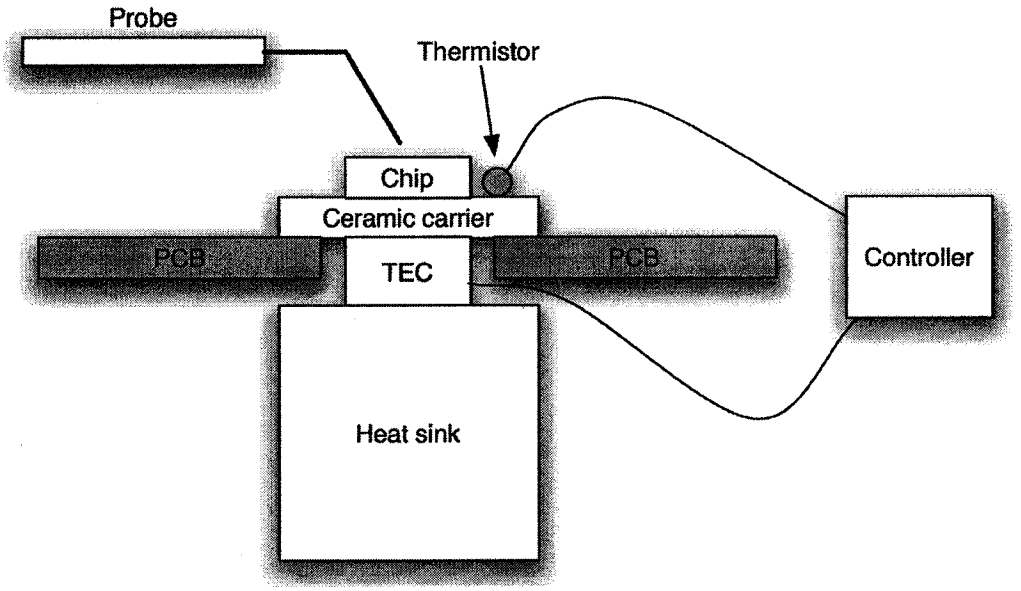


Figure 54. Temperature control of high-voltage chip

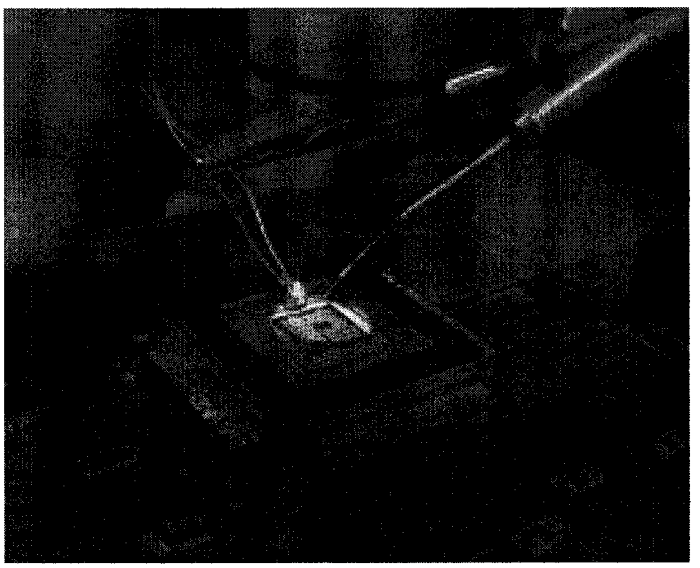


Figure 55. Probing of DAC output on HV chip

A cat-whisker probe tip is used to connect to the test points on the chip, including the flip-chip pads themselves. The cat-whisker probe is itself connected to a 100:1 high-impedance probe and then to an oscilloscope.

A Labview interface was implemented to serially provide the 384 input bits to the 4 scan chains on the chip described in section 4.2. Through this interface, the output of all 64 DACs can be independently controlled.

5.2.2 Testing results

The initial part of the testing consisted of confirming the performance of a single high-voltage N-type DMOS transistor. To do so, two separate HV test transistors were placed on-chip. Their source and bulk were tied to ground, while the drain and gate voltages were varied. The resulting current I_d was measured. The gate voltage was restricted to 0 V to 5 V while the drain ranged from 0 V to 300 V.

This test circuitry allowed us to reproduce DALSA's I-V curves. Ideally, many HV transistors would have been placed to account for low yield or any other unforeseeable problems, however area restrictions limited the testing to two HV test transistors. The experimentally measured I-V curves are shown in Figure 56 below. The curves illustrate the drain current response to a variation in the drain voltage ranging from 0 V to 300 V for various gate voltages. When the drain voltage surpasses 100 V, the drain current begins to drop. Interestingly, DALSA's documents only provide I-V curves for drain voltages in the 0 V to 100 V range. All of the tests in this section, unless otherwise mentioned, were performed with the chip temperature controlled to 35°C.

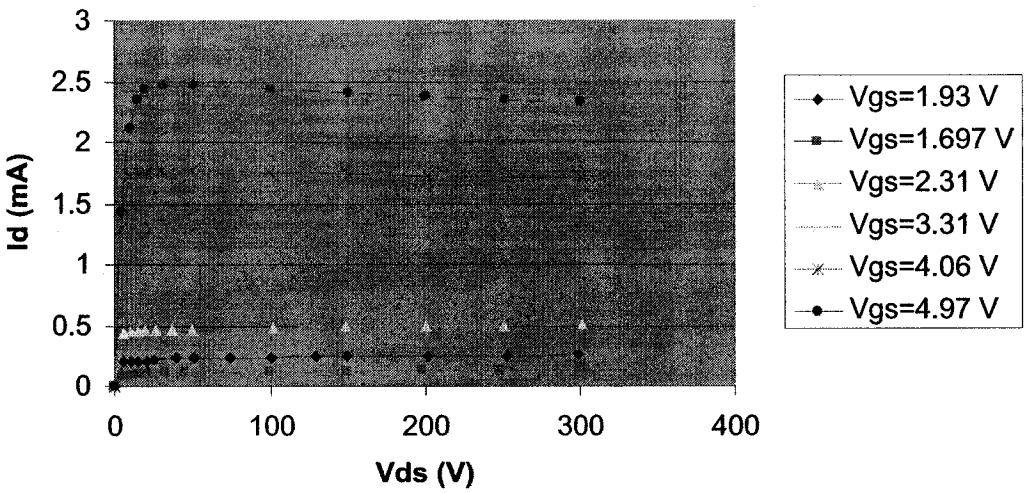


Figure 56. I-V curve for a single HV transistor

The next phase of the testing involved testing the logical functionality of the input scan chains using probe pads set at the output of the scan chains, before

the DACs. In all, 26 dies were tested. For all the tested dies, the fourth scan chain (SI4) functioned correctly. However, on all 26 dies tested, the bits coming out of scans chains 1 and 3 (SI1 and SI3) had randomly occurring errors that made the DACs for those scans chains effectively uncontrollable. Additionally, scan chain 2 (SI2) had only 5 out of 6 bits that consistently had no errors. Unfortunately, the bit with the occasional errors was the most significant bit. As a consequence of these logical errors at the output of the scan chains, only a quarter of the DACs were consistently controllable. The cause of these errors is not well understood. The four scan chains were designed and laid out on chip as identical blocks. There is no difference at all between them besides their location on the die.

After testing the functionality of the scan chains, the performance of the DACs themselves was tested. The simulated and experimentally measured output voltages of a single DAC are shown below in Figure 57.

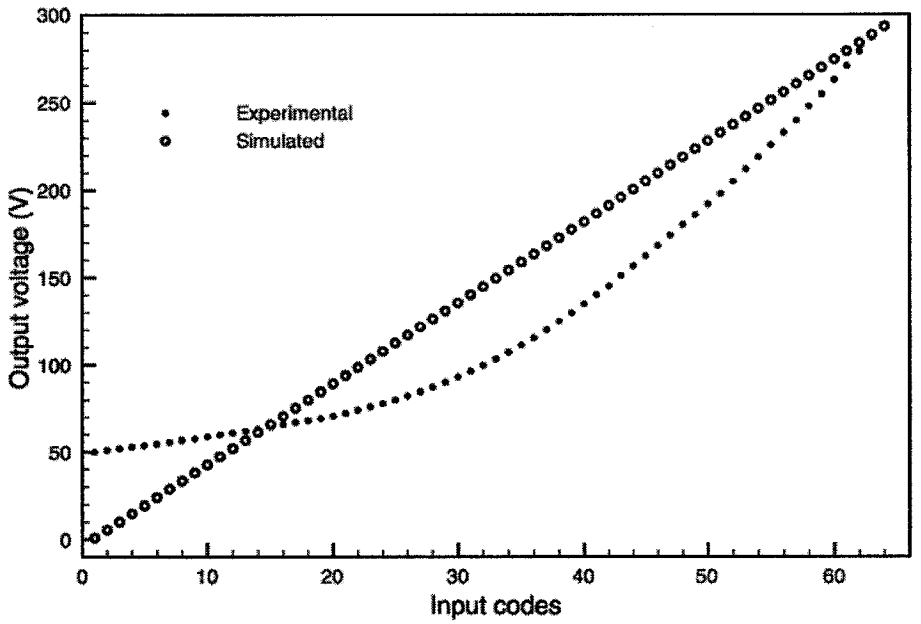


Figure 57. Output of DAC 29 (controlled by SI4)

As can be seen from the figure, the minimum output voltage is considerably higher than simulated. The minimum output voltage for all 16 functional DACs on one die are shown in Table 11 below. The DAC number

refers to the electrode that is controlled by the DAC. The electrodes on the crystal are numbered sequentially, but due to layout constraints each scan chain controls non-sequential DACs and therefore non-sequential electrodes.

Table 11. Minimum output voltage for all DACs from scan chain 4 (SI4)

DAC	Vout min (V)
41	40.7
44	43.7
43	44.1
51	44.6
50	47
58	49.1
52	49.1
9	51.3
26	51.8
59	52.5
29	53
30	53.3
60	53.8
28	53.8
27	53.9
57	57.5

As can be seen from the table, there is a large variation in minimum output voltage. By referring to the layout of the DACs controlled by scan chain 4 shown in Figure 58 below, an interesting trend emerges. The DACs with the lowest minimum voltage (i.e. 41, 44, 43, 51) are all clustered in the lower right hand corner of the die. This suggests the possibility that the minimum voltage is related to a process variation. In order to further investigate this phenomenon, the output resistance of the DACs was measured.

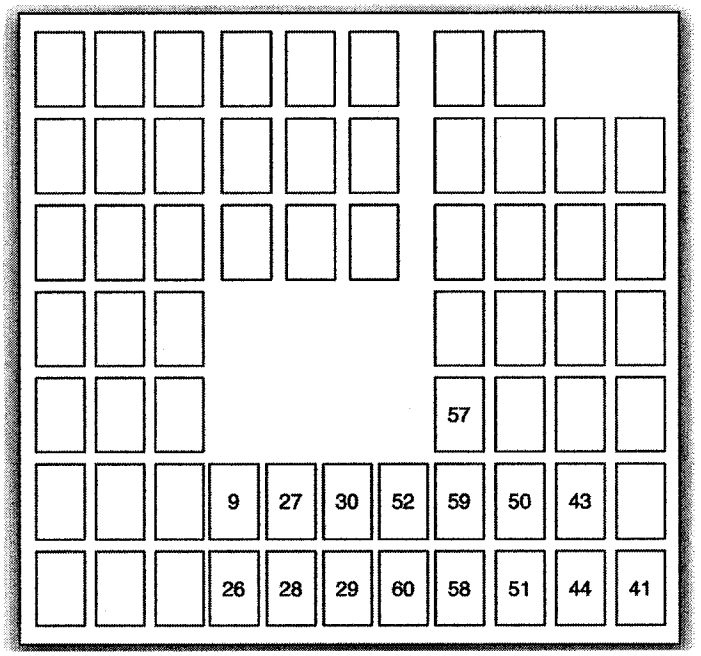


Figure 58. Location of DACs controlled by scan chain 4 (SI4)

The output resistance was measured for several DACs. The output resistance should be the same as the value of the pull-down resistor shown in Figure 40, which is 200 kΩ. The results of the measurement are shown in Table 12 below.

Table 12. Output resistance of DACs controlled by scan chain 4 (SI4)

DAC	Rout (kΩ)
41	217.9
44	218.1
43	219.5
51	218.2
50	217.5
58	218.4
52	219.3
9	217.2
26	218.5
59	218.3
29	217.5
30	218.1
60	217.8
28	219.3
27	218.5
57	219.7

As can be seen from the table, there is no distinct trend for the output resistance with respect to location. In all cases the output resistance is consistently about 18 kΩ too high. This discrepancy can be explained by the fact that the processing tolerance on the output resistor (Poly HiRes) is quite large: 5kΩ/sq ± 1.5kΩ/sq. However, this mismatch in output resistance does not explain why the minimum output voltage is so high. For a given current through the output current mirror, if the resistance of the pull-down resistor increases, the output voltage should drop, not increase. Most likely, either the current being generated by the current mirror or the sum of the currents from the current cells (or both) is not sufficiently large to pull down the voltage from 300 V to 0 V. As the DC supply voltage to the chip was reduced, the following output was measured:

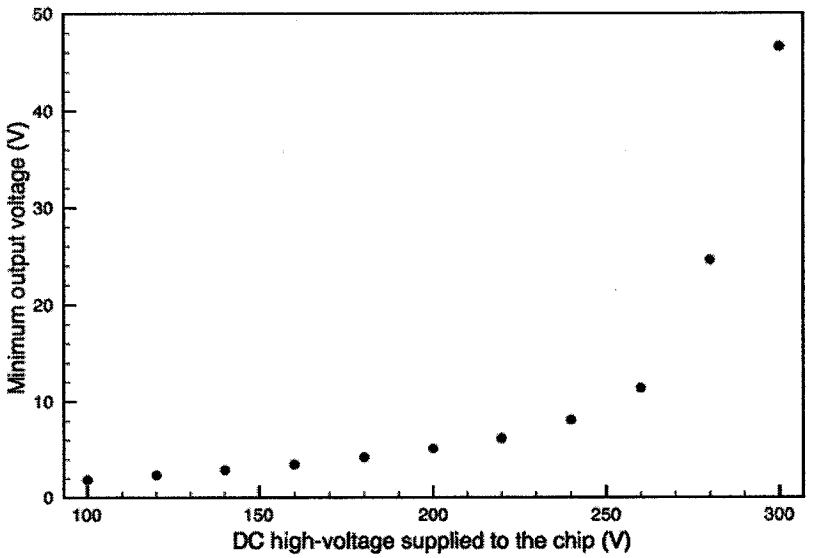


Figure 59. Impact of variation of supply voltage on minimum output voltage

As can be seen in Figure 59, as the high-voltage DC supply to the chip is reduced, the output voltage is also reduced. Without more test circuitry or probe points on the chip, it is difficult to further investigate the reasons for such a large minimum output voltage.

Due to the larger than simulated minimum output voltage, the experimentally measured INL differs significantly from the simulated values

shown in Figure 44. Both the experimentally measured DNL and INL are plotted in Figure 60.

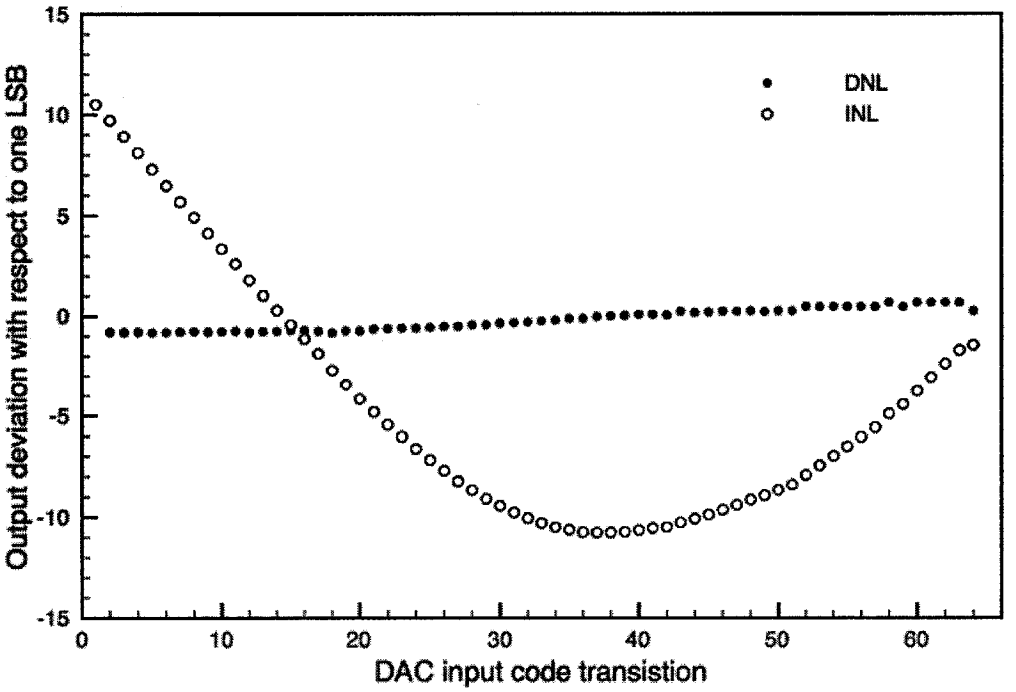


Figure 60. Experimentally measured DNL and INL

A final important parameter for the DAC performance is the switch time. The switch time is measured for the case when the DAC is providing the maximum output voltage swing. The experimentally measured rise time (10% to 90%) is less than 5.4μs, and the fall time is less than 16.2 μs. As these are considerably longer than the simulated rise and fall times (1.2 μs and 0.9 μs respectively), a careful analysis of the layout of the chip was performed. Referring back to Figure 36, the output of a single current cell is steered towards one of two possible outputs. In particular, it is steered towards I_{outb} and then on to ground when no current is required from that current cell. Unfortunately, the connection to ground was not made during the layout, such that the branch in the circuit for I_{outb} is open-circuited. As a consequence, the transistors in the current cell are turned off when the current from that cell is not needed. This slows down the performance of the current cell, and thus of the entire DAC. The layout error was not noticed before fabrication, as a "layout versus schematic" comparison

could not be performed. This feature is not yet available for the mixed high- and low-voltage transistor process.

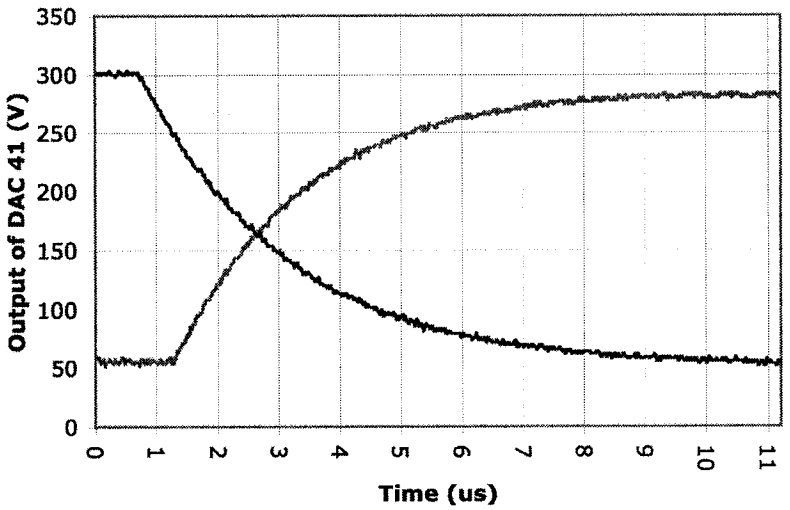


Figure 61. Switching speeds when DAC is providing the maximum output swing

5.3 Optical testing infrastructure

Since only a quarter of the DACs on the high-voltage chip could be fully controlled, a testing methodology needed to be developed to de-couple the optical testing from the electrical testing. This led to the design and fabrication of two different passive chips. One of the designs, called the "substitute" chip, is a passive chip to which the EO crystal is flip-chipped. The chip consists of traces going from the electrodes to wirebond pads. All of the voltage supplies are off-chip. The other chip design does not involve flip-chipping, but just depositing the crystal onto the surface of the chip. Both of these chips are described in the following sections as well as the printed circuit board used to control them. Once the experimental testbed has been described, the results of the optical test are presented.

5.3.1 Alternative chip designs

In the first chip design, the "substitute" chip acts as a break-out board from the flip-chip points to the wirebond pads. The location of the flip-chip pads

on the substitute chip matches the location of the flip-chip points on the high-voltage chip, just as the location of the wirebond pads matches the ones on the high-voltage chip. With this design, the substitute chip can easily replace the high-voltage chip for the optical testing and can use the same ceramic chip carrier for the packaging.

The layout of the traces on the substitute chip are shown in Figure 62 below. The metal stack-up for the traces was chosen to be compatible with both wirebonding and flip-chipping. First, a 300 Å thick layer of Titanium is deposited as it adheres well to the substrate. Afterwards, a 5000 Å thick layer of Aluminum is deposited. This second layer needs to be thick enough for the wirebond pads. Tests were conducted that determined that at least 4000 Å of Al were required for good wirebond adhesion.

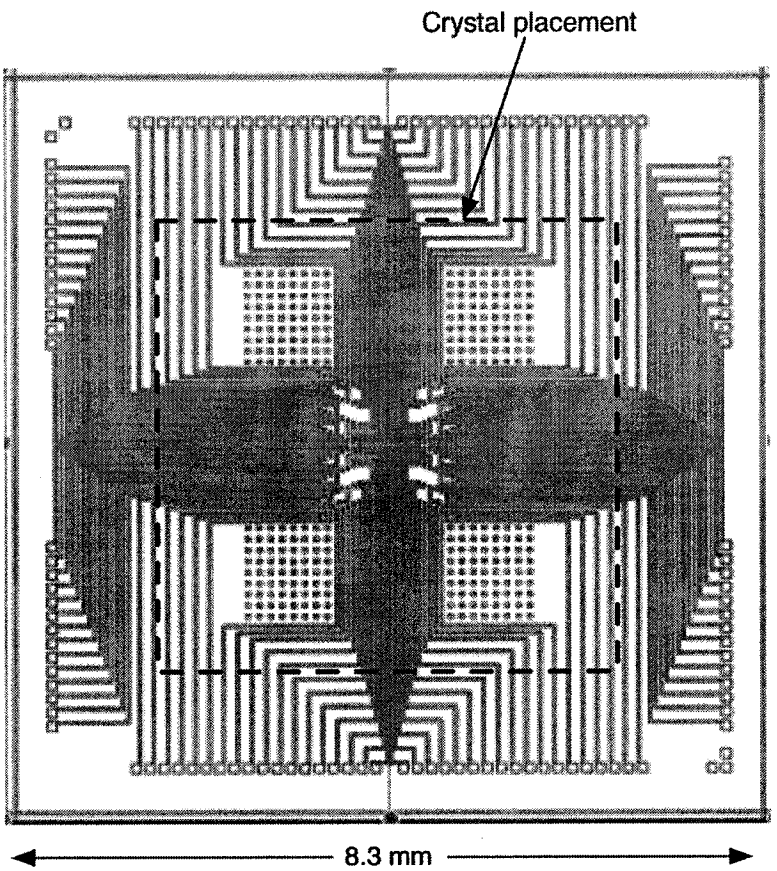


Figure 62. Autocad image of passive break-out chip

In order to prevent current leakage between the metal traces on the chip, a high-resistivity Si wafer was chosen as the substrate. The resistivity of the wafer is > 3000 Ω•cm. In order to provide further insulation, a 10 000 Å thick layer of oxide was grown on the surface of the wafer.

Additionally, a second substitute chip was designed to test the optical performance without needing to deposit electrodes onto the crystal or perform any flip-chipping. The pattern of metal traces on this chip mimics the pattern of the electrodes that would otherwise be deposited on the electro-optic crystal. The layout of the chip is shown in Figure 63.

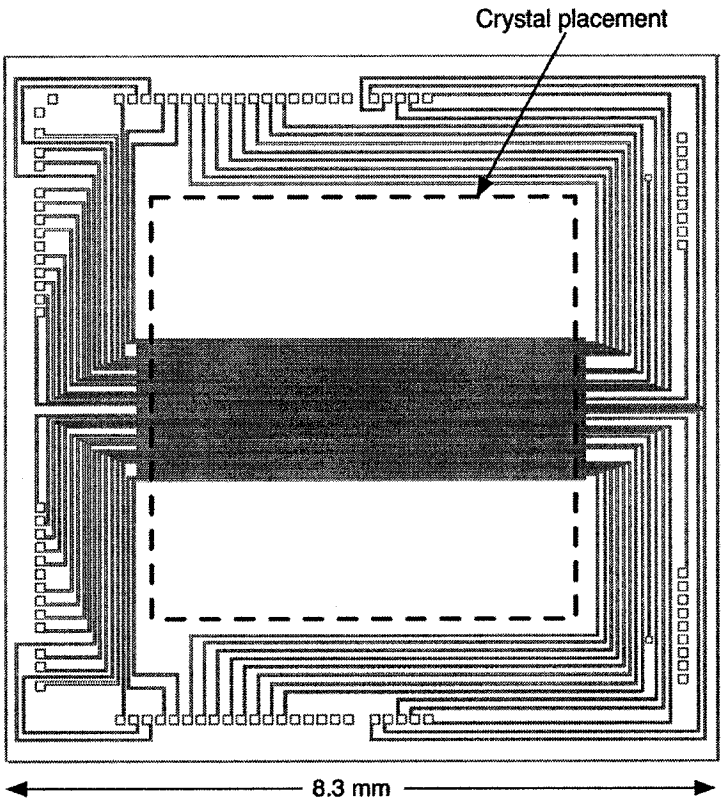


Figure 63. Autocad image of passive chip that bypasses electrode deposition

This chip is similar to the substitute chip described above, in that it is passive, has the same metal stack-up, and uses the same ceramic chip carrier. The main difference is that the center of the chip consists of the 64 electrodes that would normally be deposited onto the surface of the crystal. When the EO crystal is placed on top of this chip and voltages are applied to the electrodes on the chip,

ideally the same electric fields are created within the crystal as when the electrodes are deposited directly onto the crystal. This assumes that there is not much of an air-gap between the electrodes and the crystal.

This chip design was extensively tested to see if arcing would occur between the electrodes before any crystals were tested. The results of a destructive test are shown in Figure 64.

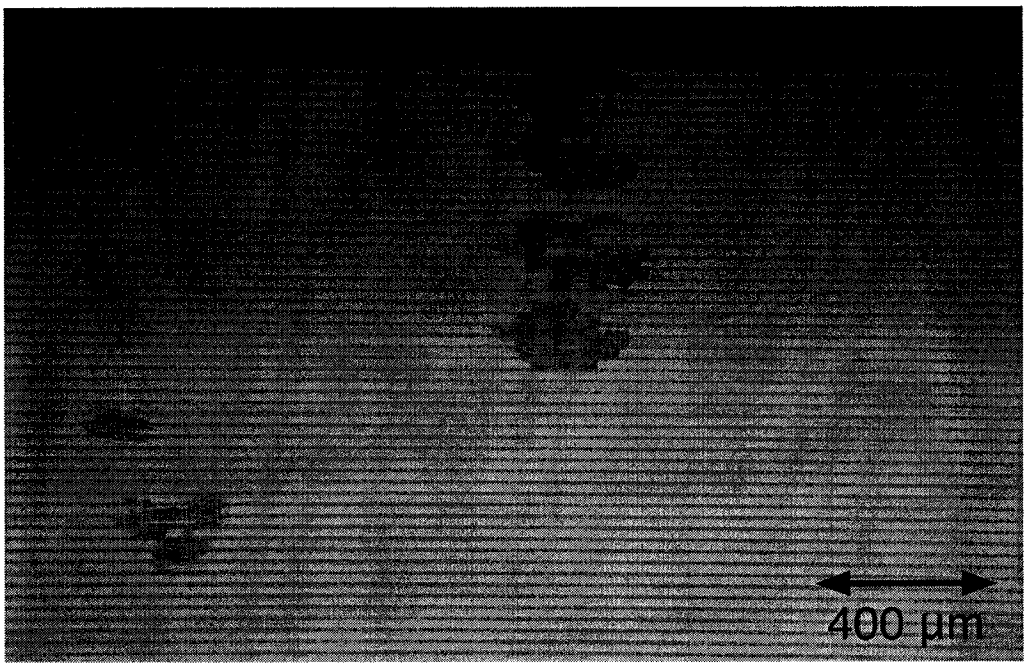


Figure 64. Damaged electrodes due to arcing on an SiO_2 substrate

In the initial tests, a thinner layer of oxide (3000 Å) and a mechanical grade Si wafer were used rather than the high-resistivity Si wafer that was described earlier. With this SiO_2 wafer, arcing occurred between the electrodes with a potential difference as low as 110 V. Once the high-resistivity Si wafer was used along with the thicker layer of oxide (10 000 Å), arcing occurred at voltages greater than 325 V for all but one of the tests. In one test, arcing occurred at 285 V. A possible explanation for this could be that there was incomplete liftoff between two of the metal electrodes and the gap between them was therefore less than 5 µm.

5.3.2 Flip-chip bumps

The flip-chip bumps were deposited onto the substitute chip in the same way that they would be deposited onto the high-voltage chip. The flip-chip bumps are Ti/Sn; they are on a 25 μm pitch, which matches the pitch of the electrodes on the crystal; each bump is 20 μm x 20 μm and is 4 μm high. Figure 65 shows a microscope image of the deposited bumps.

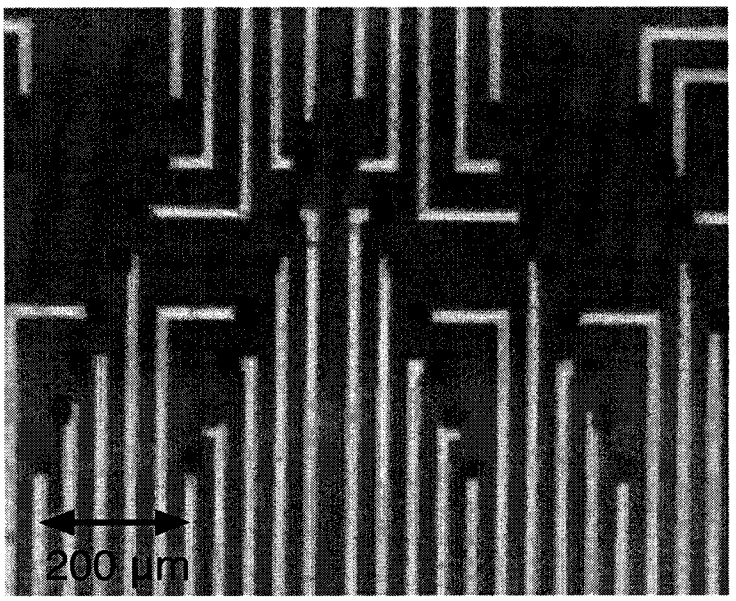


Figure 65. Flip-chip bumps deposited onto the substitute chip

Figure 66 below shows a Scanning Electron Microscope (SEM) image of the flip-chip bumps on the substitute chip. The four quadrants of bumps surrounding the flip-chip bumps for the electrodes are the 40 μm x 40 μm grounded bumps used for mechanical stability, as mentioned in section 3.1.3. The substitute chip only uses a subset of the available 40 μm x 40 μm pads on the crystal. This is due to the space requirements on the substitute chip for the metal traces going from the flip-chip points for the electrodes to the wirebond pads.

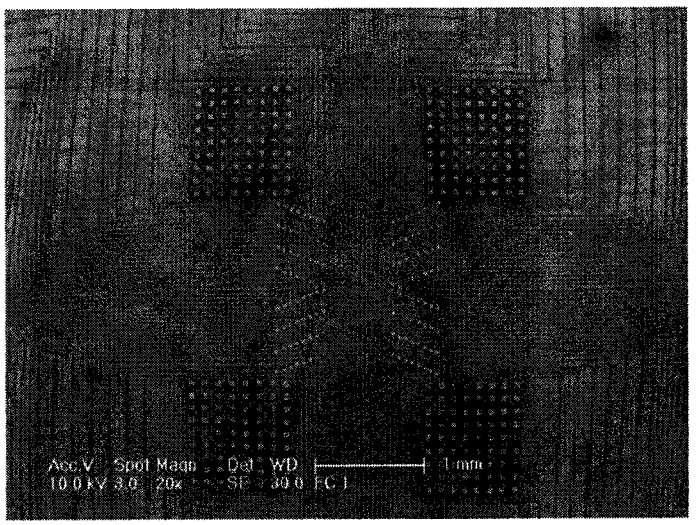


Figure 66. SEM of substitute chip with deposited flip-chip bumps

Two attempts were made to flip-chip the SBN crystal to the passive SiO_2 chip. After each flip-chip step, the device was tested for shorts in between the electrodes. In the first attempt, the flip-chip bumps were too wide and all of the electrodes were shorted together. In the second attempt, though the flip-chip bumps were of the correct dimension, there were shorts between roughly half of the electrodes. This was due to a misalignment of about 2 μm between the SBN crystal and the passive chip during the flip-chip process. Therefore, only partial optical tests could be performed on the flip-chipped SBN devices. These are presented in section 5.5.1. A photo of one of the flip-chipped SBN crystals is shown Figure 67 below.

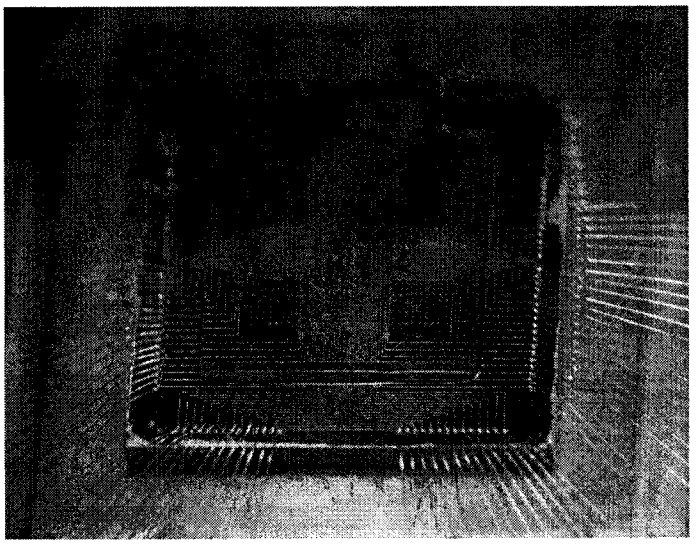


Figure 67. SBN crystal flip-chipped to a passive SiO_2 chip

5.3.3 Printed circuit board design

Since the two alternative chips designs are both passive chips, a PCB was designed to provide all 64 electrodes with the required voltages using only 8 external power supplies. The schematic of the PCB is shown in Figure 68, and a photo is shown in Figure 69.

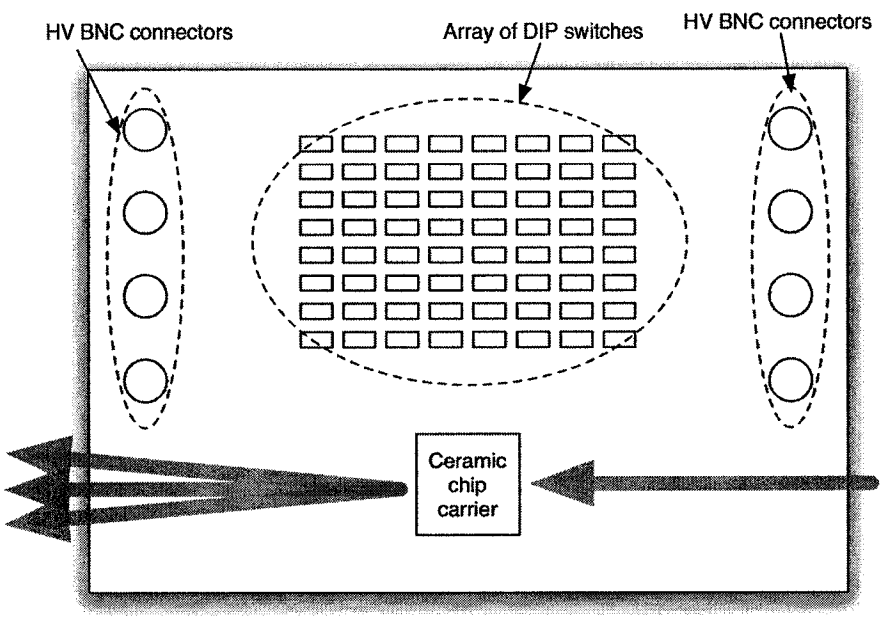


Figure 68. Schematic of PCB for alternative chip designs

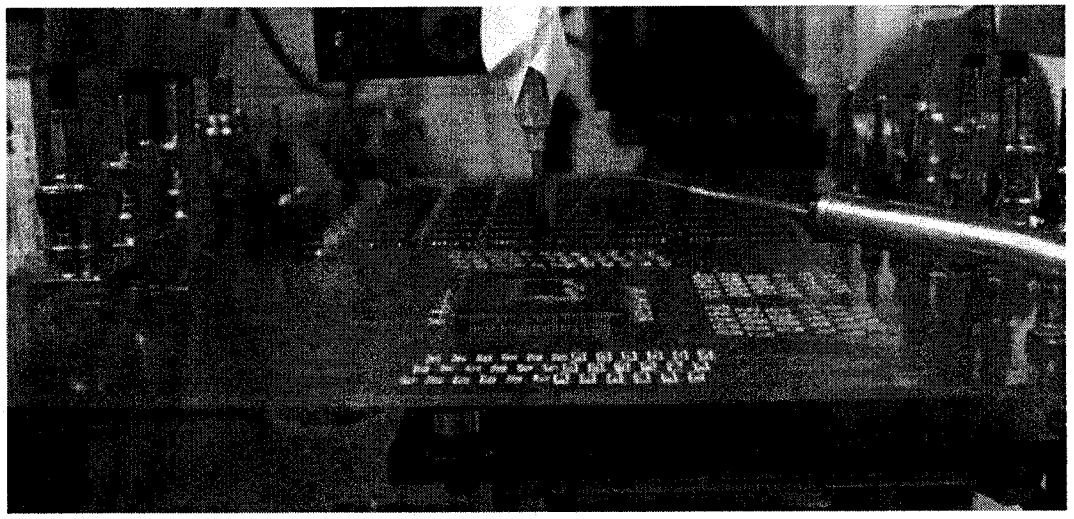


Figure 69. Photo of PCB for alternative chip designs

On the left and right hand sides of the board, there are high-voltage BNC connectors that are connected to 8 computer controlled power supplies. Each power supply is capable of generating 0 to 600 V, with a 1 mV resolution. Towards the bottom of the board is the ceramic chip carrier, with the unobstructed optical path for the 1-D ROPA design shown with the red arrows in Figure 68. Above the carrier is an array of 8 x 8 DIP switches that each contain 8 switches. The role of these DIP switches is to connect each one of the 64 electrodes on the EO crystal (or on the passive SiO_2 chip) to one of the 8 high-voltage power supplies. Because the DIP switches can be accidentally setup such that one electrode is connected to two or more power supplies, an on-board system of LEDs was developed that indicates when such shorts occur on the board. With this custom PCB, periodicities of 2 to 8 electrodes per period can be tested. To change the periodicity tested, the DIP switches must be manually reconfigured. This is somewhat time-consuming, but the simplest way to manipulate signals that can go over 300 V.

5.4 Optical testing of 2-D ROPA design

Shown in Figure 70 below is an overview of the setup in the lab used to test the 2-D ROPA design. The optical setup can be seen in the lower left. On the

shelf above the setup are the power supplies used. A computer running LabView, shown on the very right hand side of the image, is used to control the power supplies.

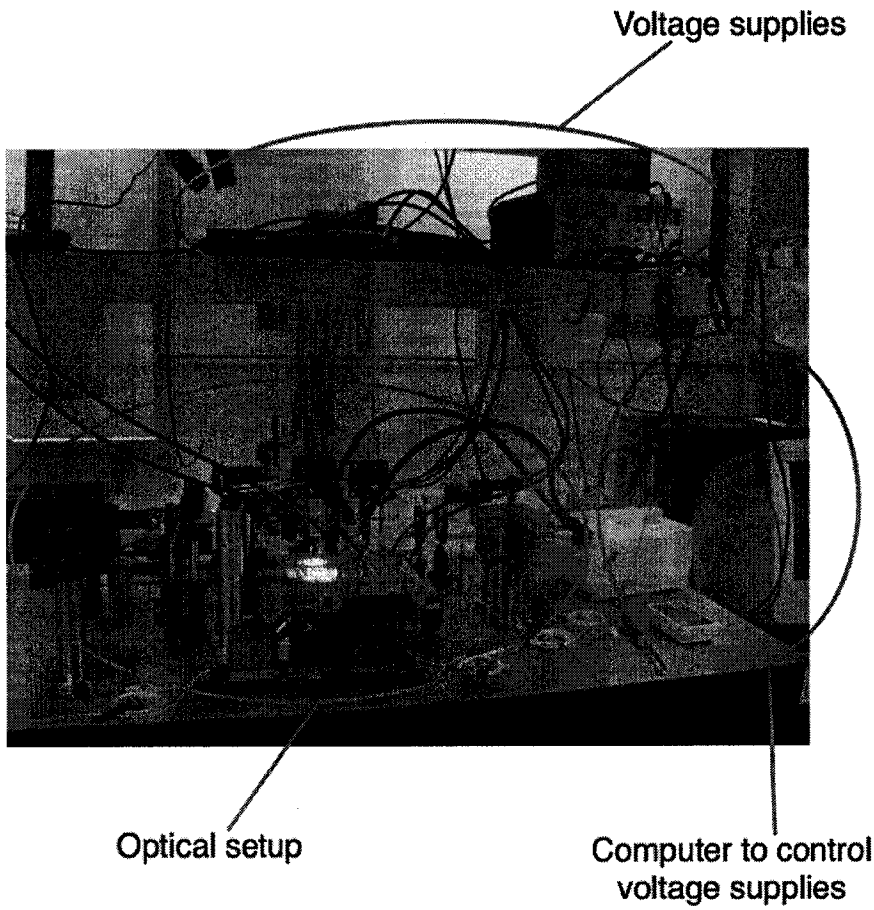


Figure 70. Overall view of testbed for 2-D ROPA design

Figure 71 is a close-up of the optical part of the setup. The red arrows indicate the optical path going from right to left. In Figure 72, the individual components that make up the optical path are highlighted.

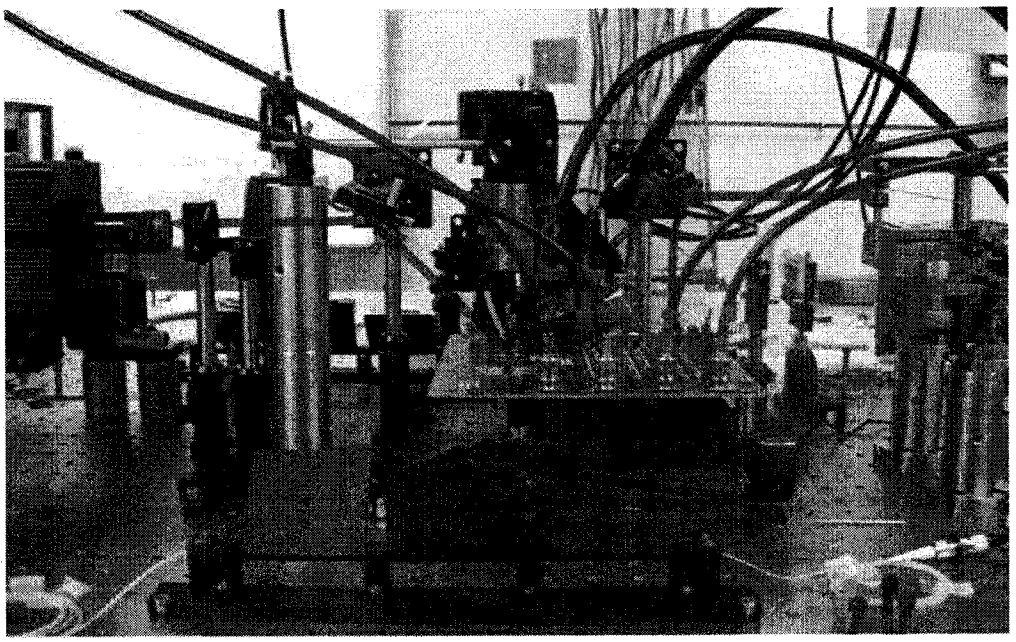


Figure 71. Light path through setup

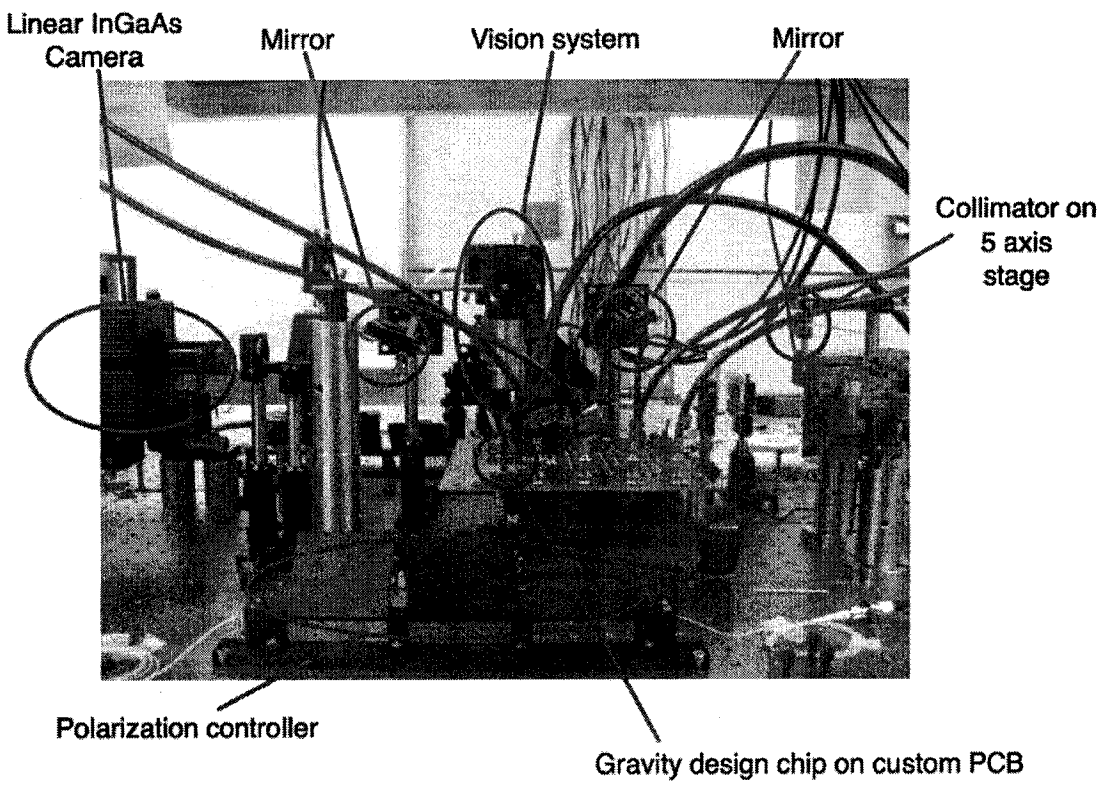
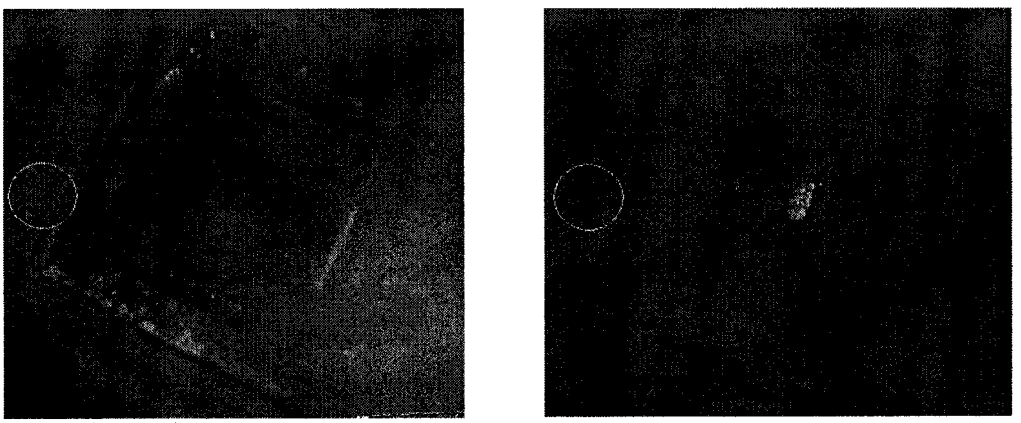


Figure 72. Components in testbed

The vision system in the center of the image above is used to verify the placement of the crystal when the passive chip that bypasses the electrode deposition is used. The placement of the crystal onto the packaged and wirebonded passive chip is done using a vacuum chuck mounted on a 3-axis stage (hidden behind the vision system on the photo). Care must be taken in order to not damage the wirebonds while placing the crystal.

Mirrors are used to control the incidence angle onto the device. In the photo, the light is incident at 50° onto the crystal. Between the second mirror (on the left) and the camera, there is a small flip-up mirror that is used to re-direct the light onto the polarimeter head, in order to verify the polarization state of the light. The beam waist at the crystal plane is 450 μm, and the beam waist at the camera plane is 490 μm. A 1° deflection of the beam through the crystal corresponds to a lateral displacement on the camera of 4.36 mm.

The image below was captured using the "vision system" and shows the crystal placed on the chip. The electrodes under the chip are visible as a dark rectangle in the center of the crystal. In Figure 73 b), the incident 1310 nm light can be seen in the center of the crystal. The vision system is thus also useful to align the input collimator to the crystal using its 5-axis stage.



(a) (b)

Figure 73. Vision system used to align light to grating, a) without input light from the collimator, b) with 1310 nm input light incident onto the crystal

The camera used to capture the images in Figure 73, as well as all of the infrared images in this chapter, is a linear InGaAs camera by Sensors Unlimited.

5.4.4 Reflection off the electrodes on the passive chip

Before depositing the crystal onto the passive chip using the vacuum chuck system, the beam reflecting off the electrodes on the passive chip was measured. The image captured using the InGaAs camera is shown in Figure 74 below. As can be seen in the figure, there is a slight diffractive effect due to the periodicity of electrodes.

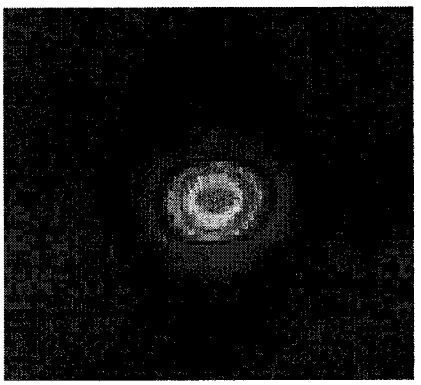
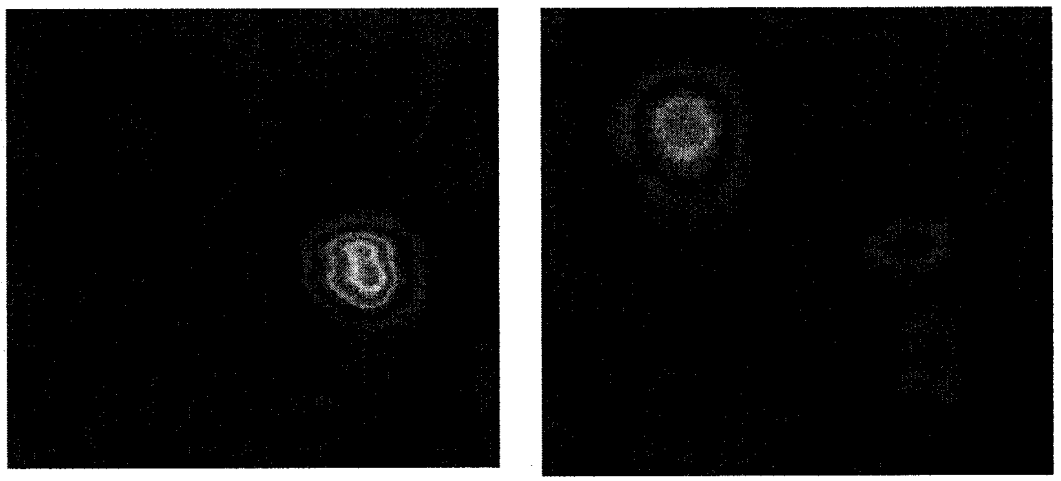


Figure 74. Light reflected off electrodes on passive chip

This spot is used as the reference beam for all insertion loss calculations for the 2-D ROPA optical testing.

5.4.5 Reflection off top surface of crystal

As was discussed in section 3.1.1, the light incident onto the 2-D ROPA design is close to the Brewster angle. The difference in reflectivity for TE and TM polarized light was measured experimentally. In Figure 75 we can see the two reflection spots off the device when the incidence angle onto the crystal is 70° ± 2°. The spot on the top left of both images is the reflection off the top surface of the $BaTiO_3$ crystal. The spot on the bottom right of the images is the reflection off the electrodes.



(a) (b)

Figure 75. Reflection off the top of the 2-D ROPA design for a) TM light, b) TE light

The power of the spots was measured using the camera itself, through the software used to control the camera. In the software, one can define an aperture on the active area of the camera and get a relative power measurement. The reflection off the top surface of the crystal is 8.75 dB greater when the light is polarized in TE configuration than when it is in TM configuration. Theoretically, the reflection should be 21 dB greater in TE configuration. It is to be expected that the experimentally measured difference between the TE and TM configurations will not be as large as the theoretical value. This is due in part to the finite extinction ratio of the incident beam (30dB), the difficulty in aligning the major axis of the extinction ratio of the beam to the crystal plane, the error in the control of the angle of incidence of the beam onto the top crystal surface, and the fact that the incident beam is a Gaussian beam rather than a plane wave.

5.4.6 Reflection of 0^{th} order mode

Before attempting to induce a grating in the crystal, the beam propagating through a $BaTiO_3$ crystal deposited onto the substitute passive chip was qualified. For these measurements, the electrodes were all grounded. The insertion loss of the crystal and the output profile of the beam varied greatly depending on the crystal quality, as can be seen in Figure 76.

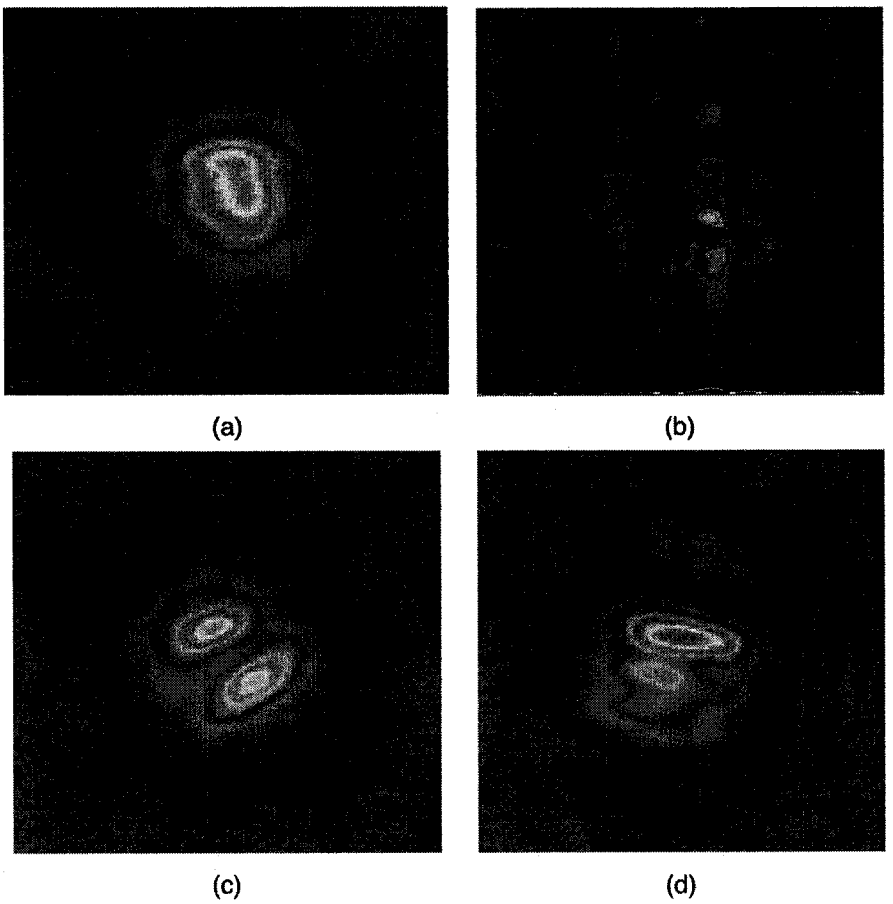


Figure 76. Beam propagating through four different $BaTiO_3$ crystals and reflecting off grounded electrodes

Figure 76 shows the 0^{th} order reflected spot going through four different $BaTiO_3$ crystals. The distortion of a beam gives an indication as to crystal quality. The best crystal is depicted in Figure 76 a), and the worst in Figure 76 b). The Insertion Loss (IL) of the beam through the four crystals is given in Table 13 below.

Table 13. Insertion loss for 0^{th} order reflected spot

Tested crystal	IL (dB)
a	1.89
b	22
c	3.4
d	4.2

For all four test results given above, the measured insertion loss was minimized by adjusting the location of the beam through the crystal. Evidently, there is a large variation in the initial crystal quality.

5.4.7 Beam deflection

In order to ground the top surface of the crystal, since the process and infrastructure is not yet in place to deposit the ITO electrode, a piece of copper tape was used instead. This is illustrated in Figure 77 below. A hole was cut in the copper tape just large enough for the incident beam of light, and the electrode was grounded using a probe tip mounted on a 3-axis stage. Though the electrode does not cover the entire surface of the crystal, the hole is not expected to have much of an influence on the electric field within the crystal. This is because the strongest E-field lines are near the electrodes along the bottom of the crystal.

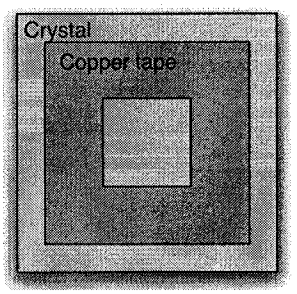
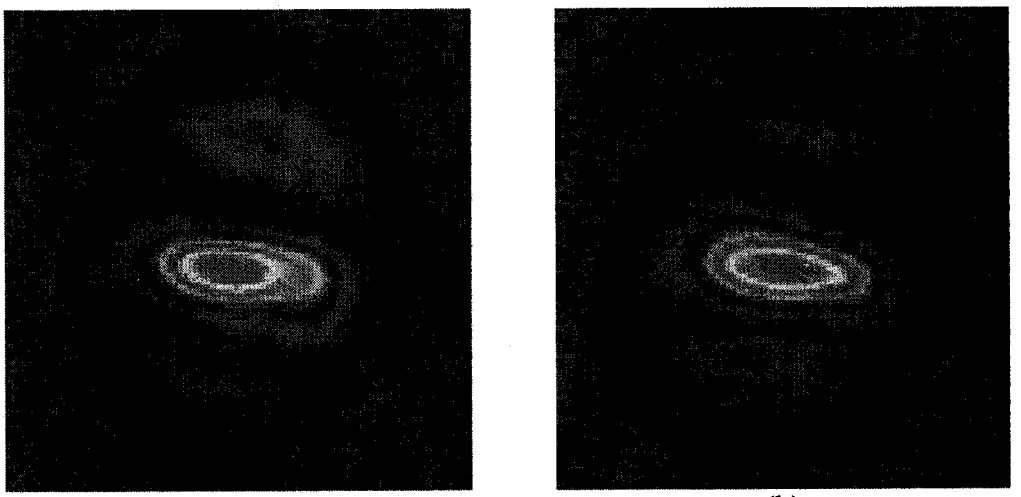


Figure 77. Top ground electrode for the 2-D ROPA

Multiple patterns of voltage were then applied to the $BaTiO_3$ crystals deposited onto the substitute passive chip shown in Figure 63. There was some deflection of the light going through the devices, but it did not correspond to the expected diffractive angular displacement. A typical example of the beam deflection is shown in Figure 78 below.



(a) (b)

Figure 78. Deflection of light through $BaTiO_3$ crystal in 2-D ROPA configuration

The image in Figure 78 a) shows the beam when no voltage is applied to the crystal. As can be seen in the image when compared to the free-space beam shown in Figure 74, there is some beam distortion due to the bulk crystal. The pattern of the distortion is very dependent on the location of the beam within the bulk crystal. When a periodic voltage pattern of 0, 100, 200, 300 V is applied across the electrodes, the resultant beam is shown in Figure 78 b). As can be seen in the figures, power did shift from the top of the image towards the bottom of the image. In order to analyze this phenomenon further, a vertical cross-sectional view of the power of the output beams for different voltage configurations is shown in Figure 79.

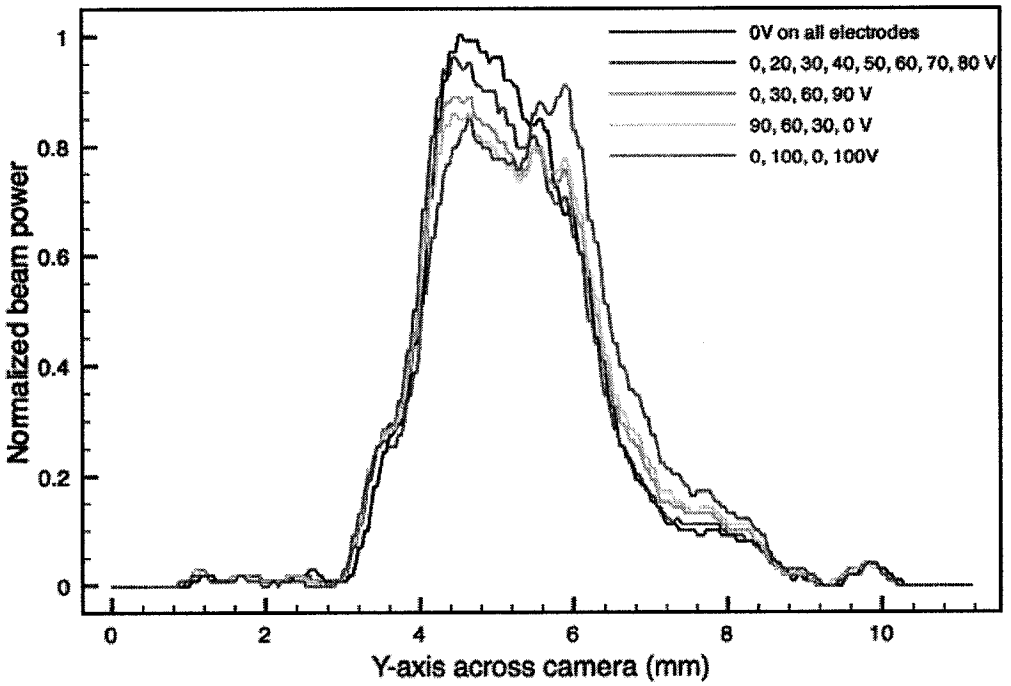


Figure 79. Cross-section of beam distortion

In the legend in Figure 79, the voltages given for each curve were periodically applied across all 64 electrodes. The voltage patterns were applied successively, and the output beam profile was captured for each voltage pattern. For none of the voltage configurations does the resulting beam distortion correspond to the simulated behavior. Instead, as the successive periodic voltage patterns were tested, the power of the output beam shifted downwards. This effect was cumulative, and disappeared after the electrode voltages returned to ground. This trend was visible regardless of the voltage pattern applied to the electrodes. This effect is therefore most likely not a diffractive effect, but refractive. However, identifying the exact cause of the distortion is difficult. Possible explanations include poor crystal quality, crystals that were not completely poled, crystals that were poled along the wrong crystal axis, crystals that were damaged or de-poled during handling and processing, misalignment between the electrodes and the crystal axis, and poor contact between the electrodes on the passive chip and the crystal.

5.5 Optical testing of 1-D ROPA design

The infrastructure used to test the 1-D ROPA is very similar to the one used to test the 2-D ROPA design. The same chip carrier, custom PCB, and two passive SiO_2 chips are used. A few differences are worth noting however. First of all, the crystal needs to be higher than the edges of the ceramic chip carrier so that the optical beam can pass through the crystal without being clipped. To do so, a spacer made of gold plated metal is used. This is shown schematically in Figure 80 below.

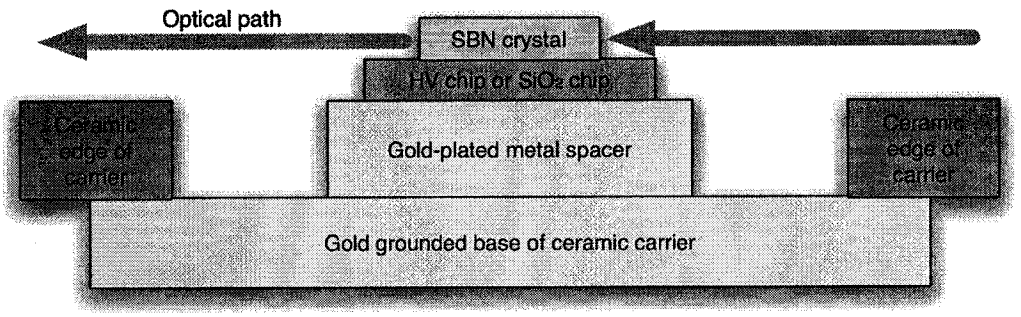


Figure 80. Spacer used to raise SBN crystal with respect to ceramic carrier

The chip is first glued to the spacer using a conductive epoxy, then the spacer is glued to the ceramic carrier using the same epoxy. The chip is then wirebonded to the spacer. Figure 81 below shows a photo of one of the passive SiO_2 chips already mounted onto the gold-plated metal spacer.

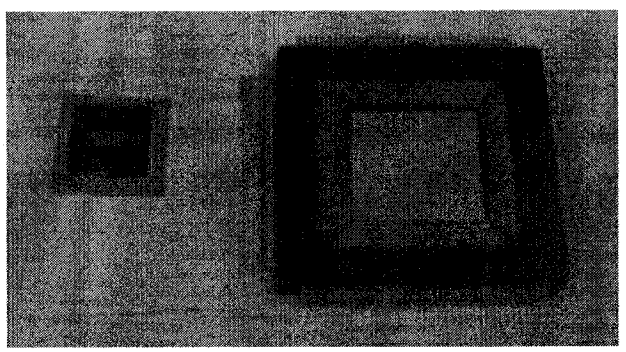


Figure 81. Chip mounted on metal spacer next to ceramic carrier

Figure 82 below shows the fully packaged flip-chipped SBN device, including the wirebonds from the passive SiO_2 chip to the ceramic carrier.

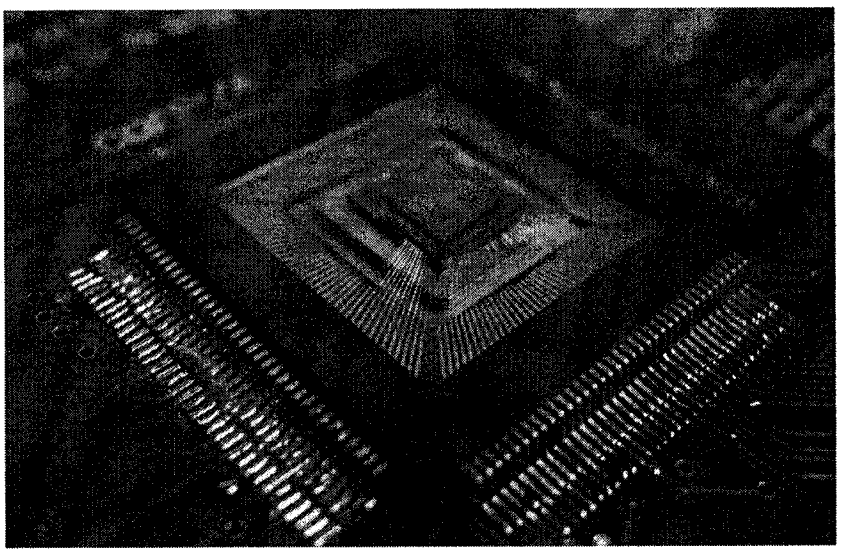


Figure 82. Packaged 1-D ROPA device

The optical setup to test the 1-D ROPA device is the same as was described in section 5.1.1 and as shown schematically in Figure 48. The input beam at the front surface of the crystal is elliptical with a waist of 760 μm x 120 μm. A photo of the setup is shown in Figure 83 below.

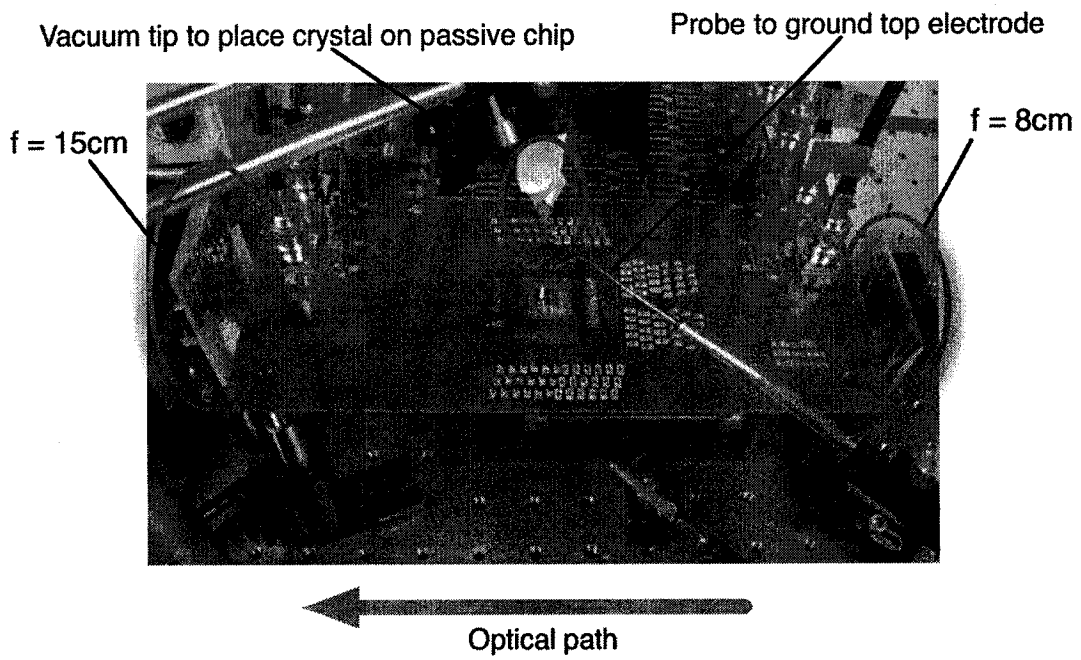


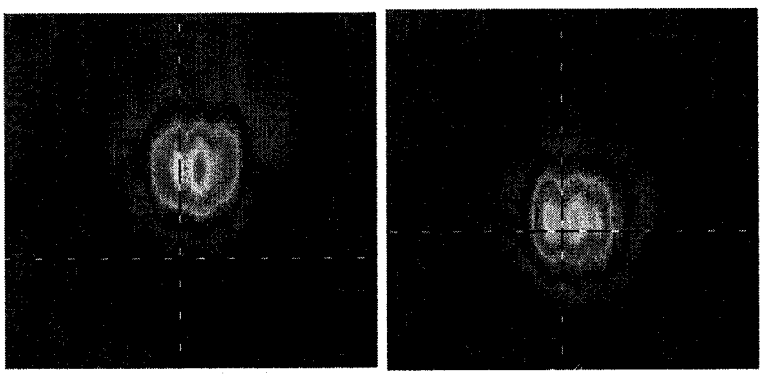
Figure 83. Setup for testing of 1-D ROPA design

The two cylindrical lenses are highlighted with red circles, as is the tip of the vacuum system used to place the crystal onto the passive SiO_2 chip. All of the electrical control is the same as for the 2-D ROPA optical test bed.

5.5.1 Beam deflection

The insertion loss of the SBN crystal with respect to the free-space beam when no voltage is applied is 1.8 dB. This is very close to the theoretical value of 1.61 dB that was calculated in section 3.2.4.

Two flip-chipped SBN devices were tested, as well as one SBN crystal deposited onto a passive SiO_2 chip shown in Figure 63. Since the electrodes for one of the flip-chipped SBN crystals were completely shorted together, and for the other crystal roughly half were shorted together, the same voltage was applied to all of the electrodes, while the top electrode was grounded. As the voltage on the electrodes was increased, the beam was deflected downwards towards the SiO_2 chip. In Figure 84 below, figure a) shows the output beam when the electrodes were grounded, and figure b) shows the beam when all of the electrodes were at 300 V. In figure b), the vertical beam translation corresponds to an angular deflection of 0.89°.



a) b)

Figure 84. Output beam of the 1-D ROPA device, a) 0 V applied to electrodes, b) 300 V applied to electrodes

Theoretically, if all of the electrodes are at the same voltage, there is a uniform electric field within the crystal that translates into a uniform change in

index of refraction. An increase in the index of refraction would slightly increase the Fresnel reflections off the two surfaces of the crystal, but should not cause a vertical deflection of the beam. One possible explanation for this behavior is that the electrode deposition process and flip-chipping caused stresses to build within the lower part of the crystal near the electrodes. Some evidence of these stresses was explored in section 5.1. Such stresses would cause a localized increase in the index of refraction, which would make the crystal behave like a graded-index lens. Applying a uniform electric field to such a device could accentuate the vertical deflection of the beam.

The same test was performed on a third SBN crystal that was just deposited onto the passive chip, without depositing electrodes on the crystal or flip-chipping the two together. The top ground electrode was created on the SBN crystal by putting a thin layer of conductive epoxy on the top surface of the crystal. The top electrode was grounded using a probe tip. When a uniform electric field was applied to the crystal, no vertical deflection was observed though there was some slight beam distortion. This supports the hypothesis that the electrodes are causing localized stresses in the crystal.

This third SBN crystal was also tested with periodic voltages applied across the electrodes. Regardless of the pattern of voltages applied, no clear horizontal beam deflection was observed. Once again, it is hard to determine the reasons for this behavior, especially given the small sample set of crystals available for testing.

5.6 Summary

This chapter presented the experimental work performed, both electrical and optical. First, the electrode deposition process was presented, and the reflectivity of the electrodes was measured. By observing the profile of a beam of light passing through an SBN crystal before and after the electrode deposition process, a slight diffractive effect could be observed, which leads to the conclusion that the electrode deposition process causes some strain within the crystal.

The testing of the high-voltage chip was then presented. To test the high-voltage chip, a custom PCB was made and a test bed was built that included temperature control of the chip. Of the four input scan chains on the chip, only one operated correctly. The 16 DACs controlled by that scan chain were tested, and were all capable of providing 64 analog output voltages, but the minimum output voltage of the DACs was close to 50 V.

Since the high-voltage chip was only partially functional, two alternative passive SiO_2 chips were developed to optically test the performance of the ROPA devices. One of the chip designs is compatible with the flip-chip process and effectively acts as a connector between the flip-chip points and wirebond pads. This chip design was used to flip-chip two SBN crystals, but many of the electrodes were shorted. The other chip design eliminates the need to deposit electrodes on the EO crystal by placing the 64 electrodes on the SiO_2 chip. The EO crystal is then deposited onto the passive chip and is held in place by gravity. This design is the simplest, but good physical contact between the bottom surface of the crystal and the electrodes is not guaranteed.

Two optical test beds were also built, one to test the 2-D ROPA design, and the other to test the 1-D ROPA design. Unfortunately, in neither case was any clear diffractive effect visible when periodic voltages were applied to the crystal. There are many possible reasons for this behavior, two of the most probable ones being poor crystal quality, and not generating the expected electric fields within the crystals due to poor physical contact between the EO crystal and the electrodes on the passive chip beneath it.

CHAPTER 6. CONCLUSIONS AND FUTURE WORK

The successful completion of a ROPA optical switch will provide a 1xN fast optical switch as well as demonstrate the successful integration of a high-voltage CMOS chip with an electro-optic crystal. To our knowledge, there are currently no experimentally demonstrated bulk electro-optic switches that operate with voltages as low as 300V. Also, there are no electro-optic switches that have made use of flip-chipping technology to control the voltages using a CMOS chip. Such a heterogeneously integrated switch could be used in an AAPN environment, which requires a high port-count optical fabric with low-loss and fast switch times.

Two different ROPA designs were presented: a 2-D ROPA switch and a 1-D ROPA switch. Both switches are designed to be 1x6 optical switches, controlled through flip-chipping by the same high-voltage CMOS chip. The choice of electro-optic crystal for each configuration was discussed within the context of providing a 2π phase shift of the incident light with electrode voltages no greater than 300 V. The electrode dimensions were chosen to prevent voltage breakdown while maximizing diffraction efficiency, and while being compatible with the flip-chipping process. The metal stack-up chosen for the electrodes is reflective at telecom wavelengths, adheres well to both EO crystals, and is sufficiently thick for flip-chipping.

The optical performance of the ROPA devices was simulated using rigorous coupled wave analysis and the diffraction efficiencies were maximized through an iterative simulated annealing algorithm. The complex index profile induced within the crystal was segmented both vertically and horizontally into slices of uniform index. The index profile for the 2-D ROPA structure was further unfolded to assure that there would be a single refractive index value within the crystal at every point. The 1-D ROPA structure was simulated a single horizontal slice at a time, and an overlap integral with a Gaussian beam was performed to calculate the total diffraction efficiency for a particular voltage profile.

The ROPA design exploits the new mixed high and low-voltage transistor process developed by DALSA Semiconductors. The overall high-voltage chip architecture consists of an array of 64 transistors. Each DAC has a thermometer-coded architecture consisting of 64 identical current cells. The sum of the currents from the current cells undergoes a current-to-voltage conversion using a high-compliance current mirror. This method of current-to-voltage conversion was chosen in order to minimize the number of high-voltage transistors used, and to thus minimize the area of the die. The layout of the chip took into consideration the optical path of the light for the 1-D ROPA, and the flip-chip pads were placed in the center of the chip for mechanical robustness of the final device. When experimentally tested, a single HV transistor performed as simulated. Only one of the four scan input scan chains was functional, and the minimum output voltage of a DAC was roughly 50V. This lead to the development of two alternative passive SiO_2 chips (and a corresponding custom PCB) that were used to test the optical performance of both the 1-D and 2-D ROPA devices.

The process that was developed to deposit the electrodes was presented, and the electrodes were successfully deposited onto EO crystals. The reflectivity of the electrodes was then measured.

When testing the 2-D ROPA device, the insertion loss due to the bulk crystal was measured, as well as the reflection off the top surface of the crystal. When applying periodic voltages across the crystal, the output profile of the beam did change, but not in a way that would be consistent with the simulated performance. Similarly, when testing the 1-D ROPA device, vertical deflection of the beam was measured, but no measurable horizontal deflection.

6.1 Future work

Much work is still required to build a fully functional ROPA device. However, the ground work in terms of design, simulation techniques and algorithms, development of a process for the electrode deposition, and building of optical test beds and custom PCBs has been done.

An essential component to any future work on the ROPA project includes partnering with material scientists to better determine initial crystal quality and to develop in-house poling methods. Developing a testbed to screen the initial crystals would greatly increase the odds of building a fully functional device. Also, there should be an ongoing investigation into alternative electro-optic materials that are more robust and easier to manufacture.

An interferometric testbed should also be built to directly measure the induced index profile within the crystal. A much clearer understanding of the optical behavior of the devices could thus be obtained.

In order to improve the performance of the high-voltage chip, a second chip should be designed and fabricated. This chip would consist mostly of test circuitry geared towards getting a better understanding of the process variations and their effect on the performance of the circuitry.

The electrode deposition process has been successfully developed, but the ITO deposition process still needs to be explored for the 2-D ROPA device. As with the electrode deposition, the temperature of the crystals has to be carefully controlled during all of the processing steps, and additionally the transparency or insertion loss of the final top electrode would need to be characterized.

It is the opinion of the author that the field of optical switching is very rich, with a lot of room for innovation. The concept of the ROPA device is inherently flexible, and just two of the many possible variations of reprogrammable diffractive optical elements were explored. The work presented in this thesis has built a foundation on which much research can be done and from which new optical devices may emerge.

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