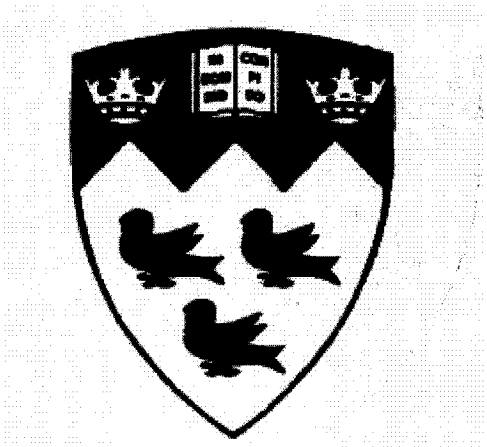
Design of a Fully Integrated Array of High-Voltage Digital-to-Analog Converters

Ehab Shoukry
Department of Electrical and Computer Engineering
Photonic Systems Group
McGill University



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ABSTRACT

This thesis presents the first fully integrated array of high-voltage (HV) digital-to-analog converters (DACs). It was designed in DALSA Semiconductor's 0.8μm CMOS/DMOS HV process technology. The 6-bit 300V DACs are based on a current-steering, thermometer coded architecture. Two designs adapted to the HV technology are proposed for the current-to-high-voltage conversion as traditional output resistor or op-amp solutions are not optimum for the HV process: one uses a high-compliance current mirror, while the other uses a simple current mirror. The DACs show a DNL of 0.16LSB and 1LSB, respectively, while the INL profile is 0.16LSB and 13LSBs for the first and second designs. The array is suited for applications requiring a set of digitally-controlled high-voltage signals.

SOMMAIRE

Cette thèse fait l'objet d'une première conception de matrice à convertisseurs numérique-analogue à haute tension sur circuit intégré. Ce projet fut conçu grâce à la technologie 0.8μm CMOS/DMOS HV de DALSA Semiconducteur. Les convertisseurs à 6-bits de 300V sont basés sur une architecture thermomètre en mode-courant. Deux circuits adaptés à la technologie sont proposés pour établir la conversion du courant à un signal haute tension : un utilise un miroir de courant à haute conformité tandis que le second comporte un miroir de courant classique. Les convertisseurs démontrent un NLD de 0.16LSB et 1LSB, pour la première et la seconde conception, respectivement. Le premier circuit démontre un profil NLI de 0.16LSB tandis que le second exhibe un profil de 13LSB. La matrice convient bien pour des applications qui requiert un groupe de signaux à haute tension contrôlé numériquement.

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Finally and most importantly, this thesis is dedicated to my Father in heaven, to whom all thanks, glory and honor are due.

CHAPTER 1 INTRODUCTION

1.1 MOTIVATION & BACKGROUND

The use of high-speed communications has proliferated over the last decade. The Internet has become a ubiquitous aspect of daily life, driving the growth of data traffic. Users are constantly adopting applications that require larger bandwidths in order to speed up data transfer. As broadband communications over the Internet gains popularity, bandwidth-on-demand becomes increasingly important to accommodate for the bursts in data traffic, videoconferencing and other 'anytime, anywhere' multimedia necessitating the development of highly flexible, intelligent networks [1].

Current optical networks still rely on electronic signals; optical signals must be converted into electrical ones in order to be regenerated, amplified or switched before being converted back into an optical signal. These optical-to-electrical-to-optical (OEO) conversions are the real bottlenecks in today's optical communications networks as they add greatly to the costs of network operation, require large amounts of power, and limit scalability. Minimizing or eliminating the OEO conversions in the data path will bring the photonic edge closer to the end user. All-optical networks will replace the electronic switches by optical ones, thus eliminating the need for OEO conversions. Evidently, the result is smaller switches and cost reduction as the expensive high-speed electronics used for signal processing are no longer required. To achieve this goal, a number of enabling technologies are currently being researched, including liquid crystals [2], [3], [4], holographic crystals [5], semiconductor amplifiers [6], micro-electro-mechanical systems (MEMS) [7], [8] and high-speed Electro-Optic (EO) switching technology [9], [10].

As part of a nation-wide, NSERC funded program, the Agile All-Photonic Network (AAPN) is researching the possibility to develop an all-photonic network core that could potentially stretch very close to the end-user by dramatically reducing

optical/electrical conversions [1]. Ideally, an optical switch in an Agile All-Photonic Network (AAPN) should:

- be fast – AAPN targets a switching speed below 1μs [11]
- be highly scalable – requires low insertion loss
- have a high port count – a 64x64 switch is targeted
- be transparent to the bit rate
- be non-mechanical for high reliability purposes

Among the technologies enumerated above, electro-optic switches hold the greatest promise to achieve the desired characteristics of an AAPN. The other technologies are either fast with low port counts (e.g. holographic: 8x8 ports with nanosecond switching) or slow and large (e.g. MEMS: 256x256 ports with millisecond switching).

1.1.1 ELECTRO-OPTIC SWITCHES

Electro-optic switches are fast, as their speed is mainly limited by the electric field switching speed. It is based on the electro-optic effect in which an electrical voltage applied to the device changes the substrate's index of refraction, thus directing the light to the desired output port. Waveguide structures have been used to implement electro-optic switches but are limited by high losses. On the other hand, bulk electro-optic crystal structures present low insertion losses but require a higher voltage level to steer the beam.

In [12] and [13], we present two different types of bulk electro-optic switches: the former is refraction-based and the latter is based on total internal reflection (TIR). In the refraction-based switch, a series of prism based devices slightly bend the light at each interface when an electric field is applied. Conversely, when no voltage is applied, the laser beam passes directly through the prisms. These two scenarios are shown in Figure 1.1. The different regions, or prisms, are obtained through poling. Once the voltage is applied, the un-inverted region increases in index, and the inverted one decreases, thus creating a large change in index of refraction, changing the light's trajectory.

In the case of a TIR switch, the idea is to have a light signal incident at a grazing angle onto an electro-optic boundary. Similar to the refraction-based switch, when no voltage is applied, the beam passes straight through but is reflected once an electric field is applied. Figure 1.2 shows the 3 port device reported in [13]. When no E-field is applied to the first or second EO device, then light passes straight through (Port 3). When a voltage is applied on both devices, then both will reflect the beam, steering it to port 1. Finally, when the first device is on and the second is off, port 2 becomes the output of interest.

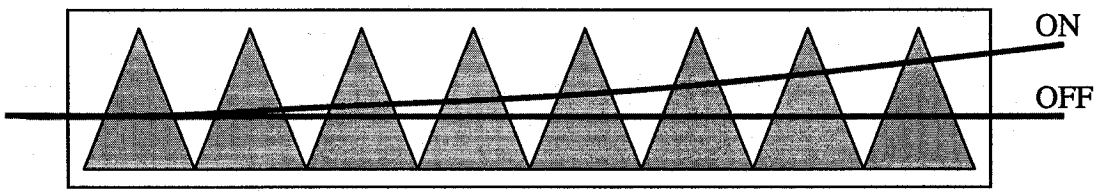

Figure 1.1: Refraction based prism scanner [14]

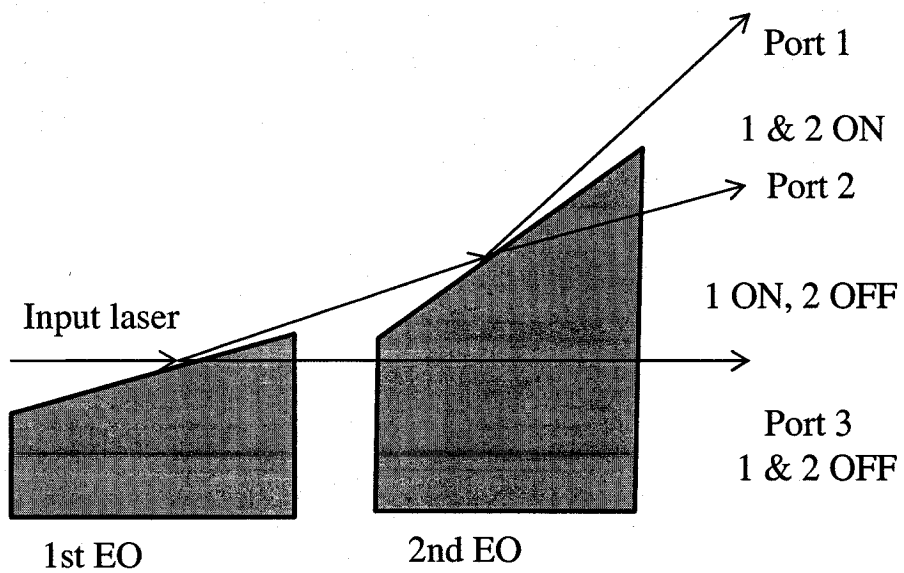

Figure 1.2: 1x3 TIR switch [13]

In both of these designs, electric fields in the range of 1200V were required. In [15] an optical switch that is both fast and that uses voltage levels that are less than 300V is proposed.

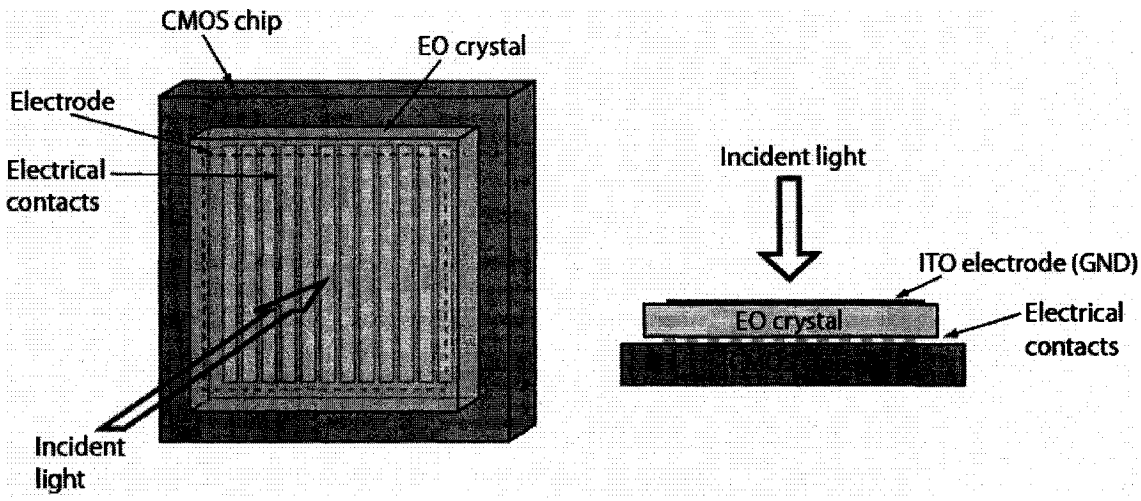

Figure 1.3: 1-D Optical Phased-Array [15]

The operating principle of the design relies on the application of multiple electric fields of varying magnitudes across an electro-optic material to create a diffractive optical element. Here, the properties of the diffractive optical element can be controlled by the configuration of the electric fields. The resulting device is known as a Reprogrammable Optical Phased Array (ROPA) or a reprogrammable diffractive optical element [16].The design, simulation, fabrication and testing of an integrated circuit providing the required large tunable electric fields is the focus of this thesis. The EO device will be flip-chipped to the high voltage CMOS chip, thus creating a fully packaged EO switch along with its associated drive electronics.

1.2 RESEARCH CONTRIBUTIONS

System integration of high voltage, analog and digital circuitry on a single die becomes attractive for these applications, as this results in reliability, cost and size improvements. Digitally controlling the high-voltage (HV) signals lays the foundation for

the miniaturization of many devices. To address the EO devices' voltage requirements, this thesis presents the design of the first fully integrated array of high-voltage (HV) CMOS/DMOS digital-to-analog converters operating from 0V to 300V. The design was done using DALSA Semiconductor's 0.8um HV process technology. The DAC array will be used for electro-optic switching applications, though the design may be tuned to accommodate a wide range of applications. For instance, by slightly changing the design, the chip may be used to supply the high-voltages required by MEMS applications. The complete design, packaging and testing of each DAC unit as well as the complete chip are presented. Methods for ensuring proper heterogeneous integration through flip-chip bonding are analyzed and a solution is provided. This heterogeneous device will be used to create a very fast 1xN optical switch for use in an agile all-photonic network. By exploiting the fine feature sizes of the electrodes that are possible through flip-chipping, and by having access to voltages up to 300V, the final optical switch will be faster and of better performance than any existing electro-optic switch.

1.3 THESIS ORGANIZATION

This thesis will start with a background on DAC Architectures in Chapter 2, followed by an overview of high-voltage technology in Chapter 3. Chapter 4 will present the design, layout and simulation of the HVDAC. This includes the theoretical background and justification for some of the design decisions. It will also present a means of providing a current-to-high-voltage conversion, as typical current-to-voltage conversions are not suitable for this HV technology. Some of the layout challenges are also discussed in this chapter. Simulation measurements such as DNL, INL and settling time are conducted to characterize the converter design. The test plan, packaging and experimental testing are examined in Chapter 5.

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CHAPTER 2 DIGITAL TO ANALOG CONVERTERS

Digital devices have increased in popularity over the last decades because of their ease of fabrication and their relatively low cost. However, 'real' world signals are typically represented by analog signals. As a result, digital-to-analog converters have become crucial circuit components as they are found in many devices performing a wide range of applications, providing a link between the digital and analog sections of a system. The ability to take a set of digital inputs and transform it to an analog output has found widespread use in the fields of telecommunications, instrumentation, control and many other areas. There are many different types of DAC architectures, each with certain strengths and weaknesses suitable for the different applications at hand. Section 2.1 will discuss the performance specifications of DACs. Section 2.2 will present the resistor string architecture and will be followed by section 2.3 which describes the charge redistribution topology. Finally, section 2.4 will describe the current steering DAC.

2.1 DAC PERFORMANCE MEASUREMENTS

In comparing digital-to-analog converters, certain figure of merits need to be considered to make a proper analysis. In this section, some of these important static and dynamic performance measures are presented.

2.1.1 MONOTONICITY

A monotonic DAC refers to one in which each voltage in the transfer curve is larger than the previous, assuming a rising voltage ramp for increasing codes [1]. In other words, as the input increases, the output also increases. The slope of a monotonic DAC

will always be of the same sign. As an example, the behaviors of a monotonic and a non-monotonic DAC are shown in Figure 2.1.

2.1.2 DNL

DNL or differential nonlinearity refers to the variations of the step size between successive code transitions from the ideal 1 LSB. For example, a DNL of 0.2 LSB would mean that the step size may vary from 0.8 LSB to 1.2 LSB.

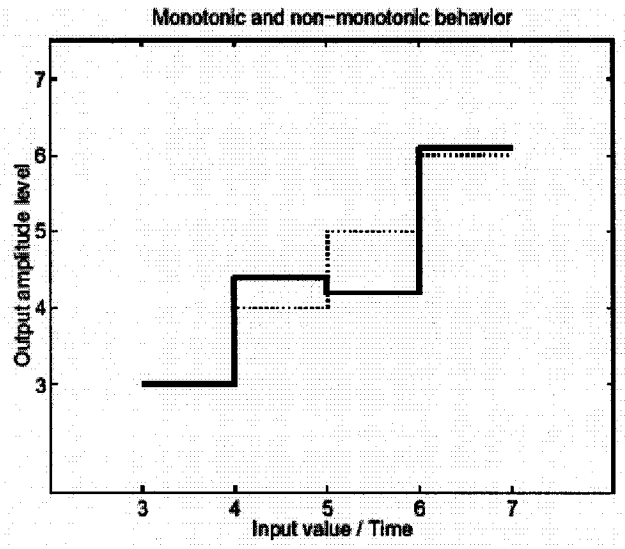

Figure 2.1: Monotonic (dashed line) vs. Non-Monotonic (solid line) DAC Output [2]

2.1.3 INL

INL or integral nonlinearity refers to the variations between the DAC output curve and a reference curve. The reference line may be one of the following three: the ideal line, the best-fit line or the endpoint line. The ideal line is, as its name implies, a line representing the ideal DAC transfer curve. The best-fit line represents the closest approximation to the data converter's actual transfer function by use of a straight line. Finally, the endpoint line is one in which the two DAC endpoints from the actual transfer curve are used to form a straight line.

2.1.4 RESOLUTION

The resolution of a digital to analog converter is defined as the change in analog steps with respect to the reference voltage V_{ref}. In other words, it refers to the number of digital input bits and its corresponding analog step sizes. An N-bit DAC would have 2^N analog outputs.

2.1.5 SETTLING TIME

Ideally, when the input codes change, the DAC analog output would automatically change to the desired value. However, due to circuit parasitics and other imperfections, DACs have a conversion time defined as the time it takes the DAC to reach the final value within a specified error band. For example, a DAC may have a settling time of 1μs to settle to 0.1% or 1% of the final value or of the full-scale range [1]. Figure 2.2 shows an example of an ideal DAC's behavior in dashed lines and its actual behavior in solid line.

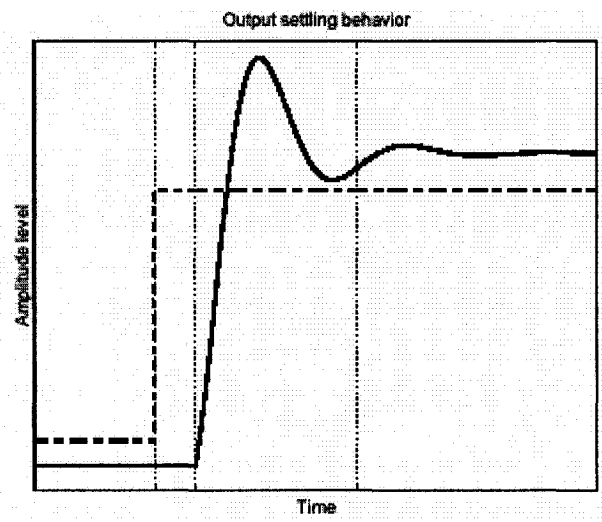

Figure 2.2: DAC Settling Time [2]

2.1.6 GLITCH

Glitches occur when all the bits in a binary weighted DAC do not switch simultaneously. The result is that for a short period preceding the settling of the code, the

output of the device presents a false code. The following example illustrates this point. We assume the following code transition:

$$0111\ldots1111 \rightarrow 1000\ldots000$$

In a situation where the MSB switches faster than the LSBs, the code 1111...111 will appear for a short time before the complete transition occurs. This code represents the maximum value and causes a large glitch to occur at the output. The glitch adds a signal dependent error to the output, significantly degrading the performance [2].

The preceding list of static and dynamic measurements forms a basis for quantifying DAC performances. Each DAC architecture has its advantages and disadvantages, some having better static performance, others better dynamic performance while others may be more cost-efficient. The following is an overview of some of the main architectures.

2.2 RESISTIVE DIVIDER DAC

One of the simplest DAC architectures is the resistive divider DAC. In this approach, for an N bit DAC, a series of 2^N resistors are switched to produce a set of voltages evenly spaced between the two rails [3]. In the 8 bit example shown in Figure 2.3, the digital inputs are encoded into 256 control bits. These in turn determine which switch turn on, thus connecting the voltage to the analog output buffer. This encoding scheme is referred to as a thermometer coded scheme. It utilizes a number of equally weighted elements such that the voltage drop across each resistor is the same.

One of the advantages of this scheme is that the DAC is inherently monotonic. For the resistive divider, this is explained by the fact that the voltage output of a resistor must be lower than the voltage tap of the resistor above it. The architecture discussed thus far uses a thermometer encoded scheme. This scheme becomes less attractive for higher resolution DACs [4]. Increasing the DAC resolution by 1 bit results in doubling the number of resistors on-chip. A more efficient use of silicon area for these higher

resolution DACs is the binary weighted approach. Binary-weighted resistor converters are popular for bipolar technology [3] but not as well suited for CMOS technology. As its name implies, each of its circuit elements is given a binary weight such that the output amplitude is given by a one-to-one mapping of the input signal, with a weight distribution given by:

$$b_i = 2^{i-1} \text{ for } i=1,2\ldots,N, \text{ where N is the number of bits}$$

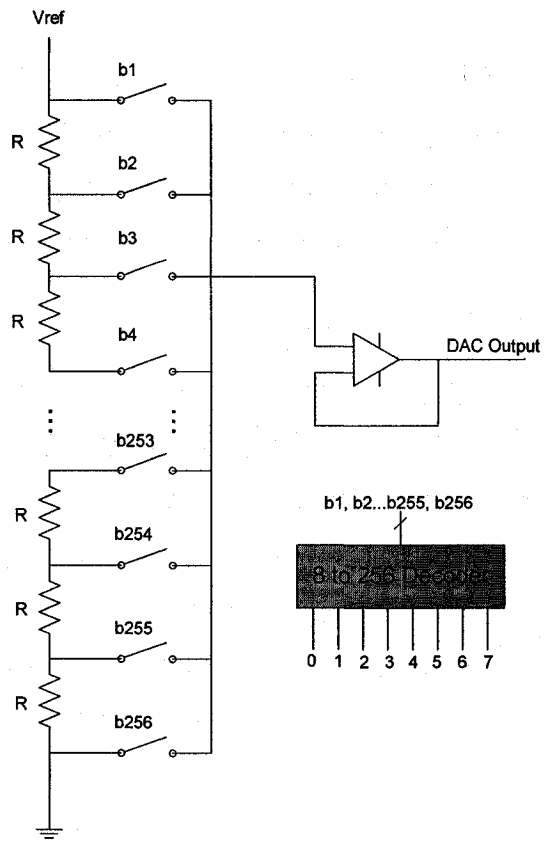

Figure 2.3: 8-bit Resistor-String DAC

Thus, for the 8-bit DAC discussed earlier, 8 resistors would be required in a binary-weighted topology instead of the previously used 256. Despite its simplicity, one of the major drawbacks of the resistor string architecture is the difficulty to match resistor values because of process variations, making this architecture suffer from poor accuracy.

2.3 CHARGE REDISTRIBUTION

The charge redistribution architecture is usually seen in a binary weighted form though thermometer coded structures may also be used. The concept is to connect an array of binary weighted capacitors to an op-amp. The bottom plates of the capacitors may switch from V_{ref} to ground while the top plates are connected to the amplifier. The operation of this topology is divided as follows. First, during the reset stage, the bottom plates are connected to ground, thus discharging the capacitors. During the charging phase, the digital input codes connected to the switches are changed while the inputs of the capacitors are connected to ground. Finally, V_{ref} is applied to the capacitors according to the digital input code. A simplified 4-bit example is shown in Figure 2.4 with an illustration of the different stages, in which the final output value will be $\frac{12}{16}V_{ref}$. Clearly, the timing and the digital control logic for the charge redistribution DAC is complex [3]. Just as for the resistor ladder structure, mismatches caused by process variations occur, making it difficult to obtain great accuracy. In addition, an important consideration in designing this type of DAC is the available chip area, as capacitors in CMOS technology take a great deal of space. In cases where speed and size are not critical, this architecture could be used [5].

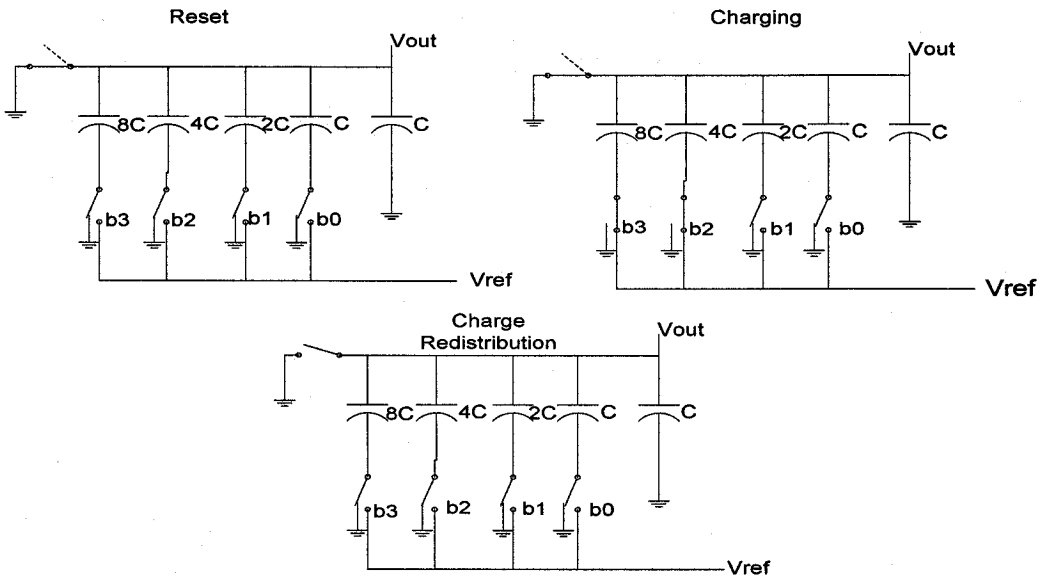

Figure 2.4: Charge Redistribution DAC - 4bit example [6]

2.4 CURRENT-STEERING DAC

Current-steering digital-to-analog converters are often used for high speed conversions [4], [7], [8], [9]. Lin and Bult designed a 10 bit, 500MSamples/s DAC based on this architecture in 1998. They present a thorough study on its design in [4]. A 1GSamples/s complete study was also presented in 2001 by Van den Bosch et al. in [9]. These topologies are well suited for the CMOS process, as all the components (current sources, switches...) are easy to make. The concept, as its name implies, is to steer current to the output branch according to the digital input code. Like the other architectures, this topology may be designed using the binary weighted approach or the thermometer coding scheme (Figure 2.5). In the latter case, each current branch produces an equal amount of current when it is turned on according to the thermometer code. This type of DAC has a good DNL error in addition to being monotonic and its linearity is not affected by glitches. Its major drawbacks are the large area consumption and its complexity [9].

On the other hand, in the binary DACs, each branch produces twice the current of the previous branch. It is therefore much simpler since no digital decoding structure is necessary to control the switches in addition to requiring less area. However, the DNL error is larger and the glitches influence the linearity of the converter. This topic is thoroughly analyzed and explained in [4].

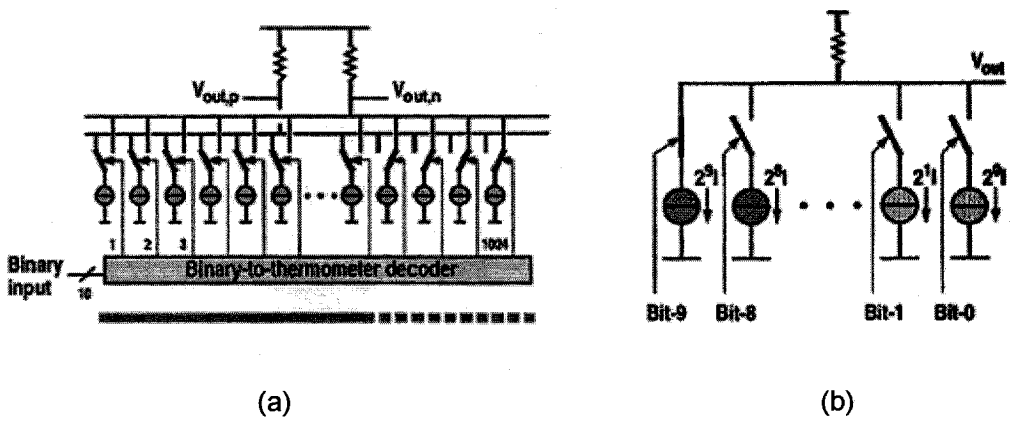

Figure 2.5: (a) Thermometer and (b)binary current steering DACs [4] (©1998 IEEE)

Briefly, as depicted in Figure 2.6, the size of the glitch in a thermometer coded DAC is proportional to the number of switches that are turned on, which in turn makes the glitch proportional to the step size. This is not the case for a binary design, thus affecting its linearity.

In order to take advantage of the good static performance of a thermometer coded DAC and the reduced chip area of a binary weighted design, high-resolution DACs often use a segmented current steering topology. In a segmented design, the most-significant bits are thermometer coded while the least significant bits are binary weighted. These structures are discussed in great length and optimal segmentation techniques are offered in [2], [4], and [9].

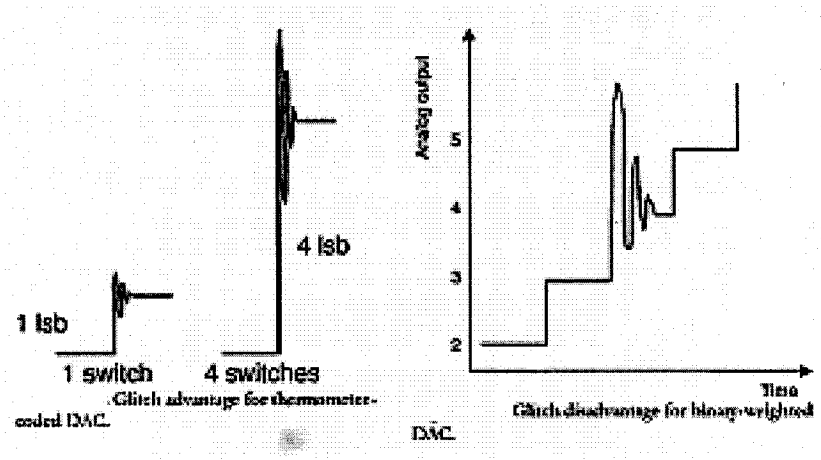

Figure 2.6: Glitch advantage of a thermometer coded DAC [4] (©1998 IEEE)

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CHAPTER 3 HIGH-VOLTAGE TECHNOLOGY

The number of transistors on integrated circuits (IC) has been on the rise since its inception. Though IC sizes may grow, the trend has resulted in the reduction in feature size of the integrated components. This scaling of technology results in advantages of increased speed, lower operating voltages and therefore lower power consumption. However, many applications require high voltages, notably intelligent motor control, biomedical applications [1], flat panel displays and optical switches including MEMS and electro-optic devices. Several high-voltage semiconductor manufacturers provide customers with high-voltage levels ranging from 10V to 600V. Amongst these foundries are the likes of Micrel Semiconductor [2], Ami Semiconductor [3], TSMC [4] and DALSA Semiconductor [5]. In selecting the foundry, the maximum breakdown voltage was the deciding factor. Micrel's technology could operate at up to 150V, Amis'limit is set at 100V whereas TSMC's process could accommodate circuitry operating at 40V. DALSA Semiconductor provided the required electric fields for functional operation of the electro-optic devices, offering two possible technologies that could supply the large voltages: 2um, 600V CMOS/DMOS technology and the 0.8um, 300V CMOS/DMOS technology. The latter was chosen due to the reduced area consumption in both the low-voltage and high-voltage sections.

3.1 HIGH-VOLTAGE MOSFETS

Among the several existing high-voltage MOSFETs, the Double Diffused Metal Oxide Semiconductor (DMOS) transistors are the most commonly used. Within this group of devices, there are two types of designs: the Vertical DMOS (V-DMOS) and Lateral DMOS (LDMOS). In the vertical device, the current begins flowing once a gate voltage greater than the threshold voltage is applied. As shown in Figure 3.1, the current

flows laterally from the source and then vertically from the top contact to the drain contact on the bottom as indicated by the arrows. Thus the wafer's silicon is used to withstand the high-voltages of the device. Since the substrate and the drift region are one in this case, it is difficult to implement other transistors on the same substrate [6], [7].

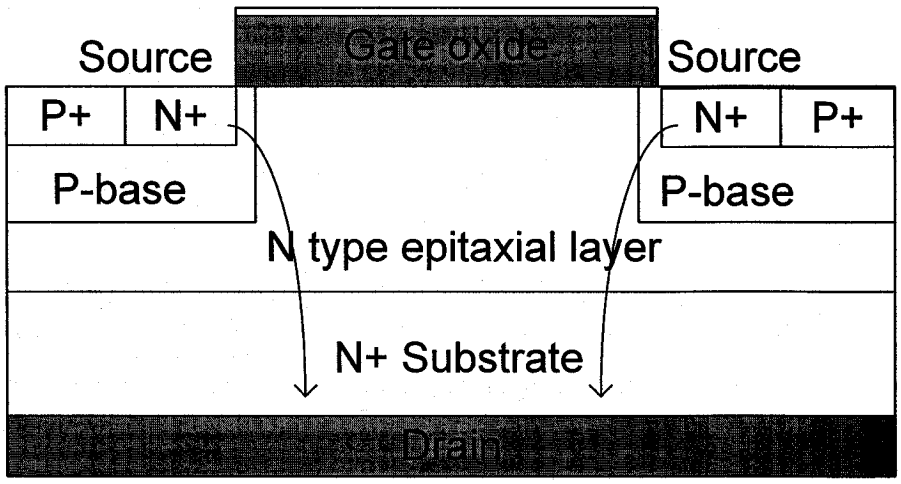

Figure 3.1: Vertical DMOS

The LDMOS corrects these deficiencies by having all the contacts on the same side. Thus, current flows laterally from the source to the drain. A technique called RESURF, which stands for reduced surface field [8], makes it possible to have these lateral high-voltage devices on a normal substrate. Therefore, LDMOS structures may be integrated with low-voltage logic.

The RESURF technique allows drain breakdown voltages of up to 600V [6], [7], [9]. In an n-type DMOS device as in Figure 3.2, a lightly doped P-Top region inside the N-Well is used in between the P-base and the drain in order to withstand the high drain-source voltage. For high drain voltages, this extra P-Top layer will deplete the drift region from above while the substrate depletes it from below, thus greatly increasing the total N-well charge that may be supported [9].

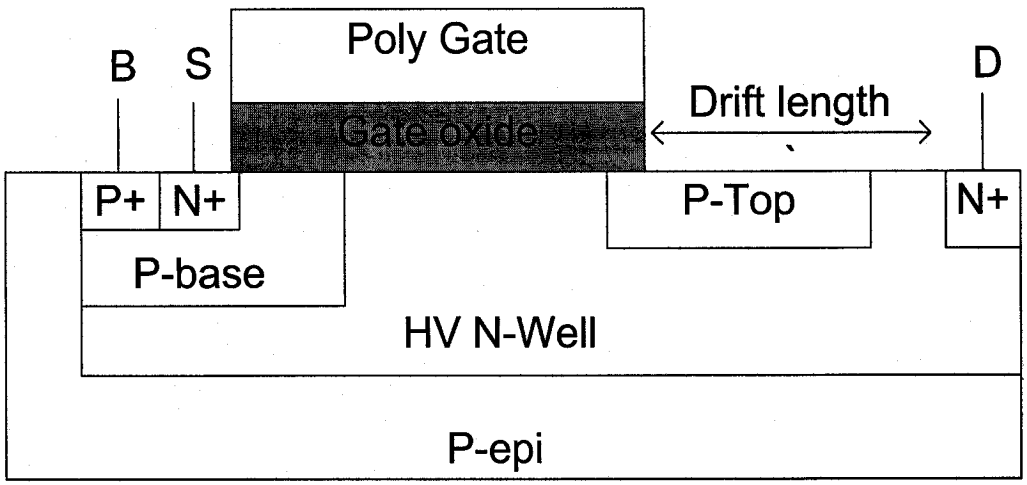

Figure 3.2: Lateral DMOS

3.2 DALSA SEMICONDUCTOR'S TECHNOLOGY LIMITATIONS

DALSA's high voltage components have certain specifications that have some bearing on the design choices. As for conventional CMOS transistors, the gate-to-source voltage V_{GS} has boundaries that affect the circuit topologies. For N-type transistors, the breakdown voltage is 15V (nominal is 5V) whereas for a p-type transistor, the V_{GS} must be larger than -16V (nominal -5V). Thus, assuming a p-type device attached to a 300V supply, its gate voltage will have to be between 295V and 300V. For example, the design of a simple inverter (Figure 3.3) becomes a complex task, as level-shifters are now required to satisfy the V_{GS} constraint [9]. In the case of a digital-to-analog converter, this constraint becomes an important design challenge, as conventional I-V conversion (using op-amps or resistors) is no longer a straightforward approach. This will be further discussed in the next chapter.

Other components, such as diodes and capacitors are not yet available for high-voltage applications. As a result, certain circuits, such as ESD protection circuitry, may not be employed. In addition, given the complexity of the high-voltage devices, the designer is given a set of high voltage transistors with predefined layouts to operate with. This limits the design's flexibility given that the designer must work around the specified

parameters and their limitations. Since transistors have fixed parameters, using different high-voltage components together also becomes a challenge.

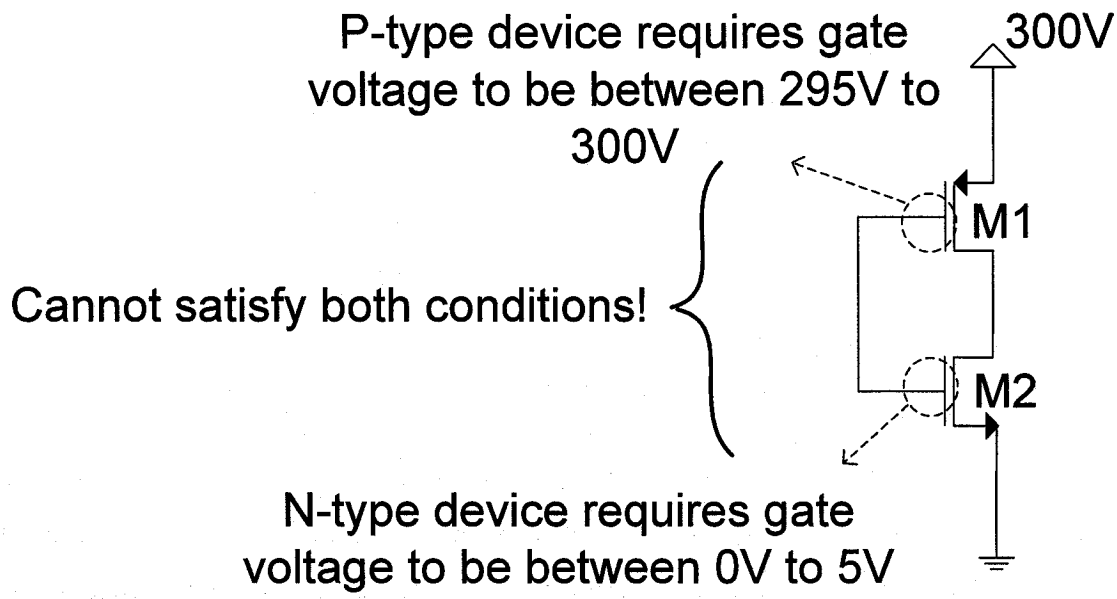

Figure 3.3: HV limitations on inverter

Another important consideration is that the N-type HV transistors cannot be used in series. Thus, cascode structures may not be utilized. Though some of DALSA's devices were initially floating-source devices (kits V2P0 & V2P1), DALSA has had trouble with these devices under conditions of high temperature (150C°) and high reverse bias (300V). This becomes a problem for designers of all sorts of analog devices. For example, current mirrors requiring a high-output impedance may not be achievable since cascode structures are not to be used. These shortcomings are currently being addressed by the foundry [10].

In the next chapter, two designs for current-to-HV conversion are presented – the first uses cascode transistors, as the N-type devices were initially supposed to be floating-source transistors (and therefore allow for a V_{BS} of 5V); the second avoids series transistors all-together.

Other issues relating to HV transistors lie in the verification process. Proper verification of the HV transistor via corner analysis is not yet available. In addition, extraction and LVS of HV transistors are not yet possible. This poses a problem in that a large circuit may not be appropriately verified. This will be further discussed in the layout challenges section of chapter four.

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CHAPTER 4 DESIGN, LAYOUT AND SIMULATION OF HVDAC

As discussed in Chapter 2, many architectures and topologies are available for digital-to-analog conversions. The characteristics targeted for a high-voltage DAC are summarized as follows:

1. the HVDAC array should be suitable for high-voltage operation,
2. the HVDAC array should be as fast as possible, and preferably achieve sub-μs settling speed in order to meet Agile-All Photonic Network's goal of having sub-μs switches,
3. the HVDAC array should be as compact as possible to reduce system cost,
4. the HVDAC array should be ready for flip-chipping to the optical device.

Process tolerances and area considerations along with the above-mentioned characteristics led to the current-steering architecture. In addition, to being well-suited to CMOS technology, they are faster and more linear than other topologies [1], [2].

4.1 CHIP ARCHITECTURE

Over the last several decades, optical-phased array designs were often based on a liquid crystal design and resulted in switching speeds on the order of milliseconds [3], [4], [5], [6] or had a small number of electrodes resulting in high optical losses[3], [7],[8]. Taking advantage of the electro-optic effect allows for high-speed operation, while exploiting a large number of electrodes in the ROPA design minimizes the optical losses. Optical simulations have shown that a 6-bit DAC provides a suitable voltage resolution for the desired optical performance of the EO switch. The overall chip architecture is shown in Figure 4.1. The ASIC consists of 64 HVDACs providing independent voltages

to the ROPA. In order to provide the 6-bit digital inputs to each DAC, 384 input pads would normally be required. This unrealistic port count is overcome by using a scan chain, shown in Figure 4.2, hence requiring only one input pad for the digital inputs. The scan_en strobe on the scan chain is asserted once all 384 inputs have been scanned in. To reduce the delay, the final design exploits four scan chains, each scanning in 96 digital inputs.

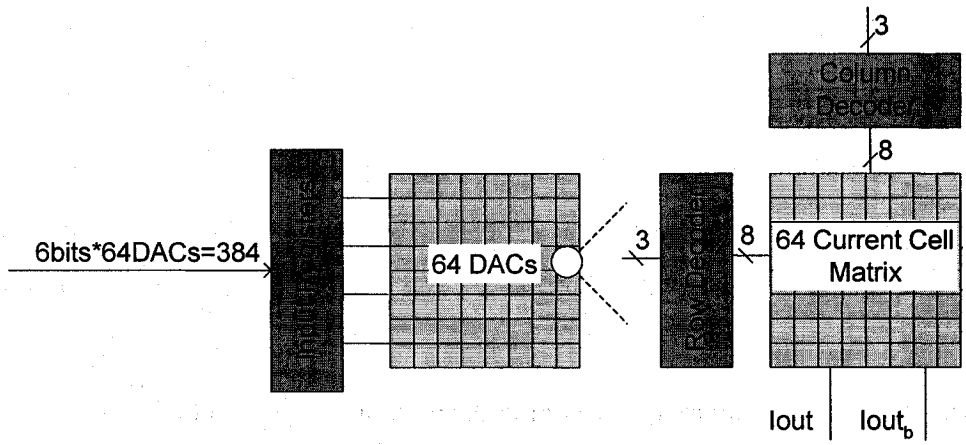

Figure 4.1: Chip architecture

Considering the voltage resolution, a thermometer coded, current-steering architecture was chosen. Thermometer coded architectures are typically used for low-bit accuracies, such as in this 6-bit case. Such an implementation requires 2^6 current sources, each connected to digital logic, forming the 8 by 8 current cell matrix. The digital signals come from a binary-to-thermometer encoder, depicted in Figure 4.1 as the row and column decoders. The three most significant bits drive the column decoder, while the three least significant bits drive the row decoder. After decoding, there are 8 row and 8 column bits which act as control signals for the current cell blocks. Table 4.1 depicts the logical operation of the decoders.

Table 4.1: 3-bit Thermometer code

A_2	A_1	A_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	0	0
1	1	0	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

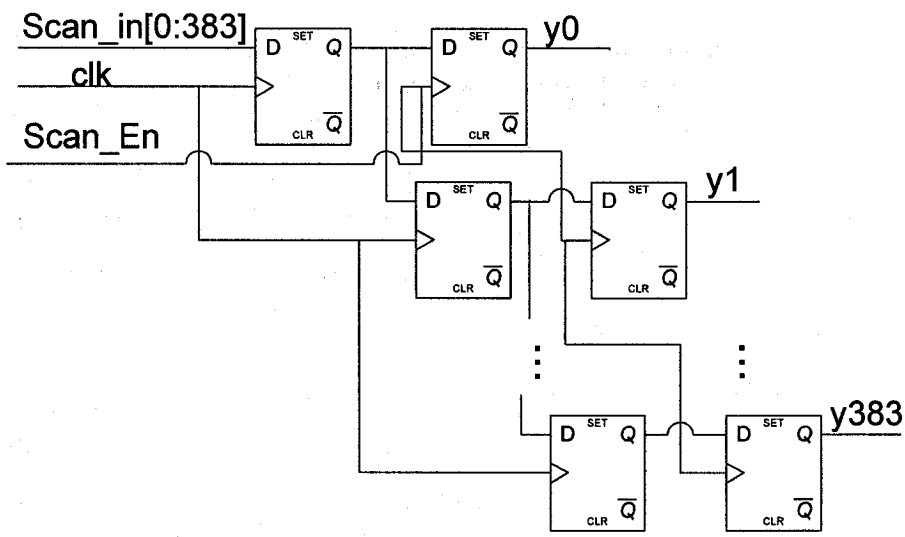

Figure 4.2: Scan-in chain

When the 6-bit input is increased by 1 least significant bit (LSB), an additional current source in the cell array matrix is turned on, thus ensuring monotonicity, low glitch energy and relaxed matching requirements on the current sources (compared to a binary

weighted DAC) [9], [10]. The number of current sources active at any given time is determined by the value of the 6-bit input: a 000000 will correspond to no current in the I_{out} branch and $63*I_{ref}$ in the I_{outb} branch while the opposite holds for the 111111 situation; varying the input code between the two extremities will result in output currents in between the two boundaries. The currents are then summed before undergoing current-to-voltage conversion. In contrast, in a binary weighted DAC, every switch connects an output current that is twice as large as the previous LSB. As explained in Chapter 2, this implementation may be simple, but a larger differential non-linearity (DNL) error ensues and the overall static and dynamic performances of the converter are compromised.

4.2 CURRENT CELL DESIGN

The circuitry of the individual current cells that compose the 8 by 8 array is shown in Figure 4.3. This cell contains some digital decoding that determines whether I_{out} or I_{outb} is active. The digital input to the current cell comes from the translated thermometer code. Since each of these current cells can either turn on the output current (switch current through I_{out}) or leave it in the off mode (switch current through I_{outb}), the goal of the decoding logic is thus reduced to determining which cells should be turned on such that it equals the thermometer code. In [11], a decoding logic that performs this task is presented. Figure 4.4 illustrates the decoder logic functionality for a given binary input. The six input bits are separated into the three MSBs and LSBs and passed to the thermometer-decoding row and column controller blocks. In this scenario, three types of rows exist: one in which all cells are turned on, one in which all cells are turned off and finally one in which some are on and some are off. In the current cell array, if the current row or column strobe is high and the previous row strobe is also high, then the current cell should be sourcing current [12], [13]. These row and column strobes are simply the thermometer input codes coming from the column and row decoders. The following equation describes the current cell decoding logic.

$$Y = Row_{n-1}\ AND\ (Row_n\ OR\ Col_n)$$

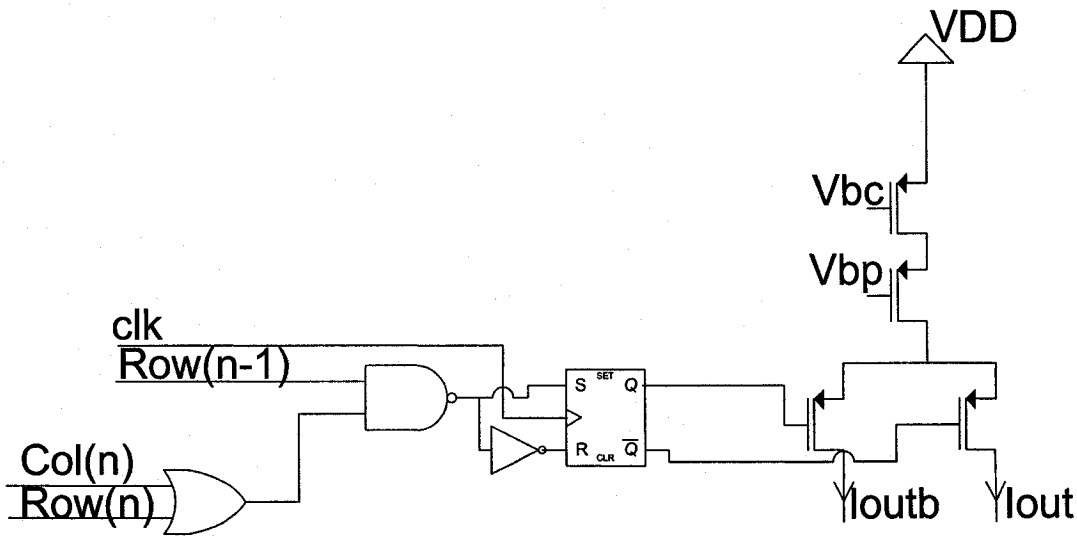

Figure 4.3: Current Cell

Following the decoding logic, the signal passes through a ratioed CMOS SR-latch [14]. By taking advantage of the intrinsic delay between the complementary output, the crossing point of the switch transistor's differential control signals is shifted, thus ensuring that these switch transistors are never simultaneously off [15] (Figure 4.5). This also guarantees that the cascode current source is never switched off. If the current source had been allowed to switch off, the potential at the output of the current source would shift towards the supply voltage (as it is being switched off). When switched on again, a large potential difference is created between the current source output and the DAC output, resulting in significant glitches during code transitions [1], [13], [15].

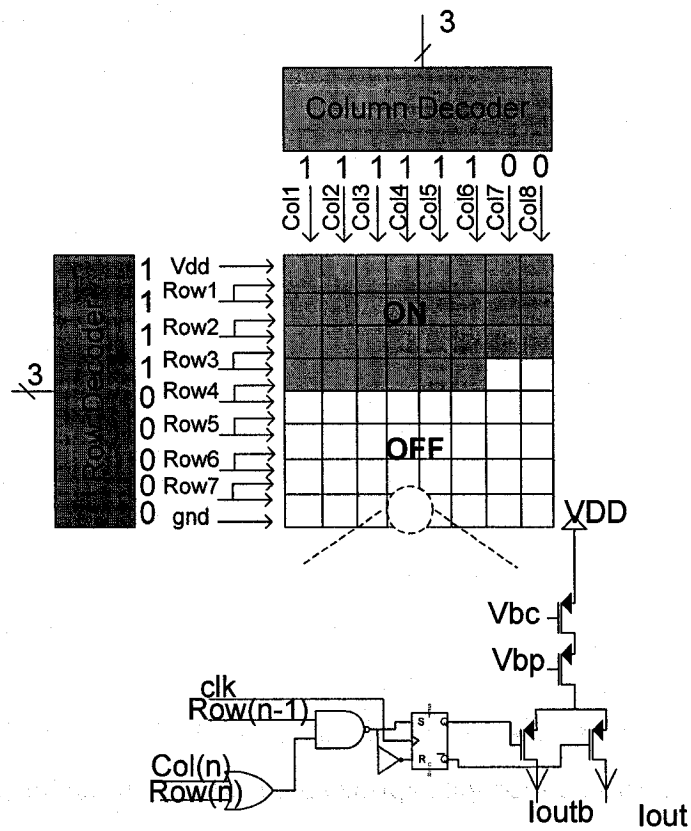

Figure 4.4: Decoder logic functionality

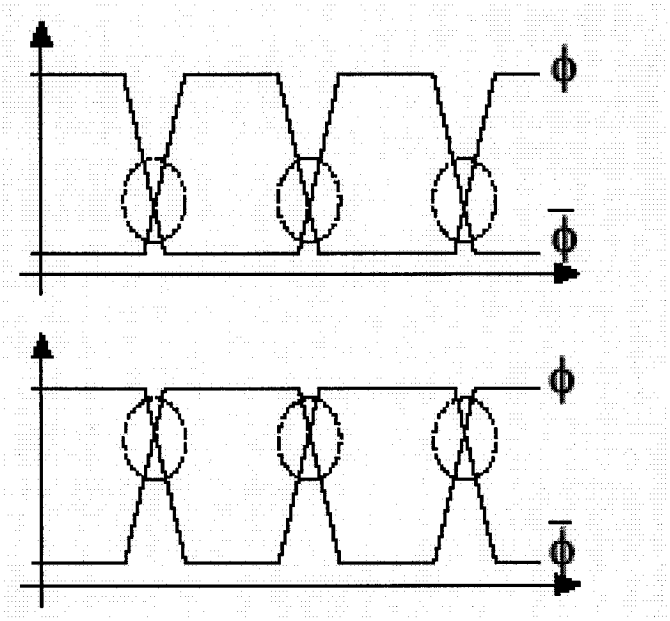

Figure 4.5: Wanted crossover point in a differential switch for a PMOS (top) and NMOS (bottom) implementation [1]

4.3 CURRENT-TO-VOLTAGE CONVERSION

Once the decoding logic has determined which current cells to turn on, the currents flowing from each cell are summed to generate the total DAC current. Due to the high-voltage requirements, standard current-steering DACs in which the I-V conversion is done using an output resistor or an op-amp (Figure 4.6(a) and Figure 4.6(b) respectively), may not be applied. Figure 4.7 illustrates in greater detail how the HV limitations affect the former method.

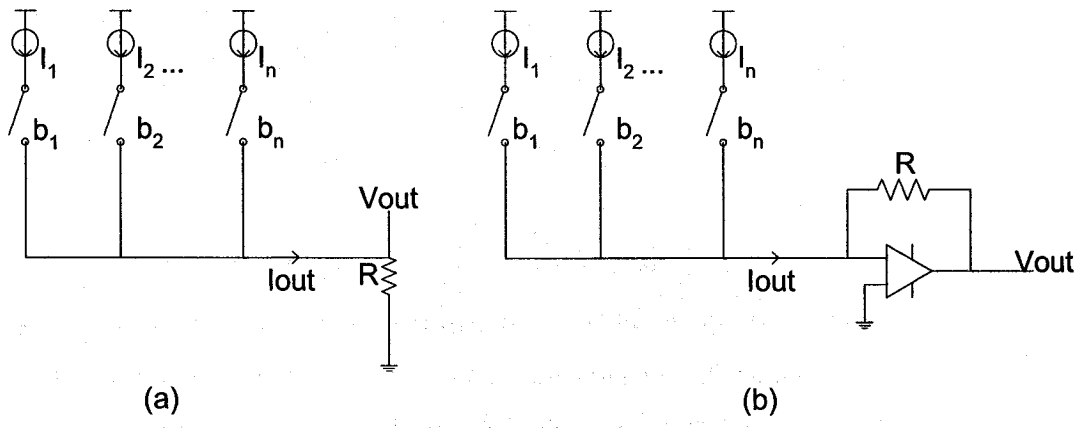

Figure 4.6:Current Steering DAC with (a) output resistor and (b) output buffer.

The design in Figure 4.7 is impractical because the current summation node would be a HV node, thus requiring all current switches in the current cells to be HV transistors. The HV transistors are larger than regular CMOS transistors, such that utilizing 128 of these (for all current switches in an N-type realization of the switch) would require a large die size. Figure 4.7 also shows the two alternative methods of implementing the current switches. In the N-type implementation, the main drawback is the elevated number of HV transistors, and therefore area, required. In addition to this problem, using the P-type alternative entails a method of providing the required gate voltages to these HV transistors, such as using level-shifters, and thus results in many more HV transistors. This is an important issue, as the overall chip will consist of 64 of these DACs. In addition, this can considerably slow down the settling speed of the converters. It is therefore crucial to circumvent this method of implementing the I-V conversion.

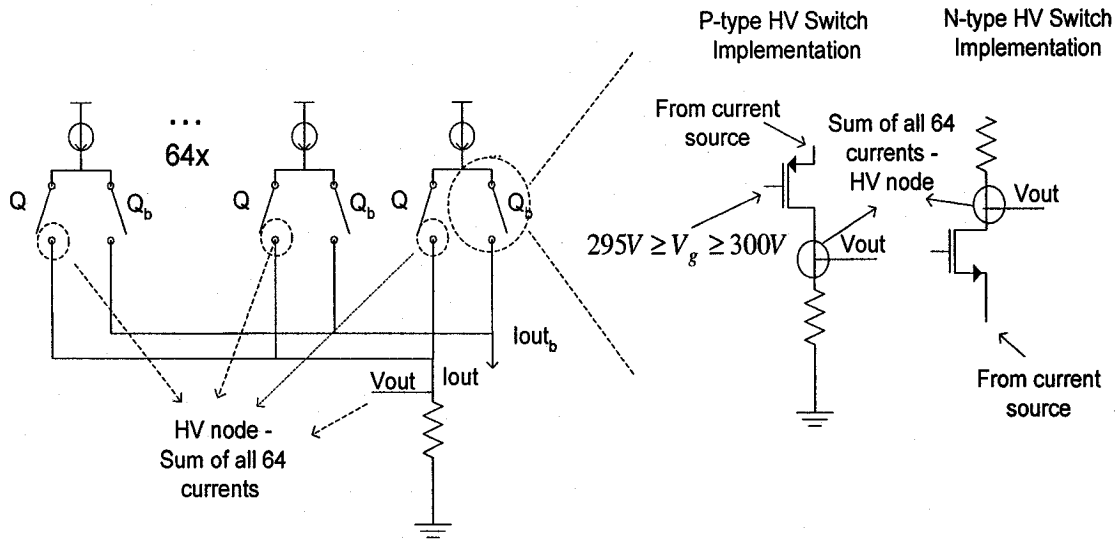

Figure 4.7: HV Limitations on current source array and transistor implementation for a single DAC unit.

The op-amp solution is also difficult to implement due to the V_{GS} constraint discussed in the previous section. Figure 4.8 depicts a simple two-stage op-amp configuration. Transistors M1 and M8 must be high-voltage transistors in order to produce the desired HV signal. However, P-type HV transistors require that their gate voltage be within 5V of the source voltage. This constraint triggers a domino effect, in the sense that transistors M2 and M3 must now be HV transistors since their gates are connected to that of M1. This implies that I_{ref}, if implemented on-chip, would also consist of HV circuitry. It is therefore evident from this simple implementation that the output stage of a typical op-amp is not the optimal solution to provide the I-V conversion, as the area quickly increases with the number of HV transistors.

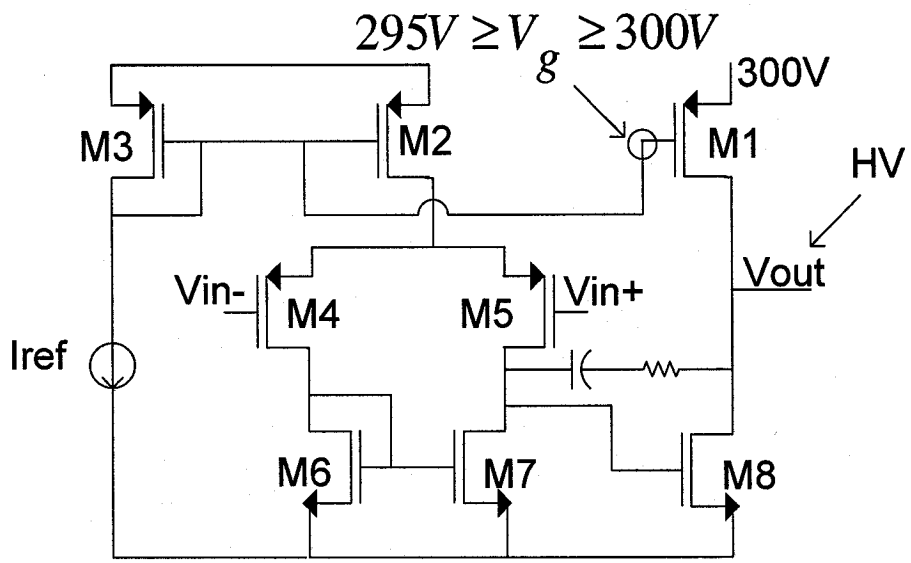

Figure 4.8: Two-stage CMOS op-amp implementation.

One effective alternative is to use a high-compliance current mirror [16] and to replace the output transistor by HV transistors. Simple current mirrors (Figure 4.9) exhibit low output impedance and the inherent V_{DS} mismatch results in large current copying errors. The currents are governed by the following equations:

$$I_{in} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}(V_{GS1} - V_{th})^2(1+\lambda V_{DS1})$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(V_{GS2} - V_{th})^2(1+\lambda V_{DS2})$$

While $V_{DS1}=V_{GS1}=V_{GS2}$, V_{DS2} may vary due to the finite output impedance. As a result, the input and output current will not be the same. Therefore, the current mismatches in a simple current mirror occur due to differences in λ and V_{DS}.

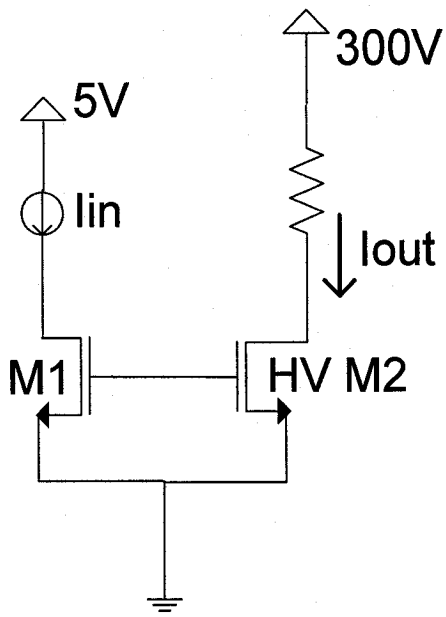

Figure 4.9: Simple current mirror.

Cascode current mirrors or many of the high-output impedance current mirrors often used are well matched for a certain input current, but once that input is changed, the error ensued in the mirroring process increases [16], [17]. For example, in the classical cascode current mirror of Figure 4.10(a) or the wide-swing cascode current mirror of Figure 4.10(b), transistors M3 buffer the drains of M2 from variations in V_{OUT}, resulting in very closely matched drain-source voltages for transistors M1 and M2. This is understood by observing the effect of cascoding on the output impedance:

$$r_{out} = r_{ds2}$$

for the simple current mirror. In the cascode case, the output resistance is:

$$r_{out} = g_{m3} r_{ds2} r_{ds3}$$

effectively increasing by the $g_{m3} r_{ds3}$ of M3, making it look like an impedance amplifier.

Additionally, in the wide-swing cascode current mirror, transistor M4 ensures that M1's drain-source voltage is matched to that of M2 [17]. However, when performing the

design for these structures, a specific current is assumed in order to deduce the desired parameters such as the W/L ratio. Varying this current while keeping the W/L ratios the same will result in variations in voltages, thus resulting in mismatches between the reference current and the output current.

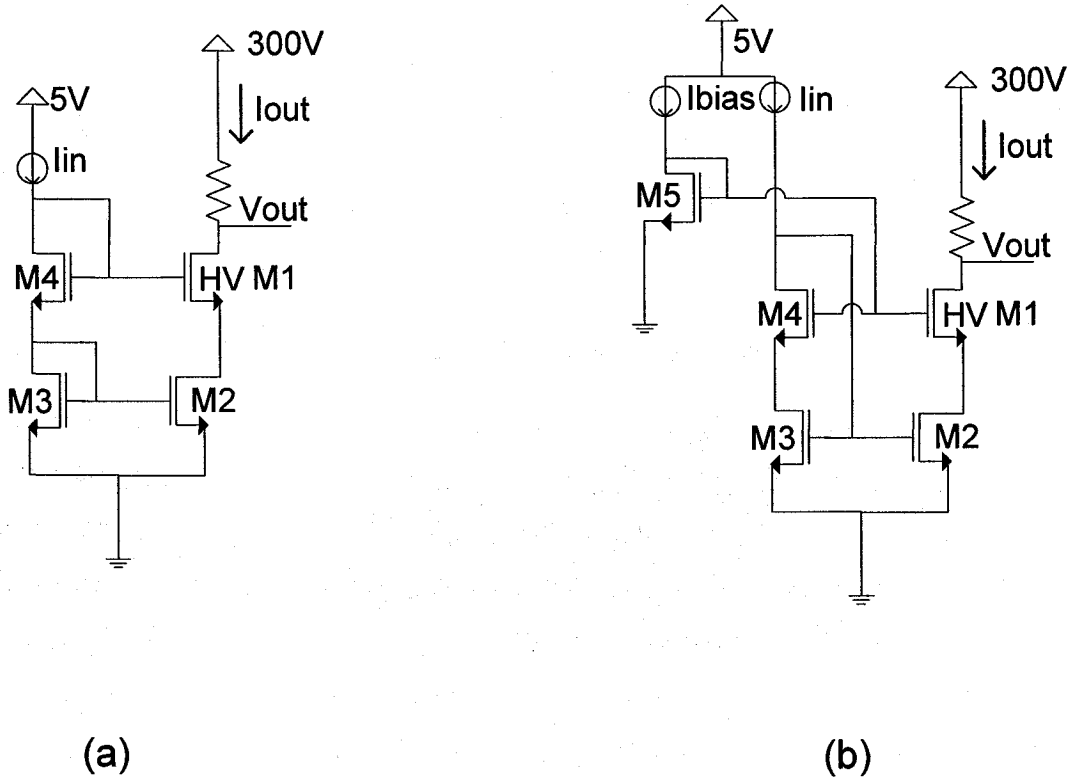

Figure 4.10: (a)Cascode current mirror and (b) Wide-swing current mirror.

For an application like that of a digital-to-analog converter, an accurate current mirror is required for a large input swing ; in this case for 0 to 2mA. The design illustrated in Figure 4.11 realizes current matching for a large swing of currents. The main condition for current matching discussed thus far has been the drain-source voltages. Therefore, the V_{DS} of transistors M1, M4, M2 and M7 must be equal or as close as possible to each other for proper operation. This is ensured by transistors M5 and M6 which provide voltage drops from the gate of M3 to the drains of M4 and M7, equal to V_{gs3}. The high-output impedance is provided by the negative active-feedback loop created by transistors M2-

M3-M7. The output impedance for a cascode transistor (without the feedback loop) is repeated here for convenience:

$$r_{out} = g_{m3} r_{ds2} r_{ds3}$$

The loop gain of M2-M3-M7 is approximately:

$$K_{loop} \approx -g_{m7} r_{ds7} // r_{ds8}$$

and the overall output impedance with the feedback loop is given by:

$$r_{out} = g_{m3} g_{m7} r_{ds2} r_{ds3} (r_{ds7} // r_{ds8})$$

thus increasing by a factor equal to the magnitude of the loop gain [16].

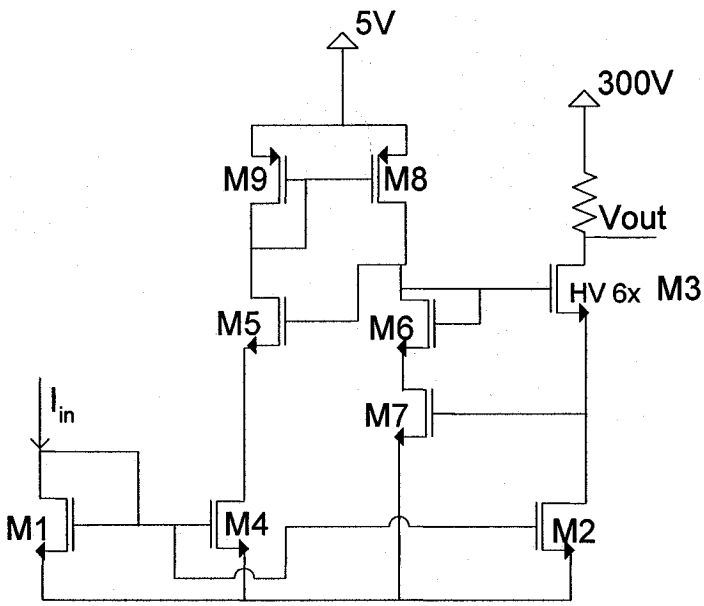

Figure 4.11: High-compliance current mirror

In this approach, the current is copied to the output node with a worst case error of 0.53 %, consequently decoupling the current switches from the HV node. This particular implementation sources up to 2mA to a capacitive load. This technique considerably reduces the number of HV transistors in each DAC unit (from 128 to 6; 6 to achieve the

desired W/L ratio since HV transistors have predefined layouts), and therefore results in a great savings in die area.

Prior to submitting the design for fabrication, DALSA Semiconductors had revised the high-voltage transistors' specifications and determined that floating source transistors were not reliable under high temperature and high voltage conditions, though they are working on making such technology possible for future works. This constraint forced a change on the current-to-high-voltage converter; cascode structures could no longer be used. A simple current mirror was designed; needless to say, the linearity errors at the two extremities of the current range were relatively high. However, after running optical simulations with the HVDAC's simulated results, it was found that for the application at hand, these outputs would provide enough distinct voltages to operate the ROPA adequately.

4.4 LAYOUT CHALLENGES

The layout of the HVDAC was done manually for all digital and analog cells. In laying out the digital and analog cells that compose the HVDAC, several important aspects of the application needed to be considered. First of all, the die is comprised of 64 HVDACs, in addition to any test circuitry that would be added. Evidently, each of these DAC units must be kept to a minimal size to reduce the cost of manufacturing. However, flip-chipping requires a large die size (7mm x 7mm) to increase maneuverability, thus setting the lower bound [18]. In order to incorporate as many test structures as possible within this minimal die size, the DAC layouts needed to be optimized to achieve the smallest dimensions. All the digital blocks were laid out in such a way that once connected together to form the current cell, a square or rectangular shaped unit would be formed. This is to ensure that the current cells could be easily tiled and connected together while forming a rectangular shaped DAC. Figure 4.12 illustrates how tiling these units results in a rectangular shaped HVDAC layout. An initial pass of the HVDAC

layout yielded a design of close to 750μm x 700μm. Several revisions of the current cell and changes in the manual placement and routing techniques yielded an HVDAC measuring of 900μm x 400μm – a 31 % savings in area for a cell to be repeated 64 times.

Integration of electronics with optics opens the door to many applications. However, special attention must be placed on the layout of the electronics to ensure proper optical performance. For instance, optical devices require an unhindered optical path free of any physical interference. This results in a requirement for careful placement of the bond pads in order to provide a clear path for the optical signal. This is depicted in Figure 4.13 and can also seen in the layout shown in Figure 4.14.

In addition, according to [19], high-voltage (300 V) electrodes in air should be placed 3um away from each other to avoid arcing. The fact that electrodes in air must be placed 3um apart also had an impact on the layout. Flip-chip pads were spaced at least 5um apart to avoid any arcing. Ground flip-chip pads were also strategically placed to ensure mechanical stability.

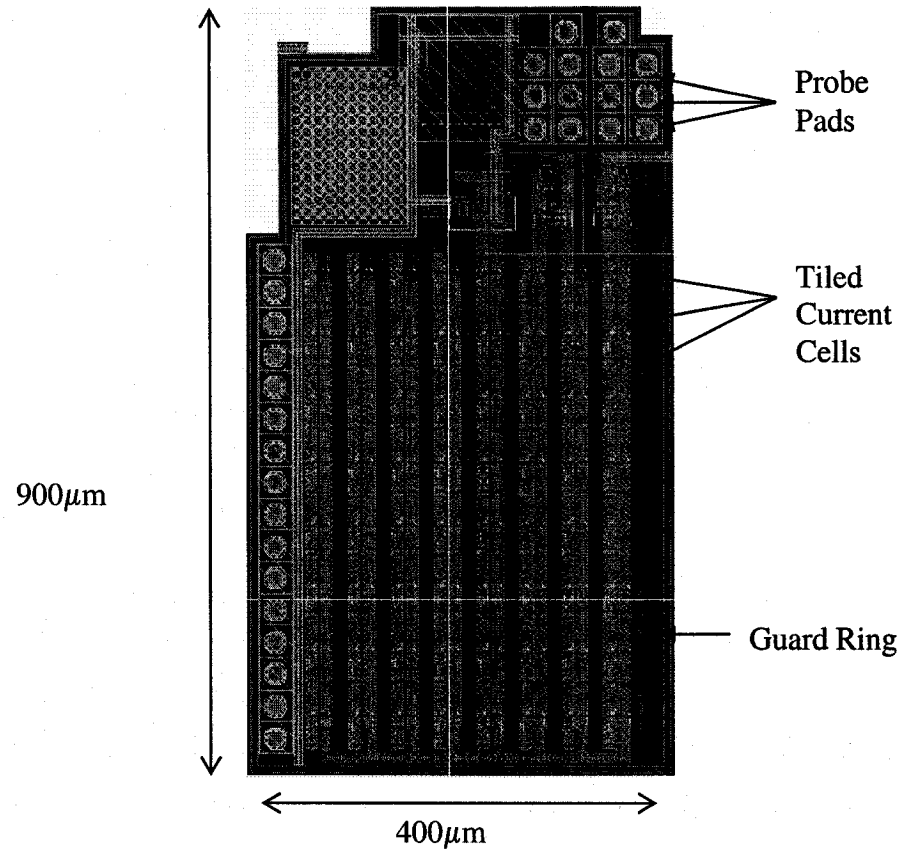

Figure 4.12: HVDAC Layout

Moreover, DALSA suggests that all high-voltage tracks be routed in either Metal 2 or Metal 3. Analog layout techniques were used with these HV signals – using minimum design rules were avoided. Though the design rules ensure that arcing would not occur, most track widths and spacings were doubled beyond the minimum requirements. Additionally, crosstalk and interference between high-voltage tracks of the same layer or even metals of different layers may possibly affect the circuit's performance. This will be studied experimentally.

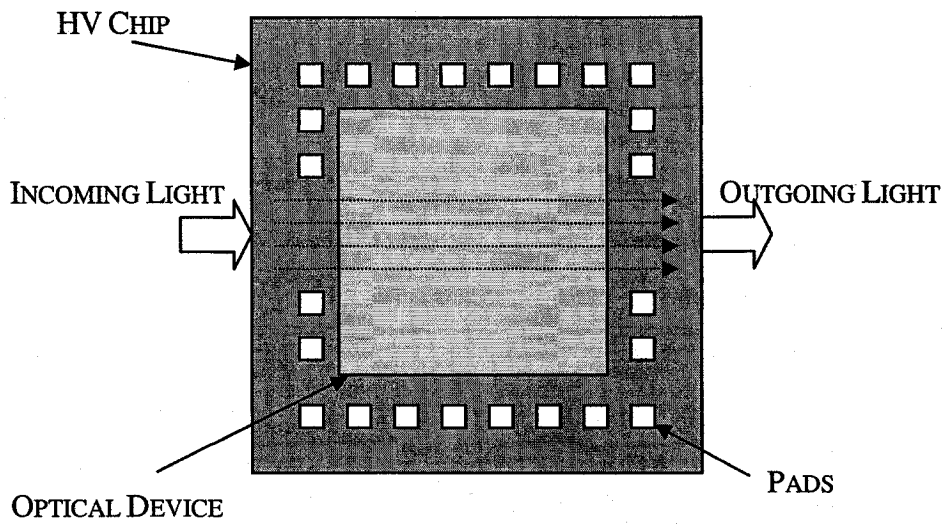

Figure 4.13: Bond Pad Placement

In addition, it is difficult to simulate a design of this size, though it is important to ensure that the design would operate as expected. One critical signal that needed to be taken into consideration was the clock. The clock input propagates through the four scan-in chains and the 64 DACs. Evidently, a clock buffer was required. To ensure proper sizing and operation, the input capacitance of each DAC and each scan- in register was calculated using the following equation:

$$C = C_{ox} W L$$

This resulted in gate capacitance of approximately 5pF for each DAC and a gate capacitance of around 6pF for each input register. Simulations were done using these values to determine how clock buffers would be required. One clock buffer was placed for every input register while a clock buffer was required for every four DAC units, ensuring that the clock signal was adequate for the operation of the system.

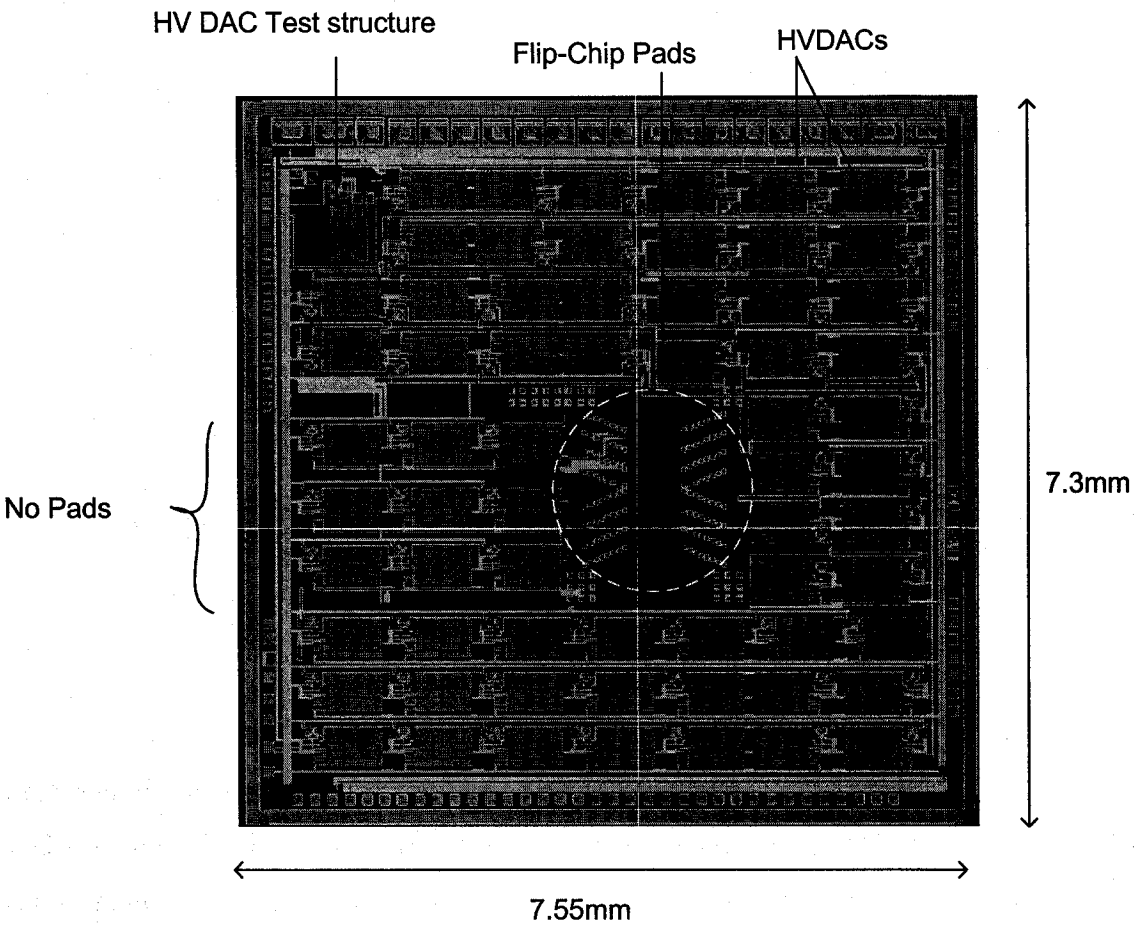

Figure 4.14: Layout of complete DAC array.

4.5 SIMULATION RESULTS

The proposed HVDAC was designed in DALSA Semiconductor's 0.8um 5V/300V, quadruple well, three metal layer, epitaxial silicon process. The DAC was simulated using Spectres. As previously mentioned, two HVDAC designs were simulated: these include the high-compliance current mirror design and the simple current mirror. Figures 4.15 and 4.16 show the DACs actual transfer curves along with the reference curve for the high compliance and simple current mirror designs respectively. From Figure 4.15, it is evident that the first design copied the current accurately and therefore produced an output that closely matched the ideal DAC's performance. This DAC's output is linear.

On the other hand, Figure 4.16 shows how the deficiencies in current copying of a simple current mirror induce errors on the actual DAC output. The output is highly non-linear at the two input code extremities and somewhat linear in the middle while deviating in value from the ideal outcome. It is clear from this figure that many output levels are almost identical. For instance, for the first ten input codes, the voltages are in the 5V to 7V range, reducing the useful output levels to be used by the optical-phased array. Simulations have shown that the number of useable levels by the ROPA is 51 for the simple current mirror. In contrast, all 64 input codes produce distinguishable voltage levels for the high compliance mirror design.

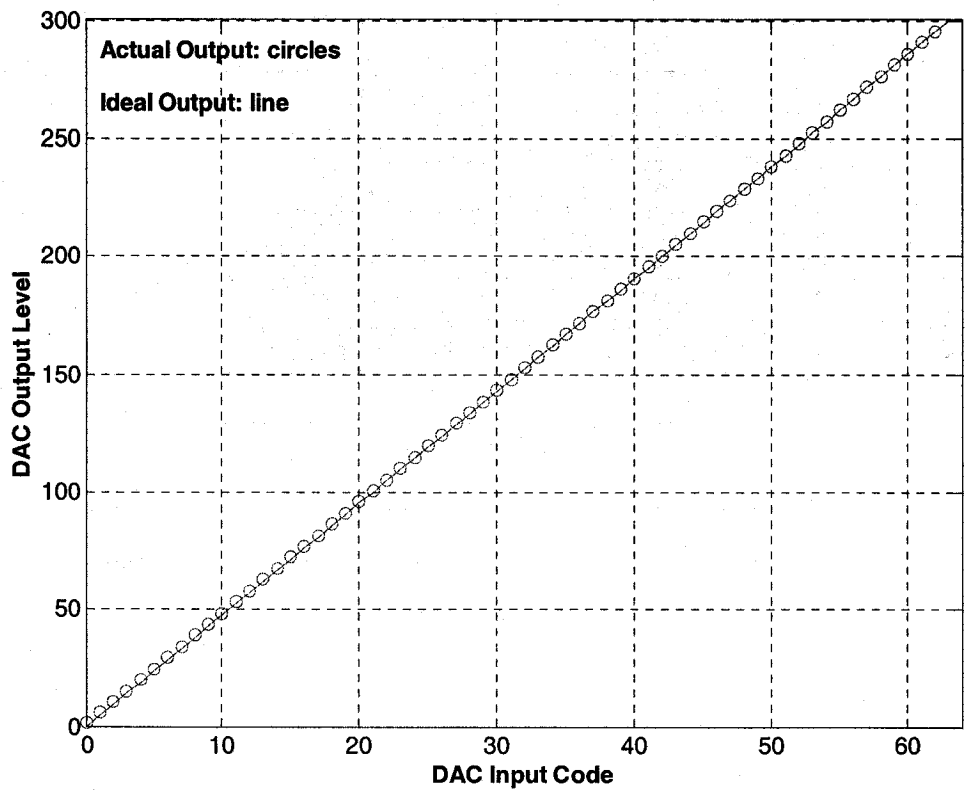

Figure 4.15: HVDAC actual output vs. the ideal output for the high-compliance mirror design.

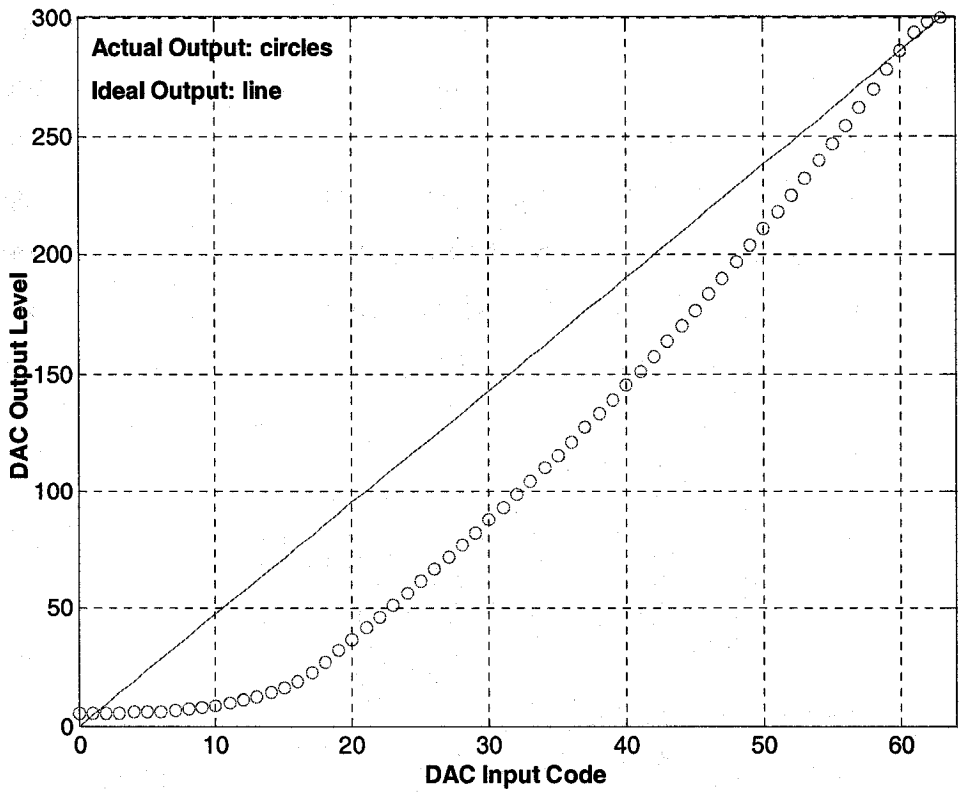

Figure 4.16: HVDAC actual output vs. the ideal output for the simple current mirror design.

Figures 4.17 and 4.18 show the differential nonlinearity error for both designs. In Chapter 2, the DNL was defined as a figure measuring the error between two successive step sizes from the ideal 1 LSB. It is therefore a measure of the DAC's linearity. From Figures 4.15 and 4.16, we could predict that the high-compliance current mirror would have a better DNL performance than the simple current mirror design. This is confirmed in Figures 4.17 and 4.18. The former figure shows a DNL specification that is within ±0.02LSBs for all code transitions, except for the first transition which has a DNL of -0.16LSBs. This is explained as follows. The first code transition, which ideally would correspond to a transition from 0V to 4.7V (4.7V transition) is actually going from 1.8V to 5V (a 3.2V transition), whereas all other transitions are approximately equal to 4.7V. The DAC only reaches 1.8V instead of 0V because of the 2 V_{DS} drops required in a cascode structure (the 2 NMOS in series of Figure 4.11 each have a turn on voltage). This difference in step sizes causes the first transitions DNL to be larger than all the others.

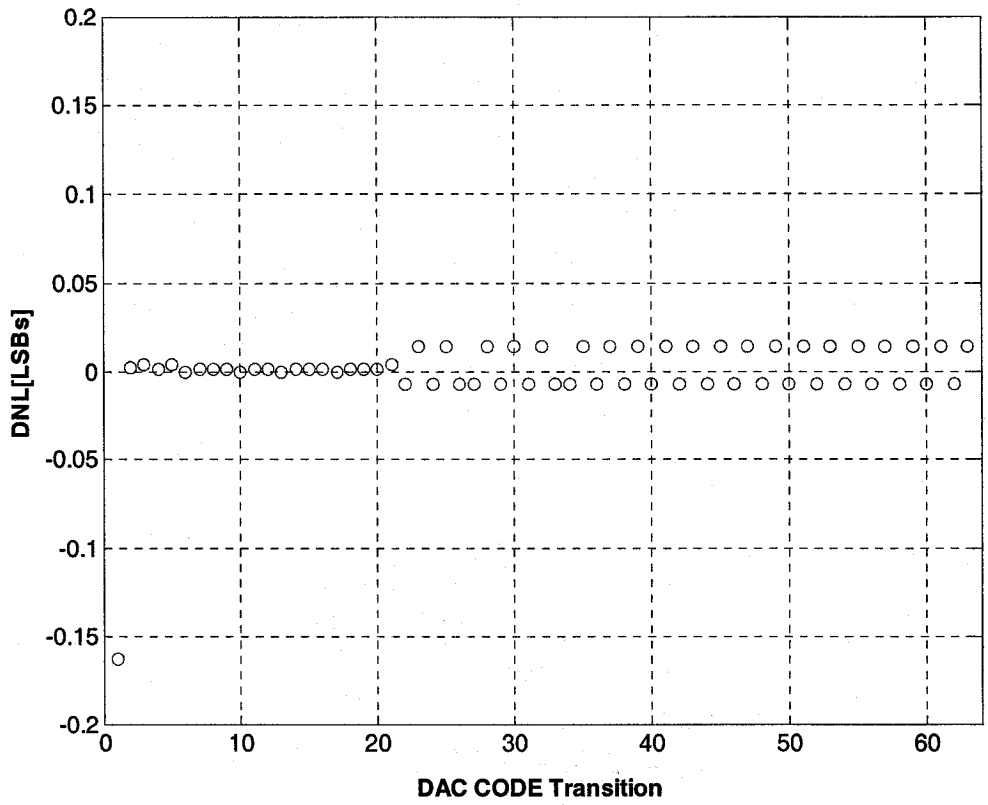

Figure 4.17: DNL profile for HVDAC using the high-compliance current mirror design.

The DNL profile of Figure 4.18 can also be predicted by observing Figure 4.16. For the first 10 or so input codes, the DNL is relatively high, approaching -1 LSB. This is understood by the fact that the difference in step sizes between these code transitions varies from 0.1V for the first few transitions to 0.6V for the tenth transition. These small step sizes obviously differ form the ideal 1 LSB step size (4.7V), thus creating such a large DNL error. As the errors in current copying induced by the simple current mirror are reduced with increasing input code, the DNL profile also improves. For example, the profile from code 15 to 30 shows that the DAC is close to linear in this region. This is verified in Figure 4.16 where the slopes of the actual curve and the ideal curve are closely matched for these inputs. Finally, as the code keeps increasing, the DAC becomes more and more nonlinear again, since the current copying errors once again increase.

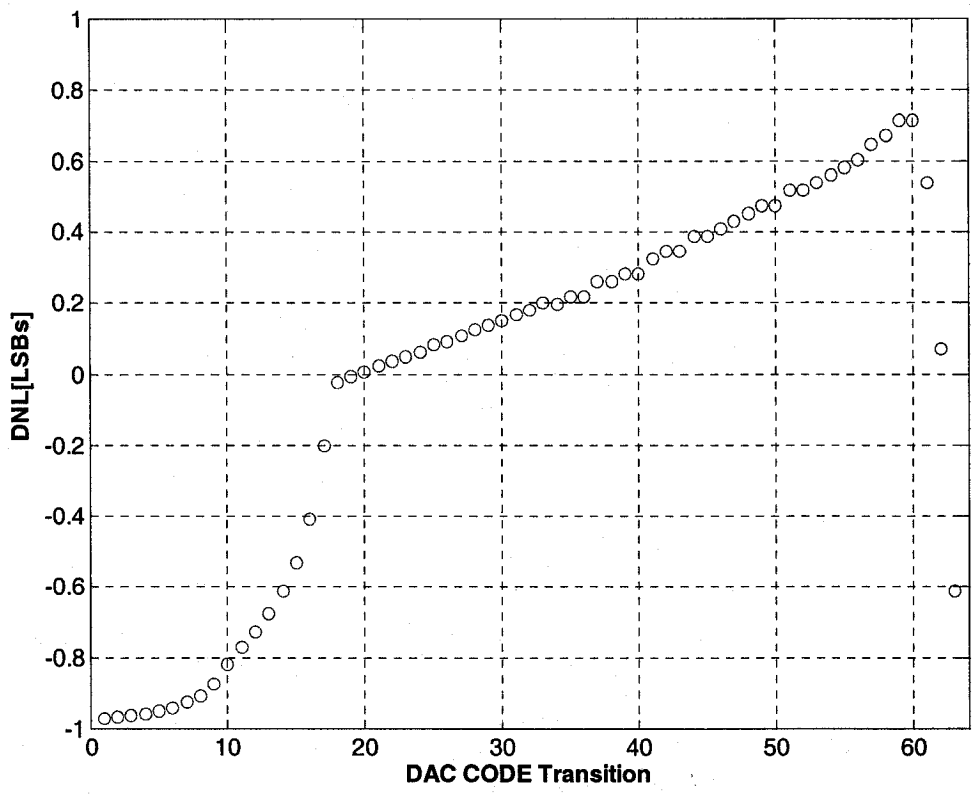

Figure 4.18: DNL profile for HVDAC using simple current mirror design.

As was the case for the DNL error, the integral nonlinearity behavior of both HVDAC designs may also be predicted from Figures 4.15 and 4.16. In Chapter 2, INL error was defined as the deviation of the actual DAC output from a reference line. A commonly used line is the endpoint line, in which a straight line is used to connect the endpoints of the transfer curve. This straight line is defined by the zero and full-scale range of the converter, thereby creating a DNL error of 0 for these two extremities. Figure 4.15, shows that the actual DAC output is closely matched to that of the used reference line. For the early code transitions, the actual output and ideal output differ slightly (in Figure 4.15, the line is not centered in the circles for these early codes) due to the above mentioned reasons. As the current mirror begins to accurately copy the current, the ideal and actual outputs are closely matched. This is easily observed in the INL

profile of Figure 4.19. For the early codes, the INL starts at -0.16LSBs and slowly rises closer to zero with increasing input code.

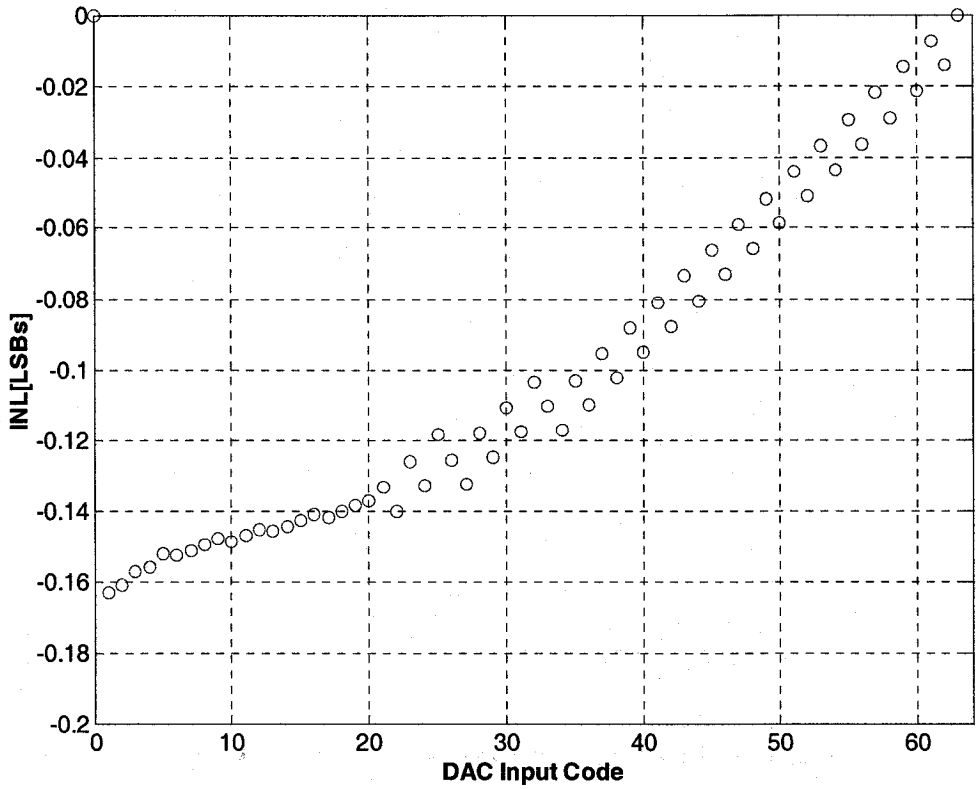

Figure 4.19: INL profile of HVDAC using high-compliance current mirror design.

Similarly, the INL profile of Figure 4.20 may be understood by analyzing Figure 4.16. The latter figure shows that the first few codes and the last few codes are close to the reference curve. This is translated in an INL error closer to 0 for these inputs. As the DAC output further deviates from the ideal output, the INL error increases to a peak of -13 LSBs at input code 20. This gap may be observed in Figure 4.16. At this point, the reference curve deviates from the ideal curve by approximately 60V. However, at this point the DAC begins to ramp up evenly enough, as observed from the DNL profile, and is therefore providing enough discrete voltages for the optical application.

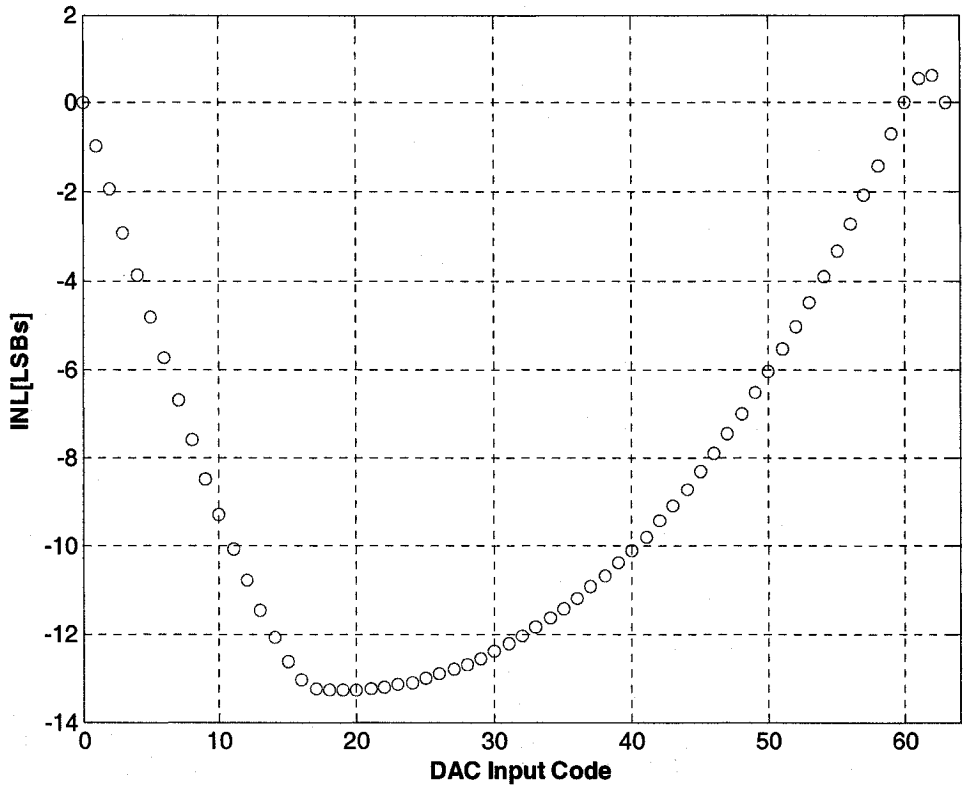

Figure 4.20: INL profile of HVDAC using simple current mirror design.

Finally, the DACs settling speeds are shown in Figures 4.21 and 4.22. The settling time of a converter was defined in Chapter 2 as the time required to reach the desired output within an acceptable error band. For the purpose of the simulations, this error band was chosen to be the time required to reach 1% of the final value. For the high-compliance current mirror design, the worst case conversion time was measured to be 2.2μs, time required to switch from 0V to 300V. In contrast, the settling speed of the simple current mirror design is greatly reduced as observed in Figure 4.22. The worst case conversion time for this circuit is 1.3μs, time required to switch from 0V to 300V (while the time required to switch from 300V to 0V is 576ns). Though this speed may be increased to be below the 1μs AAPN target, the accuracy and number of distinguishable/useable voltages of the converter would quickly decrease.

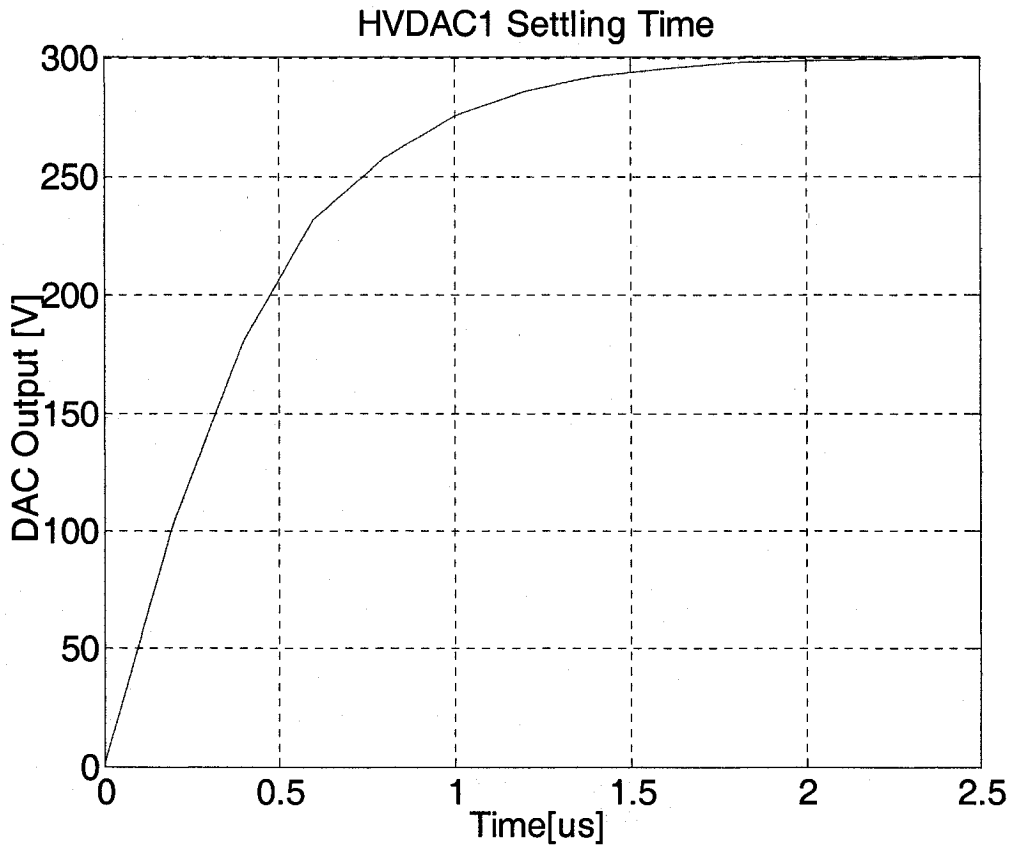

Figure 4.21: Settling speed of HVDAC using high-compliance current mirror design.

The difference in settling speeds between the two designs is mainly due to the fact that in the high-compliance current mirror, six high-voltage devices are used at the output to produce the desired W/L ratio. In contrast, the simple current mirror only uses one high-voltage transistor. This results in a higher capacitance at the output of the first design, slowing down the converter's settling speed.

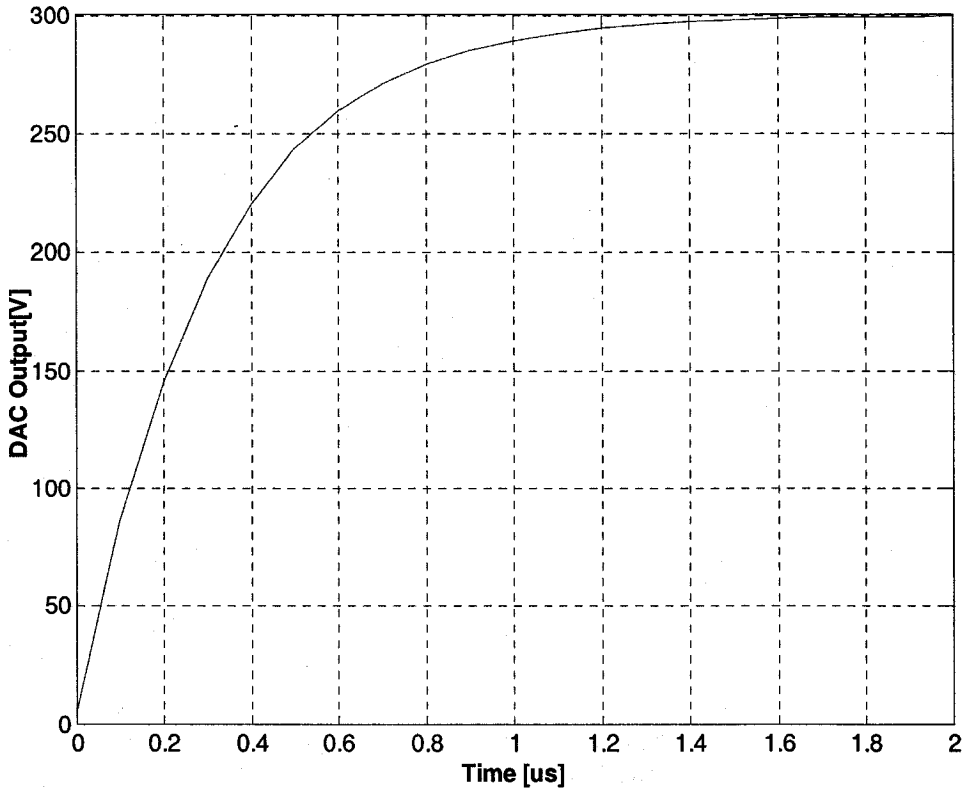

Figure 4.22: Settling speed of HVDAC using simple current mirror design.

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CHAPTER 5 TEST PLAN, PACKAGING AND EXPERIMENTAL RESULTS

Part of the work involved in designing large integrated circuits revolves around planning ahead. A good test plan should enable the designer to have an idea of what is required on-chip and off-chip for test purposes. Section 5.1 will summarize the test plan used in the design and preparation for testing. Section 5.2 will discuss some of the packaging requirements necessary to ensure proper system operation. Section 5.3 will briefly cover the heterogeneous integration. Finally, section 5.4 will cover the experimental testing.

5.1 TEST PLAN

The design of a large circuit requires proper planning in order to ensure that functional verification will be possible. To do this, certain key voltages/currents on the chip should be accessible to give an indication of where, if at all failure occur. The test points include:

- Single HV transistor
- 3-to-8 column and row encoders
- Output of SR latch in current cell
- HV Output before flip-chip
- Flip-chip connectivity

5.1.1 SINGLE HV TRANSISTOR

The novelty of the DAC array is its high-voltage aspect. To ensure that the HVDACs will indeed be able to have the required swing of 0V to 300V, we must first test the N-type DMOS transistor. To do so, separate HV test transistors have been placed on-chip; their source and bulk will be tied to VSS, while the drain and gate voltages will be varied; the current I_d will be measured. The gate voltage is restricted to 0-5V while the drain may range from 0-300V.

This procedure should allow us to reproduce DALSA's I-V curves included in [1]. Ideally, many HV transistors would have been placed to account for low yield or any other unforeseeable problems; area restrictions however limited us to only two HV test transistors.

5.1.2 3-TO-8 COLUMN AND ROW ENCODERS

As explained in Chapter 4, the digital inputs arrive from a computer and are scanned in through a series of flip-flops.

The outputs of the encoders should be measured to ensure that the proper logic propagates to the current cell. Two possible measurement solutions could have been employed: either use probe pads or use regular wire bond output pads. Since there are 64 DACs (and therefore 64 column and row encoders), the former solution was selected to minimize area consumption as wire bond pads are much larger than probing pads. This solution allows the testing of every encoder as probe pads were incorporated into each HVDAC design. If the other alternative had been used, then placing 7 wire-bond pads for test purposes would render this approach costly in terms of space while only allowing us to test one set of row and columns encoders (7 wire bond pads required per HVDAC). This test structure would also require a multiplexer to allow the signal to either flow through during normal operation or be measured off-chip in test mode (increasing area consumption). From a BIST/DFT point of view, the ideal scenario would have been to

scan out the outputs of the encoders at the great expense of die size. However, as mentioned before, the only viable solution to minimize cost is the use of probe pads.

5.1.3 OUTPUT OF SR LATCH

As was also covered in Chapter 4, the outputs of the column/row encoders flow through a NOR/NAND/SR-latch before switching the current sources on/off (Figure 5.1). Probe pads were placed at the output of the SR Latch, as depicted below for convenience, providing the necessary tools for measuring the voltage at that stage.

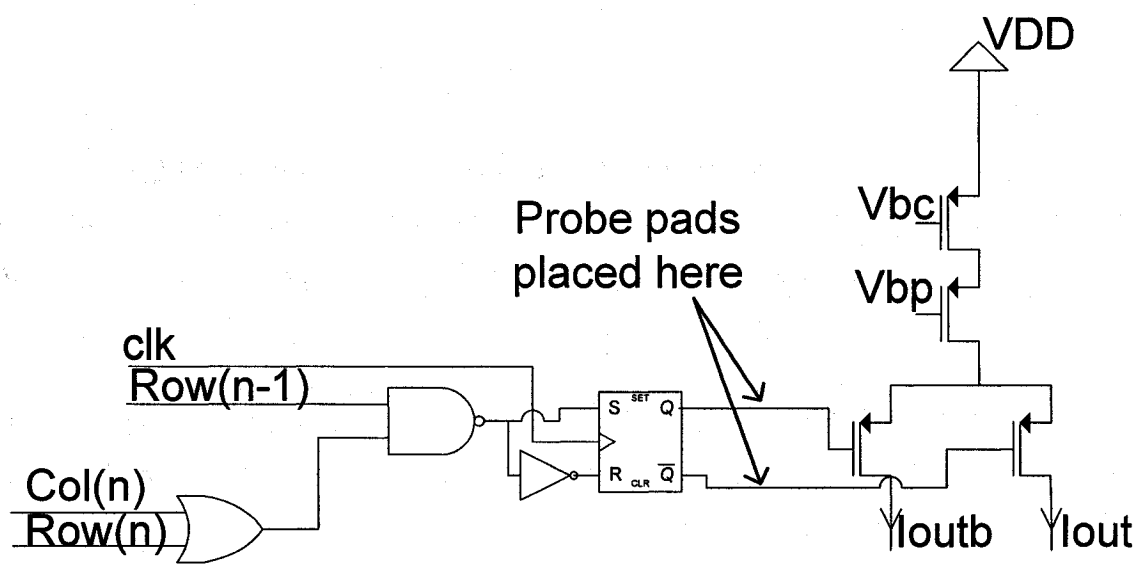

Figure 5.1:Current Cell

As was the case for the encoders, using probe pads eliminates the need for multiplexers and maximizes the number of measurable SR Latch outputs within each HVDAC. Again, in terms of BIST approaches, the ideal scenario would have been to scan-out the outputs using a chain of flip-flops at the expense of area usage.

5.1.4 HV OUTPUT BEFORE HETEROGENEOUS INTEGRATION

Once all the digital blocks have been verified to work correctly, the final stage consists of current flowing from the output of the current cell through a simple current mirror providing the current-to-voltage conversion.

At this point, probing at flip-chip pad locations will ensure proper device functionality. Measuring the worst case rise and fall times (0 →300V and 300→0V) using a high-speed probe will also determine the OPAs maximum speed performance.

5.1.5 FLIP-CHIP CONNECTIVITY

Once the CMOS/DMOS chip has been heterogeneously integrated with the EO device through flip-chip bonding, a method of ensuring connectivity between the optical and electrical devices is required. The chip requires a minimum of two flip-chip pads per electrode: one to provide the HV signal to the electro-optic device from the HVDAC and the other to test connectivity. Since probing is no longer an option after flip-chipping, the second flip-chip pad can be connected to a wire-bond pad, thus allowing measurement of the voltage at all times. This requires 64 wire-bond pads. Before settling on this solution, other alternatives were considered. One approach is to down convert the HV signal to a LV signal. This may be done through some form of voltage division (figure 5.2) followed by a scan-out chain, or through a level-shifter. However, these approaches would require too many large resistors or HV transistors rendering them impractical.

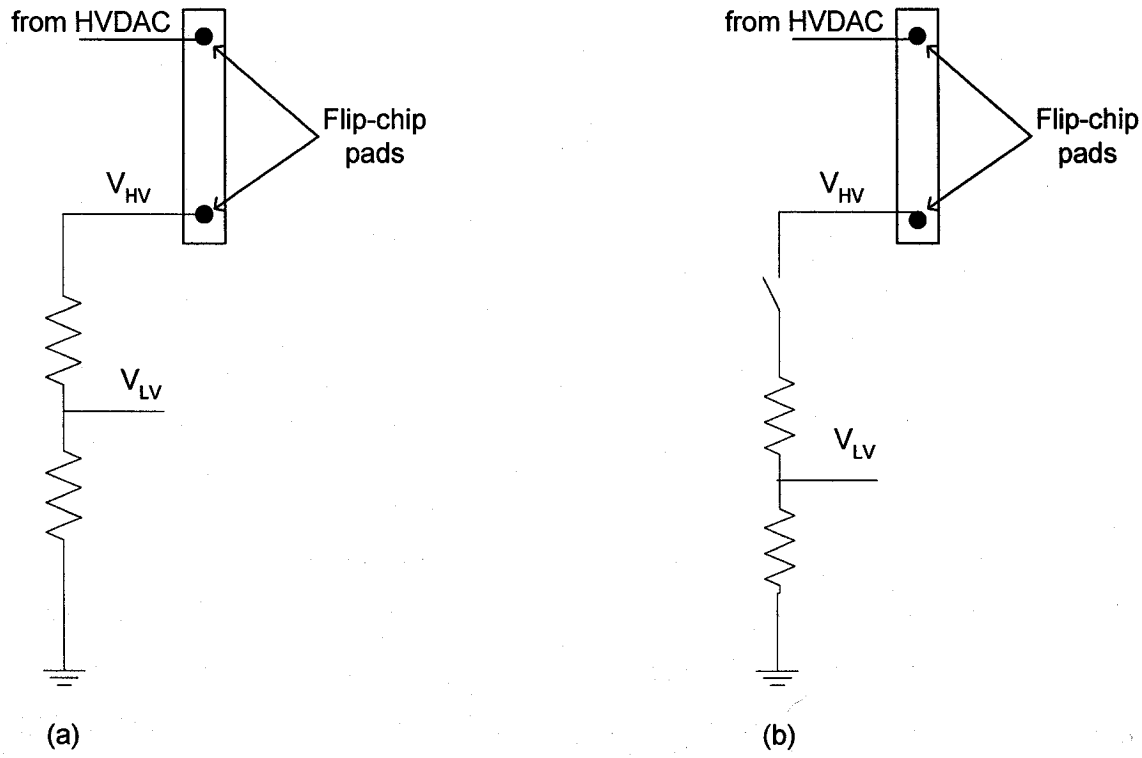

Figure 5.2: Voltage division approach to down-conversion (a) without switch (b) with switch

As an example, the large resistors required in figure 5.2 may be replaced by active load devices. However, in contrast to regular CMOS processes where this approach would optimize area consumption, HV transistors occupy much greater area then these large resistors. Moreover, the voltage division approach will also draw a large amount of current, and therefore power. In order to decrease power dissipation, a switch may be added to turn this section of the circuitry on during test mode as in figure 5.2b. Again, these switches would be HV transistors and thus the approach is too difficult to implement due to area limitations. Thus, the straight forward approach of utilizing wire bond pads is used.

5.1.6 NOTES ON TESTING THE HVCHIP

As mentioned earlier, the first step in verifying that the HV chip works is to power up an HV transistor. To test HV transistor #1, located at the bottom left of the chip

carrier on the PCB, the gate and drain of the transistor are varied while the source is tied to ground. The drain and gate voltage are varied using a high-voltage supply and 5V supply respectively. The ground for this configuration is supplied through G1's BNC connector. Similarly, HV transistor #2 may be tested in the same manner using the corresponding connections on the PCB.

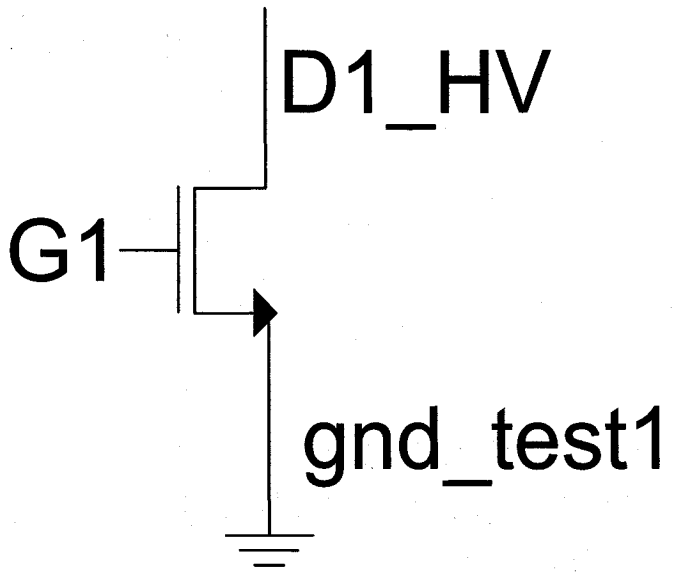

Figure 5.3: HV test transistor

Following this step, a single HVDAC unit must be tested. For this purpose, signals vdd_test1, Iref_test, and VPP_test on the PCB are turned on. The low-voltage supply should be turned on first followed by the high-voltage supply. The latter should be slowly brought up to 300V (i.e. start testing functionality with low voltages and increment). The reference current is approximately 27μA.

The 6 input bits that control the HVDAC come from the NI digital I/O card.The card is used in the pattern generation mode. For this test phase, group C of the cards digital I/O are used to control the HVDAC. DIOC0 corresponds to b1, DIOC1 to b2, DIOC2 to b3, DIOC3 to b4, DIOC4 to b5, DIOC5 to b6, and REQ2 to the clock (clk_test). The output of the DAC is measured off a header pin on the PCB (Vout_test).

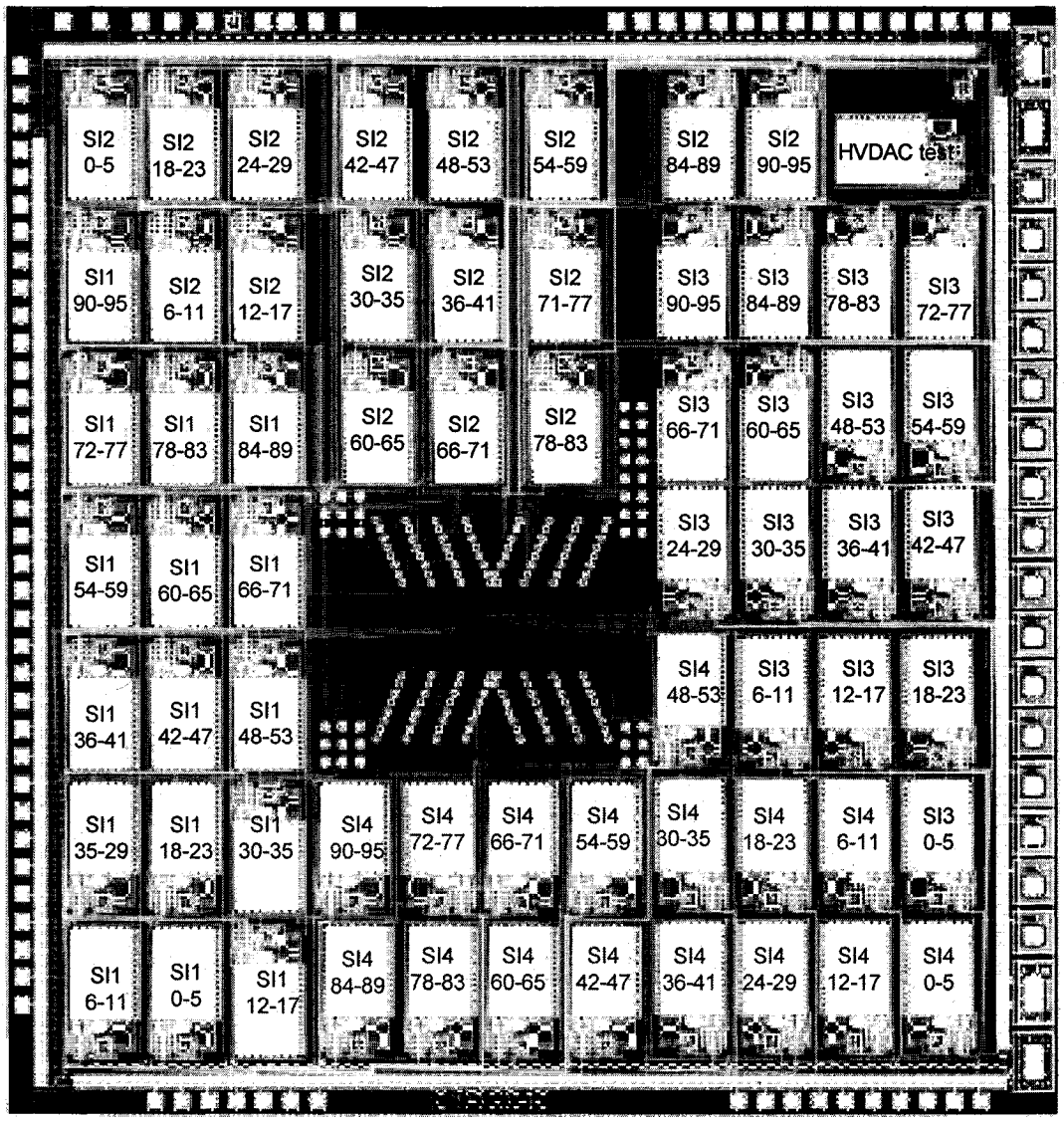

Figure 5.4: Chip showing all HVDACs and their associated scan-in bits

Once the test HVDAC is deemed to work properly, the rest of the chip may be tested. This is a more complex process as programming the proper input code becomes a little complicated. This is because:

- The inputs are divided into 4 sections and scanned-in through 4 scan-in chains, SI1, SI2, SI3, and SI4.

- The HVDAC input bits were ordered as b1,b2,b3,b6,b5,b4 in the layout (instead of b1,b2,b3,b4,b5,b6) to facilitate routing. As a result, the bits scanned in from the input registers must be ordered accordingly.

Figure 5.4 shows all the HVDACs, the scan-in registers that control them, and the corresponding bits from the scan-in registers. For example, in the lower left corner of the above figure, the HVDAC in that location is controlled by bits 6-11 of scan-in register 1. However, as mentioned above, HVDACs are placed in ways to facilitate routing, such that these bits which would normally correspond to bits 1 through 6 respectively on the HVDAC actually correspond to bits 1, 2, 3, 6, 5, 4 respectively. The complete list of correspondence are listed in tables A1.1, A1.2, A1.3 and A1.4. The inputs to the scan-in registers arrive from the NI digital I/O card. The NI outputs correspond to the following HVDAC array inputs:

DIOA0→SI2	DIOA1→SI3	DIOA2→SI4	DIOA3→ SI1
DIOA4→EN	REQ1→clk		

The simulated clock was running at 1.5μs, meaning the EN should be running at 144μs such that all the bits have time be scanned into all HVDACs.

5.2 PACKAGING

The PCB design work involved:

- Creating the parts database list
- Creating a schematic
- Creating the layout/gerber file
- Soldering parts upon receiving the board

In doing all of the above, certain things needed to be kept in mind while designing the printed circuit board, as was the case for the chip layout. As mentioned earlier, optical signals need to pass through the device without any hindrance to the light. This places a few constraints when selecting parts and placing them on-board. For instance, no parts were placed anywhere near the optical path, as may be observed in Figure 5.5. In addition, in selecting a chip carrier, it was important to ensure that the cavity was not too deep, as this could result in clipping of the optical signal if the heterogeneous device was too deep in the carrier. Finally, the parts were well spaced and the signal lines were also provided with ample room to minimize any crosstalk, interference or arcing of high-voltage lines.

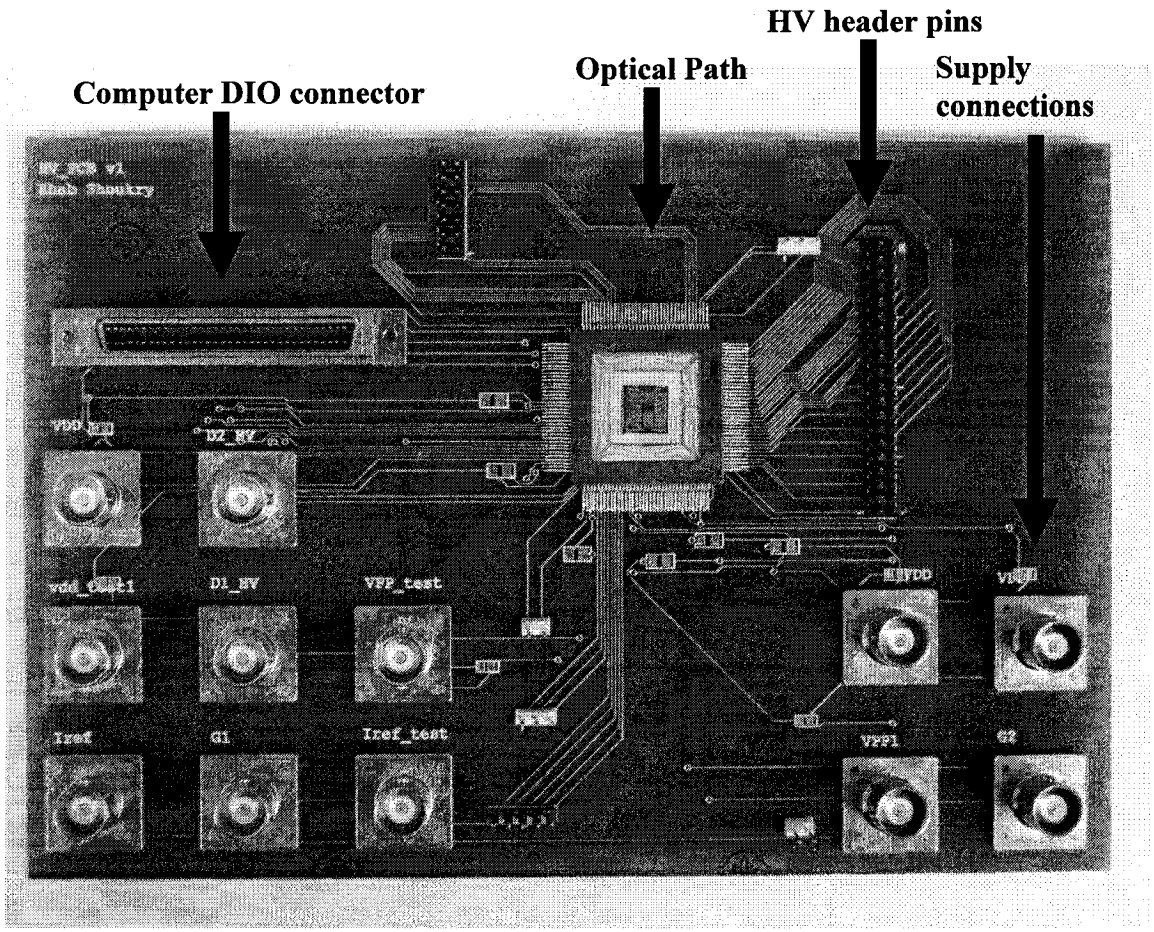

Figure 5.5: PCB with mounted chip

5.3 FLIP-CHIPPING - OVERVIEW

Currently, most integrated circuits use wire-bond pads to provide connectivity to the system. In this scheme, I/O pads are placed on the perimeter of the die. In pad-limited designs, the die area is set by the number of I/O pads on the chip. These pads are large and require large spacing between them, thus creating larger perimeters for chips with more output pads. With the miniaturization of devices and the increasing demand for high-speed technology, wire-bonding solutions become less attractive as they not only occupy space but the inherent parasitics from wire-bonding slow down the device's operation. For instance, a 1mm long bond wire having a diameter of 50μm would have a parasitic inductance of around 1.5nH.

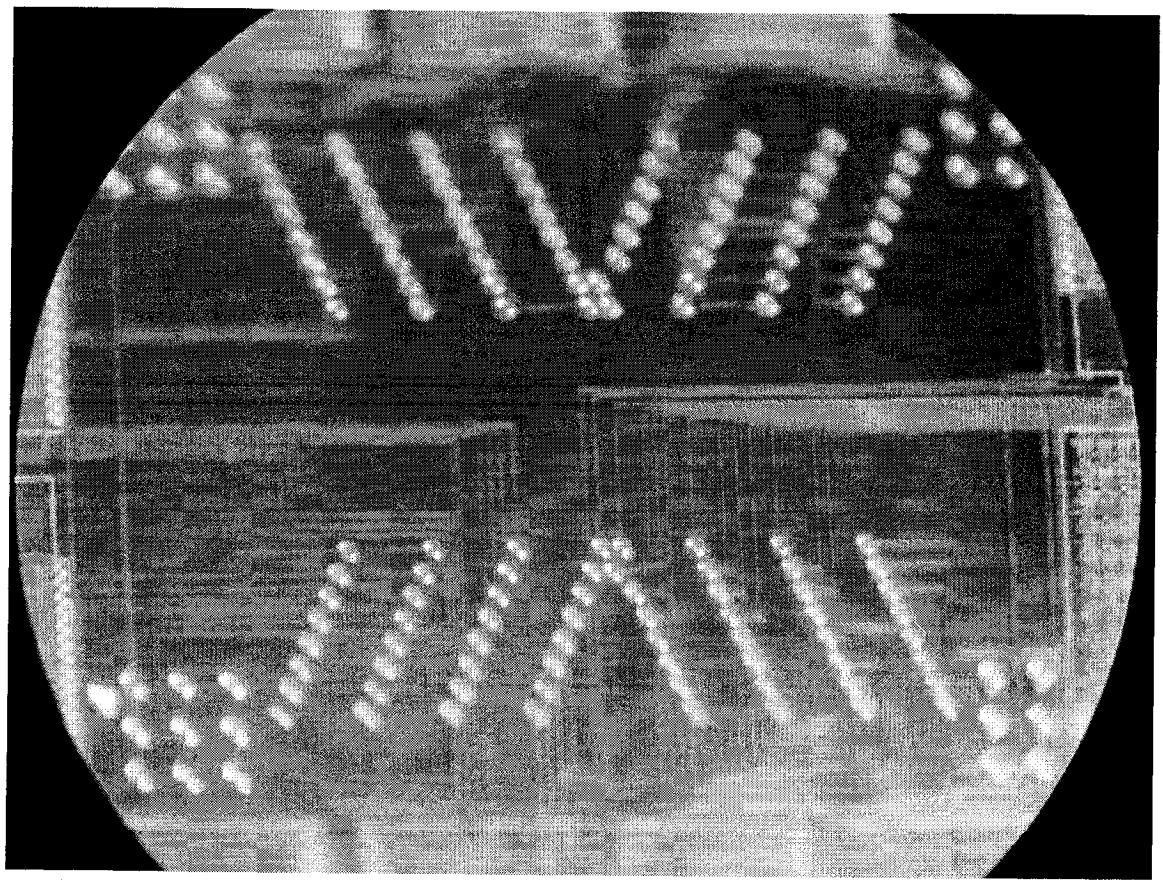

Figure 5.6: Flip-chip pads

With the continued growth in clock frequencies in applications, flip-chip solutions provide an alternative to the perimeter-distributed I/O pads. Flip-chip technology allows integrated circuits to have pads placed throughout the die area, thus increasing the number of total I/O pads that could potentially be placed on a chip without increasing the area requirements. In addition, flip-chipping considerably reduces all the parasitic effects that are caused by wire-bonding, thus improving the high-frequency performance and the bit error rate [2]. The use of this technology can be used to attach 2-D arrays of optical devices to CMOS circuits. In addition to research conducted on short reach optical interconnects, such as board to board and chip to chip connections using flip-chip methods, this technology may be used for integrating VLSI chips with MEMS or electro-optic devices. As was mentioned throughout this thesis, the HVDAC array design will be heterogeneously integrated with the optical phased array, taking advantage of flip-chip technology to provide voltages to 64 independent electrodes. This process will begin once the chip and the optical device are verified to work independently.

5.4 EXPERIMENTAL RESULTS

The testing of the high-voltage chip began as outlined in the test plan. The first die tested had one functional HV test transistor while the other one was non-functional. HV transistor #2 resulted in the following I-V curves. The first curve illustrates the drain current's response to a variation in the drain voltage ranging from 0V to 300V for various gate voltages. When the drain voltage surpasses 100V, the drain current begins to drop. This is not a typical CMOS transistor's behavior, as the current typically rises as a function of the voltage. Interestingly, DALSA's documents only provided I-V curves for drain voltages in the 0V to 100V range. That curve resembles the one shown in figure 5.8. This information was sufficient to conclude that if all HV transistors on-chip behaved as HV test transistor #2, then the chip should not have any problems related to the HV transistors' functionality. However, when time came to test HV test transistor #1, no current flowed. The transistor did not seem to power-up.

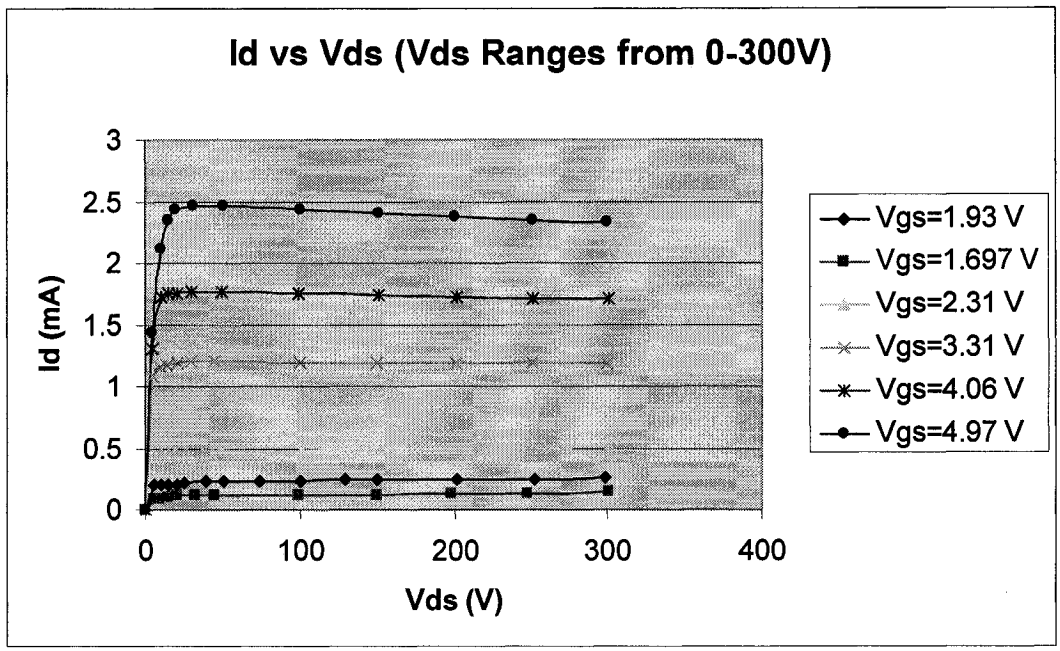

Figure 5.7: I-V curve for drain voltage varying from 0 to 300V

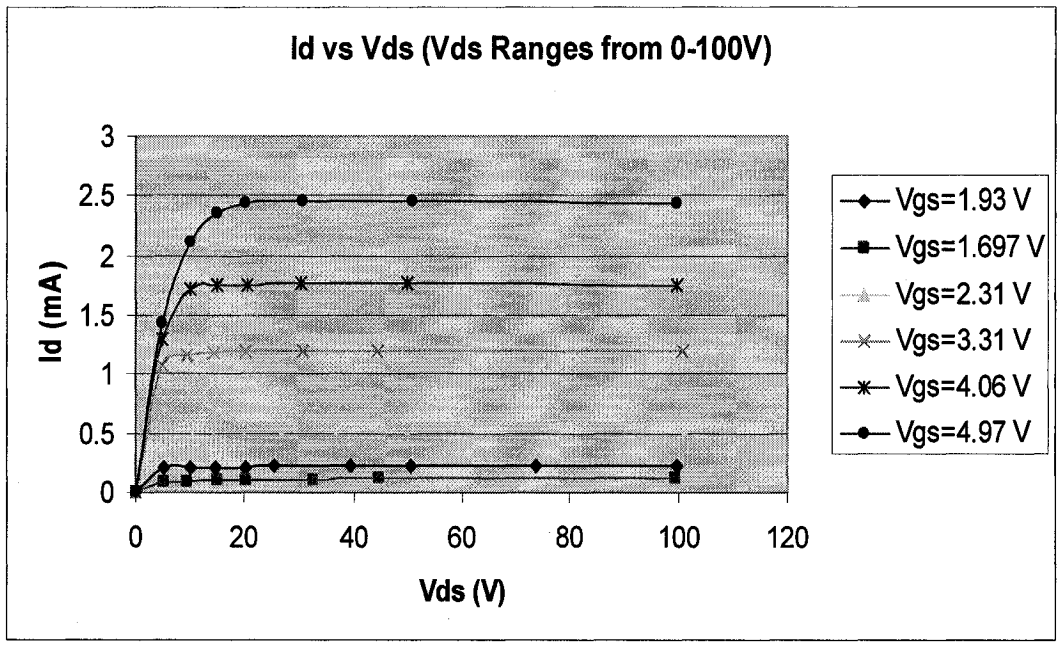

Figure 5.8: I-V curve for drain voltage varying from 0 to 100V

Having tested the 2 test transistors and observed a 50% yield, there was no guarantees as to whether the remainder of the chip would be functional. The following

step, as summarized earlier, is the probing of the row and column decoder outputs on the HVDAC test structure. Oddly, the voltmeter readings for all these outputs were around 4.2V. This was the output no matter what the bit sequence was. The wire-bond pads of each of the inputs were then measured and found to be as expected. These results could not be accounted for, as the probe pads at this stage should simply follow the outputs of a few simple low-voltage NAND-NOR-INV combinations. Having turned off the power supply, the probe at these pads still kept reading 4.2V. At this point, the computer cable was removed and the reading went back to 0V. Following these observations, the remainder of the chip was powered on and testing of the HVDAC array begun. Again, as for the test structure, nothing seemed to function as predicted in the simulations. The probe pads were pulled high and the outputs of the DACs simply followed the high-voltage supply's voltage, indicating that no current flowed through the current mirror. At this point, more dies needed to be packaged and tested to determine the cause of failure. Similar to the first die, the second one showed an I-V curve that mimicked curves in Figures 5.7 and 5.8 for HV transistor #2 but had no response for HV transistor #1. In addition, powering-up the test HVDAC structure yielded no results once again. One thing that was observed for both dies when the computer cable was hooked to the PCB is that the 5V DC supply, when turned off, would read 3.7V.

At first, these behaviors were not fully understood. Possible explanations for the failure of the two dies at that point were: bad yield, damaged dies, or faulty pad structures. After re-verifying the layout of the chip, the only noticeable differences between HV transistor #1 and #2 are:

- a probe pad is attached to transistor #1 and none to #2
- the ground and gate signals of transistor #1 come from DALSA pads whereas those of transistor #2 come from custom-made pads.

To verify whether the DALSA pads had any problems, a 5V supply was connected to the gate of transistor #1 and a voltmeter to the vdd_test pad. The latter would report a voltage drop of 1V from the gate input. For example, setting the gate to 3V would result in a

voltmeter reading of 2V on the vdd_test pad. The DALSA pads where used to provide the low-voltage signals to the chip, as this was recommended by the foundry. After further design reviews and many discussions with engineers from DALSA semiconductors, we noticed that the GND of the HV tx#1 is shorted to the vdd_test pad. Since the source of this HV tx is directly connected to the substrate, setting vdd_test to 5V would inevitably raise the substrate's voltage level. This meant that whatever we did, there would be no way of testing the HV tx#1 and the test HVDAC structure. While this short prevented us from performing tests on the HVDAC_test and HV transistor #1 test structures, the rest of the die remained unaffected because the ground and power signals of the test structure pads were kept completely separate from the ones controlling the remainder of the die.

Following these observations, the remainder of the chip was powered up. On the 23 dies tested, 6 seemed somewhat functional.

As previsouly explained, HVDACs are placed in 4 groups of 16, each receiving their control bits from one of the scan-in chains, SI1, SI2, SI3 or SI4. On all the dies tested, HVDACs controlled by SI1 and SI3 were not properly controllable. In other words, the control bits coming in to an HVDAC from one of these scan chains would not affect it as designed; instead randomly changing the control bits on SI1 or SI3 would result in random voltage levels at the outputs of their corresponding HVDACs. HVDACs controlled by SI2 had a semi-functional behavior in that 5 of the 6 bits going to one of its HVDACs seemed to be fine. That resulted in more control over the voltage levels than the SI1 and SI3 DACs, though results were not repeatable on all functional dies. Finally, the 16 HVDACs controlled by SI4 were fully controllable on all 6 functional dies. The discrepancies between the 4 HVDAC groupings are still being examined. Normally, they should all have the same output, as all HVDACs and scan chains are mirror images or rotated version of each other. For instance, SI2 and SI4 are mirror images and are rotated versions of SI1 and SI3. Thus, apart from their orientation on the die, they are exact replicas of one another.

The following is an analysis of the data collected for Die #11. Out of the four scan chains, only one scan chain (SI4) gives control over its HVDACs. In the 0-100V curves, a couple of curves vary slightly from the norm, as observed in Figure 5.9. Graphically, these curves correspond to HVDACs which are closest to the corner of the die, as illustrated in Figure 5.10. Moreover, as will be pointed out later, these same HVDACs give the smallest minimum voltages with a 300V supply attached.

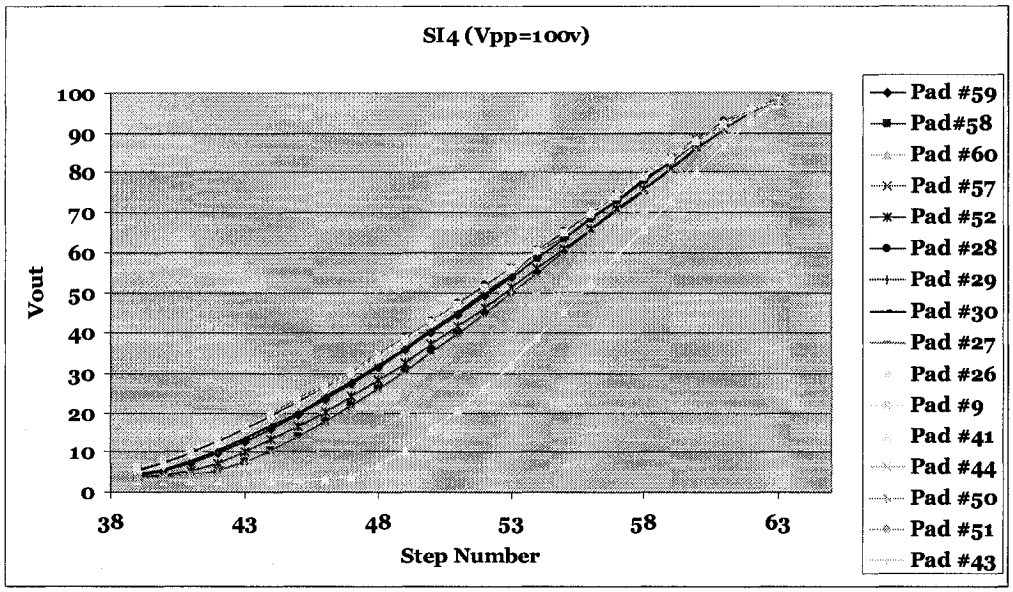

Figure 5.9: Vout vs. Step number for SI4 HVDACs

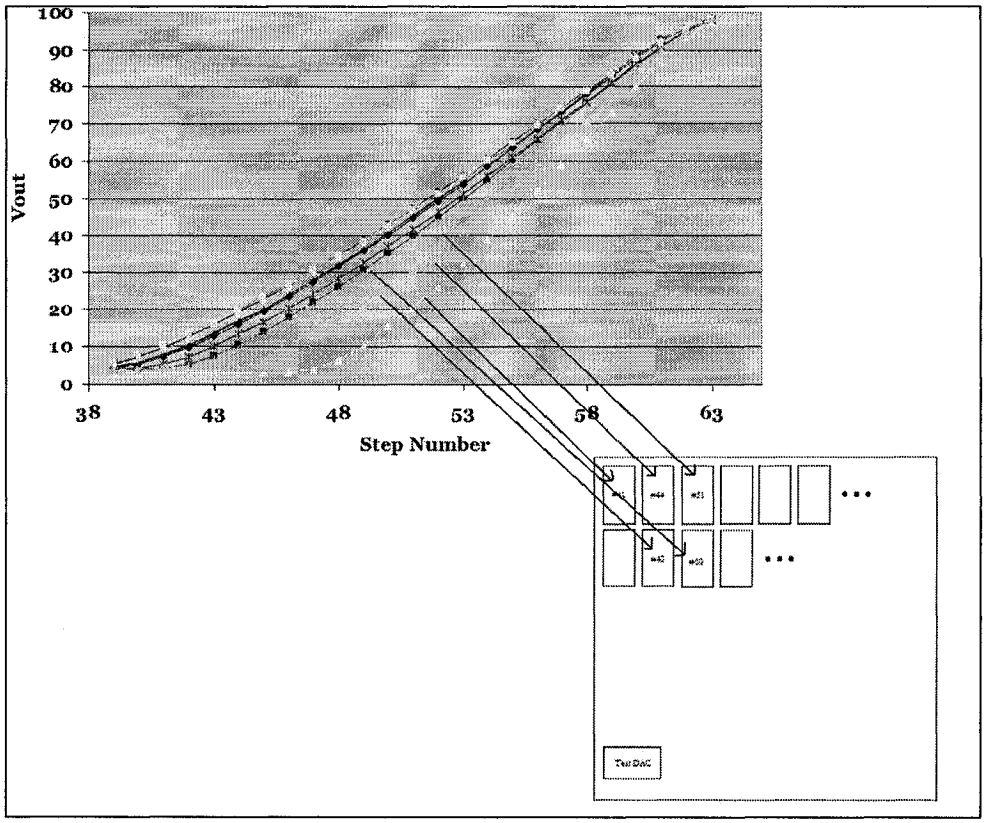

Figure 5.10: Correlation between HVDAC location and output voltage behavior

In the above figures, the curves corresponding to the norm closely match simulation results for the 0V to 100V range. However, when the supply voltage is raised to 300V, the curve tends to deviate from simulation results. The most significant difference is the minimum output voltage. In simulations, the minimum output voltage, when setting the supply to 300V, is 4.7V. However, as observed in Figure 5.11, this value is more than 15 times smaller than the actual experimental data (at Iref = 1.7 mA). Increasing the current Iref from the required 1.7mA to 3.1mA drops the minimum voltage from 78V to 50V, as seen in Figure 5.11.

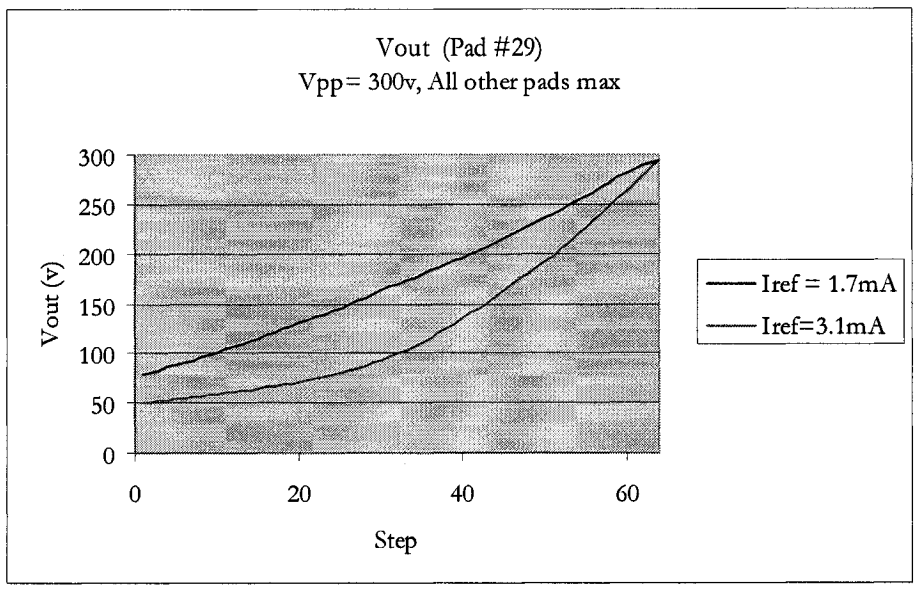

Figure 5.11: Vout vs. Step number for 0V to 300V range

This indicated that the minimum voltage and the reference current had a strong dependency for high voltage supplies. The HVDAC code was then set to draw maximum current for HVDAC #30 while all other DACs drew no current (i.e. HVDAC #30 was set to have minimum voltage level while all others were set to have maximum voltage levels). The reference current was then varied and the minimum voltage level observed. Figure 5.12 illustrates the results of these tests.

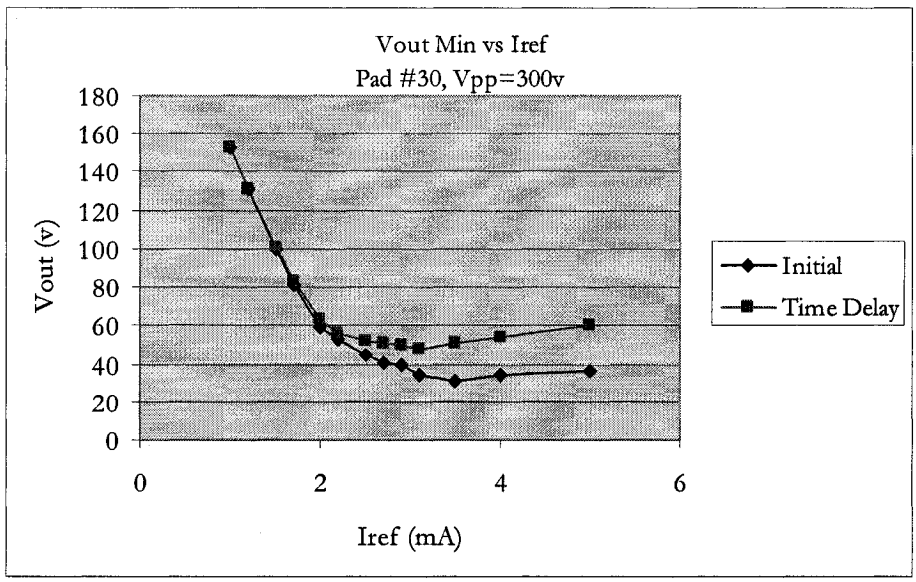

Figure 5.12: Vout min vs. Iref

Figure 5.12 also illustrates the fact that the minimum voltage slowly rises with time. For instance, the initial Vmin for Iref set at 3.1mA is 34V. Leaving these settings for a few minutes results in a Vmin of 50V for the same Iref.

As the HV supply was varied, it was alos observed that the minimum voltage was affected. Figure 5.13 shows this dependency. As one varies the HV supply beyond 250V, the minimum voltage quickly rises above 25V. Thus, a dependency exists between the minimum attainable voltage and HV supply voltage.

As mentioned previously, the minimum output voltages are also related to the location of the HVDACs on the die. Table 5.1 indicates the minimum output voltage for each pad. Figure 5.14 shows the location of pads that deviate from the norm.

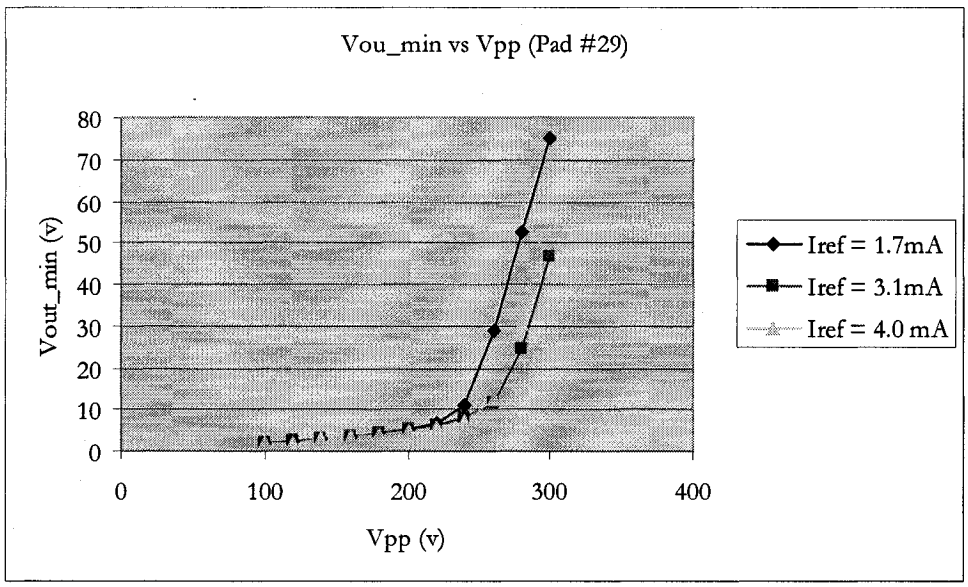

Figure 5.13: Vout min vs. HV supply voltage

Table 5.1: Correlation between minimum output voltage and HVDAC location on die

Vout_min vs Pad # (All other pads 300v, Iref = 3.1mA)	
Pad #	Vout_min
41	40.7
44	43.7
43	44.1
51	44.6
50	47
58	49.1
52	49.1
9	51.3
26	51.8
59	52.5
29	53
30	53.3
60	53.8
28	53.8
27	53.9
57	57.5

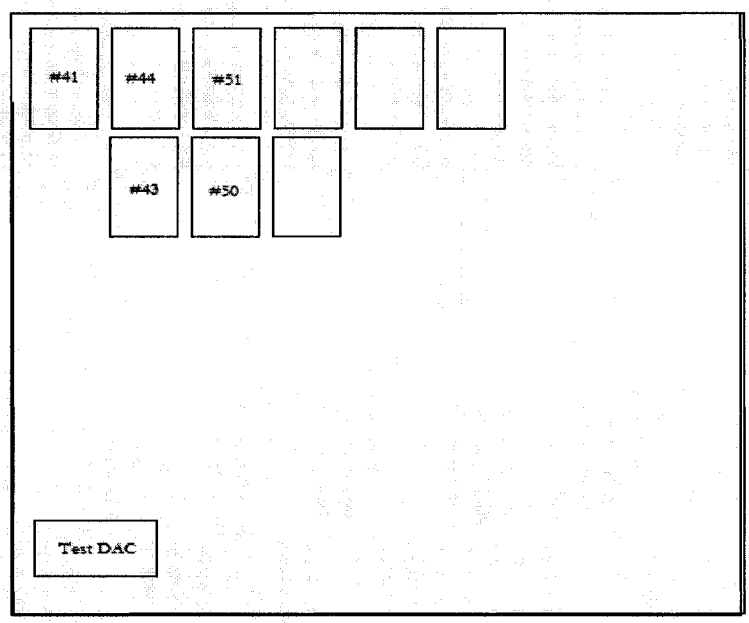

Figure 5.14: Mapping of certain HVDAC locations on die

Crosstalk and interference may also become a concern at high-voltages. In our analysis, very little was observed. For instance, HVDACs #29 and #30 have neighboring output pads. HVDAC #30 was set to 245V while HVDAC #29 was varied. The voltage at

pad 30 dropped by 1V, from 245V to 244V when HVDAC #29 was increased above 230V for the remainder of the test, as seen in Figure 5.15.

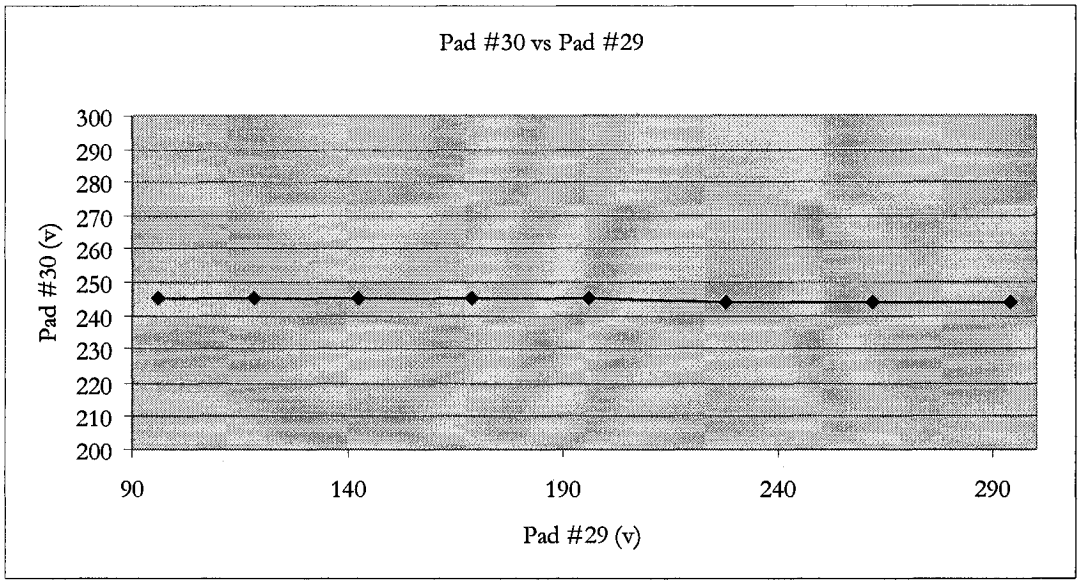

Figure 5.15: Variations in Pad 30 voltage as HVDAC 29 voltage is varied.

Having a high-voltage chip composed of 64 current-steering DACs inevitably results in large amounts of power dissipation and therefore heating of the die. A thermistor was added to monitor the die temperature. With the thermistor attached, all 16 HVDACs controlled by SI4 were set to draw maximum current (i.e. have min. voltages) while all other HVDACs were set to draw no current. The temperature was observed to quickly rise above 100 degrees C, rendering the chip unprogrammable. After letting the die cool for some time, we re-programmed it such that only one HVDAC was at Vmin (~34V with Vpp=300V) and all others at Vmax. This time, the temperature rose to ~47 degrees C, which is not unusually high. Vmin varied in the same direction as temperature, but further tests seem to indicate that the large variation in Vmin is not to be blamed solely on temperature. The impact of actively cooling the die will be further studied experimentally.

Moreover, it was observed that some dies program well (seemingly flawlessly) when Vdd is reduced below 5.0 to, for example, 4.16V for Die #23. To obtain the graphs then, with Vdd at 4.16V, the die was programmed and tested, then Vdd was increased to

5.0V and the die was tested again. Note that testing in this case meant only Vpp was varied, no programming was necessary. Vmin under these conditions behaves in a similar fashion as the simulated HVDAC under the same conditions.

The graphs below show relationships between Isupply (the current provided by the HV supply), Vmin and Vpp. It is interesting to notice that just as Vmin begins to rise almost linearly with Vpp, Isupply stops increasing. For completeness, it should be mentioned that the HV supply was not entering into a current limiting mode.

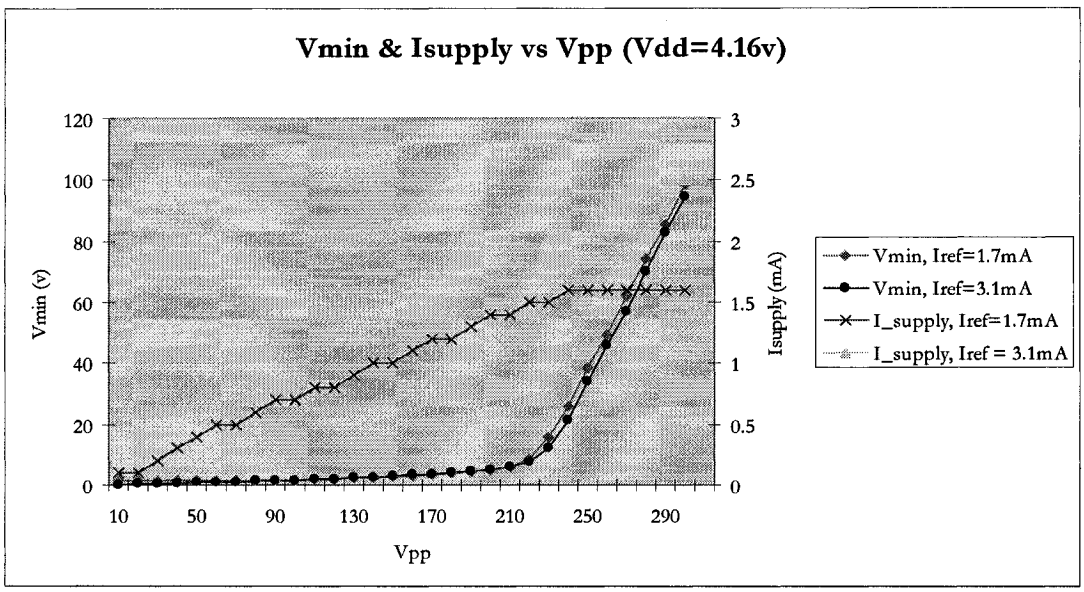

Figure 5.16: Vmin & Isupply vs. HV supply voltage with Vdd=4.16V

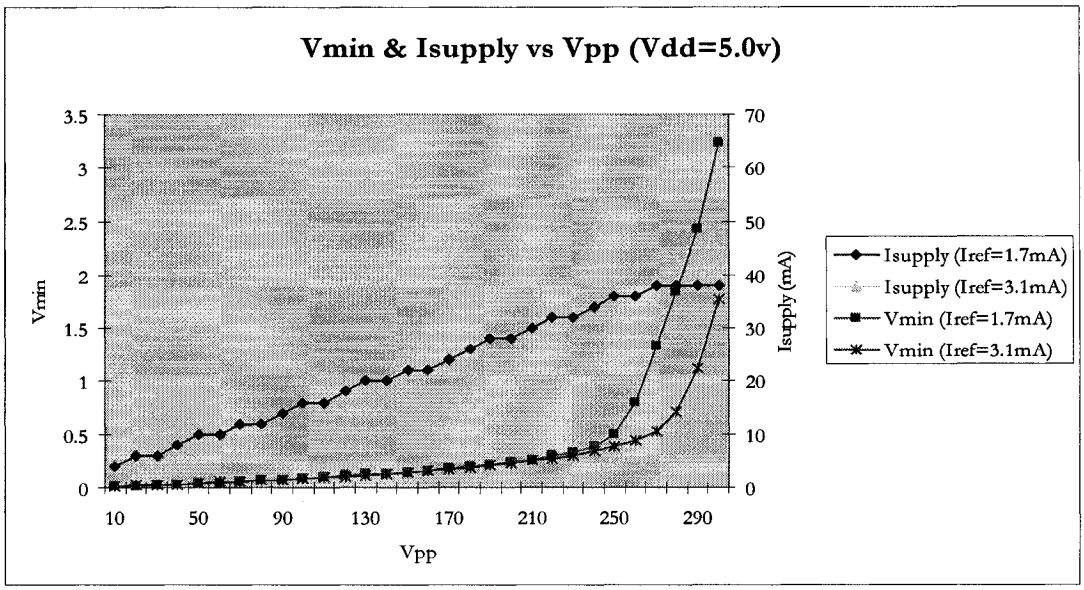

Figure 5.17: Vmin & Isupply vs. HV supply voltage with Vdd=5V

5.5 SUMMARY OF RESULTS

The HV test transistor #2 showed near theoretical curves for the 0V to 100V range, as compared to the DALSA specifications. In addition to not being able to test the test structures (HV tx #1 and HVDAC_test), the HVDACs controlled by SI1, SI2 and SI3 were considered unusable by the electro-optic crystal.

Simulation of the SI4 HVDACs were also very similar to the experimental results for the 0V to100V range. However, as the temperature or high-voltage supply were raised, discrepancies between simulation and test results arose. For instance, the simulated Vmin for an HVDAC attached to a 300V supply was 4.7V, 45V below the actual output. Needless to say, all the input codes generating output voltages between 4.7V and 50V in simulations are not represented in the tested output curve, unless, as mentioned earlier, the 5V supply is reduced to 4.16V, the chip is programmed, and the supply is raised back to 5V.

In addition, simulations of the HVDAC showed that temperature played a small role on the output voltages. Moreover, as was observed experimentally, the HVDACs may fail to program once the temperature becomes too elevated.

Thus, it was found that a link existed between the minimum output voltage and the die temperature, the high-voltage supply voltage, the HVDAC location on the die, the reference current and the low voltage supply.

5.6 REFERENCES

[1]DALSA Semiconductor, "Component Datasheets for the high-voltage CMOS/DMOS process," CDS0077.2, p.39, August 2004.

[2] A. V. Krishnamoorthy and K. W. Goossen, "Optoelectronic-VLSI: Phot onics integrated with VLSI circuits," *IEEE Journal of selected topics in Quantum Electronics*, Vol.4, pp. 899-910, November/December 1998.

CHAPTER 6 CONCLUSION AND FUTURE WORK

6.1 CONCLUSION

Optical switches have the potential of increasing bandwidth and bringing the photonic edge closer to the end-user. Integration of high voltage, digital and analog circuitry on a same die will result in many technological improvements.

This thesis presented the design of a fully integrated array of high-voltage digital-to-analog converters. Two designs were presented and simulation results were compared. The high-compliance current-mirror design showed good linearity though the speed was slightly slower than the simple current-mirror approach. The latter was less linear, though for the application at hand, linearity was not as important as having a set of attainable voltages. Based on these distinguishable voltages that were obtained through simulations, the optical design was modified to accommodate for the DAC's performance. The simulation speed of the design that was fabricated is 1.3μs, slightly slower than the target speed of an Agile All-Photonic Network. Experimental results proved to differ from simulation results for high voltage supplies above 250V. At that point, the minimum output voltage rises to 50V and more, rendering the device unusable in photonic switching. Fortunately, a technique in which the low-voltage supply is reduced prior to programming the chip proved to give good voltage levels for all HV supply ranges. Due to fabrication delays, not all dies were tested and further investigation on the behavior of the chip is ongoing.

6.2 FUTURE WORK

More discussions with DALSA engineers on the behavior of the scan chains and HVDACs based on their orientation or location on the die need to be conducted. In addition, the impact of actively cooling the die will need to be tested. Moreoever, simulations on the optical designs performance based on the experimental results obtained need to be performed. This will verify whether or not the optical efficiency of the ROPA design will be acceptable based on the programmable voltages and the reduced number of usable HVDACs. Subsequent to these simulations, the die will be sent for heterogeneous integration with the optical-phased array. The flip-chipped device will then be tested for proper flip-chip connections through header pins on the PCB (which are connected to the 2^{nd} flip-chip pad provided for connectivity testing). The device will then be tested for optical performance, resulting in a very fast, high port count optical switch.

APPENDIX

The following tables list the order of the scan-in bits for each DAC in the array.

Table A1.1 : Scan-in chain 1 and corresponding bit sequence

SI_1	b_1	b_2	b_3	b_4	b_5	b_6
0-5	1	2	3	6	5	4
6-11	1	2	3	6	5	4
12-17	4	5	6	3	2	1
18-23	1	2	3	6	5	4
24-29	1	2	3	6	5	4
30-35	4	5	6	3	2	1
36-41	4	5	6	3	2	1
42-47	4	5	6	3	2	1
48-53	4	5	6	3	2	1
54-59	4	5	6	3	2	1
60-65	4	5	6	3	2	1
66-71	4	5	6	3	2	1
72-77	4	5	6	3	2	1
78-83	4	5	6	3	2	1
84-89	4	5	6	3	2	1
90-95	4	5	6	3	2	1

Table A1.2: Scan-in chain 2 and corresponding bit sequence

SI_2	b_1	b_2	b_3	b_4	b_5	b_6
0-5	4	5	6	3	2	1
6-11	4	5	6	3	2	1
12-17	4	5	6	3	2	1
18-23	4	5	6	3	2	1
24-29	4	5	6	3	2	1
30-35	4	5	6	3	2	1
36-41	4	5	6	3	2	1
42-47	4	5	6	3	2	1
48-53	4	5	6	3	2	1
54-59	4	5	6	3	2	1
60-65	4	5	6	3	2	1
66-71	4	5	6	3	2	1
72-77	4	5	6	3	2	1
78-83	4	5	6	3	2	1
84-89	1	2	3	6	5	4
90-95	1	2	3	6	5	4

Table A1.3: Scan-in chain 3 and corresponding bit sequence

SI_3	b_1	b_2	b_3	b_4	b_5	b_6
5-0	4	5	6	3	2	1
11-6	4	5	6	3	2	1
17-12	4	5	6	3	2	1
23-18	4	5	6	3	2	1
29-24	4	5	6	3	2	1
35-30	4	5	6	3	2	1

41-36	4	5	6	3	2	1
47-42	4	5	6	3	2	1
53-48	4	5	6	3	2	1
59-54	4	5	6	3	2	1
65-60	4	5	6	3	2	1
71-66	4	5	6	3	2	1
77-72	4	5	6	3	2	1
83-78	4	5	6	3	2	1
89-84	1	2	3	6	5	4
95-90	1	2	3	6	5	4

Table A1.4: Scan-in chain 4 and corresponding bit sequence

SI_4	b_1	b_2	b_3	b_4	b_5	b_6
0-5	4	5	6	3	2	1
6-11	4	5	6	3	2	1
12-17	4	5	6	3	2	1
18-23	4	5	6	3	2	1
24-29	4	5	6	3	2	1
30-35	4	5	6	3	2	1
36-41	4	5	6	3	2	1
42-47	1	2	3	6	5	4
48-53	1	2	3	6	5	4
54-59	1	2	3	6	5	4
60-65	1	2	3	6	5	4
66-71	1	2	3	6	5	4
72-77	4	5	6	3	2	1
78-83	1	2	3	6	5	4

84-89	1	2	3	6	5	4
90-95	1	2	3	6	5	4